IPS2550

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1. Introduction

The IPS2550 is a high-speed inductive position sensor with analog sine and cosine voltage output, which can be differential or single-ended. The analog high-speed sensor is optimized for lowest propagation delay.

The IPS2550 high-speed inductive position sensor is used in automotive, industrial, medical, and consumer applications. The sensor configuration can be changed to address a wide range of applications. This document describes digital communication with the IPS2550 and the available configuration options.

The digital communication interface of the IPS2550 uses I2C Standard-mode to program, configure and to read the diagnostic status. In addition to using the dedicated SDA and SCL pins, it is also possible to communicate via I2C protocol over the analog output pins to reduce the number of wires to a sensor module. The Slave Address is programmable in the register and can be modified by applying the correct voltage at ADR_IRQN pin1, for details see section 2.3.
Note: It is highly recommended to read the *IPS2550 Datasheet* for electrical characteristics, product details, such as features, pin descriptions, functionality, and circuit descriptions before reading this manual.

1.1 Quick-Start / Default Configuration

The IPS2550 comes with a default configuration for the transmitter bias current, automatic gain control and output pins in differential sine and cosine voltage mode. Diagnostic alarm at the output pins is not active. The sensor outputs sine and cosine voltages relative to the target position after power-up without the need for programming in case the sensor coils are designed appropriately to work with the default configuration.

Default Configuration: (refer to section 3.1 for details)

Supply Mode:	5V
Output Mode:	SIN/COS differential
AGC Mode:	ON (gain booster off)
Interrupt Signaling:	Off
I2C ADR/IRQN Pin:	I2C address pin
I2C Address:	24dec (ADR pin high), 17dec (ADR pin low)
I2C Integrity check:	ON
RX configuration:	INTERLEAVED - IPS2550
TX bias current:	496µA

1.2 Programming Procedure

The programming parameters depend on the application requirements. Most parameters do not change for production parts. Some parameters can be programmed individually to compensate production tolerances. A programming procedure usually includes following steps:

1. **General Configuration** (Select the correct supply voltage, Interface mode, etc. mainly in system configuration registers Adr 0x00, 0x01, …)
2. **Transmitter Configuration** (TX Bias Current Setting, Adr 0x07)
3. **Receiver Configuration** (can be programmed individually if needed)
   a. Static Gain Adjustment if AGC is switched off (Adr 0x02)
   b. Signal Offset Compensation (Adr 0x04, 0x06)
   c. Amplitude Mismatch Compensation (Adr 0x03, 0x05)

4. **Diagnostics Configuration** (Diagnostic Mask, Alarm Levels, Adr 0x0B, 0x0C, 0x0D, 0x0F, 0x08, 0x09, 0x0A)

   Notes:

   - To avoid possible error signalling during a configuration procedure, it is recommended to enable the backend interrupt signalling (by System Configuration 1: Address 0x00 FTP; 0x40 SRB, back_end_irqn_ena) and the interrupt mask (in Interrupt Enable 1: Address 0x0B FTP; 0x4B SRB, Interrupt Enable 2: Address 0x0C FTP; 0x4C SRB and Interrupt Enable 3: Address 0x0D FTP; 0x4D SRB) at the end of the programming procedure.
   - It is recommended to disable the AGC and configure a fixed gain during configuration of offset compensation and gain mismatch registers to avoid distortion of measurements during a compensation procedure (R1 Fine Gain Compensation: Address 0x03 FTP; 0x43 SRB, R1 Offset Compensation: Address 0x04 FTP; 0x44 SRB, R2 Fine Gain Compensation: Address 0x05 FTP; 0x45 SRB, R2 Offset Compensation: Address 0x06 FTP; 0x46 SRB).

1.3 IPS2550 Block Diagram

Figure 1 shows the main components of the IPS2550.

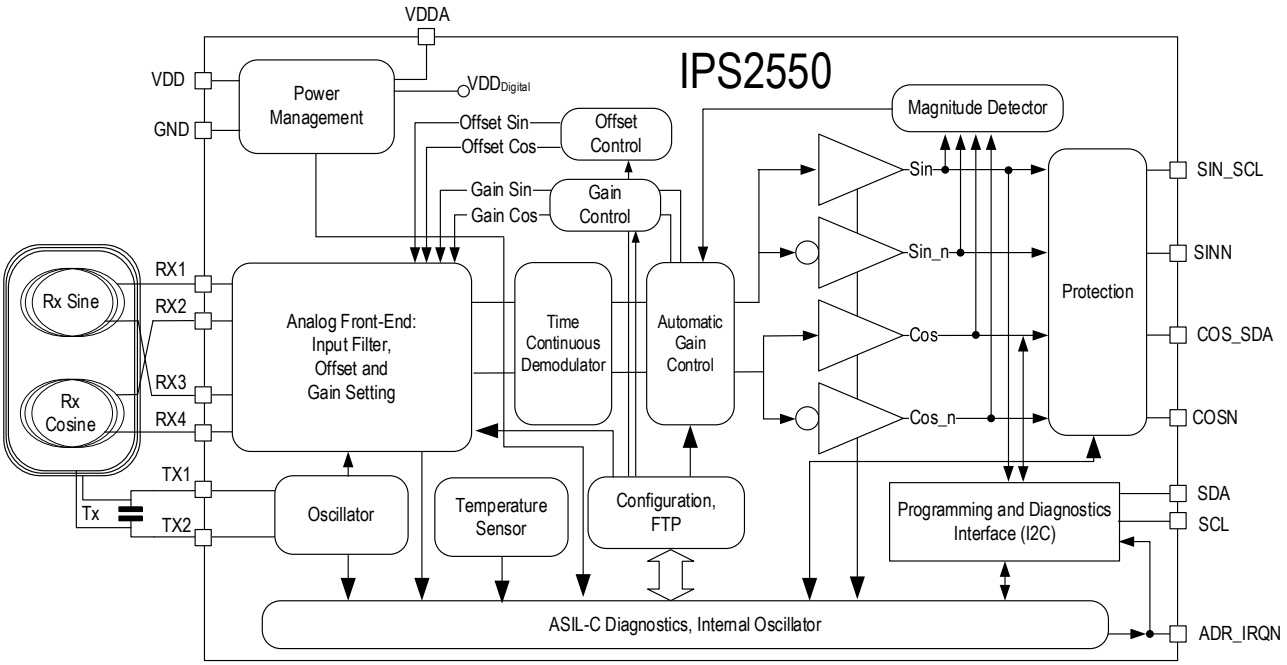

Figure 1. Block Diagram

1.4 Programming Modes

There are two different programming modes available:

- Programming over I2C pins: used for embedded applications with I2C pins permanently connected to the sensor IC.
- Programming over output pins (slower): used for remote applications like a sensor module where only supply and output pins are available.

1.4.1. Programming Over I2C Pins

The IPS2550 can be programmed with a clock frequency of up to 100kHz over the I2C interface pins SDA (pin16) and SCL (pin15). The I2C pins must be tied to VDD using two pull-ups as shown below. Communication over the I2C pins is available during operation and allows reading the diagnostic status while the differential sine cosine output is active.

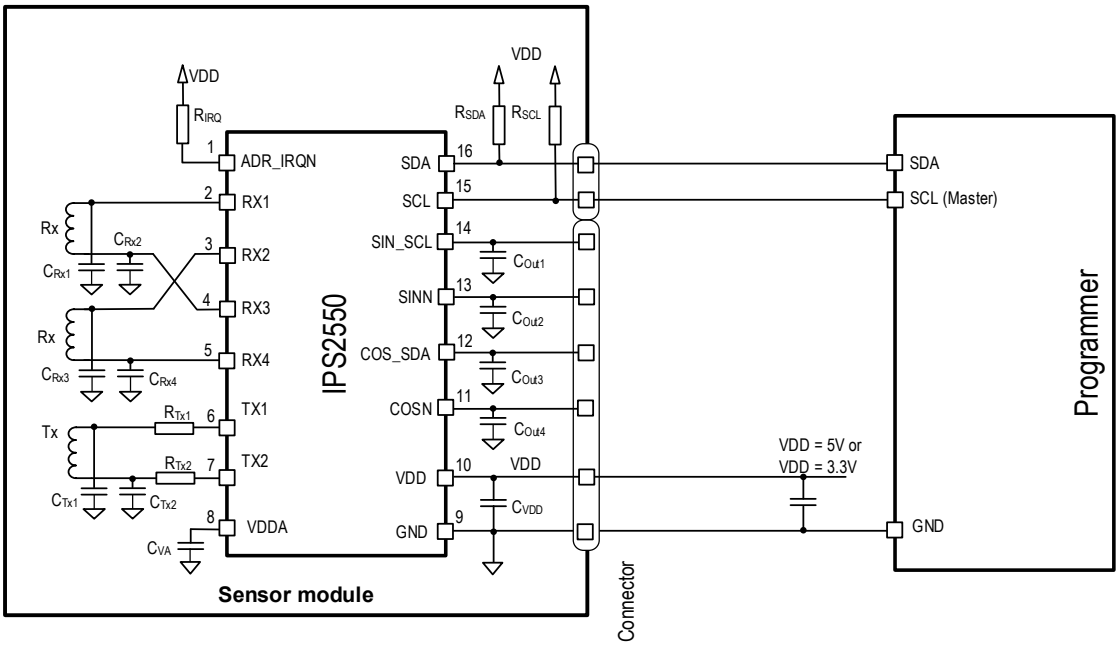

Figure 2. Programming the IPS2550 Over the I2C Interface

1.4.2. Programming Over Output Pins

The IPS2550 can be programmed with a clock frequency of up to 25kHz over the output pins COS_SDA (pin12) and SIN_SCL (pin14). The I2C pins must be tied to VDD using two pull-ups as shown in Figure 3.

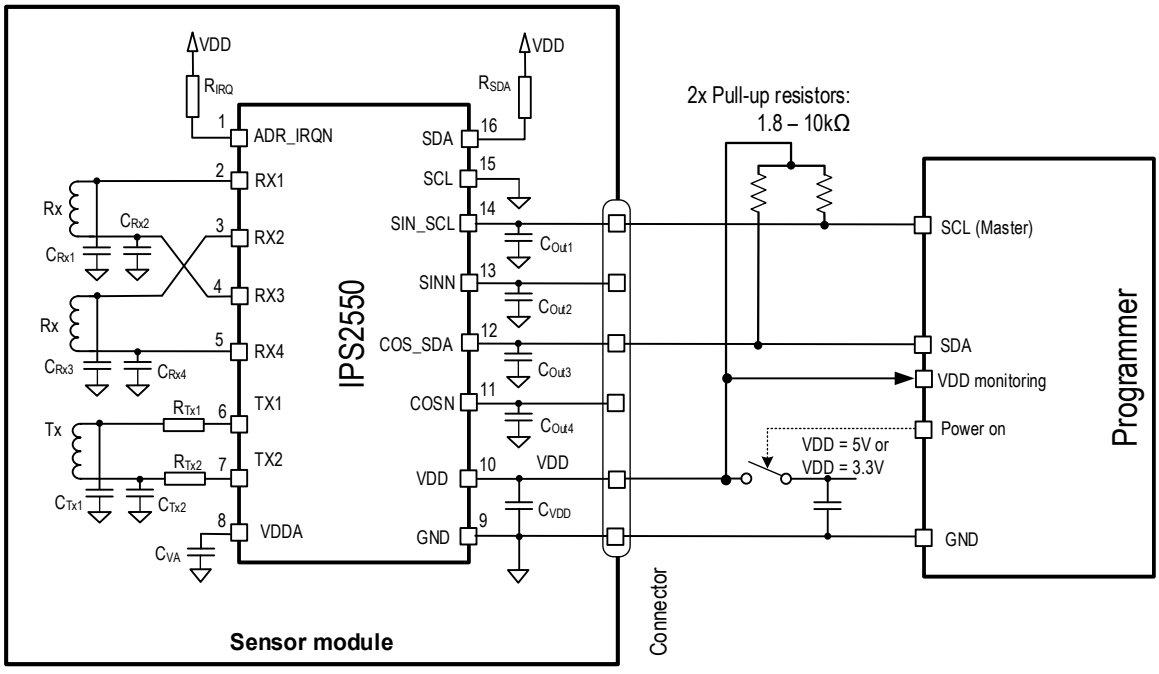

Figure 3. Programming the IPS2550 Over the Output Pins

Programming over the output pins can be enabled only by sending an unlock command within a defined timeframe during the start-up procedure. In operation mode SinP/CosP are solely analog outputs used for either mission mode data, or diagnostics. The procedure to enter and exit the Programming mode is shown below.

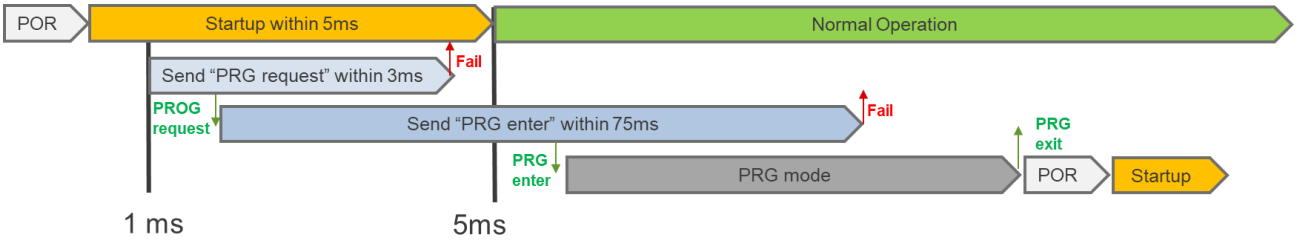

Figure 4. Enter Programming Mode Over Output Pins

To enter the Programming mode, the programming request must be sent: the master must send the Slave Address byte with R/W bit set to ‘0’ in the 1ms to 3ms time frame after the power-on-reset. If NACK is received, first step of the programming entry is not successful.

Once the programming request is received, the IPS2550 does not start in Normal Operation mode, but a programming window is enabled for 75ms.

During the programming window, a password command must be sent consisting of Slave Address, Memory Address and password code as shown in Figure 5. If the valid password command is received, the programming window counter is stopped and the IPS2550 enters the Programming mode. If no valid password command is received, the IPS2550 enters the Normal Operation mode after the programming window counter is finished after 75ms.

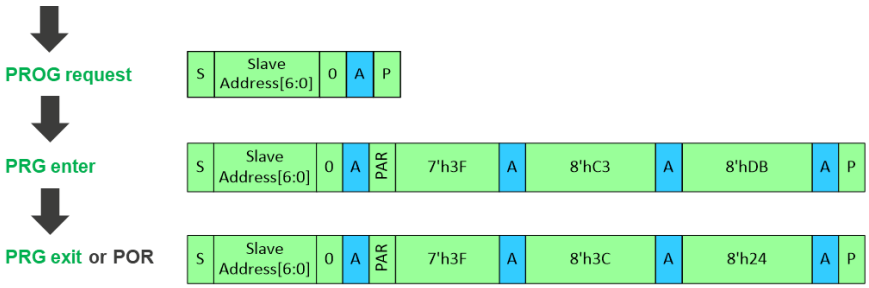

Figure 5. Enter Programming Commands

After successful configuration and programming, exit the Programming mode by sending the exit command.

Notes:

- During programming mode via the analog output pins, the analog output voltage can be read from SIN_N and COS_N pins only for sensor configuration.
- When entering the programming mode via the analog output pins, the i2c_protocol_fail flag in register Interrupt State 1: Address 0x6B SFR is set. Reset the error flag during the progamming procedure if needed.

  If IPS2550 is programmed via the analog output pins, the outbuf_vcm_fail flag in register Interrupt State 2: Address 0x6C SFR is set.

1.4.3. Programming Over Output Pins Using the IPS-Comboard

When using the IPS-comboard to program an IPS2550 over the analog output pins, consider the following:

- Select 4kHz I2C clock (automatically selected by GUI)
- Filtering capacitors must be max 47nF or lower
- For further details please refer to the User Manual of the IPS2550 Starter Kit

1.5 Automatic Gain Control (AGC)

As default, the automatic gain control is active. The AGC uses the signal of an internal magnitude detector to control the signal amplitudes into a control window as defined in the *IPS2550 Datasheet* document.

The AGC uses all available gain steps per default. If agc_plause_chk_en is activated (0x02, bit10), the AGC uses only gain steps inside the plausibility range defined in the AGC Plausibility register (Address 0x0F FTP; 0x4F SRB). If the AGC plausibility check is enabled, the agc_err bit is set when the plausibility boundary code configured in the AGC Plausibility Configuration register (agc_plause_uthresh, agc_plause_lthresh) is reached.

Note: The upper plausibility threshold must be higher than the lower plausibility threshold.

It is possible to double the overall gain by using d2a_afe_boost_sel (0x02, bit07).

Some applications may require a static gain setting. In this case, the AGC must be disabled (0x00, bit9 afe_agc_dis) and the R1/R2 gain register must be configured for the desired gain.

To see if the AGC is in range, check the agc_err bit (0x6C, bit 1).

By using bits agc_wait_tmr_sel (0x02, bits [9:8]), the wait time after a direction change of the magnitude can be configured as shown in Figure 6. The default is 10µs.

After power-up, the AGC starts to work from the gain value that is configured for R1/R2.

Note: The agc_err bit is set during start-up if an AGC start value is programmed and the magnitude exceeds the AGC target range until the correct gain value is reached. To avoid such situation during start-up, set the R1/R2 gain to a low value or '0' when using the AGC.

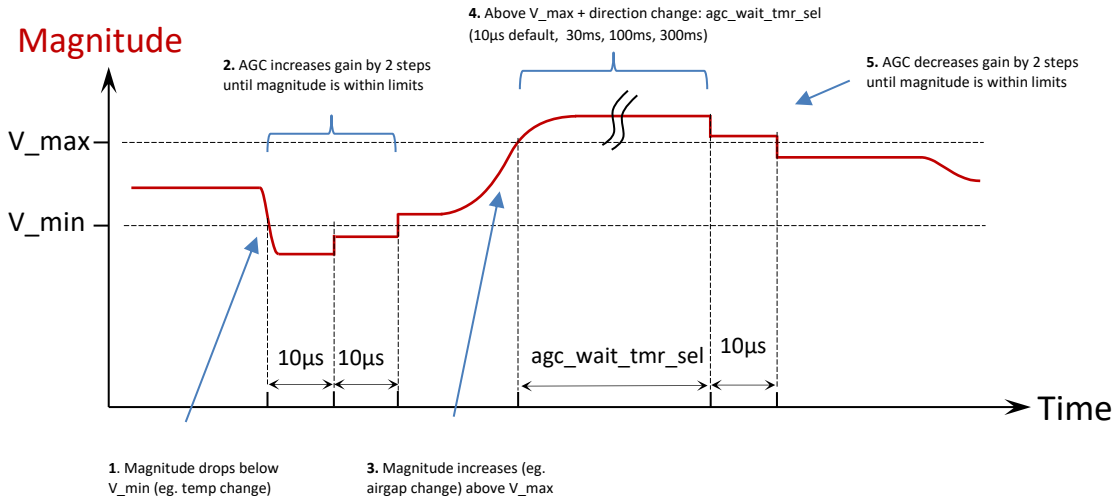

Figure 6. AGC Effect on Change in Magnitude

For lab evaluation purpose the actual AGC value can be read from the agc_gain_stage (0x78, bits[6:0]) register.

The target amplitude is 0.9V ± 0.2V (default).
Note: The default typical peak amplitude on an output pin is 0.9V, and 1.8V peak-peak if the sensor is operated within AGC range. The differential typical output voltage between positive and negative output pin is 3.6V.

2. I2C Interface

To communicate with a microcontroller, the IPS2550 uses a two-wire Inter-Integrated Circuit (I2C) interface based on the specification rev. 6. The Slave Address is programmable and pin 1 can be configured as an address or interrupt pin.

2.1 Supported Features

- Standard-mode (Sm) up to 100 kbit/s
  - Start condition
  - Stop condition
  - Acknowledge
  - 7-bit Slave Address
- Single Write Operation
- Single Read Operation

2.2 Not Supported Optional Features

The following features are not supported:

- Clock stretching
- 10-bit Slave Address
- General Call Address
- Software Reset
- Device ID

Two wires connected to the serial data pin (SIO_SDA, pin 16) and serial clock pin (SCK_SCL, pin 15) carry information between the devices connected to the bus. Both SDA and SCL pins are connected to VDD via external pull-up resistors. When the bus is free, both lines are high. An external master (host controller) initiates a transfer, generates clock signals, and terminates a transfer.

The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low.

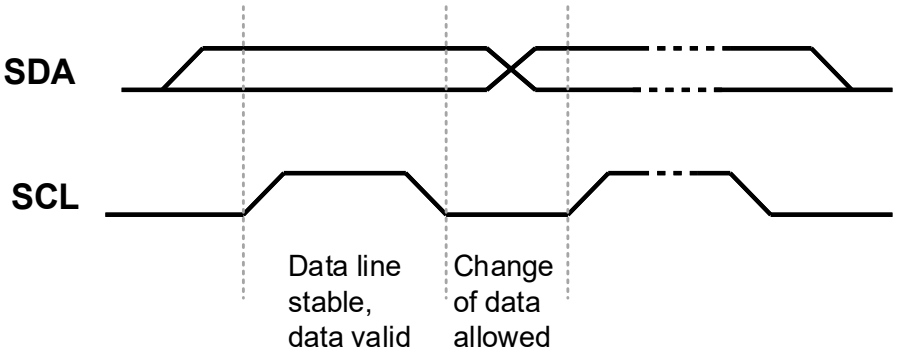

Figure 7. I2C Bit Transfer Signal State

A data transfer is initiated by a START condition (S) and is defined as a high to low transition on the SDA line while SCL is high. A STOP condition (P) is defined as a low to high transition on the SDA line while SCL is high as shown in Figure 8.

The master always generates START and STOP conditions. The bus is considered busy after the START condition. The bus is considered to be free again after the STOP condition.

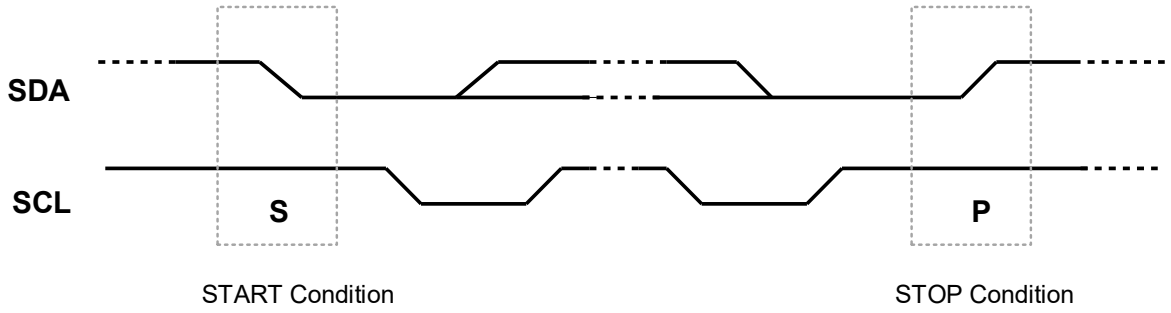

Figure 8. I2C START and STOP Conditions

If a repeated START (Sr) is generated instead of a STOP condition, the bus stays busy. In this respect, the START and repeated START conditions are functionally identical.

Every transfer block on the SDA line must have a length of 1 byte (8 bits). The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an acknowledge bit from the I2C master (see Figure 9). Data is transferred with the most significant bit (MSB) first. Data transfer with acknowledgement is mandatory.

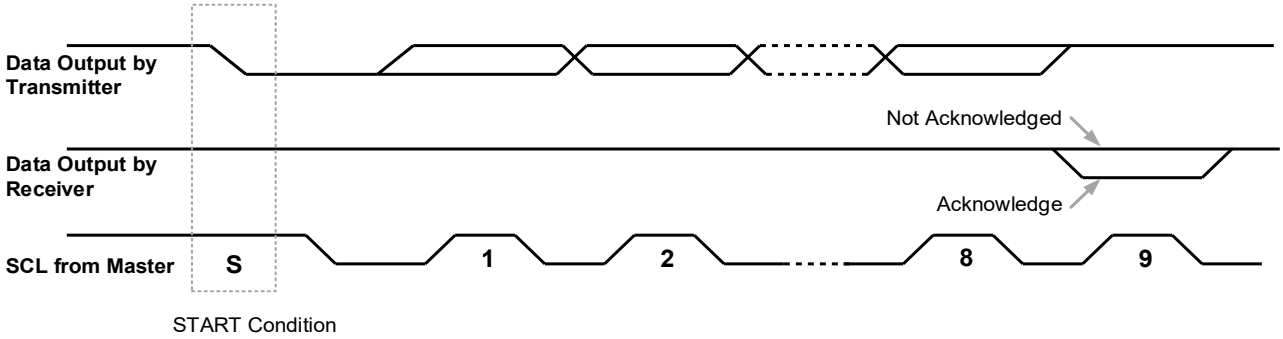

Figure 9. I2C Acknowledge Signal State

2.3 Slave Address

The IPS2550 supports a 7-bit I2C Slave Address. The Slave Address format is shown in Figure 10.

The Slave Address can be configured by four programmable bits (A6, A5, A4, A3). These bits can be modified in System Configuration 1 register (0x00, bits [7:4] i2c_slave_sub_addr). Slave address bits A2, A1, A0 are reserved bits and are set to ‘0’ if pin1 is configured as interrupt pin.

If pin1 is configured as address pin (default, System Configuration 1 (0x00, bit [0]=0b1 system_protocol)), A3 has the state of the address pin and A0 has the inverse state of the address pin.

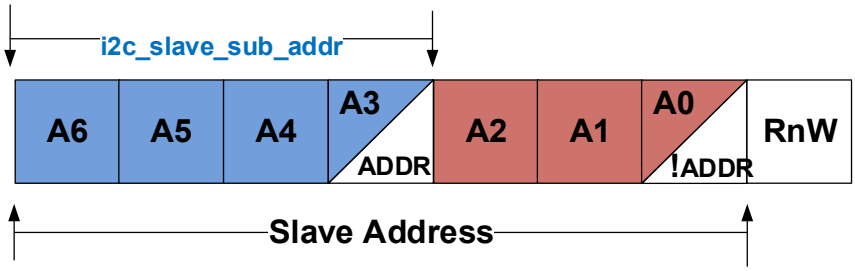

Figure 10. I2C Device Address

Up to 21 devices can be connected to the same bus when using the address pin, and up 14 devices when using different address pins. Two groups of reserved addresses (0000XXX and 1111XXX) are excluded. A list of configurable slave addresses is shown in Table 1.

Table 1. Programmable I2C Slave Addresses with ADR_IRQN PIN 1 configured for Interrupt Output (0x00, system_protocol='0')

i2c_slave_sub_addr dec	1	2	3	4	5	6	7
[A6:A0] bin	0001000	0010000	0011000	0100000	0101000	0110000	0111000
slave adr dec	8	16	24	32	40	48	56
slave adr hex	8	10	18	20	28	30	38
i2c_slave_sub_addr dec	8	9	10	11	12	13	14
[A6:A0] bin	1000000	1001000	1010000	1011000	1100000	1101000	1110000
slave adr dec	64	72	80	88	96	104	112
slave adr hex	40	48	50	58	60	68	70

Table 2. Programmable I2C Slave Addresses with ADR_IRQN Pin 1 configured for Adress Input (0x00, system_protocol='1')

		Default	**Default**				
i2c_slave_sub_addr dec	0, 1	2, 3	2, 3	4, 5	4, 5	6, 7	6, 7
[A6:A0] bin	0001000	0010001	0011000	0100001	0101000	0110001	0111000
slave adr dec	8	**17**	**24**	33	40	49	56
slave adr hex	8	**11**	**18**	21	28	31	38
ADR Pin	High	**ADR = "LOW"**	**ADR = "HIGH"**	Low	High	Low	High
i2c_slave_sub_addr dec	8, 9	8, 9	10, 11	10, 11	12, 13	12, 13	14, 15
[A6:A0] bin	1000001	1001000	1010001	1011000	1100001	1101000	1110001
slave adr dec	65	72	81	88	97	104	113
slave adr hex	41	48	51	58	61	68	71
ADR Pin	Low	High	Low	High	Low	High	Low

2.4 Operation and Frame Format

The IPS2550 supports both read and write operation. By default, the protocol integrity check is enabled for all I2C frames and can be deactivated in System Configuration 2 register (0x01, bit [2] prot_integ_check_dis).

2.5 Memory Address

The first data byte after the Slave Address is defined as memory address <MemAddr> and consists of:

- D7 Slave Address Parity Bit
- D6….D0 6-bit memory address

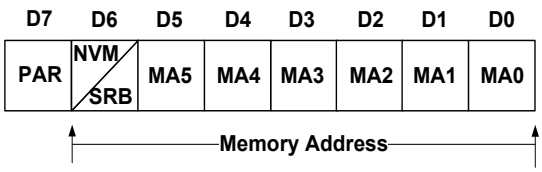

Figure 11. Memory Address Byte

2.6 Content Data Bytes

The following consecutive pairs of data bytes (<CmdData> field) contain the 11-bit information for the memory. The remaining 5-bits are reserved and fixed to '1'. The sequence is MSB first.

Data Byte N:

- D7 ….D0 <ContentData[10:3]>

Data Byte N+1:

- D7 ….D5 <ContentData[2:0]>
- D4 ….D3 <Reserved, always 2'b11>
- D2 ….D0 <Reserved>:
  - Integrity check 'On': CRC[2:0] over Memory Address and Content Data
  - Integrity check 'Off': <Reserved> (Always all 1's)
    The <Reserved> field is checked for all 1's and if the check fails the <ContentData> field is not written to the addressed memory space (no write action) and the slave receiver does not produce an acknowledge.

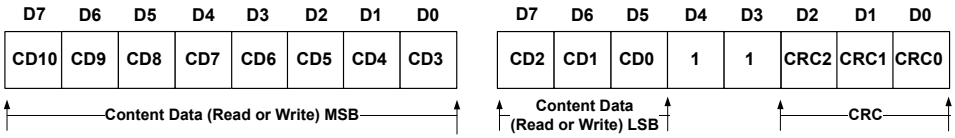

Figure 12. Content Data Bytes

2.7 SINGLE WRITE Operation

For a single write operation, the Slave Address byte has the R/W bit set to '0' and is followed by the memory address byte and two content data bytes as shown below in Figure 13. The master sends the address bytes and content data, which are acknowledged by the slave.

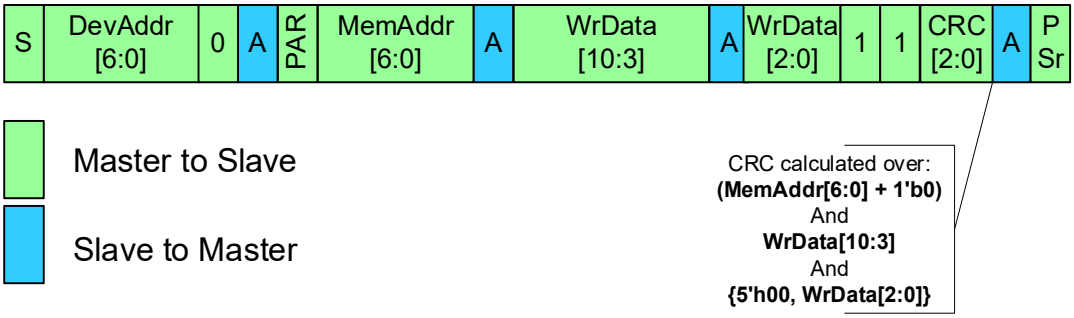

Figure 13. Single Write Frame

Notes:

- If I2C master continue to provide clocks and data after the second write data byte, the IC will NACK the next byte.
- Consider the programming time when writing to a FTP register. Refer to Table 5 for details.

2.8 SINGLE READ Operation

For a single read operation, the Slave Address byte has the R/W bit set to ‘0’, followed by the memory address byte. After a stop (P) or repeated start (Sr) condition, the Slave Address byte follows with the R/W bit set to ‘1’ and two content data bytes. The master sends the address bytes, which are acknowledged by the slave. The slave sends the content data, which are acknowledged by the master.

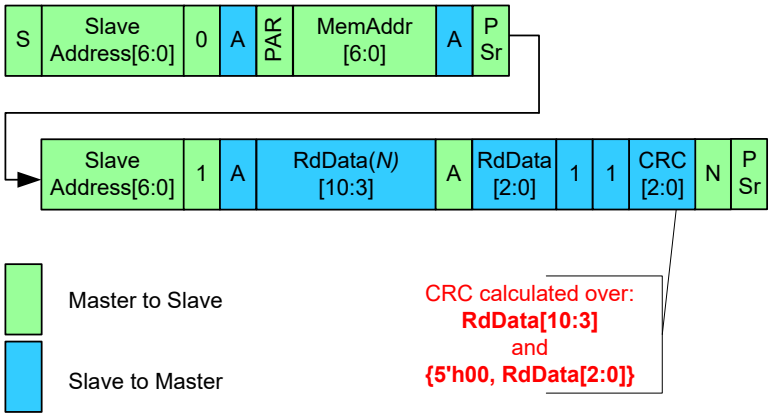

Figure 14. Single Read Frame

Note: If the I2C master continues to provide clocks after the second read data byte, the IC continues to provide the same read data.

2.9 Protocol Integrity Check

The Data Integrity Check is an extension of the I2C protocol for fail safe communication between I2C master and slave devices. This check is activated by default, and can be disabled in System Configuration 2 register (0x01, bit [2] prot_integ_check_dis).

2.9.1. Slave Address Parity Check

The IPS2550 supports an even parity check of I2C device address. If the check fails, the subsequent command is discarded and the diagnostic status “protocol_integrity_fail” is asserted.

PAR: Even parity calculated and checked for preceding received SlaveAddress address byte:

PAR = XOR ({SlaveAddr, RnW})

Table 3 shows the Slave Address field handling for verified “read/write action”.

Table 3. I2C Slave Address Byte and Memory Address Field Integrity Check

Protocol Integrity Check Disable	D7	D6……D0	Diagnostic	Description
0b1	0b1	0bxxxxxxx	Asserted	No action, no slave acknowledge
0b1	0b0	0bxxxxxxx	Idle	Read/write action
0b0	PAR_{fail}	0bxxxxxxx	Asserted	Parity check fails, no action, no slave acknowledge
0b0	PAR_{pass}	0bxxxxxxx	Idle	Parity check passes, read/write action

2.9.2. Content Data CRC check

A 16-bit word is defined and transported by two consecutive data bytes (data byte n, data byte n+1).

A 3-bit CRC field is defined to detect the presence of errors in the transmission of each 16-bit data word. If the data transferred does not pass CRC verification, no write action is taken, the slave receiver does not produce an acknowledge, and the diagnostic status “protocol_integrity_fail” is asserted.

The polynomial used to calculate the 3-bit CRC is:

$CRC(x) = x^3 + x^1 + x^0$

Table 4 shows the data word handling for verified “write action”.

Table 4. I2C <ContentData> Integrity Check

Protocol Integrity Check Disable	<ContentData>	<Reserved>		Diagnostic	Description
0b1	0bxxx_xxxx_xxxx	0b1_1111		Idle	Write action executed
0b1	0bxxx_xxxx_xxxx	0b0_0000 …. 0b1_1110		Asserted	Write action suspend, no slave acknowledge
Protocol Integrity Check Enable	**< ContentData >**	**<Reserved>**	**<CRC>**	**Diagnostic**	**Description**
0b0	0bxxx_xxxx_xxxx	0b11	Pass	Idle	Write action executed
0b0	0bxxx_xxxx_xxxx	0b11	Fail	Asserted	Write action suspend, no slave acknowledge
0b0	0bxxx_xxxx_xxxx	0b00 … 0b10	Fail	Asserted	Write action suspend, no slave acknowledge
0b0	0bxxx_xxxx_xxxx	0b00 … 0b10	Pass	Asserted	Write action suspend, no slave acknowledge

3. Memory Architecture

The memory architecture of the IPS2550 consists of three different storage blocks with a total address range of 7 bits as follows:

- Few Times Programmable (FTP) 00_{HEX} through $1F_{HEX}$
- Internal Configuration (RFU) 20_{HEX} through $3F_{HEX}$
- Shadow Register Bank (SRB) 40_{HEX} through 67_{HEX}
- Special Function Register (SFR) 68_{HEX} through $7F_{HEX}$

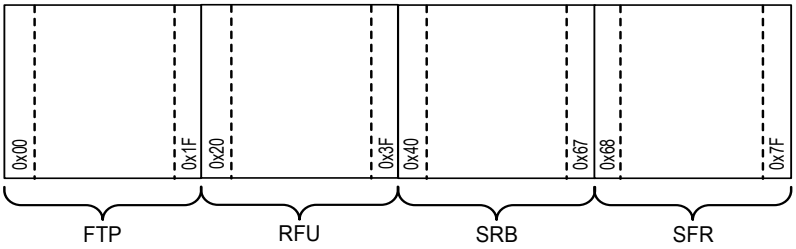

Figure 15. Memory Architecture

Notes:

- Some registers are be modified by internal processes.
- After power-on-reset (POR), most of the FTP content is mirrored into the corresponding SRB address range within the start-up time window.
- Do not change registers and bits that are marked as “Internal Configuration (RFU)” with note “Read as X”.

3.1 Memory Map and Default FTP Values

After writing to a FTP register, a programming time of minimum 3ms is required before a new command can be sent.

Table 5. FTP (Non-Volatile)

Address (hex)	Description	Bit position				Default Value
		15…12	11…8	7…4	3…0	hex
0x00	System configuration 1	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0	0x0121
0x01	System configuration 2	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0	0x0001
0x02	R1/R2 gain	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0	0x0300
0x03	R1 gain compensation	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0	0x0000

Address (hex)	Description	Bit position				Default Value
		15…12	11…8	7…4	3…0	hex
0x04	R1 offset compensation	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0	0x0000
0x05	R2 gain compensation	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0	0x0000
0x06	R2 offset compensation	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0	0x0000
0x07	Transmitter current configuration	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0	0x00BE
0x08	Transmitter frequency time-base	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0	0x00AF
0x09	Transmitter frequency lower limit	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0	0x0000
0x0A	Transmitter frequency upper limit	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0	0x07FF
0x0B	Interrupt enable 1	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0	0x0000
0x0C	Interrupt enable 2	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0	0x0000
0x0D	Interrupt enable 3	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0	0x0000
0x0E	IRQN watchdog	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0	0x0000
0x0F	AGC Plausibility configuration	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0	0x0000
0x10…0x17	Internal Configuration	Read as ‘X’				
0x18	Customer Identifier	ECC	PDED, n10..n8	n7 …..n4	n3…n0	0x0000
0x19	Product Identifier	ECC	PDED, n10..n8	n7 …..n4	n3…n0	0x0019
0x1A…0x3E	Internal Configuration	Read as ‘X’				
0x3F	Entry / Exit analog programming	Read as ‘X’				

Table 6. SRB/SFR (Volatile)

Address (hex)	Description	Bit position			
		15……12	11……8	7…..4	3…..0
0x40	System configuration 1	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0
0x41	System configuration 2	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0
0x42	R1/R2 gain	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0
0x43	R1 gain compensation	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0
0x44	R1 offset compensation	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0
0x45	R2 gain compensation	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0
0x46	R2 offset compensation	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0
0x47	Transmitter current configuration	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0
0x48	Transmitter frequency time-base	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0
0x49	Transmitter frequency lower limit	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0
0x4A	Transmitter frequency upper limit	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0
0x4B	Interrupt enable 1	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0
0x4C	Interrupt enable 2	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0
0x4D	Interrupt enable 3	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0
0x4E	IRQN watchdog	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0
0x4F	AGC Plausibility configuration	ECC	P_{DED}, n10..n8	n7 …..n4	n3…n0
0x50…0x67	Internal Configuration	Read as ‘X’			
0x68	Interrupt clear 1	Not used	‘x’, n10..n8	n7 …..n4	n3…n0
0x69	Interrupt clear 2	Not used	‘x’, n10..n8	n7 …..n4	n3…n0
0x6A	Interrupt clear 3	Not used	‘x’, n10..n8	n7 …..n4	n3…n0
0x6B	Interrupt state 1	Not used	‘x’, n10..n8	n7 …..n4	n3…n0
0x6C	Interrupt state 2	Not used	‘x’, n10..n8	n7 …..n4	n3…n0
0x6D	Interrupt state 3	Not used	‘x’, n10..n8	n7 …..n4	n3…n0
0x6E	Transmitter counter state	Not used	‘x’, n10..n8	n7 …..n4	n3…n0
0x6F	Internal Configuration	Read as ‘X’			
0x70	FTP ECC state	Not used	‘x’, n10..n8	n7 …..n4	n3…n0
0x71…0x72	Internal Configuration	Read as ‘X’			

Address (hex)	Description	Bit position			
		15……12	11……8	7…..4	3…..0
0x73	Product Identifier Version	Not used	‘x’, n10..n8	n7 …..n4	n3…n0
0x74…0x77	Internal Configuration	Read as ‘X’			
0x78	AGC_OBS	Not used	‘x’, n10..n8	n7 …..n4	n3…n0
0x79	DBIST_STS	Not used	‘x’, n10..n8	n7 …..n4	n3…n0
0x7A…0x7E	Internal Configuration	Read as ‘X’			
0x7F	External SM for checking CRC	Not used	‘x’, n10..n8	n7 …..n4	n3…n0

3.2 Register Descriptions

3.2.1. FTP (Non-Volatile) and SRB (Volatile)

Table 7. System Configuration 1: Address 0x00 FTP; 0x40 SRB

Address FTP	Address SRB	Bits	Function	Access FTP	Access SRB	Reset SRB	Default FTP
0x00	0x40	[15:12]	**Ecc:** Parity word for error correction	NA	NA	NA	NA
		[11]	**ded_par:** Parity bit for double bit error detection	NA	NA	NA	NA
		[10]	**ana_prgm_dis:** Disables programming over output pins and enables faster start-up. • 0b0: programming through analog enabled; start-up time 5ms • 0b1: programming through analog disabled; start-up time 3ms	RW	RO	0	0
		[9]	**afe_agc_dis:** Disables the automatic gain control. • 0b0: AGC enabled • 0b1: AGC disabled **Note:** If the AGC is enabled, afe_gain_code [6:0] in Table 9 is used as start value for the AGC during power-up.			0	0
		[8]	**intr_volatile_mode:** Enables dynamic interrupt signaling. If this mode is enabled, an interrupt is cleared automatically if the error disappears after a debounce time of up to 5ms. • 0b0: disable, IRQN cleared by uC host • 0b1: enable, IRQN event type			1	1
		[7:4]	**i2c_slave_sub_addr:** Programmable most significant nibble (MSN) of the I2C Slave Address. Refer to section 2.3 for details.			0x2	0x2
		[3:2]	**back_end_irqn_ena:** Enable Interrupt signaling at back-end interface. • 2'b00: interrupt signaling @ SinP/CosP/SinN/CosN OFF • 2'b01: interrupt signaling @ SinP/CosP ON; SinN/CosN OFF • 2'b10: interrupt signaling @ SinP/CosP OFF; SinN/CosN ON • 2'b11: interrupt signaling @ SinP/CosP / SinN/CosN ON **Note:** Critical alarm flags will always put the outputs in diagnostic mode.			0x3	0x0
		[1]	**back_end_protocol:** Configuration option to switch from Differential Ouptut into Single Ended mode. • 0b0: analog differntial: SINP, SINN, COSP; COSN • 0b1: analog single ended: SINP, REF, COSP, REF			0	0
		[0]	**system_protocol:** Configures Pin1 as Interrupt or address pin. • 0b0: Interrupt: I2C Slave Address: MSN & 3’b000 • 0b1: Address Pin: I2C Slave Address: MSN[3:1] and PIN1 and 3’b000 Consider reserved address groups (0000XXX and 1111XXX)			1	1

Table 8. System Configuration 2: Address 0x01 FTP; 0x41 SRB

Address FTP SRB		Bits	Function	Access FTP	Access SRB	Reset SRB	Default FTP
0x01	0x41	[15:12]	**Ecc**: Parity word for error correction	NA	NA	NA	NA
		[11]	**ded_par:** Parity bit for double bit error detection	NA	NA	NA	NA
		[10]	**thermal_shutdown_en:** Enable automatic shutdown of the transmitter (Stop excitation emitter current = 8'h00) in case the temperature exceeds the T_{OVT_ERR} (over-temperature error) threshold defined in the *IP2550 Datasheet* document.. Note: The output buffers are switched off automatically to reduce the power consumption after exceeding the T_{OVT_WARN} (temperature warning) threshold defined in the *IP2550 Datasheet* document. • 0b0: disable automatic shutdown • 0b1: enable shutdown	RW	RO	0	0
		[9:8]	**rc_amp_swap_time:** Configures the RX amplifier swapping time if RX swapping is enabled in sysconf2[7:6]: • 0b11: (For FuSa) • 0b00: 10µs • 0b01: 50µs • 0b10: 100µs • 0b11: 200µs Consider system sampling time and noise requirements when selecting swap time.			0x0	0
		[7:6]	**rc_swap:** Configuration bits to activate static or dynamic swapping of the RX amplifier (for FuSa) • 0b00: off • 0b01: R1/2 swap static • 0b10: R1/2 swap static • 0b11: R1/2 swap toggle If swapped, amplifier 2 is swapped into channel 1 and vice versa. Amplifier 2 errors are identified on channel1 output. For swap toggle, the setting is exchanged periodically, and error on one amplifier is visible as a ripple on the output signals. **If "swap toggle" is activated:** higher noise must be expected. The internal offset compensation can be used to minimize the output ripple caused by residual offsets. In this situation, the internal offset compensation for R1 and R2 cannot be used to compensate for coil offsets any more and must be compensated by the application microcontroller.			0x0	0x0
		[5]	**rc_switch:** Switch between interleaved or straight receiver pin configurations. • 0b0: interleaved connections, IPS2550 default (FuSa) • 0b1: straight connection, IPS2200 compliant			0	0
		[4:3]	**cyber_security:** Configures the I2C access mode. • 0b00: I2C read/write access • 0b01: I2C read only access • 0b10: no read/write access • 0b11: I2C read / write access			0x0	0x0
		[2]	**prot_integ_check_dis:** Deactivates the I2C integrity check. • 0b0: integrity check 'On' • 0b1: integrity check 'Off'			0	0
		[1]	**agc_mode:** Configures the output voltage target for the AGC in 5V mode. In 3V3 supply mode it is 0.9V. • 0b0 – Programming option1: 1.8Vpp mode (for 5V and 3V3 supply) • 0b1 – Programming option2: 3.0Vpp mode (for 5V mode only)			0	0

Address FTP	Address SRB	Bits	Function	Access FTP	Access SRB	Reset SRB	Default FTP
		[0]	**vdda_3v_5v:** Configuration bit for the supply voltage range. • 0b0: 3.3V mode • 0b1: 5.0V mode			1	1

Table 9. R1/R2 gain: Address 0x02 FTP; 0x42 SRB

Address FTP	Address SRB	Bits	Function	Access FTP	Access SRB	Reset SRB	Default FTP
0x02	0x42	[15:12]	**Ecc:** Parity word for error correction	NA	NA	NA	NA
		[11]	**ded_par:** Parity bit for double bit error detection	NA	NA	NA	NA
		[10]	**agc_plause_chk_en:** Enable AGC plausibility check. Behaviour defined by register agc_plause_cfg. If enabled, AGC stops gain code update when out of plausibility range. If the plausibility check is enabled, the threshold limits in register “AGC Plausibility Configuration: Address 0x0F FTP; 0x4F SRB” must be configured correctly. The upper threshold must be configured obove the lower threshold. • 0b1: enabled • 0b0: disabled	RW	RW	0	0
		[9:8]	**agc_wait_tmr_sel:** AGC timer selection when changing the gain in opposite direction: Used for selecting the wait time after the AGC direction changes. • 2'b00: 30ms • 2'b01: 100ms • 2'b10: 300ms • 2'b11: 10µs			0	0x3
		[7]	**d2a_afe_boost_sel**: Overall gain multiplication by factor of 2 • 0b1: enabled , Gain factor 2x • 0b0: disabled , Gain factor 1x			0	0

<table>
<tr><th colspan="2">Address
FTP SRB</th><th>Bits</th><th>Function</th><th colspan="2">Access
FTP SRB</th><th>Reset
SRB</th><th>Default
FTP</th></tr>
<tr><td></td><td></td><td>[6:0]</td><td>afe_gain_code: Overal gain configuration for receiver 1 and 2.

<table>
<tr><th>Code in hex</th><th>Gain Factor</th><th>Code in hex</th><th>Gain Factor</th><th>Code in hex</th><th>Gain Factor</th><th>Code in hex</th><th>Gain Factor</th></tr>
<tr><td>0x0</td><td>2.00</td><td>0x18</td><td>5.66</td><td>0x30</td><td>16.00</td><td>0x48</td><td>45.25</td></tr>
<tr><td>0x1</td><td>2.10</td><td>0x19</td><td>5.94</td><td>0x31</td><td>16.80</td><td>0x49</td><td>47.51</td></tr>
<tr><td>0x2</td><td>2.18</td><td>0x1A</td><td>6.17</td><td>0x32</td><td>17.45</td><td>0x4A</td><td>49.36</td></tr>
<tr><td>0x3</td><td>2.29</td><td>0x1B</td><td>6.48</td><td>0x33</td><td>18.32</td><td>0x4B</td><td>51.83</td></tr>
<tr><td>0x4</td><td>2.38</td><td>0x1C</td><td>6.73</td><td>0x34</td><td>19.02</td><td>0x4C</td><td>53.82</td></tr>
<tr><td>0x5</td><td>2.50</td><td>0x1D</td><td>7.06</td><td>0x35</td><td>19.98</td><td>0x4D</td><td>56.52</td></tr>
<tr><td>0x6</td><td>2.59</td><td>0x1E</td><td>7.34</td><td>0x36</td><td>20.75</td><td>0x4E</td><td>58.69</td></tr>
<tr><td>0x7</td><td>2.72</td><td>0x1F</td><td>7.70</td><td>0x37</td><td>21.79</td><td>0x4F</td><td>61.62</td></tr>
<tr><td>0x8</td><td>2.83</td><td>0x20</td><td>8.00</td><td>0x38</td><td>22.62</td><td>0x50</td><td>64.00</td></tr>
<tr><td>0x9</td><td>2.97</td><td>0x21</td><td>8.40</td><td>0x39</td><td>23.76</td><td>0x51</td><td>67.20</td></tr>
<tr><td>0xA</td><td>3.09</td><td>0x22</td><td>8.72</td><td>0x3A</td><td>24.68</td><td>0x52</td><td>69.79</td></tr>
<tr><td>0xB</td><td>3.24</td><td>0x23</td><td>9.16</td><td>0x3B</td><td>25.91</td><td>0x53</td><td>73.28</td></tr>
<tr><td>0xC</td><td>3.36</td><td>0x24</td><td>9.51</td><td>0x3C</td><td>26.91</td><td>0x54</td><td>76.10</td></tr>
<tr><td>0xD</td><td>3.53</td><td>0x25</td><td>9.99</td><td>0x3D</td><td>28.26</td><td>0x55</td><td>79.90</td></tr>
<tr><td>0xE</td><td>3.67</td><td>0x26</td><td>10.38</td><td>0x3E</td><td>29.34</td><td>0x56</td><td>83.01</td></tr>
<tr><td>0xF</td><td>3.85</td><td>0x27</td><td>10.89</td><td>0x3F</td><td>30.81</td><td>0x57</td><td>87.16</td></tr>
<tr><td>0x10</td><td>4.00</td><td>0x28</td><td>11.31</td><td>0x40</td><td>32.00</td><td>0x58</td><td>90.50</td></tr>
<tr><td>0x11</td><td>4.20</td><td>0x29</td><td>11.88</td><td>0x41</td><td>33.60</td><td>0x59</td><td>95.02</td></tr>
<tr><td>0x12</td><td>4.36</td><td>0x2A</td><td>12.34</td><td>0x42</td><td>34.90</td><td>0x5A</td><td>98.72</td></tr>
<tr><td>0x13</td><td>4.58</td><td>0x2B</td><td>12.96</td><td>0x43</td><td>36.64</td><td>0x5B</td><td>103.66</td></tr>
<tr><td>0x14</td><td>4.76</td><td>0x2C</td><td>13.46</td><td>0x44</td><td>38.05</td><td>0x5C</td><td>107.65</td></tr>
<tr><td>0x15</td><td>4.99</td><td>0x2D</td><td>14.13</td><td>0x45</td><td>39.95</td><td>0x5D</td><td>113.03</td></tr>
<tr><td>0x16</td><td>5.19</td><td>0x2E</td><td>14.67</td><td>0x46</td><td>41.50</td><td>0x5E</td><td>117.38</td></tr>
<tr><td>0x17</td><td>5.45</td><td>0x2F</td><td>15.41</td><td>0x47</td><td>43.58</td><td>0x5F</td><td>123.24</td></tr>
</table>
</td><td></td><td></td><td>0x0</td><td>0x0</td></tr>
</table>

Table 10. R1 Fine Gain Compensation: Address 0x03 FTP; 0x43 SRB

Address FTP	Address SRB	Bits	Function	Access FTP	Access SRB	Reset SRB	Default FTP
0x03	0x43	[15:12]	**Ecc:** Parity word for error correction	NA	NA	NA	NA
		[11]	**ded_par:** Parity bit for double bit error detection	NA	NA	NA	NA
		[10:7]	**RFU:** Read as X	RW	RO	0x0	0x0
		[6:0]	**afe_r1_gain_cal:** Used for increasing the amplitude of receiver 1 to compensate amplitude mismatch caused by not ideal coils. Overall range is 16% with 0.125% step size. • 0x00: no correction • 0x01: 0.125% • 0x02: 0.250% • 0x03: 0.375% • … • 0x7E: 15.875% • 0x7F: 16%		RW	0x00	0x00

The output signals can have amplitude mismatch resulting from production tolerances or a non-ideal coil structure. Such amplitude mismatch leads to increased angle non-linearity that is calculated from sine and cosine signals. Therefore, the application microcontroller usually calculates and eliminate the amplitude mismatch before angle calculation. IPS2550 is able to eliminate such amplitude mismatch already within the sensor IC as shown in Figure 16. The left picture shows amplitude mismatch on the cosine channel causing angle error, the right picture shows the error and the improved signal after compensation.

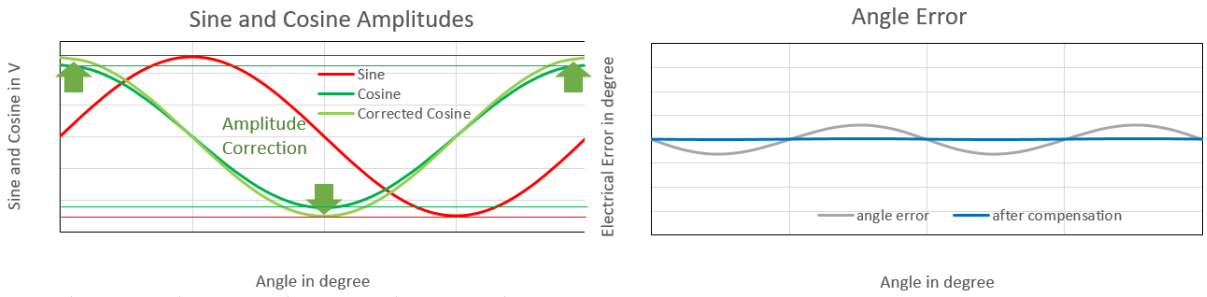

Figure 16. Compensated and Uncompensated Amplitude Mismatch

Table 11. R1 Offset Compensation: Address 0x04 FTP; 0x44 SRB

Address FTP	Address SRB	Bits	Function	Access FTP	Access SRB	Reset SRB	Default FTP
0x04	0x44	[15:12]	**Ecc**: Parity word for error correction	NA	NA	NA	NA
		[11]	**ded_par:** Parity bit for double bit error detection	NA	NA	NA	NA
		[10]	**dis_fsm_output_err:** Use for disabling the FSM output error interrupt signalizing. • 0b0: signalizing enabled • 0b1: signalizing disabled	RW	RW	0	0
		[9]	**bist_dis:** Used for disabling the BIST (Built-in Self Test during startup) • 0b0: Diagnostic BIST enabled • 0b1: Diagnostic BIST disabled			0	0
		[8]	**dis_r12_short_fail:** Disable diagnostic alarm at R1/2 short fail. • 1'b0: enabled, R1/2 short fail triggers diagnostic state • 1'b1: disabled, R1/2 short fail doesn't trigger diagnostic state			0	0
		[7]	**afe_r1_offset_cal:** Define the offset compensation polarity. • 0b0: addition • 0b1: subtraction			0	0
		[6:0]	**afe_r1_offset_cal:** R1 Offset compensation relative to the LC oscillator amplitude. Used for reducing the signal offset caused by non-ideal coils. Overall range is 0.2% relative to the LC oscillator amplitude, the step size is 0.0015%. • 0x00: no correction • 0x01: 0.0015% • 0x02: 0.0030% • 0x03: 0.0045% • … • 0x7E: 0.189% • 0x7F: 0.1905%			0x00	0x00

The output signals can have offset resulting from production tolerances or a non-ideal coil structure. Such offset leads to increased angle non-linearity that is calculated from the sine and cosine signals. Therefore, the application microcontroller usually calculates and eliminate signal offset before angle calculation. IPS2550 is able to eliminate such offset already within the sensor IC as shown in Figure 17. The left picture shows signal offset on the cosine channel causing angle error, the right picture shows the error and the improved signal after compensation.

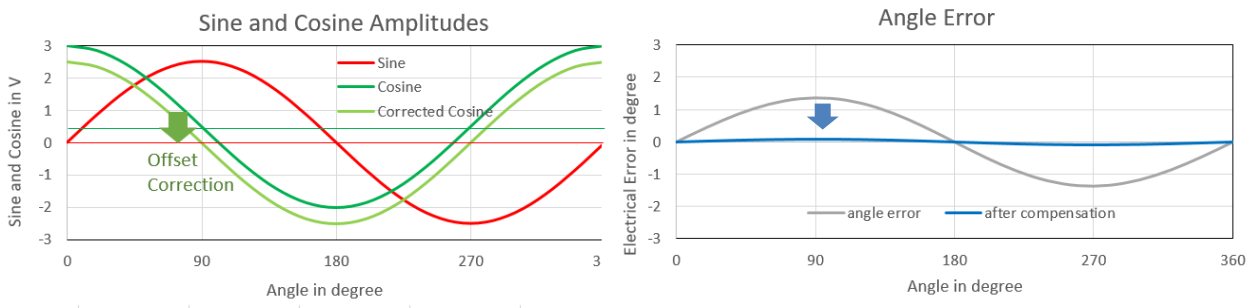

Figure 17. Compensated and Uncompensated Signal Offset

Table 12. R2 Fine Gain Compensation: Address 0x05 FTP; 0x45 SRB

Address FTP	Address SRB	Bits	Function	Access FTP	Access SRB	Reset SRB	Default FTP
0x05	0x45	[15:12]	**Ecc:** Parity word for error correction	NA	NA	NA	NA
		[11]	**ded_par:** Parity bit for double bit error detection	NA	NA	NA	NA
		[10:7]	**RFU:** Read as X	RW	RO	0x0	0x0
		[6:0]	**afe_r2_gain_cal:** Used for increasing the amplitude of receiver 1 to compensate amplitude mismatch caused by non-ideal coils. Overall range is 16%, one step is 0.125% • 0x00: no correction • 0x01: 0.125% • 0x02: 0.250% • 0x03: 0.375% • … • 0x7E: 15.875% • 0x7F: 16%		RW	0x00	0x0

Table 13. R2 Offset Compensation: Address 0x06 FTP; 0x46 SRB

Address FTP	Address SRB	Bits	Function	Access FTP	Access SRB	Reset SRB	Default FTP
0x06	0x46	[15:12]	**Ecc:** Parity word for error correction	NA	NA	NA	NA
		[11]	**ded_par:** Parity bit for double bit error detection	NA	NA	NA	NA
		[10:8]	**RFU:** Read as X	RW	RO	0x0	0x0
		[7]	**afe_r2_offset_cal:** Define the applied offset polarity. Offset compensation polarity. • 0b0: addition • 0b1: subtraction		RW	0x00	0x00
		[6:0]	**afe_r2_offset_cal:** Offset compensation relative to the LC oscillator amplitude. Used for reducing the signal offset cause by non-ideal coils. Overall range is 0.2%, the step size is 0.0015%. • 0x00: no correction • 0x01: 0.0015% • 0x02: 0.0030% • 0x03: 0.0045% • ... • 0x7E: 0.189% • 0x7F: 0.1905%				

Table 14. Transmitter Current Configuration: Address 0x07 FTP; 0x47 SRB

Address FTP	Address SRB	Bits	Function	Access FTP	Access SRB	Reset SRB	Default FTP
0x07	0x47	[15:12]	**Ecc:** Parity word for error correction	NA	NA	NA	NA
		[11]	**ded_par:** Parity bit for double bit error detection	NA	NA	NA	NA
		[10:8]	**RFU:** Read as X	RW	RO	0x0	0x0
		[7:6]	**exc_current_cal:** LC oscillator bias current setting multiplication factor. Multiplication factor for LC oscillator bias current. • 0b00: mult. 1 • 0b01: mult. 4 • 0b10: mult. 16 • 0b11: mult. 64		RW	0x00	0xBE
		[5:0]	**exc_current_cal:** Base value for LC oscillator bias current. The total current is the base value multiplied by the multiplication factor. Calculate the bias current based on LC tank parameters and bias current equation as follows: • 0b00_0000 = 0.0µA • 0b00_0001 = 0.5µA • 0b00_0010 = 1.0µA • 0b11_1111 = 31.5µA				

The transmitter current for the LC Tank as shown in Figure 18 must be configured based on the application requirements. Reducing the transmitter bias current decreases the transmitter amplitude and lowers the total current consumption. The behavior is not linear and depends on the configuration of the LC oscillator.

Note that the oscillator requires sufficient bias current to ensure stable oscillation. Refer to following equation to estimate the bias current setting. The estimated value might be adjusted to meet application requirements.

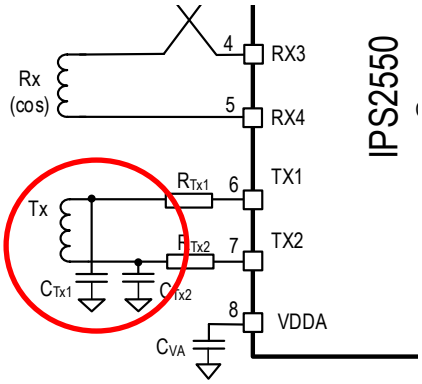

Figure 18. Transmitter current configuration for LC Tank

$$I_{BIAS} = VDD / (35 \times L\_Tx \times Q \times F)$$

Where:

VDD = Supply voltage in Volt

L_TX = Inductance of transmitter coil in Henry

F = Transmitter oscillator frequency in Hz

Q = Quality factor of the Transmitter coil, it is calculated according to the following formula:

$$Q = \frac{1}{R_{L\_TX}}\sqrt{\frac{L\_Tx}{C}}$$

Where:

R_{L_TX} = Resistance of the Transmitter Coil

C = Capacitance of the Transmitter resonator ($C = C_{Tx1}/2$)

For Example:

If L = 6µH, R = 1Ω, C = 345pF (such that the transmitter oscillates at F = 3.5MHz) and VDD = 5V

According to the formula above:

Q = 132

I_{BIAS} = 51.5µA

The bit configuration for the bias current base value and multiplication factor can be selected from Table 15. An example is highlighted by blue, where 26 dec for the base value and 1 dec for the multiplication factor is shown.

Table 15. Transmitter Bias Current in µA

		exc_current_cal[5:0]: Base value in dec															
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
exc_current_cal [7:6]: Multiplication factor	**0:1x**	0	0.5	1	1.5	2	2.5	3	3.5	4	4.5	5	5.5	6	6.5	7	7.5
	1:4x	0	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30
	2:16x	0	8	16	24	32	40	48	56	64	72	80	88	96	104	112	120
	3:64x	0	32	64	96	128	160	192	224	256	288	320	352	384	416	448	480
		16	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**
	0:1x	8	8.5	9	9.5	10	10.5	11	11.5	12	12.5	13	13.5	14	14.5	15	15.5
	1:4x	32	34	36	38	40	42	44	46	48	50	52	54	56	58	60	62
	2:16x	128	136	144	152	160	168	176	184	192	200	208	216	224	232	240	248
	3:64x	512	544	576	608	640	672	704	736	768	800	832	864	896	928	960	992
		32	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**	**45**	**46**	**47**
	0:1x	16	16.5	17	17.5	18	18.5	19	19.5	20	20.5	21	21.5	22	22.5	23	23.5
	1:4x	64	66	68	70	72	74	76	78	80	82	84	86	88	90	92	94
	2:16x	256	264	272	280	288	296	304	312	320	328	336	344	352	360	368	376
	3:64x	1024	1056	1088	1120	1152	1184	1216	1248	1280	1312	1344	1376	1408	1440	1472	1504
		48	**49**	**50**	**51**	**52**	**53**	**54**	**55**	**56**	**57**	**58**	**59**	**60**	**61**	**62**	**63**
	0:1x	24	24.5	25	25.5	26	26.5	27	27.5	28	28.5	29	29.5	30	30.5	31	31.5
	1:4x	96	98	100	102	104	106	108	110	112	114	116	118	120	122	124	126
	2:16x	384	392	400	408	416	424	432	440	448	456	464	472	480	488	496	504
	3:64x	1536	1568	1600	1632	1664	1696	1728	1760	1792	1824	1856	1888	1920	1952	1984	2016

Table 16. Transmitter Frequency Time-Base: Address 0x08 FTP; 0x48 SRB

Address FTP	Address SRB	Bits	Function	Access FTP	Access SRB	Reset SRB	Default FTP
0x08	0x48	[15:12]	**Ecc:** Parity word for error correction	NA	NA	NA	NA
		[11]	**ded_par:** Parity bit for double bit error detection	NA	NA	NA	NA
		[10:0]	**exc_freq_wdg**[1]**:** Time base setting for the TX frequency measurement. • 0x000: counter off • 0x001: 1 osc_dig cycle • 0x002: 2 osc_dig cycles • … • 0x7FF: 2047 osc_dig cycles	RW	RW	0x00	0xAF

1. Configures the time base for the transmitter frequency measurement. The default value is 175dec or AF hex. Do not change the time-base configuration. Refer to Table 17 and Table 18 for details on transmitter frequency.

Table 17. Transmitter Frequency Lower Limit: Address 0x09 FTP; 0x49 SRB

Address FTP	Address SRB	Bits	Function	Access FTP	Access SRB	Reset SRB	Default FTP
0x09	0x49	[15:12]	**Ecc:** Parity word for error correction	NA	NA	NA	NA
		[11]	**ded_par:** Parity bit for double bit error detection	NA	NA	NA	NA
		[10:0]	**exc_freq_ll:** Lower limit fort the TX frequency alarm. • 0x000: 0 osc_dig cycle • 0x001: 1 osc_dig cycle • 0x002: 2 osc_dig cycles • … • 0x7FF: 2047 osc_dig cycles	RW	RW	0x00	0x00

The programmed time base must be AF hex (default) in FTP 0x08 and SRB 0x48. For this time base, the lower limit is calculated as:

$$exc\_frq\_ll = \frac{F_{TXlow}}{20000}$$

Where

F_{TXlow} = lower frequency limit in Hz

Example: Lower limit is 2.8 Mhz

$$exc\_frq\_ll = \frac{2800000}{20000} = 140 \text{ dec}$$

Table 18. Transmitter Frequency Upper Limit: Address 0x0A FTP; 0x4A SRB

Address FTP	Address SRB	Bits	Function	Access FTP	Access SRB	Reset SRB	Default FTP
0x0A	0x4A	[15:12]	**Ecc:** Parity word for error correction	NA	NA	NA	NA
		[11]	**ded_par:** Parity bit for double bit error detection	NA	NA	NA	NA
		[10:0]	**exc_freq_ul:** Upper limit fort the TX frequency alarm. • 0x000: 0 osc_dig cycle • 0x001: 1 osc_dig cycle • 0x002: 2 osc_dig cycles • … • 0x7FF: 2047 osc_dig cycles	RW	RW	0x00	0x7FF

The programmed time base must be AF hex (default) in FTP 0x08 and SRB 0x48. For this time base, the upper limit is calculated as:

$$exc\_frq\_ul = \frac{F_{TXup}}{20000}$$

Where: F_{TXup} = upper frequency limit in Hz

Example: Upper limit is 4.2 Mhz: $exc\_frq\_ll = \frac{4200000}{20000}$ = 210 dec

Table 19. Interrupt Enable 1: Address 0x0B FTP; 0x4B SRB

Address FTP	Address SRB	Bits	Function	Access FTP	Access SRB	Reset SRB	Default FTP
0x0B	0x4B	[15:12]	**Ecc:** Parity word for error correction	NA	NA	NA	NA
		[11]	**ded_par:** Parity bit for double bit error detection	NA	NA	NA	NA
		[10]	**Overvoltage_vdd:** Enables Interrupt at VDD over-voltage alarm • 0b0: irstate1[10] disable to drive interrupt request IRQN • 0b1: irstate1[10] drives interrupt request IRQN	RW	RW	0	0
		[9]	**Undervoltage:_vdd:** Enables Interrupt at VDD under-voltage alarm • 0b0: irstate1[9] disable to drive interrupt request IRQN • 0b1: irstate1[9] drives interrupt request IRQN			0	0
		[8]	**Temperature alarm:** Enables Interrupt at temperature alarm if the junction temperature exceeds the warning level. • 0b0: irstate1[8] disable to drive interrupt request IRQN • 0b1: irstate1[8] drives interrupt request IRQN			0	0
		[7]	**data_access_fail:** Enables Interrupt at I2C access timeout • 0b0: irstate1[7] disable to drive interrupt request IRQN • 0b1: irstate1[7] drives interrupt request IRQN			0	0
		[6]	**i2c_protocol_fail:** Enables Interrupt at I2C protocol fail • 0b0: irstate1[6] disable to drive interrupt request IRQN • 0b1: irstate1[6] drives interrupt request IRQN			0	0
		[5]	**srb_ded SRB:** double bit error detection / SFR testmode register 1/2 parity bit error detection. Enables Interrupt at SRB DED error • 0b0: irstate1[5] disable to drive interrupt request IRQN • 0b1: irstate1[5] drives interrupt request IRQN			0	0
		[4]	**srb_sed SRB:** Enables Interrupt at SRB SED error • 0b0: irstate1[4] disable to drive interrupt request IRQN • 0b1: irstate1[4] drives interrupt request IRQN			0	0
		[3]	**nvm_ded:** Enables Interrupt at FTP DED error • 0b0: irstate1[3] disable to drive interrupt request IRQN • 0b1: irstate1[3] drives interrupt request IRQN			0	0
		[2]	**nvm_sed:** Enables Interrupt at FTP SED error • 0b0: irstate1[2] disable to drive interrupt request IRQN • 0b1: irstate1[2] drives interrupt request IRQN			0	0
		[1]	**lc_osc_freq_fail:** Enables Interrupt at TX frequency alarm (see limits register exc_freq_ll, exc_freq_ul, and exc_freq_wdg) • 0b0: irstate1[1] disable to drive interrupt request IRQN • 0b1: irstate1[1] drives interrupt request IRQN			0	0
		[0]	**lc_osc_stuck:** Enables Interrupt at LC oscillator stuck alarm • 0b0: irstate1[0] disable to drive interrupt request IRQN • 0b1: irstate1[0] drives interrupt request IRQN			0	0

Table 20. Interrupt Enable 2: Address 0x0C FTP; 0x4C SRB

Address FTP	Address SRB	Bits	Function	Access FTP	Access SRB	Reset SRB	Default FTP
0x0C	0x4C	[15:12]	**Ecc:** Parity word for error correction	NA	NA	NA	NA
		[11]	**ded_par:** Parity bit for double bit error detection	NA	NA	NA	NA
		[10]	**csn_data_overvoltage:** Enables Interrupt at IRQN_CSN/DATA pin overvoltage alarm • 0b0: irstate2[10] disable to drive interrupt request IRQN • 0b1: irstate2[10] drives interrupt request IRQN	RW	RW	0	0
		[9]	**vdda_undervoltage:** Enables Interrupt at VDDA under-voltage alarm • 0b0: irstate2[9] disable to drive interrupt request IRQN • 0b1: irstate2[9] drives interrupt request IRQN			0	0
		[8]	**apb_transfer_fail:** APB bus transfer failure. Any write access of read-only register are rejected by the APB-bus control and flagged (see sys_conf2[6]). Enables Interrupt at APB bus transfer failure • 0b0: irstate2[8] disable to drive interrupt request IRQN • 0b1: irstate2[8] drives interrupt request IRQN			0	0
		[7]	**irqn watchdog:** Enables Interrupt at interrupt watchdog timeout. The watchdog timer is used to test the interrupt system. If the watchdog is enabled, an interrupt is triggered at watchdog timeout (for configuration options see Table 22). To get the interrupt signaled at Pin1 (ADR_IRQN), the system_protocol setting must be configured for interrupt, and intr_volatile_mode must be diabled as shown in Table 7. • 0b0: irstate2[7] disable to drive interrupt request IRQN • 0b1: irstate2[7] drives interrupt request IRQN			0	0
		[6]	**seal_ring_break:** Enables Interrupt at sealring break / mechanical failure • 0b0: irstate2[6] disable to drive interrupt request IRQN • 0b1: irstate2[6] drives interrupt request IRQN			0	0
		[5]	**fsm_err:** Enables Interrupt at Internal Finit State Machine (FSM) error • 0b0: irstate3[1] disable to drive interrupt request IRQN • 0b1: irstate3[1] drives interrupt request IRQN			0	0
		[4]	**outbuf_vcm_fail:** VCM voltage level of SINP/N or COSP/N not equal VDD/2. Enables Interrupt at output buffer VCM error. • 0b0: irstate2[4] disable to drive interrupt request IRQN • 0b1: irstate2[4] drives interrupt request IRQN			0	0
		[3]	**outbuf_current_fail:** Output buffer SINP, SINN, COSP, COSN exceeds limit. Enables Interrupt at output buffer error. • 0b0: irstate2[3] disable to drive interrupt request IRQN • 0b1: irstate2[3] drives interrupt request IRQN			0	0
		[2]	**vddd_overvoltage:** Digital power supply overvoltage Enables Interrupt at digital supply overvoltage. • 0b0: irstate3[4] disable to drive interrupt request IRQN • 0b1: irstate3[4] drives interrupt request IRQN			0	0
		[1]	**agc_err:** AGC control loop error - boundary code reached, amplitude NOT in range. Enables Interrupt at AGC range alarm. • 0b0: irstate3[3] disable to drive interrupt request IRQN • 0b1: irstate3[3] drives interrupt request IRQN			0	0

Address FTP SRB		Bits	Function	Access FTP SRB		Reset SRB	Default FTP
		[0]	**rx_fail:** Receiver path fail: short to GND / VDD or R1P/N or R2P/N open, LPF fail or short between R1 and R2. Enables Interrupt at RX coil error. • 0b0: irstate2[0] disable to drive interrupt request IRQN • 0b1: irstate2[0] drives interrupt request IRQN			0	0

Table 21. Interrupt Enable 3: Address 0x0D FTP; 0x4D SRB

Address FTP SRB		Bits	Function	Access FTP SRB		Reset SRB	Default FTP
0x0D	0x4D	[15:12]	**Ecc:** Parity word for error correction	NA	NA	NA	NA
		[11]	**ded_par**: Parity bit for double bit error detection	NA	NA	NA	NA
		[10:2]	**RFU:** Read as X	RW	RW	0x0	0
		[1]	**tx_coil_fail:** Transmitter coil short to VDD or open Enables Interrupt at TX coil error. • 0b0: irstate3[0] disable to drive interrupt request IRQN • 0b1: irstate3[0] drives interrupt request IRQN			0	0
		[0]	**bist_err:** Failure in BIST for the test mechanism. Enables Interrupt at BIST failure. • 0b0: irstate3[2] disable to drive interrupt request IRQN • 0b1: irstate3[2] drives interrupt request IRQN			0	0

Table 22. IRQN Watchdog: Address 0x0E FTP; 0x4E SRB

Address FTP SRB		Bits	Function	Access FTP SRB		Reset SRB	Default FTP
0x0E	0x4E	[15:12]	**ecc** Parity word for error correction	NA	NA	NA	NA
		[11]	**ded_par** Parity bit for double bit error detection	NA	NA	NA	NA
		[10:0]	**irq_wdg** Timer value for interrupt request watchdog timer • 11'h000: 584µs • 11'h001: 584µs×2 = 1.168ms • 11'h002: 584µs×3 = 1.752ms • … • 11'h7FF: 584µs×2048 = 1.196s	RW	RW	0x00	0x00

Table 23. AGC Plausibility Configuration: Address 0x0F FTP; 0x4F SRB

Address FTP	Address SRB	Bits	Function	Access FTP	Access SRB	Reset SRB	Default FTP
0x0F	0x4F	[15:12]	**Ecc**: Parity word for error correction	NA	NA	NA	NA
		[11]	**ded_par**: Parity bit for double bit error detection	NA	NA	NA	NA
		[10]	**RFU**: Read as X	RW	RW	0	0
		[9:5]	**agc_plause_uthresh**: ACG upper threshold for plausibility check (absolute gain value). **Note**:The upper threshold must be configured above the lower threshold. • 5'h0: gain code 2 • 5'h1: gain code 5 • 5'h2: gain code 8 • 5'h3: gain code 11 • … • 5'h1D: gain code 89 • 5'h1E: gain code 92 • 5'h1F: gain code 95			0x1F	0x00
		[4:0]	**agc_plause_lthresh:** ACG lower threshold for plausibility check (absolute gain value) **Note**: The lower threshold must be configured below the upper threshold. • 5'h0: gain code 2 • 5'h1: gain code 5 • 5'h2: gain code 8 • 5'h3: gain code 11 • … • 5'h1D: gain code 89 • 5'h1E: gain code 92 • 5'h1F: gain code 95			0x00	0x00

Table 24. Customer Identification: Address Register 0x18 FTP

Address FTP	Address SRB	Bits	Function	Access FTP	Access SRB	Reset SRB	Default FTP
0x18	*NO SRB*	[15:12]	**Ecc:** Parity word for error correction	NA	NA	NA	NA
		[11]	**ded_par:** Parity bit for double bit error detection	NA	NA	NA	NA
		[10:8]	**RFU:** Read as X	RO	NA	NA	NA
		[7:0]	**customer_id:** Customer Programmable Identification: Used by the customer to program a customer specific identification code.	RW	NA	NA	0x0

Table 25. Product Identifier: Address 0x19 FTP

Address FTP	Address SRB	Bits	Function	Access FTP	Access SRB	Reset SRB	Default FTP
0x19	*NO SRB*	[15:12]	**Ecc:** Parity word for error correction	NA	NA	NA	NA
		[11]	**ded_par:** Parity bit for double bit error detection	NA	NA	NA	NA
		[10:8]	**RFU:** Read as X	RO	NA	NA	NA
		[7:0]	**product_id:** Renesas traceability: Product Identification Factory traceability code		NA	NA	0x19

3.2.2. SFR (Special Functions Register)

Table 26. Interrupt Clear 1: Address 0x68 SFR

Address FTP SRB	Bits	Function	Access FTP SRB	Reset SRB
0x68	[15:12]	NA	NA	NA
	[11]	NA	NA	NA
	[10]	**Overvoltage:** Over-voltage detection • 0b0: no action • 0b1: reset irstate	WO	0
	[9]	**Undervoltage:** Under-voltage detection • 0b0: no action • 0b1: reset irstate		0
	[8]	**Temperature alarm:** Clears the temperature alarm. • 0b0: no action • 0b1: reset irstate		0
	[7]	**data_access_fail:** I2C data access timeout • 0b0: no action • 0b1: reset irstate		0
	[6]	**i2c_protocol_fail:** I2C interface serial received data fail / data access aborted • 0b0: no action • 0b1: reset irstate		0
	[5]	**srb_ded SRB:** Double bit error detection / SFR testmode register 1/2 parity bit error detection • 0b0: no action • 0b1: reset irstate		0
	[4]	**srb_sed SRB:** Single bit error detection and correction 0b0: no action 0b1: reset irstate		0
	[3]	**nvm_ded NVM:** Double bit error detection • 0b0: no action • 0b1: reset irstate		0
	[2]	**nvm_sed NVM:** Single bit error detection and correction • 0b0: no action • 0b1: reset irstate		0
	[1]	**lc_osc_freq_fail:** LC oscillator frequency range check (see limits register 0x07, 0x08, and 0x0A) • 0b0: no action • 0b1: reset irstate		0
	[0]	**lc_osc_stuck:** LC oscillator stuck check • 0b0: no action • 0b1: reset irstate		0

Table 27. Interrupt Clear 2: Address 0x69 SFR

Address FTP SRB	Bits	Function	Access FTP SRB	Reset SRB
0x69	[15:12]	NA	NA	NA
	[11]	NA	NA	NA
	[10]	**csn_data_overvoltage:** IRQN_CSN/DATA pin over-voltage • 0b0: no action • 0b1: reset irstate	WO	0
	[9]	**vdda_undervoltage**: VDDA under-voltage • 0b0: no action • 0b1: reset irstate		0
	[8]	**apb_transfer_fail:** APB bus transfer failure. Any write access of read-only register are rejected by the APB-bus control, and they are flagged. (see sys_conf2.6) • 0b0: no action • 0b1: reset irstate		0
	[7]	**irqn watchdog:** Timeout of interrupt watchdog • 0b0: no action • 0b1: reset irstate		0
	[6]	**seal_ring_break:** Seal ring break • 0b0: no action • 0b1: reset irstate		0
	[5]	**fsm_err:** Internal Finit State Machine (FSM) error detected • 0b0: no action • 0b1: reset irstate		0
	[4]	**outbuf_vcm_fail:** VCM voltage level of SINP/N or COSP/N not equal to VDD/2 • 0b0: no action • 0b1: reset irstate		0
	[3]	**outbuf_current_fail:** Output buffer SINP, SINN, COSP, COSN exceeds limit. • 0b0: no action • 0b1: reset irstate		0
	[2]	**vddd_overvoltage:** Digital power supply over-voltage • 0b0: no action • 0b1: reset irstate		0
	[1]	**agc_err:** AGC control loop error - boundary code reached, amplitude NOT in range • 0b0: no action • 0b1: reset irstate		0
	[0]	**rx_fail:** Receiver path fail: short to GND / VDD or R1P/N or R2P/N open, LPF fail or short between R1 and R2 • 0b0: no action • 0b1: reset irstate		0

Table 28. Interrupt Clear 3: Address 0x6A SFR

Address FTP SRB	Bits	Function	Access FTP SRB	Reset SRB
0x6A	[15:12]	NA	NA	NA
	[11]	NA	NA	NA
	[10:2]	**RFU:** NA	NA	NA
	[1]	**tx_coil_fail:** Transmitter coil short to GND / VDD or open • 0b0: no action • 0b1: reset irstate	WO	0
	[0]	**bist_err:** Failure in BIST for the test mechanism • 0b0: no action • 0b1: reset irstate		0

Table 29. Interrupt State 1: Address 0x6B SFR

Address FTP SRB	Bits	Function	Access FTP SRB	Reset SRB
0x6B	[15:12]	NA	NA	NA
	[11]	NA	NA	NA
	[10]	**Overvoltage:** Over-voltage detection • 0b0: idle • 0b1: interrupt request	RO	0
	[9]	**Undervoltage:** Under-voltage detection • 0b0: idle • 0b1: interrupt request		0
	[8]	**Temperature alarm:** Error flag indicating that the temperature exceeds the T_{OVT_WARN} (warning threshold) defined in the *IP2550 Datasheet* document. The output buffers are switched off automatically to reduce the power consumption after exceeding the warning threshold. • 0b0: idle • 0b1: interrupt request		0
	[7]	**data_access_fail:** I2C data access timeout • 0b0: idle • 0b1: interrupt request		0
	[6]	**i2c_protocol_fail:** I2C interface serial received data fail / data access aborted • 0b0: idle • 0b1: interrupt request		0
	[5]	**srb_ded:** SRB double bit error detection / SFR testmode register 1/2 parity bit error detection • 0b0: idle • 0b1: interrupt request		0
	[4]	**srb_sed:** SRB single bit error detection and correction • 0b0: idle • 0b1: interrupt request		0
	[3]	**nvm_ded:** NVM double bit error detection • 0b0: idle • 0b1: interrupt request		0
	[2]	**nvm_sed:** NVM single bit error detection and correction • 0b0: idle • 0b1: interrupt request		0
	[1]	**lc_osc_freq_fail:** LC oscillator frequency range check (see limits register 0x07, 0x08, 0x0A) • 0b0: idle • 0b1: interrupt request		0
	[0]	**lc_osc_stuck:** LC oscillator stuck check • 0b0: idle • 0b1: interrupt request		0

Table 30. Interrupt State 2: Address 0x6C SFR

Address FTP SRB	Bits	Function	Access FTP SRB	Reset SRB
0x6C	[15:12]	NA	NA	NA
	[11]	NA	NA	NA
	[10]	**csn_data_overvoltage:** IRQN_CSN/DATA pin over-voltage • 0b0: idle • 0b1: interrupt request	RO	0x000
	[9]	**vdda_undervoltage:** VDDA under-voltage • 0b0: idle • 0b1: interrupt request		0
	[8]	**apb_transfer_fail:** APB bus transfer failure. Any write access of read-only register are rejected by the APB-bus control, and are flagged (see sys_conf2.6) • 0b0: idle • 0b1: interrupt request		0
	[7]	**irqn watchdog:** Timeout of interrupt watchdog • 0b0: idle • 0b1: interrupt request		0
	[6]	**seal_ring_break:** Seal ring break • 0b0: idle • 0b1: interrupt request		0
	[5]	**fsm_err:** Internal Finit State Machine (FSM) error detected • 0b0: idle • 0b1: interrupt request		0
	[4]	**outbuf_vcm_fail:** VCM voltage level of SINP/N or COSP/N not equal to VDD/2. • 0b0: idle • 0b1: interrupt request **Note**: This bit is set during programming over the analog output pins.		0
	[3]	**outbuf_current_fail:** Output buffer SINP, SINN, COSP, COSN exceeds the limit. • 0b0: idle • 0b1: interrupt request		0
	[2]	**vddd_overvoltage:** Digital power supply over-voltage • 0b0: idle • 0b1: interrupt request		0
	[1]	**agc_err:** AGC control loop error - boundary code reached, amplitude NOT in range • 0b0: idle • 0b1: interrupt request		0
	[0]	**rx_fail:** Receiver path fail: short to GND / VDD or R1P/N or R2P/N open, LPF fail or short between R1 and R2 • 0b0: idle • 0b1: interrupt request		0

Table 31. Interrupt State 3: Address 0x6D SFR

Address FTP SRB	Bits	Function	Access FTP SRB	Reset SRB
0x6D	[15:12]	NA	NA	NA
	[11]	NA	NA	NA
	[10:3]	**RFU:** Read as X	RO	0
	[2]	**dig_osc_fail:** Digital oscillator fail • 0b0: idle • 0b1: interrupt request	RO	0
	[1]	**tx_coil_fail:** Transmitter coil short to GND / VDD or open • 0b0: idle • 0b1: interrupt request		0
	[0]	**bist_err:** Failure in BIST for the test mechanism • 0b0: idle • 0b1: interrupt request		0

Table 32. Transmitter Counter State: Address 0x6E SFR

Address FTP SRB	Bits	Function	Access FTP SRB	Reset SRB
0x6E	[15:12]	NA	NA	NA
	[11]	NA	NA	NA
	[10:0]	**transmitter_cntr:** Excitation frequency counter • 0x000: 0 excitation cycle • 0x001: 1 excitation cycle • 0x002: 2 excitation cycles • … • 0x7FF: 2047 excitation cycles	RO	0x000

The transmitter frequency can be calculated from the transmitter_cntr value.

For a time base value of AF hex (default) in register 0x48, the frequency is calculated as:

$$F_{TX} = transmitter\ cntr * 20000$$

Example for a timebase of 50µs (0x08 = AF_{hex}):

$$F_{TX} = 200 * 20000 = 4\ MHz$$

Table 33. FTP ECC State: Address 0x70 SFR

Address FTP SRB	Bits	Function	Access FTP SRB	Reset SRB
0x70	[15:11]	RFU: Read as X	RO	0x0
	[10]	**ded_flag:** Double error detection flag • 0b0: Idle • 0b1: Asserted		0x000
	[9]	**sec_flag**: Single Error Correction flag • 0b0: idle • 0b1: Asserted		
	[8]	**sec_id8**: Renesas internal use		
	[7]	**sec_id4**: Renesas internal use		
	[6]	**sec_id2**: Renesas internal use		
	[5]	**sec_id1**: Renesas internal use		
	[4:0]	**ftp_fail_addr:** Last failed FTP address with SEC or DED detection		

Table 34. Product Identifier Version: Address 0x73 SFR

Address FTP SRB	Bits	Function	Access FTP SRB	Reset SRB
0x73	[15:8]	**RFU:** Read as X	RO	0x00
	[7:4]	**prod_version:** Renesas traceability: product version • 0x00: A silicon		0x00
	[3:0]	**prod_sub_version:** Renesas traceability: product subversion • 0x00: Engineering version • 0x01: Engineering version • 0x02: Production version		0x00

Table 35. AGC_OBSERVATION: Address 0x78 SFR

Address FTP SRB	Bits	Function	Access FTP SRB	Reset SRB
0x78	[15:11]	NA	RO	0x00
	[10:7]	**RFU:** Read as X		0
	[6:0]	**agc_gain_stage:** Current AGC code value		0x00

The current AGC code value indicates the signal strength at the inputs.

Table 36. DBIST_STS: Address 0x79 SFR

Address SFR	Bits	Function	Access SFR	Reset SFR
0x79	[15:11]	NA	RO	0x00
	[10:9]	**RFU:** Read as X		0
	[8]	**dbist_secded_chks_fail:** Fail in the SECDED checks		0
	[7]	**dbist_irst_chks_fail:** Fail in the IRSTATE registers		0
	[6]	**dbist_lc_chks_fail:** Fail in the LC oscillator stuck and frequency measurement mechanisms		0
	[5]	**dbist_agc_chks_fail:** Fail in the AGC window comparators (debouncers and synchronization logic)		0
	[4]	**dbist_fsm_chks_fail:** Fail in the internal FSM error detection mechanims		0
	[3]	**dbist_ilm_chks_fail:** Fail in the current limitation window comparators (debouncers and synchronization logic)		0
	[2]	**dbist_vcm_chks_fail:** Fail in the VCM window comparators (debouncers and synchronization logic)		0
	[1]	**dbist_grp2_chks_fail:** Fails in the second group of signals tested in parallel: undervolgate_vdd, undervolgate_vdda		0
	[0]	**dbist_grp1_chks_fail:** Fails in the first group of signals tested in parallel: rx_fail,overvoltage_vdd, overvoltage_vddd, temperature, tx_fail,agc_err, dig_osc_fail,data_access_fail		0

Table 37. External SM for Checking I2C CRC: Address 0x7F SFR

Address FTP SRB	Bits	Function	Access FTP SRB	Reset SRB
0x7F	[15:11]	NA	RO	0x00
	[10]	**Programmed:** Set to 1 upon first write access; sticky write		0
	[9:0]	**ext_sm_self_test:** Perform the self test of the I2C CRC externally using following steps: 1. Read the default value. The IC provides an incorrect CRC that must be detected by the controller. 2. Write a value to 0x7 [9:0] with an incorrect CRC. The 0x6B [6] flag is raised and must be checked. Depending on the settings, this flag can be cleared. 3. Write any value to 0x7 [9:0] with the correct CRC and check the flag at 0x6B [6]. 4. Read the modified value at 0x7F and verify that the IC provides the correct CRC.	RW	0x2A3

4. Glossary

Term	Description
FTP	Few Times Programmable
FSM	Finite State Machine
I^2C	Inter-Integrated Circuit; serial two-wire data bus
LSB	Least Significant Bit
MSB	Most Significant Bit
MSN	Most Significant Nibble
NVM	Nonvolatile Memory
POR	Power-On Reset
RFU	Reserved for Future Use
SRB	Shadow Register Bank

5. Revision History

Revision Date	Description of Change
Dec 15, 25	Updated description for external SM for checking I2C CRC
Nov.28.24	Minor corrections to address values.
Apr.26.24	Pin numbering updated for system_protocol. Some typos corrected
Mar.20.24	Values for 7E and 7F are updated in registers 4, 44, 6, and 46.
Jul.7.21	Updated descriptions for AGC, Register 0x7A and corrections in formating
May.5.21	Updated descriptions for sensor programming, I2C addresses, FTP/SRB, and flags.
Jan.19.21	Initial release

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