NEC

User's Manual

IMAPCAR2-300-USB board

Hardware

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Table of Contents

1 Introduction

The IMAPCAR2-300-USB board is a development board of the IMAPCAR2-300.

1.1 Numeric Notation

- Binary : XXXXB. That means, for example, “10B”is 2 in decimal
- Decimal : XXXX
- Hexadecimal : 0xXXXX or XXXXH. That means, for example, “0x10” and “10H” is 16 in decimal

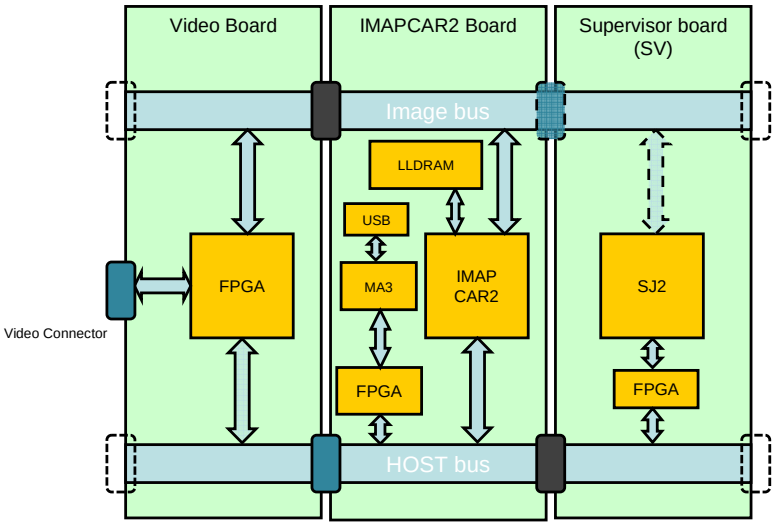
2 Specification

GPU	IMAPCAR2-300	NEC Electronics : Vision Controller IMAPCAR2-300： Operation clock：108MHz LLDRAM : Operation clock：216MHz
CPU	V850E/MA3	NEC Electronics : Microcontroller UPD70F3134AYGJ-UEN-A Operation clock: 80MHz
Memory	LLDRAM	NEC Electronics: uPD48288236 or equivalent 288M-bit: 1M words x 36 bits x 8 banks
	Serial FLASH	ST: M25P80 (8Mbit SPI)
Peripherals	FPGA(S841PLD01)	Xilinx SPARTAN3A: XC3S700AFGG400 (400pin FBGA) Fixed input clock IMAPCAR2 input clock: 27MHz V850E/MA3 input clock: 8MHz USB input clock: 30MHz Optional clock 8pin-DIP3.3V type SV Board/ MA3 Basarbita MISC DIPSW:SW1[0:7] LED[0:7] Configuration ROM:XCF04S (1 unit)
	USB	+ NEC Electronics：USB2.0 Function Controller : uPD720122GC-9EU (100pin-TQFP)
Others	Switches	PowerRESET (Reconfiguration of FPGA) HardRESET (system reset) INTP[0:2] S841PLD01-DIPSW: 8bit(SW1) + 4bit(SW4) JTAG Wire setting (SW2) IMAPCAR2 MODE setting (SW3,5,6,7)
	LED	S841PLD01-LED:8bit FAILDC COFIG-DONE PowerON
	Debugging	No break debugging I/F Flash writer I/F N-Wire I/F
Power Supply		+12V (± 2V), 1A or more (when a single board is used)

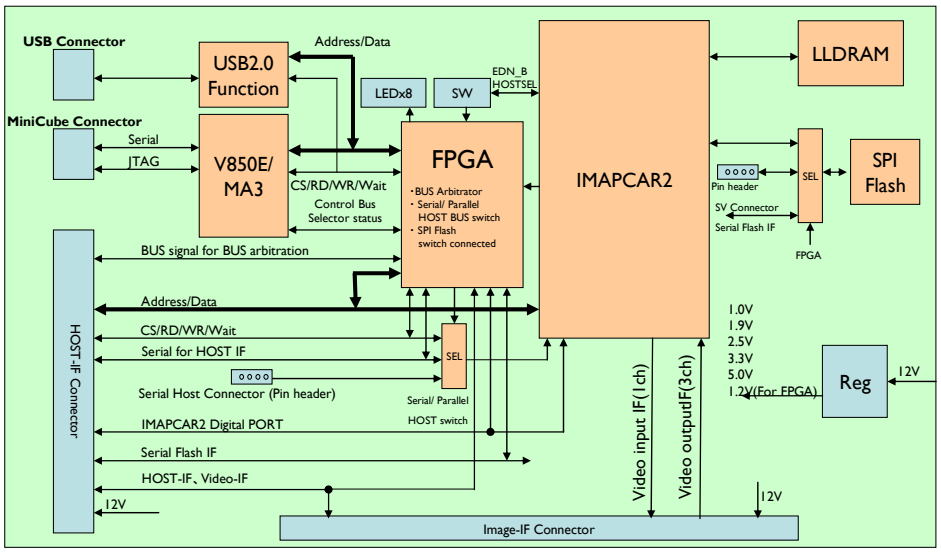
3 Composition

3.1 Block diagram

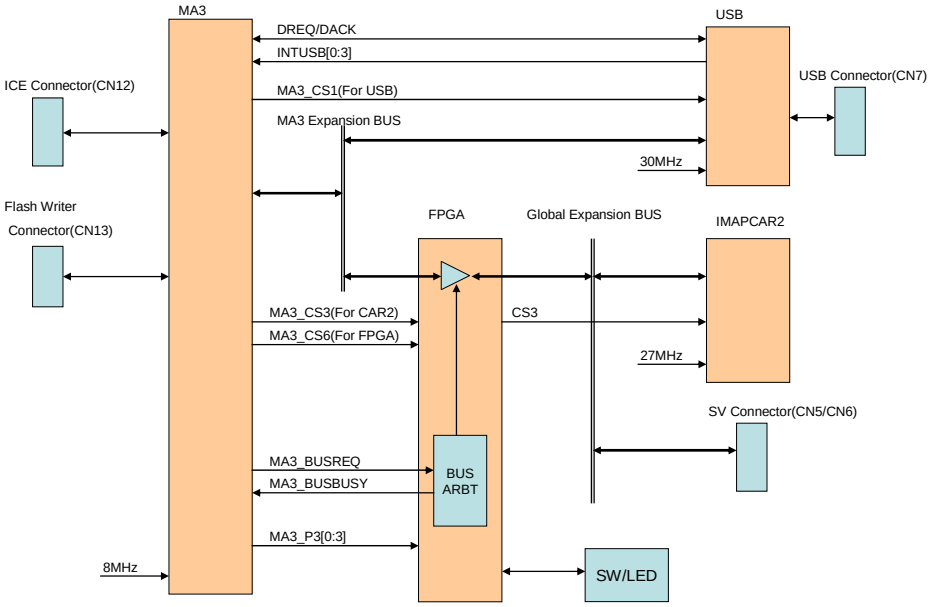
The system configuration chart and the detailed block diagram of the IMAPCAR2-300-USB board are defined in the figures below:



IMAPCAR2-300-USB Board: System Configuration Chart



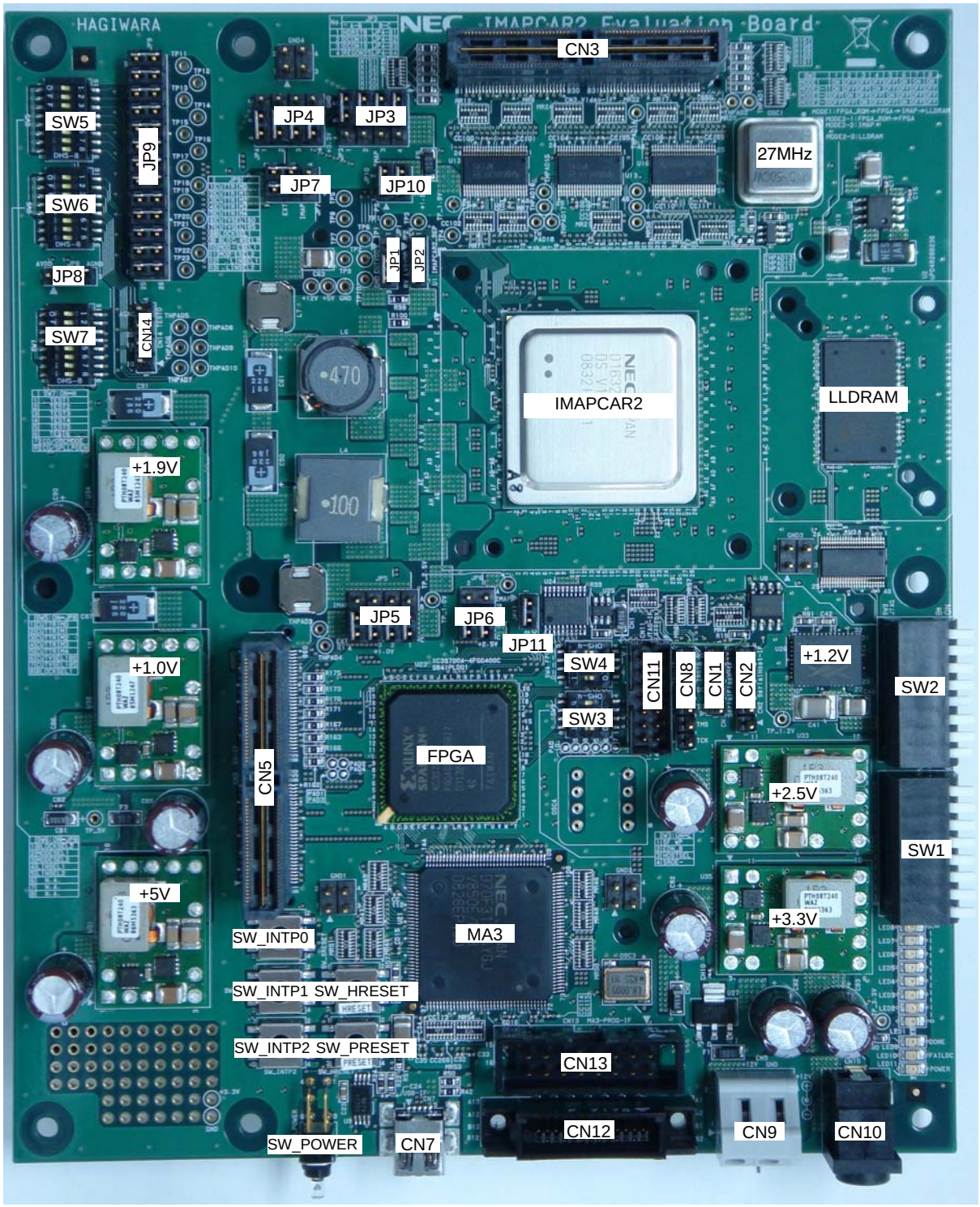
IMAPCAR2-300-USB Board: Detailed Block Diagram



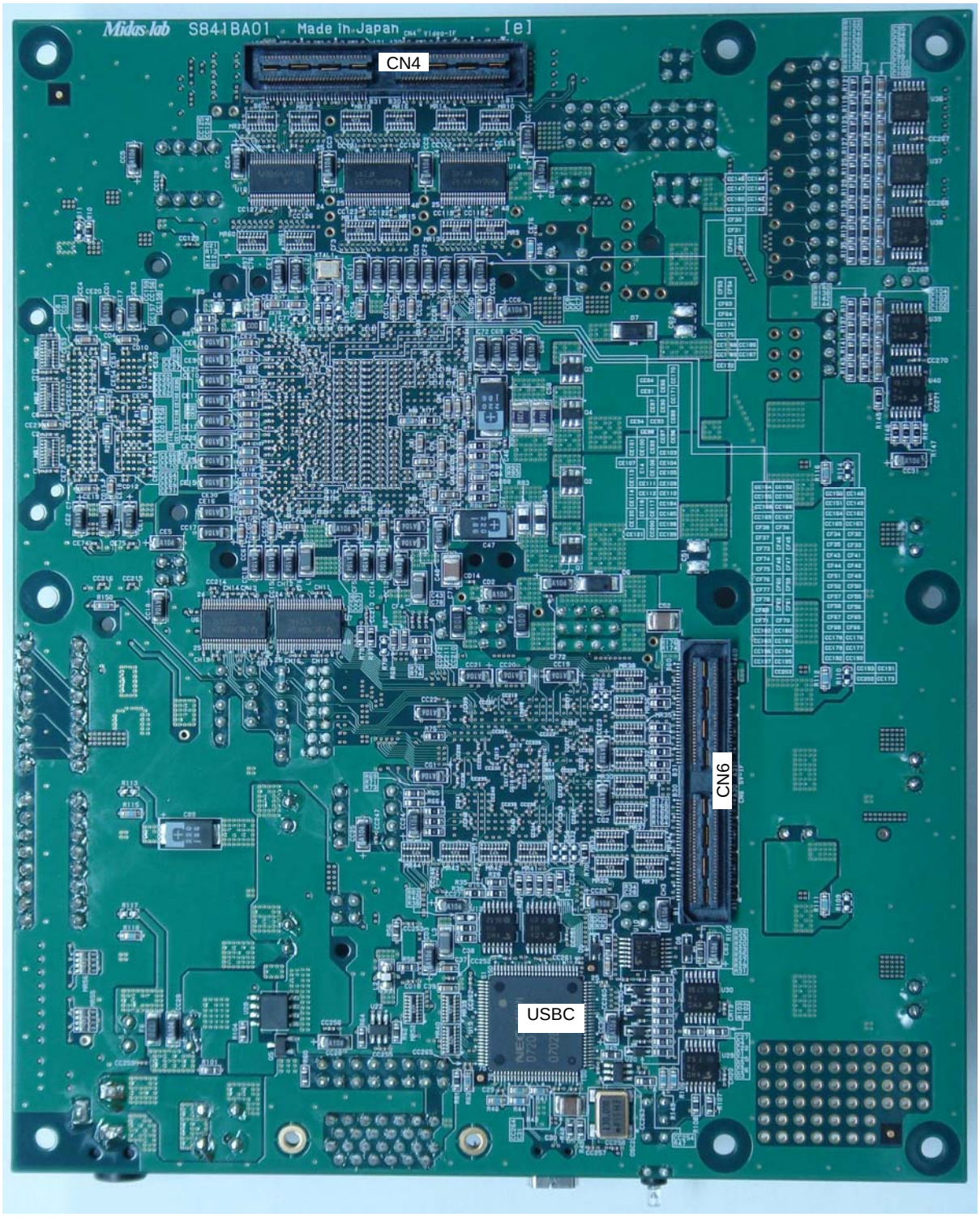
Peripheral Block Diagram

3.2 General view

The figure below shows the general view of the PCB



Top view



Back view

4 Description of the board

4.1 Switches

4.1.1 Power On Switch

At each press on the SW-Power switch, the board will be switched on or switched off. When the board is on, a LED will be on to indicate the board status.

4.1.2 Power Reset Switch

This switch will generate a power-on reset. That means that the entire system including the boards connected to the IMAPCAR2-300-USB is reset by using this Power Reset switch (SW-PRESET) and the FPGA will be reconfigured.

4.1.3 Hard Reset switch

The entire system including the boards connected to the IMAPCAR2-300-USB is reset by using this Hard Reset switch (SW-HRRESET)

4.1.4 Interrupt and switch (SW INTP0, 1, 2)

The SW-INTP0, 1, 2 are connected to the pins INTP[0:2] of IMAPCAR2. By pushing one of these switches, an external interrupt in the IMAPCAR2 device will be generated

4.1.5 SW1

These LEDs represent the status of some device output pins. Three different output configurations are supported by the board. The configuration is defined by a FPGA internal register (LED_SEL, fore more details, see the chapter 5.4.2 FPGA (S841PLD01))

- (1)SW_SEL=0

SW Number	Function	Details	Initialization
1	IMAPCAR2 input port 0	IMPCAR2 PORT00	OFF
2		IMPCAR2 PORT01	OFF
3		IMPCAR2 PORT02	OFF
4		IMPCAR2 PORT03	OFF
5		IMPCAR2 PORT04	OFF
6		IMPCAR2 PORT05	OFF
7		IMPCAR2 PORT06	OFF
8		IMPCAR2 PORT07	OFF

SW1(SW_SEL=0)

- (2)SW_SEL=1

SW Number	Function	Details	Initialization
1	IMAPCAR2 input port 1	Not used	OFF
2		Not used	OFF
3		Not used	OFF
4		IMPCAR2 PORT11	OFF
5		IMPCAR2 PORT12.	OFF
6		IMPCAR2 PORT13.	OFF
7		IMPCAR2 PORT14.	OFF
8		IMPCAR2 PORT15.	OFF

SW1(SW_SEL=1)

- (3)SW_SEL=2

SW Number	Function	Details	Initialization
1	V850E/MA3 input port	V850E/MA3 P32	OFF
2		V850E/MA3 P32	OFF
3		Unconnected (High-Z)	OFF
4		Unconnected (High-Z)	OFF
5		Unconnected (High-Z)	OFF
6		Unconnected (High-Z)	OFF
7		Unconnected (High-Z)	OFF
8		Unconnected (High-Z)	OFF

SW1(SW_SEL=2)

- (4)SW_SEL=3(default)

SW Number	Function	Details	Initialization
1		Unconnected (High-Z)	OFF
2		Unconnected (High-Z)	OFF
3		Unconnected (High-Z)	OFF
4		Unconnected (High-Z)	OFF
5		Unconnected (High-Z)	OFF
6		Unconnected (High-Z)	OFF
7		Unconnected (High-Z)	OFF
8		Unconnected (High-Z)	OFF

SW1(SW_SEL=3)

（1), (2) & (3) Please configure the port of IMAPCAR2 and V850E/MA3 as in input mode.

4.1.6 SW2

JTAG Debug switches: Please do not set it other than the following mode.

MODE1 : FPGA_ROM -> FPGA -> IMAPCAR2 -> LLDRAM
MODE2-1(default) : FPGA_ROM -> FPGA
MODE2-2 : IMAPCAR2
MODE2-3 : LLDRAM

SW number	1	2	3	4	5	6	7	8
MODE1	ON	OFF	OFF	OFF	OFF	ON	ON	ON
MODE2-1	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF
MODE2-2	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF
MODE2-3	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF

4.1.7 SW3

Board system configuration.

SW number	Signal name	Function	Initialization
1	SF_WP	Serial Flash memory write protection configuration. ON : Write Protection is activated OFF : Write Protection is NOT activated	OFF
2	EDN_B	EDN_B IMAPCAR2 configuration ON: Big Indian. OFF : Little Indian	OFF
3	HOSTSEL	HOSTSEL IMAPCAR2 Configuration. ON : Serial I/F between the Host and IMAPCAR2 OFF : Parallel I/F between the Host and IMAPCAR2	OFF
4	SROE-	Video output buffer ON : Video output enable OFF : Video output disable	ON

SW3

4.1.8 SW4

FPGA configuration switches. Please do not switch the SW4-4 (SW4-4 = OFF)

SW number	Function	Details	Initialization
1	Serial Flash configuration	SW4[2:1]=OFF,OFF：SPI Flash connected to IMAPCAR2 SW4[2:1]=OFF,ON：SPI Flash connected to microcontroller SW4[2:1]=ON,OFF：SPI Flash connected to CN1 connected SW4[2:1]=ON,ON ：Not connected	OFF
2			OFF
3	Serial HOST configuration	ON : serial host connected to microcontroller OFF: serial host connected to CN2 connector	ON
4	Board test	ON: Do not use this configuration OFF: The ordinary mode	OFF

SW4

4.1.9 SW5

System configuration: IMAPCAR2 Input pin configuration

SW Number	Signal Name	Function	Initialization
1	CUTTRIM0	ON : JP8 setting level (see chapter 4.2.5 for more details about JP8) OFF : Low level	Undefined
2	CUTTRIM1		Undefined
3	CUTTRIM2		Undefined
4	CUTTRIM3		Undefined
5	CUTTRIM4		Undefined
6	CUTVSEL180		Undefined
7	CUTVSEL185		Undefined
8	BLOCKSEL1		Undefined

SW5

4.1.10 SW6

System configuration: IMAPCAR2 Input pin configuration

SW Number	Signal Name	Function	Initialization
1	BLOCKSEL2	ON : JP8 setting level (see chapter 4.2.5 for more details about JP8) OFF : Low level	Undefined
2	MODESEL1		Undefined
3	MODESEL2		Undefined
4	LINSEL1		Undefined
5	LINSEL2		Undefined
6	N.A.		Undefined
7	N.A.		Undefined
8	N.A.		Undefined

SW6

4.1.11 SW7

System configuration: IMAPCAR2 Input pin configuration

SW Number	Signal Name	Function	Initialization
1	TEST1	ON : High Level OFF : Low level。	Undefined
2	TEST2		Undefined
3	TEST3		Undefined
4	TEST4		Undefined
5	TEST5		Undefined
6	TEST6		Undefined
7	IC0/OSCMODE		Undefined
8	IC0/SPLLPDEN		Undefined

SW7

4.2 Jumper setting

This chapter describes the different jumper configurations.

4.2.1 JP1

IMAPCAR2 CUTVDD Configuration.

Please do not change the factory setting

Jumper pin	Selection	Factory setting
1-2	TP1	Open
2-3	GND	Connected

JP1

4.2.2 JP2

IMAPCAR2 LVSDD Configuration.

Please do not change the factory setting

Jumper pin	Selection	Factory setting
1-2	JP2	Open
2-3	REGVDD	Connected

JP2

4.2.3 JP3, JP4

IMAPCAR2 pin configuration

Please do not change the factory setting

	IMAPCAR2 Pin Name	JP3		Factory setting
		A-B	B-C	
1	HDRSTB	HDRSTB(SV)	JP4-B1	B-C
2	DCON10	DCON10(SV)	JP4-B2	B-C
3	DCON19	DCON19(SV)	JP4-B3	B-C
4	REGON25	REGON25(SV)	JP4-B4	B-C

	JP4		Factory setting
	A-B	B-C	
1	+3.3V	GND	A-B
2	+3.3V	GND	A-B
3	+3.3V	GND	A-B
4	+3.3V	GND	A-B

4.2.4 JP6, JP6, JP7

IMAPCAR2 Power supply configuration

Please do not change the factory setting

JP5

	JP5(1.0V)		Factory setting
	A-B	B-C	
1	IMAP-REG	EXT	A-B
2	IMAP-REG	EXT	A-B
3	IMAP-REG	EXT	A-B
4	IMAP-REG	EXT	A-B

JP6,JP7

	JP6(2.5V)		Factory setting
	A-B	B-C	
1	IMAP-REG	EXT	A-B
2	IMAP-REG	EXT	A-B

	JP7(1.9V)		Factory setting
	A-B	B-C	
1	IMAP-REG	EXT	A-B
4	IMAP-REG	EXT	A-B

4.2.5 JP8

IMAPCAR2 Configuration: SW5 level definition

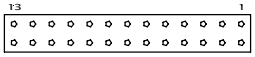
Please do not change the factory setting

Jumper pin	Selection	Factory setting
1-2	+3.3V	Open
2-3	GND	Connected

4.2.6 JP9

IMAPCAR2 Configuration: SW5 is connected to IMAPCAR2

Please do not change the factory setting (all jumpers are connected)



	IMAPCAR PIN NAME
1	CUTTRIM0
2	CUTTRIM1
3	CUTTRIM2
4	CUTTRIM3
5	CUTTRIM4
6	CUTVSEL180
7	CUTVSEL185
8	BLOCKSEL1
9	BLOCKSEL2
10	MODESEL1
11	MODESEL2
12	LINSEL1
13	LINSEL2

4.2.7 JP10

Setting to measure the current consumption of LLVDD19

Please do not change the factory setting (1-2 connected / 3-4 connected)

Jumper pin	Selection	Factory Setting
1-2	+1.9V	Connected
3-4	+1.9V	Connected

4.2.8 JP11

IMAPCAR2 Configuration: FAILDC configuration

Please do not change the factory setting (FAILDC connected to the SV board).

Jumper pin	Selection	Factory Setting
1-2	FAILDC -> SV board	Connected

4.3 LED

4.3.1 S841PLD01 LED (LED1-8)

These LEDs represent the status of some device output pins. Three different output configurations are supported by the board. The configuration is defined by a FPGA internal register (LED_SEL, fore more details, see the chapter 5.4.2 FPGA (S841PLD01))

(1)LED_SEL=0

LED No.	Description
LED1	IMAPCAR2 PORT00 pin value
LED2	IMAPCAR2 PORT01 pin value
LED3	IMAPCAR2 PORT02 pin value
LED4	IMAPCAR2 PORT03 pin value
LED5	IMAPCAR2 PORT04 pin value
LED6	IMAPCAR2 PORT05 pin value
LED7	IMAPCAR2 PORT06 pin value
LED8	IMAPCAR2 PORT07 pin value。

(2)LED_SEL=1

LED No.	Description
LED1	Not used
LED2	Not used
LED3	Not used
LED4	IMAPCAR2 PORT11 pin value。
LED5	IMAPCAR2 PORT12 pin value。
LED6	IMAPCAR2 PORT13 pin value。
LED7	IMAPCAR2 PORT14 pin value。
LED8	IMAPCAR2 PORT15 pin value。

(3)LED_SEL=2

LED No.	Description
LED1	IMAPCAR2 PORT00 pin value
LED2	IMAPCAR2 PORT01 pin value
LED3	IMAPCAR2 PORT02 pin value
LED4	IMAPCAR2 PORT30 pin value
LED5	IMAPCAR2 PORT31 pin value
LED6	IMAPCAR2 BREAK pin value
LED7	IMAPCAR2 COUNTEND pin value。
LED8	IMAPCAR2 ERROROUT pin value 。

4.3.2 LED09 (DONE)

The LED09 (DONE) indicates the FPGA configuration status.
This LED is on when the FPGA is correctly configured.

4.3.3 LED10 (FAILDC)

The LED10 (FAILDC) indicates the IMAPCAR2 FAILDC status.
If an issue is detected on the IMAPCAR2 power supply, this LED is ON

4.3.4 LED11 (POWER)

The LED11 (POWER) indicates the status of power supply.
This LED is on when the board is correctly supplied

4.4 Connectors

This chapter describes the specification of each connector.

4.4.1 Serial Flash Memory (CN1)

4.4.2 Serial Flash Memory (CN1)

Connector to access to M25P80 (serial Flash).

Switch must be set as defined in the chapter "4.1.8SW4").

Supplier : Omron

Model : XG8V-0431

pin No.	I/O	端子名
1	O	FLSI
2	I	FLSO
3	I	FLCKB
4	―	GND

CN1

4.4.3 Serial Host Interface (CN2)

Connector to access to the serial of Host IF of IMAPCAR2.

SW must be set as defined in the chapter. "4.1.7SW3, 4.1.8SW4".

Supplier: Omron

Model: XG8V-0531

pin No.	I/O	端子名
1	I	HSCKB
2	I	HSI
3	O	HSO
4	I	HSCS
5	―	GND

CN2

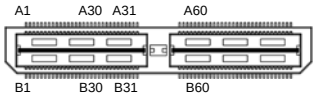
4.4.4 Video Board Interface (CN3, CN4)

Video Board connectors

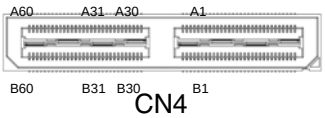
Supplier : Samtec

Model : CN3: QTH-060-05-L-D-A

CN4: QSH-060-01-L-D-A A



CN3



CN4

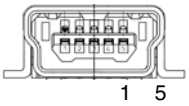
	Signal name	IO	B		A	IO	Signal Name		Discriptpion
SV⇔CAR2⇔VIO	PIO_VIO[4]	IO	1	N	1	IO	UART0_RX/PIO_VIO[0]	SV⇔CAR2⇔VIO	UART0 RX/General Purpose IO
	ODDEVENI[0]	I	2	P	2	IO	UART0_TX/PIO_VIO[2]	SV⇔CAR2⇔VIO	UART0 TX/General Purpose IO
	HSYNCI_B[0]	I	3	N	3	I	VSYNCI_B[0]		
	SCLKI[0]	I	4	P	4	I	SCLK2I[0]		
	ch0_idata[0]/SRI[0]	I	5	N	5	I	ch0_idata[1]/SRI[1]		
	ch0_idata[2]/SRI[2]	I	6	P	6	I	ch0_idata[3]/SRI[3]		CAR2 VIN Ch0
CAR2←VIO	ch0_idata[4]/SRI[4]	I	7	N	7	I	ch0_idata[5]/SRI[5]	CAR2←VIO	
	ch0_idata[6]/SRI[6]	I	8	P	8	I	ch0_idata[7]/SRI[7]		
	ch0_idata[8]/SRI[8]	I	9	N	9	I	ch0_idata[9]/SRI[9]		
	ch0_idata[10]/SRI[10]	I	10	P	10	I	ch0_idata[11]/SRI[11]		
	ch0_idata[12]	I	11	N	11	I	ch0_idata[13]		CAR2 VIN Ch0(Preliminary)(*1)
	ch0_idata[14]	I	12	P	12	I	ch0_idata[15]		
SV⇔CAR2⇔VIO	PIO_VIO[5]	IO	13	N	13	IO	UART1_RX/PIO_VIO[1]	SV⇔CAR2⇔VIO	UART1 RX/General Purpose IO
	ODDEVENI[1]	I	14	P	14	IO	UART1_TX/PIO_VIO[3]	SV⇔CAR2⇔VIO	UART1 TX/General Purpose IO
	HSYNCI_B[1]	I	15	N	15	I	VSYNCI_B[1]		
	SCLKI[1]	I	16	P	16	I	SCLK2I[1]		
	ch1_idata[0]/SRI[12]	I	17	N	17	I	ch1_idata[1]/SRI[13]		
	ch1_idata[2]/SRI[14]	I	18	P	18	I	ch1_idata[3]/SRI[15]		CAR2 VIN ch1
CAR2←VIO	ch1_idata[4]/SRI[16]	I	19	N	19	I	ch1_idata[5]/SRI[17]	CAR2←VIO	
	ch1_idata[6]/SRI[18]	I	20	P	20	I	ch1_idata[7]/SRI[19]		
	ch1_idata[8]/SRI[20]	I	21	N	21	I	ch1_idata[9]/SRI[21]		
	ch1_idata[10]/SRI[22]	I	22	P	22	I	ch1_idata[11]/SRI[23]		
	ch1_idata[12]	I	23	N	23	I	ch1_idata[13]		CAR2 VIN ch1(Preliminary)(*1)
	ch1_idata[14]	I	24	P	24	I	ch1_idata[15]		
SV⇔CAR2⇔VIO	PIO_VIO[10]	IO	25	N	25	IO	UART2_RX/PIO_VIO[6]	SV⇔CAR2⇔VIO	UART2 RX//General Purpose IO
	ODDEVENI[2]	I	26	P	26	IO	UART2_TX/PIO_VIO[8]	SV⇔CAR2⇔VIO	UART2 TX//General Purpose IO
	HSYNCI_B[2]	I	27	N	27	I	VSYNCI_B[2]		
CAR2←VIO	SCLKI[2]	I	28	P	28	I	SCLK2I[2]	CAR2←VIO	CAR2 VIN ch2
	ch2_idata[0]/SRI[24]	I	29	N	29	I	ch2_idata[1]/SRI[25]		
	ch2_idata[2]/SRI[26]	I	30	P	30	I	ch2_idata[3]/SRI[27]		
	ch2_idata[4]/SRI[28]	I	31	N	31	I	ch2_idata[5]/SRI[29]		
	ch2_idata[6]/SRI[30]	I	32	P	32	I	ch2_idata[7]/SRI[31]		
CAR2←VIO	ch2_idata[8]/SRI[32]	I	33	N	33	I	ch2_idata[9]/SRI[33]	CAR2←VIO	CAR2 VIN ch2
	ch2_idata[10]/SRI[34]	I	34	P	34	I	ch2_idata[11]/SRI[35]		
	ch2_idata[12]/SRI[36]	I	35	N	35	I	ch2_idata[13]/SRI[37]		
	ch2_idata[14]/SRI[38]	I	36	P	36	I	ch2_idata[15]/SRI[39]		
SV⇔CAR2⇔VIO	PIO_VIO[11]	IO	37	N	37	IO	UART3_RX/PIO_VIO[7]	SV⇔CAR2⇔VIO	UART3 RX/General Purpose IO
	ODDEVENO0	O	38	P	38	IO	UART3_TX/PIO_VIO[9]	SV⇔CAR2⇔VIO	UART3 TX/General Purpose IO
	HSYNCO0_B	O	39	N	39	O	VSYNCO0_B		CAR2 VOUT common
	SCLKO0	O	40	P	40	O	SCLK2O0		
	ch0_odata[0]/SRO[0]	O	41	N	41	O	ch0_odata[1]/SRO[1]		
	ch0_odata[2]/SRO[2]	O	42	P	42	O	ch0_odata[3]/SRO[3]		CAR2 VOUT ch0
	ch0_odata[4]/SRO[4]	O	43	N	43	O	ch0_odata[5]/SRO[5]		
	ch0_odata[6]/SRO[6]	O	44	P	44	O	ch0_odata[7]/SRO[7]		
CAR2→VIO	ch1_odata[0]/SRO[8]	O	45	N	45	O	ch1_odata[1]/SRO[9]	CAR2→VIO	
	ch1_odata[2]/SRO[10]	O	46	P	46	O	ch1_odata[3]/SRO[11]		CAR2 VOUT ch1
	ch1_odata[4]/SRO[12]	O	47	N	47	O	ch1_odata[5]/SRO[13]		
	ch1_odata[6]/SRO[14]	O	48	P	48	O	ch1_odata[7]/SRO[15]		
	ch2_odata[0]/SRO[16]	O	49	N	49	O	ch2_odata[1]/SRO[17]		
	ch2_odata[2]/SRO[18]	O	50	P	50	O	ch2_odata[3]/SRO[19]		CAR2 VOUT ch2
	ch2_odata[4]/SRO[20]	O	51	N	51	O	ch2_odata[5]/SRO[21]		
	ch2_odata[6]/SRO[22]	O	52	P	52	O	ch2_odata[7]/SRO[23]		
SV⇔CAR2⇔VIO	CSI0_RX/PIO_VIO[13]	IO	53	N	53	IO	CSI1_RX/PIO_VIO[12]	SV⇔CAR2⇔VIO	CSI1 RX/General Purpose IO
SV⇔CAR2⇔VIO	CSI0_TX/PIO_VIO[15]	IO	54	P	54	IO	CSI1_TX/PIO_VIO[14]	SV⇔CAR2⇔VIO	CSI1 TX/General Purpose IO
SV⇔CAR2⇔VIO	CSI0_CLK/PIO_VIO[17]	IO	55	N	55	IO	VSYNC (PIO_VIO[16])	SV⇔CAR2⇔VIO	
SV⇔CAR2⇔VIO	I2C_SDA (PIO_VIO[19])	IO	56	P	56	IO	PIO_VIO[18]	SV⇔CAR2⇔VIO	
SV⇔CAR2⇔VIO	I2C_SCL (PIO_VIO[21])	IO	57	N	57	IO	PIO_VIO[20]	SV⇔CAR2⇔VIO	
CAR2→VIO	12V	–	58	P	58	–	12V	CAR2→VIO	Power
	12V	–	59	N	59	–	12V		
–	–	–	60	P	60	–	12V		

CN3,CN4

4.4.5 USB Interface (CN7)

Suppliers : Molex

Model : 67503-1020



Pin No.	Pin Name
1	VBUS
2	D-
3	D+
4	ID
5	GND

CN7

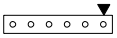
4.4.6 JTAG Interface (CN8, CN11)

CN8 is the JTAG connector.

Switch must be set as defined in the chapter "4.1.6SW2" reference.

Supplier : Omron

Model : XG8V-0631



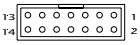
pin No.	I/O	Pin Name
1	I	TCK
2	I	TMS
3	I	TDI
4	O	TDO
5	I	TRSTB
6	—	GND

CN8

CN11 is a program designed for FPGA made by Xilinx. <CN8>

Supplier : Molex

Model : 87831-1420



pin No.	Pin Name	I/O	pin No.	Pin Name	I/O
1	GND	-	2	Vref(+3.3V)	O
3	GND	-	4	TMS	I
5	GND	-	6	TCK	I
7	GND	-	8	TDO	O
9	GND	-	10	TDI	I
11	GND	-	12	N.C.	-
13	GND	-	14	N.C.	-

CN11

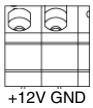
4.4.7 Power Interface (CN9, CN10)

Connector for power supply

<CN9>

Supplier : Sato Parts

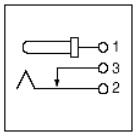
Model : ML-950-2



CN9

<CN10>

Panel mount power socket, 2,1 mm 5A 12V



pin	信号名
1	+12V
2	GND
3	N.C.

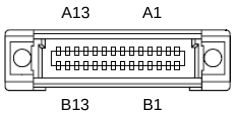
CN10

4.4.8 V850E/MA3 N-Wire Interface

V850E/MA3 N-Wire connector

Supplier : KEL

Model : 8830E-026-170S-F



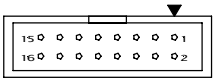
pin No.	Pin Name	I/O	pin No.	Pin Name	I/O
A1	GND	-	B1	GND	-
A2	GND	-	B2	GND	-
A3	GND	-	B3	GND	-
A4	GND	-	B4	GND	-
A5	GND	-	B5	GND	-
A6	GND	-	B6	GND	-
A7	DDI	I	B7	GND	-
A8	DCK	I	B8	GND	-
A9	DMS	I	B9	GND	-
A10	DDO	O	B10	GND	-
A11	DRST-	I	B11	N.C.	-
A12	N.C.	-	B12	N.C.	-
A13	MODE1	I	B13	Vref(+3.3V)	-

4.4.9 V850E/MA3 Flash Programmer Interface

V850E/MA Flash Programmer Interface

Supplier : Omron

Model : XG4C-1631



pin No.	Pin Name	I/O	pin No.	Pin Name	I/O
1	GND	-	2	RESET-	I
3	SO0	O	4	+3.3V	-
5	SI0	I	6	N.C.	-
7	SCK0	IO	8	PCM0	IO
9	N.C.	-	10	N.C.	-
11	+2.5V	-	12	MODE0	I
13	N.C.	-	14	MODE1	I
15	N.C.	-	16	N.C.	-

CN13

4.4.10 TESTO Interface

IMAPCAR2 TESTO pin monitor connector.

Supplier : Omron

Model : XG8V-0431

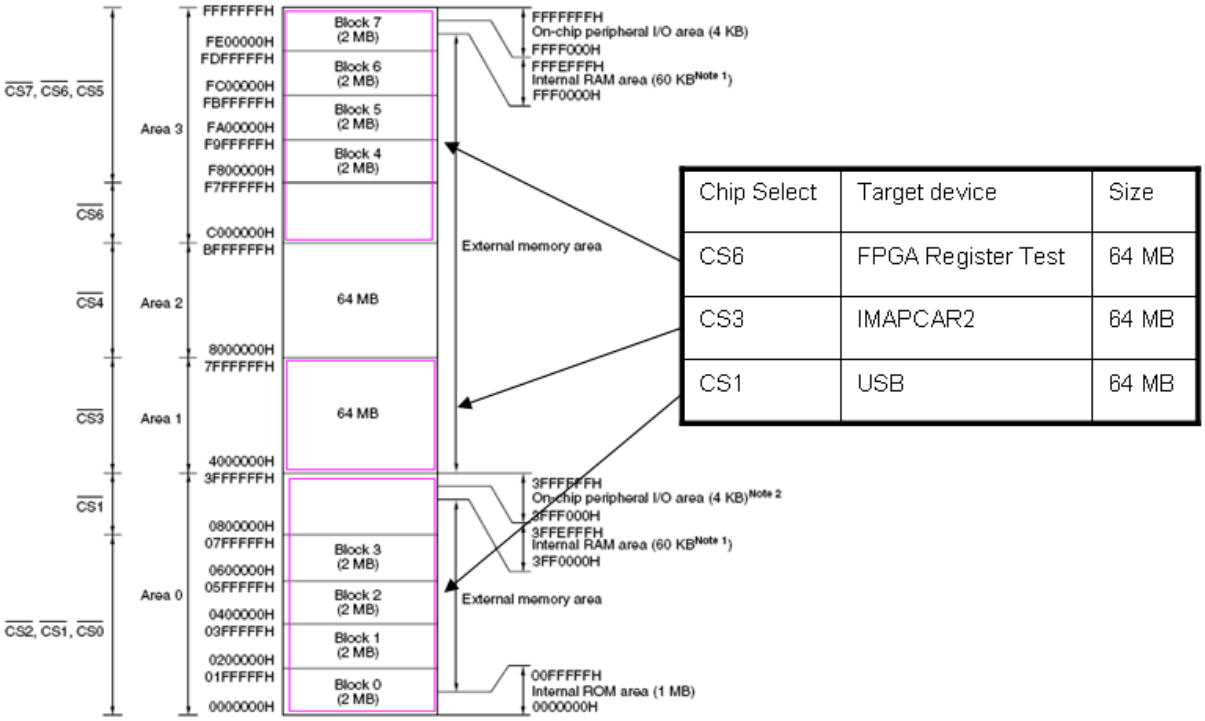
pin No.	I/O	Pin Name
1	O	TESTO10
2	O	TESTO19
3	O	TESTO25
4	—	GND

CN14

5 Hardware components

5.1 V850E/MA3 Memory map

5.1.1 Full Memory map



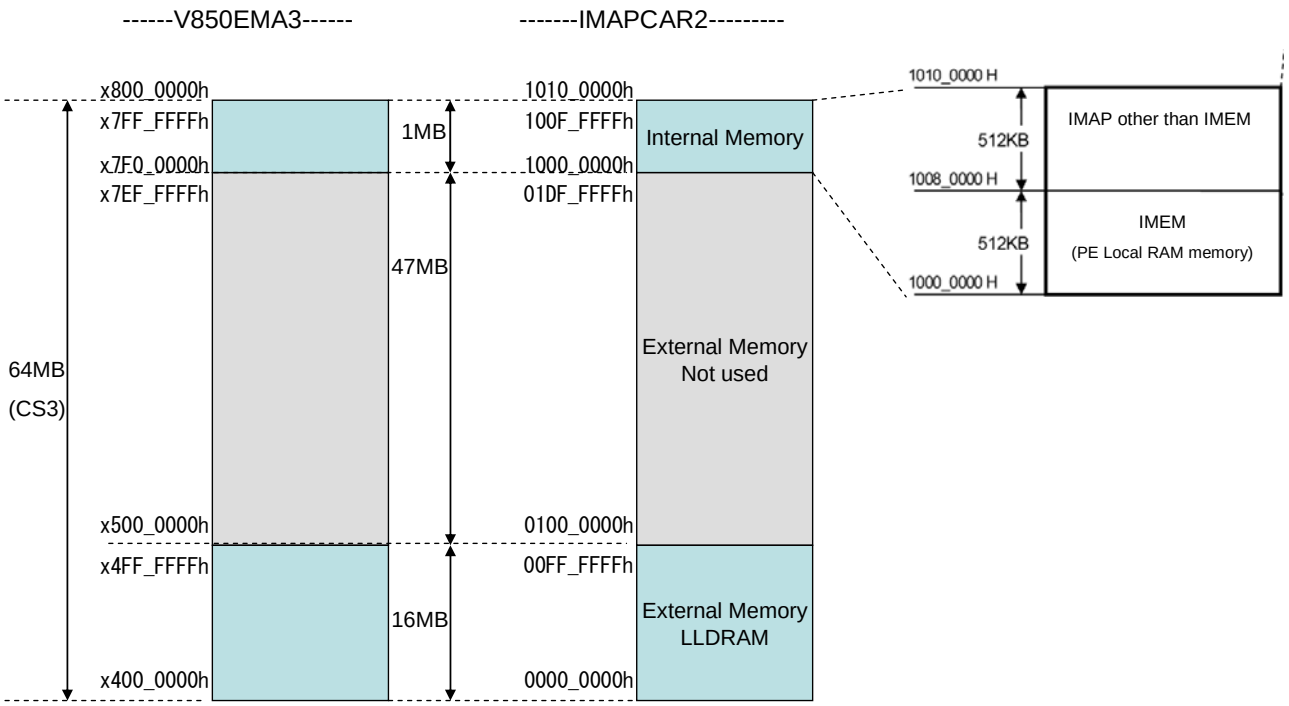
Chip Select	Target device	Size
CS6	FPGA Register Test	64 MB
CS3	IMAPCAR2	64 MB
CS1	USB	64 MB

5.1.2 Memory block: CS1 area (USB Function Controller)

USB2.0 Function Controller: uPD720122

For details, please refer to the user's manual device

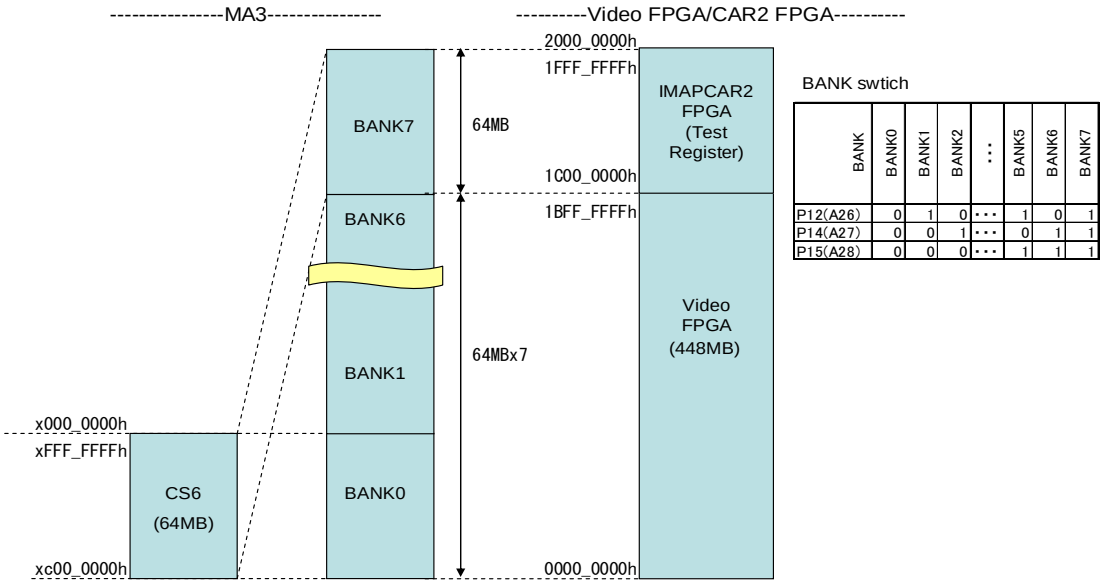
5.1.3 Memory block: CS3 area (IMAPCAR2)



Comments:

- When V850E.MA3 access between 0x7F0_0000 and 0x7FF_FFFF, the FPGA will automatically convert the IMAPCAR2 address between 0x1000_0000 to 0x100F_FFFF
- The expanded address (P15,P14 and P12 = A28:26) is not used
- 32MB of LLDRAM bas been implemented on the board. V850E/MA3 can access only to 16MB of LLDRAM

5.1.4 Memory block: CS6 area (FPGA and Video Board)



BANK	BANK0	BANK1	BANK2	・・・	BANK5	BANK6	BANK7
P12(A26)	0	1	0	・・・	1	0	1
P14(A27)	0	0	1	・・・	0	1	1
P15(A28)	0	0	0	・・・	1	1	1

5.2 V850E/MA3 : Specific Registers

Define the recommended values of the V850E/MA3 registers (these values depend on the operation frequency please set them correctly).

You need to initialize the following registers.

Register Name	Address	Value
VSWC	0xFFFFF06e	0x24
CKC	0xFFFFF822	0x03

External memory controller: The following registers need to be initialized to access correctly to the external memory

Register Name	Address	Value
PMCAL	0xFFFFF040	0xFFFF
PMCAH	0xFFFFF042	0xFFFF
PMCDL	0xFFFFF044	0xFFFF
PMCCS	0xFFFFF048	0x4A
PMCCT	0xFFFFF04A	0x30
PMCCM	0xFFFFF04C	0x01
PMCBD	0xFFFFF052	0x01
PMC0	0xFFFFF440	0x10
PFC0	0xFFFFF460	0x10
P1	0xFFFFF402	0xFF
PM1	0xFFFFF422	0xCB
PMC2	0xFFFFF444	0x10
PFC2	0xFFFFF464	0x10
P5	0xFFFFF40A	0x00
PM5	0xFFFFF42A	0xFE
CSC0	0xFFFFF060	0x2010
CSC1	0xFFFFF062	0x2010
BCT0	0xFFFFF480	0x8080
BCT1	0xFFFFF482	0x0800
DWC0	0xFFFFF484	0x1747
DWC1	0xFFFFF486	0x7177
ASC	0xFFFFF48A	0xCF33
BCC	0xFFFFF488	0xDF73

5.3 Other devices

5.3.1 LLDRAM

Supplier : NEC Electronics

Part Number : uPD48288236

5.3.2 USB Controller

Supplier : NEC Electronics

Part Number : uPD720122

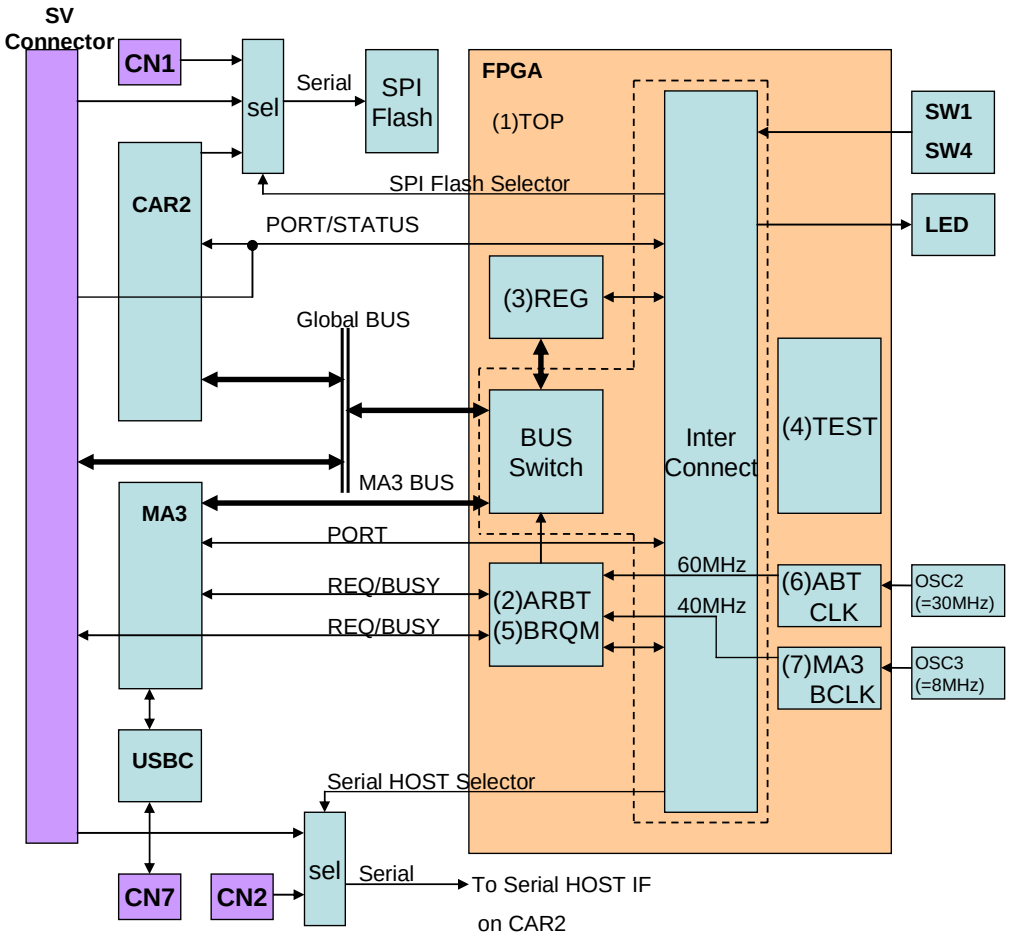
5.3.3 FPGA (S841PLD01)

Supplier : Xilinx

Part Number : Spartan-3A series (XC3S700AFG400)

5.4 FPGA (S841PLD01) Interface

5.4.1 Internal Block Diagram



5.4.2 FPGA (S841PLD01) register

The following registers are mapped in the CS6 of the V850E/MA3 (see chapter 5.1.4 for more details)

MA3 Address(CS6)	R/W	Register Name
0F00_0000h	R	Register version 1。
0F00_0002h	R	Register version 2
0F00_0010h	R/W	Test register 0
0F00_0012h	R/W	Test register 1
0F00_0014h	R/W	Test register 3
0F00_0040h	R/W	BUSREQ Control Register
0F00_0100h-1FFh	R/W	Test module area. SW4 [4] is valid in ON. (Confidential)

5.4.2.1 Version register 1 (Address: 0F00_0000h; 16-bit access only)

Bit Number	Name	R/W	Function	Initial Value
[7:0]	MIN_VER	R	Minor Version	3
[15:8]	MEJ_VER	R	Major Version	2

5.4.2.2 Version register 2 (Address: 0F00_0002h; 16-bit access only)

Bit Number	Name	R/W	Function	Initial Value
[15:0]	Custum_VER	R	Customer versions	0

5.4.2.3 Test Register 0 (Address: 0F00_0010h; 16-bit access only)

Bit Number	Name	R/W	Function	Initial Value
[1:0]	LED_SEL	R/W	LED function code (see the chapter "4.3.1S841PLD01-LED (LED1-8)") for more details.）	0
[7:2]	Reserved	R/W	Set to 0	0
[9:8]	SW_SEL	R/W	SW1 Function register (see the chapter "4.1.5 SW1" more details.）	3
[15:10]	Reserved	R/W	‘Set to 0	0

5.4.2.4 Test Register 1 (Address: 0F00_0012h; 16-bit access only)

Bit Number	Name	R/W	Function	Initial Value
[15:0]	WORK0	R/W	Multipurpose work register	0

5.4.2.5 Test Register 2 (Address: 0F00_0014h; 16-bit access only)

Bit Number	Name	R/W	Function	Initial Value
[15:0]	WORK1	R/W	Multipurpose work register	0

5.4.2.6 BUSREQ (Address: 0F00_0040h; 16-bit access only)

Bit Number	Name	R/W	Function	Initial Value
[3:0]	BRQ_CR	R/W	BUSREQ release counter. SV number	3
[14:3]	Reserved	R	Fixed to 0。	0
[15]	Reserved	R	Fixed to 0	0

5.4.3 FPGA (S841PLD01) pin assignment

PIN No.	XC3S700AFG400 Pin Name	BANK	IOB TYPE	I/O	Pin Name	Note
B1	IO_L02P_3	3	I/O	I	MA3_A[1]	V850E/MA3 Address
C1	IO_L03P_3	3	I/O	I	MA3_A[2]	V850E/MA3 Address
C2	IO_L02N_3	3	I/O	I	MA3_A[3]	V850E/MA3 Address
D1	IO_L05P_3	3	I/O	I	MA3_A[4]	V850E/MA3 Address
D2	IO_L03N_3	3	I/O	I	MA3_A[5]	V850E/MA3 Address
D3	IO_L01N_3	3	I/O	I	MA3_A[6]	V850E/MA3 Address
D4	IO_L01P_3	3	I/O	I	MA3_A[7]	V850E/MA3 Address
E1	IO_L05N_3	3	I/O	I	MA3_A[8]	V850E/MA3 Address
E3	IO_L10P_3	3	I/O	I	MA3_A[9]	V850E/MA3 Address
F1	IO_L13P_3	3	I/O	I	MA3_A[10]	V850E/MA3 Address
F2	IO_L10N_3	3	I/O	I	MA3_A[11]	V850E/MA3 Address
F3	IO_L09P_3	3	I/O	I	MA3_A[12]	V850E/MA3 Address
F4	IO_L06P_3	3	I/O	I	MA3_A[13]	V850E/MA3 Address
G1	IO_L13N_3/VREF_3	3	VREF	I	MA3_A[14]	V850E/MA3 Address
G3	IO_L12P_3	3	I/O	I	MA3_A[15]	V850E/MA3 Address
G4	IO_L09N_3	3	I/O	I	MA3_A[16]	V850E/MA3 Address
G5	IO_L06N_3	3	I/O	I	MA3_A[17]	V850E/MA3 Address
G6	IP_L04N_3/VREF_3	3	VREF		N.C.	
G7	IP_L04P_3	3	INPUT		N.C.	
H2	IO_L12N_3	3	I/O	I	MA3_A[18]	V850E/MA3 Address
H3	IO_L14N_3	3	I/O	I	MA3_A[19]	V850E/MA3 Address
H4	IO_L08N_3	3	I/O	I	MA3_A[20]	V850E/MA3 Address
H6	IO_L08P_3	3	I/O	I	MA3_A[21]	V850E/MA3 Address
H7	IP_3	3	INPUT		N.C.	
J1	IO_L17P_3/LHCLK0	3	LHCLK	I	MA3_A[22]	V850E/MA3 Address
J2	IO_L16N_3	3	I/O	I	MA3_A[23]	V850E/MA3 Address
J3	IO_L16P_3	3	I/O	I	MA3_A[24]	V850E/MA3 Address
J4	IO_L14P_3	3	I/O	I	MA3_A[25]	V850E/MA3 Address
J5	IO_L07N_3	3	I/O		N.C.	
J6	IO_L07P_3	3	I/O		N.C.	
J7	IP_L11N_3/VREF_3	3	VREF		N.C.	
J8	IP_L11P_3	3	INPUT		N.C.	
K2	IO_L17N_3/LHCLK1	3	LHCLK	I	MA3_A[26]	V850E/MA3 Address
K3	IO_L18P_3/LHCLK2	3	LHCLK	I	MA3_A[27]	V850E/MA3 Address
K4	IO_L20P_3/LHCLK4	3	LHCLK	I	MA3_A[28]	V850E/MA3 Address
K5	IP_L19N_3	3	INPUT		N.C.	
K6	IP_L19P_3	3	INPUT		N.C.	
K7	IP_L15N_3	3	INPUT		N.C.	
K8	IP_L15P_3	3	INPUT		N.C.	
L1	IO_L21P_3/TRDY2/LHCLK6	3	LHCLK	I/O	MA3_D[0]	V850E/MA3Data
L3	IO_L18N_3/IRDY2/LHCLK3	3	LHCLK	I/O	MA3_D[1]	V850E/MA3Data
L5	IO_L20N_3/LHCLK5	3	LHCLK	I/O	MA3_D[2]	V850E/MA3Data
L6	IP_L23N_3	3	INPUT		N.C.	
L7	IP_L23P_3	3	INPUT		N.C.	
M1	IO_L21N_3/LHCLK7	3	LHCLK	I/O	MA3_D[3]	V850E/MA3Data
M2	IO_L22P_3/VREF_3	3	VREF	I/O	MA3_D[4]	V850E/MA3Data
M3	IO_L22N_3	3	I/O	I/O	MA3_D[5]	V850E/MA3Data
M4	IO_L24P_3	3	I/O	I/O	MA3_D[6]	V850E/MA3Data
M5	IO_L24N_3	3	I/O		N.C.	
M6	IP_L31P_3	3	INPUT		N.C.	
M7	IP_L27N_3	3	INPUT		N.C.	

M8	IP_L27P_3	3	INPUT		N.C.	
N1	IO_L25P_3	3	I/O	I/O	MA3_D[7]	V850E/MA3Data
N2	IO_L25N_3	3	I/O	I/O	MA3_D[8]	V850E/MA3Data
N3	IO_L26P_3	3	I/O	I/O	MA3_D[9]	V850E/MA3Data
N4	IO_L26N_3	3	I/O	I/O	MA3_D[10]	V850E/MA3Data
N6	IP_L35N_3	3	INPUT		N.C.	
N7	IP_L31N_3	3	INPUT		N.C.	
P1	IO_L28P_3	3	I/O	I/O	MA3_D[11]	V850E/MA3Data
P3	IO_L29P_3	3	I/O	I/O	MA3_D[12]	V850E/MA3Data
P4	IO_L29N_3	3	I/O	I/O	MA3_D[13]	V850E/MA3Data
P5	IP_L35P_3	3	INPUT		N.C.	
P6	IP_L39P_3	3	INPUT		N.C.	
P7	IP_L39N_3/VREF_3	3	VREF		N.C.	
R1	IO_L28N_3	3	I/O	I/O	MA3_D[14]	V850E/MA3Data
R2	IO_L30P_3	3	I/O	I/O	MA3_D[15]	V850E/MA3Data
R3	IO_L30N_3	3	I/O	I	MA3_CSB3	MA3 CS3
R4	IO_L33N_3	3	I/O	I	MA3_CSB6	MA3 CS6
R5	IO_L36P_3	3	I/O		N.C.	
T1	IO_L32P_3/VREF_3	3	VREF	I	MA3_RDB	MA3 RD
T2	IO_L32N_3	3	I/O	I	MA3_WRB	MA3 WR
T3	IO_L33P_3	3	I/O	O	MA3_WAITB	MA3 WAIT
T4	IO_L36N_3	3	I/O	I	MA3_BUSSTAT	
U1	IO_L34P_3	3	I/O	I	MA3_BURST	
U3	IO_L34N_3	3	I/O	I	MA3_BUSRESET	
V1	IO_L37P_3	3	I/O	I	MA3_BUSREQ	MA3 bus request(P50)
V2	IO_L37N_3	3	I/O	O	MA3_BUSBUSY	MA3 bus acknowledge(P51)
W1	IO_L38P_3	3	I/O		N.C.	
W2	IO_L38N_3	3	I/O		N.C.	
Y2	IO_L02N_2/CSO_B	2	DUAL	I	P13_UC0	V850E/MA port(P30)
Y3	IO_L03P_2	2	I/O	I	P13_UC1	V850E/MA port (P31)
W4	IO_L03N_2	2	I/O	I	P13_UC2	V850E/MA port (P32)
Y4	IO_L08P_2	2	I/O	I	P13_UC3	V850E/MA port (P33)
U5	IO_L05N_2	2	I/O		N.C.	
V5	IO_L05P_2	2	I/O		N.C.	
Y5	IO_L08N_2	2	I/O		N.C.	
T6	IO_L04P_2	2	I/O	I	SW1_[1]	PUP is required
U6	IO_L06N_2	2	I/O	I	SW1_[2]	PUP is required
V6	IO_L09P_2/VS1	2	DUAL	I	SW1_[3]	PUP is required
W6	IO_L09N_2/VS0	2	DUAL	I	SW1_[4]	PUP is required
Y6	IO_L10P_2	2	I/O		N.C.	
R7	IO_L04N_2	2	I/O	I	SW1_[5]	PUP is required
T7	IO_L06P_2	2	I/O	I	SW1_[6]	PUP is required
U7	IO_L07N_2/VS2	2	DUAL	I	SW1_[7]	PUP is required
V7	IO_L12P_2/D7	2	DUAL	I	SW1_[8]	PUP is required
Y7	IO_L10N_2	2	I/O		N.C.	
P8	IP_2/VREF_2	2	VREF		N.C.	
R8	IP_2	2	INPUT		N.C.	
T8	IO_L07P_2/RDWR_B	2	DUAL	O	C2_RESET_	CAR2 RESET OUT
V8	IO_L13P_2	2	I/O	I	SRESET_	SW RESET IN
W8	IO_L12N_2/D6	2	DUAL		N.C.	
N9	IP_2/VREF_2	2	VREF		N.C.	
P9	IP_2	2	INPUT		N.C.	
T9	IO_L11P_2	2	I/O		N.C.	
U9	IO_L11N_2	2	I/O		N.C.	

V9	IO_L13N_2	2	I/O		N.C.	
W9	IO_L15P_2/GCLK12	2	GCLK		N.C.	
Y9	IO_L15N_2/GCLK13	2	GCLK		N.C.	
P10	IP_2/VREF_2	2	VREF		N.C.	
R10	IP_2	2	INPUT		N.C.	
T10	IO_L14N_2/D4	2	DUAL		N.C.	
U10	IO_L14P_2/D5	2	DUAL		N.C.	
V10	IO_L16P_2/GCLK14	2	GCLK	I	CLKCPLD	MA3 X1(8MHz)
W10	IO_L16N_2/GCLK15	2	GCLK		N.C.	
P11	IP_2/VREF_2	2	VREF		N.C.	
T11	IP_2	2	INPUT		N.C.	
U11	IO_L18P_2/GCLK2	2	GCLK		N.C.	
V11	IO_L17N_2/GCLK1	2	GCLK		N.C.	
Y11	IO_L17P_2/GCLK0	2	GCLK	I	CLK1_C	CAR2 X2(27MHz)
N12	IP_2/VREF_2	2	VREF		N.C.	
P12	IP_2	2	INPUT		N.C.	
R12	IO_L19N_2	2	I/O	I	EDNB	CAR2 Indian
T12	IO_L19P_2	2	I/O	I	HOSTSEL	CAR2 HOSTSEL
V12	IO_L18N_2/GCLK3	2	GCLK		N.C.	
W12	IO_L20N_2/MOSI/CSI_B	2	DUAL		N.C.	
Y12	IO_L20P_2	2	I/O		N.C.	
P13	IP_2	2	INPUT		N.C.	
R13	IO_L23N_2	2	I/O		N.C.	
T13	IO_L23P_2	2	I/O		N.C.	
U13	IO_L22P_2/AWAKE	2	PWRMGMT		N.C.	
W13	IO_L21N_2	2	I/O		N.C.	
Y13	IO_L21P_2	2	I/O		N.C.	
R14	IP_2/VREF_2	2	VREF		N.C.	
T14	IO_L25N_2	2	I/O	O	LED[0]	LED1
V14	IO_L25P_2	2	I/O	O	LED[1]	LED2
W14	IO_L24N_2/D3	2	DUAL	O	LED[2]	LED3
T15	IO_L27N_2	2	I/O	O	LED[3]	LED4
U15	IO_L27P_2	2	I/O	O	LED[4]	LED5
V15	IO_L26N_2/D1	2	DUAL	O	LED[5]	LED6
Y15	IO_L26P_2/D2	2	DUAL	O	LED[6]	LED7
U16	IO_L29N_2	2	I/O	O	LED[7]	LED8
V16	IO_L29P_2	2	I/O	I	SW4_[1]	PUP is required
W16	IO_L28N_2	2	I/O	I	SW4_[2]	PUP is required
Y16	IO_L28P_2	2	I/O	I	SW4_[3]	PUP is required
U17	IO_L31N_2	2	I/O	I	SW4_[4]	PUP is required
V17	IO_L31P_2	2	I/O		N.C.	
Y17	IO_L30P_2	2	I/O		N.C.	
Y18	IO_L30N_2	2	I/O		N.C.	
B19	IO_L38N_1/A25	1	DUAL	I	SV_WAITB[0]	CAR2 WAITB[0]
B20	IO_L38P_1/A24	1	DUAL	I	SV_WAITB[1]	CAR2 WAITB[1]
C19	IO_L37N_1/A23	1	DUAL	I	SV_WAITB[2]	CAR2 WAITB[2]
C20	IO_L37P_1/A22	1	DUAL	I	YOBI_BUSBUSY	Preliminary
D18	IO_L34N_1	1	I/O	I	YOBI_BUSREQ	Preliminary
D20	IO_L34P_1	1	I/O	I	SV_BUSREQ	SV bus request
E18	IO_L33P_1	1	I/O	O	SV_BUSBUSY	SV bus acknowledge
E19	IO_L32N_1	1	I/O	I	SV_BUSRESET_	Reset
E20	IO_L32P_1	1	I/O	I	SV_BUSSTAT	Reserved
F16	IO_L36N_1/A21	1	DUAL	I	SV_BURST	
F17	IO_L33N_1	1	I/O	I/O	PORT0_[0]	CAR2 PORT[00]

F18	IO_L30N_1/A19	1	DUAL	I/O	PORT0_[1]	CAR2 PORT[01]
F19	IO_L29N_1/A17	1	DUAL		N.C.	
F20	IO_L29P_1/A16	1	DUAL		N.C.	
G14	IP_L39N_1	1	INPUT		N.C.	
G15	IP_L39P_1/VREF_1	1	VREF		N.C.	
G16	IO_L36P_1/A20	1	DUAL	I/O	PORT0_[2]	CAR2 PORT[02]
G17	IO_L30P_1/A18	1	DUAL	I/O	PORT0_[3]	CAR2 PORT[03]
G18	IO_L28P_1	1	I/O	I/O	PORT0_[4]	CAR2 PORT[04]
G20	IO_L26N_1/A15	1	DUAL	I/O	PORT0_[5]	CAR2 PORT[05]
H14	IP_L35N_1	1	INPUT		N.C.	
H15	IP_L35P_1	1	INPUT		N.C.	
H17	IO_L28N_1	1	I/O	I/O	PORT0_[6]	CAR2 PORT[06]
H18	IO_L25N_1/A13	1	DUAL	I/O	PORT0_[7]	CAR2 PORT[07]
H19	IO_L25P_1/A12	1	DUAL	I/O	FLSCKB	CAR2 PORT[08]
H20	IO_L26P_1/A14	1	DUAL	I/O	FLSI	CAR2 PORT[09]
J13	IP_L31N_1	1	INPUT		N.C.	
J14	IP_L31P_1/VREF_1	1	VREF		N.C.	
J15	IP_L27N_1	1	INPUT		N.C.	
J16	IP_L27P_1	1	INPUT		N.C.	
J17	IO_L24P_1	1	I/O	I/O	FLSO	CAR2 PORT[10]
J18	IO_L22N_1/A11	1	DUAL	I/O	PORT1_[1]	CAR2 PORT[11]
J19	IO_L22P_1/A10	1	DUAL	I/O	PORT1_[2]	CAR2 PORT[12]
J20	IO_L21N_1/RHCLK7	1	RHCLK	I/O	PORT1_[3]	CAR2 PORT[13]
K14	IP_L23N_1	1	INPUT		N.C.	
K15	IP_L23P_1/VREF_1	1	VREF		N.C.	
K16	IO_L24N_1	1	I/O	I/O	PORT1_[4]	CAR2 PORT[14]
K18	IO_L20P_1/RHCLK4	1	RHCLK	I/O	PORT1_[5]	CAR2 PORT[15]
K20	IO_L21P_1/IRDY1/RHCLK6	1	RHCLK	I	INTP[0]	SW-INTP0
L13	IP_L19N_1	1	INPUT		N.C.	
L14	IP_L19P_1	1	INPUT		N.C.	
L15	IO_L16P_1/A8	1	DUAL	I	INTP[1]	SW-INTP1
L16	IO_L16N_1/A9	1	DUAL	I	INTP[2]	SW-INTP2
L17	IO_L20N_1/RHCLK5	1	RHCLK	I	CSI_CLK	SV_CSI_CLK
L18	IO_L18N_1/TRDY1/RHCLK3	1	RHCLK	I	CSI_RX	SV_CSI_RX
L19	IO_L18P_1/RHCLK2	1	RHCLK	O	CSI_TX	SV_CSI_TX
M13	IP_L15N_1	1	INPUT		N.C.	
M14	IP_L15P_1/VREF_1	1	VREF		N.C.	
M15	IP_L11N_1/VREF_1	1	VREF		N.C.	
M16	IP_L11P_1	1	INPUT		N.C.	
M17	IO_L14P_1/A6	1	DUAL	I	CSI_CS	SV_CSI_CS
M18	IO_L14N_1/A7	1	DUAL	I	ERROROUT	CAR2 ERROROUT
M19	IO_L17P_1/RHCLK0	1	RHCLK		NC	
M20	IO_L17N_1/RHCLK1	1	RHCLK	I/O	YOBI_PORT[3]	PUP is required
N14	IP_1/VREF_1	1	VREF		N.C.	
N15	IO_L12P_1/A2	1	DUAL	I	HDRSTB	PUP is required
N17	IO_L12N_1/A3	1	DUAL	I	DCON10	PUP is required
N18	IO_L13P_1/A4	1	DUAL	I	DCON19	PUP is required
N19	IO_L13N_1/A5	1	DUAL	I	REGON25	PUP is required
P14	IP_L04P_1	1	INPUT		N.C.	
P15	IP_L04N_1/VREF_1	1	VREF		N.C.	
P16	IO_L07P_1	1	I/O		FAILDC	
P17	IO_L07N_1	1	I/O	I/O	G_SRESET_	PUP is required
P18	IO_L10P_1	1	I/O	I/O	YOBI_PORT[1]	PUP is required
P20	IO_L10N_1/VREF_1	1	VREF	I/O	YOBI_PORT[2]	PUP is required
R16	IO_L03N_1/A1	1	DUAL		N.C.	
R17	IO_L08N_1	1	I/O		N.C.	

R18	IO_L08P_1	1	I/O		N.C.	
R19	IO_L09P_1	1	I/O	I/O	PIO_VIO18	PUP is required
R20	IO_L09N_1	1	I/O	I/O	PIO_VIO20	PUP is required
T17	IO_L03P_1/A0	1	DUAL	I	COUNTEND	CAR2 COUNTEND
T18	IO_L05P_1	1	I/O	I	BREAK	CAR2 BREAK
T20	IO_L05N_1	1	I/O	O	SF_C2SEL_	Serial Flash CAR2 Select
U18	IO_L02N_1/LDC0	1	DUAL	O	SF_SVSEL_	Serial Flash SV Select
U19	IO_L06P_1	1	I/O	O	SF_HDSEL_	Serial Flash CN1 Select
U20	IO_L06N_1	1	I/O	O	SH_MA3SEL_	Host MA3 Select
V19	IO_L02P_1/LDC1	1	DUAL	O	SH_SVSEL_	Serial Host SV Select
V20	IO_L01N_1/LDC2	1	DUAL	O	SH_HDSEL_	Serial Host CN2 Select
W20	IO_L01P_1/HDC	1	DUAL		N.C.	
A2	IO_L32P_0/VREF_0	0	VREF	I/O	SV_A[1]	SV address
A3	IO_L30P_0	0	I/O	I/O	SV_A[2]	SV address
B3	IO_L30N_0	0	I/O	I/O	SV_A[3]	SV address
A4	IO_L29P_0	0	I/O	I/O	SV_A[4]	SV address
C4	IO_L29N_0	0	I/O	I/O	SV_A[5]	SV address
A5	IO_L26P_0	0	I/O	I/O	SV_A[6]	SV address
B5	IO_L26N_0	0	I/O	I/O	SV_A[7]	SV address
C5	IO_L28P_0	0	I/O	I/O	SV_A[8]	SV address
A6	IO_L25P_0	0	I/O	I/O	SV_A[9]	SV address
C6	IO_L25N_0	0	I/O	I/O	SV_A[10]	SV address
D6	IO_L28N_0	0	I/O	I/O	SV_A[11]	SV address
E6	IO_L31P_0	0	I/O	I/O	SV_A[12]	SV address
F6	IO_L31N_0	0	I/O		N.C.	
A7	IO_L24N_0	0	I/O	I/O	SV_A[13]	SV address
B7	IO_L24P_0	0	I/O	I/O	SV_A[14]	SV address
C7	IO_L21P_0	0	I/O	I/O	SV_A[15]	SV address
E7	IO_L27P_0	0	I/O	I/O	SV_A[16]	SV address
F7	IO_L27N_0	0	I/O		N.C.	
A8	IO_L18N_0/GCLK11	0	GCLK	I/O	SV_A[17]	SV address
B8	IO_L20P_0	0	I/O	I/O	SV_A[18]	SV address
C8	IO_L20N_0	0	I/O	I/O	SV_A[19]	SV address
D8	IO_L21N_0	0	I/O	I/O	SV_A[20]	SV address
E8	IO_L23P_0	0	I/O		N.C.	
F8	IO_L23N_0	0	I/O		N.C.	
G8	IP_0	0	INPUT		N.C.	
A9	IO_L18P_0/GCLK10	0	GCLK	I/O	SV_A[21]	SV address
B9	IO_L19P_0	0	I/O	I/O	SV_A[22]	SV address
C9	IO_L19N_0	0	I/O	I/O	SV_A[23]	SV address
E9	IO_L22P_0	0	I/O	I/O	SV_A[24]	SV address
F9	IO_L22N_0/VREF_0	0	VREF		N.C.	
G9	IP_0	0	INPUT		N.C.	
H9	IP_0	0	INPUT		N.C.	
A10	IO_L16P_0/GCLK6	0	GCLK		N.C.	
C10	IO_L16N_0/GCLK7	0	GCLK		N.C.	
D10	IO_L17P_0/GCLK8	0	GCLK		N.C.	
E10	IO_L17N_0/GCLK9	0	GCLK	I	OSC4	optional clock
G10	IP_0	0	INPUT		N.C.	
H10	IP_0	0	INPUT		N.C.	
B11	IO_L14P_0	0	I/O	I/O	SV_A[25]	SV address
C11	IO_L14N_0	0	I/O		N.C.	
D11	IO_L15P_0/GCLK4	0	GCLK	I	USBCLK	USB Clock(30MHz)
E11	IO_L15N_0/GCLK5	0	GCLK		N.C.	

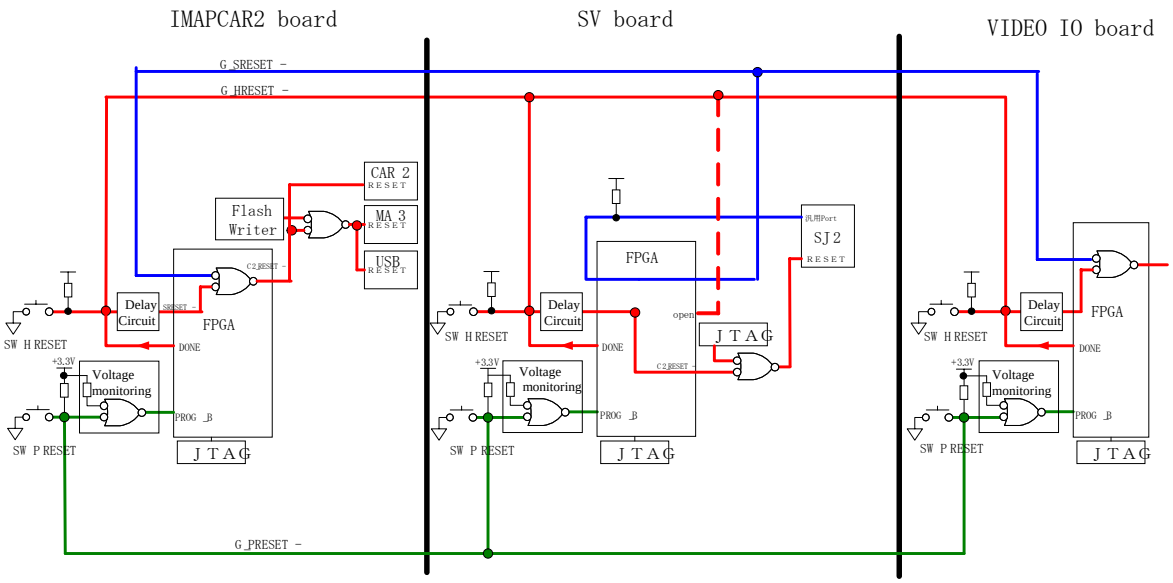
F11	IP_0	0	INPUT		N.C.	
G11	IP_0/VREF_0	0	VREF		N.C.	
H11	IP_0	0	INPUT		N.C.	
A12	IO_L13N_0	0	I/O	I/O	SV_A[26]	SV address
B12	IO_L13P_0	0	I/O	I/O	SV_A[27]	SV address
C12	IO_L11N_0	0	I/O	I/O	SV_A[28]	SV address
D12	IO_L12P_0	0	I/O	I/O	SV_D[0]	SV data
F12	IO_L12N_0	0	I/O		N.C.	
G12	IP_0	0	INPUT		N.C.	
H12	IP_0	0	INPUT		N.C.	
B13	IO_L11P_0	0	I/O	I/O	SV_D[1]	SV data
C13	IO_L10N_0/VREF_0	0	VREF	I/O	SV_D[2]	SV data
E13	IO_L09P_0	0	I/O	I/O	SV_D[3]	SV data
F13	IO_L09N_0	0	I/O	I/O	SV_D[4]	SV data
G13	IP_0	0	INPUT		N.C.	
A14	IO_L07N_0	0	I/O	I/O	SV_D[5]	SV data
C14	IO_L07P_0	0	I/O	I/O	SV_D[6]	SV data
D14	IO_L10P_0	0	I/O	I/O	SV_D[7]	SV data
E14	IP_0	0	INPUT		N.C.	
F14	IP_0	0	INPUT		N.C.	
A15	IO_L08N_0	0	I/O	I/O	SV_D[8]	SV data
B15	IO_L08P_0	0	I/O	I/O	SV_D[9]	SV data
C15	IO_L06N_0	0	I/O	I/O	SV_D[10]	SV data
D15	IO_L06P_0	0	I/O	I/O	SV_D[11]	SV data
E15	IO_L03N_0	0	I/O		N.C.	
A16	IO_L05N_0	0	I/O	I/O	SV_D[12]	SV data
C16	IO_L05P_0	0	I/O	I/O	SV_D[13]	SV data
D16	IO_L03P_0	0	I/O	I/O	SV_D[14]	SV data
A17	IO_L04N_0	0	I/O	I/O	SV_D[15]	SV data
B17	IO_L04P_0/VREF_0	0	VREF	I/O	SV_RDB	SV RD
C17	IO_L02N_0	0	I/O	I/O	SV_WRB	SV WR
D17	IO_L02P_0/VREF_0	0	VREF	I/O	SV_CSB[0]	SV CS0
A18	IO_L01N_0	0	I/O	I/O	SV_CSB[1]	SV CS1
B18	IO_L01P_0	0	I/O	I/O	SV_CSB[2]	SV CS2
A1	GND	GND	GND		GND	
A11	GND	GND	GND		GND	
A20	GND	GND	GND		GND	
B14	GND	GND	GND		GND	
B6	GND	GND	GND		GND	
C18	GND	GND	GND		GND	
C3	GND	GND	GND		GND	
D9	GND	GND	GND		GND	
E12	GND	GND	GND		GND	
E5	GND	GND	GND		GND	
F15	GND	GND	GND		GND	
G19	GND	GND	GND		GND	
G2	GND	GND	GND		GND	
H13	GND	GND	GND		GND	
H8	GND	GND	GND		GND	
J11	GND	GND	GND		GND	
J9	GND	GND	GND		GND	
K1	GND	GND	GND		GND	
K10	GND	GND	GND		GND	
K12	GND	GND	GND		GND	
K17	GND	GND	GND		GND	
L11	GND	GND	GND		GND	
L20	GND	GND	GND		GND	
L4	GND	GND	GND		GND	

L9	GND	GND	GND		GND	
M10	GND	GND	GND		GND	
M12	GND	GND	GND		GND	
N11	GND	GND	GND		GND	
N13	GND	GND	GND		GND	
N8	GND	GND	GND		GND	
P19	GND	GND	GND		GND	
P2	GND	GND	GND		GND	
R6	GND	GND	GND		GND	
R9	GND	GND	GND		GND	
T16	GND	GND	GND		GND	
U12	GND	GND	GND		GND	
V18	GND	GND	GND		GND	
V3	GND	GND	GND		GND	
W15	GND	GND	GND		GND	
W7	GND	GND	GND		GND	
Y1	GND	GND	GND		GND	
Y10	GND	GND	GND		GND	
Y20	GND	GND	GND		GND	
A13	VCCAUX	VCCAUX	VCCAUX		+3.3V	Configuration IF power
E16	VCCAUX	VCCAUX	VCCAUX		+3.3V	Configuration IF power
H1	VCCAUX	VCCAUX	VCCAUX		+3.3V	Configuration IF power
K13	VCCAUX	VCCAUX	VCCAUX		+3.3V	Configuration IF power
L8	VCCAUX	VCCAUX	VCCAUX		+3.3V	Configuration IF power
N20	VCCAUX	VCCAUX	VCCAUX		+3.3V	Configuration IF power
T5	VCCAUX	VCCAUX	VCCAUX		+3.3V	Configuration IF power
Y8	VCCAUX	VCCAUX	VCCAUX		+3.3V	Configuration IF power
J10	VCCINT	VCCINT	VCCINT		+1.2V	
J12	VCCINT	VCCINT	VCCINT		+1.2V	
K11	VCCINT	VCCINT	VCCINT		+1.2V	
K9	VCCINT	VCCINT	VCCINT		+1.2V	
L10	VCCINT	VCCINT	VCCINT		+1.2V	
L12	VCCINT	VCCINT	VCCINT		+1.2V	
M11	VCCINT	VCCINT	VCCINT		+1.2V	
M9	VCCINT	VCCINT	VCCINT		+1.2V	
N10	VCCINT	VCCINT	VCCINT		+1.2V	
B10	VCCO_0	0	VCCO		+3.3V	
B16	VCCO_0	0	VCCO		+3.3V	
B4	VCCO_0	0	VCCO		+3.3V	
D13	VCCO_0	0	VCCO		+3.3V	
D7	VCCO_0	0	VCCO		+3.3V	
F10	VCCO_0	0	VCCO		+3.3V	
D19	VCCO_1	1	VCCO		+3.3V	
H16	VCCO_1	1	VCCO		+3.3V	
K19	VCCO_1	1	VCCO		+3.3V	
N16	VCCO_1	1	VCCO		+3.3V	
T19	VCCO_1	1	VCCO		+3.3V	
R11	VCCO_2	2	VCCO		+3.3V	
U14	VCCO_2	2	VCCO		+3.3V	
U8	VCCO_2	2	VCCO		+3.3V	

W11	VCCO_2	2	VCCO		+3.3V	
W17	VCCO_2	2	VCCO		+3.3V	
W5	VCCO_2	2	VCCO		+3.3V	
E2	VCCO_3	3	VCCO		+3.3V	
H5	VCCO_3	3	VCCO		+3.3V	
L2	VCCO_3	3	VCCO		+3.3V	
N5	VCCO_3	3	VCCO		+3.3V	
U2	VCCO_3	3	VCCO		+3.3V	
F5	TDI	VCCAUX	JTAG		TDI	For configuration
E4	TMS	VCCAUX	JTAG		TMS	For configuration
E17	TDO	VCCAUX	JTAG		TDO	For configuration
A19	TCK	VCCAUX	JTAG		TCK	For configuration
D5	PROG_B	VCCAUX	CONFIG		PROG_B	For configuration
W19	DONE	VCCAUX	CONFIG		DONE	For configuration
W18	IO_L32P_2/D0/DIN/MISO	2	DUAL		DIN	For configuration
Y19	IO_L32N_2/CCLK	2	DUAL		CCLK	For configuration
Y14	IO_L24P_2/INIT_B	2	DUAL		INIT_B	For configuration
V13	IO_L22N_2/DOUT	2	DUAL		DOUT	For configuration
W3	IO_L02P_2/M2	2	DUAL		M2	GND
U4	IO_L01P_2/M1	2	DUAL		M1	GND
V4	IO_L01N_2/M0	2	DUAL		M0	GND
B2	IO_L32N_0/PUDC_B	0	DUAL		PUDC_B	+3.3V
R15	SUSPEND	1	PWRMGMT		SUSPEND	GND

5.5 System Reset

Please find the diagram of the system reset



Green line : Power reset.

Red line : a hard reset.

Blue Line : Soft Reset

Please see the chapters "4.1.2 Power Reset Switch (SW-PRESET)" & "4.1.3 Hard reset switch (SW-HRESET)" for more information about switch function

5.6 Port assignation

5.6.1 V850E/MA3 Port

Port name	Shared function	Signal name	Feature	PUP/PDN
P00	TOP00/INTP000/EVTP0/TIP0/INTPP00	Unused		47KΩPUP
P01	TOP01/INTP001/INTPP01	Unused		47KΩPUP
P04	DMARQ0/INTP11/TCLR10/INTP004	EP2_DRQ-	USB DMAREQ input(*1)	None
P05	DMARQ1/TCUD10/INTP10/INTP005	INTUSB3	USB INTB_ALL input	None
P06	DMARQ2/TMS/INTP106	MA3_DMS	N-Wire signal	47KΩPUP
P07	DMARQ3/TCK/INTP107	MA3_DCK	N-Wire signal	47KΩPUP
P10	TOQB1/INTP010/INTPQ0/TOQ0	INTUSB1	USB INT1B input	None
P11	TOQT1/INTP011/INTPQ1/TOQ1	INTUSB0	USB INT0B input	None
P12	TOQT2/INTP012/INTPQ2/TOQ2	MA3_A26	Extended address bit [26] output.	47KΩPUP
P13	TOQT3/INTP013/INTPQ3/TOQ3	INTUSB2	USB INT2B input	None
P14	TOQB2/INTP114/TIQ	MA3_A27	Extended address bit [27] output.	47KΩPUP
P15	TOQB3/INTP115/EVTQ	MA3_A28	Extended address bit [28] output.	47KΩPUP
P20	NMI	Unused		10KΩPDN
P21	TOP10/INTPP10/EVTP1/TIP1/INTP021	MA3_MODE0	FLMD1input (used by the Flash programmer)	4.7KΩPDN
P22	TOP11/INTPP11/INTP022	Unused		47KΩPUP
P24	TC0/INTP124	EP2TC-	USB TC output (*1)	None
P25	TC1/TIUD10/TO10/INTP125	USBM2	USB M2input	None
P26	TC2/TDI/INTP126	MA3_DDI	N-Wire signal。	47KΩPUP
P27	TC3/TDO	MA3_DDO	N-Wire signal	47KΩPUP
P30	TXD2/SO2/INTP130	P13_UC0	Multi-purpose general-purpose FPGA IO.	47KΩPUP
P31	RXD2/SI2/INTP131	P13_UC1	Multi-purpose general-purpose FPGA IO.	47KΩPUP
P32	ASCK2/SCK2/INTP132	P13_UC2	Multi-purpose general-purpose FPGA IO.	47KΩPUP
P33	TXD3/SDA/INTP133	P13_UC3	Multi-purpose general-purpose FPGA IO.	47KΩPUP
P34	RXD3/SCL/INTP134	MA3_MODE1	FLMD0input (used by the Flash programme and N-Wire)	4.7KΩPDN
P37	ADTRG/INTP137	Unused		10KΩPDN
P40	TXD0/SO0	MA3_SO0	Flash Writer-SI/RXD	47KΩPUP
P41	RXD0/SI0	MA3_SI0	Flash Writer-SO/TXD。	47KΩPUP
P42	ASCK0/SCK0	MA3_SCK0	Flash Writer-SCK。	47KΩPUP
P43	TXD1/SO1	Unused		47KΩPUP
P44	RXD1/SI1	Unused		47KΩPUP
P45	ASCK1/SCK1	Unused		47KΩPUP
P50	TOP20/INTPP20/EVTP2/TIP2/INTP050	MA3_BUSREQ	Bus Request output signal for FPGA bus arbitration	10KΩPDN
P51	TOP21/INTPP21/INTP051	MA3_BUSBUSY	Bus Busy input signal for FPGA bus arbitration。	10KΩPDN
P70	ANI0	GND	Not used. Connected to GND	
P71	ANI1	GND	Not used. Connected to GND	
P72	ANI2	GND	Not used. Connected to GND	
P73	ANI3	GND	Not used. Connected to GND	
P74	ANI4	GND	Not used. Connected to GND	

P75	ANI5	GND	Not used. Connected to GND	
P76	ANI6	GND	Not used. Connected to GND	
P77	ANI7	GND	Not used. Connected to GND	
P80	ANO0	Unused		10KΩPDN
P81	ANO1	Unused		10KΩPDN
PAL0	A0	Unused		47KΩPUP
PAL1	A1	MA3_A1	External Memory interface : Address	47KΩPUP
PAL2	A2	MA3_A2		47KΩPUP
PAL3	A3	MA3_A3		47KΩPUP
PAL4	A4	MA3_A4		47KΩPUP
PAL5	A5	MA3_A5		47KΩPUP
PAL6	A6	MA3_A6		47KΩPUP
PAL7	A7	MA3_A7		47KΩPUP
PAL8	A8	MA3_A8		47KΩPUP
PAL9	A9	MA3_A9		47KΩPUP
PAL10	A10	MA3_A10		47KΩPUP
PAL11	A11	MA3_A11		47KΩPUP
PAL12	A12	MA3_A12		47KΩPUP
PAL13	A13	MA3_A13		47KΩPUP
PAL14	A14	MA3_A14		47KΩPUP
PAL15	A15	MA3_A15		47KΩPUP
PAH0	A16	MA3_A16		47KΩPUP
PAH1	A17	MA3_A17		47KΩPUP
PAH2	A18	MA3_A18		47KΩPUP
PAH3	A19	MA3_A19		47KΩPUP
PAH4	A20	MA3_A20		47KΩPUP
PAH5	A21	MA3_A21		47KΩPUP
PAH6	A22	MA3_A22		47KΩPUP
PAH7	A23	MA3_A23		47KΩPUP
PAH8	A24	MA3_A24		47KΩPUP
PAH9	A25	MA3_A25		47KΩPUP
PDL0	AD0	MA3_D0	External Memory interface : Data	47KΩPUP
PDL1	AD1	MA3_D1		47KΩPUP
PDL2	AD2	MA3_D2		47KΩPUP
PDL3	AD3	MA3_D3		47KΩPUP
PDL4	AD4	MA3_D4		47KΩPUP
PDL5	AD5	MA3_D5		47KΩPUP
PDL6	AD6	MA3_D6		47KΩPUP
PDL7	AD7	MA3_D7		47KΩPUP
PDL8	AD8	MA3_D8		47KΩPUP
PDL9	AD9	MA3_D9		47KΩPUP
PDL10	AD10	MA3_D10		47KΩPUP
PDL11	AD11	MA3_D11		47KΩPUP
PDL12	AD12	MA3_D12		47KΩPUP
PDL13	AD13	MA3_D13		47KΩPUP
PDL14	AD14	MA3_D14		47KΩPUP
PDL15	AD15	MA3_D15		47KΩPUP
PCS0	CS0	Unused		47KΩPUP
PCS1	CS1	MA3_CS1-	Chip select for USB Controller. Have to be set in output	47KΩPUP
PCS2	CS2/IOWR	Unused		47KΩPUP

PCS3	CS3	MA3_CS3-	Chip select for IMAPCAR2. Have to be set in output	47KΩPUP
PCS4	CS4	Unused		47KΩPUP
PCS5	CS5/IORD	Unused		47KΩPUP
PCS6	CS6	MA3_CS6-	Chip select for Video Board/ FPGA (S841PLD01). Have to be set in output	47KΩPUP
PCS7	CS7	Unused		47KΩPUP
PCT0	LBE/LWR/LDQM	Unused		47KΩPUP
PCT1	UBE/UWR/UDQM	Unused		47KΩPUP
PCT4	RD	MA3_RD-	External Memory Interface : Read output signal	47KΩPUP
PCT5	WR/WE	MA3_WR-	External Memory Interface : Write output signal	47KΩPUP
PCT6	ASTB	Unused		47KΩPUP
PCT7	BCYST	Unused		47KΩPUP
PCM0	WAIT	MA3_WAIT-	External Memory Interface : Wait output signal	47KΩPUP
PCM1	BUSCLK	Unused		47KΩPUP
PCM2	HLDAK	MA3_BUSSTAT	Bus Status input signal for FPGA bus arbitration (‘0’：bus is used、’1’：idle bus)	10KΩPDN
PCM3	HLDRQ	MA3_BURST	Bus Burst output signal for FPGA bus arbitration (*2)	10KΩPDN
PCM4	REFRQ	MA3_BUSRESET	Bus Reset output signal for FPGA bus arbitration (*2)	10KΩPDN
PCD0	SDCKE	Unused		47KΩPUP
PCD1	SDCLK	Unused		47KΩPUP
PCD2	SDCAS	Unused		47KΩPUP
PCD3	SDRAS	Unused		47KΩPUP
PBD0	DMAAK0	EP2_DAK-	USB DMAAK output(*1)	None
PBD1	DMAAK1	Unused		47KΩPUP
PBD2	DMAAK2	Unused		47KΩPUP
PBD3	DMAAK3	Unused		47KΩPUP

Note (* 1): currently unavailable.

Note (* 2): unused

5.6.2 IMAPCAR2 Port

IMAPCAR2 Port (PORT[00:15]) description

Port Name	Shared function	Signal name	Features	PUP/PDN
PORT00	None	PORT0_0	General Purpose I / O port. Connected to the FPGA board and SV	47KΩ PUP
PORT01	None	PORT0_1	General Purpose I / O port. Connected to the FPGA board and SV	47KΩ PUP
PORT02	None	PORT0_2	General Purpose I / O port. Connected to the FPGA board and SV	47KΩ PUP
PORT03	None	PORT0_3	General Purpose I / O port. Connected to the FPGA board and SV	47KΩ PUP
PORT04	None	PORT0_4	General Purpose I / O port. Connected to the FPGA board and SV	47KΩ PUP
PORT05	None	PORT0_5	General Purpose I / O port. Connected to the FPGA board and SV	47KΩ PUP
PORT06	None	PORT0_6	General Purpose I / O port. Connected to the FPGA board and SV	47KΩ PUP
PORT07	None	PORT0_7	General Purpose I / O port. Connected to the FPGA board and SV	47KΩ PUP
PORT08	FLSCK_B	C2_FLSCKB	Serial Flash clock pin. (* 1)	47KΩ PUP
PORT09	FLSI	C2_FLSI	Serial Flash input pin. (* 1)	47KΩ PUP
PORT10	FLSO	C2_FLSO	Serial Flash output pin. (* 1)	47KΩ PUP
PORT11	None	PORT1_1	Serial Flash Chip pin out	47KΩ PUP
PORT12	None	PORT1_2	General Purpose I / O port. Connected to the FPGA board and SV (*2)	47KΩ PUP
PORT13	None	PORT1_3	General Purpose I / O port. Connected to the FPGA board and SV。	47KΩ PUP
PORT14	None	PORT1_4	General Purpose I / O port. Connected to the FPGA board and SV	47KΩ PUP
PORT15	None	PORT1_5	General Purpose I / O port. Connected to the FPGA board and SV	47KΩ PUP

Note (* 1); SW must be set. ("4.1.8SW4" Please see.)

Note (* 2); SV from Serial Flash board is used as chip select.

5.7 Clock

IMAPCAR2-300-USB Board Clock configuration