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User's Manual

IE-703102-MC-EM1, IE-703102-MC-EM1-A

In-circuit Emulator Optional Board

Target device
V850E/MS1™

Document No. U13876EJ1V0UM00 (1st edition)
Date Published December 1998 N CP(K)

[MEMO]

M7A 96.10

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- Device availability
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- Product release schedule
- Availability of related technical literature
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INTRODUCTION

Readers

This manual is intended for users who design and develop application systems using the V850E/MS1™.

Purpose

The purpose of this manual is to describe the proper operation of the IE-703102-MC-EM1 and IE-703102-MC-EM1-A, and their basic specifications.

Organization

This manual is broadly divided into the following parts.

- Overview
- Name and function of components
- Cautions

How to Read This Manual

It is assumed that the reader of this manual has general knowledge of electrical engineering, logic circuits, and microcontrollers.
The IE-703102-MC-EM1 and IE-703102-MC-EM1-A are used connected to the IE-703102-MC in-circuit emulator. This manual explains the basic setup procedure and switch settings of the IE-703102-MC-EM1 and IE-703102-MC-EM1-A. For the names and functions, and the connection of parts, refer to the **IE-703102-MC User's Manual**, which is a separate volume.

To understand the basic specifications and operation methods broadly
→ Read this manual in the order listed in **CONTENTS**.

To know the operation methods and command functions of the IE-703102-MC, IE-703102-MC-EM1, and IE-703102-MC-EM1-A
→ Read the user's manual of the debugger (separate volume) that is used.

Conventions

Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeral representations:	Binary ··· ×××× or ××××B
	Decimal ··· ××××
	Hexadecimal ··· ××××H

Prefixes representing the powers of 2 (address space, memory capacity):
K (kilo): $2^{10} = 1024$
M (mega): $2^{20} = 1024^2$

Terminology

The meanings of terms used in this manual are listed below.

Target device	Device that is emulated.
Target system	The system (user-built system) to be debugged. This includes the target program and user-configured hardware.

Product Names Unless otherwise specified, the IE-703102-MC-EM1 is treated as the representative model in this manual. When using the IE-703102-MC-EM1-A, read IE-703102-MC-EM1 as IE-703102-MC-EM1-A. For functional differences between IE-703102-MC-EM1 and IE-703102-MC-EM1-A, refer to **CHAPTER 1 OVERVIEW.**

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

○ **Documents related to V850E/MS1**

Document Name	Document Number
V850E/MS1 User's Manual-Hardware	U12688E
V850E/××× User's Manual-Architecture	U12197E
μPD703100-40, 703101-33, 703102-33 Data Sheet	To be prepared
μPD703100-A40, 703101-A33, 703102-A33 Data Sheet	To be prepared
μPD70F3102-33 Data Sheet	U13844E
μPD70F3102-A33 Data Sheet	U13845E

○ **Documents related to development tools (User's Manual)**

Product Name		Document Number
IE-703102-MC (In-circuit emulator)		U13875E
IE-703102-MC-EM1, IE-703102-MC-EM1-A (In-circuit emulator optional board)		This manual
CA850 (C Compiler package)	Operation UNIX™ based	U12839E
	Operation Windows™ based	U12827E
	C language	U12840E
	Assembly Language	U10543E
ID850 (Integrated debugger)	Operation Windows based	U13716E
RX850 (Real-time OS)	Basics	U13430E
	Technical	U13431E
	Installation	U13410E
RX850 Pro (Real-time OS)	Fundamental	Under preparation
	Technical	U13772E
	Installation	U13774E
RD850 (Task debugger)[Note]		U11158E
RD850 (Ver. 3.0) (Task debugger)		U13737E
AZ850 (System performance analyzer) Operation		U11181E

Note Supports ID850 (Ver. 1.31 only)

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LIST OF FIGURES

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[MEMO]

CHAPTER 1 OVERVIEW

The IE-703102-MC-EM1 is an optional board for the in-circuit emulator IE-703102-MC. By connecting the IE-703102-MC-EM1 to IE-703102-MC, hardware and software can be debugged efficiently in system development using the V850E/MS1.

IE-703102-MC-EM1 is an optional board when **HV_{DD} = 5 V**
IE-703102-MC-EM1-A is an optional board when **HV_{DD} = 3.3 V**

In this manual, the basic setup sequences and switch settings of the IE-703102-MC-EM1 when connecting it to the IE-703102-MC are described. For the names and functions of the parts of the IE-703102-MC, and for the connection of elements, refer to the **IE-703102-MC User's Manual (U13875E)** which is a separate volume.

1.1 Hardware Configuration

Separately sold hardware

In-circuit emulator (IE-703102-MC)

Optional board (IE-703102-MC-EM1 IE-703102-MC-EM1-A)	IE-703102-MC can be used as in-circuit emulator for V850E/MS1 by adding these boards.

Separately sold hardware

Extension probe (SC-×××SDA[Note 1])	General-purpose extension probe made by TOKYO ELETECH CORPORATION.
PC interface board (IE-70000-××-IF-B IE-70000-××-IF-C IE-70000-PCI-IF IE-70000-CD-IF-A)	These boards are used to connect the IE-703102-MC to a personal computer. These boards are inserted in the expansion slot of the personal computer. ××: 98 (for PC-9800 series C bus)[Note 2] PC (for IBM PC/AT™ compatible ISA bus)[Note 2] IE-70000-PCI-IF : for PCI bus IE-70000-CD-IF-A : for PCMCIA socket
Network module (IE-70000-MC-SV3)	The module is used when a workstation controls the IE-703102-MC via ethernet™.
Power adapter (IE-70000-MC-PS-B)	AC adapter dedicated to the NEC's in-circuit emulator

Notes 1. For further information, contact Daimaru Kogyo Co., Ltd.
Tokyo Electronic Components Division (TEL +81-3-3820-7112)
Osaka Electronic Components Division (TEL +81-6-244-6672)

2. These interface boards cannot be used for the PC98-NX series.

1.2 Features (When Connected to IE-703102-MC)

- Maximum operation frequency: 40 MHz (HV_{DD} = 3.3 V or 5.0 V operation)
- Extremely lightweight and compact
- Higher equivalence with target device can be achieved by omitting buffer between signal cables.
- Following pins can be masked.
  $\overline{\text{RESET}}$, NMI, $\overline{\text{WAIT}}$, $\overline{\text{HLDRQ}}$
- Two methods of connection to target system:
  - Direct connection of the IE-703102-MC-EM1
  - Attach an extension probe (sold separetely) to the connection tab of the IE-703102-MC-EM1.
- Dimensions of the IE-703102-MC-EM1 are as follows.

Parameter		Value
Power dissipation		0.4 W (at 40-MHz operation frequency)[Note]
External dimensions (Refer to **APPENDIX A DIMENSIONS**)	Height	15 mm
	Length	207 mm
	Width	96 mm
Weight		170 g

Note The power dissipation is 11.4 W when IE-703102-MC + IE-703102-MC-EM1.

1.3 Function Specifications (When Connected to IE-703102-MC)

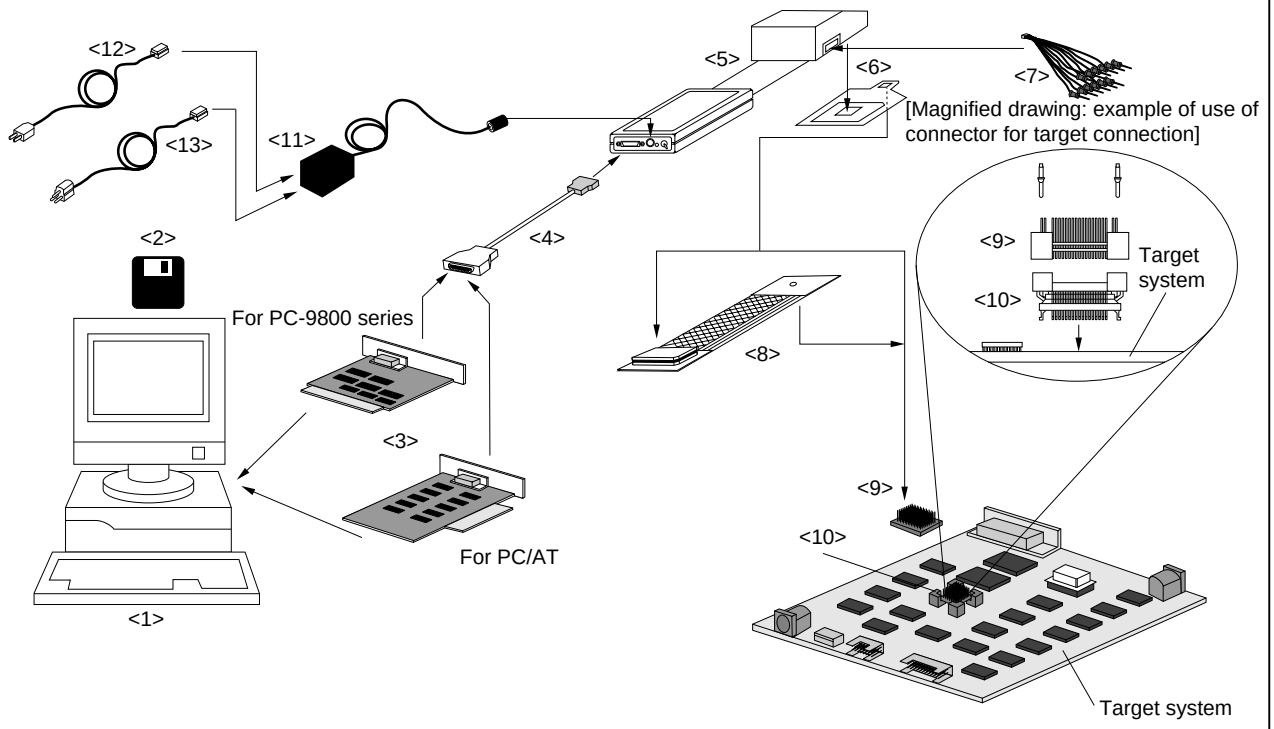
Parameter			Specification
Emulation memory capacity	Internal ROM		128 Kbytes
	External memory		2 Mbytes
Execution/pass detection Coverage memory capacity	Internal ROM		128 Kbytes
	External memory	In ROM-less mode	2 Mbytes
		When using iROM	1 Mbyte
Memory access detection Coverage memory capacity	External memory		1 Mbyte
Trace memory capacity			168 bits × 32 Kframes
Time measurement function			Can be measured with time tag and timers (3 lines)
External logic probe			8-bit external trace is possible
			Event setting for trace/break is possible
Break function			Event break
			Step execution break
			Forced break
			Fail safe break • Illegal access to peripheral I/O • Access to guard space • Write to the ROM space

Caution Some of the functions may not be supported depending on the debugger used.

1.4 System Configuration

The system configuration when connecting the IE-703102-MC-EM1 to the IE-703102-MC, which is then connected to a personal computer (PC-9800 series or PC/AT compatible) is shown below.

Figure 1-1. System Configuration



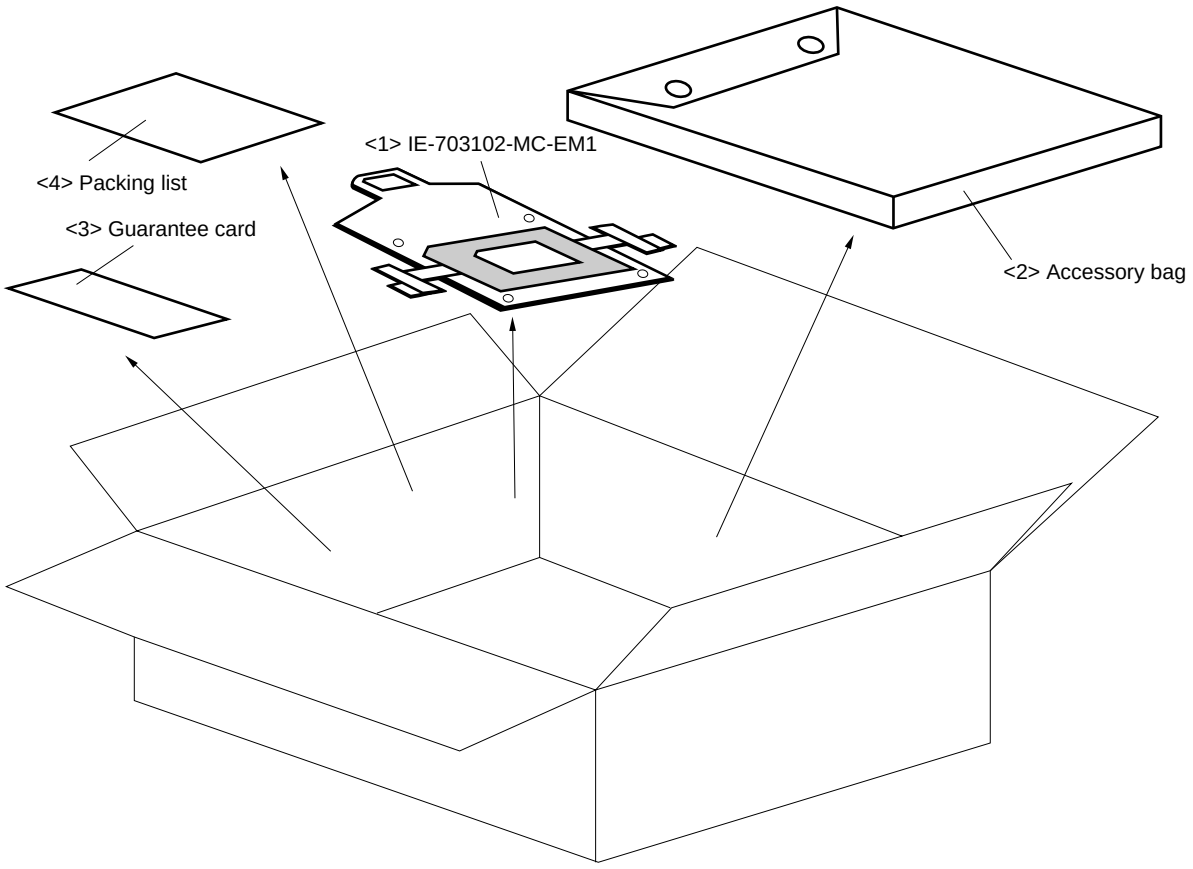
Remark

<1> Personal computer (PC-9800 series or PC/AT compatible)
<2> Debugger (sold separately)
<3> PC interface board (IE-70000-98-IF-B/IE-70000-98-IF-C, IE-70000-PC-IF-B/IE-70000-PC-IF-C : sold separately)
<4> PC interface cable (included with IE-703102-MC)
<5> In-circuit emulator (IE-703102-MC: sold separately)
<6> In-circuit emulator option board (IE-703102-MC-EM1)
<7> External logic probe (included with IE-703102-MC)
<8> Extension probe (SC-144SD, SC-144SD PR: sold separately)
<9> Connector for emulator connection (YQPACK144SD: included)
<10> Connector for target connection (NQPACK144SD: included)
<11> Power adapter (IE-70000-MC-PS-B: sold separately)
<12> AC100-V power cable (sold separately: included with IE-70000-MC-PS-B)
<13> AC220-V power cable (sold separately: included with IE-70000-MC-PS-B)

1.5 Contents in Carton

The carton of the IE-703102-MC-EM1 contains a main unit, guarantee card, packing list, and accessory bag. Make sure that the accessory bag contains this manual and connector accessories. In case of missing or damaged contents, contact an NEC sales representative or an NEC distributor.

Figure 1-2. Contents in Carton



<1> IE-703102-MC-EM1 × 1
<2> Accessory bag × 1
<3> Guarantee card × 1
<4> Packing list × 1

Make sure that the accessory bag contains this manual and an accessory list (1 sheet).

1.6 Connection between IE-703102-MC and IE-703102-MC-EM1

The procedure for connecting the IE-703102-MC and IE-703102-MC-EM1 is described below.

Caution Connect carefully so as not to break or bend connector pins.

<1> Remove the pod cover (upper and lower) of the IE-703102-MC.
<2> Set the PGA socket lever of the IE-703102-MC-EM1 to the OPEN position as shown in Figure 1-3 (b).
<3> Connect the IE-703102-MC-EM1 to the PGA socket at the back of the pod (refer to **Figure 1-3 (c)**). When connecting, position the IE-703102-MC and IE-703102-MC-EM1 so that they are horizontal.
Spacers can be connected to fix the pod. (refer to **APPENDIX D MOUNTING OF PLASTIC SPACER**)
<4> Set the PGA socket lever of the IE-703102-MC-EM1 to the CLOSE position as shown in Figure 1-3 (b).
<5> Fix the IE-703102-MC-EM1 between the pod covers (upper and lower) with nylon rivets.
<6> Secure the pod cover (upper) end with nylon rivets.

Figure 1-3. Connection between IE-703102-MC and IE-703102-MC-EM1 (1/2)

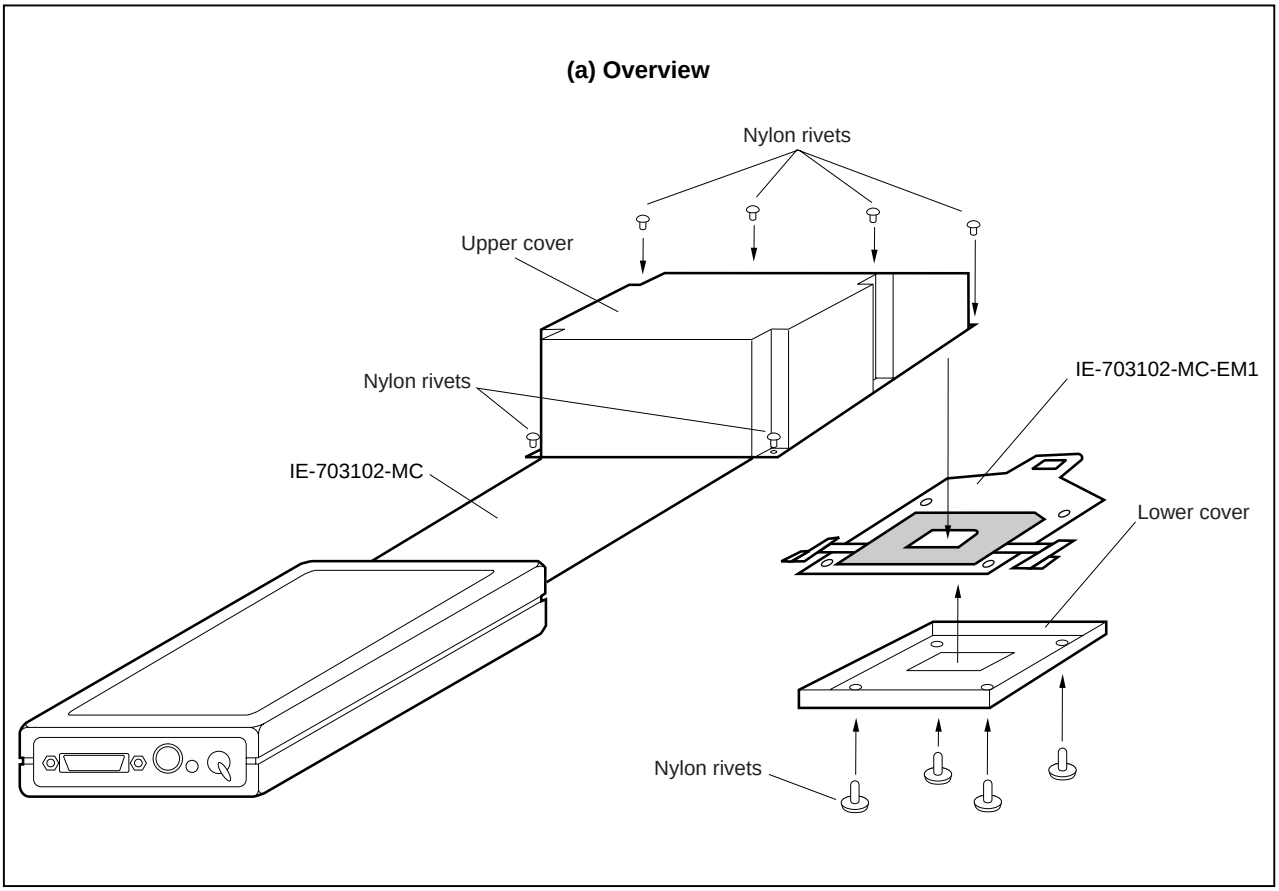
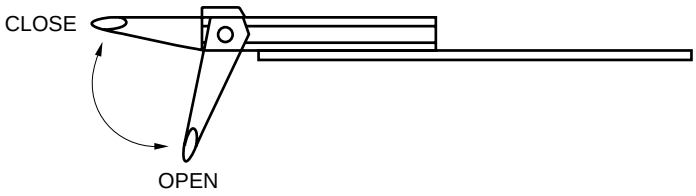
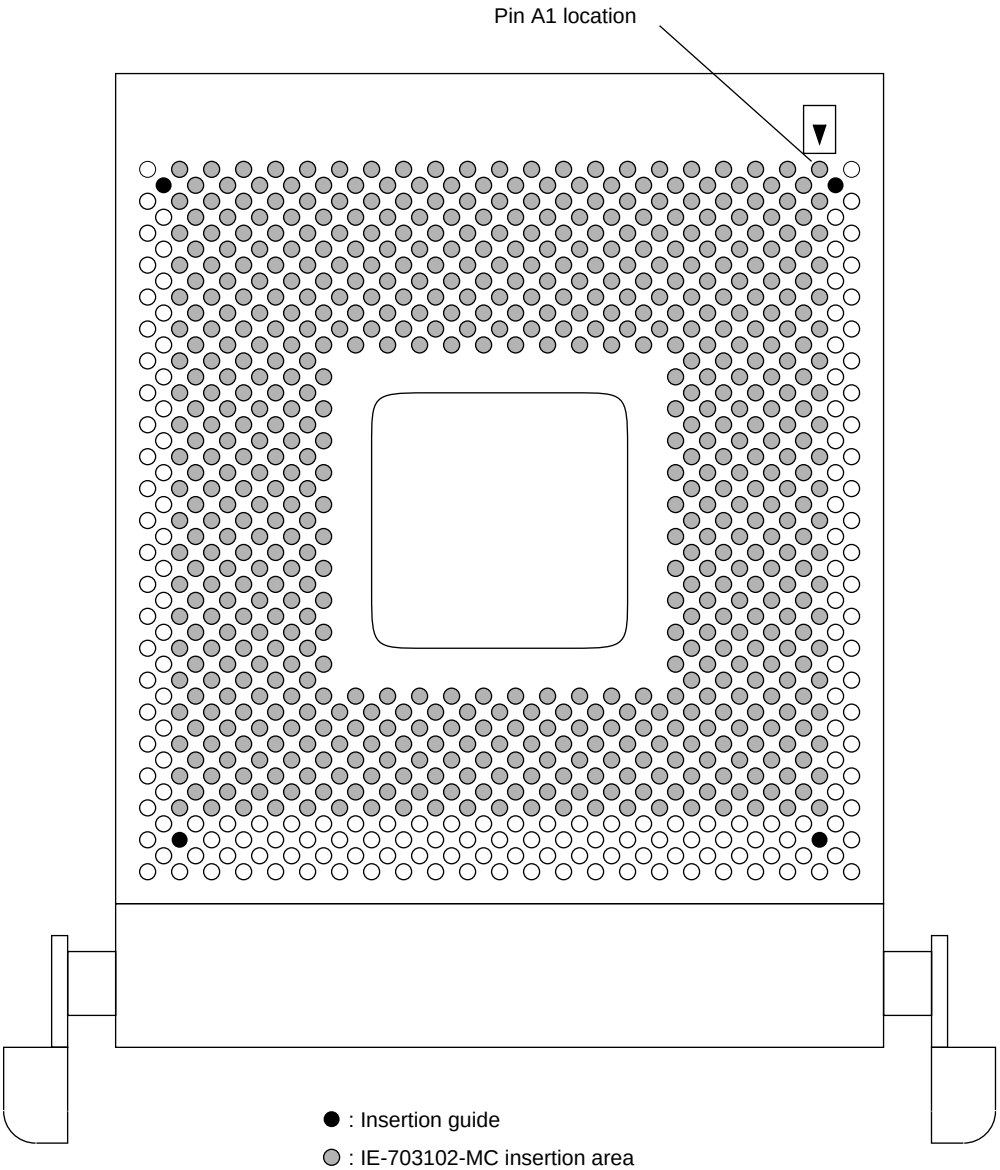


Figure 1-3. Connection between IE-703102-MC and IE-703102-MC-EM1 (2/2)

(b) PGA Socket Lever of IE-703102-MC-EM1



(c) Connecting part (IE-703102-MC-EM1)

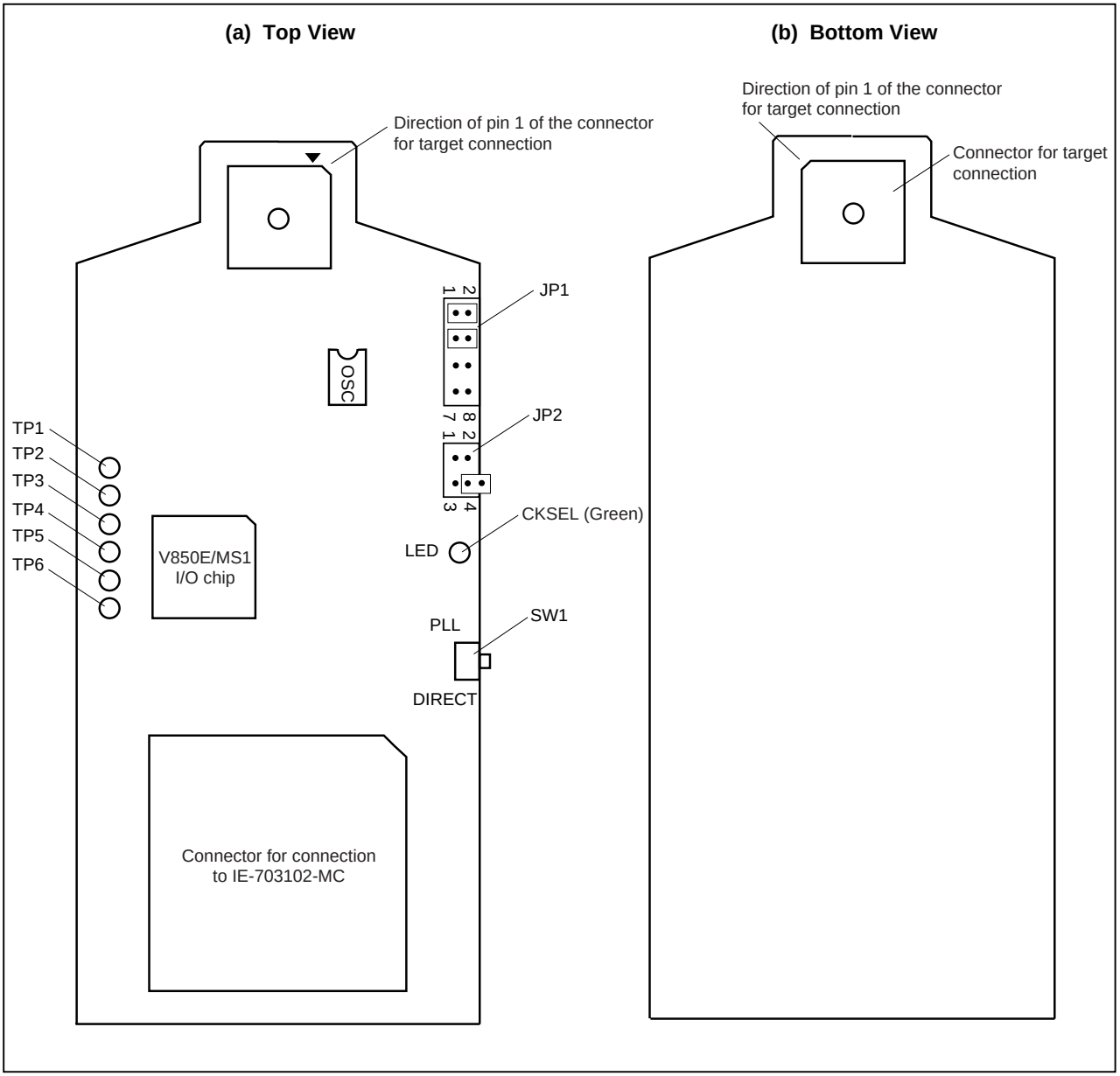


CHAPTER 2 NAME AND FUNCTION OF COMPONENTS

This chapter describes the names, functions, and switch settings of components comprising the IE-703102-MC-EM1. For the details of the pod, jumper, and switch positions, etc., refer to the **IE-703102-MC User's Manual**.

2.1 Component Name and Function of IE-703102-MC-EM1

Figure 2-1. IE-703102-MC-EM1



(1) Test pin (TP1 to TP6)

To leave the DMA cycle or refresh cycle in the tracer, or break these cycles, connect these pins to the external logic probe.

- TP1: GND
- TP2: REFRQ
- TP3: DMAAK0
- TP4: DMAAK1
- TP5: DMAAK2
- TP6: DMAAK3

(2) SW1

This is a switch for clock mode switching (for details, refer to **2.2 Clock Settings**).

(3) JP1

This is a switch jumper for the clock supply source (for details, refer to **2.2 Clock Settings**).

(4) JP2

This is a switch jumper for the power supply (for details, refer to **2.4 Power Supply Settings**).

(5) LED (CKSEL: Green)

LED Status	When Used as a Stand-Alone Unit	When Used in Target System Connection
ON	SW1 = DIRECT	The CKSEL signal from the target system is high
OFF	SW1 = PLL	The CKSEL signal from the target system is low

(6) Connector for IE-703102-MC connection

This is a connector for connecting the IE-703102-MC.

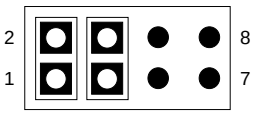
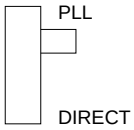
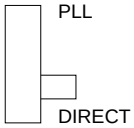
(7) Connector for target connection

This is a connector for connecting the target system or the extension probe.

2.2 Clock Settings

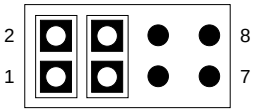
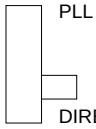
This section describes the clock settings. For JP1 and SW1, refer to Figure 2-1.

Table 2-1. Clock Setting (When the Emulator is Used as a Stand-Alone Unit)

Clock Supply Source Setting			Clock Mode Setting
Clock Supply Method		JP1 Setting[Note]	SW1 Setting (CKSEL Setting)
Internal clock	PLL mode		
	Direct mode		

Note Setting any other state is prohibited.

Table 2-2. Clock Setting (When the Emulator is Used in Target System Connection)

Clock Supply Source Setting			Clock Mode Setting	
Clock Supply Method		JP1 Setting[Note 1]	SW1 Setting (CKSEL Setting)	CKSEL Setting of Target System
Internal clock/target clock[Note 2]	PLL mode			Low level
	Direct mode			High level

Notes 1. Setting any other state is prohibited.

2. Switching the internal clock and target clock is done with the debugger.

2.3 MODE Pin Setting

The emulator operation mode can be changed with the MODE pin setting.

2.3.1 MODE pin setting when emulator is used as stand-alone unit

When the emulator is used as a stand-alone unit, MODE0 and MODE1 in the emulator are set as follows.
The setting cannot be changed.

Table 2-3. MODE Pin Setting when Emulator is Used as Stand-Alone Unit

Emulator Operation	Settings Inside Emulator	
	MODE0	MODE1
Single-chip mode 0	Low-level input	High-level input

2.3.2 MODE pin setting when emulator is used connected to target system

When the emulator is connected to a target system, set the MODE pins of the target system as follows based on the emulator operations.

The MODE2 and MODE3 signals in the target system are not used in the emulator.

Table 2-4. MODE Pin Setting when Emulator is Used Connected to Target System

Emulator Operation	Target System Setting	
	MODE0	MODE1
ROM-less mode 0	Low-level input	Low-level input
ROM-less mode 1	High-level input	Low-level input
Single-chip mode 0	Low-level input	High-level input
Single-chip mode 1	High-level input	High-level input

2.4 Power Supply Settings

Using the JP2 setting, the IE-703102-MC-EM1 can switch between operation using the emulator as a stand-alone unit (using the power of the emulator) and operation using the emulator connected to the target system (using the power of the target system).

2.4.1 JP2 setting when the emulator operates as a stand-alone unit and target system power is off

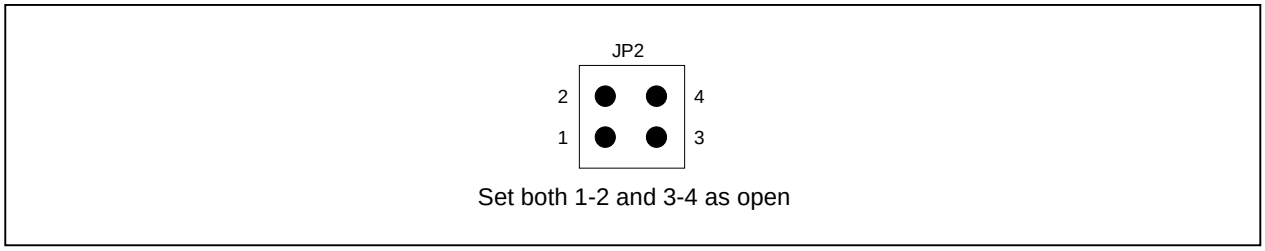
The IE-703102-MS-EM1 operates using the emulator's power supply when the emulator operates as a stand-alone unit and target system power is off. Depending on the product, the condition of the power is as follows.

- **IE-703102-MC-EM1 : V_{DD} = 3.3 V, HV_{DD} = 5.0 V**
- **IE-703102-MC-EM1-A : V_{DD} = 3.3 V, HV_{DD} = 3.3V**

Figure 2-2 shows the JP2 setting.

Caution If the JP2 setting is incorrect, the emulator may be damaged.

Figure 2-2. Power Supply Settings (When the Emulator Operates as a Stand-Alone Unit and Target System Power is Off)



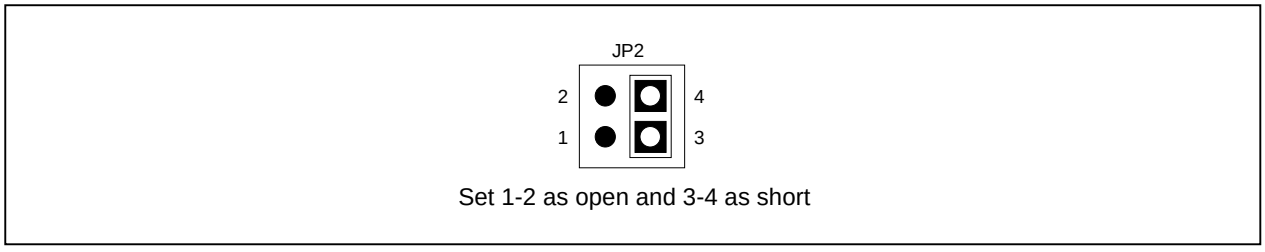
Set both 1-2 and 3-4 as open

2.4.2 JP2 setting when power of the target system is on

The IE-703102-MC-EM1 operates using the target system's power supply when the power of the target system is on. Figure 2-3 shows the JP2 setting.

Caution If the JP2 setting is incorrect, the emulator may be damaged.

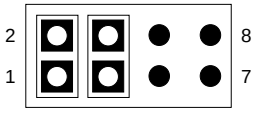
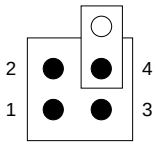
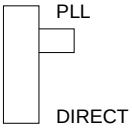
Figure 2-3. Power Supply Setting (When Power of the Target System is On)



Set 1-2 as open and 3-4 as short

[MEMO]

CHAPTER 3 FACTORY SETTINGS

Item	Setting	Remark
JP1		All settings other than those set in the factory are prohibited.
JP2		Setting that supplies the IE-703102-MC-EM1 with the power of the emulator (when the emulator operates as a stand-alone unit and target system power is off).
SW1		Set to PLL mode.
Crystal oscillator	8.000-MHz crystal oscillator is mounted.	If SW1 is set to the factory setting, the CPU operates at 40 MHz.

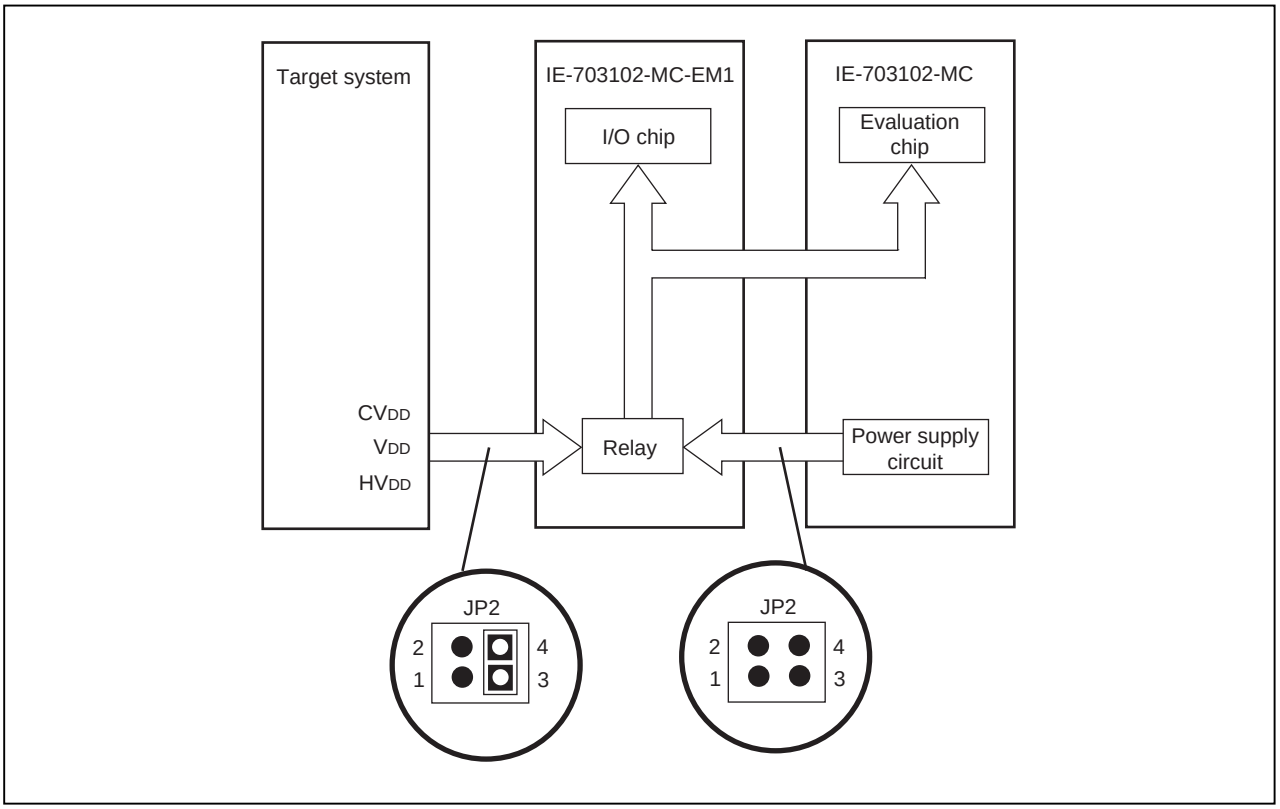
[MEMO]

CHAPTER 4 CAUTIONS

4.1 V_{DD} and HV_{DD} of Target System

(1) V_{DD} and HV_{DD} in the target system are used to operate the circuit in the emulator.
(2) When JP2 is set as 1-2 : open and 3-4 : short, the evaluation chip in the emulator operates on V_{DD} and HV_{DD} from the target system.
(3) When JP2 is set as 1-2 : open and 3-4 : open, the emulator recognizes the target system power is off and operates with the 3.3 V power supply.

Figure 4-1. Schematic Diagram of Power Supply Flow

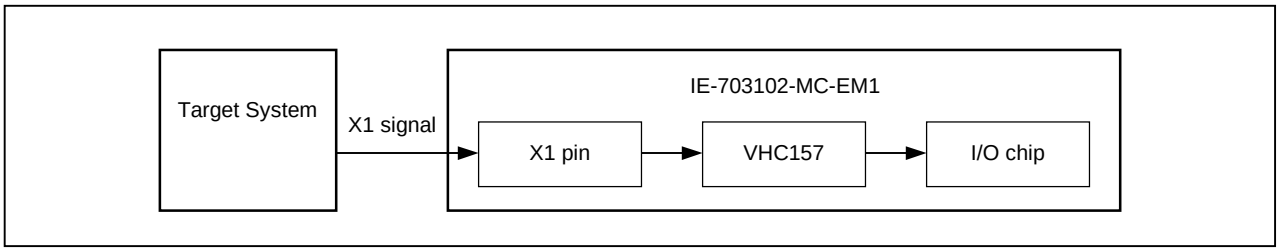


4.2 X1 Signal

The input signal (X1 signal) from the target system is delayed (for $t_{pLH} = t_{pHL} = 13.2$ ns (MAX.)) because it passes through VHC157 before it is input to the I/O chip of the emulator.

In addition, the DC characteristics change. The input voltage becomes $V_{IH} = 2.31$ V (MIN.) and $V_{IL} = 0.99$ V (MAX.). The input current becomes $I_{IN} = \pm 1.0$ μA (MAX.).

Figure 4-2. Diagram of X1 Signal Flow



4.3 Pin Termination

(1) MODE0 to MODE3 pins

When the emulator operates as a stand-alone unit, the operation mode of the emulator is single-chip mode 0. The MODE0 to MODE3 pins are connected as follows.

- MODE0: Connected to V_{SS} via a resistor (33 kΩ). (Pull-down)
- MODE1: Connected to V_{DD} via a resistor (5.1 kΩ). (Pull-up)
- MODE2: Unconnected
- MODE3: Unconnected

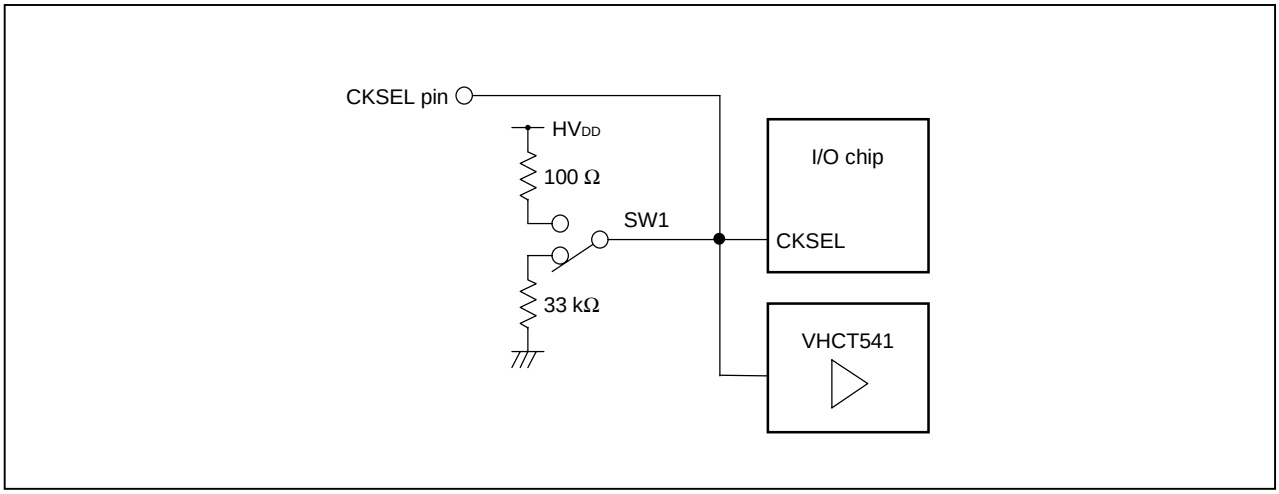
(2) $\overline{\text{RESET}}$ pin

This pin is connected to V_{DD} via a resistor (5.1 kΩ). (Pull-up)

(3) CKSEL pin

Pull-up/pull-down switching is possible with SW1.

Figure 4-3. Circuit Diagram of CKSEL Pin



4.4 Internal RAM and ROM

Because the internal RAM (iRAM) and internal ROM (iROM) capacities of the emulator are set in steps, the memory capacity is different from that of the target device. If access is performed to addresses that exceed the target device capacity, the memory of the emulator is accessed. Memory capacities are as follows.

Table 4-1. Memory Capacity Limitation List

(a) iRAM capacity (Unit: byte)

Target Device	Emulator
1 K	1 K
2 K	2 K
3 K	3 K
4 K (V850E/MS1)	4 K
5 K to 6 K	6 K
7 K to 8 K	8 K
9 K to 10 K	10 K
11 K to 12 K	12 K
13 K to 16 K	16 K
17 K to 20 K	20 K
21 K to 24 K	24 K
25 K to 28 K	28 K
29 K to 36 K	36 K
37 K to 44 K	44 K
45 K to 52 K	52 K
53 K to 60 K	60 K

(b) iROM capacity (Unit: byte)

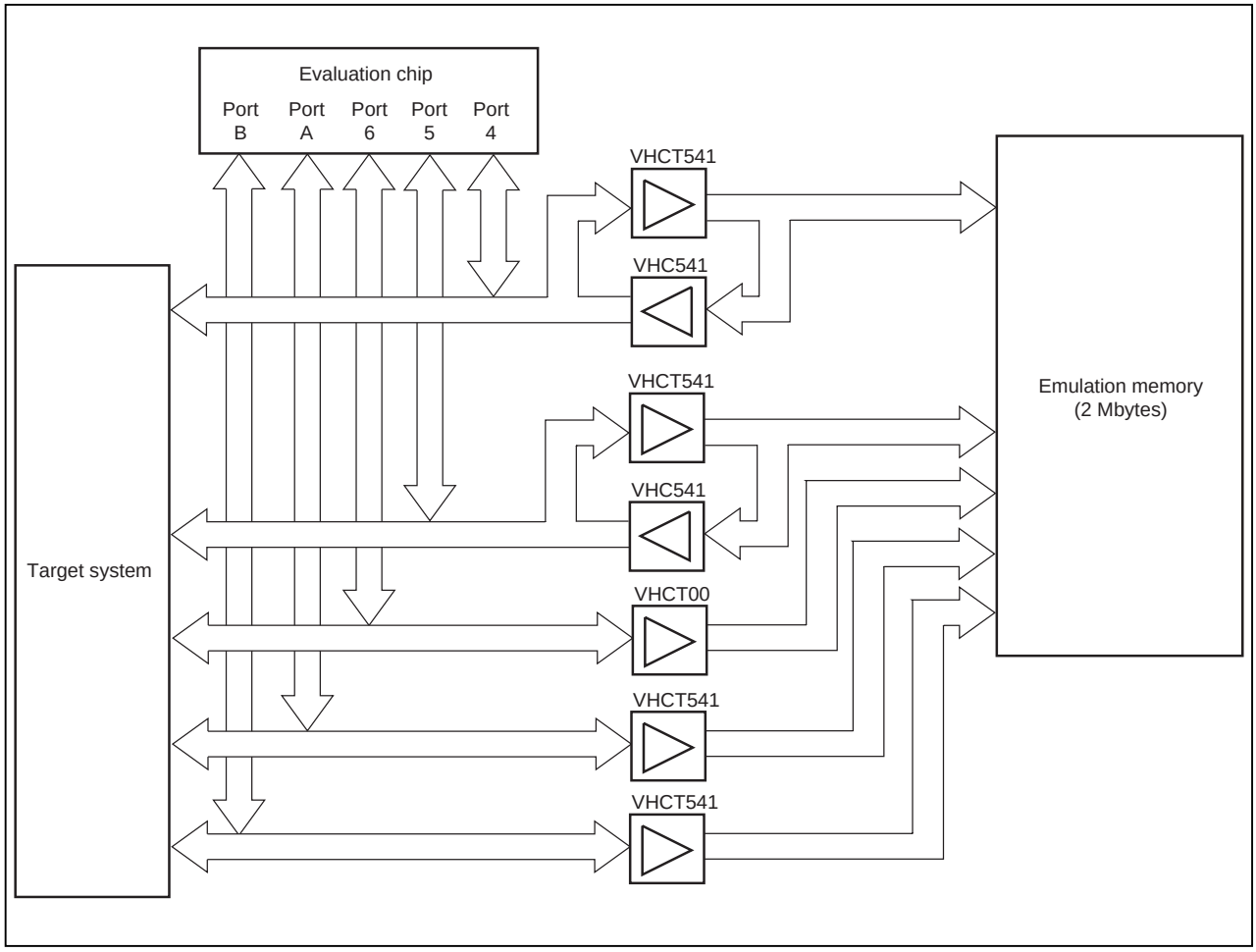
Target Device	Emulator (Emulation Memory)
1 K to 32 K	32 K
33 K to 64 K	64 K
65 K to 128 K(V850E/MS1)	128 K
129 K to 256 K	256 K
257 K to 512 K	512 K[Note]

Note The emulator is mounted iROM emulation memory of 512 Kbytes.

4.5 Port 4 to 6, A, and B

Ports 4 to 6, A, and B are connected to VHCT541, VHC541, and VHCT00, respectively.

Figure 4-4. Circuit Diagram of Port 4 to 6, A, and B



4.6 Bus Interface Pin

There are the following differences between the emulator and the target device in the operation of the pins for bus interface.

Table 4-2. Bus Interface Pin Operation List (1/3)

(a) During break

Pin Name	Waiting for Emulator Command	Internal Memory					External Memory			
		Internal ROM	Internal RAM		Internal Peripheral I/O		Emulation RAM		Target System	
		R	R	W	R	W	R	W	R	W
A0 to A23	**Note**	**Note**					**Note**		**Note**	
D0 to D15	Hi-Z	Hi-Z					**Note**		**Note**	
$\overline{WE}$	H	H					H		**Note**	
$\overline{OE}$	H	H					H		**Note**	
$\overline{RD}$	H	H					H		**Note**	
$\overline{ADV}$/$\overline{BCYST}$	**Note**	H					**Note**		**Note**	
$\overline{UWR}$/$\overline{UCAS}$	H	H					H		**Note**	
$\overline{LWR}$/$\overline{LCAS}$	H	H					H		**Note**	
$\overline{IORD}$	H	H					H		**Note**	
$\overline{IOWR}$	H	H					H		**Note**	
$\overline{CS0}$ to $\overline{CS7}$	H	H					H		**Note**	
$\overline{RAS0}$ to $\overline{RAS7}$	H	H					H		**Note**	
$\overline{REFRQ}$	H	H					H		**Note**	
$\overline{WAIT}$	Invalid	**Note**					Maskable			
$\overline{HLDRQ}$	Maskable	Maskable					Maskable			
$\overline{HLDAK}$	**Note**	**Note**					**Note**			

Note Performs the same operation as the cycle that is generated by the target device program execution.

Remarks 1. R : Read
W : Write

2. H : High-level output
Hi-Z : High-impedance

Table 4-2. Bus Interface Pin Operation List (2/3)

(b) During user program execution

Pin Name	Internal Memory							External Memory					
	Internal ROM		Internal RAM			Internal Peripheral I/O		Emulation RAM			Target System		
	F	R	F	R	W	R	W	F	R	W	F	R	W
A0 to A23	**Note**							**Note**			**Note**		
D0 to D15	Hi-Z							**Note**			**Note**		
$\overline{WE}$	H							H			**Note**		
$\overline{OE}$	H							H			**Note**		
$\overline{RD}$	H							H			**Note**		
$\overline{ADV}$/ $\overline{BCYST}$	H							**Note**			**Note**		
$\overline{UWR}$/ $\overline{UCAS}$	H							H			**Note**		
$\overline{LWR}$/ $\overline{LCAS}$	H							H			**Note**		
$\overline{IROD}$	H							H			**Note**		
$\overline{IOWR}$	H							H			**Note**		
$\overline{CS0}$ to $\overline{CS7}$	H							H			**Note**		
$\overline{RAS0}$ to $\overline{RAS7}$	H							H			**Note**		
$\overline{REFRQ}$	H							H			**Note**		
$\overline{WAIT}$	**Note**							Maskable					
$\overline{HLDRQ}$	Maskable							Maskable					
$\overline{HLDAK}$	**Note**							**Note**					

Note Performs the same operation as the cycle that is generated by the target device program execution.

Remarks 1. F : Fetch
R : Read
W : Write

2. H : High-level output
Hi-Z : High-impedance

Table 4-2. Bus Interface Pin Operation List (3/3)
(c) Refresh cycle

Pin Name	Operation
A0 to A23	**Note**
D0 to D15	**Note**
$\overline{WE}$	**Note**
$\overline{OE}$	**Note**
$\overline{RD}$	**Note**
$\overline{ADV}$/$\overline{BCYST}$	**Note**
$\overline{UWR}$/$\overline{UCAS}$	**Note**
$\overline{LWR}$/$\overline{LCAS}$	**Note**
$\overline{IORD}$	**Note**
$\overline{IOWR}$	**Note**
$\overline{CS0}$ to $\overline{CS7}$	**Note**
$\overline{RAS0}$ to $\overline{RAS7}$	**Note**
$\overline{REFRQ}$	**Note**
$\overline{WAIT}$	Maskable
$\overline{HLDRQ}$	Maskable
$\overline{HLDAK}$	**Note**

Note Performs the same operation as the cycle that is generated by the target device program execution.

4.7 Emulation Memory Operation Timing Difference

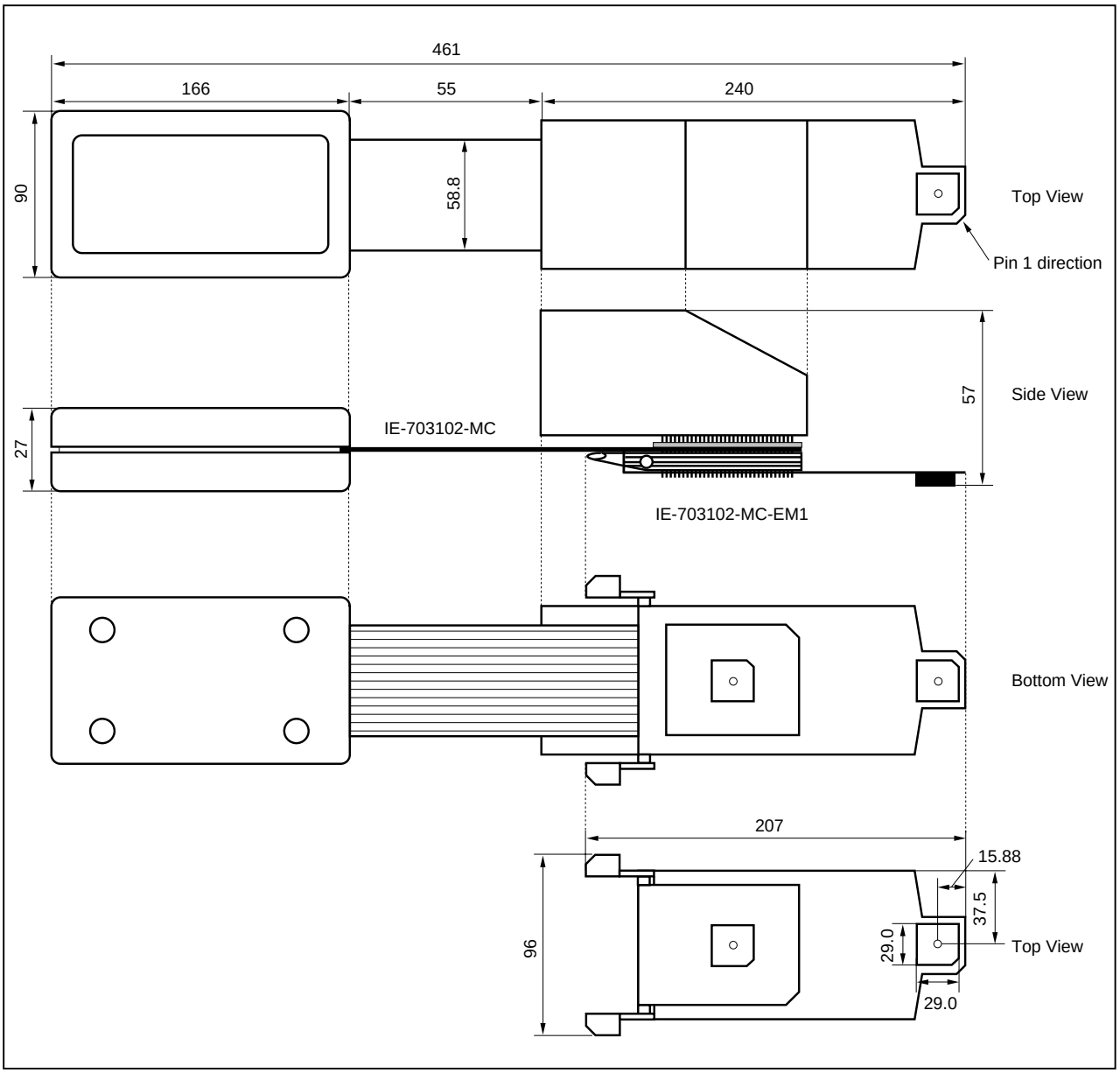
When the area of the DRAM, synchronous flash memory, or page ROM in the target system has been allocated to the emulation memory, the operation timing is the SRAM access timing.

When measuring the performance by using the emulation memory, adjust the setting so that the wait set matches the memory access timing that is actually used.

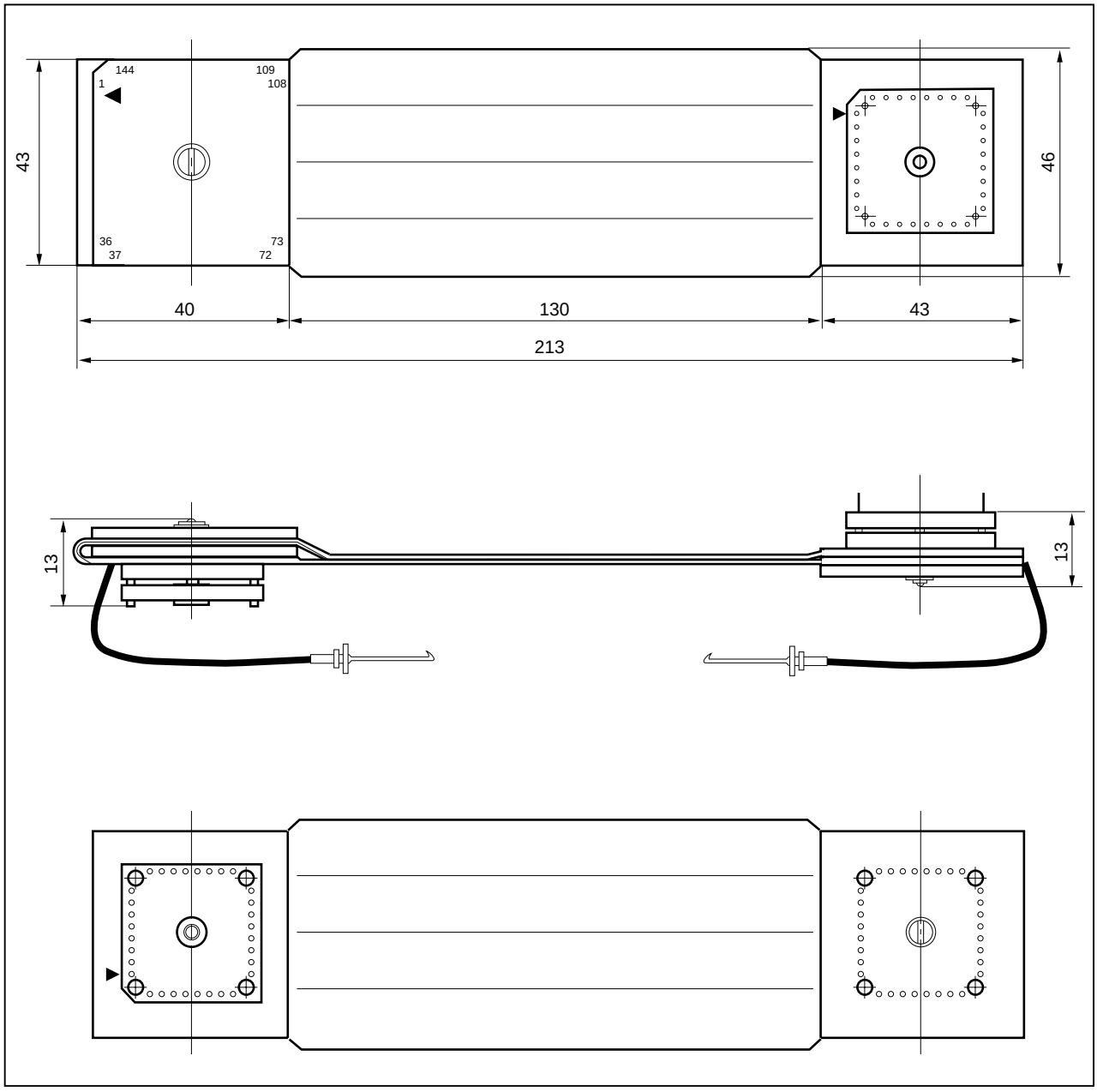
[MEMO]

APPENDIX A DIMENSIONS

(1) IE-703102-MC + IE-703102-MC-EM1 (Unit: mm)

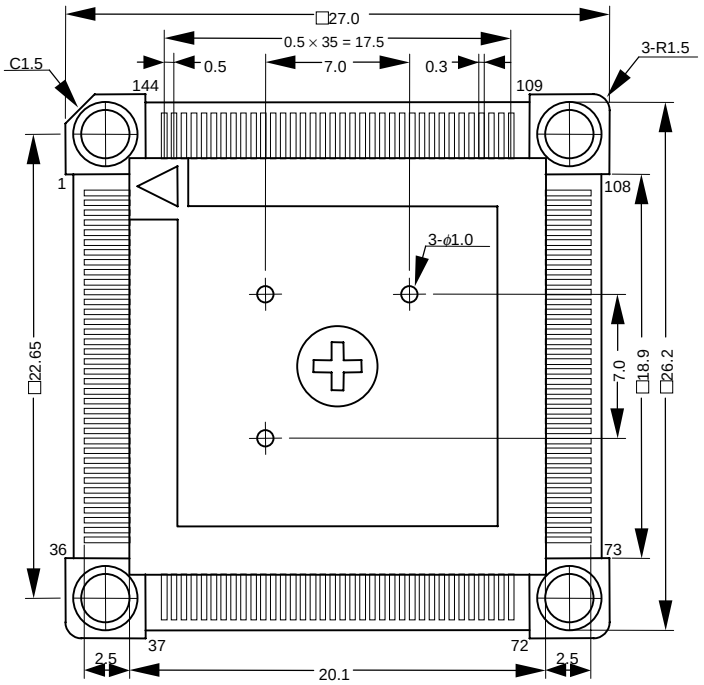


(2) SC-144SD (Unit: mm)

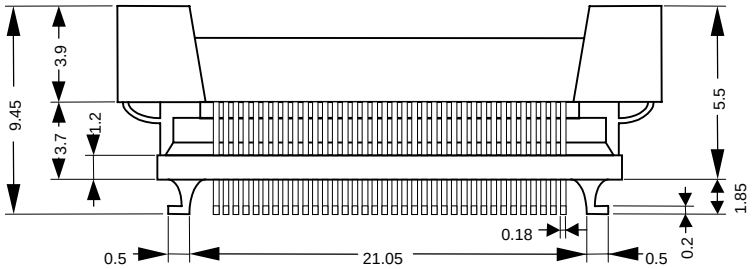


(3) NQPACK144SD (Unit: mm)

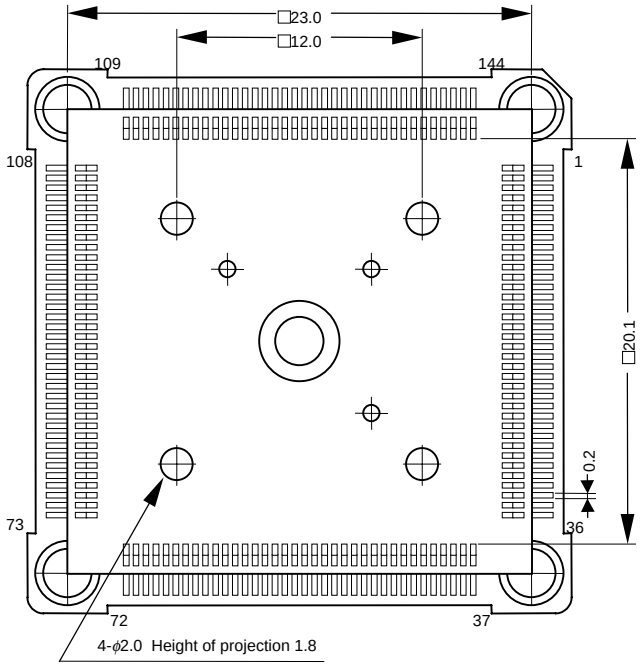
[Top View]



[Side View]

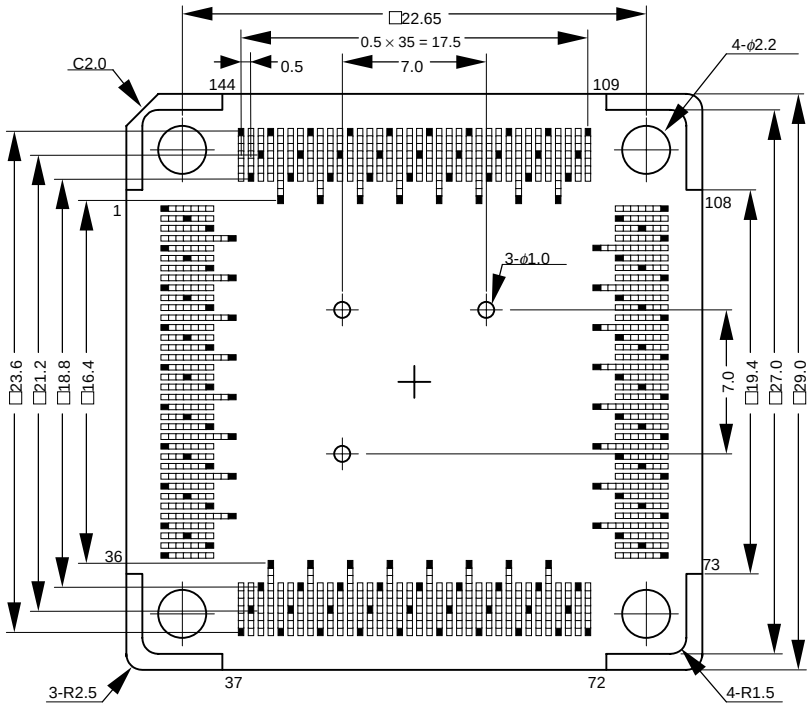


[Bottom View]

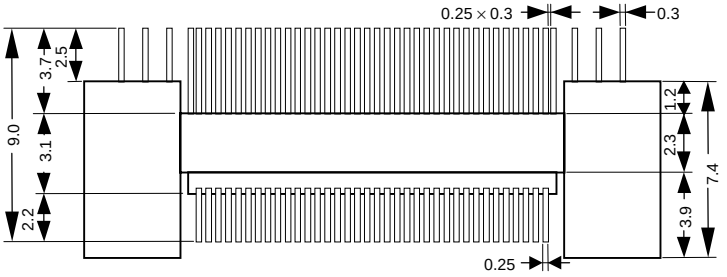


(4) YQPACK144SD (Unit: mm)

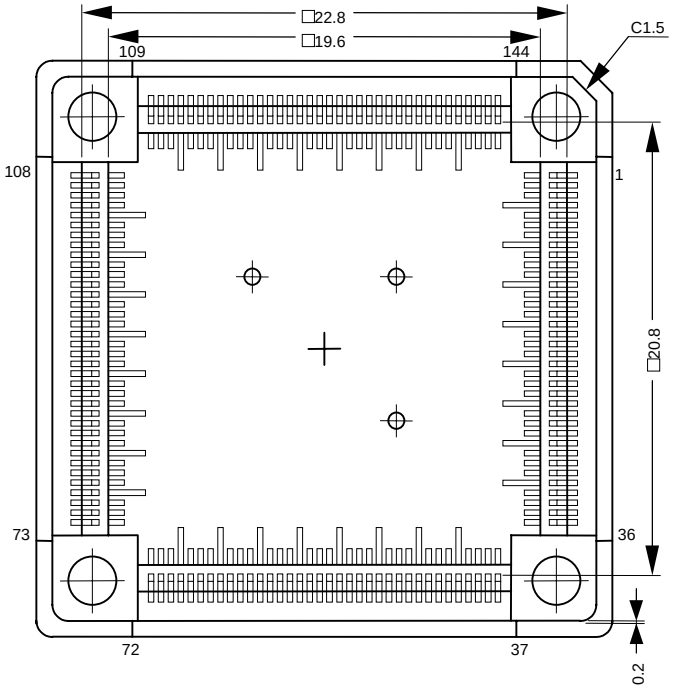
[Top View]



[Side View]

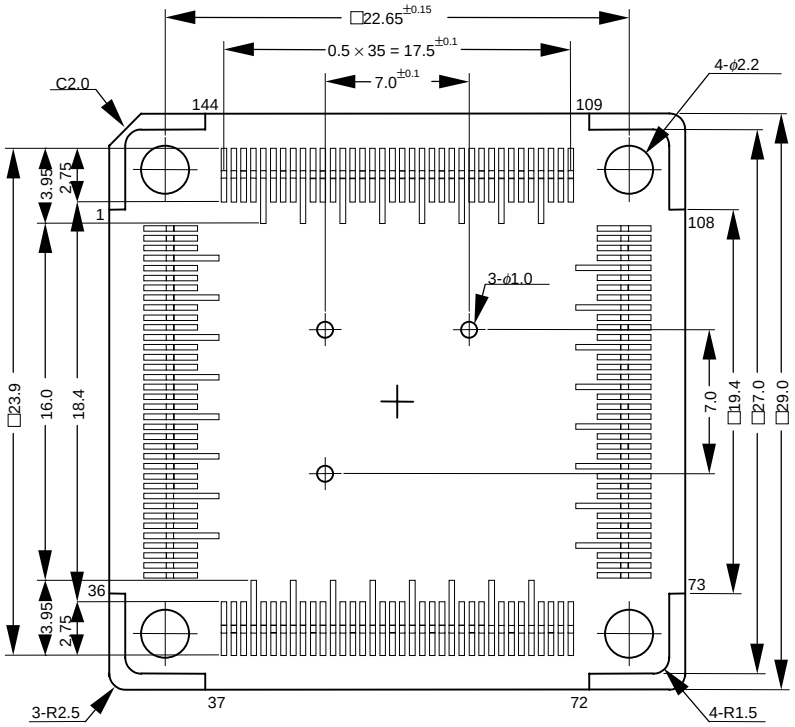


[Bottom View]

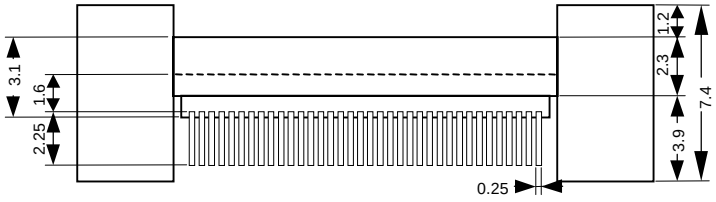


(5) HQPACK144SD (Unit: mm)

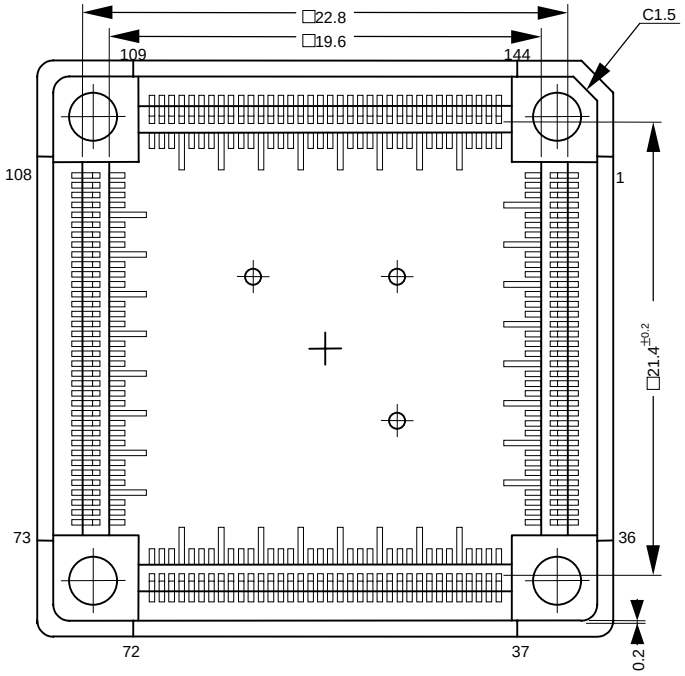
[Top View]



[Side View]



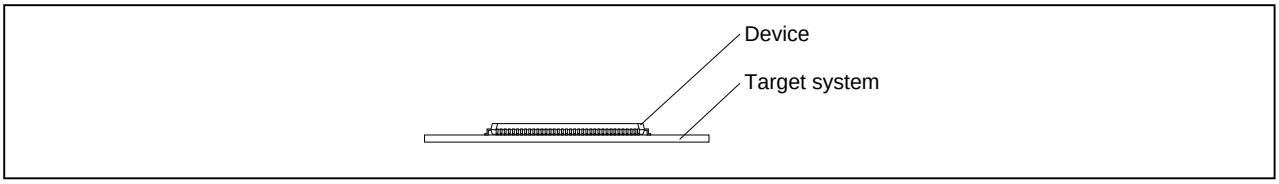
[Bottom View]



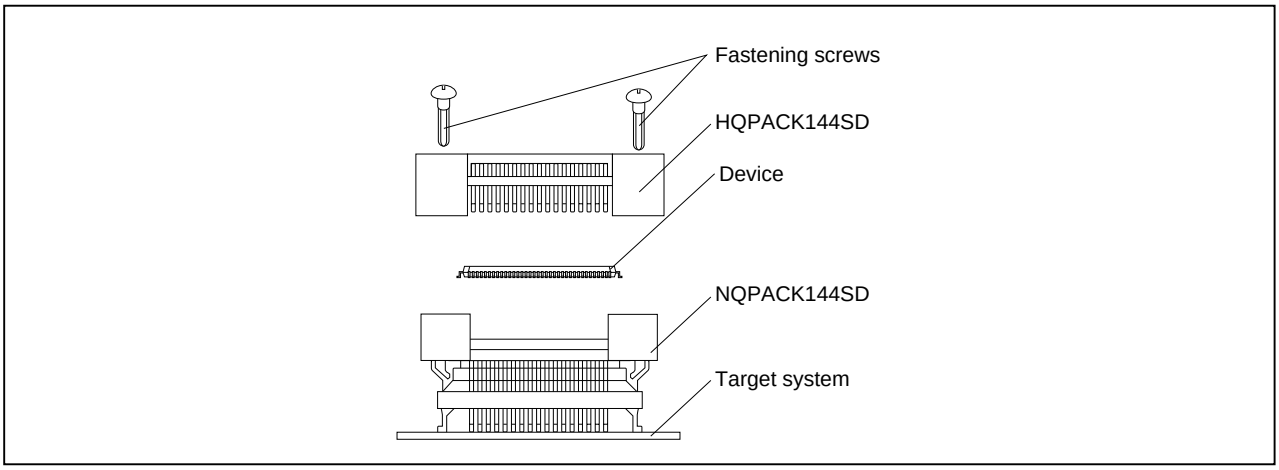
[MEMO]

APPENDIX B EXAMPLE OF USE OF CONNECTOR FOR TARGET CONNECTION

(1) When directly connecting device to target system (Connector for target connection is not used)

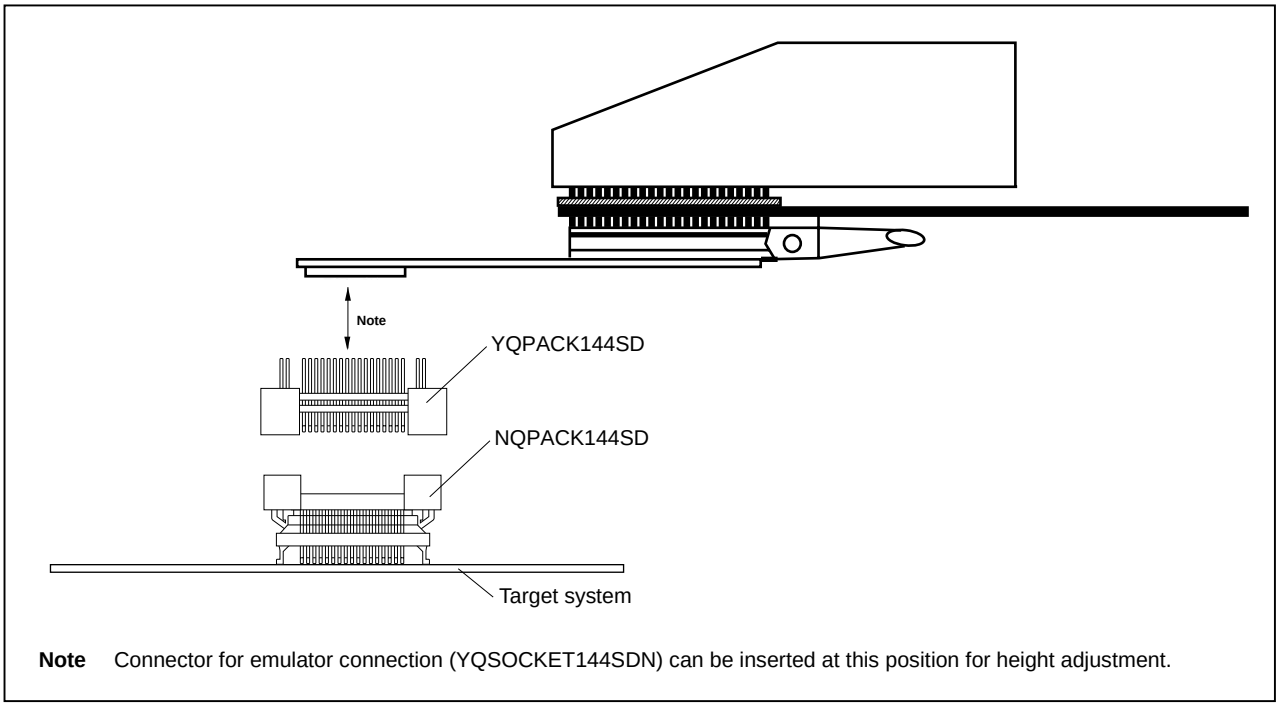


(2) When equipping device by using connector for target connection



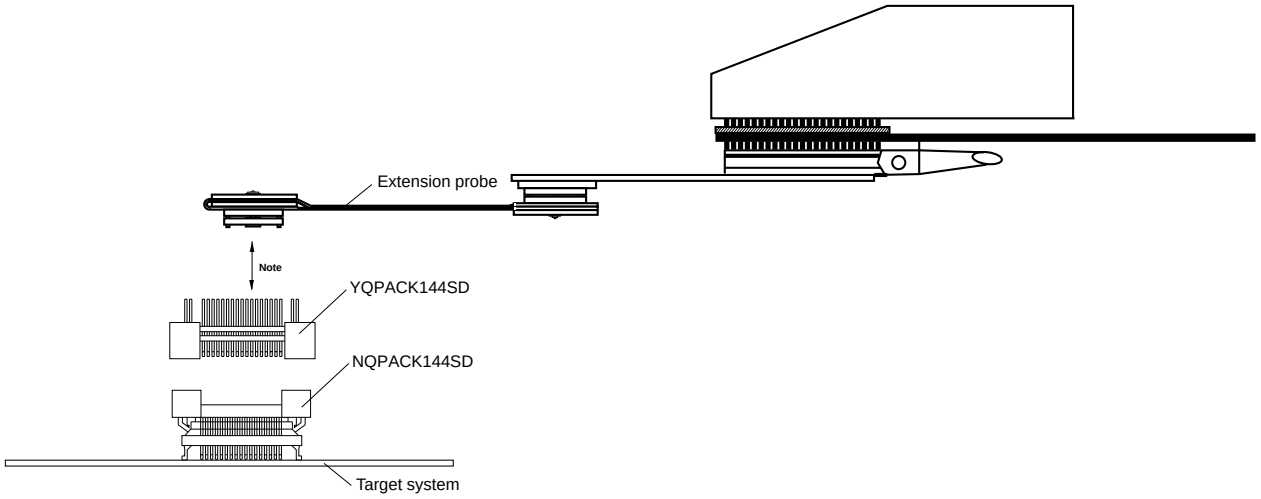
(3) Connection between emulator and target system

(a) When extension probe is not used



Note Connector for emulator connection (YQSOCKET144SDN) can be inserted at this position for height adjustment.

(b) Example of use of extension probe



Note Connector for emulator connection (YQSOCKET144SDN) can be inserted at this position for height adjustment.

APPENDIX C CONNECTORS FOR TARGET CONNECTION

C.1 Use

(1) When mounting NQPACK144SD to target system

<1> Coat the tip of four projections (points) at the bottom of the NQPACK144SD with two-component type epoxy adhesive (cure time longer than 30 min.) and bond the NQPACK144SD to the target system. If not bonded properly, the pad of the printed circuit board may peel off when the emulator is removed from the target system. If the lead of the NQPACK144SD does not coincide with the pad of the target system easily, perform step <2> to adjust the position.

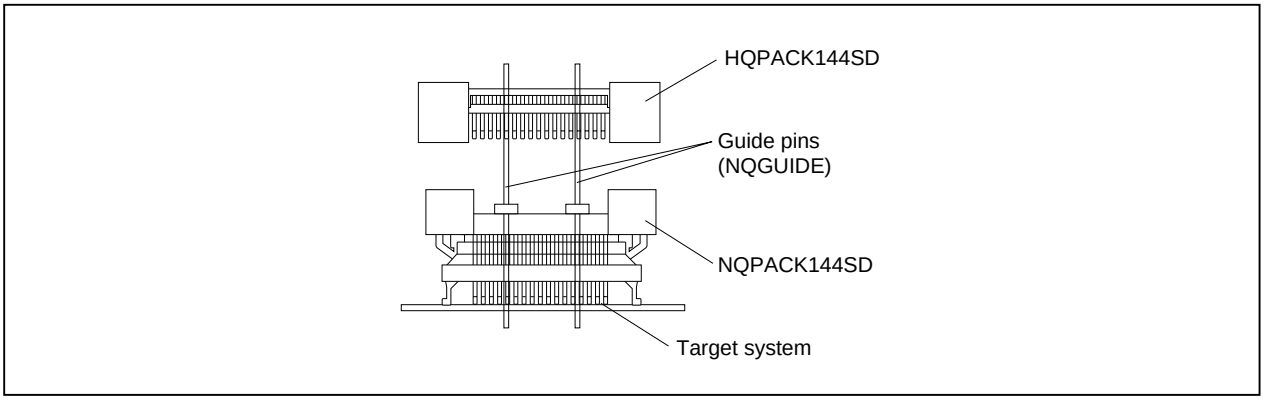
<2> To adjust the position, insert the guide pins for position-adjustment (NQGUIDE) provided with NQPACK144SD into the pin holes at the upper side of NQPACK144SD (refer to **Figure C-1**). The diameter of a hole is ϕ = 1.0 mm. There are three non-through holes (refer to **APPENDIX A DIMENSIONS**).

<3> After setting the HQPACK144SD, solder NQPACK144SD to the target system. By following this sequence, adherence of flux or solder sputtering to contact pins of the NQPACK144SD can be avoided.

Recommended soldering condition… Reflow : 240°C, 20 sec. max.
Partial heating : 240°C, 10 sec. max. (per pin row)

<4> Remove the guide pins.

Figure C-1. Mounting of NQPACK144SD



Remark NQPACK144SD: Connector for target connection
HQPACK144SD: Cover for device installation

(2) When setting device

Caution Check for abnormal conditions such as resin burr or bent pins before setting a device to the NQPACK144SD. Moreover, check that the hold pins of the HQPACK144SD are not broken or bent before setting HQPACK144SD. If there are broken or bent pins, fix them with a thin, flat plate such as a blade.

<1> Make sure that the NQPACK144SD is clean and the device pins are parallel (flat) before setting a device to the NQPACK144SD. Then, after mounting the NQPACK144SD to the target board, set the device and HQPACK144SD (refer to **Figure C-2**).

<2> Using the screws provided with the HQPACK144SD (four locations: M2 × 6 mm), secure the HQPACK144SD, device, and NQPACK144SD.
Tighten the screws in a crisscross pattern with the provided screwdriver or driver with torque gauge (avoid tightening strongly only one screw). Tighten the screws with 0.55 kg·f·cm (0.054 N·m) max. torque. Excessive tightening may diminish conductivity.
At this time, each pin is fixed inside the plastic wall dividers by the contact pin of the NQPACK144SD and the hold pin of the HQPACK144SD (refer to **Figure C-3**). Thus, pins cannot cause a short with pins of neighboring devices.

Figure C-2. Mounting Device

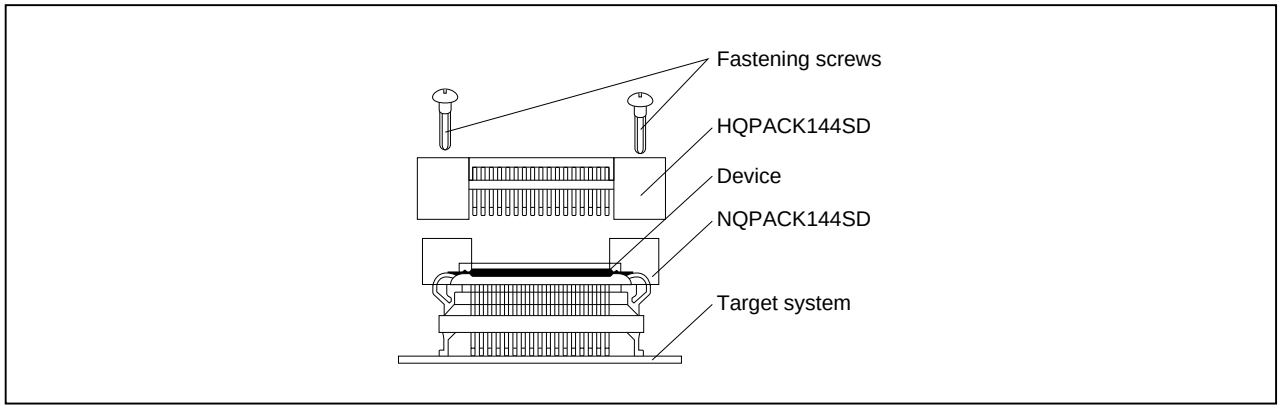
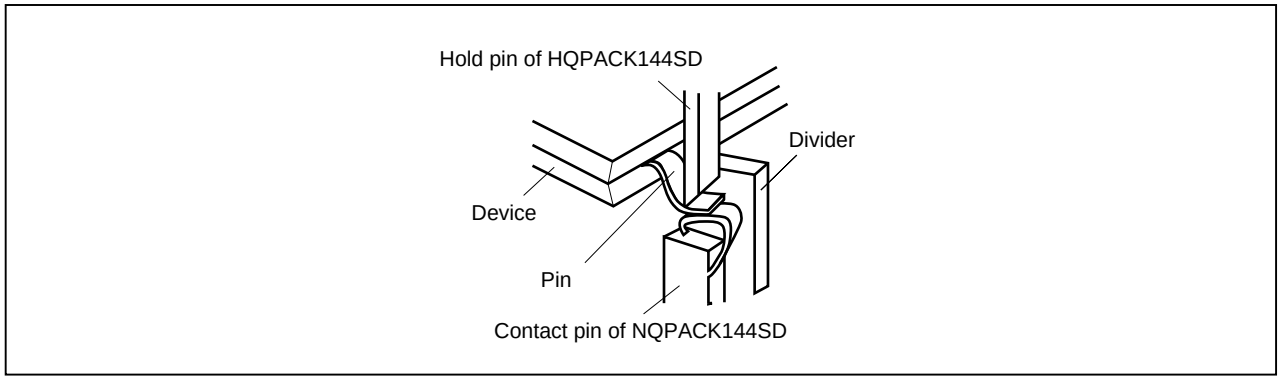


Figure C-3. NQPACK100SD and Device Pin



C.2 Cautions on Handling Connectors

(1) When taking connectors out of the case, remove the sponge while holding the main unit.

(2) When soldering the NQPACK144SD to the target system, cover the HQPACK144SD to protect it against splashing flux.

Recommended soldering conditions… Reflow : 240°C, 20 sec. max.
Partial heating : 240°C, 10 sec. max. (per pin row)

(3) Check for abnormal conditions such as resin burr or bent pins before setting a device to the NQPACK144SD. Moreover, check that the hold pins of the HQPACK144SD are not broken or bent before setting HQPACK144SD. If there are broken or bent pins, fix them with a thin, flat plate such as a blade.

(4) When securing the YQPACK144SD (connector for emulator connection) or HQPACK144SD to the NQPACK144SD with screws, tighten the four screws temporarily with the provided screwdriver or driver with torque gauge, then tighten the screws in a crisscross pattern (with 0.054 N·m max. torque).
Excessive tightening of only one screw may diminish conductivity.
If the conductivity is diminished after screw-tightening, stop tightening, remove the screws and check whether the NQPACK144SD is stained and make sure the device pins are parallel.

(5) Device pins do not have high strength. Repeatedly connecting to the NQPACK144SD may cause pins to bend. When setting a device to the NQPACK144SD, check and adjust bent pins.

[MEMO]

APPENDIX D MOUNTING OF PLASTIC SPACER

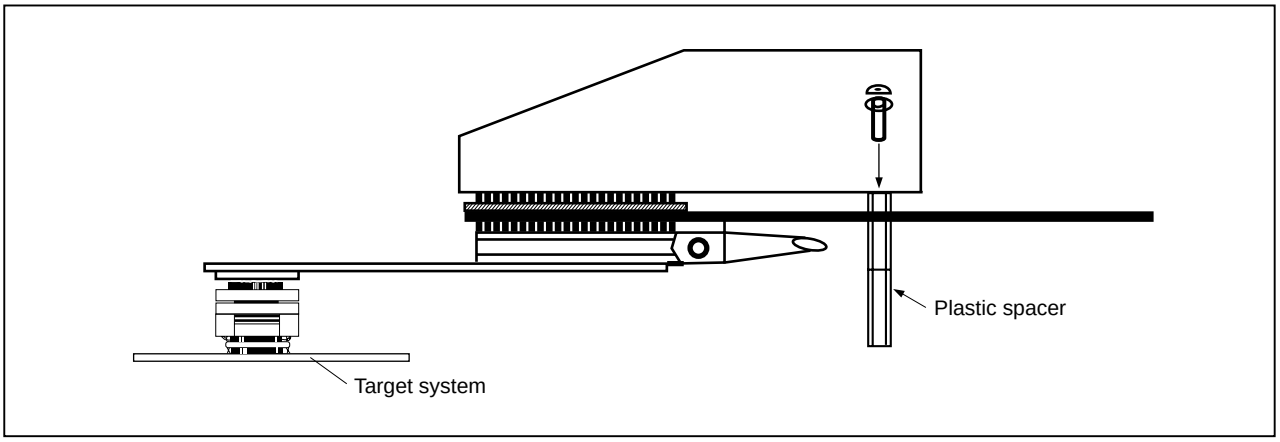
This chapter describes the mounting method for the plastic spacer supplied with the IE-703102-MC.

When using the emulator connected to the target system, mount the plastic spacer as shown in Figure D-1 to fix the pod horizontally.

(1) Mounting IE-703102-MC to plastic spacer

<1> Remove the nylon rivet from the rear part of the pod.
<2> Tighten the plastic spacer with the supplied plastic screw.
<3> To adjust the height, use a user spacer or stand.

Figure D-1. Mounting Method of Plastic Spacer



[MEMO]

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