User Manual

GreenPAK DIP Development Platform

UM-GP-007

Abstract

This user manual provides basic guidelines for the developers to get familiar with the GreenPAK DIP Development Platform. It gives an overview of the hardware, as well as the functional description of this platform, and shows the example projects using SLG46534.

Contents

Figures

Tables

1 Terms and Definitions

DIP	Dual In-Line Package
GND	Ground
GP	General Purpose
IC	Integrated Circuit
IDE	Integrated Development Environment
LED	Light Emitting Diode
LUT	Look Up Table
MCU	Microcontroller Unit
OTP	One-Time Programable
NC	Not Connected
RAM	Random-Access Memory
TP	Test Point
USB	Universal Serial Bus
V_{DD}	Power Supply

2 Introduction

Thank you for choosing Renesas Electronics products. The GreenPAK DIP Development Platform allows you to develop your custom design using GreenPAK mixed signal ICs. You can design your own projects starting from a blank project, or by altering the sample projects provided at https://www.renesas.com/.

2.1 GreenPAK Designer

GreenPAK Designer is an easy-to-use full-featured integrated development environment (IDE) that allows you to specify exactly how you want the device to be configured. This provides you direct access to all GreenPAK device features and complete control over the routing and configuration of a PAK project with just one tool.

With GreenPAK Designer, you can:

- Design the configuration which corresponds to your project needs;
- Verify the project using software interface to GreenPAK DIP Development Platform hardware;
- With simple-to-use and intuitive software and hardware tools you can reduce your project development time and get to market faster.

To start working with GreenPAK Designer please take the following steps:

- Download and install GreenPAK Designer software;
- Configure modules that you will need for your project;
- Interconnect and configure modules;
- Specify the pin out;
- Test your design with the GreenPAK DIP Development Platform.

2.2 Support

Free support for GreenPAK DIP Development Platform is available online at https://www.renesas.com/.

At facebook : https://www.facebook.com/RenesasElectronics/.

GreenPAK Designer will automatically notify you when a new version of software is available. For manual updates please go to https://www.renesas.com/software-tool/go-configure-software-hub.

These resources are also available under the **Help** menu of GreenPAK Designer.

3 Getting Started

3.1 Introduction

This chapter describes how to install and configure the GreenPAK DIP Development Platform. Section 4 provides the details of hardware operation. Section 5 provides an instructions on how to create a simple project example.

3.2 Install Software

GreenPAK Designer software is available free of charge from the Renesas website at https://www.renesas.com/software-tool/go-configure-software-hub page.

3.3 Uninstall Software

The software can be uninstalled in the way typical for your operating system. Please refer to your operating system support documentation if you need the specific instructions or visit Section 2.2 of this document for additional support from Renesas.

4 Hardware

4.1 Overview

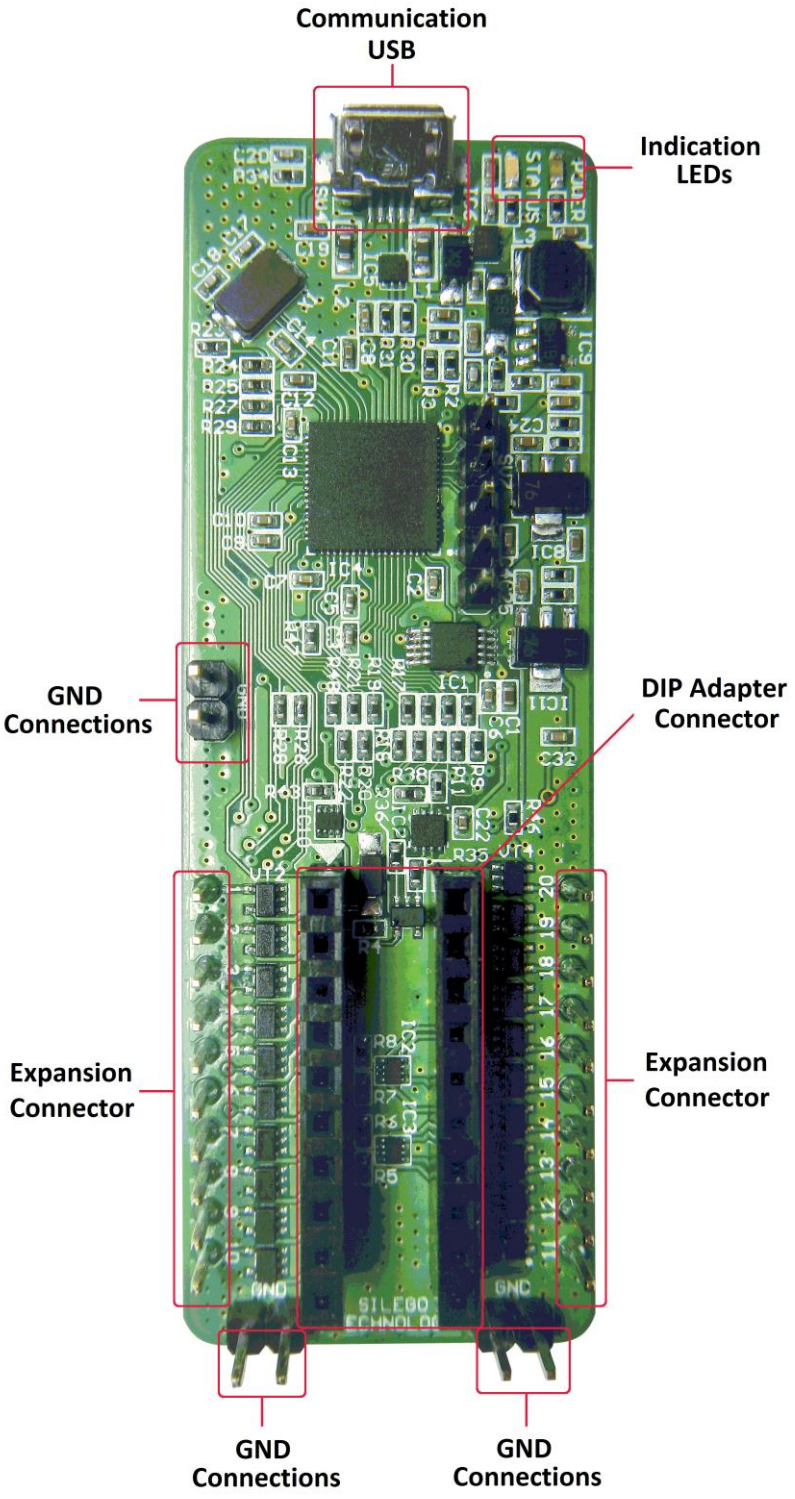


Figure 1: GreenPAK DIP Development Board, Top View

4.2 Functional Description

4.2.1 Power Supply

The main power source of the GreenPAK DIP Development Board is the USB power line. The Development Board can deliver power from 1.7 V to 5.5 V. To provide this power range the Development Board is equipped with a boost converter.

4.2.2 USB Communication

The board has the USB communications interface that uses the USB mini-B connector. This interface provides communication with the software control tool and supplies power to the board, as described in Section 4.2.1.

4.2.3 GND Connections

There are 4 GND pins on the left side, 2 pins on the right side. These can be used for test equipment (oscilloscope, multimeter, and others) ground reference connection or to connect external test circuitry ground.

4.2.4 DIP Adapter Connections

The GreenPAK DIP Development Board should be used with a DIP Adapter board. Its main purpose is to connect the GreenPAK chip to the GreenPAK DIP Development Board. Information about DIP Adapters is available online at https://www.renesas.com/SLG4DVKDIP#documents.

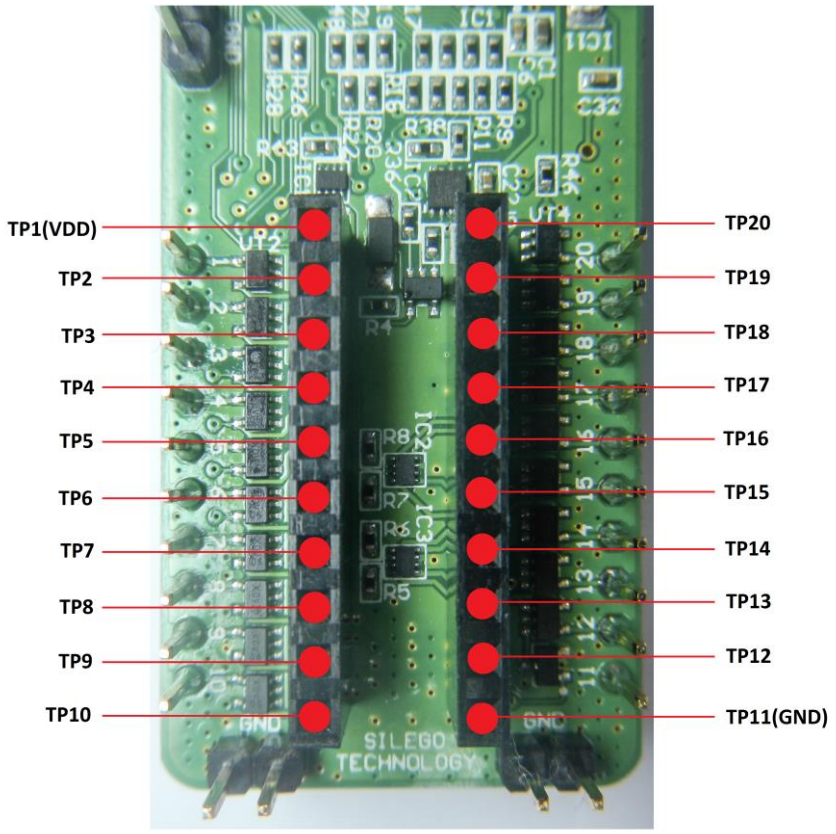


Figure 2: DIP Adapter Connector Pinout

4.2.5 Expansion Connector

This 20-pins connector is in the right and left bottom part of the Development Board. The Expansion Connector is a standard 0.1” female connector compatible with breadboard, see Figure 3.

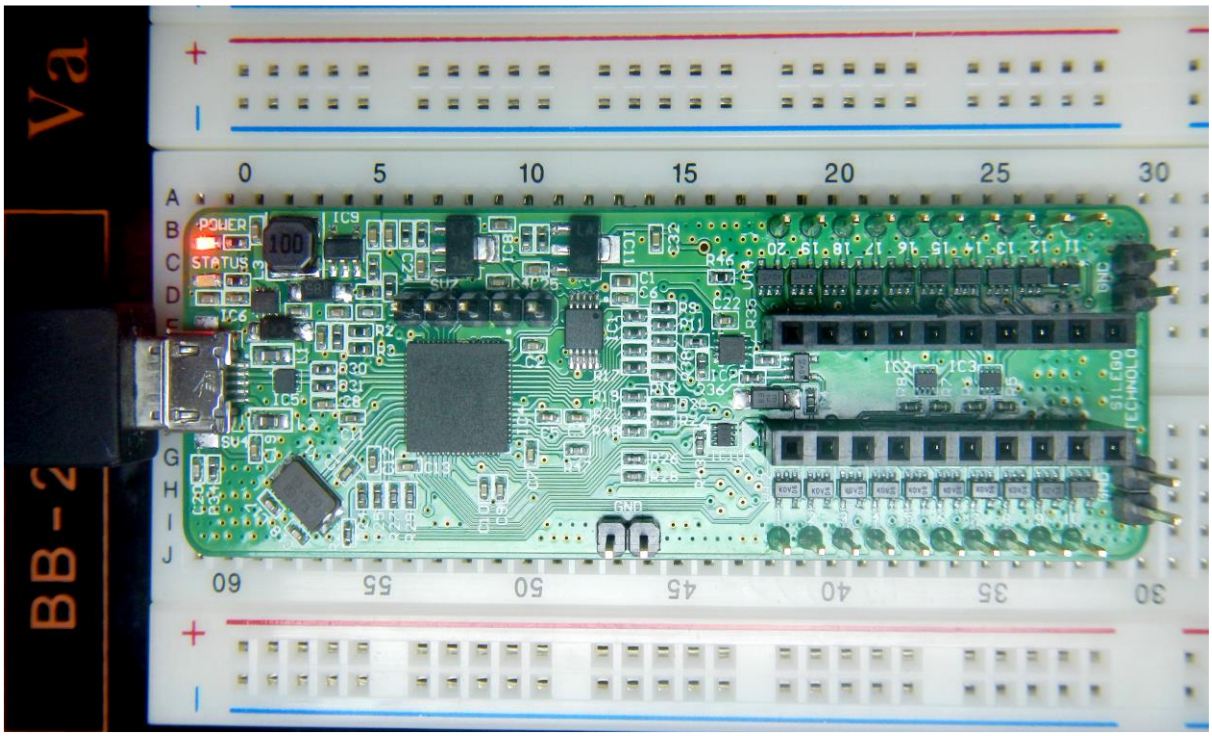


Figure 3: Breadboard with GreenPAK DIP Development Board

This port was designed to connect the GreenPAK DIP Development Board to external circuits and apply external power, signal sources, and loads. It can be used to apply the GreenPAK chip into your custom design with minimal additional tools.

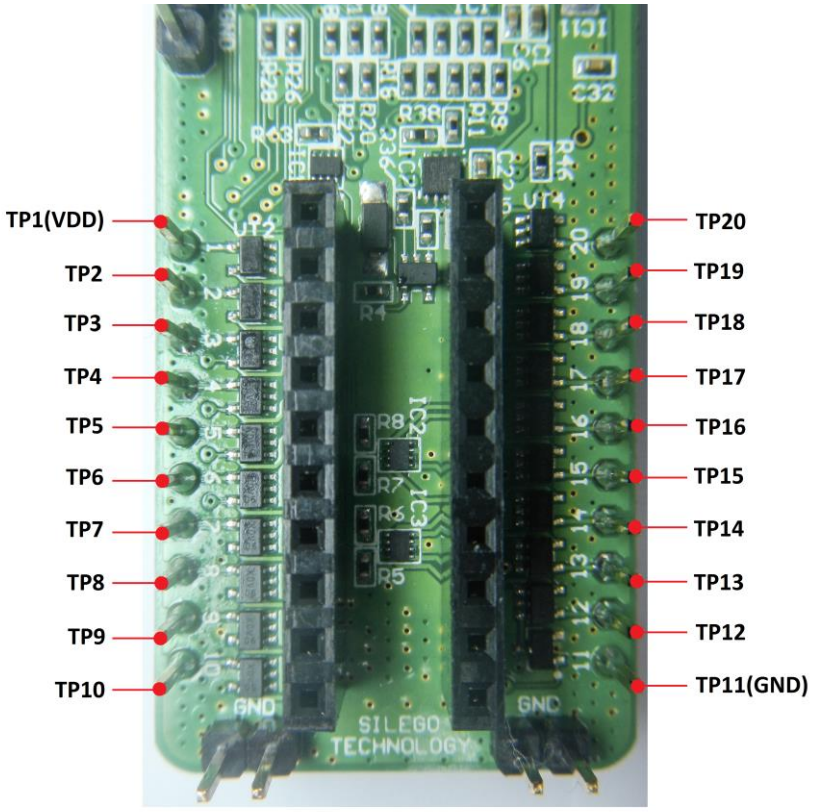


Figure 4: Expansion Connector Pinout

Each pin, except GND and NC, is controlled through individual analog switch. GreenPAK Designer can enable or disable external pins, as it is shown on Figure 5. There is no individual control of each key: when one key is turned on, all others are also turned on.

Figure 5: Expansion Connector Control in GreenPAK Designer

The Expansion Connector is enabled only in Emulation mode or Test mode. To enter either of these two modes, the target GreenPAK device must be inside the socket the DIP Adapter Connector. When the Test mode button is pressed, the software will first read the chip to verify if it was inserted correctly, and then configure the GreenPAK DIP Development Board as it was set in Emulation mode. After the Emulation button is pressed, the software will automatically perform the following steps:

- Check chip presence;
- Open all expansion port switches (allowing external signals/loads to be left connected to Expansion Connector);
- Load target configuration into the target GreenPAK device using internal power;
- Configure Development Board as it was selected in Emulation Tool window.

Note that the GreenPAK device has internal OTP memory which is normally loaded into RAM registers at initialization time. “Emulation mode” will bypass this load and write the updated version of the project directly into the RAM register inside the GreenPAK chip many times, but after power loss all internal data will be lost. Also, when the GreenPAK chip is already programmed - user can use Emulation mode

to load another project and test it on the emulation tool during the Emulation mode, in that case emulation data will be cleared. The “Emulation mode” is not necessary for checking programmed parts: in this case the “Test mode” will supply power to the device, which will perform the standard load of configuration data from OTP to RAM.The difference between the “Emulation” and the “Test mode” is that in the “Test mode” the process of loading configuration memory is skipped and after the chip power the OTP memory loads into RAM registers.

The Expansion Connector has the following type of connections:

1. V_{DD}
2. GND
3. Data

The V_{DD} connection allows the user to both use internal power supply to power the external circuit, and use external power source as the on-board chip power. This selection to use either internal or external power is made in the Emulator Controls window.

The GND connection is connected directly to the GreenPAK DIP Development Board ground and cannot be controlled or switched.

Data connections are the easiest way to connect external signals to the GreenPAK chip. They are software controlled switches that are controlled in the Emulator Controls window.

4.2.6 Pins Connectivity

The Socket connector has the following type of connections:

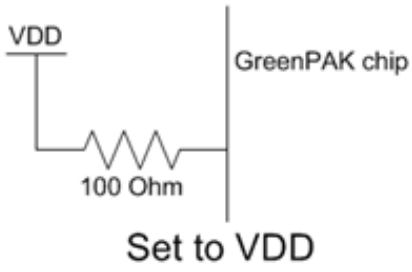
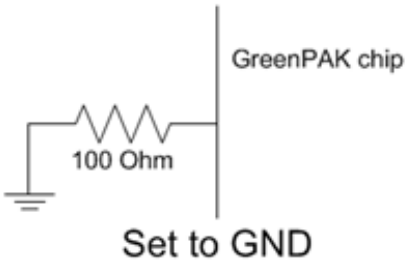
1. V_{DD}
2. GND
3. Data

The GreenPAK DIP Development Board supports connecting five types of loads and signal sources. Each source has its own special purpose.

For V_{DD} pins is only available a signal generator connection.

For the Data pins the following connections are available: V_{DD}, GND, Pull-up, Pull-down, Configurable Button.

Table 1: Data Pins Connections Schematics

Connect PIN to V_{DD} through 100 Ω resistor		Connect PIN to GND through 100 Ω resistor	

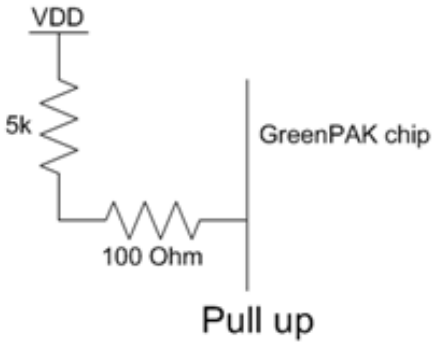
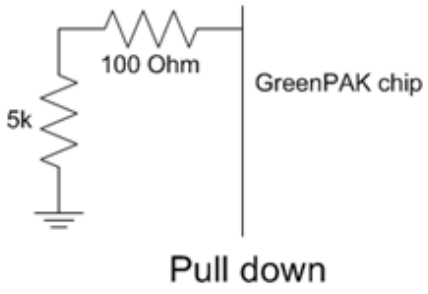
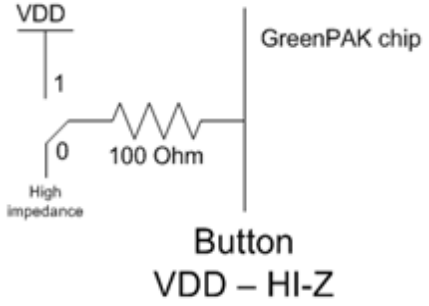
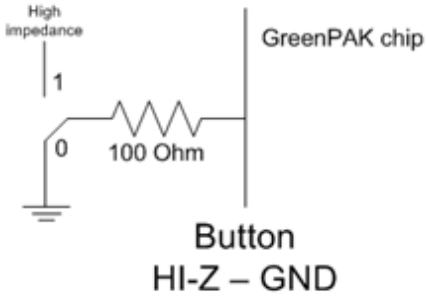
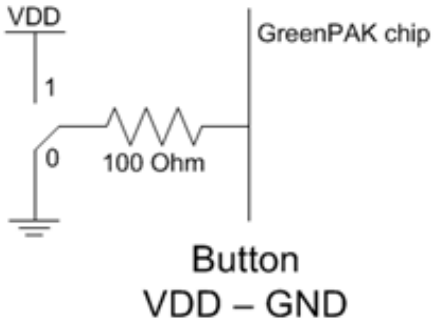
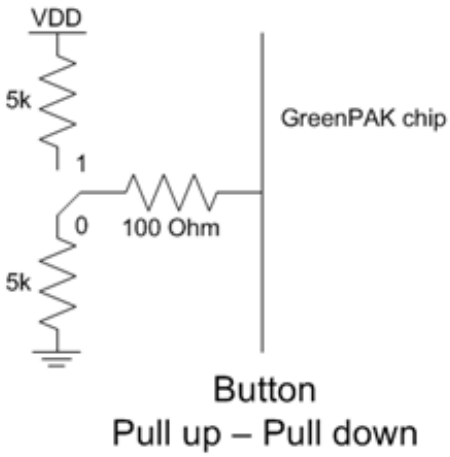
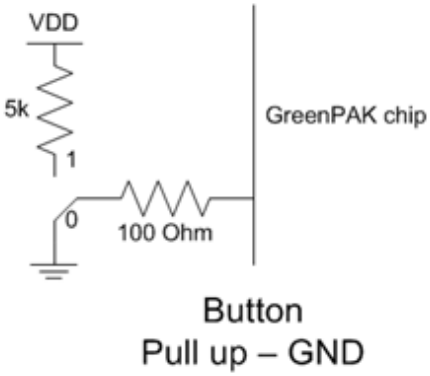
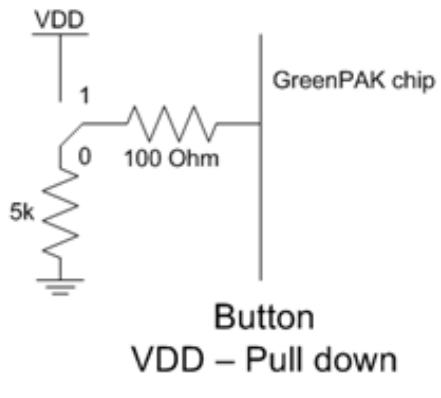
Connect PIN to V_{DD} through MCU 5 kΩ Pull-up resistor + 100 Ω resistor		Connect PIN to GND through MCU 5 kΩ Pull-down resistor + 100 Ω resistor	
Upper connection to V_{DD} through 100 Ω resistor; bottom connection to high impedance MCU input		Upper connection to high impedance MCU input; bottom connection to GND through 100 Ω resistor	
Upper connection to V_{DD} through 100 Ω resistor; bottom connection to GND through 100 Ω resistor		Upper connection to V_{DD} through MCU 5 kΩ Pull-up resistor + 100 Ω resistor; bottom connection to GND through MCU 5k Pull-down resistor + 100 Ω resistor	
Upper connection to V_{DD} through MCU 5 kΩ Pull-up resistor + 100 Ω resistor; bottom connection to GND through 100 Ω resistor		Upper connection to V_{DD} through 100 Ω resistor; bottom connection to GND through MCU 5 kΩ Pull-down resistor + 100 Ω resistor	

Figure 6 shows the schematic connection of the GP V_{DD} pins.

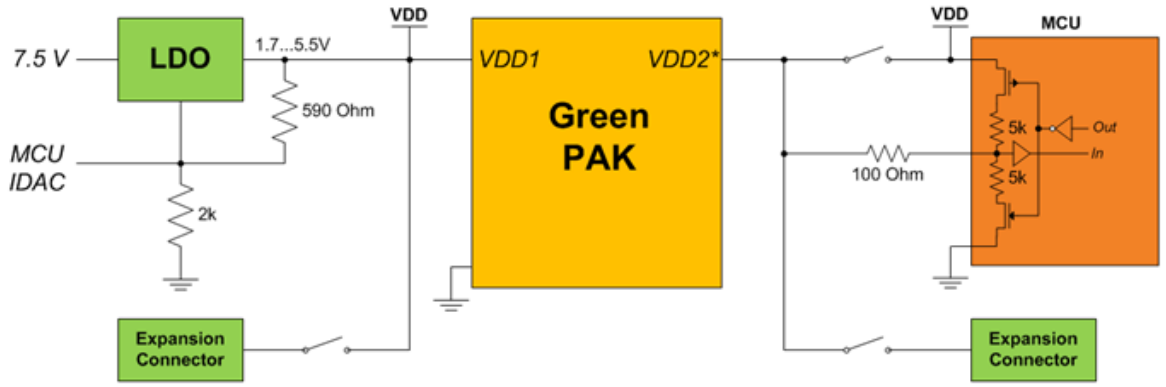


Figure 6: Schematic Connection of the V_{DD} Pin

Note 1 If chip has V_{DD2}. For more information see chip datasheet.

Figure 7 shows the schematic connection of the GP data pins.

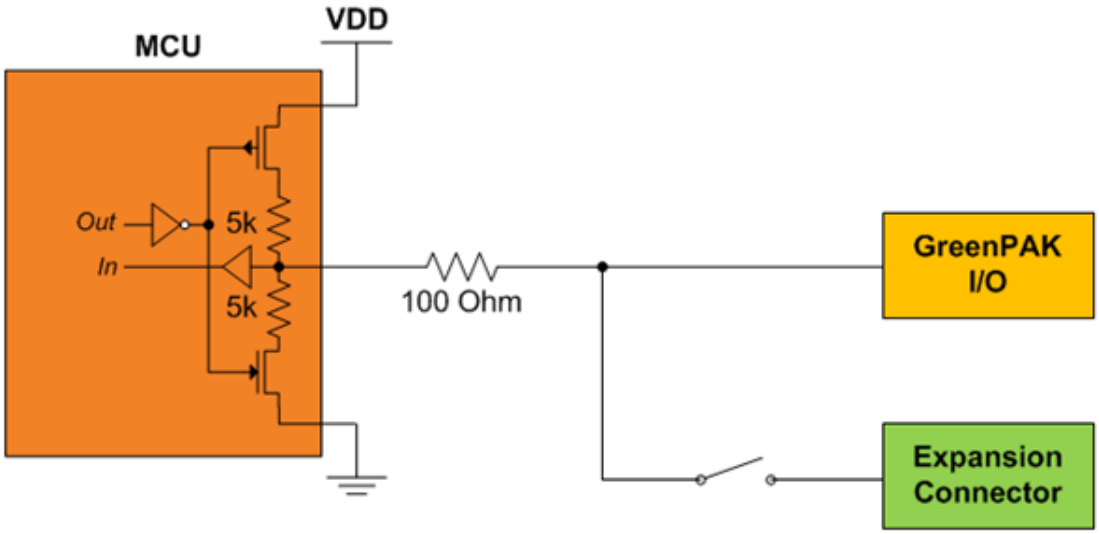


Figure 7: Schematic Connection of the Data Pin

4.2.7 Chip PIN versus Development Board Test Point

Before you start working with a chip you need to understand the difference between such concepts as PIN (chip pin) and TP (the Development Board test point). Figure 8 shows where PINs and TPs are.

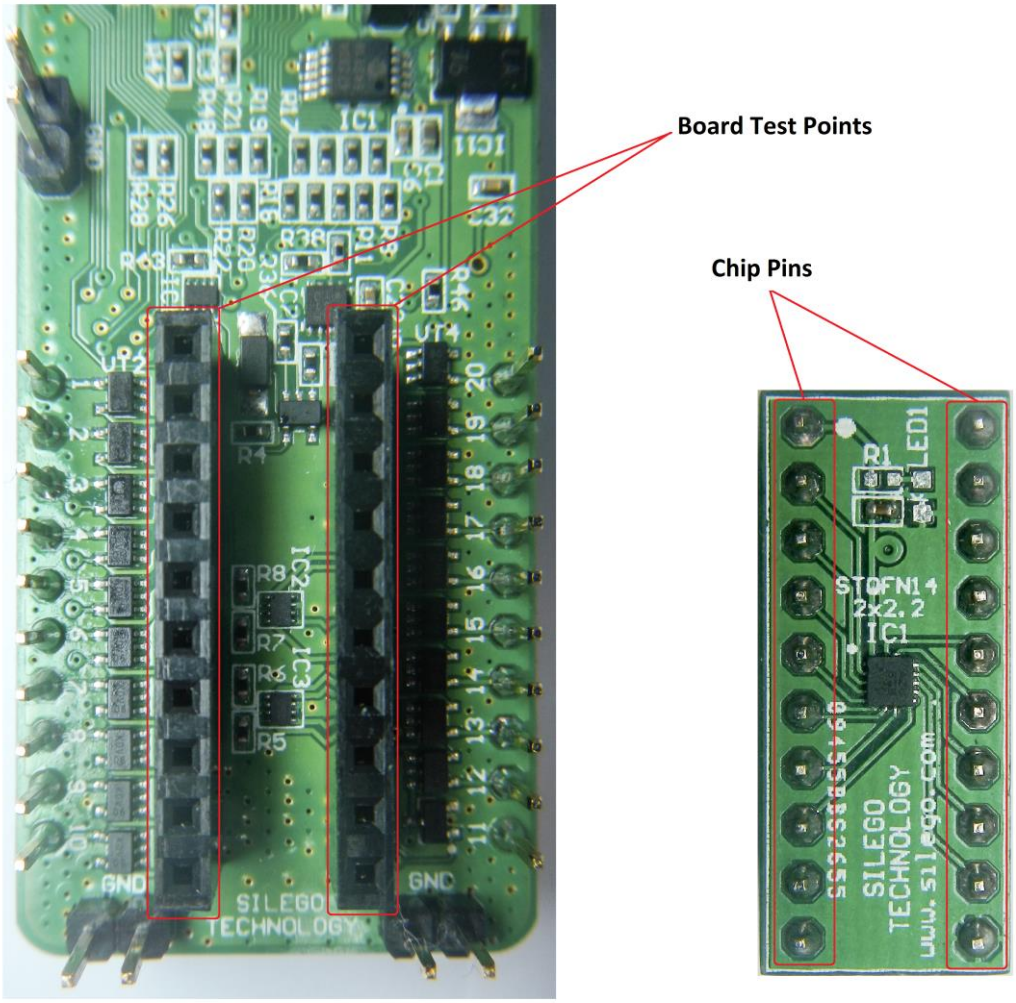


Figure 8: Pins and TPs Location

PINs refer to the physical pins that are on the chip package (their marking can be seen in the datasheet). TPs refer to the DIP Adapter and Expansion connector pins. TP and PIN numbers may not match since different PINs on the chip have different functions, see Figure 9.

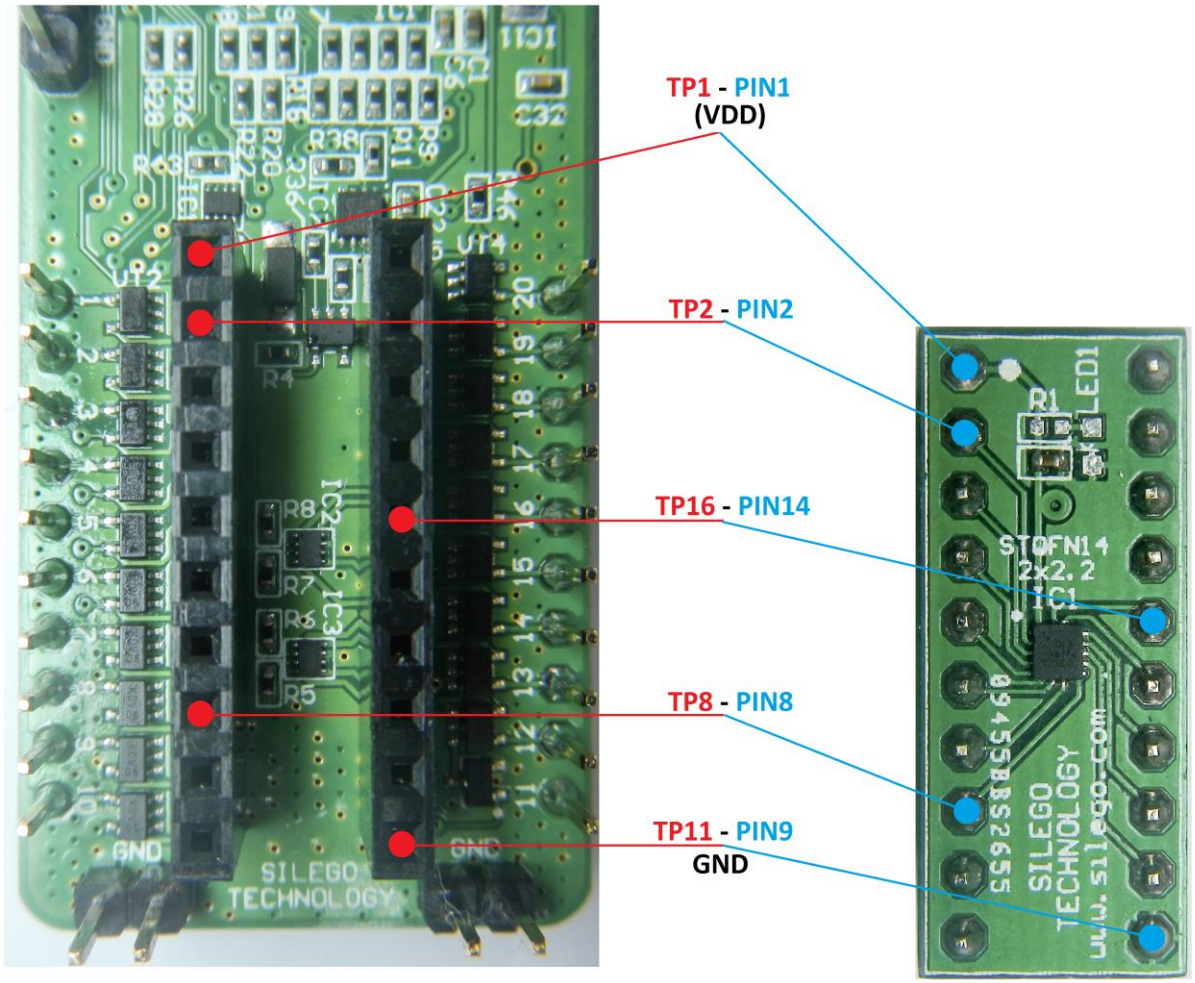


Figure 9: Pins and TPs Accordance (for SLG46534)

5 Example Projects using SLG46534

5.1 Project: Counter with Clock Enable

Blocks required:

- 1 digital input
- 2 digital outputs
- 2 Look Up Tables with two inputs
- 1 Counter
- 1 Oscillator

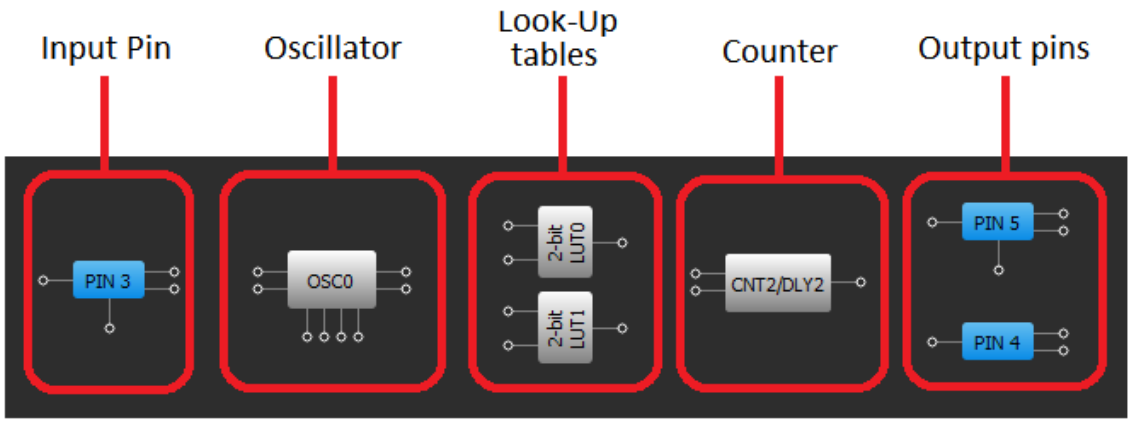


Figure 10: GreenPAK Designer Components

All these components can be found in Components List. If there are no components on the work area - make sure this component is enabled by checking appropriate boxes.

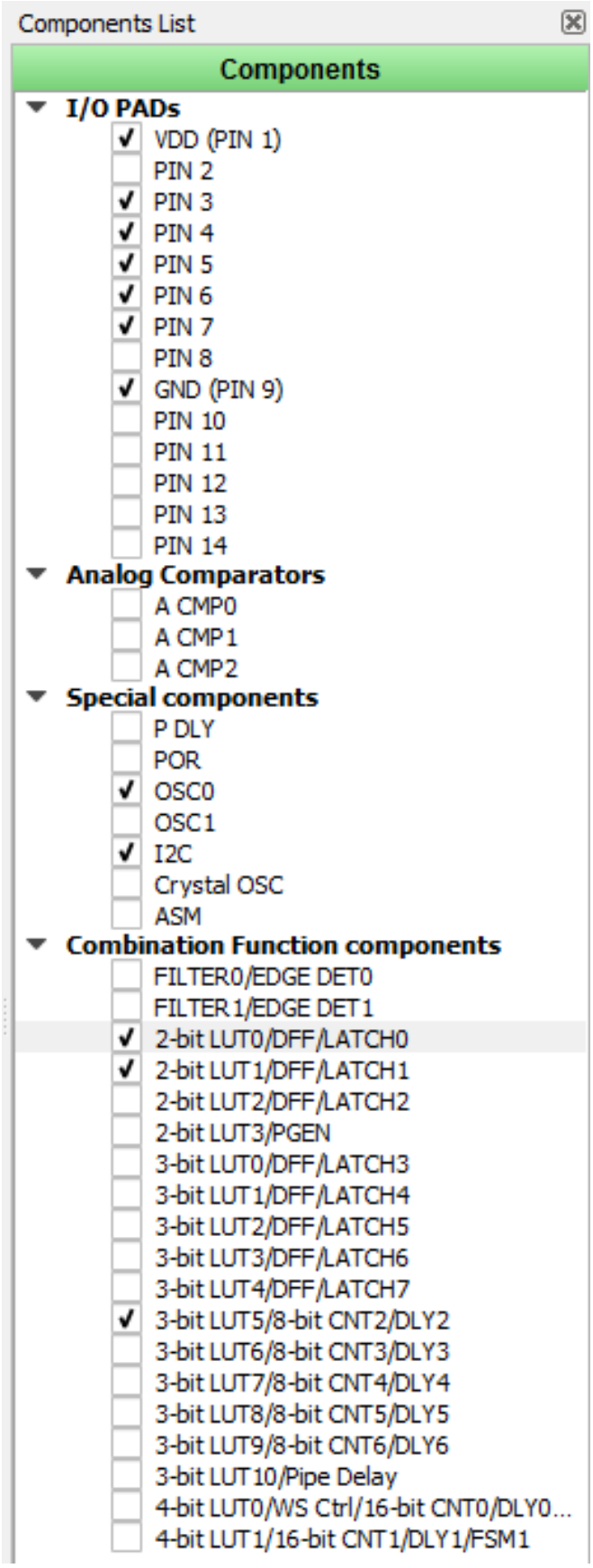


Figure 11: GreenPAK Designer Components List

Table 2: GreenPAK Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	V_{DD}	PWR	Supply Voltage
3	Enable	Digital Input	Digital Input
4	Counter Output	Push-Pull Output	Digital Output
5	Oscillator Output	Push-Pull Output	Digital Output
9	GND	GND	Ground

All components used in this project are shown on Figure 10. Next step is to configure selected blocks. Double click on PIN4 to open “Properties” panel. Select “Digital output” in **I/O Selection** field and then select “1x push pull” from the drop-down menu in **Output mode** field and hit “Apply” button. Make the same settings for PIN5.

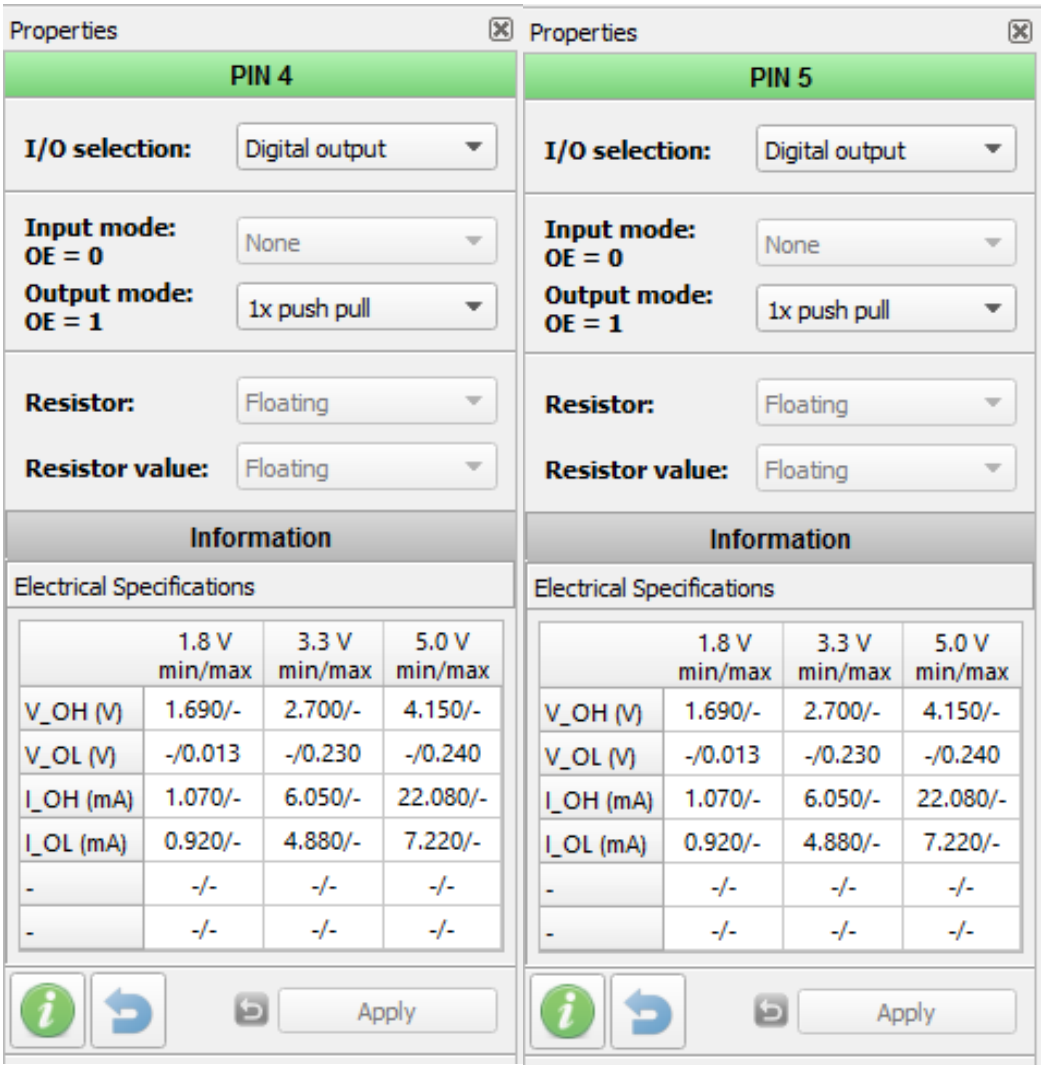


Figure 12: Pin 4, 5 Mode

The next component in this design is Look Up Table. First Look Up Table (LUT0) is used to generate logic “1” only when there are high logic levels on both inputs (AND gate). Select AND gate from “Standard gates” drop-down menu or set table manually. Second Look Up Table (LUT1) is configured as NOR gate. It is used to generate reset signal for counter on PIN3 falling edge.

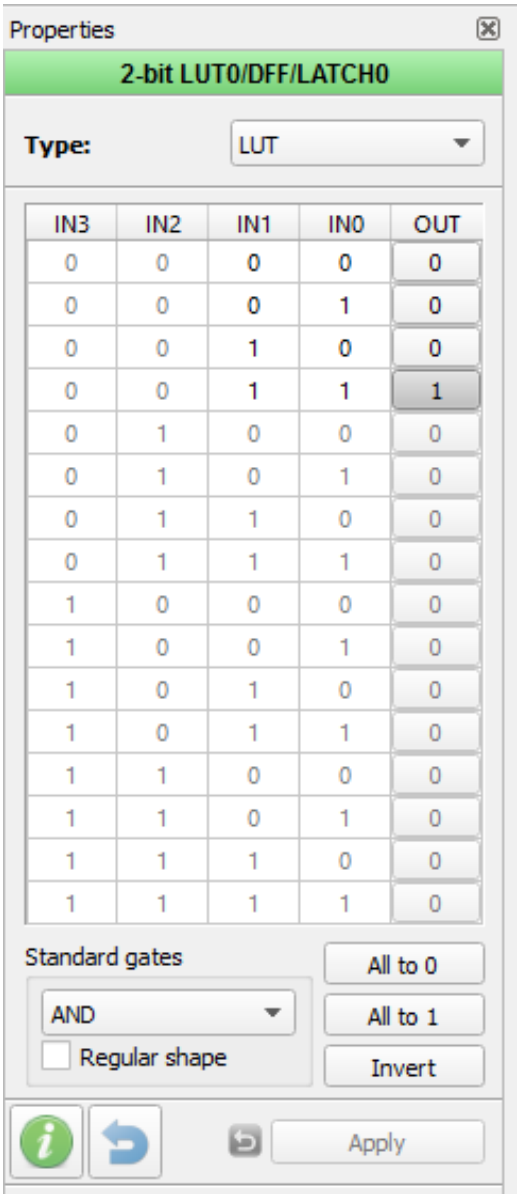


Figure 13: Look Up Table Properties Configured as an AND Gate

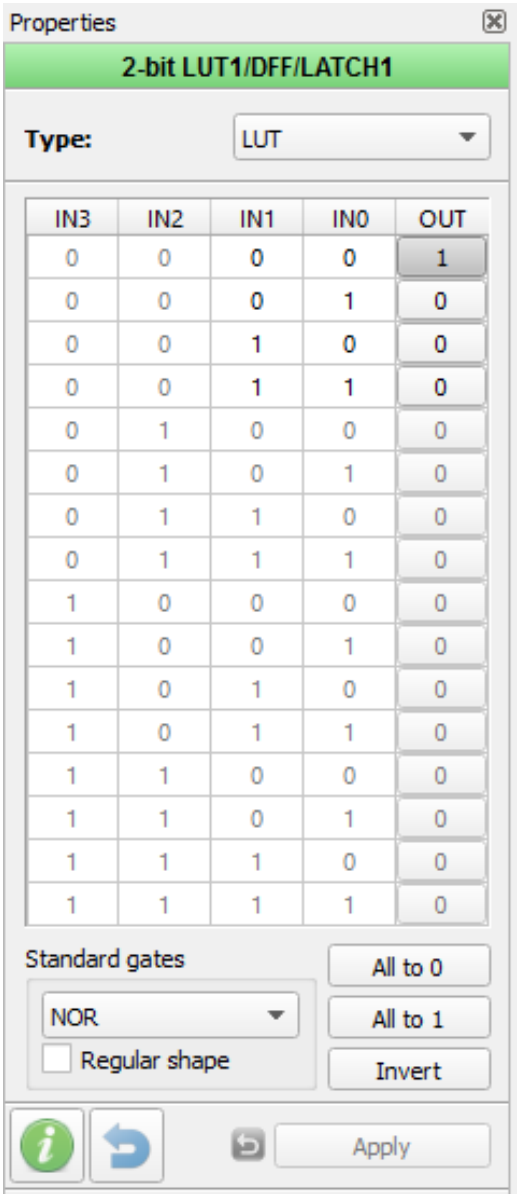


Figure 14: Look Up Table Properties Configured as a NOR Gate

Figure 15 shows counter properties.

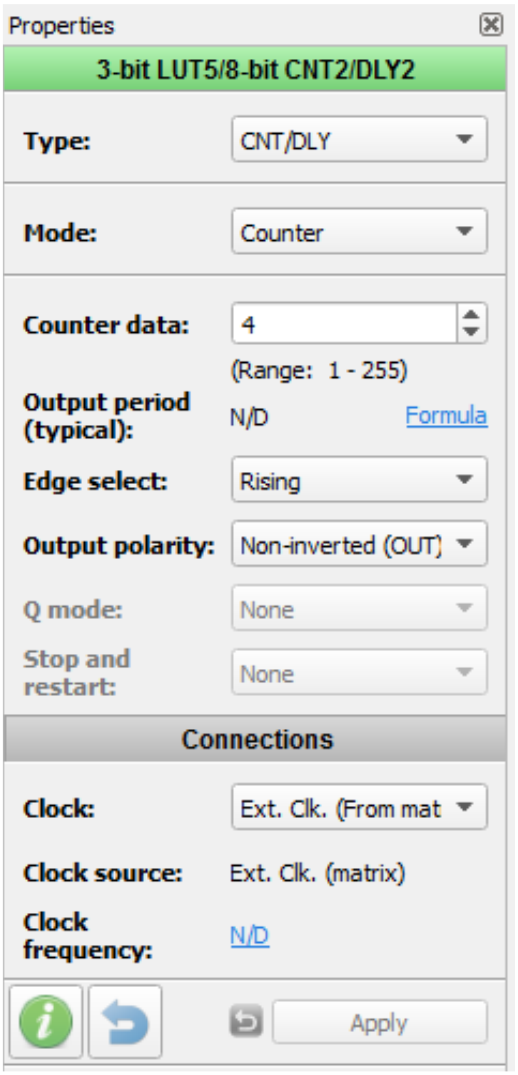


Figure 15: Counter Properties

Figure 16 shows oscillator properties.

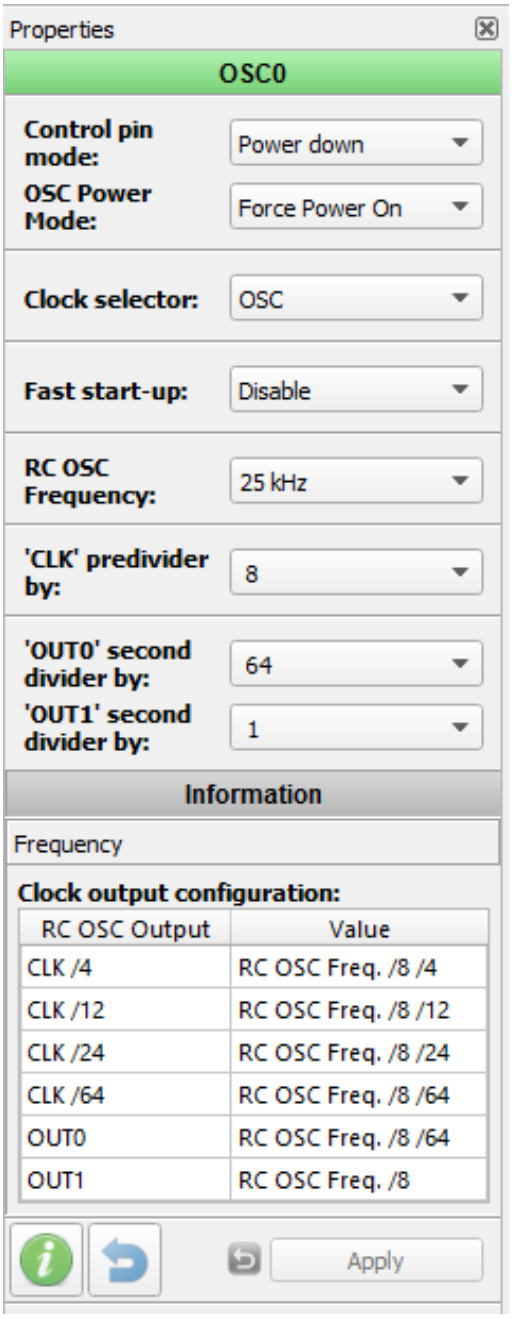


Figure 16: Oscillator Properties

The Final step is to connect each of the selected components. Use Wire tool to perform this action. To connect two pins select “Set Wire” 

and then click on the first and the second pins of the module or modules that you want to connect. The trace will be automatically routed.

Figure 17 displays ready project with configured blocks and wire connections.

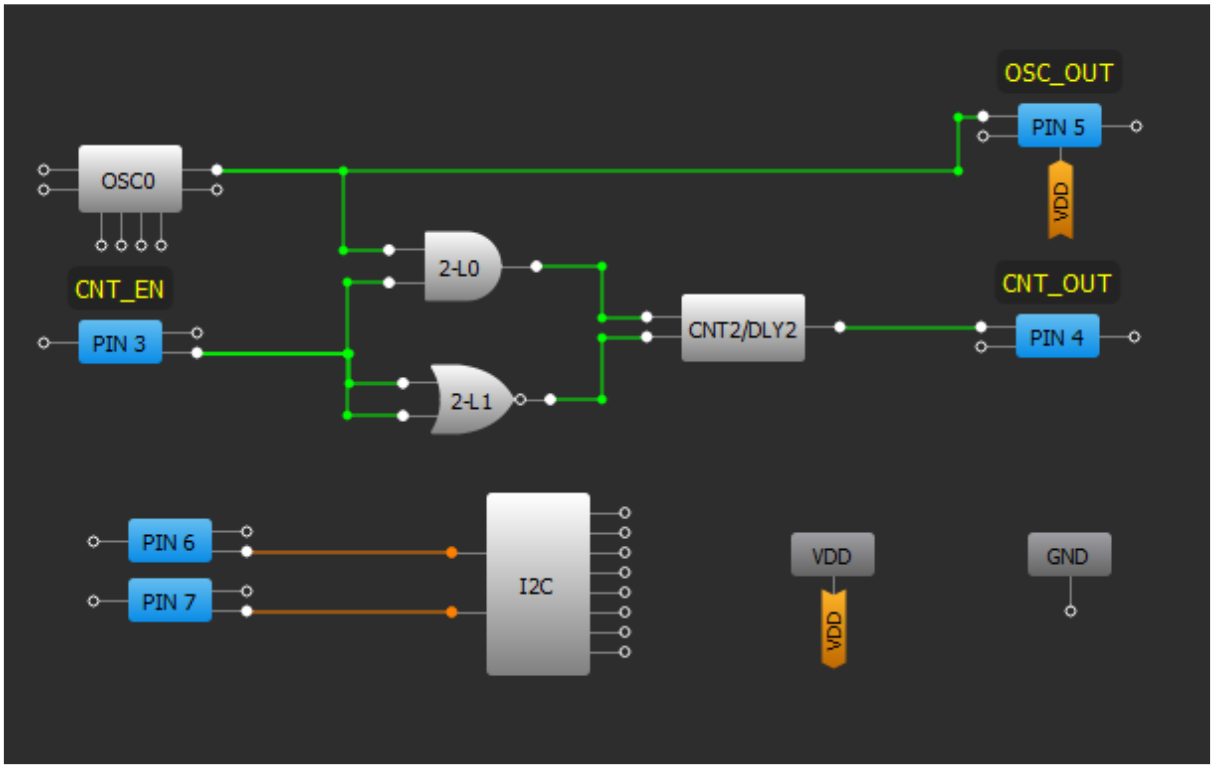


Figure 17: Ready Project in GreenPAK Designer

Use the GreenPAK DIP Development Board to test this project. Connect USB cable to GreenPAK DIP Development Board, if everything is correct, you will see two blinks of green LED, and then LED becomes red. Then press “Emulation” button. This will open emulation tool. Using it you can load code of your project to the chip.

In emulation tool from drop down menu in the right down corner select “GreenPAK DIP Development Board”, see Figure 18.

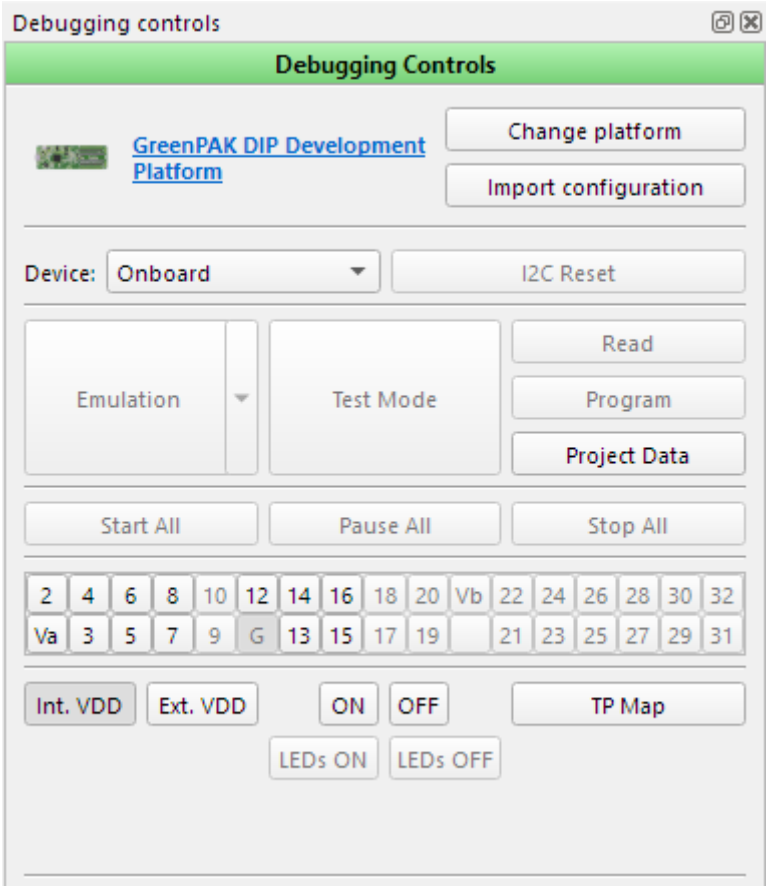


Figure 18: GreenPAK Designer, Emulation Tool

To test this project, we will use the following tools:

- Signal generator. Signal generator is applied to V_{DD} pin to power GreenPAK chip;
- Button is a software simulation of the real button. It switches PIN between V_{DD} and GND signal levels.

The Signal generator is presented as power source for the GreenPAK chip (at V_{DD} pin). By default, it's configured to output source constant 3.3 V. To see signal generators settings click on the “Edit” button near the V_{DD} pin, see Figure 19.

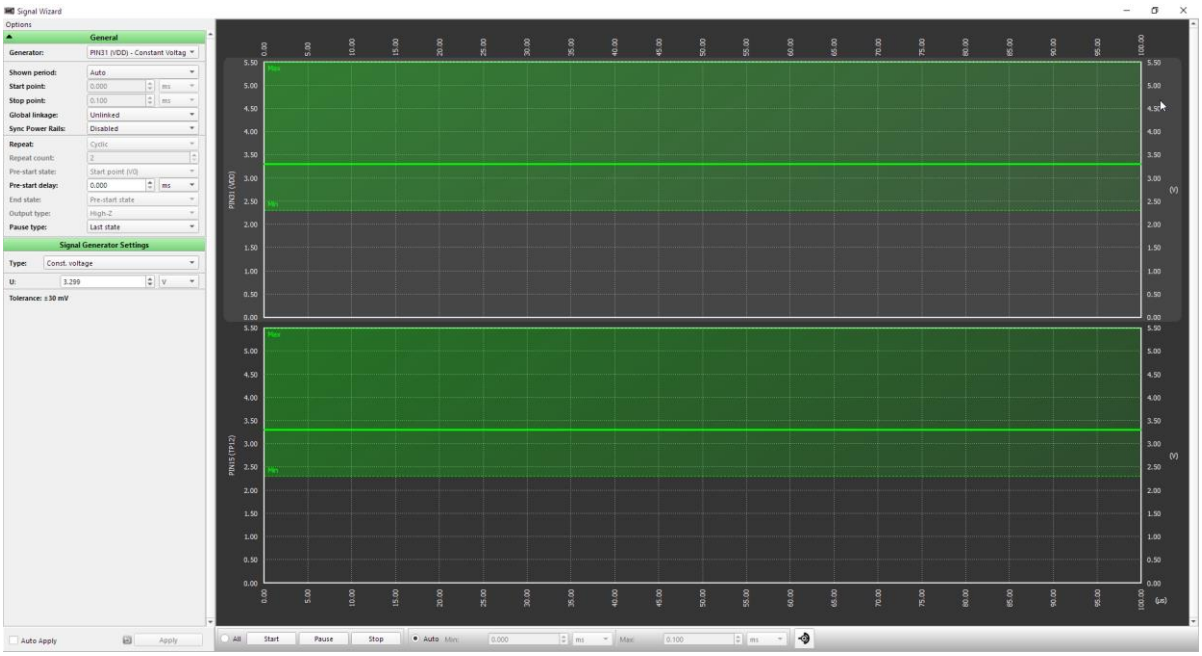


Figure 19: Generator Settings Window

It is necessary to connect virtual button to the PIN3. To do so click on “Button” item in TP3 context menu.

After all settings have done, click button “Emulation” from Emulation Tool window to start emulation process.

Functionality Waveform
Channel 1 (yellow/top) – Oscillator Output
Channel 2 (light blue/2nd line) – Button, 1 - enable Counter; 0 - disable Counter
Channel 3 (magenta/3rd line) – Counter output

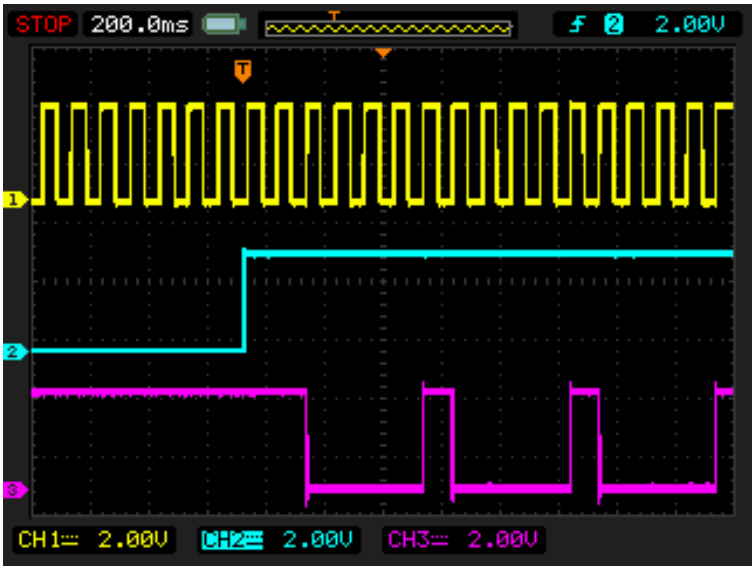


Figure 20: Waveform, Triggered on Button Pressed

Channel 1 (yellow/top) – Oscillator Output
Channel 2 (light blue/2nd line) – Button, 1 - enable Counter; 0 - disable Counter
Channel 3 (magenta/3rd line) – Counter output

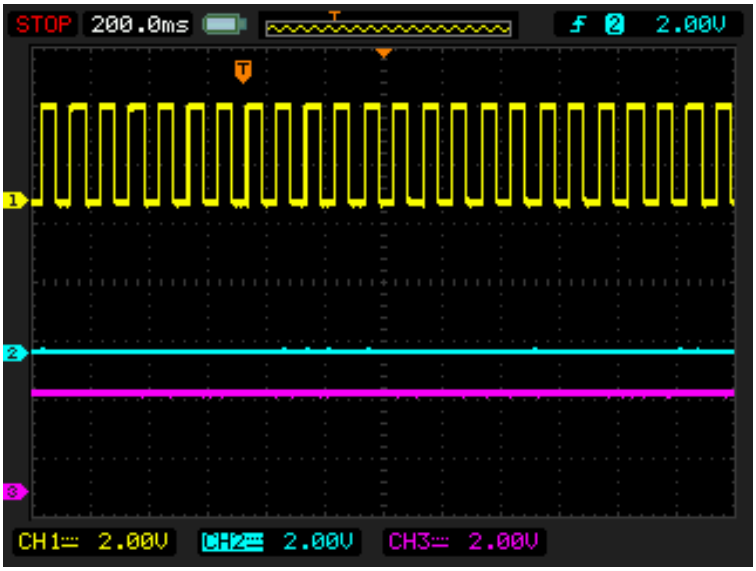


Figure 21: Waveform, no Triggered on Button Released

Channel 1 (yellow/top) – Oscillator Output
Channel 2 (light blue/2nd line) – Button, 1 - enable Counter; 0 - disable Counter
Channel 3 (magenta/3rd line) – Counter output

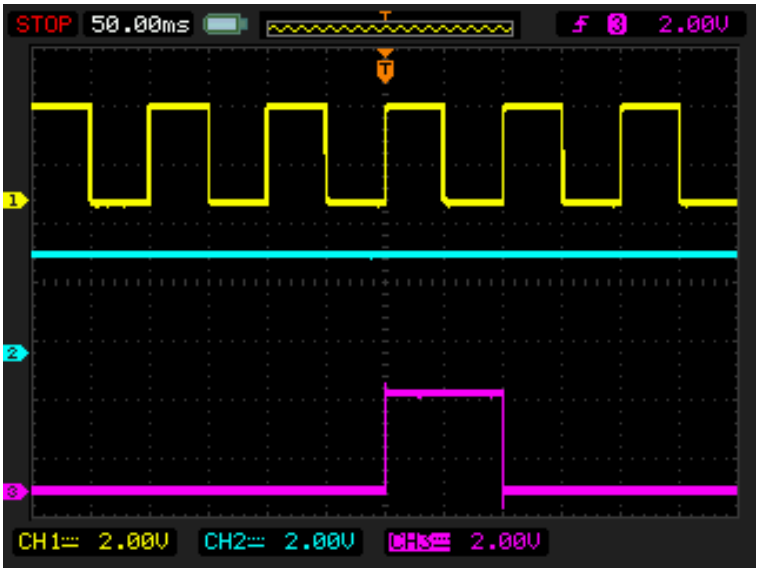


Figure 22: Waveform of the Pulse Width of the Logic Generator and Count End Signal

As it is shown in Figure 21 and Figure 22 Counter works only when the button is pressed.

6 Conclusion

This Development Platform is a truly versatile tool. It allows the designer to create a custom project within minutes.

For more information please visit our website https://www.renesas.com/.

Appendix A Electrical Specification

Mode	Parameter	Min	Typ	Max	Units
General	Test Point Capacitance	20	--	--	pF
	Input Leakage Current	--	--	1	nA
	Max Current through Protection Diode to V_{DD}	--	--	0.1	mA
Power Supply	Voltage Range	1.7	--	5.5	V
	V_{DD} Max Current	--	--	100	mA
	Voltage Output Total Error	--	--	±30	mV
Virtual Button, V_{DD}/GND, Pull-Up/Down Driver	Output Level High	--	V_{DD}	--	--
	Output Level Low	--	GND	--	--
	Strong Drive (V_{DD}/GND) Resistance	--	100	--	Ω
	Pull-Up/Down Resistance	3.5	5.6	8.5	kΩ
Expansion Connector Switch	Max Voltage	--	--	5.5	V
	Continuous Current through Any Terminal	--	--	±400	mA
	Switch On-Resistance	--	1.2	--	Ω
	External V_{DD} Switch On-Resistance	--	1.2	--	Ω
	On Leakage Current	-1	--	1	uA
	Off Leakage Current	-1	--	1	uA

Revision History

Revision	Date	Description
1.1	23-Mar-2022	Renesas rebranding
1.0	15-Sep-2021	Updated according to Dialog's Writing Guideline

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

RoHS Compliance

Renesas Electronics Corporation's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.