

## ForgeFPGA Socket Card #1

ForgeFPGA™ Socket Card #1 is a development board designed for emulation and prototyping of ForgeFPGA integrated circuits.

### Specifications

The "ForgeFPGA Socket Card #1" provides a connection between the pins of a ForgeFPGA and a Development Board. This board can be used for design prototyping with various boot modes. The Socket Card supports the PMOD standard, allowing the connection of different PMOD adapters.

### Board Contents

Includes ForgeFPGA Socket Card #1 board.

### Features

- Programming and Emulation
- Standalone Boot Option
- Onboard 4-Mbit SPI Flash
- PMOD Connectors
- Clock Generator from 2.5 kHz to 200 MHz
- Standalone Power Connectors

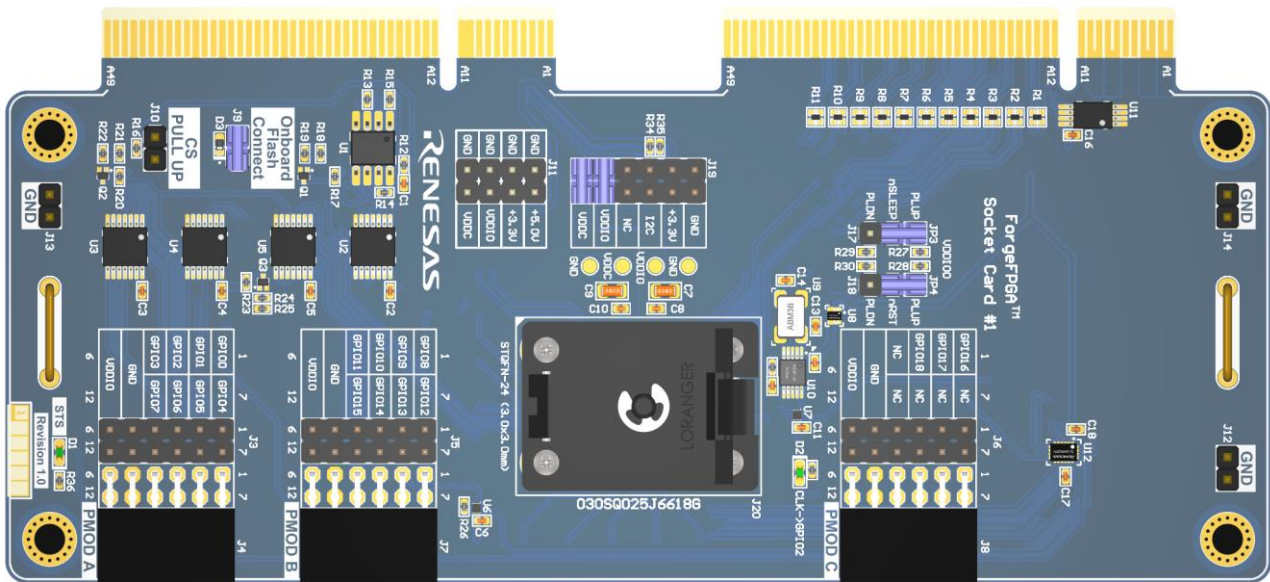


Figure 1. ForgeFPGA Socket Card #1

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# 1. Functional Description

The figure below shows the board view and identifies its main components. This board can be used in conjunction with the Go Configure Development Board via the Dual Interaction Connector to transmit and process signals. It can also operate as a standalone unit. The chip can be powered either by the Development Board or through the External Power connector, and signals on the GPIO are accessible through the 12-pin GPIO connectors or PMOD connectors.

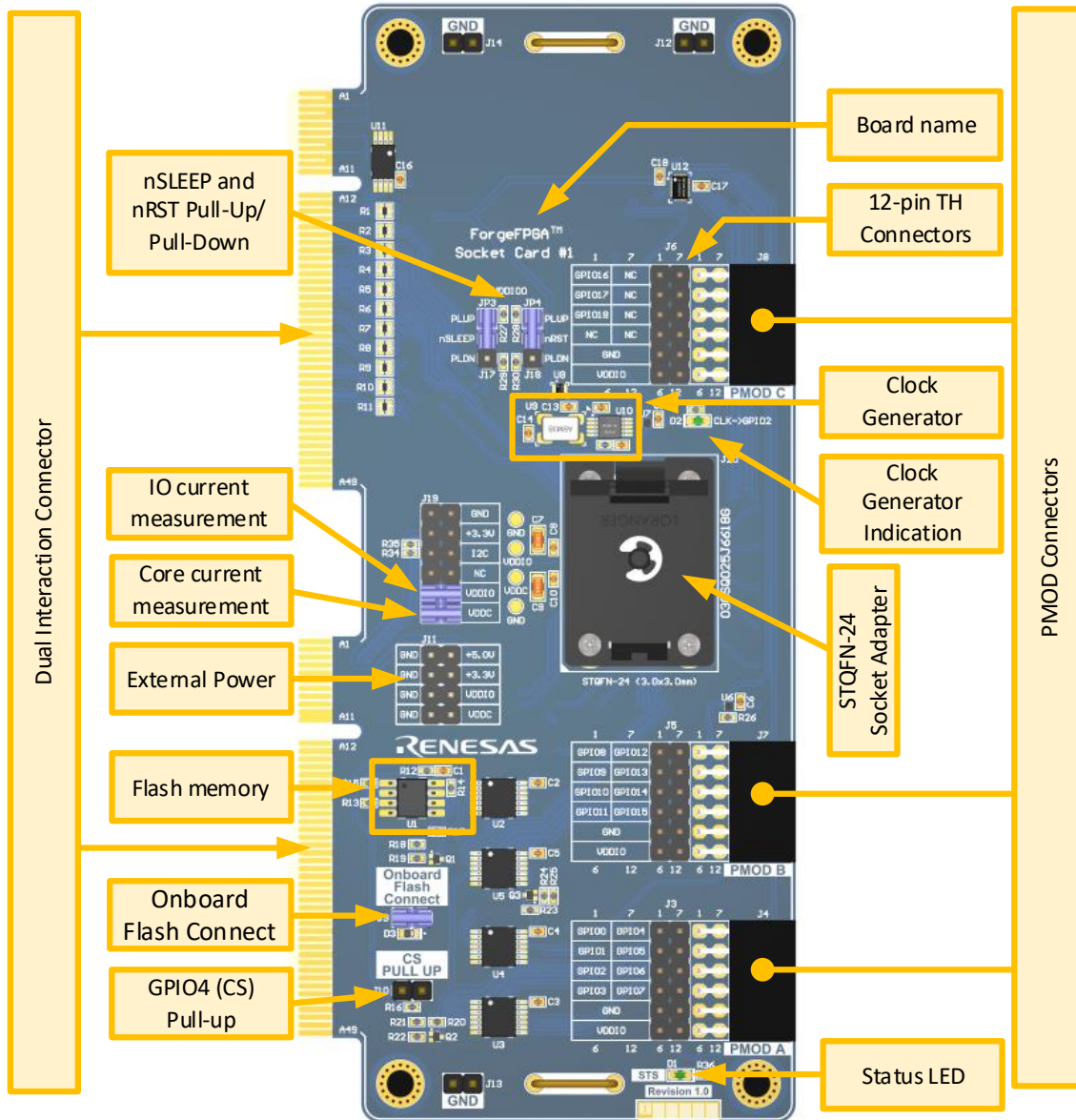
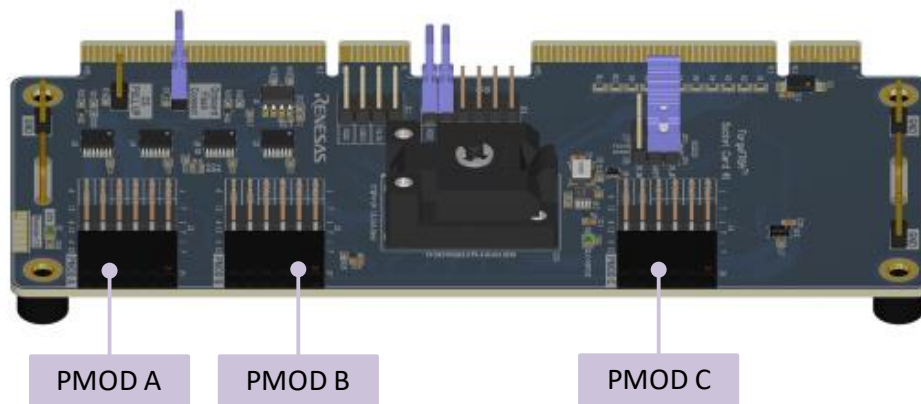


Figure 2. ForgeFPGA Socket Card #1 Components

## 1.1 PMOD and GPIO Connectors

Access to the socket pins is provided through the GPIO and PMOD connectors, both of which share the same pinout. Note that programming signals from the Interaction Connector to the GPIO/PMOD are gated during programming and emulation entry sequences.



6	5	4	3	2	1
12	11	10	9	8	7

Figure 3. PMOD and GPIO Connector

Table 1. PMOD A-C and External Connectors Pinout

GPIO/PMOD A		GPIO/PMOD B		GPIO/PMOD C	
PMOD PIN #	GPIO #	PMOD PIN #	GPIO #	PMOD PIN #	GPIO #
1	GPIO0	1	GPIO8	1	GPIO16
2	GPIO1	2	GPIO9	2	GPIO17
3	GPIO2	3	GPIO10	3	GPIO18
4	GPIO3	4	GPIO11	4	-
5	GND	5	GND	5	GND
6	VDDIO0	6	VDDIO0	6	VDDIO0
7	GPIO4	7	GPIO12	7	-
8	GPIO5	8	GPIO13	8	-
9	GPIO6	9	GPIO14	9	-
10	GPIO7	10	GPIO15	10	-
11	GND	11	GND	11	GND
12	VDDIO0	12	VDDIO0	12	VDDIO0

Table 2. GPIO and PMOD Connector Characteristics

Parameter	Description	Min	Typ	Max	Unit
I <sub>L</sub>	Input leakage current	-	2	-	μA
C <sub>IO</sub>	Input-Output Pin Capacitance	-	7	-	pF
R <sub>ON</sub>	Series Resistance	-	25	52	Ω
V <sub>IN</sub>	Input Voltage	-0.5	-	VDDIO	V

## 1.2 ForgeFPGA Current Measuring

ForgeFPGA Socket Card #1 also includes an option for measuring IC power consumption. To perform this measurement, remove the jumpers (as shown on **Figure 4**) and connect a current meter in their place. The typical load should not exceed 200 mA. Under normal operation, when current measurement is not required, the jumpers should remain installed on the board.

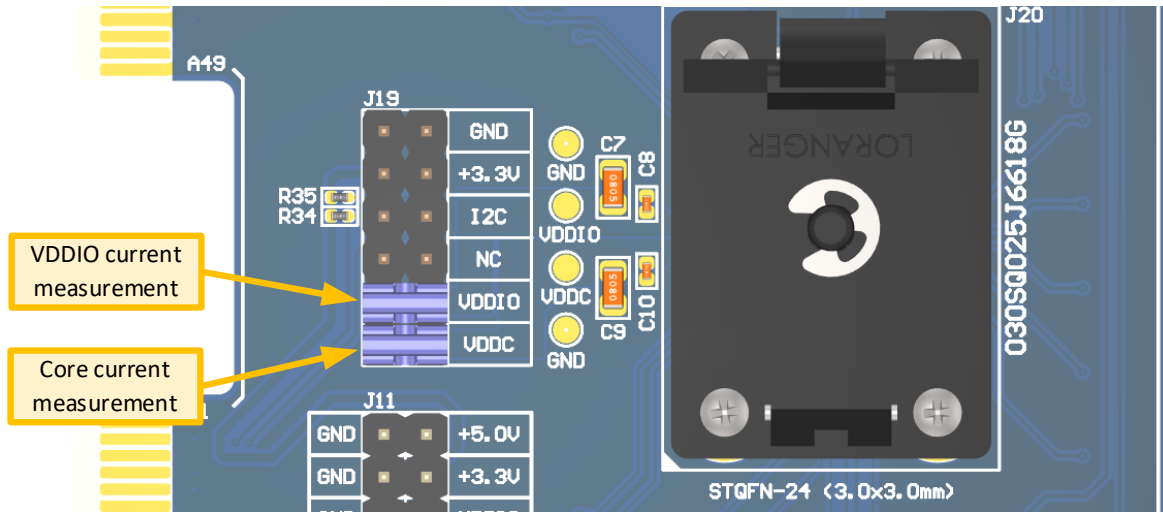


Figure 4. ForgeFPGA Current Measurement Setup

## 1.3 SPI Interface between ForgeFPGA and Flash Memory

Figure 5 shows the SPI flash interface connection between ForgeFPGA IC and Flash Memory.

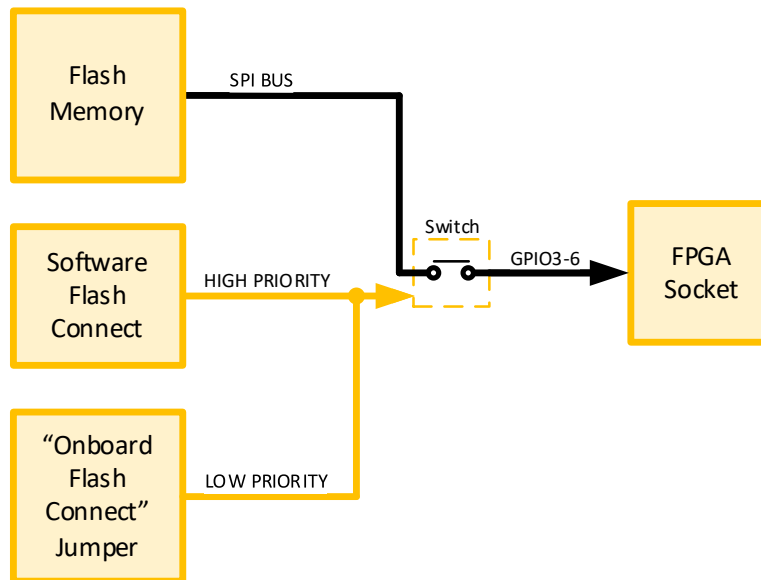
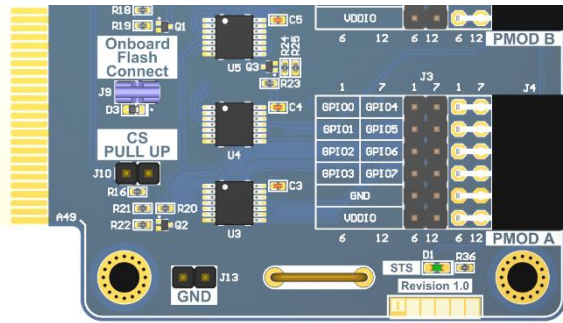


Figure 5. SPI interface Connection

The “Onboard Flash Connect” and “CS PULL UP” jumpers should be installed when using the board with the Development Board. Note that jumper removal or configuration changes are overridden and controlled by the Development Board. The table in **Figure 6** shows the correct jumper setup for standalone operation.



Mode	Onboard Flash Connect	CS PULL UP
Internal OTP Memory	0	0
SPI FLASH Memory	1	X
EXT Flash Memory	0	1

Figure 6. Memory Selection Table for Boot Configuration

External Flash Memory can be connected to Socket Card by using PMOD A.

Figure 7 shows how to connect External Flash Memory to PMOD A.

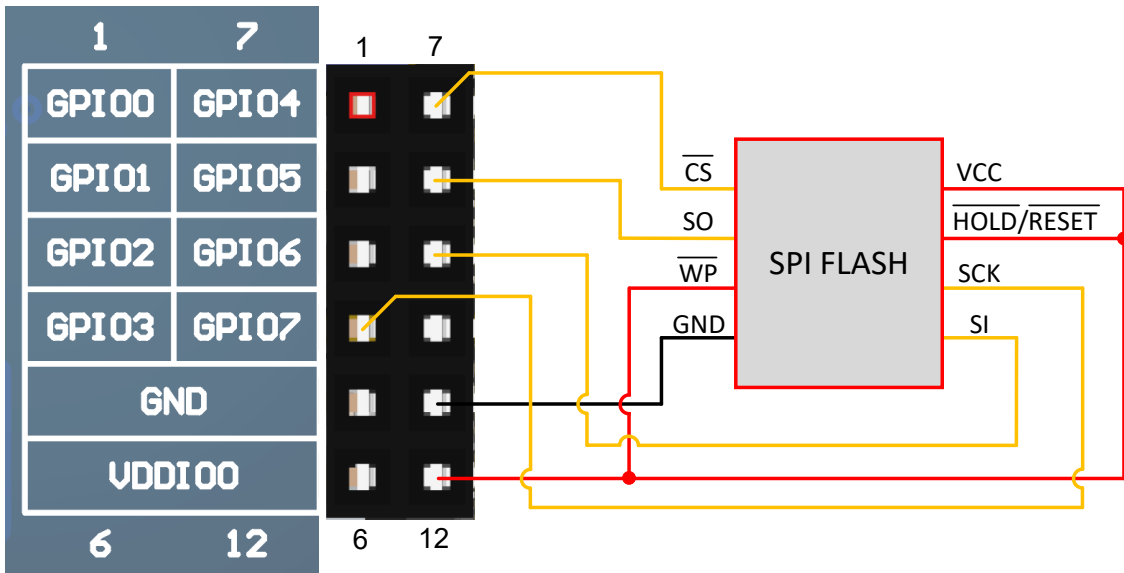


Figure 7. Connection of External Flash Memory to PMOD A

## 1.4 “External Power” Connector

ForgeFPGA Socket Card #1 can also operate with an external power supply. In this case, four separate power supply channels must be connected to the “External Power” (J11) connector (shown in **Figure 8**). The voltage and current levels for VDDIO0, VDDIO1, and VDDC must comply with the ForgeFPGA IC specifications. The “5.0V” terminal should be supplied with 5.0 V to power the commutation switches. The external power supply option can only be used when the Socket Card is not connected to the Go Configure Development Board.

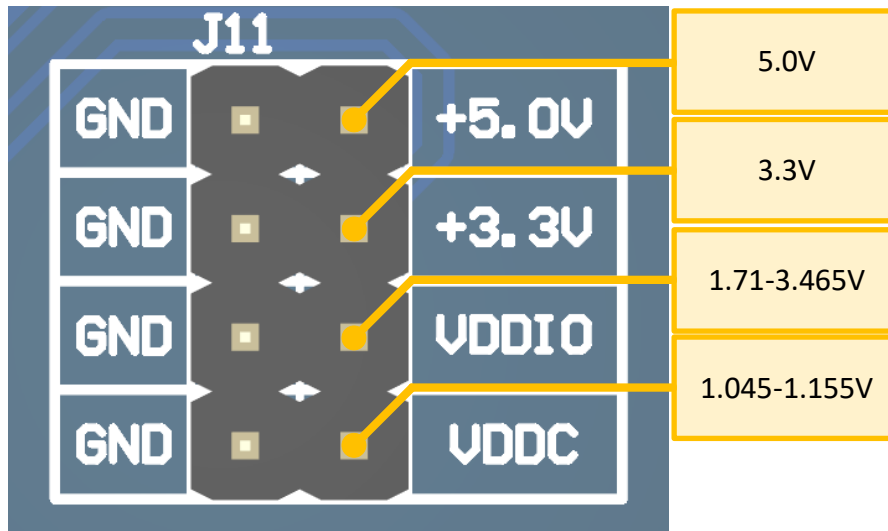


Figure 8. External Power Connector Pinout

## 1.5 Clock Generator

ForgeFPGA Socket Card #1 has I<sup>2</sup>C Programmable CMOS Clock Generator – Si5351A-B-GTR.

It used for drive PLL input of ForgeFPGA – GPIO2.

**Table 3** shows main characteristics of Clock Generator.

**Table 3. Main Characteristics of Clock Generator**

Parameter	Description	Min	Typ	Max	Unit
$F_{CLK}$	Frequency Range	0.0025	-	200	MHz
$J_{PER}$	Period Jitter	-	70	155	ps, pk-pk
$V_{DDOx}$	Output Buffer Voltage	-	VDDIO	-	V
$I_{DDOx}$	Output Buffer Supply Current (Per Output)	-	2.2	5.6	mA

## 1.6 Status LED

The status LED indicates the current operation being performed on the chip:

**Chip Standard operations:**

- Read

**Flash operations:**

- Read

- Program
  - Emulation
  - Test Mode
- Program
  - Erase
  - Test Mode

The position of the Status LED (D1) is shown on **Figure 9**.



**Figure 9. Status LED**

## 2. Working with ForgeFPGA Products

To start working with ForgeFPGA products using the Socket Card, two methodologies are available:

- Using the Go Configure Development Board.
- In standalone mode, where the ForgeFPGA configuration is downloaded from the onboard SPI flash.

### 2.1 Standalone Working Mode

As previously described, ForgeFPGA can boot from onboard flash as an SPI host. There are two ways of programming onboard flash: program with the Development Board or program the flash IC manually. The programming pins for the flash chip are accessible through the PMOD A connector. To program manually, the Socket Card must be powered via the “EXT Power” connector. If the VDDIO voltage is equal to or greater than 3.0 V, the “5V” and “VDDIO” pins can be powered from the same source.

For these operations, the ForgeFPGA must be disabled by applying logic LOW (0) to the “PWR” pins. Additionally, the “Onboard Flash Connect” and “CS PULL UP” jumpers must be installed. If the SPI flash is programmed correctly, setting logic HIGH (1) to both the PWR and EN pins will allow the ForgeFPGA to boot from the SPI flash.

### 2.2 Configuration with Go Configure Development Board

To begin working with ForgeFPGA products, connect the platform to a PC using a USB Type-C cable and apply power.

**Important:** The USB cable should be connected directly to the PC. Avoid using USB hubs or docking stations. Ensure the Socket Card is properly connected to the Go Configure Development Board as shown on **Figure 10**.

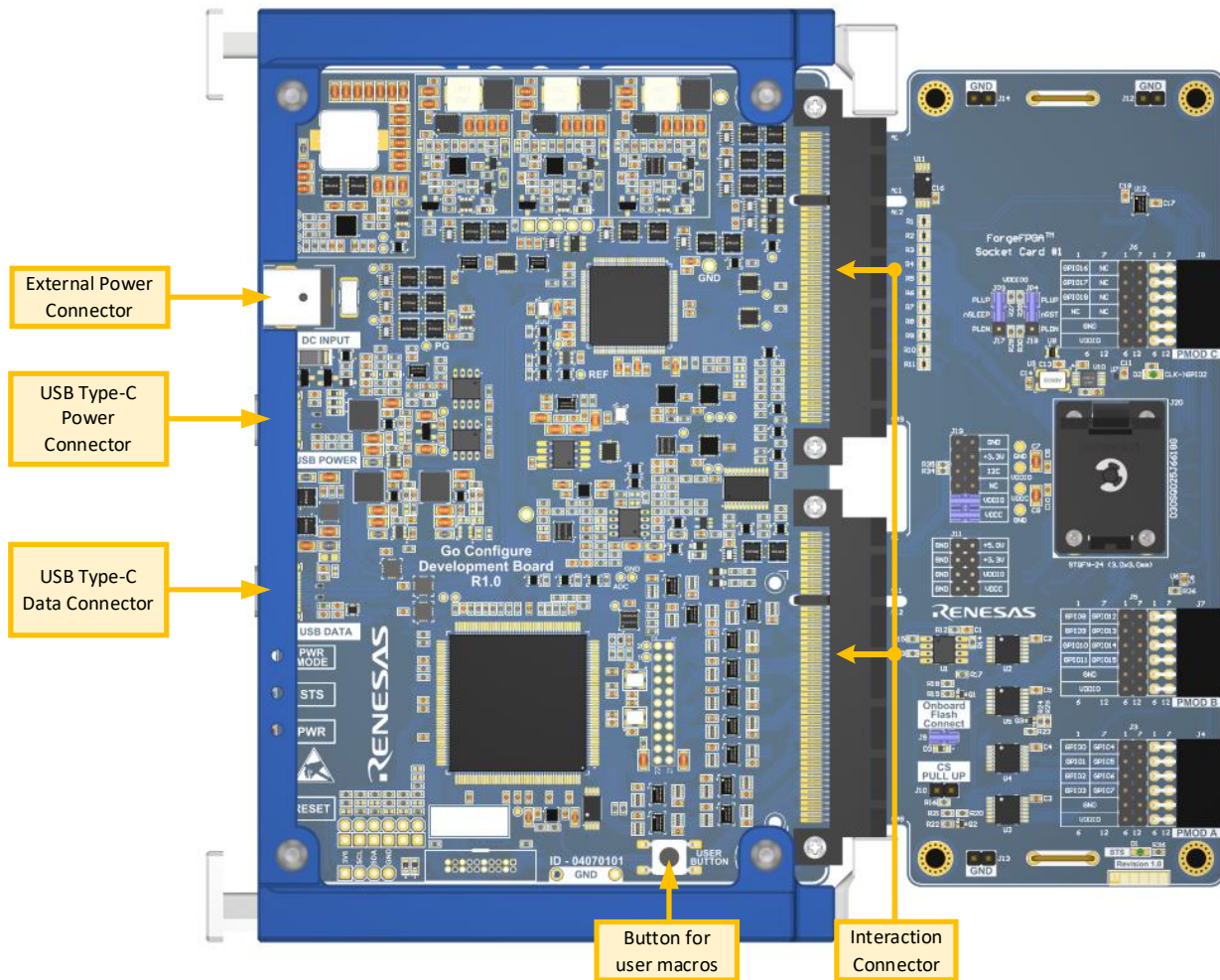


Figure 10. Development Kit

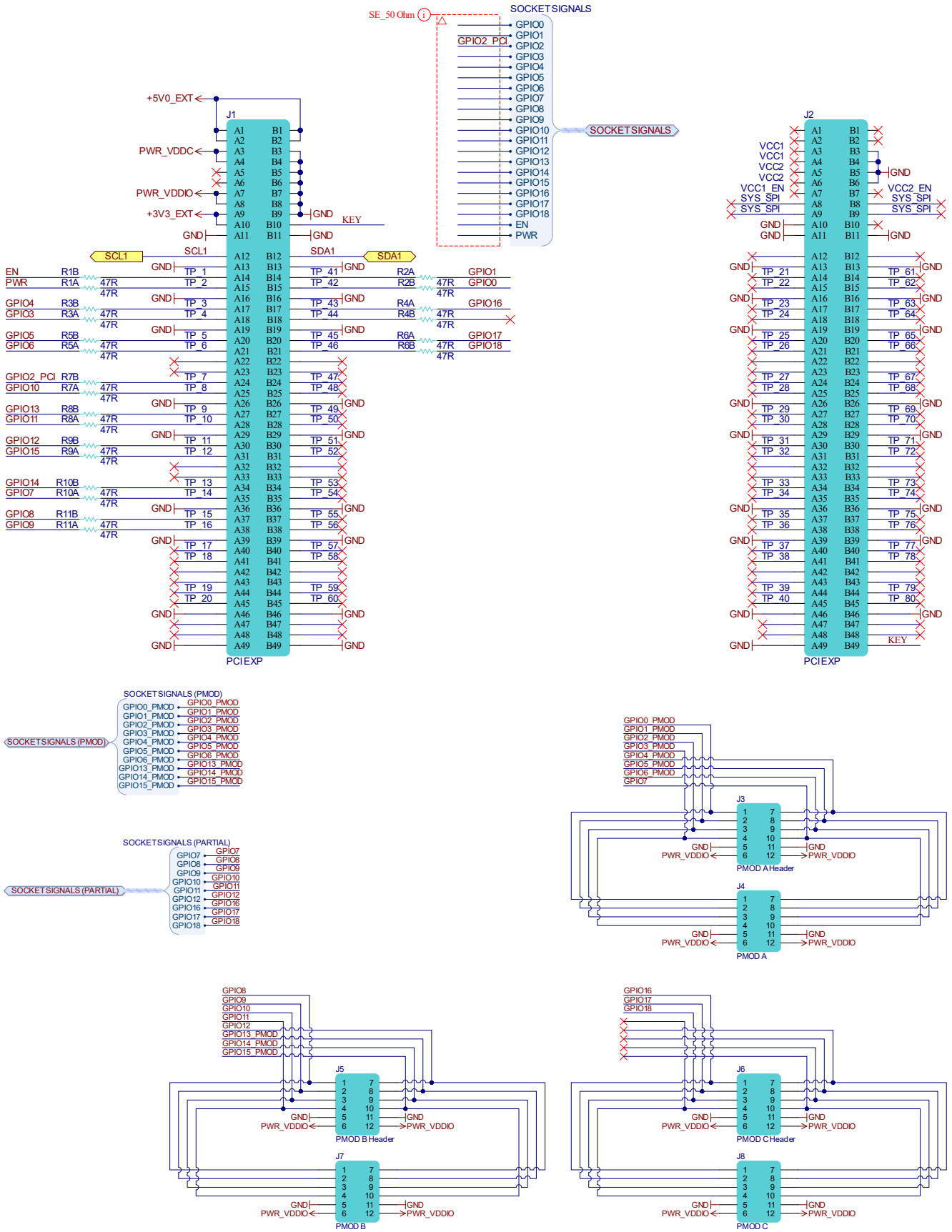
If all the connections are correct, then the red LED (PWR) will automatically turn on. After selecting “Go Configure Development Board” in Go Configure “Debug” tab, the blue LED will blink several times, and the “HW-FW” version will appear in the bottom-left corner of the debugging control window.

The following debug options are available:

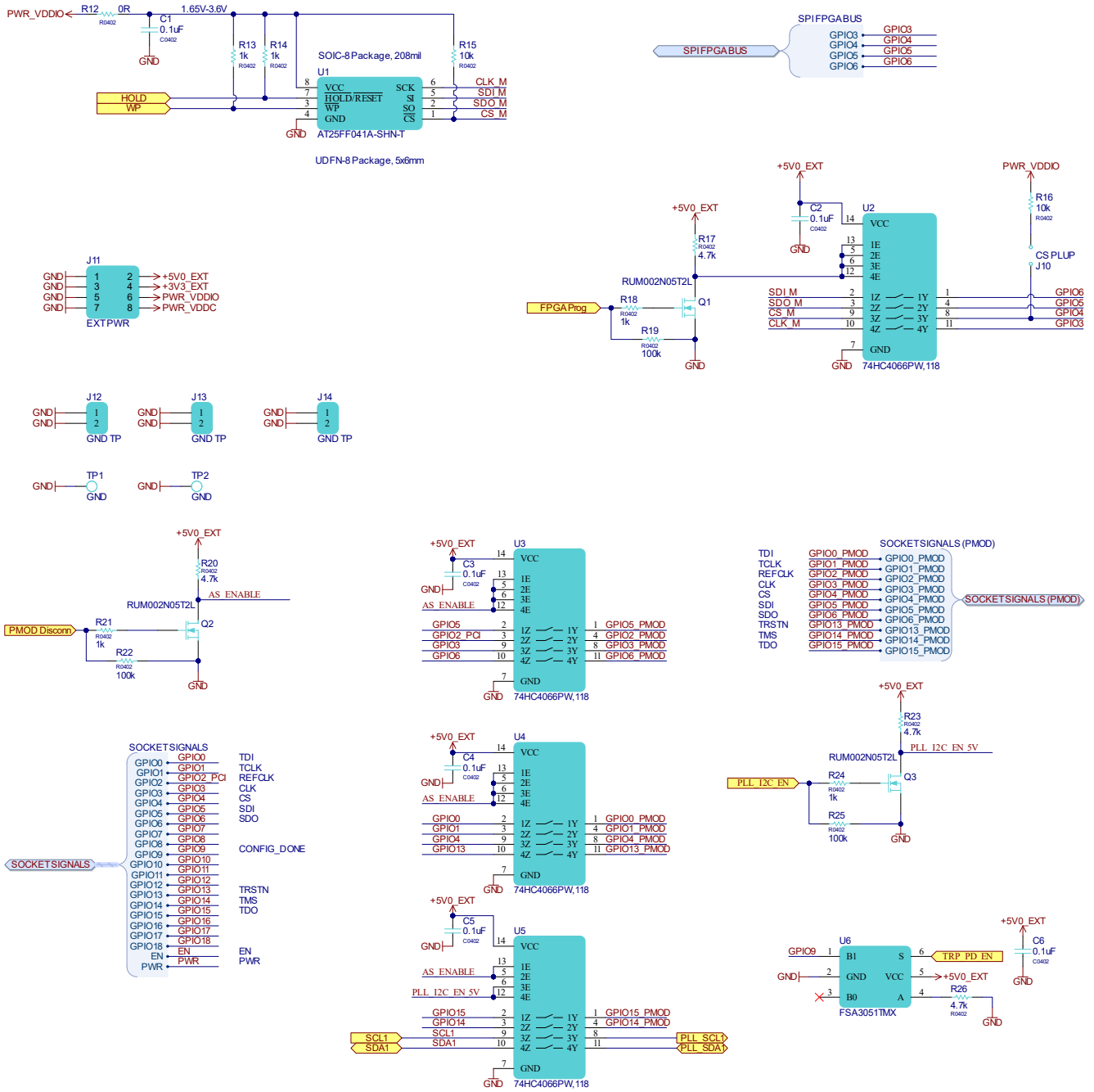
- Emulation – allows debugging of the current project. This mode is available only after synthesis and bitstream generation in the FPGA Editor.
- Test Mode – enables debugging of a programmed project.
- Test Mode\* – used to debug a project loaded from SPI Flash.
- Read – reads the configuration from the programmed chip and opens the project in a new software instance or in the “Project Data” window of the current instance.
- Program – programs the chip with the current project.
- TP Map – displays the test point map in the workspace, reflecting the physical test points on the development platform.

The more detailed information about Go Configure software can be found in [“Go Configure™ Software Hub User Guide”](#)

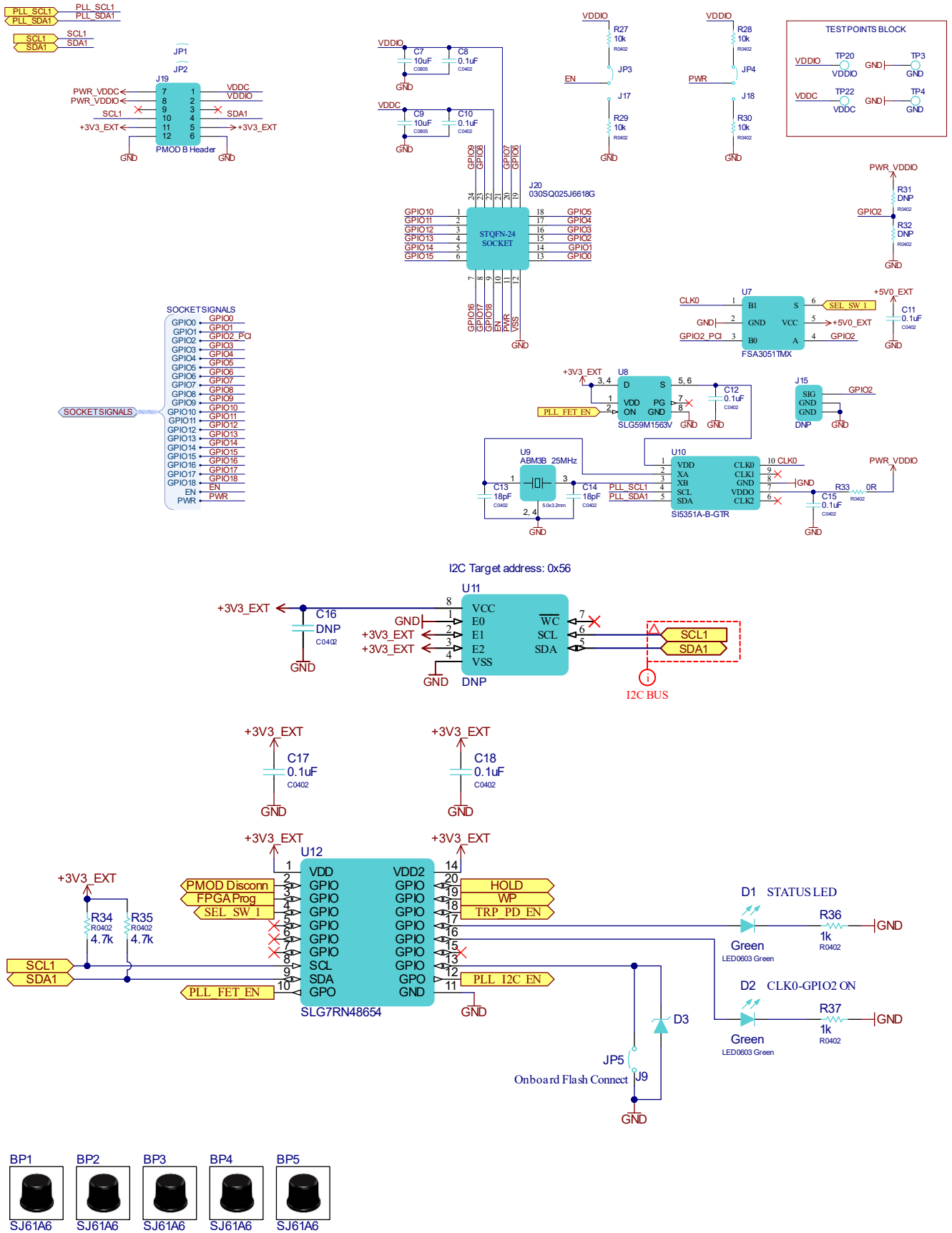
### 3. Schematic Diagram



# ForgeFPGA Socket Card #1 User Manual



# ForgeFPGA Socket Card #1 User Manual



## 4. Bill Of Materials

#	Designator	Manufacturer Part Number	Manufacturer	Quantity
1	BP1, BP2, BP3, BP4, BP5	SJ61A6	3M	5
2	C1-C6, C8, C10-C12, C15, C17, C18	GCM155R71C104KA55D	Murata	13
3	C7, C9	GRM21BR61C106KE15L	Murata	2
4	C13, C14	CL05C180JB5NNNC	Samsung	2
5	C16	DNP	DNP	1
6	D1, D2	150060GS75000	Würth Electronics	2
7	D3	DESD5V0U1BB-7	Diodes	1
8	J3, J5, J6, J19	67996-212HLF	Amphenol ICC / FCI	4
9	J4, J7, J8	PPPC062LJBN-RC	Sullins	3
10	J9, J10	68000102HLF	Amphenol ICC / FCI	2
11	J11	10129381-908001BLF	Amphenol ICC / FCI	1
12	J12, J13, J14	68000102HLF	Amphenol ICC / FCI	3
13	J15	DNP	DNP	1
14	J17, J18	68000103HLF	Amphenol ICC / FCI	2
15	J20	030SQ025J6618G	Renesas Electronics America Inc	1
16	JP1, JP2, JP3, JP4, JP5	NPC02SXON-RC	Sullins	5
17	Q1, Q2, Q3	RUM002N05T2L	Rohm	3
18	R1-R11	S41X043470JP	CTS	11
19	R12, R33	RC0402JR-070RL	Yageo	2
20	R13, R14, R18, R21, R24, R36, R37	RC0402JR-071KL	Yageo	7
21	R15, R16, R27, R28, R29, R30	RC0402JR-0710KL	Yageo	6
22	R17, R20, R23, R26, R34, R35	RC0402JR-074K7L	Yageo	6
23	R19, R22, R25	RC0402JR-07100KL	Yageo	3
24	R31, R32	DNP	DNP	2
25	U1	AT25FF041A-SHN-T	Renesas	1
26	U2, U3, U4, U5	74HC4066PW,118	Nexperia	4
27	U6, U7	FSA3051TMX	ON Semiconductor / Fairchild	2
28	U8	SLG59M1563V	Renesas Electronics America Inc	1
29	U9	ABM3B-25.000MHZ-D2Y-T	Abracon	1
30	U10	SI5351A-B-GTR	Skyworks Solutions	1
31	U11	DNP	DNP	1
32	U12	SLG7RN48654	Renesas Electronics America Inc	1

## 5. Ordering Information

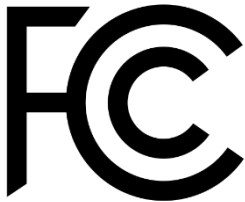
Part Number	Description
SLG7SC1	ForgeFPGA Socket Card #1 (ID-06030202)
SLG47910V-SKT	ForgeFPGA Socket Card #1, 20 Samples of SLG47910V and SLG479PMODLED Adapter

## 6. Certifications

The ForgeFPGA Socket Card #1 complies with the following certifications/standards.

### 6.1 EMC/EMI Standards

- FCC Notice (Class A)



This device complies with FCC 47 CFR part 15, subpart B. Operation is subject to the following two conditions:

(1) The equipment should be handled using standard CMOS device precautions. The user must take all precautions to avoid the build-up of static electricity while working with this equipment. All test and measurement tools, including the workbench, must be grounded. The user/operator must be grounded using the wrist strap. The connectors and/or device pins should not be touched with bare fingers.

(2) This Class A digital device complies with the FCC rules outlined in 47 CFR Part 15. This equipment may cause radio frequency noise when used in a residential area. In such cases, the user/operator of the equipment may be required to take appropriate countermeasures at their own responsibility.

- CE Class B (EMC)



This product is in conformity with the following Directive(s) of the European Parliament and of the Council on the harmonisation of the laws of the Member States relating to Electromagnetic Compatibility 2014/30/EU (EMC Directive). The equipment can be operated under the following conditions:

(1) The equipment should be handled using standard CMOS device precautions. The user must take all precautions to avoid the build-up of static electricity while working with this equipment. All test and measurement tools, including the workbench, must be grounded. The user/operator must be grounded using the wrist strap. The connectors and/or device pins should not be touched with bare fingers.

(2) This is a 'Class B' (EN 55032:2015) device. This equipment may cause radio frequency noise when used in a residential area. In such cases, the user/operator of the equipment may be required to take appropriate countermeasures at their own responsibility.

- UKCA Class B (EMC)



This product conforms to the following relevant UK Statutory Instrument(s) (and their amendments): 2016 No. 1091 Electromagnetic Compatibility Regulations 2016. The equipment can be operated under the following conditions:

(1) The equipment should be handled using standard CMOS device precautions. The user must take all precautions to avoid the build-up of static electricity while working with this equipment. All test and measurement tools, including the workbench, must be grounded. The user/operator must be grounded using the wrist strap. The connectors and/or device pins should not be touched with bare fingers.

(2) This is a 'Class B' (BS EN 55032:2015) equipment. This equipment may cause radio frequency noise when used in a residential area. In such cases, the user/operator of the equipment may be required to take appropriate countermeasures at their own responsibility.

### 6.2 Material Selection, Waste, Recycling, and Disposal Standards

- 2011/65/EU Restriction of Hazardous Substances (RoHS Directive) + amendment (EU) 2015/863 (RoHS3)
- 2012/19/EU Waste Electrical and Electronic Equipment (WEEE Directive)
- 2012 No. 3032 The Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment Regulations
- 2013 No. 3113 Waste Electrical and Electronic Equipment Regulations

## 7. Revision History

Revision	Date	Description
1.02	Mar 18, 2026	Fixed typos
1.01	Mar 05, 2026	Added Certifications section
1.00	Nov 10, 2025	Initial release.