

RZ/A3M Group

Evaluation Kit for RZ/A3M Microprocessor Group EK-RZ/A3M v1 User's Manual

Renesas RZ Family RZ/A Series

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1. Precaution against Electrostatic Discharge (ESD)

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2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power is supplied until the power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

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8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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This Evaluation Kit is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area, or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

• Ensure attached cables do not lie across the equipment.

- · Reorient the receiving antenna.
- Increase the distance between the equipment and the receiver.
- · Connect the equipment into an outlet on a circuit different from that which the receiver is connected.
- · Power down the equipment when not in use.
- Consult the dealer or an experienced radio/TV technician for help.
- Note: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken:

- The user is advised that mobile phones should not be used within 10 m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Evaluation Kit does not represent an ideal reference design for an end product and does not fulfill the regulatory standards for an end product.



Renesas RZ Family

EK-RZ/A3M v1

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1. Kit Overview

The EK-RZ/A3M, an Evaluation Kit for RZ/A3M MPU Group, enables users to seamlessly evaluate the features of the RZ/A3M MPU group and develop embedded systems applications using Flexible Software Package (FSP) and e² studio IDE. The users can utilize rich on-board features along with their choice of popular ecosystems add-ons to bring their big ideas to life.

The EK-RZ/A3M kit consists of two boards: the EK-RZ/A3M board featuring the RZ/A3M MPU, and the MIPI Graphics Expansion Board 2.

The key features of the EK-RZ/A3M board are categorized in three groups (consistent with the architecture of the kit, with a few exceptions) as follows:

MPU Native Pin Access

- R9A07G066M04GBG MPU (referred to as RZ MPU)
- 1 GHz, Arm[®] Cortex[®]-A55 Single MPCore core
- 128 KB SRAM
- Built-in DDR3L-SDRAM (128 MB)
- 244 pins, BGA package
- Native pin access through 1 x 14-pin, and 1 x 40-pin header (not populated)
- Parallel graphics display interface connector (not populated)
- 4-Lane MIPI Display connector (present at the underside of the EK-RZ/A3M board)
- MPU current measurement points for precision current consumption measurement
- Multiple clock sources RZ MPU crystal oscillator providing a precision 24.000 MHz reference clock. Additional low-precision clocks are available internal to the RZ MPU

System Control and Ecosystem Access

- Four 5 V input sources
 - USB (Debug, High Speed, Power Only)
 - External power supply (using surface mount clamp test points and power input vias)
- Two Debug modes
 - Debug on-board (SWD and JTAG)
 - Debug in (SWD and JTAG)
- User LEDs and buttons
 - Three User LEDs (red, blue, green)
 - Power LED (white) indicating availability of regulated power
 - Debug LED (yellow) indicating the debug connection
 - Two User buttons
 - One Reset button
- Five most popular ecosystems expansions
 - Two Seeed Grove[®] system (I²C/Analog) connectors (not populated)
 - SparkFun[®] Qwiic[®] connector (not populated)
 - Two Digilent Pmod[™] (SPI, UART and I²C) connectors
 - Arduino[™] (Uno R3) connector
 - MikroElektronika[™] mikroBUS connector (not populated)

Special Feature Access

- USB High Speed Host and Device (USB-C connector)
- 32 MB (256 Mb) External Quad-SPI NOR Flash
- 128 MB (1024 Mb) External Quad-SPI NAND Flash
- Audio CODEC with speaker out and combined headphone / microphone connectors
- Real Time Clock
- Micro SD card socket
- Configuration switches
- MPU boot configuration switches





Figure 1. EK-RZ/A3M Board Top Side





Figure 2. EK-RZ/A3M Board Bottom Side



1.1 Assumptions and Advisory Notes

- 1. It is assumed that the user has a basic understanding of microprocessors and embedded systems hardware.
- 2. It is recommended that the user refers to the *EK-RZ/A3M Quick Start Guide* to get acquainted with the kit and the Quick Start example project that EK-RZ/A3M board comes pre-programmed with.
- 3. Flexible Software Package (FSP) and Integrated Development Environment (IDE) such as e² studio are required to develop embedded applications on EK-RZ/A3M kit.
- 4. Instructions to download and install software, import example projects, build them and program the EK-RZ/A3M board are provided in the quick start guide.
- 5. The MPU fitted to the EK board may not contain the latest version of the on-chip boot firmware.



2. Kit Contents

The following components are included in the kit:

- 1. EK-RZ/A3M v1 board
- 2. USB-C to USB-C cable
- 3. USB-C to USB-A cable
- 4. USB-C to USB-A female host cable
- 5. MIPI Graphics Expansion Board 2
- 6. Display mounting hardware (spacers and fixing screws)



Figure 3. EK-RZ/A3M Kit Contents



3. Ordering Information

• EK-RZ/A3M v1 kit orderable part number: RTK9EKZA3MS10001BE

Notes: 1:The underlined character in the orderable part number represents the kit version. 2:The MIPI Graphics Expansion Board 2 orderable part number: RTKAPPLCDMS02001BE

- Dimensions
 - EK-RZ/A3M board dimensions: 84 mm (width) x 180 mm (length)
 - MIPI Graphics Expansion Board 2 dimensions: 132 mm (width) x 100 mm (length)

4. Hardware Architecture and Default Configuration

4.1 Kit Architecture

The EK-RZ/A3M board is designed with three sections or areas to help shorten the learning curve of the users and maximize the design and knowledge reuse among similar kits. The contents of these three areas are conceptually standardized among similar kits.

Kit area	Area features	Area present on all similar kits	Functionality is:
MPU Native Pin Access Area	RZ MPU, breakout pin headers for all MPU I/O and power, Current Measurement, MIPI Graphics Expansion Port, Quad-SPI Flash (NOR and NAND), Parallel Graphics Display Port	Yes	MPU dependent
Special Feature Access Area	Configuration Switches, MPU boot configuration switches MPU special features: Audio CODEC, Real Time Clock, Micro SD card socket, USB Power	No	MPU dependent
System Control and Ecosystem Access Area	Power, Debug MCU, User LED and buttons, reset, ecosystem connectors and USB High Speed Host and Device	Yes	Same or similar across similar kits

Note: The Quad-SPI NAND and NOR Flash devices are among the Special Feature Access features. Normally, they would be in the Special Feature Access Area, however, to optimize the layout, routing, and performance, they are placed in the MPU Native Pin Access area. This also applies to the USB High Speed port which is among the Special Features however, has been placed in the System Control and Ecosystem Access Area.





Figure 4. EK-RZ/A3M Board Functional Area Definitions



4.2 System Block Diagram



Figure 5. EK-RZ/A3M Board Block Diagram



4.3 Jumper Configuration

Two types of jumpers are provided on the EK-RZ/A3M board.

- 1. Copper jumpers (trace-cut type and solder bridge type)
- 2. Traditional pin header jumpers

The following sections describe each type and their default configuration.

4.3.1 Copper Jumpers

Copper jumpers are of two types, designated trace-cut and solder-bridge.

A **trace-cut jumper** is provided with a narrow copper trace connecting its pads. The silk screen overlay printing around a trace-cut jumper is a solid box. To isolate the pads, cut the trace between pads adjacent to each pad, then remove the connecting copper foil either mechanically or with the assistance of heat. Once the etched copper trace is removed, the trace-cut jumper is turned into a solder-bridge jumper for any later changes.

A **solder-bridge** jumper is provided with two isolated pads that may be joined together by one of three methods:

- Solder may be applied to both pads to develop a bulge on each and the bulges joined by touching a soldering iron across the two pads.
- A small wire may be placed across the two pads and soldered in place.
- A SMT resistor, size 0805, 0603, or 0402, may be placed across the two pads and soldered in place. A zero-ohm resistor shorts the pads together.

For any copper jumper, the connection is considered **closed** if there is an electrical connection between the pads (default for trace-cut jumpers.) The connection is considered **open** if there is no electrical connection between the pads (default for the solder-bridge jumpers.)



Figure 6. Copper Jumpers

4.3.2 Traditional Pin Header Jumpers

These jumpers are traditional small pitch jumpers that require an external shunt to open/close them. The traditional pin jumpers on the EK-RZ/A3M board are 2 mm pitch headers and require compatible 2 mm shunt jumpers.

4.3.3 Default Jumper Configuration

The following table describes the default configuration for each jumper on the EK-RZ/A3M board. This includes copper jumpers (Ex designation) and traditional pin jumpers (Jx designation).

The Circuit Group for each jumper is the designation found in the board schematic (available in the Design Package). Functional details for many of the listed jumpers may be found in sections associated with each functional area of the kits.

Location	Circuit Group	Default Open/Closed	Function
E1	Pmod 2	Closed	Connects U5 pin 2 to P1_3 (CTS1)
E2	SD Card	Closed	Connects SD card I/O voltage select to P9_4
E3	Arduino	Open	Connects Arduino AREF to +3.3V
E4	Grove	Open	Connects J28 pin 2 to AN1
E5	Grove	Open	Connects J28 pin 1 to AN0
E6	Grove	Closed	Connects J28 pin 1 to SCL1
E7	Grove	Closed	Connects J28 pin 2 to SDA1

Table 2. Default Jumper Configuration



Location	Circuit Group	Default Open/Closed	Function	
E8	Debugger	Closed	Connects debugger JLOB_TRST to the RZ MPU TRST_L pin via E11	
E9	RTC	Closed	Connects Q1 pin 3 (RTC interrupt) to P10_0 (IRQ0)	
E10	Pmod 2	Closed	Connects U5 pin 14 to P1_4 (RTS1)	
E11	Debugger	Closed	Connects debugger JLOB_TRST to the RZ MPU TRST_L pin via E8	
E12	Port expander	Closed	Connects port expander U2 interrupt to P10_0	
E13	GPIO	Open	Connects P23_0 to pin header J2 pin 2	
E14	GPIO	Open	Connects P23_1 to pin header J2 pin 3	
E15	Power supply	Open	Bypasses reverse supply protection diode D3	
E16	Power supply	Open	Bypasses reverse supply protection diode D6	
E17	Power supply	Open	Bypasses reverse supply protection diode D14	
E18	Power supply	Closed	Disconnects the +3.3V supply rail from the PMIC	
E19	Power supply	Closed	Disconnects the +1.8V supply rail from the PMIC	
E20	Power supply	Closed	Disconnects the +1.35V supply rail from the PMIC	
E21	Power supply	Closed	Disconnects the +1.1V supply rail from the PMIC	
E22	Power supply	Open	Bypasses reverse supply protection diode D4	
E25	Pmod 1	Closed	Connects pins 6 and 12 of J26 to +3.3 V	
E26	User LED	Closed	Connects LED2 (green) to P20_3 (MTIOC2A)	
E27	User LED	Closed	Connects LED1 (blue) to P10_1 (MTIOC0B)	
E28	User LED	Closed	Connects LED3 (red) to P20_4 (MTIOC2B)	
E29	Debugger Power	Closed	Connects Debug MCU power to +3.3 V	
E30	Debugger	Closed	Connects the JTAG GND Detect pin 9 on J20 and J13 to GND	
E31	User switch	Closed	Connects SW1 to P10_3 (IRQ3)	
E32	User switch	Closed	Connects SW2 to P11_1 (IRQ5)	
E35	Pmod 1	Open	Connects pins 6 and 12 of J26 to +5 V	
J9	J-Link OB	Link 2-3	Configures RA4M2_RESET_L for on-board debugger mode	
J15	SD Card	Link 1-2	Connects SD Card Detect to P11_3 (allows the SD card to be used with the RGB LCD)	



4.3.4 Board Configuration Switch Settings

The EK-RZ/A3M features an I²C I/O Port Expander (PI4IOE5V6408) at U15 and has the I²C address 0x43. The port expander is connected to the configuration switches SW4.

The following table describes the function and default configuration for each switch that selects the operational peripheral pins on the EK-RZ/A3M board.

The Circuit Group for each switch is the designation found in the board schematic (available in the Design Package). Functional details for many of the listed switches may be found in sections associated with each functional area of the kit.

Table 3. Default Switch Configuration (SW4)

Switch	Switch Definition	Position (Default)	Function	Conflict
SW4-1	Pmod 1 Mode Select 1	OFF	Please see Table 18	Please see Table 18
		ON		
SW4-2	Pmod 1 Mode Select 2	OFF	-	
		ON		
SW4-3	Pmod 2 Mode Select	OFF	SPI Mode Selected	-
		ON	UART Mode Selected	-
SW4-4	USBHS Role Toggle	OFF	Toggles USBHS between Host	-
		ON	and Device mode	-
SW4-5	QSPI Flash	OFF	NOR Flash Selected	-
	wode Select	ON	NAND Flash Selected	-

Note: There are no conflicting settings for SW4.



Figure 7. Configuration Switch (SW4)



4.3.5 MPU Boot Mode Switch Settings

During the RZ MPU reset sequence, the boot mode settings on MD_BOOT0, MD_BOOT1, MD_BOOT2, MD_CLKS, MD_OSCDRV0 and MD_OSCDRV1 are sampled and applied. Once the MPU has started, these pins may be used as GPI0. Care must be taken though to ensure that these pins are not driven by external devices during start up. The pins are sampled during the rising edge of the PRST_N pin.

Five-way switch, SW5, is used to configure the MPU boot mode, along with three other settings.

Caution: Please avoid setting the MPU Boot mode to mode 6, as the QSPI does not support 1.8V.

Table 4. Default Switch Configuration (SW5)

Switch	Switch Definition	Position (Default)	Function	Conflict
SW5-1	EK-RZ/A3M Boot Mode Select 1	OFF	Please see Table 5	-
		ON		
SW5-2	EK-RZ/A3M Boot Mode Select 2	OFF		
		ON		
SW5-3	SSCG function	OFF	Enables the SSCG function of PLL3 *1	-
		ON	Disables the SSCG function of PLL3 *1	-
SW5-4	Debug mode	OFF	JTAG mode	-
		ON	SWD mode	-
SW5-5	Test reset	OFF	TRST# asserted	-
		ON	TRST# not asserted	-

^{*1} Please refer to the RZ/A3M hardware manual for further details

Note: There are no conflicting settings for SW5.

Table 5. EK-RZ/A3M Mode Switch Boot Modes

MD_BOOT2 is pulled high, so boot mode 3 is not available.

Boot mode	Description	SW5-2 (MD_BOOT1)	SW5-1 (MD_BOOT0)
Mode 4	Boot from 3.3V QSPI NOR flash	Off	Off
Mode 5	Boot from program downloaded from SCIF	Off	On
Mode 6	Boot from 1.8V QSPI NAND flash (Do not use)	On	Off
Mode 7	Boot from 3.3V QSPI NAND flash	On	On



Figure 8. Boot Mode Switch (SW5)



5. System Control and Ecosystem Access Area

The following figure shows the System Control and Ecosystem Access area on the EK-RZ/A3M board. Subsequent sections detail the features and functionality provided in the area.



Figure 9. System Control and Ecosystem Access Area



5.1 Power

The EK-RZ/A3M kit is designed for +5 V operation. An on-board Power Management IC (DA9080) is used to convert the 5 V supply to 3.3 V, 1.8 V. 1.35 V and 1.1 V supplies. These supplies are used to power the RZ MPU and other peripheral features. The PMIC also includes a 3.3 V LDO, which is used as a low-noise supply for the CODEC VDD_MIC power pin and is available on J2 for external use.

5.1.1 Power Supply Options

This section describes the different ways in which EK-RZ/A3M kit can be powered.



Figure 10. Power Supply Options

5.1.1.1 Option 1: Debug USB

5 V may be supplied from an external USB host to the USB Debug connector (J10) labelled DEBUG1 on the board. Power from this source is connected to the Main System 5 V Power. Reverse current protection is provided between this connector and the Main System 5 V Power. Under rare circumstances, the voltage-drop across this diode can prevent the on-board USB from functioning correctly. This problem can be resolved by shorting E15 to bypass the diode.

5.1.1.2 Option 2: USB High Speed

5 V may be supplied from an external USB host to the USB High Speed connector (J7) labelled USB HIGH SPEED on the board. Power from this source is connected to the Main System 5 V Power. Reverse current protection is provided between this connector and the Main System 5 V Power. Under rare circumstances, the voltage-drop across this diode can prevent the on-board USB from functioning correctly. This problem can be resolved by shorting E16 to bypass the diode.

5.1.1.3 Option 3: USB-C Power Only Connector

5 V may be supplied to the board via the power-only USB connector (J6). Reverse current protection is provided between this connector and the Main System 5 V Power. Under rare circumstances, the voltagedrop across this diode can prevent the on-board USB from functioning correctly. This problem can be resolved by shorting E17 to bypass the diode.

5.1.1.4 Option 4: 5 V Test Points

5 V may be supplied from an external power supply to test points on the board. TP7 (5 V) and TP9 (GND) are loop-style test points, and J60 provides large via style test points that can accommodate a 0.1" pin header or connector. Reverse current protection is provided at J60-1 whereas TP7 directly connects to the 5V input pins of the Power Management IC (PMIC) U13 and to the Main System 5V Power. Care must be taken before applying an external supply to this test point to ensure that that the polarity is correct. Failure to do so could result in damage to components on the PCB.

These test points can be found at the top left of the board above Pmod 1.





Figure 11. 5 Volt Test Point Location

5.1.2 Power Supply Considerations

The power required by the RZ MPU is provided by the DA9080 Power Management IC (PMIC). This PMIC has four buck regulators that provide the 1.1 V, 1.35 V, 1.8 V, and 3.3 V supplies required by the MPU, and ensures that these supplies ramp up and down with the correct sequence and timing during power-up and power-down. The device provides two Power Good outputs (PG1 and PG2) that go high when associated regulator outputs are stable. These two open-drain outputs have been connected together on the EK-RZ/A3M board and are used to provide the system reset signal (RESET_L).

Additionally, the PMIC provides a 3.3 V LDO. This supply has been made available for use externally.

The maximum current that can be drawn from these supplies is shown in Table 6.

Supply	Default Supply Voltage	Maximum Current
Buck 1	3.3 V	1.5 A
Buck 2	1.8 V	1.5 A
Buck 3	1.35 V	1.5 A
Buck 4	1.1 V	5.0 A
LDO	3.3 V	200 mA

Table 6. DA9080 PMIC Supply Output Capabilities

Make sure the total current required by the RZ MPU, any active on-board features, and any connected peripheral devices do not exceed these limits.

Note: The total current available depends on the configuration of the host USB port, for example an enumerated USB-A port may have a maximum output current capability of 500 mA. In these cases, multiple power sources may be required, for example by using power-only USB-C connector J6.

The DA9080 PMIC provides a number of features such as the ability to adjust buck regulator output voltages and includes two analog inputs. These features can be accessed via the connected I²C port (I2C0 Address: 0x1B).

Please note that with the attached LCD display, the power consumption of this board can be up to 3 A at 5 V. To satisfy this requirement, use of the USB-C power-only connector (J6) is recommended along with a power supply that is capable of supplying 3 Amps. A single USB-C connection can be limited to 1.5 Amps, so it may be necessary to use two USB-C sources to satisfy the power required, for example J6 and J10.

5.1.3 Power-up Behavior

When powered, the white LED near the center of the board (the "dash" in the EK-RZ/A3M name) will illuminate. For more details on initial power up behavior, see the *EK-RZ/A3M Quick Start Guide*.

5.1.4 PMIC Diagnostic Connector

The Power Management IC (PMIC) implements a number of status and control registers that are exposed via its I²C interface. These registers can be accessed by firmware running on the RZ MPU and by software running on a suitable external device. J8 (not fitted) has been provided for this purpose.



5.2 Debug and Trace

The EK-RZ/A3M board supports the following three debug modes.

Table 7. Debug Modes

Debug Modes	Debugger MCU (the device that connects to the IDE on PC)	Target MPU (the device that is being debugged)	Debugging Interface/Protocol	Connector Used
Debug on-board	RA4M2 (on-board)	RZ/A3M (on-board)	SWD, JTAG	USB-C (J10)
Debug in	External debugging tools	RZ/A3M (on-board)	SWD, JTAG	20-pin connector (J20) or 10-pin connector (J13)

Notes:

- See Table 9 for the Debug USB connector pin definition.
- See Table 12 for the 20-pin JTAG connector pin definition.
- See Table 13 for the 10-pin JTAG connector pin definition.

The following table summarizes the jumper configuration for each of the debug modes.

Table 8. Jumper Connection Summary for Different Debug Modes

Debug Modes	J9
Debug on-board	Link 2-3
Debug in	Link 1-2

5.2.1 Debug On-Board

The on-board debug functionality is provided using Renesas RA4M2 Debug MCU and SEGGER J-Link[®] firmware. Debug USB-C connector (J10) connects the RA4M2 Debug MCU to an external USB Full Speed Host, allowing re-programming and debugging of the target RZ MPU firmware. This connection is the default debug mode for the EK-RZ/A3M board.

The RA4M2 Debug MCU connects to the target RZ MPU using the JTAG or SWD interface. Please refer to Table 4 for detailed configuration information.

Table 9. Debug USB Port Assignments

Debug USB Port Assignments		EK-RZ/A3M
Pin	Description	Signal/Bus
J10-A1	GND	GND
J10-A2	TX1+	NC
J10-A3	TX1-	NC
J10-A4	VBUS	P5V_USB_DBG
J10-A5	CC1	USB_JLOB_CC1
J10-A6	DA+	USB_D_P
J10-A7	DA-	USB_D_N
J10-A8	SBU1	NC
J10-A9	VBUS	P5V_USB_DBG
J10-A10	RX2-	NC
J10-A11	RX2+	NC
J10-A12	GND	GND
J10-B1	GND	GND
J10-B2	TX2+	NC
J10-B3	TX2-	NC
J10-B4	VBUS	P5V_USB_DBG



Debug USB Port Assignments		EK-RZ/A3M
Pin	Description	Signal/Bus
J10-B5	CC2	USB_JLOB_CC2
J10-B6	DB+	USB_D_P
J10-B7	DB-	USB_D_N
J10-B8	SBU2	NC
J10-B9	VBUS	P5V_USB_DBG
J10-B10	RX1-	NC
J10-B11	RX1+	NC
J10-B12	GND	GND
J10-S1	SHIELD	GND
J10-S2	SHIELD	GND
J10-S3	SHIELD	GND
J10-S4	SHIELD	GND

A yellow indicator, LED5, shows the visual status of the debug interface. When the EK-RZ/A3M board is powered on, and LED5 is blinking, it indicates that the RA4M2 Debug MCU is not connected to a programming host. When LED5 is on solid, it indicates that the RA4M2 Debug MCU is connected to a programming interface.

To configure the EK-RZ/A3M board to use the Debug On-Board mode, configure the jumpers using the following table.

Table 10. Debug On-Board Jumper Configuration

Location	Jumper Position	Function
J9	Link 2-3	RA4M2 Debug MCU in normal operation mode



Figure 12. EK-RZ/A3M Debug Interface



5.2.2 Debug In

One 20-pin Cortex[®] Debug Connector at J20 supports JTAG, SWD debug. One 10-pin Cortex[®] Debug Connector at J13 supports JTAG and SWD. Either of these connectors may be used for external debug of the target RZ MPU.

To configure the EK-RZ/A3M board to use the Debug In mode, configure the jumpers using the following table.

Table 11. Debug In Mode Jumper Configuration

Location	Jumper Position	Function
J9	Link 1-2	RA4M2 Debug MCU is held in RESET

Table 12. JTAG/SWD Port Assignments (J20)

JTAG/SWD Port Assignments			EK-RZ/A3M
Pin	JTAG Pin Name	SWD Pin Name	Signal/Bus
J20-1	Vtref	Vtref	+3V3
J20-2	TMS`	SWDIO	TMS_SWDIO
J20-3	GND	GND	GND
J20-4	ТСК	SWCLK	TCK_SWCLK
J20-5	GND	GND	GND
J20-6	TDO	SWO	TDO_SWO/P21_1
J20-7	Key	Key	NC
J20-8	TDI	N/A	TDI/P21_0
J20-9	GNDDetect	GNDDetect	GND (cut E30 to open)
J20-10	nSRST	nSRST	RESET_L
J20-11	GND	GND	GND
J20-12	N/A	N/A	NC
J20-13	GND	GND	GND
J20-14	N/A	N/A	NC
J20-15	GND	GND	GND
J20-16	N/A	N/A	NC
J20-17	GND	GND	GND
J20-18	N/A	N/A	NC
J20-19	GND	GND	GND
J20-20	N/A	N/A	NC

Table 13. JTAG/SWD Port Assignments (J13)

JTAG/SWD Port Assignments			EK-RZ/A3M
Pin	JTAG Pin Name	SWD Pin Name	Signal/Bus
J13-1	Vtref	Vtref	+3V3
J13-2	TMS	SWDIO	TMS_SWDIO
J13-3	GND	GND	GND
J13-4	TCK	SWCLK	TCK_SWCLK
J13-5	GND	GND	GND
J13-6	TDO	SWO	TDO_SWO/P21_1
J13-7	Key	Key	NC
J13-8	TDI	N/A	TDI/P21_0
J13-9	GNDDetect	GNDDetect	GND (cut E30 to open)
J13-10	nSRST	nSRST	RESET_L

Note: The Cortex[®] Debug Connector is fully described in the Arm[®] CoreSight[™] Architecture Specification.



5.3 Ecosystem

The System Control and Ecosystem area provides users the option to simultaneously connect several thirdparty add-on modules compatible with five most popular ecosystems using the following connectors:

- 1. Two Seeed Grove[®] system (I²C/Analog) connectors (not populated)
- 2. SparkFun® Qwiic® connector (not populated)
- 3. Two Digilent Pmod[™] (SPI, UART and I²C) connectors
- 4. Arduino[™] (Uno R3) connector
- 5. MikroElektronika[™] mikroBUS connector (not populated)

5.3.1 Seeed Grove[®] Connections

5.3.1.1 Grove 1

A Seeed Grove[®] I²C connector footprint is provided at J27. The RZ MPU acts as a two-wire serial master in I²C mode, and a connected module acts as a two-wire serial slave.

Table 14. Grove 1 Port Assignments

Grove 1 Connector		EK-RZ/A3M
Pin	Description	Signal/Bus
J27-1	SCL	SCL0
J27-2	SDA	SDA0
J27-3	VCC	+3.3 V
J27-4	GND	GND

5.3.1.2 Grove 2

A Seeed Grove[®] I²C connector footprint is provided at J28. The RZ MPU acts as a two-wire serial master, and a connected module acts as a two-wire serial slave.

To use analog pins AN0 and AN1 for analog input, the user must interface with the PMIC to obtain the reading. The I^2C address is 0x1B.

Option links E4, E5, E6 and E7 provide the capability to convert this connector to an analog Seeed Grove[®] implementation.

Table 15. Grove 2 Port Assignments

Grove 2 0	Connector	EK-RZ/A3M		
Pin	Description	Signal/Bus		
J28-1	SCL	P8_3 (SCL1) ^{*1}	AN0 ^{*2}	
J28-2	SDA	P8_2 (SDA1) ^{*1}	AN1*2	
J28-3	VCC	+3.3 V		
J28-4	GND	GND	GND	

^{*1} Jumpers E4 and E5 are open, E6 and E7 are closed

^{*2} Jumpers E4 and E5 are closed, E6 and E7 are open



Figure 13. Seeed Grove[®] and SparkFun[®] Qwiic[®] Connector Footprints

5.3.2 SparkFun[®] Qwiic[®] Connections

A SparkFun[®] Qwiic[®] connector footprint is provided at J30. The Main MPU acts as a two-wire serial master, and a connected module acts as a two-wire serial slave (data lines shared with Grove 1).



Table 16. Qwiic Port Assignments

Qwiic Connector		EK-RZ/A3M
Pin	Description	Signal/Bus
J30-1	GND	GND
J30-2	VCC	+3.3 V
J30-3	SDA	SDA0
J30-4	SCL	SCL0

5.3.3 Digilent Pmod[™] Connectors

Two 12-pin connectors are provided to support Pmod modules where the RZ MPU acts as the master, and the connected module acts as a slave device.

These interfaces may be configured in firmware to support several Pmod types such as Type-2A (expanded SPI), Type-3A (expanded UART) and Type-6A (I²C). Configured using SW4-1 and SW4-2 for Pmod 1 and SW4-3 for Pmod 2. These options are also configurable in software using the IO expander (U2).

The default 12-pin Pmod interface supports +3.3 V devices. Please ensure that any Pmod device installed is compatible with a +3.3 V supply.

5.3.3.1 Pmod 1

A 12-pin Pmod connector is provided at J26, Pmod 1.

This Pmod connector is controlled by switch SW4 options (SW4-1) and (SW4-2).

 Table 17. Pmod 1 Port Assignments

Pmod 1	Connector			EK-RZ/A3M	Pmod 1 C	onfiguration
Pin	Option Type-2A (SPI) ^{*1}	Option Type-3A (UART) ^{*1}	Option Type-6A (l ² C)* ¹	Signal/Bus	Short	Open
J26-1	SS			P12_1 (SSL0)		
		CTS		P12_0 (CTS2)		
			INT	P11_2 (IRQ6)		
J26-2	MOSI			P11_3 (MOSI0)		
		TXD		P2_3 (TXD2)		
			RESET	P12_0 (GPIO)		
J26-3	MISO			P12_0 (MISO0)		
		RXD		P3_0 (RXD2)		
			SCL	SCL0		
J26-4	SCK			P11_2 (CK0)		
		RTS		P12_1 (RTS2)		
			SDA	SDA0		
J26-5	GND			GND		
J26-6	VCC ^{*2}			+3.3 V	E25	E35
				+5.0 V	E35	E25
J26-7	IRQ			P5_1 (IRQ7)		
J26-8	RESET (m	aster to slave	e)	P0_2		
J26-9	GPIO			P0_1		
J26-10	GPIO			P0_0		
J26-11	GND			GND		
J26-12	VCC*2			+3.3 V	E25	E35
				+5.0 V	E35	E25

^{*1} Option is selected by setting switches SW4-1 and SW4-2 as follows:



Table 18. Pmod 1 Mode Selection

SW4-2	SW4-1	Selected Function	Conflict
Off	Off	SPI	SD Card ^{*1}
Off	On	UART	-
On	Off	I ² C	-
On	On	Disabled	-

- ^{*1} Conflict: To use Pmod 1 in SPI mode at the same time as using the SD card, then J15 must be linked 2-3 (use P3_1 for card detect).
- Caution: 5 V optional supply is provided (J26-6 and J26-12), however the interface must only be driven with 3.3 V signals from the Pmod 1. The EK-RZ/A3M will only provide 3.3 V signal levels to the Pmod 1.



Figure 14. Pmod 1 Connector

Pmod 2

A 12-pin Pmod connector is provided at J25, Pmod 2.

Table 19. Pmod 2 Port Assignments

Pmod 2 Connector			EK-RZ/A3M Signal/Bus	
Pin	Option	Option	SPI	UART
	Type-2A (SPI) *1	Type-3A (UART) *1		
J25-1	SS	CTS	P2_0 (SSL1)	P1_3 (CTS1)
J25-2	MOSI	TXD	P1_3 (MOSI1)	P1_0 (TXD1)
J25-3	MISO	RXD	P1_4 (MISO1)	P1_1 (RXD1)
J25-4	SCK	RTS	P1_2 (CK1)	P1_4 (RTS1)
J25-5	GND		GND	
J25-6	VCC		+3.3 V	
J25-7	IRQ		P11_0 (IRQ4)	
J25-8	RESET (master to	slave)	P4_2	
J25-9	GPIO		P4_1	
J25-10	GPIO		P4_0	
J25-11	GND		GND	
J25-12	VCC		+3.3 V	

^{*1} Option is selected by setting switches SW4-3 as follows:

Table 20. Pmod 2 Mode Selection

SW4-3	Selected Function
Off	SPI
On	UART

Note: If CTS and RTS are not needed when using Type-3A (UART) mode, then they may be disconnected via trace-cut links E1 and E10.





Figure 15. Pmod 2 Connector

5.3.4 Arduino[™] Connector

Near the center of the System Control and Ecosystem Access area is an Arduino[™] Uno R3 compatible connector interface.

To use analog pins A0 and A1 for analog input, the user must interface with the PMIC to obtain the reading. The I2C address is 0x1B.

Table 21.	Arduino	Uno	Port A	ssignments
-----------	---------	-----	--------	------------

Arduino	Compatible Co	onnectors		EK-RZ/A3M
Pin	Description			Signal/Bus
J18-1	N.C.			NC
J18-2	IOREF			+3.3 V
J18-3	RESET			P2_1
J18-4	3.3 V			+3.3 V
J18-5	5 V			+5 V
J18-6	GND			GND
J18-7	GND			GND
J18-8	VIN			NC
J19-1	A0			AN0 (can be read via the DA9080 PMIC using I ² C0)
J19-2	A1			AN1 (can be read via the DA9080 PMIC using I ² C0)
J19-3	A2			NC
J19-4	A3			NC
J19-5	A4			NC
J19-6	A5			NC
J23-1	D0	RXD		P7_1 (RXD4 / MTIOC1A)
J23-2	D1	TXD		P7_0 (TXD4)
J23-3	D2	INT0		P4_5 (IRQ5 / MTIOC7C)
J23-4	D3	INT1	PWM	P5_0 (IRQ6 / MTIOC7D)
J23-5	D4			P8_0 (IRQ0 / MTIOC1B)
J23-6	D5		PWM	P3_3 (IRQ4 / MTIOC6C)
J23-7	D6		PWM	P5_2 (MTIOC8B)
J23-8	D7			P5_3 (MTIOC2A)
J24-1	D8			P6_4
J24-2	D9		PWM	P5_4 (MTIOC2B)
J24-3	D10	SPI_SS	PWM	P2_0 (SSLB / MTIOC3B)
J24-4	D11	SPI_MOSI	PWM	P1_3 (MOSIB)
J24-5	D12	SPI_MISO		P1_4 (MISOB / MTIOC3A)
J24-6	D13	SPI_SCK		P1_2 (CKB)
J24-7	GND			GND
J24-8	ARDUINO_A	REF		+3.3 V



Arduino Compatible Connectors		EK-RZ/A3M
Pin	Description	Signal/Bus
J24-9	I2C_SDA	SDA0
J24-10	I2C_SCL	SCL0



Figure 16. Arduino Uno Connectors

5.3.5 MikroElektronika™ mikroBUS Connector

In the center of the System Control and Ecosystem Access area is a mikroBUS compatible connector interface. This interface is compliant with mikroBUS Standard Specifications revision 2.00.

To use analog pins AN for analog input, the user must interface with the PMIC to obtain the reading. The I^2C address is 0x1B.

Table 22. mi	kroBUS Port	Assignments
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mikroBUS Port Connectors		EK-RZ/A3M
Pin	Description	Signal/Bus
J21-1	AN (Analog)	AN0 (can be read via the DA9080 PMIC using I ² C0)
J21-2	RST (Reset)	P6_2 (MIKROBUS_RESET_L)
J21-3	CS (SPI Chip Select)	P2_0 (SSLB)
J21-4	SCK (SPI Clock)	P1_2 (CKB)
J21-5	MISO	P1_4 (MISOB)
J21-6	MOSI	P1_3 (MOSIB)
J21-7	+3.3 V	+3.3 V
J21-8	GND	GND
J22-1	PWM	P5_0 (MTIOC7D)
J22-2	INT (Hardware Interrupt)	P4_5 (IRQ5)
J22-3	RX (UART Receive)	P7_1 (RXD4)
J22-4	TX (UART Transmit)	P7_0 (TXD4)
J22-5	SCL (I ² C Clock)	SCL0
J22-6	SDA (I ² C Data)	SDA0
J22-7	+5 V	+5 V
J22-8	GND	GND





5.4 Miscellaneous

5.4.1 User and Power LEDs

Five LEDs are provided on the EK-RZ/A3M board.

Behavior of the LEDs on the EK-RZ/A3M board is described in the following table.

Table 23. EK-RZ/A3M Board LED Functions

Designator	Color	Function	MPU Control Port
LED1	Blue	User LED	P10_1
LED2	Green	User LED	P20_3
LED3	Red	User LED	P20_4
LED4	White	Power on indicator	+3.3 V
LED5	Yellow	Debug LED	J-Link OB MCU

The user LEDs may be isolated from the main MPU, so the associated ports can be used for other purposes. To separate LED1 from P10_1, trace cut jumper E27 must be open. To separate LED2 from P20_3, trace cut jumper E26 must be open. To separate LED3 from P20_4, trace cut jumper E28 must be open.

Please note that P20_3 is also connected to the boot mode selection switch SW2-3. Depending on the setting of this switch, LED2 may glow until P20_3 is configured as an output and driven to turn the LED either on or off.



Figure 17. User LEDs



Figure 18. Power LED





Figure 19. Debug LED

5.4.2 User and Reset Switches

Three miniature, momentary, mechanical push-button type SMT switches are mounted on the EK-RZ/A3M board.

Pressing the reset switch (SW3) generates a reset signal to restart the RZ MPU.

Table 24. EK-RZ/A3M Board Switches

Designator	Function	MPU Control Port	Button Color
SW3	MPU Reset Switch	PRST_N	Red
SW2	User Switch	P11_1 (IRQ5)	Blue
SW1	User Switch	P10_3 (IRQ3)	Blue

The user switches SW1 and SW2 may be isolated from the main MPU, so the associated ports can be used for other purposes. To separate SW1 from P10_3, trace cut jumper E31 must be open. To separate SW2 from P11_1, trace cut jumper E32 must be open.



Figure 20. Reset and User Switches



6. Special Feature Access Area

The Special Feature Access area provides features specific to the RZ/A3M MPU group such as SD card, audio CODEC and USB High Speed (Host and Device). The switches to control the peripheral interface selection is also provided.

Note: Normally the Quad-SPI devices would be in this area, however, to optimize the layout for these highspeed devices, they have been placed in the MPU Native Pin Access area.



Figure 21. Special Feature Access Area

6.1 USB High Speed

The USB-C connection jack (J7) connects the RZ MPU USB High Speed interface to an external USB interface, allowing communications for testing and use of the RZ MPU firmware. This connection can be configured as either a USB Device or a USB Host interface.

USB-C power controller U4 is compliant with USB Power Delivery Specification Revision 3.0 and USB Power Delivery Specification Revision 2.0. The controller will automatically negotiate power level and direction as required depending on the device attached. This is done independently from the data configuration (Device or Host) of the USB port. As an Upward Facing Port (UFP) the controller is programmed to request a maximum of 3A of 5V power from the attached device. As a Downward Facing Port (DFP) the controller is programmed to supply a maximum of 3A of 5V power to the attached device. There are some circumstances though (for example an attached device that can be either an upstream device or a downstream device) when the mode negotiated (UFP or DFP) is not what is desired. In this case, toggling SW4-4 (turn on, then turn off) will cause the power controller to swap to the other mode.

For a USB Device configuration, configure the RZ MPU firmware to use the USB High Speed port in device mode. Power from an external USB Host on this connection (UFP) is typically used to provide power to the EK-RZ/A3M board.

For a USB Host configuration, configure the RZ MPU firmware to use the USB High Speed port in host mode. In this configuration (DFP) power to J7 is typically supplied via Q11 under the control of U4. The total current available is 3 A. Note that the input power sources must be configured with enough power for both the EK-RZ/A3M board and the USB High Speed port in host mode. To use devices with a USB Type-A connector, connect a USB Type-A female to USB-C male cable to J7. Devices with a USB-C connector do not require this cable.

Table 25. USB High Speed Port Assignments

USB High Speed Connector		EK-RZ/A3M
Pin	Description	Signal/Bus
J7-A1	GND	GND
J7-A2	TX1+	NC
J7-A3	TX1-	NC
J7-A4	VBUS	USBHS_cVBUS_CON



USB High Speed Connector		EK-RZ/A3M
Pin	Description	Signal/Bus
J7-A5	CC1	USB_HS_CC1
J7-A6	DA+	USBHS_P
J7-A7	DA-	USBHS_N
J7-A8	SBU1	NC
J7-A9	VBUS	USBHS_cVBUS_CON
J7-A10	RX2-	NC
J7-A11	RX2+	NC
J7-A12	GND	GND
J7-B1	GND	GND
J7-B2	TX2+	NC
J7-B3	TX2-	NC
J7-B4	VBUS	USBHS_cVBUS_CON
J7-B5	CC2	USB_HS_CC2
J7-B6	DB+	USBHS_P
J7-B7	DB-	USBHS_N
J7-B8	SBU2	NC
J7-B9	VBUS	USBHS_cVBUS_CON
J7-B10	RX1-	NC
J7-B11	RX1+	NC
J7-B12	GND	GND
J7-S1	SHIELD	GND
J7-S2	SHIELD	GND
J7-S3	SHIELD	GND
J7-S4	SHIELD	GND



Figure 22. USB High Speed Connector



6.2 Quad-SPI Flash

Included on the EK-RZ/A3M board is U16, a 256 Mb (32 MB) Quad serial flash NOR memory (MX25L25645GZNI) and U19, a 1024Mb (128MB) Quad serial NAND flash memory (W25N01GVZEIG). Only one device can be used at a time, and this is selected using SW4-5 (see table below). The RZ MPU defaults to standard SPI mode initially and the flash memory is enabled for XIP (Execute-In-Place) mode directly after power-on.

Table 26. QSPI Flash Memory Selection

Switch	Off	On
SW4-5	32MB NOR flash MX25L25645GZNI selected	128MB NAND flash W25N01GVZEIG selected

Table 27. Quad-SPI Flash Assignments

Quad-SPI Flash Signal Description	EK-RZ/A3M Signal/Bus
QSPI_SEL	SW4-5 (PI4IOE5V6408 I/O expander P4)
QSPI_FLASH_CS#	QSPI_SSL
QSPI_FLASH_CLK	QSPI0_SPCLK
QSPI_FLASH_DQ0	QSPI0_IO0
QSPI_FLASH_DQ1	QSPI0_IO1
QSPI_FLASH_DQ2	QSPI0_IO2
QSPI_FLASH_DQ3	QSPI0_IO3



Figure 23. Quad-SPI Flash (labelled as "QUADSPI" on silkscreen text)

6.3 SD Card Connector

Included on the EK-RZ/A3M board is a micro-SD card socket (J11) and circuitry to select the SD card I/O voltage (1.8 V or 3.3 V). Table 28 below gives the SD card connections and port assignments.

Table 28. SD Card Socket Connections

J11 Pin	Function	EK-RZ/A3M signal
1	DAT2	P22_3 (SD0_DATA2)
2	DAT3	P22_4 (SD0_DATA3)
3	CMD	P22_0 (SD0_CMD)
4	VDD	+3.3 V
5	CLK	SD0_CLK
6	VSS	GND
7	DAT0	P22_1 (SD0_DATA0)
8	DAT1	P22_2 (SD0_DATA1)
9	SW1	P11_3 or P3_1 (see Table 29 below) (SD0_CD)



Note: The SD card can be used at the same time as the RGB LCD, or at the same time as Pmod 1. See Table 29 for the options.

	Table 29.	SD	Card	Detect	Port	Selection
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J15 Setting	EK-RZ/A3M Signal For SD0_CD	Description
Link 1-2	P11_3	The SD card can be used at the same time as the Parallel Graphics Display Port, but not at the same time as Pmod1
Link 2-3	P3_1	The SD card can be used at the same time as Pmod1, but not at the same time as the Parallel Graphics Display Port
		J15 TP6 SD CD

Figure 24. SD Card Detect Port Selection Header

Table 30. SD Card I/O Voltage Selection

Voltage	P9_4 level	Description
1.8 V	1	Set the SD card I/O voltage to 1.8 V
3.3 V	0 (default)	Set the SD card I/O voltage to 3.3 V

P9_4 can be disconnected and used for other purposes by cutting link E2. If this is done, then the SD card I/O voltage will be set to 3.3 V.



Figure 25. Micro SD Card Socket

6.4 Real Time Clock (RTC)

Included on the EK-RZ/A3M is an ISL1208IB8Z Real Time Clock chip. This can be backed up if desired by fitting an EDS224Z3R6V supercapacitor at C26.

The connections to the RZ MPU are detailed in Table 31.

Table 31. RTC Connections

RTC Connection	RZ/A3M MPU Connection	Description
IRQ#	P10_0 (IRQ0)	Connects the RTC interrupt pin to IRQ0. Note that this interrupt is shared with the PI4IOE5V6408 I/O expander U2. To also use this interrupt for the RTC, solder-blob link E9 needs to be made
SCL	SCL0	I ² C port 0 SCL
SDA	SDA0	I ² C port 0 SDA





Figure 26. Real Time Clock (RTC)

6.5 DA7212 Audio CODEC

The DA7212 is an ultra-low power audio CODEC targeting portable audio devices. The input paths support stereo FM line input and up to four analog (or two analog and two digital) microphones with two independent microphone biases. Audio output terminals are provided at J14 for connection to an external speaker and J17 for a combined connection to headphones and a microphone. The CODEC's Digital Audio Interface (DAI) has I²S input and output lines, and control registers can be accessed via the I²C port 0. Connections to and from the device are listed in Table 32.

Table 32. Audio CODEC Port Pin Assignme	nts
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SSIE/ I ² S Audio COI	DEC		EK-RZ/A3M
Device Pin Name Connector Pin		Description	Signal/Bus
MIC1_P	J17-1	Mic input 1 P	-
HP_L	J17-2	Headphone output L	-
HP_R	J17-3	Headphone output R	-
SP_P	J14-2	Speaker output +	-
SP_N	J14-1, J14-3	Speaker output -	-
SDA	-	I ² C data	SDA0
SCL	-	I ² C clock	SCL0
DATIN	-	DA7212 data input	P9_2
DATOUT	-	DA7212 data output	P9_3
BCLK	-	DA7212 bit clock	P9_0
WCLK	-	DA7212 word clock (L/R select)	P9_1
MCLK	-	DA7212 master clock	24MHz CODEC_CLK
GND_SENSE	J17-4	Headphone output ground reference	-
GND_CP	-	Digital ground/charge pump	GND
GND_A	-	Analog ground	GND
VDD_SP	-	Speaker driver supply	+5V
VDD_A	-	Analog supply	+1.8V
VDIG	-	Digital supply (LDO Output)	-
VDD_IO	-	Digital interface supply	+3.3V
DACREF	-	Audio DAC reference capacitor	-
VMID	-	Audio mid-rail reference capacitor	-
VREF	-	Bandgap reference capacitor	-





Figure 27. Audio CODEC (U12), Speaker Connector (J14), and Audio Jack (J17)

6.6 Parallel Graphics Display Expansion Interface

The RZ MPU parallel graphics display expansion ports can be configured with 8-8-8, and 6-6-6 color depth. Table 33 shows the Parallel Graphics Expansion Port Assignments and signal names for the EK-RZ/A3M board.

Some ports used for the parallel graphics display expansion port are also used by Arduino, Pmod and mikroBUS ports. To ensure correct operation, please do not use the parallel graphics display at the same time as Arduino, Pmod or mikroBUS.

Parallel Graphics Display Expansion Port		EK-RZ/A3M	-	
Pin	Description	Signal/Bus	RGB Signal (RGB888)	RGB Signal (RGB666)
J1-1	BL_EN	P10_2	BL_EN	BL_EN
J1-2	SDA	SDA1	SDA1	SDA1
J1-3	TP_INT	P8_1	INT	INT
J1-4	SCL	SCL1	SCL1	SCL1
J1-5	+3.3 V	+3.3 V	+3.3 V	+3.3 V
J1-6	DISP_RESET	RESET_L	RESET_L	RESET_L
J1-7	+3.3 V	+3.3 V	+3.3 V	+3.3 V
J1-8	+5 V	+5 V	+5 V	+5 V
J1-9	DISP_VSYNC	P0_3	P0_3	P0_3
J1-10	DISP_CLK	P0_2	P0_2	P0_2
J1-11	DISP_DE	P0_1	P0_1	P0_1
J1-12	DISP_HSYNC	P0_0	P0_0	P0_0
J1-13	-	NC	-	-
J1-14	-	NC	-	-
J1-15	DISP_DATA17	P4_4	B1	B1
J1-16	DISP_DATA16	P4_3	B0	B0
J1-17	DISP_DATA19	P5_0	B3	B3
J1-18	DISP_DATA18	P4_5	B2	B2
J1-19	DISP_DATA21	P5_2	B5	B5
J1-20	DISP_DATA20	P5_1	B4	B4
J1-21	DISP_DATA23	P5_4	B7	NC
J1-22	DISP_DATA22	P5_3	B6	NC
J1-23	DISP_DATA9	P3_0	G1	G1
J1-24	DISP_DATA8	P2_3	G0	G0
J1-25	DISP_DATA11	P3_2	G3	G3

Table 33. Parallel Graphics Display Expansion Interface Assignments



Parallel Graphics Display Expansion Port		EK-RZ/A3M		
Pin	Description	Signal/Bus	RGB Signal (RGB888)	RGB Signal (RGB666)
J1-26	DISP_DATA10	P3_1	G2	G2
J1-27	DISP_DATA13	P4_0	G5	G5
J1-28	DISP_DATA12	P3_3	G4	G4
J1-29	DISP_DATA15	P4_2	G7	NC
J1-30	DISP_DATA14	P4_1	G6	NC
J1-31	DISP_DATA1	P1_1	R1	R1
J1-32	DISP_DATA0	P1_0	R0	R0
J1-33	DISP_DATA3	P1_3	R3	R3
J1-34	DISP_DATA2	P1_2	R2	R2
J1-35	DISP_DATA5	P2_0	R5	R5
J1-36	DISP_DATA4	P1_4	R4	R4
J1-37	DISP_DATA7	P2_2	R7	NC
J1-38	DISP_DATA6	P2_1	R6	NC
J1-39	GND	GND	GND	GND
J1-40	GND	GND	GND	GND



Figure 28. Parallel Graphics Display Expansion Port Connector



7. MPU Native Pin Access Area



Figure 29. Native Pin Access Area

7.1 Pin Headers (not populated)

The EK-RZ/A3M board pin header footprints, J1, J2 and J3 provide access to nearly all RZ MPU interface signals, and to voltages for all RZ MPU power ports. Each header pin is labelled with the voltage or port connected to that pin. Refer to the RZ/A3M MPU Group User's Manual for details of each port function, and the EK-RZ/A3M board schematic for pin header port assignments.

7.2 MPU Current Measurement

Included in the Native Pin Access area are current measurement resistors and test points to measure the MPU USB controller current and the MPU core power current.

The EK-RZ/A3M board provides precision 5 m Ω resistors (Yageo, part number PS0612FKE070R005L) for current measurement of the main 1.1 V, 1.35 V, 1.8V and 3.3 V MPU power supplies. Measure the voltage drop across these resistors and use Ohm's Law to calculate the current. For convenience, TP1 and TP3 are provided to measure the main 1.1 V MPU supply current. TP2 and TP4 are provided to measure the 3.3 V MPU supply current. TP17 and TP18 are provided to measure the 1.8 V MPU supply current. TP19 and TP20 are provided to measure the 1.35 V MPU supply current. See Figure 31 - Figure 34 for the locations of TP1, TP2, TP3, TP4, TP17, TP18, TP19 and TP20 on the schematic.



Figure 30. RZ +3.3 V Supply Current Measurement Circuit





Figure 31. RZ +1.8 V Supply Current Measurement Circuit



Figure 32. RZ +1.35 V Supply Current Measurement Circuit



Figure 33. RZ +1.1 V Supply Current Measurement Circuit



Figure 34. RZ MPU Supply Current Measurement Resistors and Test Points



8. Expansion Boards

The EK-RZ/A3M kit includes the MIPI Graphics expansion board 2.

8.1 MIPI Graphics Expansion Board 2

8.1.1 Connecting the Graphics Expansion Board 2 to the EK-RZ/A3M Board

The MIPI Graphics Expansion Board 2 features an 1280 x 720 TFT LCD with capacitive touch overlay to be connected to the RZ MPU using the MIPI Graphics Expansion Port (J32). It is attached using adhesive pads. LCD connectors are under the LCD panel and above the PCB, they will not be accessible when the display is mounted.



Figure 35. EK-RZ/A3M Board Connected with MIPI Graphics Expansion Board 2



8.1.2 Signal Assignments

The MIPI Graphics Expansion Port J32 connects the EK-RZ/A3M board to the MIPI Graphics Expansion Board 2 supplied as part of the kit.

MIPI Expansion	n Port Assignments	EK-RZ/A3M
Pin	Description	Signal/Bus
J32-1	GND	GND
J32-2	GND	GND
J32-3	DATA0_P	DSI_DATA0_P
J32-4	DATA1_P	DSI_DATA1_P
J32-5	DATA0_N	DSI_DATA0_N
J32-6	DATA1_N	DSI_DATA1_N
J32-7	GND	GND
J32-8	GND	GND
J32-9	DATA2_P	DSI_DATA2_P
J32-10	DATA3_P	DSI_DATA3_P
J32-11	DATA2_N	DSI_DATA2_N
J32-12	DATA3_N	DSI_DATA3_N
J32-13	GND	GND
J32-14	GND	GND
J32-15	CLK_P	DSI_CLK_P
J32-16	NC	NC
J32-17	CLK_N	DSI_CLK_N
J32-18	GND	GND
J32-19	GND	GND
J32-20	I ² C SDA	SDA1
J32-21	DIMMER	P10_2
J32-22	I ² C SCL	SCL1
J32-23	TP_INT	P8_1 (IRQ1)
J32-24	TP_RESET	RESET_L
J32-25	GND	GND
J32-26	GND	GND
J32-27	NC	NC
J32-28	NC	NC
J32-29	NC	NC
J32-30	NC	NC
J32-31	NC	NC
J32-32	NC	NC
J32-33	GND	GND
J32-34	GND	GND
J32-35	+1.8 V	+1.8 V
J32-36	+1.8 V	+1.8 V
J32-37	+3.3 V	+3.3 V
J32-38	+3.3 V	+3.3 V
J32-39	+5 V	+5 V
J32-40	+5 V	+5 V

Table 34.	MIPI Graphics	Expansion Po	ort Assignments
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9. Certifications

The EK-RZ/A3M v1 kit meets the following certifications/standards. See page 3 of this user's manual for the disclaimer and precautions.

9.1 EMC/EMI Standards

• FCC Notice (Class A)

FC This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. NOTE- This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- $-\!\!-\!$ Consult the dealer or an experienced radio/television technician for help.
- Innovation, Science and Economic Development Canada ICES-003 Compliance:
- CAN ICES-3 (A)/NMB-3(A)
- CE Class A (EMC)

This product is herewith confirmed to comply with the requirements set out in the Council

Directives on the Approximation of the laws of the Member States relating to Electromagnetic Compatibility Directive 2014/30/EU.

Warning – This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures to correct this interference.

• UKCA Class A (EMC)

This product is in conformity with the following relevant UK Statutory Instrument(s) (and its amendments): 2016 No. 1091 Electromagnetic Compatibility Regulations 2016.

CA Warning – This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures to correct this interference.

- Taiwan: Chinese National Standard 13438, C6357 compliance, Class A limits
- Australia/New Zealand AS/NZS CISPR 32:2015, Class A

9.2 Material Selection, Waste, Recycling and Disposal Standards

- EU RoHS
- WEEE
- China SJ/T 113642014, 10-year environmental protection use period.

9.3 Safety Standards

• UL 94V-0



10. Design and Manufacturing Information

The design and manufacturing information for the EK-RZ/A3M v1 kit is available in the "EK-RZ/A3M v1 Design Package" available on <u>renesas.com/ek-rza3m</u>

- Design package file name: ek-rza3m-v1-designpackage.zip
- Design package contents:
 - 1. EK-RZ/A3M Board design package: ek-rza3m-v1-designpackage.zip
 - 2. MIPI Graphics Expansion Board 2 design package: app_lcd-ek_mipi_2-v1-designpackage.zip

Table 35. EK-RZ/A3M Board Design Package Contents

File Type	Content	File/Folder Name
File (PDF)	Schematics	ek-rza3m-v1-schematics
File (PDF)	Mechanical Drawing	ek-rza3m-v1-mechdwg
File (PDF)	3D Drawing	ek-rza3m-v1-3d
File (PDF)	BOM	ek-rza3m-v1-bom
Folder	Manufacturing Files	Manufacturing Files
Folder	Design Files	Design Files-Altium Designer

Table 36. MIPI Graphics Expansion Board 2 Design Package Contents

File Type	Content	File/Folder Name
File (PDF)	Schematics	app_lcd-ek_mipi_2-v1-schematics
File (PDF)	Mechanical Drawing	app_lcd-ek_mipi_2-v1-mechdwg
File (PDF)	3D Drawing	app_lcd-ek_mipi_2-v1-3d
File (PDF)	BOM	app_lcd-ek_mipi_2-v1-bom
Folder	Manufacturing Files	Manufacturing Files
Folder	Design Files	Design Files-Altium

11. Website and Support

Visit the following URLs to learn about the kit and the RZ family of microprocessors, download tools and documentation, and get support.

EK-RZ/A3M ResourcesreneRZ Product InformationreneRenesas SupportreneRA Flexible Software Package (FSP)rene

renesas.com/ek-rza3m renesas.com/rz renesas.com/support renesas.com/fsp



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