

RA8T2 Group

Evaluation Kit for RA8T2 Microcontroller Group
EK-RA8T2 v1
User's Manual

Renesas RA Family
RA8 Series

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1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Precautions

This Evaluation Kit is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area, or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- Ensure attached cables do not lie across the equipment.
- Reorient the receiving antenna.
- Increase the distance between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that which the receiver is connected.
- Power down the equipment when not in use.
- Consult the dealer or an experienced radio/TV technician for help.

Note: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken:

- The user is advised that mobile phones should not be used within 10 m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Evaluation Kit does not represent an ideal reference design for an end product and does not fulfill the regulatory standards for an end product.

Renesas RA Family

EK-RA8T2 v1
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1. Kit Overview

The EK-RA8T2, an Evaluation Kit for RA8T2 MCU Group, enables users to seamlessly evaluate the features of the RA8T2 MCU group and develop embedded systems applications using Flexible Software Package (FSP) and e² studio IDE. Users have access to a range of on-board features and may also use compatible ecosystem add-ons to implement their projects.

The key features of the EK-RA8T2 board are categorized in three groups (consistent with the architecture of the kit, with a few exceptions) as follows:

MCU Native Pin Access

- R7KA8T2LFLCAC MCU (referred to as RA MCU)
- 1 GHz, Arm® Cortex®-M85 core
- 250 MHz, Arm® Cortex®-M33 core
- 1 MB MRAM, 2 MB SRAM with ECC
- 289 pins, BGA package
- Native pin access through 2 x 40-pin headers (not populated)
- SDRAM pin access through 2 x 26-pin headers (not populated)
- Ethernet pin access through 4 x 14-pin headers (not populated)
- GPTP pin access through 2 x 5-pin headers (not populated)
- TAS status pin access through 1 x 5-pin headers (not populated)
- MCU current measurement points for precision current consumption measurement
- Multiple clock sources – RA MCU oscillator and sub-clock oscillator crystals, providing precision 24.000 MHz and 32,768 Hz reference clocks. Additional low-precision clocks are available internal to the RA MCU

System Control and Ecosystem Access

- USB Full Speed Host and Device (USB-C connector)
- PMIC Diagnostic Port pin access through 4-pin header (not populated)
- Three 5 V input sources
 - USB (Debug, Full Speed)
 - External power supply (using surface mount clamp test points and power input vias)
- Three Debug modes
 - Debug on-board (SWD and JTAG)
 - Debug in (ETM, SWD, SWO, and JTAG)
 - Debug out (SWD, SWO, and JTAG)
- User LEDs, Status LEDs and switches
 - Three User LEDs (red, blue, green)
 - Power LED (white) indicating availability of regulated power
 - Debug LED (yellow) indicating the debug connection
 - Two User switches
 - One Reset switch
- Five most popular ecosystems expansions
 - Two Seeed Grove® system (I²C/I³C/Analog) connectors (not populated)
 - SparkFun Qwiic® connector (not populated)
 - Two Digilent Pmod™ (SPI, UART and I²C) connectors
 - Arduino™ (Uno R3) connector
 - MikroElektronika mikroBUS™ connector (not populated)
- Combined debugger and MCU boot configuration switches

Special Feature Access

- Ethernet (RJ45 GMII interface) x 2
- 64 MB (512 Mb) External Octo-SPI Flash (present in the MCU Native Pin Access area)
- 64 MB (512 Mb) SDRAM (present in the MCU Native Pin Access area)
- Hardware Configuration switches
- EtherCAT ID configuration switches
- 32 Kb EEPROM

- Ethernet activity LEDs (green x 2, yellow x 2)
- EtherCAT LEDs (red x 1, green x 3)
- Network LEDs (red x 2, green x 2)
- CAN-FD interface x 2
- Isolated MODBUS / RS485 interface

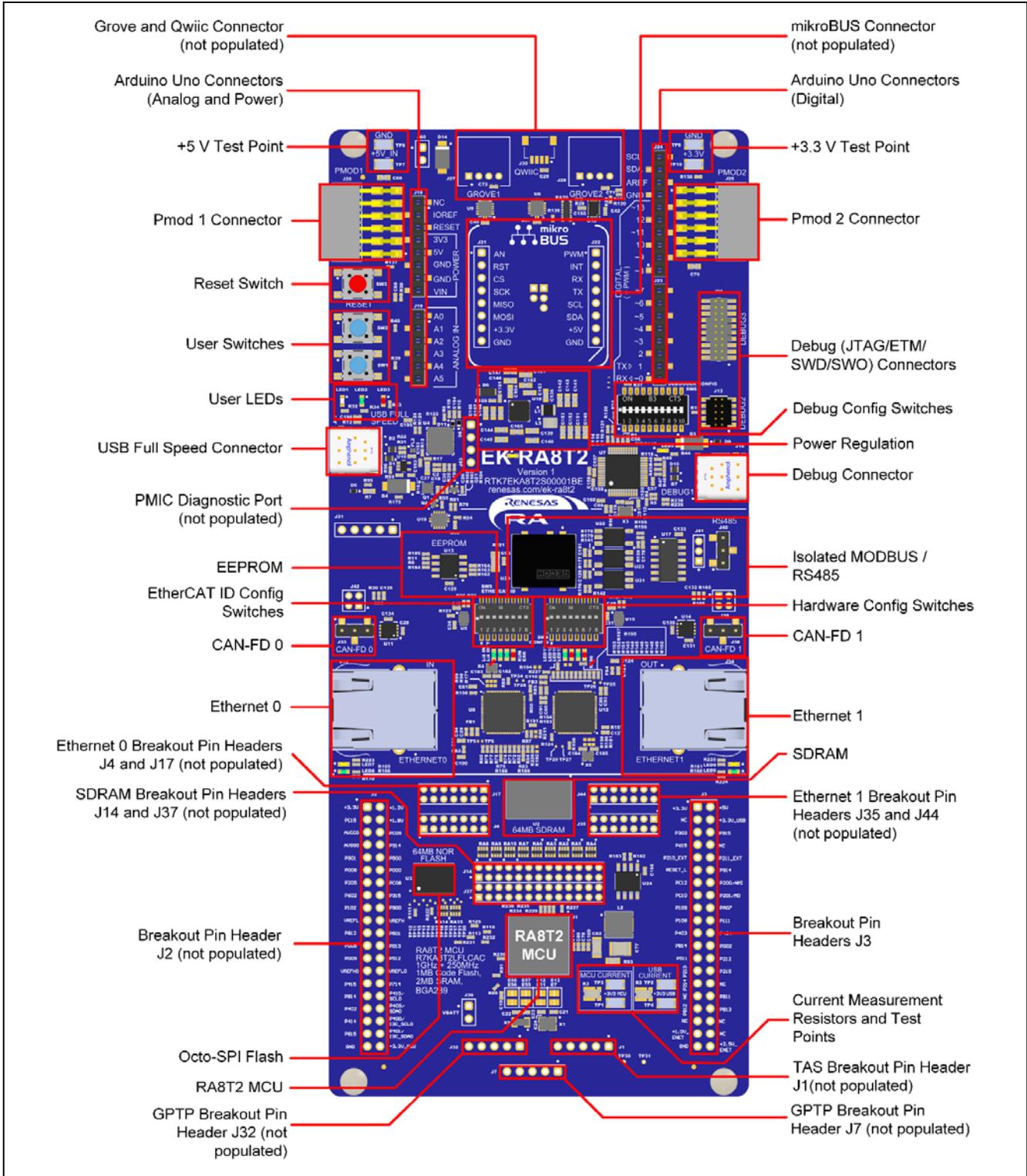


Figure 1. EK-RA8T2 Board Top Side

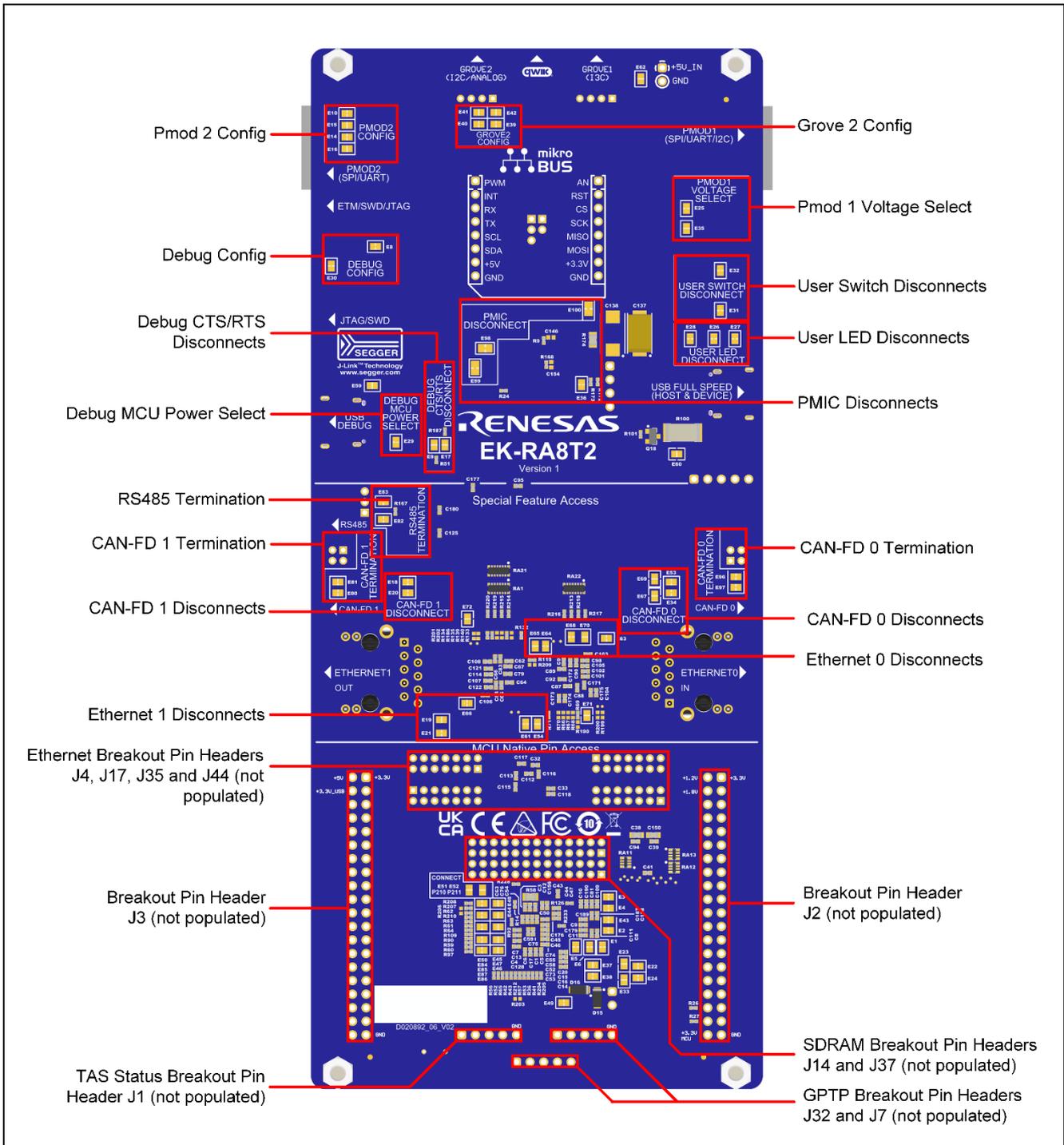


Figure 2. EK-RA8T2 Board Bottom Side

1.1 Assumptions and Advisory Notes

1. It is assumed that the user has a basic understanding of microcontrollers and embedded systems hardware.
2. It is recommended that the user refers to the *EK-RA8T2 Quick Start Guide* to get acquainted with the kit and the Quick Start example project that EK-RA8T2 board comes pre-programmed with.
3. Flexible Software Package (FSP) and Integrated Development Environment (IDE) such as e² studio are required to develop embedded applications on EK-RA8T2 kit.
4. Instructions to download and install software, import example projects, build them and program the EK-RA8T2 board are provided in the quick start guide.
5. The MCU fitted to the EK board may not contain the latest version of the on-chip boot firmware.

2. Kit Contents

The following components are included in the kit:

1. EK-RA8T2 v1 board
2. Board standoffs

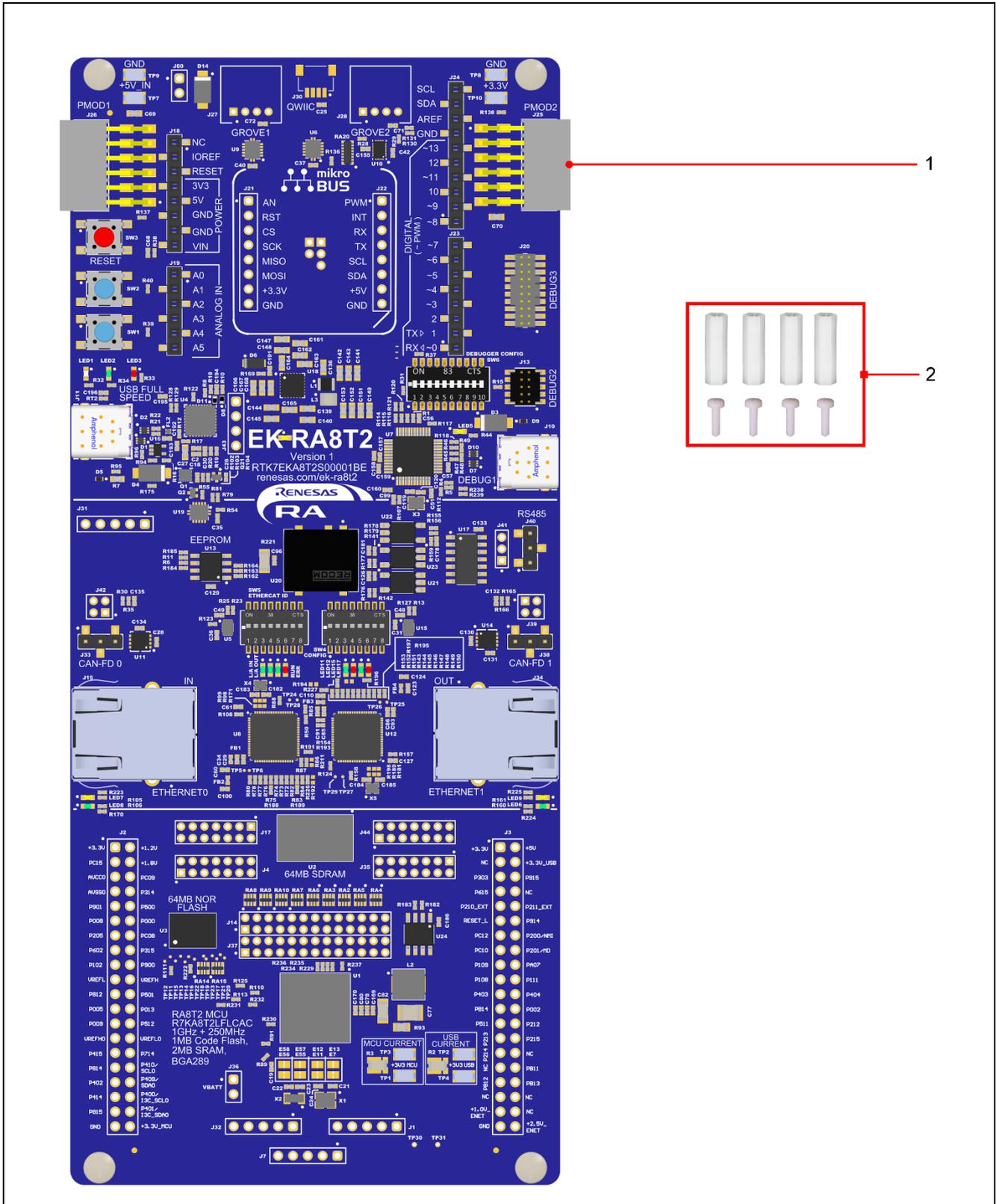


Figure 3. EK-RA8T2 Kit Contents

3. Ordering Information

- EK-RA8T2 v1 kit orderable part number: RTK7EKA8T2S00001BE

Notes: 1. The underlined character in the orderable part number represents the kit version.

- Dimensions
 - EK-RA8T2 board dimensions: 84 mm (width) x 195 mm (length)

4. Hardware Architecture and Default Configuration

4.1 Kit Architecture

The EK-RA8T2 board is designed with three sections or areas to help shorten the learning curve of the users and maximize the design and knowledge reuse among similar kits. The contents of these three areas are conceptually standardized among similar kits.

Table 1. Kit Architecture

Kit area	Area features	Area present on all similar kits	Functionality is:
MCU Native Pin Access Area	RA MCU, breakout pin headers for all MCU I/O and power, Current Measurement, Octo-SPI Flash, SDRAM	Yes	MCU dependent
Special Feature Access Area	Hardware Configuration Switches, EtherCAT ID Configuration Switches, EtherCAT LEDs, Network LEDs, Ethernet Phy LEDs, MCU special features: Ethernet, CAN-FD, isolated MODBUS / RS485 and EEPROM	No	MCU dependent
System Control and Ecosystem Access Area	Power, Debug MCU, User LEDs and Switches, USB Full Speed Host and Device, Reset Switch, Ecosystem Connectors and MCU Boot and Debugger Configuration Switches	Yes	Same or similar across similar kits

Note: The Octo-SPI Flash and SDRAM are among the Special Feature Access features. Normally, they would be in the Special Feature Access Area, however, to optimize the layout, routing, and performance, they are placed in the MCU Native Pin Access area.

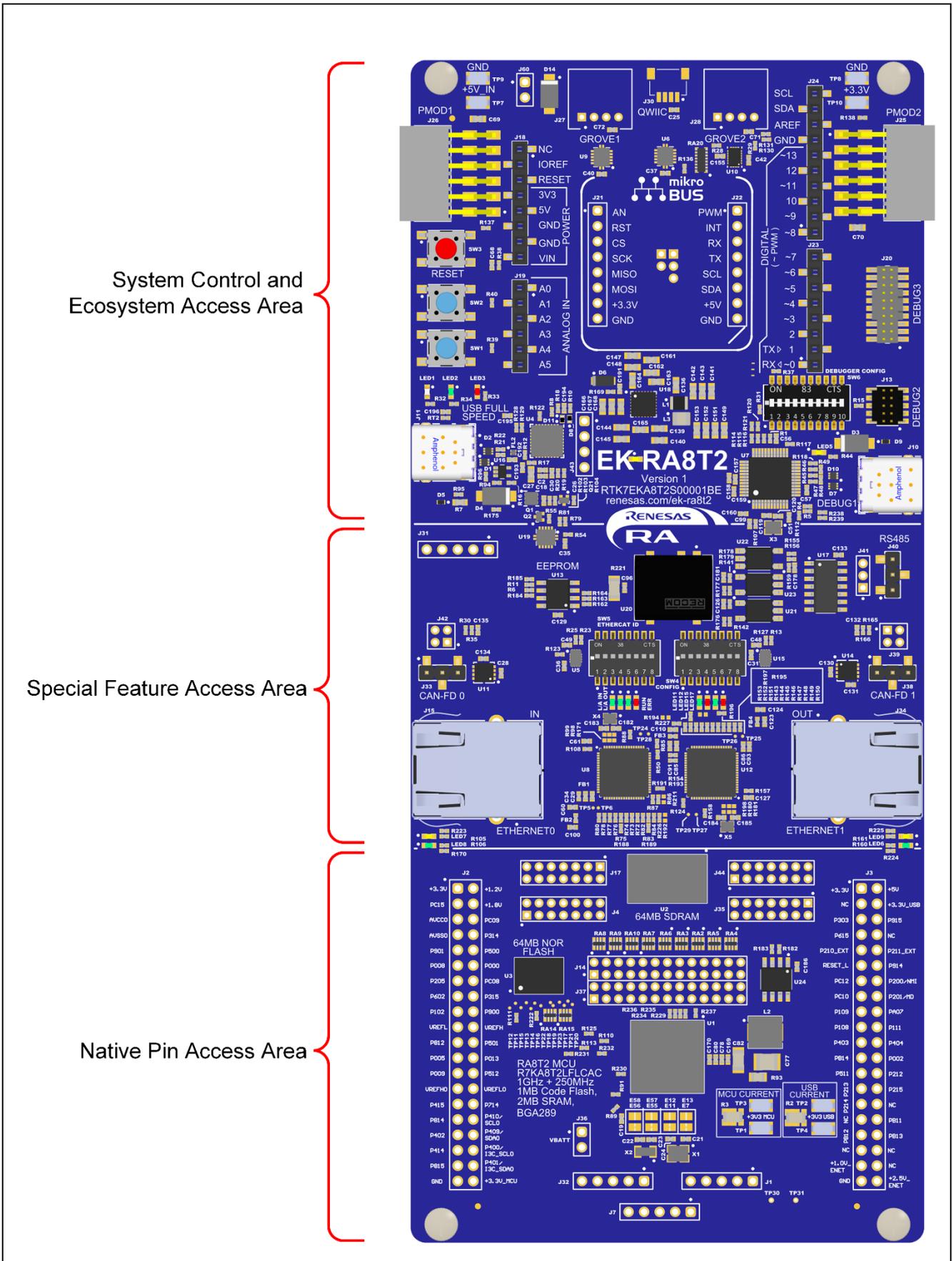


Figure 4. EK-RA8T2 Board Functional Area Definitions

4.2 System Block Diagram

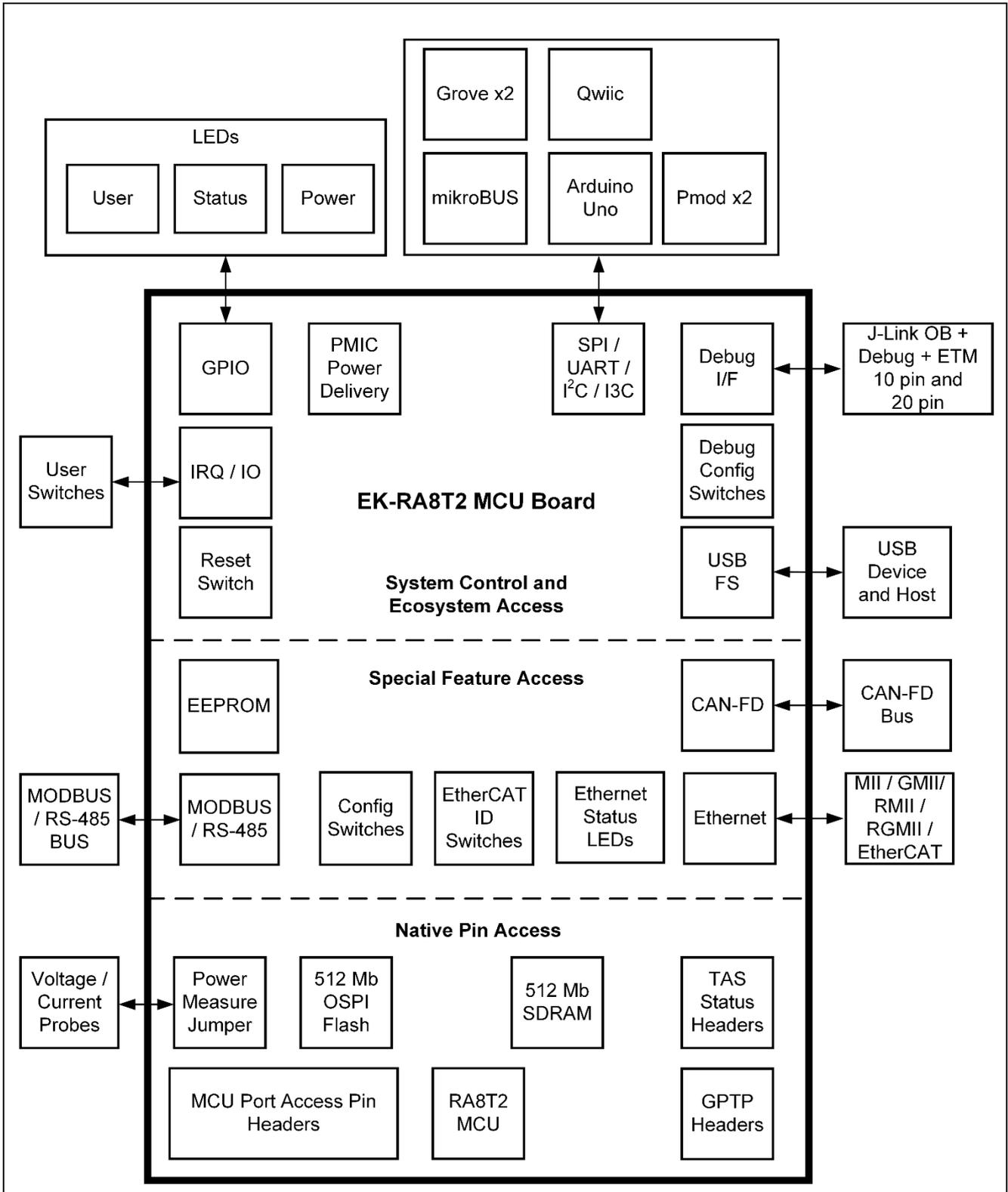


Figure 5. EK-RA8T2 Board Block Diagram

4.3 Jumper Configuration

Two types of jumpers are provided on the EK-RA8T2 board.

1. Copper jumpers (trace-cut type and solder bridge type)
2. Traditional pin header jumpers

The following sections describe each type and their default configuration.

4.3.1 Copper Jumpers

Copper jumpers are of two types, designated **trace-cut** and **solder-bridge**.

A **trace-cut jumper** is provided with a narrow copper trace connecting its pads. The silk screen overlay printing around a trace-cut jumper is a solid box. To isolate the pads, cut the trace between pads adjacent to each pad, then remove the connecting copper foil either mechanically or with the assistance of heat. Once the etched copper trace is removed, the trace-cut jumper is turned into a solder-bridge jumper for any later changes.

A **solder-bridge** jumper is provided with two isolated pads that may be joined together by one of three methods:

- Solder may be applied to both pads to develop a bulge on each and the bulges joined by touching a soldering iron across the two pads.
- A small wire may be placed across the two pads and soldered in place.
- A SMT resistor, size 0805, 0603, or 0402, may be placed across the two pads and soldered in place. A zero-ohm resistor shorts the pads together.

For any copper jumper, the connection is considered **closed** if there is an electrical connection between the pads (default for trace-cut jumpers.) The connection is considered **open** if there is no electrical connection between the pads (default for the solder-bridge jumpers.)

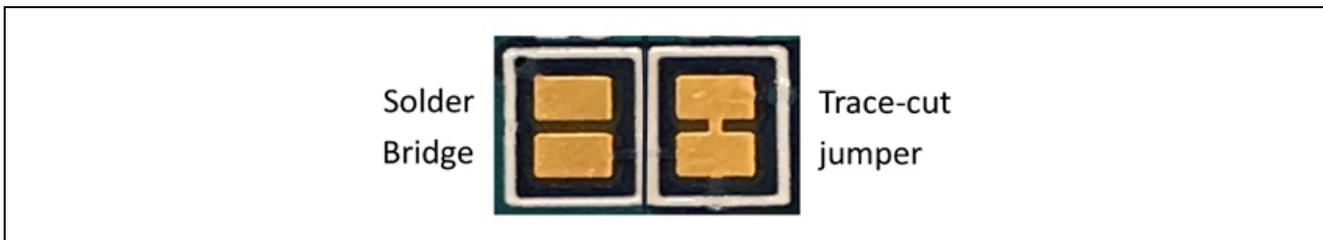


Figure 6. Copper Jumpers

4.3.2 Traditional Pin Header Jumpers

These jumpers are traditional small pitch jumpers that require an external shunt to open/close them. The traditional pin jumpers on the EK-RA8T2 board are 2 mm pitch headers and require compatible 2 mm shunt Jumpers.

4.3.3 Default Jumper Configuration

The following table describes the default configuration for each jumper on the EK-RA8T2 board. This includes copper jumpers (Ex designation) and traditional pin jumpers (Jx designation).

The Circuit Group for each jumper is the designation found in the board schematic (available in the Design Package). Functional details for many of the listed jumpers may be found in sections associated with each functional area of the kits.

Table 2. Default Jumper Configuration

Location	Circuit Group	Default Position	Function
J39	CAN-FD 1	Not populated	Link 1-2 to connect CAN-FD_L to R165 Link 3-4 to connect CAN-FD_H to R166
J41	RS485	Not populated	Link 1-2 to connect A/Y to R167
J42	CAN-FD 0	Not populated	Link 1-2 to connect CAN-FD_L to R30 Link 3-4 to connect CAN-FD_H to R35
E1	MCU Power	Closed	Connects VREFL to GND

Location	Circuit Group	Default Position	Function
E2	MCU Power	Closed	Connects VREFH to +3.3 V
E3	MCU Power	Closed	Connects AVCC0 to +3.3 V
E4	MCU Power	Closed	Connects AVSS0 to GND
E5	MCU Power	Closed	Connects VREFL0 to GND
E6	MCU Power	Closed	Connects VREFH0 to +3.3 V
E49	MCU Power	Closed	Connects VBATT to +3.3 V (P3V3_MCU)
E7	MCU Clock	Closed	Connects P212/EXTAL to 24 MHz crystal
E11	MCU Clock	Closed	Connects P213/XTAL to 24 MHz crystal
E12	MCU Clock	Open	Connects P213/XTAL to pin header J3 pin 26
E13	MCU Clock	Open	Connects P212/EXTAL to pin header J3 pin 27
E22	USB FS	Closed	Connects P814 (USB_D_P) to USBFS_P
E23	USB FS	Open	Connects P814 to pin header J2 pin 31
E24	USB FS	Closed	Connects P815 (USB_D_N) to USBFS_N
E33	USB FS	Open	Connects P815 to pin header J2 pin 37
E55	MCU Clock	Closed	Connects XCIN/P215 to 32.768 KHz crystal
E56	MCU Clock	Closed	Connects XCOU/P214 to 32.768 KHz crystal
E57	MCU Clock	Open	Connects XCIN/P215 to J3 pin 29
E58	MCU Clock	Open	Connects XCOU/P214 to J3 pin 28
E9	Debug	Open	Connects P512 (CTS) to Debug MCU port P408
E17	Debug	Open	Connects P511 (CTS_RTS) to Debug MCU port P409
E44	Debug	Open	Connects P304 (TDATA3) to J20 pin 20
E45	Debug	Open	Connects P305 (TDATA2) to J20 pin 18
E46	Debug	Open	Connects P306 (TDATA1) to J20 pin 16
E47	Debug	Open	Connects P307 (TDATA0) to J20 pin 14
E48	Debug	Open	Connects P308 (TCLK) to J20 pin 12
E51	Debug	Open	Connects P210 (SWDIO) to pin header J3 pin 9
E52	Debug	Open	Connects P211 (SWCLK) to pin header J3 pin 10
E30	JTAG	Closed	Connects the JTAG GND Detect pin on J20 and J13 to GND
E8	JTAG	Closed	Connects JTAG TDATA1 to JLOB_TRST
E29	Debug MCU Power	Closed	Connects the Debug MCU power to +3.3 V
E26	User LED	Closed	Connects P303 to User LED2
E27	User LED	Closed	Connects P714 to User LED1
E28	User LED	Closed	Connects PA07 to User LED3
E31	User Switch	Closed	Connects P009 to User Switch SW1
E32	User Switch	Closed	Connects P008 to User Switch SW2
E36	Power	Closed	Connects the PMIC PGOOD output to RESET_L
E43	Arduino	Closed	Connects ARDUINO_AREF to VREFH
E25	Pmod 1	Closed	Connects +3.3 V to Pmod 1 pins 6 and 12
E35	Pmod 1	Open	Connects +5.0 V to Pmod 1 pins 6 and 12
E10	Pmod 2	Closed	Connects PC15 (CTS6) to Pmod 2 pin 1
E14	Pmod 2	Closed	Connects PC11 (RTS6) to Pmod 2 pin 4
E15	Pmod 2	Open	Connects PC11 (SS6) to Pmod 2 pin 1
E16	Pmod 2	Open	Connects PC12 (SCK6) to Pmod 2 pin 4
E39	Grove 2	Closed	Connects P410 (I ² C SCL0) to Grove 2 pin 1
E40	Grove 2	Closed	Connects P409 (I ² C SDA0) to Grove 2 pin 2
E41	Grove 2	Open	Connects P005 (AN005) to Grove 2 pin 2
E42	Grove 2	Open	Connects P002 (AN002) to Grove 2 pin 1
E37	Ethernet 0	Open	Connects P407 to P407_GPTP_PTPOUT3

Location	Circuit Group	Default Position	Function
E38	Ethernet 0	Closed	Connects P407 to P407_USB_VBUS
E63	Ethernet 0	Closed	Connects ETH_PHY_CLK0 to U8 pin 63 (XTAL1)
E64	Ethernet 0	Closed	Connects P710 to U8 pin 60 (LED0)
E65	Ethernet 0	Open	Connects P710 to U8 pin 52 (FASTLINK_FAIL)
E68	Ethernet 0	Closed	Connects U8 pin 61 (REFCLK_SEL_1) to R91
E70	Ethernet 0	Open	Connects U8 pin 62 (REFCLK_SEL_0) to R89
E19	Ethernet 1	Open	Connects U12 pin 62 (REFCLK_SEL_0) to R113
E21	Ethernet 1	Closed	Connects U12 pin 61 (REFCLK_SEL_1) to R110
E50	Ethernet 1	Closed	Connects P308 to P308_ENET1_TXER
E54	Ethernet 1	Open	Connects P106 to U12 pin 52 (FASTLINK_FAIL)
E61	Ethernet 1	Closed	Connects P106 to U12 pin 60 (LED0)
E66	Ethernet 1	Closed	Connects ETH_PHY_CLK1 to U12 pin 63 (XTAL1)
E84	Ethernet 1	Closed	Connects P304 to P304_ENET1_TXD3
E85	Ethernet 1	Closed	Connects P305 to P305_ENET1_TXD2
E86	Ethernet 1	Closed	Connects P306 to P306_ENET1_TXD1
E87	Ethernet 1	Closed	Connects P307 to P307_ENET1_TXD0
E18	CAN-FD 1	Closed	Connects P415 to U14 pin 1 (TXD)
E20	CAN-FD 1	Closed	Connects P414 to U14 pin 4 (RXD)
E80	CAN-FD 1	Closed	Connects CAN-FD 1_L to R165
E81	CAN-FD 1	Closed	Connects CAN-FD 1_H to R166
E34	CAN-FD 0	Closed	Connects P203 to U11 pin 1 (TXD)
E53	CAN-FD 0	Closed	Connects P202 to U11 pin 4 (RXD)
E96	CAN-FD 0	Closed	Connects CAN-FD 0_L to R30
E97	CAN-FD 0	Closed	Connects CAN-FD 0_H to R35
E59	Power	Open	Shorts 5V USB Debug diode D3 to eliminate the forward voltage drop
E60	Power	Open	Shorts 5V USB Full Speed diode D4 to eliminate the forward voltage drop
E62	Power	Open	Shorts 5V EXT diode D14 to eliminate the forward voltage drop
E98	Power	Closed	Connects the PMIC 1 V supply output to the 1 V rail
E99	Power	Closed	Connects the PMIC 3.3 V supply output to the 3.3 V rail
E100	Power	Closed	Connects the PMIC 2.5 V supply output to the 2.5 V rail
E82	RS485	Closed	Connects B/Z to R167
E83	RS485	Closed	Connects A/Y to R167

4.3.4 Hardware Configuration Switch SW4

The EK-RA8T2 features an I²C I/O Port Expander (PI4IOE5V6408) at U15 which has the I²C address 0x43. The port expander is connected to the configuration switches SW4 and allows the settings to be read (when the I/O expander port is set to input) or overridden (when the I/O expander port is set to output) by software.

The following table describes the function and default configuration for each switch that controls the operational peripheral pins on the EK-RA8T2 board.

Functional details for many of the listed switches may be found in sections associated with each functional area of the kit.

Table 3. Hardware Configuration Switch (SW4) Definitions

Switch	Switch Definition	Position (Default)	Function	Conflict
SW4-1	Pmod 1 Mode Select 1	OFF	Please see Table 19	-
		ON		
SW4-2	Pmod 1 Mode Select 2	OFF		
		ON		
SW4-3	CAN-FD 0	OFF	CAN 0 normal mode	-
		ON	CAN 0 standby mode	-
SW4-4	CAN-FD 1	OFF	CAN 1 normal mode	-
		ON	CAN 1 standby mode	-
SW4-5	No Function	OFF	-	-
		ON	-	-
SW4-6	Ethernet	OFF	Ethernet PHY COMA_MODE pin set low ^{*1}	-
		ON	Ethernet PHY COMA_MODE pin set high ^{*1}	-
SW4-7	USBFS Role Toggle	OFF	Toggles USBFS between Host and Device mode	-
		ON		
SW4-8	RS485 enable	OFF	RS485 enabled	Arduino and mikroBUS™
		ON	RS485 disabled	-

^{*1} Please refer to the VSC8541-02 data sheet for details

Note: There are no conflicting switch settings for SW4.

4.3.5 MCU Boot Mode and Debugger Configuration Switch SW6

SW6 configures the MCU Boot Mode and the J-Link on board debugger. The table below describes the function and default configuration of this switch block.

Table 4. MCU Boot Mode and Debugger Configuration Switch (SW6) Definitions

Switch	Switch Definition	Position (Default)	Function
SW6-1	RA8T2 MCU Boot mode configuration	OFF	P201/MD is pulled up (normal boot mode)
		ON	P201/MD is pulled down (USB boot mode)
SW6-2	Not used	OFF	
		ON	
SW6-3	RA8T2 MCU Boot mode debugger connection	OFF	P201/MD isolated from debugger JLOB_SWCLK
		ON	P201/MD connected to debugger JLOB_SWCLK
SW6-4	RA8T2 MCU Reset ^{*1}	OFF	RA8T2 MCU RESET_L isolated from GND
		ON	RA8T2 MCU RESET_L connected to GND
SW6-5	Debugger connect ^{*1 *2}	OFF	RA8T2 MCU RESET_L isolated from JLOB_RESET_L
		ON	RA8T2 MCU RESET_L connected to JLOB_RESET_L
SW6-6	RA4M2 debugger reset	OFF	RA4M2 debugger RES pin isolated from GND
		ON	RA4M2 debugger RES pin connected to GND
SW6-7	Debugger connect ^{*2}	OFF	P208 isolated from JTAG_TDI
		ON	P208 connected to JTAG_TDI
SW6-8	Debugger connect ^{*2}	OFF	P209 isolated from JTAG_TDO
		ON	P209 connected to JTAG_TDO
SW6-9	Debugger connect ^{*2}	OFF	P210 isolated from JTAG_TMS
		ON	P210 connected to JTAG_TMS
SW6-10	Debugger connect ^{*2}	OFF	P211 isolated from JTAG_TCK
		ON	P211 connected to JTAG_TCK

^{*1} SW6-4 and SW6-5 are complimentary so that if one is ON, then the other should be OFF.

^{*2} SW6-5 and SW6-7 through SW6-10 serve to isolate the debugger from the RA8T2 MCU and so will generally be all ON at the same time, or all OFF.

5. System Control and Ecosystem Access Area

The following figure shows the System Control and Ecosystem Access area on the EK-RA8T2 board. Subsequent sections detail the features and functionality provided in the area.

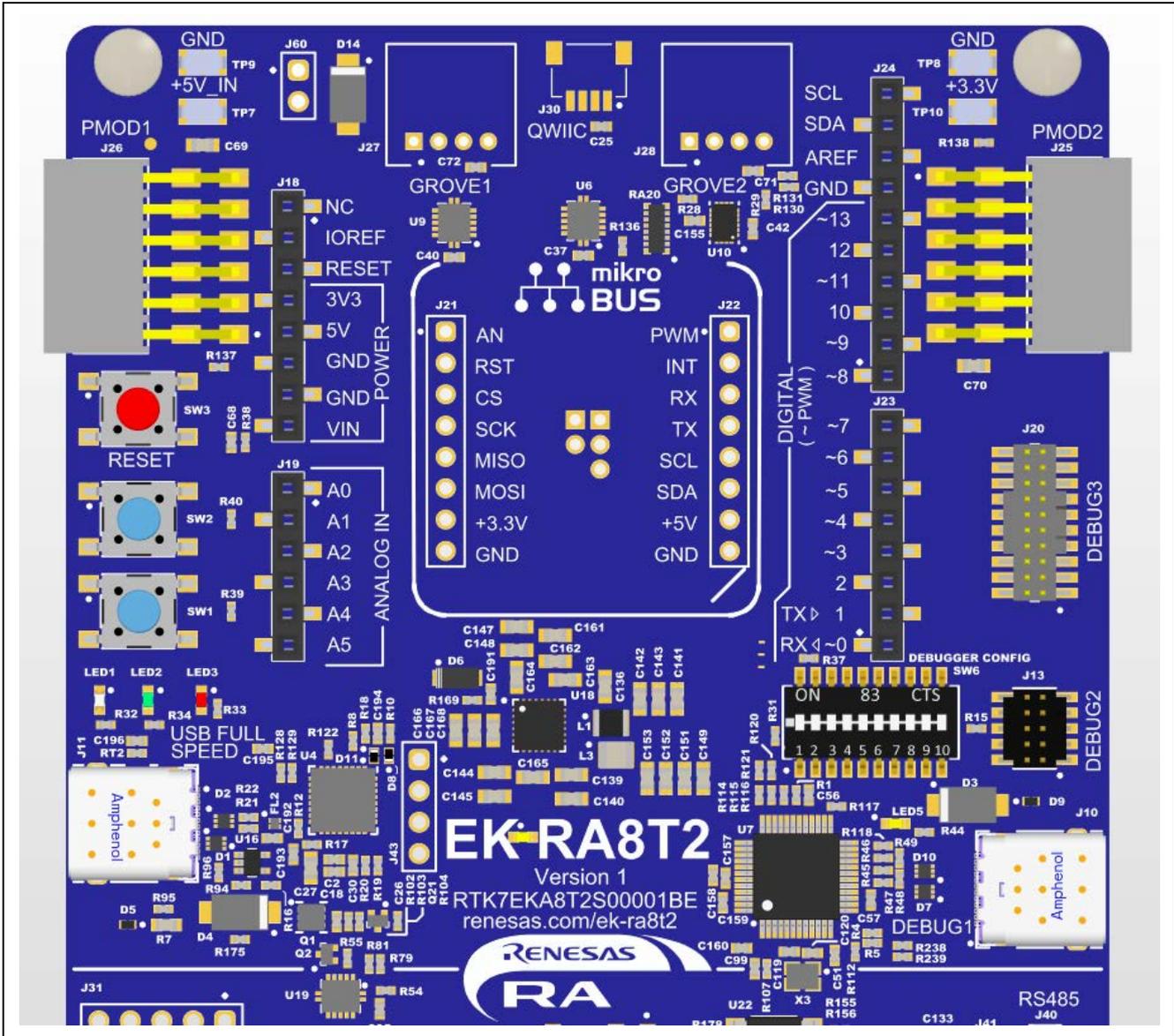


Figure 7. System Control and Ecosystem Access Area

5.1 Power

The EK-RA8T2 kit is designed for +5 V operation. An on-board Power Management IC (PMIC) DA9279 is used to convert the 5 V supply to a 3.3 V system supply as well as 1.0 V and 2.5 V for the Ethernet circuitry. The PMIC also provides 1.8 V and 1.2 V supplies that are not used on the board but are available for the user. The maximum current available from each output of the PMIC is shown on the table below.

Table 5. PMIC Outputs

Channel	Type	Output voltage	Maximum Current
1	BUCK	1.0 V	1.5 A
2	BUCK	3.3 V	3.0 A
3	LDO	1.2 V	300 mA
4	LDO	2.5 V	350 mA
5	LDO	1.8 V	150 mA

5.1.1 Power Supply Options

This section describes the different ways in which EK-RA8T2 kit can be powered.

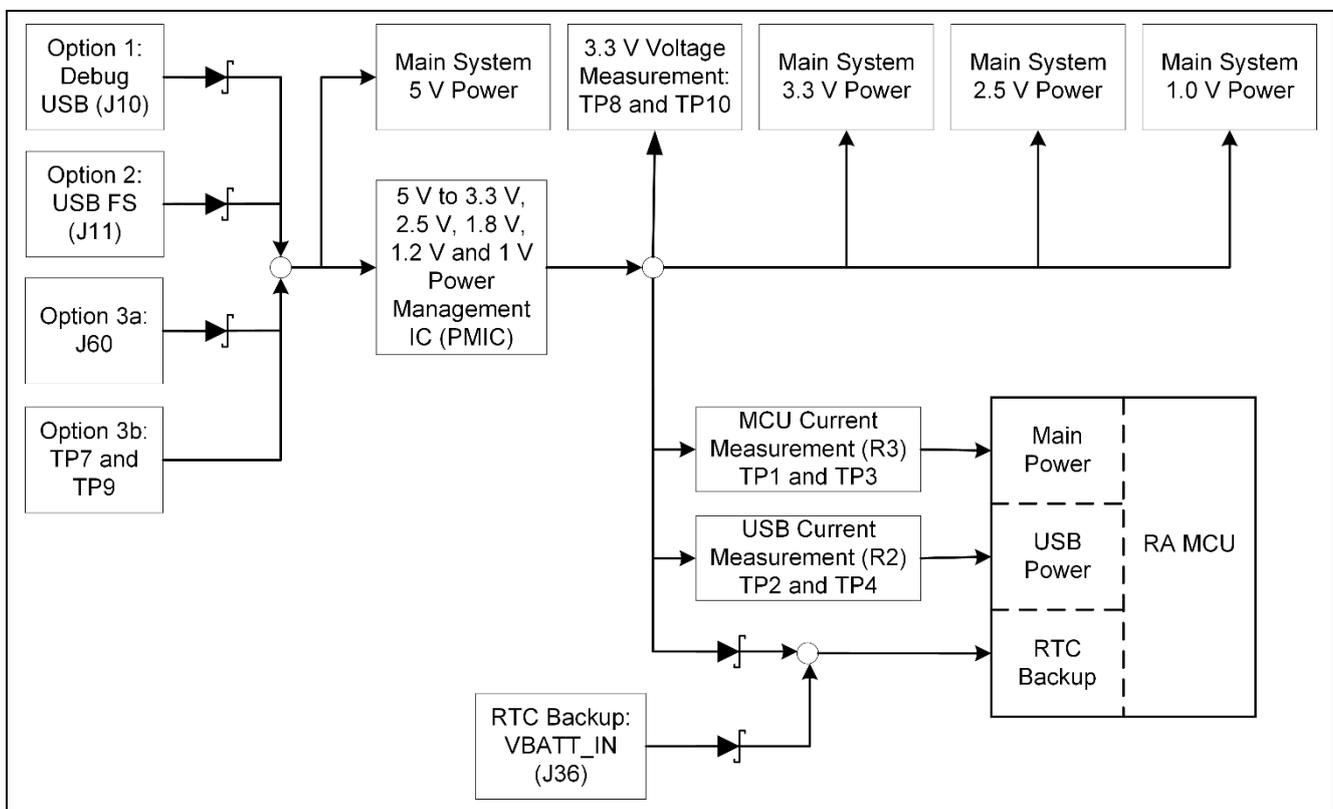


Figure 8. Power Supply Options

5.1.1.1 Option 1: Debug USB

5 V may be supplied from an external USB host to the USB Debug connector (J10) labelled DEBUG1 on the board. Power from this source is connected to the Main System 5 V Power. Reverse current protection is provided between this connector and the Main System 5 V Power by D3. Link E59 can be shorted to eliminate the voltage drop across D3, at the expense of removing the reverse polarity protection from this input.

5.1.1.2 Option 2: USB Full Speed

5 V may be supplied from an external USB host to the USB Full Speed connector (J11) labelled USB FULL SPEED on the board. Power from this source is connected to the Main System 5 V Power. Reverse current

protection is provided between this connector and the main System 5 V Power by D4. Link E60 can be shorted to eliminate the voltage drop across D4, at the expense of removing the reverse polarity protection from this input.

5.1.1.3 Option 3: 5 V Test Points

5 V may be supplied from an external power supply to test points on the board. TP7 (5 V) and TP9 (GND) are loop-style test points, and J60 provides large via style test points that can accommodate a 0.1" pin header or connector. Reverse current protection is provided at J60-1 by D14 whereas TP7 directly connects to the 5V input pin of the voltage regulator U8 and to the Main System 5V Power. Care must be taken before applying an external supply to this test point to ensure that the polarity is correct. Failure to do so could result in damage to components on the PCB. Link E62 can be shorted to eliminate the voltage drop across D14, at the expense of removing the reverse polarity protection from this input.

These test points can be found at the top left of the board above Pmod1.

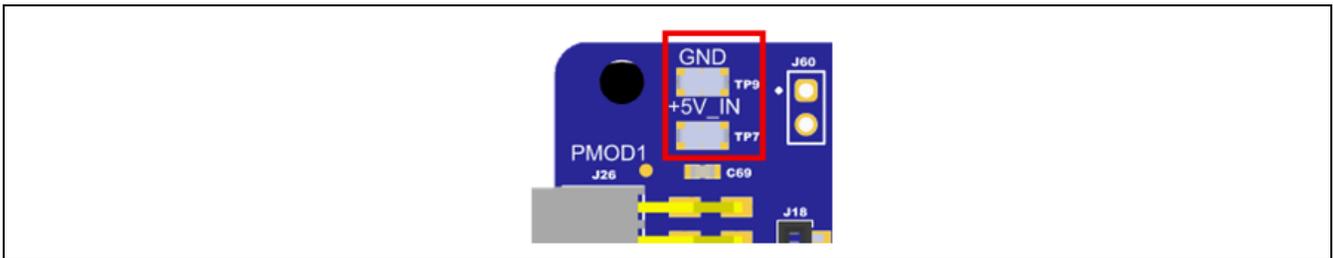


Figure 9. +5V Test Point Location

5.1.1.4 RTC Backup: VBATT Supply

The MCU provides a battery backup function that maintains power to certain MCU peripherals in the event of a power loss (for example the Real Time Clock). A battery (lithium coin cell, etc.) can be connected to J36 (not populated) to provide this power. Reverse current protection is provided at J36-2 by D15. For further details see the MCU hardware manual.

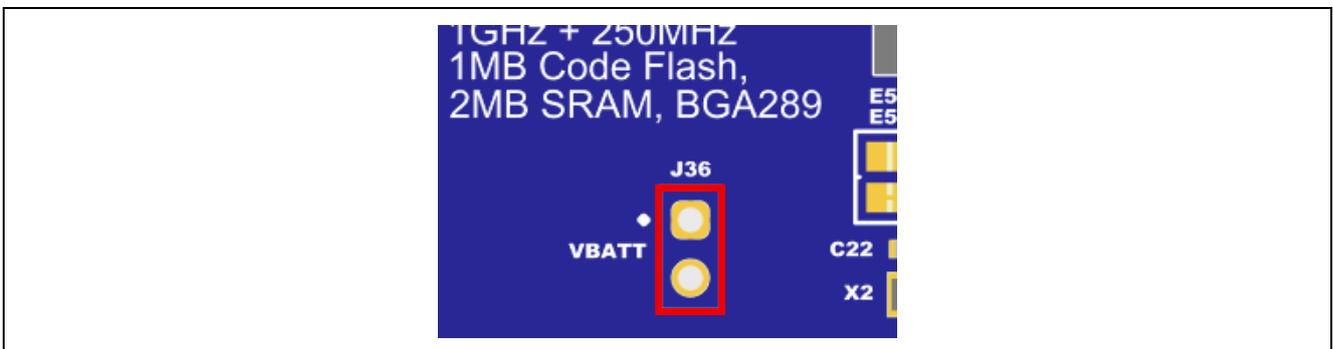


Figure 10. VBATT supply (J36) location

5.1.2 Power Supply Considerations

The RA MCU is powered by the DA9279 Power Management IC (PMIC), which operates with a 5 V input and uses two buck regulators and three LDOs to supply voltages of 1 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V required by components on the evaluation kit.

The PMIC manages supply sequencing and timing for power-up and power-down. It has a PGOOD output that indicates when all regulators are stable. On the EK-RA8T2 board, the open-drain output creates the system reset signal (RESET_L). This supply can be used externally. Maximum output currents for these supplies are specified in Table 5.

It is important that the total current drawn by the RA MCU, active on-board features, and any connected peripherals do not exceed these limits. The available current also depends on the host USB port's configuration; for instance, a standard USB-A port may provide up to 500 mA.

The DA9279 PMIC supports features including adjustable buck regulator output voltages, which can be configured via the I²C interface (I²C0 Address: 0x6B).

5.1.3 Power-up Behavior

When powered, the white LED near the center of the board (the “dash” in the EK-RA8T2 name) will light up. For more details on initial power up behavior, see the *EK-RA8T2 Quick Start Guide*.

5.1.4 PMIC Diagnostic Connector

The Power Management IC (PMIC) implements a number of status and control registers that are exposed via its I²C interface. These registers can be accessed from the RA MCU and by DA9279 GUI software running on a suitable external device. J43 (not populated) has been provided to connect to the external software. To avoid conflicts when using the external tool, remove R172 and R173, which disconnect the rest of the board.

5.2 Debug and Trace

The EK-RA8T2 board supports the following three debug modes.

Table 6. Debug Modes

Debug Modes	Debugger MCU (the device that connects to the IDE on PC)	Target MCU (the device that is being debugged)	Debugging Interface/Protocol	Connector Used
Debug on-board	RA4M2 (on-board)	RA8T2 (on-board)	SWD, JTAG	USB-C (J10)
Debug in	External debugging tools	RA8T2 (on-board)	SWD, SWO, ETM, JTAG	20-pin connector (J20) or 10-pin connector (J13)
Debug out	RA4M2 (on-board)	Any external RA MCU	SWD, SWO, JTAG	USB-C (J10) plus either 20-pin connector (J20) or 10-pin connector (J13)

Notes:

- See Table 8 for the Debug USB connector pin definition.
- See Table 11 for the 20-pin JTAG connector pin definition.
- See Table 12 for the 10-pin JTAG connector pin definition.

The following table details the switch configuration for each of the debug modes.

Table 7. Switch 6 Configuration Summary for Different Debug Modes

Debug Modes	SW6-3	SW6-4	SW6-5	SW6-6	SW6-7 through to SW6-10
Debug on-board	Off	Off	On	Off	All on
Debug in	Off	Off	On	On	All on
Debug out	Off	On	Off	Off	All off

5.2.1 Debug On-Board

The on-board debug functionality is provided using Renesas RA4M2 Debug MCU and SEGGER J-Link[®] firmware. Debug USB-C connector (J10) connects the RA4M2 Debug MCU to an external USB Full Speed Host, allowing reprogramming and debugging of the target RA MCU firmware. This connection is the default debug mode for the EK-RA8T2 board.

The RA4M2 Debug MCU connects to the target RA MCU using the SWD and JTAG interface.

Table 8. Debug USB Port Assignments

Debug USB Port Assignments		EK-RA8T2
Pin	Description	Signal/Bus
J10-A1	GND	GND
J10-A2	TX1+	NC
J10-A3	TX1-	NC
J10-A4	VBUS	+5V_USB_DBG
J10-A5	CC1	USB_JLOB_CC1
J10-A6	DA+	USB_JLOB_P

Debug USB Port Assignments		EK-RA8T2
Pin	Description	Signal/Bus
J10-A7	DA-	USB_JLOB_N
J10-A8	SBU1	NC
J10-A9	VBUS	+5V_USB_DBG
J10-A10	RX2-	NC
J10-A11	RX2+	NC
J10-A12	GND	GND
J10-B1	GND	GND
J10-B2	TX2+	NC
J10-B3	TX2-	NC
J10-B4	VBUS	+5V_USB_DBG
J10-B5	CC2	USB_JLOB_CC2
J10-B6	DB+	USB_JLOB_P
J10-B7	DB-	USB_JLOB_N
J10-B8	SBU2	NC
J10-B9	VBUS	+5V_USB_DBG
J10-B10	RX1-	NC
J10-B11	RX1+	NC
J10-B12	GND	GND
J10-S1	SHIELD	GND
J10-S2	SHIELD	GND
J10-S3	SHIELD	GND
J10-S4	SHIELD	GND

A yellow indicator, LED5, shows the visual status of the debug interface. When the EK-RA8T2 board is powered on, and LED5 is blinking, it indicates that the RA4M2 Debug MCU is not connected to a programming host. When LED5 is on solid, it indicates that the RA4M2 Debug MCU is connected to a programming interface.

To configure the EK-RA8T2 board to use the Debug On-Board mode, configure SW6 using the following table.

Table 9. Debug On-Board Switch Configuration

Switch	Setting	Function
SW6-3	Off	RA8T2 MCU P201/MD not connected to JTAG TCK
SW6-4	Off	RA8T2 MCU RESET_L not connected to GND
SW6-5	On	Target RA8T2 MCU RESET_L connected to debugger JLOB_RESET_L
SW6-6	Off	RA4M2 debugger reset not connected to GND
SW6-7 to SW6-10	All on	Target RA8T2 MCU debug signals connected to the debugger interface

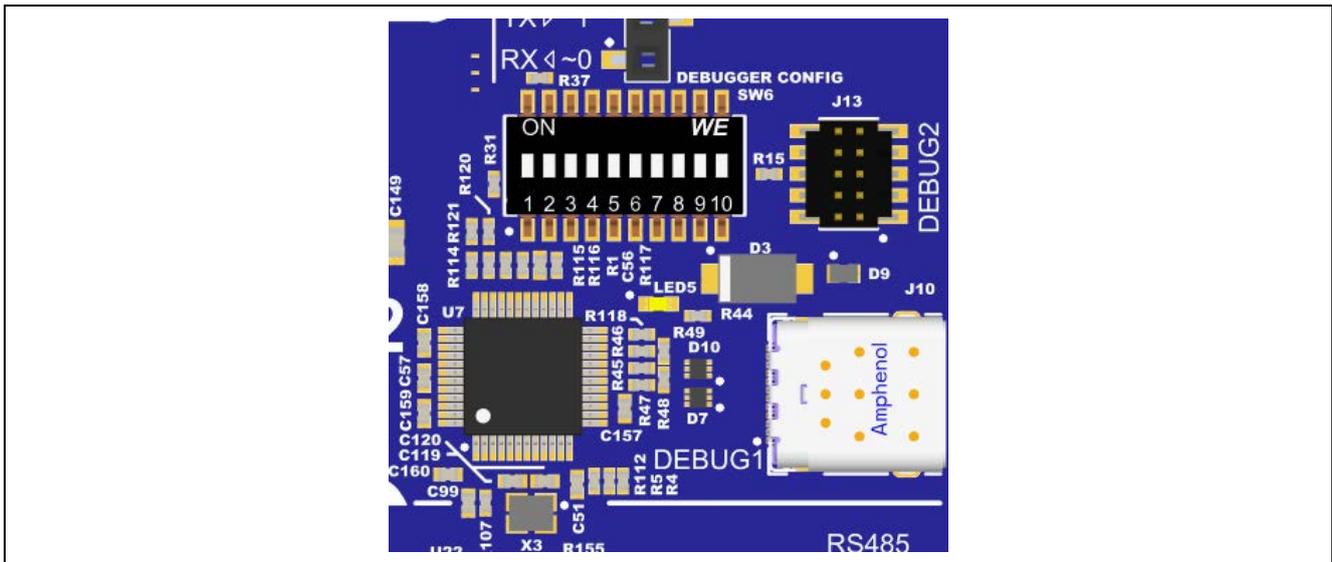


Figure 11. EK-RA8T2 Debug Interface

5.2.2 Debug In

One 20-pin Cortex® Debug Connector at J20 supports JTAG, SWD, SWO and ETM (TRACE) debug. One 10-pin Cortex® Debug Connector at J13 supports JTAG, SWD and SWO. Either of these connectors may be used for external debug of the target RA MCU.

To configure the EK-RA8T2 board to use the Debug In mode, configure SW6 using the following table.

Table 10. Debug In Mode Switch Configuration

Switch	Setting	Function
SW6-3	Off	RA8T2 MCU P201/MD not connected to JTAG TCK
SW6-4	Off	RA8T2 MCU RESET_L not connected to GND
SW6-5	On	Target RA8T2 MCU RESET_L connected to debug connector JTAG_RESET_L
SW6-6	On	RA4M2 debugger reset connected to GND (RA4M2 held in reset)
SW6-7 to SW6-10	All on	Target RA8T2 MCU debug signals connected to the debugger interface

Table 11. JTAG/SWO/SWD/ETM Port Assignments

JTAG Port Assignments				EK-RA8T2
Pin	JTAG Pin Name	SWD Pin Name	ETM Pin Name	Signal/Bus
J20-1	Vtref	Vtref	Vtref	+3V3
J20-2	TMS	SWDIO	TMS/SWDIO	P210/SWDIO/TMS
J20-3	GND	GND	GND	GND
J20-4	TCK	SWCLK	TCK/SWCLK	P211/SWCLK/TCK
J20-5	GND	GND	GND	GND
J20-6	TDO	SWO/EXTa	TDO/SWO	P209/SWO/TDO
J20-7	Key	Key	Key	NC
J20-8	TDI	NC/EXTb	TDI	P208/TDI
J20-9	GNDDetect	GNDDetect	GNDDetect	GND (cut E30 to open)
J20-10	nSRST	nSRST	nSRST	RESET_L
J20-11	GND	GND	GND	GND
J20-12	N/A	N/A	TCLK	P308/TCLK*
J20-13	GND	GND	GND	GND
J20-14	N/A	N/A	TDATA0	P307/TDATA0*
J20-15	GND	GND	GND	GND
J20-16	N/A	N/A	TDATA1	P306/TDATA1*

JTAG Port Assignments				EK-RA8T2
Pin	JTAG Pin Name	SWD Pin Name	ETM Pin Name	Signal/Bus
J20-17	GND	GND	GND	GND
J20-18	N/A	N/A	TDATA2	P305/TDATA2*
J20-19	GND	GND	GND	GND
J20-20	N/A	N/A	TDATA3	P304/TDATA3*

* Please connect E44, E45, E46, E47 and E48 before use

Table 12. JTAG/SWD/SWO Port Assignments

JTAG/SWD/SWO Port Assignments			EK-RA8T2
Pin	JTAG Pin Name	SWD Pin Name	Signal/Bus
J13-1	Vtref	Vtref	+3V3
J13-2	TMS	SWDIO	P210/SWDIO/TMS
J13-3	GND	GND	GND
J13-4	TCK	SWCLK	P211/SWCLK/TCK
J13-5	GND	GND	GND
J13-6	TDO	SWO/EXTa	P209/SWO/TDO
J13-7	Key	Key	NC
J13-8	TDI	NC/EXTb	P208/TDI
J13-9	GNDDetect	GNDDetect	GND (cut E30 to open)
J13-10	nSRST	nSRST	RESET_L

Note: The Cortex® Debug Connector is fully described in the Arm® CoreSight™ Architecture Specification.

5.2.3 Debug Out

The EK-RA8T2 board can be configured to use the RA4M2 Debug MCU to debug target RA MCU on an external board.

A yellow indicator, LED5, shows the visual status of the debug interface. When the EK-RA8T2 board is powered on, and LED5 is blinking, this indicates that the RA4M2 Debug MCU is not connected to a programming host. When LED5 is solid on, this indicates that the RA4M2 Debug MCU is connected to a programming interface. When the debug interface is actively in use, the LED will flicker randomly.

To configure the EK-RA8T2 board to use the Debug Out mode, configure SW6 according to the following table.

Table 13. Debug Out Switch Configuration

Switch	Setting	Function
SW6-3	Off	RA8T2 MCU P201/MD isolated from JTAG TCK
SW6-4	On	RA8T2 MCU RESET_L connected to GND
SW6-5	Off	RA8T2 MCU RESET_L isolated from debugger JTAG_RESET_L
SW6-6	Off	RA4M2 debugger reset not connected to GND
SW6-7 to SW6-10	All off	RA8T2 MCU debug signals isolated from the debugger interface

5.2.4 Debug Serial

The debug port can act as a virtual COM port that supports serial communication. See Table 14 below.

Table 14. Debug Serial Port Assignment

RA8T2 Port Assignment	Debugger U7 Serial Port Assignment
P805 (TXD8)	P301 (RXD2)
P806 (RXD8)	P302 (TXD2)
P512 (CTS8) ^{*1}	P408 (RTS)
P511 (RTS8) ^{*2}	P409 (CTS)

^{*1} Connected by soldering link E9

^{*2} Connected by soldering link E17

5.3 Ecosystem

The System Control and Ecosystem area provides users with the option to simultaneously connect several third-party add-on modules compatible with the five most popular ecosystems using the following connectors:

1. Two Seeed Grove® system (I²C/I3C/Analog) connectors (not populated)
2. SparkFun Qwiic® connector (not populated)
3. Two Digilent Pmod™ (SPI, UART and I²C) connectors
4. Arduino™ (Uno R3) connector
5. MikroElektronika mikroBUS™ connector (not populated)

5.3.1 Seeed Grove® Connections

5.3.1.1 Grove 1

A Seeed Grove® I3C connector (not populated) is provided at J27. The RA MCU acts as a two-wire serial master in I3C mode or I²C mode, and a connected module acts as a two-wire serial slave.

Table 15. Grove 1 Port Assignments

Grove 1 Connector		EK-RA8T2
Pin	Description	Signal/Bus
J27-1	I3C_SCL ^{*1}	P400/I3C_SCL0
J27-2	I3C_SDA ^{*1}	P401/I3C_SDA0
J27-3	VCC	+3.3 V
J27-4	GND	GND

^{*1} Pullup resistors need to be enabled in software to use I²C (see section 5.4.2).

5.3.1.2 Grove 2

A Seeed Grove® I²C connector (not populated) is provided at J28. The RA MCU acts as a two-wire serial master, and a connected module acts as a two-wire serial slave.

Option links E39, E40, E41 and E42 provide the capability to convert this connector to an analog Seeed Grove® implementation.

Table 16. Grove 2 Port Assignments

Grove 2 Connector		EK-RA8T2	
Pin	Description	Signal/Bus	
J28-1	SCL	P410/SCL0 ^{*1}	P002 (AN002) ^{*2}
J28-2	SDA	P409/SDA0 ^{*1}	P005 (AN005) ^{*2}
J28-3	VCC	+3.3 V	
J28-4	GND	GND	

^{*1} Jumpers E39 and E40 are closed, E41 and E42 are open.

^{*2} Jumpers E39 and E40 are open, E41 and E42 are closed.

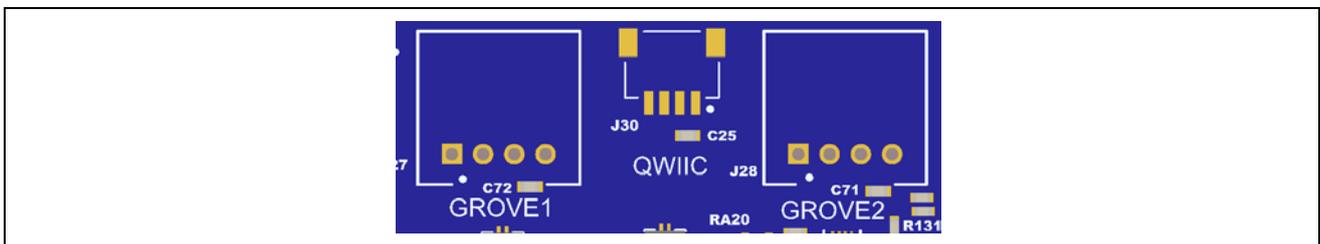


Figure 12. Seed Grove® and SparkFun Qwiic® Connector Footprints

5.3.2 SparkFun Qwiic® Connections

A SparkFun Qwiic® connector (not populated) is provided at J30. The Main MCU acts as a two-wire serial master, and a connected module acts as a two-wire serial slave (data lines shared with Grove 1).

Table 17. Qwiic® Port Assignments

Qwiic® Connector		EK-RA8T2
Pin	Description	Signal/Bus
J30-1	GND	GND
J30-2	VCC	+3.3 V
J30-3	I3C_SDA ^{*1}	P401/I3C_SDA0
J30-4	I3C_SCL ^{*1}	P400/I3C_SCL0

^{*1} Pullup resistors need to be enabled in software to use I²C (see section 5.4.2).

5.3.3 Digilent Pmod™ Connectors

Two 12-pin connectors are provided to support Pmod modules where the RA MCU acts as the master, and the connected module acts as a slave device.

These interfaces may be configured in firmware to support several Pmod types such as Type-2A (expanded SPI) and Type-3A (expanded UART).

The EK-RA8T2 board also provides quick switches so the 12-pin connector may alternatively be used for Pmod Type-6A (I²C).

The default 12-pin Pmod interface supports +3.3 V devices. Please ensure that any Pmod device installed is compatible with a +3.3 V supply.

Note: Both Pmods use the SCI peripheral in “Simple SPI” mode and so do not offer the full functionality of the SPI peripheral. Please see the hardware manual for full details of the SCI “Simple SPI” mode.

5.3.3.1 Pmod 1

A 12-pin Pmod connector is provided at J26, Pmod 1.

This Pmod connector is controlled by switch options SW4-1 and SW4-2. These pins are set low by default with SW4-1 and SW4-2 OFF therefore, Pmod 1 is in SPI mode.

Table 18. Pmod 1 Port Assignments

Pmod 1 Connector				EK-RA8T2	Pmod 1 Configuration	
Pin	Option Type-2A (SPI) ^{*1}	Option Type-3A (UART) ^{*1}	Option Type-6A (I ² C) ^{*1}	Signal/Bus	Short	Open
J26-1	SS		IRQ	P804 (SS2/IRQ14)		
		CTS	IRQ	P800 (CTS2/IRQ11)		
J26-2	MOSI	TXD	RST	P801 (MOSI2/TXD2/RST)		
J26-3	MISO	RXD		P802 (MISO2/RXD2)		
			SCL	P410 (SCL0)		
J26-4	SCK			P803 (SCK2)		
		RTS		P804 (RTS2)		
		SDA		P409 (SDA0)		
J26-5	GND			GND		
J26-6	VCC ^{*2}			+3.3 V	E25	E35
				+5.0 V	E35	E25
J26-7	IRQ			P006 (IRQ11-DS)		
J26-8	RESET (master to slave)			P713		
J26-9	GPIO			P010		
J26-10	GPIO			P712		
J26-11	GND			GND		
J26-12	VCC ^{*2}			+3.3 V	E25	E35
				+5.0 V	E35	E25

^{*1} Option is selected by setting switches SW4-1 and SW4-2 (see Table 19)

² Caution: 5 V optional supply is provided (J26-6 and J26-12), however the interface must only be driven with 3 V signals from the Pmod 1. The EK-RA8T2 will only provide 3.3 V signal levels to the Pmod 1.

Table 19. Pmod 1 Switch Configuration

SW4-1	SW4-2	Selected function	Conflicts
Off	Off	SPI	-
On	Off	UART	-
Off	On	I ² C	-
On	On	None (invalid)	-

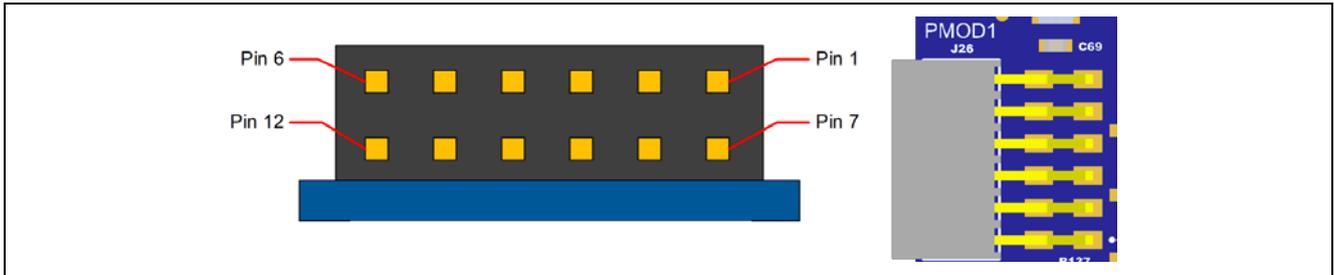


Figure 13. Pmod 1 Connector

5.3.3.2 Pmod 2

A 12-pin Pmod connector is provided at J25, Pmod 2.

Table 20. Pmod 2 Port Assignments

Pmod 2 Connector			EK-RA8T2	Pmod 2 Configuration	
Pin	Option Type-2A (SPI)	Option Type-3A (UART)	Signal/Bus	Short	Open
J25-1	SS		PC11 (SS6)	E15	E10
J25-1		CTS	PC15 (CTS6)	E10	E15
J25-2	MOSI	TXD	PC14 (MOSI6/TXD6)		
J25-3	MISO	RXD	PC13 (MISO6/RXD6)		
J25-4	SCK		PC12 (SCK6)	E16	E14
J25-4		RTS	PC11 (RTS6)	E14	E16
J25-5	GND		GND		
J25-6	VCC		+3.3 V		
J25-7	IRQ		P012 (IRQ15)		
J25-8	RESET (master to slave)		P807		
J25-9	GPIO		P111		
J25-10	GPIO		P914		
J25-11	GND		GND		
J25-12	VCC		+3.3 V		

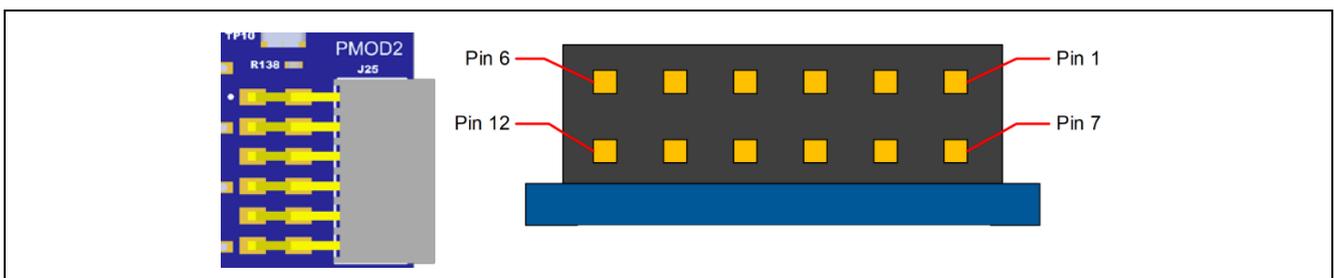


Figure 14. Pmod 2 Connector

5.3.4 Arduino™ Connector

Near the center of the System Control and Ecosystem Access area is an Arduino™ Uno R3 compatible connector interface. The Arduino connector cannot be used in conjunction with CAN-FD 0 and RS485.

Table 21. Arduino Uno Port Assignments

Arduino Compatible Connectors				EK-RA8T2
Pin	Description			Signal/Bus
J18-1	NC			NC
J18-2	IOREF			+3.3 V
J18-3	RESET			RESET_L
J18-4	3.3 V			+3.3 V
J18-5	5 V			+5 V
J18-6	GND			GND
J18-7	GND			GND
J18-8	VIN			NC
J19-1	A0			P001 (AN001)
J19-2	A1			P007 (AN007)
J19-3	A2			P003 (AN003)
J19-4	A3			P004 (AN004)
J19-5	A4			P014 (AN014/DA0)
J19-6	A5			P015 (AN015/DA1)
J23-1	D0	RXD	PWM	P808 (RXD7/GTIOC13B) ^{*1}
J23-2	D1	TXD		P809 (TXD7) ^{*1}
J23-3	D2	INT0		P011 (IRQ16)
J23-4	D3	INT1	PWM	P811 (IRQ22/GTIOC10B)
J23-5	D4		PWM	P810 (IRQ21/GTIOC10A) ^{*1}
J23-6	D5		PWM	P601 (IRQ29/GTIOC6A)
J23-7	D6		PWM	P600 (IRQ30/GTIOC6B)
J23-8	D7		PWM	P502 (IRQ26/GTIOC12B)
J24-1	D8		PWM	P903 (IRQ1/GTIOC11A)
J24-2	D9		PWM	P110 (IRQ20/GTIOC9B)
J24-3	D10	SPI_SS		P204 (IRQ26/SSLA)
J24-4	D11	SPI_MOSI	PWM	P202 (MOSIA/GTIOC5B) ^{*2}
J24-5	D12	SPI_MISO		P313 (IRQ27/MISOA)
J24-6	D13	SPI_SCK	PWM	P203 (IRQ2-DS/RSPCKA/GTIOC5A) ^{*2}
J24-7	GND			GND
J24-8	AREF			ARDUINO_AREF (VREFH)
J24-9	I3C_SDA			P401/I3C_SDA0 ^{*3}
J24-10	I3C_SCL			P400/I3C_SCL0 ^{*3}

^{*1} Shared with RS485, turn on SW4-8 to use for Arduino

^{*2} Shared with CAN-FD0, cut E34 and E53 to use for Arduino

^{*3} Pullup resistors need to be enabled in software to use I²C (see section 5.4.2).

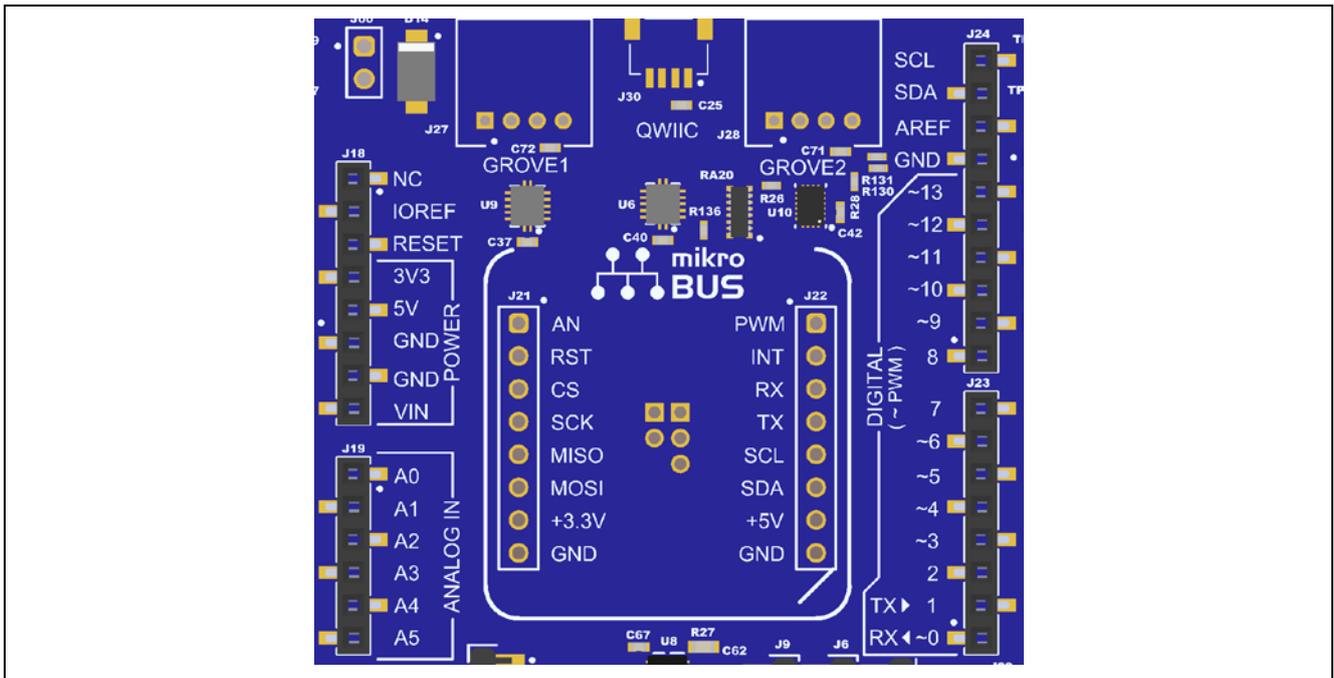


Figure 15. Arduino Uno Connectors

5.3.5 MikroElektronika mikroBUS™ Connector

In the center of the System Control and Ecosystem Access area is a mikroBUS™ compatible connector interface. The mikroBUS™ connector cannot be used in conjunction with CAN-FD 0, RS485 or Arduino. This interface is compliant with mikroBUS™ Standard Specifications revision 2.00. Please note that the mikroBUS™ connectors, J21 and J22, are not populated.

Table 22. mikroBUS™ Port Assignments

mikroBUS™ Port Connectors		EK-RA8T2
Pin	Description	Signal/Bus
J21-1	AN (Analog)	P004 (AN004)
J21-2	RST (Reset)	P402 (MIKROBUS™ RESET L)
J21-3	CS (SPI Chip Select)	P204 (SSLA0)
J21-4	SCK (SPI Clock)	P203 (RSPCKA)
J21-5	MISO	P313 (MISOA)
J21-6	MOSI	P202 (MOSIA)
J21-7	+3.3 V	+3.3 V
J21-8	GND	GND
J22-1	PWM	P810 (GTIOC10A)
J22-2	INT (Hardware Interrupt)	P903 (IRQ1)
J22-3	RX (UART Receive)	P808 (RXD7)
J22-4	TX (UART Transmit)	P809 (TXD7)
J22-5	I3C_SCL ^{*1}	P400/I3C_SCL0
J22-6	I3C_SDA ^{*1}	P401/I3C_SDA0
J22-7	+5 V	+5 V
J22-8	GND	GND

^{*1} Pullup resistors need to be enabled in software to use I²C (see section 5.4.2).

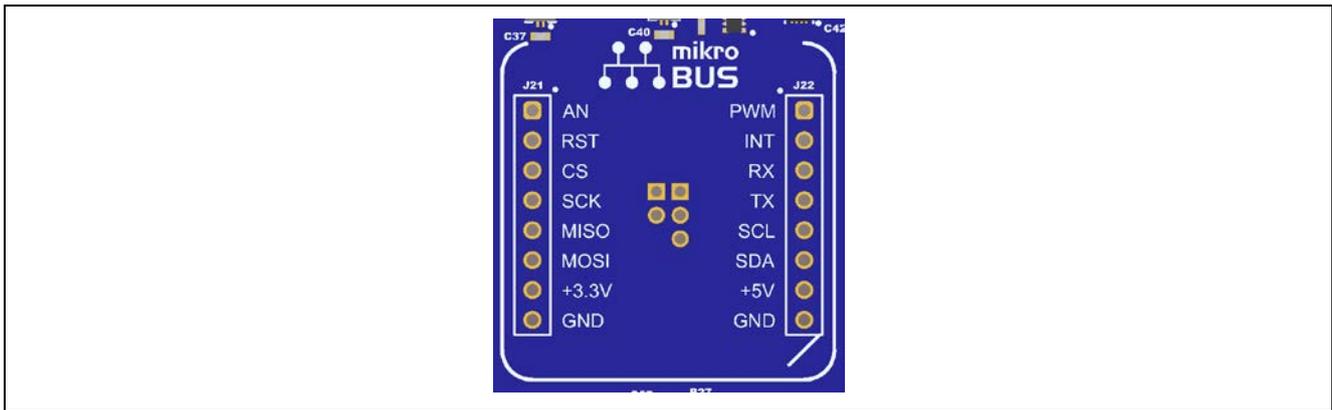


Figure 16. mikroBUS™ Connector

5.4 Connectivity

5.4.1 USB Full Speed

The USB-C connection jack (J11) connects the RA MCU USB Full Speed interface to an external USB interface, allowing communications for testing and use of the RA MCU firmware. This connection can be configured as either a USB device or a USB host interface.

For a USB Device configuration, set P500 to low and configure the RA MCU firmware to use the USB Full Speed ports in device mode. Power from an external USB Host on this connection can be used to provide power to the EK-RA8T2 board.

For a USB Host configuration, set P500 to high and configure the RA MCU firmware to use the USB Full Speed ports in host mode. In this configuration, power to J11 is supplied from U4. The total current available is 2 A. Note that the input power sources must be configured with enough power for both the EK-RA8T2 board and the USB Full Speed port in host mode. Connect a USB type-A female to USB-C male cable to J11. USB device cables or devices can be connected to the USB Full Speed port using this cable.

Table 23. USB Full Speed Port Assignments

USB Full Speed Connector		EK-RA8T2
Pin	Description	Signal/Bus
J11-A1	GND	GND
J11-A2	TX1+	NC
J11-A3	TX1-	NC
J11-A4	VBUS	USBFS_cVBUS_CON
J11-A5	CC1	USB_FS_CC1
J11-A6	DA+	USBF_P
J11-A7	DA-	USBF_N
J11-A8	SBU1	NC
J11-A9	VBUS	USBFS_cVBUS_CON
J11-A10	RX2-	NC
J11-A11	RX2+	NC
J11-A12	GND	GND
J11-B1	GND	GND
J11-B2	TX2+	NC
J11-B3	TX2-	NC
J11-B4	VBUS	USBFS_cVBUS_CON
J11-B5	CC2	USB_FS_CC2
J11-B6	DB+	USBF_P
J11-B7	DB-	USBF_N
J11-B8	SBU2	NC
J11-B9	VBUS	USBFS_cVBUS_CON
J11-B10	RX1-	NC
J11-B11	RX1+	NC

USB Full Speed Connector		EK-RA8T2
Pin	Description	Signal/Bus
J11-B12	GND	GND
J11-S1	SHIELD	GND
J11-S2	SHIELD	GND
J11-S3	SHIELD	GND
J11-S4	SHIELD	GND

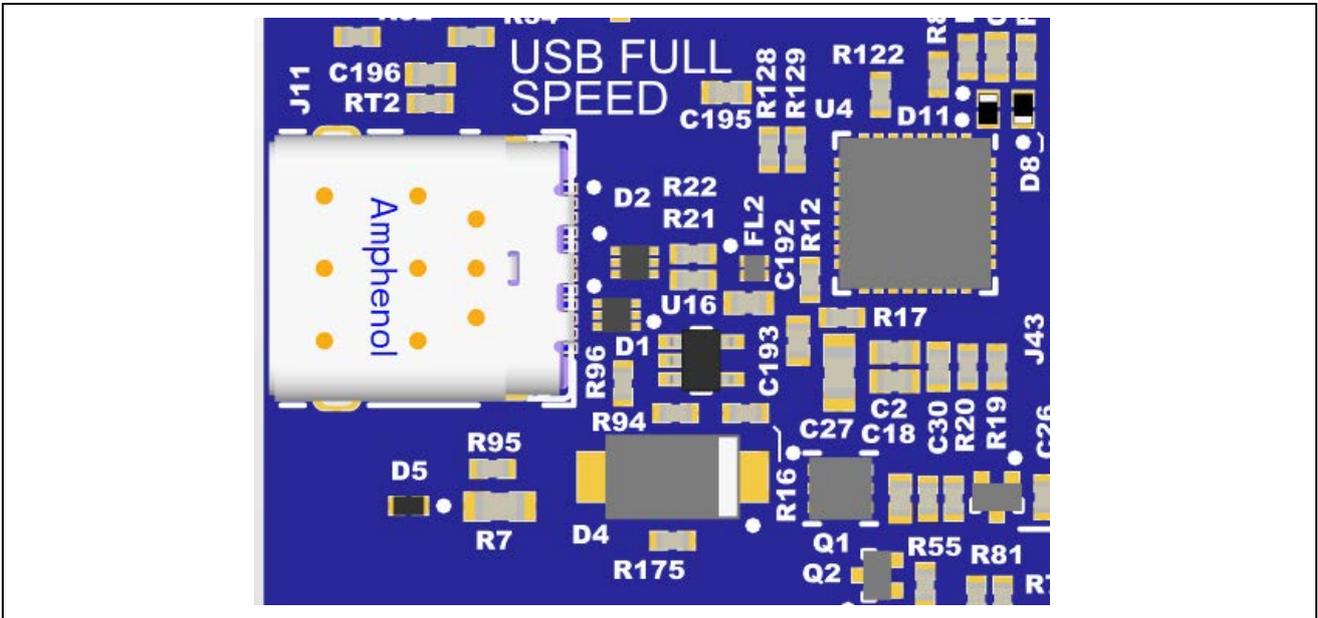


Figure 17. USB Full Speed Connector

5.4.2 I3C

The I3C port connects the Arduino, mikroBUS™, Grove 1, and Qwiic® connectors to the RA MCU I3C interface via P400 and P401. When P108 and P109 are set high, the RA MCU I3C peripheral can be used in I²C mode.

All configurations are shown in Table 24.

Table 24. I²C/I3C Pullup Configuration

I3C	I ² C	P108 & P109	Usable connectors
P400 (SCL0) & P401 (SDA0)	N/A	Inputs (high impedance) or outputs (driven high) ^{*1}	Arduino, mikroBUS™, Grove 1, and Qwiic®
N/A	P400 (SCL0) & P401 (SDA0)	Push-pull outputs driven high	

^{*1}Please refer to the I3C specification for management and control of the I3C pull-ups

5.5 Miscellaneous

5.5.1 User and Status LEDs

Seventeen LEDs are provided on the EK-RA8T2 board.

Behavior of the LEDs on the EK-RA8T2 board is described in the following table.

Table 25. EK-RA8T2 Board LED Functions

Designator	Color	Function	MCU Control Port
LED1	Blue	User LED	P714
LED2	Green	User LED	P303
LED3	Red	User LED	PA07
LED4	White	Power on indicator	+3.3 V

Designator	Color	Function	MCU Control Port
LED5	Yellow	Debug LED	J-Link OB MCU
LED6	Green	Ethernet PHY LED	Ethernet 1 PHY IC LED0
LED7	Yellow	Ethernet PHY LED	Ethernet 0 PHY IC LED1
LED8	Green	Ethernet PHY LED	Ethernet 0 PHY IC LED0
LED9	Yellow	Ethernet PHY LED	Ethernet 1 PHY IC LED1
LED10	Green	EtherCAT LED (CATLEDRUN)	PB08
LED11	Green	Network LED0	P615
LED12	Red	Network LED1	PC08
LED13	Red	EtherCAT LED (CATLEDERR)	PB11
LED14	Green	EtherCAT LED (CATLINKACT1)	PB13
LED15	Green	Network LED2	PC09
LED16	Green	EtherCAT LED (CATLINKACT0)	PB12
LED17	Red	Network LED3	PC10

The user LEDs may be isolated from the main MCU, so the associated ports can be used for other purposes. To separate LED1 from P714, trace cut jumper E27 must be open. To separate LED2 from P303, trace cut jumper E26 must be open. To separate LED3 from PA07, trace cut jumper E28 must be open.

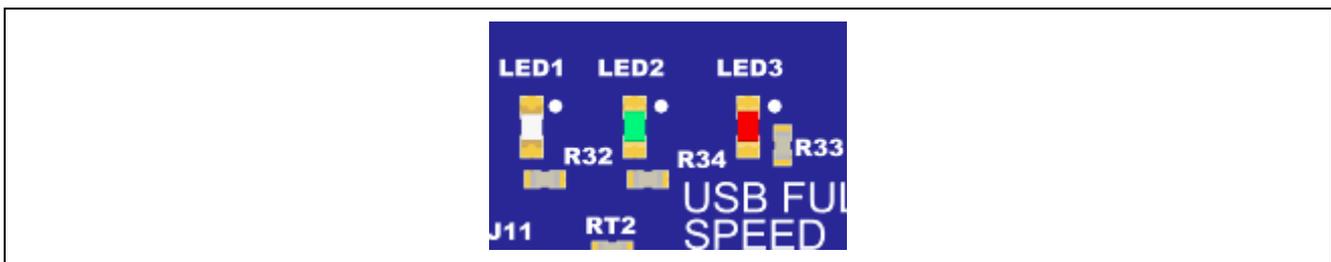


Figure 18. User LEDs



Figure 19. Power LED

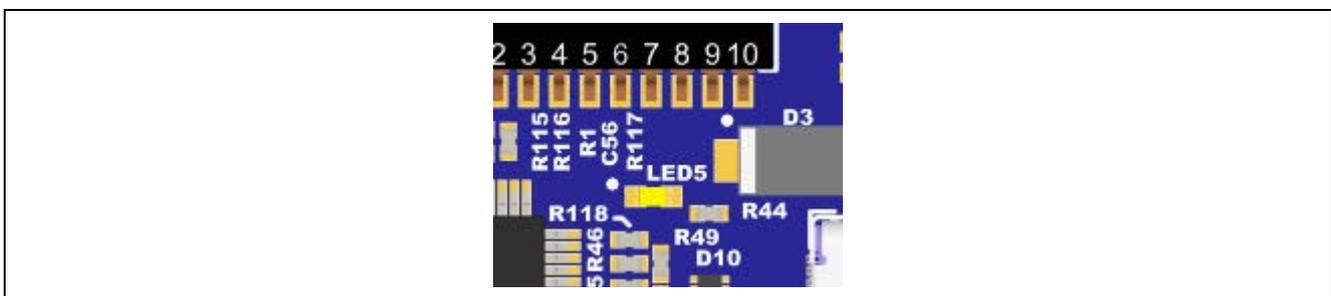


Figure 20. Debug LED



Figure 21. Ethernet 0 PHY LEDs



Figure 22. Ethernet 1 PHY LEDs

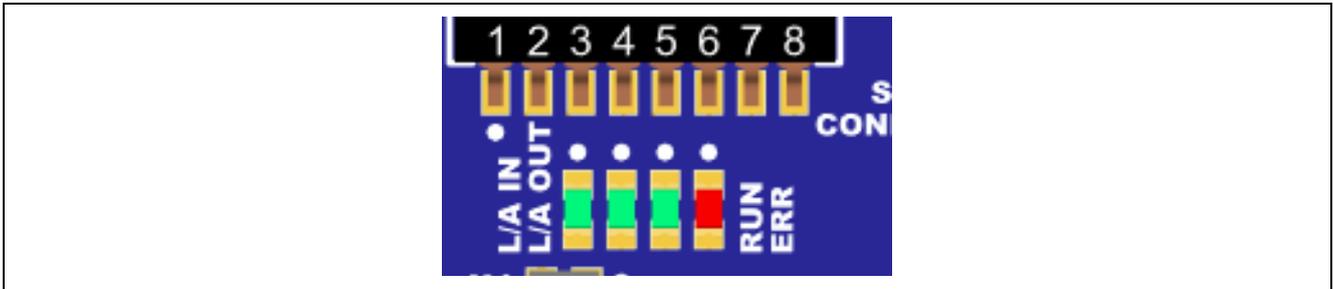


Figure 23. EtherCAT LEDs

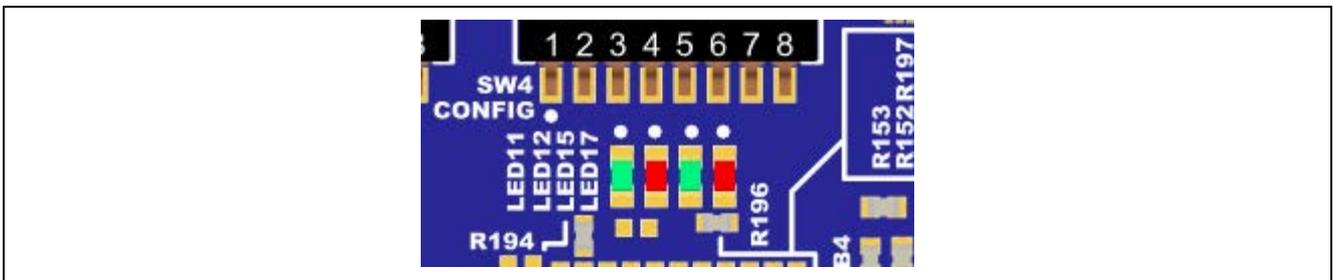


Figure 24. Network LEDs

5.5.2 User and Reset Switches

Three miniature, momentary, mechanical push-button type SMT switches are mounted on the EK-RA8T2 board.

Pressing the reset switch (SW3) generates a reset signal to restart the RA MCU.

Table 26. EK-RA8T2 Board Switches

Designator	Function	MCU Control Port	Switch Color
SW1	User Switch	P009 (IRQ13-DS)	Blue
SW2	User Switch	P008 (IRQ12-DS)	Blue
SW3	MCU Reset Switch	RESET_L	Red

The user switches SW1 and SW2 may be isolated from the main MCU, so the associated ports can be used for other purposes. To separate SW1 from P009, trace cut jumper E31 must be open. To separate SW2 from P008, trace cut jumper E32 must be open.

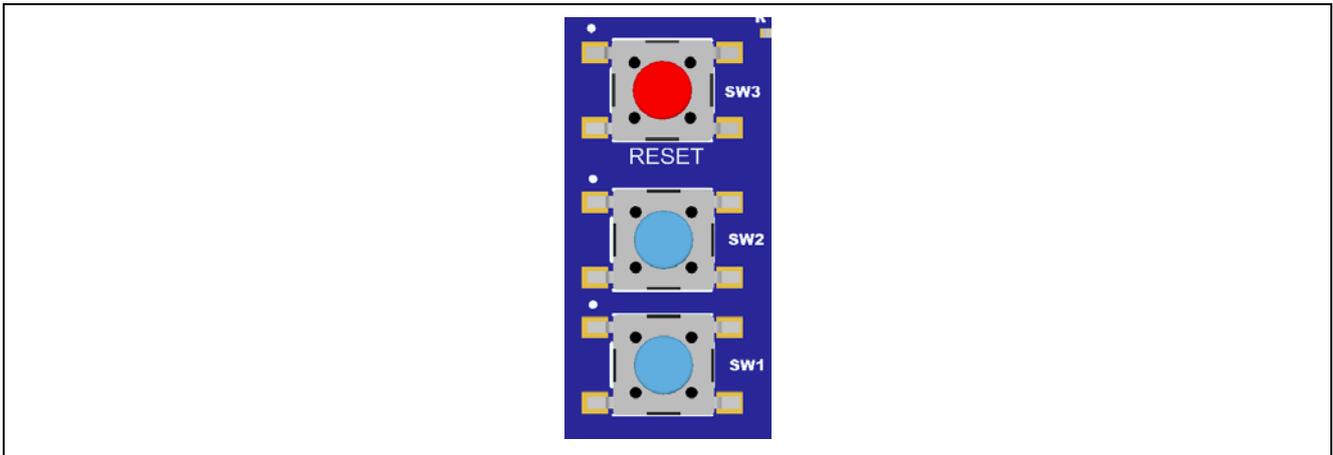


Figure 25. Reset and User Switches

5.5.3 MCU Boot Mode

A switch (SW6-1) is provided to select the boot mode (P201/MD) of the RA MCU. For normal operation, or Single-Chip mode, turn SW6-1 OFF. To enter SCI Boot mode or USB boot mode, turn SW6-1 ON.

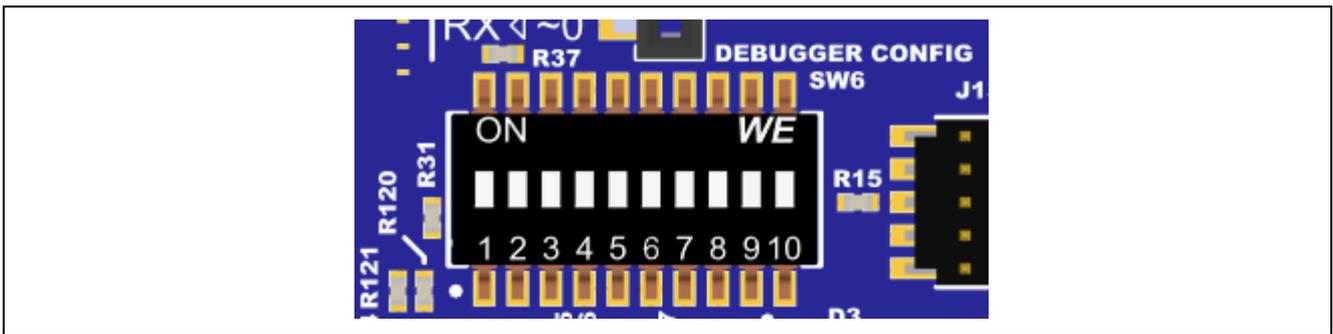


Figure 26. Boot Mode

6. Special Feature Access Area

The Special Feature Access area provides features specific to the RA8T2 MCU group such as GMII Ethernet Physical Layer Transceivers and isolated RS485. The switches to control the peripheral interface selection are also provided. The following special features are present:

1. Ethernet 0 and Ethernet 1
2. EEPROM
3. Octo-SPI Flash
4. SDRAM
5. CAN-FD 0 and CAN-FD 1
6. RS485

Note: Normally the SDRAM and Octo-SPI devices would be in this area, however, to optimize the layout for these high-speed devices, these components have been placed in the MCU Native Pin Access area.

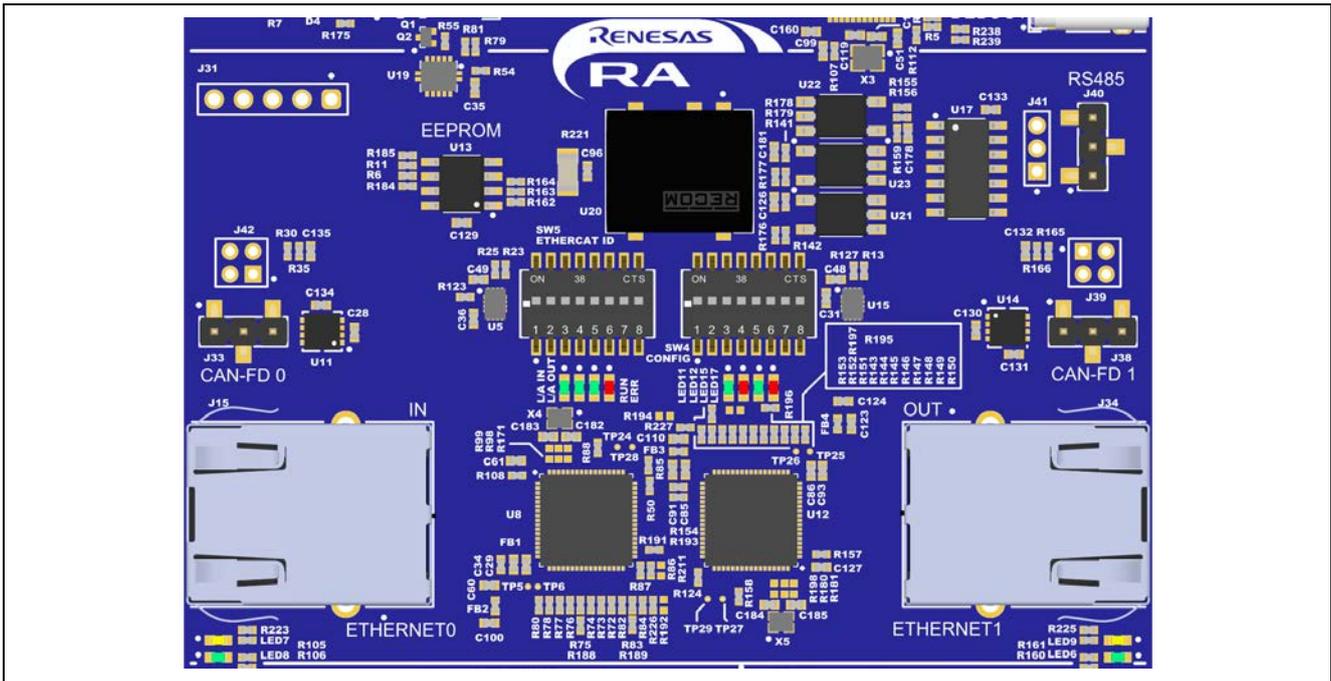


Figure 27. Special Feature Access Area

6.1 Ethernet

The Ethernet interfaces use two GMII Ethernet Physical Layer Transceivers (PHY) (U8 and U12), each connected to an RJ45 standard Ethernet connector (J15 and J34) with integrated magnetics. For Ethernet 0 status information is given by LED7 (yellow) and LED8 (green), both situated next to J15. For Ethernet 1 status information is given by LED9 (yellow) and LED6 (green), both situated next to J34. The Ethernet clock is sourced from the MCU via clock buffer U24.

6.1.1 EtherCAT ID Switch

SW5 can be used to set the EtherCAT ID. It is connected to I/O expander (U5) which can be accessed over the I²C bus slave address: 0x44 (7-bits).

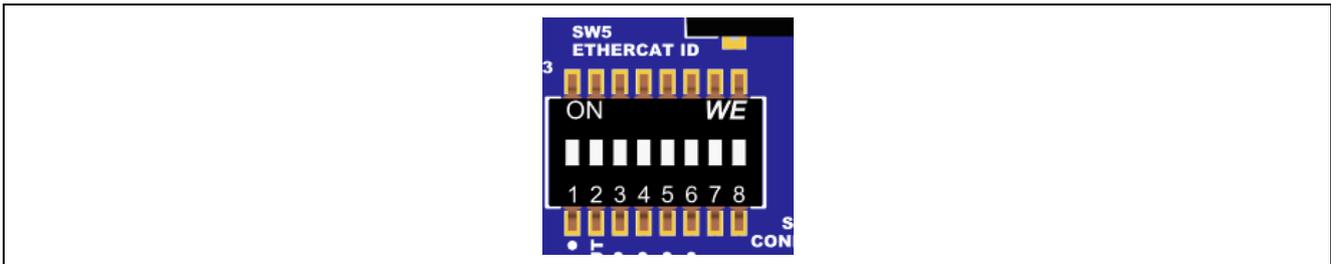


Figure 28. EtherCAT ID Switch

6.1.2 Configuring Ethernet for Different Modes of Operation

The tables below show how to configure the Ethernet mode of operation.

Table 27. Ethernet Channel 0 Mode Configuration

	R87	R188	R189	R190	R191	R192	R203	R211	R212	R86
MII (default)	Fit	Fit	Fit	Not fit	Fit	Not fit	Not fit	Not fit	0R	39R
GMII	Fit	Fit	Fit	Not fit	Fit	Not fit	Not fit	Not fit	0R	39R
EtherCAT	Fit	Fit	Not fit	Not fit	Fit	Fit	Not fit	Not fit	0R	39R
RGMII	Not fit	Fit	N/A	Not fit	N/A	Not fit	Not fit	Fit	39R	0R
RMII	Not fit	Not fit	N/A	Fit	Not fit	Fit	Fit	Not fit	0R	39R

Table 28. Ethernet Channel 1 Mode Configuration

	R119	R196	R197	R195	R193	R194	R206	R209	R210	R154
MII (default)	Fit	Fit	Fit	Not fit	Fit	Not fit	Not fit	Not fit	0R	39R
GMII	Fit	Fit	Fit	Not fit	Fit	Not fit	Not fit	Not fit	0R	39R
EtherCAT	Fit	Fit	Not fit	Not fit	Fit	Fit	Not fit	Not fit	0R	39R
RGMII	Not fit	Fit	N/A	Not fit	N/A	Not fit	Not fit	Fit	39R	0R
RMII	Not fit	Not fit	N/A	Fit	Not fit	Fit	Fit	Not fit	0R	39R

6.1.3 Ethernet PHY

Table 29. Ethernet 0 Port Assignments

Ethernet Signal Description (GMII)	EK-RA8T2
	Signal/Bus
PHY clock	P902
MDINT	P513
MDC	P708
MDIO	P709
MII_TXCLK	PB01
TXD0	PB00
TXD1	PB02
TXD2	PB03
TXD3	PB04
TXD4	PD07
TXD5	PB07
TXD6	PB06
TXD7	PB05
TX_EN	P705
TX_ER	P707
GTX_CLK	P706
RXD0	P702
RXD1	P701
RXD2	P700
RXD3	P406
RXD4	PD03
RXD5	PD04
RXD6	PD05
RXD7	PD06
RX_DV	P405
RX_ER	P704
RX_CLK	P703
NRESET#	P711
Link status	P710
COL	NC
CRS	NC

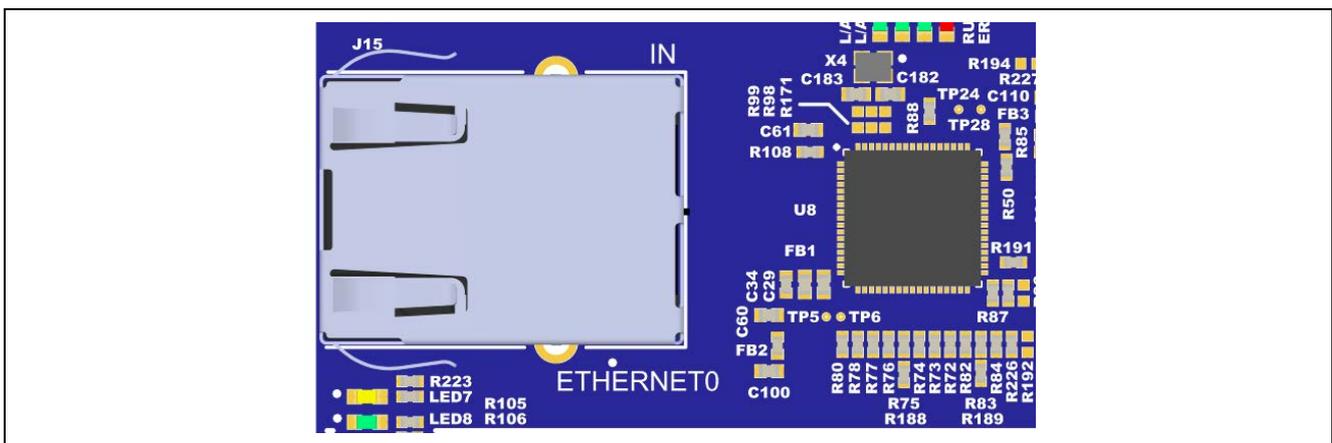


Figure 29. Ethernet 0 Connector

Table 30. Ethernet 1 Port Assignments

Ethernet Signal Description (GMII)	EK-RA8T2
	Signal/Bus
PHY clock	P902
MDINT	P107
MDC	P708
MDIO	P709
MII_TXCLK	P311
TXD0	P307
TXD1	P306
TXD2	P305
TXD3	P304
TXD4	P910
TXD5	P911
TXD6	P912
TXD7	P913
TX_EN	P310
TX_ER	P308
GTX_CLK	P309
RXD0	P906
RXD1	P907
RXD2	P908
RXD3	P909
RXD4	P904
RXD5	P207
RXD6	PD01
RXD7	PD02
RX_DV	P206
RX_ER	P312
RX_CLK	P905
NRESET#	P711
Link status	P106
COL	NC
CRS	NC

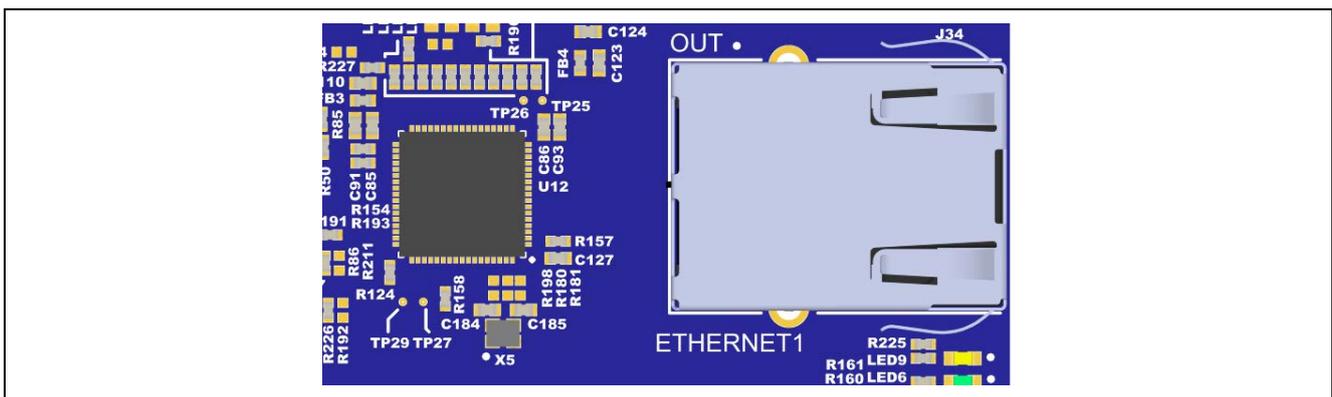


Figure 30. Ethernet 1 Connector

Table 31. Ethernet Components

Component	Manufacturer	Manufacturer Part Number
Ethernet PHY	Microsemi	VSC8541XMV-02
RJ45 Connector	Abracon	ARJM11C7-502-AB-ER2-T

6.2 EEPROM

The EK-RA8T2 supplies an 32Kbit 24CW320T-I/SN EEPROM (U13) which can be used for EtherCAT or general external storage.



Figure 31. EEPROM

6.3 Octo-SPI Flash

Included on the EK-RA8T2 board is a 512 Mb (64 MB) Octal serial NOR flash memory (IS25LX512M-JHLE). The Octo-SPI serial flash device (U3) connects to the Octo-SPI peripheral on the RA MCU and defaults to standard SPI mode initially. The flash memory is enabled for XIP (Execute-In-Place) mode directly after it is powered on.

Table 32. Octo-SPI Flash Assignments

Octo-SPI Flash Signal Description	EK-RA8T2
Description	Signal/Bus
PC07_OSPI_FLASH_RESET#	PC07
PC06_OSPI_FLASH_ERR#	PC06
P603_OSPI_FLASH_C	P603
PC05_OSPI_FLASH_S#	PC05
P607_OSPI_FLASH_DQS	P607
PC01_OSPI_FLASH_DQ0	PC01
P605_OSPI_FLASH_DQ1	P605
PC04_OSPI_FLASH_DQ2	PC04
PC02_OSPI_FLASH_DQ3	PC02
PC03_OSPI_FLASH_DQ4	PC03
PC00_OSPI_FLASH_DQ5	PC00
P606_OSPI_FLASH_DQ6	P606
P604_OSPI_FLASH_DQ7	P604

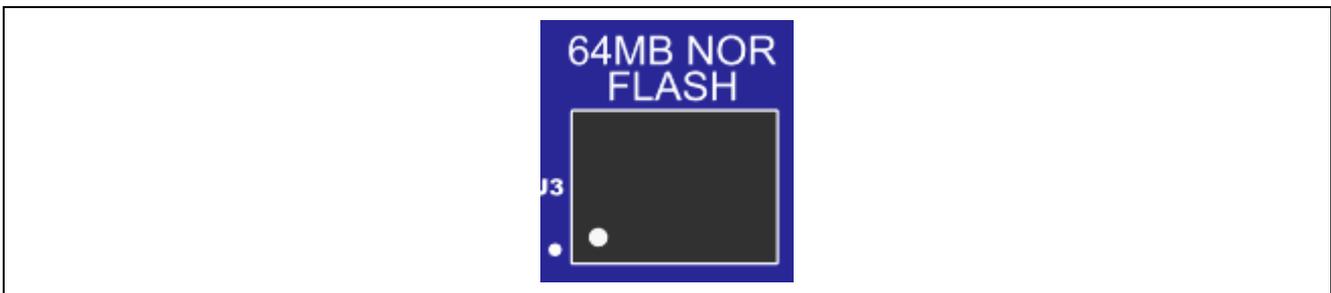


Figure 32. Octo-SPI Flash (labelled as “64MB NOR FLASH” on silkscreen text)

6.4 SDRAM

Included in the EK-RA8T2 board is a 512 Mb (64 MB organized as 16M x 32 bits) SDRAM (U2) (IS42S16320F-6BLI).

Table 33. SDRAM Assignments

SDRAM	EK-RA8T2
Description	Signal/Bus
A0	PA04
A1	PA03
A2	PA02
A3	PA01
A4	PA00
A5	P503
A6	P504
A7	P505
A8	P506
A9	P507
A10	P508
A11	P509
A12	P510
BA0	P608
BA1	PD00
DQ0	P302
DQ1	P301
DQ2	P300
DQ3	P112
DQ4	P113
DQ5	P114
DQ6	P115
DQ7	P609
DQ8	PA11
DQ9	PA12
DQ10	PA13
DQ11	PA14
DQ12	P610
DQ13	P611
DQ14	P612
DQ15	P613
CKE	PA06
CLK	PA15
DQML	P614
DQMH	PA05
WE#	PA08
CAS#	PA09
RAS#	PA10
CS#	P813

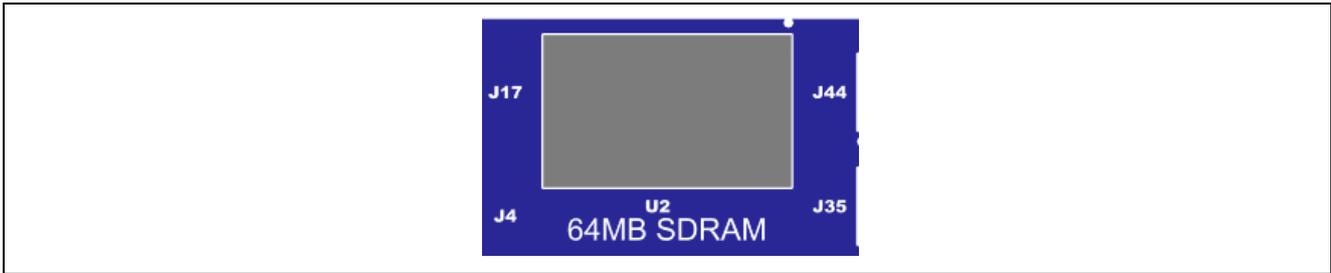


Figure 33. SDRAM

6.5 CAN FD Buses

The EK-RA8T2 board provides two CAN FD buses, each driven by a CAN FD bus transceiver U11 and U14 (MCP2562FD-E/MF). External connections to each CAN FD bus are made using 0.1” pitch 3-pin male headers J33 and J38. For CAN FD 0, the links E96 and E97 provide termination resistors which can be removed by cutting the circuit links. This can be reconnected through J42 (not populated). For CAN FD 1, the links E80 and E81 provide termination resistors which can be removed by cutting the circuit links. This can be reconnected through J39 (not populated).

The ports used by CAN FD 0 (P202 and P203) are shared with the Arduino and mikroBUS™ interfaces, and the board is configured to allocate these ports to CAN FD 0 by default. To use the ports for Arduino or mikroBUS™ instead, cut links E34 and E53.

The ports used by CAN FD 1 (P414 and P415) can be used for GPIO if CAN FD 1 is not in use. Cut links E18 and E20 to disconnect them from U14 for use as GPIO.

Table 34. CAN FD 0 Bus Connections Between U11 and RA8T2

CAN FD 0 Signal Description	EK-RA8T2 Port
RXD	P202
TXD	P203
STBY	SW4-3

Table 35. CAN FD 0 Connector Pin Assignments

CAN FD 0 Connector (J33)	Function
1	CANH
2	CANL
3	GND

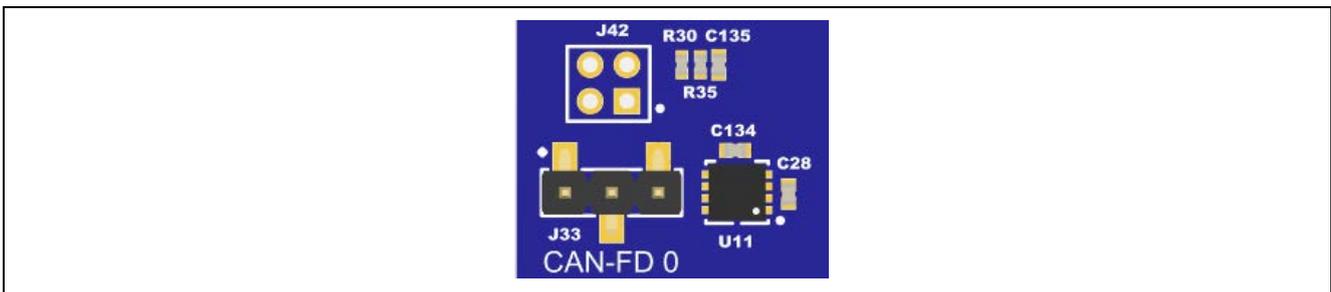


Figure 34. CAN FD 0 Connector and Transceiver

Table 36. CAN FD 1 Bus Connections Between U14 and RA8T2

CAN FD 1 Signal Description	EK-RA8T2 Port
RXD	P414
TXD	P415
STBY	SW4-4

Table 37. CAN FD 1 Connector Pin Assignments

CAN FD 1 Connector (J38)	Function
1	CANH
2	CANL
3	GND

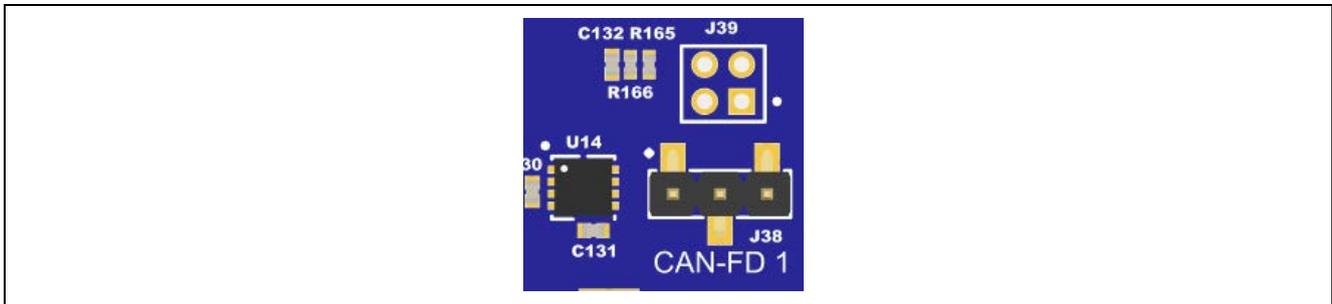


Figure 35. CAN FD 1 Connector and Bus Transceiver

6.6 MODBUS / RS485

The EK-RA8T2 board provides a MODBUS / RS-485 bus transceiver U17 (ISL3176EIBZ) that is connected to the RA MCU via optical isolators and multiplexer switches 74CBTLV3126BQ (U19C and U19D). The bus transceiver is powered by an isolated 3.3 V power supply (U20). External connection to the MODBUS / RS-485 bus is made using the 0.1" pitch 3-pin male header J40. The ports used by RS485 interface (P808, P809 and P810) are shared with the Arduino and mikroBUS™ interfaces. To disconnect them from the RS485 interface so that they can be used for Arduino or mikroBUS™, SW4-8 should be set to on.

Table 38. MODBUS / RS-485 Bus Connections Between U17 and RA8T2

MODBUS / RS-485 Signal Description	EK-RA8T2 Port
RO	P808 (RXD7)
RE#	P810 (DE7)
DE	P810 (DE7)
DI	P809 (TXD7)

Table 39. MODBUS / RS-485 Port Assignments

MODBUS / RS-485 Connector (J40)	Function
1	B/Z
2	GND
3	A/Y

Note: Pins 1 (B/Z) and 3 (A/Y) of J40 are connected to a termination resistor by E82 and E83. To disconnect the termination resistor, cut E82 or E83. J41 can be populated to reconnect the termination resistor.

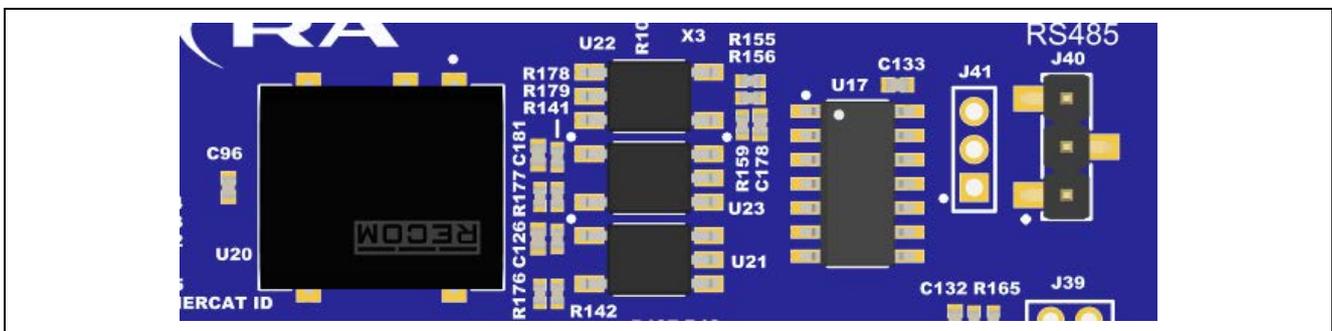


Figure 36. MODBUS / RS-485 Connector, Bus Transceiver and isolated circuit

7. MCU Native Pin Access Area

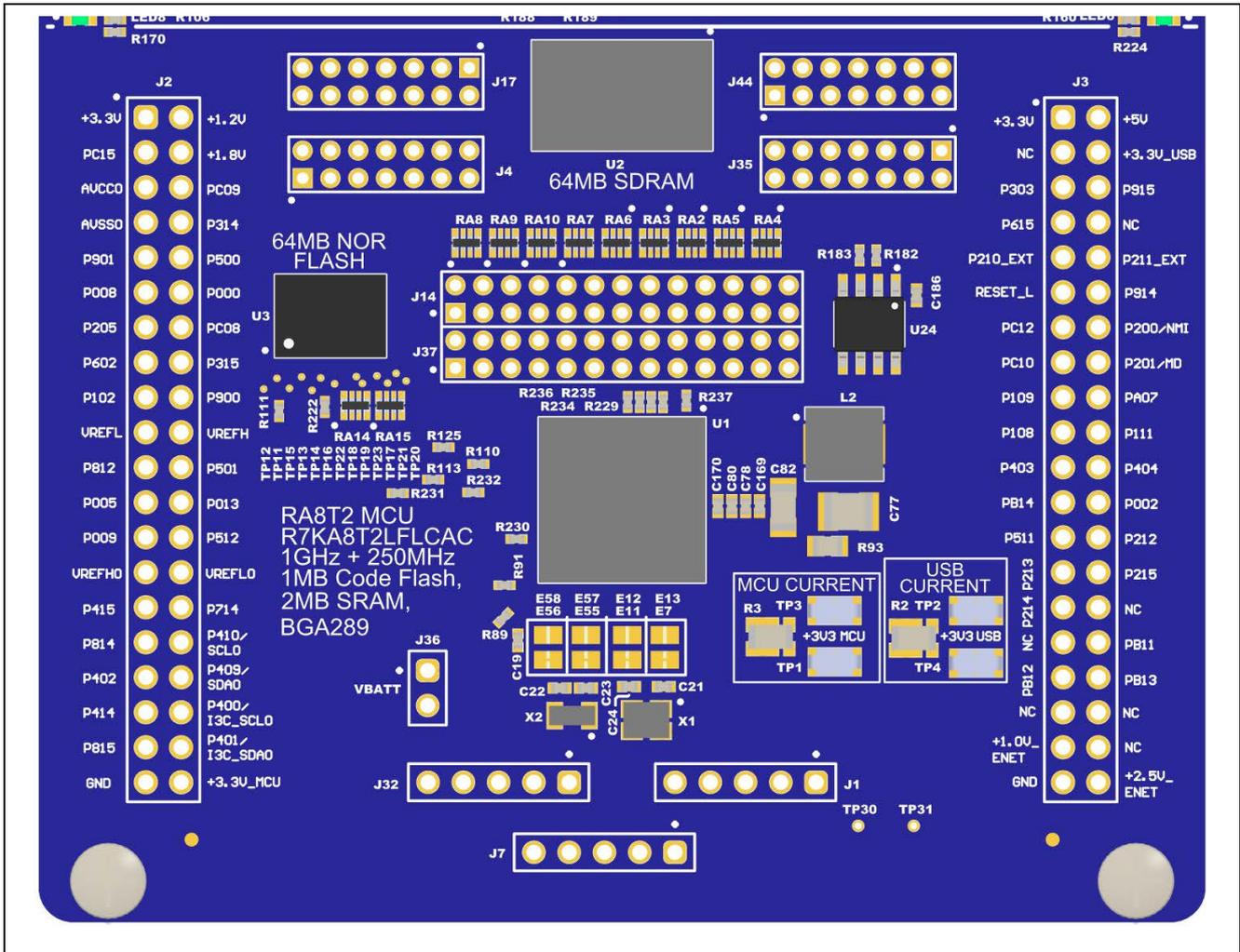


Figure 37. Native Pin Access Area

7.1 Breakout Pin Headers (not populated)

The EK-RA8T2 board pin header connectors (not populated), J2, and J3 provide access to nearly all RA MCU interface signals, and voltages for all RA MCU power ports. Each header pin is labelled with the voltage or port connected to that pin. Refer to the RA8T2 MCU Group User's Manual for details of each port function, and the EK-RA8T2 board schematic for pin header port assignments.

Pin header connectors (not populated): J14 and J37 provide access to the SDRAM interface pins.
 J4, J17, J35 and J44 provide access to the Ethernet interface pins.
 J1 provides access to the TAS status checking interface pins.
 J7 and J32 provide access to the GTP interface pins.

7.2 MCU and USB Current Measurement

Included in the Native Pin Access area are current measurement resistors and test points to measure the MCU USB controller current and the MCU core power current.

The EK-RA8T2 board provides precision 5 mΩ resistors (Yageo, part number PS0612FKE070R005L) for current measurement of the main 3.3 V MCU power and the 3.3 V USB MCU power. Measure the voltage drop across these resistors and use Ohm's Law to calculate the current. For convenience, TP1 and TP3 are provided to measure the main 3.3 V MCU power, and TP2 and TP4 are provided to measure the 3.3 V USB MCU power. See Figure 40 for the location of TP1, TP2, TP3 and TP4.

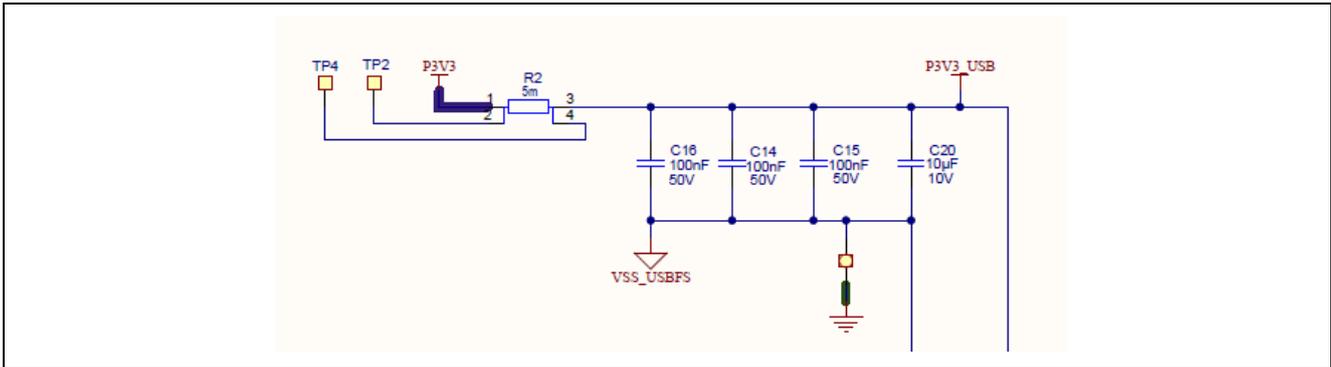


Figure 38. RA USB Current Measurement Circuit

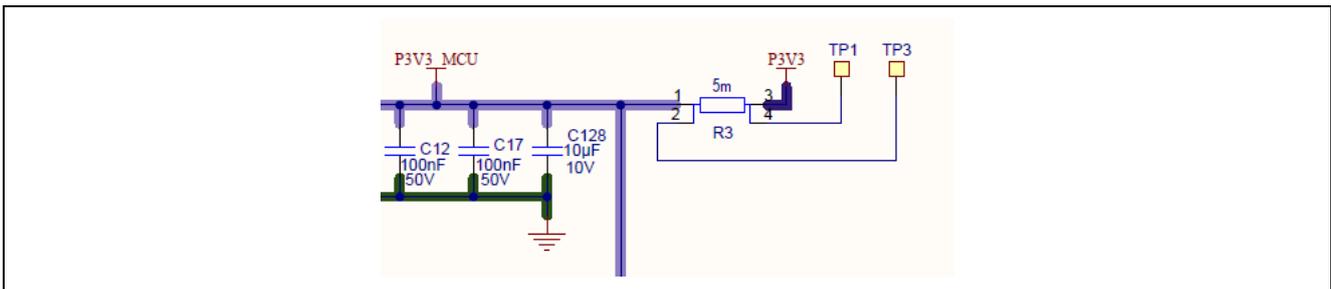


Figure 39. RA +3.3 V Current Measurement Circuit

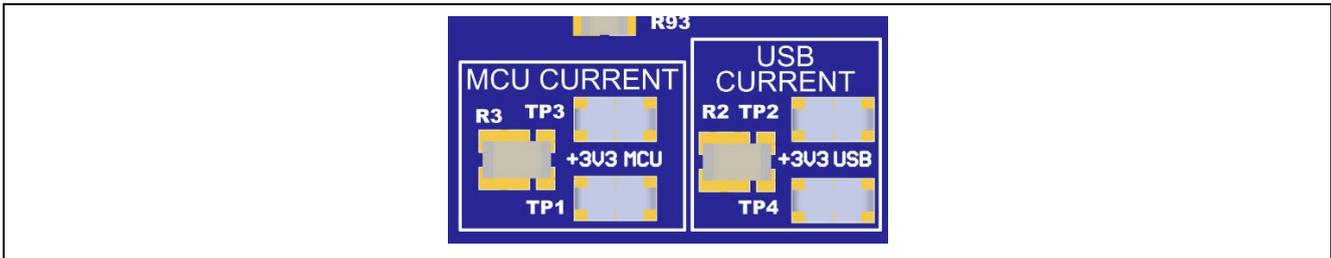


Figure 40. RA MCU and USB Current Measurement

8. Recommended Parts

Table 40 lists recommended part numbers for optional components that can be fitted as required.

Table 40. Part Numbers

Designator(s)	Description	Manufacturer	Part Number
J1, J7, J32	5-way male header	Würth Elektronik	613 005 211 21
J2, J3	40-way male header	Würth Elektronik	613 040 211 21
J4, J17	14-way male header	Sullins Connector Solutions	NRPN072PAEN-RC
J14, J37	26-way male header	Sullins Connector Solutions	NRPN132PAEN-RC
J27, J28	Seeed Grove [®] system connector	Seeed Studio	110990037
J30	SparkFun Qwiic [®] connector	JST	SM04B-SRSS-TB(LF)(SN)
J21, J22	mikroBUS [™] connector	Samtec	CES-108-01-T-S

9. Certifications

The EK-RA8T2 v1 kit meets the following certifications/standards. See page 3 of this user's manual for the disclaimer and precautions.

9.1 EMC/EMI Standards

- FCC Notice (Class A)



This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

NOTE- This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/television technician for help.

- Innovation, Science and Economic Development Canada ICES-003 Compliance:

CAN ICES-3 (A)/NMB-3(A)

- CE Class A (EMC)



This product is herewith confirmed to comply with the requirements set out in the Council Directives on the Approximation of the laws of the Member States relating to Electromagnetic Compatibility Directive 2014/30/EU.

Warning – This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures to correct this interference.

- UKCA Class A (EMC)



This product is in conformity with the following relevant UK Statutory Instrument(s) (and its amendments): 2016 No. 1091 Electromagnetic Compatibility Regulations 2016.

Warning – This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures to correct this interference.

- Taiwan: CNS 15936, Class A limits 警告：為避免電磁干擾，本產品不應安裝或使用於住宅環境
- Australia/New Zealand AS/NZS CISPR 32:2015, Class A

9.2 Material Selection, Waste, Recycling and Disposal Standards

- EU RoHS
- WEEE Directive (2012/19/EU) & The Waste Electrical and Electronic Equipment Regulations 2013
 - The WEEE (Waste Electrical and Electronic Equipment) regulations put responsibilities on producers for the collection and recycling or disposal of electrical and electronic waste. Return of WEEE under these regulations is applicable in the UK and European Union.
 - This equipment (including all accessories) is not intended for household use. After use the equipment cannot be disposed of as household waste, and the WEEE must be treated, recycled and disposed of in an environmentally sound manner.
- Renesas Electronics Europe GmbH can take back end of life equipment. Register for this service at;
- <https://www.renesas.com/en/form/weee-questionnaire>
- China SJ/T 113642014, 10-year environmental protection use period.



9.3 Safety Standards

- UL 94V-0

10. Design and Manufacturing Information

The design and manufacturing information for the EK-RA8T2 v1 kit is available in the “EK-RA8T2 v1 Design Package” available on [renesas.com/ek-ra8t2](https://www.renesas.com/ek-ra8t2).

- EK-RA8T2 Board Design Package: ek-ra8t2-v1-designpackage.zip

Table 41. EK-RA8T2 Board Design Package Contents

File Type	Content	File/Folder Name
File (PDF)	Schematics	ek-ra8t2-v1-schematics
File (PDF)	Mechanical Drawing	ek-ra8t2-v1-mechdwg
File (PDF)	3D Drawing	ek-ra8t2-v1-3d
File (PDF)	BOM	ek-ra8t2-v1-bom
Folder	Manufacturing Files	Manufacturing Files
Folder	Design Files	Design Files - Altium

11. Website and Support

Visit the following URLs to learn about the kit and the RA family of microcontrollers, download tools and documentation, and get support.

EK-RA8T2 Resources	renesas.com/ek-ra8t2
RA Kit Information	renesas.com/ra/kits
RA Product Information	renesas.com/ra
RA Product Support Forum	renesas.com/ra/forum
RA Videos	renesas.com/ra/videos
Renesas Support	renesas.com/support
RA Flexible Software Package (FSP)	renesas.com/fsp

Revision History

Rev.	Date	Description	
		Page	Summary
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1.01	Feb.13.26	41	Updated Table 28

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