User's Manual

RA8E2 Group

Evaluation Kit for RA8E2 Microcontroller Group
EK-RA8E2 v1
User's Manual

Renesas RA Family
RA8 Series

Renesas Electronics
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1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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This Evaluation Kit is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area, or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- Ensure attached cables do not lie across the equipment.
- Reorient the receiving antenna.
- Increase the distance between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that which the receiver is connected.
- Power down the equipment when not in use.
- Consult the dealer or an experienced radio/TV technician for help.

Note: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken:

- The user is advised that mobile phones should not be used within 10 m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Evaluation Kit does not represent an ideal reference design for an end product and does not fulfill the regulatory standards for an end product.

Renesas RA Family

EK-RA8E2 v1

Contents

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1. Kit Overview

The EK-RA8E2, an Evaluation Kit for RA8E2 MCU Group, enables users to seamlessly evaluate the features of the RA8E2 MCU group and develop embedded systems applications using Flexible Software Package (FSP) and e^2 studio IDE. The users can utilize rich on-board features along with their choice of popular ecosystems add-ons to bring their big ideas to life.

The EK-RA8E2 board features the RA8E2 MCU, OSPI Flash, SDRAM, CAN-FD and a Parallel Graphics Expansion Port.

The key features of the EK-RA8E2 board are categorized in three groups (consistent with the architecture of the kit, with a few exceptions) as follows:

MCU Native Pin Access

- R7FA8E2AFDCBD MCU (referred to as RA MCU)
- 480 MHz, Arm® Cortex®-M85 core
- 1 MB Code Flash, 672 kB SRAM
- 224 pins, BGA package
- Native pin access through 2 x 20-pin, and 2 x 40-pin headers (not populated)
- MCU current measurement points for precision current consumption measurement
- Multiple clock sources – RA MCU oscillator and sub-clock oscillator crystals, providing precision 24.000 MHz and 32,768 Hz reference clocks. Additional low-precision clocks are available internal to the RA MCU

System Control and Ecosystem Access

- USB Full Speed Host and Device (USB-C connector)
- Three 5 V input sources
  - USB (Debug, Full Speed)
  - External power supply (using surface mount clamp test points and power input vias)
- Three Debug modes
  - Debug on-board (SWD and JTAG)
  - Debug in (ETM, SWD, SWO, and JTAG)
  - Debug out (SWD, SWO, and JTAG)
- User LEDs and buttons
  - Three User LEDs (Red, Blue, Green)
  - Power LED (white) indicating availability of regulated power
  - Debug LED (yellow) indicating the debug connection
  - Two User buttons
  - One Reset button
- Five most popular ecosystems expansions
  - Two Seeed Grove® system (I^{2}C/Analog) connectors (not populated)
  - SparkFun® Qwiic® connector (not populated)
  - Two Digilent Pmod™ (SPI, UART and I^{2}C) connectors
  - Arduino™ (Uno R3) connector
  - MikroElektronika™ mikroBUS connector (not populated)
- MCU boot configuration jumper

Special Feature Access

- 64 MB (512 Mb) External Octo-SPI NOR Flash (present in the MCU Native Pin Access area)
- 64 MB (512 Mb) SDRAM (present in the MCU Native Pin Access area)
- Parallel Graphics Expansion Port (present in the MCU Native Pin Access area)
- CAN-FD
- Configuration Switch (SW4)

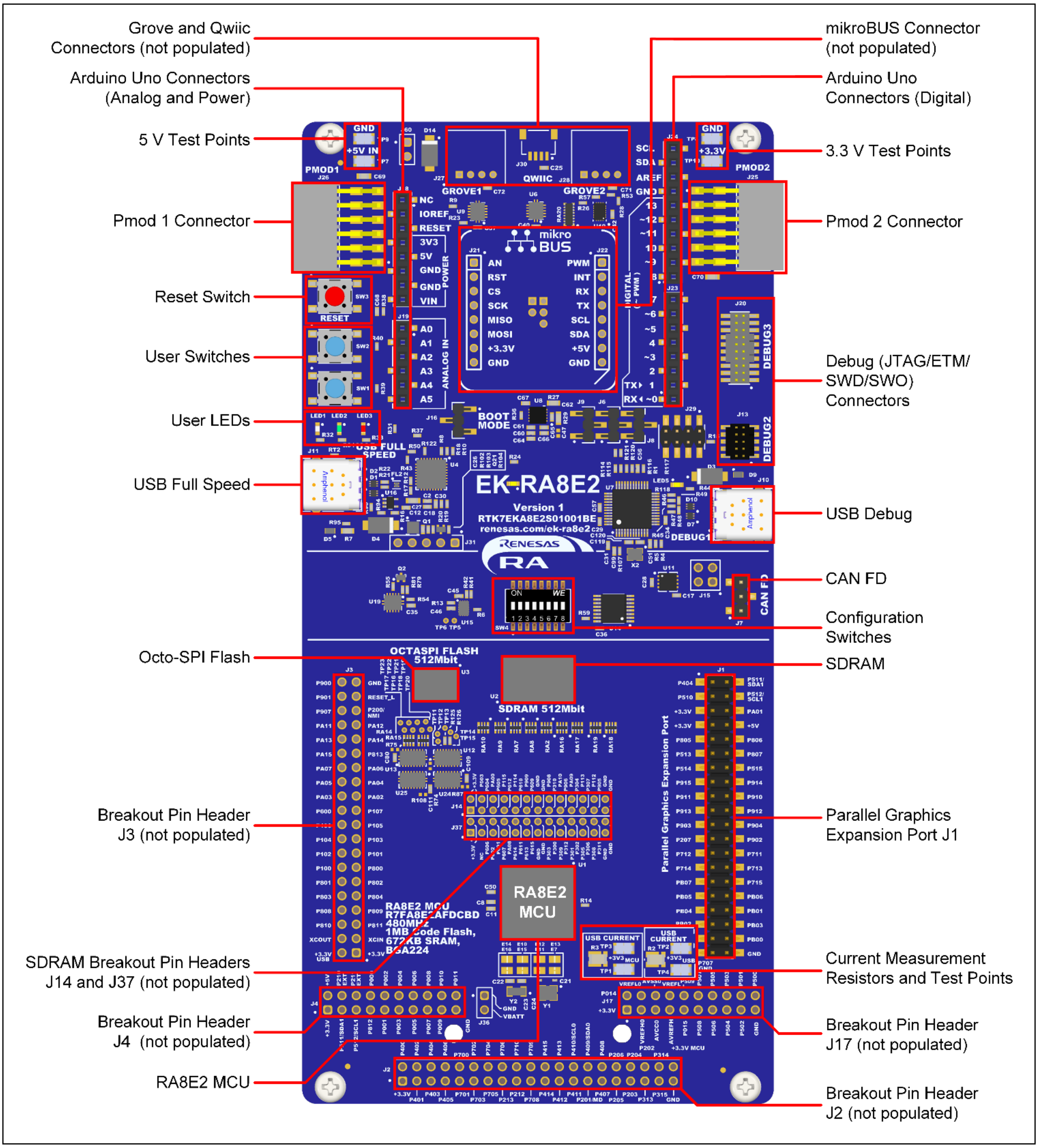

Figure 1. EK-RA8E2 Board Top Side

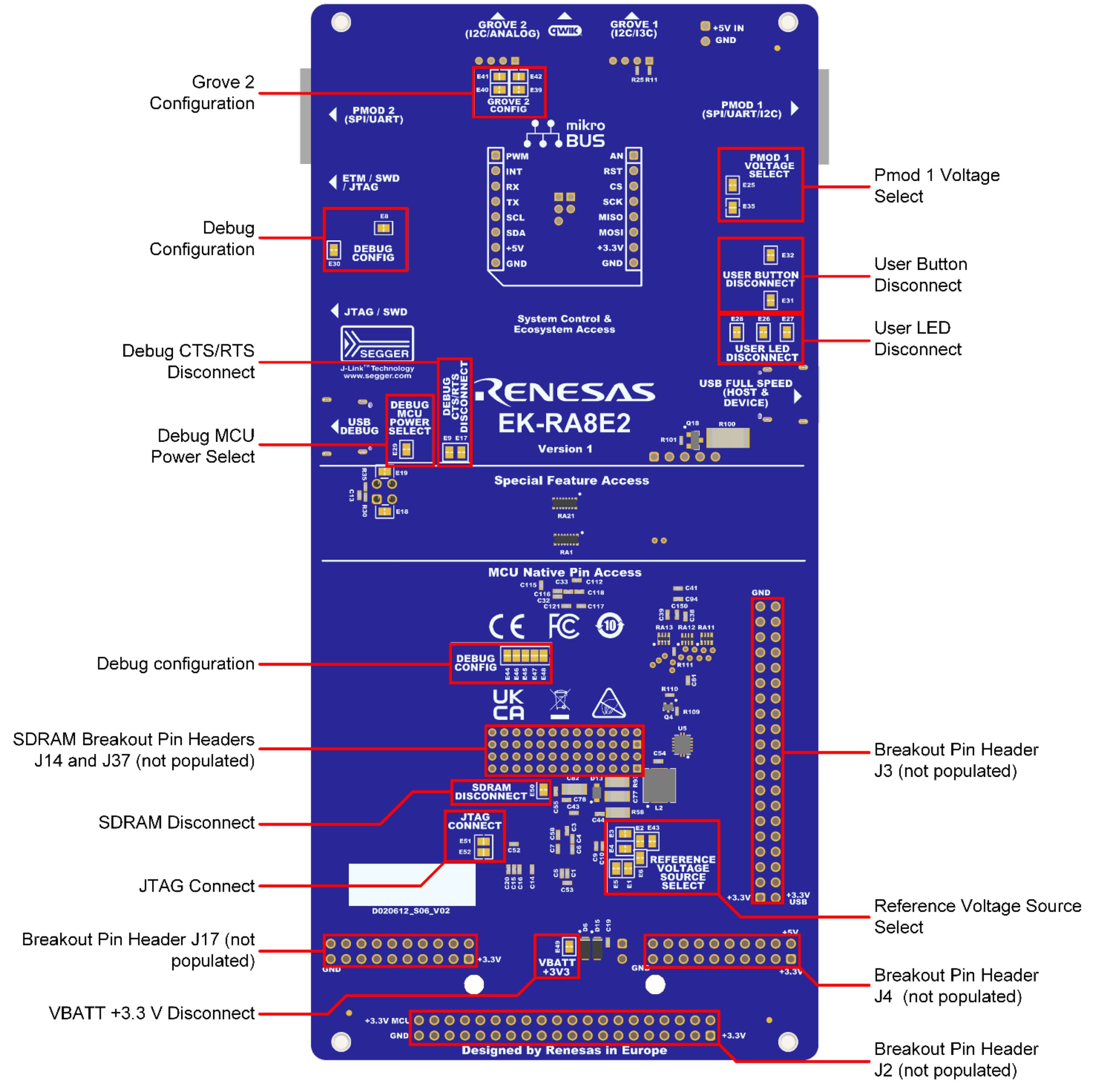

Figure 2. EK-RA8E2 Board Bottom Side

1.1 Assumptions and Advisory Notes

1. It is assumed that the user has a basic understanding of microcontrollers and embedded systems hardware.
2. It is recommended that the user refers to the *EK-RA8E2 Quick Start Guide* to get acquainted with the kit and the Quick Start example project that EK-RA8E2 board comes pre-programmed with.
3. Flexible Software Package (FSP) and Integrated Development Environment (IDE) such as e^2 studio are required to develop embedded applications on EK-RA8E2 kit.
4. Instructions to download and install software, import example projects, build them and program the EK-RA8E2 board are provided in the quick start guide.
5. The MCU fitted to the EK board may not contain the latest version of the on-chip boot firmware.

2. Kit Contents

The following components are included in the kit:

1. EK-RA8E2 v1 board
2. USB-C to USB-C cable
3. USB-A to USB-C cable
4. USB-C to USB-A female host cable
5. Parallel Graphics Expansion Board 2
6. Display mounting hardware (spacers and fixing screws)

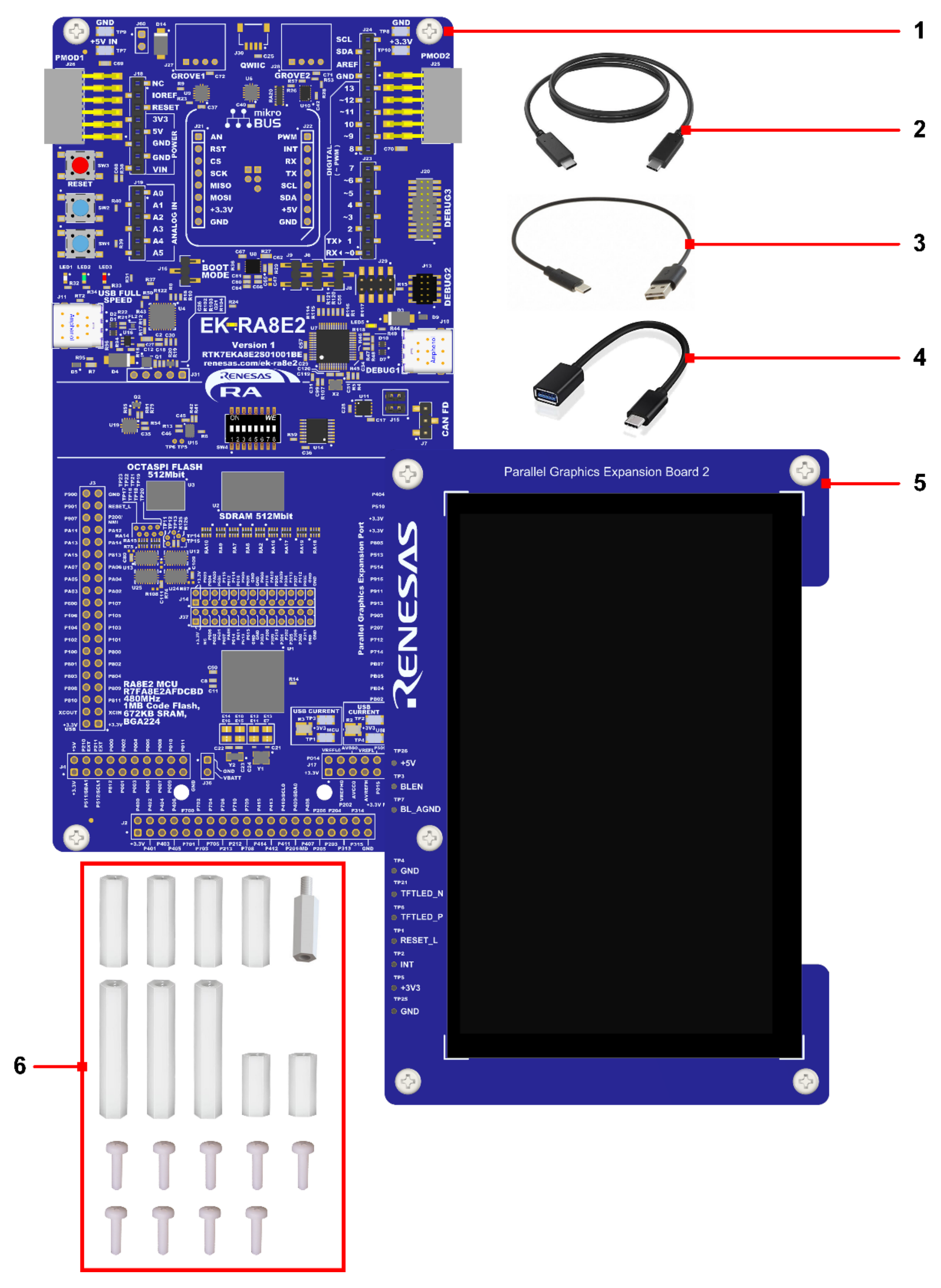

Figure 3. EK-RA8E2 Kit Contents

3. Ordering Information

EK-RA8E2 v1 kit orderable part number: RTK7EKA8E2S01001BE

Note: 1. The underlined character in the orderable part number represents the kit version.
2. The Parallel Graphics Expansion Board 2 orderable part number: RTKAPPLCDPS02001BE

Dimensions:

1. EK-RA8E2 board: 84 mm (width) x 175 mm (length)
2. Parallel Graphics Expansion Board 2: 95mm (width) x 140mm (length)

4. Hardware Architecture and Default Configuration

4.1 Kit Architecture

The EK-RA8E2 board is designed with three sections or areas to help shorten the learning curve of users and maximize the design and knowledge reuse among similar kits. The contents of these three areas are conceptually standardized among similar kits.

Table 1. Kit Architecture

Kit area	Area features	Area present on all similar kits	Functionality is:
MCU Native Pin Access Area	RA MCU, breakout pin headers for all MCU I/O and power, current measurement Parallel Graphics Expansion Port, Octo-SPI Flash, and SDRAM	Yes	MCU dependent
Special Feature Access Area	Configuration Switches MCU special features: CAN-FD	No	MCU dependent
System Control and Ecosystem Access Area	Power, Debug MCU, User LEDs and buttons, reset, ecosystem connectors, USB Full Speed Host and Device, and Boot configuration	Yes	Same or similar across similar kits

Note: The Octo-SPI Flash, SDRAM and Parallel Graphics Expansion Port are among the Special Feature Access features. Normally, they would be in the Special Feature Access Area, however, to optimize the layout, routing, and performance, they are placed in the MCU Native Pin Access area.

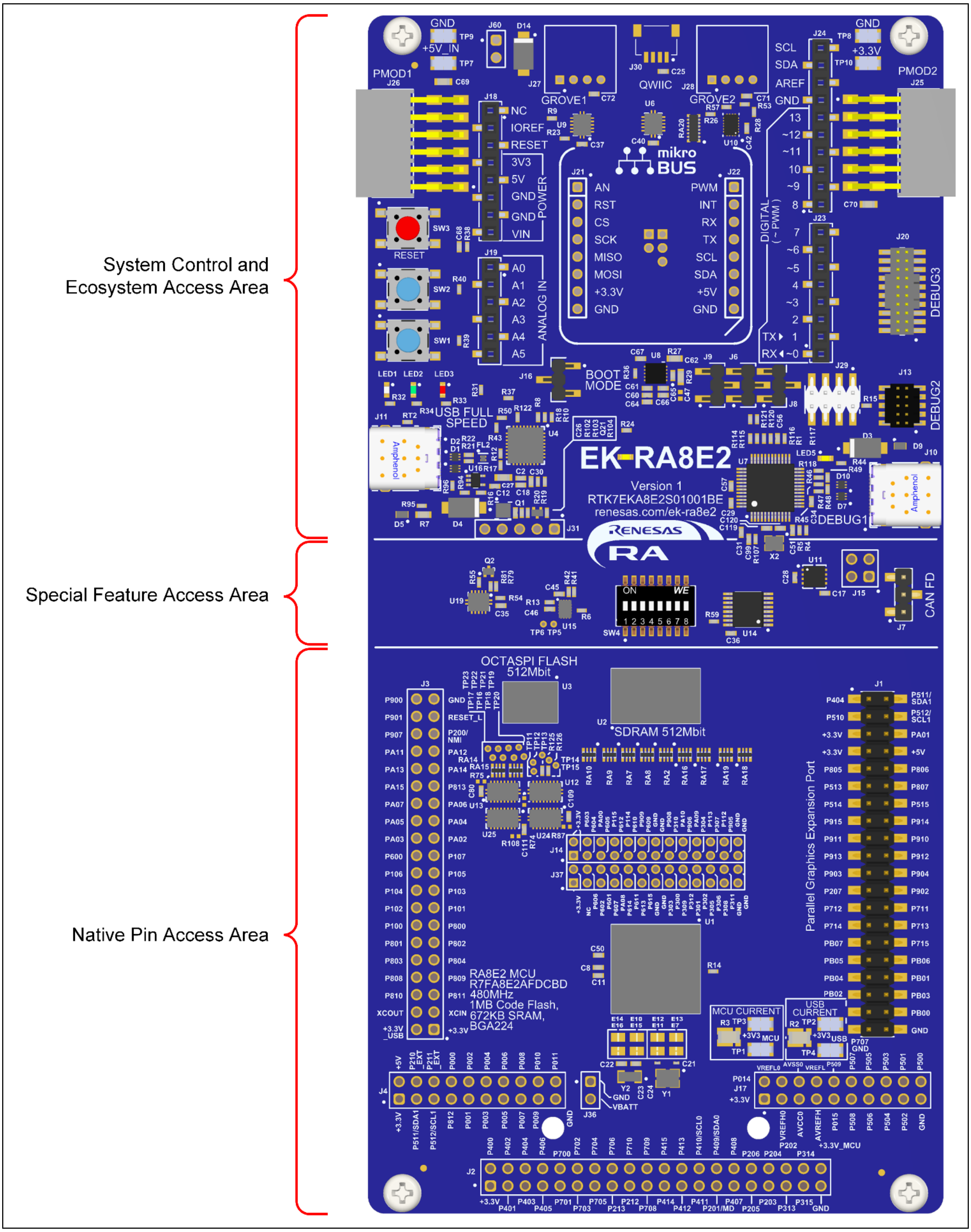

Figure 4. EK-RA8E2 Board Functional Area Definitions

4.2 System Block Diagram

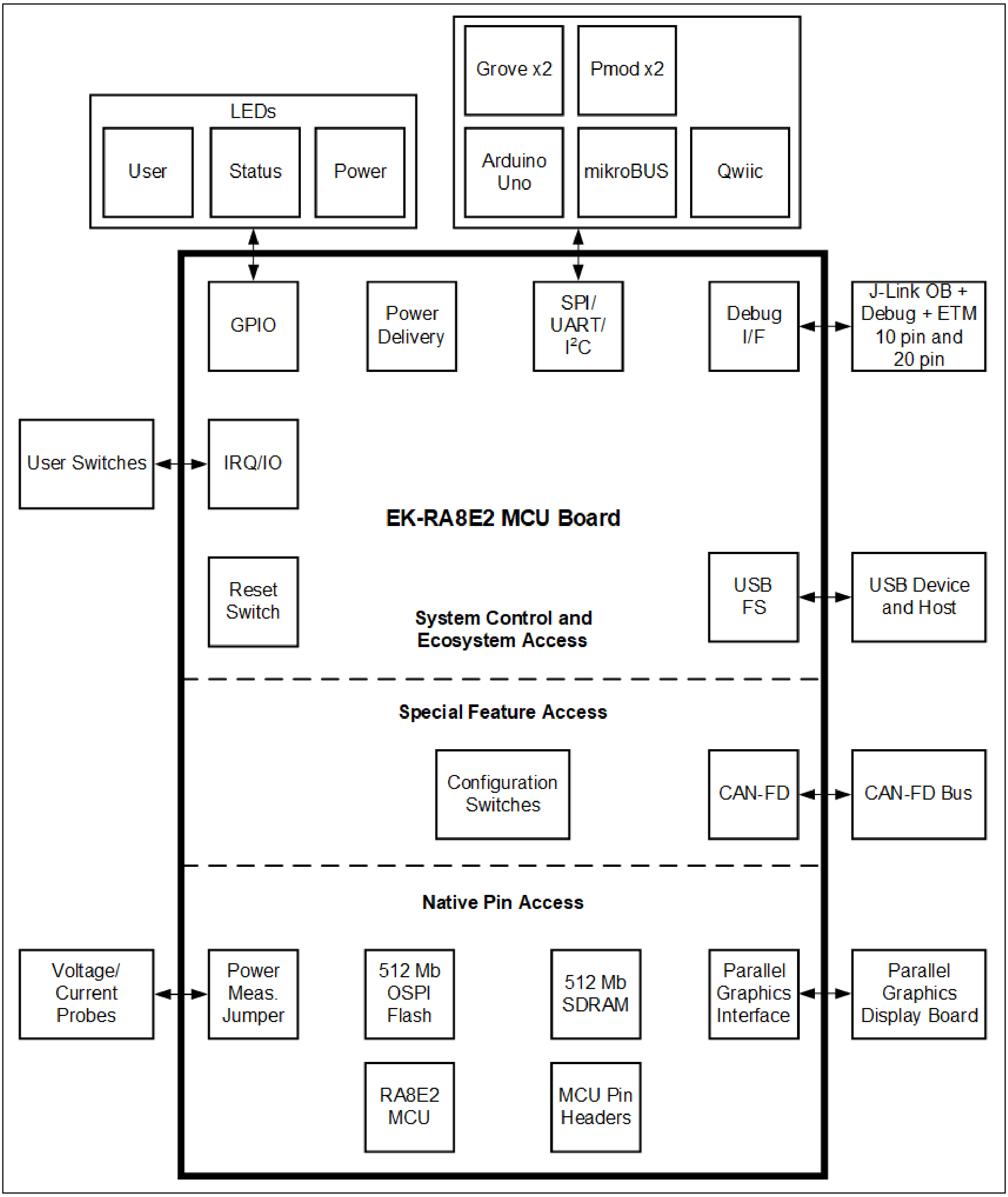

Figure 5. EK-RA8E2 Board Block Diagram

4.3 Jumper Configuration

Two types of jumpers are provided on the EK-RA8E2 board.

1. Copper jumpers (trace-cut type and solder bridge type)
2. Traditional pin header jumpers

The following sections describe each type and their default configuration.

4.3.1 Copper Jumpers

Copper jumpers are of two types, designated **trace-cut** and **solder-bridge**.

A **trace-cut jumper** is provided with a narrow copper trace connecting its pads. The silk screen overlay printing around a trace-cut jumper is a solid box. To isolate the pads, cut the trace between pads adjacent to each pad, then remove the connecting copper foil either mechanically or with the assistance of heat. Once the etched copper trace is removed, the trace-cut jumper is turned into a solder-bridge jumper for any later changes.

A **solder-bridge** jumper is provided with two isolated pads that may be joined together by one of three methods:

- Solder may be applied to both pads to develop a bulge on each and the bulges joined by touching a soldering iron across the two pads.
- A small wire may be placed across the two pads and soldered in place.
- A SMT resistor, size 0805, 0603, or 0402, may be placed across the two pads and soldered in place. A zero-ohm resistor shorts the pads together.

For any copper jumper, the connection is considered **closed** if there is an electrical connection between the pads (default for trace-cut jumpers.) The connection is considered **open** if there is no electrical connection between the pads (default for the solder-bridge jumpers.)

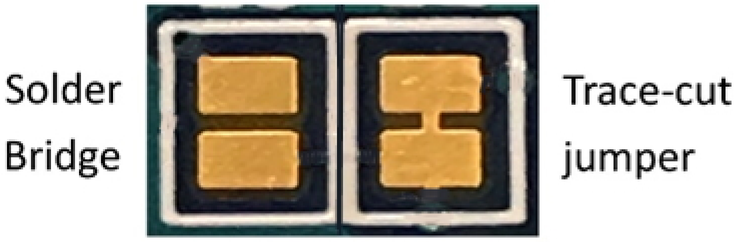

Figure 6. Copper Jumpers

4.3.2 Traditional Pin Header Jumpers

These jumpers are traditional small pitch jumpers that require an external shunt to open/close them. The traditional pin jumpers on the EK-RA8E2 board are 2 mm pitch headers and require compatible 2 mm shunt jumpers.

4.3.3 Default Jumper Configuration

The following table describes the default configuration for each jumper on the EK-RA8E2 board. This includes copper jumpers (Ex designation) and traditional pin jumpers (Jx designation).

The Circuit Group for each jumper is the designation found in the board schematic (available in the Design Package). Functional details for many of the listed jumpers may be found in sections associated with each functional area of the kits.

Table 2. Default Jumper Configuration

Location	Circuit Group	Default Open/Closed	Function
J6	J-Link OB	Jumper on pins 2-3	Configures J-Link OB connection to MCU mode
J8	J-Link OB	Jumper on pins 1-2	Configures the MCU for normal operation
J9	J-Link OB	Jumper on pins 2-3	Configures RA4M2 RESET_L for on-board debugger mode
J15	CAN-FD	Not Fitted	Replacement for E18 and E19 when both cut
J16	MCU Boot Mode	Jumper on pins 2-3	Configures the MCU for normal boot mode

Location	Circuit Group	Default Open/Closed	Function
J29	J-Link OB	Jumper on pins 1-2 Jumper on pins 3-4 Jumper on pins 5-6 Jumper on pins 7-8	Connects the J-Link OB debugger to the RA MCU
E1	MCU Power	Closed	Connects VREFL to GND
E2	MCU Power	Closed	Connects VREFH to +3.3 V
E3	MCU Power	Closed	Connects AVCC0 to +3.3 V
E4	MCU Power	Closed	Connects AVSS0 to GND
E5	MCU Power	Closed	Connects VREFL0 to GND
E6	MCU Power	Closed	Connects VREFH0 to +3.3 V
E7	MCU Clock	Closed	Connects P212/EXTAL to 24 MHz crystal
E8	Debug	Closed	Connects debugger JLOB_TRST to JTAG connectors
E9	J-Link Virtual COM Port	Closed	Connects P709 (RTS) to Debugger P408
E10	MCU Clock	Open	Connects XCIN to J3 pin 3
E11	MCU Clock	Closed	Connects P213/XTAL to 24 MHz crystal
E12	MCU Clock	Open	Connects P213/XTAL to J2 pin 15
E13	MCU Clock	Open	Connects P212/EXTAL J2 pin 17
E14	MCU Clock	Open	Connects XCOUT to J3 pin 4
E15	MCU Clock	Closed	Connects XCIN/P215 to 32.768 KHz crystal
E16	MCU Clock	Closed	Connects XCOUT/P214 to 32.768 KHz crystal
E17	J-Link Virtual COM Port	Closed	Connects P710 (CTS) to Debugger P409
E18	CAN-FD	Closed	Connects to CAN-FD L to terminating network
E19	CAN-FD	Closed	Connects to CAN-FD H to terminating network
E25	Pmod1	Closed	Connects PMOD1 +3.3V to pins 6 and 12
E26	User LED	Closed	Connects P406 to User LED2
E27	User LED	Closed	Connects P205 to User LED1
E28	User LED	Closed	Connects P405 to User LED3
E29	Debug MCU Power	Closed	Connects the Debug MCU power to +3.3 V
E30	Debugger	Closed	Connects the JTAG GND Detect pin on J20 and J13 to GND
E31	User Switch	Closed	Connects P001 to User Switch SW1
E32	User Switch	Closed	Connects P008 to User Switch SW2
E35	Pmod1	Open	Connects PMOD1 +5V pins 6 and 12
E39	Grove 2	Closed	Connects I^2C SCL1 to Grove 2 pin 1
E40	Grove 2	Closed	Connects I^2C SDA1 to Grove 2 pin 2
E41	Grove 2	Open	Connects P005 (AN001) to Grove 2 pin 2
E42	Grove 2	Open	Connects P002 (AN102) to Grove 2 pin 1
E43	Arduino	Closed	Connects VREFH to the Arduino AREF pin
E44	Debugger	Open	Connects P304 to J20 pin 20
E45	Debugger	Open	Connects P305 to J20 pin 18
E46	Debugger	Open	Connects P306 to J20 pin 16
E47	Debugger	Open	Connects P307 to J20 pin 14
E48	Debugger	Open	Connects P308 to J20 pin 12
E49	MCU Power	Closed	Connects VBATT to +3.3_MCU
E50	SDRAM	Closed	Connects P115 to SDRAM_CS_L
E51	Pin Headers	Open	Connects P210 to J4 pin 4
E52	Pin Headers	Open	Connects P211 to J4 pin 6

4.3.4 Default Switch Configuration

The EK-RA8E2 features an I^2C I/O Port Expander (PI4IOE5V6408) at U15 and has the I^2C address 0x43. The port expander is connected to the configuration switches SW4.

The following table describes the function and default configuration for each switch that selects the operational peripheral pins on the EK-RA8E2 board.

The Circuit Group for each switch is the designation found in the board schematic (available in the Design Package). Functional details for many of the listed switches may be found in sections associated with each functional area of the kits.

Table 3. Switch Configuration Definitions (SW4)

Switch	Switch Definition	Position (Default)	Function	Conflict
SW4-1	Pmod 1 Mode Select 1	**OFF**	Please see Table 16	Please see Table 16
		ON		
SW4-2	Pmod 1 Mode Select 2	**OFF**		
		ON		
SW4-3	Octo-SPI Select	**OFF**	Octo-SPI Active	Pmod 1 (SPI and UART)
		ON	Octo-SPI Inactive	-
SW4-4	Pmod 2 Mode Select	**OFF**	SPI mode selected	-
		ON	UART mode selected	-
SW4-5	Test Point 5	**OFF**	Connect Test Point 5 to +3.3 V	-
		ON	Connect Test Point 5 to GND	-
SW4-6	Test Point 6	**OFF**	Connect Test Point 6 to +3.3 V	-
		ON	Connect Test Point 6 to GND	-
SW4-7	USBFS Role Toggle	**OFF**	Toggles USBFS between Host and Device mode	-
		ON		-
SW4-8	Not Connected	**OFF**	-	-
		ON		-

Note: There are no conflicting settings for SW4.

5. System Control and Ecosystem Access Area

The following figure shows the System Control and Ecosystem Access area on the EK-RA8E2 board. Subsequent sections detail the features and functionality provided in the area.

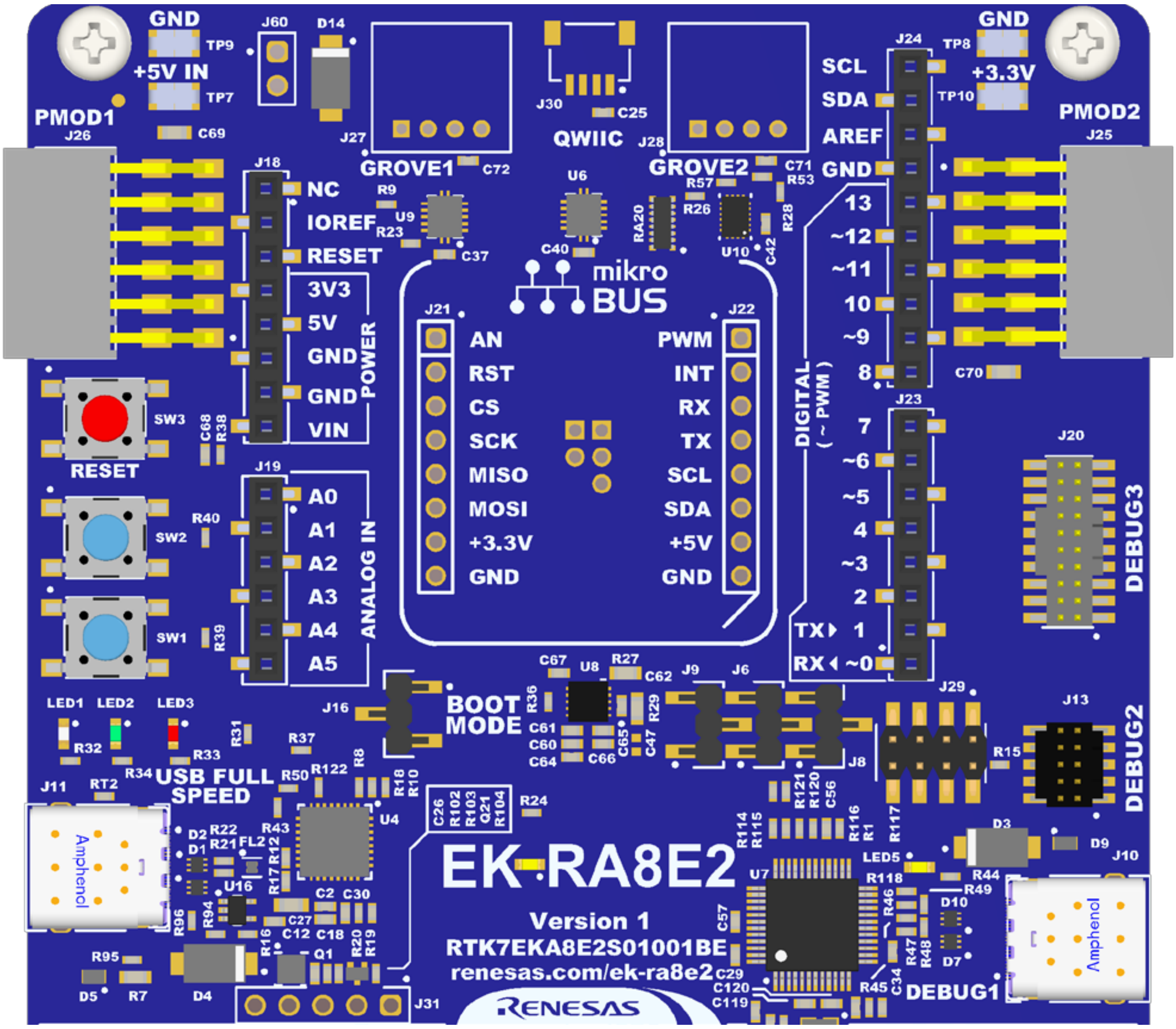

Figure 7. System Control and Ecosystem Access Area

5.1 Power

The EK-RA8E2 kit is designed for +5 V operation. An on-board Low Dropout Regulator (ISL80103IRAJZ) is used to convert the 5 V supply to a 3.3 V supply. The +3.3 V supply is used to power the RA MCU and other peripheral features.

5.1.1 Power Supply Options

This section describes the different ways in which EK-RA8E2 kit can be powered.

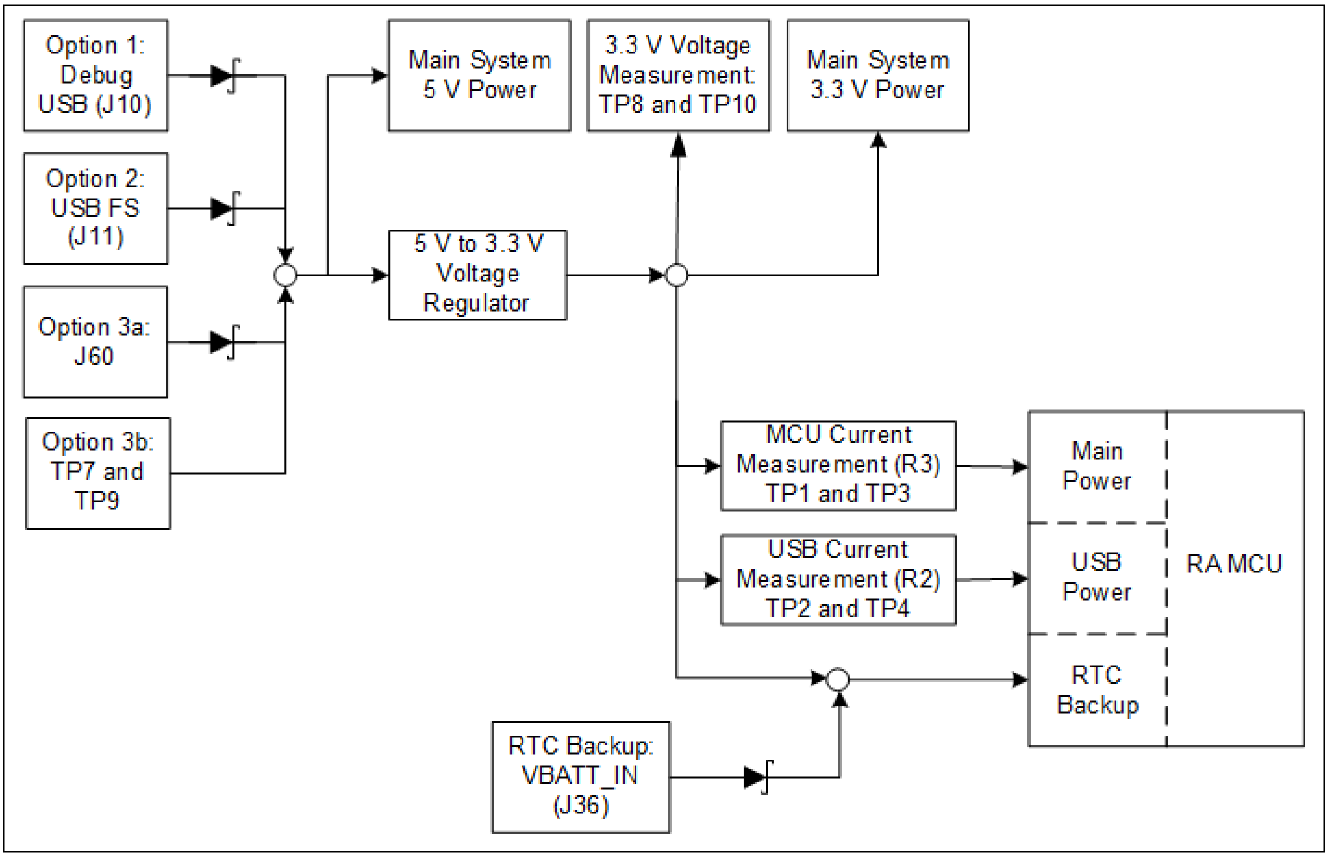

Figure 8. Power Supply Options

5.1.1.1 Option 1: Debug USB

5 V may be supplied from an external USB host to the USB Debug connector (J10) labelled DEBUG1 on the board. Power from this source is connected to the main system 5 V power. Reverse current protection is provided between this connector and the main system 5 V power.

5.1.1.2 Option 2: USB Full Speed

5 V may be supplied from an external USB host to the USB Full Speed connector (J11) labelled USB FULL SPEED on the board. Power from this source is connected to the main system 5 V power. Reverse current protection is provided between this connector and the main system 5 V power.

5.1.1.3 Option 3: 5 V Test Points

5 V may be supplied from an external power supply to test points on the board. TP7 (5 V) and TP9 (GND) are loop-style test points, and J60 provides large via style test points that can accommodate a 0.1” pin header or connector. The two types of test points are electrically equivalent, and both are provided for user convenience. Power from this source is connected to the main system 5 V power. These test points can be found at the top left of the board above Pmod1.

Reverse current protection is provided at J60-1, whereas TP7 directly connects to the 5V input pin of the voltage regulator U8 and to the Main System 5V Power. Care must be taken before applying an external supply to this test point to ensure that that the polarity is correct. Failure to do so could result in damage to components on the PCB.

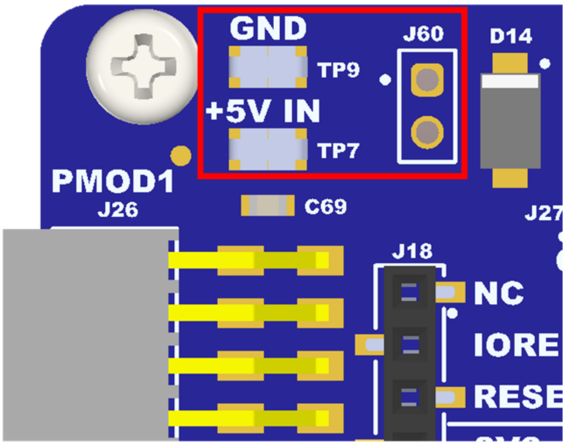

Figure 9. Test Point Location

5.1.1.4 RTC Backup: VBATT Supply

The MCU provides a battery backup function that maintains power to certain MCU peripherals in the event of a power loss (for example the Real Time Clock). A battery (lithium coin cell etc.) can be connected to J36 (not fitted) to provide this power. For further details see the MCU hardware manual.

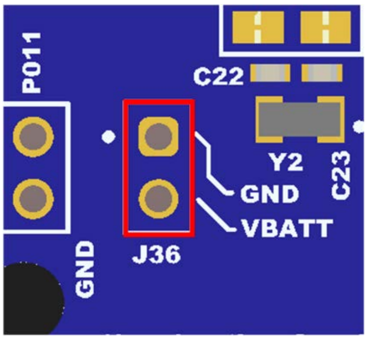

Figure 10. VBATT supply (J36) Location

5.1.2 Power Supply Considerations

The on-board LDO regulator which supplies +3.3 V has a built-in current limit of 3.0 A. Make sure the total current required by the RA MCU, any active on-board features, and any connected peripheral devices does not exceed this limit.

Note: The total current available from a typical enumerated USB host is 500 mA maximum. Depending on the configuration of the kit, multiple power sources may be required.

5.1.3 Power-up Behavior

When powered, the white LED near the center of the board (the “dash” in the EK-RA8E2 name) will light up. For more details on initial power up behavior, see the *EK-RA8E2 Quick Start Guide*.

5.2 Debug and Trace

The EK-RA8E2 board supports the following three debug modes.

Table 4. Debug Modes

Debug Modes	Debugger MCU (the device that connects to the IDE on PC)	Target MCU (the device that is being debugged)	Debugging Interface/Protocol	Connector Used
Debug on-board	RA4M2 (on-board)	RA8E2 (on-board)	SWD, JTAG	USB-C (J10)
Debug in	External debugging tools	RA8E2 (on-board)	SWD, SWO, ETM, JTAG	20-pin connector (J20) or 10-pin connector (J13)
Debug out	RA4M2 (on-board)	Any external RA MCU	SWD, SWO, JTAG	USB-C (J10) plus either 20-pin connector (J20) or 10-pin connector (J13)

Notes:

- See Table 6 for the Debug USB connector pin definition.
- See Table 9 for the 20-pin JTAG connector pin definition.
- See Table 10 for the 10-pin JTAG connector pin definition.

The following table summarizes the jumper configuration for each of the debug modes.

Table 5. Jumper Connection Summary for Different Debug Modes

Debug Modes	J8	J9	J29
Debug on-board	Jumper on pins 1-2	Jumper on pins 2-3	Jumpers on pins 1-2, 3-4, 5-6, 7-8
Debug in	Jumper on pins 1-2	Jumper on pins 1-2	Jumpers on pins 1-2, 3-4, 5-6, 7-8
Debug out	Jumper on pins 2-3	Jumper on pins 2-3	All pins open

5.2.1 Debug On-Board

The on-board debug functionality is provided using Renesas RA4M2 Debug MCU and SEGGER J-Link® firmware. Debug USB-C connector (J10) connects the RA4M2 Debug MCU to an external USB Full Speed Host, allowing re-programming and debugging of the target RA MCU firmware. This connection is the default debug mode for the EK-RA8E2 board.

The RA4M2 Debug MCU connects to the target RA MCU using the SWD interface or the JTAG interface.

Table 6. Debug USB Port Assignments

Debug USB Port Assignments		EK-RA8E2
Pin	**Description**	**Signal/Bus**
J10-A1	GND	GND
J10-A2	TX1+	N.C.
J10-A3	TX1-	N.C.
J10-A4	VBUS	+5V_USB_DBG
J10-A5	CC1	USB_JLOB_CC1
J10-A6	DA+	USB_JLOB_P
J10-A7	DA-	USB_JLOB_N
J10-A8	SBU1	N.C.
J10-A9	VBUS	+5V_USB_DBG
J10-A10	RX2-	N.C.
J10-A11	RX2+	N.C.
J10-A12	GND	GND
J10-B1	GND	GND

Debug USB Port Assignments		**EK-RA8E2**
Pin	**Description**	**Signal/Bus**
J10-B2	TX2+	N.C.
J10-B3	TX2-	N.C.
J10-B4	VBUS	+5V_USB_DBG
J10-B5	CC2	USB_JLOB_CC2
J10-B6	DB+	USB_JLOB_P
J10-B7	DB-	USB_JLOB_N
J10-B8	SBU2	N.C.
J10-B9	VBUS	+5V_USB_DBG
J10-B10	RX1-	N.C.
J10-B11	RX1+	N.C.
J10-B12	GND	GND
J10-S1	SHIELD	GND
J10-S2	SHIELD	GND
J10-S3	SHIELD	GND
J10-S4	SHIELD	GND

A yellow indicator, LED5, shows the visual status of the debug interface. When the EK-RA8E2 board is powered on, and LED5 is blinking, it indicates that the RA4M2 Debug MCU is not connected to a programming host. When LED5 is on solid, it indicates that the RA4M2 Debug MCU is connected to a programming interface.

To configure the EK-RA8E2 board to use the Debug On-Board mode, configure the jumpers using the following table.

Table 7. Debug On-Board Jumper Configuration

Location	Default Open/Closed	Function
J8	Jumper on pins 1-2	Target RA MCU RESET_L connected to debugger JTAG_RESET_L
J9	Jumper on pins 2-3	RA4M2 Debug MCU in normal operation mode
J29	Jumpers on pins 1-2, 3-4, 5-6, 7-8	Target RA MCU debug signals connected to the debugger interface

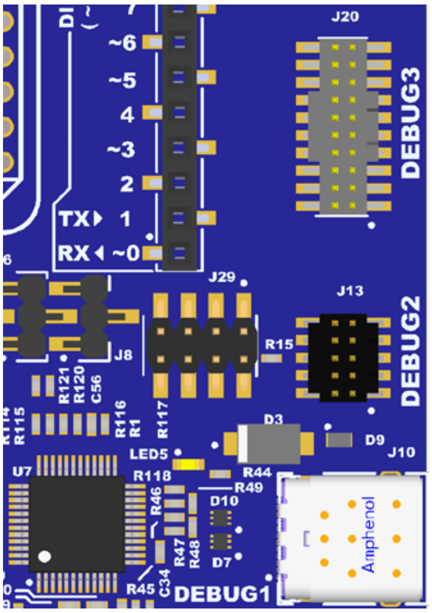

Figure 11. EK-RA8E2 Debug Interface

5.2.2 Debug In

One 20-pin Cortex® Debug Connector at J20 supports JTAG, SWD, SWO and ETM (TRACE) debug. One 10-pin Cortex® Debug Connector at J13 supports JTAG, SWD and SWO. Either of these connectors may be used for external debug of the target RA MCU.

To configure the EK-RA8E2 board to use the Debug In mode, configure the jumpers as shown in Table 8.

Table 8. Debug In Mode Jumper Configuration

Location	Default Open/Closed	Function
J8	Jumper on pins 1-2	Target RA MCU RESET_L connected to debug RESET_L
J9	Jumper on pins 1-2	RA4M2 Debug MCU is held in RESET
J29	Jumpers on pins 1-2, 3-4, 5-6, 7-8	Target RA MCU debug signals connected to the debug interface

Table 9. JTAG/SWO/SWD/ETM Debug Port Assignments

JTAG Port Assignments				EK-RA8E2
Pin	**JTAG Pin Name**	**SWD Pin Name**	**ETM Pin Name**	**Signal/Bus**
J20-1	Vtref	Vtref	Vtref	+3V3
J20-2	TMS	SWDIO	TMS / SWDIO	P210 / SWDIO / TMS
J20-3	GND	GND	GND	GND
J20-4	TCK	SWCLK	TCK / SWCLK	P211 / SWCLK / TCK
J20-5	GND	GND	GND	GND
J20-6	TDO	SWO	TDO / SWO	P209 / TDO
J20-7	Key	Key	Key	N.C.
J20-8	TDI	N/A	TDI / N/A	P208 / TDI
J20-9	GNDDetect	GNDDetect	GNDDetect	GND (cut E30 to open)
J20-10	nSRST	nSRST	nSRST	RESET_L
J20-11	GND	GND	GND	GND
J20-12	N/A	N/A	TCLK	P308 / TCLK*
J20-13	GND	GND	GND	GND
J20-14	N/A	N/A	TDATA0	P307 / TDATA0*
J20-15	GND	GND	GND	GND
J20-16	N/A	N/A	TDATA1	P306 / TDATA1*
J20-17	GND	GND	GND	GND
J20-18	N/A	N/A	TDATA2	P305 / TDATA2*
J20-19	GND	GND	GND	GND
J20-20	N/A	N/A	TDATA3	P304 / TDATA3*

* Option to Isolate with E pad

Table 10. JTAG/SWO/SWD Debug Port Assignments

JTAG Port Assignments			EK-RA8E2
Pin	**JTAG Pin Name**	**SWD Pin Name**	**Signal/Bus**
J13-1	Vtref	Vtref	+3V3
J13-2	TMS	SWDIO	P210/SWDIO/TMS
J13-3	GND	GND	GND
J13-4	TCK	SWCLK	P211/SWCLK/TCK
J13-5	GND	GND	GND
J13-6	TDO	SWO	P209/TDO
J13-7	Key	Key	N.C.
J13-8	TDI	N/A	P208/TDI
J13-9	GNDDetect	GNDDetect	GND (cut E30 to open)
J13-10	nSRST	nSRST	RESET_L

Note: The Cortex® Debug Connector is fully described in the Arm® CoreSight™ Architecture Specification.

5.2.3 Debug Out

The EK-RA8E2 board can be configured to use the RA4M2 Debug MCU to debug target RA MCU on an external board.

A yellow indicator, LED5, shows the visual status of the debug interface. When the EK-RA8E2 board is powered on, and LED5 is blinking, this indicates that the RA4M2 Debug MCU is not connected to a programming host. When LED5 is on solid, this indicates that the RA4M2 Debug MCU is connected to a programming interface. When the debug interface is actively in use, the LED will flicker randomly.

To configure the EK-RA8E2 board to use the Debug Out mode, configure the jumpers according to the following table.

Table 11. Debug Out Jumper Configuration

Location	Default Open/Closed	Function
J8	Jumper on pins 2-3	On-board RA MCU is held in RESET
J9	Jumper on pins 2-3	RA4M2 Debug MCU in normal operation mode
J29	All jumpers removed	Disconnects the on-board RA MCU debug signals from the Debug Interface

5.3 Ecosystem

The System Control and Ecosystem area provides users the option to simultaneously connect several third-party add-on modules compatible with five most popular ecosystems using the following connectors:

1. Two Seeed Grove® system (I^2C /Analog) connectors (not populated)
2. SparkFun® Qwiic® connector (not populated)
3. Two Digilent Pmod™ (SPI, UART and I^2C) connectors
4. Arduino™ (Uno R3) connector
5. MikroElektronika™ mikroBUS connector (not populated)

5.3.1 Seeed Grove® Connectors

5.3.1.1 Grove 1

A Seeed Grove® I^2C connector footprint is provided at J27. The RA MCU acts as a two-wire serial master, and a connected module acts as a two-wire serial slave.

Table 12. Grove 1 Port Assignments

Grove 1 Connector		EK-RA8E2
Pin	**Description**	**Signal/Bus**
J27-1	SCL	P410 (SCL0)
J27-2	SDA	P409 (SDA0)
J27-3	VCC	+3.3 V
J27-4	GND	GND

5.3.1.2 Grove 2

A Seeed Grove® I^2C connector footprint is provided at J28. The RA MCU acts as a two-wire serial master, and a connected module acts as a two-wire serial slave.

Option links E39, E40, E41 and E42 provide the capability to convert this connector to an analog Seeed Grove® implementation.

Table 13. Grove 2 Port Assignments

Grove 2 Connector		EK-RA8E2	
Pin	**Description**	**Signal/Bus**	
J28-1	I2C_SCL	P512 (SCL1) *1	P002(AN102) *2
J28-2	I2C_SDA	P511 (SDA1) *1	P005(AN001) *2
J28-3	VCC	+3.3 V	
J28-4	GND	GND	

[*1] Jumpers E39 and E40 are closed, E41 and E42 are open
[*2] Jumpers E39 and E40 are open, E41 and E42 are closed

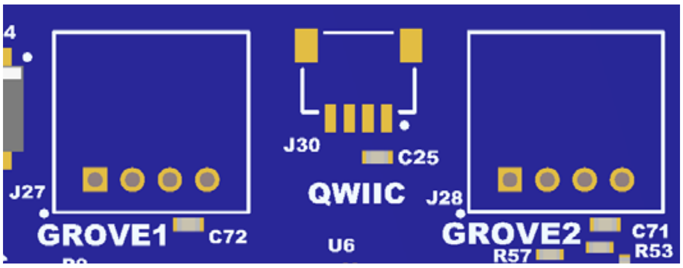

Figure 12. Seeed Grove® and SparkFun® Qwiic® Connector Footprints

5.3.2 SparkFun® Qwiic® Connector

A SparkFun® Qwiic® connector footprint is provided at J30. The main MCU acts as a two-wire serial master, and a connected module acts as a two-wire serial slave (data lines shared with Grove 2).

Table 14. Qwiic Port Assignments

Qwiic Connector		EK-RA8E2
Pin	**Description**	**Signal/Bus**
J30-1	GND	GND
J30-2	VCC	+3.3 V
J30-3	SDA	P409 (SDA0)
J30-4	SCL	P410 (SCL0)

5.3.3 Digilent Pmod™ Connectors

Two 12-pin connectors are provided to support Pmod modules where the RA MCU acts as the master, and the connected module acts as a slave device.

These interfaces may be configured in firmware to support several Pmod types such as Type-2A (expanded SPI), Type-3A (expanded UART) and Type-6A (I^2C). Configured using SW4-1 and SW4-2 for Pmod 1 and SW4-4 for Pmod 2. These options are also configurable in software using the IO expander (U15).

The default 12-pin Pmod interface supports +3.3 V devices. Please ensure that any Pmod device installed is compatible with a +3.3 V supply.

Note: Both Pmods use the SCI peripheral in “Simple SPI” mode and so do not offer the full functionality of the SPI peripheral. Please see the hardware manual for full details of the SCI “Simple SPI” mode.

5.3.3.1 Pmod 1

A 12-pin Pmod connector is provided at J26, Pmod 1.

Table 15. Pmod 1 Port Assignments

Pmod 1 Connector				EK-RA8E2
Pin	**Option Type-2A (SPI)** [*1]	**Option Type-3A (UART)** [*1]	**Option Type-6A (I^2C)** [*1]	**Signal/Bus**
J26-1	SS			PA05 (SS2)
		CTS		PA06 (CTS2)
			IRQ	P206 (IRQ0-DS)
J26-2	MOSI	TXD		PA03 (MOSI2/TXD2)
			RESET	P408 (GPIO)
J26-3	MISO	RXD		PA02 (MISO2/RXD2)
			SCL	P512 (SCL1)

Pmod 1 Connector				**EK-RA8E2**
J26-4	SCK			PA04 (SCK2)
		RTS		PA05 (RTS2)
			SDA	P511 (SDA1)
J26-5	GND			GND
J26-6	VCC			+3.3 V (close E25, open E35)
				+5.0 V (close E35, open E25)
J26-7	IRQ			P006 (IRQ11-DS)
J26-8	RESET (master to slave)			PA11
J26-9	GPIO			PA12
J26-10	GPIO			PA13
J26-11	GND			GND
J26-12	VCC			+3.3 V (close E25, open E35)
				+5.0 V (close E35, open E25)

[1] Option is selected by setting switches SW4-1 and SW4-2 as follows:

Table 16. Pmod 1 Function Selection

SW4-1	SW4-2	Selected function	Conflict
Off	Off	SPI	Octo-SPI
On	Off	UART	Octo-SPI
Off	On	I^2C	-
On	On	Invalid	Invalid

Caution: 5 V optional supply is provided (J26-6 and J26-12), however the interface must only be driven with 3.3 V signals from the Pmod 1. The EK-RA8E2 will only provide 3.3 V signal levels to the Pmod 1.

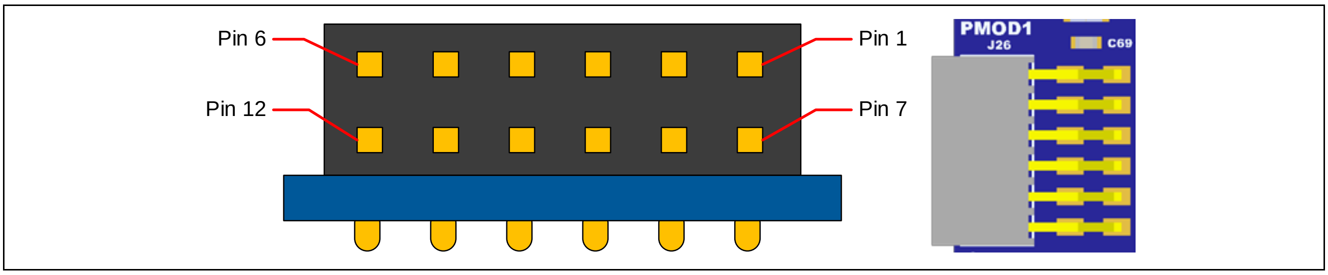

Figure 13. Pmod 1 Connector

5.3.3.2 Pmod 2

A 12-pin Pmod connector is provided at J25, Pmod 2.

Table 17. Pmod 2 Port Assignments

Pmod 2 Connector			**EK-RA8E2**
Pin	**Option Type-2A (SPI)** [1]	**Option Type-3A (UART)** [1]	**Signal/Bus**
J25-1	SS		P314 (SS3)
J25-1		CTS	P313 (CTS3)
J25-2	MOSI	TXD	P900 (MOSI3/TXD3)
J25-3	MISO	RXD	P901(MISO3/RXD3)
J25-4	SCK		P315 (SCK3)
J25-4		RTS	P314 (RTS3)
J25-5	GND		GND
J25-6	VCC		+3.3 V
J25-7	IRQ		P508 (IRQ1)

Pmod 2 Connector			**EK-RA8E2**
Pin	**Option Type-2A (SPI)** [*1]	**Option Type-3A (UART)** [*1]	**Signal/Bus**
J25-8	GPIO		P809
J25-9	GPIO		P810
J25-10	GPIO		P811
J25-11	GND		GND
J25-12	VCC		+3.3 V

[*1] If using Type-2A (SPI), SW4-4 is OFF
If using Type-3A (UART), SW4-4 is ON

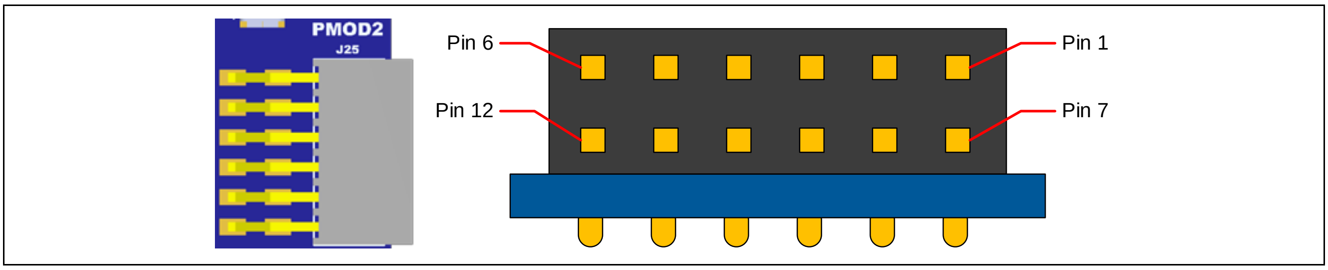

Figure 14. Pmod 2 Connector

5.3.4 Arduino™ Connector

Near the center of the System Control and Ecosystem Access area is an Arduino™ Uno R3 compatible connector interface.

Table 18. Arduino Uno Port Assignments

Arduino Compatible Connectors				**EK-RA8E2**
Pin	**Description**			**Signal/Bus**
J18-1	N.C.			N.C.
J18-2	IOREF			+3.3 V
J18-3	RESET			RESET_L (ARDUINO_RESET_L)
J18-4	3.3 V			+3.3 V
J18-5	5 V			+5 V
J18-6	GND			GND
J18-7	GND			GND
J18-8	VIN			N.C.
J19-1	A0			P009 (AN006)
J19-2	A1			P007 (AN004)
J19-3	A2			P003 (AN104)
J19-4	A3			P004 (AN000)
J19-5	A4			P014 (AN007/DA0)
J19-6	A5			P015 (AN015)
J23-1	D0	RX		P401 (RXD1/IRQ5-DS)
J23-2	D1	TX		P400 (TXD1/IRQ0)
J23-3	D2	INT0		P509 (IRQ2)
J23-4	D3	INT1	PWM	P202 (GPIO / IRQ3-DS / GTIOC5B)
J23-5	D4			P506 (GPIO)
J23-6	D5		PWM	P403 (GPIO / IRQ14-DS / GTIOC3A)
J23-7	D6		PWM	P203 (GPIO / IRQ2-DS / GTIOC5A)
J23-8	D7			P504 (GPIO)
J24-1	D8			P505 (GPIO)
J24-2	D9		PWM	P204 (GPIO / GTIOC4B)

Arduino Compatible Connectors				EK-RA8E2
Pin	**Description**			**Signal/Bus**
J24-3	D10	SPI_SS		P703 (SSLA)
J24-4	D11	SPI_MOSI	PWM	P701 (MOSIA/GTIOC5B)
J24-5	D12	SPI_MISO	PWM	P700 (MISOA/GTIOC5A)
J24-6	D13	SPI_SCK		P702 (RSPCKA)
J24-7	GND			GND
J24-8	ARDUINO_AREF			+3.3 V
J24-9	SDA			P409/SDA0 (SDA0)
J24-10	SCL			P410/SCL0 (SCL0)

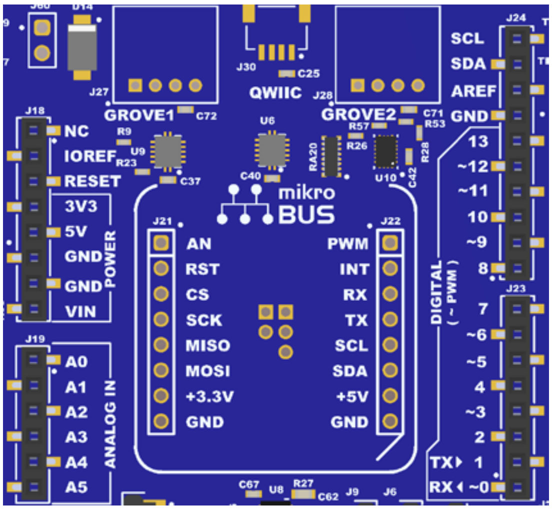

Figure 15. Arduino Uno Connectors

5.3.5 MikroElektronika™ mikroBUS Connector

In the center of the System Control and Ecosystem Access area is a mikroBUS compatible connector footprint. This interface is compliant with mikroBUS Standard Specifications revision 2.00.

Table 19. mikroBUS Assignments

mikroBUS Connectors		EK-RA8E2
Pin	**Description**	**Signal/Bus**
J21-1	AN (Analog)	P004 (AN000)
J21-2	RST (Reset)	P507 (MIKROBUS RESET_L)
J21-3	CS (SPI Chip Select)	P703 (SSLA0)
J21-4	SCK (SPI Clock)	P702 (RSPCKA)
J21-5	MISO	P700 (MISOA)
J21-6	MOSI	P701 (MOSIA)
J21-7	+3.3 V	+3.3 V
J21-8	GND	GND
J22-1	PWM	P403 (GTIOC3A)
J22-2	INT (Hardware Interrupt)	P010 (IRQ14)
J22-3	RX (UART Receive)	P401 (RXD1)
J22-4	TX (UART Transmit)	P400 (TXD1)
J22-5	SCL	P410/SCL0 (SCL0)
J22-6	SDA	P409/SDA0 (SDA0)
J22-7	+5 V	+5 V
J22-8	GND	GND

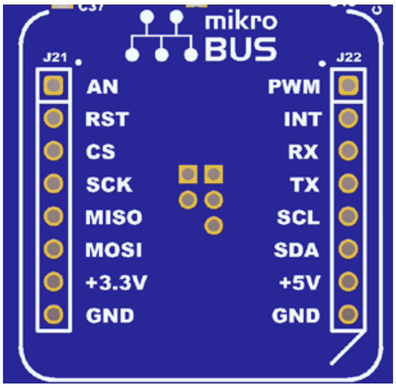

Figure 16. mikroBUS Connector

5.4 Connectivity

5.4.1 USB Full Speed

The USB-C connection jack (J11) connects the RA MCU USB Full Speed interface to an external USB interface, allowing communications for testing and use of the RA MCU firmware. This connection can be configured as either a USB device or a USB host interface.

For a USB Device configuration, set P500 to low and configure the RA MCU firmware to use the USB Full Speed ports in device mode. Power from an external USB Host on this connection can be used to provide power to the EK-RA8E2 board.

For a USB Host configuration, set P500 to high and configure the RA MCU firmware to use the USB Full Speed ports in host mode. In this configuration, power to J11 is supplied from U4. The total current available is 2 A. Note that the input power sources must be configured with enough power for both the EK-RA8E2 board and the USB Full Speed port in host mode. Connect a USB type-A female to USB-C male cable to J11. USB device cables or devices can be connected to the USB Full Speed port using this cable.

Table 20. USB Full Speed Port Assignments

USB Full Speed Connector		**EK-RA8E2**
Pin	**Description**	**Signal/Bus**
J11-A1	GND	GND
J11-A2	TX1+	N.C.
J11-A3	TX1-	N.C.
J11-A4	VBUS	USBFS_cVBUS_CON
J11-A5	CC1	USB_FS_CC1
J11-A6	DA+	USBF_P
J11-A7	DA-	USBF_N
J11-A8	SBU1	N.C.
J11-A9	VBUS	USBFS_cVBUS_CON
J11-A10	RX2-	N.C.
J11-A11	RX2+	N.C.
J11-A12	GND	GND
J11-B1	GND	GND
J11-B2	TX2+	N.C.
J11-B3	TX2-	N.C.
J11-B4	VBUS	USBFS_cVBUS_CON
J11-B5	CC2	USB_FS_CC2
J11-B6	DB+	USBFS_P
J11-B7	DB-	USBFS_N
J11-B8	SBU2	N.C.
J11-B9	VBUS	USBFS_cVBUS_CON
J11-B10	RX1-	N.C.
J11-B11	RX1+	N.C.
J11-B12	GND	GND

USB Full Speed Connector		EK-RA8E2
Pin	**Description**	**Signal/Bus**
J11-S1	SHIELD	GND
J11-S2	SHIELD	GND
J11-S3	SHIELD	GND
J11-S4	SHIELD	GND

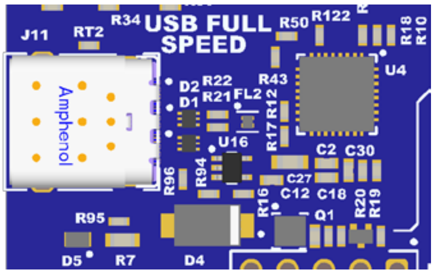

Figure 17. USB Full Speed Connector

5.5 Miscellaneous

5.5.1 User and Power LEDs

Five LEDs are provided on the EK-RA8E2 board.

Behavior of the LEDs on the EK-RA8E2 board is described in the following table.

Table 21. EK-RA8E2 Board LED Functions

Designator	Color	Function	MCU Control Port
LED1	Blue	User LED	P205
LED2	Green	User LED	P406
LED3	Red	User LED	P405
LED4	White	Power on indicator	+3.3 V
LED5	Yellow	Debug LED	+5V_USB_DBG

The user LEDs may be isolated from the main MCU, so the associated ports can be used for other purposes. To separate LED1 from P205, trace cut jumper E27 must be open. To separate LED2 from P406, trace cut jumper E26 must be open. To separate LED3 from P405, trace cut jumper E28 must be open.

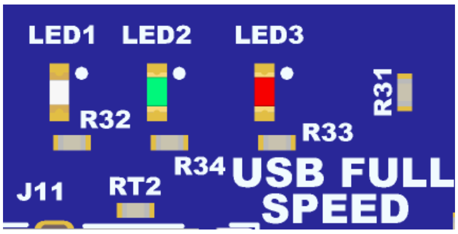

Figure 18. User LEDs

Figure 19. Power LED

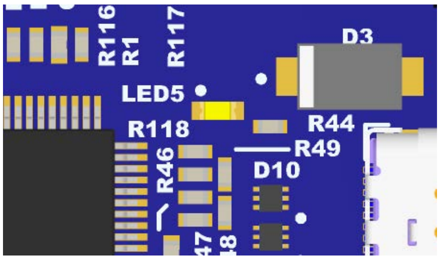

Figure 20. Debug LED

5.5.2 User and Reset Switches

Three miniature, momentary, mechanical push-button type SMT switches are mounted on the EK-RA8E2 board.

Pressing the reset switch (SW3) generates a reset signal to restart the RA MCU.

Table 22. EK-RA8E2 Board Switches

Designator	Function	MCU Control Port	Button Color
SW3	MCU Reset Switch	RESET_L	Red
SW2	User Switch	P008 (IRQ12-DS)	Blue
SW1	User Switch	P001 (IRQ7-DS)	Blue

The user switches SW1 and SW2 may be isolated from the main MCU, so the associated ports can be used for other purposes. To separate SW1 from P001, trace cut jumper E31 must be open. To separate SW2 from P008, trace cut jumper E32 must be open.

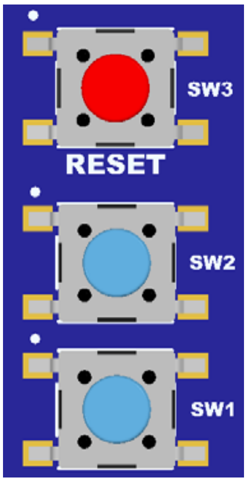

Figure 21. Reset and User Switches

5.5.3 MCU Boot Mode

A three-pin header (J16) is provided to select the boot mode (P201/MD) of the RA MCU. For normal operation, or Single-Chip mode, place jumper on J16 2-3. To enter SCI Boot mode or USB boot mode, place a jumper on J16 1-2.

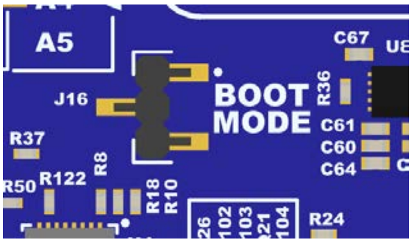

Figure 22. Boot Mode

6. Special Feature Access Area

Note: Normally the SDRAM and Octo-SPI devices would be in this area, however, to optimize the layout for this high-speed device, these components have been placed in the MCU Native Pin Access area.

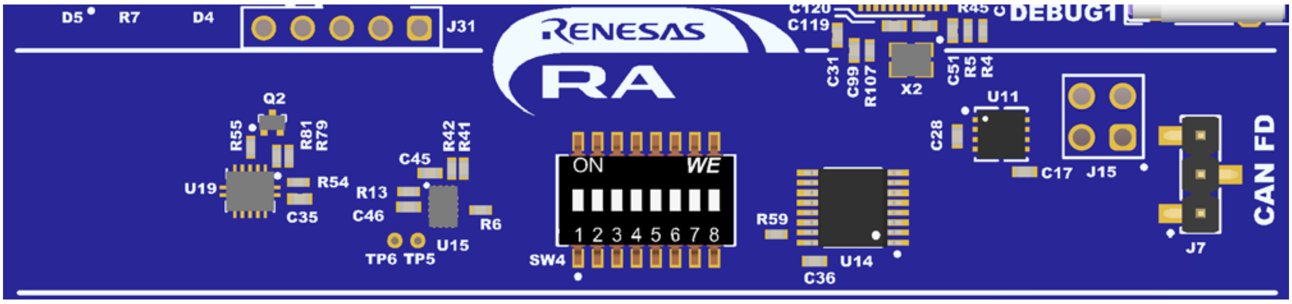

Figure 23. Special Feature Access Area

6.1 Octo-SPI Flash

Included on the EK-RA8E2 board is a 512 Mb (64 MB) Octo-SPI serial NOR flash memory (MX25LW51245GXDI00-T). The Octo-SPI serial NOR flash device (U3) connects to the Octo-SPI peripheral on the RA MCU and defaults to standard SPI mode initially. The NOR flash memory is enabled for XIP (Execute-In-Place) mode directly after power-on.

The Octo-SPI signals are not provided on an external pin header due to the high speed of this interface.

Table 23. Octo-SPI Flash Assignments

Octo-SPI Flash Signal Description	EK-RA8E2
OSPI_FLASH_RESET_L	P106
OSPI_FLASH_IRQ_L	P105
OSPI_FLASH_CLK	P808
OSPI_FLASH_CS_L	P104
OSPI_FLASH_DQS	P801
OSPI_FLASH _SIO0	P100
OSPI_FLASH _SIO1	P803
OSPI_FLASH _SIO2	P103
OSPI_FLASH _SIO3	P101
OSPI_FLASH _SIO4	P102
OSPI_FLASH _SIO5	P800
OSPI_FLASH _SIO6	P802
OSPI_FLASH _SIO7	P804

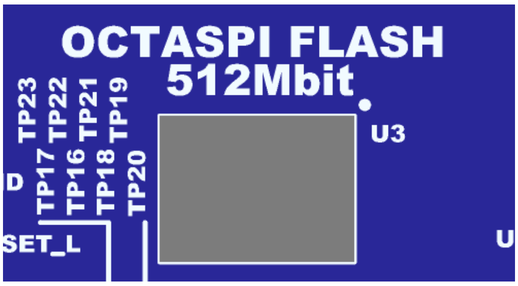

Figure 24. Octo-SPI Flash

6.1.1 OSPI Flash Read / Write Byte Order

The MX25LW51245GXDI00 flash device uses the byte order shown in Figure 25 below (taken from the Macronix MX25LW51245G data sheet) when writing or reading data in DOPI mode.

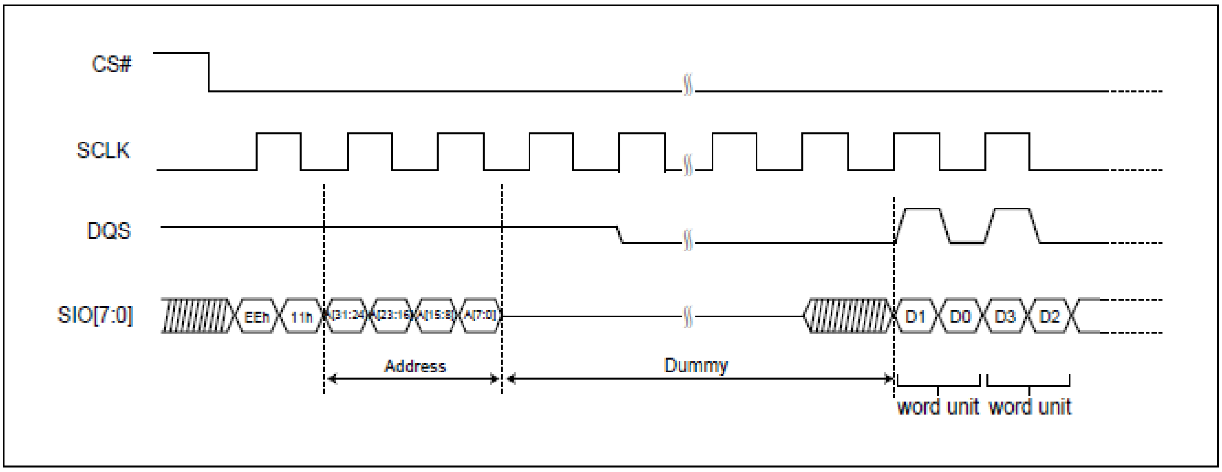

Figure 25. Octo-SPI Flash Read Write Byte Order in DOPI mode

This order (D1, D0, D3, D2 ...) differs from the order that is used when reading or writing data in SPI mode (D0, D1, D2, D3, …). The mode used for reading data must be the same as the mode used for writing data therefore, this must be taken into consideration.

6.2 SDRAM

Included in the EK-RA8E2 board is a 512 Mb (64 MB organized as 32M x 16 bits) SDRAM (IS42S16320F–6BLI) (U2). The SDRAM pins are accessible through J14 and J37 pin headers (not fitted).

Table 24. SDRAM Assignments

SDRAM Description	EK-RA8E2 Signal/Bus
SDRAM_A0	P300
SDRAM_A1	P301
SDRAM_A2	P302
SDRAM_A3	P303
SDRAM_A4	P304
SDRAM_A5	P305
SDRAM_A6	P306
SDRAM_A7	P307
SDRAM_A8	P308
SDRAM_A9	P309
SDRAM_A10	P310
SDRAM_A11	P311
SDRAM_A12	P312
SDRAM_BA0	P905
SDRAM_BA1	P906
SDRAM_DQ0	P601
SDRAM_DQ1	P602
SDRAM_DQ2	P603
SDRAM_DQ3	P604
SDRAM_DQ4	P605
SDRAM_DQ5	P606
SDRAM_DQ6	P607

SDRAM	**EK-RA8E2**
Description	**Signal/Bus**
SDRAM_DQ7	PA00
SDRAM_DQ8	P609
SDRAM_DQ9	P610
SDRAM_DQ10	P611
SDRAM_DQ11	P612
SDRAM_DQ12	P613
SDRAM_DQ13	P614
SDRAM_DQ14	P615
SDRAM_DQ15	PA08
SDRAM_CKE	P113
SDRAM_CLK	PA09
SDRAM_DQMH	P112
SDRAM_DQML	PA10
SDRAM_WE_L	P114
SDRAM_CAS_L	P909
SDRAM_RAS_L	P908
SDRAM_CS_L	P115

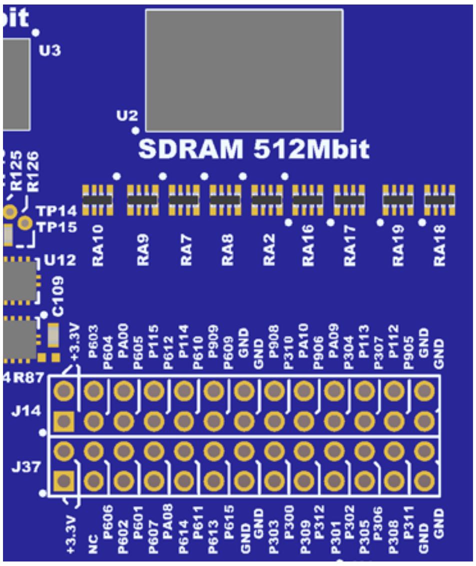

Figure 26. SDRAM

6.3 CAN-FD Bus

The EK-RA8E2 board provides a CAN-FD bus transceiver (MCP2558FDT–H/MF)(U11) that is connected directly to the RA MCU. External connection to the CAN-FD bus is made using the 0.1” pitch 3-pin male header J7.

Resistors R30 and R35 comprise the 60.4 Ohm termination resistors needed on a CAN network. To remove these resistors, remove links E18 and E19. To reattach these resistors, link 1-2 and 3-4 on the not fitted connector J15.

Table 25. CAN FD Bus Connections Between U11 and RA8E2

CAN FD Signal Description	EK-RA8E2 Port
TXD	P704
RXD	P705
S	P706

Table 26. CAN FD Port Assignments

CAN FD Connector (J7)	Function
1	CAN-FD_H
2	CAN-FD_L
3	GND

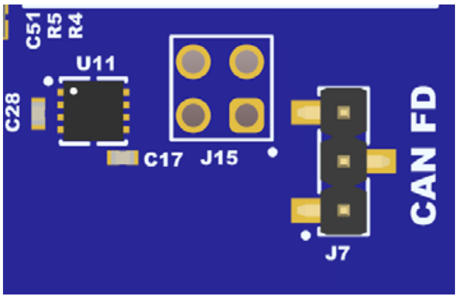

Figure 27. CAN FD Connector and Chip

7. MCU Native Pin Access Area

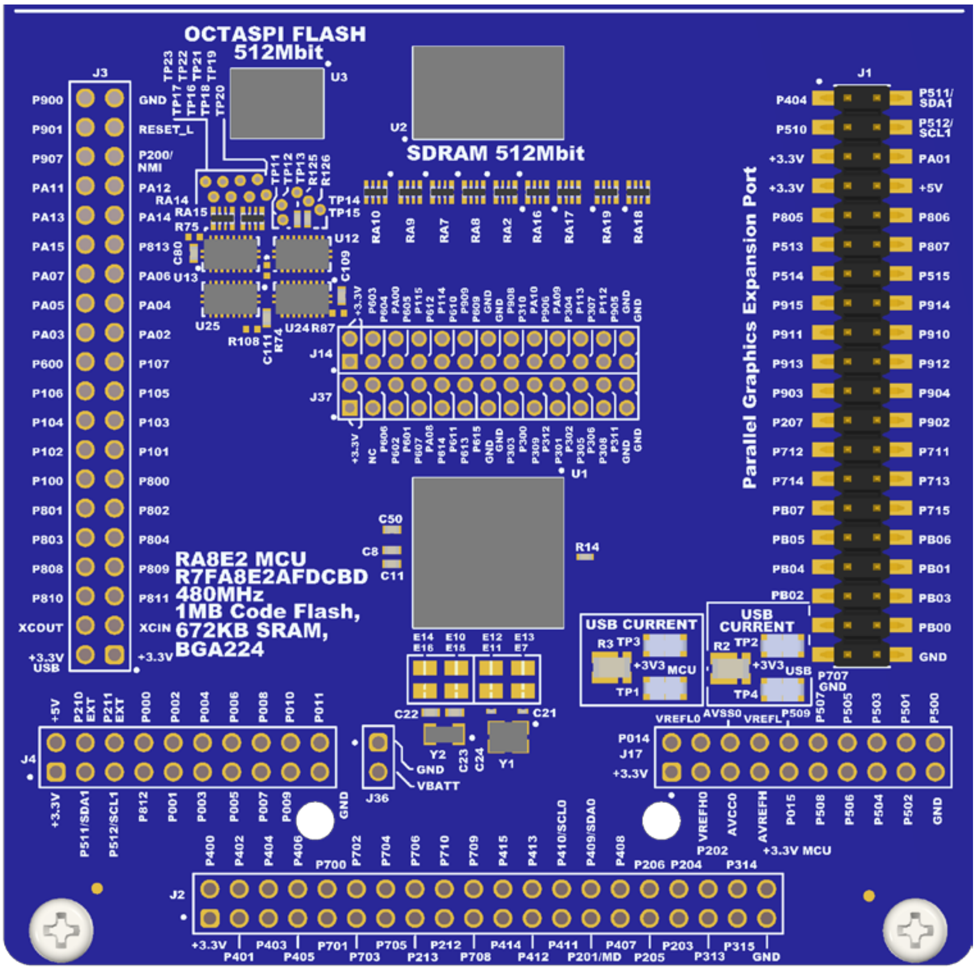

Figure 28. Native Pin Access Area

7.1 Breakout Pin Headers (not populated)

The EK-RA8E2 board pin header footprints, J2, J3, J4 and J17 provide access to nearly all RA MCU interface signals, and to voltages for all RA MCU power ports. Each header pin is labelled with the voltage or port connected to that pin. Refer to the RA8E2 MCU Group User’s Manual for details of each port function, and the EK-RA8E2 board schematic for pin header port assignments.

Pin header footprints J14 and J37 provide access to the SDRAM interface pins.

7.2 MCU and USB Current Measurement

Included in the Native Pin Access area are current measurement resistors and test points to measure the MCU USB controller current and the MCU core power current.

The EK-RA8E2 board provides precision 5 mΩ resistors (Yageo, part number PS0612FKE070R005L) for current measurement of the main 3.3 V MCU power and the 3.3 V USB MCU power. Measure the voltage drop across these resistors and use Ohm’s Law to calculate the current. For convenience, TP1 and TP3 are provided to measure the main 3.3 V MCU power, and TP2 and TP4 are provided to measure the 3.3 V USB MCU power. See Figure 31 for the location of TP1, TP2, TP3 and TP4.

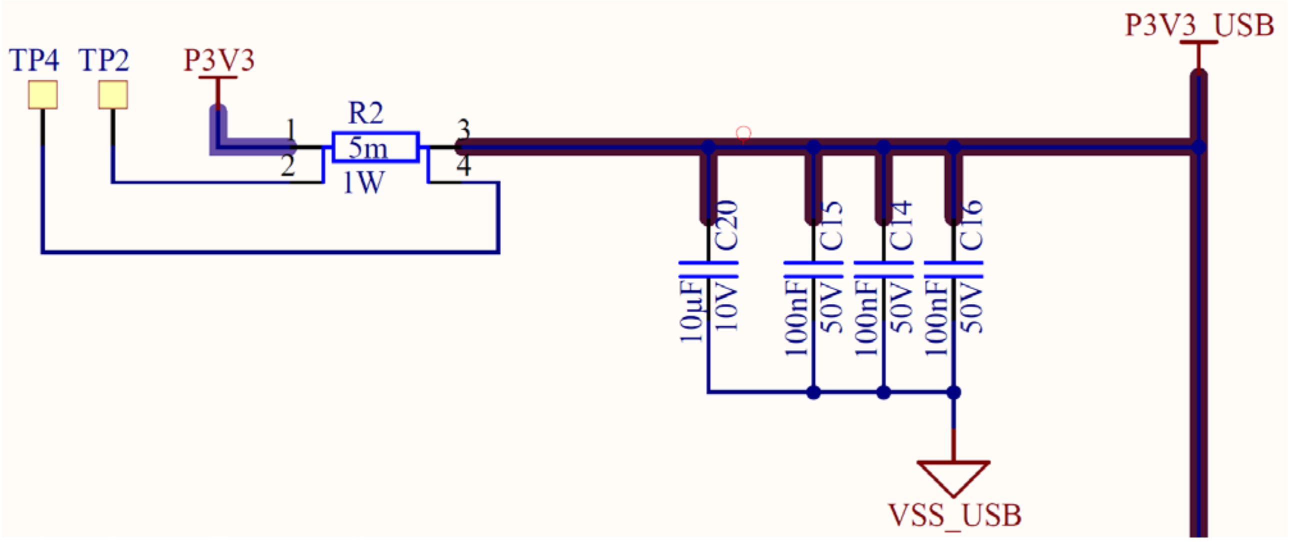

Figure 29. RA USB Current Measurement Circuit

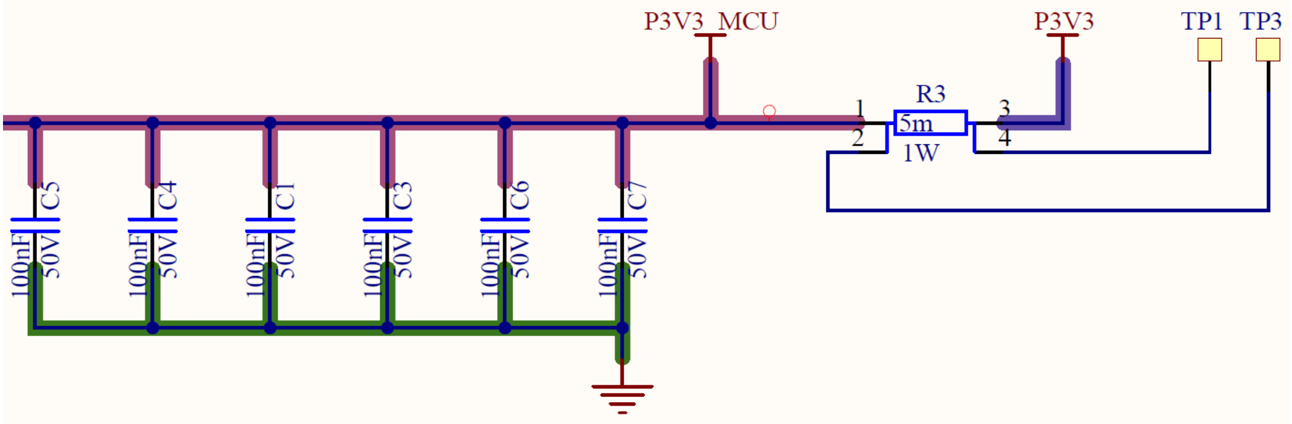

Figure 30. RA +3.3 V Current Measurement Circuit

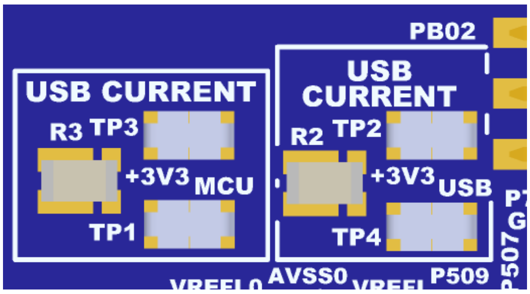

Figure 31. RA MCU and USB Current Measurement

8. Expansion Boards

8.1 Parallel Graphics Expansion Board 2

The EK-RA8E2 kit includes the Parallel Graphics Expansion Board 2. The Parallel Graphics Expansion Board 2 features a WVGA (800×480) Display with capacitive touchscreen connected to the RA MCU using the Parallel Graphics Expansion Port (J1).

8.1.1 Connecting the Parallel Graphics Expansion Board 2 to the EK-RA8E2 Board

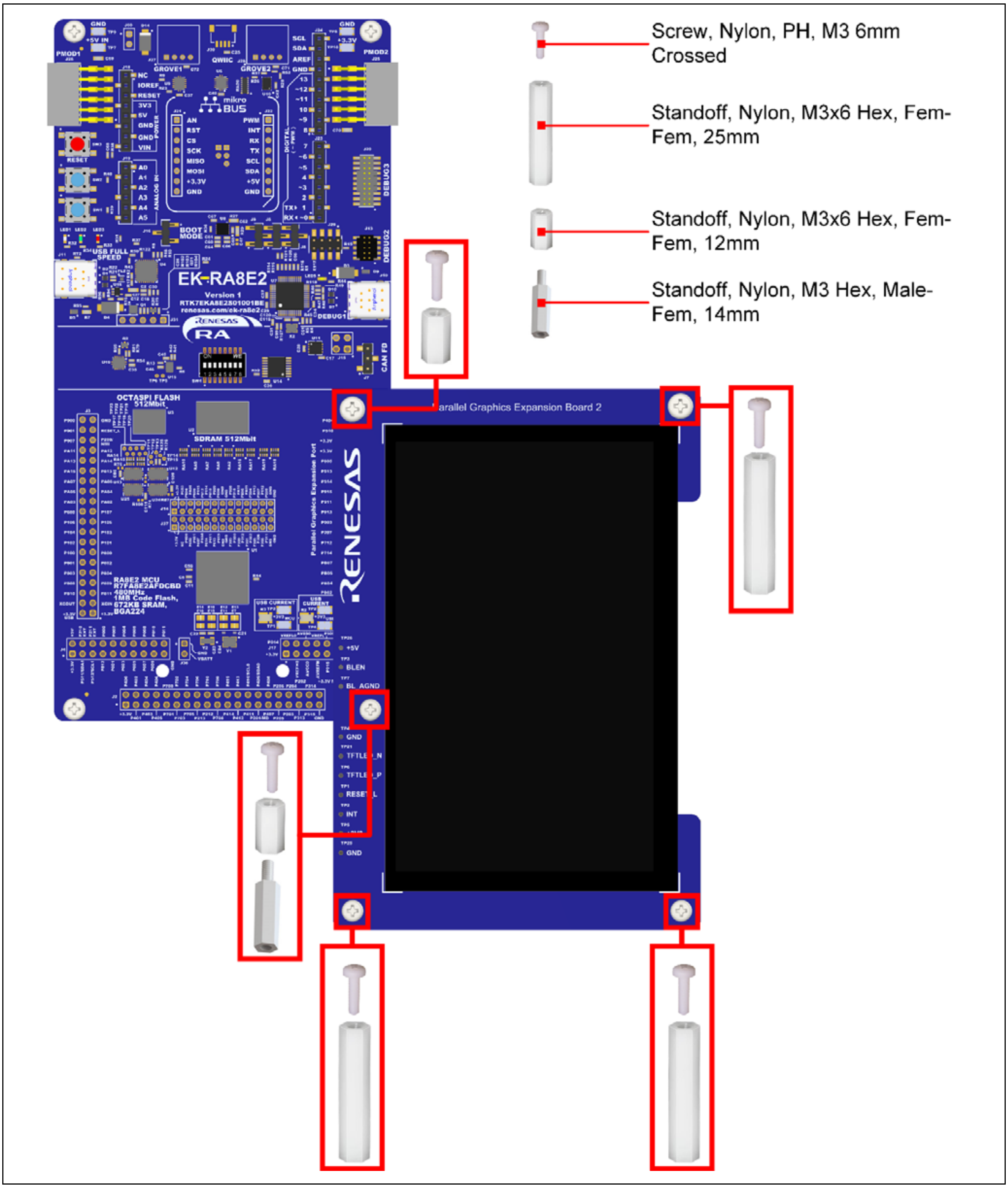

Figure 32. EK-RA8E2 Board Connected with Parallel Graphics Expansion Board 2

8.1.2 Parallel Graphics Expansion Port

The Parallel Graphics Expansion Port (J1) connects the EK-RA8E2 board to the Parallel Graphics Expansion Board 2 supplied in the kit. The RA MCU parallel graphics expansion port can be configured with 8-8-8, 6-6-6, and 5-6-5 color depth. Table 27 shows the Parallel Graphics Expansion Port Assignments and signal names for the EK-RA8E2 board.

Note that P510, which is used as the interrupt for the capacitive touch portion of the LCD, must have the internal pull-up feature enabled in the RA8E2 MCU configuration. This will ensure proper responsiveness of the LCD capacitive touch overlay.

TCON3 (P515) is used to enable the LCD. To ensure the LCD functions, set P515 to initial high state in the FSP pin configuration or set the P515 high in software when LCD is required

Table 27. Parallel Graphics Expansion Port Assignments

Parallel Graphics Expansion Port		**EK-RA8E2**			
Pin	**Description**	**Signal/Bus**	**RGB Signal (RGB888)**	**RGB Signal (RGB666)**	**RGB Signal (RGB565)**
J1-1	DISP_BLEN	P404	BLEN	BLEN	BLEN
J1-2	IIC_SDA	P511	SDA	SDA	SDA
J1-3	DISP_INT	P510	INT	INT	INT
J1-4	IIC_SCL	P512	SCL	SCL	SCL
J1-5	+3.3 V	+3.3 V	+3.3 V	+3.3 V	+3.3 V
J1-6	DISP_RST	PA01	RST	RST	RST
J1-7	+3.3 V	+3.3 V	+3.3 V	+3.3 V	+3.3 V
J1-8	+5 V	+5 V	+5 V	+5 V	+5 V
J1-9	LCDC_TCON0	P805	VSYNC/TCON0	VSYNC/TCON0	VSYNC/TCON0
J1-10	LCDC_CLK	P806	CLK	CLK	CLK
J1-11	LCDC_TCON2	P513	DE/TCON2	DE/TCON2	DE/TCON2
J1-12	LCDC_TCON1	P807	HSYNC/TCON1	HSYNC/TCON1	HSYNC/TCON1
J1-13	LCDC_EXTCLK	P514	EXTCLK	EXTCLK	EXTCLK
J1-14	LCDC_TCON3	P515	LCD Enable	LCD Enable	LCD Enable
J1-15	LCDC_DATA01	P915	B1	B3	B4
J1-16	LCDC_DATA00	P914	B0	B2	B3
J1-17	LCDC_DATA03	P911	B3	B5	B6
J1-18	LCDC_DATA02	P910	B2	B4	B5
J1-19	LCDC_DATA05	P913	B5	B7	G2
J1-20	LCDC_DATA04	P912	B4	B6	B7
J1-21	LCDC_DATA07	P903	B7	G3	G4
J1-22	LCDC_DATA06	P904	B6	G2	G3
J1-23	LCDC_DATA09	P207	G1	G5	G6
J1-24	LCDC_DATA08	P902	G0	G4	G5
J1-25	LCDC_DATA11	P712	G3	G7	R3
J1-26	LCDC_DATA10	P711	G2	G6	G7
J1-27	LCDC_DATA13	P714	G5	R3	R5
J1-28	LCDC_DATA12	P713	G4	R2	R4
J1-29	LCDC_DATA15	PB07	G7	R5	R7
J1-30	LCDC_DATA14	P715	G6	R4	R6
J1-31	LCDC_DATA17	PB05	R1	R7	N.C.
J1-32	LCDC_DATA16	PB06	R0	R6	N.C.
J1-33	LCDC_DATA19	PB04	R3	N.C.	N.C.
J1-34	LCDC_DATA18	PB01	R2	N.C.	N.C.
J1-35	LCDC_DATA21	PB02	R5	N.C.	N.C.
J1-36	LCDC_DATA20	PB03	R4	N.C.	N.C.
J1-37	LCDC_DATA23	P707	R7	N.C.	N.C.
J1-38	LCDC_DATA22	PB00	R6	N.C.	N.C.
J1-39	GND	GND	GND	GND	GND

Parallel Graphics Expansion Port		**EK-RA8E2**			
Pin	**Description**	**Signal/Bus**	**RGB Signal (RGB888)**	**RGB Signal (RGB666)**	**RGB Signal (RGB565)**
J1-40	GND	GND	GND	GND	GND

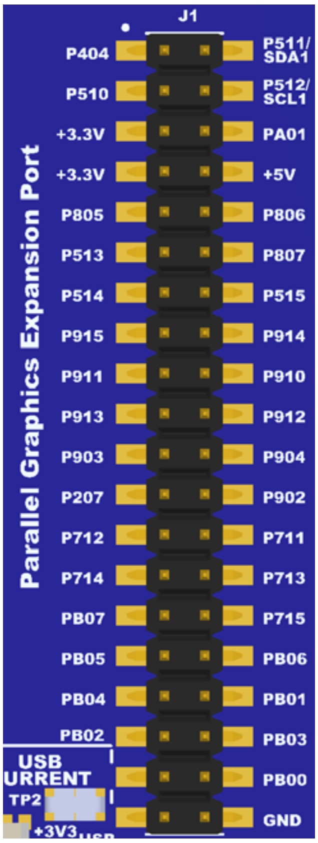

Figure 33. Parallel Graphics Expansion Port

9. Certifications

The EK-RA8E2 v1 kit meets the following certifications/standards. See page 3 of this user's manual for the disclaimer and precautions.

9.1 EMC/EMI Standards

- FCC Notice (Class A)

  This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

  NOTE- This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

  - Reorient or relocate the receiving antenna.
  - Increase the separation between the equipment and receiver.
  - Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
  - Consult the dealer or an experienced radio/television technician for help.
- Innovation, Science and Economic Development Canada ICES-003 Compliance:

  CAN ICES-3 (A)/NMB-3(A)
- CE Class A (EMC)

  This product is herewith confirmed to comply with the requirements set out in the Council Directives on the Approximation of the laws of the Member States relating to Electromagnetic Compatibility Directive 2014/30/EU.

  Warning – This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures to correct this interference.
- UKCA Class A (EMC)

  This product is in conformity with the following relevant UK Statutory Instrument(s) (and its amendments): 2016 No. 1091 Electromagnetic Compatibility Regulations 2016.

  Warning – This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures to correct this interference.
- Taiwan: Chinese National Standard 13438, C6357 compliance, Class A limits
- Australia/New Zealand AS/NZS CISPR 32:2015, Class A

9.2 Material Selection, Waste, Recycling and Disposal Standards

- EU RoHS
- WEEE
- China SJ/T 113642014, 10-year environmental protection use period.

9.3 Safety Standards

- UL 94V-0

10. Design and Manufacturing Information

The design and manufacturing information for the EK-RA8E2 v1 kit is available in the "EK-RA8E2 v1 Design Package" available on renesas.com/ek-ra8e2

- Design packages:
  - EK-RA8E2 Board design package: ek-ra8e2-v1-designpackage.zip
  - Parallel Graphics Expansion Board 2 design package: app_lcd-ek_par_2-v1-designpackage.zip

Table 28. EK-RA8E2 Board Design Package Contents

File Type	Content	File/Folder Name
File (PDF)	Schematics	ek-ra8e2-v1-schematics
File (PDF)	Mechanical Drawing	ek-ra8e2-v1-mechdwg
File (PDF)	3D Drawing	ek-ra8e2-v1-3d
File (PDF)	BOM	ek-ra8e2-v1-bom
Folder	Manufacturing Files	Manufacturing Files
Folder	Design Files	Design Files-Altium

Table 29. Parallel Graphics Expansion Board 2 Design Package Contents

File Type	Content	File/Folder Name
File (PDF)	Schematics	app_lcd-ek_par_2-v1-schematics
File (PDF)	Mechanical Drawing	app_lcd-ek_par_2-v1-mechdwg
File (PDF)	3D Drawing	app_lcd-ek_par_2-v1-3d
File (PDF)	BOM	app_lcd-ek_par_2-v1-bom
Folder	Manufacturing Files	Manufacturing Files
Folder	Design Files	Design Files-Altium

11. Website and Support

Visit the following URLs to learn about the kit and the RA family of microcontrollers, download tools and documentation, and get support.

EK-RA8E2 Resources	renesas.com/ek-ra8e2
RA Kit Information	renesas.com/ra/kits
RA Product Information	renesas.com/ra
RA Product Support Forum	renesas.com/ra/forum
RA Videos	renesas.com/ra/videos
Renesas Support	renesas.com/support
RA Flexible Software Package (FSP)	renesas.com/fsp

Revision History

Rev.	Date	Description	
		Page	**Summary**
1.00	May.20.25	—	Initial release
1.01	Jun.06.25	36	Updated Figure 32
1.02	Jun.16.25	9	Updated Figure 3

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