NEC

User's Manual

EB-V850ES/KJ1+-EE

Demonstration Kit for the K_Line Family

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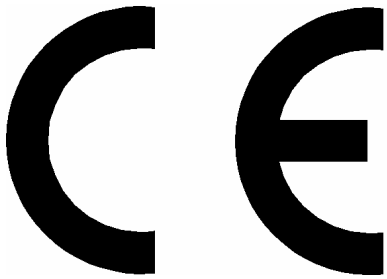

EB-V850ES/KJ1+-EE complies with the EMC protection requirements

WARNING

This is a 'Class A' (EN 55022 : 1998) equipment. This equipment can cause radio frequency noise when used in the residential area. In such cases, the user/operator of the equipment may be required to take appropriate countermeasures under his responsibility.

EEDT-ST-001-11

CAUTION

This equipment should be handled like a CMOS semiconductor device. The user must take all precautions to avoid build-up of static electricity while working with this equipment. All test and measurement tool including the workbench must be grounded. The user/operator must be grounded using the wrist strap. The connectors and/or device pins should not be touched with bare hands.

EEDT-ST-004-10

Revision History

Date	Revision	Chapter	Description
06-04-2005	V1.00	---	First release

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1. Introduction

EB-V850ES/KJ1+-EE is a demonstration kit for the NEC's K_Line V850ES microcontroller family. It supports onboard FLASH programming and real time execution of application programs. The board is prepared to be connected to user hardware parts such as digital I/O or analogue signals.

1.1 Main features of *EB-V850ES/KJ1+-EE*

- Easy to use device demonstration capabilities
  EB-V850ES/KJ1+-EE contains elements to easily demonstrate simple I/O-functions, i.e. push buttons, LED output, AD reference voltage, I/O lines, UART serial interface.

- Power supply via USB interface
  EB-V850ES/KJ1+-EE is powered via USB interface, no separate power supply is needed.

- N-Wire interface
  The *EB-V850ES/KJ1+-EE* is equipped with a KEL adapter in order to connect the QB-V850MINI-EE or IE-V850E1-CD-NW on-chip debug emulator to use on-chip debug function of the V850ES/KJ1+ device. Please note, the QB-V850MINI-EE and IE-V850E1-CD-NW are separate products from NEC and there are not included in this starterkit package.

- FPL, FLASH programming software
  A windows based FLASH programming software allows to select and download application programs to the *EB-V850ES/KJ1+-EE* board for evaluation purposes.

- Analogue to digital signal conversion is supported

- Various input / output signals available, such as

  - All I/O ports prepared to be connected to user hardware
  - Timer input / output signals
  - Two or three wire serial I/O
  - UART interface, via USB UART chip FT232
  - 8 analogue input lines
  - 2 analogue output lines
  - 7 segment LED
  - 2 push buttons prepared for external interrupt generation

- The IAR Embedded Workbench for V850 and the IAR C-SPY debugger / simulator are included. These packages are restricted in such that maximum program code size is limited to 16 kByte.

- Full documentation is included for the NEC V850ES/KJ1+ device, the IAR Systems Embedded Workbench, IAR Systems C-SPY debugger / simulator and the NEC FPL FLASH programming software.

_EB-V850ES/KJ1+-EE_ is not intended for code development. NEC does not allow and does not support in any way any attempt to use _EB-V850ES/KJ1+-EE_ in a commercial or technical product.

1.2 System requirements

HOST PC

A PC supporting Windows 98SE, Windows ME, Windows 2000 or Windows XP is required for the IAR Systems Embedded Workbench demo-version and the FPL FLASH programming software.
Pentium 166 MHz (at least), 128 MB of RAM, 256-color display (1024 * 768), mouse, CD-ROM drive and 200 Mbytes of free hard disk space are required to install the tool packages.

Above listed requirements are valid for the IAR Systems Embedded Workbench and the FPL FLASH programming software.

Host interface

USB interface that enables communication based on USB (Ver1.1 or later)

1.3 Package contents

Please verify that you have received all parts listed in the package contents list attached to the *EB-V850ES/KJ1+-EE* package. If any part is missing or seems to be damaged, please contact the dealer from whom you received your *EB-V850ES/KJ1+-EE*.

Note: Updates to this User Manual, additional documentation and/or utilities for *EB-V850ES/KJ1+-EE*, if available, may be downloaded from the NEC WEB page(s) at **http://www.ee.nec.de/updates**.

2. *EB-V850ES/KJ1+-EE* system configuration

The *EB-V850ES/KJ1+-EE* system configuration is given in the diagram below:

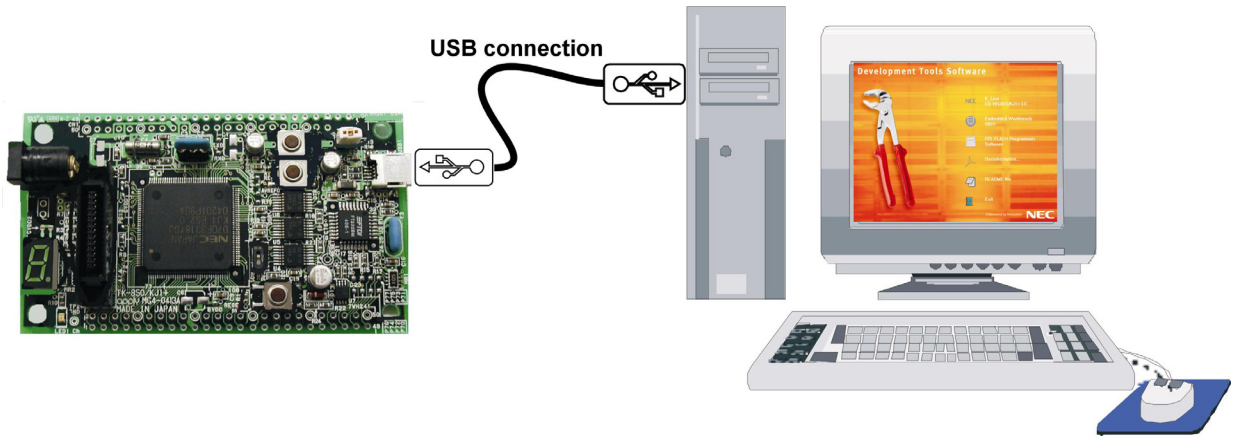


Figure 1: *EB-V850ES/KJ1+-EE* system configuration

2.1 *EB-V850ES/KJ1+-EE*

EB-V850ES/KJ1+-EE is a demonstration kit for the NEC K_Line V850ES family devices. As a typical device from K_Line family the V850ES/KJ1+ device is used. The board is connected to the host system via USB interface cable. The host system may be used for onboard FLASH programming of the V850ES/KJ1+ internal FLASH memory and to allow execution of application programs on *K_Line board* platform.

The *EB-V850ES/KJ1+-EE* board is equipped with an 5.0000 MHz oscillator, allows running the V850ES/KJ1+ CPU at 20MHz. Sub-clock is provided with 32.768 kHz.

2.2 Host computer

The USB host interface enables communication to the *EB-V850ES/KJ1+-EE* board. The USB UART chip FT232 allows application software to access the USB device in the same way as it would access a standard RS232 interface. The FTDI's Virtual COM Port (VCP) driver appears to the windows system as an extra Com Port, in addition to any existing hardware Com Ports.

For a detailed specification of the host interface please refer to the **CHAPTER 11 CONNECTORS AND CABLES** of this document.

2.3 Power supply via USB interface

EB-V850ES/KJ1+EE is powered by USB interface, no separate power supply is needed. The USB interface provides the *EB-V850ES/KJ1+-EE* board with 5V supply voltage.

3. *EB-V850ES/KJ1+-EE* board components

The *EB-V850ES/KJ1+-EE* board is equipped with push buttons, a 7 segment LED and several connectors in order to be connected to user hardware or host computers.

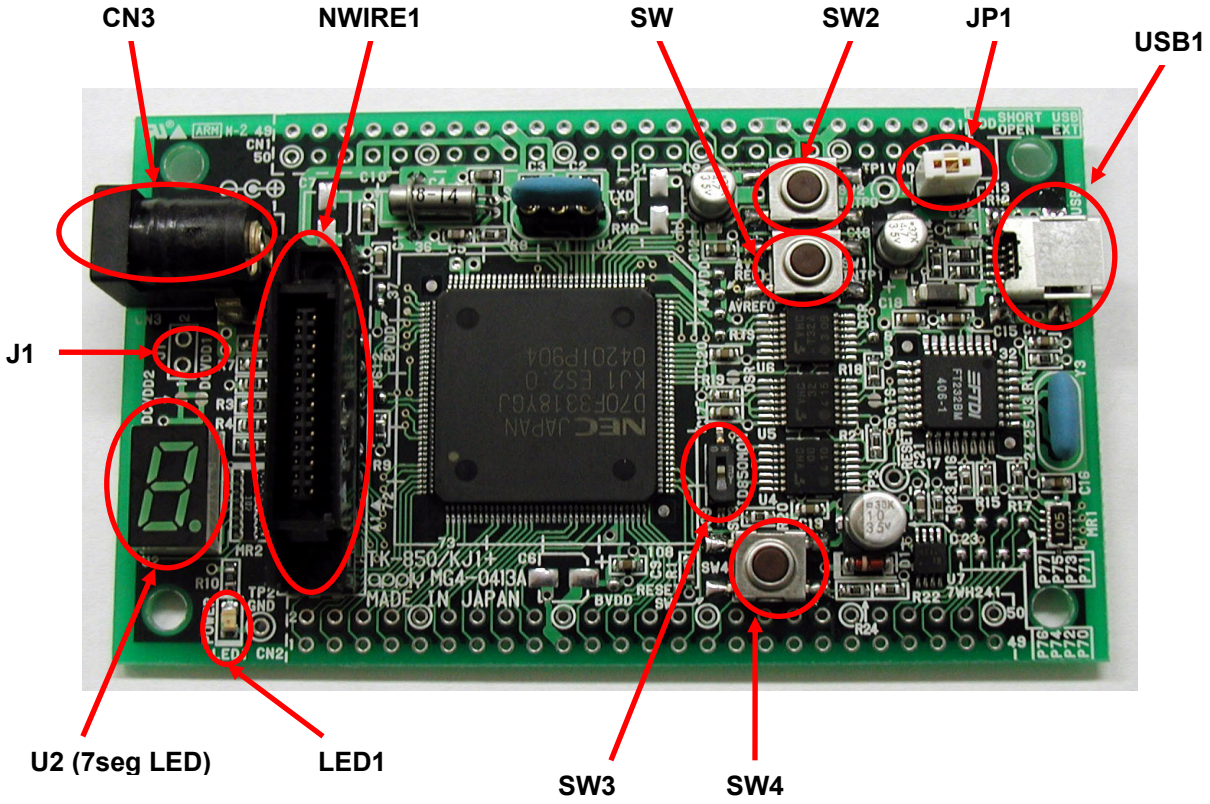


Figure 2: *EB-V850ES/KJ1+-EE* board connectors, switches and LED's

Some of the *EB-V850ES/KJ1+-EE* components are free for user application hardware and software. Please read the user's manual of the V850ES/KJ1+ device carefully to get information about the electrical specification of the available I/O ports before you connect any external signal to the *EB-V850ES/KJ1+-EE* board.

3.1 User button SW1

SW1 is a push button connecting Vss to external interrupt input INTP1 of the CPU. This is equal to port P04 of the V850ES/KJ1+ CPU. The port may be programmed to generate interrupt INTP1. The necessary initialisation for this purpose is described in the user's manual of the V850ES/KJ1+ device. Please note, when using SW1 turn ON the built-in pull-up resistor of V850ES/KJ1+ device, register PU0.

3.2 User button SW2

SW2 is a push button connecting Vss to external interrupt input INTP0 of the CPU. This is equal to port P03 of the V850ES/KJ1+ CPU. The port may be programmed to generate interrupt INTP0. The necessary initialisation for this purpose is described in the user's manual of the V850ES/KJ1+ device. Please note, when using SW2 turn ON the built-in pull-up resistor of V850ES/KJ1+ device, register PU0.

3.3 Programming switch SW3

SW3 controls the programming mode of the *EB-V850ES/KJ1+-EE* board. Setting SW3 to ON allows to reprogram the internal FLASH memory of the V850ES/KJ1+ device using the FPL FLASH programming software.

SW3	Operation mode
OFF (default)	Normal operation mode
ON	FLASH memory programming mode

Table 1: Programming switch SW3

Within normal operation mode the user program stored in the FLASH memory of the V850ES/KJ1+ device is executed.

3.4 RESET button SW4

SW4 is a reset button. It activates the power on reset. It is connected to the reset circuit of the *EB-V850ES/KJ1+-EE* board.

3.5 Power LED LED1

LED1 is the Power LED. LED1 is activated if power is supplied to the *EB-V850ES/KJ1+-EE* board.

3.6 Power supply selector JP1

Jumper JP1 selects the power supply of the *EB-V850ES/KJ1+-EE* board. Closing jumper JP1 (default setting) supplies power (Vcc=5V) from the USB interface line. When opening JP1, external power can be supplied by using connectors CN3 or J1.

JP1	Mode
closed (default)	Power supplied by USB interface
open	External power supply

Table 2: Power supply selector, JP1

Note: When choosing external power supply, please open jumper JP1!

3.7 External power supply

External power can be supply by connecting a 5V AC adapter to connector CN3. Per default, the external power is supplied to the connector CN1 only (pins 10, 12 and 16). To power the complete board via external power supply, the soldering bridges DCVDD1 and DCVDD2 must be closed.

CN3	Function
Center (1)	Vcc = 5V
Ring (2,3)	Gnd

Table 3: External power supply, connector CN3

Additionally a stabilizing 5V power supply can be connected directly to the connector J1 instead of using a 5V AC adapter. Also in this case the soldering bridges DCVDD1 and DCVDD2 must be closed.

J1	Function
1	Vcc = 5V
2	Gnd

Table 4: External power supply, connector J1

Note: When using an external power supply, please open jumper JP1!

3.8 USB interface connector USB1

USB1 connector allows connecting the FPL FLASH programming software to the *EB-V850ES/KJ1+-EE* board in order to program application software into the CPU internal flash memory. The board power supply of 5V is also provided by this connector.

Additionally connector USB1 connects UART0 of the V850ES/KJ1+ device to the host system.

3.9 N-Wire connector NWIRE1

The NWIRE1 connector allows connecting the QB-V850MINI-EE or alternative the IE-V850E1-CD-NW on-chip debug emulator to the *EB-V850ES/KJ1+-EE* board in order to use on-chip debug function of the V850ES/KJ1+ device.

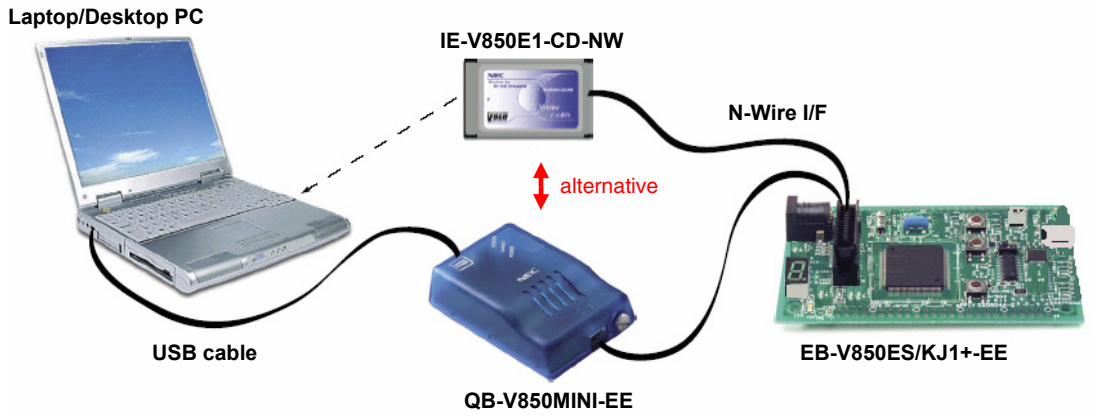


Figure 3: On-chip debugging system configuration

Please note, the QB-V850MINI-EE and IE-V850E1-CD-NW are separate products from NEC and are not included in this starterkit package.

NWIRE1	Signal Name	description	NWIRE1	Signal Name	description
A1	TRCCLK	not connected	B1	GND_0	connected to Vss
A2	TRCDATA0	not connected	B2	GND_1	connected to Vss
A3	TRCDATA1	not connected	B3	GND_2	connected to Vss
A4	TRCDATA2	not connected	B4	GND_3	connected to Vss
A5	TRCDATA3	not connected	B5	GND_4	connected to Vss
A6	TRCEND	not connected	B6	GND_5	connected to Vss
A7	DDI	connected to P52	B7	GND_6	connected to Vss
A8	DCK	connected to P54	B8	GND_7	connected to Vss
A9	DMS	connected to P55	B9	GND_8	connected to Vss
A10	DDO	connected to P53	B10	GND_9	connected to Vss
A11	DRST_	connected to P05	B11	GPIO2	connected to Vss
A12	GPIO0	connected to RESET0	B12	GPIO3	connected to Vss
A13	GPIO1	connected to FLMD0 logic	B13	TRGT_VDD	connected to EV_{DD}

Table 5: N-Wire connector NWIRE1

NOTE: To enable on-chip debugging for the V850ES/KJ1+ CPU set switch SW3 to OFF.

3.10 External LED U2

The 7 segment LED U2 is connected to port P60-P67 of the V850ES/KJ1+ device. A low signal output at each port switches the corresponding LED on.

Port V850ES/KJ1+	Segment	LED U2
P60	A	
P61	B	
P62	C	
P63	D	
P64	E	
P65	F	
P66	G	
P67	DP	

Table 6: External LED U2

Example: The figure of 0 to 9 can be displayed by writing the following values to the port register P6.

P6, register value	LED U2	P6, register value	LED U2
0xC0	0	0x92	5
0xF9	1	0x83	6
0xA4	2	0xF8	7
0xB0	3	0x80	8
0x99	4	0x98	9

3.11 External connectors CN1 and CN2

CN1 and CN2 are connectors for external user hardware. Please read the user's manual of the V850ES/KJ1+ device carefully to get information about the electrical specification of the available I/O ports.

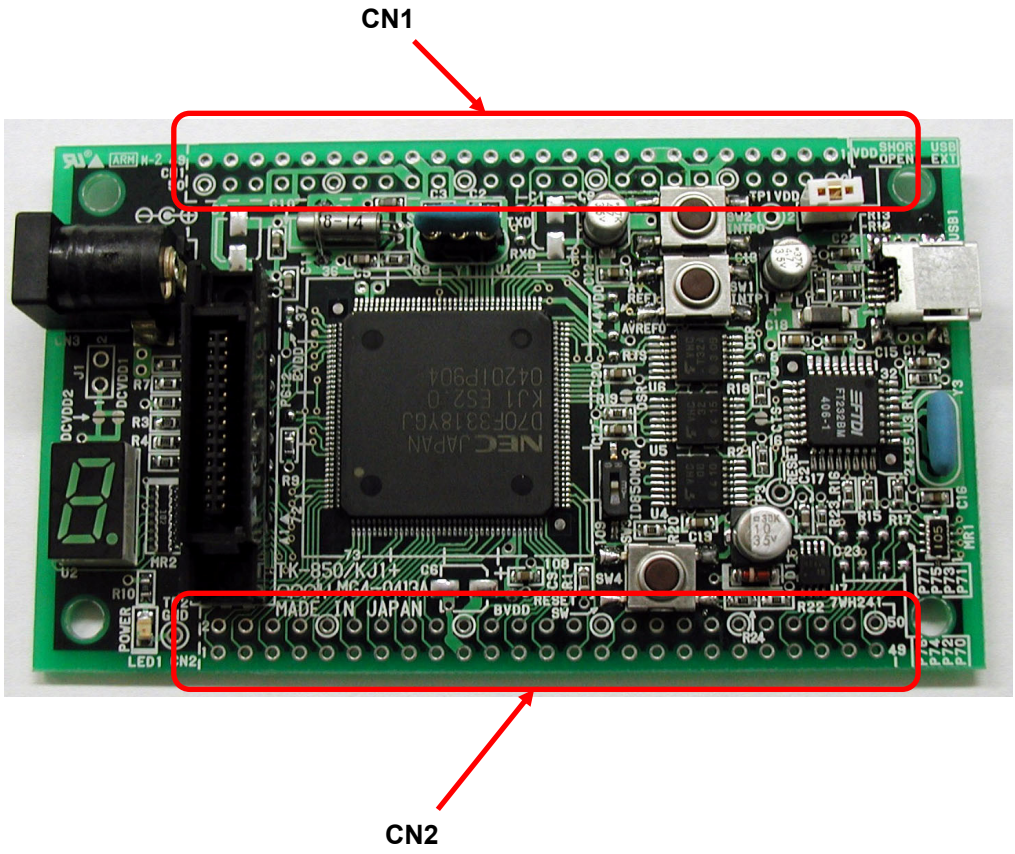


Figure 4: External connectors CN1 and CN2

CN1	Signal name	V850ES/KJ1+ Pin name	Comment
1	AV_{REF0}	AV_{REF0}	Connected to V_{DD} by soldering bridge
2	Vss	AVss, Vss, EVss, BVss	
3	P10	P10/ANO0	
4	P11	P11/ANO1	
5	AV_{REF1}	AV_{REF1}	Connected to V_{DD} by soldering bridge
6	P00	P00/TOH0	
7	P01	P01/TOH1	
8	P614	P614	Connected to FLDM0 control logic
9	V_{DD}	V_{DD}	
10	+12V		Connected to CN3 and J1
11	Vss	AVss, Vss, EVss, BVss	
12	+12V		Connected to CN3 and J1
13	V_{DD}	V_{DD}	
14	RESET0	RESET	Connected to reset circuit
15	V_{DD}	V_{DD}	
16	+12V		Connected to CN3 and J1
17	P02	P02/NMI	
18	P03	P03/INTP0	SW2
19	P04	P04/INTP1	SW1
20	P05	P05/INTP2	
21	P06	P06/INTP3	
22	P40	P40/SI00/RXD2	
23	P41	P41/SO00/TXD2	
24	P42	P42/SCK00	
25	P30	P30/TXD0/TO02	Connected to RXD by soldering bridge
26	P31	P31/RXD0/INTP7/TO03	Connected to TXD by soldering bridge
27	P32	P32/ASCK0/ADTRG/TO01	
28	P33	P33/TI000/TO00/TIP00/TOP00	
29	P34	P34/TI001/TO00/TIP01/TOP01	
30	P35	P35/TI010/TO01	
31	P36	P36	
32	P37	P37	
33	Vss	AVss, Vss, EVss, BVss	
34	EV_{DD}	EV_{DD}	Connected to V_{DD} by soldering bridge
35	P38	P38/SDA0	
36	P39	P39/SCL0	
37	P50	P50/TI011/RTP00/KR0	
38	P51	P51/TI50/RTP01/KR1	
39	P52	P52/TO50/RTP02/KR2	
40	P53	P53/SIA0/RTP03/KR3	
41	P54	P54/SOA0/RTP04/KR4	
42	P55	P55/SCKA0/RTP05/KR5	
43	P90	P90/A0/TXD1/KR6	
44	P91	P91/A1/RXD1/KR7	
45	P92	P92/A2/TI020/TO02	
46	P93	P93/A3/TI021	
47	P94	P94/A4/TI030/TO03	
48	P95	P95/A5/TI031	
49	P96	P96/A6/TI51/TO51	
50	P97	P97/A7/SI01	

Table 7: Connector CN1

CN2	Signal name	V850ES/KJ1+ Pin name	Comment
1	P98	P98/A8/SO01	
2	P99	P99/A9/SCK01	
3	P910	P910/A10/SIA1	
4	P911	P911/A11/SOA1	
5	P912	P912/A12/SCKA1	
6	P913	P913/A13/INTP4	
7	P914	P914/A14/INTP5	
8	P915	P915/A15/INTP6	
9	PCS0	PCS0/CS0	
10	PCS1	PCS1/CS1	
11	PCM0	PCM0/WAIT	
12	PCM1	PCM1/CLKOUT	
13	PCM2	PCM2/HLDAK	
14	PCM3	PCM3/HLDRQ	
15	PCT0	PCT0/WR0	
16	PCT1	PCT1/WR1	
17	PCT4	PCT4/RD	
18	PCT6	PCT6/ASTB	
19	Vss	AVss, Vss, EVss, BVss	
20	BV_{DD}	BV_{DD}	Connected to V_{DD} by soldering bridge
21	PDL0	PDL0/AD0	
22	PDL1	PDL1/AD1	
23	PDL2	PDL2/AD2	
24	PDL3	PDL3/AD3	
25	PDL4	PDL4/AD4	
26	PDL5	PDL5/AD5/FLMD1	
27	PDL6	PDL6/AD6	
28	PDL7	PDL7/AD7	
29	PDL8	PDL8/AD8	
30	PDL9	PDL9/AD9	
31	PDL10	PDL10/AD10	
32	PDL11	PDL11/AD11	
33	PDL12	PDL12/AD12	
34	PDL13	PDL13/AD13	
35	PDL14	PDL14/AD14	
36	PDL15	PDL15/AD15	
37	PDH0	PDH0/A16	
38	PDH1	PDH1/A17	
39	PDH2	PDH2/A18	
40	PDH3	PDH3/A19	
41	PDH4	PDH4/A20	
42	PDH5	PDH5/A21	
43	P77	P77/ANI7	Connected to 1M• pull down resistor by soldering bridge
44	P76	P76/ANI6	Connected to 1M• pull down resistor by soldering bridge
45	P75	P75/ANI5	Connected to 1M• pull down resistor by soldering bridge
46	P74	P74/ANI4	Connected to 1M• pull down resistor by soldering bridge
47	P73	P73/ANI3	Connected to 1M• pull down resistor by soldering bridge
48	P72	P72/ANI2	Connected to 1M• pull down resistor by soldering bridge
49	P71	P71/ANI1	Connected to 1M• pull down resistor by soldering bridge
50	P70	P70/ANI0	Connected to 1M• pull down resistor by soldering bridge

Table 8: Connector CN2

3.12 Soldering Bridges

Some terminals of the V850ES/KJ1+ device can be customized by opening the corresponding soldering bridge. By opening the soldering bridge the connection to the onboard circuit is cut. Accordingly, the corresponding signals can be used for external user hardware using connectors CN1 and CN2. For more details please refer to the board schematics, pages 66-67.

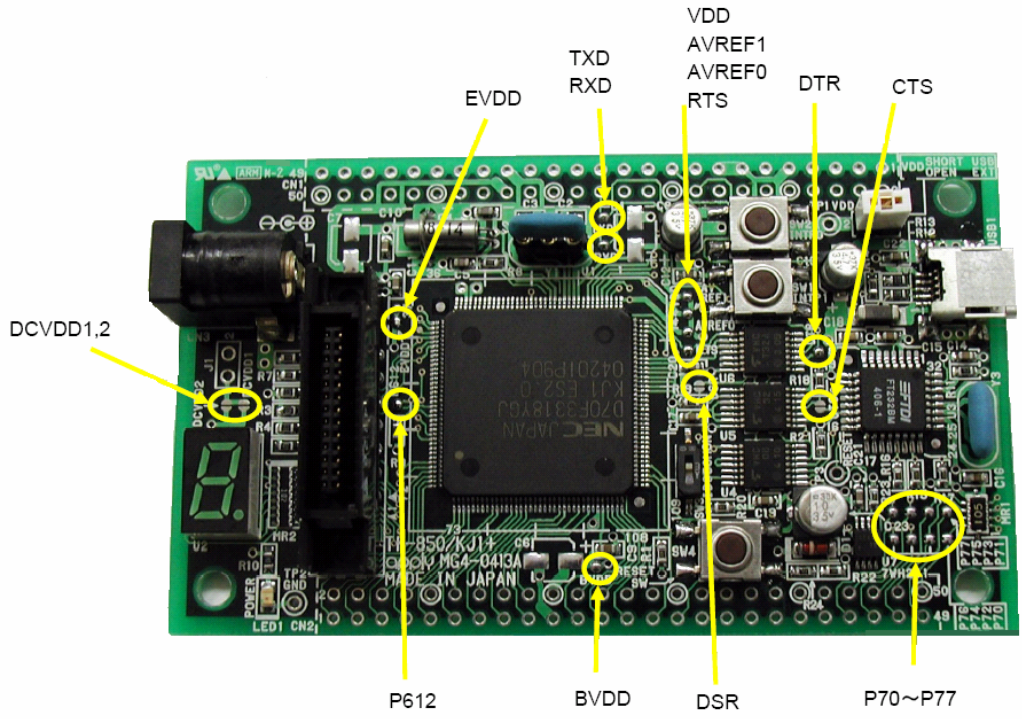


Figure 5: Arrangement of soldering bridges

Soldering bridge name	Factory setting	Comment
P70 – P77	Closed	Connected to 1M• pull down resistor
RXD, TXD	Closed	Terminal RXD / P31 and TXD / P30 of FT232 circuit.
CTS, DSR	Open	Terminal CTS / P613 and DSR / P611 of FT232 circuit
DTR, RTS	Closed	Terminal DTR / P610 and RTS / P69 of FT232 circuit
P612	Closed	Connected to TXD line
V_{DD}	Closed	Connected to terminal REGC
AV_{REF0}, AV_{REF1}	Closed	Connected to V_{DD}
BV_{DD}	Closed	Connected to V_{DD}
EV_{DD}	Closed	Connected to V_{DD}
DCVDD1, DCVDD2	Open	When using external power supply, via connector CN3 and J1, the soldering bridge must be closed.

Table 9: Soldering brigdes

3.13 V850ES/KJ1+ memory map

The V850ES/KJ1+ memory layout is shown in the table below.

Address area	0x3FFFFFF 0x3FFF000	SFR Area	Free for user application software
	0x3FFEFFF 0x3FFB000	16 KB Internal RAM	
	0x3FFAFFF 0x1000000	Access prohibited area	
	0x0FFFFFF 0x0100000	External memory	
	0x00FFFFF 0x0040000	Access prohibited area	
	0x003FFFF 0x0000000	256 KB Flash memory	Free for user application Software

Table 10: V850ES/KJ1+ memory map

The *EB-V850ES/KJ1+-EE* does not reserve any resources of the V850ES/KJ1+ device, consequently all available memory of the device is free for application software.

4. *EB-V850ES/KJ1+-EE* installation and operation

4.1 Getting started

The windows based FPL FLASH programming software allows to select and download application programs to *EB-V850ES/KJ1+-EE* starterkit. As communication interface between PC host system and the *EB-V850ES/KJ1+-EE* board a USB interface line is needed. Before you can download and run a program, hardware and software must be installed properly.

4.1.1 CD-ROM contents

The CD-ROM shows following directory structure:

EB_V850ESKJ1_EE (F:)	CD-ROM ROOT
Acrobat	- Acrobat Reader for 32Bit Windows OS
Doc	- Documentation
FPL	- FPL FLASH programming software
Drivers	… USB driver
FPL	… FPL setup directory
PRM	… PRM parameter file
IAR Embedded Workbench V850	- IAR Embedded Workbench for V850
SampleProgram	- Sample program for *EB-V850ES/KJ1+-EE*
IAR	… IAR sample project
GHS	… Green Hills sample project

Table 11: *EB-V850ES/KJ1+-EE* CD-ROM directory structure

5. Hardware installation

After unpacking *EB-V850ES/KJ1+-EE,* connect the board to your host computer using the provided USB interface cable. When *EB-V850ES/KJ1+-EE* is connected, the USB driver needs to be installed on the host machine. Please refer to the following **CHAPTER 6 SOFTWARE INSTALLATION**.

6. Software installation

The *EB-V850ES/KJ1+-EE* package comes with several software demo packages:

- IAR Systems Embedded Workbench for V850, including C compiler, assembler, linker, librarian and IAR C-SPY debugger / simulator
- FPL FLASH programming software
- Sample programs

The IAR Systems Embedded Workbench and the FPL FLASH programming GUI must be installed on your PC. For detailed installation hints, refer to the following chapters and to the corresponding documentation of the IAR Embedded Workbench.

The sample programs can be downloaded to the *EB-V850ES/KJ1+-EE* board directly from the CDROM. Only if you intend to modify or debug (simulate) the sample programs it is necessary to copy them to your local hard disk.

Remark: Before modification or re-building of sample programs, do not forget to remove "Read-only" attribute of copied files.

6.1 IAR Systems Embedded Workbench for V850 installation

To install the IAR Systems Embedded Workbench for V850 including the C-SPY debugger / simulator, select the `SETUP` program in the directory `\IAR Embedded Workbench V850\ewv850\` of the CDROM. The setup dialogues will guide you through the installation process.

6.2 FPL FLASH programming GUI installation

To install the FPL FLASH programming GUI select the `SETUP` program in the directory `\FPL\` of the CDROM. The setup dialogues will guide you through the installation process.

6.3 Sample program installation

The sample program does not require any installation for download to the *EB-V850ES/KJ1+-EE* board. If the sample program shall be modified it is required to copy them into any directory of your local hard disk. A file copy using the Windows explorer is the recommended procedure.

Remark: Before modification or re-building of sample program, do not forget to remove "Read-only" attribute of copied files.

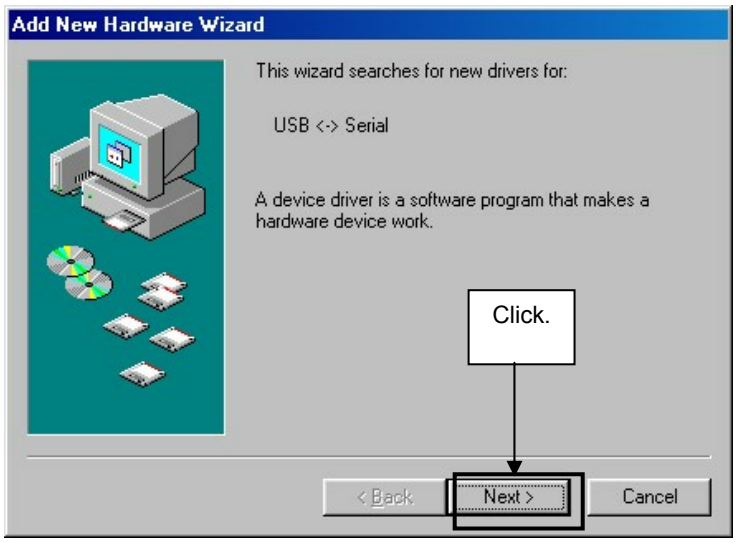
6.4 USB Driver Installation

When the *EB-V850ES/KJ1+-EE* board and FPL is used, the driver needs to be installed on the host machine. Install the driver according to the following procedure:

6.4.1 Installation on Windows 98SE/Me

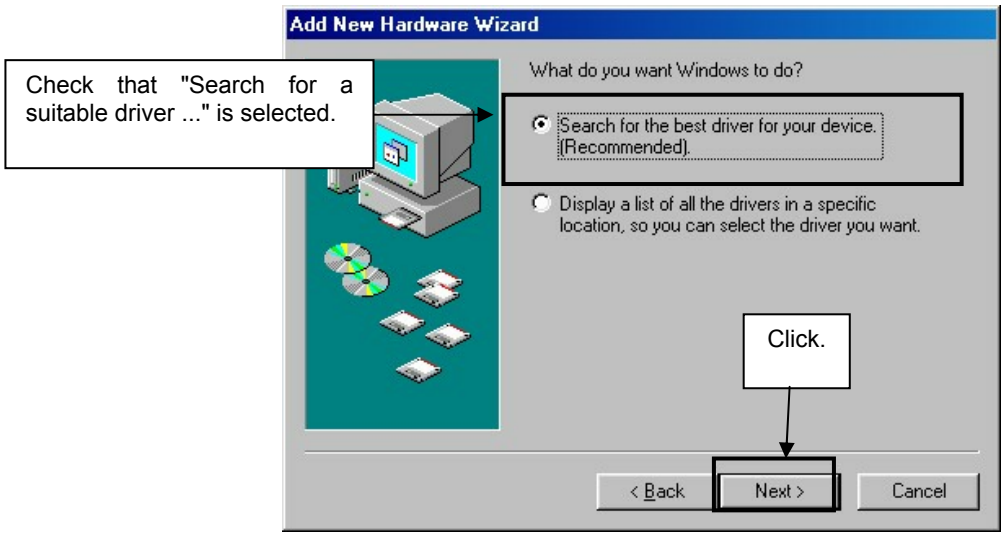
1. When the *EB-V850ES/KJ1+-EE* board is connected with the host machine, the board is recognized by Plug and Play, and the wizard for adding new hardware is started. Click Next>.

Figure 6: Add New Hardware Wizard (Windows 98SE)



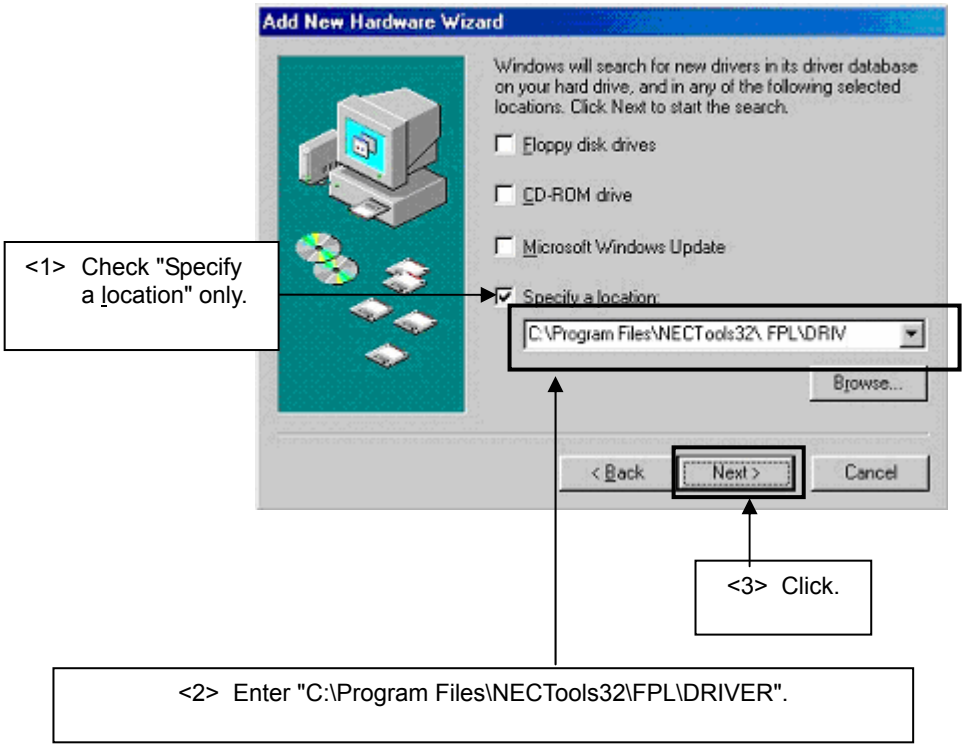
2. The window below is displayed. So, check that "Search for a suitable driver ..." is selected, then click Next>.

Figure 7: Search Method (Windows 98SE)



3. Check the "Specify a location" check box only and enter "C:\Program Files\NECTools32\FPL\DRIVER" in the address bar, then click Next>.

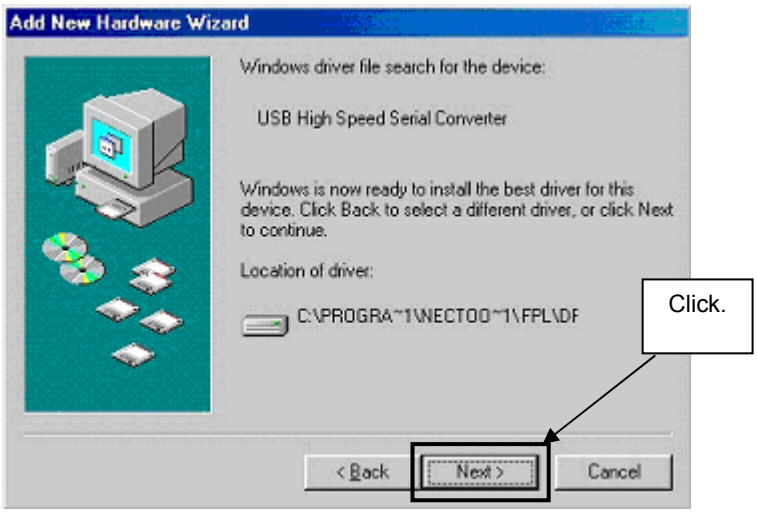
Figure 8: Search Location Specification (Windows 98SE)



Remark If the installation destination folder is changed at the time of GUI software installation, enter "new-folder\DRIVER".

4. The window below is displayed. Click Next>.

Figure 9: Checking Driver to Be Installed (Windows 98SE)



5. When the window below is displayed, the installation of the USB driver is completed. Click Finish. The installation of the USB Serial Port driver is then automatically performed.

Figure 10: Installation Completion (Windows 98SE)

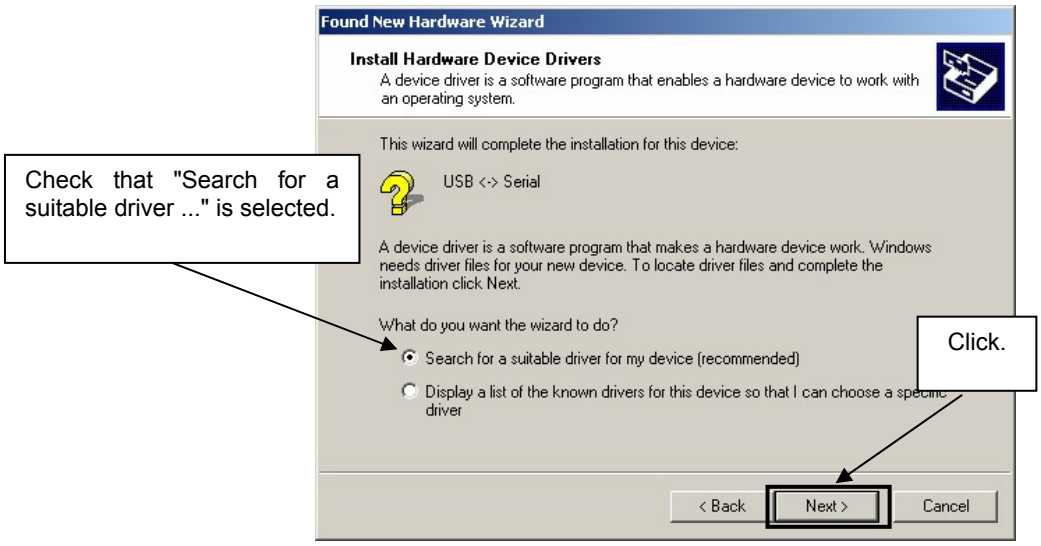
6.4.2 Installation on Windows 2000

1. When the *EB-V850ES/KJ1+-EE* board is connected with the host machine, the board is recognized by Plug and Play, and the wizard for finding new hardware is started. Click Next>.

Figure 11: Found New Hardware Wizard 1 (Windows 2000)

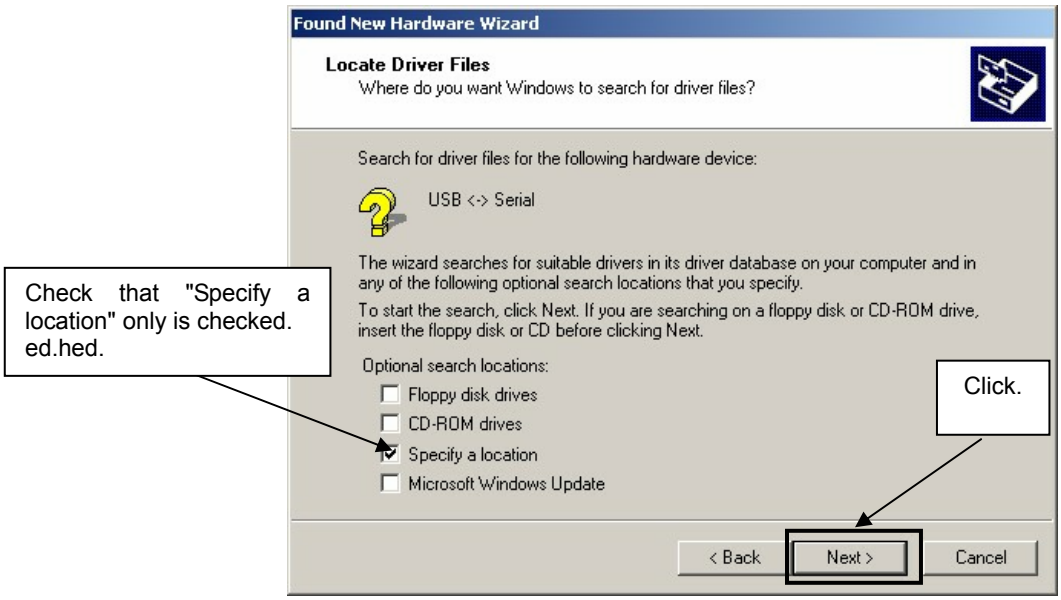
2. The window below is displayed. So, check that "Search for a suitable driver ..." is selected, then click Next>.

Figure 12: Search Method 1 (Windows 2000)



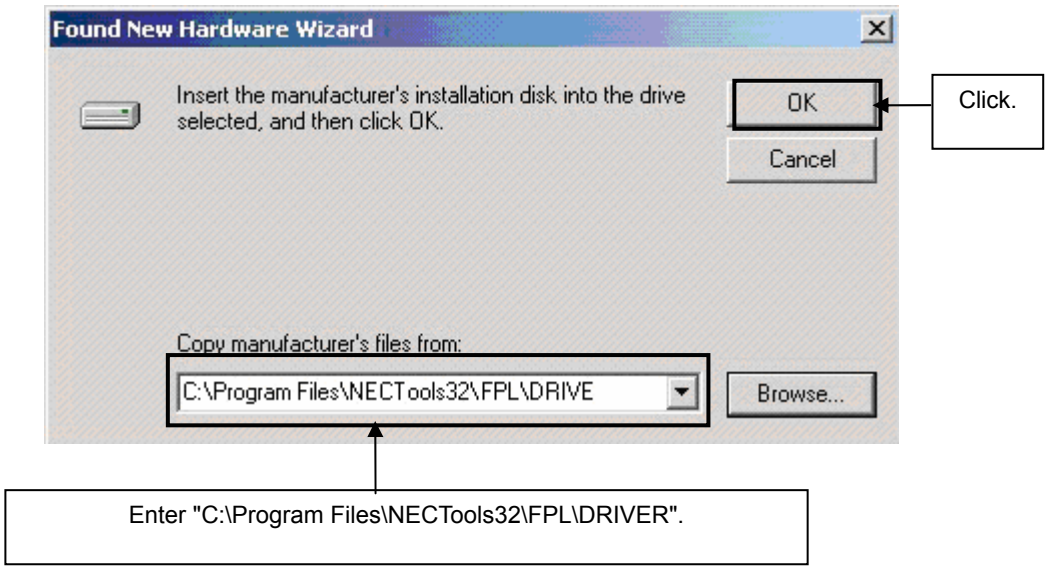
3. Check the "Specify a location" check box only, then click Next>.

Figure 13: Driver File Location 1 (Windows 2000)



4. Enter "C:\Program Files\NECTools32\FPL\DRIVER" in the address bar, then click OK.

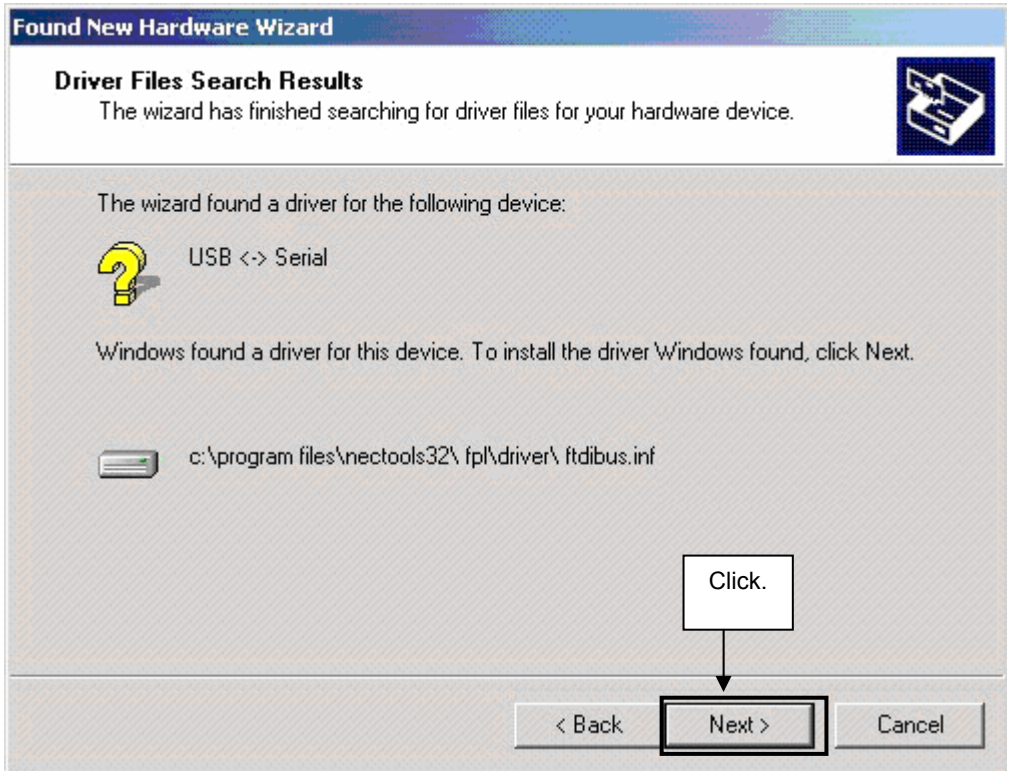
Figure 14: Address Specification 1 (Windows 2000)



Remark If the installation destination folder is changed at the time of GUI software installation, enter "new-folder\FPL\DRIVER".

5. Click Next>.

Figure 15: Driver File Search 1 (Windows 2000)



6. Click Finish to complete the installation of the USB driver.

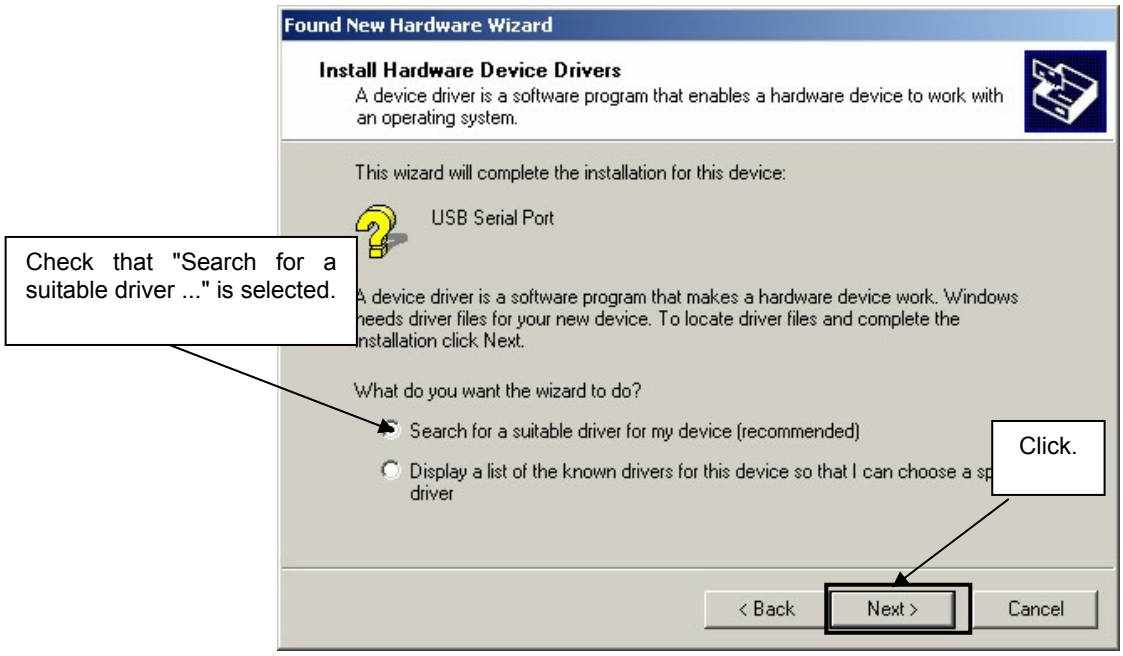
Figure 16: USB Driver Installation Completion 1 (Windows 2000)

7. Proceed to the installation of the USB Serial Port driver. Click Next>.

Figure 17: Found New Hardware Wizard 2 (Windows 2000)

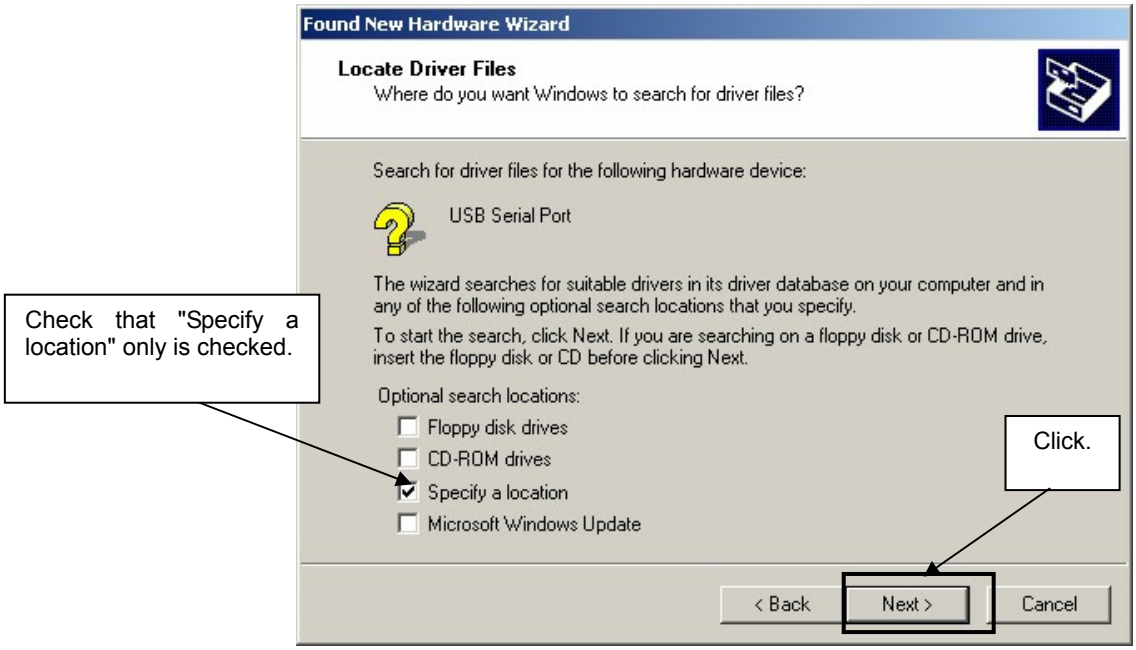
8. The window below is displayed. So, check that "Search for a suitable driver ..." is selected, then click Next>.

Figure 18: Search Method 2 (Windows 2000)



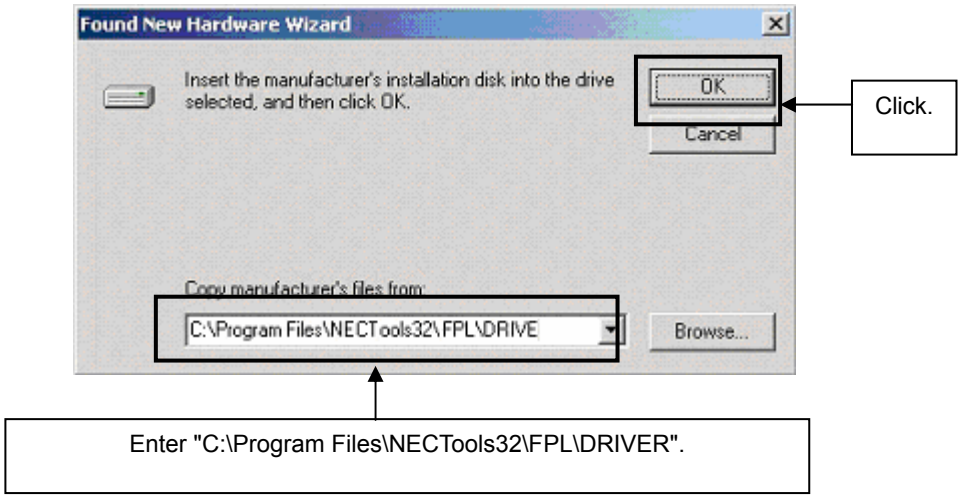
9. Check the "Specify a location" check box only, then click Next>.

Figure 19: Driver File Location 2 (Windows 2000)



10. Enter "C:\Program Files\NECTools32\FPL\DRIVER" in the address bar, then click OK.

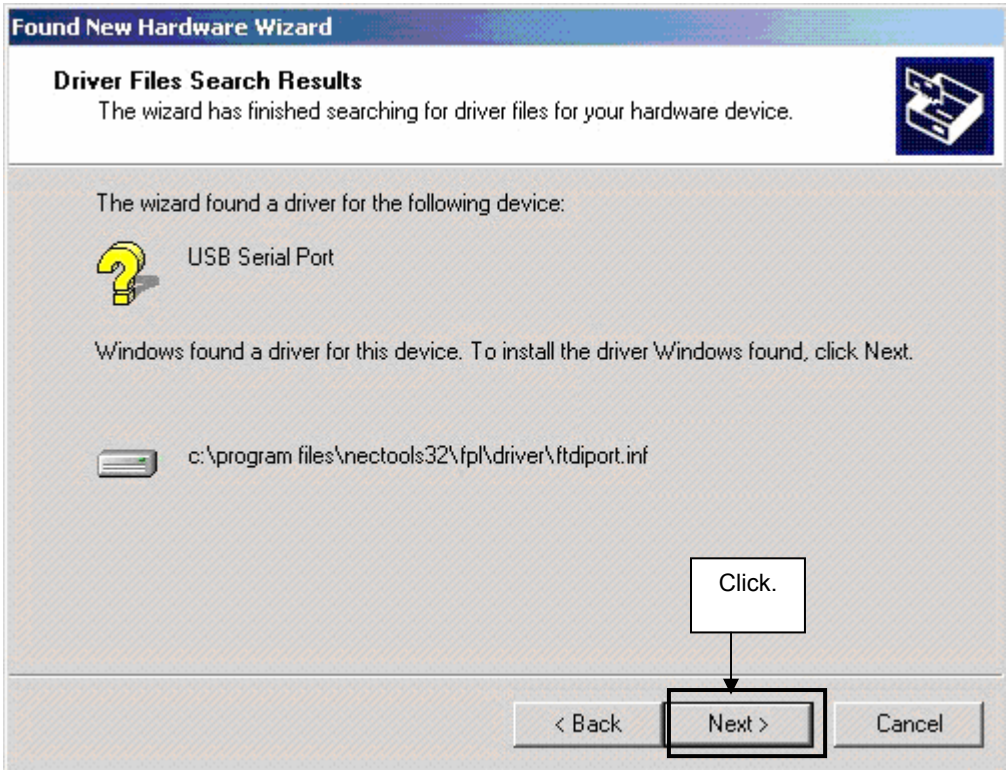
Figure 20: Address Specification 2 (Windows 2000)



Remark If the installation destination folder is changed at the time of GUI software installation, enter "new-folder\DRIVER".

11. Click Next>.

Figure 21: Driver File Search 2 (Windows 2000)



12. Click Finish to complete the installation of the USB driver.

Figure 22: USB Driver Installation Completion 2 (Windows 2000)

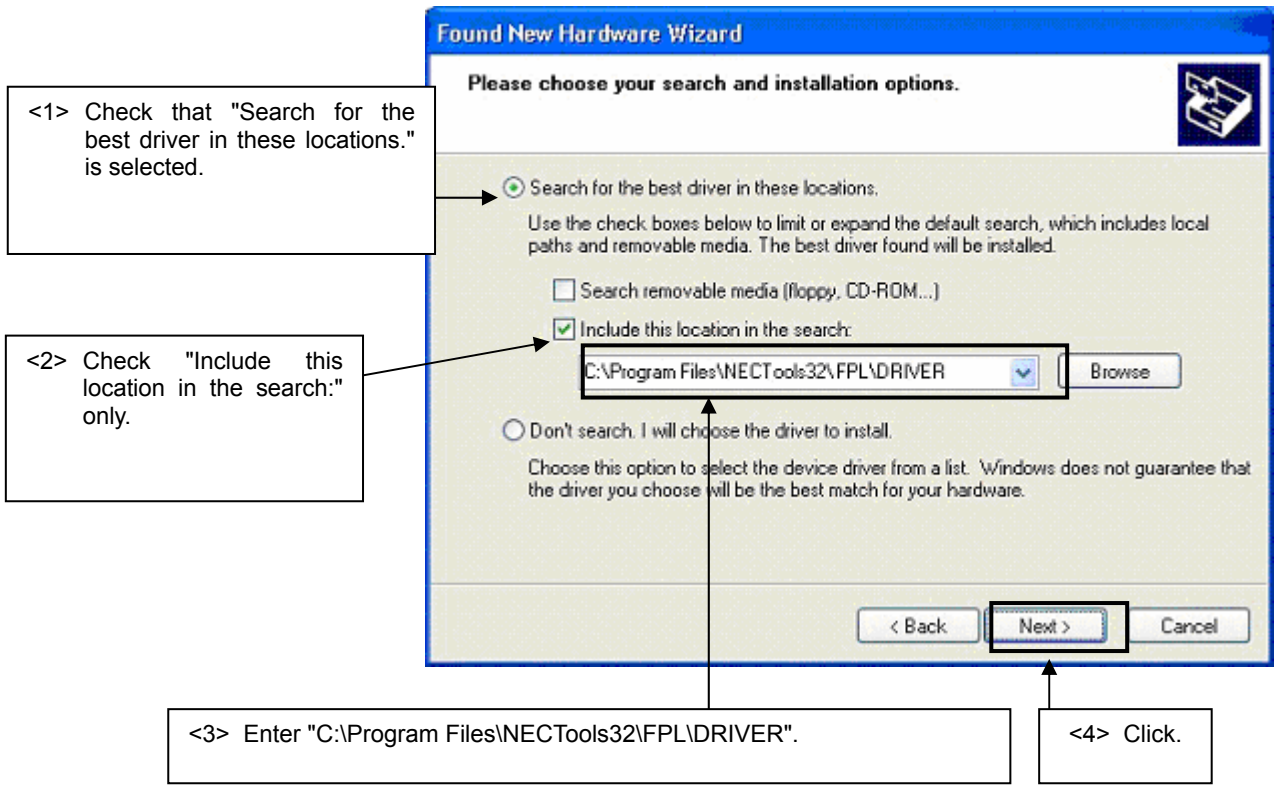
6.4.3 Installation on Windows XP

1. When the *EB-V850ES/KJ1+-EE* board is connected with the host machine, the board is recognized by Plug and Play, and the wizard for finding new hardware is started. Check that "Install from a list or specific ..." is selected, then click Next>.

Figure 23: Found New Hardware Wizard 1 (Windows XP)

2. Check that "Search for the best driver in these locations." is selected. Check the "Include this location in the search:" check box and enter "C:\Program Files\NECTools32\FPL\DRIVER" in the address bar, then click Next>.

Figure 24: Search Location Specification 3 (Windows XP)



3. As shown below, "has not passed Windows Logo testing to verify its compatibility with Windows XP." is displayed. Click Continue Anyway.

Figure 25: Windows XP Logo Testing 3 (Windows XP)

4. When the window below is displayed, the installation of the USB driver is completed. Click Finish.

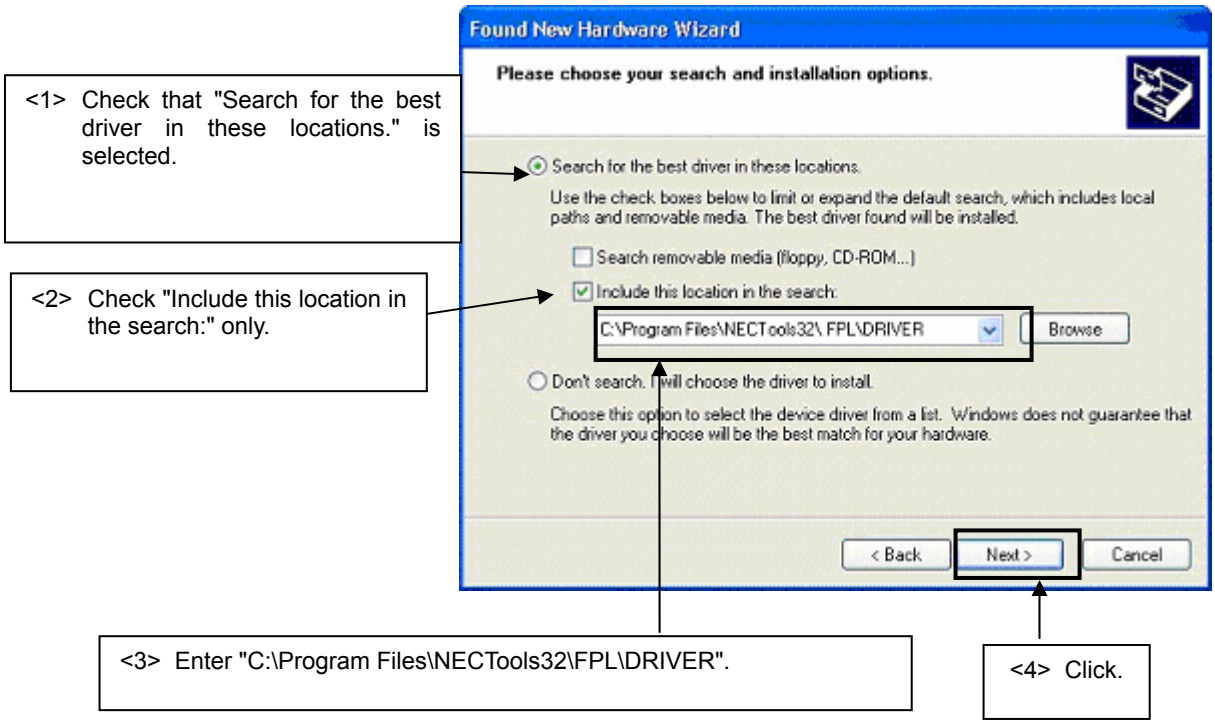
Figure 26: USB Driver Installation Completion 1 (Windows XP)

5. Proceed to the installation of the USB Serial Port driver. Click Next>.

Figure 27: Found New Hardware Wizard 2 (Windows XP)

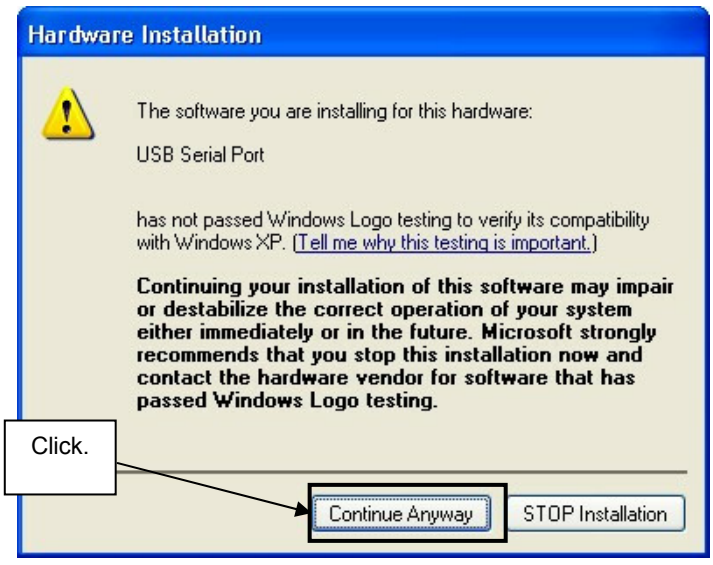
6. Check that "Search for the best driver in these locations." is selected. Check the "Include this location in the search:" check box and enter "C:\Program Files\NECTools32\FPL\DRIVER", then click Next>.

Figure 28: Search Location Specification 2 (Windows XP)



7. As shown below, "has not passed Windows Logo testing to verify its compatibility with Windows XP." is displayed. Click Continue Anyway.

Figure 29: Windows XP Logo Testing 2 (Windows XP)



8. When the window below is displayed, the installation of the USB driver is completed. Click Finish.

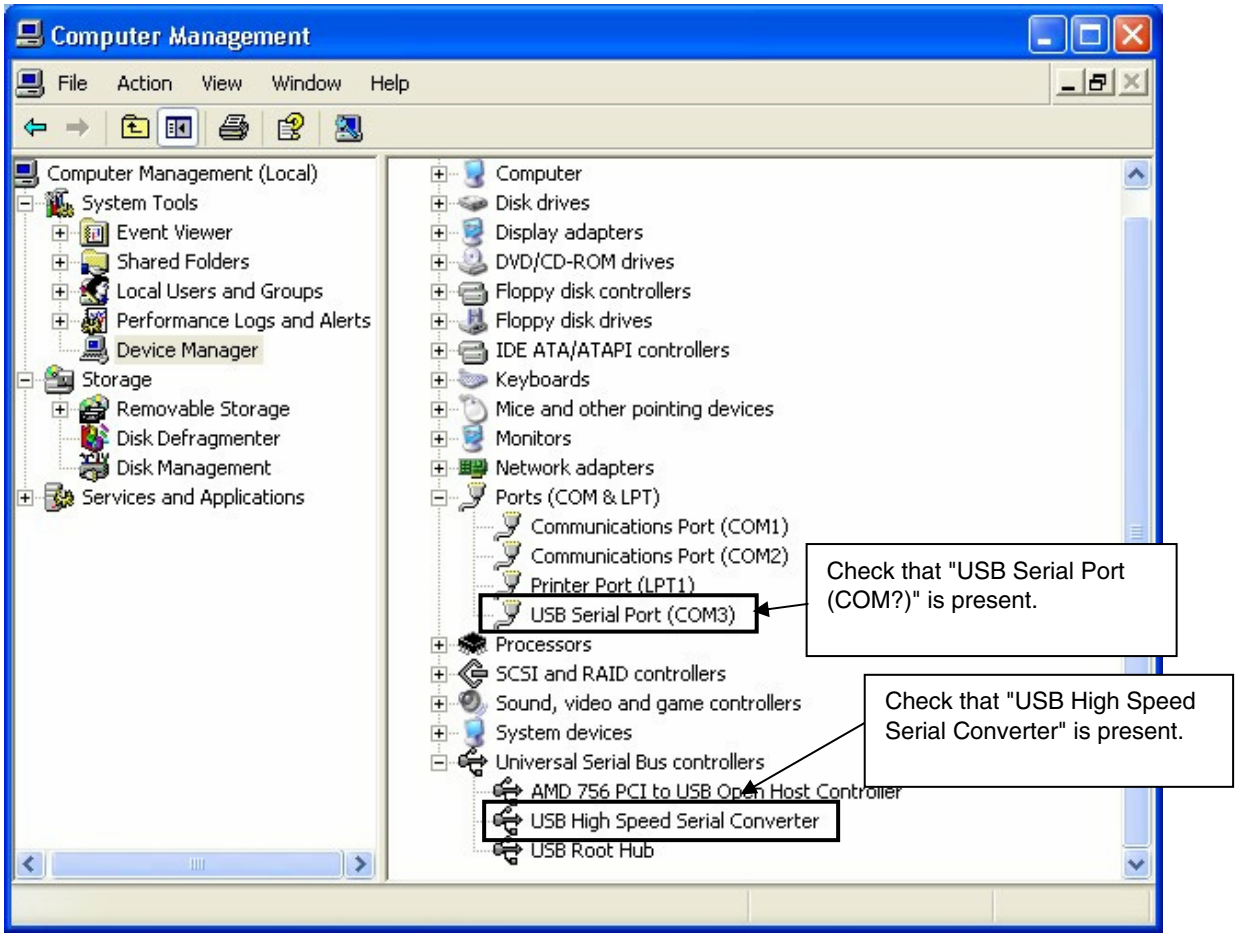
Figure 30: USB Serial Port2 Driver Installation Completion (Windows XP)

6.5 Confirmation of USB Driver Installation

After installing the two types of drivers, check that the drivers have been installed normally, according to the procedure below. When using the *EB-V850ES/KJ1+-EE* board in combination with FPL GUI, the information to be checked here is needed.

By clicking the "Device Manager" tab, check that the drivers are installed normally.

Figure 31: Device Manager



For Windows 98SE/Me

Caution Do not select Update and Erase when communicating with the target device.

For Windows 2000/XP

Caution Do not perform "Hardware Modification Scan" when communicating with the target device.

Remark In the GUI port list box, the same communication port as COM? of USB Serial Port (COM?) needs to be selected.

If the drivers above are not displayed, or the mark "×" or "!" is prefixed, refer to **CHAPTER 9 TROUBLESHOOTING**.

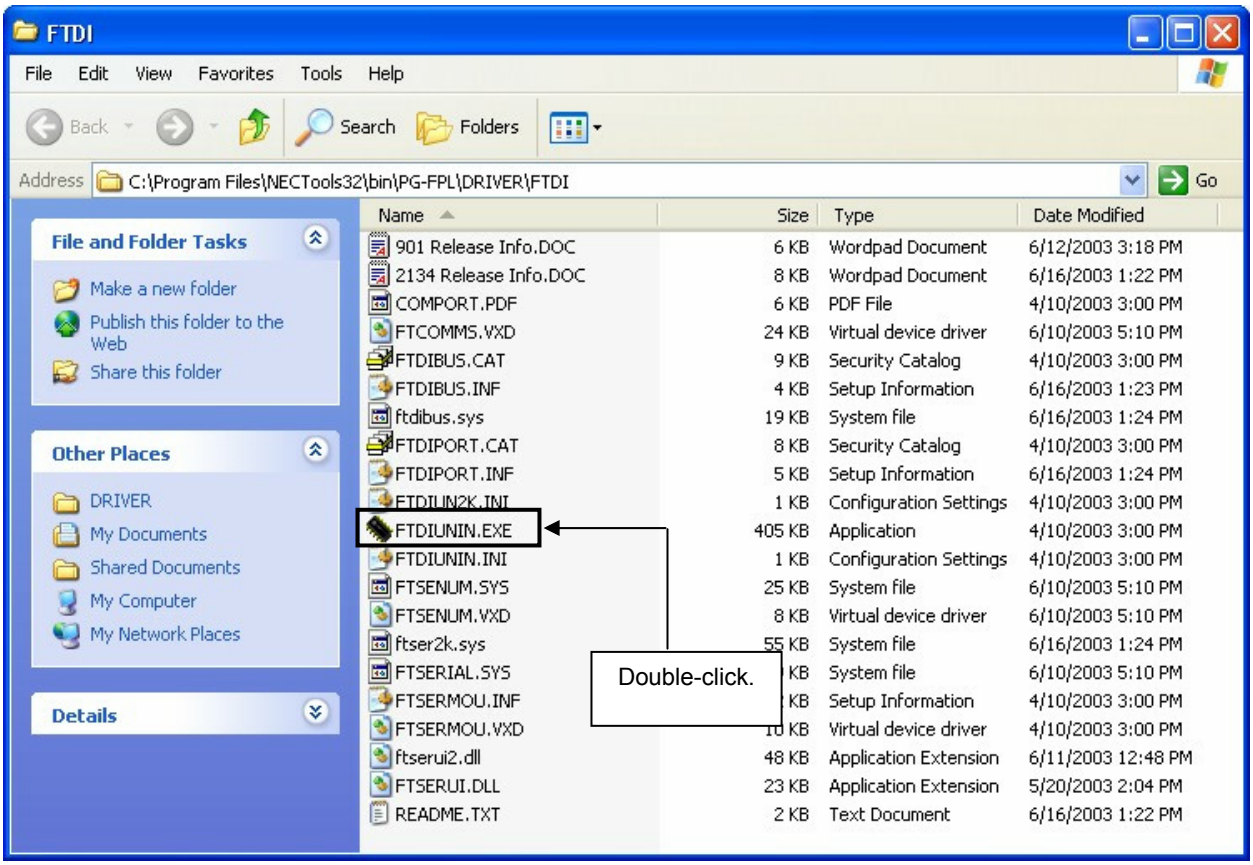
6.6 Driver Uninstallation

The driver uninstallation program is installed on the host machine when the FPL software is installed. Use the procedure below for driver uninstallation.

1. When using Windows XP, log on as the computer administrator. When using Windows 2000, log on as the Administrator.

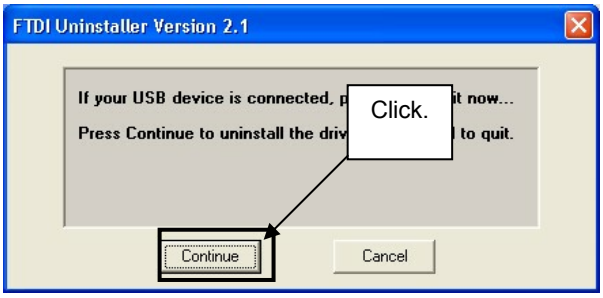
2. Double-click in the order from "My Computer" to "(C:)" to "Program Files" to "NECTools32" to "FPL" to "DRIVER". "Ftdiunin.exe" is displayed. Double-click "Ftdiunin.exe".

Figure 32: Driver Uninstallation



3. Click Continue.

Figure 33: Driver Uninstaller



4. Click Finish to complete driver uninstallation.

Figure 34: Completion of Driver Uninstallation

Caution	If the GUI software is uninstalled earlier, "Ftdiunin.exe" is also deleted. At this time, delete "USB Serial Port (COM?)" and "USB High Speed Serial Converter" from Device Manager manually.

7. FPL FLASH programming software

7.1 Introduction

The parameter file of the V850ES/KJ1+ device is installed automatically during installation of FPL GUI, folder <FPL install-path>\PRM. Nevertheless, newest version of parameter file for the µPD70F3318 device can by download from the NEC Electronics Web site.

Download the parameter file for the PG-FP4 from the following NEC Electronics Web site:

http://www.ee.nec.de/updates

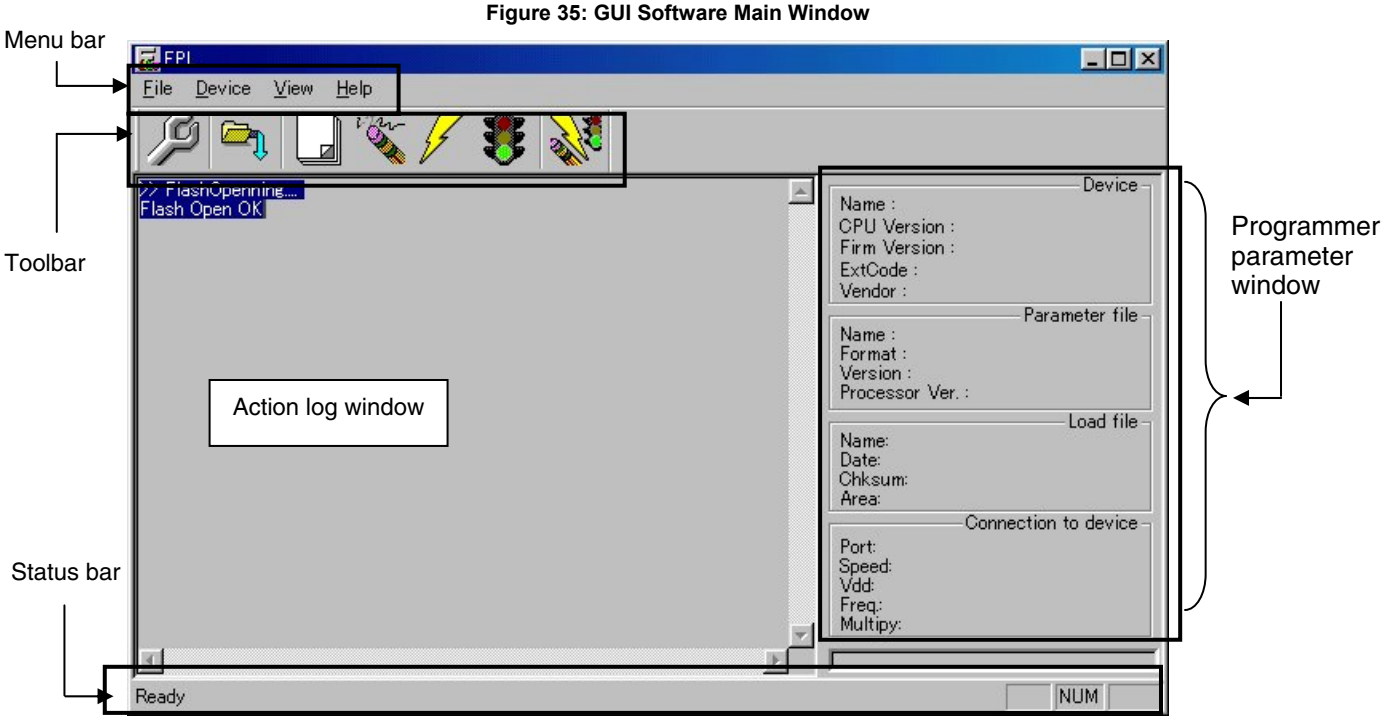
Copy the parameter file downloaded from the NEC Electronics Web site into sub-directory <FPL.EXE-install-path>\PRM created during GUI software setup (refer to **CHAPTER 6 SOFTWARE INSTALLATION**)..

7.2 Starting up the GUI Software

- GUI software startup
  Select FPL.EXE from the start menu to start the FPL GUI software.

When the GUI software is started normally, the following screen appears.

Figure 35: GUI Software Main Window



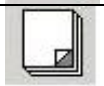
This window consists of the following items:

Name	Display Information
Menu bar (displayed at the top)	Displays menu items executable by the FPL.
Toolbar (displayed under the menu bar)	Displays frequently used commands as icons.
Action log window (displayed under the toolbar)	Displays an FPL action log.
Programmer parameter window (displayed to the right of the action log window)	Displays programming parameter settings.
Status bar	Displays status.

7.3 Toolbar

The toolbar contains buttons for starting the important procedures of the FPL.

Figure 36: Toolbar Buttons

	[Device] → [Setup] button
	[File] → [Load] button
	[Device] → [Blank Check] button
	[Device] → [Erase] button
	[Device] → [Program] button
	[Device] → [Verify] button
	[Device] → [Autoprocedure(EPV)] button

7.4 Menu Bar

Depending on the actual device status and device type, some menu items may be enabled or disabled.

7.4.1 [File] menu

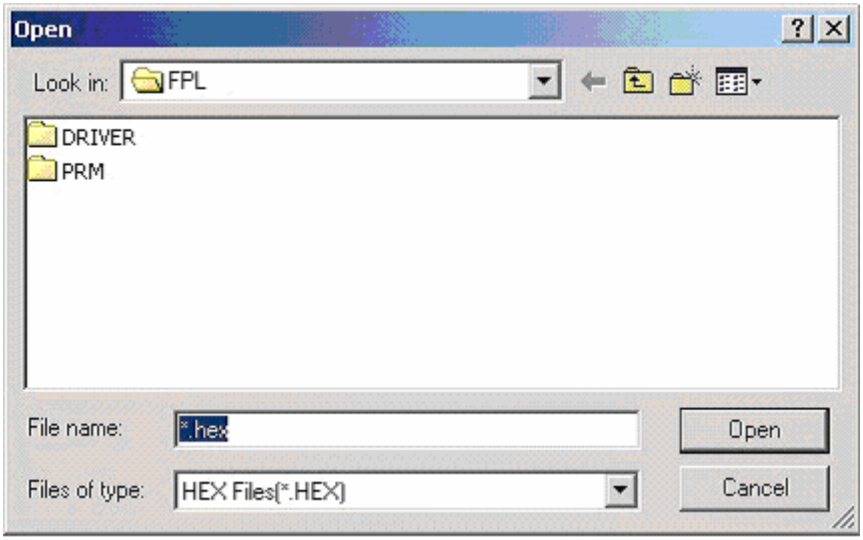
Clicking the [File] menu displays the pull-down menu as shown below.
This menu mainly contains commands related to file operation.

Figure 37: [File] Menu

(1) [Load] command

The [Load] command allows you to select a program file.
The selected program file is programmed into the flash memory of the device by executing the [Program] command or [Autoprocedure(EPV)] command.

Figure 38: HEX File Selection Window



The file selection window for program loading displays the most recently used directory to which a user program has been loaded. After a user program is loaded, a checksum calculation is made and the result is displayed in the programmer parameter window.

[Open button]
Selects a user program as a program to be written to the target device.

[Cancel button]
Closes the window without selecting a program.

(2) [Quit] command

The [Quit] menu is the command for terminating the FPL GUI software. Clicking × on the right side of the task bar also terminates the FPL GUI software.
User settings are saved in the FPL.INI[Note] file, so that the GUI software starts up next time with the same settings.

Note FPL.INI is created in the Windows folder when Windows 98SE, Windows Me, or Windows XP is used.
When Windows 2000 is used, FPL.INI is created in the Winnt folder.

7.4.2 [Device] menu

Clicking the [Device] menu displays the pull-down menu as shown below.
This menu mainly contains commands for programming operations such as deletion, programming, and verification on the target device.

Figure 39: [Device] Menu

(1) [Blank Check] command

The [Blank Check] command allows you to make a blank check on the target device connected to the FPL. If the flash memory of the target device is erased, a blank check is terminated normally. If the flash memory is not completely erased, the indication "not blank" is provided. Before starting programming, erase the flash memory of the target device.

(2) [Erase] command

The [Erase] command erases the flash memory of the target device connected to the FPL. While the flash memory is being erased, the progress status is displayed in the action log window to indicate programmer operation.
The execution on the [Blank Check] command before the [Erase] command is executed follows the setting of 'Command options' of the Advance tab displayed by selecting [Device] → [Setup].
Upon completion of [Erase] command execution, the GUI software displays the result of executing the command on the target device.

(3) [Program] command

The [Program] command sends a specified user program to the target device and writes the program to the flash memory.
The execution of Verify operation for detecting an error in user program communication from the FPL to the target device after the execution of the [Program] command follows the setting of the 'Command options' on the Advance tab displayed by selecting [Device] → [Setup].
During programming, the progress status is displayed in the action log window to indicate programmer operation. This progress status display window displays the progress status on target device programming by percentage.
Upon completion of [Program] command execution, the GUI software displays the result of executing the command on the target device.

(4) [Verify] command

The [Verify] command sends a specified user program to the target device connected with the FPL, and performs verification against the data written to the flash memory of the target device.
During verification, the progress status is displayed in the action log window to indicate programmer operation. This progress status display window displays the progress status of target device verification by percentage.
Upon completion of [Verify] command execution, the GUI software displays the result of executing the command on the target device.

(5) [Security] command

This command is not supported.

(6) [Checksum] command

The [Checksum] command reads the checksum value of the target device connected with the FPL.
This value differs from the value displayed in the parameter window of the main window.

(7) [Autoprocedure(EPV)] command

The [Autoprocedure(EPV)] command executes the [Erase] command, [Program] command and [Verify] command in succession.
When a user program is to be resent to the target device for comparison with the data written to the flash memory of the target device because of a user program communication error, execute the [Program] command by selecting [Device] → [Setup] and specifying 'Command options' on the Advance tab, then set the automatic execution of the [Verify] command.
During EPV execution, the progress status is displayed in the action log window to indicate programmer operation. For a selected command, its execution operation, and messages, refer to **CHAPTER 8 HOW TO USE FPL**.
Upon completion of [Autoprocedure(EPV)] command execution, the GUI software displays the result of executing the command on the target device.

(8) [Signature read] command

The [Signature read] command reads the signature information (device name, flash memory information, and so forth) of the target.

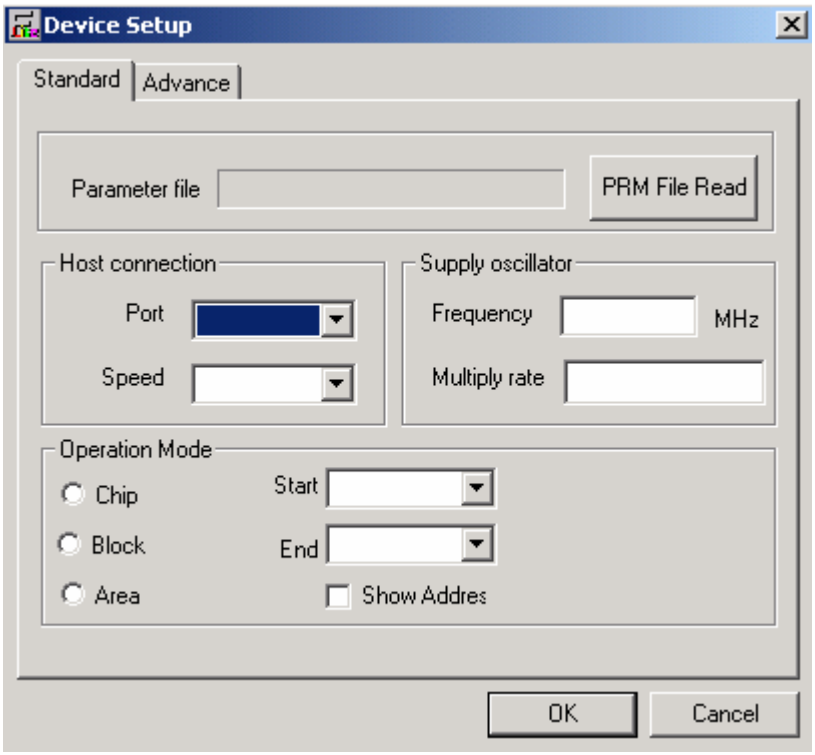
(9) [Setup] command

The [Setup] menu allows you to make settings related to flash memory rewriting according to the user environment and to set command options. Each time the GUI software is started, the most recently used parameter file (.PRM) is read and the settings are displayed. The [Setup] menu allows you to modify the settings of items other than those items consisting of shadowed characters according to the user environment.

(a) Standard setup

This menu is used to set the environment for rewriting the flash memory of the target device.
The mode of communication with the target, the operating clock, and so forth differ depending on the device used. For details, refer to the manual of the device used, when making settings.
The window shown below is opened.

Figure 40: Device Setup Window - Standard



This window shows all basic options that can be set in accordance with the user environment and target device.

[OK button]
Clicking the OK button saves the settings on the Standard and Advance menus and closes the window.

[Cancel button]
Clicking the Cancel button closes the window without saving the settings on the Standard and Advance menus.

<1> Parameter file

This file holds parameters and timing data required to rewrite the flash memory of the target device. Do not modify the data in the parameter file because the data is related to the guarantee of rewrite data.

The parameter file is protected by the checksum function. If the checksum result indicates an error, the FPL does not accept the parameter file.

Figure 41: Setup Window - Parameter File Selection

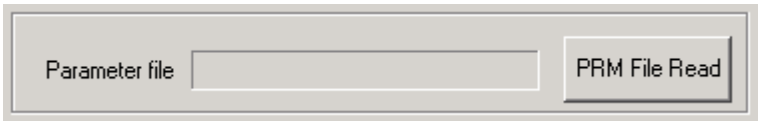
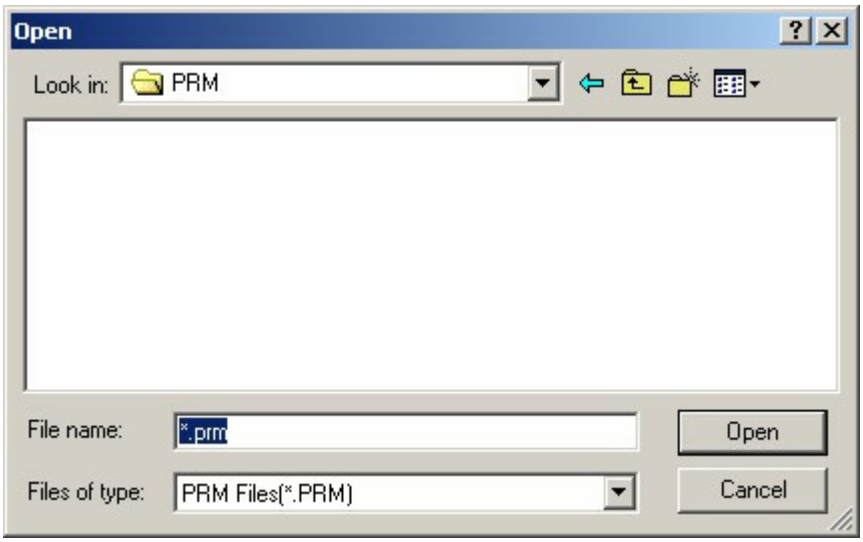


Figure 42: Parameter File Selection Window



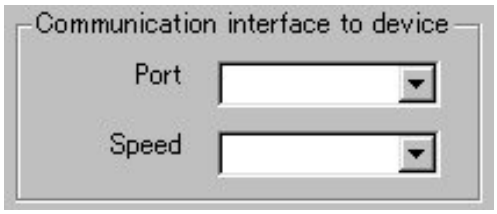
[PRM File Read button]

A window for specifying a parameter file is displayed. Specify a desired file then click Open.

<2> Communication interface to device

"Communication interface to device" is used to select a channel for communication between the *EB-V850ES/KJ1+-EE* board and host machine.

Figure 43: Setup Window - Communication interface to device



[Port list box]

Select a channel for communication between the *EB-V850ES/KJ1+-EE* board and host machine.

- COM1 to COM16

Remark Selectable ports can be checked using Device Manager. For details, refer to **CHAPTER 6.5 Confirmation of USB Driver Installation**.

[Speed list box]

Select a communication rate for the selected communication channel from the following:

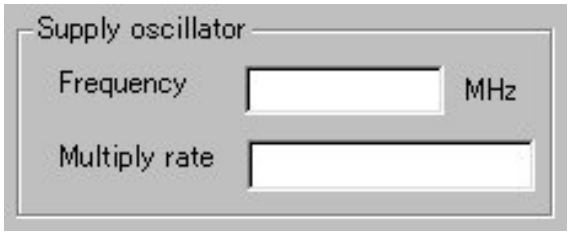
- 9600 bps
- 19200 bps
- 38400 bps

Remark For selectable communication rates, refer to the user's manual of the device used.

<3> Supply oscillator

"Supply oscillator" is used to select a clock that determines programming, data transfer, and a transfer rate.

Figure 44: Setup Window - Supply Oscillator Selection



[Frequency box]

Sets the clock frequency of the target system.

The range of operating frequency varies from one device to another. So, check the specifications of the device used before making a setting.

[Multiply rate]

Specifies the division rate or multiplication rate of the target device.

If the target device has an on-chip PLL circuit, enter a division rate or multiplication rate according to the use environment.

The selectable division rate or multiplication rate differs depending on the device. Check the specifications of the device used before making a setting.

If the target device does not have an on-chip PLL circuit, select "1.0".

On the initial screen, the default setting is displayed according to the parameter file.

<4> Operation Mode

The setting of "Operation Mode" may divide the flash memory of some target devices into blocks or areas.

This menu is used to select an operation mode of the flash memory. Some devices do not have the block and area division modes, and some devices have only one of the modes. In these cases, a nonexisting mode is unchoosable.

Figure 45: Setup Window - Operation Mode

[When Chip is selected]

The entire flash memory area of the target device is subject to rewrite processing.

[When Block is selected]

Specify the Block number range subject to rewrite processing by using Start/End.
The Start/End list boxes display the Block numbers where the flash memory of the target device is configured.

[When Area is selected]

Specify the Area number range subject to rewrite processing by using Start/End.
The Start/End list boxes display the Area numbers where the flash memory of the target device is configured.

[Show Address check box]

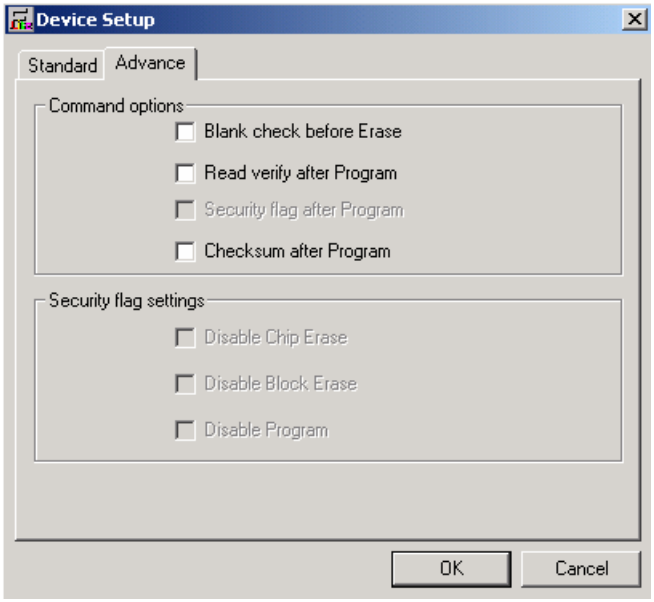
Specify whether numbers or addresses are displayed in the Start/End list boxes.
If this check box is checked, addresses are displayed.
If this check box is not checked, numbers are displayed.

(b) Advance setup

The Advance setup menu is used to specify the command options and security flag settings.

When "Advance" is clicked, the following window is displayed:

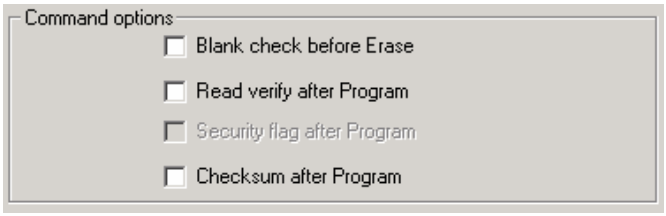
Figure 46: Device Setup Window - Advance



<1> Command options

This dialog box is used to specify the FPL flash processing command options.

Figure 47: Setup Window - Command options



[Blank check before Erase check box]

If this check box is checked, blank check is made before the Erase command or EPV command is executed.

If the result of a blank check indicates OK, erase processing is not executed.

[Read verify after Program check box]

If this check box is checked, write data is sent from the programmer after execution of the Program command and EPV command, then the data is verified against the data written to the flash memory.

[Security flag after Program check box] Not usable

[Checksum after Program check box]

If this check box is checked, the flash memory checksum value of the target device is read from the target device after execution of the Program command and EPV command.

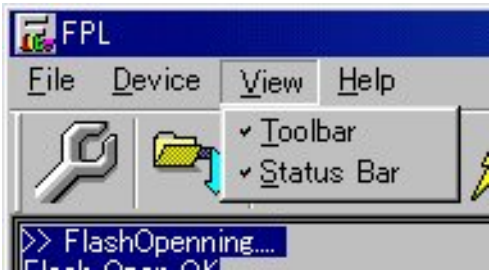
This value differs from the value displayed in the parameter window of the main window.

<2> Security flag settings Not usable

7.4.3 [View] menu

Clicking the [View] menu displays the pull-down menu shown below.
This menu contains commands for setting whether to display the toolbar and status bar.

Figure 48: [View] Menu



(1) [Toolbar] command

Checking the [Toolbar] command displays the toolbar. Unchecking the command hides the toolbar.

(2) [Status Bar] command

Checking the [Status Bar] command displays the status bar. Unchecking the command hides the status bar.

7.4.4 [Help] menu

Clicking the [Help] menu displays the following pull-down menu:

Figure 49: [Help] Menu

(1) [About FPL] command

The [About FPL] command opens the program entry window as shown below and indicates the version.

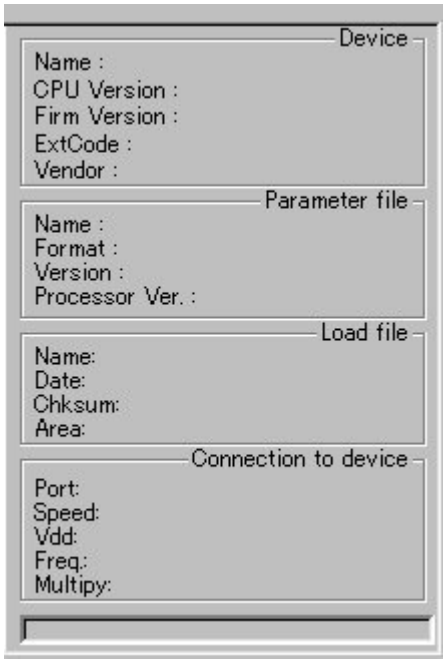
Clicking OK terminates the display.

Figure 50: About FPL Window

7.5 Programmer Parameter Window

This window displays the settings of the programming parameters.

Figure 51: Programmer Parameter Window



[Device]
Updated after communication with the target device to display information about the target device.

[Parameter file]
Updated after [Setup] command execution to display information about a read parameter file.

[Load file]
Updated after [Load] command execution to select information about a selected program file.

[Connection to device]
Updated after [Setup] command execution to display information about the connection with the target device.

8. How to use FPL FLASH programming software

This chapter explains the basic operations of the FPL GUI for programming the *EB-V850ES/KJ1+-EE* board. This chapter covers how to start the system, execute the EPV command, and program the target V850ES/KJ1+ device.

The conditions of the series of operations described in this chapter are as follows:

Hardware configuration of *EB-V850ES/KJ1+-EE*:

Board	:	*EB-V850ES/KJ1+-EE*
CPU	:	V850ES/KJ1+
Target device	:	μPD70F3318
Clock	:	5 MHz
Voltage level	:	5 V

Software configuration of FPL:

Parameter file:		70F3318.PRM
Clock setting	:	5 MHz Multiplied by 4
Port	:	COM4 (38400 bps)
Operation mode:		Chip
Write HEX	:	KJ1_DEMO.hex
Option setting	:	Blank check before Erase

(1) Installing the FPL GUI software

Install the FPL GUI software on the host machine you are using, by referring to **CHAPTER 6 SOFTWARE INSTALLATION** (if the software has not been installed yet).

(2) Installing the driver

Install the USB driver on the host machine you are using, by referring to **CHAPTER 6 SOFTWARE INSTALLATION** (if the driver has not been installed yet).

(3) Installing the parameter file

The parameter file for the V850ES/KJ1+ device is installed automatically during installation of FPL GUI, folder <FPL install-path>\PRM. Nevertheless, newest version of parameter file for the μPD70F3318 device can by download from the NEC Electronics Web site.

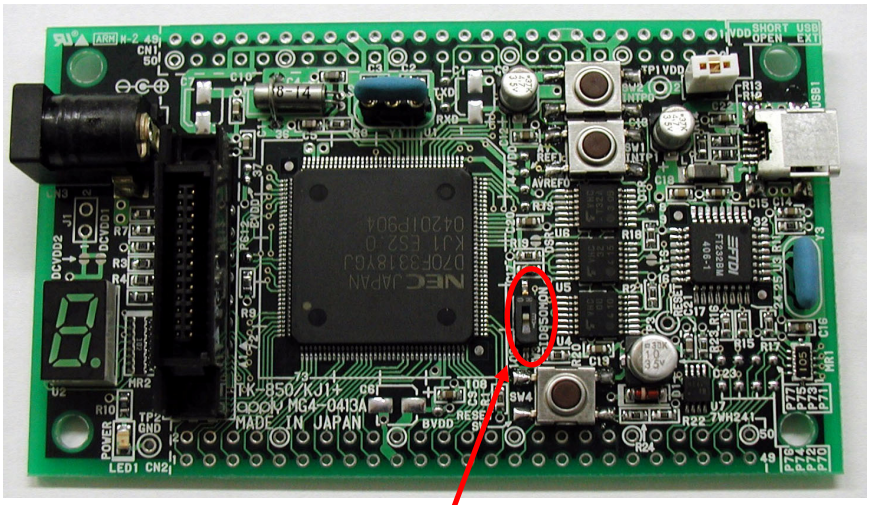
Download the parameter file for the PG-FP4 from the following NEC Electronics Web site:

http://www.ee.nec.de/updates

Copy the parameter file downloaded from the NEC Electronics Web site into sub-directory <FPL.EXE-install-path>\PRM created during GUI software setup (refer to **CHAPTER 6 SOFTWARE INSTALLATION**)..

(4) Connecting and starting

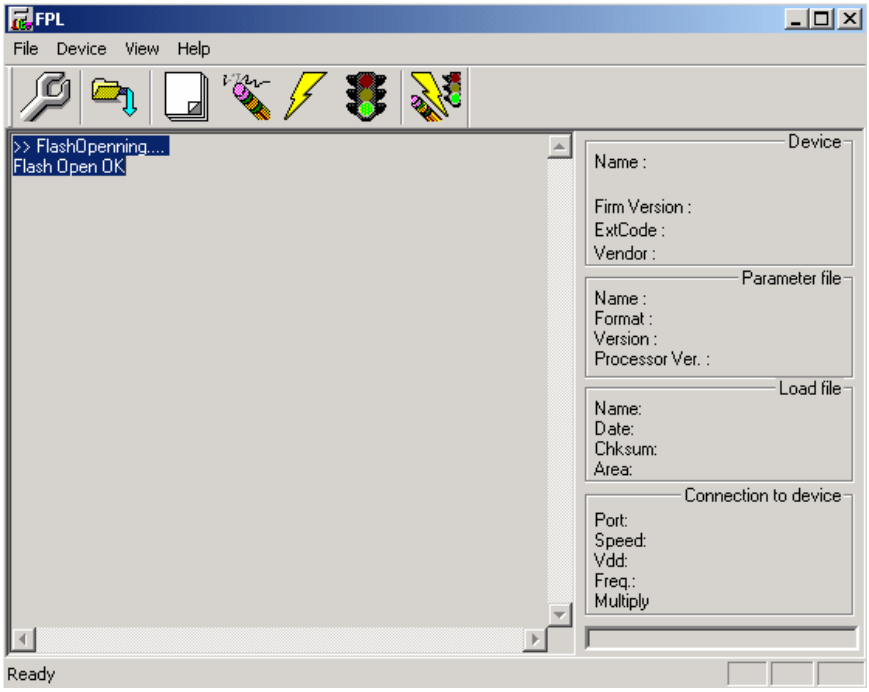
<1> Set the *EB-V850ES/KJ1+-EE* board to the FLASH programming mode by switching SW3 to ON:



<2> <Plug and Play> Connect the *EB-V850ES/KJ1+-EE* board with the host machine via the USB cable. If the connection was already done, press the reset button SW4 to release the FLASH programming mode.

<3> Start the FPL GUI.

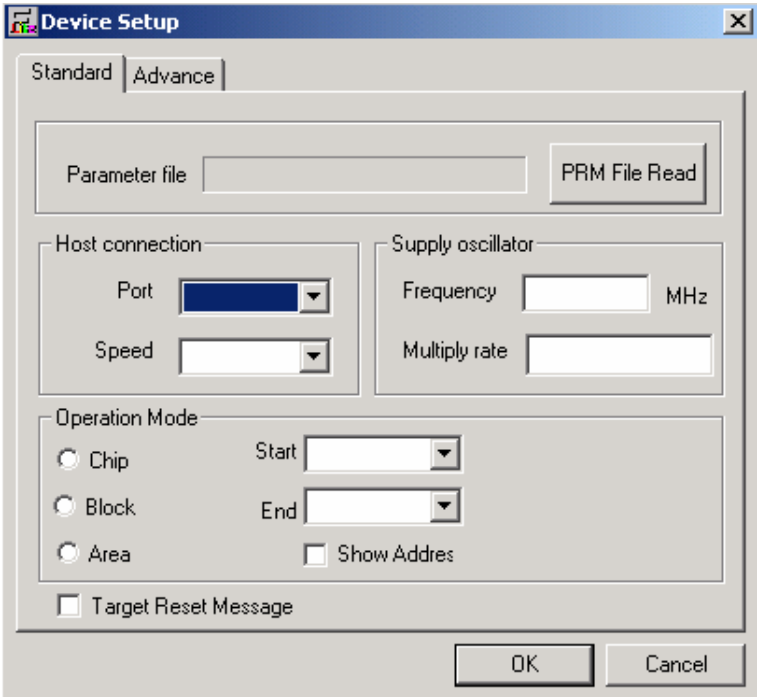
Figure 52: GUI Software Startup Screen



(5) Setting the programming environment

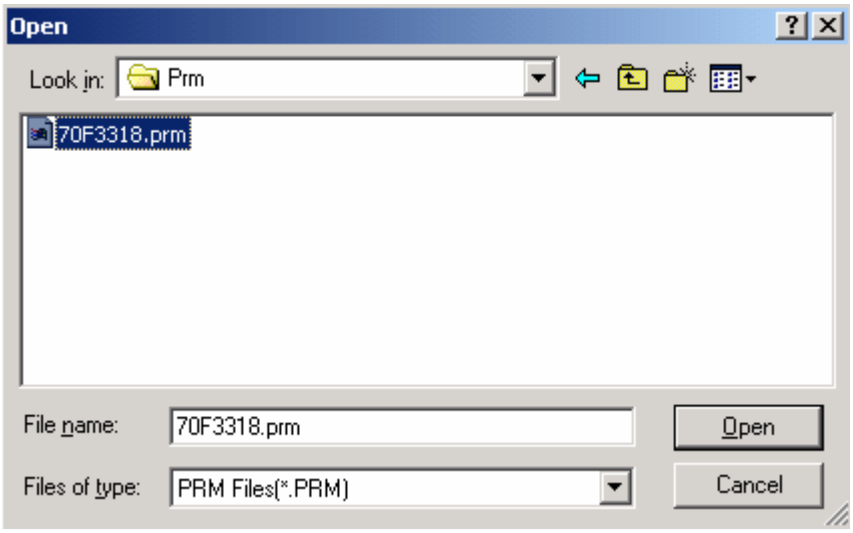
<1> Select [Device] → [Setup] from the menu bar.
<2> The Standard dialog box for device setup is activated.

Figure 53: <Standard Device Setup> Dialog Box



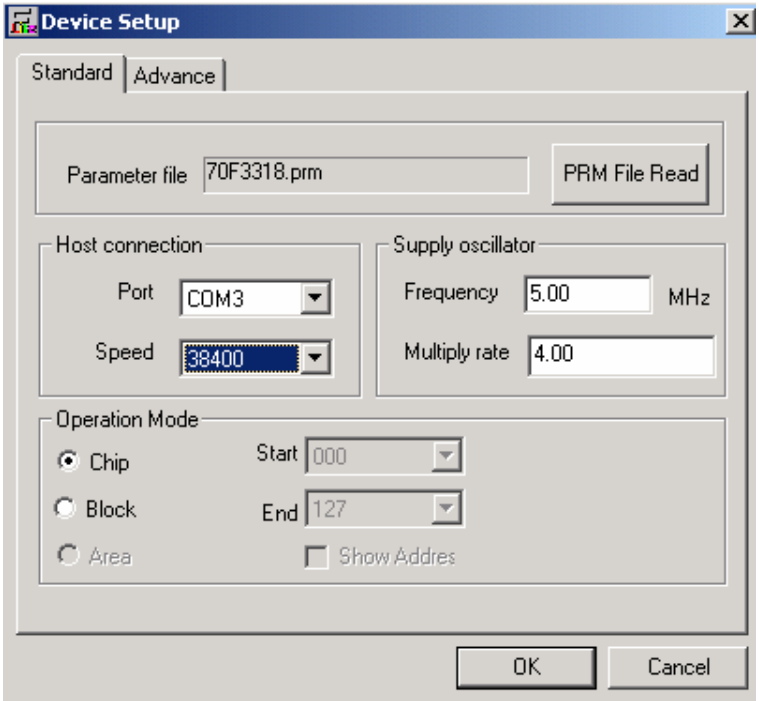
<3> Click PRM File Read to open the parameter file selection window.
Select the parameter file “70F3318.prm” then click Open.

Figure 54: Parameter File Selection



<4> From the Port list box, select the communication port that matches the host machine being used. Select the communication speed of the Host connection.

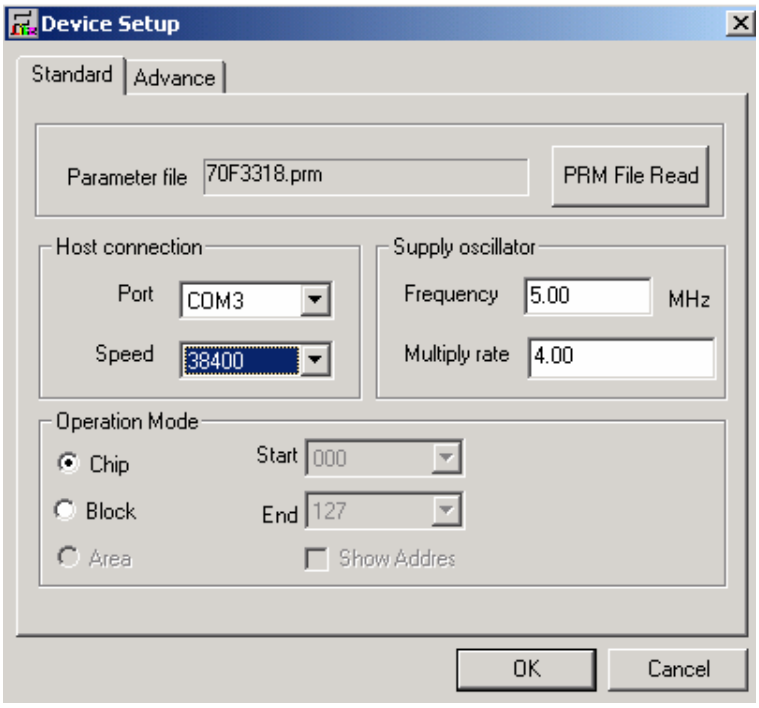
Figure 55: Port Selection



Remark Selectable ports can be checked using Device Manager. For details, refer to **CHAPTER 6.5 Confirmation of USB Driver Installation**.

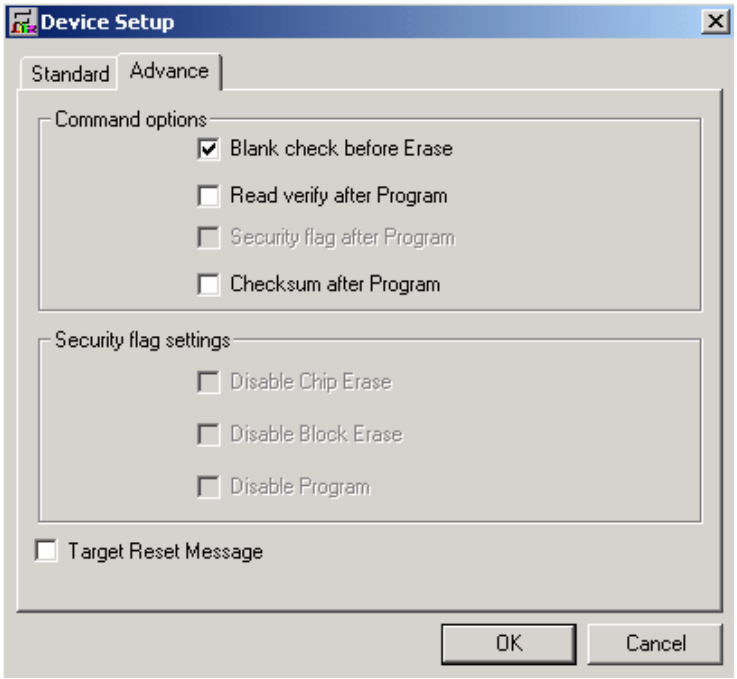
<5> Set "Supply oscillator" according to the specifications of the *EB-V850ES/KJ1+-EE* board, “Frequency = 5.00 MHz” and “Multiply rate = 4.00”. In "Operation Mode", please specify the “Chip” mode. The following figure shows the recommended settings:

Figure 56: <Standard Device Setup> Dialog Box after Setting



<6> Switch to the Advance dialog box.

Figure 57: <Advance Device Setup> Dialog Box

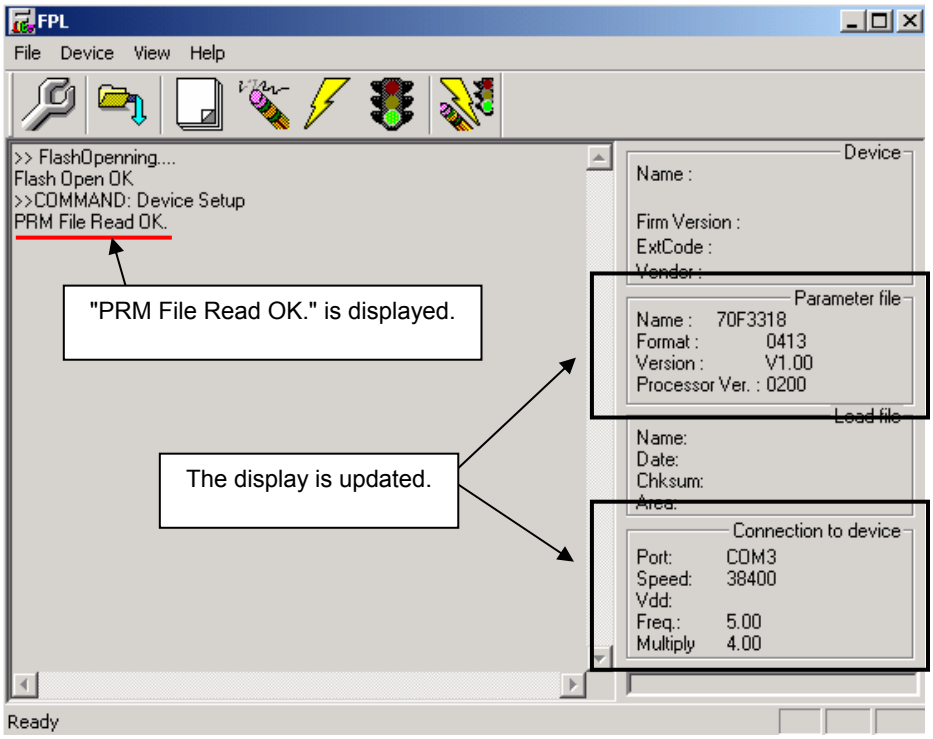


<Command options>

Blank check before Erase : Checked

<7> Click the OK button. The GUI software sets the parameters.
When the settings have been completed, the following screen is displayed:

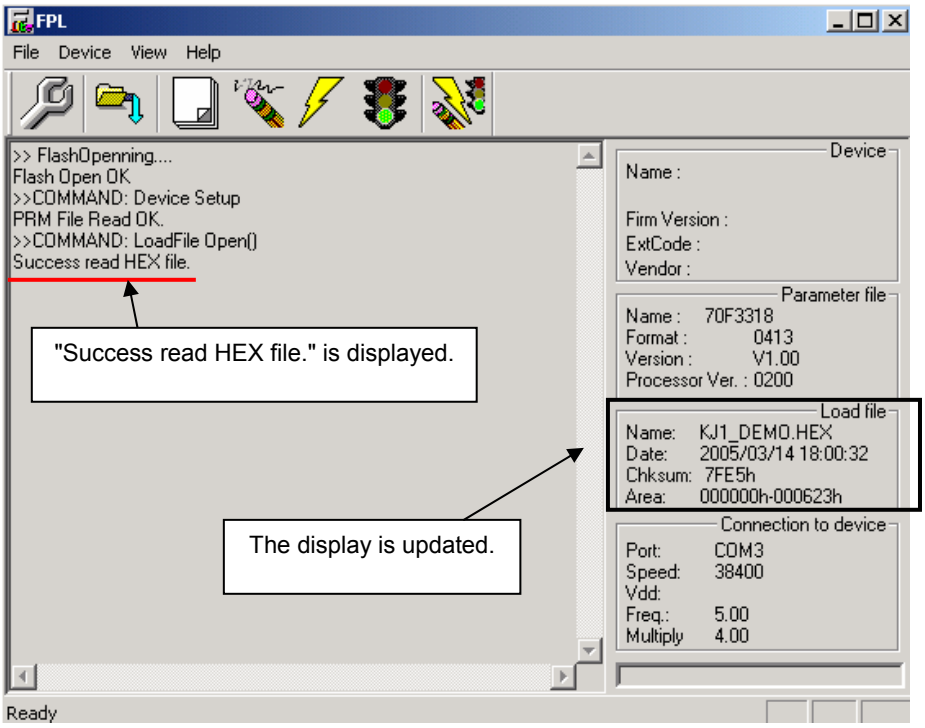
Figure 58: Completion of Parameter Setting



(6) Selecting a user program

<1> Select [File] → [Load].
<2> Select a program file to be written to the target device, then click Open.

Figure 59: After Downloading

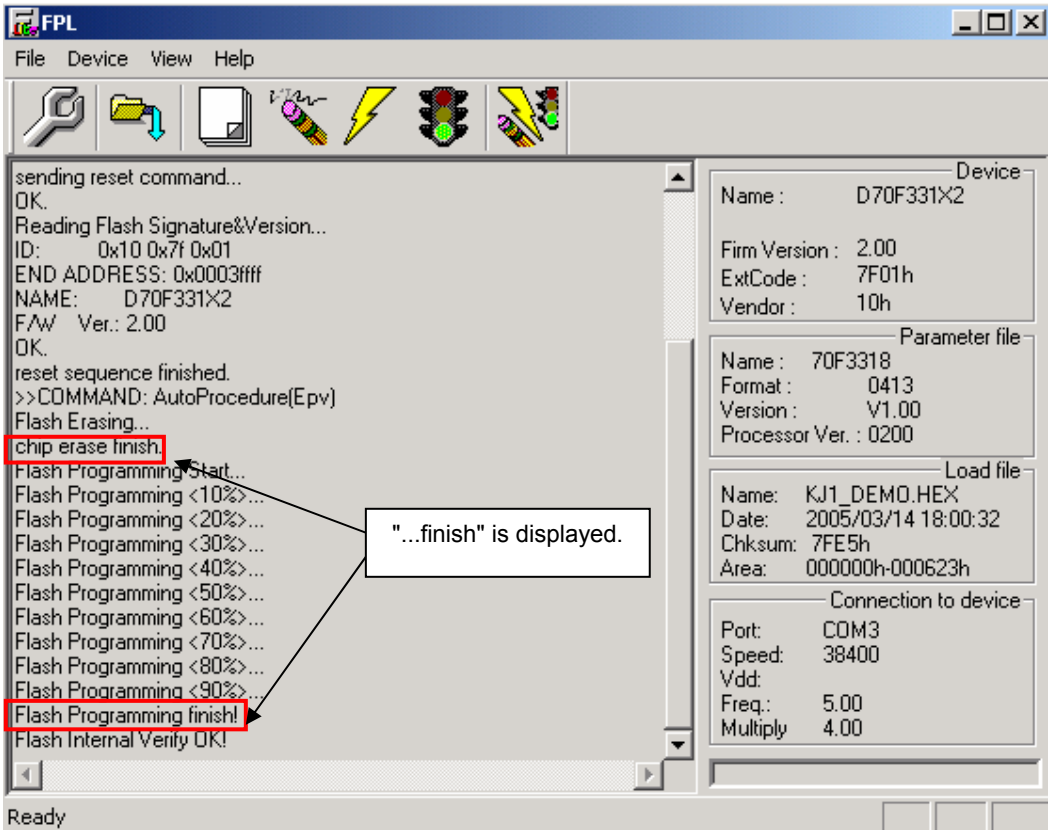


(7) [Autoprocedure(EPV)] command execution

Select [Device] → [Autoprocedure(EPV)] from the menu bar.

When the [Autoprocedure(EPV)] command is executed, Blank Check → Erase → Program and FLASH Internal Verify are executed sequentially for the μPD70F3318 device.

Figure 60: After EPV Execution



(8) Terminating the GUI

Select [File] → [Quit] to terminate the GUI software. All settings executed so far are saved in the FPL.INI file, so that those settings can be reused when the GUI software is restarted.

(9) Execute "KJ1_DEMO" application

Set the *EB-V850ES/KJ1+-EE* board to the normal operation mode by switching SW3 to OFF.

< Plug and Play> the *EB-V850ES/KJ1+-EE* board to start in normal operation mode or press the reset button SW4 to release the normal operation mode.

(10) Restarting the GUI

When the system is restarted, the same screen as shown in Figure 58 appears.

9. TROUBLESHOOTING

In driver installation, recognition based on Plug and Play is disabled.

Cause:
The USB connector may not be inserted normally into the USB port of the personal computer.
Action:
Check that the USB connector is inserted fully into the USB port of the personal computer. Alternatively, disconnect the USB connector, then insert the USB connector again after a while.

The driver file cannot be found at a specified location.

Cause:
The FPL FLASH programming software may not be installed correctly.
Action:
Install the GUI software again by referring to **CHAPTER 6 Software Installation**.

In checking by Device Manager, "USB Serial Port" or "USB High Speed Serial Converter" is not displayed. Alternatively, the "!" or "×" is prefixed.

Cause:
The USB connector may not be inserted normally into the USB port of the personal computer.
Action:
Check that the USB connector is inserted fully into the USB port of the personal computer. Alternatively, disconnect the USB connector from the USB port, then insert the USB connector again after a while.

Cause:
The driver may not be installed correctly.
Action:
<1> When this product is connected to the personal computer, right-click the driver marked with "!" or "×".
Click Erase when displayed.
<2> On Device Manager, execute [Hardware Modification Scan].
<3> Install the driver again with Plug and Play.

Cause:
The device may not be recognized (in the case of connection with the USB hub).
Action:
Try the following:
- Disconnect the USB connector, then insert the USB connector again.
- Connect the USB connector to another port of the USB hub.

If the same symptom occurs, do not use the USB hub, but directly connect the connector to the USB port of the personal computer.

When this product is connected with a personal computer, the "Add New Hardware Wizard" screen is displayed.

Cause:
If the USB connector of this product is not inserted into the USB port used at the installation time but into another USB port, this product may be recognized as a new hardware item.
Action:
Install the driver by referring to **CHAPTER 6.4 USB Driver Installation**.

Communication with the *EB-V850ES/KJ1+-EE* board is disabled.

Cause:
The driver may not be installed correctly.
Action:
Check if "USB Serial Port" and "USB High Speed Serial Converter" are installed correctly by referring to **CHAPTER 6.4 USB Driver Installation**.

Cause:
The COM port selected via the “Port list box” within device setup menu of FPL may not be set correctly.
Action:
Set the port checked using Device Manager.

Cause:
The *EB-V850ES/KJ1+-EE* board is operating in normal mode.
Action:
Set the board to the FLASH programming mode by setting SW3 to ON.

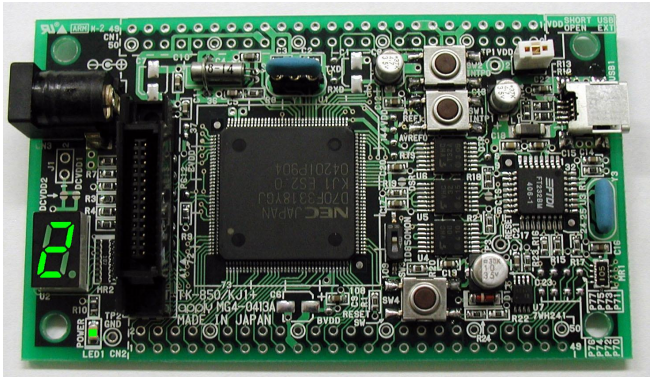
Cause:
The PRM file selected in [Device Setup] may be incorrect.
Action:
Use the corresponding PRM file that matches the target device. For information about the PRM file, refer to **CHAPTER 7 FPL FLASH programming software.**

Cause:
The setting of "Supply oscillator" in [Device Setup] may be incorrect.
Action:
Make a correct setting according to the specifications of the target device.

10. Sample program

The software package contains a sample program demonstrating the board features of the *EB-V850ES/KJ1+-EE* board. There are two versions of the sample project available. One sample project is based on the Green Hills Development Environment for V850, Version 4.0.5 and the other one on the IAR Systems Embedded Workbench for V850, Version 3.10A. The Green Hills project is located in the `/ghs` directory and IAR project in the `/iar` directory.

The sample program realizes a simple up / down counter. After program start the watch timer is initialized to generate a 0.5 sec counter reference, based on the 32.768 kHz sub-clock. The actual count value is displayed by driving the 7 segment LED U2. By pressing button SW1 and SW2 the count direction can be changed. Additionally the actual count value is transferred via UART0 to a terminal program running on the host machine. The data transfer speed is set to 115200 bps per default.



To start first trials based on the *EB-V850ES/KJ1+-EE* starterkit the IAR Embedded Workbench for V850 including the IAR C-SPY debugger / simulator is part of software tool package. This version is restricted in such that maximum program code size is limited to 16 kByte. For details of using the IAR Embedded Workbench and the IAR C-SPY debugger / simulator please refer to the corresponding manuals.

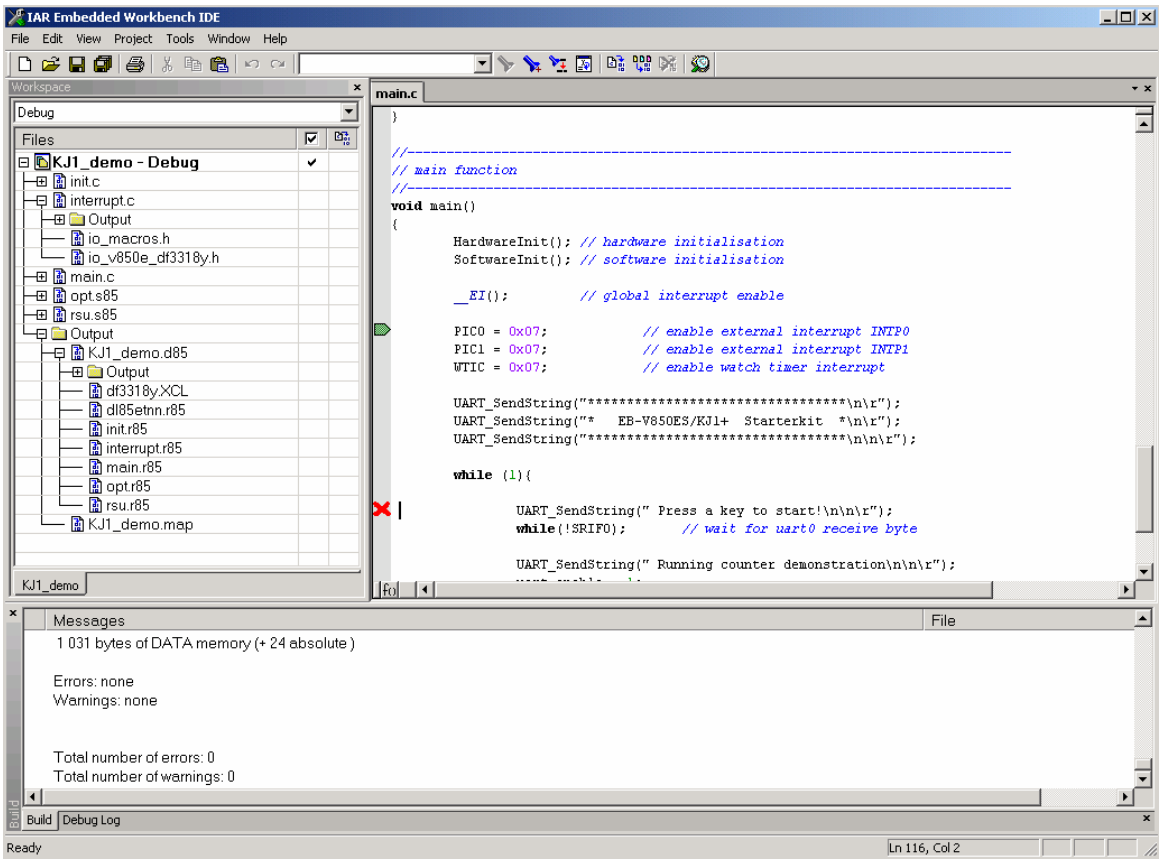


Figure 61: IAR Embedded Workbench V850

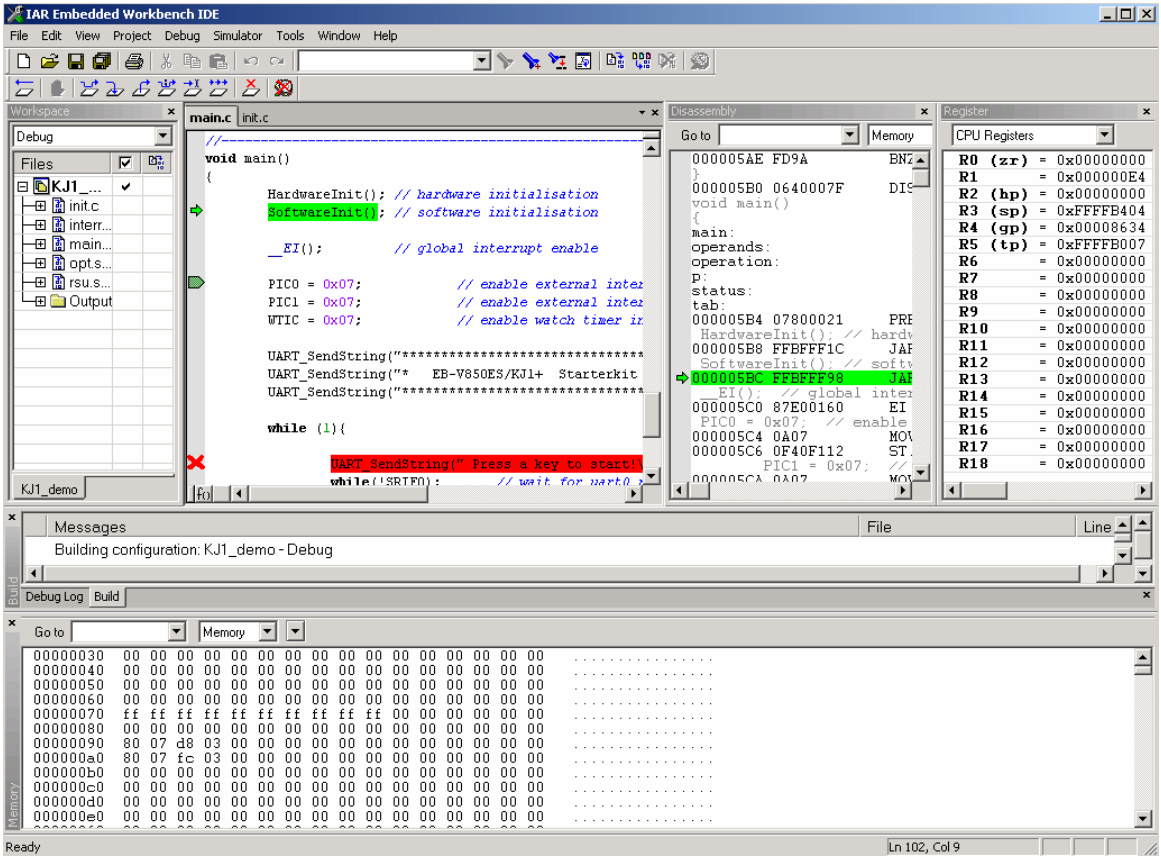


Figure 62: IAR C-SPY Debugger / Simulator V850

11. Connectors and Cables

11.1 USB host connector USB1

Figure 63: Connector USB1, USB Mini-B Type Host Connector Pin Configuration

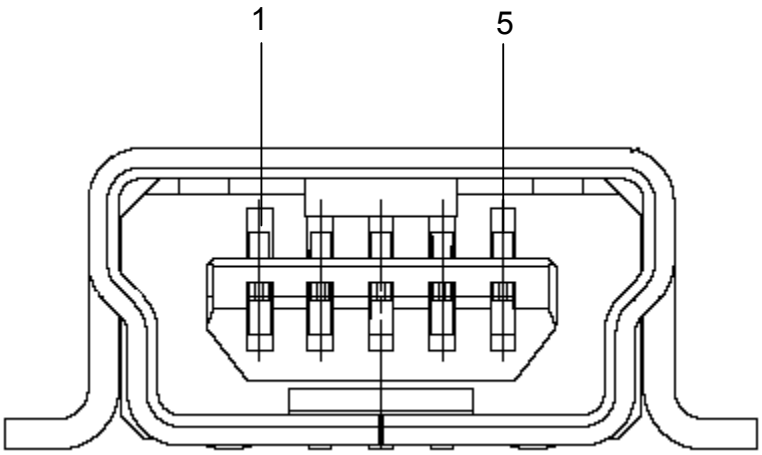


Table 12: Pin Configuration of USB Connector USB1

USB Connector USB1	Signal Name
1	VBUS
2	D-
3	D+
4	N.C.
5	GND

For connection with the host machine, use a USB cable (Mini-B type). For confirmation, NEC Electronics used only the USB cable delivered with the *EB-V850ES/KJ1+-EE* board.

11.2 USB interface cable (Mini-B type)

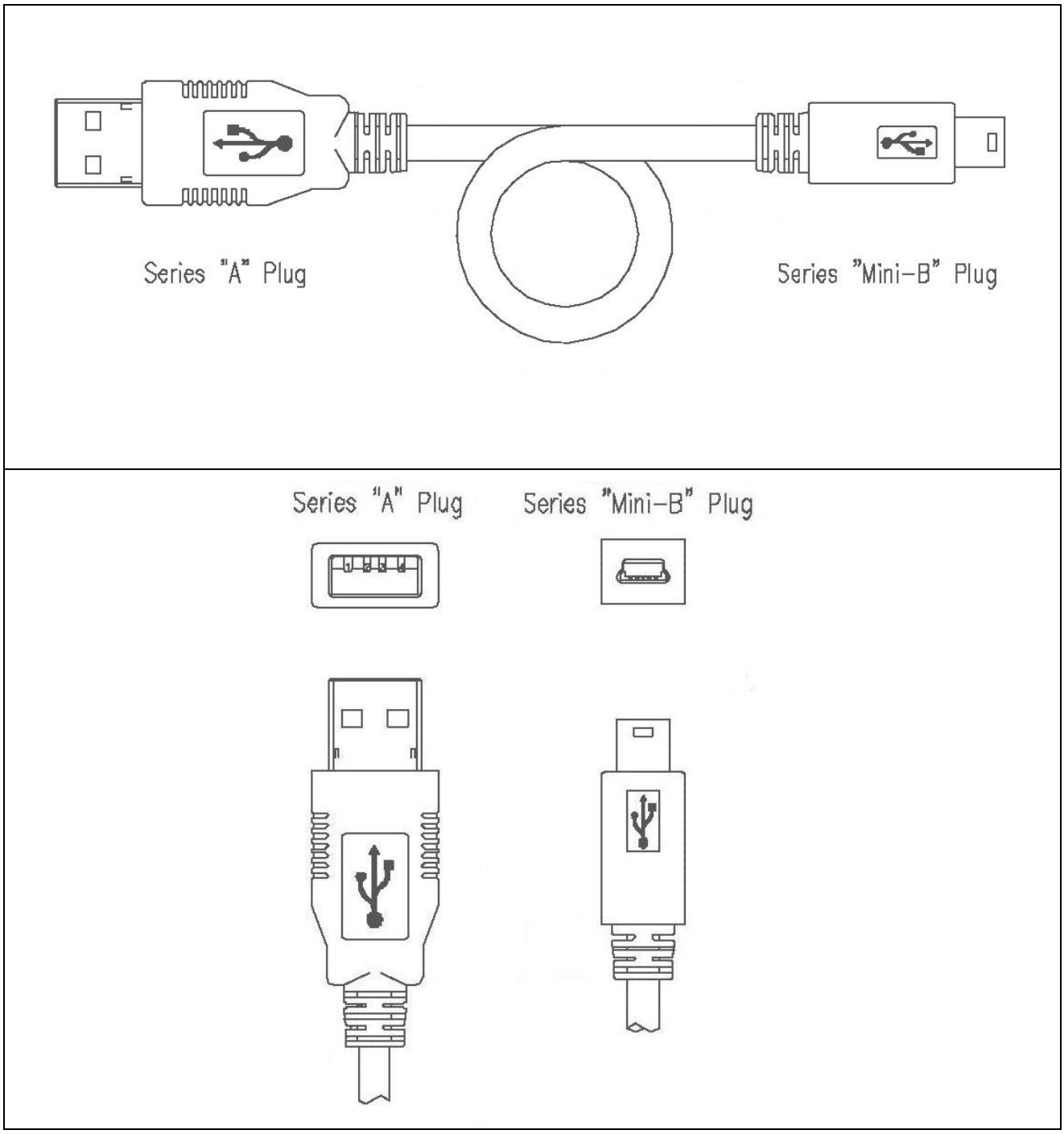


Figure 64: USB interface cable (Mini-B type)

12. Schematics

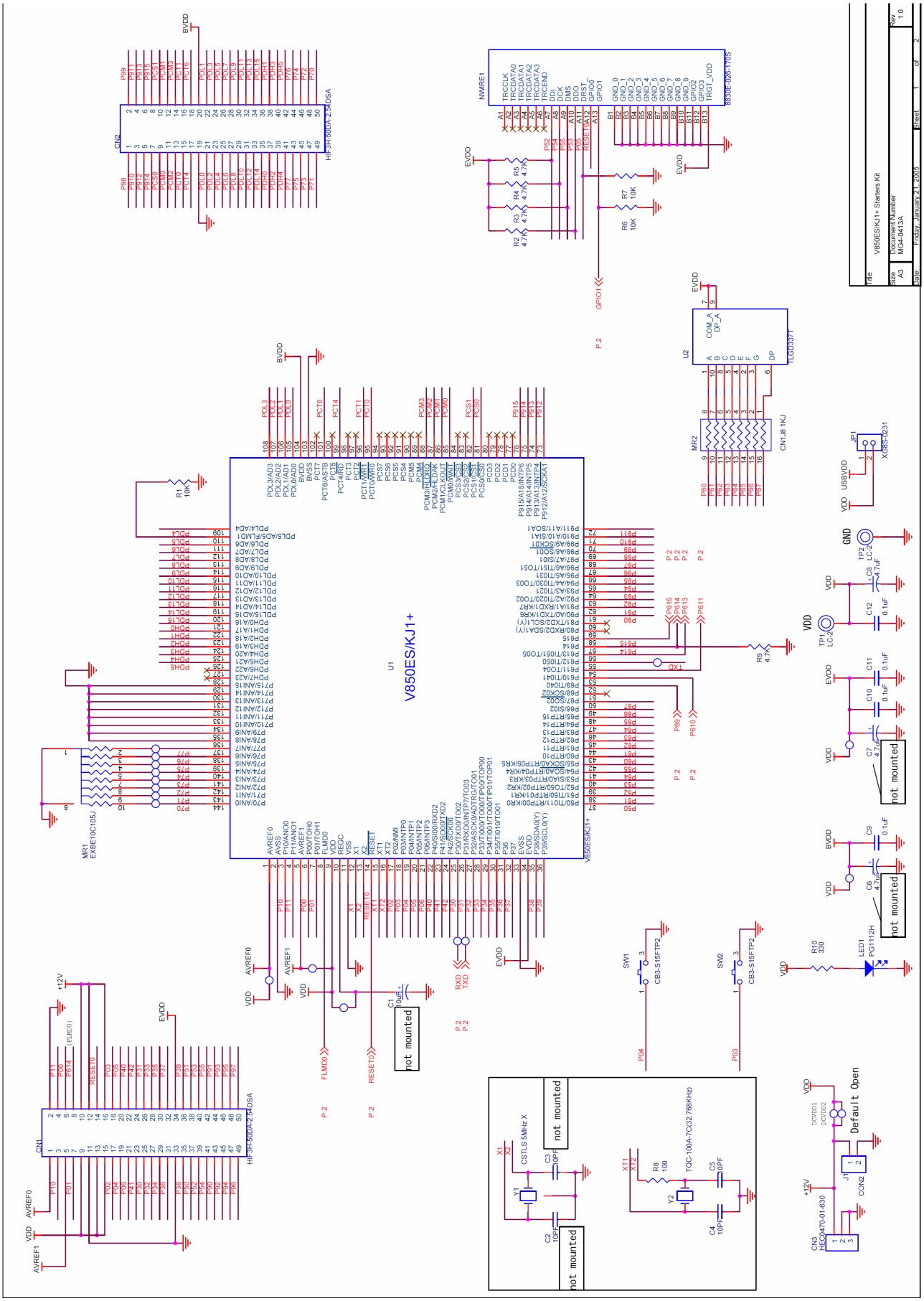


Figure 65: EB-V850ES/KJ1+-EE board schematics 1/2

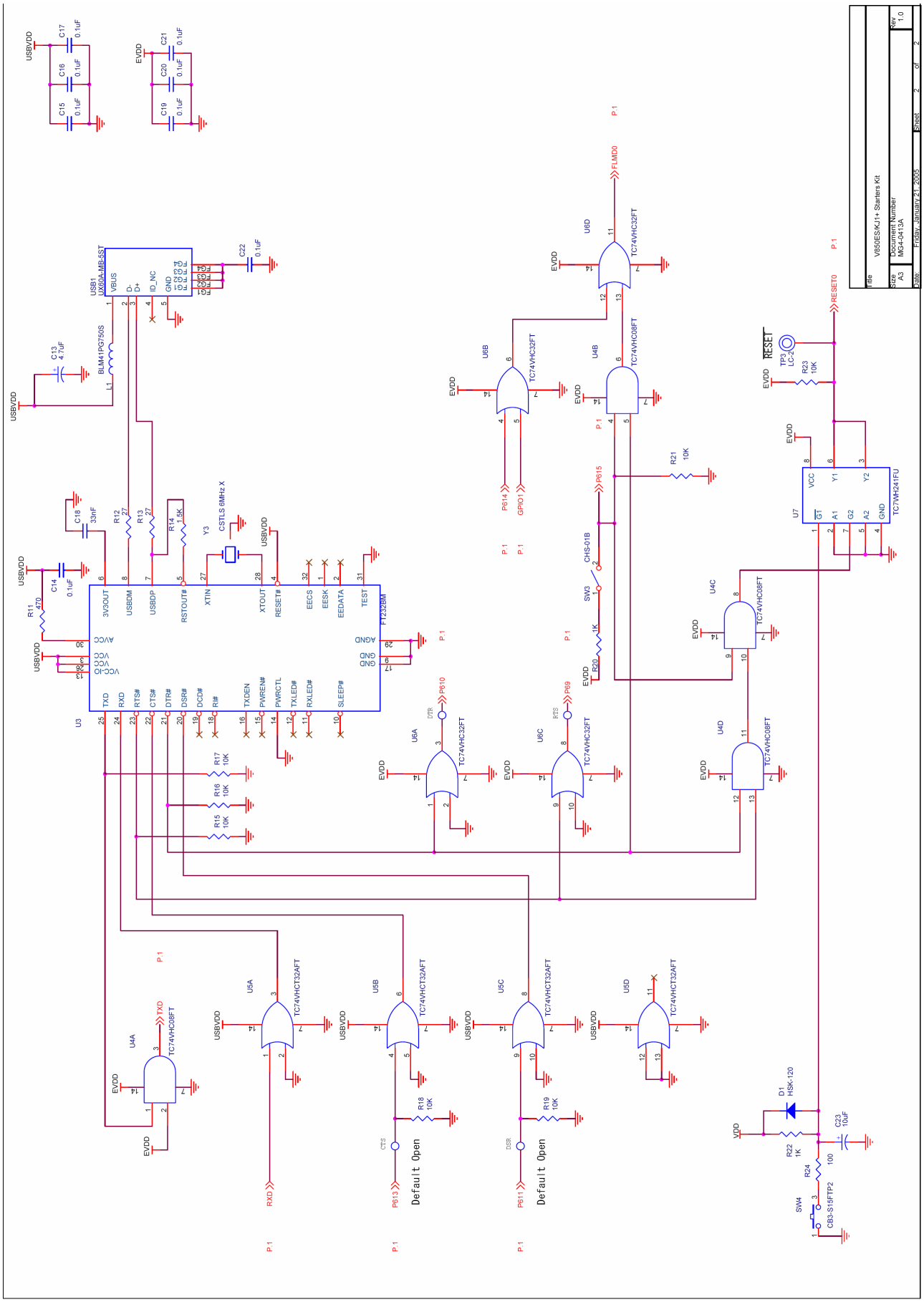


Figure 66: *EB-V850ES/KJ1+-EE* board schematics 2/2