E2 Emulator, E2 Emulator Lite, E1/E20 Emulator

Supplementary Manual: Connection of RH850/F1KH and RH850/F1KM Devices

Supported Devices:

RH850 Family

RH850/F1KH Group

RH850/F1KM Group

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Contact us if you have any questions about the precautions described here.

WARNING WARNING indicates a potentially dangerous situation that will cause death or heavy wound unless it is avoided.

CAUTION CAUTION indicates a potentially dangerous situation that will cause a slight injury or a medium-degree injury or property damage unless it is avoided.

To avoid a possible danger, the following diagrammatic symbols are used to call your attention.

△ means WARNING or CAUTION.

Example:  CAUTION AGAINST AN ELECTRIC SHOCK

⃠ means PROHIBITION.

Example:  DISASSEMBLY PROHIBITED

● means A FORCIBLE ACTION.

Example:  UNPLUG THE POWER CABLE FROM THE RECEPTACLE.

⚠ WARNING

Warnings for AC Power Supply:

Do not repair or remodel the emulator product by yourself in order to prevent danger such as an electric shock or fire and for the sake of quality assurance. For after-sale services in case of a mechanical or electrical fault, please contact your local distributor.

Always switch off the Host machine and user system before connecting or disconnecting any cables or parts. Neglect of this precaution will result in getting an electric shock or will result in the emulator product or user system emitting smoke or catching fire. Also, the user program under debug will be destroyed.

Make sure that the connectors on both ends of the user-system interface cable are facing the right way relative to the user-side connector on the emulator and the connector on the user system, respectively.

Neglect of this precaution will result in getting an electric shock or will result in the emulator product or user system emitting smoke or catching fire.

Warning for Modification:

Do not modify the emulator. Personal injury due to electric shock may occur if the emulator is modified. Modifying the product will void your warranty.

Warning for Installation:

Do not set the emulator in water or areas of high humidity. Make sure that the product does not get wet. Spilling water or some other liquid into the product may cause un-repairable damage.

Warning for Use Temperature:

The emulator is to be used in an environment with a maximum ambient temperature of 35°C.

Care should be taken that this temperature is not exceeded.

⚠ CAUTION

Caution to Be Taken for Handling the Emulator:

Exercise caution when handling the emulator. Be careful not to apply a mechanical shock.

Do not touch the connector pins of the emulator and the target MCU connector pins directly. Static electricity may damage the internal circuits.

When attaching and removing the cable, hold the plug of the cable and do not touch the cable. When installing the emulator, do not flex the cable excessively or pull the emulator or the board by the cable connected to it. The cable may cause a break.

Do not tape the flexible cable or apply adhesives to secure the cable. The shielding material on the surface of the cable may come off.

Caution to Be Taken for System Malfunctions:

If the emulator malfunctions because of interference like external noise, do the following to remedy the trouble.

(1) Exit the emulator debugger, and shut OFF the emulator and the user system.

(2) After a lapse of 10 seconds, turn ON the power of the emulator and the user system again, then launch the emulator debugger.

Caution to Be Taken for Disposal:

Penalties may be applicable for incorrect disposal of this waste, in accordance with your national legislation.

WEEE Directive (2012/19/EU)

The Waste Electrical and Electronic Equipment Regulations 2013

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Table of Contents

1. Outline

The Renesas emulators—E2 Emulator, E2 Emulator Lite, E1 Emulator, and E20 Emulator—are tools used in combination with debuggers such as CS+ and e² studio to debug user programs. This manual describes the emulator connection methods and precautions for use when debugging target devices using the E2 Emulator, E2 Emulator Lite, E1 Emulator, or E20 Emulator.

1.1 Target Devices

The target devices covered by this manual are listed below:

RH850/F1KH Group
RH850/F1KM Group

The contents of this manual do not apply to devices other than those listed above.

In addition, within the RH850/F1KH Group and F1KM Group, the configuration settings and usage limitations when using the emulator differ depending on device configurations and supported functions.

1.2 Features of E2 Emulator, E2 Emulator Lite, E1 Emulator, or E20 Emulator

(1) E2 Emulator (RTE0T00020KCE00000R, hereafter referred to as the E2)

The E2 is a standard model emulator equipped with the following features:

- Download function for flash memory and other memories
- Trace function for checking the execution history of user programs
- Execution time measurement function for user programs
- Basic debugging functions

In addition, the E2 can also be used as a flash programming tool (Renesas Flash Programmer, hereafter referred to as the RFP).
In addition to the basic debugging functions supported by RH850 microcontrollers, extended debugging functions can be used.

(2) E2 Emulator Lite (RTE0T0002LKCE00000R, hereafter referred to as the E2 Lite)

The E2 Lite is an entry-level model emulator equipped with the following features:

- Download function for flash memory and other memories
- Basic debugging functions

It is easy to introduce due to its low cost and is suitable for basic debugging purposes.
In addition, the E2 Lite can also be used as a flash programming tool (RFP).

(3) E1 Emulator (R0E000010KCE00, hereafter referred to as the E1)

The E1 is an entry-level model emulator equipped with the following features:

- Download function for flash memory and other memories
- Basic debugging functions

It is easy to introduce due to its low cost and is suitable for basic debugging purposes.
In addition, the E1 can also be used as a flash programming tool (RFP).

(4) E20 Emulator (R0E000020KCE00, hereafter referred to as the E20)

The E20 is a standard model emulator equipped with the following features:

- Download function for flash memory and other memories
- Large-capacity trace memory
- Basic debugging functions

In addition, the E20 can also be used as a flash programming tool (RFP).
The functions used for debugging of the RH850 family by using the E20 are the same as in the E1. Large trace function, a characteristic function of the E20, cannot be used.

1.3 Configuration of manuals

In addition to this manual, be sure to read the Manuals for each emulator unit, the Manual for the target device.

Name of Document	Document No.
E2 Emulator RTE0T00020KCE00000R Manual	R20UT3538E
E2 emulator Lite RTE0T0002LKCE00000R Manual	R20UT3240E
E1 Emulator R0E000010KCE00 E20 Emulator R0E000200KCE00 Manual	R20UT0398E

For the restrictions on the target device, also read the following documents.

- Manual for the target device
- Documents describing restrictions on the target device

2. Connecting the Emulator and User System

This chapter describes the hardware connection methods for connecting each emulator to the RH850/F1KH Group and F1KM Group.

2.1 Connector mounted on the user system

Table 2-1 shows the 14-pin connector recommended for emulator connection by each emulator. When other components are mounted around the connector, do not mount components with heights exceeding 10 mm within 5 mm of the connector on the user system as shown in Figure 2-1.

When designing the user system that mounts the 14-pin connector, refer to this section in this manual and the manual for the target device.

Table 2-1 Recommended Connector

	Type Number	Manufacturer	Specification
14-pin connector	7614-6002	3M Japan Limited	14-pin straight type (Japan)
	2514-6002	3M Limited	14-pin straight type (other countries)

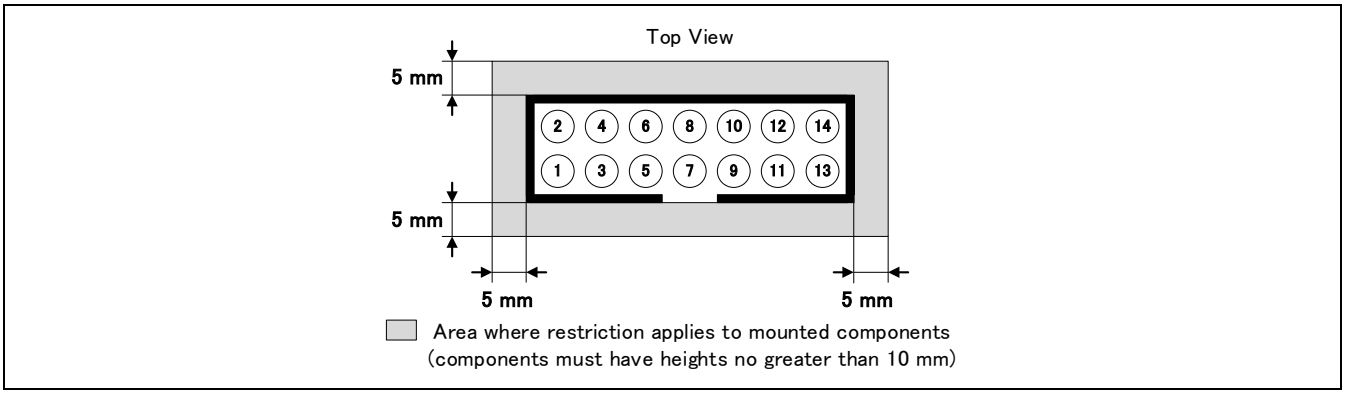


Figure 2-1 Area where Restriction Applies to Mounted Components

- For the connection of the E2 Lite and E1
  Figure 2-2 shows an example of the connection of the user-system interface cable of the E2 Lite and E1 to a 14-pin connector.

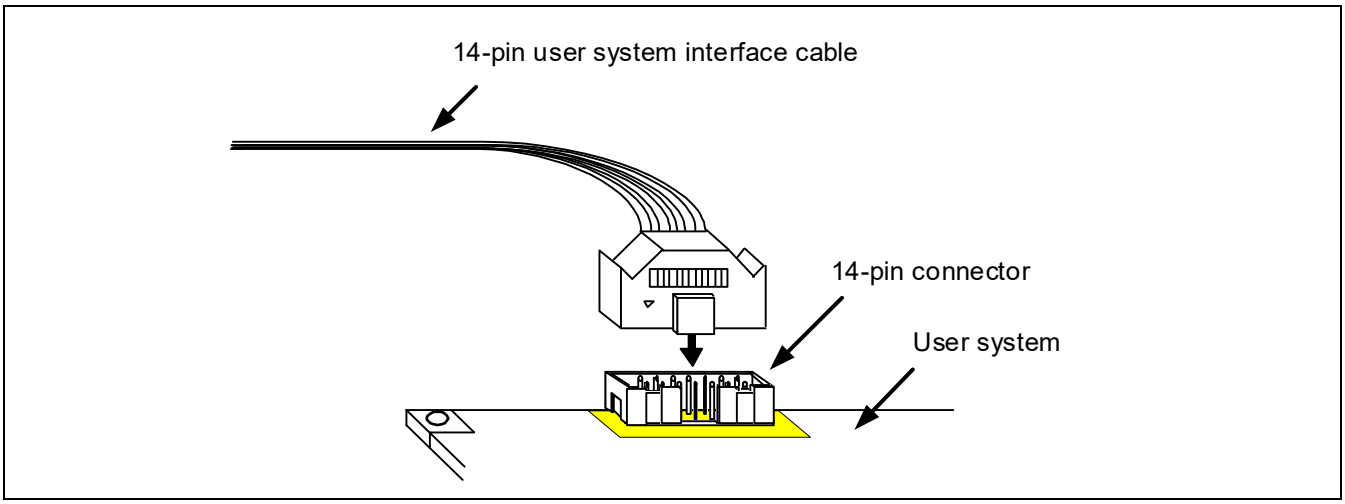


Figure 2-2 Connecting the User-System Interface Cable to the 14-pin Connector in the E2 Lite and E1

Note:

If the E2 Lite is used in combination with the connector conversion adapter and the user-system interface cable supplied with the E2, the debugger cannot establish a connection with the RH850 device.
When using the E2 Lite, be sure to use the user-system interface cable that is supplied with the E2 Lite.

- For the connection of the E20
  To use the E20 with a 14-pin connector, use the 38-pin/14-pin connector conversion adapter [R0E000200CKA00] that comes with the E20.

- For the connection of the E2

  To use the E2 with a 14-pin connector, use the connector conversion adapter that comes with the E2 and the user-system interface cable. Figure 2-3 shows an example of the connection.

  After connecting the user-system interface cable to the connector conversion adapter, connect the connector conversion adapter to the connector on the user system.

  The connector conversion adapter is provided with a switch. Setting for the switch must be on the “1” side for the RH850. Operation is not guaranteed if the switch is on the “3” side. For setting the switch, refer to Table 2-2.

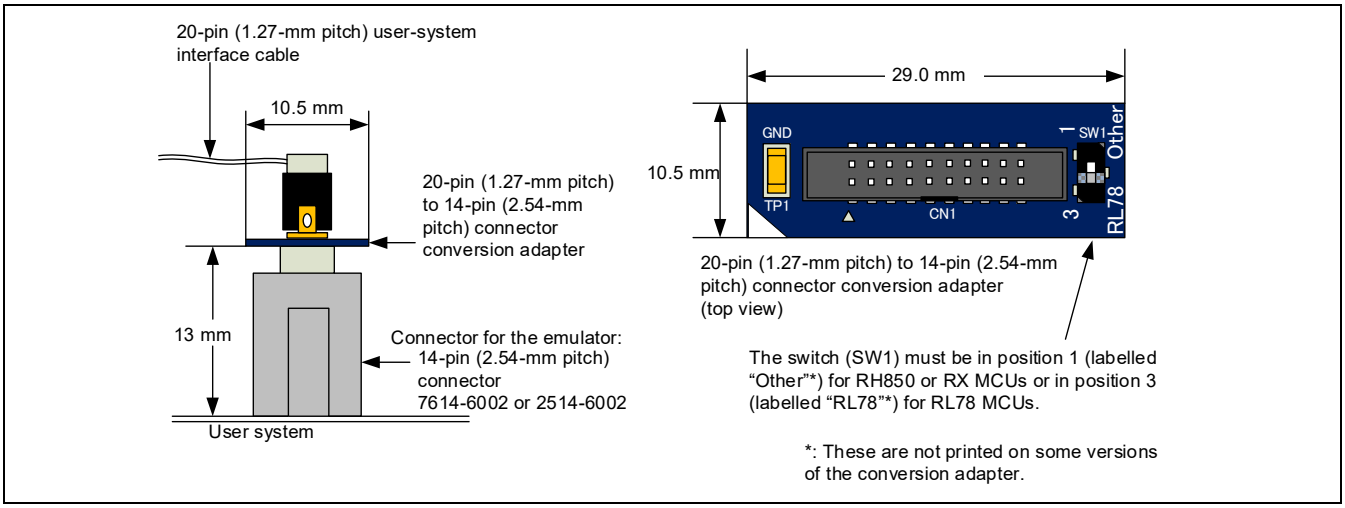


Figure 2-3 Connecting the User-System Interface Cable to the 14-pin Connector in the E2

Table 2-2 Setting of Switches (SW1)

Setting	Description
1	The target device is an RH850 microcontroller (default setting).
3	The target device is an RL78 microcontroller.

CAUTION

Note on connector insertion and removal (1):

When connecting or disconnecting the user-system interface cable and the user system, grasp the connector cover at the end of the cable or both sides of the board of the connector conversion adapter. Pulling the cable itself will damage the wiring.

If a 20-pin (1.27-mm pitch) user-system interface cable of the E2 becomes disconnected, purchase the following maintenance product: RTE0T00020KCAC0000J.

CAUTION

Note on connector insertion and removal (2):

Be aware that the user-system interface cable or the connector conversion adapter must be inserted with the correct orientation. Connecting the user-system interface cable or the connector conversion adapter with the wrong orientation may cause damage.

2.2 Pin assignments of the connector

Table 2-3 shows the pin assignments of the 14-pin connector.

Table 2-3 Pin Assignments of the 14-pin Connector

Pin No.	Pin Name (#: Active Low, -: Not used)						I/O (*4)
	Debugging			Programming			
	4-pin LPD	1-pin LPD	JTAG	2-wire UART	1-wire UART	CSI	
1	LPDCLK	-	TCK	-	-	FPCK	Input
2 (*1)	GND	GND	GND	GND	GND	GND	-
3	LPDRST#	-	TRST#	-	-	-	Input
4	FPMD0	FPMD0	FPMD0	FPMD0	FPMD0	FPMD0	Input
5	LPDO	-	TDO	FPDT	-	FPDT	Output
6	-	-	-	FPMD1	FPMD1	FPMD1	Input
7	LPDI/LPDIO	LPDIO	TDI	FPDR	FPDR	FPDR	Input/Output
8	TVDD	TVDD	TVDD	TVDD	TVDD	TVDD	-
9	-	-	TMS	-	-	-	Input
10 (*3)	EVTO	-	EVTO	-	-	-	Output
11	LPDCLKO	-	RDY#	-	-	-	Output
12 (*1)	GND	GND	GND	GND	GND	GND	-
13 (*2)	RESET#	RESET#	RESET#	RESET#	RESET#	RESET#	Input
14 (*1)	GND	GND	GND	GND	GND	GND	-

Notes: 1. Securely connect pins 2, 12, and 14 of the connector to GND of the user system. These pins are used for electrical GND and to monitor connection with the user system by each emulator.

2. Be particularly sure to connect pin 13 before using the emulator.

3. The EVTO pin provides for the output of event signals from the device to the E2. Although connecting the EVTO pin is not essential, we recommend connecting this pin in advance.

   In some devices, the EVTO pin is not present or is only available as a pin function multiplexed with other functions. When the EVTO pin is a multiplexed pin function and the event output function is to be used, set the EVTO pin so that it will function as the EVTO pin by making the required register settings described in the manual for the device.

4. Input and output are defined from the perspective of the target device.

CAUTION

Unused pins:

Do not apply signals from the user system to unused pins. Doing so may damage the pins.

2.3 Connection interface and modes

The operating mode and the connection interface of the E2, E2 Lite, E1, or E20 is switched in the ways shown in Table 2-4 according to whether it is in use for debugging (when a debugger is in use) or programming (when the Flash Programmer is in use). The serial programming mode may still be used even if the debugger is in use. When flash memory is programmed by the downloading function of the debugger, the flash self-programming function is used.

Table 2-4 Modes and Connection Interfaces

Usage	Tool		Device Mode	Connection Interface
Programming	RFP		Serial programming mode	[E2, E1, E20] 1- or 2-wire UART or CSI [E2 Lite] 1- or 2-wire UART
Debugging	CS+, e^2 studio, or MULTI*1	When OPJTAG is automatically set (connected)*2	Serial programming mode	[E2, E1, E20] When 1-pin LPD is selected, 1-wire UART is used. When 4-pin LPD is selected, 2-wire UART is used.
		During debugging	Normal operation mode or user boot mode	[E2] 1- or 4-pin LPD or JTAG [E2 Lite] JTAG [E1, E20] 1- or 4-pin LPD

Notes: 1. This refers to the MULTI integrated development environment from Green Hills Software. It is simply referred to as MULTI in the remainder of this document.

2. OPJTAG automatic setting function: When a device is debugged, the OPJTAG bit in the option byte register determines the type of connection interface. Debugging will not start if the interface selected by the OPJTAG bit does not match that selected by the debugger. If the OPJTAG automatic setting function is enabled, the emulator makes a transition to the serial programming mode without fail and reads the OPJTAG bit. If the interface differs from that selected by the debugger, the OPJTAG bit is rewritten, the mode is switched to the normal operating mode, and debugging will start.

   When this function is enabled to start debugging, since the mode is switched to the serial programming mode, some emulation may be impossible since the initial values in memory and of ECC errors after a reset are undefined. Therefore, only use the OPJTAG automatic setting function when the OPJTAG bit in the option byte register is to be modified. For details on setting this function, refer to the manual for the debugger you are using.

   With CS+, select “Yes” as the [Set OPJTAG in LPD connection before connecting] property on the [Connect Settings] tabbed page to enable the OPJTAG automatic setting function.

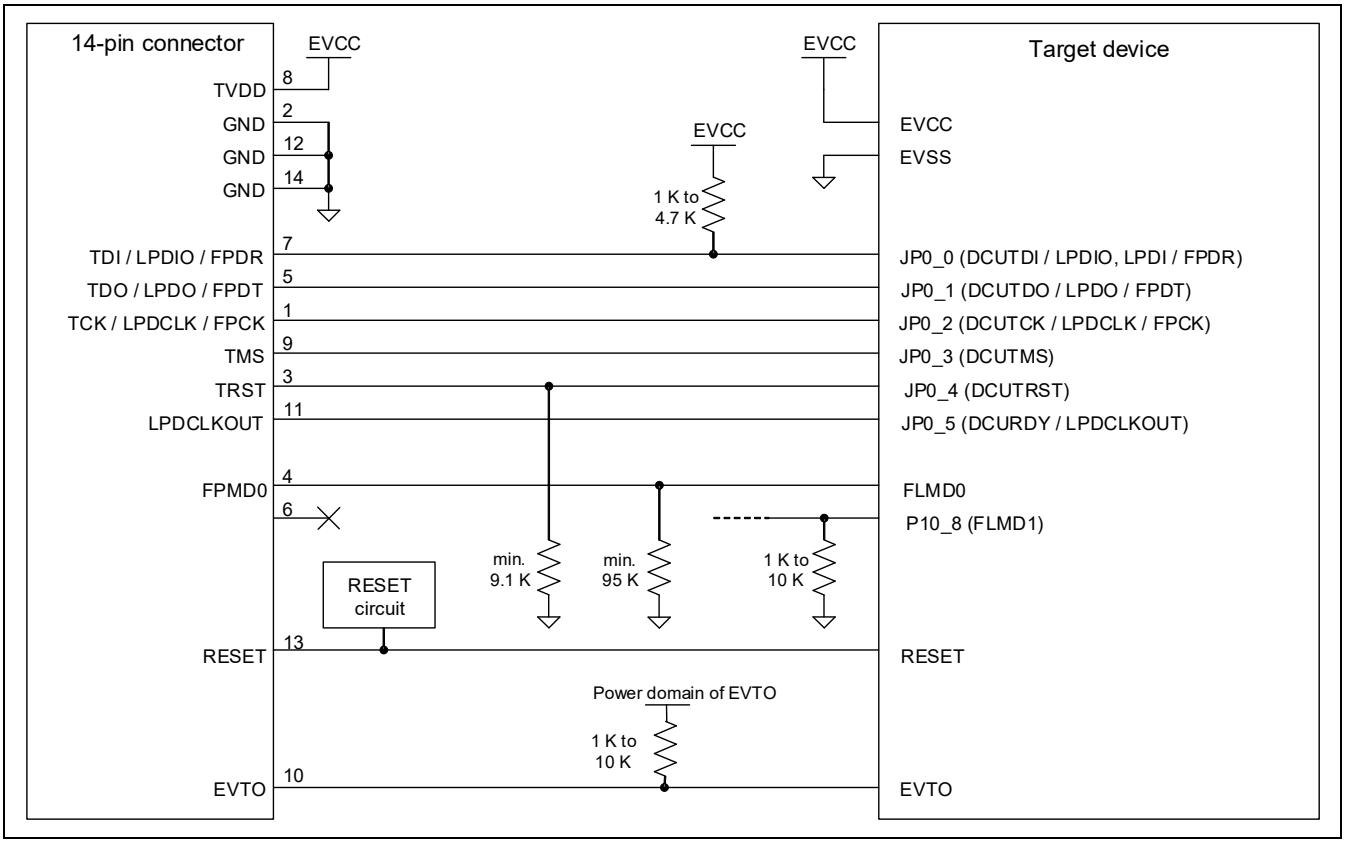
2.4 Examples of recommended connections between the connector and MCU

This section describes examples of recommended connections between the connector for each emulator and the target device. The recommended connection examples differ depending on the application shown in Table 2-4. Refer to Table 2-5 and design an appropriate circuit. Be sure to take the specifications of the target device as well as measures to prevent noise into consideration when designing your circuit.

Table 2-5 Purpose of each emulator and the Corresponding Example of Recommended Connections

Purpose	Figure
Debugging (1-pin LPD, 4-pin LPD or JTAG) and programming (1-wire UART, 2-wire UART or CSI)	Figure 2-4
Debugging (1-pin LPD) and programming (1-wire UART)	Figure 2-5
Only programming (1-wire UART or 2-wire UART)	Figure 2-6
Only programming (CSI)	Figure 2-7

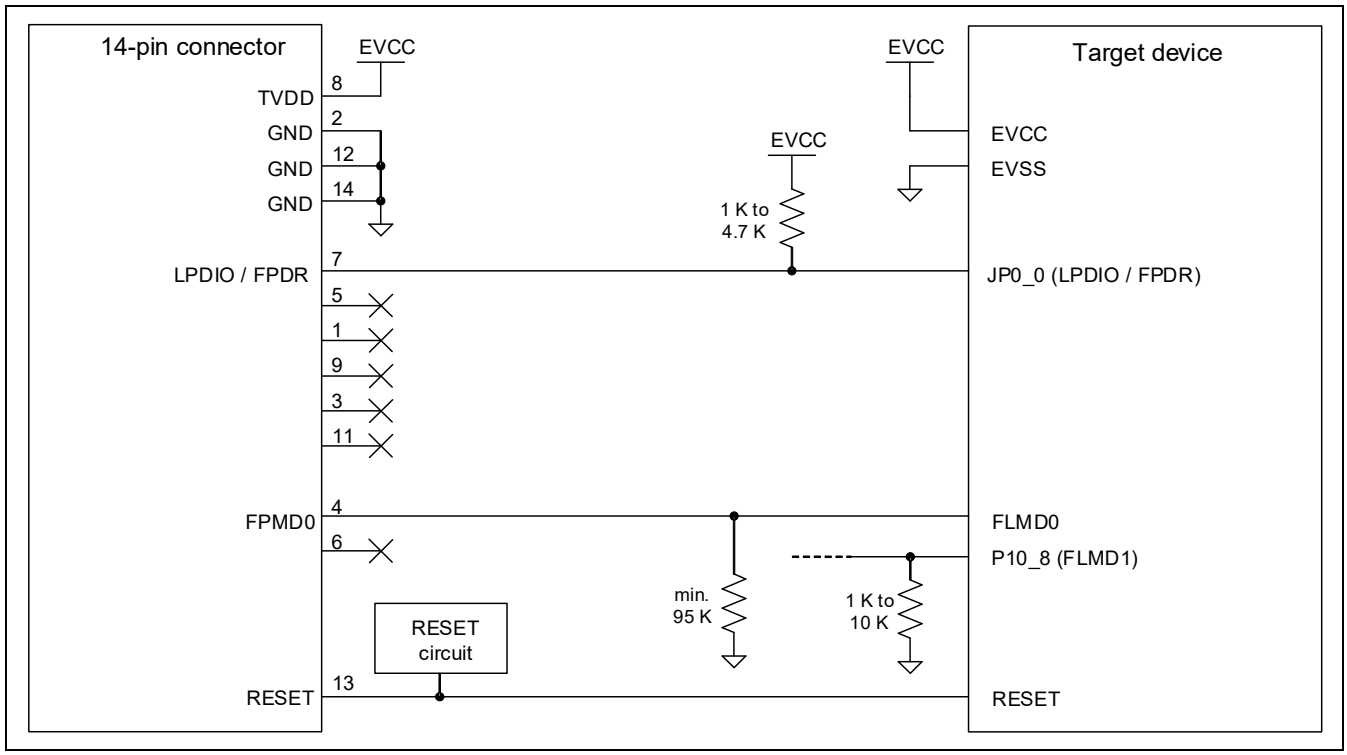
2.4.1 Debugging (1-pin LPD, 4-pin LPD, or JTAG) and programming (1-wire UART, 2-wire UART, or CSI)



Refer to section 2.4.5, Precautions for Wiring and Board Design, for precautions when designing the board.

Figure 2-4 Example of Connection

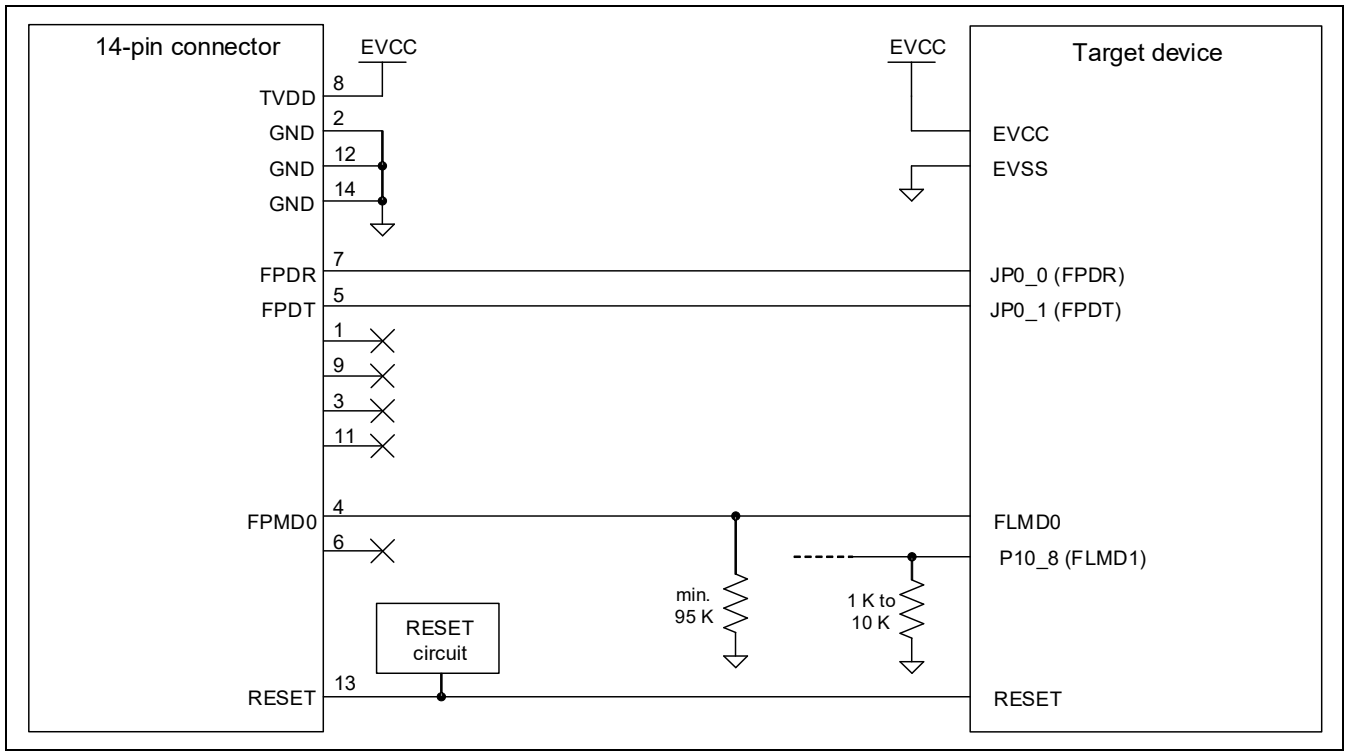
2.4.2 Debugging (1-pin LPD) and programming (1-wire UART)



Refer to section 2.4.5, Precautions for Wiring and Board Design, for precautions when designing the board.

Figure 2-5 Example of Connection

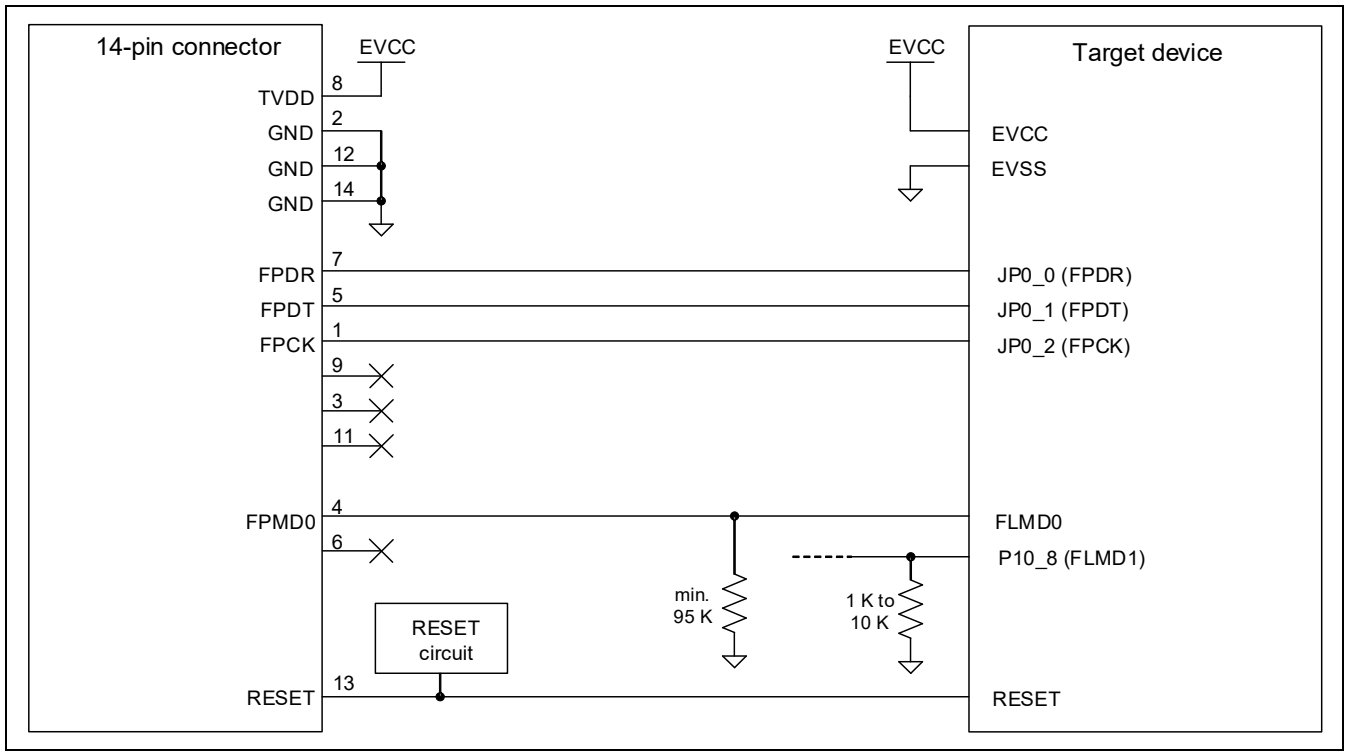
2.4.3 Only programming (1-wire UART, or 2-wire UART)



Refer to section 2.4.5, Precautions for Wiring and Board Design, for precautions when designing the board.

Figure 2-6 Example of Connection

2.4.4 Only programming (CSI)



Refer to section 2.4.5, Precautions for Wiring and Board Design, for precautions when designing the board.

Figure 2-7 Example of Connection

2.4.5 Precautions for Wiring and Board Design

(1) The circuit shall be designed so that the FLMD1 pin is always driven to the low-level during programming.

(2) Pulling up for JP0_0 is only necessary if you are using the 1-pin LPD interface.

(3) When debugging proceeds with an LPD connection by using an E1, do not enable the pull-up function of the JP0-3 ports in the user program.

(4) Make wiring runs between the 14-pin connector and target device as short as possible (within 50 mm is recommended). Do not connect the signal lines between the connector and target device to other signal lines.

(5) Use GND to apply a guard ring for the wiring which runs between the 14-pin connector and target device. Do not route high-speed signal lines parallel to each other or allow them to cross each other.

(6) Pin names may vary among target devices. Refer to the hardware manual for the target device you are using for the actual pin names.

(7) Proceed with appropriate processing for pins of target devices which do not require connection to the emulator in accord with the descriptions in “Handling of Unused Pins” in the hardware manual for the target device.

(8) During programming (using the RFP or automatically setting OPJTAG), the emulator outputs the high level on FPMD0 and the low-level on FPMD1 to place the device in the serial programming mode. If necessary, connect FPMD1 and FLMD1.

(9) Normally, no signals are output on FPMD0 and FPMD1 during debugging. That is, the pins are placed in the high-impedance (Hi-z) state. The high level may be output on FPMD0 during rewriting of the internal flash memory by the downloading function and so on.

(10) Handle the mode pins correctly in accord with the instructions in the hardware manual for the target device when using the user boot mode.

(11) When designing the target system, refer to section 2.4.6, Connecting the RESET pin, and section 2.4.7, Connecting the TVDD pin, for RESET and TVDD connections.

CAUTION

Connection of emulators from other manufacturers:

If you use an emulator from another manufacturer for debugging, be sure to read its manual beforehand.

2.4.6 Connecting the RESET pin

While the emulator is in use, pin 13 (RESET pin) of the 14-pin connector must be connected to the reset pin of the target device. Figure 2-8 shows an example.

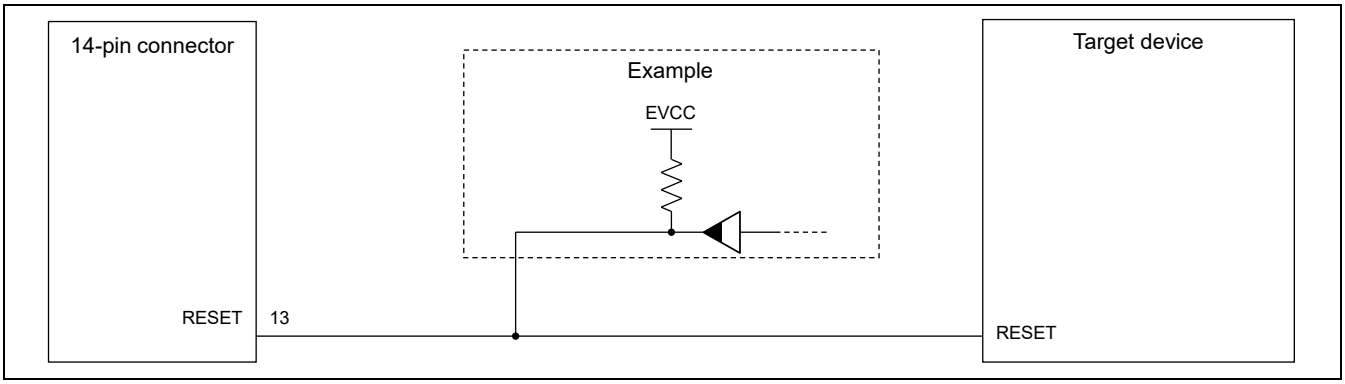


Figure 2-8 Example of Connecting a Reset Circuit

Each emulator fixes the RESET pin to a low-level before the debugger or RFP is activated. After the debugger or RFP is activated, the emulator either keeps the pin at the low-level or places it in the high-impedance state in accord with the operation of the debugger or RFP.

- Output of the reset circuit should be either n-channel open drain or be a signal generated solely by a resistor and capacitor (and possible other components).
- For the target device in this manual, pull the RESET signal up to the EVCC voltage.
- Pin 13 (RESET) of each emulator is pulled up (by a 100-kΩ resistor) within the emulator (refer to chapter 5, Internal Circuits of the Emulator).
- The RESET pin of the target device may be pulled up or down within the device. On this point, refer to the manual for the target device.
- The maximum sink current accepted by the RESET pin of each emulator is 2 mA. Select an appropriate pull-up resistance which does not surpass this value.
- Adjust the time constant of the reset circuit so that the time elapsing before the signal reaches 80% of the high level from the low-level is within 900 μs.
- When you use hot plug-in, consider installation of a capacitor between the reset signal and GND in order to suppress a noise. In this case, however, the specifications of the time described above must be satisfied.

2.4.7 Connecting the TVDD pin

(1) Power source monitoring function

Connect the power source on the user system to pin 8 (TVDD pin) of the 14-pin connector. For the target device in this manual, this will be the source of the EVCC voltage.

The power source connected to the TVDD pin provides power to the final stage output buffer and first stage input buffer on the emulator circuit. When the emulator is connected, it will draw current as described below in addition to the current drawn by the user system.

- E2, E2 Lite, or E1: Approximately 20 mA when TVDD is 3.3 V, and approximately 40 mA when TVDD is 5.0 V
- E20: Approximately Approx. 40 mA when TVDD is 3.3 V, and approximately 100 mA when TVDD is 5.0 V

(2) Power supply function (applies only to the E2, E2 Lite, or E1)

The E2 or E1 can also supply power at 3.3 V or 5.0 V from the TVDD pin to the user system. The E2 Lite can also supply power at 3.3 V from the TVDD pin to the user system. (at a current of up to 200 mA) When using this function, take care of the following points.

- Do not use this function if power is being separately supplied to the user system. Doing so may damage the E2, E2 Lite, or E1.
- Do not use this function for a user system which draws a current of 200 mA or more. Doing so may damage the E2, E2 Lite, or E1, or the host machine's USB interface.
- Make sure that the supplied voltage is within the range required by the user system.
- E1: When 5.0 V is supplied, the actual voltage may be 0.5 V or more below 5.0 V, depending on the host machine environment.
- E2: When 5.0 V is supplied, the actual voltage may be 0.3 V or more below 5.0 V, depending on the host machine environment.

Power supply from the E2, E2 Lite, or E1 depends on the quality of the USB power supply of the host machine, and as such, precision is not guaranteed. When writing a program that requires reliability, do not use the power supply function of the E2, E2 Lite, or E1. Use a stable, separate power supply for the user system. When writing a program for mass production processes, use the Renesas Flash Programmer.

⚠ CAUTION

Turning the Power On/Off:

When supplying power, ensure that there are no shorts between the user system and power circuit. Only connect the emulator after confirming that there are no mismatches of alignment on the user system port connector. Incorrect connection will result in the host machine, the emulator, and the user system emitting smoke or catching fire.

2.4.8 Hot plug-in connection

If there is a possibility you will be using hot plug-in connection, you will need to configure the circuit as shown below. Pin 8 of the E1 is connected to a 4.7-uF capacitor as shown in (1) in Figure 2-9, so hot plug-in connection of the emulator may lead to a momentary drop in the power-supply voltage on the user system. This might cause the MCU to be reset.

As shown in (2) in Figure 2-9, this effect can be reduced by placing a ferrite bead (or inductor) and relatively large capacitor with low equivalent series resistance near the TVDD line of the connector for connection of the emulator. However, this measure will not completely eliminate the voltage drop. Note that hot plug-in connection is only for use during debugging, and a separately sold hot plug-in adapter is necessary to use this function otherwise.

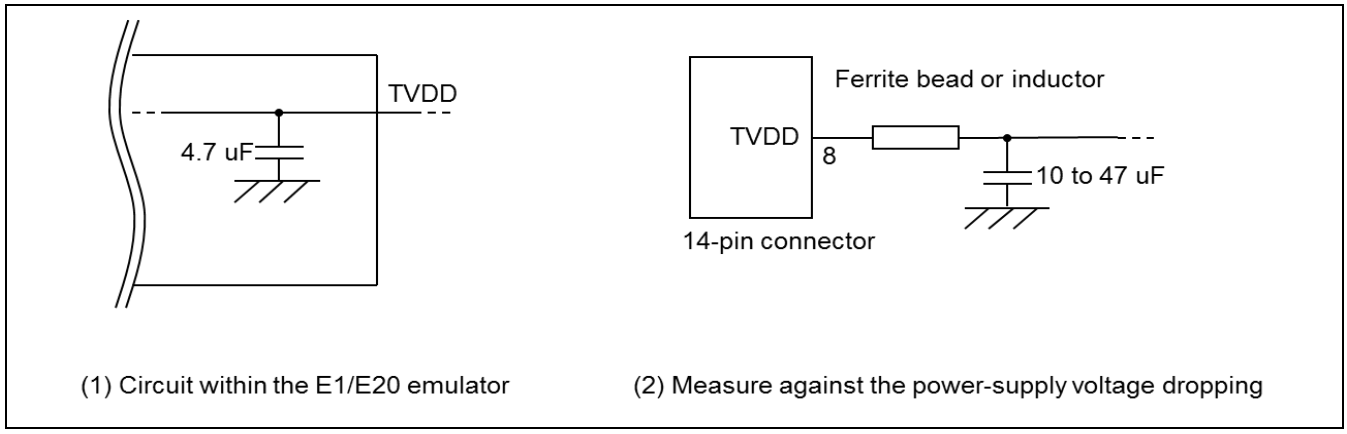


Figure 2-9 Circuit Configuration for Hot Plug-in

- Hot plug-in adapter for the E1
  For hot plug-in connection to the E1, use the hot plug-in adapter for the E1 emulator (R0E000010ACB00) that is separately available from Renesas.

Hot plug-in connection can be used with the E2 and E2 Lite without the need for a hot plug-in adapter. For details, refer to the E2 or E2 Lite Manual.

Each emulator do not support the hot plug-out function. Do not disconnect the user-system interface cable during debugging.

CAUTION

Note on the hot plug-out function:

While the power of the user system is on, do not unplug the user-system interface cable.
The emulator and the user system may be damaged.

2.4.9 Isolator

For a debugging environment where there is a difference in potential between the GND of the user system and that of the host PC, use the isolator (R0E000010ACB20) which is separately available from Renesas.

2.4.10 Small connector conversion adapter

A small connector conversion adapter (R0E000010CKZ11) is separately available from Renesas for user system boards which are too small to mount the 14-pin connector that is the standard connector for the E2, E2 Lite, and E1. By using the adapter, you can reduce the area taken up by the connector mounted on your system.

However, when you use the small connector conversion adapter, be aware that the pin assignments of the connector differ from those of the standard interface connector for the E2, E2 Lite and E1.

2.5 E2 expansion interface (external trigger input and output)

Using the expansion interface of the E2 (the connector for the interface can be found by removing the cover on which SELF CHECK is printed) enables the input and output of external triggers.

If you are using the input or output of external triggers, connect the expansion interface (GND: pin 13) on the E2 to the GND on the user system via one of the test leads which are provided with the E2. Then, according to the pin assignments shown in Figure 2-8, connect the expansion interface of the E2 to the pins on the user system via the test leads.

For details on the expansion interface, refer to the E2 Emulator Manual.

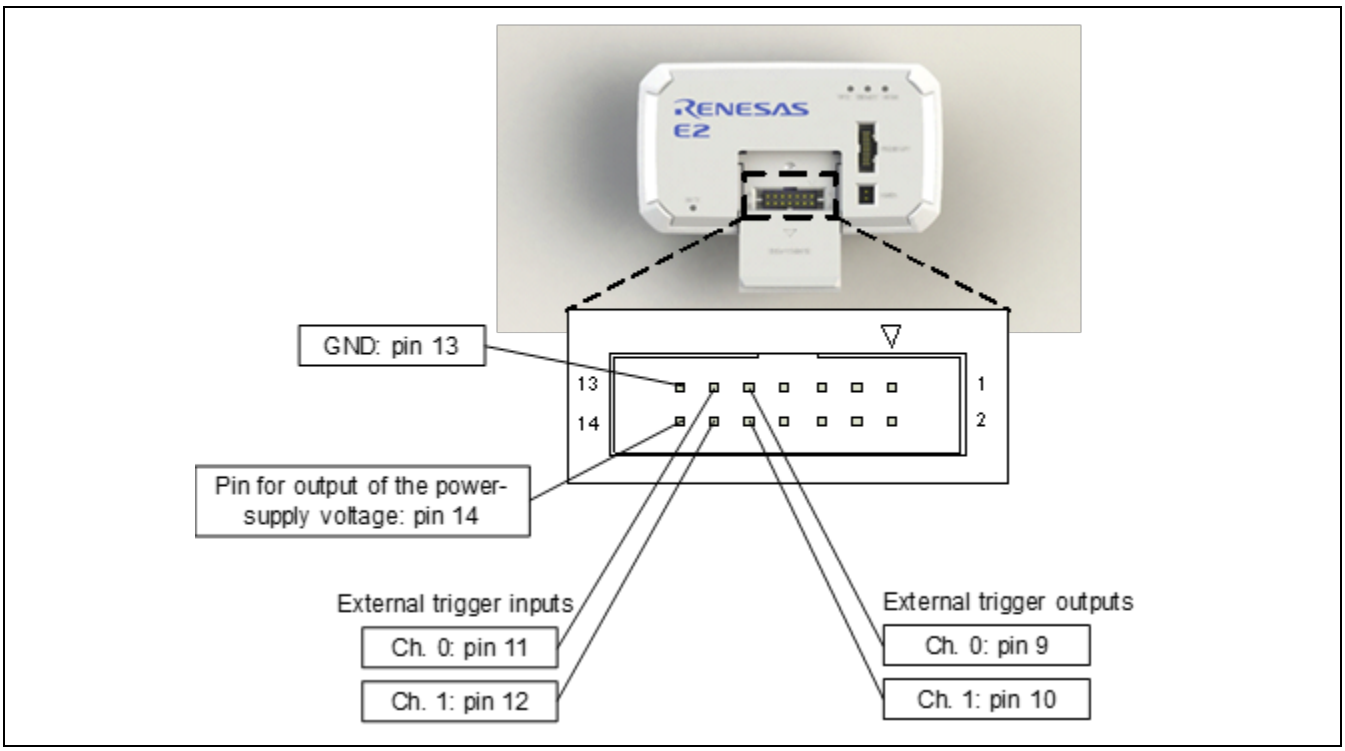


Figure 2-10 Expansion Interface of the E2

CAUTION

Expansion interface:

Connect the expansion interface with attention to the range of voltages avoiding conflicts between signals. Incorrect connection may damage the E2 and the user system or result in them emitting smoke or catching fire.

3. Functional Overview

3.1 List of functions

Table 3-1 shows functions common to each emulator.

Table 3-2 shows functions specific to the E2.

Support for some debugging-related functions also depends on the debugger. Refer to the manual, etc. for the debugger you are using.

Table 3-1 Common functions of each emulator

Broad Category	Medium Category	Narrow Category	E2, E1, E20	E2 Lite
Hardware in general	Corresponding host machine		Computer equipped with a USB port, OS depends on the debugger	
	Host machine interface		USB 2.0 (full speed or high speed)	
	Power supply for the emulator		No need (the host computer supplies power through the USB)	
	Power supply function		3.3 V or 5.0 V (with current up to 200 mA) can be supplied from TVDD to the user system (make settings with the debugger) (only when the emulator is the E2 or E1)	3.3 V (with current up to 200 mA) can be supplied from TVDD to the user system (make settings with the debugger)
	User system interface		14-pin connector	
	Connection to the user system		Connection by the provided user-system interface cable	
	Connection interface		【E2/E1/E20】 LPD 1pin 500kbps/1Mbps/2Mbps LPD 4pin 3MHz/5.5MHz/11MHz 【E2】 JTAG 6.25MHz/11MHz	JTAG 6MHz
	Hot plug-in connection		Possible (To use with the E1, requires a separately sold hot plug-in adapter)	
Debugging-related items	Break	Software break	In ROM and RAM areas combined: 2000 points	
		Hardware break	12 points including those used for both execution and access conditions (8 points only for execution conditions, and 4 points for either execution or CPU access conditions)	
		Event break	Available	
		Forced break	Available	
		Peripheral breaks	Available*2	
		Trace-full break	Available (internal trace memory and E2 storage)	-
		External trigger input break	Available (E2 only)	-
	Event	Number of events that can be set	8 points for execution, 8 points for CPU access, 4 points for DMA access, and 4 points for GRAM access (RH850/F1KH only)	
		Available function	Break, trace, performance measurement	Break, performance measurement
		Combination of events	OR, sequential	

Broad Category	Medium Category	Narrow Category	E2, E1, E20	E2 Lite
Debugging-related items (cont.)	Tracing (only for devices including an internal trace RAM)	Destination for storage	Internal trace memory	-
		Size	Branch only: 1,000 branches Data trace only: 1,000 cycles of access Software trace only: 1,000 to 2,000 instructions	-
		Traced data	Branches, cycles of data access, cycles of DMA access, cycles of GRAM access (RH850/F1KH only), and software trace	-
		Conditions to start and stop recording of data	Stopping program execution, event-based condition settings	-
		Data-trace conditions	Event conditions	-
		Priority of trace acquisition	Real-time trace mode (priority given to speed) Non-real-time trace mode (priority given to data)	-
		Trace memory recording method	Ring mode (overwriting mode) Trace-full stop mode Trace-full break mode Halting tracing due to the input of an external trigger (E2 only)	-
	Multi-core debugging	Mode selection	Asynchronous debugging or synchronous debugging	
		Initially stopped debugging	Programs can be executed in the initially stopped state after a reset.	

Broad Category	Medium Category	Narrow Category		E1, E20, E2	E2 Lite
Debugging-related items (cont.)	Perfor-mance mea-sure-ment	Time (1)	Measurement section	From run to break	-
			Item measured	Execution time*4	-
			Performance	32-bit counters	-
		Time (2)	Measurement section	From run to break, or between two event points	-
			Items measured	Execution time, total execution time, pass count, maximum execution time, minimum execution time*4	-
			Performance	32-bit counters (for three sections)	-
		Other than time (when you are using a device that includes trace functions, or the emulation adapter)	Items measured	Number of instructions executed (all or branches only), number of interruptions accepted (EI level or FE level), number of exceptions accepted (instruction asynchronous or instruction synchronous), clock cycles (all, while interrupts are inhibited, or other than for the processing of interrupts)	
			Measurement section	From run to break, or between two event points	
			Items measured	Latest value, total value, pass count, maximum value, minimum value	
			Performance	32-bit counters (for four sections)	
	Pseudo real-time RAM monitoring Direct memory modification			Available (occupies a bus (steals cycles))*1	
	Emulator detection by user programs			Available*3 Debugging startup register Initial value: 0000 0000_H Address: FA00 2078_H (CPU1) Address: FA00 2078_H (CPU2: RH850/F1KH only)	
	Debugging console			Not available	
	Downloading of the external flash memory			Not possible	
	Security			16-byte ID code authentication	
	Security ID settings			Not available	
	Security flag settings			Not available	
	Activating the settings of the Intelligent Cryptographic Unit (Master/Slave type) (ICUM/ICUS)			Not possible	
	Main core debug			Possible	

Broad Category	Medium Category	Narrow Category	E1, E20, E2	E2 Lite
Programming-related items	Connection interface		2-wire UART, 1-wire UART, CSI	2-wire UART, 1-wire UART
	Security ID settings		Available	-
	Security flag settings		Available	-
	Activating the settings of the Intelligent Cryptographic Unit (Master/Slave type) (ICUM/ICUS)		Possible	-

Notes: 1. Only available for the local RAM, global RAM, and retention RAM areas.

2. The function to stop peripheral I/O operation in a break is called the peripheral break function.
   Whether peripheral emulation functions are set or not is determined by the debugger.
   Refer to the manual for the debugger you are using for how to set them.
   Refer to the manual for the MCU you are using to check whether peripheral emulation functions are set.
3. For this function, any 32-bit value which is debugging information from the debugger is specified and held in the debugging startup register while the emulator is connected. This function can be used to determine the state of the emulator being connected or not from within user programs (refer to section 4.3.30, Emulator detection by user programs.).
4. The resolution of the measured times depends on the interface used for the connection (e.g., 90.9-nsec resolution for a 4-pin LPD connection running at 11 MHz).

Table 3-2 Specifications Specific to the E2

Broad Category	Medium Category	Narrow Category	E2
Debugging-related items	Software tracing (LPD output) *1	Target CPU	Selection of a single CPU. For multiple-core devices: When the debugger is connected to the emulator, a single target CPU is selected. If the target CPU is changed, the debugger must be re-connected to the emulator (only available in the synchronous debugging mode).
		Destination for storage	“E2 storage”: memory for storage in the E2
		Internal buffer	Eight stages*4
		Traced data	Software trace data + timestamps (given by the E2)*2 Resolution: 8.333 ns, maximum 27 days
		Conditions to start and stop recording of data	Starting and stopping of program execution (breaks)
		Priority of trace acquisition	Real-time trace mode (priority given to speed) Non-real-time trace mode (priority given to data)
		Trace memory recording method	Ring mode (overwriting mode) Trace-full stop mode Trace-full break mode
	External trigger input/output*1	Input signal channels	E2 expansion interface: 2ch. 0: pin 11, ch. 1: pin 12
		Output signal channels	E2 expansion interface: 2ch. 0: pin 9, ch. 1: pin 10
		Interface voltage	When the emulator is not supplying power to the user system: TVDD voltage Any voltage between 1.8 V to 5.0 V When the emulator is supplying power to the user system: Voltage being supplied to the user system
		Conditions for detection of trigger inputs	Edge detection (rising, falling, or both edges) Level detection (low or high)
		Operation when a trigger is input	When software tracing (LPD output) is in use: Break When software tracing (LPD output) is not in use: Break or stopping of recording in internal trace memory
		Condition for detection of trigger outputs	Break detection*3
		Operation when a trigger is output	Output of a low or high pulse (from 1 μsec to 65535 μsec) can be specified.

Notes: 1. When the software tracing (LPD output), external trigger input, or external trigger output functions are in use, access to memory during the execution of a program, changes to event conditions, the reading of internal trace memory, and the display of state indicators such as STOP are disabled. In addition, using the [Debug initial stop state] property that executes a program in the initially stopped state (for CS+) and the FETCHSTOP command (for the MULTI integrated development environment from Green Hills Software) are also not available.

2. A timestamp indicates the time that the E2 acquires the software tracing data, not the time the instruction in the software being debugged was executed. The E2 requires execution of the program by the MCU to start only after it has started counting its timestamp values. Since the start of counting timestamp values cannot be precisely synchronized with the start of program execution, the timestamps which have been added to the software tracing data stored from the head of the E2 storage may include some errors.
3. In general, when the software tracing (LPD output) function is not in use, breaks are not detectable during the 10-μsec period after a program has started to run, but the period becomes 100-μsec when the low-speed internal oscillator (LS IntOSC) is the operating clock for the emulator.
4. The output of the combination of a PC value and the corresponding immediate or register value uses one stage of the internal buffer. When software tracing data has been stored up to the seventh stage of the internal buffer, an overflow message is stored in the eighth stage.

3.2 Software tracing function

Devices of the RH850 family support debugging instructions for the output of software trace data. Software trace data are stored in the internal trace memory of the device and output to the emulator via the LPD pins, which is the debugging-connection interface. Unlike conventional tracing, the software tracing function does not cater for the setting of events or conditions so that trace data are output when the settings match the results of program execution; instead, this function helps the user to embed debugging instructions in the program to be executed as checkpoints or for the purpose of the output of specific information or register values and output of the history execution to the emulator side as trace data. Make use of this function as a new way of debugging.

The E2 provides trace data for display and supports LPD output. We also provide several types of helpful solution functions for the E2. For details, refer to the relevant application notes on the following Web site.

https://www.renesas.com/us/en/products/software-tools/tools/emulator/e2.html

For details of the debugging instructions, refer to the RH850 G3M/G3MH/G3K/G3KH Manual: Debugging Instructions. Table 3-3 gives an overview of these instructions.

When the emulator is not connected and the debugging instructions embedded in a program are executed, Software trace data are not output from the LPD interface.

Table 3-3 Debugging Instructions for Software Tracing

Debugging Instruction	Function	Interval between Execution of the Embedded Instruction and the LPD Output*	
		4-pin LPD (11 MHz)	1-pin LPD (2 Mbps)
DBCP	Outputs the current PC value as software trace data.	5.182 µsec	28.500 µsec
DBTAG imm10	Outputs a 10-bit immediate (imm10) value as software trace data. Output of the PC value is also selectable.	1.727 µsec (without the PC value)	9.500 µsec (without the PC value)
DBPUSH rh-rt (General-purpose registers are specified as rh ≤ rt (in ascending order).)	Outputs the register numbers and values of general-purpose registers from rh to rt as software trace data. Output of the PC value is also selectable.	5.182 µsec (Output one register without the PC value)	28.500 µsec (Output one register without the PC value)

Note: This item indicates the time required for the LPD output of software trace data generated by executing a debugging instruction. When this interval follows the execution of a debugging instruction, overflows (losses) of software trace data can be avoided. Even if the debugging instruction is executed with a short interval, the device has an internal buffer for tracing and an overflow (a loss of data) will not occur immediately; however, note that an overflow occurs if the internal buffer becomes full. For DBPUSH instruction, set the total number of the registers to less than 5 to avoid an overflow.

4. Notes on Usage

Cautionary notes on using each emulator are given below.

Conventions:

[E2]: Notes applicable to the E2.

[E2 Lite]: Notes applicable to the E2 Lite

[E1]: Notes applicable to the E1.

[E20]: Notes applicable to the E20.

Otherwise, the notes apply in common to each emulator.

4.1 General cautionary notes

4.1.1 Handling of devices which were used for debugging

Do not use devices that were used for debugging in mass-production. This is because writing to the flash memory of such devices has already proceeded during debugging, so we cannot guarantee the number of times rewriting of the flash memory can proceed. Debugger errors occur when programming of the flash memory is no longer possible. Replace the device in such situations.

4.1.2 Quality of flash programming

To improve the quality, follow the guidelines below.

- Circuits are designed as described in the manuals for the MCU and the emulator.
- The MCU, the emulator, and software are used as described in respective manuals.
- The supply of power to the user system is stable.

4.1.3 Notice Regarding Changes to Windows Driver Policy

Due to the Windows driver policy change introduced in April 2026, the USB driver for Renesas emulator products may fail to load properly on the host PC, preventing the emulator from operating.

When this issue occurs, opening the properties of the applicable product in Device Manager will display the device status as Code 39, along with the message: "This file has been blocked by your application control policy."

(1) **Conditions**

This issue occurs on host PCs running the following OS versions when the cumulative update for Windows 11 (KB5083769) or any later update is applied, and certain conditions* are met.

- Windows 11 24H2
- Windows 11 25H2
- Windows 11 26H1 or later (the applicable update is included by default)

For details, please refer to "The Windows Driver Policy" on Microsoft Support.

(2) **Workarounds and Restrictions**

For the applicable workarounds, refer to the separately issued Tool News (R20TS1242JJ0100).
For restrictions related to these workarounds, also refer to the same Tool News.

4.2 Notes on differences in operation between the actual device and the emulator

4.2.1 DBTRAP instruction

The DBTRAP instruction is used for software break functions and thus cannot be used in programs with the emulator.

4.2.2 Serial programming function

The serial programming function cannot be used with the emulator during debugging.

4.2.3 Current drawn

More current is drawn when an emulator is connected than when it is not connected. That is, the target device consumes more power during debugging than in normal operation since the debugging functions are operating.

4.2.4 Initialization of RAM areas

When an emulator is connected, local RAM, global RAM, and retention RAM areas are initialized to 0000 0000_H. This leads to the following differences from the actual device.

- The initial values in the RAM area after starting an emulator are different from the initial values (undefined values).
- ECC errors due to non-initialization of RAM are not detected with the emulator. If the emulator is not connected and the operation is incorrect, check that the RAM areas have been initialized.

To emulate ECC errors, set the following options.

- The RAM area is not initialized when the emulator is started.
- OPJTAG is not set for an LPD connection before the emulator is connected.

However, if a RAM area is not initialized, the following functions are not available.

- Downloading to on-chip flash memory
- Changes to on-chip flash memory by using the [Memory] panel or the [Disassemble] panel
- Setting of software breaks
- Rewriting of the option byte

4.2.5 OTP flag

Do not set the one-time programming (OTP) flag in self-programming with the emulator. Note that setting of the flag makes downloading from the debugger to flash memory impossible.

4.2.6 Option byte register

The debugger cannot write new values to the bits of the option byte register indicated below since they are used by the emulator. Also, do not attempt self-programming to write new values to these bits.

- OPJTAG1 and OPJTAG0 bits (bits 30 and 29 of the OPBT0 register)
  The values of the OPJTAG1 and OPJTAG0 bits are as follows.
  When the 4-pin LPD interface is selected: 01B
  When the 1-pin LPD interface is selected: 10B
  When the JTAG interface is selected: 11B

4.2.7 Initially stopped state (when a debugger is connected or a reset is applied)

When a debugger is connected or applies a reset, it forcibly releases all CPUs from their initially stopped states and places the target device in the break state, regardless of whether the debugger is in the synchronous or asynchronous debugging mode. If a program is to be executed in this situation, note that all CPUs will not have entered the initially stopped state.

Using the [Debug initial stop state] property (for CS+) and the FETCHSTOP command (for the MULTI integrated development environment from Green Hills Software) enables execution of a program with the CPUs in the initially stopped state. For details of the procedure, refer to the manual for the debugger.

In addition, when an initially stopped core or a core on standby is to be debugged and operation that is close to that of the actual device is required, set the [Debug the initial stop state and the standby mode] property (for CS+) or the initstop boot-up option (for MULTI) to enable this. In this case, an initially stopped core will stay in the initially stopped state following release from a reset and applications that include use of the standby mode of devices can be synchronously debugged. For details of the method, refer to the relevant application note (R20AN0577EJ0100).

When software tracing (LPD output) and E2 expansion interfaces (external trigger input and output) are in use, the function for executing a program in the initially stopped state after a reset cannot be used.

4.3 Cautionary notes on debugging

4.3.1 Power to the target system while debugging

Do not turn the power to the target system off during debugging. Doing so will require reconnection of the debugger.

4.3.2 Hardware break (access) function (the timing of a break occurring)

When the hardware break (access) function is in use, a break in response to the reading or writing of specified data will occur after the instruction. Other hardware breaks (access) occur before the instruction.

4.3.3 Multiplexed functions of pins used for OCD signals

Multiplexed functions of pins used for on-chip debugging (OCD) cannot be used during debugging.

4.3.4 Debugging interface [E2] [E1] [E20]

The E2, E1, and E20 support 1- and 4-pin LPD interfaces. The E2 also supports the JTAG interface.
The E2 Lite supports only the JTAG interface.

Operation is as follows if the setting of the OPJTAG1 and OPJTAG0 bits of the option byte 0 register is "11B" (JTAG: the JTAG interface is selected in the case of a blank chip) and the emulator is connected via the 1- and 4-pin LPD interfaces.

- When starting (connecting) the E2, E1, or E20
  Settings of the option byte 0 register are changed from the setting for JTAG to that for 1- or 4-pin LPD by the debugger on connection to an emulator.
  Therefore, the OPJTAG1 and OPJTAG0 bits of the option byte 0 register are either "10B" (1-pin LPD) or "01B" (4-pin LPD) during emulator operation.
- When exiting from a session with (disconnecting) the E2, E1, or E20
  Settings of the option byte 0 register can be changed by the debugger.
  — The value of the OPJTAG1 and OPJTAG0 bits of the option byte 0 register can be changed to "11B" (for JTAG), which requires rewriting of the flash memory.
  — The setting of the OPJTAG1 and OPJTAG0 bits of the option byte 0 register can be left as "01B" (for 4-pin LPD) or "10B" (for 1-pin LPD).
  When the LPD interface is also used the next time the emulator is connected, we recommend exit from the program without changing the settings from that for the LPD interface.

If power to the target system is turned off because of an abnormal end to the emulator session, the OPJTAG1 and OPJTAG0 bits of the option byte 0 register are not rewritten and so retain the value "01B" (for 4-pin LPD) or "10B" (for 1-pin LPD). If you wish to change the OPJTAG1 and OPJTAG0 bits of the option byte 0 register to "11B" (for JTAG), please do so at the end of the E2, E1, or E20 session.

4.3.5 Initialization of RAM areas

All RAM areas for use by a program must be initialized when an emulator is in use. Before the emulator is used, if any setting is made to initialize the RAM area when the emulator is started, ECC errors are not generated since the debugger initializes the RAM area. However, when the actual device is operated with a program which does not initialize the RAM area, ECC errors will be generated, preventing normal program operation.

ROMization is also required because any data downloaded from the emulator to the RAM area before program execution will also be initialized. For details, refer to the manual for the compiler you are using.

4.3.6 Trace function (when a device with a trace function is in use) [E2] [E1] [E20]

The following restrictions apply to the trace function.

- In the case of section trace, for example, the instruction immediately before the fetched instruction that actually caused tracing to start might be included in trace data.
- In some cases, acquired trace information will be lost. This depends on the program being executed. The lost information cannot be restored, but the fact of the loss is indicated (displayed). Information might be lost when access to data by the CPU is continuous and frequent.
- When priority in tracing is given to non-realtime operation, the functions to stop tracing when the trace memory becomes full (trace-full stop function) and when a specified number of trace messages have been acquired following an event (trace delay-stop function) are not available. To use these functions, give priority to realtime operation.
- When data-qualified tracing (point tracing), i.e. tracing only of data in access to a specific address, is specified, tracing proceeds with any data conditions ignored, even if read access conditions are set. Tracing is still governed by conditions other than data conditions.

4.3.7 Power-saving modes

When a power-saving mode is in use, the restrictions below apply.

- For debugging of a program, ensure that the program sets WUFMSK0[31] to 0.
- Release from the stop, DeepSTOP, or cyclic stop mode follows any of the following operations or conditions while the user program is being executed.
  - Break
  - Memory access
  - Forcibly stopping tracing
  - Setting an event
  - Enabling of the trace-full stop or trace-delay stop functions
- The power supply to the Iso area (CPU, RAM, peripheral module, etc.) is not stopped in the DeepSTOP mode during debugging. For this reason, RAM or registers which have undefined initial values retain these values. Be sure to initialize them after returning to the run mode.

4.3.8 Turning the power on/off

Turn the power of each emulator and the user system following the procedure below.

- When a separate power supply is used for the user system

<When using the emulator>

(1) Check the power is off.
Check that the user system is turned off. When using the E20, check its power switch is off.
(2) Connect the user system.
Connect the emulator and the user system with a user-system interface cable.
(3) Connect the host machine and turn on the emulator.
Connect the emulator and the host machine with a USB interface cable. The E2, E2 Lite, or E1 is turned on by connecting the USB interface cable. When using the E20, turn on its power switch.
(4) Turn on the user system.
(5) Launch the debugger.

<When finished using the emulator>

(1) Close the debugger.
(2) Turn off the user system.
(3) Turn off the emulator and disconnect the emulator.
When using the E20, turn off its power switch. Disconnect the USB interface cable from the emulator. The E2, E2 Lite or E1 is turned off by disconnecting from the USB interface cable.
(4) Disconnect the user system.
Disconnect the user-system interface cable from the user system.

CAUTION

Note on the user system power supply:

While the power of the user system is on, do not turn off the host machine, unplug the USB interface cable, or turn off the power switch of the E20.
The user system may be damaged due to leakage current.

- When power is supplied to the user system from the E2, E2 Lite, or E1.

<When using the emulator>

(1) Check the power is off.
Check that the user system is turned off.
(2) Connect the user system.
Connect the emulator and user system with a user-system interface cable.
(3) Connect the host machine and turn on the emulator.
Connect the emulator and host machine with a USB interface cable, then turn on the emulator.
(4) Launch the debugger.
Launch the debugger and select the setting of power supply to the user system.

<When finished using the emulator>

(1) Close the debugger.
Close the debugger.
(2) Turn off the emulator and disconnect the emulator.
Disconnect the USB interface cable from the emulator, then turn off the emulator.
(3) Disconnect the user system.
Disconnect the user-system interface cable from the user system.

4.3.9 Resets while the emulator is in use

Table 4-1 shows the states of a device while the emulator is in use and the operation of resets issued by the user system or the user program (i.e. user system reset). During single stepping, the emulator masks the user-system resets so that it can continue to emulate each line of source code of the program in non-realtime. In C-source-level stepping, resets are masked in different ways depending on the debugger; one method is to use single stepping and another is to set a temporary breakpoint and execute the user program. Accordingly, this document cannot define whether a reset is masked by the emulator or not; refer to the manual for the debugger you are using.

Table 4-1 State of a Device and Masking of User-system Resets by the Emulator

		State of a device			
		In breaks	**In single stepping**	**In user program execution**	**In C-source-level stepping**
Reset mask specification on the debugger	**Resets not masked**	Resets masked*		Resets not masked	Depends on the debugger
	Resets masked	Resets masked*			

- When a reset is issued by a debugger (by pressing the reset button of the debugger or in some other way), the reset is always enabled regardless of enabling or disabling of reset masking. After a reset is issued by the debugger, breaks are generated for all CPUs.
- Resets generated in the states marked (*) in Table 4-1 are held pending. For example, when a setting for software-reset processing is made during single-stepped execution or a software reset by setting a register is applied by the debugger during a break, the reset is held pending and performed after the reset mask is removed.
- Do not allow the generation of a reset in the form of a pin reset from the target system other than while a program is in execution regardless of the presence of masking as described above. A reset generated while the program is running may cause the debugger to hang.

4.3.10 Interrupts while the emulator is in use

Table 4-2 shows the states of a device while the emulator is in use and the operation of interrupts. During single stepping, the emulator masks interrupts so that it can continue to emulate each line of source code of the program in non-realtime. When interrupt processing is to be stepped through, set a breakpoint at the beginning of the interrupt processing and generate an interrupt during execution of the user program. A break will then be generated at the beginning of the interrupt processing. In C-source-level stepping, interrupts are masked in different ways depending on the debugger; one method is to use single stepping and another is to set a temporary breakpoint and execute the user program. Accordingly, this document cannot define whether interrupts are masked by the emulator or not; refer to the manual for the debugger you are using.

Table 4-2 State of a Device and Masking of Interrupts by the Emulator

State of a device			
In breaks	**In single stepping**	**In user program execution**	**In C-source-level stepping**
Interrupts masked*		Interrupts not masked (operation according to the specification of the user system)	Depends on the debugger

- Interrupts (EIINT, FEINT, and FPI) generated in the state marked (*) in Table 4-2 are held pending and interrupt processing proceeds after interrupt masking is canceled.

4.3.11 HALT mode and stepped execution of the HALT instruction

A break leads to release from HALT mode.

When a HALT instruction is encountered during single-stepped execution (execution in units of assembly instruction), a break is set at the next instruction following the HALT instruction, and the mode does not change to the HALT state. When a HALT instruction is encountered during C-source-level stepped execution, whether or not the transition to the HALT state proceeds depends on the facilities of the debugger.

4.3.12 Stepped execution of an instruction which would lead to a transition to the DeepSTOP mode on the actual device

Stepped execution has two variants: Single step execution (execution in units of assembly instructions) and C-source-level stepped execution (execution in units of statements or functions in C language source code). When an instruction which would lead to a transition to the DeepSTOP mode on the actual device is executed during single step execution, the program breaks at the address at the time of the reset and does not switch to the DeepSTOP mode. When an instruction which would lead to a transition to the DeepSTOP mode on the actual device is executed during C-source-level stepped execution, whether or not the transition to the DeepSTOP mode proceeds depends on the facilities of the debugger.

4.3.13 Cautionary point regarding connecting an emulator (pin reset)

If reset is kept asserted during communication preparation between the emulator and the MCU when the emulator is connected, the communication will not operate properly.

Do not keep reset asserted when the emulator is connected.

4.3.14 Cautionary point regarding connecting an emulator (time required for preparing to communicate)

When the emulator is connected, the program written in the MCU starts executing from the reset vector before communication preparation between the emulator and the MCU is completed. As a result, unintended operation may occur.

If execution of the program on the MCU may cause issues, insert the following wait time* between reset release and execution of the target program.

- For the 1-pin LPD interface, waiting for at least 140 ms is required.
- For the 4-pin LPD interface, waiting for at least 12 ms is required.
- For the JTAG interface, waiting for at least 12 ms is required.

Note: Time required for preparing communications depends on the host PC environment and the operating frequency of the MCU.

4.3.15 Cautionary point regarding connecting an emulator (internal reset)

When a program that triggers an internal reset (such as a software reset or watchdog overflow reset) immediately after reset is stored in the MCU, the internal reset occurs before communication preparation between the emulator and the MCU is completed when the emulator is connected. As a result, communication will not operate properly.

When debugging a program that performs an internal reset, insert the following wait time* between reset release and execution of the internal reset.

- For the 1-pin LPD interface, waiting for at least 140 ms is required.
- For the 4-pin LPD interface, waiting for at least 12 ms is required.
- For the JTAG interface, waiting for at least 12 ms is required.

Note: Time required for preparing communications depends on the host PC environment and the operating frequency of the MCU.

4.3.16 Cautionary point regarding connecting an emulator (DeepSTOP mode)

When a program that transitions to the DeepSTOP mode immediately after reset is stored, the MCU enters the DeepSTOP mode before communication between the emulator and the MCU is established when the emulator is connected. As a result, communication will not operate properly.

When debugging a program that transitions to the DeepSTOP mode, insert the following wait time* between reset release and execution of the instruction that transitions to the DeepSTOP mode.

- For the 1-pin LPD interface, waiting for at least 140 ms is required.
- For the 4-pin LPD interface, waiting for at least 12 ms is required.
- For the JTAG interface, waiting for at least 12 ms is required.

Note: Time required for preparing communications depends on the host PC environment and the operating frequency of the MCU.

4.3.17 Cautionary points regarding hot plug-in connection

- Before proceeding with hot plug-in connection, set the OPJTAG [1:0] bits in the corresponding option byte register according to the debugging interface to be selected. When the OPJTAG [1:0] bits of the option byte register do not match the debugging interface to be used, a connection error occurs.
- Allowing hot plug-in connection prevents usage of the optional isolator (the isolator is only for use with the RH850 and RL78 groups).
- Allowing hot plug-in connection prevents the supply of power to the user system by the E2, E2 Lite or E1.
- If hot plug-in connection is not to be used, the RAM area will be initialized* when the emulator is started. Allowing hot plug-in connection prevents this initialization and makes the masking of pins impossible. Thus, when the emulator is started without initializing the RAM area to be used by a program, ECC errors occur. Therefore, make sure to initialize the RAM area to be used by a program before setting up the system for hot plug-in connection.
- After completing hot plug-in connection, the user program will be running. At this time, only the emulator functions listed below are available.
  - Read or write access to the internal RAM area
  - Forced break
  - CPU reset

  Apply a forced break if you wish to return to using all functions supported by the emulator. After the forced break, functions equivalent to those that can be used after normal starting of a program become available.

Note: The RAM area is only initialized if the setting is made to initialize the RAM area when the emulator is started.

4.3.18 Cases where hot plug-in connection is not possible

Hot plug-in connection cannot be used when the microcontroller is in any of states listed below.

- Reset input state
- Cyclic run mode
- Cyclic stop mode

4.3.19 Standby mode released by hot plug-in connection

Hot plug-in connection releases the microcontroller from standby in the form of either of the states below.

- Stop mode
- DeepSTOP mode (A reset will occur due to the specifications of the device.)

4.3.20 Performance measurement

In the case of measuring a specific section, if the intervals between the start and the end of one measurement, and between the end of that measurement and the start of the next is short, the measurement is not possible. To obtain correct measurements, the interval* should be long enough.

Note: The required detection interval depends on the operating frequency and the LPD communications frequency of the MCU.

4.3.21 Rewriting of on-chip flash memory (working RAM)

When the debugger performs any operation that involves programming of the flash memory* during a break, part of the internal RAM area is used as a working RAM area. The 4-KB area (for the E2 or E2 Lite) or the 9-KB area (for the E1 or E20) from the last address of the local RAM area of CPU1 is initially set as the working RAM area. If a device has no local RAM area, the retention RAM area is used.

The debugger can change the working RAM area. After the debugger has saved the values from the working RAM area and rewrites the flash memory, it restores the saved values to the working RAM area. To guarantee the values, it is required to set an area to which there will be no access by the DMAC or any external master to the working RAM area so that operation may continue even if the device enters the break state.

Note: Rewriting of flash memory proceeds in response to any of the operations below.

- Downloading to on-chip flash memory
- Changes to on-chip flash memory by using the [Memory] panel or the [Disassemble] panel
- Setting or cancellation of software breaks
- Re-execution after a software break is encountered (including stepped execution)

4.3.22 Rewriting of on-chip flash memory (clock monitor)

The debugger changes the PLL multipliers when the flash memory is being rewritten*. Thus, rewriting the flash memory raises a possibility of the frequency becoming higher than that currently in use. If the frequency surpasses the upper limit which was set by the clock monitor (CLMA), this prevents rewriting of the flash memory. If the change in the clock frequency due to the debugger is a problem, set [Change the clock to flash writing] in the [Property] panel to [No].

Note: Rewriting of flash memory proceeds in response to any of the operations below.

- Downloading to on-chip flash memory
- Changes to on-chip flash memory by using the [Memory] panel or the [Disassemble] panel
- Setting or cancellation of software breaks
- Re-execution after a software break is encountered (including stepped execution)

4.3.23 Breaks during execution of code for making clock settings

The flash memory cannot be programmed if a break occurs while the MCU is running code written to memory for making clock settings (setting of the main oscillator or PLL frequency divider and so on).

If you wish either of the following types of operation to proceed when a break has occurred during clock settings, set [Change the clock to flash writing] in the [Property] panel to [No].

- Any operation that involves programming of the flash memory (e.g. re-downloading)
- Setting or cancellation of software breakpoints

Also, do not set software breakpoints within code for making clock settings.

4.3.24 Event functions (64-bit access)

Do not set any access events with the condition in 64-bit units. The emulator may detect access in a unit other than 64 bits as satisfying such conditions or other events may not operate normally.

4.3.25 Event functions (in the order of event detection)

In the following cases, since the orders of instructions and event detection may not operate as set, to measure the time or performance in sequential events, section tracing, and desired sections may not be possible.

- An event is set for consecutive instructions, but the two instructions are executed at the same time.
- An access event detects adjacent read and write instructions, since the timing of event detection differs in write and read access and the timing may be detected in the order of reading then writing, even though the instructions are executed in the order of writing then reading.

4.3.26 Event functions (bit-manipulation instructions)

When a read or write access condition is set for an event, the writing cycle of read-modify-write generated by a bit-manipulation instruction is not detected as an event. This condition cannot be used as a trigger for a break, trace acquisition, or performance measurement in the case of such instructions.

4.3.27 Satisfaction of two break conditions before a single break

If another read-access event is detected immediately before a transition to the break state due to a forced break or an event break, a further break will occur immediately after execution of the program is resumed because the break request was accepted as a read-access event at the time of resumption.

4.3.28 Software break functions (RAM areas)

The software break function is implemented by replacing instructions. Thus, note that no break will occur if the value at an address where a software break has been set is rewritten by a user program which is running.

4.3.29 Cases where no break occur

No breaks occur when the CPU is in any of states listed below.

- Initially stopped state
- Reset state
- DeepSTOP mode (in case of synchronous debugging mode)
- Cyclic run mode (in case of synchronous debugging mode)
- Cyclic stop mode (in case of synchronous debugging mode)

If you want to generate a break for a CPU in run mode with a device that includes an initially stopped CPU or for a CPU in cyclic run mode during synchronous debugging, refer to section 4.2.7, Initially stopped state (when a debugger is connected or a reset is applied).

4.3.30 Emulator detection by user programs

Even if debugging information is specified, note that the value will be initialized to 0000 0000_H if a reset is generated. Debugging information is specified again when a break occurs in all CPUs and when the user program is re-executed after a reset.

4.3.31 Software tracing (LPD output) function when the 1-pin LPD interface is selected [E2]

When the 1-pin LPD is selected and a break is generated as a forced break, a trace-full break from the E2 storage, or a break due to the input of an external trigger, software tracing (LPD output) cannot be used when execution of the program is subsequently resumed. To proceed with software tracing (LPD output) again, re-connect the emulator to the debugger.

4.3.32 Cautionary point regarding trace data acquired by software tracing (LPD output) [E2]

When a break is generated as a forced break, a trace-full break from the E2 storage, or a break due to the input of an external trigger, information from a debugging instruction that was executed immediately before the break will not be stored in the E2 storage.

When a debugging instruction is executed during single-stepped execution and a software break or hardware break is specified and executed by the debugging instruction, software trace data are not output through the LPD interface.

When trace acquisition is stopped due to a break generated by a software break, hardware break, event break, or trace-full break from internal trace memory, the history of execution from a DBCP instruction executed in the debugging area is stored as the final trace data in the E2 storage and internal trace memory after the break in execution.

4.3.33 Cyclic run mode and cyclic stop mode

This item only applies to the F1KH group.

When the microcontroller enters the cyclic run mode or cyclic stop mode, the core other than CPU1 is stopped. Debugging must only proceed as asynchronous debugging. That is, synchronous debugging is not usable in this situation. Otherwise, refer to section 4.2.7, Initially stopped state (when a debugger is connected or a reset is applied). Also, since the core other than CPU1 is stopped during asynchronous debugging, it cannot be debugged.

4.3.34 Cautionary point regarding asynchronous debugging mode (peripheral break function)

This item only applies to the F1KH group.

In the asynchronous debugging mode, peripheral break functions cannot be used. Even if peripheral break functions are enabled, peripheral functions are not stopped.

4.3.35 Cautionary point regarding asynchronous debugging mode (reset)

This item only applies to the F1KH group.

In the asynchronous debugging mode, when any of CPUs is in the break state, no resets are acceptable.

4.3.36 Cautionary point regarding asynchronous debugging mode (watchdog timer)

This item only applies to the F1KH group.

In the asynchronous debugging mode, when any of CPUs is in the break state, counters are stopped in WDTA0, WDTA1, and WDTA2.

4.3.37 Cautionary point regarding asynchronous debugging mode (ECC error)

This item only applies to the F1KH group.

During execution of a user program, there may be a case that the ECC error function does not normally operate for flash memory.

Example: When any CPU accesses flash memory during execution of a user program causing an ECC error and another CPU which is in the break state accesses the same resources in the memory window at the same timing, the debugger temporarily controls the ECC error and no ECC error occurs in any CPU.

4.3.38 Cautionary point regarding asynchronous debugging mode (specific sequence)

This item only applies to the F1KH group.

During execution of a user program, there may be a case that the specific sequence is not satisfied.

Example: When any CPU accesses the specific I/O register during execution of a user program and another CPU which is in the break state accesses the same peripheral function in the I/O register window at the same timing, the specific sequence from any CPU is not satisfied and normal accessing is disabled.

4.3.39 Initially stopped state of CPU2 (forced break)

This item only applies to the F1KH group.

You cannot select CPU2 and cause a forced break when CPU2 is in its initially stopped state immediately after release from the reset state. A forced break is not possible until CPU1 has released CPU2 from its initially stopped state.

4.3.40 Initially stopped state of CPU2 (synchronous break)

This item only applies to the F1KH group.

In the synchronous debugging mode, a break may occur for all CPUs. However, if any of CPUs is in the initially stopped state, note that no break will occur. A breakpoint must be set in the program at a point after all CPUs have been released from the initially stopped state. If you want to generate a break earlier than this, use the asynchronous debugging mode or refer to section 4.2.7, Initially stopped state (when a debugger is connected or a reset is applied).

4.3.41 Breakpoints in the code flash P/E mode or data flash P/E mode

During debugging of a user program which makes the target device enter the code flash P/E mode or data flash P/E mode, we recommend using hardware breakpoints rather than software breakpoints.

Since flash memory cannot be programmed while the target device is in the code flash P/E mode or data flash P/E mode, software breakpoints can neither be added nor deleted from the code flash memory. Accordingly, actually adding or deleting them on the target device is not possible. Only add or delete software breakpoints in the code flash memory after the target device is in a mode other than the code flash P/E mode or data flash P/E mode.

If a break is generated at a software breakpoint in the code flash memory while the target device is in the code flash P/E mode or data flash P/E mode, the break will be generated at the current address (that of the software breakpoint), so attempting to execute the user program will again lead to a break and the program will not run beyond the current address. In such cases, apply a reset.

4.3.42 Software breakpoints in the code flash memory in the cyclic run mode

Since flash memory cannot be programmed while the target device is in the cyclic run mode, software breakpoints can neither be added nor deleted from the code flash memory. Accordingly, actually adding or deleting them on the target device is not possible. Only add or delete software breakpoints in the code flash memory after the target device is in a mode other than the cyclic run mode.

5. Internal Circuits of the Emulator

Figure 5-1 and Figure 5-2 respectively show those of the E2 (product revision C) and the E2 (product revision D). Figure 5-3 show the internal circuit of the E2 Lite. Figure 5-4 and Figure 5-5 show the internal circuits of the E1 or E20.

The alphabet at the end of serial No. written on the E2 main unit indicates the product revision.

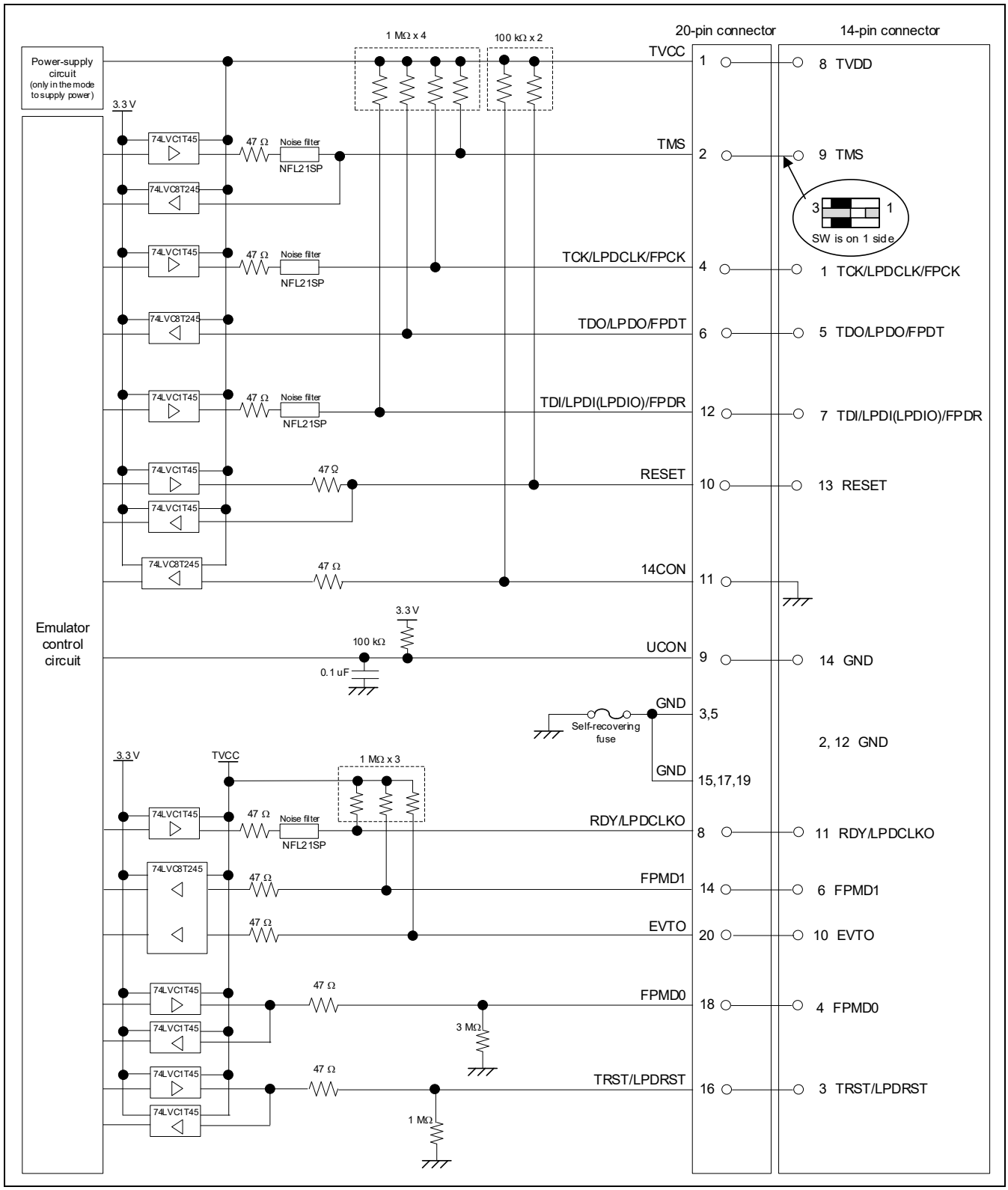


Figure 5-1 Interface Circuits in the E2
(1-Pin LPD, 4-Pin LPD, JTAG, 1-Wire UART, 2-Wire UART, CSI) (Rev. C)

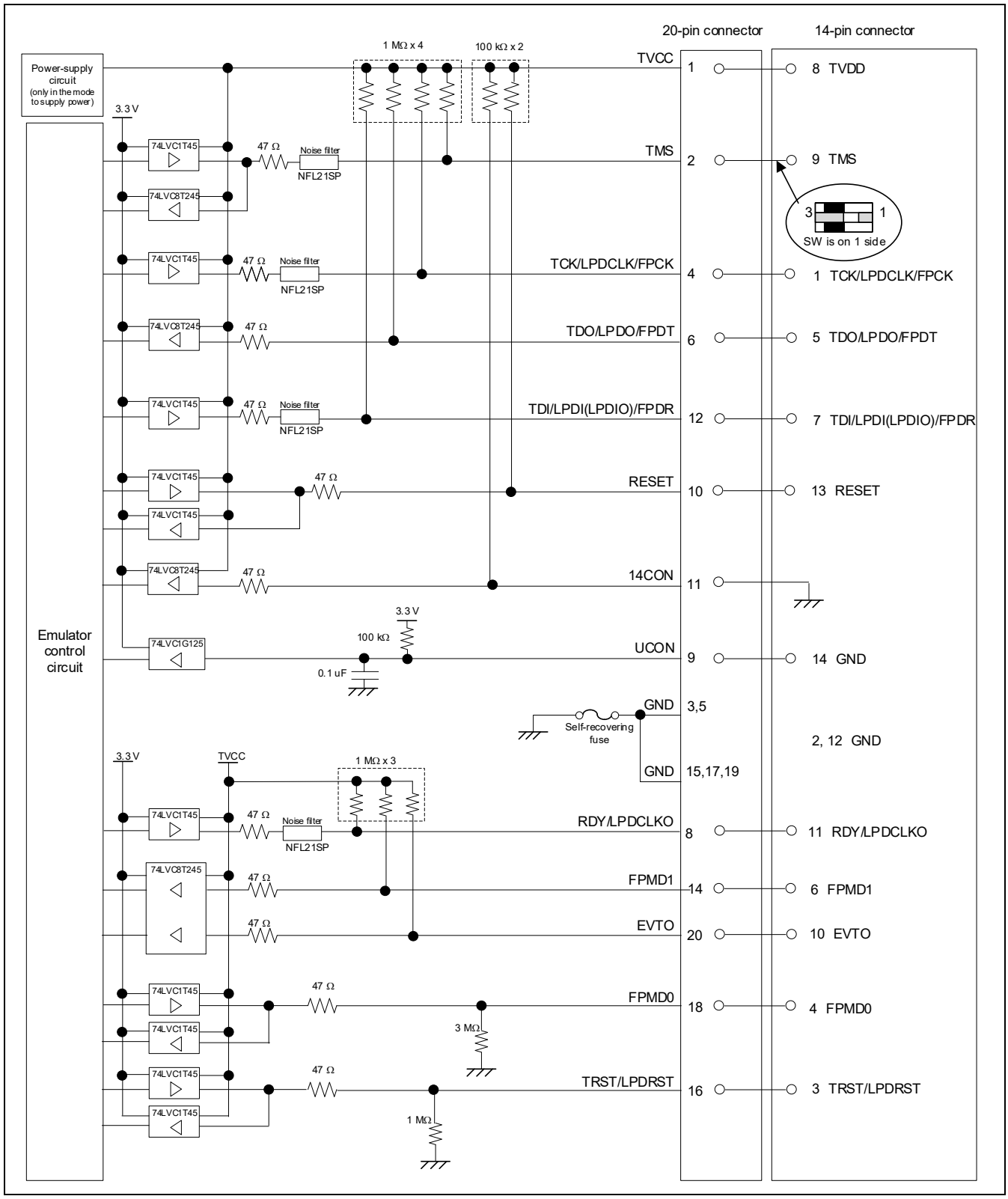


Figure 5-2 Interface Circuits in the E2
(1-Pin LPD, 4-Pin LPD, JTAG, 1-Wire UART, 2-Wire UART, CSI) (Rev. D)

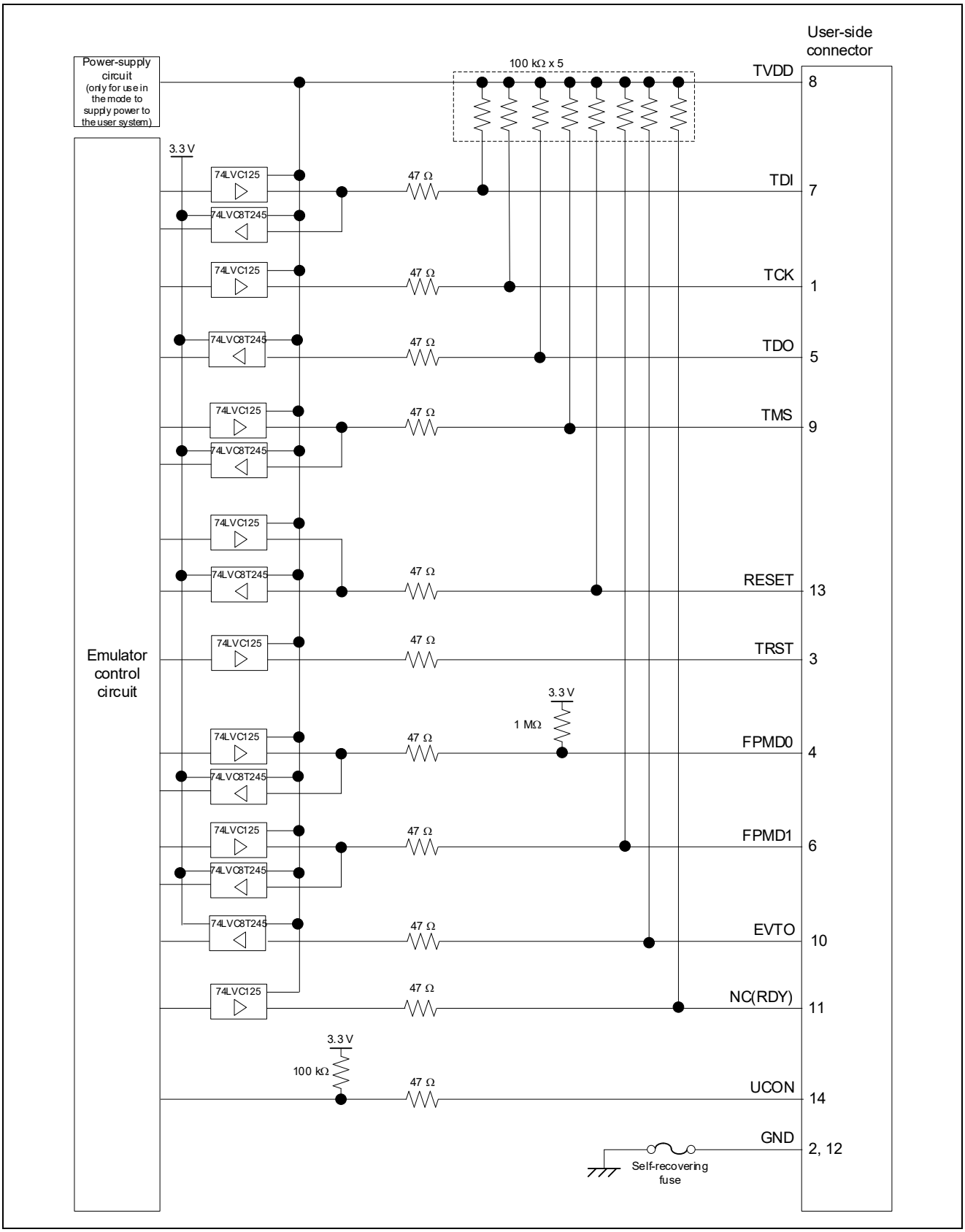


Figure 5-3 Interface Circuits in the E2 Lite

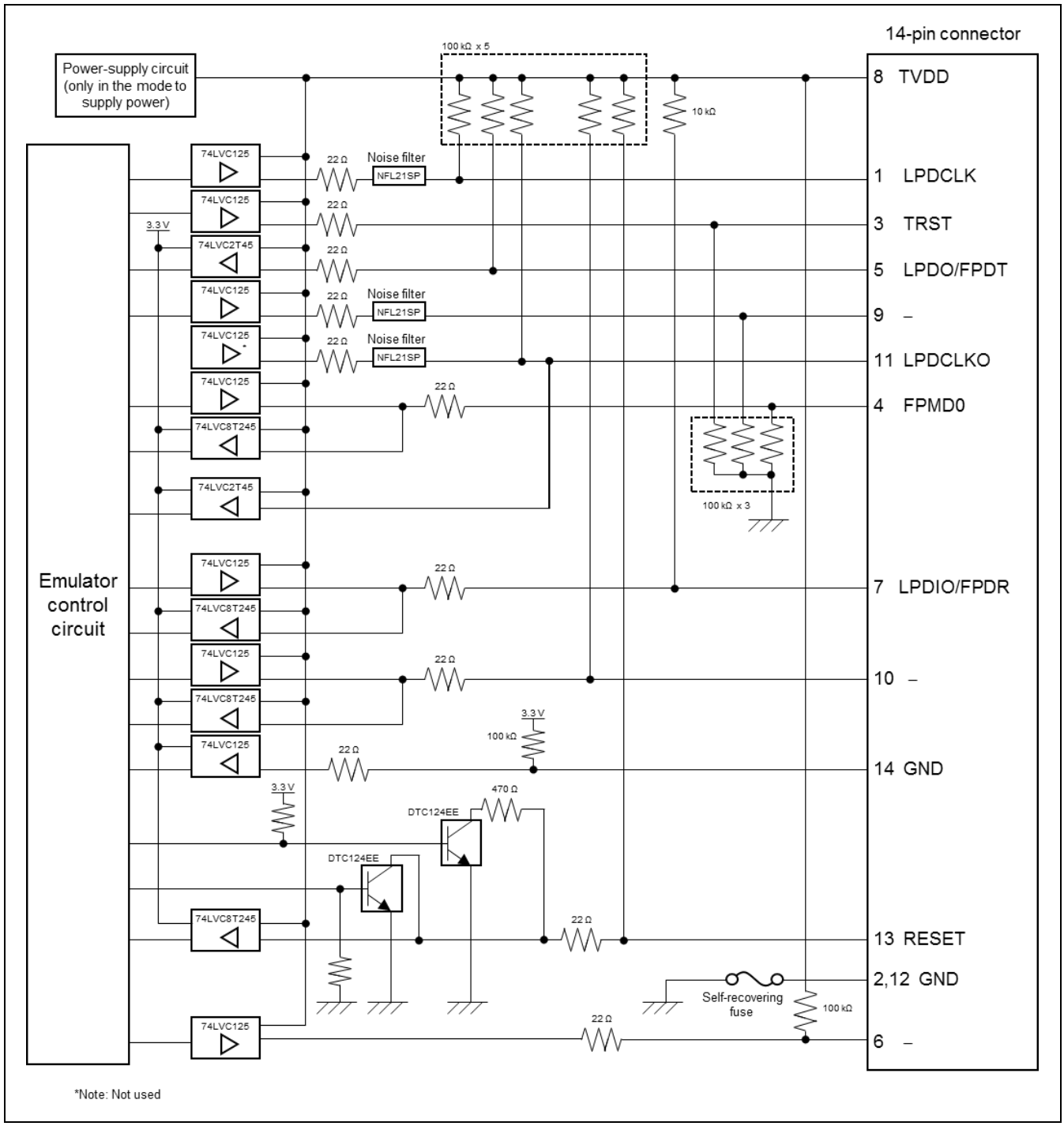


Figure 5-4 Interface Circuits in the E1 or E20 (1-Pin LPD, 1-Wire UART)

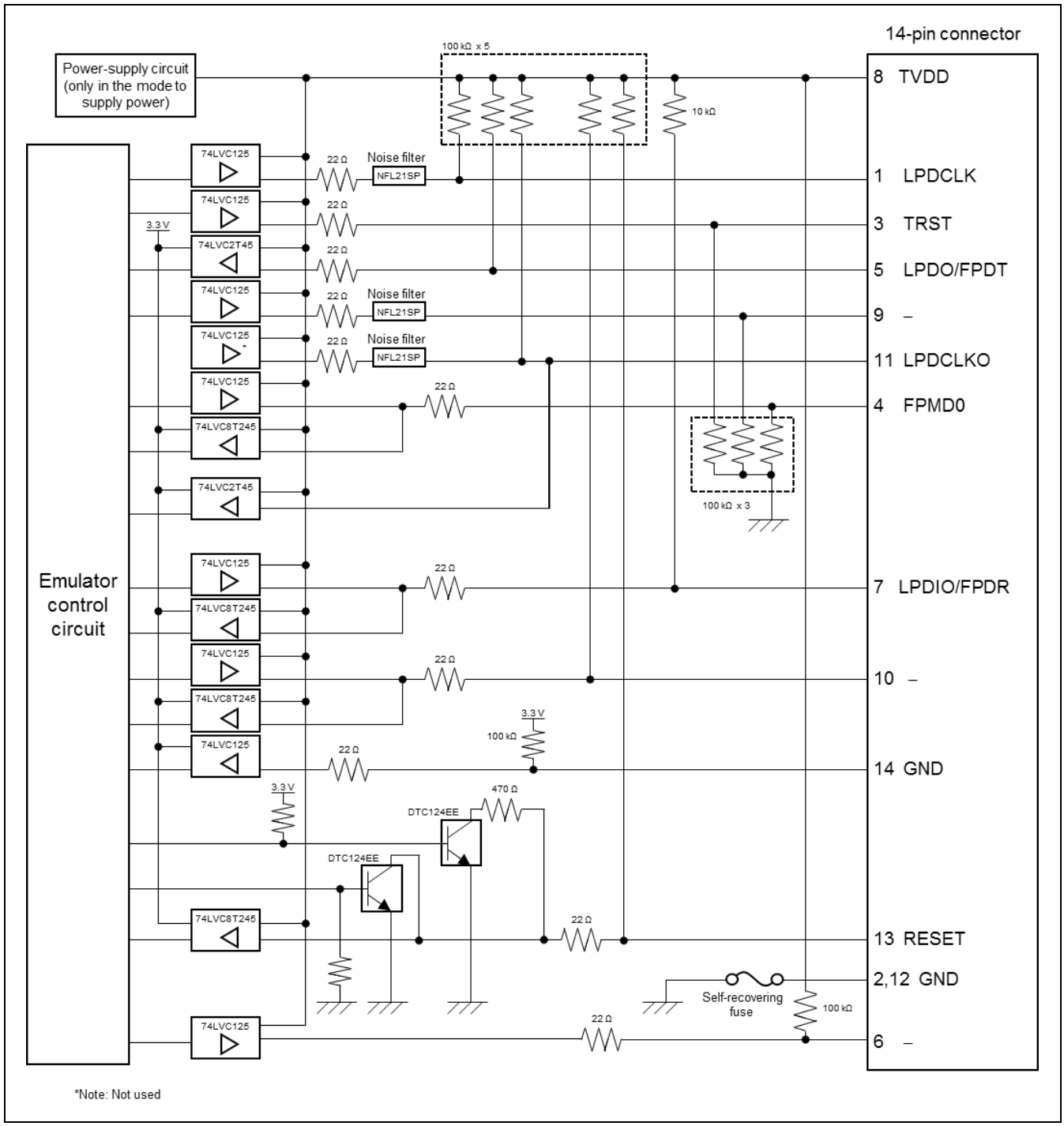


Figure 5-5 Interface Circuits in the E1 or E20 (4-Pin LPD, 2-Wire UART)

6. Troubleshooting

This chapter gives examples of problems that may arise while each emulator is being used in combination with a debugger and of remedies for these problems. Also read the sections of each emulator manual, on the Renesas homepage, and in manuals for debuggers which include FAQs or information on troubleshooting. The error codes for CS+ are also listed below. If you are using a debugger other than that of CS+, refer to the manual for the given debugger.

6.1 Problems when the emulator is connected

Table 6-1 Problems when the Emulator is Connected (1/4)

Problem	Remedy	Error Code in CS+
Inability to connect with the debugging tool (emulator) This error may occur in the flash programming mode.	When OPJTAG automatic setting is enabled for the setting of the debugger, switch the device to the flash programming mode when it is connected and check and change the value of the OPJTAG bit in the option byte (refer to section 2.3, Connection interface and modes.). If this fails, the error message shown at right will appear. Check the following items. • Control of pin resets for the transition to the flash programming mode may be wrong. When an emulator is connected, do not input a reset signal to the pin on the circuit other than from the emulator. Check the notes (e.g. the time the signal takes to reach the high level from the low-level) given in section 2.4.6, Connecting the RESET pin or whether the electrical characteristics requirements of the reset pin of the device are satisfied. • The connection between the emulator and the target device may be wrong. Refer to section 2.4, Examples of recommended connections between the connector and MCU, and check the circuit between the emulator and the target device. • Check that mode pins such as FLMD1, which are not controlled by the emulator, are being handled in ways that allow transitions to the flash programming mode.	E1203237
	• The value set for MainOSC may be wrong. Check whether the frequency of MainOSC on the board matches the value set for connecting the debugger.	E1203275
	• The connection between the emulator and the target device (particularly that of the FLMD0 pin) may be wrong. Refer to section 2.4, Examples of recommended connections between the connector and MCU, and check the circuit between the emulator and the target device.	E1203276

Table 6-2 Problems when the Emulator is Connected (2/4)

Problem	Remedy	Error Code in CS+
Inability to connect with the debugging tool (emulator) Error in LPD connection	• The OPJTAG bit in the option byte may not be specifying the correct connection interface (LPD). Enable OPJTAG automatic setting as the setting for the debugger to allow rewriting of the option byte when the emulator is started or use a flash programmer (e.g. the RFP) to change the value of the OPJTAG bit before connecting the debugger. • The condition in cautionary note given in section 4.3.14, Cautionary point regarding connecting an emulator (time required for preparing to communicate) on the time required for preparing communications before the emulator is connected to the target device may not be satisfied. Use a flash programmer (e.g. the RFP) to erase the code flash memory and check whether this makes the emulator connectable to the target device. • When the emulator is connected other than with a hot plug-in connection, although the emulator controls the pin reset, this may fail. Check the notes (e.g. the time the signal takes to reach the high level from the low-level) given in section 2.4.6, Connecting the RESET pin or whether the electrical characteristics requirements of the reset pin of the device are satisfied. • The connection between the emulator and the target device may be wrong. Refer to section 2.4, Examples of recommended connections between the connector and MCU, and check the circuit between the emulator and the target device. • The specifications for communications may not be being satisfied due to the state of the target board. Set the LPD transfer rate to a low rate and check whether the emulator can then be re-connected. • The value of the option byte may not be correct. Check that the value of the option byte has been specified with suitable settings according to the hardware manual for the MCU in use by using a Flash Programmer (RFP, etc.). • When the power supply function from the emulator is used, the supply voltage may drop below the voltage set in the debugger depending on the host machine environment and user system conditions. As a result, the device may not meet its electrical characteristics and may not operate properly. In such cases, it does not use the power supply function. Instead, supply power to the user system using an external power supply that meets the specifications.	E1203240
	• The RESET pin of the target device may be active. Make sure that the RESET pin is at the inactive level during connection of the emulator.	E1203274

Table 6-3 Problems when the Emulator is Connected (3/4)

Problem	Remedy	Error Code in CS+
Inability to connect with the debugging tool (emulator) Non-matching of security IDs	• ID authentication may fail when the debugger is connected. Check that the entered ID code is correct. • The condition in cautionary note given in section 4.3.14, Cautionary point regarding connecting an emulator (time required for preparing to communicate) on the time required for preparing communications before the emulator is connected to the target device may not be satisfied. Use a flash programmer (e.g. the RFP) to erase the code flash memory and check whether this makes the emulator connectable to the target device.	C0602202

Table 6-4 Problems when the Emulator is Connected (4/4)

Problem	Remedy	Error Code in CS+
Inability to connect with the debugging tool (emulator) Errors in JTAG connection	• The OPJTAG bit in the option byte may not be specifying the correct connection interface (JTAG). Use a flash programmer (e.g. the RFP) to change the value of the OPJTAG bit before connecting the debugger. • The condition in cautionary note given in section 4.3.14, Cautionary point regarding connecting an emulator (time required for preparing to communicate) on the time required for preparing communications before the emulator is connected to the target device may not be satisfied. Use a flash programmer (e.g. the RFP) to erase the code flash memory and check whether this makes the emulator connectable to the target device. • When the emulator is connected other than with a hot plug-in connection, although the emulator controls the pin reset, this may fail. Check the notes (e.g. the time the signal takes to reach the high level from the low-level) given in section 2.4.6, Connecting the RESET pin or whether the electrical characteristics requirements of the reset pin of the device are satisfied. • The connection between the emulator and the target device may be wrong. Refer to section 2.4, Examples of recommended connections between the connector and MCU, and check the circuit between the emulator and the target device. • The specifications for communications may not be being satisfied due to the state of the target board. Set the JTAG transfer rate to a low rate and check whether the emulator can then be re-connected. • The value of the option byte may not be correct. Check that the value of the option byte has been specified with suitable settings according to the hardware manual for the MCU in use by using a Flash Programmer (RFP, etc.). • When the power supply function from the emulator is used, the supply voltage may drop below the voltage set in the debugger depending on the host machine environment and user system conditions. As a result, the device may not meet its electrical characteristics and may not operate properly. In such cases, it does not use the power supply function. Instead, supply power to the user system using an external power supply that meets the specifications.	E1203331
	• The RESET pin of the target device may be active. Make sure that the RESET pin is at the inactive level during connection of the emulator.	E1203332

6.2 Problems after the emulator is connected

Table 6-5 Problems after the Emulator is Connected

Problem	Remedy	Error Code in CS+
Inability to generate breaks	• The reset signal may have been at the active level for a long time. If a reset is input for more than 8 seconds, forced breaks will be disabled. Wait for the end of the reset input or change the setting for masking resets. • Supply of a clock signal to the CPU may have stopped. Do not stop supply of a clock signal to the CPU. If supply of a clock signal to the CPU is stopped, power to the target must be turned off and then on again. Turn off the power to the target and re-connect the debugger. • The condition in cautionary note given in section 4.3.7, Power-saving modes on the power-saving modes may not be satisfied. Wait for the target device to be switched to the normal mode or cancel masking of resets and input a reset to the pin on the target board. During debugging, be sure to set a wake-up source in the WUFMSK0 register.	E1200674

Revision History	E2 Emulator, E2 Emulator Lite, E1/E20 Emulator Supplement Manual (Connection of RH850/F1KH and RH850/F1KM)

Rev.	Date	Description	
		Page	Summary
1.00	Jul.01.17	—	First Edition issued
1.10	Jan.15.18	Whole document	Description related to the F1KH group were added.
		5-6	Descriptions were added in section 2.1.
		19	Table 3-1 was updated.
		24	“Top cover” was changed to “the connector for the interface can be found by removing the cover”.
		36	Descriptions were added to section 4.2.24.
1.20	Oct.01.18	6	Figure 2-3 was updated.
		Whole document	Remove the descriptions about “high-speed internal oscillator is the input to the PLL”.
		10-14	The descriptions were added about the connection of FLMD1 and FPMD1.
		25	Descriptions were added to section 4.1.7.
		27	Section 4.2.6 was skipped.
		35	Section 4.2.25 was modified.
2.00	Oct.09.20	20	Note 4 was added to table 3-1.
		22	Note 4 was added to table 3-2.
		34	Statements were added to section 4.2.20, Cautionary point regarding hot plug-in connection.
		37	Statements were added to section 4.2.32, Cases where no break occurs.
		38	A statement was added to section 4.2.36, Cyclic run mode and cyclic stop mode.
		40	Sections 4.2.44 and 4.2.45 were newly added.
		45	Remedies for two types of error (E1203275 and E1203276) were added to table 6-1.
		46	A remedy for one type of error (E1203274) was added to table 6-2.

3.00	May.30.25	3	A description on the user-system interface cable (discontinued product) of the E2 emulator was added in section 2.1.
		4	Pin assignments of JTAG and CSI were added to table 2-3 in section 2.2.
		5	JTAG and CSI were added to table 2-4 in section 2.3. A description was added as a note.
		6	JTAG and CSI were added to table 2-5 in section 2.4.
		7	An example of recommended connections for JTAG was added to section 2.4.1. A description was added as a note.
		9	A description was added as a note in section 2.4.2.
		11	An example of recommended connections for CSI was added to section 2.4.4.
		13	Section 2.4.7, Hot plug-in connection, was added.
		17	JTAG was added to connection interface in table 3-1 in chapter 3.
		23	The notation of JTAG was added to section 4.1.6.
		24	A description of the debugging interface was added to section 4.2.5.
		30	A description of the debugging interface was added to section 4.2.20.
		38, 39	Internal circuits were divided into Rev. C and Rev. D and descriptions related to JTAG were added in chapter 5.
		42	Statements on troubleshooting for errors in JTAG connection were added to table 6-3 in section 6.1.
3.10	Jul.31.25	38, 39	Figure 5-3 and figure 5-4 were updated in chapter 5.
3.20	Jun.30.26	-	Added support for E2 Emulator Lite throughout the document.
		50, 52	Added troubleshooting procedures for the power supply function to Tables 6-2 and 6-4 in chapter 6.

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