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AS17246

Device File

PC-9800 Series (MS-DOS™) Based

IBM PC/AT™ (PC DOS™) Based

Target Device

μPD17240

μPD17241

μPD17242

μPD17243

μPD17244

μPD17245

μPD17246

[MEMO]

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J01.2

INTRODUCTION

Device files are files that store data specific to 17K Series devices (device data). This data is required when using the following 17K Series software development support tools.

- RA17K Assembler package
- *SIMPLEHOST*™

The AS17246 contains the following device files.

- Device file for μ PD17240
- Device file for μ PD17241
- Device file for μ PD17242
- Device file for μ PD17243
- Device file for μ PD17244
- Device file for μ PD17245
- Device file for μ PD17246

Each device file is configured using the file extension .DEV.

[List of Files Included in AS17246]

Device File	Configured File Name	Target Device
AS17246	D17240.DEV	μ PD17240
	D17241.DEV	μ PD17241
	D17242.DEV	μ PD17242
	D17243.DEV	μ PD17243
	D17244.DEV	μ PD17244
	D17245.DEV	μ PD17245
	D17246.DEV	μ PD17246

For details on operating the RA17K assembler package and the device files of the μ PD17240, 17241, 17242, 17243, 17244, 17245, and 17246, refer to the **RA17K Assembler Package User's Manual (U10305E)**.

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CHAPTER 1 DEVICE DATA

The device files provide the following device-related data at assembly.

(1) Program memory (ROM) capacity

μ PD17240: 2048 $\times$ 16 bits (0000H to 07FFH)
 μ PD17241: 4096 $\times$ 16 bits (0000H to 0FFFH)
 μ PD17242: 6144 $\times$ 16 bits (0000H to 17FFH)
 μ PD17243: 8192 $\times$ 16 bits (0000H to 1FFFH)
 μ PD17244: 10240 $\times$ 16 bits (0000H to 1FFFH, 2000H to 27FFH)
 μ PD17245: 12288 $\times$ 16 bits (0000H to 1FFFH, 2000H to 2FFFH)
 μ PD17246: 16384 $\times$ 16 bits (0000H to 1FFFH, 2000H to 3FFFH)

(2) Data memory (RAM) capacity

447 $\times$ 4 bits (BANK0, BANK1, BANK2, BANK3)

(3) Usable instructions

See **CHAPTER 2 INSTRUCTION SET**.

(4) Register files, port registers, and peripheral register read/write data

See **CHAPTER 3 RESERVED SYMBOLS**.

(5) Reserved symbols

See **CHAPTER 3 RESERVED SYMBOLS**.

(6) Device files and device and SE board numbers

A number for each device and a SE board number to indicate the best SE board for developing various products are registered in the device files. These numbers are also included in the ICE and PRO files output by the RA17K assembler package. The device files are used for when the in-circuit emulator checks the development environment and for checking when masks are ordered.

Table 1-1. Relationship Between Device File and Device Number/SE Board Number

Device File	Device Name	Device Number	SE Board Number	SE Board
AS17246	μ PD17240	6D	6D	EM-17246 ^{Note}
	μ PD17241	6E		
	μ PD17242	6F		
	μ PD17243	70		
	μ PD17244	71		
	μ PD17245	72		
	μ PD17246	73		

Note This is a product of Naito Densai Machida Mfg. Co., Ltd. For details, consult Naito Densai Machida Mfg. Co., Ltd. (Tel: +81-45-475-4191).

CHAPTER 2 INSTRUCTION SET

2.1 Instruction Set Summary

b₁₄ to b₁₁ b₁₅		0		1	
		BIN	HEX		
		0000	0	ADD	r, m
		0001	1	SUB	r, m
		0010	2	ADDC	r, m
		0011	3	SUBC	r, m
		0100	4	AND	r, m
		0101	5	XOR	r, m
		0110	6	OR	r, m
		0111	7	INC AR INC IX RORC r MOVT DBF, @AR PUSH AR POP AR GET DBF, p PUT p, DBF PEEK WR, rf POKE rf, WR BR @AR CALL @AR RET SYSCAL Note RETSK RETI EI DI STOP s HALT h NOP	
		1000	8	LD	r, m
		1001	9	SKE	m, #n4
		1010	A	MOV	@r, m
		1011	B	SKNE	m, #n4
		1100	C	BR	addr (page 0)
		1101	D	BR	addr (page 1)
		1110	E	BR	addr (page 2)
		1111	F	BR	addr (page 3)
				ST	m, r
				SKGE	m, #n4
				MOV	m, @r
				SKLT	m, #n4
				CALL	addr (page 0)
				MOV	m, #n4
				SKT	m, #n
				SKF	m, #n

Note μ PD17244, 17245, and 17246 only

2.2 Conventions

AR:	Address register
ASR:	Address stack register indicated by stack pointer
addr:	Program memory address (lower 11 bits)
BANK:	Bank register
CMP:	Compare flag
CY:	Carry flag
DBF:	Data buffer
entry:	System segment entry address
h:	Halt release conditions
INTEF:	Interrupt enable flag
INTR:	Register automatically saved to the stack when interrupt occurs
INTSK:	Interrupt stack register
IX:	Index register
MP:	Data memory row address pointer
MPE:	Memory pointer enable flag
m:	Data memory address indicated by m _R , m _C
m _R :	Data memory row address (higher)
m _C :	Data memory column address (lower)
n:	Bit position (4 bits)
n4:	Immediate data (4 bits)
PAGE:	Page (bits 11 and 12 of program counter)
PC:	Program counter
p:	Peripheral address
p _H :	Peripheral address (higher 3 bits)
p _L :	Peripheral address (lower 4 bits)
r:	General register column address
rf:	Register file address
rf _R :	Register file row address (higher 3 bits)
rf _C :	Register file column address (lower 4 bits)
SP:	Stack pointer
s:	Stop release condition
WR:	Window register
(x):	Contents addressed at x

2.3 List of Instructions

Instruction Set	Mnemonic	Operand	Operation	Instruction Code			
				Opcode	Operand		
Addition	ADD	r, m	$(r) \leftarrow (r) + (m)$	00000	m _R	m _C	r
		m, #n4	$(m) \leftarrow (m) + n4$	10000	m _R	m _C	n4
	ADDC	r, m	$(r) \leftarrow (r) + (m) + CY$	00010	m _R	m _C	r
		m, #n4	$(m) \leftarrow (m) + n4 + CY$	10010	m _R	m _C	n4
	INC	AR	$AR \leftarrow AR + 1$	00111	000	1001	0000
		IX	$IX \leftarrow IX + 1$	00111	000	1000	0000
Subtraction	SUB	r, m	$(r) \leftarrow (r) - (m)$	00001	m _R	m _C	r
		m, #n4	$(m) \leftarrow (m) - n4$	10001	m _R	m _C	n4
	SUBC	r, m	$(r) \leftarrow (r) - (m) - CY$	00011	m _R	m _C	r
		m, #n4	$(m) \leftarrow (m) - n4 - CY$	10011	m _R	m _C	n4
Logical operation	OR	r, m	$(r) \leftarrow (r) \vee (m)$	00110	m _R	m _C	r
		m, #n4	$(m) \leftarrow (m) \vee n4$	10110	m _R	m _C	n4
	AND	r, m	$(r) \leftarrow (r) \wedge (m)$	00100	m _R	m _C	r
		m, #n4	$(m) \leftarrow (m) \wedge n4$	10100	m _R	m _C	n4
	XOR	r, m	$(r) \leftarrow (r) \oplus (m)$	00101	m _R	m _C	r
		m, #n4	$(m) \leftarrow (m) \oplus n4$	10101	m _R	m _C	n4
Decision	SKT	m, #n	$CMP \leftarrow 0$, if $(m) \wedge n = n$, then skip	11110	m _R	m _C	n
	SKF	m, #n	$CMP \leftarrow 0$, if $(m) \wedge n = 0$, then skip	11111	m _R	m _C	n
Comparison	SKE	m, #n4	$(m) - n4$, skip if zero	01001	m _R	m _C	n4
	SKNE	m, #n4	$(m) - n4$, skip if not zero	01011	m _R	m _C	n4
	SKGE	m, #n4	$(m) - n4$, skip if not borrow	11001	m _R	m _C	n4
	SKLT	m, #n4	$(m) - n4$, skip if borrow	11011	m _R	m _C	n4
Rotation	RORC	r	► CY → (r)_{b3} → (r)_{b2} → (r)_{b1} → (r)_{b0} —	00111	000	0111	r

Instruction Set	Mnemonic	Operand	Operation	Instruction Code			
				Opcode	Operand		
Transfer	LD	r, m	$(r) \leftarrow (m)$	01000	m _R	m _C	r
	ST	m, r	$(m) \leftarrow (r)$	11000	m _R	m _C	r
	MOV	@r, m	if MPE = 1: $(MP, (r)) \leftarrow (m)$ if MPE = 0: $(BANK, m_R, (r)) \leftarrow (m)$	01010	m _R	m _C	r
		m, @r	if MPE = 1: $(m) \leftarrow (MP, (r))$ if MPE = 0: $(m) \leftarrow (BANK, m_R, (r))$	11010	m _R	m _C	r
		m, #n4	$(m) \leftarrow n4$	11101	m _R	m _C	n4
	MOVT	DBF, @AR	SP $\leftarrow$ SP - 1, ASR $\leftarrow$ PC, PC $\leftarrow$ AR, DBF $\leftarrow$ (PC), PC $\leftarrow$ ASR, SP $\leftarrow$ SP + 1	00111	000	0001	0000
	PUSH	AR	SP $\leftarrow$ SP - 1, ASR $\leftarrow$ AR	00111	000	1101	0000
	POP	AR	AR $\leftarrow$ ASR, SP $\leftarrow$ SP + 1	00111	000	1100	0000
	GET	DBF, p	DBF $\leftarrow$ (p)	00111	p _H	1011	p _L
	PUT	p, DBF	(p) $\leftarrow$ DBF	00111	p _H	1010	p _L
	PEEK	WR, rf	WR $\leftarrow$ (rf)	00111	rf _R	0011	rf _C
	POKE	rf, WR	(rf) $\leftarrow$ WR	00111	rf _R	0010	rf _C
Branch	BR	addr	Note 1		addr		
		@AR	PC $\leftarrow$ AR	00111	000	0100	0000
Subroutine	CALL	addr	SP $\leftarrow$ SP - 1, ASR $\leftarrow$ PC PC ₁₁ $\leftarrow$ 0, PC ₁₀₋₀ $\leftarrow$ addr	11100	addr		
		@AR	SP $\leftarrow$ SP - 1, ASR $\leftarrow$ PC PC $\leftarrow$ AR	00111	000	0101	0000
	SYSCAL ^{Note 2}	entry	SP $\leftarrow$ SP - 1, ASR $\leftarrow$ PC, SGR $\leftarrow$ 1, PC _{12,11} $\leftarrow$ 0, PC ₁₀₋₈ $\leftarrow$ entry _H , PC ₇₋₄ $\leftarrow$ 0, PC ₃₋₀ $\leftarrow$ entry _L	00111	entry _H	0000	entry _L
	RET		PC $\leftarrow$ ASR, SP $\leftarrow$ SP + 1	00111	000	1110	0000
	RETSK		PC $\leftarrow$ ASR, SP $\leftarrow$ SP + 1 and skip	00111	001	1110	0000
	RETI		PC $\leftarrow$ ASR, INTR $\leftarrow$ INTSK, SP $\leftarrow$ SP + 1	00111	010	1110	0000
Interrupt	EI		INTEF $\leftarrow$ 1	00111	000	1111	0000
	DI		INTEF $\leftarrow$ 0	00111	001	1111	0000
Other	STOP	s	STOP	00111	010	1111	s
	HALT	h	HALT	00111	011	1111	h
	NOP		No operation	00111	100	1111	0000

Note 1. The operation and operation codes “BR addr” of the μ PD17240, 17241, 17242, 17243, 17244, 17245, and 17246 are as follows:

(a) μ PD17240

Operand	Operation	Op Code
addr	PC ₁₀₋₀ $\leftarrow$ addr	01100

(b) μ PD17241

Operand	Operation	Op Code
addr	$PC_{10-0} \leftarrow \text{addr}, \text{Page} \leftarrow 0$	01100
	$PC_{10-0} \leftarrow \text{addr}, \text{Page} \leftarrow 1$	01101

(c) μ PD17242

Operand	Operation	Op Code
addr	$PC_{10-0} \leftarrow \text{addr}, \text{Page} \leftarrow 0$	01100
	$PC_{10-0} \leftarrow \text{addr}, \text{Page} \leftarrow 1$	01101
	$PC_{10-0} \leftarrow \text{addr}, \text{Page} \leftarrow 2$	01110

(d) μ PD17243, 17244, 17245, 17246

Operand	Operation	Op Code
addr	$PC_{10-0} \leftarrow \text{addr}, \text{Page} \leftarrow 0$	01100
	$PC_{10-0} \leftarrow \text{addr}, \text{Page} \leftarrow 1$	01101
	$PC_{10-0} \leftarrow \text{addr}, \text{Page} \leftarrow 2$	01110
	$PC_{10-0} \leftarrow \text{addr}, \text{Page} \leftarrow 3$	01111

Note 2. μ PD17244, 17245, and 17246 only

2.4 Macro Instructions Embedded in Assembler (RA17K)

Conventions

flag n: FLG-type symbol
 n: Bit No.
 <>: Contents inside <> symbols can be omitted

	Mnemonic	Operand	Operation	n
Embedded macros	SKTn	flag 1, ... flag n	if (flag 1) to (flag n) = all "1", then skip	$1 \leq n \leq 4$
	SKFn	flag 1, ... flag n	if (flag 1) to (flag n) = all "0", then skip	$1 \leq n \leq 4$
	SETn	flag 1, ... flag n	(flag 1) to (flag n) $\leftarrow$ 1	$1 \leq n \leq 4$
	CLRn	flag 1, ... flag n	(flag 1) to (flag n) $\leftarrow$ 0	$1 \leq n \leq 4$
	NOTn	flag 1, ... flag n	if (flag n) = "0", then (flag n) $\leftarrow$ 1 if (flag n) = "1", then (flag n) $\leftarrow$ 0	$1 \leq n \leq 4$
	INITFLG	<NOT> flag 1, ... <NOT> flag n	if description = NOT flag n, then (flag n) $\leftarrow$ 0 if description = flag n, then (flag n) $\leftarrow$ 1	$1 \leq n \leq 4$
	BANKn		(BANK) $\leftarrow$ n	$0 \leq n \leq 15$
Extended instructions	BRX	Label	Jump Label	—
	CALLX	function-name	CALL sub-routine	—
	SYSCALX ^{Note}	function-name or expression	CALL system sub-routine	—
	INITFLGX	<NOT/INV> flag 1, ... <NOT/INV> flag n	if description = NOT (or INV) flag, (flag) $\leftarrow$ 0 if description = flag, (flag) $\leftarrow$ 1	$n \leq 4$

Note μ PD17244, 17245, and 17246 only

CHAPTER 3 RESERVED SYMBOLS

The symbols defined for the μ PD17240, 17241, 17242, 17243, 17244, 17245, and 17246 are described on the following pages.

Symbols will be defined for the following.

- Data buffers (DBF)
- System registers (SYSREG)
- Port registers
- Register files (control register)
- Peripheral hardware registers
- Other

3.1 Data Buffers (DBF)

Symbol Name	Attribute	Value	R/W	Description
DBF3	MEM	0.0CH	R/W	Data buffer bits 15 to 12
DBF2	MEM	0.0DH	R/W	Data buffer bits 11 to 8
DBF1	MEM	0.0EH	R/W	Data buffer bits 7 to 4
DBF0	MEM	0.0FH	R/W	Data buffer bits 3 to 0

3.2 System Registers (SYSREG)

Symbol Name	Attribute	Value	R/W	Description
AR3	MEM	0.74H	R/W	Address register bits 15 to 12
AR2	MEM	0.75H	R/W	Address register bits 11 to 8
AR1	MEM	0.76H	R/W	Address register bits 7 to 4
AR0	MEM	0.77H	R/W	Address register bits 3 to 0
WR	MEM	0.78H	R/W	Window register
BANK	MEM	0.79H	R/W	Bank register
IXH	MEM	0.7AH	R/W	Index register bits 10 to 8
MPH	MEM	0.7AH	R/W	Memory pointer bits 6 to 4
MPE	FLG	0.7AH.3	R/W	Memory pointer enable flag
IXM	MEM	0.7BH	R/W	Index register bits 7 to 4
MPL	MEM	0.7BH	R/W	Memory pointer bits 3 to 0
IXL	MEM	0.7CH	R/W	Index register bits 3 to 0
RPH	MEM	0.7DH	R/W	General register pointer bits 6 to 3
RPL	MEM	0.7EH	R/W	General register pointer bits 2 to 0
BCD	FLG	0.7EH.0	R/W	BCD operation flag
PSW	MEM	0.7FH	R/W	Program status word
CMP	FLG	0.7FH.3	R/W	Compare flag
CY	FLG	0.7FH.2	R/W	Carry flag
Z	FLG	0.7FH.1	R/W	Zero flag
IXE	FLG	0.7FH.0	R/W	Index enable flag

3.3 Port Registers

Symbol Name	Attribute	Value	R/W	Description
P0A3	FLG	0.70H.3	R/W	Port 0A bit 3
P0A2	FLG	0.70H.2	R/W	Port 0A bit 2
P0A1	FLG	0.70H.1	R/W	Port 0A bit 1
P0A0	FLG	0.70H.0	R/W	Port 0A bit 0
P0B3	FLG	0.71H.3	R/W	Port 0B bit 3
P0B2	FLG	0.71H.2	R/W	Port 0B bit 2
P0B1	FLG	0.71H.1	R/W	Port 0B bit 1
P0B0	FLG	0.71H.0	R/W	Port 0B bit 0
P0C3	FLG	0.72H.3	R/W	Port 0C bit 3
P0C2	FLG	0.72H.2	R/W	Port 0C bit 2
P0C1	FLG	0.72H.1	R/W	Port 0C bit 1
P0C0	FLG	0.72H.0	R/W	Port 0C bit 0
P0D3	FLG	0.73H.3	R/W	Port 0D bit 3
P0D2	FLG	0.73H.2	R/W	Port 0D bit 2
P0D1	FLG	0.73H.1	R/W	Port 0D bit 1
P0D0	FLG	0.73H.0	R/W	Port 0D bit 0
P0E3	FLG	0.6FH.3	R/W	Port 0E bit 3
P0E2	FLG	0.6FH.2	R/W	Port 0E bit 2
P0E1	FLG	0.6FH.1	R/W	Port 0E bit 1
P0E0	FLG	0.6FH.0	R/W	Port 0E bit 0
P1A2	FLG	1.70H.2	R/W	Port 1A bit 2
P1A1	FLG	1.70H.1	R/W	Port 1A bit 1
P1A0	FLG	1.70H.0	R/W	Port 1A bit 0
P1B0	FLG	1.71H.0	R/W	Port 1B bit 0

3.4 Register Files (Control Registers)

Symbol Name	Attribute	Value	R/W	Description
SP	MEM	0.81H	R/W	Stack pointer
SYSCK	FLG	0.82H.0	R/W	System clock selection flag
WDTRES	FLG	0.83H.3	R/W	Watchdog timer reset flag
BTMCK	FLG	0.83H.2	R/W	Basic interval timer mode selection flag
BTMRES	FLG	0.83H.1	R/W	Basic interval timer reset flag
P1AHL2	FLG	0.85H.2	R/W	P1A2 port standby release level selection flag
P1AHL1	FLG	0.85H.1	R/W	P1A1 port standby release level selection flag
P1AHL0	FLG	0.85H.0	R/W	P1A0 port standby release level selection flag
P1AKEY2	FLG	0.86H.2	R/W	P1A2 port key matrix usage selection flag
P1AKEY1	FLG	0.86H.1	R/W	P1A1 port key matrix usage selection flag
P1AKEY0	FLG	0.86H.0	R/W	P1A0 port key matrix usage selection flag
P1ABPU2	FLG	0.87H.2	R/W	P1A2 port pull-up resistor selection flag
P1ABPU1	FLG	0.87H.1	R/W	P1A1 port pull-up resistor selection flag
P1ABPU0	FLG	0.87H.0	R/W	P1A0 port pull-up resistor selection flag
INT	FLG	0.8FH.0	R	INT pin status flag
NRZBF	FLG	0.91H.0	R/W	NRZ buffer data flag
NRZ	FLG	0.92H.0	R/W	NRZ data flag
REMen	FLG	0.92H.1	R/W	Carrier output selection flag
REMCK1	FLG	0.93H.1	R/W	Clock selection flag for carrier creation
REMCK0	FLG	0.93H.0	R/W	Clock selection flag for carrier creation
P1BHL0	FLG	0.95H.2	R/W	P1B0 port standby release level selection flag
P1BKEY0	FLG	0.95H.1	R/W	P1B0 port key matrix usage selection flag
P1BBPU0	FLG	0.95H.0	R/W	P1B0 port pull-up resistor selection flag
P0EKEY3	FLG	0.96H.3	R/W	P1E3 port key matrix usage selection flag
P0EKEY2	FLG	0.96H.2	R/W	P1E2 port key matrix usage selection flag
P0EKEY1	FLG	0.96H.1	R/W	P1E1 port key matrix usage selection flag
P0EKEY0	FLG	0.96H.0	R/W	P1E0 port key matrix usage selection flag
P0EBPU3	FLG	0.97H.3	R/W	P0E3 pull-up resistor setting flag
P0EBPU2	FLG	0.97H.2	R/W	P0E2 pull-up resistor setting flag
P0EBPU1	FLG	0.97H.1	R/W	P0E1 pull-up resistor setting flag
P0EBPU0	FLG	0.97H.0	R/W	P0E0 pull-up resistor setting flag
IEG	FLG	0.9FH.0	R/W	INT pin interrupt edge selection flag
INTSEL	FLG	0.9FH.1	R/W	INT selection flag
RAMFLAG	FLG	0.0A1H.0	R/W	RAM retention flag
P1ABIO2	FLG	0.0A5H.2	R/W	P1A2 I/O selection flag
P1ABIO1	FLG	0.0A5H.1	R/W	P1A1 I/O selection flag
P1ABIO0	FLG	0.0A5H.0	R/W	P1A0 I/O selection flag

Symbol Name	Attribute	Value	R/W	Description
P0BBIO3	FLG	0.0A6H.3	R/W	P0B3 input/output selection flag (1 = output port)
P0BBIO2	FLG	0.0A6H.2	R/W	P0B2 input/output selection flag (1 = output port)
P0BBIO1	FLG	0.0A6H.1	R/W	P0B1 input/output selection flag (1 = output port)
P0BBIO0	FLG	0.0A6H.0	R/W	P0B0 input/output selection flag (1 = output port)
P0EBIO3	FLG	0.0A7H.3	R/W	P0E3 input/output selection flag (1 = output port)
P0EBIO2	FLG	0.0A7H.2	R/W	P0E2 input/output selection flag (1 = output port)
P0EBIO1	FLG	0.0A7H.1	R/W	P0E1 input/output selection flag (1 = output port)
P0EBIO0	FLG	0.0A7H.0	R/W	P0E0 input/output selection flag (1 = output port)
IPBTM	FLG	0.0AFH.2	R/W	Basic interval timer interrupt enable flag
IP	FLG	0.0AFH.1	R/W	INT pin interrupt enable flag
IPTM	FLG	0.0AFH.0	R/W	8-bit timer interrupt enable flag
TMEN	FLG	0.0B3H.3	R/W	Timer enable flag
TMRES	FLG	0.0B3H.2	R/W	Timer reset flag
TMCK1	FLG	0.0B3H.1	R/W	8-bit timer clock source selection (bit 1)
TMCK0	FLG	0.0B3H.0	R/W	8-bit timer clock source selection (bit 0)
P0DGIO	FLG	0.0B7H.3	R/W	P0D input/output selection flag
P0CGIO	FLG	0.0B7H.2	R/W	P0C input/output selection flag
IRQBTM	FLG	0.0BDH.0	R/W	Basic interval timer interrupt request flag
IRQ	FLG	0.0BEH.0	R/W	INT pin interrupt request flag
IRQTM	FLG	0.0BFH.0	R/W	Timer interrupt request flag

3.5 Peripheral Hardware Registers

Symbol Name	Attribute	Value	R/W	Description
NRZLTMM	DAT	03H	R/W	NRZ modulo register – low
NRZHTMM	DAT	04H	R/W	NRZ modulo register – high
TMC	DAT	05H	R	Timer counter
TMM	DAT	06H	W	8-bit timer modulo register
AR	DAT	40H	R/W	Peripheral address of address register

3.6 Other

Symbol Name	Attribute	Value	Description
USECAP	DAT	0FF11H	Oscillator incorporating capacitor used
NOUSECAP	DAT	0FF22H	Oscillator incorporating capacitor not used
USEPOC	DAT	0FF33H	POC circuit used
NOUSEPOC	DAT	0FF44H	POC circuit not used
DBF	DAT	0FH	Peripheral address for GET/PUT instruction data buffer
IX	DAT	01H	Peripheral address for INC instruction index register
AR_EPA1	DAT	8040H	AR especially when the EPA bit is ON
AR_EPA0	DAT	4040H	AR especially when the EPA bit is OFF

3.7 List of Reserved Words (in Alphabetical Order)

3.7.1 Instructions and quasi-directives

ADD	EXIT	NIBBLE6	SET2
ADDC	EXITR	NIBBLE6V	SET3
AND	EXTRN	NIBBLE7	SET4
BANK0	FLG	NIBBLE7V	SFCOND
BANK1	GET	NIBBLE8	SKE
BANK2	GLOBAL	NIBBLE8V	SKF
BANK3	HALT	NOBMAC	SKF1
BELOW	IF	NOLIST	SKF2
BR	IFCHAR	NOMAC	SKF3
C14344	IFNCHAR	NOP	SKF4
C4444	INC	NOT1	SKGE
CALL	INCLUDE	NOT2	SKLT
CASE	INITFLG	NOT3	SKNE
CLR1	IRP	NOT4	SKT
CLR2	LAB	OBMAC	SKT1
CLR3	LBMAC	OMAC	SKT2
CLR4	LD	OPTION	SKT3
CSEG	LFCOND	OR	SKT4
DAT	LIST	ORG	SMAC
DB	LITERAL	OTHER	ST
DI	LMAC	PEEK	STOP
DW	MACRO	POKE	SUB
EI	MEM	POP	SUBC
EJECT	MOV	PUBLIC	SUMMARY
ELSE	MOVT	PURGE	SYSCAL ^{Note}
END	NIBBLE	PUSH	TAG
ENDCASE	NIBBLE1	PUT	TITLE
ENDIF	NIBBLE2	REPT	XOR
ENDIFC	NIBBLE2V	RET	ZZZERROR
ENDIFNC	NIBBLE3	RETI	ZZZMCHK
ENDM	NIBBLE3V	RETSK	ZZZMSG
ENDOP	NIBBLE4	RORC	ZZZOPT
ENDP	NIBBLE4V	SBMAC	
ENDR	NIBBLE5	SET	
EOF	NIBBLE5V	SET1	

Note Exists only in the AS17244, 17245, and 17246.

3.7.2 Registers and flags

AR	NOUSECAP	P0EBIO3	SP
AR0	NOUSEPOC	P0EBPU0	SYSCK
AR1	NRZ	P0EBPU1	TMC
AR2	NRZBF	P0EBPU2	TMCK0
AR3	NRZHTMM	P0EBPU3	TMCK1
AR_EPA0	NRZLTMM	P0EKEY0	TMEN
AR_EPA1	P0A0	P0EKEY1	TMM
BANK	P0A1	P0EKEY2	TMRES
BCD	P0A2	P0EKEY3	USECAP
BTMCK	P0A3	P1A0	USEPOC
BTMRES	P0B0	P1A1	WDTRES
CMP	P0B1	P1A2	WR
CY	P0B2	P1ABIO0	Z
DBF	P0B3	P1ABIO1	ZZZ0
DBF0	P0BBIO0	P1ABIO2	ZZZ1
DBF1	P0BBIO1	P1ABPU0	ZZZ2
DBF2	P0BBIO2	P1ABPU1	ZZZ3
DBF3	P0BBIO3	P1ABPU2	ZZZ4
IEG	P0C0	P1AHL0	ZZZ5
INT	P0C1	P1AHL1	ZZZ6
INTSEL	P0C2	P1AHL2	ZZZ7
IP	P0C3	P1AKEY0	ZZZ8
IPBTM	P0CGIO	P1AKEY1	ZZZ9
IPTM	P0D0	P1AKEY2	ZZZDEVID
IRQ	P0D1	P1B0	ZZZEPA
IRQBTM	P0D2	P1BBPU0	ZZZLSARG
IRQTM	P0D3	P1BHL0	ZZZPRINT
IX	P0DGIO	P1BKEY0	ZZZSKIP
IXE	P0E0	PSW	ZZZSYDOC
IXH	P0E1	RAMFLAG	ZZZALBMAC
IXL	P0E2	REMCK0	ZZZALMAC
IXM	P0E3	REMCK1	ZZZARGC
MPE	P0EBIO0	REMEM	ZZZLINE
MPH	P0EBIO1	RPH	
MPL	P0EBIO2	RPL	

CHAPTER 4 LOAD MODULE FILE FORMAT

The HEX-format load module files output by the RA17K assembler package come in two output formats: ICE files and PRO files.

These two types of files must be used in accordance with the target application. In addition to a user program area, these files are also provided with other areas, such as an assembly environment data area and an in-circuit emulator operating environment data area.

(1) HEX-format load module file format

The data contained in the HEX-format load module files output by the assembler is output in the format shown in the example below.

[Example of HEX-format load module file format]

```

: 10 0002 00 2B41000BFC80F...3A20 EC
|   |   |   |   |
<1> <2> <3> <4>           <5>           <6>
```

```

: 00 0000 01 FF
|   |   |   |
<1> <2> <3> <4> <6>
```

<1> Record mark

This indicates the start of a record.

<2> Number of codes (2 digits)

This indicates the number of codes (byte data) stored in a record. This value is expressed as a hexadecimal number, with a maximum value of 10H (16 codes). The value for the final record is 00H.

<3> Address (4 digits)

This indicates the start address of the codes appearing in a particular record. The value for the final record is 0000H, and is unrelated to the address.

<4> Record type (2 digits)

A value of 00H indicates that the record is a "data record", and a value of 01H indicates it is the "final record".

<5> Code (up to 32 digits (16 bytes))

Codes are output to this field one byte at a time, up to 16 bytes.

<6> Check sum (2 digits)

The data from fields <2>, <3>, <4>, <5>, and <6> is added in byte units and output to this field (with even parity) as byte data with a value of 00H for the lowest byte.

(2) ICE files

ICE files are files that are output by the RA17K assembler package in a HEX-format exclusive to the in-circuit emulator (IE-17K, IE-17K-ET, or EMU-17K^{Note}). Figure 4-1 shows the output format when assembly is performed using the AS17240, 17241, 17242, 17243, 17244, 17245, and 17246.

Note Manufactured by I.C Corp.

Figure 4-1. ICE File Format (1/7)

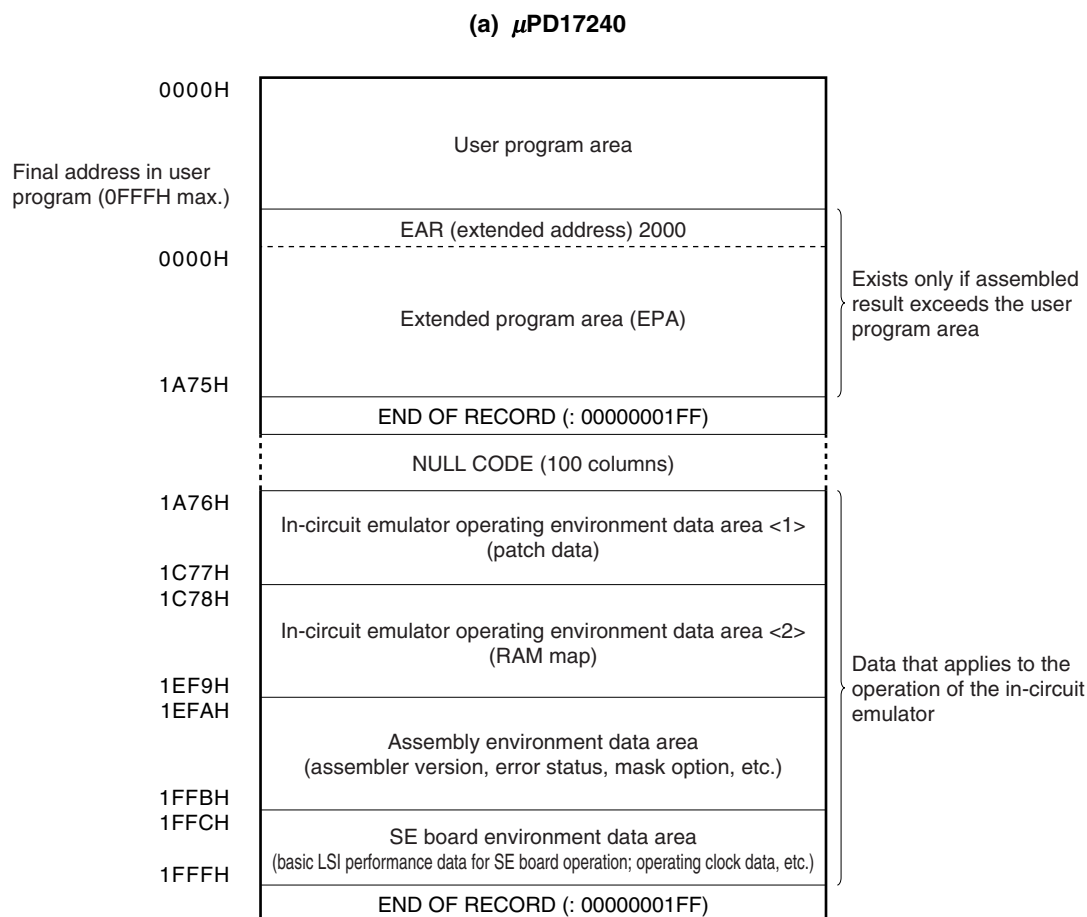


Figure 4-1. ICE File Format (2/7)

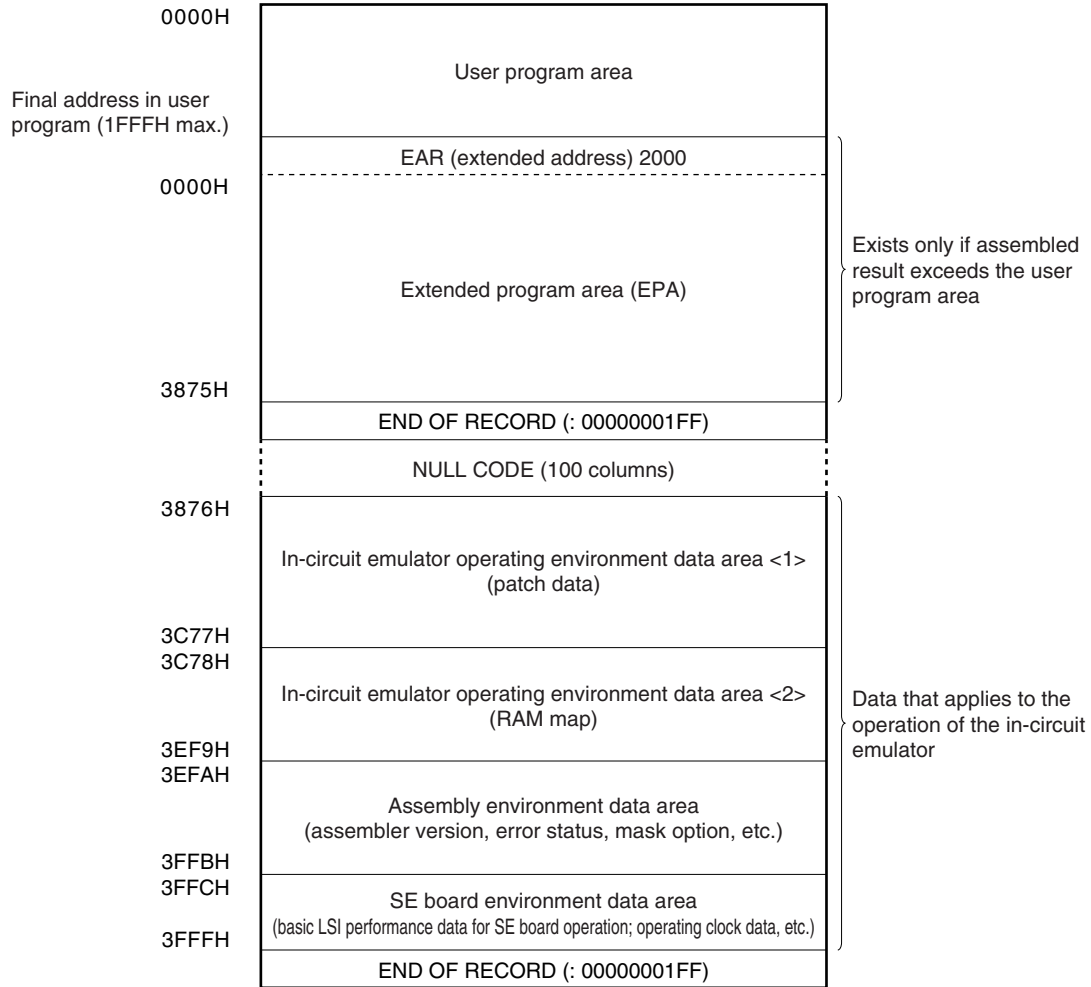
(b) μ PD17241

Figure 4-1. ICE File Format (3/7)

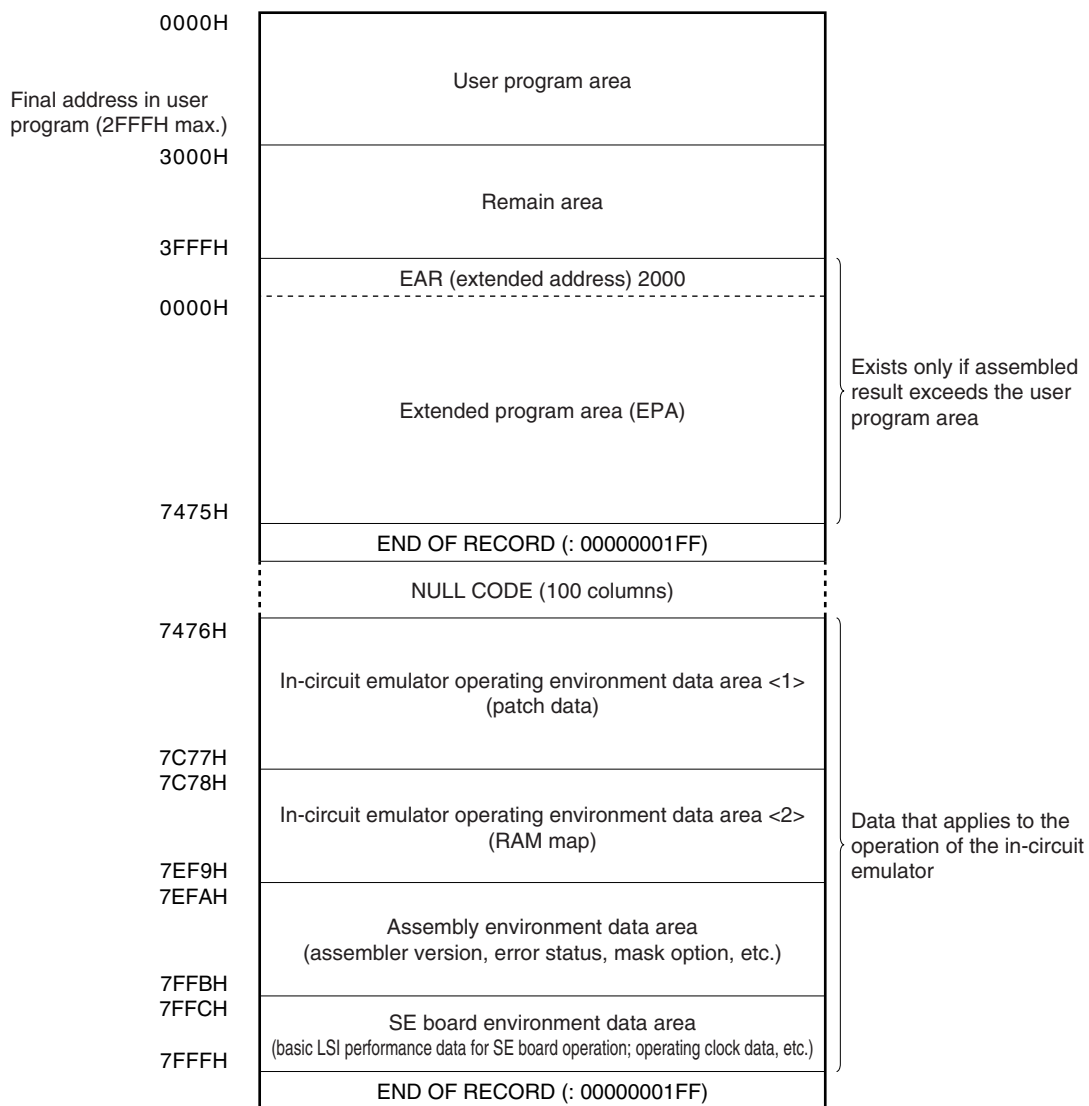
(c) μ PD17242

Figure 4-1. ICE File Format (4/7)

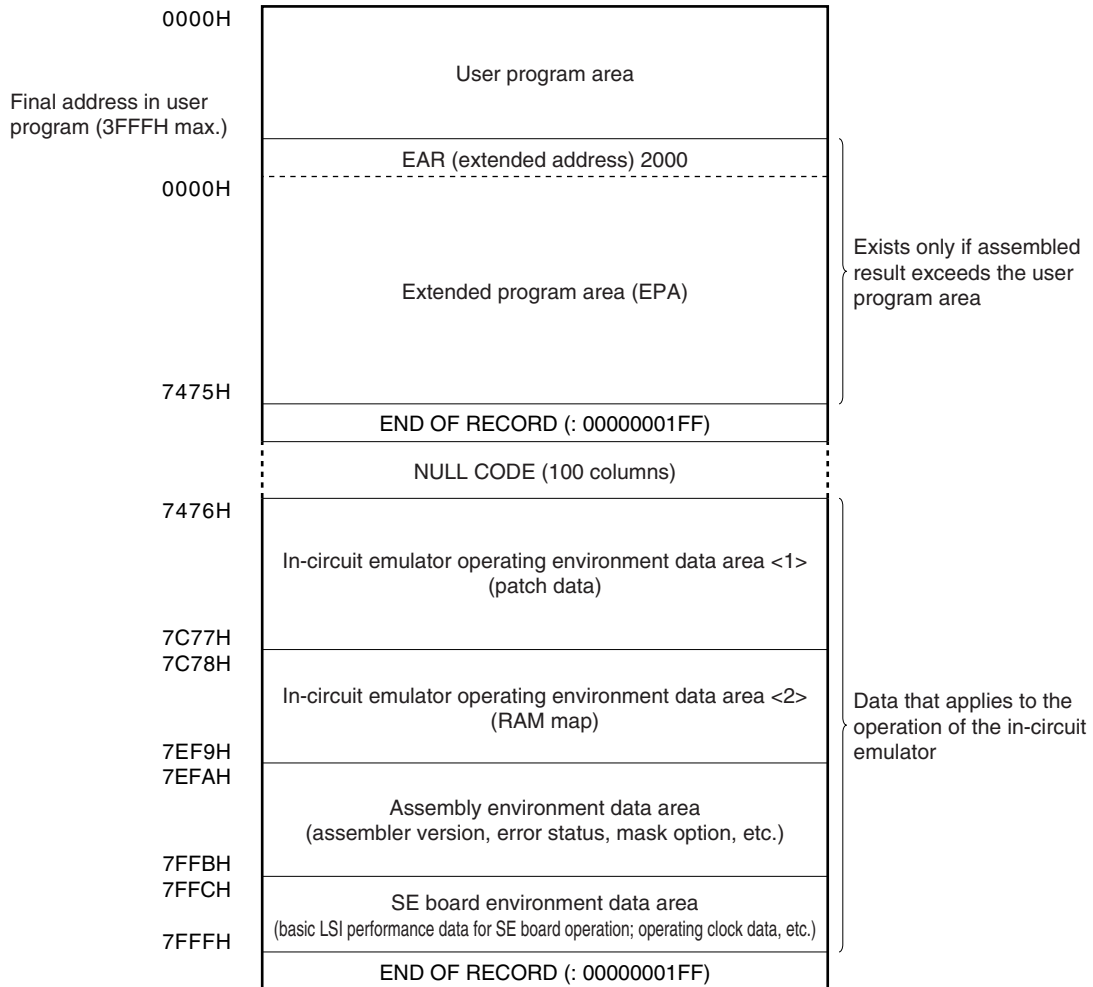
(d) μ PD17243

Figure 4-1. ICE File Format (5/7)

(e) μ PD17244

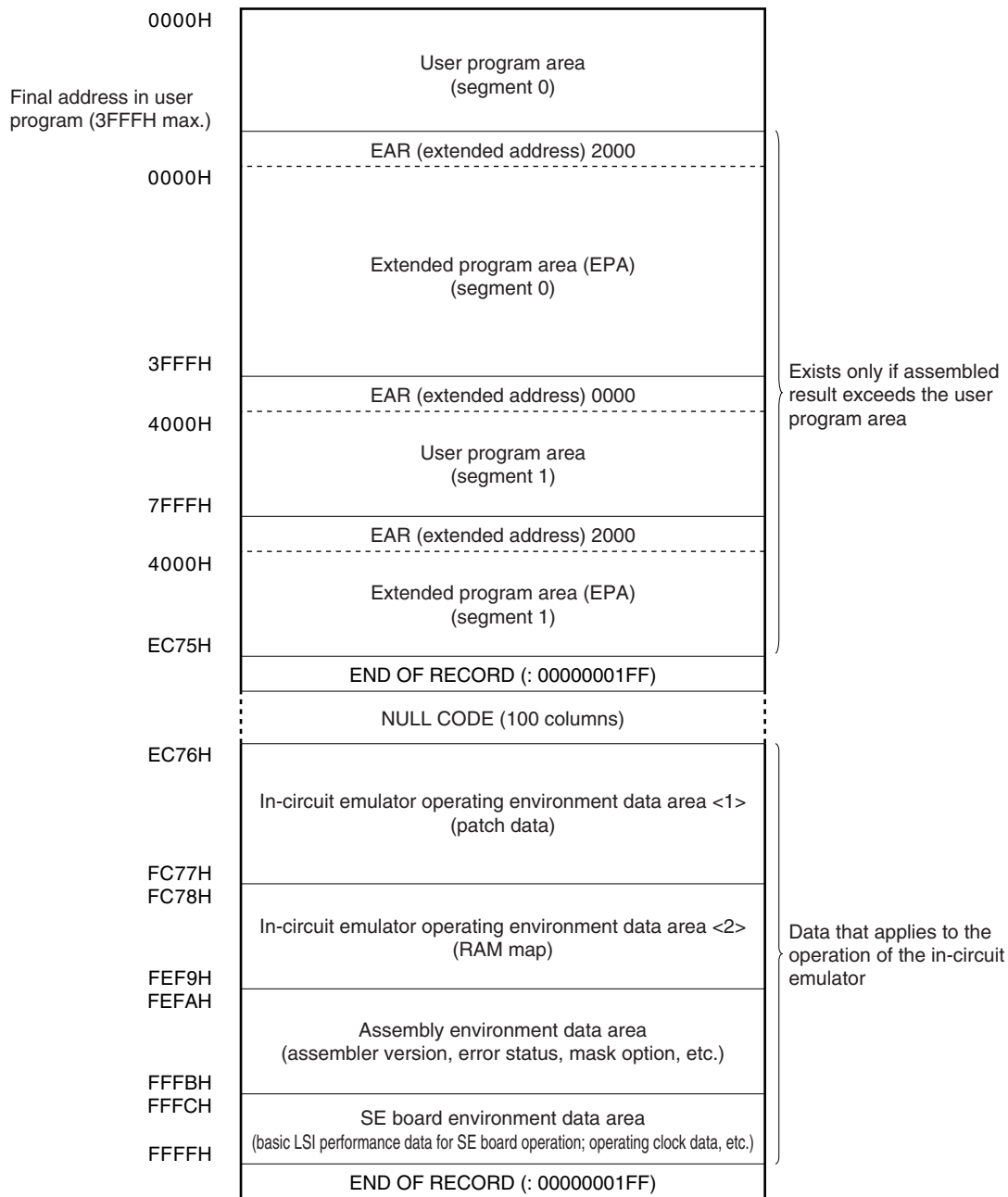
0000H	User program area (segment 0)	
Final address in user program (3FFFH max.)		
0000H	EAR (extended address) 2000	
	Extended program area (EPA) (segment 0)	
3FFFH		
	EAR (extended address) 0000	Exists only if assembled result exceeds the user program area
4000H	User program area (segment 1)	
4FFFH		
5000H	Remain area (segment 1)	
7FFFH		
	EAR (extended address) 2000	
4000H	Extended program area (EPA) (segment 1)	
EC75H	END OF RECORD (: 00000001FF)	
	NULL CODE (100 columns)	
EC76H	In-circuit emulator operating environment data area <1> (patch data)	
FC77H		
FC78H	In-circuit emulator operating environment data area <2> (RAM map)	Data that applies to the operation of the in-circuit emulator
FEF9H		
FEFAH	Assembly environment data area (assembler version, error status, mask option, etc.)	
FFFBH		
FFFCH	SE board environment data area (basic LSI performance data for SE board operation; operating clock data, etc.)	
FFFFH	END OF RECORD (: 00000001FF)	

Figure 4-1. ICE File Format (6/7)

(f) μ PD17245

0000H	User program area (segment 0)	
Final address in user program (3FFFH max.)		
	EAR (extended address) 2000	
0000H		
	Extended program area (EPA) (segment 0)	
3FFFH		
	EAR (extended address) 0000	
4000H	User program area (segment 1)	Exists only if assembled result exceeds the user program area
5FFFH		
6000H	Remain area (segment 1)	
7FFFH		
	EAR (extended address) 2000	
4000H	Extended program area (EPA) (segment 1)	
EC75H	END OF RECORD (: 00000001FF)	
	NULL CODE (100 columns)	
EC76H	In-circuit emulator operating environment data area <1> (patch data)	
FC77H		
FC78H	In-circuit emulator operating environment data area <2> (RAM map)	Data that applies to the operation of the in-circuit emulator
FEF9H		
FEFAH	Assembly environment data area (assembler version, error status, mask option, etc.)	
FFFBH		
FFFCH	SE board environment data area (basic LSI performance data for SE board operation; operating clock data, etc.)	
FFFFH		
	END OF RECORD (: 00000001FF)	

Figure 4-1. ICE File Format (7/7)

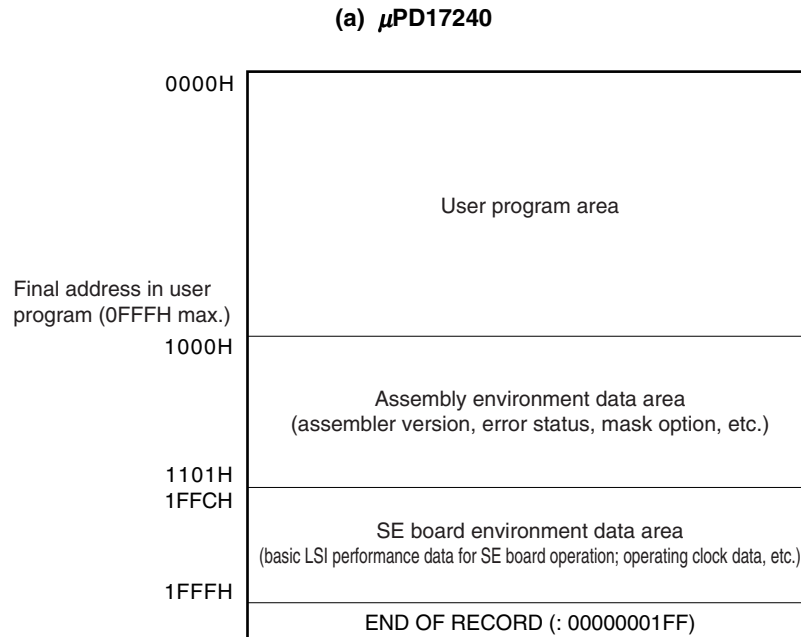
(g) μ PD17246

(3) PRO files

PRO files are files that are output by the RA17K assembler package and contain HEX data, exclusive to PROM and one-time PROM products, that is used for mask ordering and to perform evaluation using discrete SE boards. This data is output by specifying /PRO with an assembly option during assembly.

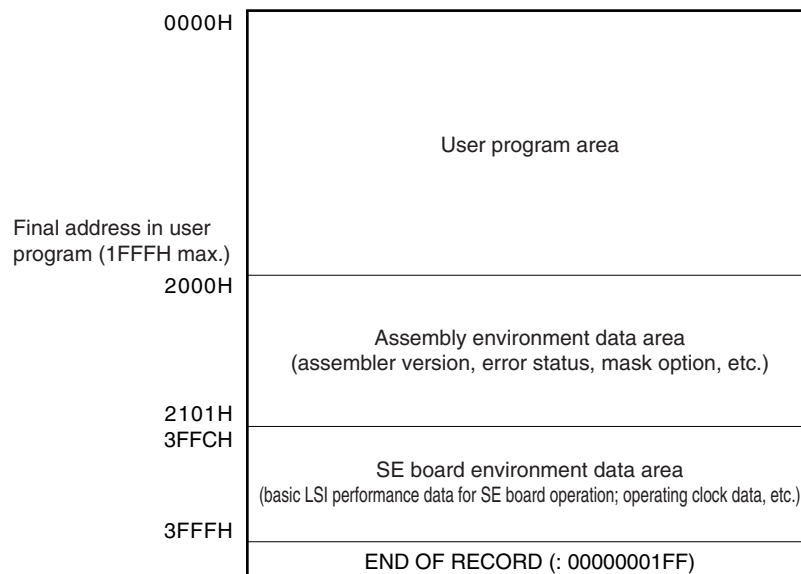
Figure 4-2 shows the output format when assembly is performed using a device file.

Figure 4-2. PRO File Format (1/7)



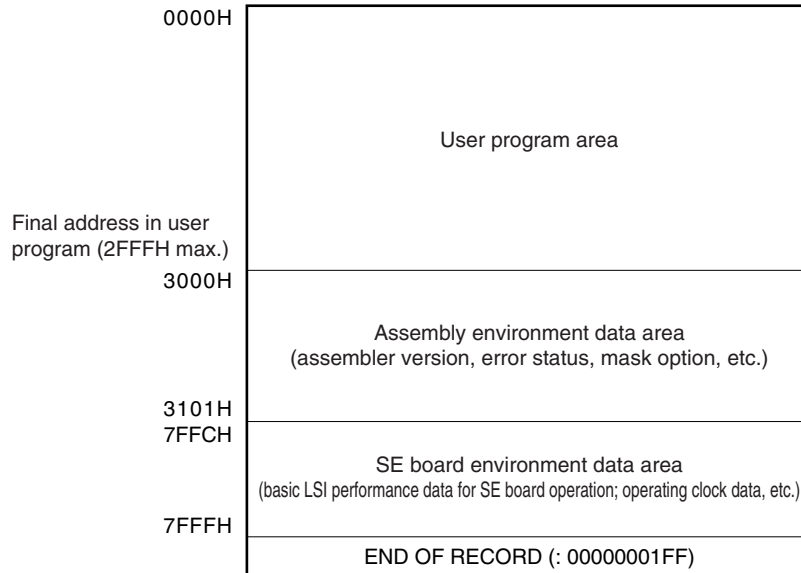
- Remarks**
1. Mask option data used for creating LSI masks is also included in the assembly environment data area, so when ordering masks, mask option documentation is not required.
 2. The range 1102H to 1FFBH does not exist in PRO files.

Figure 4-2. PRO File Format (2/7)

(b) μ PD17241

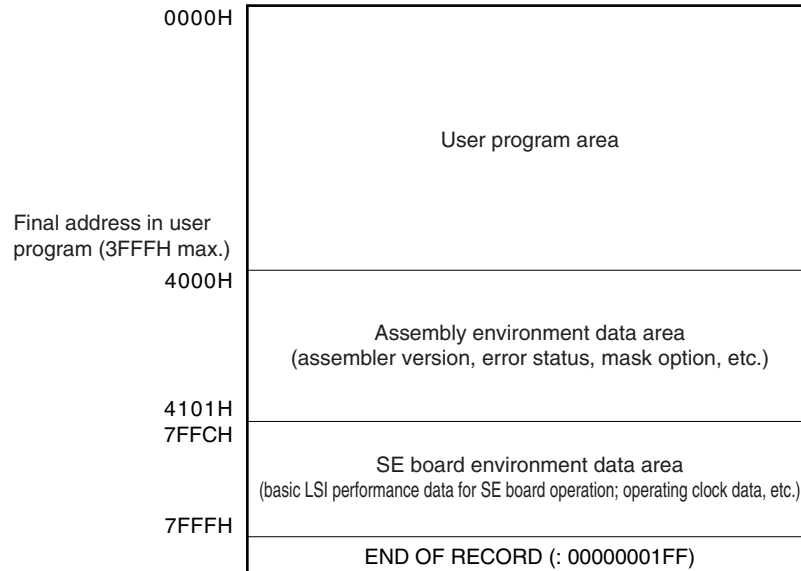
- Remarks**
1. Mask option data used for creating LSI masks is also included in the assembly environment data area, so when ordering masks, mask option documentation is not required.
 2. The range 2102H to 3FFBH does not exist in PRO files.

Figure 4-2. PRO File Format (3/7)

(c) μ PD17242

- Remarks**
1. Mask option data used for creating LSI masks is also included in the assembly environment data area, so when ordering masks, mask option documentation is not required.
 2. The range 3102H to 7FFBH does not exist in PRO files.

Figure 4-2. PRO File Format (4/7)

(d) μ PD17243

- Remarks**
1. Mask option data used for creating LSI masks is also included in the assembly environment data area, so when ordering masks, mask option documentation is not required.
 2. The range 4102H to 7FFBH does not exist in PRO files.

Figure 4-2. PRO File Format (5/7)

(e) μ PD17244

0000H	User program area (segment 0)
3FFFH	
4000H	User program area (segment 1)
4FFFH	
5000H	Assembly environment data area (assembler version, error status, mask option, etc.)
5101H	
5101H	SE board environment data area (basic LSI performance data for SE board operation; operating clock data, etc.)
FFFBH	
FFFFH	END OF RECORD (: 00000001FF)

- Remarks**
- Mask option data used for creating LSI masks is also included in the assembly environment data area, so when ordering masks, mask option documentation is not required.
 - The range 5102H to FFFBH does not exist in PRO files.

Figure 4-2. PRO File Format (6/7)

(f) μ PD17245

0000H	User program area (segment 0)
3FFFH	
4000H	User program area (segment 1)
5FFFH	
6000H	Assembly environment data area (assembler version, error status, mask option, etc.)
6101H	
6FFCH	SE board environment data area (basic LSI performance data for SE board operation; operating clock data, etc.)
FFFFH	
	END OF RECORD (: 00000001FF)

- Remarks**
1. Mask option data used for creating LSI masks is also included in the assembly environment data area, so when ordering masks, mask option documentation is not required.
 2. The range 6102H to FFFBH does not exist in PRO files.

Figure 4-2. PRO File Format (7/7)**(g) μ PD17246**

0000H	User program area (segment 0)
3FFFH	
4000H	User program area (segment 1)
7FFFH	
8000H	Assembly environment data area (assembler version, error status, mask option, etc.)
8101H	
FFCH	SE board environment data area (basic LSI performance data for SE board operation; operating clock data, etc.)
FFFFH	
	END OF RECORD (: 00000001FF)

- Remarks**
1. Mask option data used for creating LSI masks is also included in the assembly environment data area, so when ordering masks, mask option documentation is not required.
 2. The range 8102H to FFFBH does not exist in PRO files.

(4) File comparison of load module files

Even when there are no changes in the source file, changes may occur in the assembler output results (i.e. the assembly environment data area). This is because the data in the assembly environment data area includes items such as the source file creation date.

Table 4-1. Items for Which Assembler Output Result may Change Even When Source File Is Unchanged (1/7)**(a) AS17240**

Item	Address	
	ICE File	PRO File
Program name (character string of up to 32 bytes, specified by assembly option /' PROG=')	1F19H	101FH
<i>SIMPLEHOST</i> data	1FADH	10B3H
Error or warning status	1FB0H	10B6H
File creation date (YMDT) ^{Note}	1FB3H to 1FBDH	10B9H to 10C3H
Device name	1FC8H to 1FD7H	10D7H to 10DDH
Device file version	1FDDH	10E3H
Assembler version	1FE1H	10E7H

Note The creation date/time of the most recent file is written in the source or sequence file.

Caution Do not change only the load module files.

Change load module files by changing the source file or reassembling. Revising load module files only may cause a mismatch of the histories of other files, resulting in bugs.

Table 4-1. Items for Which Assembler Output Result May Change Even When Source File Is Unchanged (2/7)**(b) AS17241**

Item	Address	
	ICE File	PRO File
Program name (character string of up to 32 bytes, specified by assembly option /' PROG=')	3F19H	201FH
<i>SIMPLEHOST</i> data	3FADH	20B3H
Error or warning status	3FB0H	20B6H
File creation date (YMDT) ^{Note}	3FBEH to 3FC7H	20C4H to 20CDH
Device name	3FC8H to 3FD7H	20CEH to 20DDH
Device file version	3FDDH	20E3H
Assembler version	3FE1H	20E7H

Note The creation date/time of the most recent file is written in the source or sequence file.

Caution Do not change only the load module files.

Change load module files by changing the source file or reassembling. Revising load module files only may cause a mismatch of the histories of other files, resulting in bugs.

Table 4-1. Items for Which Assembler Output Result May Change Even When Source File Is Unchanged (3/7)**(c) AS17242**

Item	Address	
	ICE File	PRO File
Program name (character string of up to 32 bytes, specified by assembly option /' PROG=')	7F19H	301FH
<i>SIMPLEHOST</i> data	7FADH	30B3H
Error or warning status	7FB0H	30B6H
File creation date (YMDT) ^{Note}	7FBEH to 7FC7H	30C4H to 30CDH
Device name	7FC8H to 7FD7H	30CEH to 30DDH
Device file version	7FDDH	30E3H
Assembler version	7FE1H	30E7H

Note The creation date/time of the most recent file is written in the source or sequence file.

Caution Do not change only the load module files.

Change load module files by changing the source file or reassembling. Revising load module files only may cause a mismatch of the histories of other files, resulting in bugs.

Table 4-1. Items for Which Assembler Output Result May Change Even When Source File Is Unchanged (4/7)

(d) AS17243

Item	Address	
	ICE File	PRO File
Program name (character string of up to 32 bytes, specified by assembly option /' PROG=')	7F19H	401FH
<i>SIMPLEHOST</i> data	7FADH	40B3H
Error or warning status	7FB0H	40B6H
File creation date (YMDT) ^{Note}	7FBEH to 7FC7H	40C4H to 40CDH
Device name	7FC8H to 7FD7H	40CEH to 40DDH
Device file version	7FDDH	40E3H
Assembler version	7FE1H	40E7H

Note The creation date/time of the most recent file is written in the source or sequence file.

Caution Do not change only the load module files.

Change load module files by changing the source file or reassembling. Revising load module files only may cause a mismatch of the histories of other files, resulting in bugs.

Table 4-1. Items for Which Assembler Output Result May Change Even When Source File Is Unchanged (5/7)**(e) AS17244**

Item	Address	
	ICE File	PRO File
Program name (character string of up to 32 bytes, specified by assembly option /' PROG=')	FF19H	501FH
<i>SIMPLEHOST</i> data	FFADH	50B3H
Error or warning status	FFB0H	50B6H
File creation date (YMDT) ^{Note}	FFBEH to FFC7H	50C4H to 50CDH
Device name	FFC8H to FFD7H	50CEH to 50DDH
Device file version	FFDDH	50E3H
Assembler version	FFE1H	50E7H

Note The creation date/time of the most recent file is written in the source or sequence file.

Caution Do not change only the load module files.

Change load module files by changing the source file or reassembling. Revising load module files only may cause a mismatch of the histories of other files, resulting in bugs.

Table 4-1. Items for Which Assembler Output Result May Change Even When Source File Is Unchanged (6/7)

(f) AS17245

Item	Address	
	ICE File	PRO File
Program name (character string of up to 32 bytes, specified by assembly option /' PROG=')	FF19H	601FH
<i>SIMPLEHOST</i> data	FFADH	60B3H
Error or warning status	FFB0H	60B6H
File creation date (YMDT) ^{Note}	FFBEH to FFC7H	60C4H to 60CDH
Device name	FFC8H to FFD7H	60CEH to 60DDH
Device file version	FFDDH	60E3H
Assembler version	FFE1H	60E7H

Note The creation date/time of the most recent file is written in the source or sequence file.

Caution Do not change only the load module files.

Change load module files by changing the source file or reassembling. Revising load module files only may cause a mismatch of the histories of other files, resulting in bugs.

Table 4-1. Items for Which Assembler Output Result May Change Even When Source File Is Unchanged (7/7)**(g) AS17246**

Item	Address	
	ICE File	PRO File
Program name (character string of up to 32 bytes, specified by assembly option /' PROG=')	FF19H	801FH
<i>SIMPLEHOST</i> data	FFADH	80B3H
Error or warning status	FFB0H	80B6H
File creation date (YMDT) ^{Note}	FFBEH to FFC7H	80C4H to 80CDH
Device name	FFC8H to FFD7H	80CEH to 80DDH
Device file version	FFDDH	80E3H
Assembler version	FFE1H	80E7H

Note The creation date/time of the most recent file is written in the source or sequence file.

Caution Do not change only the load module files.

Change load module files by changing the source file or reassembling. Revising load module files only may cause a mismatch of the histories of other files, resulting in bugs.

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