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Renesas Electronics Corporation

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RENESAS

USER'S MANUAL

Phase-out/Discontinued

AS17207 DEVICE FILE

PC-9800 SERIES (MS-DOS™) BASED

IBM PC/AT™ (PC DOS™) BASED

VERSION 1

Document No. EEU-1360
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USER'S MANUAL

NEC

AS17207 DEVICE FILE

PC-9800 SERIES (MS-DOS) BASED

IBM PC/AT (PC DOS) BASED

VERSION 1

PREFACE

The AS17207 is a device file for use with the AS17K assembler unit to assemble μPD17207 programs.

The AS17207 provides upon assemble the μPD17207 program memory capacity, data memory capacity, usable instructions, reserved symbols, mask option information, etc.

Refer to the AS17K User's Manual (EEU-1287) for details of the AS17K assembler unit and AS17207 device file manipulating procedure.

CONTENTS

Contents of Table

CHPATER 1. DEVICE INFORMATION

The AS17207 device file provides upon assemble the following information concerning the μPD17207.

(1) Program memory (ROM) capacity
4096 x 16 bits (0000H to 0FFFH)

(2) Data memory (RAM) capacity
336 x 4 bits (BANK 0 to BANK 2)

(3) Usable instructions
Refer to **Chapter 2 "μPD17207 Instruction Set".**

(4) Register file, port register and peripheral register read and write information
Refer to **Chapter 3 "Reserved Symbols".**

(5) Reserved symbols
Refer to **Chpater 3 "Reserved Symbols".**

CHAPTER 2. μPD17207 INSTRUCTION SET

2.1 OUTLINE OF INSTRUCTION SET

b_{14}-b_{11} \ b_{15}		0		1	
BIN	HEX				
0000	0	ADD	r, m	ADD	m, #i
0001	1	SUB	r, m	SUB	m, #i
0010	2	ADDC	r, m	ADDC	m, #i
0011	3	SUBC	r, m	SUBC	m, #i
0100	4	AND	r, m	AND	m, #i
0101	5	XOR	r, m	XOR	m, #i
0110	6	OR	r, m	OR	m, #i
0111	7	INC INC MOVT BR CALL RET RETSK EI DI RETI PUSH POP GET PUT PEEK POKE RORC STOP HALT NOP	AR IX DBF, @AR @AR @AR AR AR DBF, p p, DBF WR, RA RA, WR r s h		
1000	8	LD	r, m	ST	m, r
1001	9	SKE	m, #i	SKGE	m, #i
1010	A	MOV	@r, m	MOV	m, @r
1011	B	SKNE	m, #i	SKLT	m, #i
1100	C	BR	addr (page0)	CALL	addr (page0)
1101	D	BR	addr (page1)	MOV	m, #i
1110	E			SKT	m, #n
1111	F			SKF	m, #n

2.2 LEGEND

M	:	Data memory
m	:	Data memory address except banks
m_H	:	Data memory row address
m_L	:	Data memory column address
R	:	General register
r	:	General register column address
RP	:	General register pointer
RF	:	Register file
rf	:	Register file address
rf_H	:	Register file address (upper 3 bits)
rf_L	:	Register file address (lower 4 bits)
AR	:	Address register
IX	:	Index register
IXE	:	Index enable flag
DBF	:	Data buffer
WR	:	Window register
MP	:	Data memory row address pointer
MPE	:	Memory pointer enable flag
PE	:	Peripheral register
p	:	Peripheral address
p_H	:	Peripheral address (upper 3 bits)
p_L	:	Peripheral address (lower 4 bits)
PC	:	Program memory counter
SP	:	Stack pointer
STACK	:	Stack value indicated by the stack pointer
BANK	:	Bank register
(AR)ROM	:	Program memory data indicated by the address register
INTEF	:	Interrupt enable flag
i	:	Immediate data (4 bits)
n	:	Bit position (4 bits)
addr	:	Program memory address (11 bits)
PAGE	:	Most significant bit of program counter
CY	:	Carry flag
s	:	Stop release condition
h	:	Halt release condition
[ ]	:	Data memory or register address
( )	:	Data memory or register value

2.3 INSTRUCTION LIST

Instruction	Mnemonic	Operand	Operation	Machine Code			
				Opcode	3 Bits	4 Bits	4 Bits
Add	ADD	r, m	(R) ← (R) + (M)	00000	m_H	m_L	r
		m, i	(M) ← (M) + i	10000	m_H	m_L	i
	ADDC	r, m	(R) ← (R) + (M) + (CY)	00010	m_H	m_L	r
		m, #i	(M) ← (M) + i + (CY)	10010	m_H	m_L	i
	INC	AR	(AR) ← (AR) + 1	00111	000	1001	0000
		IX	(IX) ← (IX) + 1	00111	000	1000	0000
Subtraction	SUB	r, m	(R) ← (R) − (M)	00001	m_H	m_L	r
		m, #i	(M) ← (M) − i	10001	m_H	m_L	i
	SUBC	r, m	(R) ← (R) − (M) − (CY)	00011	m_H	m_L	r
		m, #i	(M) ← (M) − i − (CY)	10011	m_H	m_L	i
Comparison	SKE	m, #i	(M) − i, skip if zero	01001	m_H	m_L	i
	SKGE	m, #i	(M) − i, skip if not borrow	11001	m_H	m_L	i
	SKLT	m, #i	(M) − i, skip if borrow	11011	m_H	m_L	i
	SKNE	m, #i	(M) − i, skip if not zero	01011	m_H	m_L	i
Logical	AND	m, #i	(M) ← (M) AND i	10100	m_H	m_L	i
		r, m	(R) ← (R) AND (M)	00100	m_H	m_L	r
	OR	m, #i	(M) ← (M) OR i	10110	m_H	m_L	i
		r, m	(R) ← (R) OR (M)	00110	m_H	m_L	r
	XOR	m, #i	(M) ← (M) XOR i	10101	m_H	m_L	i
		r, m	(R) ← (R) XOR (M)	00101	m_H	m_L	r
Transfer	LD	r, m	(R) ← (M)	01000	m_H	m_L	r
	ST	m, r	(M) ← (R)	11000	m_H	m_L	r
	MOV	@r, m	if MPE = 1: [(MP), (R)] ← (M) if MPE = 0: [(m_H), (R)] ← (M)	01010	m_H	m_L	r
		m, @r	if MPE = 1: (M) ← [(MP), (R)] if MPE = 0: (M) ← [(m_H), (R)]	11010	m_H	m_L	r
		m, #i	(M) ← i	11101	m_H	m_L	i
	MOVT	DBF, @AR	SP ← (SP) − 1, STACK ← PC, DBF ← (AR) ROM, PC ← STACK, SP ← (SP) + 1	00111	000	0001	0000
	PUSH	AR	(SP) ← (SP) − 1, (STACK) ← (AR)	00111	000	1101	0000
	POP	AR	(AR) ← (STACK), (SP) ← (SP) + 1	00111	000	1100	0000
	PEEK	WR, rf	(WR) ← (RF)	00111	rf_H	0011	rf_L
	POKE	rf, WR	(RF) ← (WR)	00111	rf_H	0010	rf_L
	GET	DBF, p	(DBF) ← (PE)	00111	P_H	1011	P_L
	PUT	p, DBF	(PE) ← (DBF)	00111	P_H	1010	P_L
Decision	SKT	m, #n	CMP ← 0, skip if M_N = all "1"	11110	m_H	m_L	n
	SKF	m, #n	CMP ← 0, skip if M_N = all "0"	11111	m_H	m_L	n

Instruction	Mnemonic	Operand	Operation	Machine Code			
				Opcode	3 Bits	4 Bits	4 Bits
Branch	BR	addr	PC ← addr, PAGE ← 0	01100	addr		
			PC ← addr, PAGE ← 1	01101	addr		
		@AR	PC ← AR	00111	000	0100	0000
Shift	RORC	r	(CY) → (R) → CY	00111	000	0111	r
Subroutine	CALL	addr	SP ← (SP) − 1, STACK ← ((PC) + 1), PC ← addr, PAGE ← 0	11100	addr		
		@AR	SP ← (SP) − 1, STACK ← ((PC) + 1), PC ← (AR)	00111	000	0101	0000
	RET		PC ← (STACK), SP ← (SP) + 1	00111	000	1110	0000
	RETSK		PC ← (STACK), SP ← (SP) + 1 and skip	00111	001	1110	0000
	RETI		PC ← (STACK), SP ← (SP) + 1	00111	100	1110	0000
Interrupt	EI		INTEF ← 1	00111	000	1111	0000
	DI		INTEF ← 0	00111	001	1111	0000
Others	STOP	s	STOP	00111	010	1111	s
	HALT	h	HALT	00111	011	1111	h
	NOP		No operation	00111	100	1111	0000

2.4 ASSEMBLER (AS17K) INTRINSIC MACRO INSTRUCTIONS

Legend

flag : One of flag1 to flagn

flag1 to flagn : Flag names indicated by reserved words

n : Number

< > : May be omitted.

	Mnemonic	Operand	n	Operation
Intrinsic macro instructions	SKTn	flag1, ... flagn	$1 \leqq n \leqq 4$	if (flag1) to (flagn) = all "1", then skip
	SKFn	flag1, ... flagn	$1 \leqq n \leqq 4$	if (flag1) to (flagn) = all "0", then skip
	SKTn	flag1, ... flagn	$1 \leqq n \leqq 4$	(flag1) to (flagn) ← 1
	CLRn	flag1, ... flagn	$1 \leqq n \leqq 4$	(flag1) to (flagn) ← 0
	NOTn	flag1, ... flagn	$1 \leqq n \leqq 4$	if (flag) = "0", then (flag) ← 1, & if (flag) = "1", then (flag) ← 0
	INITFLG	<NOT> flag1, ... <NOT> flagn	4	if description = NOT flag, then (flag) ← 0 if description = flag, then (flag) ← 1
	BANKn		$0 \leqq n \leqq 2$	(BANK) ← n

CHAPTER 3. RESERVED SYMBOLS

The symbols defined in the μPD17207 device file are shown below and on the following pages. The defined symbols are listed below.

- Data buffer
- System register
- LCD segment data register
- Port register
- Register file (control register)
- Peripheral register

3.1 DATA BUFFER

Symbol Name	Attribute	Value	R/W	Description
DBF3	MEM	0.0CH	R/W	Bits 15 to 12 of data buffer
DBF2	MEM	0.0DH	R/W	Bits 11 to 8 of data buffer
DBF1	MEM	0.0EH	R/W	Bits 7 to 4 of data buffer
DBF0	MEM	0.0FH	R/W	Bits 3 to 0 of data buffer

3.2 SYSTEM REGISTER

Symbol Name	Attribute	Value	R/W	Description
AR3	MEM	0.74H	R	Bits 15 to 12 of address register
AR2	MEM	0.75H	R/W	Bits 11 to 8 of address register
AR1	MEM	0.76H	R/W	Bits 7 to 4 of address register
AR0	MEM	0.77H	R/W	Bits 3 to 0 of address register
WR	MEM	0.78H	R/W	Window register
BANK	MEM	0.79H	R/W	Bank register
IXH	MEM	0.7AH	R/W	Bits 11 to 8 of index register
MPH	MEM	0.7AH	R/W	Bits 7 to 4 of memory pointer
MPE	FLG	0.7AH.3	R/W	Memory pointer enable flag
IXM	MEM	0.7BH	R/W	Bits 7 to 4 of index register
MPL	MEM	0.7BH	R/W	Bits 3 to 0 of memory pointer
IXL	MEM	0.7CH	R/W	Bits 3 to 0 of index register
RPH	MEM	0.7DH	R/W	Bits 7 to 4 of register pointer
RPL	MEM	0.7EH	R/W	Bits 3 to 0 of register pointer
PSW	MEM	0.7FH	R/W	Program status word
BCD	FLG	0.7EH.0	R/W	BCD operation flag
CMP	FLG	0.7FH.3	R/W	Compare flag
CY	FLG	0.7FH.2	R/W	Carry flag
Z	FLG	0.7FH.1	R/W	Zero flag
IXE	FLG	0.7FH.0	R/W	Index register enable flag

3.3 LCD SEGMENT DATA REGISTER

Symbol Name	Attribute	Value	R/W	Description
LCDD0	MEM	0.40H	R/W	LCD segment 0
LCDD1	MEM	0.41H	R/W	LCD segment 1
LCDD2	MEM	0.42H	R/W	LCD segment 2
LCDD3	MEM	0.43H	R/W	LCD segment 3
LCDD4	MEM	0.44H	R/W	LCD segment 4
LCDD5	MEM	0.45H	R/W	LCD segment 5
LCDD6	MEM	0.46H	R/W	LCD segment 6
LCDD7	MEM	0.47H	R/W	LCD segment 7
LCDD8	MEM	0.48H	R/W	LCD segment 8
LCDD9	MEM	0.49H	R/W	LCD segment 9
LCDD10	MEM	0.4AH	R/W	LCD segment 10
LCDD11	MEM	0.4BH	R/W	LCD segment 11
LCDD12	MEM	0.4CH	R/W	LCD segment 12
LCDD13	MEM	0.4DH	R/W	LCD segment 13
LCDD14	MEM	0.4EH	R/W	LCD segment 14
LCDD15	MEM	0.4FH	R/W	LCD segment 15
LCDD16	MEM	0.50H	R/W	LCD segment 16
LCDD17	MEM	0.51H	R/W	LCD segment 17
LCDD18	MEM	0.52H	R/W	LCD segment 18
LCDD19	MEM	0.53H	R/W	LCD segment 19
LCDD20	MEM	0.54H	R/W	LCD segment 20
LCDD21	MEM	0.55H	R/W	LCD segment 21
LCDD22	MEM	0.56H	R/W	LCD segment 22
LCDD23	MEM	0.57H	R/W	LCD segment 23
LCDD24	MEM	0.58H	R/W	LCD segment 24
LCDD25	MEM	0.59H	R/W	LCD segment 25
LCDD26	MEM	0.5AH	R/W	LCD segment 26
LCDD27	MEM	0.5BH	R/W	LCD segment 27
LCDD28	MEM	0.5CH	R/W	LCD segment 38
LCDD29	MEM	0.5DH	R/W	LCD segment 39
LCDD30	MEM	0.5EH	R/W	LCD segment 30
LCDD31	MEM	0.5FH	R/W	LCD segment 31
LCDD32	MEM	0.60H	R/W	LCD segment 32
LCDD33	MEM	0.61H	R/W	LCD segment 33
LCDD34	MEM	0.62H	R/W	LCD segment 34
LCDD35	MEM	0.63H	R/W	LCD segment 35

3.4 PORT REGISTER

Symbol Name	Attribute	Value	R/W	Description
P0A0	FLG	0.70H.0	R/W	Bit 0 of port 0A
P0A1	FLG	0.70H.1	R/W	Bit 1 of port 0A
P0A2	FLG	0.70H.2	R/W	Bit 2 of port 0A
P0A3	FLG	0.70H.3	R/W	Bit 3 of port 0A
P0B0	FLG	0.71H.0	R/W	Bit 0 of port 0B
P0B1	FLG	0.71H.1	R/W	Bit 1 of port 0B
P0B2	FLG	0.71H.2	R/W	Bit 2 of port 0B
P0B3	FLG	0.71H.3	R/W	Bit 3 of port 0B
P0C0	FLG	0.72H.0	R/W	Bit 0 of port 0C
P0C1	FLG	0.72H.1	R/W	Bit 1 of port 0C
P0C2	FLG	0.72H.2	R/W	Bit 2 of port 0C
P0C3	FLG	0.72H.3	R/W	Bit 3 of port 0C
P0D0	FLG	0.73H.0	R/W	Bit 0 of port 0D
P0D1	FLG	0.73H.1	R/W	Bit 1 of port 0D
P0D2	FLG	0.73H.2	R/W	Bit 2 of port 0D
P0D3	FLG	0.73H.3	R/W	Bit 3 of port 0D
P1A0	FLG	1.70H.0	R/W	Bit 0 of port 1A
P1A1	FLG	1.70H.1	R/W	Bit 1 of port 1A
P1A2	FLG	1.70H.2	R/W	Bit 2 of port 1A
P1A3	FLG	1.70H.3	R/W	Bit 3 of port 1A

3.5 REGISTER RILE (CONTROL REGISTER)

Symbol Name	Attribute	Value	R/W	Description
SP	MEM	0.81H	R/W	Stack pointer
SYSCK	FLG	0.82H.1	R/W	System clock selection
XEN	FLG	0.82H.0	R/W	Main clock enable
WDTRES	FLG	0.83H.3	R/W	Watchdog timer reset
WTMMD	FLG	0.83H.2	R/W	Clock timer mode selection
WTMRES	FLG	0.83H.1	R/W	Clock timer mode reset
VDDDET1	FLG	0.87H.3	R	VDD detect flag 1
VDDDET0	FLG	0.87H.2	R	VDD detect flag 0
INT	FLG	0.8FH.0	R	Interrupt pin status
NRZBF	FLG	0.91H.0	R/W	NRZ buffer data
NRZ	FLG	0.92H.0	R/W	NRZ data
ADCCMP	FLG	0.0A0H.0	R/W	Comparator result
VREFEN	FLG	0.0A1H.3	R/W	ADC enable flag
ADCEN	FLG	0.0A1H.2	R/W	ADC enable flag
ADCCH1	FLG	0.0A1H.1	R/W	ADC channel select #1
ADCCH0	FLG	0.0A1H.0	R/W	ADC channel select #0
SIOTS	FLG	0.0A2H.3	R/W	Serial interface
SIOHIZ	FLG	0.0A2H.2	R/W	SO port selection
SIOCK1	FLG	0.0A2H.1	R/W	Serial interface clock #1
SIOCK0	FLG	0.0A2H.0	R/W	Serial interface clock #0
NRZEN	FLG	0.0A3H.2	R/W	NRZ enable flag
TMOE	FLG	0.0A3H.1	R/W	Timer output enable flag
SIOEN	FLG	0.0A3H.0	R/W	SIO enable flag
P0DBIO3	FLG	0.0A7H.3	R/W	P0D port bit 3 input/output set flag
P0DBIO2	FLG	0.0A7H.2	R/W	P0D port bit 2 input/output set flag
P0DBIO1	FLG	0.0A7H.1	R/W	P0D port bit 1 input/output set flag
P0DBIO0	FLG	0.0A7H.0	R/W	P0D port bit 0 input/output set flag
IPSIO	FLG	0.0AFH.3	R/W	INTSIO interrupt enable flag
IPWTM	FLG	0.0AFH.2	R/W	Clock timer interrupt enable flag
IP	FLG	0.0AFH.1	R/W	INT interrupt enable flag
IPTM	FLG	0.0AFH.0	R/W	8-bit timer interrupt enable flag
LCDEN	FLG	0.0B1H.3	R/W	LCD display enable flag
LCDCK2	FLG	0.0B1H.2	R/W	LCD display clock set #2
LCDCK1	FLG	0.0B1H.1	R/W	LCD display clock set #1
LCDCK0	FLG	0.0B1H.0	R/W	LCD display clock set #0

Symbol Name	Attribute	Value	R/W	Description
LCDMD3	FLG	0.0B2H.3	R/W	LCD display mode set #3
LCDMD2	FLG	0.0B2H.2	R/W	LCD display mode set #2
LCDMD1	FLG	0.0B2H.1	R/W	LCD display mode set #1
LCDMD0	FLG	0.0B2H.0	R/W	LCD display mode set #0
TMEN	FLG	0.0B3H.3	R/W	Timer enable flag
TMRES	FLG	0.0B3H.2	R/W	Timer reset flag
TMCK1	FLG	0.0B3H.1	R/W	Timer clock source selection
TMCK0	FLG	0.0B3H.0	R/W	Timer clock source selection
P1AGIO	FLG	0.0B7H.3	R/W	P1A port input/output set flags
P0CGIO	FLG	0.0B7H.2	R/W	P0C port input/output set flags
P0BGIO	FLG	0.0B7H.1	R/W	P0B port input/output set flags
P0AGIO	FLG	0.0B7H.0	R/W	P0A port input/output set flags
IRQSIO	FLG	0.0BBH.3	R/W	SIO interrupt request flag
IRQWTM	FLG	0.0BCH.2	R/W	Clock timer interrupt request flag
IRQ	FLG	0.0BDH.1	R/W	INT interrupt request flag
IRQTM	FLG	0.0BEH.0	R/W	8-bit timer interrupt request flag

3.6 PERIPHERAL REGISTER

Symbol Name	Attribute	Value	R/W	Description
SIOSFR	DAT	01H	R/W	Serial I/O register
TMM	DAT	02H	W	8-bit timer modulo register
TMC	DAT	02H	R	8-bit timer count register
NRZLTMM	DAT	03H	R/W	NRZ low-level period set modulo register
NRZHTMM	DAT	04H	R/W	NRZ high-level period set modulo register
ADCR	DAT	05H	R/W	ADC reference voltage set register
AR	DAT	40H	R/W	Address register

3.7 RESERVED WORD LIST (IN ALPHABETICAL ORDER)

3.7.1 Instructions and Pseudo-Instructions

ADD
ADDC
AND
BANK0
BANK1
BANK2
BELOW
BR
C14344
C4444
CALL
CASE
CLR1
CLR2
CLR3
CLR4
CSEG
DAT
DB
DI
DW
EI
EJECT
ELSE
END
ENDCASE
ENDIF
ENDIFC
ENDIFNC
ENDM
ENDOP
ENDP
ENDR
EOF
EXIT
EXITR
ENTRN
FLG
GET
CLOBAL
HALT
IF
IFCHAR
IFNCHAR
INC
INCLUDE
INITFLG
IRP
LAB
LBMAC
LD
LFCOND
LIST
LITERAL
LMAC
MACRO
MEM
MOV
MOVT
NIBBLE
NIBBLE1
NIBBLE2
NIBBLE2V
NIBBLE3
NIBBLE3V
NIBBLE4
NIBBLE4V
NIBBLE5
NIBBLE5V
NIBBLE6
NIBBLE6V
NIBBLE7
NIBBLE7V
NIBBLE8
NIBBLE8V
NOBMAC
NOLIST
NOMAC
NOP
NOT1
NOT2
NOT3
NOT4
OBMAC
OMAC
OPTION
OR
ORG
OTHER
PEEK
POKE
POP
PUBLIC
PURGE
PUSH
PUT
REPT
RET
RETI
RETSK
RORC
SBMAC
SET
SET1
SET2
SET3
SET4
SFCOND
SKE
SKF
SKF1
SKF2
SKF3
SKF4
SKGE
SKLT
SKNE
SKT
SKT1
SKT2
SKT3
SKT4
SMAC
ST
STOP
SUB
SUBC
SUMMARY
TAG
TITLE
XOR
ZZZERROR
ZZZMCHK
ZZZMSG
ZZZOPT

Phase-out/Discontinued

3.7.2 Registers and Flags

ADCCH0
ADCCH1
ADCCMP
ADCEN
ADCR
AR
AR0
AR1
AR2
AR3
AR_EPA0
AR_EPA1
BANK
BCD
CMP
CY
DBF
DBF0
DBF1
DBF2
DBF3
INT
IP
IPSIO
IPTM
IPWTM
IRQ
IRQSIO
IRQTM
IRQWTM
IX
IXE
IXH
IXL
IXM
LCDCK0
LCDCK1
LCDCK2
LCDD0
LCDD1
LCDD10
LCDD11
LCDD12
LCDD13
LCDD14
LCDD15
LCDD16
LCDD17
LCDD18
LCDD19
LCDD2
LCDD20
LCDD21
LCDD22
LCDD23
LCDD24
LCDD25
LCDD26
LCDD27
LCDD28
LCDD29
LCDD3
LCDD30
LCDD31
LCDD32
LCDD33
LCDD34
LCDD35
LCDD4
LCDD5
LCDD6
LCDD7
LCDD8
LCDD9
LCDEN
LCDMD0
LCDMD1
LCDMD2
LCDMD3
MPE
MPH
MPL
NOX
NOXT
NRZ
NRZBF
NRZEN
NRZHTMM
NRZLTMM
OPEN
P0A0
P0A1
P0A2
P0A3
P0AGIO
P0B0
P0B1
P0B2
P0B3
P0BGIO
P0C0
P0C1
P0C2
P0C3
P0CGIO
P0D0
P0D1
P0D2
P0D3
P0DBIO0
P0DBIO1
P0DBIO2
P0DBIO3
P1A0
P1A1
P1A2
P1A3
P1AGIO
PSW
RESPLUP
RPH
RPL
SIOCK0
SIOCK1
SIOEN
SIOHIZ
SIOSFR
SIOTS
SP
SYSCK
TMC
TMCK0
TMCK1
TMEN
TMM
TMOE
TMRES
USEX
USEXT
VDDDET0
VDDDET1
VREFEN
WDTRE
WR
WTMMD
WTMRES
XEN
Z
ZZZ0
ZZZ1
ZZZ2
ZZZ3
ZZZ4
ZZZ5
ZZZ6
ZZZ7
ZZZ8
ZZZ9
ZZZDEVID
ZZZEPA
ZZZLSARG
ZZZPRINT
ZZZSKIP
ZZZSYDOC
ZZZALBMZC
ZZZALMAC
ZZZARGC
ZZZLINE

CHAPTER 4. MASK OPTION DEFINITION PSEUDO-INSTRUCTIONS

When creating a μPD17207 program, it is necessary to specify mask options in the assembler source program using mask option definition psuedo-instructions.

Mask options are necessary for the following items:

- $\overline{\text{RESET}}$ pin pull-up resistor on-chip
- Connection of main clock and subclock (system clock selection)

4.1 OPTION AND ENDOP PSEUDO-INSTRUCTIONS

The block from the OPTION pseudo-instruction to the ENDOP pseudo-instruction is called the mask option definition block.

The mask option define block description format is shown below.

[Description format]

Symbol Field	Mnemonic Field	Operand Field	Comment Field
[Label:]	OPTION		[;comment]
	:		
	ENDOP		

4.2 MASK OPTION DEFINITION PSEUDO-INSTRUCTIONS

A mask option definition example is shown below.

Symbol Field	Mnemonic Field	Operand Field	Comment Field
[Label:]	OPTION		[;comment]
	OPTRES	RESPLUP	; pull-up
	OPTCK	USEX, USEXT	; used main clock
	ENDOP		; used subclock

Table 4-1 "Mask Option Definition Pseudo-instruction List" shows pseudo-instructions which can be used in the mask option define block.

Table 4-1 Mask Option Definition Pseudo-Instruction List

Item	Mask Option Definition Pseudo-Instruction	First Operand	Second Operand
$\overline{\text{RESET}}$ pin pull-up resistor	OPTRES	RESPLUP (with pull-up resistor) OPEN (without pull-up resistor)	
System clock	OPTCK	Main clock	Subclock
		USEX (main clock is used as system clock) NOX (not used main clock)	USEXT (subclock is used as system clock) NOXT (not used subclock)

Remarks: If both main clock and subclock are used as system clock, select main clock at reset. After this selection, the subclock can be selected by using instruction in program.

Phase-out/Discontinued

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