To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   “Specific”: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

USER'S MANUAL

RENESAS

AS17071

DEVICE FILE

Version V1

PC-9800 Series (MS-DOS™) Base
IBM PC/AT™ (PC DOS™) Base

Target Device: μPD17071
μPD17072
μPD17073

Document No. U11116EJ3V0UM00 (3rd edition)
(Previous No. EEU-1512)
Date Published April 1996 P
Printed in Japan

Major Revised Points in this Publication

Page	Contents
Throughout	A description of the μPD17071 device files has been added.
Cover, Introduction	• AS17073 has been deleted. • The product name has been changed from AS17072 to AS17071.
Introduction	The explanation has been changed: The μPD17072 and 17073 device files have been included in the AS17071.

The mark ★ shows major revised points.

Introduction

Device files are files those contain data (device data) that is unique to and dependent upon the 17K Series devices. This data is required when using the following 17K Series software development tools.

- AS17K assembler or RA17K assembler package (under development)
- *SIMPLEHOST®*

The following device files are included in the AS17071. ★

- μPD17071 device file
- μPD17072 device file
- μPD17073 device file

The device files have the file extension .DEV.

[Files Included in the AS17071]

File names
D17071 .DEV, D17072 .DEV, D17073 .DEV

For details of the AS17K assembler and the use of device files bundled with the μPD17071, 17072 and AS17073, see the **AS17K Assembler User's Manual (EEU-1287)**.

[MEMO]

CONTENTS

[MEMO]

CHAPTER 1 DEVICE DATA

In assembly time, the device files provide the following data related to the device.

(1) Program memory (ROM) capacity

μPD17071: 2048 × 16 bits (0000H - 07FFH) ★
μPD17072: 3072 × 16 bits (0000H - 0BFFH)
μPD17073: 4096 × 16 bits (0000H - 0FFFH)

(2) Data memory (RAM) capacity

μPD17071: 128 × 4 bits (BANK0, BANK1) ★
μPD17072, 17073: 176 × 4 bits (BANK0, BANK1)

(3) Usable instructions

See **CHAPTER 2 INSTRUCTION SET.**

(4) Peripheral control registers, port register, and peripheral hardware register read and write data

See **CHAPTER 3 RESERVED SYMBOLS.**

(5) Reserved symbols

See **CHAPTER 3 RESERVED SYMBOLS.**

(6) Device files, device numbers, and SE board numbers

Device files contain a register of device numbers for each device and SE board numbers to indicate optimum SE boards for developing various products. These device files are also included in ICE files and PRO files output by the assembler (AS17K). These devices are used when the in-circuit emulator checks the development environment and during checking of mask orders.

Table 1-1. Relations among Device Files, Device Numbers, and SE Board Numbers

Device file (version)	Device name	Device number	SE board number	SE board
AS17071 (V1)	μPD17071	58H	4CH	SE-17072
	μPD17072	4CH		
	μPD17073	4FH		

★

[MEMO]

CHAPTER 2 INSTRUCTION SET

2.1 Instruction Set Summary

b_{14} - b_{11} \ b_{15}		0		1	
BIN	HEX				
0000	0	ADD	r, m	ADD	m, #n4
0001	1	SUB	r, m	SUB	m, #n4
0010	2	ADDC	r, m	ADDC	m, #n4
0011	3	SUBC	r, m	SUBC	m, #n4
0100	4	AND	r, m	AND	m, #n4
0101	5	XOR	r, m	XOR	m, #n4
0110	6	OR	r, m	OR	m, #n4
0111	7	INC RORC MOVT PUSH POP GET PUT BR CALL RET RETSK RETI EI DI STOP HALT NOP	AR r DBF, @AR AR AR DBF, p p, DBF @AR @AR s h		
1000	8	LD	r,m	ST	m, r
1001	9	SKE	m, #n4	SKGE	m, #n4
1010	A	MOV	@r,m	MOV	m, @r
1011	B	SKNE	m, #n4	SKLT	m, #n4
1100	C	BR	addr (page 0)	CALL	addr
1101	D	BR	addr (page 1)	MOV	m, #n4
1110	E			SKT	m, #n
1111	F			SKF	m, #n

2.2 Legend

AR : Address register
ASR : Address stack register indicated by stack pointers
addr : Program memory address (lower 11 bits)
BANK : Bank register
CMP : Compare flag
CY : Carry flag
DBF : Data buffer
h : Halt cancellation conditions
INTEF : Interrupt enable flag
INTR : Register that is automatically saved to a stack when an interrupt occurs
INTSK : Interrupt stack register
MP : Data memory row address pointer
MPE : Memory pointer enable flag
m : Data memory address indicated by mR and mC
mR : Data memory row address (high)
mC : Data memory column address (low)
n : Bit position (4 bits)
n4 : Immediate data (4 bits)
PAGE : Page (Bit 11 of program counter)
PC : Program counter
p : Peripheral address
pH : Peripheral address (higher 3 bits)
pL : Peripheral address (lower 4 bits)
r : General register column address
SP : Stack pointer
s : Stop cancellation conditions
(×) : × indicates addressed contents

2.3 Instruction List

Instruction set	Mnemonic	Operand	Operation	Instruction code			
				Op code	Operand		
Add	ADD	r, m	(r) ← (r) + (m)	00000	m_R	mc	r
		m, #n4	(m) ← (m) + n4	10000	m_R	mc	n4
	ADDC	r, m	(r) ← (r) + (m) + CY	00010	m_R	mc	r
		m, #n4	(m) ← (m) + n4 + CY	10010	m_R	mc	n4
	INC	AR	AR ← AR + 1	00111	000	1001	0000
Subtract	SUB	r, m	(r) ← (r) − (m)	00001	m_R	mc	r
		m, #n4	(m) ← (m) − n4	10001	m_R	mc	n4
	SUBC	r, m	(r) ← (r) − (m) − CY	00011	m_R	mc	r
		m, #n4	(m) ← (m) − n4 − CY	10011	m_R	mc	n4
Logical operation	OR	r, m	(r) ← (r) ∨ (m)	00110	m_R	mc	r
		m, #n4	(m) ← (m) ∨ n4	10110	m_R	mc	n4
	AND	r, m	(r) ← (r) ∧ (m)	00100	m_R	mc	r
		m, #n4	(m) ← (m) ∧ n4	10100	m_R	mc	n4
	XOR	r, m	(r) ← (r) ∀ (m)	00101	m_R	mc	r
		m, #n4	(m) ← (m) ∀ n4	10101	m_R	mc	n4
Decision	SKT	m, #n	CMP ← 0, if (m) ∧ n = n, then skip	11110	m_R	mc	n
	SKF	m, #n	CMP ← 0, if (m) ∧ n = 0, then skip	11111	m_R	mc	n
Comparison	SKE	m, #n4	(m) − n4, skip if zero	01001	m_R	mc	n4
	SKNE	m, #n4	(m) − n4, skip if not zero	01011	m_R	mc	n4
	SKGE	m, #n4	(m) − n4, skip if not borrow	11001	m_R	mc	n4
	SKLT	m, #n4	(m) − n4, skip if borrow	11011	m_R	mc	n4
Rotation	RORC	r	→ CY → (r) $_{b3}$ → (r) $_{b2}$ → (r) $_{b1}$ → (r) $_{b0}$ →	00111	000	0111	r
Transfer	LD	r, m	(r) ← (m)	01000	m_R	mc	r
	ST	m, r	(m) ← (r)	11000	m_R	mc	r
	MOV	@r, m	if MPE = 1 : (MP, (r)) ← (m) if MPE = 0 : (BANK, m_R, (r)) ← (m)	01010	m_R	mc	r
		m, @r	if MPE = 1 : (m) ← (MP, (r)) if MPE = 0 : (m) ← (BANK, m_R, (r))	11010	m_R	mc	r
		m, #n4	(m) ← n4	11101	m_R	mc	n4
	MOVT	DBF, @AR	SP ← SP−1, ASR ← PC, PC ← AR, DBF ← (PC), PC ← ASR, SP ← SP + 1	00111	000	0001	0000
	PUSH	AR	SP ← SP −1, ASR ← AR	00111	000	1101	0000
	POP	AR	AR ← ASR, SP ← SP + 1	00111	000	1100	0000
	GET	DBF, p	DBF ← (p)	00111	p_H	1011	p_L
	PUT	p, DBF	(p) ← DBF	00111	p_H	1010	p_L

Instruction set	Mnemonic	Operand	Operation	Instruction code			
				Op code	Operand		
Branch	BR	addr	**Note**	**Note**	addr		
		@AR	PC ← AR	00111	000	0100	0000
Subroutine	CALL	addr	SP ← SP – 1, ASR ← PC PC_{11} ← 0, PC_{10-0} ← addr	11100	addr		
		@AR	SP ← SP –1, ASR ← PC PC ← AR	00111	000	0101	0000
	RET		PC ← ASR, SP ← SP + 1	00111	000	1110	0000
	RETSK		PC ← ASR, SP ← SP + 1 and skip	00111	001	1110	0000
	RETI		PC ← ASR, INTR ← INTSK, SP ← SP + 1	00111	010	1110	0000
Interrupt	EI		INTEF ← 1	00111	001	1111	0000
	DI		INTEF ← 0	00111	001	1111	0000
Other	STOP	s	STOP	00111	010	1111	s
	HALT	h	HALT	00111	011	1111	h
	NOP		No operation	00111	100	1111	0000

Note The "BR addr" operation of the μPD17071, 17072 and 17073 and its op codes are as follows:

(a) μPD17071

Mnemonic	Operand	Operation	Op Code
BR	addr	PC_{10-0} ← addr	01100

(b) μPD17072, 17073

Mnemonic	Operand	Operation	Op Code
BR	addr	PC_{10-0} ← addr, PAGE ← 0	01100
		PC_{10-0} ← addr, PAGE ← 1	01101

2.4 Macro Instructions Bundled with Assembler (AS17K)

Legend

flag n : FLG-type symbol
n : Bit No.
< > : Contents between < > symbols can be omitted.

Instruction set	Mnemonic	Operand	Operation	n
Bundled macros	SKTn	flag 1, ··· flag n	if (flag 1) to (flag n) = all "1", then skip	1 ≤ n ≤ 4
	SKFn	flag 1, ··· flag n	if (flag 1) to (flag n) = all "0", then skip	1 ≤ n ≤ 4
	SETn	flag 1, ··· flag n	(flag 1) to (flag n) ← 1	1 ≤ n ≤ 4
	CLRn	flag 1, ··· flag n	(flag 1) to (flag n) ← 0	1 ≤ n ≤ 4
	NOTn	flag 1, ··· flag n	if (flag n) = "0", then (flag n) ← 1 if (flag n) = "1", then (flag n) ← 0	1 ≤ n ≤ 4
	INTFLG	<NOT> flag 1, ··· <<NOT> flag n>	if description = NOT flag n, then (flag n) ← 0 if description = flag n, then (flag n) ← 1	1 ≤ n ≤ 4
	BANKn		(BANK) ← n	n = 0, 1

[MEMO]

CHAPTER 3 RESERVED SYMBOLS

The symbols defined for the μPD17071, 17072 and 17073 device files are described on the following pages. These symbols are listed below.

- Data buffer (DBF)
- System register (SYSREG)
- LCD segment register
- Port register
- Peripheral control register
- Peripheral hardware register
- Other

3.1 Data Buffer (DBF)

Symbol name	Attribute	Value	R/W	Description
DBF3	MEM	0.0CH	R/W	DBF bits b15 to b12
DBF2	MEM	0.0DH	R/W	DBF bits b11 to b8
DBF1	MEM	0.0EH	R/W	DBF bits b7 to b4
DBF0	MEM	0.0FH	R/W	DBF bits b3 to b0

3.2 System Register (SYSREG)

Symbol name	Attribute	Value	R/W	Description
AR2	MEM	0.75H	R/W	Address register bits b11 to b8
AR1	MEM	0.76H	R/W	Address register bits b7 to b4
AR0	MEM	0.77H	R/W	Address register bits b3 to b0
BANK	MEM	0.79H	R/W	Bank register
BCD	FLG	0.7EH.0	R/W	BCD flag
PSW	MEM	0.7FH	R/W	Program status word
CMP	FLG	0.7FH.3	R/W	Compare flag
CY	FLG	0.7FH.2	R/W	Carry flag
Z	FLG	0.7FH.1	R/W	Zero flag

3.3 LCD Segment Register

Symbol name	Attribute	Value	R/W	Description
LCDD14	MEM	1.41H	R/W	LCD segment register
LCDD13	MEM	1.42H	R/W	LCD segment register
LCDD12	MEM	1.43H	R/W	LCD segment register
LCDD11	MEM	1.44H	R/W	LCD segment register
LCDD10	MEM	1.45H	R/W	LCD segment register
LCDD9	MEM	1.46H	R/W	LCD segment register
LCDD8	MEM	1.47H	R/W	LCD segment register
LCDD7	MEM	1.48H	R/W	LCD segment register
LCDD6	MEM	1.49H	R/W	LCD segment register
LCDD5	MEM	1.4AH	R/W	LCD segment register
LCDD4	MEM	1.4BH	R/W	LCD segment register
LCDD3	MEM	1.4CH	R/W	LCD segment register
LCDD2	MEM	1.4DH	R/W	LCD segment register
LCDD1	MEM	1.4EH	R/W	LCD segment register
LCDD0	MEM	1.4FH	R/W	LCD segment register

3.4 Port Register

Symbol name	Attribute	Value	R/W	Description
P0A3	FLG	0.70H.3	R/W	Port 0A bit b3
P0A2	FLG	0.70H.2	R/W	Port 0A bit b2
P0A1	FLG	0.70H.1	R/W	Port 0A bit b1
P0A0	FLG	0.70H.0	R/W	Port 0A bit b0
P0B3	FLG	0.71H.3	R/W	Port 0B bit b3
P0B2	FLG	0.71H.2	R/W	Port 0B bit b2
P0B1	FLG	0.71H.1	R/W	Port 0B bit b1
P0B0	FLG	0.71H.0	R/W	Port 0B bit b0
P0C1	FLG	0.72H.1	R/W	Port 0C bit 1
P0C0	FLG	0.72H.0	R/W	Port 0C bit 0
P0D3	FLG	0.73H.3	R/W	Port 0D bit 3
P0D2	FLG	0.73H.2	R/W	Port 0D bit 2
P1A3	FLG	1.70H.3	R/W[Note]	Port 1A bit 3
P1A2	FLG	1.70H.2	R/W[Note]	Port 1A bit 2
P1A1	FLG	1.70H.1	R/W[Note]	Port 1A bit 1
P1A0	FLG	1.70H.0	R/W[Note]	Port 1A bit 0
P1B3	FLG	1.71H.3	R/W	Port 1B bit 3
P1B2	FLG	1.71H.2	R/W	Port 1B bit 2
P1B1	FLG	1.71H.1	R/W	Port 1B bit 1
P1B0	FLG	1.71H.0	R/W	Port 1B bit 0
P1C0	FLG	1.72H.0	R/W	Port 1C bit 0

Note These ports are input-only ports. The assembler and IE-17K will not output error messages if an instruction to output from these ports has been entered. Also, if the messages are actually executed on a device, the operation will have no change.

3.5 Peripheral Control Register

★ (1) μPD17071

Symbol name	Attribute	Value	R/W	Description
LCDEN	FLG	1.50H.0	R/W	LCD driver display start flag
BTM0CY	FLG	1.51H.0	R & Res	Basic timer zero carry-FF status detection flag
CE	FLG	1.52H.0	R	CE pin status detection flag
P1APLD3	FLG	1.53H.3	R/W	P1A3/AD1 pin's pull-down resistor select flag
P1APLD2	FLG	1.53H.2	R/W	P1A2/AD0 pin's pull-down resistor select flag
P1APLD1	FLG	1.53H.1	R/W	P1A1 pin's pull-down resistor select flag
P1APLD0	FLG	1.53H.0	R/W	P1A0 pin's pull-down resistor select flag
SP	MEM	1.54H	R/W	Stack pointer
BTM1CKD	FLG	1.59H.0	R	Basic timer 1 clock detection flag
BEEP0CK1	FLG	1.5BH.1	R/W	BEEP clock select flag
BEEP0CK0	FLG	1.5BH.0	R/W	BEEP clock select flag
IFCMD1	FLG	1.62H.3	R/W	IF counter mode select flag
IFCMD0	FLG	1.62H.2	R/W	IF counter mode select flag
IFCCK1	FLG	1.62H.1	R/W	IF counter clock select flag
IFCCK0	FLG	1.62H.0	R/W	IF counter clock select flag
IFCG	FLG	1.63H.0	R	IF counter gate status detection flag (0: closed, 1: open)
IFCSTRT	FLG	1.64H.1	W	IF counter count start flag
IFCRES	FLG	1.64H.0	W	IF counter reset flag
PLLMD3	FLG	1.65H.3	R	PLL mode select flag (fixed to "0")
PLLMD2	FLG	1.65H.2	R	PLL mode select flag (fixed to "0")
PLLMD1	FLG	1.65H.1	R/W	PLL mode select flag
PLLMD0	FLG	1.65H.0	R/W	PLL mode select flag
PLLRFCK3	FLG	1.66H.3	R	PLL reference frequency select flag (fixed to "0")
PLLRFCK2	FLG	1.66H.2	R/W	PLL reference frequency select flag
PLLRFCK1	FLG	1.66H.1	R/W	PLL reference frequency select flag
PLLRFCK0	FLG	1.66H.0	R/W	PLL reference frequency select flag
PLLR17	FLG	1.67H.3	R/W	PLL data flag
PLLR16	FLG	1.67H.2	R/W	PLL data flag
PLLR15	FLG	1.67H.1	R/W	PLL data flag
PLLR14	FLG	1.67H.0	R/W	PLL data flag
PLLR13	FLG	1.68H.3	R/W	PLL data flag
PLLR12	FLG	1.68H.2	R/W	PLL data flag
PLLR11	FLG	1.68H.1	R/W	PLL data flag
PLLR10	FLG	1.68H.0	R/W	PLL data flag
PLLR9	FLG	1.69H.3	R/W	PLL data flag
PLLR8	FLG	1.69H.2	R/W	PLL data flag
PLLR7	FLG	1.69H.1	R/W	PLL data flag
PLLR6	FLG	1.69H.0	R/W	PLL data flag

Symbol name	Attribute	Value	R/W	Description
PLLR5	FLG	1.6AH.3	R/W	PLL data flag
PLLR4	FLG	1.6AH.2	R/W	PLL data flag
PLLR3	FLG	1.6AH.1	R/W	PLL data flag
PLLR2	FLG	1.6AH.0	R/W	PLL data flag
PLLR1	FLG	1.6BH.3	R/W	PLL data flag
PLLPUT	FLG	1.6CH.0	W	PLL data set flag
PLLUL	FLG	1.6DH.0	R & Res	PLL unlock FF flag
P0BBIO3	FLG	1.6EH.3	R/W	$P0B_3$ I/O select flag
P0BBIO2	FLG	1.6EH.2	R/W	$P0B_2$ I/O select flag
P0BBIO1	FLG	1.6EH.1	R/W	$P0B_1$ I/O select flag
P0BBIO0	FLG	1.6EH.0	R/W	$P0B_0$ I/O select flag
P0DBIO3	FLG	1.6FH.3	R/W	$P0D_3$ I/O select flag
P0DBIO2	FLG	1.6FH.2	R/W	$P0D_2$ I/O select flag
P0CBIO1	FLG	1.6FH.1	R/W	$P0C_1$ I/O select flag
P0CBIO0	FLG	1.6FH.0	R/W	$P0C_0$ I/O select flag

(2) μPD17072, 17073

Symbol name	Attribute	Value	R/W	Description
ADCON	FLG	1.50H.1	R/W	Power supply setting flag for A/D converter control signal
LCDEN	FLG	1.50H.0	R/W	LCD driver enable flag
BTM0CY	FLG	1.51H.0	R & Res	Basic timer zero carry-FF status detection flag
CE	FLG	1.52H.0	R	CE pin status detection flag
P1APLD3	FLG	1.53H.3	R/W	P1A3/AD1 pin's pull-down resistor select flag
P1APLD2	FLG	1.53H.2	R/W	P1A2/AD0 pin's pull-down resistor select flag
P1APLD1	FLG	1.53H.1	R/W	$P1A_1$ pin's pull-down resistor select flag
P1APLD0	FLG	1.53H.0	R/W	$P1A_0$ pin's pull-down resistor select flag
SP	MEM	1.54H	R/W	Stack pointer
SYSCK	FLG	1.55H.0	R/W	System clock select flag (1: 106.6 μs, 0: 53.3 μs)
INT	FLG	1.56H.2	R/W	INT pin status detection flag
BRM1CK	FLG	1.56H.1	R/W	Basic timer 1 clock select flag
IEG	FLG	1.56H.0	R/W	INT pin interrupt request detection edge direction select flag
IPSIO	FLG	1.57H.2	R/W	Serial interface interrupt enable flag
IPBTM1	FLG	1.57H.1	R/W	Basic timer 1 interrupt enable flag
IP	FLG	1.57H.0	R/W	INT pin interrupt enable flag
IRQ	FLG	1.58H.0	R/W	INT pin interrupt request detection flag
IRQBTM1	FLG	1.59H.0	R/W	Basic timer 1 interrupt request detection flag
IRQSIO	FLG	1.5AH.0	R/W	Serial interface interrupt request detection flag
BEEP0CK1	FLG	1.5BH.1	R/W	BEEP clock select flag
BEEP0CK0	FLG	1.5BH.0	R/W	BEEP clock select flag
ADCCH3	FLG	1.5CH.3	R	A/D converter channel select flag (fixed to "0")
ADCCH2	FLG	1.5CH.2	R	A/D converter channel select flag (fixed to "0")
ADCCH1	FLG	1.5CH.1	R/W	A/D converter channel select flag
ADCCH0	FLG	1.5CH.0	R/W	A/D converter channel select flag
ADCRFSEL3	FLG	1.5DH.3	R/W	A/D converter reference voltage setting flag
ADCRFSEL2	FLG	1.5DH.2	R/W	A/D converter reference voltage setting flag
ADCRFSEL1	FLG	1.5DH.1	R/W	A/D converter reference voltage setting flag
ADCRFSEL0	FLG	1.5DH.0	R/W	A/D converter reference voltage setting flag
ADCSTRT	FLG	1.5EH.0	R/W	A/D converter comparison start flag
ADCCMP	FLG	1.5FH.0	R	A/D converter comparison result detection flag
SIOSEL	FLG	1.60H.2	R/W	Serial in/Serial out pin select flag
SIOHIZ	FLG	1.60H.1	R/W	Serial interface/general-purpose port select flag
SIOTS	FLG	1.60H.0	R/W	Serial interface transmit/receive start flag

Symbol name	Attribute	Value	R/W	Description
SIOCK3	FLG	1.61H.3	R	Serial interface I/O clock select flag (fixed to "0")
SIOCK2	FLG	1.61H.2	R	Serial interface I/O clock select flag (fixed to "0")
SIOCK1	FLG	1.61H.1	R/W	Serial interface I/O clock select flag
SIOCK0	FLG	1.61H.0	R/W	Serial interface I/O clock select flag
IFCMD1	FLG	1.62H.3	R/W	IF counter mode select flag
IFCMD0	FLG	1.62H.2	R/W	IF counter mode select flag
IFCCK1	FLG	1.62H.1	R/W	IF counter clock select flag
IFCCK0	FLG	1.62H.0	R/W	IF counter clock select flag
IFCG	FLG	1.63H.0	R	IF counter gate status detection flag (0: closed, 1: open)
IFCSTRT	FLG	1.64H.1	W	IF counter count start flag
IFCRES	FLG	1.64H.0	W	IF counter reset flag
PLLMD3	FLG	1.65H.3	R	PLL mode select flag (fixed to "0")
PLLMD2	FLG	1.65H.2	R	PLL mode select flag (fixed to "0")
PLLMD1	FLG	1.65H.1	R/W	PLL mode select flag
PLLMD0	FLG	1.65H.0	R/W	PLL mode select flag
PLLRFCK3	FLG	1.66H.3	R	PLL reference frequency select flag (fixed to "0")
PLLRFCK2	FLG	1.66H.2	R/W	PLL reference frequency select flag
PLLRFCK1	FLG	1.66H.1	R/W	PLL reference frequency select flag
PLLRFCK0	FLG	1.66H.0	R/W	PLL reference frequency select flag
PLLR17	FLG	1.67H.3	R/W	PLL data flag
PLLR16	FLG	1.67H.2	R/W	PLL data flag
PLLR15	FLG	1.67H.1	R/W	PLL data flag
PLLR14	FLG	1.67H.0	R/W	PLL data flag
PLLR13	FLG	1.68H.3	R/W	PLL data flag
PLLR12	FLG	1.68H.2	R/W	PLL data flag
PLLR11	FLG	1.68H.1	R/W	PLL data flag
PLLR10	FLG	1.68H.0	R/W	PLL data flag
PLLR9	FLG	1.69H.3	R/W	PLL data flag
PLLR8	FLG	1.69H.2	R/W	PLL data flag
PLLR7	FLG	1.69H.1	R/W	PLL data flag
PLLR6	FLG	1.69H.0	R/W	PLL data flag
PLLR5	FLG	1.6AH.3	R/W	PLL data flag
PLLR4	FLG	1.6AH.2	R/W	PLL data flag
PLLR3	FLG	1.6AH.1	R/W	PLL data flag
PLLR2	FLG	1.6AH.0	R/W	PLL data flag
PLLR1	FLG	1.6BH.3	R/W	PLL data flag
PLLPUT	FLG	1.6CH.0	W	PLL data set flag
PLLUL	FLG	1.6DH.0	R & Res	PLL unlock FF flag

Symbol name	Attribute	Value	R/W	Description
P0BBIO3	FLG	1.6EH.3	R/W	$P0B_3$ I/O select flag
P0BBIO2	FLG	1.6EH.2	R/W	$P0B_2$ I/O select flag
P0BBIO1	FLG	1.6EH.1	R/W	$P0B_1$ I/O select flag
P0BBIO0	FLG	1.6EH.0	R/W	$P0B_0$ I/O select flag
P0DBIO3	FLG	1.6FH.3	R/W	$P0D_3$ I/O select flag
P0DBIO2	FLG	1.6FH.2	R/W	$P0D_2$ I/O select flag
P0CBIO1	FLG	1.6FH.1	R/W	$P0C_1$ I/O select flag
P0CBIO0	FLG	1.6FH.0	R/W	$P0C_0$ I/O select flag

3.6 Peripheral Hardware Register

★ (1) μPD17071

Symbol name	Attribute	Value	R/W	Description
AR	DAT	40H	R/W	GET/PUT/PUSH/CALL/BR/MOVT instruction address register
IFC	DAT	43H	R	Middle frequency (IF) counter data register

(2) μPD17072, 17073

Symbol name	Attribute	Value	R/W	Description
SIOSFR	DAT	03H	R/W	Serial interface presettable shift register
AR	DAT	40H	R/W	GET/PUT/PUSH/CALL/BR/MOVT instruction address register
IFC	DAT	43H	R	Middle frequency (IF) counter data register

3.7 Other

Symbol name	Attribute	Value	R/W	Description
DBF	DAT	0FH	–	Fixed operand value for GET/PUT/MOVT instructions
AR_EPA1	DAT	8040H	–	Operand (EPA bit ON) for CALL/BR/MOVT instructions
AR_EPA0	DAT	4040H	–	Operand (EPA bit OFF) for CALL/BR/MOVT instructions

3.8 List of Reserved Words (in Alphabetical Order)

3.8.1 Instructions and pseudo-instructions

(1) μPD17071 ★

ADD	EXTRN	NIBBLE5V	SET2
ADDC	FLG	NIBBLE6	SET3
AND	GET	NIBBLE6V	SET4
BANK0	GLOBAL	NIBBLE7	SFCOND
BANK1	HALT	NIBBLE7V	SKE
BELOW	IF	NIBBLE8	SKF
BR	IFCHAR	NIBBLE8V	SKF1
C14344	IFNCHAR	NOBMAC	SKF2
C4444	INC	NOLIST	SKF3
CALL	INCLUDE	NOMAC	SKF4
CASE	INITFLG	NOP	SKGE
CLR1	IRP	NOT1	SKLT
CLR2	LAB	NOT2	SKNE
CLR3	LBMAC	NOT3	SKT
CLR4	LD	NOT4	SKT1
CSEG	LFCOND	OBMAC	SKT2
DAT	LIST	OMAC	SKT3
DB	LITERAL	OR	SKT4
DW	LMAC	ORG	SMAC
EJECT	MACRO	OTHER	ST
ELSE	MEM	POP	STOP
END	MOV	PUBLIC	SUB
ENDCASE	MOVT	PURGE	SUBC
ENDIF	NIBBLE	PUSH	SUMMARY
ENDIFC	NIBBLE1	PUT	TAG
ENDIFNC	NIBBLE2	REPT	TITLE
ENDM	NIBBLE2V	RET	XOR
ENDP	NIBBLE3	RETSK	ZZZERROR
ENDR	NIBBLE3V	RORC	ZZZMCHK
EOF	NIBBLE4	SBMAC	ZZZMSG
EXIT	NIBBLE4V	SET	
EXITR	NIBBLE5	SET1	

(2) μPD17072, 17073

ADD	EXITR	NIBBLE5V	SET2
ADDC	EXTRN	NIBBLE6	SET3
AND	FLG	NIBBLE6V	SET4
BANK0	GET	NIBBLE7	SFCOND
BANK1	GLOBAL	NIBBLE7V	SKE
BELOW	HALT	NIBBLE8	SKF
BR	IF	NIBBLE8V	SKF1
C14344	IFCHAR	NOBMAC	SKF2
C4444	IFNCHAR	NOLIST	SKF3
CALL	INC	NOMAC	SKF4
CASE	INCLUDE	NOP	SKGE
CLR1	INITFLG	NOT1	SKLT
CLR2	IRP	NOT2	SKNE
CLR3	LAB	NOT3	SKT
CLR4	LBMAC	NOT4	SKT1
CSEG	LD	OBMAC	SKT2
DAT	LFCOND	OMAC	SKT3
DB	LIST	OR	SKT4
DI	LITERAL	ORG	SMAC
DW	LMAC	OTHER	ST
EI	MACRO	POP	STOP
EJECT	MEM	PUBLIC	SUB
ELSE	MOV	PURGE	SUBC
END	MOVT	PUSH	SUMMARY
ENDCASE	NIBBLE	PUT	TAG
ENDIF	NIBBLE1	REPT	TITLE
ENDIFC	NIBBLE2	RET	XOR
ENDIFNC	NIBBLE2V	RETI	ZZZERROR
ENDM	NIBBLE3	RETSK	ZZZMCHK
ENDP	NIBBLE3V	RORC	ZZZMSG
ENDR	NIBBLE4	SBMAC	
EOF	NIBBLE4V	SET	
EXIT	NIBBLE5	SET1	

3.8.2 Registers and flags

(1) μPD17071 ★

AR	LCDD12	P1A0	PLLR7
AR0	LCDD13	P1A1	PLLR8
AR1	LCDD14	P1A2	PLLR9
AR2	LCDD2	P1A3	PLLRFCK0
AR_EPA0	LCDD3	P1APLD0	PLLRFCK1
AR_EPA1	LCDD4	P1APLD1	PLLRFCK2
BANK	LCDD5	P1APLD2	PLLRFCK3
BCD	LCDD6	P1APLD3	PLLUL
BEEP0CK0	LCDD7	P1B0	PSW
BEEP0CK1	LCDD8	P1B1	SP
BTM0CY	LCDD9	P1B2	Z
BTM1CKD	LCDEN	P1B3	ZZZ0
CE	P0A0	P1C0	ZZZ1
CMP	P0A1	PLLMD0	ZZZ2
CY	P0A2	PLLMD1	ZZZ3
DBF	P0A3	PLLMD2	ZZZ4
DBF0	P0B0	PLLMD3	ZZZ5
DBF1	P0B1	PLLPUT	ZZZ6
DBF2	P0B2	PLLR1	ZZZ7
DBF3	P0B3	PLLR10	ZZZ8
IFC	P0BBIO0	PLLR11	ZZZ9
IFCCK0	P0BBIO1	PLLR12	ZZZDEVID
IFCCK1	P0BBIO2	PLLR13	ZZZEPA
IFCG	P0BBIO3	PLLR14	ZZZLSARG
IFCMD0	P0C0	PLLR15	ZZZPRINT
IFCMD1	P0C1	PLLR16	ZZZSKIP
IFCRES	P0CBIO0	PLLR17	ZZZSYDOC
IFCSTRT	P0CBIO1	PLLR2	ZZZALBMAC
LCDD0	P0D2	PLLR3	ZZZALMAC
LCDD1	P0D3	PLLR4	ZZZARGC
LCDD10	P0DBIO2	PLLR5	ZZZLINE
LCDD11	P0DBIO3	PLLR6	

(2) μPD17072, 17073

ADCCH0	IFCG	P0B3	PLLR13
ADCCH1	IFCMD0	P0BBIO0	PLLR14
ADCCH2	IFCMD1	P0BBIO1	PLLR15
ADCCH3	IFCRES	P0BBIO2	PLLR16
ADCCMP	IFCSTRT	P0BBIO3	PLLR17
ADCON	INT	P0C0	PLLR2
ADCRFSEL0	IP	P0C1	PLLR3
ADCRFSEL1	IPBTM1	P0CBIO0	PLLR4
ADCRFSEL2	IPSIO	P0CBIO1	PLLR5
ADCRFSEL3	IRQ	P0D2	PLLR6
ADCSTRT	IRQBTM1	P0D3	PLLR7
AR	IRQSIO	P0DBIO2	PLLR8
AR0	LCDD0	P0DBIO3	PLLR9
AR1	LCDD1	P1A0	PLLRFCK0
AR2	LCDD10	P1A1	PLLRFCK1
AR_EPA0	LCDD11	P1A2	PLLRFCK2
AR_EPA1	LCDD12	P1A3	PLLRFCK3
BANK	LCDD13	P1APLD0	PLLUL
BCD	LCDD14	P1APLD1	PSW
BEEP0CK0	LCDD2	P1APLD2	SIOCK0
BEEP0CK1	LCDD3	P1APLD3	SIOCK1
BTM0CY	LCDD4	P1B0	SIOCK2
BTM1CK	LCDD5	P1B1	SIOCK3
CE	LCDD6	P1B2	SIOHIZ
CMP	LCDD7	P1B3	SIOSEL
CY	LCDD8	P1C0	SIOSFR
DBF	LCDD9	PLLMD0	SIOTS
DBF0	LCDEN	PLLMD1	SP
DBF1	P0A0	PLLMD2	SYSCK
DBF2	P0A1	PLLMD3	Z
DBF3	P0A2	PLLPUT	ZZZ0
IEG	P0A3	PLLR1	ZZZ1
IFC	P0B0	PLLR10	ZZZ2
IFCCK0	P0B1	PLLR11	ZZZ3
IFCCK1	P0B2	PLLR12	ZZZ4

ZZZ5
ZZZ6
ZZZ7
ZZZ8
ZZZ9
ZZZDEVID
ZZZEPA
ZZZLSARG
ZZZPRINT
ZZZSKIP
ZZZSYDOC
ZZZALBMAC
ZZZALMAC
ZZZARGC
ZZZLINE

[MEMO]

CHAPTER 4 LOAD MODULE FILE FORMAT

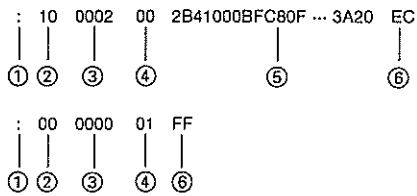
HEX-format load module files output by the assembler (AS17K) have two types of output file formats: ICE files and PRO files.

These two types of files must be used according to the target application. Besides having a user program area, they also have an assembly environment data area, an in-circuit emulator operating environment data area, and other areas.

(1) HEX-format load module file format

The data contained in HEX-format load module files output by the assembler is output in the following format.

[Example of HEX-format load module file format]



① Record mark

This indicates the start of a record.

② Code amount (2 digits)

This indicates the amount of code (byte data) stored in a record. This value is expressed as a hexadecimal number, with a maximum value of 10H (16 units). The value for the end record is 00H.

③ Address (4 digits)

This indicates the start address of the code shown in a record. The value for the end record is 0000H, and has no relation to the address.

④ Record type (2 digits)

A value of 00H indicates "data record" as the record type and a value of 01H indicates "end record."

⑤ Code (up to 32 digits (16 bytes))

Code is output to this field one byte at a time, up to 16 bytes.

⑥ Check sum (2 digits)

Data from fields ②, ③, ④, ⑤ and ⑥ is output to this field (with even parity) as byte data with an LSB value of 00H based on byte-unit sums.

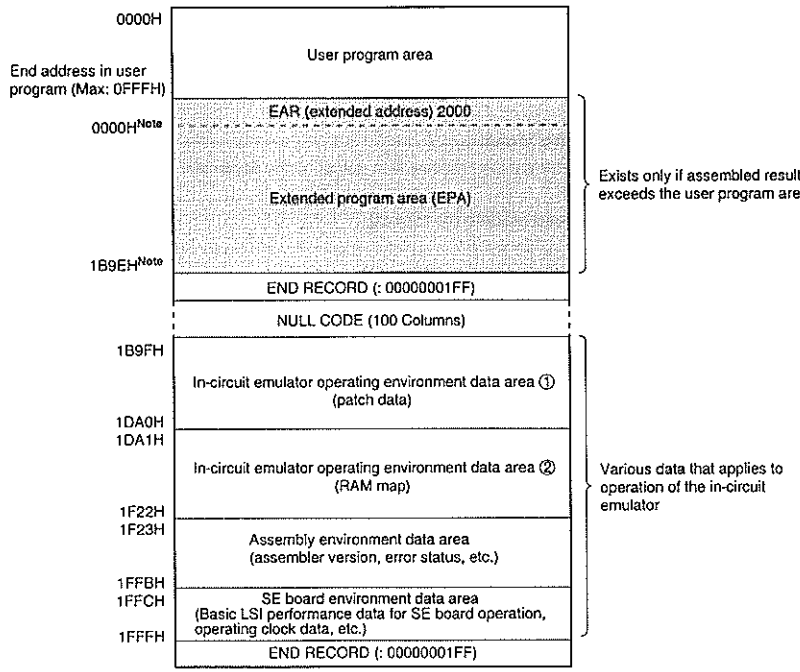
(2) ICE files

ICE files are output as HEX-format files exclusive to the in-circuit emulator (IE-17K, IE-17K-ET, or EMU-17K Note) output by the AS17K assembler. Figure 4-1 shows the output format assembled using the device files.

Note Manufactured by I.C Corp.

Figure 4-1. ICE File Format (1/2)

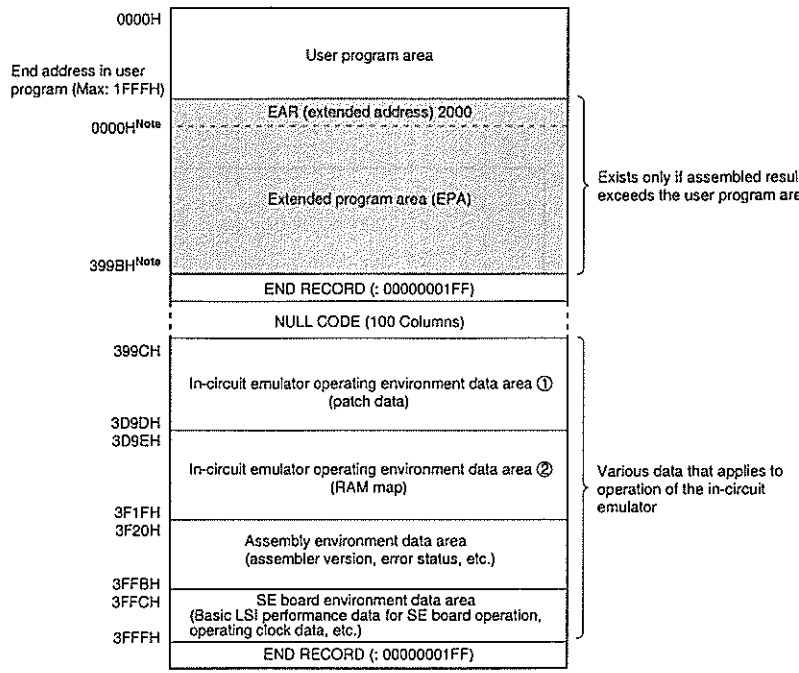
★ (a) μPD17071



Note Range for in-circuit emulator is 8000H to 9B9EH.

Figure 4-1. ICE File Format (2/2)

(b) μPD17072, 17073



Note Range for in-circuit emulator is 8000H to B99BH.

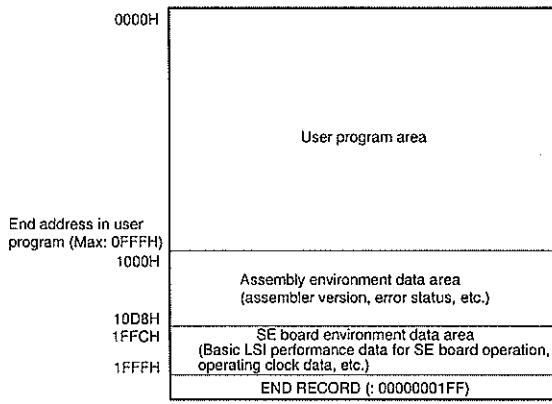
(3) PRO files

PRO files are output as HEX-format files exclusive to the PROM and single-write PROM products that are used for mask order and stand-alone SE board evaluations that are output by the AS17K assembler. These are output when "/PRO" is specified as an assembly option during assemble.

Figure 4-2 shows the output format assembled using the device files.

Figure 4-2. PRO File Format (1/2)

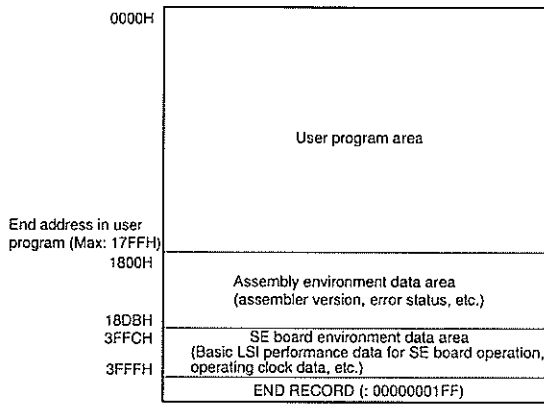
★ (a) μPD17071



Remark The range of 10D9H to 1FFBH does not exist in PRO files.

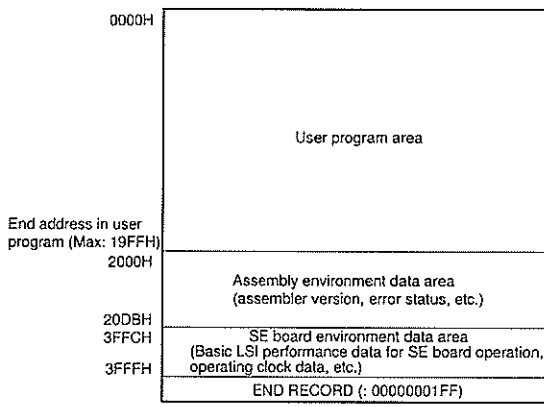
Figure 4-2. PRO File Format (2/2)

(b) μPD17072



Remark The range of 18DCH to 3FFBH does not exist in PRO files.

(c) μPD17073



Remark The range of 20DCH to 3FFBH does not exist in PRO files.

(4) File comparison of load module files

Even when there are no changes in the source file, changes may occur in the assembler results (i.e., the assembly environment data area). This is because the data in the assembly environment data area includes items such as the source file creation date.

Table 4-1. Items in Assembly Environment Data Area Which Are Subject to Change even when Source File Does not Change (1/3)

★ **(a) μPD17071**

Item	Address	
	ICE file	PRO file
Program name Note 1 (character string of up to 64 bytes, specified by assembly option /' PROG='.)	1F23H - 1F62H	1000H - 103FH
SIMPLEHOST data	1FADH	108AH
Error or warning status	1FB0H	108DH
Source file creation date (YY/MM/DD) and time Note 2	1FBEH - 1FC7H	109BH - 10A4H
Device name	1FC8H - 1FD7H	10A5H - 10B4H
Device file version	1FDCH, 1FDDH	10B9H, 10BAH
Assembler version	1FDEH - 1FE1H	10BBH - 10BEH

Notes 1. When using the RA17K (under development), the following 32 bytes are the program name area.
In ICE files : 1F23H to 1F42H
In PRO files: 1000H to 101FH
The RA17K uses the remaining 32 bytes as a system reserved area.

2. The most recent creation date/time data among the modules is written in source files or sequence files.

Caution Do not make changes to load module files only.
Change load files by changing the source file and then reassembling. Revising load files only may cause the histories of other files to become mismatched, resulting in bugs.

Table 4-1. Items in Assembly Environment Data Area Which Are Subject to Change even when Source File Does not Change (2/3)

(b) μPD17072

Item	Address	
	ICE file	PRO file
Program name [Note 1] (character string of up to 64 bytes, specified by assembly option /' PROG='.)	3F20H - 3F5FH	1800H - 183FH
SIMPLEHOST data	3FADH	188DH
Error or warning status	3FB0H	1890H
Source file creation date (YY/MM/DD) and time [Note 2]	3FBEH - 3FC7H	189EH - 18A7H
Device name	3FC8H - 3FD7H	18A8H - 18B7H
Device file version	3FDCH, 3FDDH	18BCH, 18BDH
Assembler version	3FDEH - 3FE1H	18BEH - 18C1H

Notes 1. When using the RA17K (under development), the following 32 bytes are the program name area.
In ICE files : 3F20H to 3F3FH
In PRO files: 1800H to 181FH
The RA17K uses the remaining 32 bytes as a system reserved area.

2. The most recent creation date/time data among the modules is written in source files or sequence files.

Caution Do not make changes to load module files only.
Change load files by changing the source file and then reassembling. Revising load files only may cause the histories of other files to become mismatched, resulting in bugs.

Table 4-1. Items in Assembly Environment Data Area Which Are Subject to Change even when Source File Does not Change (3/3)

(c) μPD17073

Item	Address	
	ICE file	PRO file
Program name [Note 1] (character string of up to 64 bytes, specified by assembly option /' PROG='.)	3F20H - 3F5FH	2000H - 203FH
SIMPLEHOST data	3FADH	208DH
Error or warning status	3FB0H	2090H
Source file creation date (YY/MM/DD) and time [Note 2]	3FBEH - 3FC7H	209EH - 20A7H
Device name	3FC8H - 3FD7H	20A8H - 20B7H
Device file version	3FDCH, 3FDDH	20BCH, 20BDH
Assembler version	3FDEH - 3FE1H	20BEH - 20C1H

Notes 1. When using the RA17K (under development), the following 32 bytes are the program name area.
In ICE files : 3F20H to 3F3FH
In PRO files: 2000H to 201FH
The RA17K uses the remaining 32 bytes as a system reserved area.

2. The most recent creation date/time data among the modules is written in source files or sequence files.

Caution Do not make changes to load module files only.
Change load files by changing the source file and then reassembling. Revising load files only may cause the histories of other files to become mismatched, resulting in bugs.

NEC

Facsimile Message

Although NEC has taken all possible steps to ensure that the documentation supplied to our customers is complete, bug free and up-to-date, we readily accept that errors may occur. Despite all the care and precautions we've taken, you may encounter problems in the documentation. Please complete this form whenever you'd like to report errors or suggest improvements to us.

From:

Name

Company

Tel. FAX

Address

Thank you for your kind support.

North America
NEC Electronics Inc.
Corporate Communications Dept.
Fax: 1-800-729-9288

Hong Kong, Philippines, Oceania
NEC Electronics Hong Kong Ltd.
Fax: +852-2886-9022/9044

Asian Nations except Philippines
NEC Electronics Singapore Pte. Ltd.
Fax: +65-250-3583

Europe
NEC Electronics (Europe) GmbH
Technical Documentation Dept.
Fax: +49-211-6503-274

Korea
NEC Electronics Hong Kong Ltd.
Seoul Branch
Fax: 02-551-0451

Japan
NEC Corporation
Semiconductor Solution Engineering Division
Technical Information Support Dept.
Fax: 044-548-7900

South America
NEC do Brasil S.A.
Fax: +55-11-889-1689

Taiwan
NEC Electronics Taiwan Ltd.
Fax: 02-719-5951

I would like to report the following error/make the following suggestion:

Document title: _____

Document number: _____ Page number: _____

If possible, please fax the referenced page or drawing.

Document Rating	Excellent	Good	Acceptable	Poor
Clarity	❑	❑	❑	❑
Technical Accuracy	❑	❑	❑	❑
Organization	❑	❑	❑	❑