

RZ/N2H Group

Encoder I/F FA-CODER sample program

Summary

This document describes the RZ/N2H Encoder I/F FA-CODER® sample program package.

For FA-CODER® communication protocol specifications and encoder specifications, contact Tamagawa Seiki Co., Ltd.

Functionality Checked Device

RZ/N2H Evaluation Board (RTK9RZN2Hxxxxxxx)

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1. Package Contents

This package contains the following contents.

The RZ/N2H FA-CODER interface supports up to 11 axes, but the sample program supports only 1 axis of them. If you use with 2 axes or more simultaneously, modify the sample program to support required axes.

1.1 Software

- Source code

No.	Name	Version number
1	RZ/N2H FA-CODER sample program (CR52 ver. *)	4.0
2	RZ/N2H FA-CODER sample program (CA55 ver. *)	4.0

Note: This sample program has a CR52 version that runs on the CPU core Cortex-R52 and a CA55 version that runs on the CPU core Cortex-A55. CR52 ver. and CA55 ver. are descriptions of the respective version.

1.2 Documents

No.	Document name	Version	File name
1	RZ/N2H Group Encoder I/F FA-CODER Sample Program Release Note	4.00	(j) r11an0928jj0400-rzn2h.pdf (e) r11an0928ej0400-rzn2h.pdf (this document)
2	RZ/N2H Group FA-CODER Sample Program Application Note	4.00	(j) r11an0927jj0400-rzn2h-fa-coder.pdf (e) r11an0927ej0400-rzn2h-fa-coder.pdf

2. File Structure

The file structure and contents of this package are detailed below.

Top

```

├─ r11an0928jj0400-rzn2h.pdf
├─ r11an0928ej0400-rzn2h.pdf
└─ workspace
    ├─ Software
    │   ├─ iccarm
    │   │   ├─ RZ_N2H_CR52_fac.zip      : RZ/N2H FA-CODER sample program set
    │   │   │                               CR52 ver. (IAR)
    │   │   └─ RZ_N2H_CA55_fac.zip      : RZ/N2H FA-CODER sample program set
    │   │   │                               CA55 ver. (IAR)
    │   └─ gcc
    │       ├─ RZ_N2H_CR52_fac.zip      : RZ/N2H FA-CODER sample program set
    │       │                               CR52 ver. (e2 studio)
    │       └─ RZ_N2H_CA55_fac.zip      : RZ/N2H FA-CODER sample program set
    │       │                               CA55 ver. (e2 studio)
    └─ Documents
        ├─ r11an0927jj0400-rzn2h-fa-coder.pdf
        └─ r11an0927ej0400-rzn2h-fa-coder.pdf

```

The file structure of the RZ_N2H_CR52_fac.zip and RZ_N2H_CA55_fac.zip are shown below.

Top folder

```

├─ configuration.xml      : FSP Configuration data
├─ ( Environment File Depending on Build Tool )
└─ src
    ├─ hal_entry.c        : FA-CODER sample program
    ├─ fac_main.c         : FA-CODER sample program
    ├─ siochar.c          : SCI_UART sample program
    ├─ syscalls.c         : SCI_UART sample program
    ├─ sio_char.h         : SCI_UART sample program
    └─ drv
        └─ fac
            ├─ iodefne_fac.h      : FAC register definition file
            ├─ r_fac_rzt2.c       : FAC driver file
            ├─ r_fac_rzt2_config.h : FAC driver file
            ├─ r_fac_rzt2_dat.h   : FAC driver file
            ├─ r_fac_rzt2_if.h    : FAC driver file
            ├─ r_scie.c          : FAC driver file
            └─ r_scie.h          : FAC driver file

```

3. About FA-CODER Sample Program

This section contains information necessary to use the complete set of FA-CODER sample programs.

3.1 Software Information

3.1.1 Base OS

This sample program is OS-independent.

3.1.2 Memory Size

Memory size used by this sample program and FA-CODER driver is shown in following table. This table does not include memory size used by Flexible Software Package or C language libraries of the compiler, but for the DMAC driver portion which is used for the FA-CODER encoder interface.

(1) CR52 ver.

Items		Memory Size	
		EWARM [kBytes]	e ² studio [kBytes]
FA-CODER driver	Code	7.6	7.0
	Data (with initial value)	0.0	0.0
	Data (without initial value)	2.7	2.7
	Constant Data	0.7	0.7
DMAC driver for encoder interface *	Code	2.8	2.0
	Data (with initial value)	0.0	0.0
	Data (without initial value)	0.2	0.2
	Constant Data	0.0	0.0
Sample program	Code	4.3	4.9
	Data (with initial value)	0.0	0.0
	Data (without initial value)	0.5	0.5
	Constant Data	2.2	2.2

Note: The DMAC driver is used for the FA-CODER interface. It is called from inside of the FA-CODER driver. The function using DMAC driver is enabled only in the CR52 version.

(2) CA55 ver.

Items		Memory Size	
		EWARM [kBytes]	e ² studio [kBytes]
FA-CODER driver	Code	11.8	10.0
	Data (with initial value)	0.0	0.0
	Data (without initial value)	3.3	3.4
	Constant Data	1.1	1.4
Sample program	Code	6.9	8.8
	Data (with initial value)	0.1	0.0
	Data (without initial value)	0.5	0.6
	Constant Data	2.4	3.0

3.2 Hardware Information

3.2.1 Device

RZ/N2H

3.2.2 Target Board

(1) Board Name

RZ/N2H Evaluation Board (RTK9RZN2Hxxxxxxxx)

(2) Setting of Target Board

The target board configuration is as follows.

DSW2-6: OFF

DSW5-1: OFF, DSW5-2: OFF, DSW5-3: OFF, DSW5-7: OFF, DSW5-8: OFF

DSW7-3: OFF, DSW7-4: ON

DSW12-5: ON, DSW12-6: OFF, DSW12-7: ON, DSW12-8: OFF

DSW13-1: OFF, DSW13-2: ON, DSW13-3: OFF, DSW13-4: ON

DSW18-5: OFF, DSW18-6: ON

DSW20-1: OFF, DSW20-3: OFF, DSW20-5: OFF

DSW21-2: OFF, DSW21-3: ON, DSW21-4: OFF, DSW21-5: ON, DSW21-6: OFF

DSW3-1: ON, DSW3-2: OFF, DSW3-3: ON, DSW3-6: OFF (Set to xSPI1 boot mode)

JP8: Short between 2-3 pins (Set VDD1833_2 to 3.3 V)

JP9: Short between 2-3 pins (Set VDD1833_3 to 3.3 V)

JP23: Short between 1-2 pins, Open between 3-4 pins, and between 5-6 pins (Set VDD1833_6 to 3.3 V)

(3) Used Pins of the Target Board

The correspondence between the pin used as the encoder I/F and the pin header of the target board is as follows. Channel FACODER8 is not available.

Channel	Pin Name	Pin Header	Input/Output	Voltage Domain	Description
FACODER0	RXDE00	CN44 #9	input	VDD33	Data reception pin
	TXDE00	CN44 #7	output	VDD33	Request output pin
	DEE00	CN44 #5	output	VDD33	Drive/receive control pin
FACODER1	RXDE01	CN44 #8	input	VDD33	Data reception pin
	TXDE01	CN44 #6	output	VDD33	Request output pin
	DEE01	CN44 #4	output	VDD1833_5	Drive/receive control pin
FACODER2	RXDE02	CN43 #23	input	VDD33	Data reception pin
	TXDE02	CN43 #21	output	VDD33	Request output pin
	DEE02	CN43 #27	output	VDD33	Drive/receive control pin
FACODER3	RXDE03	CN43 #24	input	VDD1833_6	Data reception pin
	TXDE03	CN43 #22	output	VDD1833_6	Request output pin
	DEE03	CN43 #18	output	VDD1833_6	Drive/receive control pin
FACODER4	RXDE04	CN44 #27	input	VDD33	Data reception pin
	TXDE04	CN44 #25	output	VDD33	Request output pin
	DEE04	CN44 #23	output	VDD33	Drive/receive control pin

Channel	Pin Name	Pin Header	Input/Output	Voltage Domain	Description
FACODER5	RXDE05	CN43 #14	input	VDD1833_6	Data reception pin
	TXDE05	CN43 #12	output	VDD1833_6	Request output pin
	DEE05	CN43 #10	output	VDD1833_6	Drive/receive control pin
FACODER6	RXDE06	CN42 #18	input	VDD1833_3	Data reception pin
	TXDE06	CN42 #16	output	VDD1833_3	Request output pin
	DEE06	CN42 #14	output	VDD1833_3	Drive/receive control pin
FACODER7	RXDE07	CN42 #36	input	VDD1833_3	Data reception pin
	TXDE07	CN42 #34	output	VDD1833_3	Request output pin
	DEE07	CN42 #24	output	VDD1833_3	Drive/receive control pin
FACODER8	RXDE08	-	-	-	N.A.
	TXDE08	-	-	-	N.A.
	DEE08	-	-	-	N.A.
FACODER9	RXDE09	CN51 #18	input	VDD1833_2	Data reception pin
	TXDE09	CN51 #16	output	VDD1833_2	Request output pin
	DEE09	CN51 #14	output	VDD1833_2	Drive/receive control pin
FACODER10	RXDE10	CN51 #27	input	VDD1833_2	Data reception pin
	TXDE10	CN51 #25	output	VDD1833_2	Request output pin
	DEE10	CN51 #23	output	VDD1833_2	Drive/receive control pin
FACODER11	RXDE11	CN51 #26	input	VDD1833_2	Data reception pin
	TXDE11	CN51 #24	output	VDD1833_2	Request output pin
	DEE11	CN51 #22	output	VDD1833_2	Drive/receive control pin

3.3 Procedures on Development Environments: CR52 ver.

3.3.1 Preparation before Executing the Sample Program

This sample program communicates with a PC. The USB connection terminal on the target board is CN27. Select higher-numbered port from COM ports that appear at connecting the board with the host PC.

The terminal software of the host PC is set as shown in the following table.

Function	Setting
Communication method	Asynchronous serial transmission/reception
Sending / receiving order	LSB first
Transfer rate	19200 bps
Character length	8 bits
Stop bit length	1 bit
Parity function	None
Hardware flow control	None

3.3.2 EWARM from IAR Systems

(1) Build Environment

IAR Embedded Workbench for Arm (EWARM)

Version 9.60.3 + patch (EWARM_Patch_for_RZT2H_N2H_rev1.0)

RENESAS FSP Smart Configurator (FSP SC) 2025-12

RENESAS Flexible Software Package (FSP) for RZ v4.0.0

(2) Execution Environment ICE

IAR I-jet

(3) Build Procedure for Sample Programs

The build procedure for the sample program is as follows.

- 1 Extract RZ_N2H_CR52_fac.zip and copy the extracted source files to the desired location.
- 2 Activate EWARM.
- 3 Select [File] menu -> [Open Workspace].
- 4 Open the extracted source file RZ_N2H_fac.eww.
- 5 Start the FSP Smart Configurator from the [Tools] menu of the EWARM IDE. *

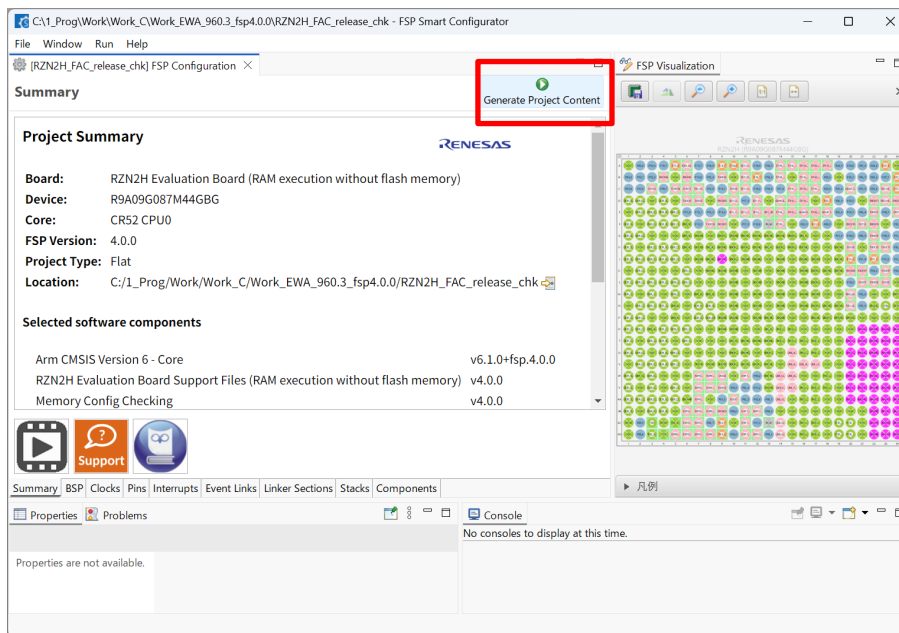
Note: The following procedure adds the activation of the FSP Smart Configurator to the [Tools] menu of the EWARM IDE. Select [Tools] menu -> [Tool Configuration] in the EWARM IDE. Select the [New] button, specify a table string in each field, and press [OK].

Field	String
Menu text	FSP Smart Configurator
Command	\$RASC_EXE_PATH\$
Argument	--compiler IAR configuration.xml
Initial directory	\$PROJ_DIR\$

String for the command is variable holding the path of the Smart Configurator execution file, rasc.exe. If the path written as RASC_EXE_PATH in the buildinfo.ipcf file does not match with your rasc.exe installation path, please edit the buildinfo.ipcf to fit with your installation path.

You can also start the FSP Smart Configurator directly from the command prompt by specifying the folder where it is installed.

- 6 In the FSP Configuration pane of the Smart Configurator, click Generate Project Content. The rz_cfg, rz_gen, script and .setting folders will be generated.



- 7 When project generation is complete, close the Smart Configurator.
 8 Select [Rebuild All] from the [Project] menu of EWARM.
 The file Debug\Exe\RZ_N2H_fac.out is generated.

(4) Sample Program Execution Procedure

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

- 1 Select [Project] menu -> [Download and Debug].
- 2 Select [Debug] menu -> [Execute].

(5) Execution Result of the Sample Program

Run the sample program and enter commands in the terminal software window. For commands, see 4.11.7 console commands in the RZ/N2H Group FA-CODER Sample Program Application Note.

```

COM5 - Tera Term VT
ファイル(F) 編集(E) 設定(S) コントロール(O) ウィンドウ(W) ヘルプ(H)
Tama sample program start
R_FAC_GetVersion = 4.0

tamagawa>single
single command
result:success
single turn data:      8388591
request id:           0H
parity bit(request id): 0H
information code:     0H
encoder alarm:        2H
communication alarm:  0H
cro data:             4DH
tamagawa>
  
```

3.3.3 e² studio from RENESAS

(1) Build Environment

RENESAS e² studio 2025-12

Toolchain version: GNU Arm Embedded 13.3.1.arm-13-24

RENESAS Flexible Software Package (FSP) for RZ v4.0.0

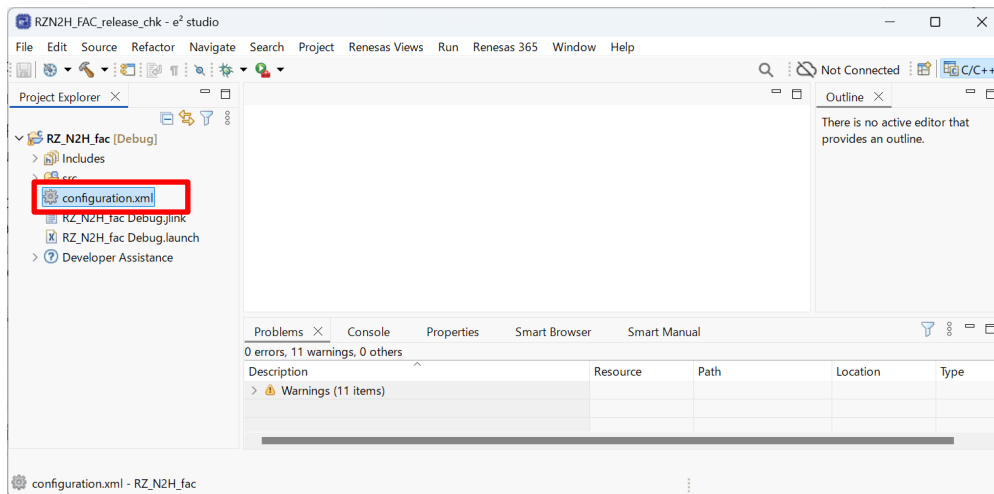
(2) Execution Environment ICE

SEGGER J-Link™ v8.60

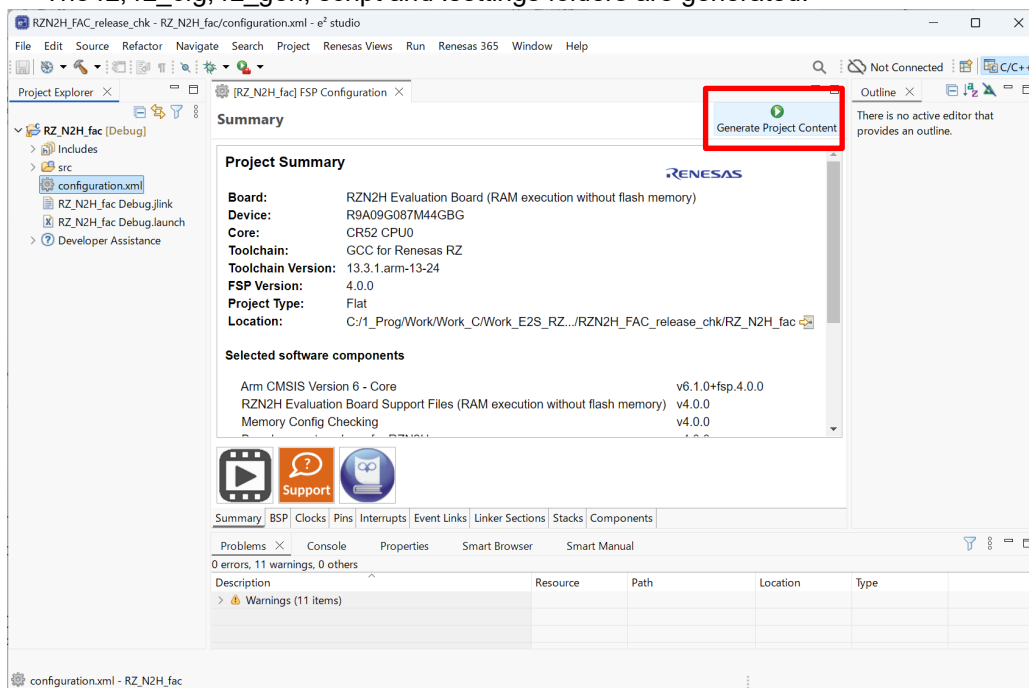
(3) Build Procedure of the Sample Program

The procedure for building the sample program is as follows.

- 1 Extract RZ_N2H_CR52_fac.zip and copy the extracted source files to the desired location.
- 2 After launching e² studio and moving to the workspace, click the [File] menu ->[Import] and select Existing project to workspace and click [Next].
- 3 On the project import screen, select the folder where the sample program was expanded as the root directory.
- 4 Select a project, check Copy Project to Workspace, and click [Finish].
- 5 Double-click the configuration.xml in the Project Explorer pane of e² studio to open it.



- 6 Click Generate Project Content in the FSP Configuration pane of e² studio.
The rz, rz_cfg, rz_gen, script and .settings folders are generated.



- 7 Select [Project] menu -> [Build All].
The file Debug\RZ_N2H_fac.elf is generated.

(4) Execution Procedure of the Sample Program

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

- 1 Select [Run] menu -> [Debug As] -> [Renesas GDB Hardware Debugging].
- 2 Click [Debug] to start downloading to internal RAM.
- 3 Click [Run] menu -> [Resume] to run the sample program.

(5) Execution Result of the Sample Program

Run the sample program and enter commands in the terminal software window. For commands, see 4.11.7 console commands in the RZ/N2H Group FA-CODER Sample Program Application Note.

```

COM5 - Tera Term VT
ファイル(F) 編集(E) 設定(S) コントロール(O) ウィンドウ(W) ヘルプ(H)
Tama sample program start
R_FAC_GetVersion = 4.0

tamagawa>single
single command
result:success
single turn data:      8388591
request id:           0H
parity bit(request id): 0H
information code:     0H
encoder alarm:        2H
communication alarm:  0H
crc data:             4DH
tamagawa>

```

3.4 Procedures on Development Environments: CA55 ver.

3.4.1 Preparation before Executing the Sample Program

This sample program communicates with a PC. The USB connection terminal on the target board is CN27. Select lower-numbered port from COM ports that appear at connecting the board with the host PC.

The terminal software of the host PC is set as shown in the following table.

Function	Setting
Communication method	Asynchronous serial transmission/reception
Sending / receiving order	LSB first
Transfer rate	19200 bps
Character length	8 bits
Stop bit length	1 bit
Parity function	None
Hardware flow control	None

3.4.2 EWARM from IAR Systems

(1) Build Environment

IAR Embedded Workbench for Arm (EWARM)

Version 9.60.3 + patch (EWARM_Patch_for_RZT2H_N2H_rev1.0)

RENESAS FSP Smart Configurator (FSP SC) 2025-12

RENESAS Flexible Software Package (FSP) for RZ v4.0.0

(2) Execution Environment ICE

IAR I-jet

(3) Build Procedure for Sample Programs

The build procedure for the sample program is as follows.

- 1 Extract RZ_N2H_CA55_fac.zip and copy the extracted source files to the desired location.
- 2 Activate EWARM.
- 3 Select [File] menu -> [Open Workspace].
- 4 Open the extracted source file RZ_N2H_CA55_0_fac.eww.
- 5 Start the FSP Smart Configurator from the [Tools] menu of the EWARM IDE. *

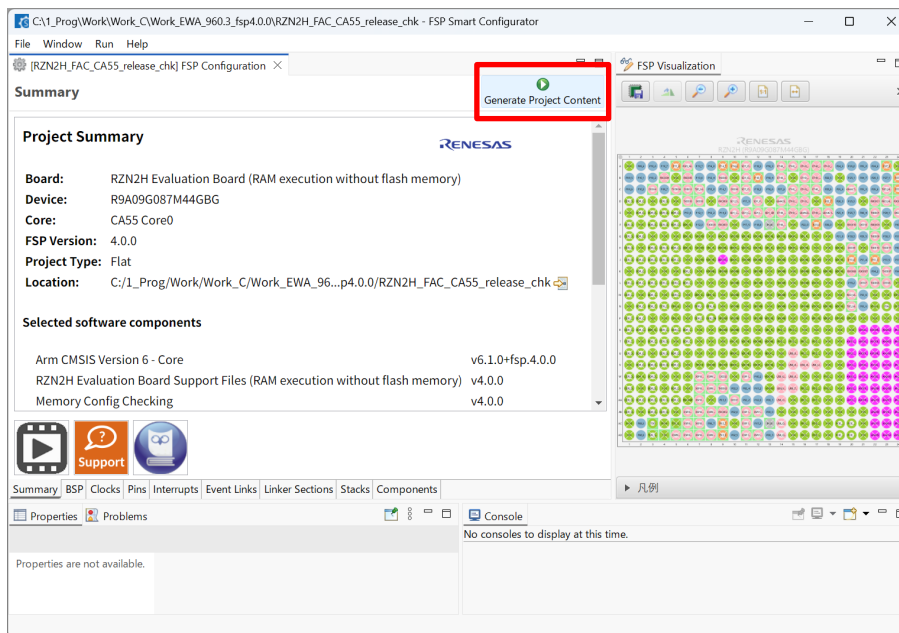
Note: The following procedure adds the activation of the FSP Smart Configurator to the [Tools] menu of the EWARM IDE. Select [Tools] menu -> [Tool Configuration] in the EWARM IDE. Select the [New] button, specify a table string in each field, and press [OK].

Field	String
Menu text	FSP Smart Configurator
Command	\$RASC_EXE_PATH\$
Argument	--compiler IAR configuration.xml
Initial directory	\$PROJ_DIR\$

String for the command is variable holding the path of the Smart Configurator execution file, rasc.exe. If the path written as RASC_EXE_PATH in the buildinfo.ipcf file does not match with your rasc.exe installation path, please edit the buildinfo.ipcf to fit with your installation path.

You can also start the FSP Smart Configurator directly from the command prompt by specifying the folder where it is installed.

- 6 In the FSP Configuration pane of the Smart Configurator, click Generate Project Content. The rz, rz_cfg, rz_gen, script and .setting folders will be generated.



- 7 When project generation is complete, close the Smart Configurator.
 8 Select [Rebuild ALL] from the [Project] menu of EWARM.
 The file Debug\Exe\RZ_N2H_CA55_0_fac.out is generated.

(4) Sample Program Execution Procedure

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

- 1 Select [Project] menu -> [Download and Debug].
- 2 Select [Debug] menu -> [Execute].

(5) Execution Result of the Sample Program

Run the sample program and enter commands in the terminal software window. For commands, see 4.11.7 console commands in the RZ/N2H Group FA-CODER Sample Program Application Note.

```

COM5 - Tera Term VT
ファイル(F) 編集(E) 設定(S) コントロール(O) ウィンドウ(W) ヘルプ(H)
Tama sample program start
R_FAC_GetVersion = 4.0

tamagawa>single
single command
result:success
single turn data:      8388591
request id:           0H
parity bit(request id): 0H
information code:     0H
encoder alarm:        2H
communication alarm:  0H
orc data:             4DH
tamagawa>
  
```

3.4.3 e² studio from RENESAS

(1) Build Environment

RENESAS e² studio 2025-12

Toolchain version: GCC Arm A-Profile (AArch64 bare-metal) 13.2.1.20231009

RENESAS Flexible Software Package (FSP) for RZ v4.0.0

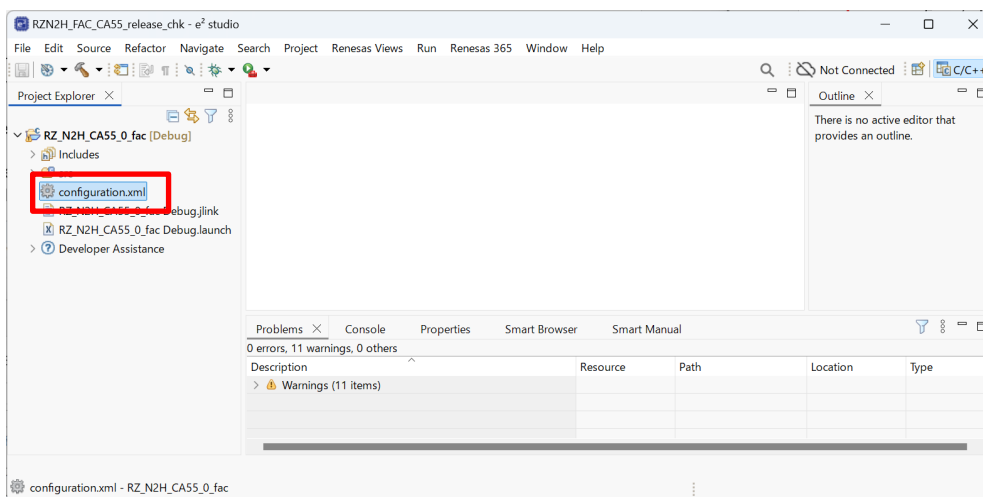
(2) Execution Environment ICE

SEGGER J-Link™ v8.60

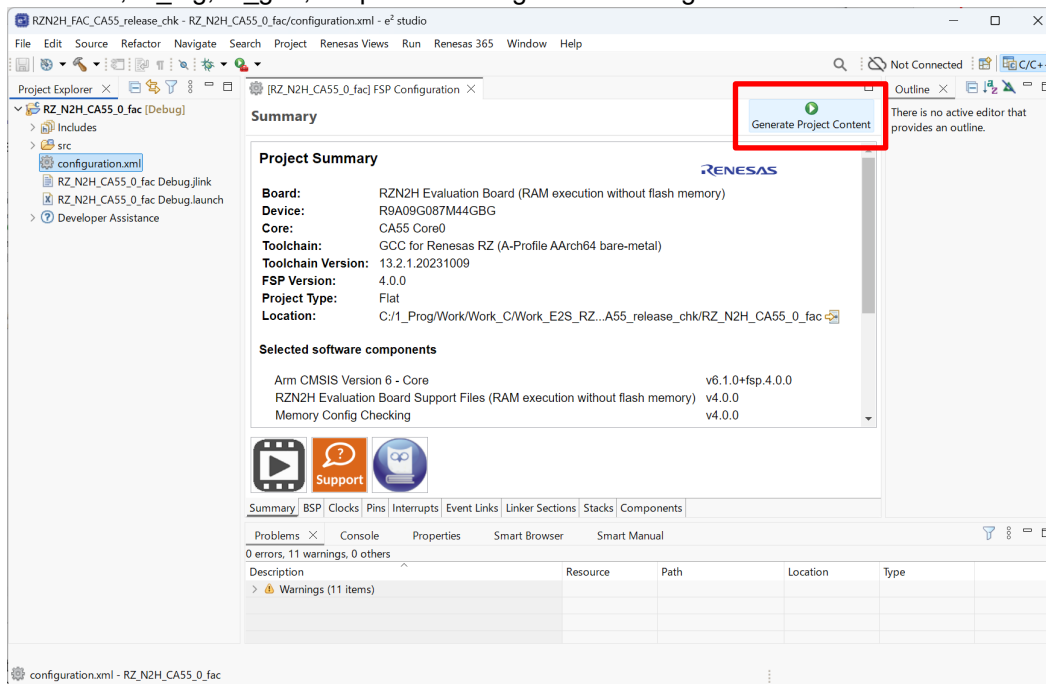
(3) Build Procedure of the Sample Program

The procedure for building the sample program is as follows.

- 1 Extract RZ_N2H_CA55_fac.zip and copy the extracted source files to the desired location.
- 2 After launching e² studio and moving to the workspace, click the [File] menu ->[Import] and select Existing project to workspace and click [Next].
- 3 On the project import screen, select the folder where the sample program was expanded as the root directory.
- 4 Select a project, check Copy Project to Workspace, and click [Finish].
- 5 Double-click the configuration.xml in the Project Explorer pane of e² studio to open it.



- 6 Click Generate Project Content in the FSP Configuration pane of e² studio.
The rz, rz_cfg, rz_gen, script and .settings folders are generated.



- 7 Select [Project] menu -> [Build All].
The Debug\RZ_N2H_CA55_0_fac.elf file will be generated.

(4) Execution Procedure of the Sample Program

After executing the "build procedure", connect the target board and debugger correctly, and perform the following operations.

- 1 Select [Run] menu -> [Debug As] -> [Renesas GDB Hardware Debugging].
- 2 Click [Debug] to start downloading to internal RAM.
- 3 Click [Run] menu -> [Resume] to run the sample program.

(5) Execution Result of the Sample Program

Run the sample program and enter commands in the terminal software window. For commands, see 4.11.7 console commands in the RZ/N2H Group FA-CODER Sample Program Application Note.

```

COM5 - Tera Term VT
ファイル(F) 編集(E) 設定(S) コントロール(O) ウィンドウ(W) ヘルプ(H)
Tama sample program start
R_FAC_GetVersion = 4.0

tamagawa>single
single command
result:success
single turn data:      8388591
request id:           0H
parity bit(request id): 0H
information code:     0H
encoder alarm:        2H
communication alarm:  0H
crc data:             4DH
tamagawa>

```

Revision History

Rev.	Date	Description	
		Page	Summary
2.00	Dec 23.24	-	First Edition issued
3.00	Nov 7.25	1	Update description of the trademarks.
		2, 3	Update revisions of the application note and the release note. Update sample program version to 3.0. (Use FIFO for communication buffer. Support FSP v3.0.0.)
		4	Update memory size information.
		7 to 14	Update build environment for FSP v3.0.0. Figures are replaced.
4.00	Apr 3.26	2, 3	Update revisions of the application note and the release note. Update sample program version to 4.0. (Support FSP v4.0.0.) Updated the file structure.
		4	Update memory size information.
		7 to 14	Update build environment for FSP v4.0.0. Figures are replaced.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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