RICBox GUI Software for VersaClock 7

This guide assists those using the Renesas IC Toolbox (RICBox) software to configure and control a VersaClock® 7 device. This includes (but is not limited to) the RC21012 and RC31012 devices.

Contents

1. Installation and Setup

Ensure that the latest version of the Renesas IC Toolbox software is installed. New versions are released frequently and can provide a better experience with new functionality. The Renesas IC Toolbox software can be located on the VersaClock 7 Evaluation Kit page.

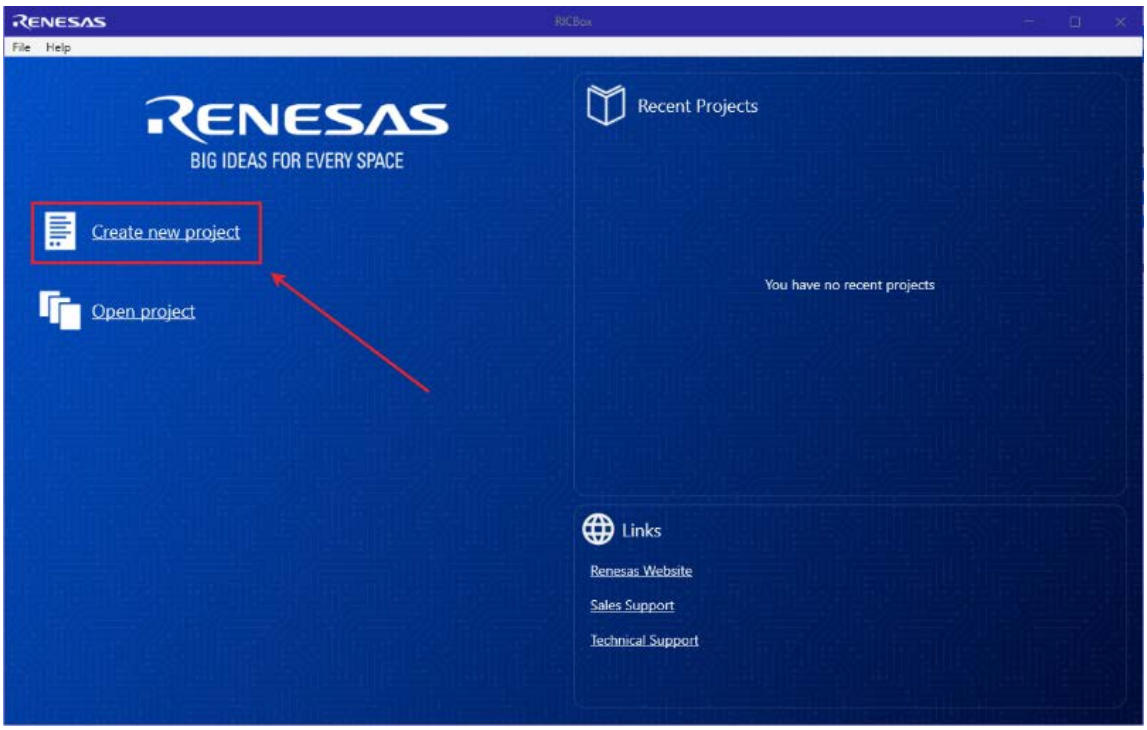
Each device that is compatible with the Renesas IC Toolbox software has its own individual installer. This is a convenient executable file that installs to a computer that already has the Renesas IC Toolbox software. The VersaClock 7 installer can be located on the VersaClock 7 Evaluation Kit page. Always check for newer versions as new features are frequently added.

Download the installer and follow the prompts before proceeding through this document.

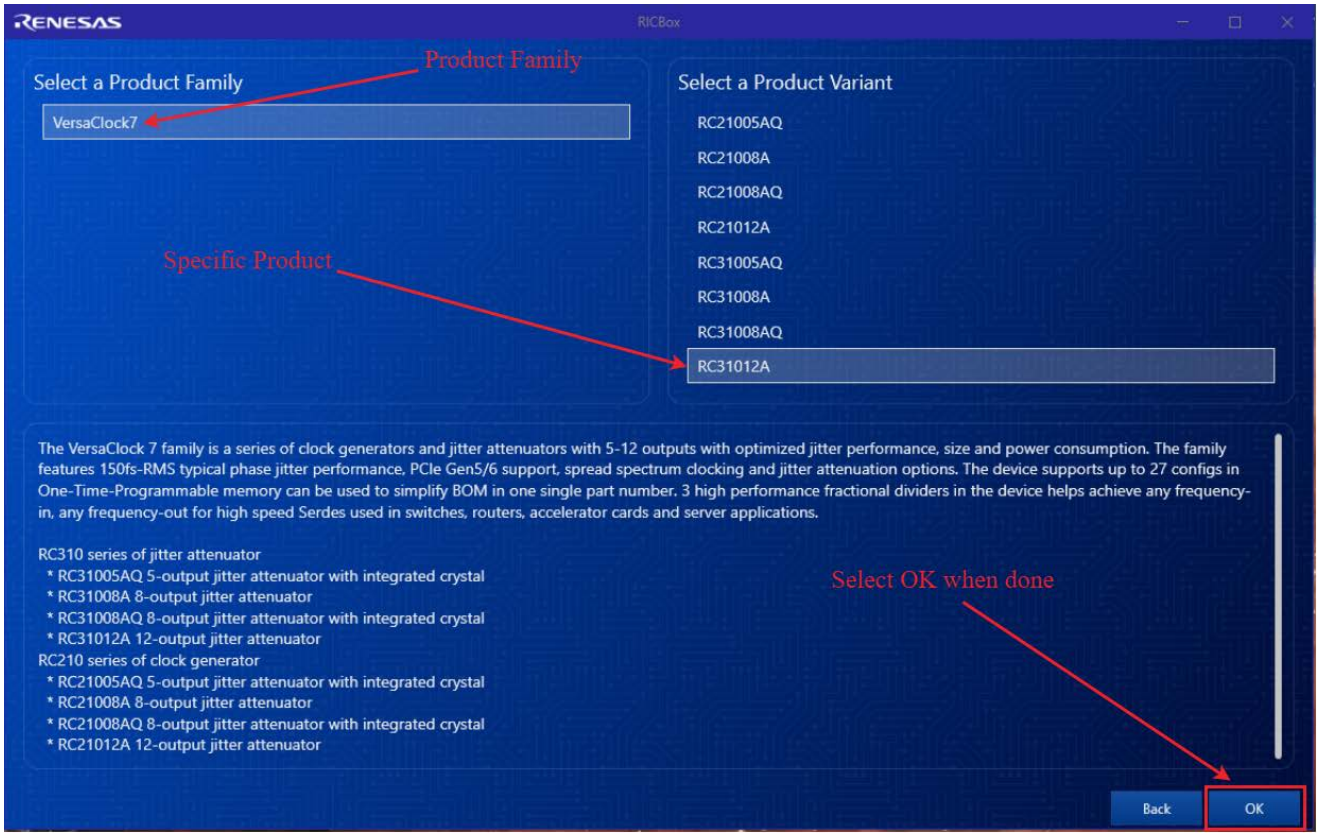
2. Loading and Creating Configurations

2.1 Creating a New Configuration

To create a new configuration, open the Renesas IC Toolbox software and click the *Create new project* button.



In the “Select Product Family” section, select VersaClock7. From the “Select Product” section, select the working device. Click the *OK* button to open up the new configuration. It may take a couple of minutes to open for the first time.

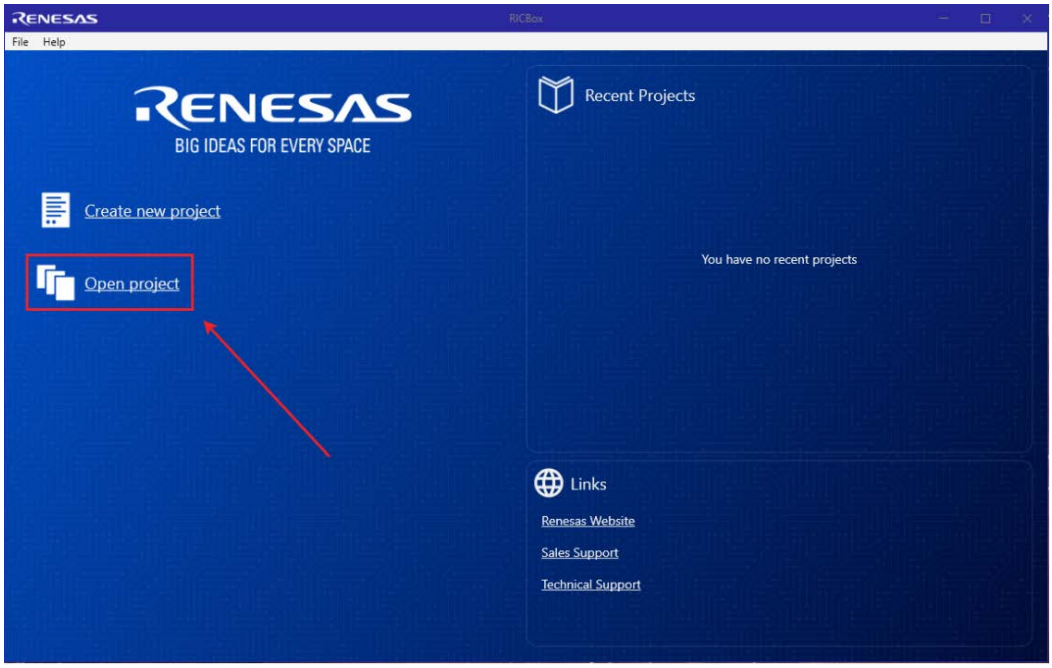


Note: Some variations between devices may show up in this guide. The intent of this guide is to encompass an overview of the entire device family.

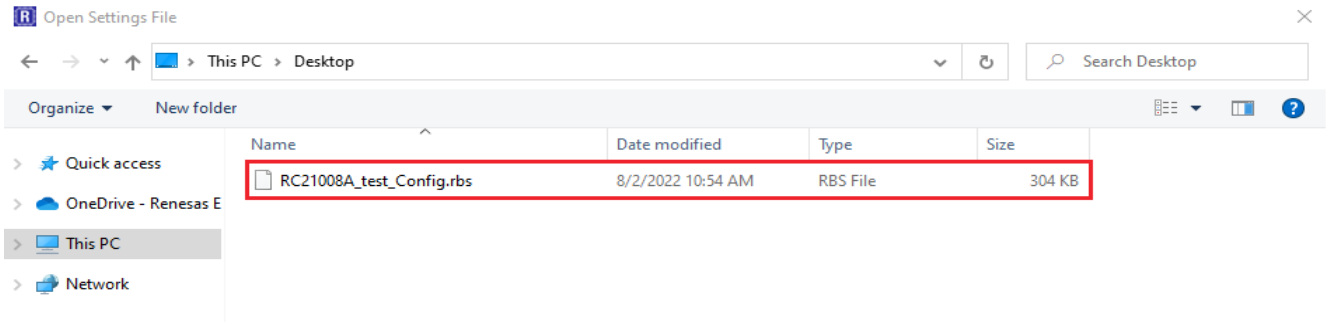
2.2 Loading a Settings File

Loading a settings file is similar to creating a new one. To load an existing settings file, click on the *Open project* button just after opening the Renesas IC Toolbox software. This will open a file browser.

Note: Recently used settings files are under the “Recent Projects” section.



Navigate to the directory that stores the settings file and select it. Renesas IC Toolbox settings files have the file type '.rbs'.

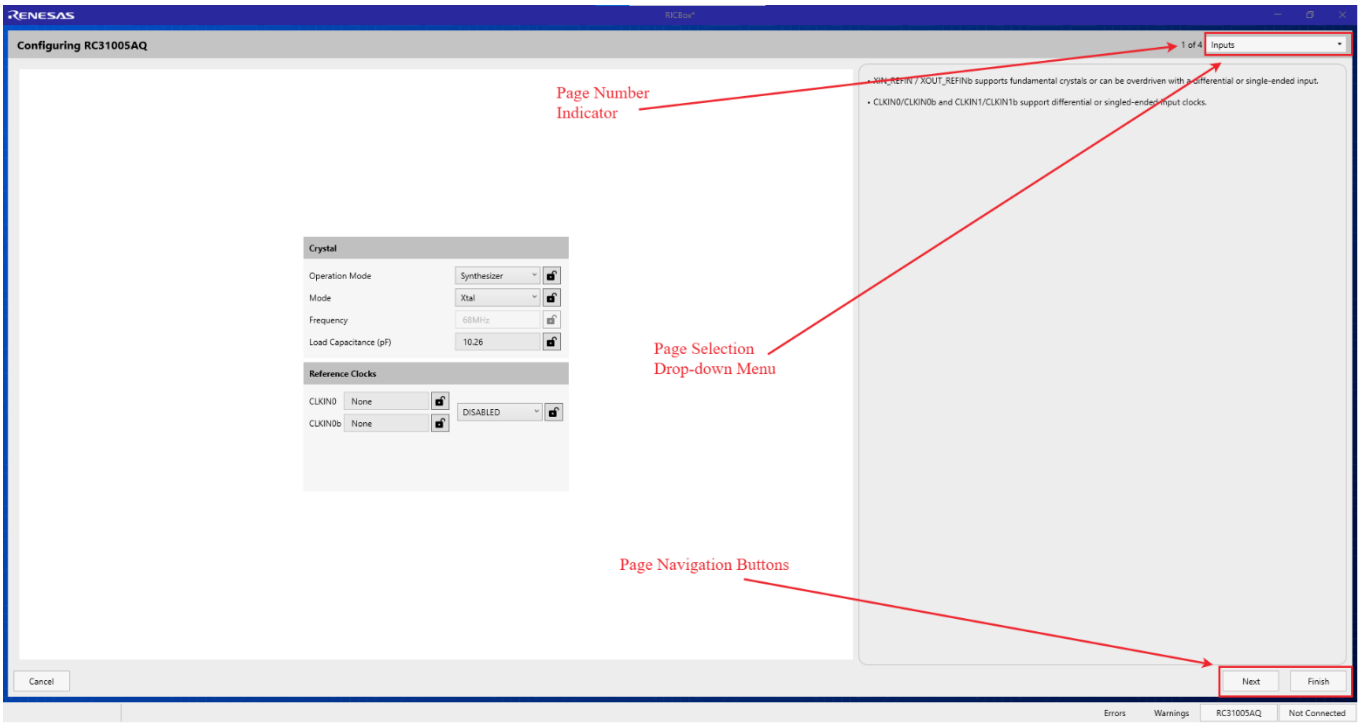


3. Wizard Setup

When creating a new configuration, the wizard page will be the first screen to appear. For VersaClock 7 devices, there are four separate wizard pages: **Inputs**, **DPLL**, **Spread Spectrum**, and **Outputs**. Each section pertains to a different portion of the device that needs to be configured for proper functionality.

Note: Some VersaClock 7 devices may not have a DPLL.

Navigation to individual sections can be performed by using the *Next* and *Previous* buttons in the lower right corner of the screen or the drop-down menu in the upper right. Select the *Finish* button to enter the control panel page.

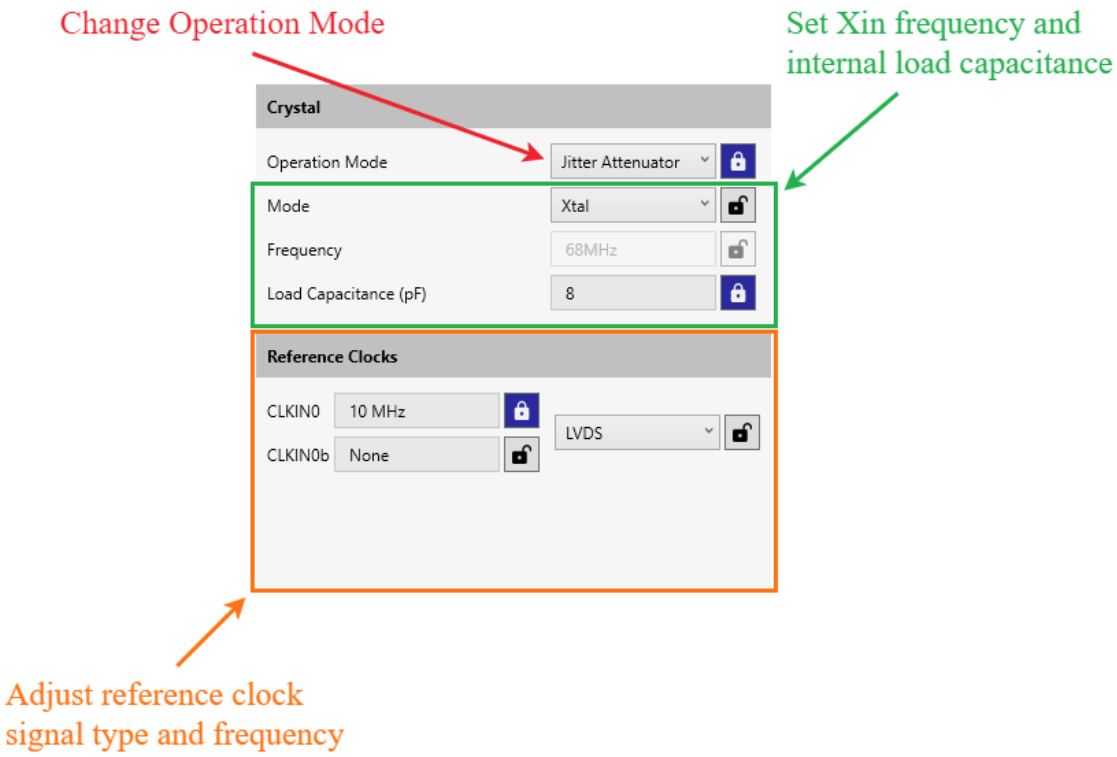


3.1 Inputs

There are two sections to make note of when configuring the inputs: **Crystal** and **Reference Clocks**. The Crystal section is used when creating a configuration that is either in synthesizer mode and uses a clock at the XIN pin, or in any Jitter Attenuator mode. The same applies for the CLKIN section. Device mode is through the "Operation Mode" dropdown menu. Device modes include **Synthesizer**, **Jitter Attenuator**, and **DCO**.

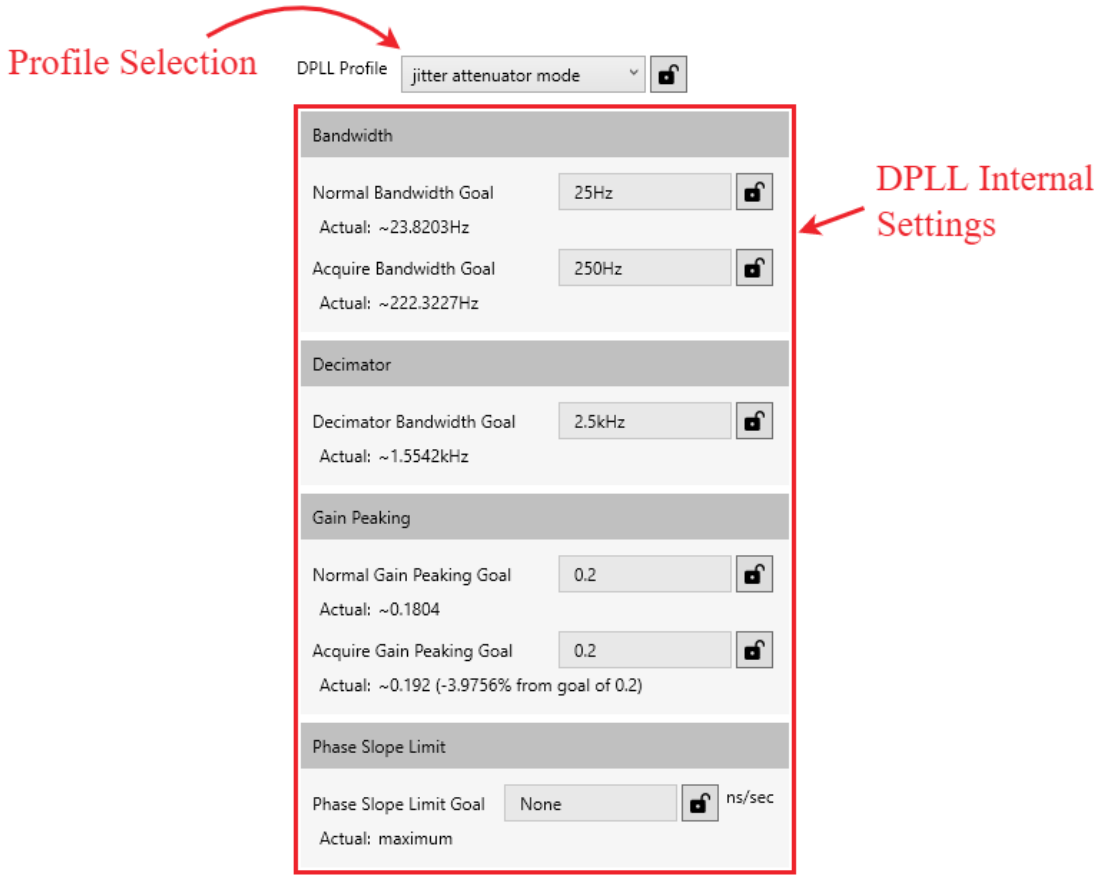
Descriptions of each mode can be found on the right side panel of the page.

Note: Some devices may not have both Jitter Attenuator and DCO modes together.



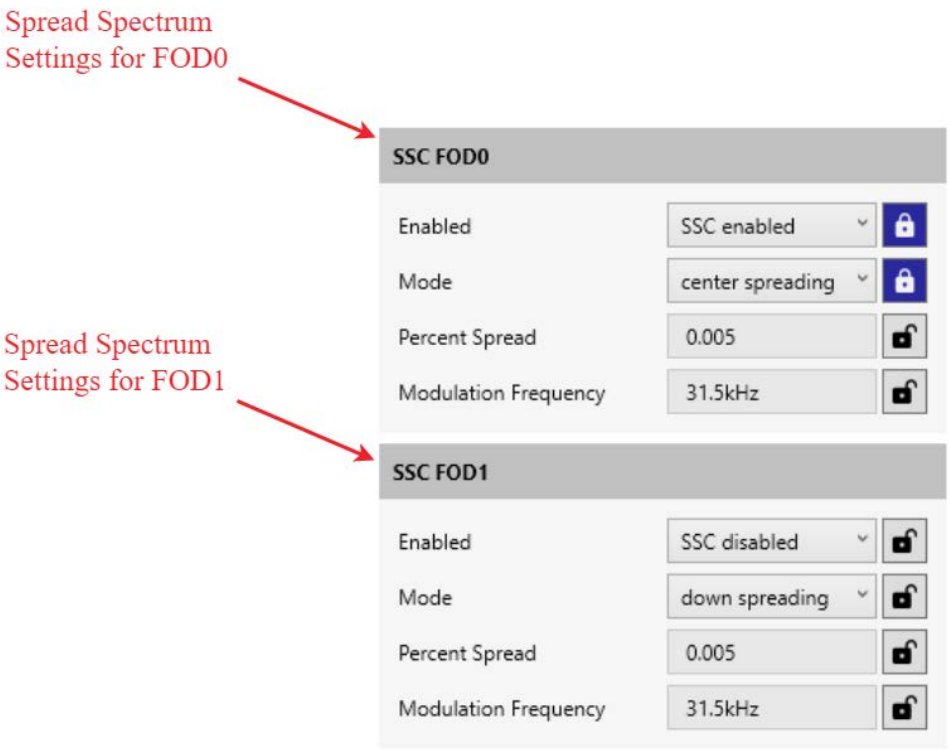
3.2 DPLL

If the device is configured for jitter attenuator mode, the DPLL section will become available. The DPLL section enables manual adjustment of the bandwidth, decimator, gain peaking, and phase slope limit values. Alternatively, there's the option to select a predefined SyncE profile that will automatically populate the adjustable settings. Descriptions of each section and the SyncE profiles are on the right of the page.



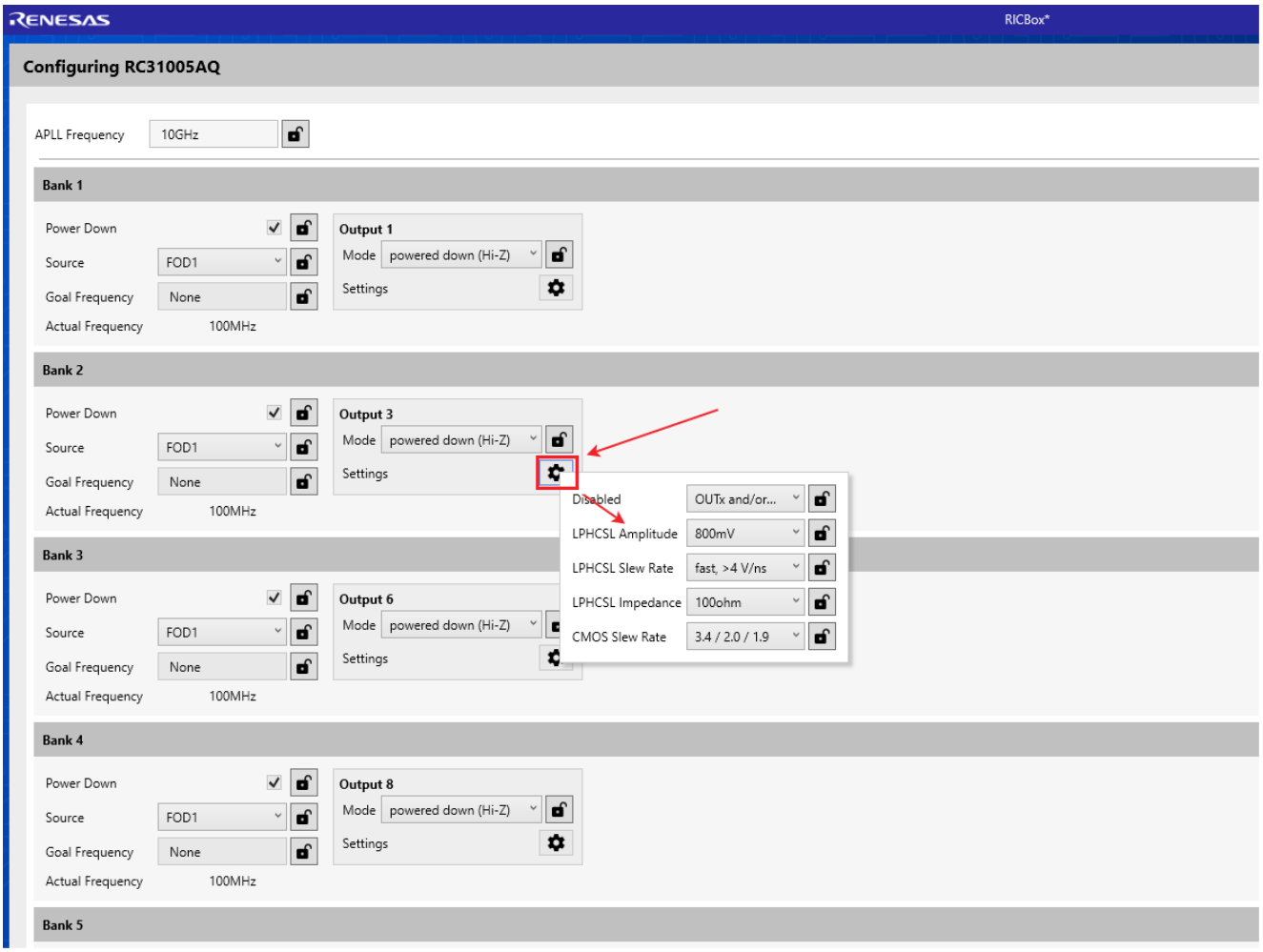
3.3 Spread Spectrum

The spread spectrum section enables spectrum spreading on either **FOD0** or **FOD1** or both. The mode for the spread spectrum engine can be set to down spreading or center spreading. The modulation frequency and the percent spread can also be configured in this section.



3.4 Outputs

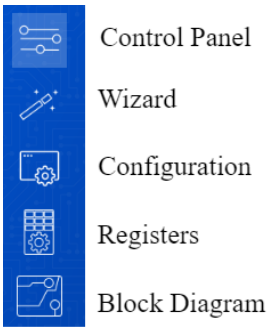
The outputs section enables setting the output frequencies and adjusting the overall VCO frequency. Outputs can be further configured by clicking on the symbol next to the output field. This gives the ability to enable/disable the output, select the output type, and adjust the signal settings.



4. Side Panel Buttons

The side panel consists of five separate buttons. Each button opens a separate page. Each page has a unique view, allowing the configuration of the device from different perspectives.

- *Control Panel* button opens the device overview page.
- *Wizard* button opens the initial wizard page.
- *Configuration* button displays the register settings in a readable text format with a search engine.
- *Registers* button shows a graphic of the registers in the device.
- *Block Diagram* button opens a configurable block diagram view.

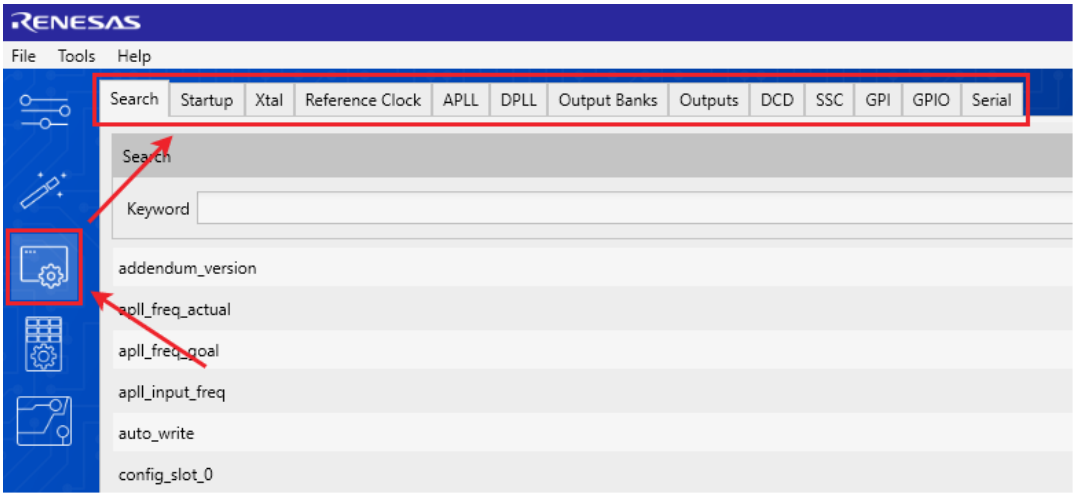


5. Control Panel View

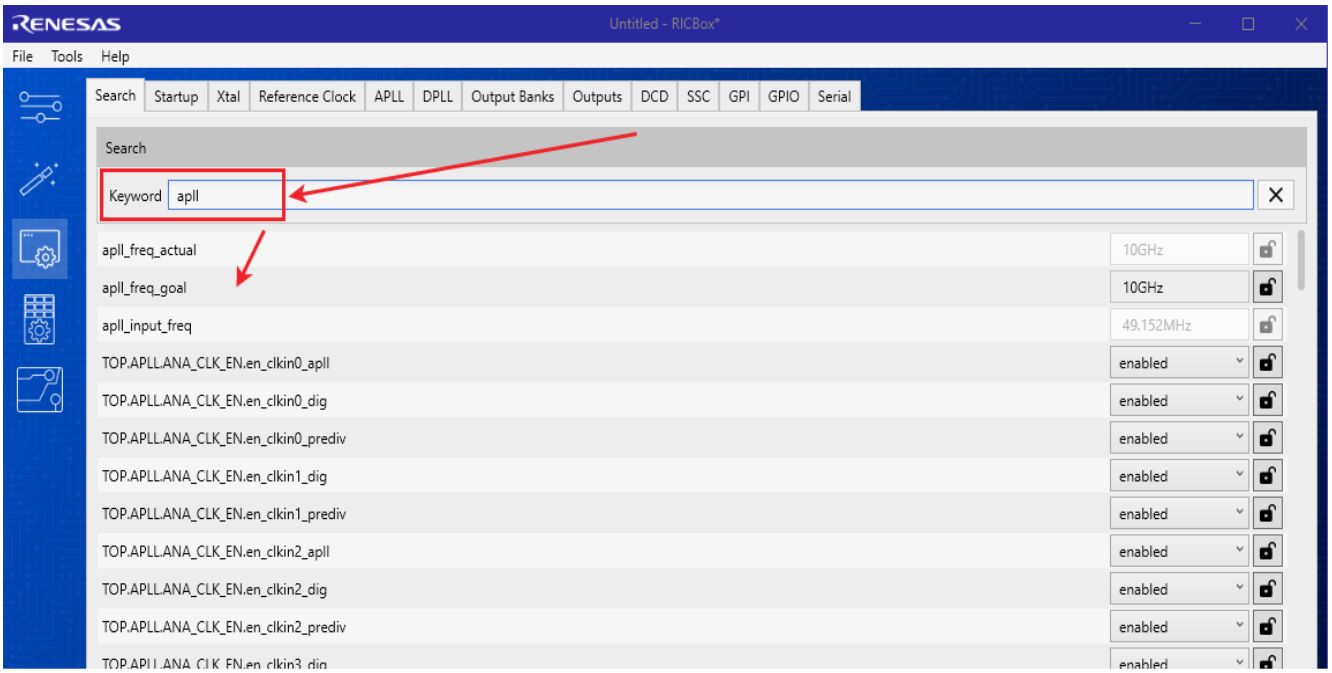
The control panel view displays an overview page depicting the major settings for the device. This page can be used as an important reference for the overall device configuration.

6. Configuration View

Configuration view enables easy movement through register settings via the tabs at the top of the page. Each section has all of the critical registers and data fields listed to configure the device block.



The search tab provides access to the configurable fields through a search bar. The search engine can be used to find any specific configurable field.

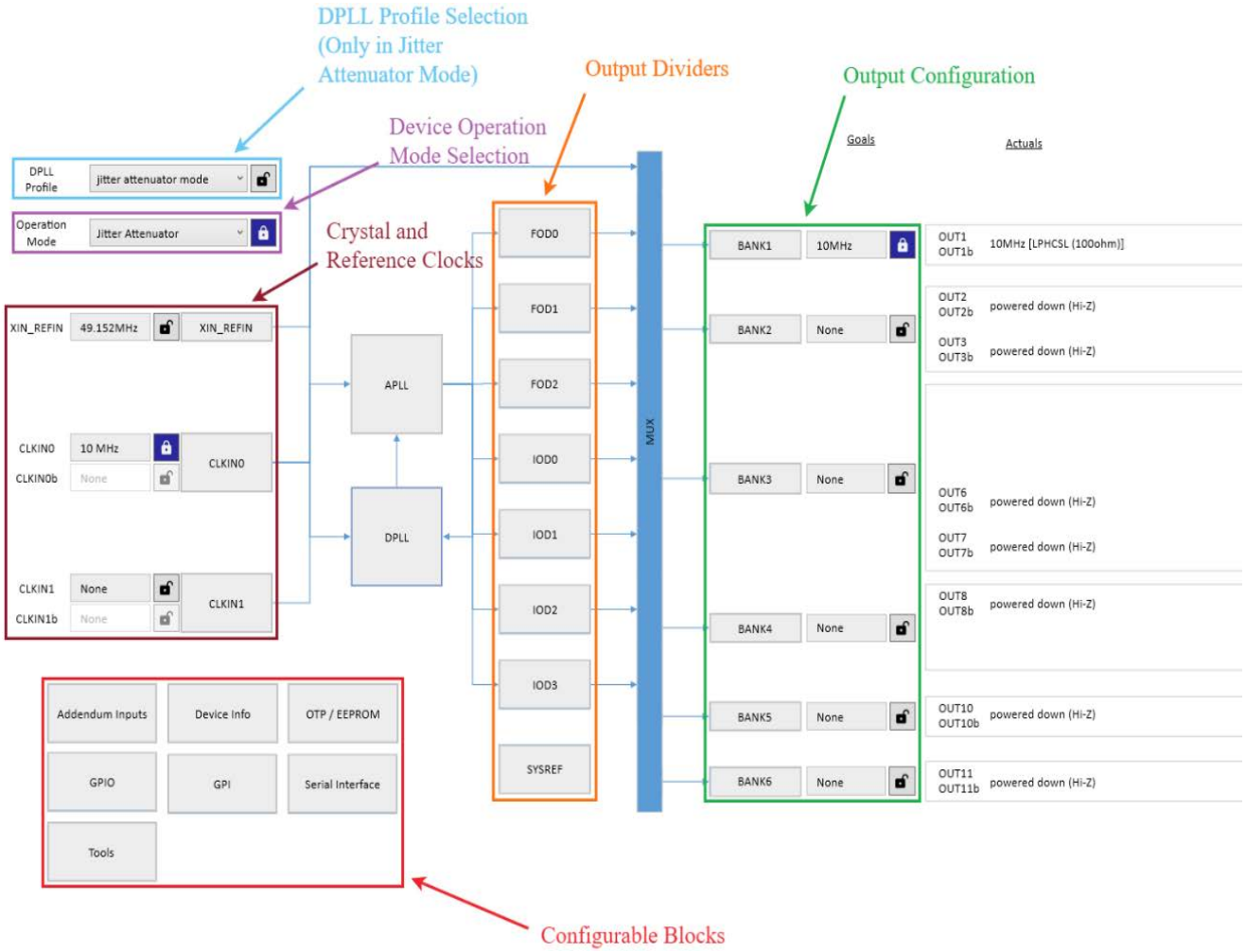


7. Register View

The register view shows a graphical diagram of the registers and enables reading or writing any of the individual registers. By clicking on the individual register block, the given registers for that block will appear to the right. They can either be adjusted by writing directly to the diagram or entering values into the data fields on the right.

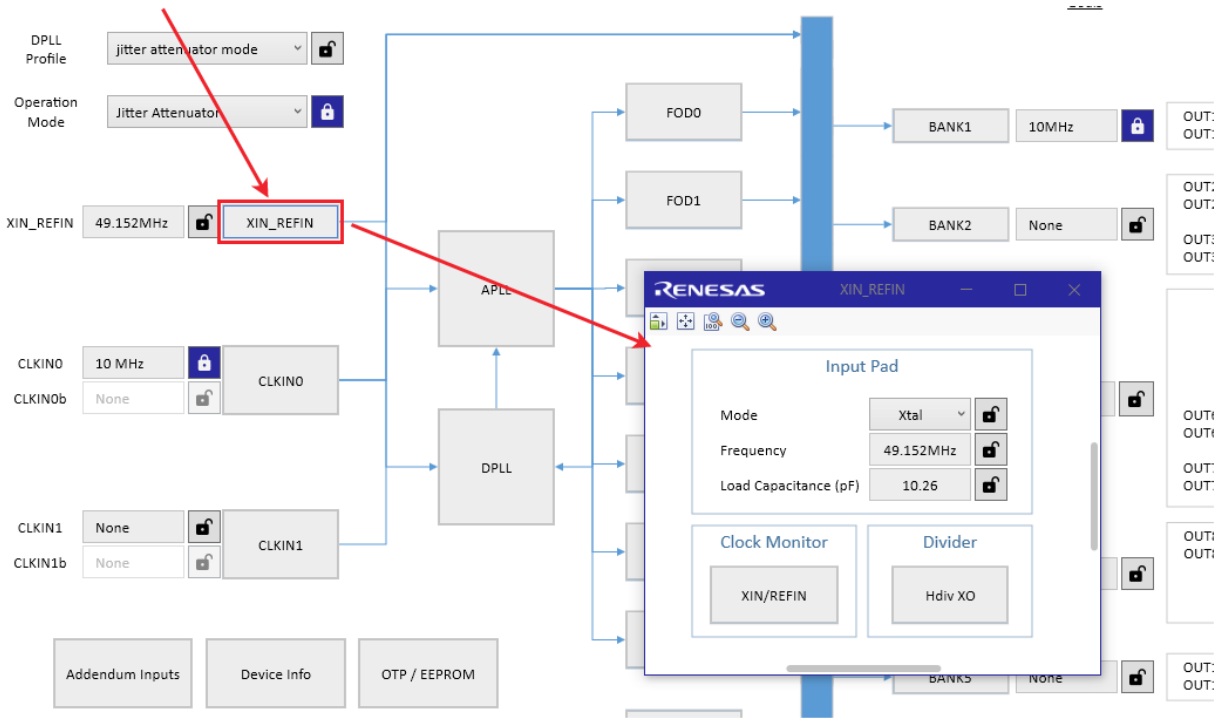
8. Block Diagram View

The block diagram view reflects the datasheet representation of the VersaClock 7 devices. The main diagram enables adjustment of the operation mode, setting the output frequency and type, changing the output divider, setting the Xin frequency and the input frequency, and viewing the output frequency estimate. Each block has its own pop-out page. This can be accessed by clicking on the block.



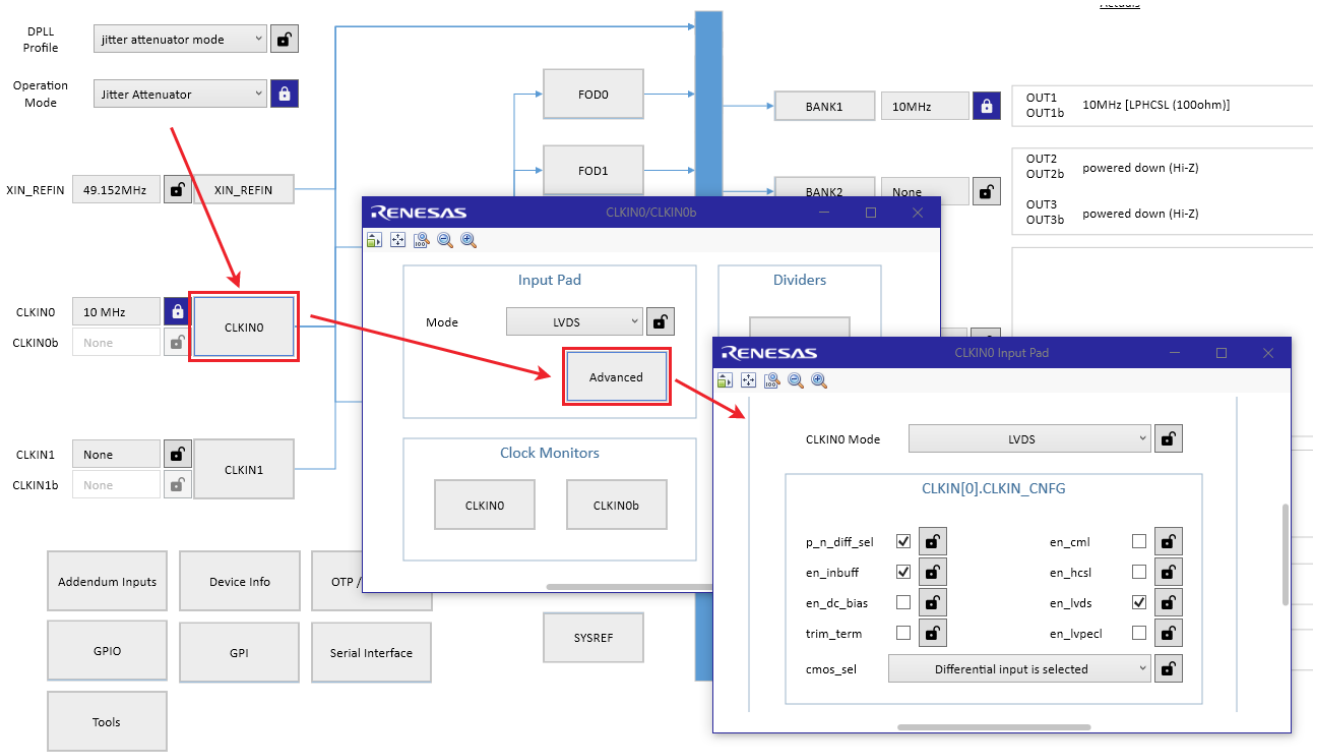
8.1 OSC Block

Clicking on the *XIN_REFIN* block gives access to the settings that configure the Xin frequency and internal tuning capacitors.



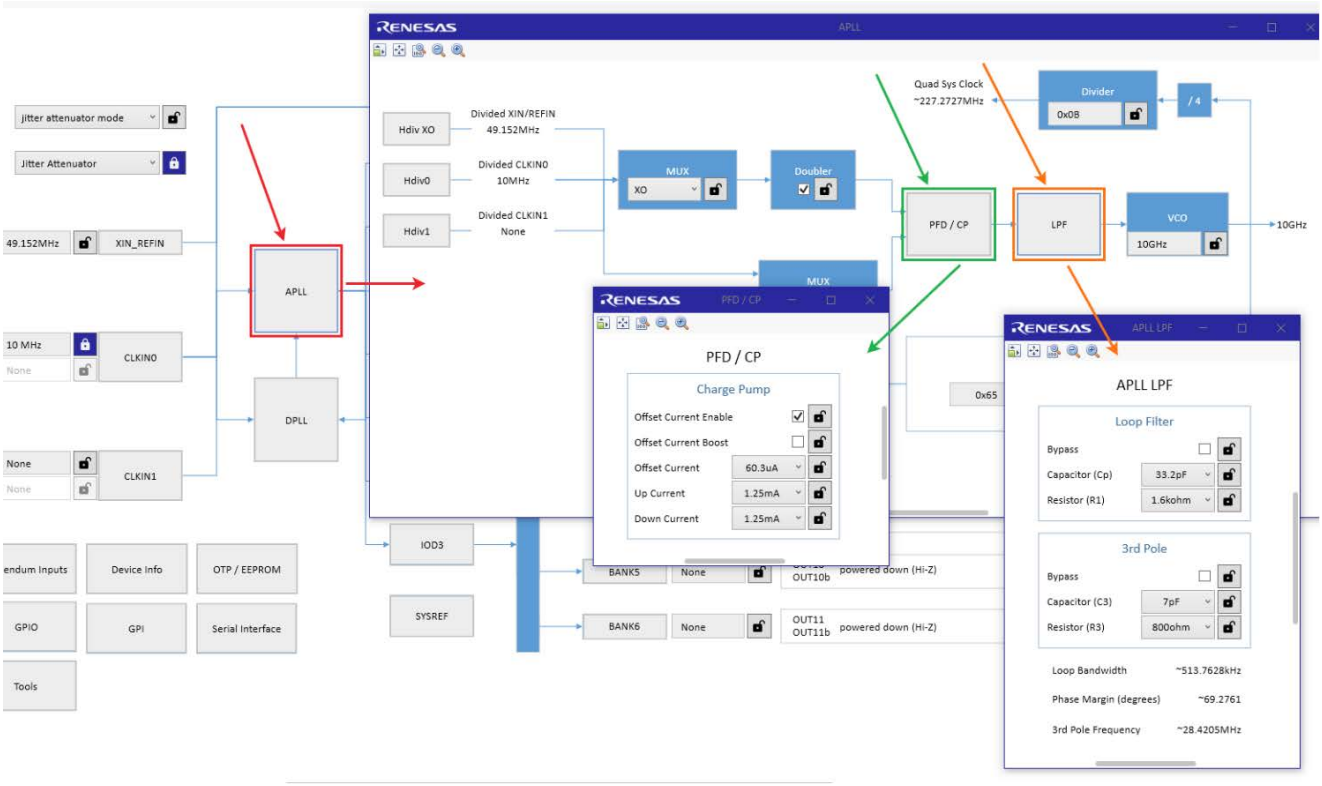
8.2 Inputs Block

Clicking on the *CLKINx* block allows the control of the input signal type selection, input terminations, and input clock monitors.



8.3 APLL Block

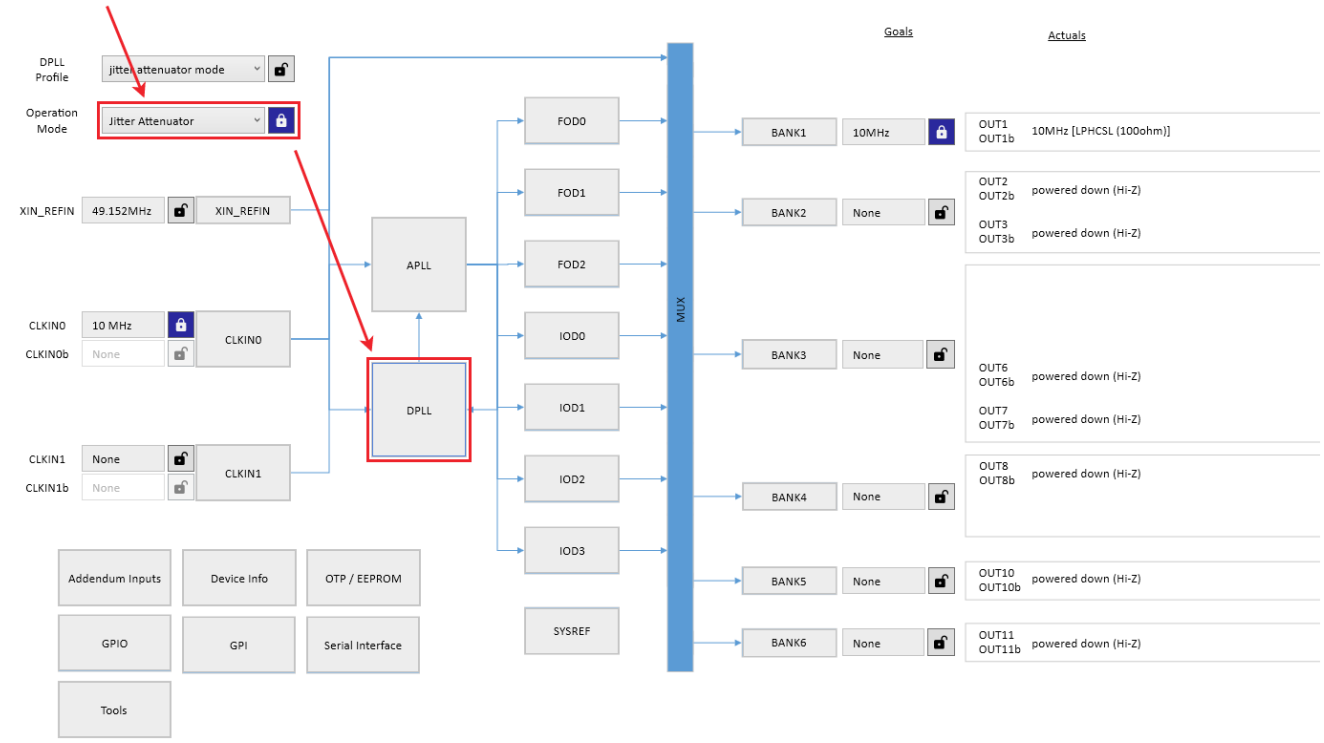
Clicking on the *APLL* block enables configuration of the input mux, charge pump settings, and internal low pass filter settings. The VCO frequency and the Feedback Divider value can also be changed from here.

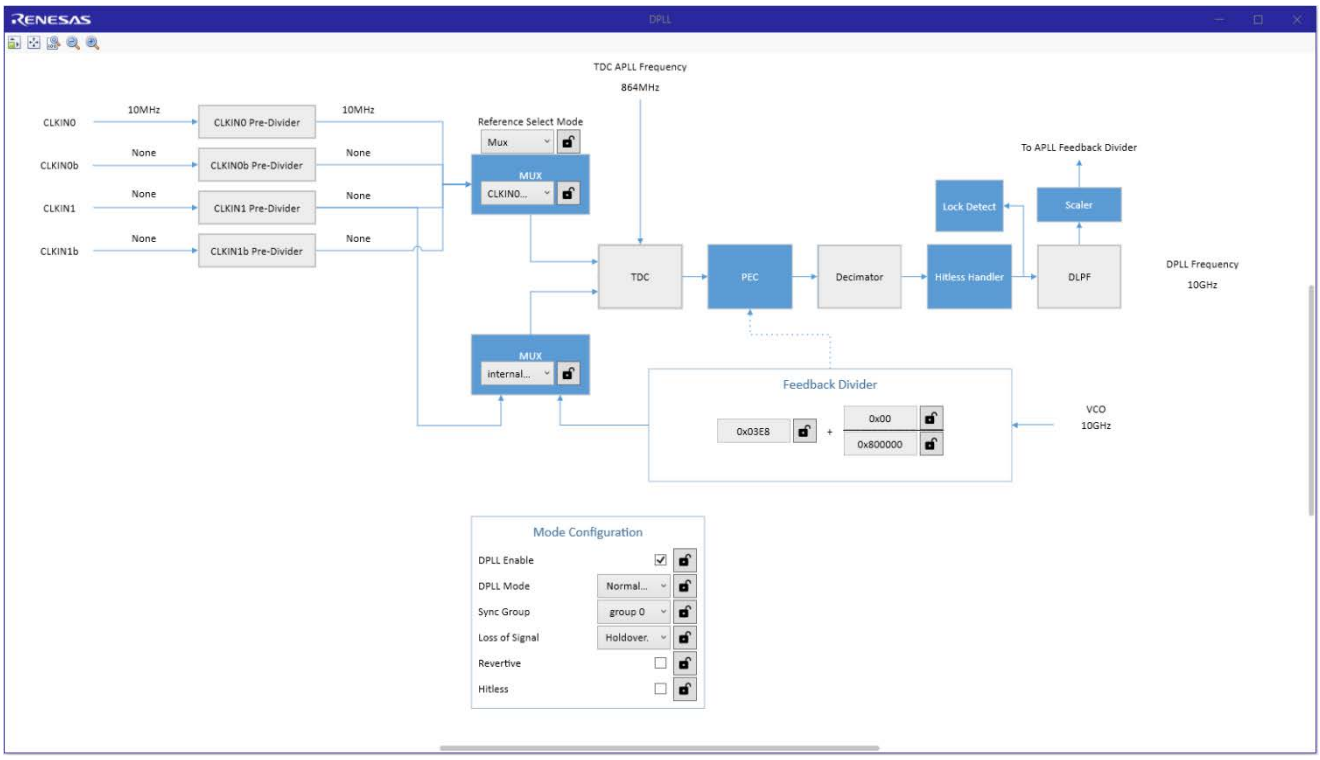


8.4 DPLL Block

The *DPLL* block is only accessible when the device operation mode is set to “Jitter Attenuator”. This block contains all features pertaining to the DPLL. Clicking on the *DPLL* block enables revertive or hitless switching, adjustment of the phase offset, and the ability to change the digital loop filter settings.

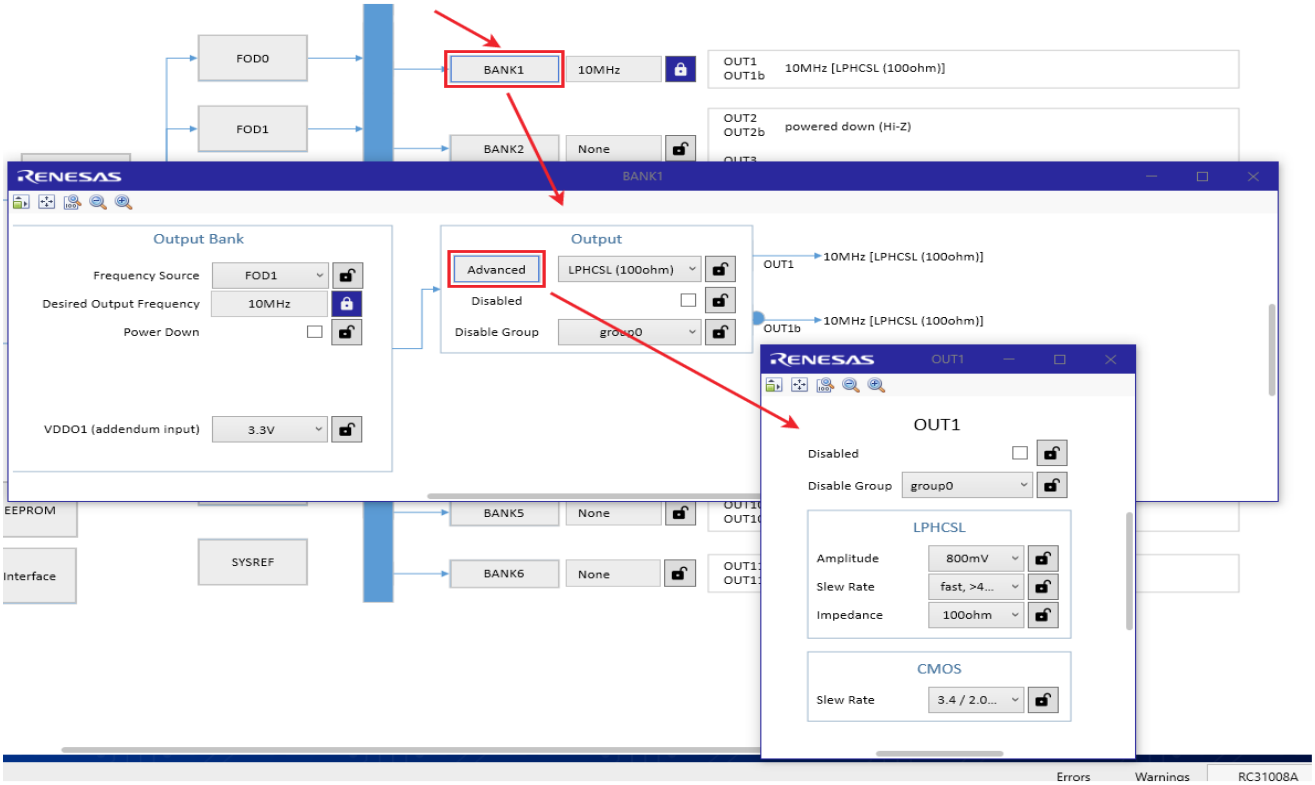
Note: Some VersaClock 7 devices may not have the ability to use this feature.





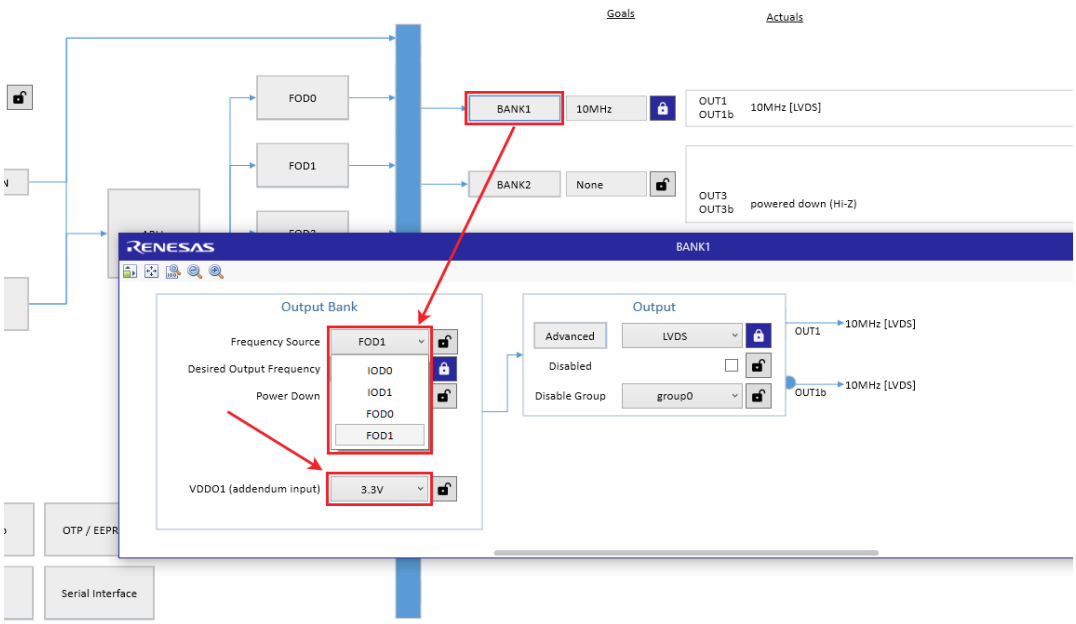
8.5 Outputs Block

Each output can be configured by clicking on the appropriate *Bank* button on the main block diagram. For a broader range of adjustable settings, click on the *Advanced* button.



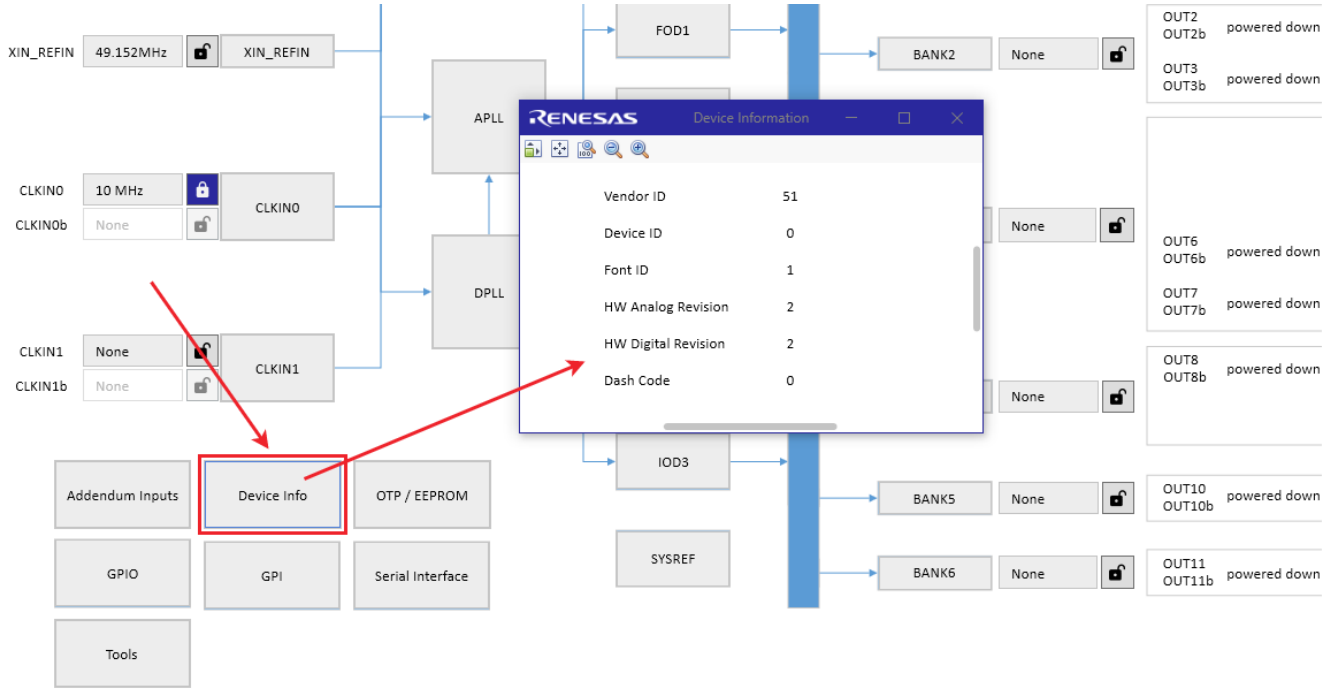
The frequency source for each output bank can be set to either an Integer Output Divider (IOD) or a Fractional Output Divider (FOD). The addendum input (VDDO) for each output bank can be set to one of the following:

- 1.8V
- 2.5V
- 3.3V
- NC (not connected)



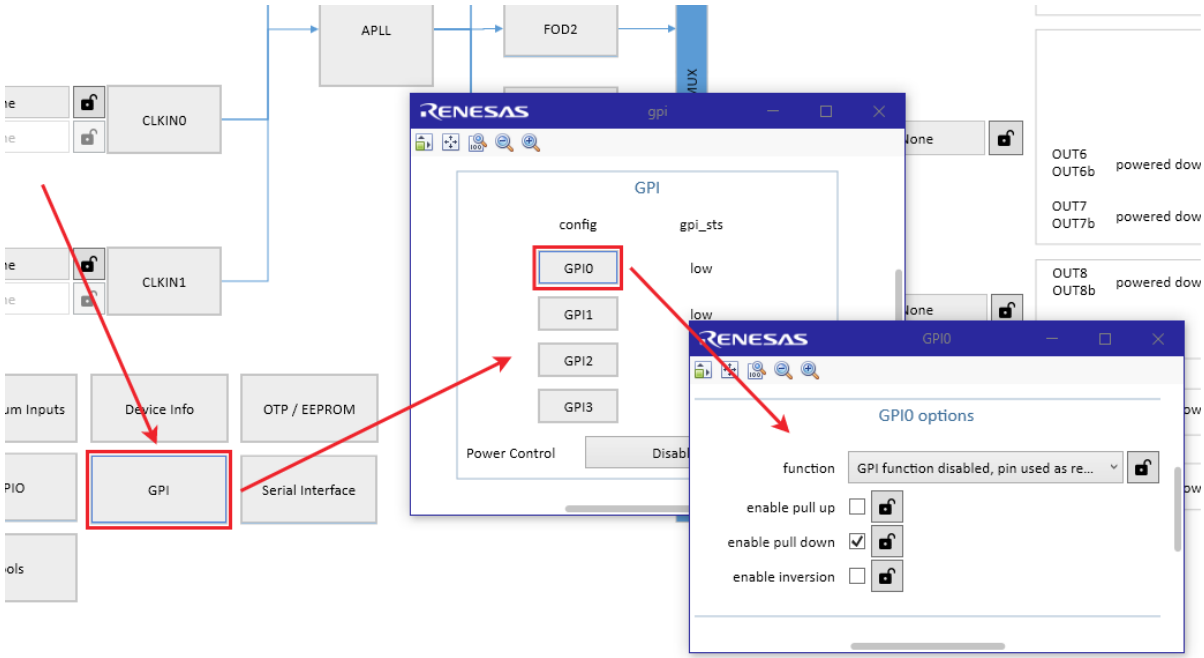
8.6 Device Info

The *Device Info* button opens a window that contains the Vendor ID, Device ID, Rev ID, and Dash Code.



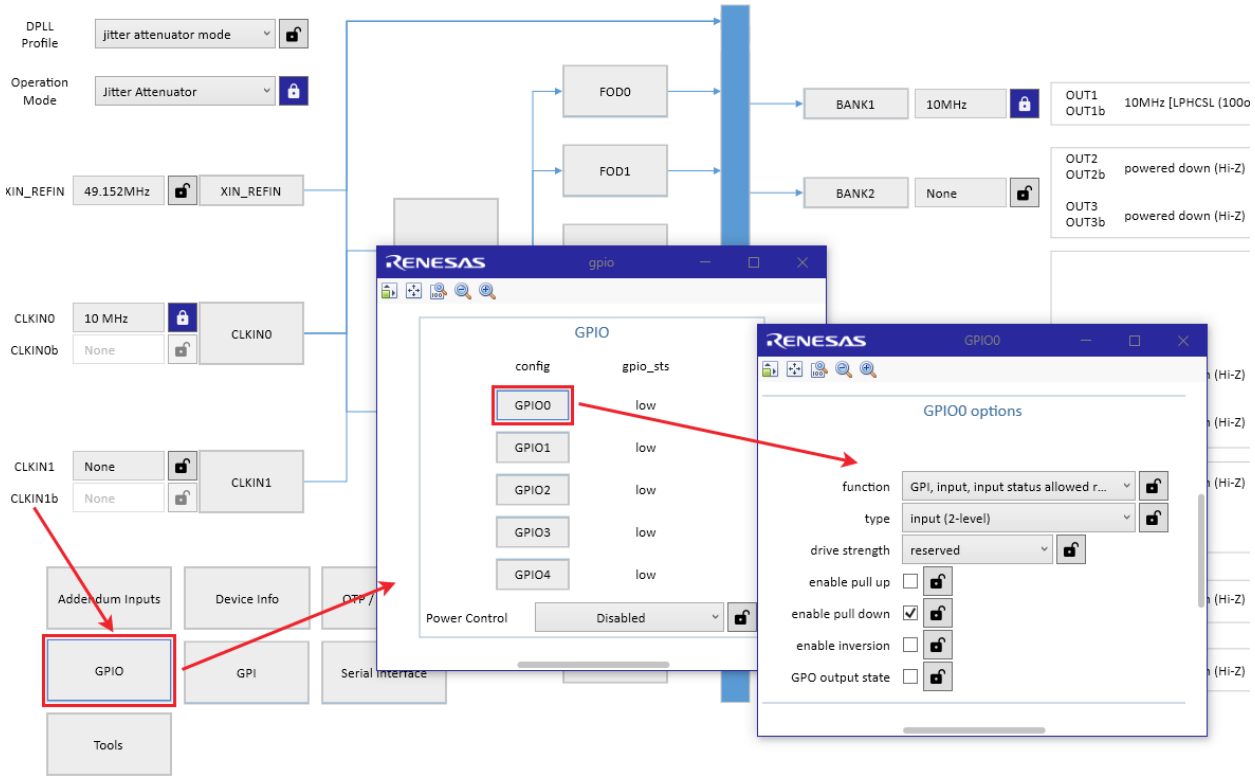
8.7 GPI Block

Clicking on the *GPI* block enables configuration of the input functionality, enable/disable pull-up/pull-down, and enable/disable inversion.



8.8 GPIO Block

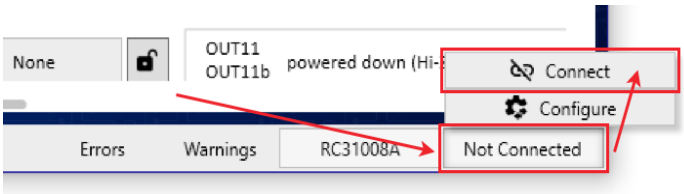
Clicking on the *GPIO* block enables configuration of the output enable pin, internal SDA and SCL pull-ups, and the lock detection.



9. Device Connection

Device connection can be achieved through the bottom right corner of every page. To connect one of the Renesas evaluation boards, ensure the device is powered and connected to the working computer. Then, click the *Not Connected* button in the corner of the screen. This will lead to a small pop-out page. Click the connect symbol in the corner of the page to establish a connection to the device.

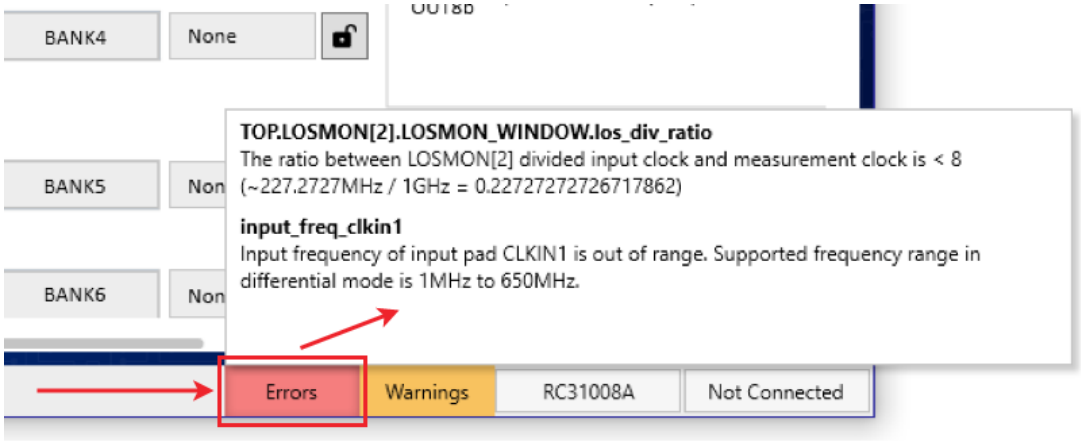
See the *Evaluation Board User Manual* for more information regarding device connection. This manual is located on the [VersaClock 7 Evaluation Kit] page.



10. Errors and Warnings

When adjusting the values in the configuration, errors or warnings may arise. These are used to help users stay within the limitations of the device and give recommendations to how to configure it. Errors must be cleared before writing to the device.

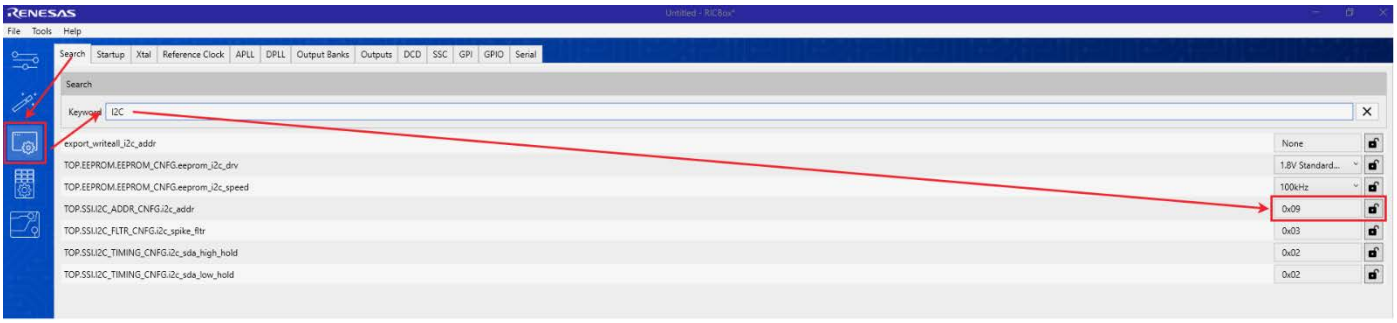
The bottom right corner of the screen shows how many errors or warnings have occurred. Click on one to view the contents.



11. Common Configurable Settings

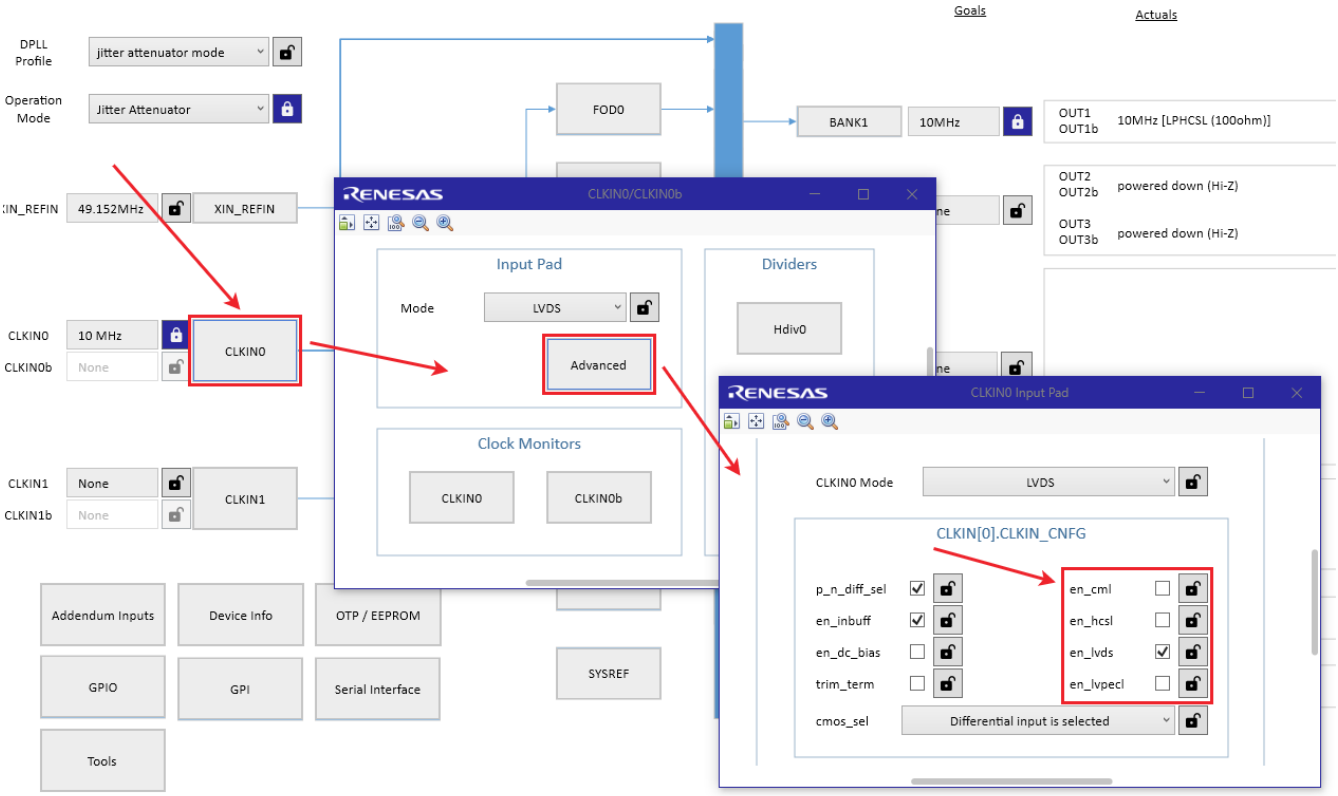
11.1 Changing the I²C Device Address

1. Enter the configuration view.
2. Type “I2C” into the search bar.
3. Change the ‘TOP.SSI.I2C_ADDR_CNFG.i2c_addr’ setting to the desired address.



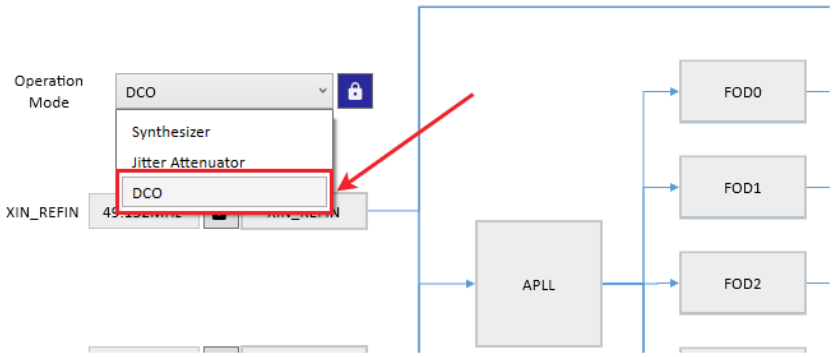
11.2 Disabling the Internal Input Terminations

1. Go to the block diagram view.
2. Click on the *CLKINx* block.
3. Click on the *Advanced* block.
4. Enable/Disable the terminations.

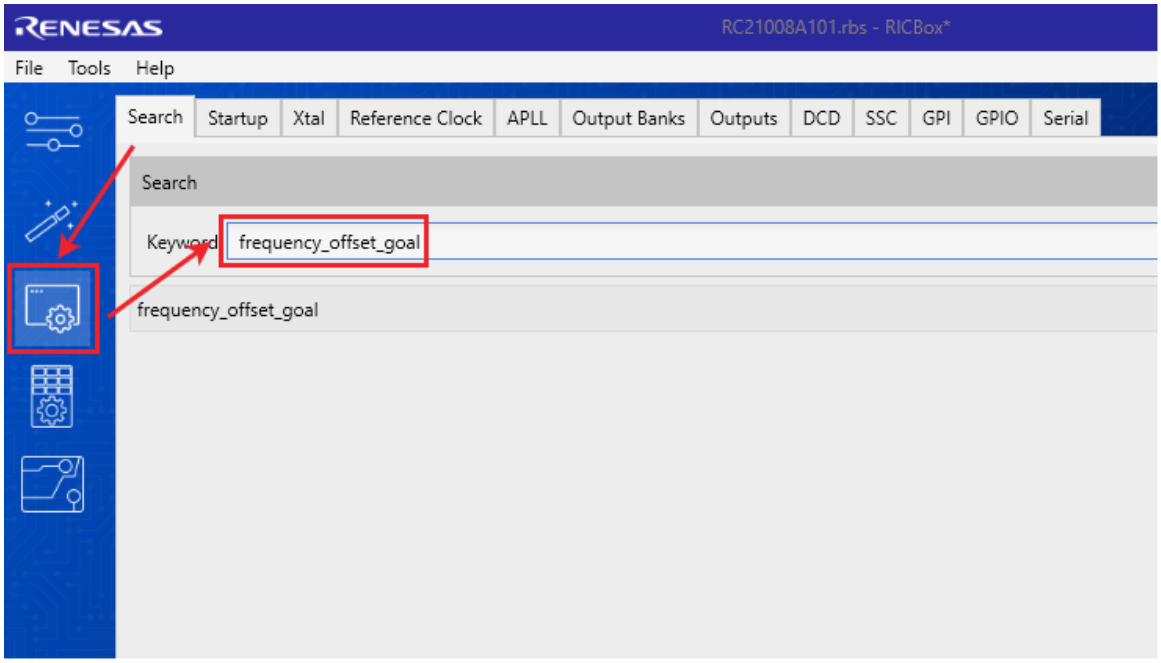


11.3 Configuring the Device for Write Frequency Mode

1. Go to the block diagram view.
2. Change the Operation Mode to “DCO”.



3. Go to the *Configuration* view.
4. Search for “frequency_offset_goal”.



5. Adjust the frequency control word through the “frequency_offset_goal” data field.

12. Revision History

Revision	Date	Description
1.00	Aug 18, 2022	Initial release.

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