RICBox GUI Software for FemtoClock3-Wireless

This document explains how to use the Renesas IC Toolbox (RICBox) software to configure and control FemtoClock3-Wireless devices. For general RICBox instructions, see the RICBox Software Manual.

Contents

1. Installation and Setup

Ensure that the latest version of the Renesas IC Toolbox (RICBox) software is installed. New versions are released frequently and can provide a better experience with new functionality. The RICBox software can be installed directly from the RICbox webpage on the Renesas website.

Note: Both RICBox software and FemtoClock3-Wireless device plugin must be installed to access the user interface. If the device is not listed in the RICBox plugin list, then manual installation is required. For instructions on how to install the latest version of RICBox, device plugins, and maintain updates, see sections 1 and 11 of the RICBox Software Manual.

2. Loading and Creating Configurations

2.1 Creating a new Configuration

1. Start > RICBox
2. Click Create new project.

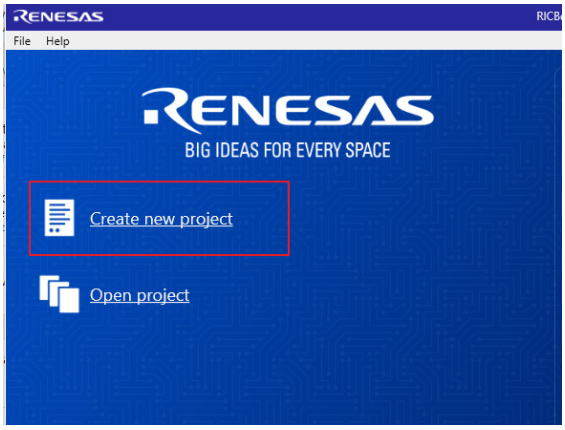

Figure 1. Open New Project in RICBox

3. Use the **Select a Product Family** box to choose the “FemtoClock3” devices.
4. Select the variant being evaluated and click **OK**. In this example, RC38312A is used.

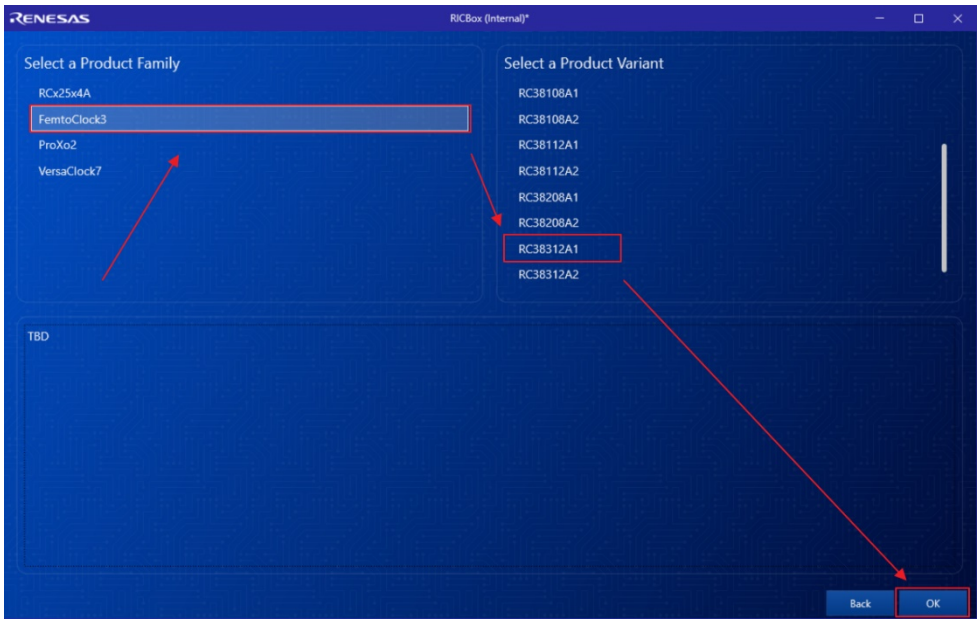

Figure 2. Selecting RC38312A Device GUI in RICBox

2.2 Loading a Settings File

Loading a settings file is like creating a new one.

1. To load an existing settings file, click on the **Browse** button just after opening the RICBox software. This will take the user to a file browser.

   Note: Recently used settings files are under the “Recent Files” section.

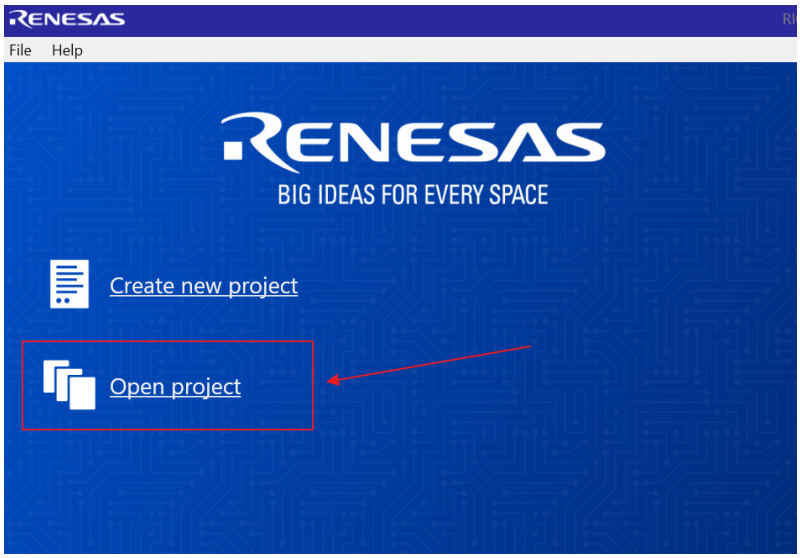

Figure 3. Open Existing Project

2. Navigate to the directory that stores the settings file and select it. RICBox settings files have the file type ‘.rbs’.

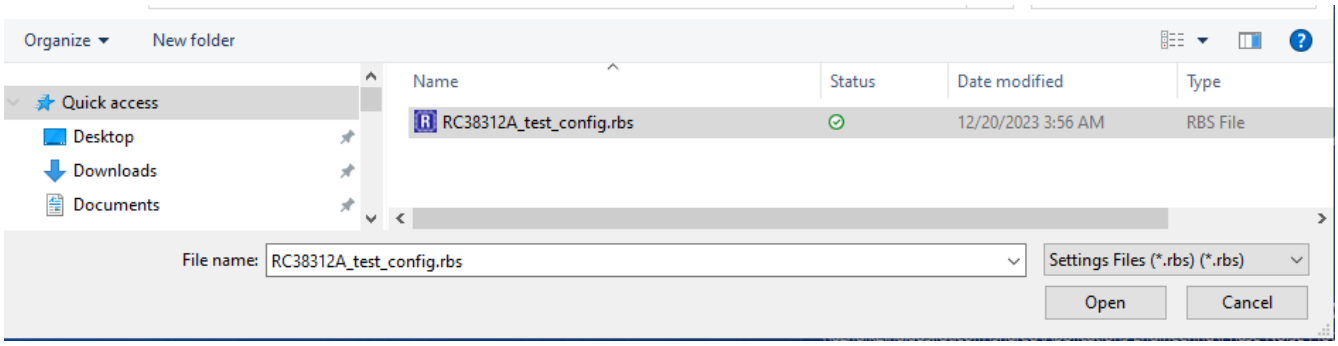

Figure 4. Select .rbs File

2.3 Adding Configurations to a Settings File

More than one device configuration can be created at a time. Different configurations can hold differing device settings but still be saved to the same RICBox settings file (.rbs).

1. In the lower right corner of a plugin GUI click on the part number box to view the configuration selection drop-down menu.

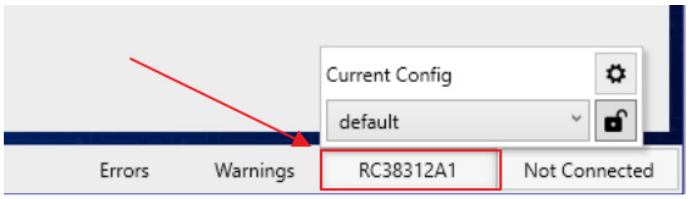

Figure 5. Configuration Menu

Use this menu to change the currently active configuration. The initial configuration is always labeled *default*.

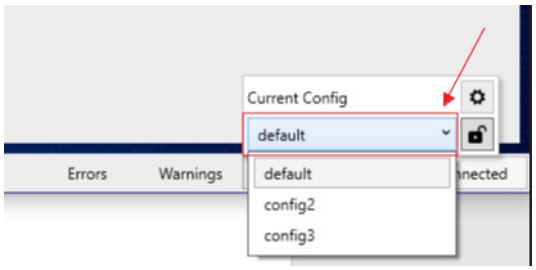

Figure 6. Configuration Selection

2. Click on the settings button to view the configurations pop-up menu.

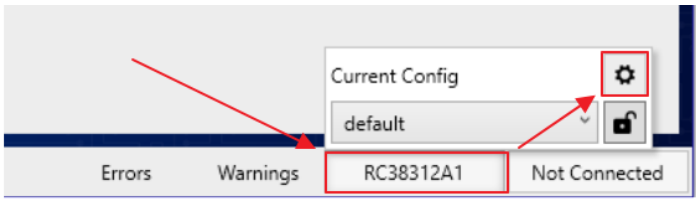

Figure 7. Configuration Settings

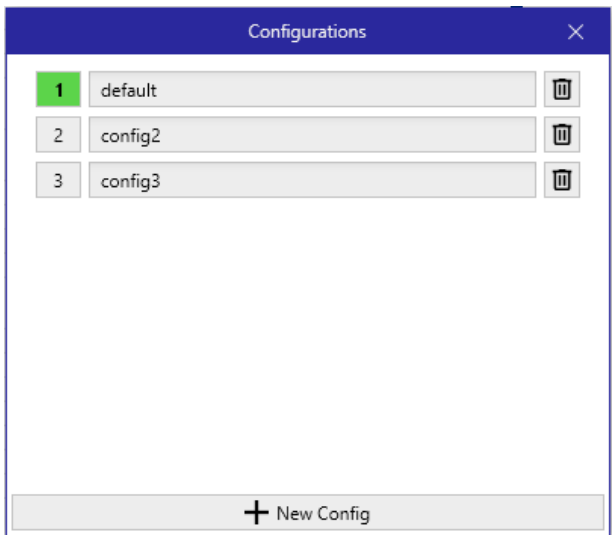

Figure 8. Configurations Pop-up Menu

3. Click the numbers to change the currently active configuration. Green is the active configuration.

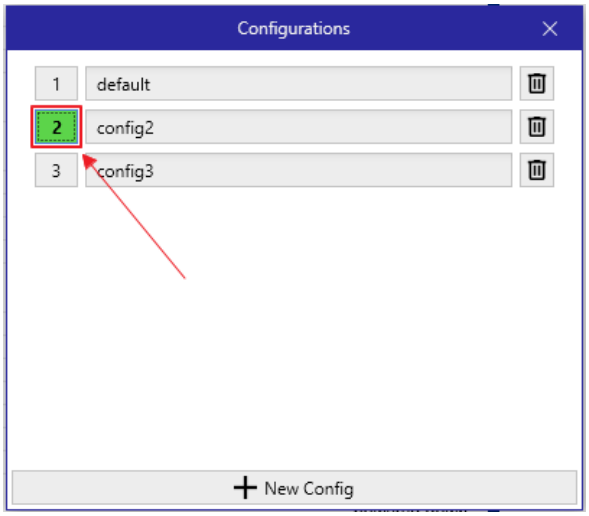

Figure 9. Currently Active Configuration

3. Side Panel Buttons

The side panel consists of five separate buttons. Each button opens a separate page. Each page has a unique view, allowing the configuration of the device from different perspectives.

- **Overview** button opens the device overview page.
- **Wizard** button opens the initial wizard page.
- **Configuration** button displays the register settings in a readable text format with a search engine.
- **Register** button shows a graphic of the registers in the device.
- **Block Diagram** button opens a configurable block diagram view

Figure 10. Side Panel Buttons

4. Control Panel (Device Overview)

The control panel view displays an overview page depicting the major settings for the device. This page can be used as an important reference for the overall device configuration.

RC38312A1

Settings	
Dash Code	
Modes	
DPLL[0]	ja
DPLL[1]	synth
DPLL[2]	synth
Inputs	
XIN	49.152MHz
CLKIN0	10MHz
CLKIN1	None
CLKIN2	None
CLKIN3	None
nCLKIN0	None
nCLKIN1	None
nCLKIN2	None
nCLKIN3	None
SysClock	
Quad sys clock	~227.2727MHz
Outputs	
OUT0	disabled
OUT1	disabled
OUT2	disabled
OUT3	disabled
OUT4	disabled
OUT5	disabled
OUT6	disabled
OUT7	disabled
OUT8	disabled
OUT9	disabled
OUT10	disabled
OUT11	disabled
APLL	
APLL Frequency	10GHz (-0.006ppt from goal of 10GHz)
VCO Output FFO	FFO = XO * LPF_0
Divider	~203.4505
Loop Bandwidth	~1.1057MHz
Phase Margin	~78.552 degrees
Third Pole Frequency	~31.831MHz
DPLL[0]	
Enabled	yes
DPLL Profile	JAMODE (jitter attenuator mode)
DPLL Frequency	10GHz
FOD Output FFO	FFO = XO
Divider	500
Normal Bandwidth	~24.392Hz
Acquire Bandwidth	~243.9197Hz
Decimator Bandwidth	~1.5542kHz
Normal Gain Peaking	~0.1964 (-1.776% from goal of 0.2)dB
Acquire Gain Peaking	~0.1925 (-3.7496% from goal of 0.2)dB
DPLL[1]	
Enabled	no
DPLL[2]	
Enabled	no

Figure 11. Control Panel (Device Overview)

5. Configuration View

Configuration view enables easy movement through register settings via the tabs at the top of the page. Each section has all the critical registers and data fields listed to configure the device block.

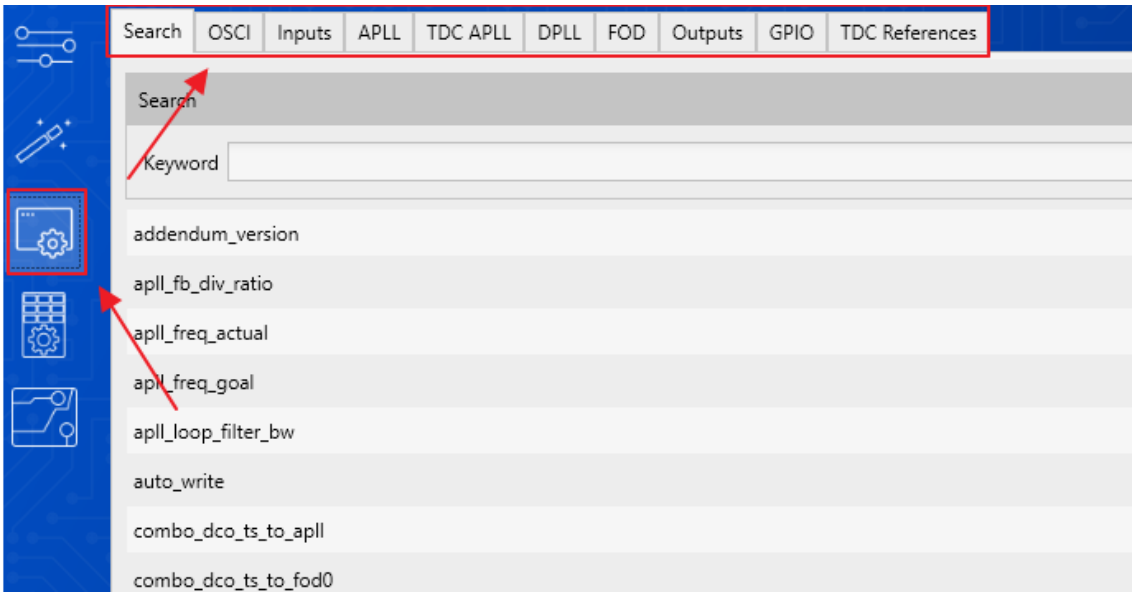

Figure 12. Configuration View

The search tab provides access to the configurable fields through a search bar. The search engine can be used to find any specific configurable field.

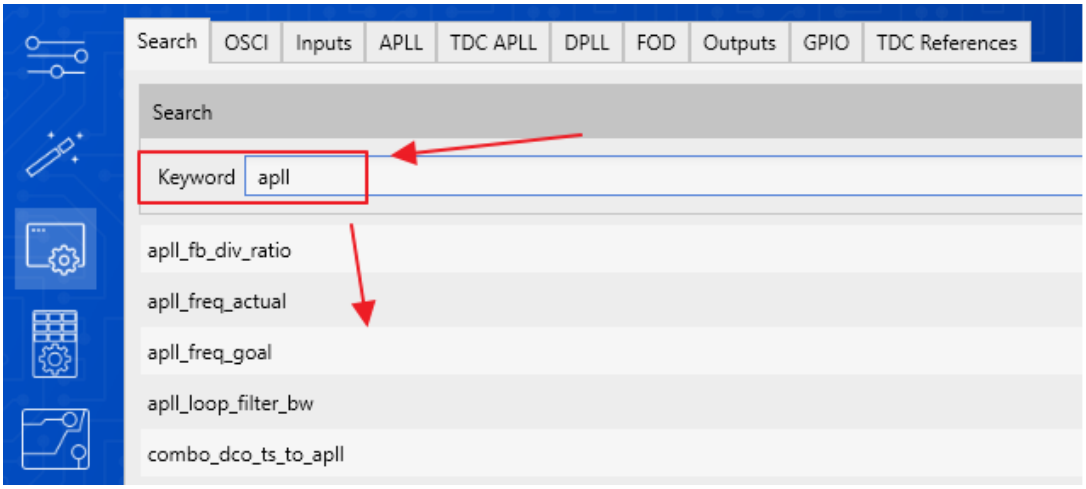

Figure 13. Search for Registers

6. Register View

The register view shows a graphical diagram of the registers and enables reading or writing any of the individual registers. By clicking on the individual register block, the given registers for that block will appear to the right. They can either be adjusted by writing directly to the diagram or entering values into the data fields on the right.

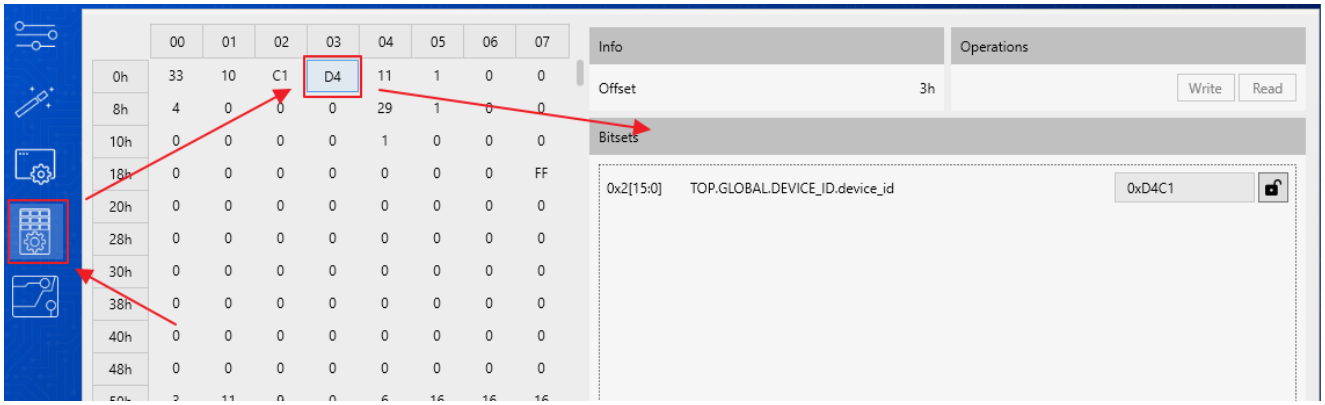

Figure 14. Register View

7. Block Diagram View

The Block Diagram view shows the datasheet representation of the FemtoClock3-Wireless devices. The main diagram allows setting the output frequency, setting the XIN frequency, setting the input frequencies, and viewing the output frequency estimate. Each block has its own pop-out page. This can be accessed by clicking on the block.

Note: Grey blocks can be clicked to access additional menus. White and blue shaded blocks are inaccessible.

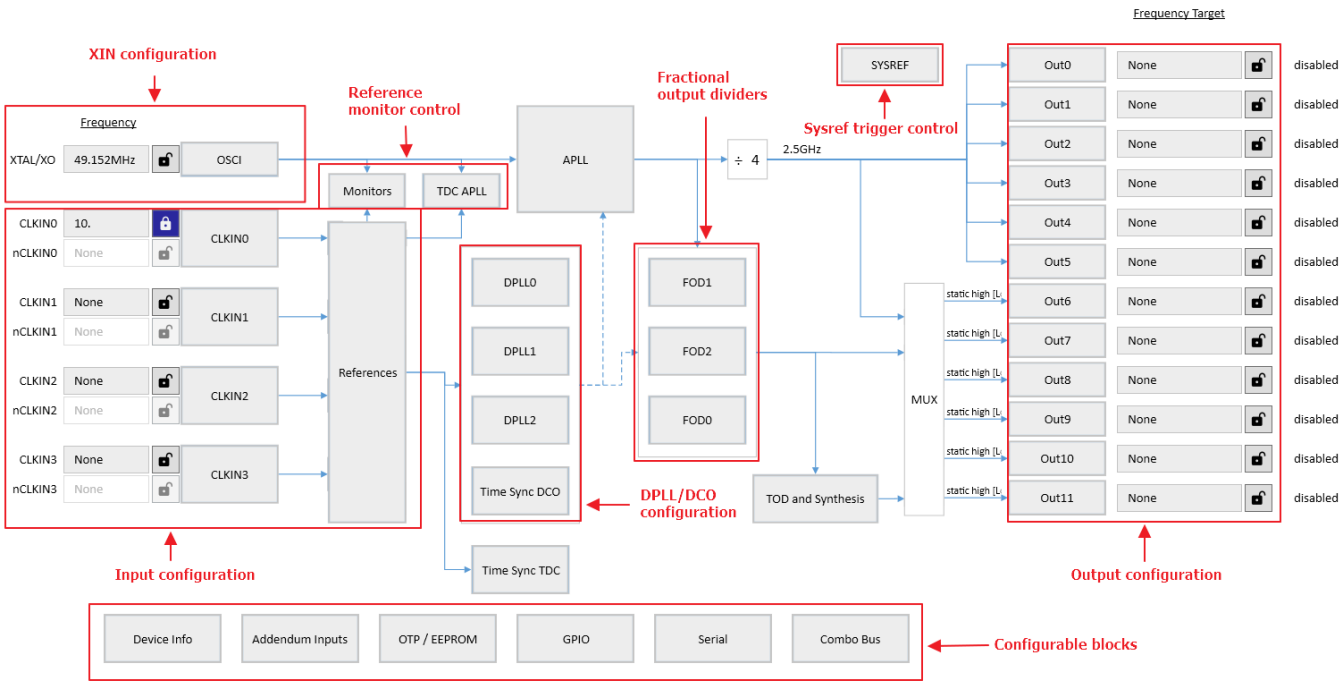

Figure 15. Main Block Diagram

7.1 OSCI Block

The OSCI block can be used to control the crystal frequency and the input capacitance. The GUI assumes a default value of 8.03pF load capacitance as a combination of fixed internal and PCB stray capacitance. Entering a higher value will adjust the internal tuning cap settings.

For more information about load capacitance for FemtoClock3-Wireless, see the “Load Capacitance” section of the application note, *Choosing the Correct Crystal or XO for FemtoClock 3 and FemtoClock 3 Wireless*.

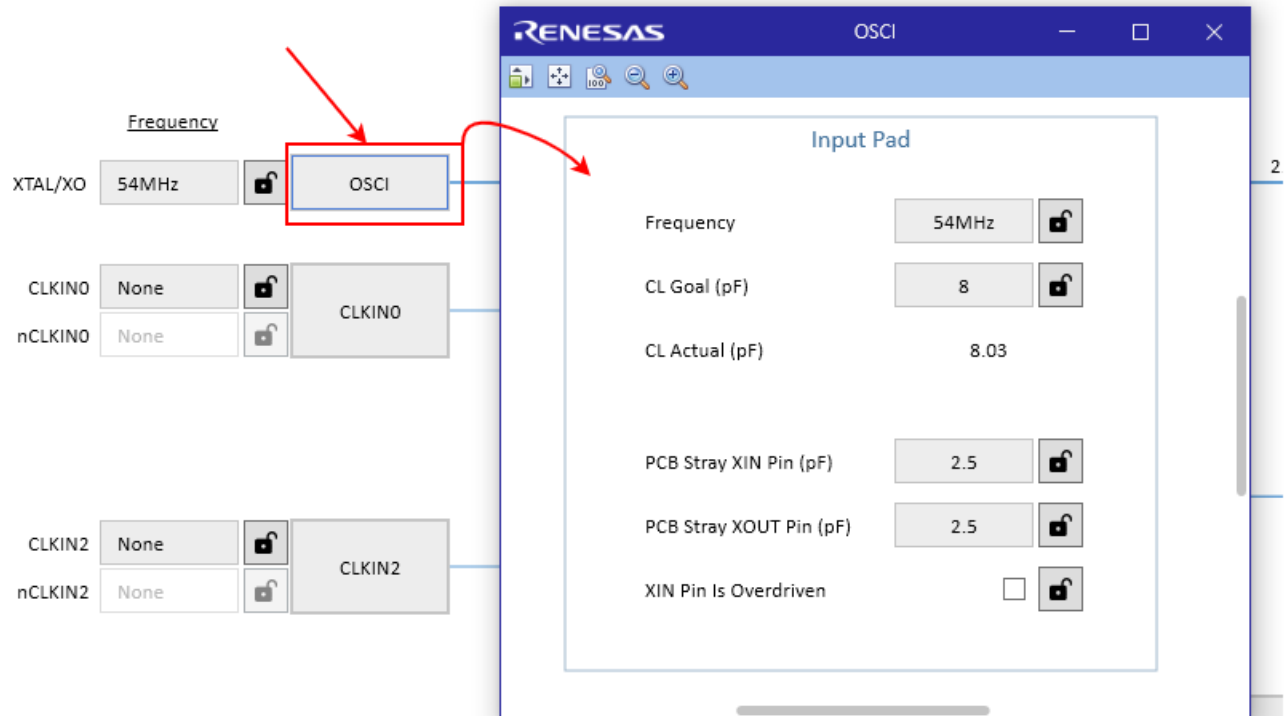

Figure 16. OSCI Block

7.2 APLL Block

The APLL block gives access to the crystal frequency, VCO frequency, low pass filter (LPF) resistor, and feedback divider. The feedback divider is automatically calculated by the software when the VCO frequency and crystal frequency are set.

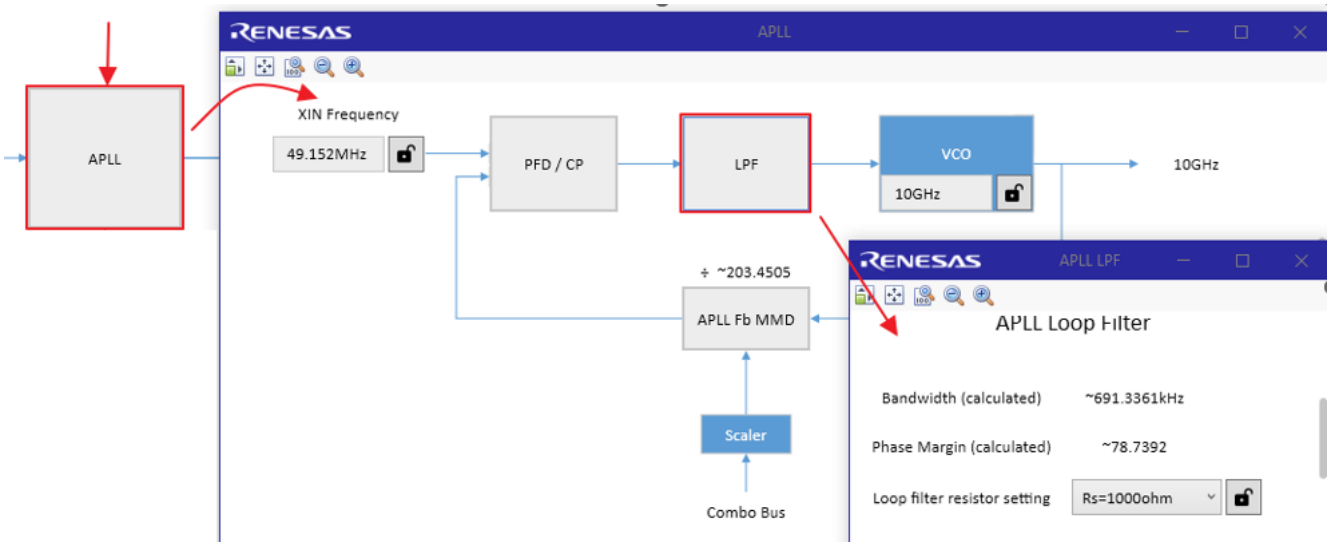

Figure 17. APLL Block

7.3 Outputs Block

The Outputs Block consists of the output reference selection, integer output divider (IOD), and output signal type selection.

Output references can be selected between FODs and VCO/N. This indicated the input frequency that is divided down by the IOD. The input reference is displayed on the main diagram.

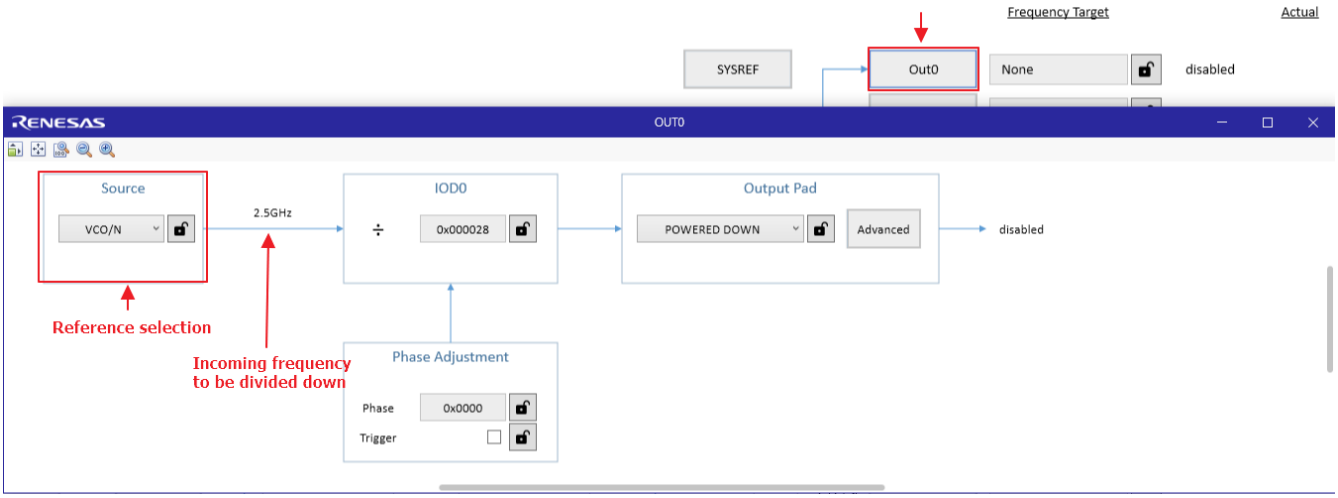

Figure 18. Outputs Block

Note: Out0 to Out5 can only reference VCO/N.

Output frequency can range between 1MHz to 1GHz for differential signals and 1MHz to 250MHz for single-ended signals. Output type can be selected between LVDS, HSCL, and CML. Outputs 8–11 can support CMOS.

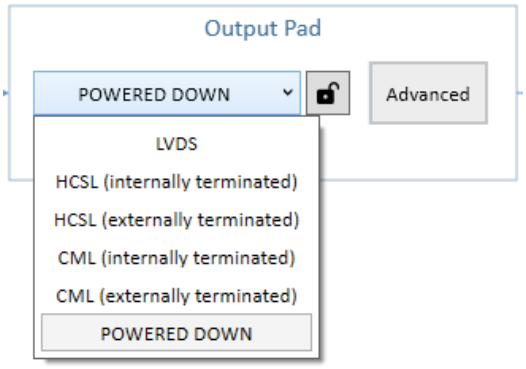

Figure 19. Output Signal Type Selection

The Advanced Block allows for configuring the output frequency, terminations, and voltage/amplitude settings. The Enable Source section dropdown menu chooses how the output enable is controlled, either through GPIO or register setting.

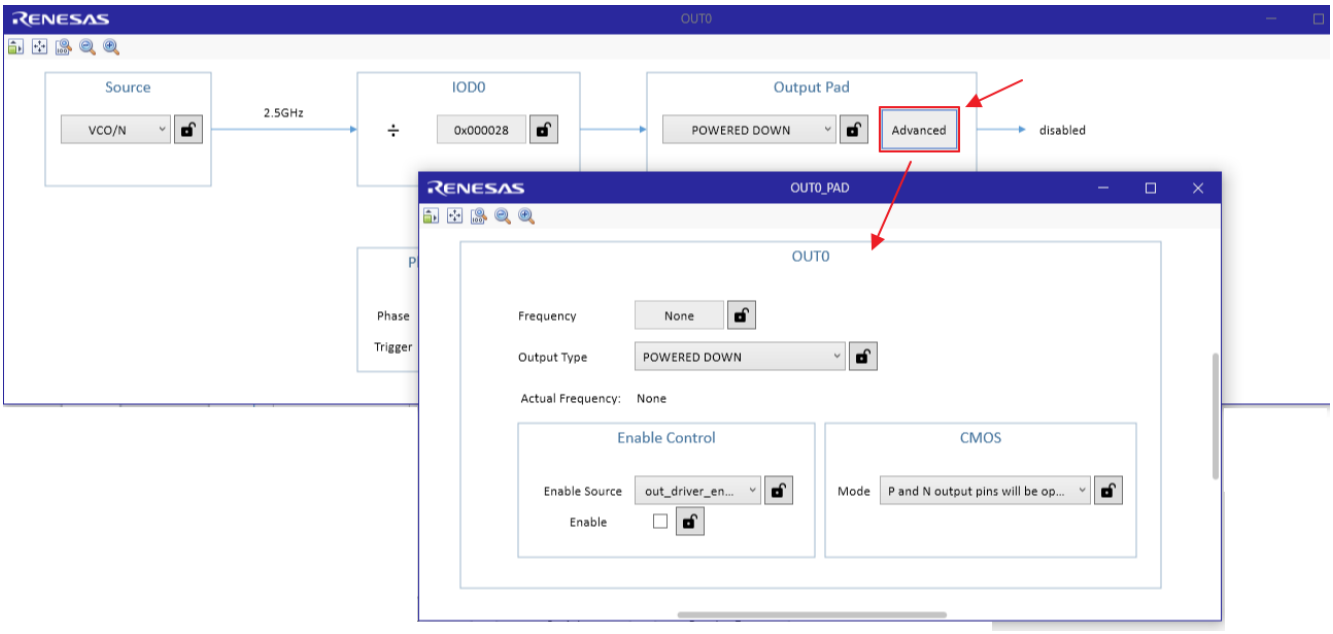

Figure 20. Output Signal Advanced Settings

7.4 FOD Block

The FOD block is used to control the fraction output dividers. The page shows settings for FOD output frequency, FOD mode, and the fractional output divider.

The FOD input reference is the VCO frequency. FOD output frequency ranges from 120MHz to 700MHz. The divider is automatically calculated by the software when the FOD frequency is set.

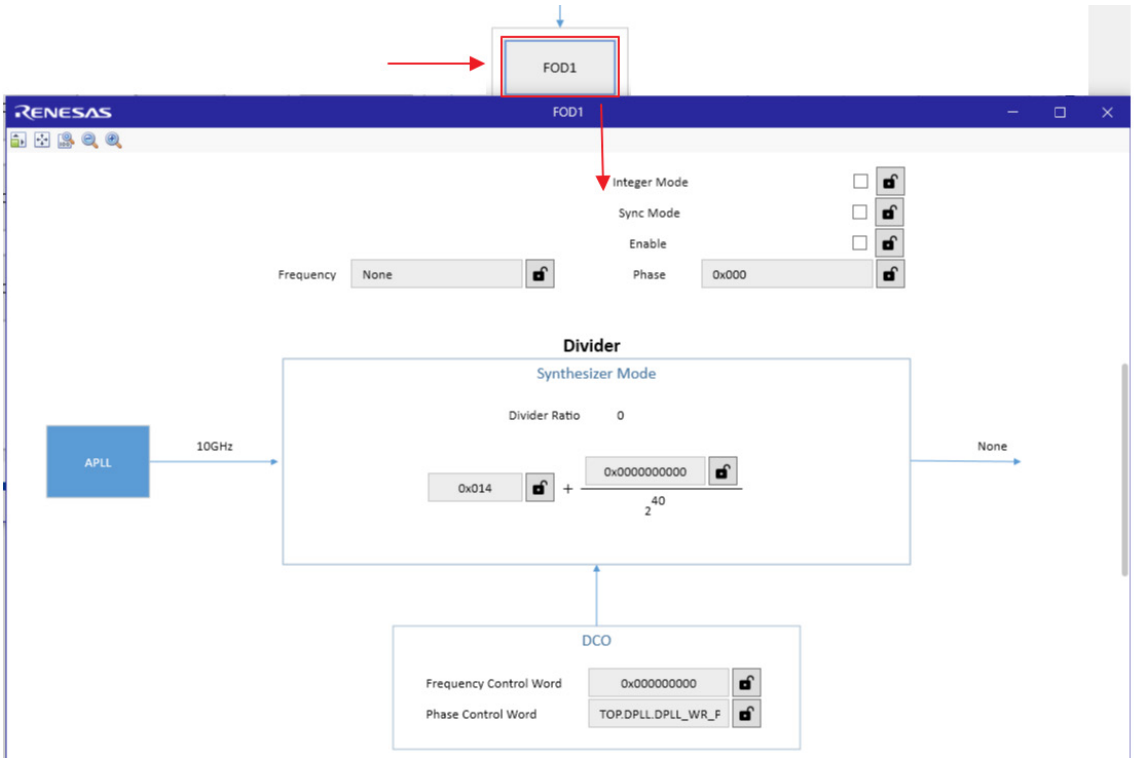

Figure 21. FOD Block

7.5 CLKIN Inputs Block

Clicking on the **CLKIN**x block allows the control of the input signal type selection, frequency, and AC-coupling.

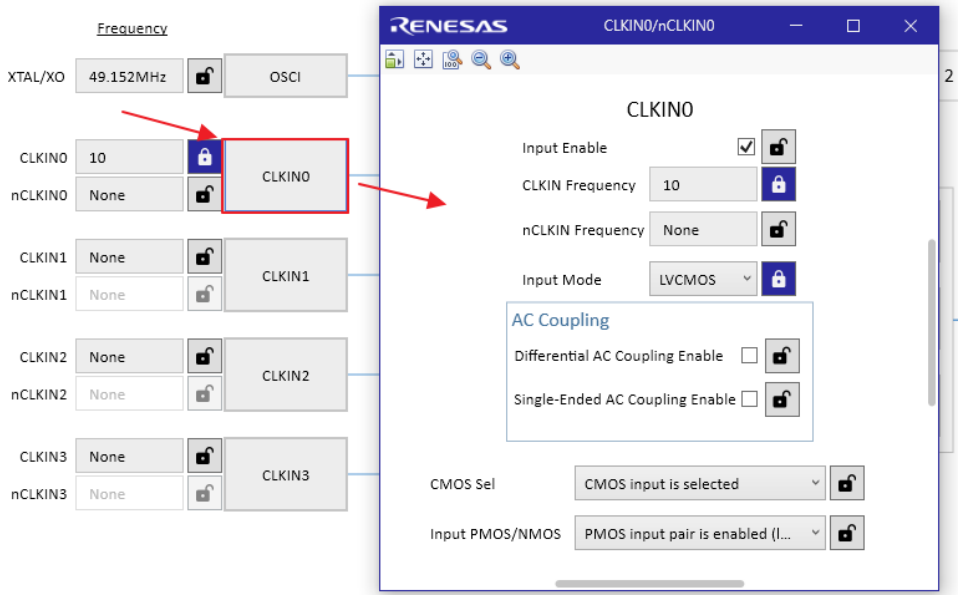

Figure 22. CLKIN Block

7.6 References Block

Clock inputs are connected to a mux to determine which reference each clock corresponds to. Any DPLL can choose between references 0–3 as its input.

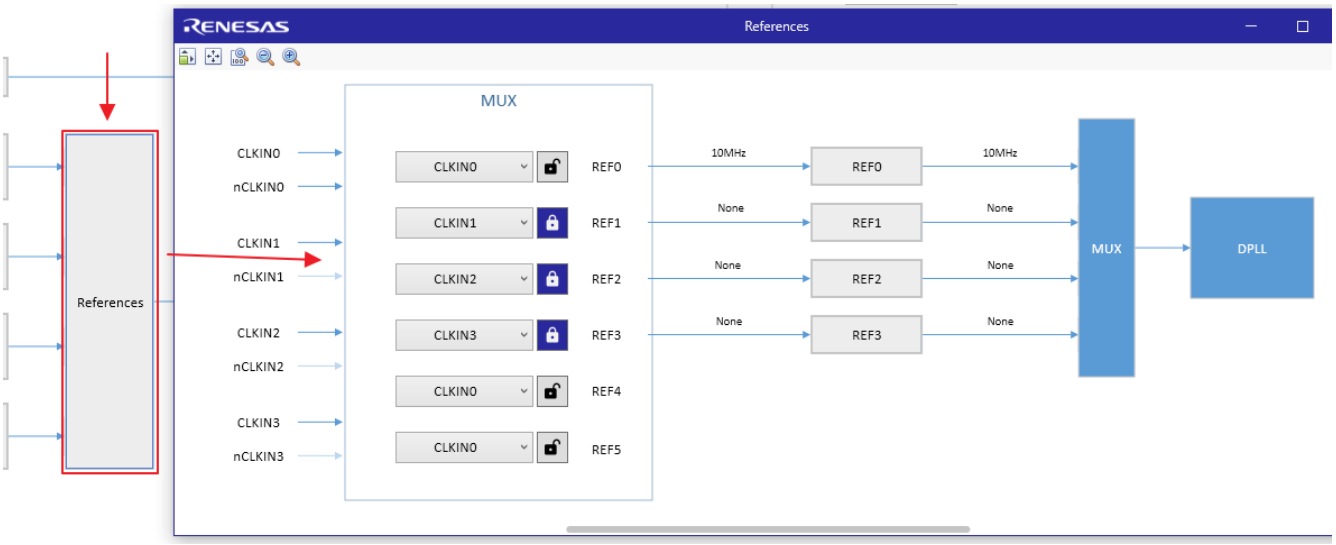

Figure 23. References Block

References must be divided down below 33MHz for the DPLL to lock to them. The input reference divider is accessible through the ref buttons. Clock loss of signal and frequency monitors are available through the Clock Monitor Button.

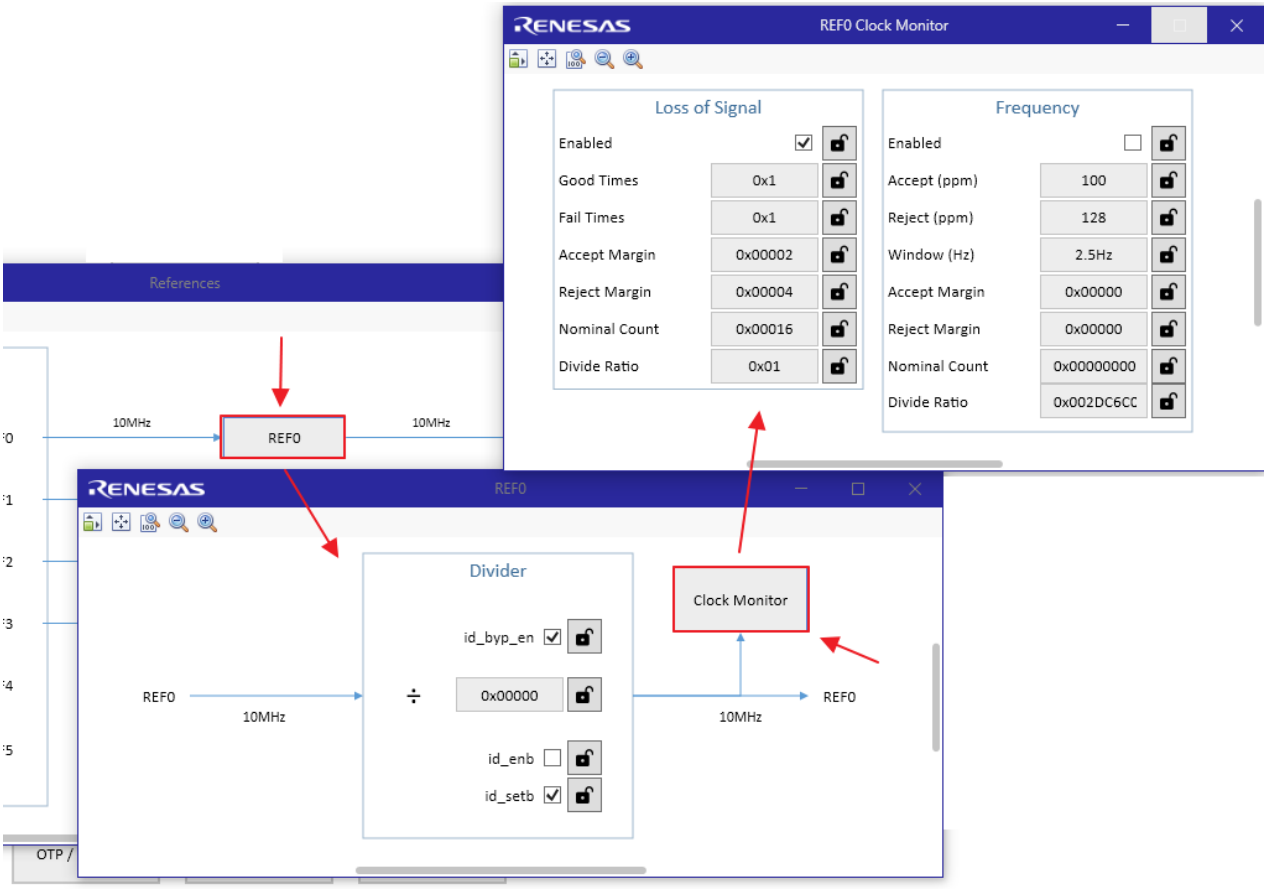

Figure 24. Advanced Reference Settings

7.7 DPLL Block

The DPLL blocks contain all features pertaining to the DPLL. Clicking on the DPLL Block shows settings for reference selection, feedback selection, operation mode, and the ability to change the digital loop filter settings.

Note: Only DPLL0 can switch between VCO and FOD0 feedback clocks as input.

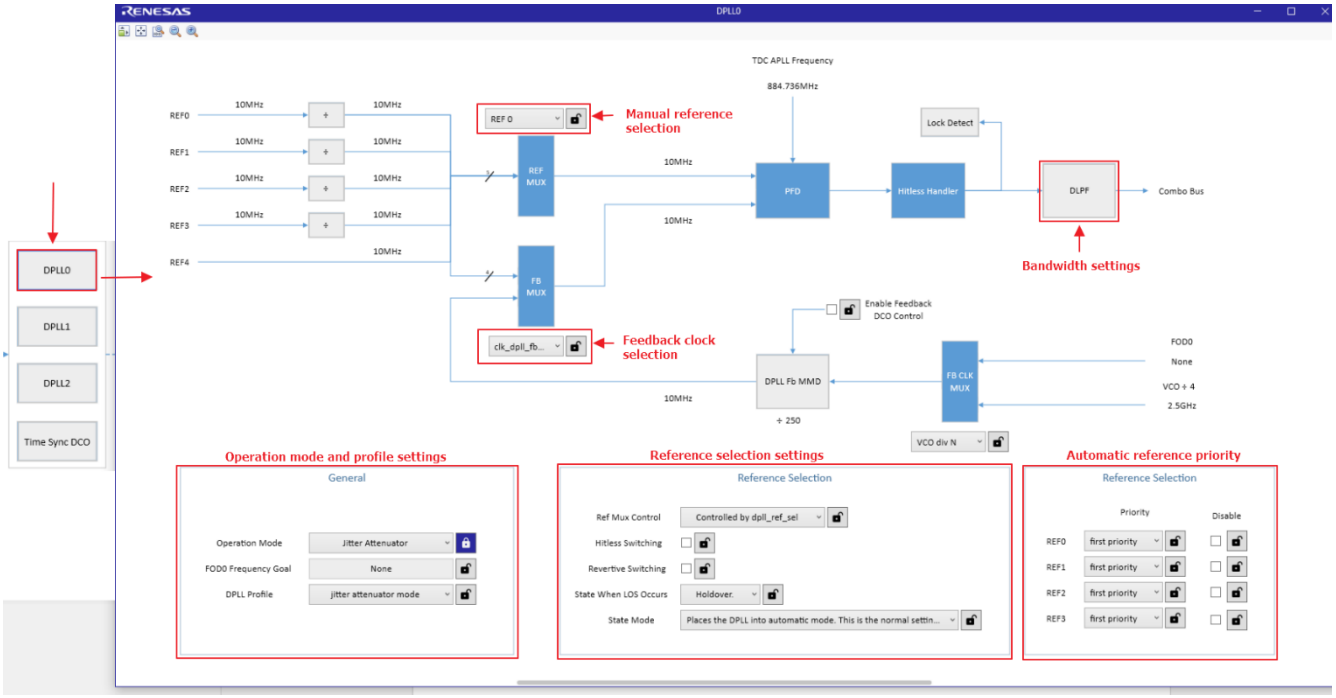

Figure 25. DPLL Block

7.8 GPIO Block

Clicking on the GPIO Block enables configuration of the GPIO function, polarity, output drive strength, and pull-up/down.

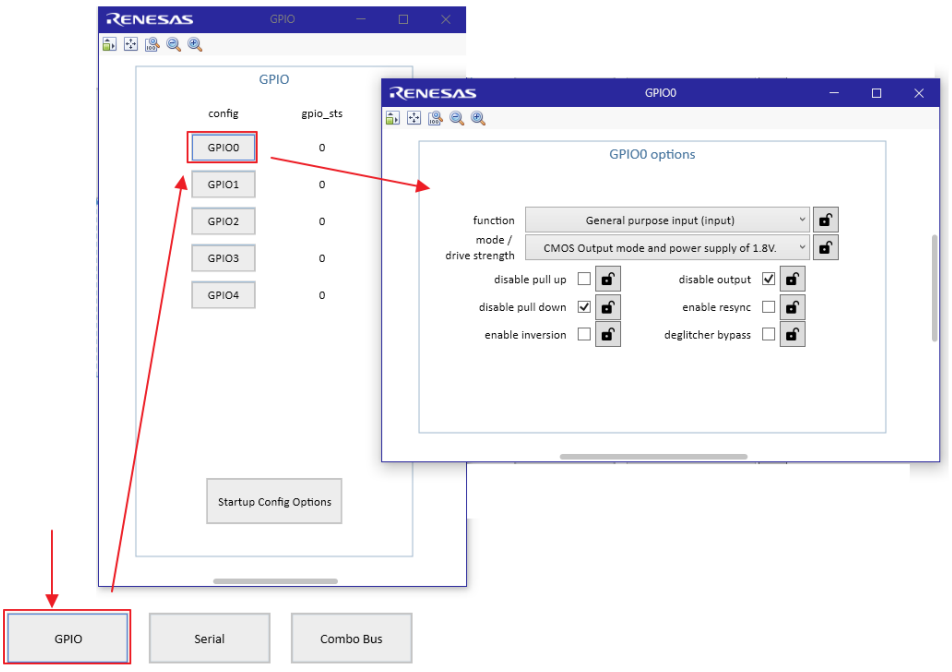

Figure 26. GPIO Block

7.9 Serial Block

The Serial Block displays settings for serial communication protocol, I^2C address selection, and SPI interface type.

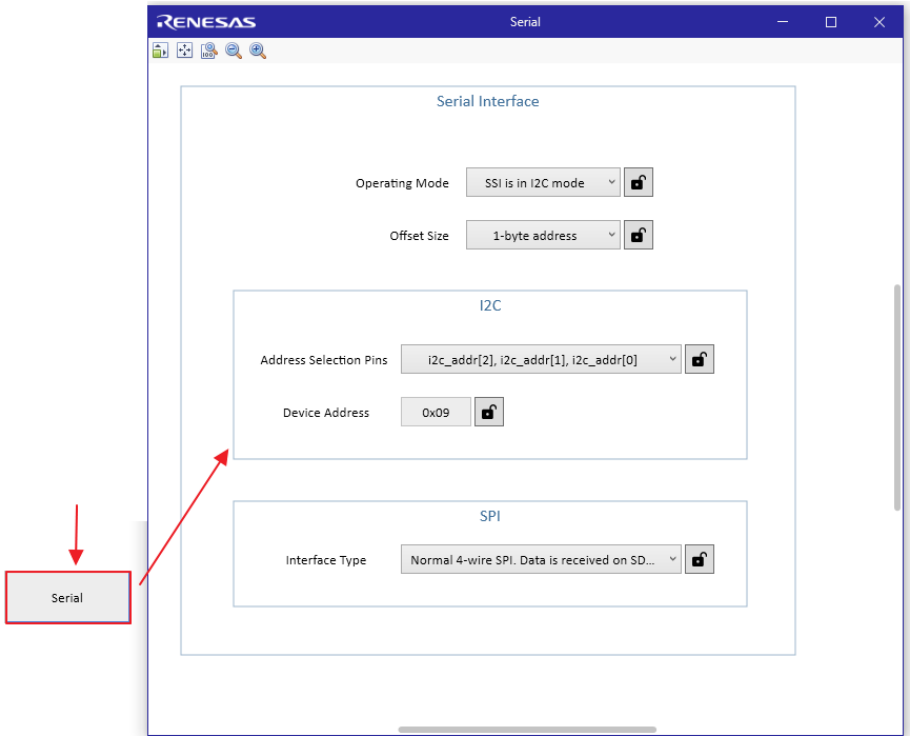

Figure 27. Serial Block

7.10 Combo Bus Block

The Combo Bus Block depicts the setup of the clock domains of the configuration.

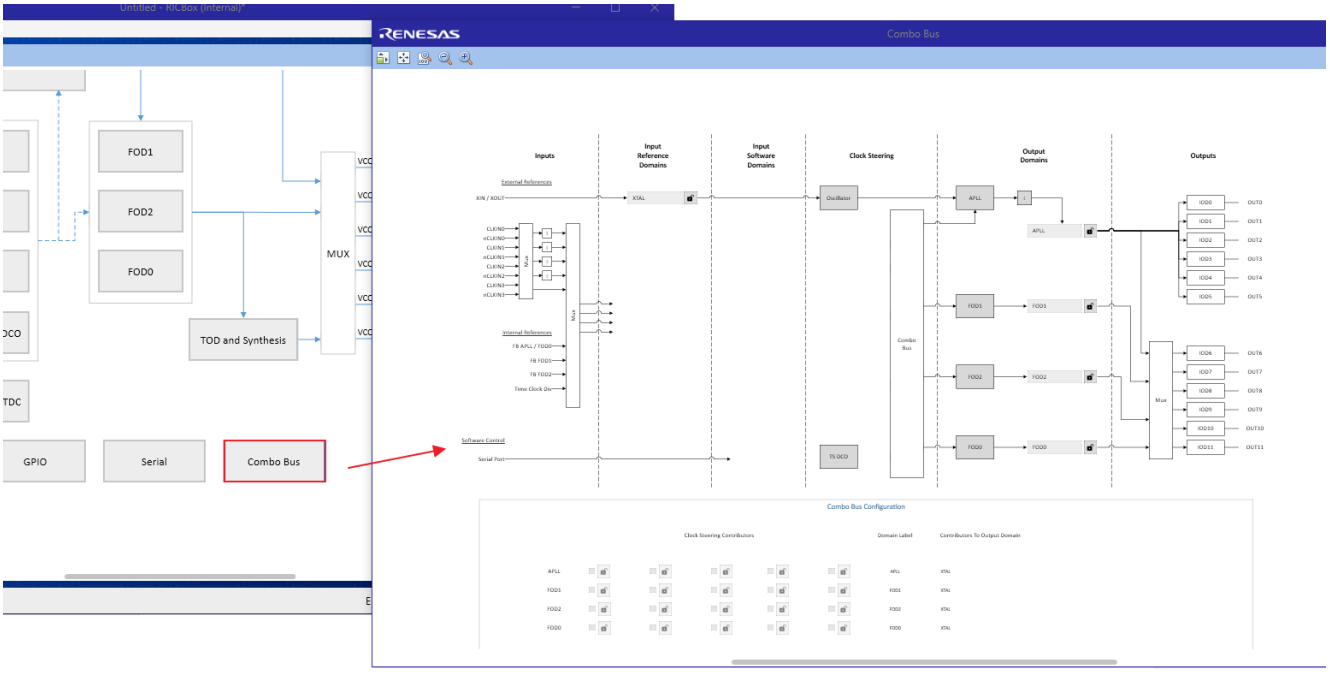

Figure 28. Combo Bus Block

The diagram at the top of the page shows the enabled input domains and how they are connected to the output domains moving to the right as shown in Figure 29.

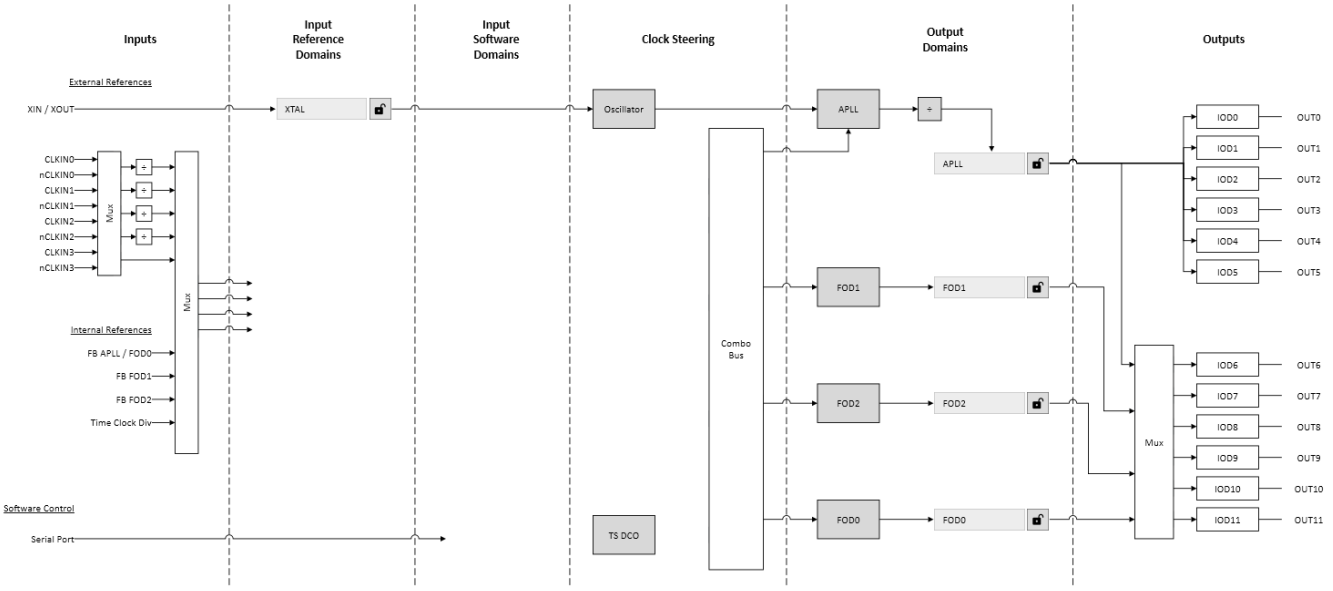

Figure 29. Combo Bus Block (Top)

Enabling additional DPLLs or DCOs adds more to the diagram. Label the input domains and output domains as needed for representation as shown in Figure 30. These labels do not change any registers in the device and are only used to clarify the input and output domains for the user.

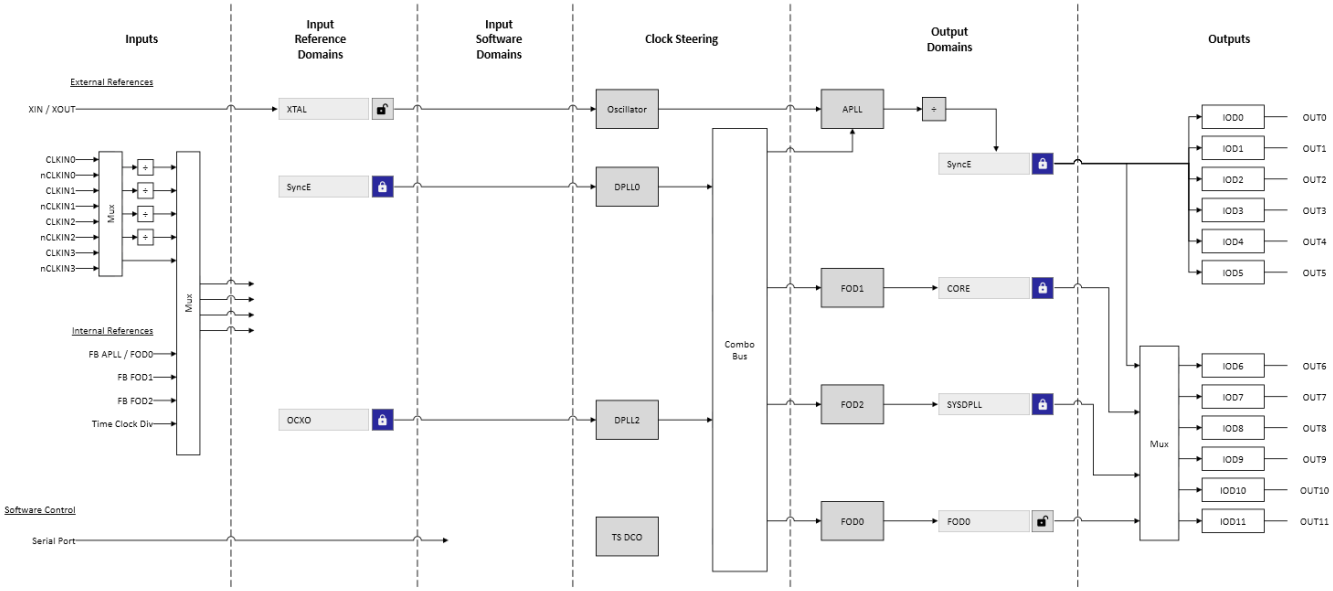

Figure 30. Combo Bus Block – Labeling Input and Output Domains

The bottom of the page shows a matrix layout of checkboxes (see Figure 31). The rows are labeled APLL, FOD0, FOD1, and FOD2 as output domains. The columns are for each DPLL or DCO that is enabled as clock steering contributors. Checking off any of these boxes will adjust device register settings to apply the frequency information from the clock steering contributor in the column to the domain in the row.

The labels at the far right of the matrix show how each domain is steered by its clock contributors. Click on the checkboxes to see the labels updated.

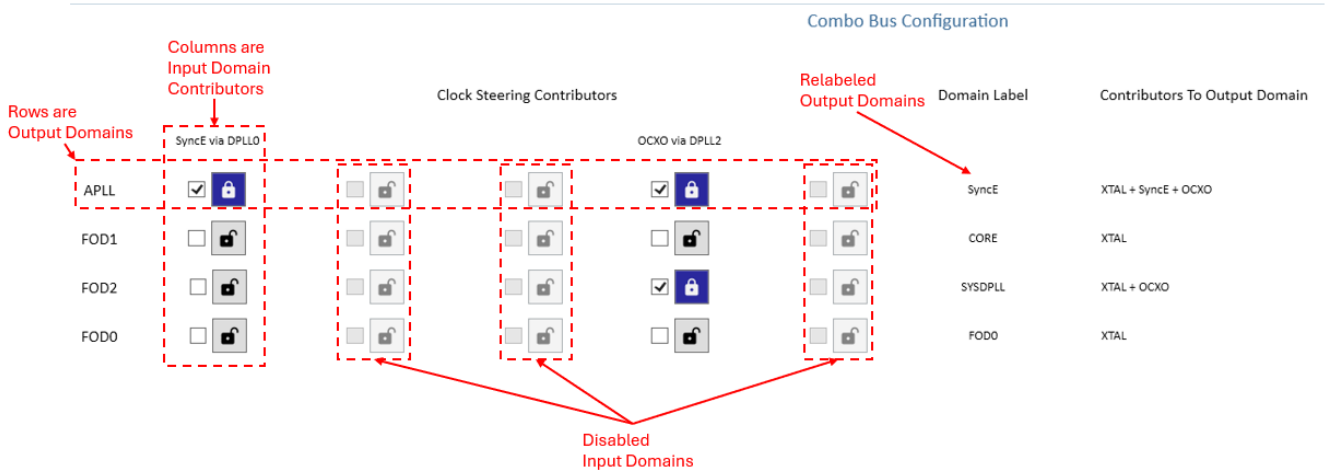

Figure 31. Combo Bus Block (Bottom)

The first row (APLL domain) is relabeled as the SyncE domain. The APLL domain has three input domain frequency offset contributors:

- XTAL by default
- SyncE via DPLL0
- OCXO via DPLL2

These contributors are listed in the final column of Figure 31. In general, the input domain frequency offset contributors are additive, which means a +6ppm offset from the XTAL, a -2ppm offset from the SyncE, and a -1ppm offset from the OCXO would yield a +3ppm total frequency offset at the output domain. However, while DPLL0 is locked, the output tracks the SyncE input domain (-2ppm) because a DPLL output always tracks its input. If DPLL0 is unlocked, the SyncE output will be the sum of the contribution from the XTAL and the OCXO. If both DPLL0 and DPLL2 are unlocked, the SyncE output will only have the XTAL contribution. SyncE uses the APLL domain to achieve the best jitter. The APLL domain avoids any muxes and FODs at the output.

The second row (FOD1) and fourth row (FOD0) are relabeled CORE and FOD0, respectively. Both output domains do not have any direct inputs. Their only input contributors are the XTAL. The device manages this by using the APLL domain but subtracting the SyncE and OCXO domains internally.

The third row (FOD2) is relabeled as the SYSDPLL domain. The FOD2 domain has two input domain frequency offset contributors:

- XTAL by default
- OCXO via DPLL2

The device manages this by using the APLL domain but subtracting the SyncE domain internally. While DPLL2 is locked, the output tracks the OCXO input domain. If DPLL2 is unlocked, the SYSDPLL output will only have the XTAL contribution.

Any of the three contributors for the APLL domain row can be unselected, except the XTAL. The XTAL contribution is always present by default. The three input domains, DPLL0_FB, DPLL1 and Time Sync DCO, are disabled and greyed out. If the configuration uses DPLL0_FB, DPLL1, or Time Sync DCO, those columns will become selectable.

7.11 SYSREF Block

The SYSREF Block allows the configuration of SYSREF pulse type, trigger settings, pulse/pause count, and defines what outputs are considered SYSREF signals.

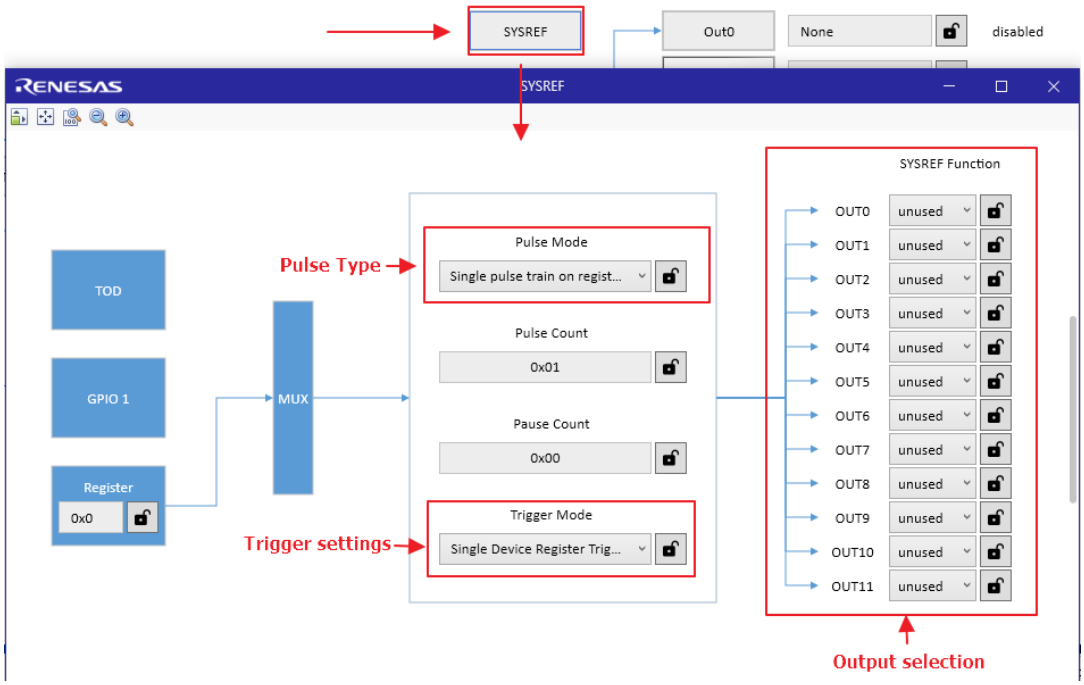

Figure 32. SYSREF Block

1. Set up a given output as either a SYSREF signal or device source, then select the trigger and pulse modes.

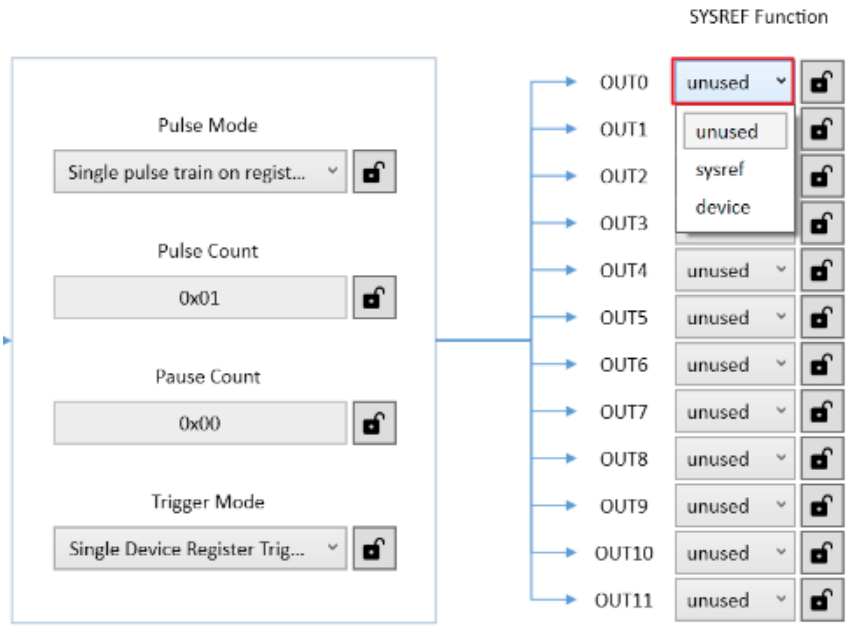

Figure 33. SYSREF Output Assignment

a. *Trigger Mode* – The source of the SYSREF trigger.

   i. Register – Write to the init_SYSREF bit using serial connection to trigger a SYSREF event.

   Note: For SYSREF configuration and control registers, see sections 4.9 of the relevant *RC3x Programming Guide*.

ii. GPIO – The SYSREF event triggers when GPIO1 sees an active input signal.

Note: Only GPIO1 can be programmed as an input to trigger a SYSREF event. No other GPIOs have this function.

iii. TOD – SYSREF is triggered with a TOD event.

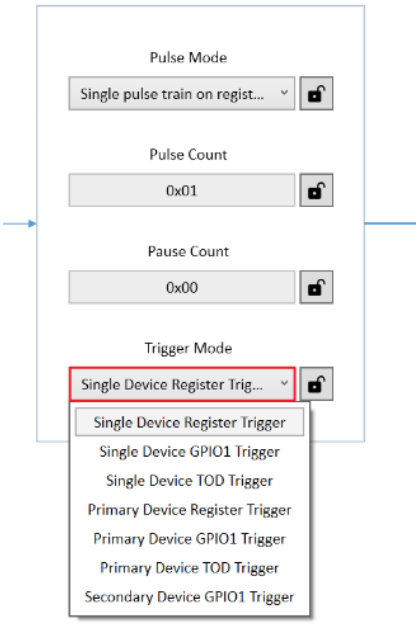

Figure 34. SYSREF Trigger Mode

b. *Pulse Mode* – The type of pulse/pause pattern generated by the SYSREF clock. Pulse mode differs between trigger types. When a register is used to trigger the SYSREF clock then pulse mode can be configured to:

i. Single pulse train – Only one pulse train is generated after the register trigger.

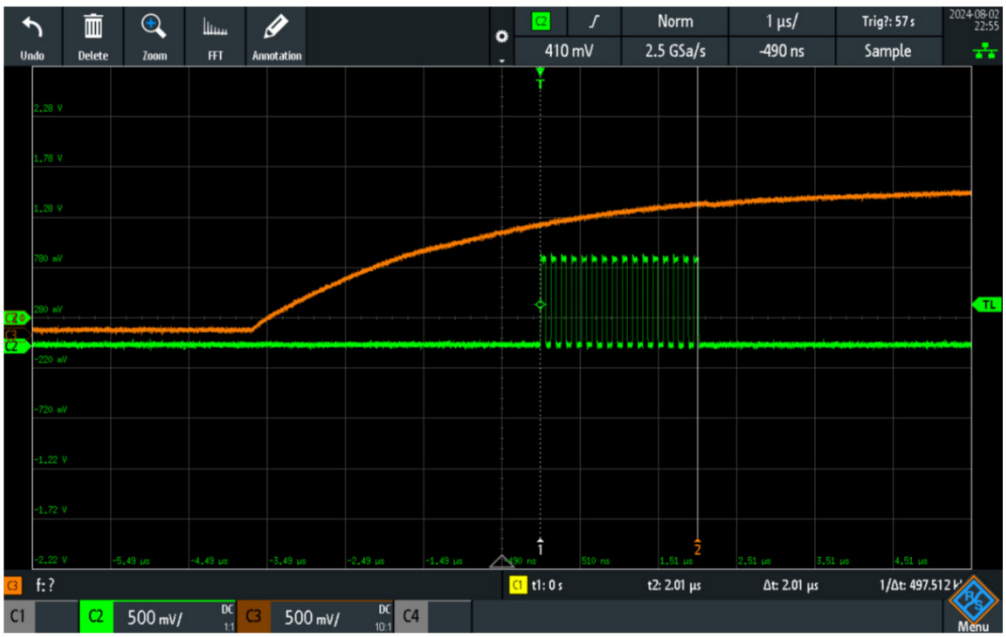

Figure 35. Single Pulse Train (0x10 Pulses) (7.68MHz (Green) and GPIO Trigger (Orange))

ii. Continuous pulse/pause train – A continuous train of pulses and pauses defined by the pulse and pause counts.

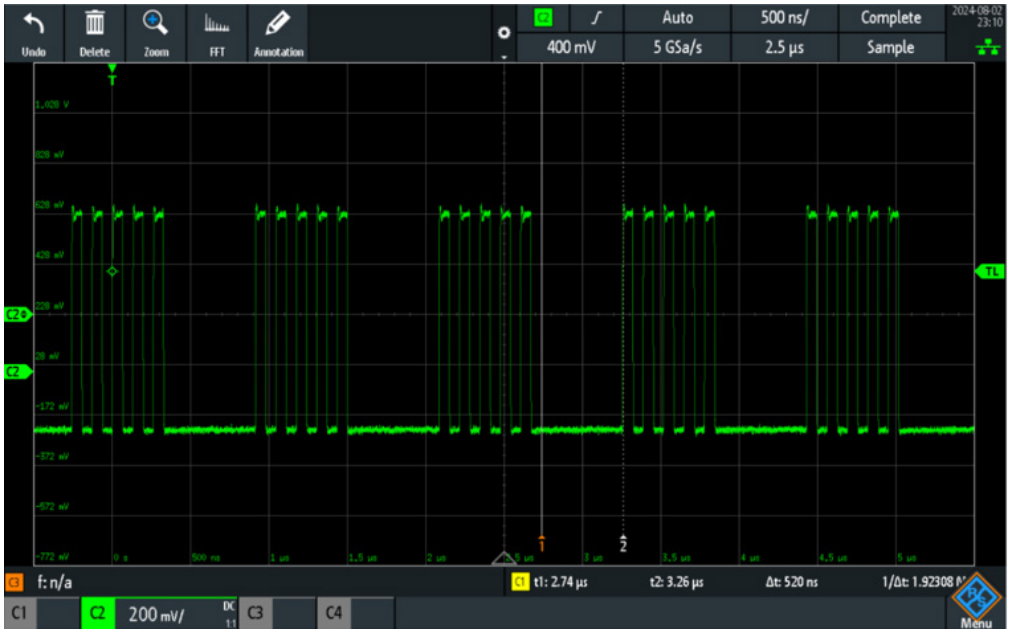

Figure 36. Continuous Pause/Pulse Train with 5 Pulses and 4 Pauses at 7.68MHz

iii. Continuous without pause – A continuous clock output until the end of the SYSREF event.

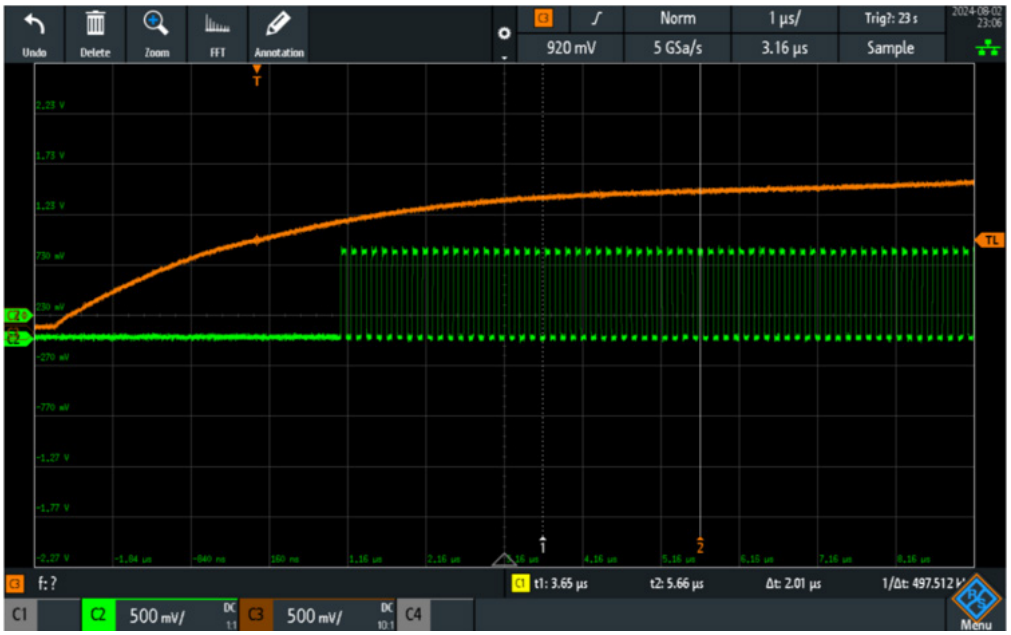

Figure 37. Continuous 7.68MHz Pulse (Green) with GPIO Dip Switch Trigger (Orange)

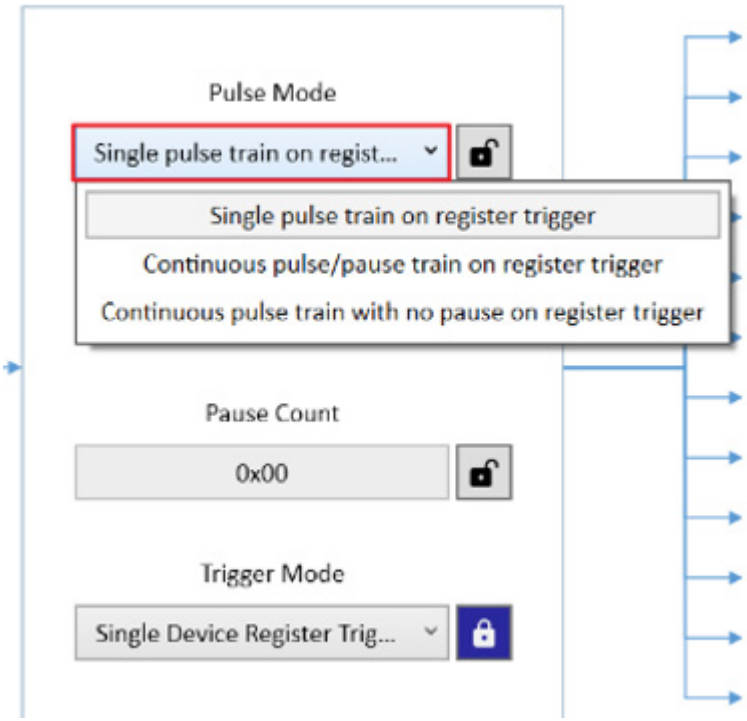

Figure 38. SYSREF Pulse Mode Register Trigger

If the SYSREF signal is triggered by GPIO or TOD, then the pulse mode can be continuous or single pulse train depending on the trigger edge.

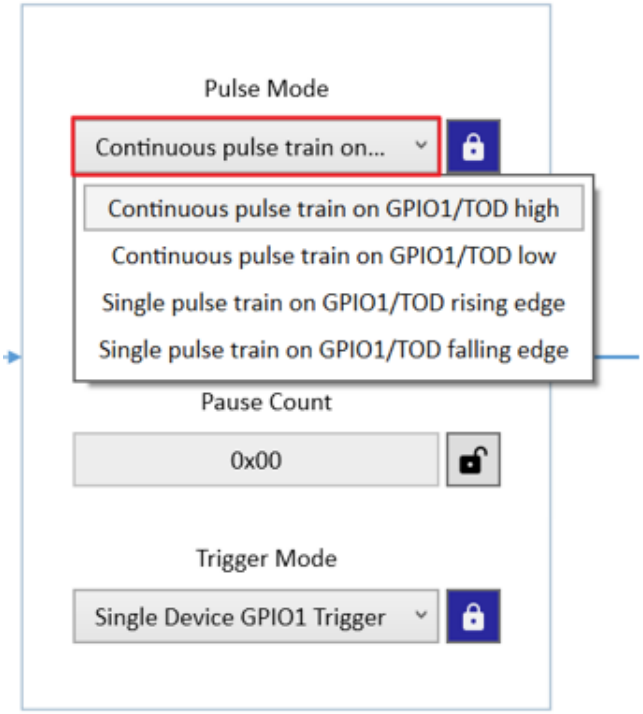

Figure 39. SYSREF Pulse Mode GPIO/TOD Trigger

Pulse count is the number of pulses in a pulse train. If single pulse train is selected, then the device will output the number of pulses denoted in pulse count before finishing the SYSREF event.

In continuous pulse/pause mode, the pulse count is the number of pulses that will be output before pausing. Then, the signal will pause for the number of pulses based on the pause count. The cycle is repeated until the sysref_init bit is set to 0.

Note: Only register trigger can be used for Continuous pulse/pause mode.

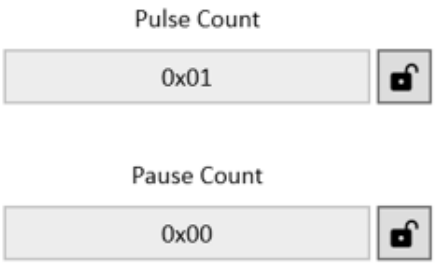

Figure 40. SYSREF Pulse and Pause Counts

When a GPIO is used as an input trigger, the GPIO settings must be configured. Newer versions of the RICBox plugin automatically configure GPIO1 as input when the trigger source is selected.

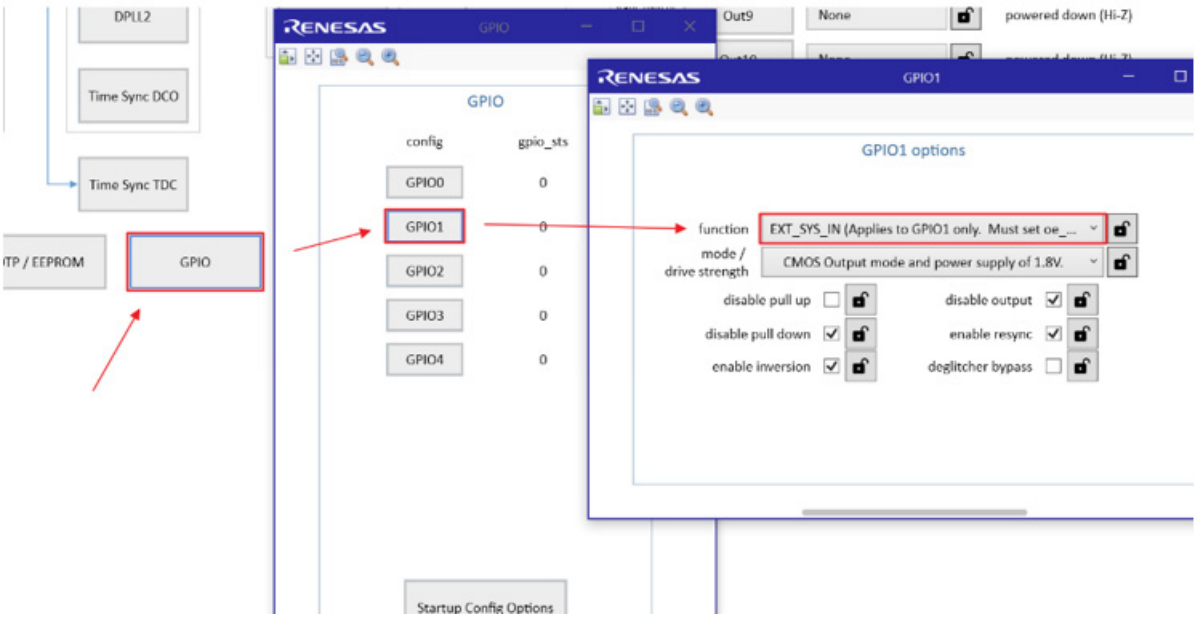

Figure 41. GPIO1 SYSREF EXT_SYS_IN

GPIO0 can be used as an external trigger output for a cascaded SYSREF signal between devices. Use the EXT_SYS_OUT setting to configure GPIO0 as SYSREF output.

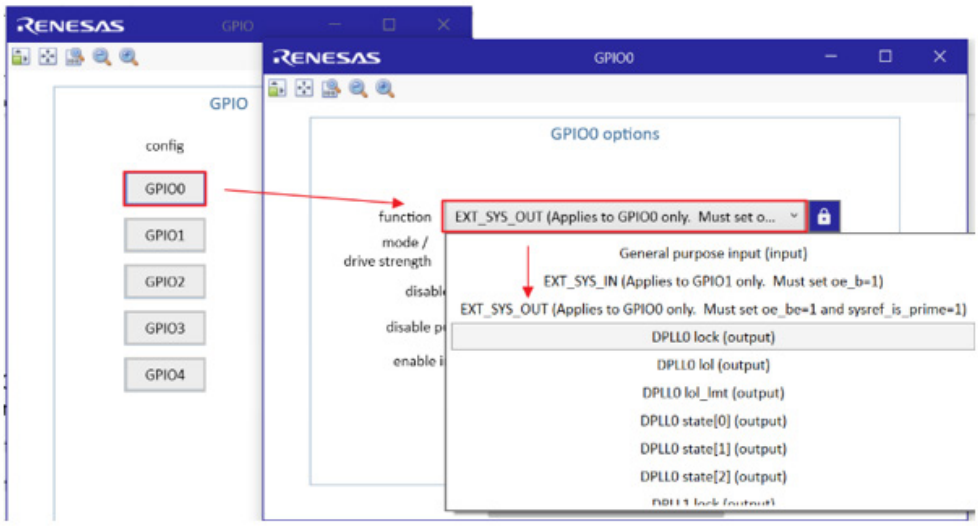

Figure 42. GPIO0 SYSREF EXT_SYS_OUT

When selecting the trigger source, there are options for primary and secondary sources. The primary source is the main device in the cascaded chain where secondary is receiving a trigger from primary device.

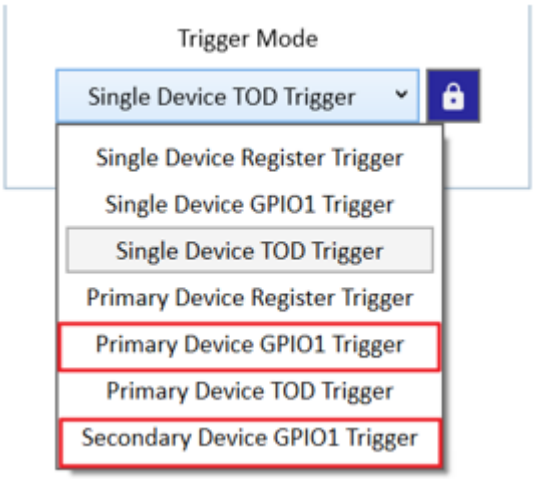

Figure 43. SYSREF Primary and Secondary Trigger Selections

Note: When any SYSREF event ends, wait at least 3 SYSREF clock periods before starting another event.

7.12 Time Sync TDC Block

1. Click the Time Sync TDC block in the main diagram.

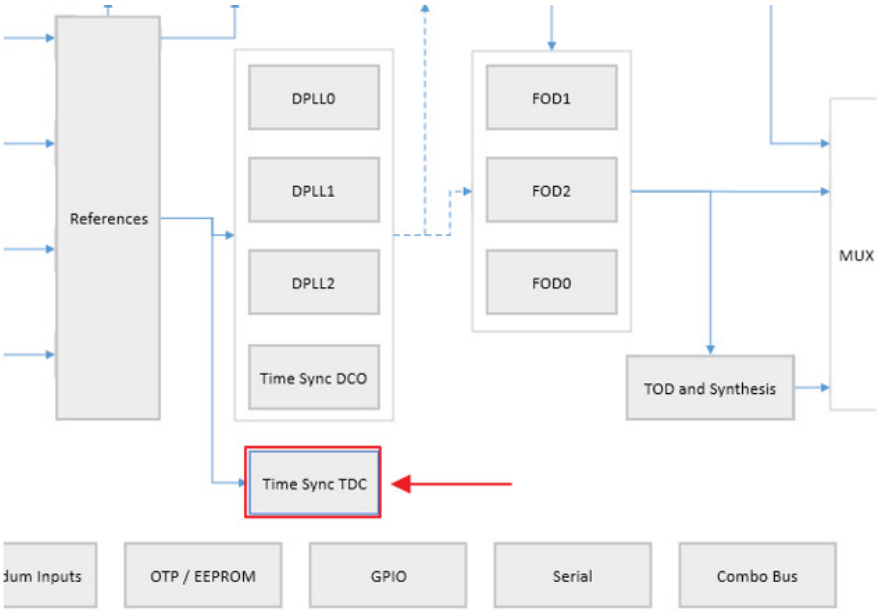

Figure 44. Time Sync TDC Block Location in the RICBox GUI

2. Select the Time Sync channel input clock source used for TDC coarse measurement.

   A FOD must be configured and enabled as Time Sync channel reference source for coarse measurement.

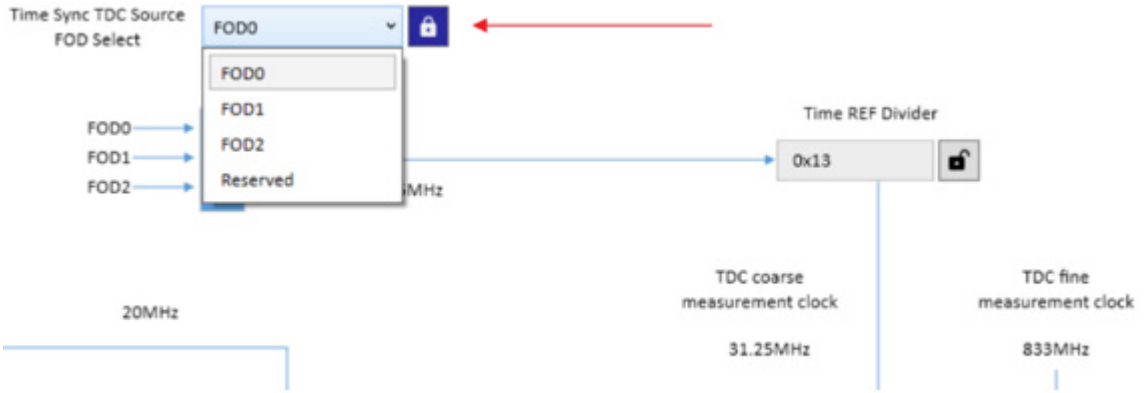

Figure 45. Time Sync TDC Source FOD Select

3. Enable Time Sync TDC.

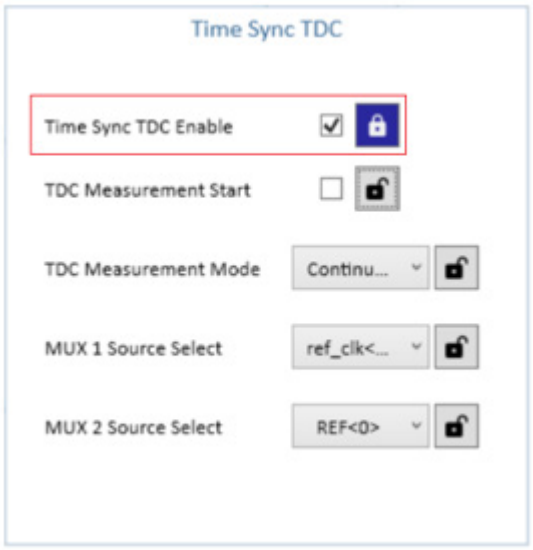

Figure 46. Time Sync TDC Enable Button

4. Select TDC measurement mode between one-shot and continuous.

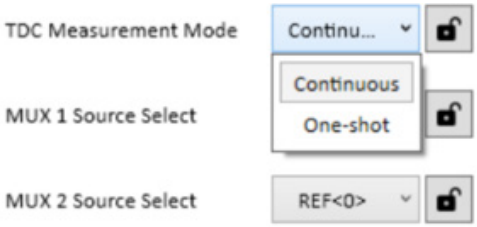

Figure 47. TDC Measurement Mode Select

5. Select input reference clocks to measure.
   - The input clocks must be the same frequency.
   - Ref_clk5 and ref_clk6 are dedicated reference input to the time sync TDC.

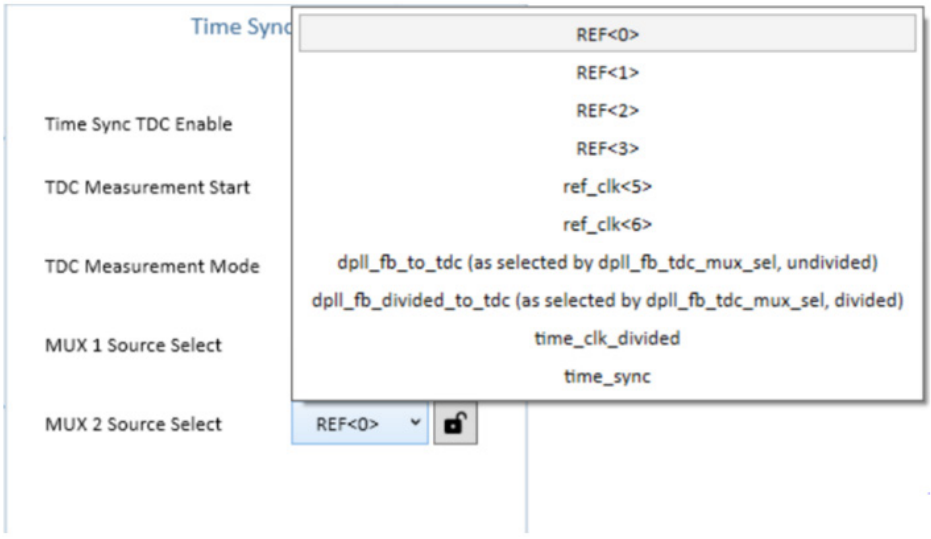

Figure 48. Time Sync TDC Reference Input Select

6. Connect to a device and program its registers with the “program” button. This step is not necessary if the program button has already been clicked prior to step 1.
7. Enable the input measurement.

Figure 49. TDC Measurement Start Button

8. Open the RICBox command line interface by going to tools → CLI.

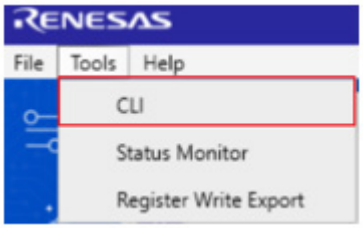

Figure 50. RICBox Command Line Interface Location

   a. Type “write TOP.TIME_SYNC_TDC.TDC_FIFO_READ_REQ.fifo_read_req 1” to load measured values to the fine and coarse value registers.
   b. Type “read TOP.TIME_SYNC_TDC.TDC_FIFO_READ.fifo_read_val_fine” to read fine measurement value.

```
> write TOP.TIME_SYNC_TDC.TDC_FIFO_READ_REQ.fifo_read_req 1
Wrote 1 byte(s) to offset 0xB2F
> read TOP.TIME_SYNC_TDC.TDC_FIFO_READ.fifo_read_val_fine
0x1ADD
```

Figure 51. RICBox Command Line Interface Register Write and Read Example

   c. Type “read TOP.TIME_SYNC_TDC.TDC_FIFO_READ.fifo_read_val_coarse” to read the coarse measurement value.

Once coarse and fine values have been read, the offset between the two input clocks can be calculated as:

$$Offset = \left(\frac{tdc\_coarse\_meas}{F_{TDCcoarse}} \times\right) + \left(\frac{tdc\_fine\_meas}{62 \times F_{TDCfine}}\right)$$

Where:

- tdc_coarse_meas is read from TOP.TIME_SYNC_TDC.TDC_FIFO_READ.fifo_read_val_coarse; this value is **signed**.
- tdc_fine_meas is read from TOP.TIME_SYNC_TDC.TDC_FIFO_READ.fifo_read_val_fine; this value is **signed**.
- $F_{TDCcoarse}$ is TDC coarse measurement clock frequency.

- $F_{TDCfine}$ is the TDC fine measurement clock frequency.

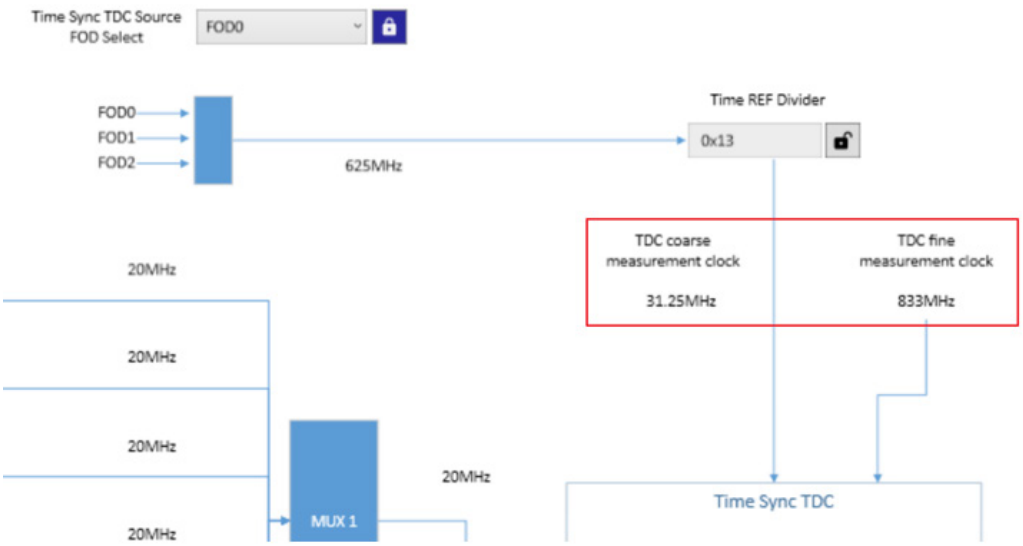

Figure 52. TDC Coarse Measurement Clock and TDC Fine Measurement Clock

8. Device Connection

Device connection can be achieved through the bottom right corner of every page.

1. To connect one of the Renesas evaluation boards, ensure the device is powered and connected to the working computer.
2. Click the **Not Connected** button in the corner of the screen. This will lead to a small pop-out page.
3. Click the connect symbol in the corner of the page to establish a connection to the device.

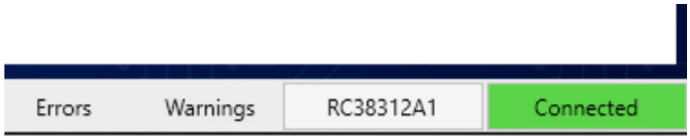

Figure 53. Device Connection

Note: Section 4 of the RICBox Software Manual has more information about device connection features.

9. Common Configurable Settings

9.1 Saving/Programming EEPROM Images

1. Establish a connection to a device with the EEPROM attached.

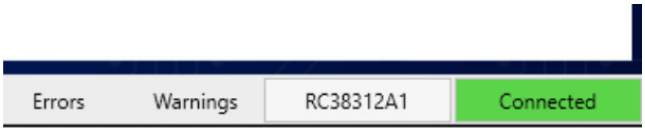

Figure 54. Device Connection

2. Go to the OTP/EEPROM section of the block diagram.
3. Use the configuration type dropdown menu to select **SingleConfig**.
4. Populate the SingleConfig drop-down menu with the configuration name that is being programmed to the EEPROM.
5. Click the program button in the lower corner of the page.

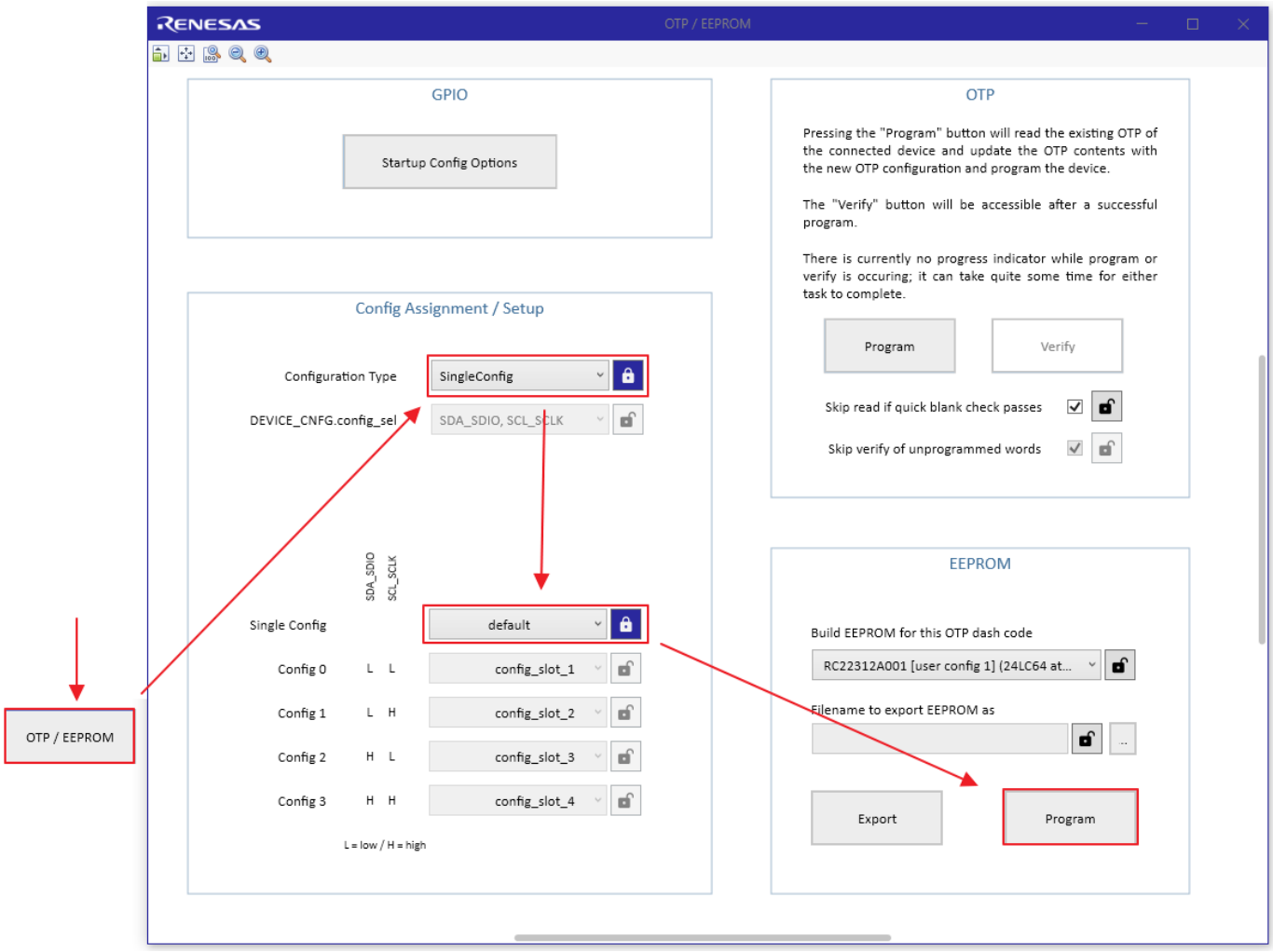

Figure 55. Programming a Connected EEPROM Device

Note: The Adding Configurations to a Settings File section highlights configuration naming. Section 13 of the RICBox Software Manual discusses multiple configuration support.

Note: FemtoClock3 software only supports programming one configuration into EEPROM at a time.

6. Choose the save location by clicking the button next to the EEPROM filename entry box.
7. Click the Export button to save the EEPROM image to the specified location.

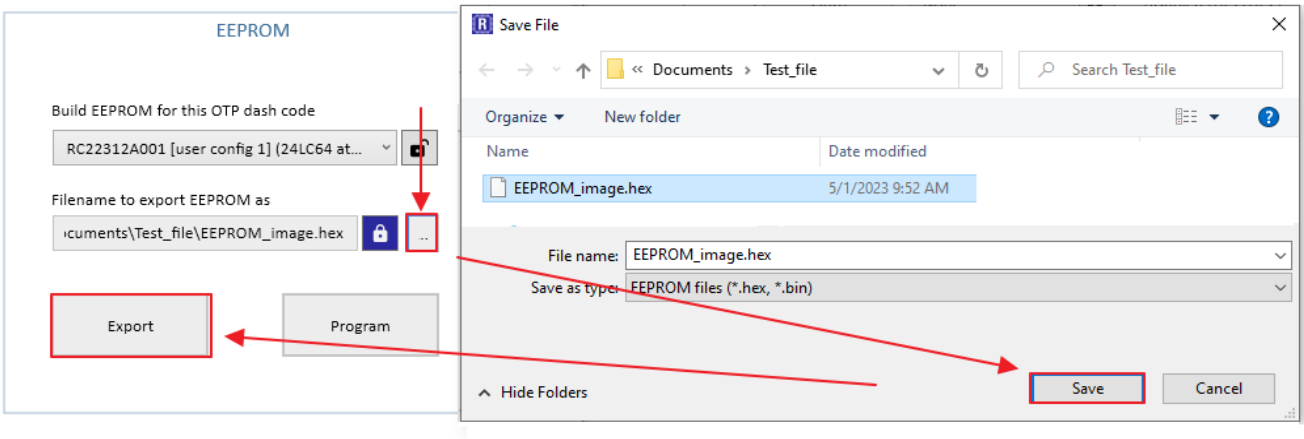

Figure 56. Saving EEPROM Image

Note: Ensure to specify the file extension as ".bin" or ".hex" when naming the file.

10. Revision History

Revision	Date	Description
1.02	May 6, 2025	Added section 7.10.
1.01	Nov 1, 2024	▪ Updated "OSCI Block" with new information and photo ▪ Updated "SYSREF Block" ▪ Added "Time Sync TDC Block"
1.00	Mar 12, 2024	Initial release.

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