RICBox GUI Software for FemtoClock4

Introduction

This document explains how to use the Renesas IC Toolbox (RICBox) software to configure and control FemtoClock4 devices. For general RICBox instructions, see the RICBox Software Manual.

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1. Installation and Setup

Ensure that the latest version of the Renesas IC Toolbox (RICBox) software is installed. New versions are released frequently and can provide a better experience with new functionality. The RICBox software can be installed directly from the RICbox webpage on the Renesas website.

Note: Both RICBox software and FemtoClock4 device plugin must be installed to access the user interface. If the device is not listed in the RICBox plugin list, then manual installation is required. For instructions on how to install the latest version of RICBox, device plugins, and maintain updates, see sections 1 and 11 of the RICBox Software Manual.

2. Loading and Creating Configurations

2.1 Creating a new Configuration

1. Start > RICBox
2. Click Create new project.

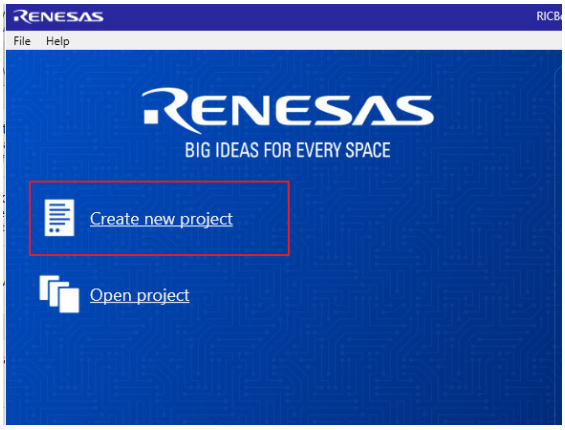


Figure 1. Open New Project in RICBox

3. Use the **Select a Product Family** box to choose the “FemtoClock4” devices.
4. Select the variant being evaluated and click **OK**. In this example, RC38616A is used.

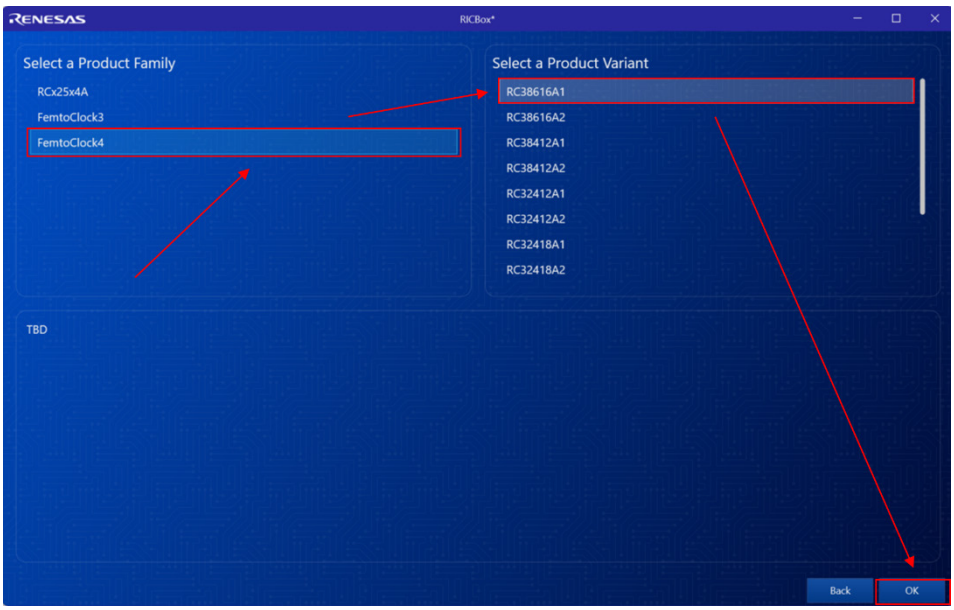


Figure 2. Selecting RC38616A Device GUI in RICBox

2.2 Loading a Settings File

Loading a settings file is like creating a new one.

1. To load an existing settings file, click on the **Browse** button just after opening the RICBox software. This will take the user to a file browser.

   Note: Recently used settings files are under the “Recent Files” section.

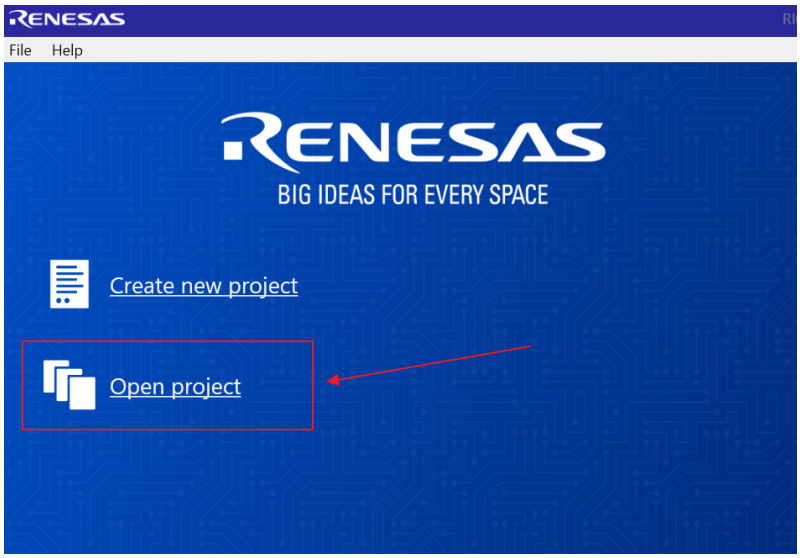


Figure 3. Open Existing Project

2. Navigate to the directory that stores the settings file and select it. RICBox settings files have the file type ‘**.rbs**’.

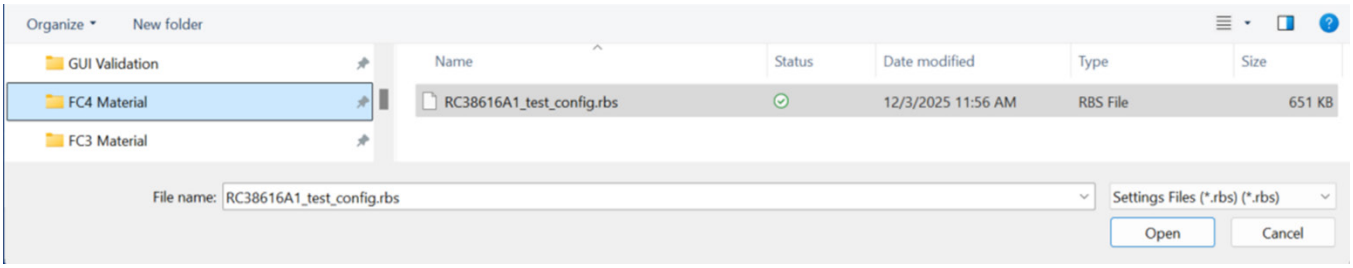


Figure 4. Select .rbs File

2.3 Adding Configurations to a Settings File

More than one device configuration can be created at a time. Different configurations can hold differing device settings but still be saved to the same RICBox settings file (.rbs).

1. In the lower right corner of a plugin GUI click on the part number box to view the configuration selection drop-down menu.

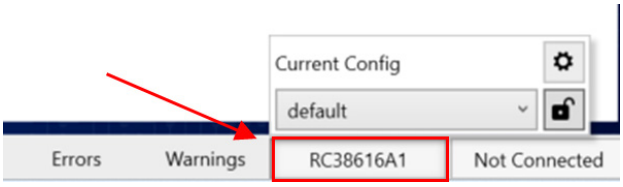


Figure 5. Configuration Menu

Use this menu to change the currently active configuration. The initial configuration is always labeled *default*.

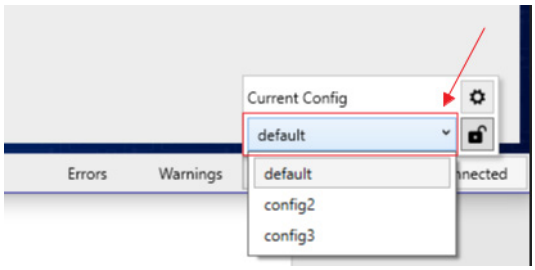


Figure 6. Configuration Selection

2. Click on the settings button to view the configurations pop-up menu.

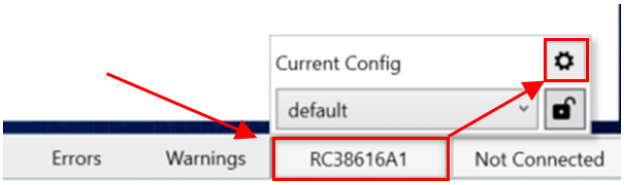


Figure 7. Configuration Settings

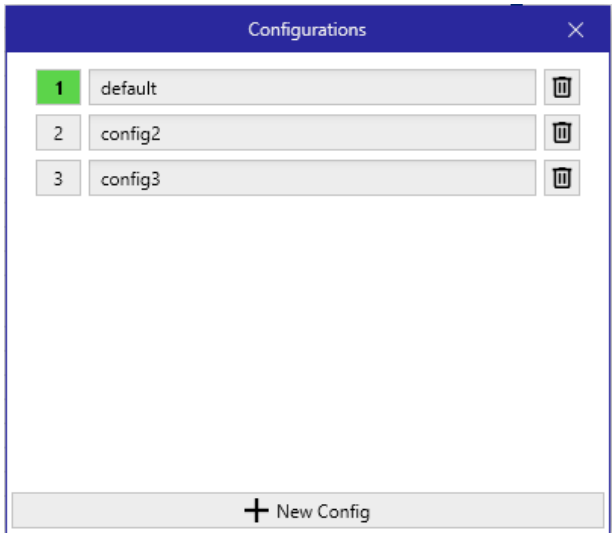


Figure 8. Configurations Pop-up Menu

3. Click on the numbers to change the currently active configuration. Green is the active configuration.

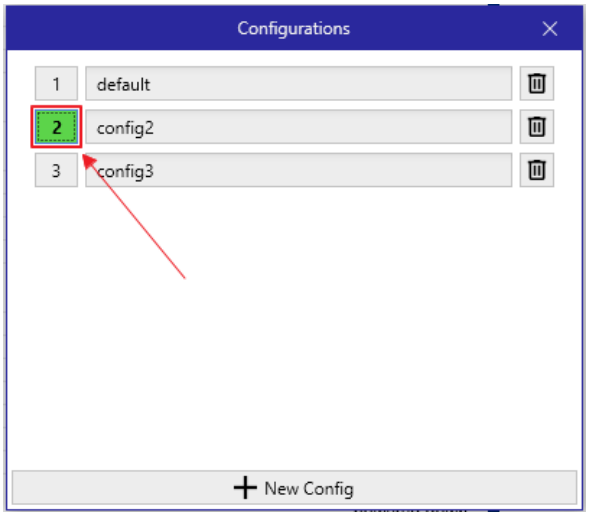


Figure 9. Currently Active Configuration

3. Side Panel Buttons

The side panel consists of four separate buttons. Each button opens a separate page. Each page has a unique view, allowing the configuration of the device from different perspectives.

- **Overview** button opens the device overview page.
- **Configuration** button displays the register settings in a readable text format with a search engine.
- **Register** button shows a graphic of the registers in the device.
- **Block Diagram** button opens a configurable block diagram view.

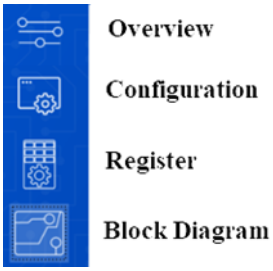


Figure 10. Side Panel Buttons

4. Control Panel (Device Overview)

The control panel view displays an overview page depicting the major settings for the device. This page can be used as an important reference for the overall device configuration.



RC38616A1	2.0.0.dev3403804+2484ea8c
Settings	
Dash Code	
Inputs	
XIN	None
REF_CLK	68MHz
CLKIN0	None
(nCLKIN0) CLKIN4	None
CLKIN1	None
(nCLKIN1) CLKIN5	None
CLKIN2	None
(nCLKIN2) CLKIN6	None
CLKIN3	None
(nCLKIN3) CLKIN7	None
CLKIN8	None
CLKIN9	None
CLKIN10	None
SysClock	
Quad sys clock	250MHz
Outputs	
OUT0	powered down
OUT1	powered down
OUT2	powered down
OUT3	powered down
OUT4	powered down
OUT5	powered down
OUT6	powered down
OUT7	powered down
OUT8	powered down
OUT9	powered down
OUT10	powered down
OUT11	powered down
OUT12	powered down
OUT13	powered down
OUT14	powered down
OUT15	powered down
OUT16	powered down
OUT17	powered down
APLL	
APLL Frequency	10GHz (0.0058ppt from goal of 10GHz)
Divider	~147.0588
Combo bus contributors	FFO = REF
Loop Bandwidth	~509.23kHz (1.846% from goal of 500kHz)
Phase Margin	~63.2349°
FOD0	
Enabled	no
FOD1	
Enabled	no
FOD2	
Enabled	no

Figure 11. Control Panel (Device Overview)

5. Configuration View

Configuration view enables easy movement through register settings via the tabs at the top of the page. Each section has all the critical registers and data fields listed to configure the device block.

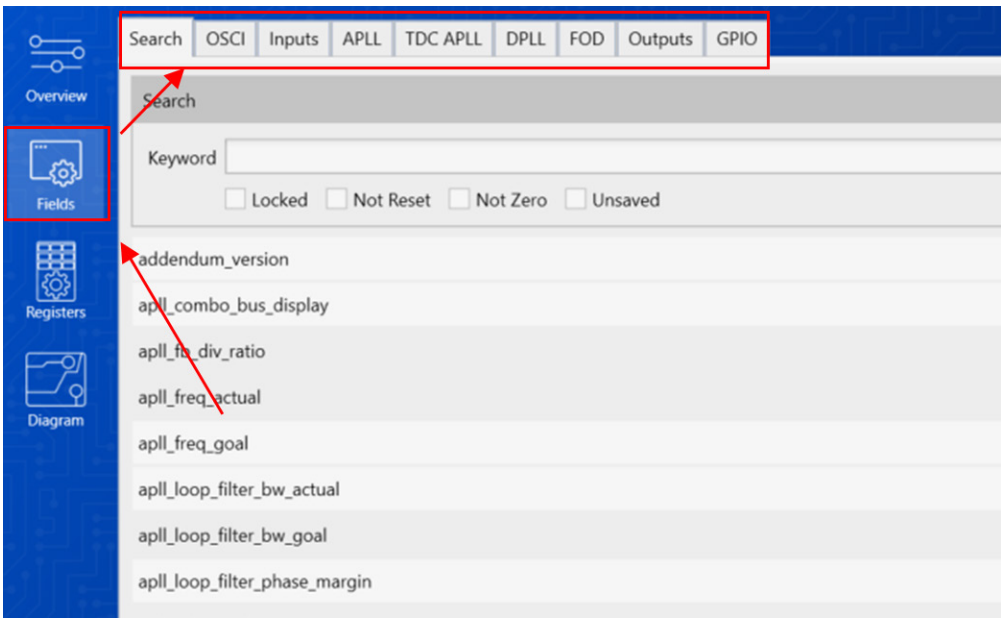


Figure 12. Configuration View

The search tab provides access to the configurable fields through a search bar. The search engine can be used to find any specific configurable field.

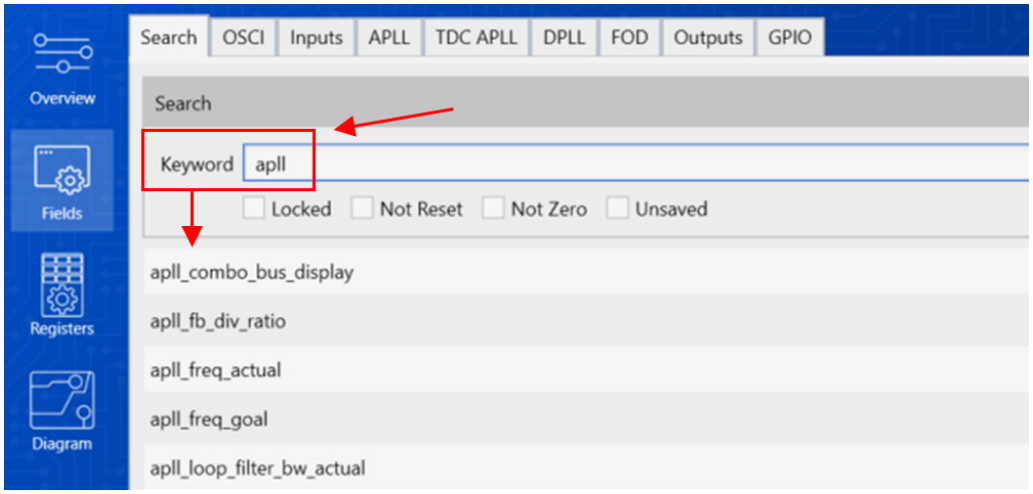


Figure 13. Search for Registers

6. Register View

The register view shows a graphical diagram of the registers and enables reading or writing any of the individual registers. By clicking on the individual register block, the given registers for that block will appear to the right. They can either be adjusted by writing directly to the diagram or entering values into the data fields on the right.

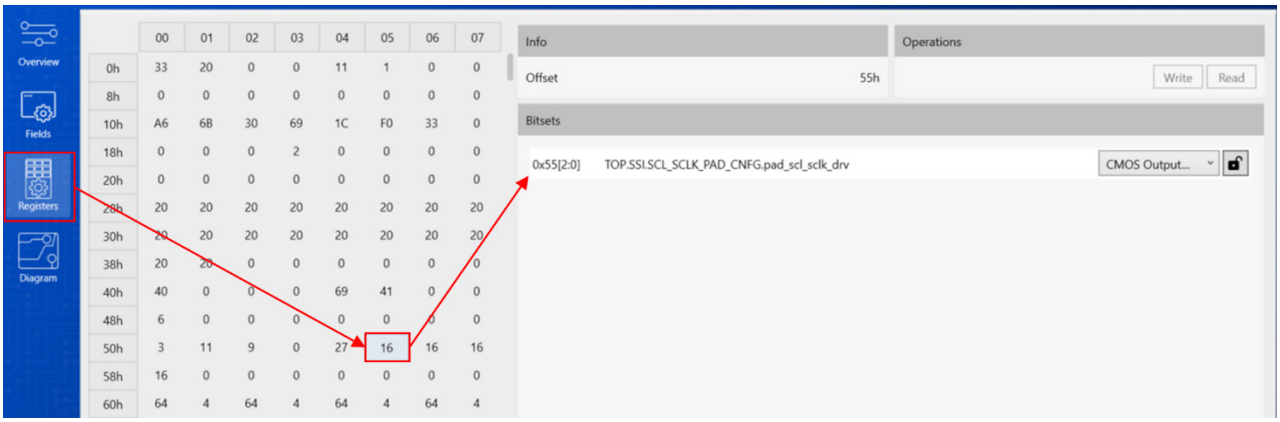


Figure 14. Register View

7. Block Diagram View

The Block Diagram view shows the datasheet representation of the FemtoClock4 devices. The main diagram allows setting the output frequency, setting the XIN frequency, setting the input frequencies, and viewing the output frequency estimate. Each block has its own pop-out page. This can be accessed by clicking on the block.

Note: Grey blocks can be clicked to access additional menus. White and blue shaded blocks are inaccessible.

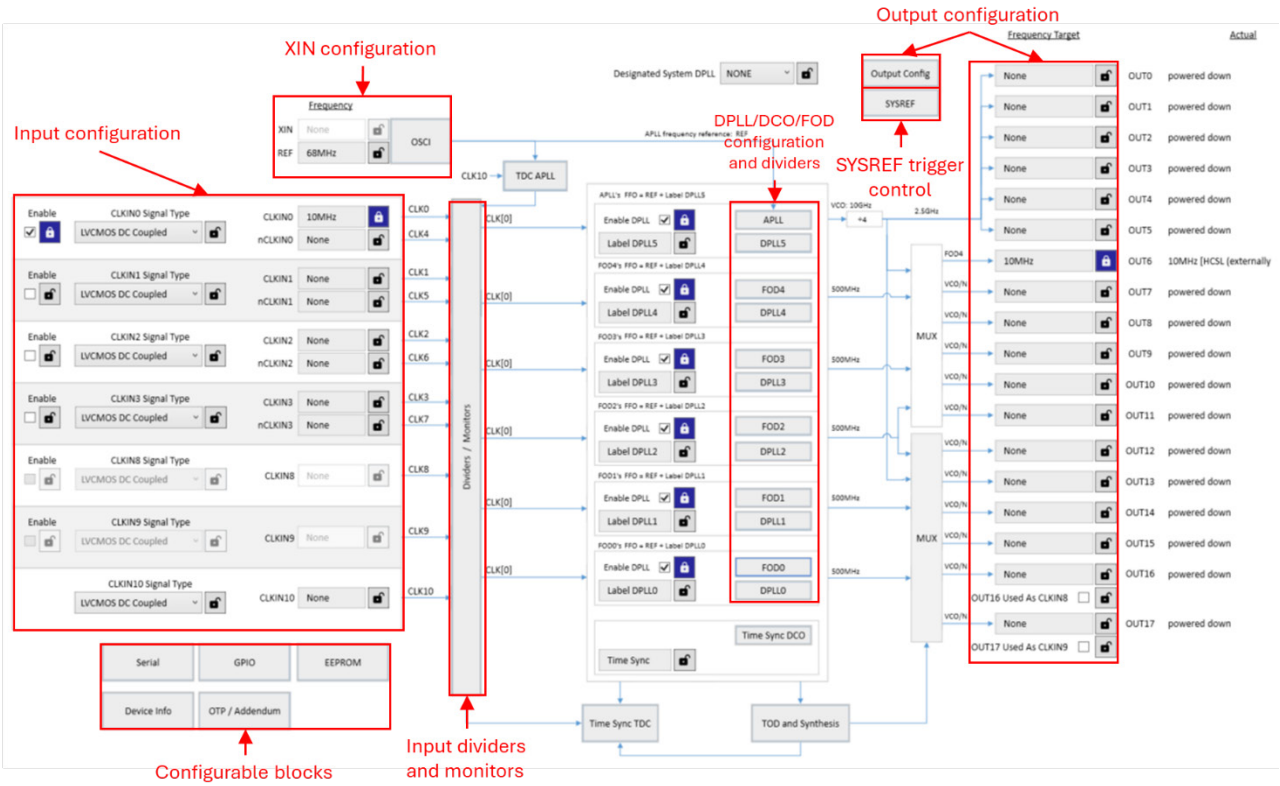


Figure 15. Main Block Diagram

7.1 OSCI Block

The OSCI block can be used to control the crystal frequency and the input capacitance. The GUI assumes a default value of 5.5pF load capacitance on each leg as a combination of fixed internal and PCB stray capacitance. Adjusting for a higher value will adjust the internal tuning cap settings.

For more information about load capacitance for FemtoClock4, see the “Load Capacitance” section of the application note, *Choosing the Correct Crystal or XO for FemtoClock 3 and FemtoClock 3 Wireless*.

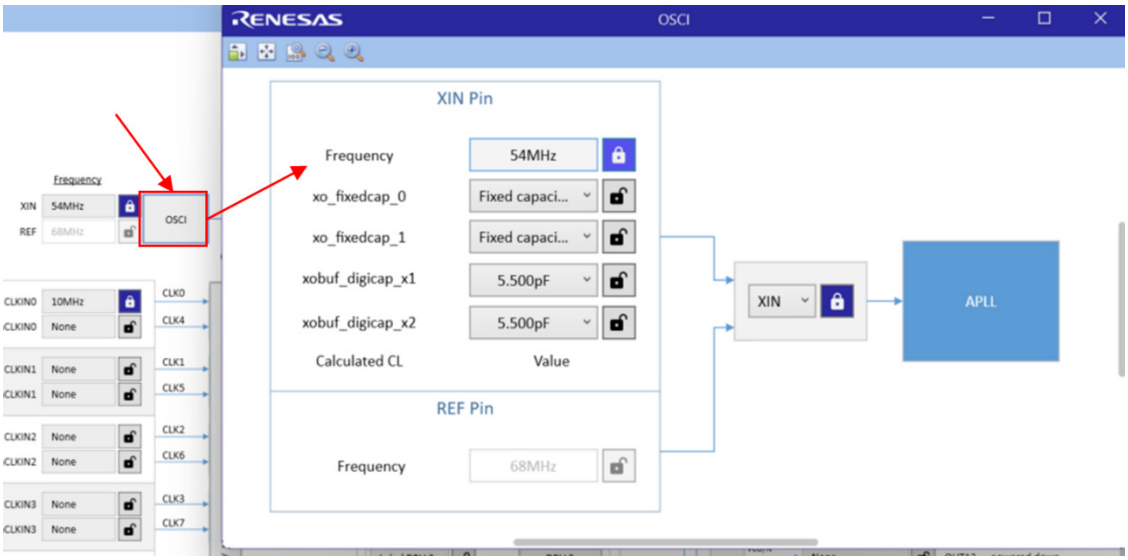


Figure 16. OSCI Block

7.2 APLL Block

The APLL block gives access to the crystal frequency, VCO frequency, low pass filter (LPF) resistor, and feedback divider. The feedback divider is automatically calculated by the software when the VCO frequency and crystal frequency are set.

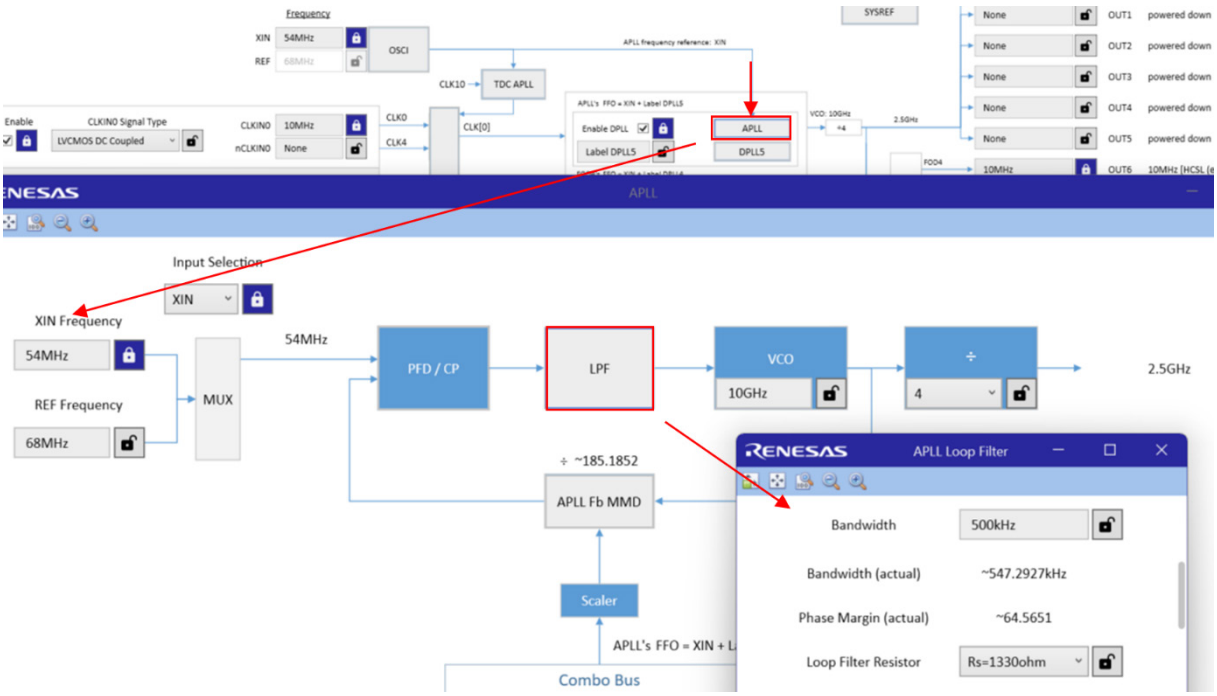


Figure 17. APLL Block

7.3 Outputs Block

The Output Block consists of the output reference selection, integer output divider (IOD), and output signal type selection.

Output references can be selected between FODs and VCO/N. This indicates the input frequency that is divided down by the IOD. The input reference is displayed on the main diagram.

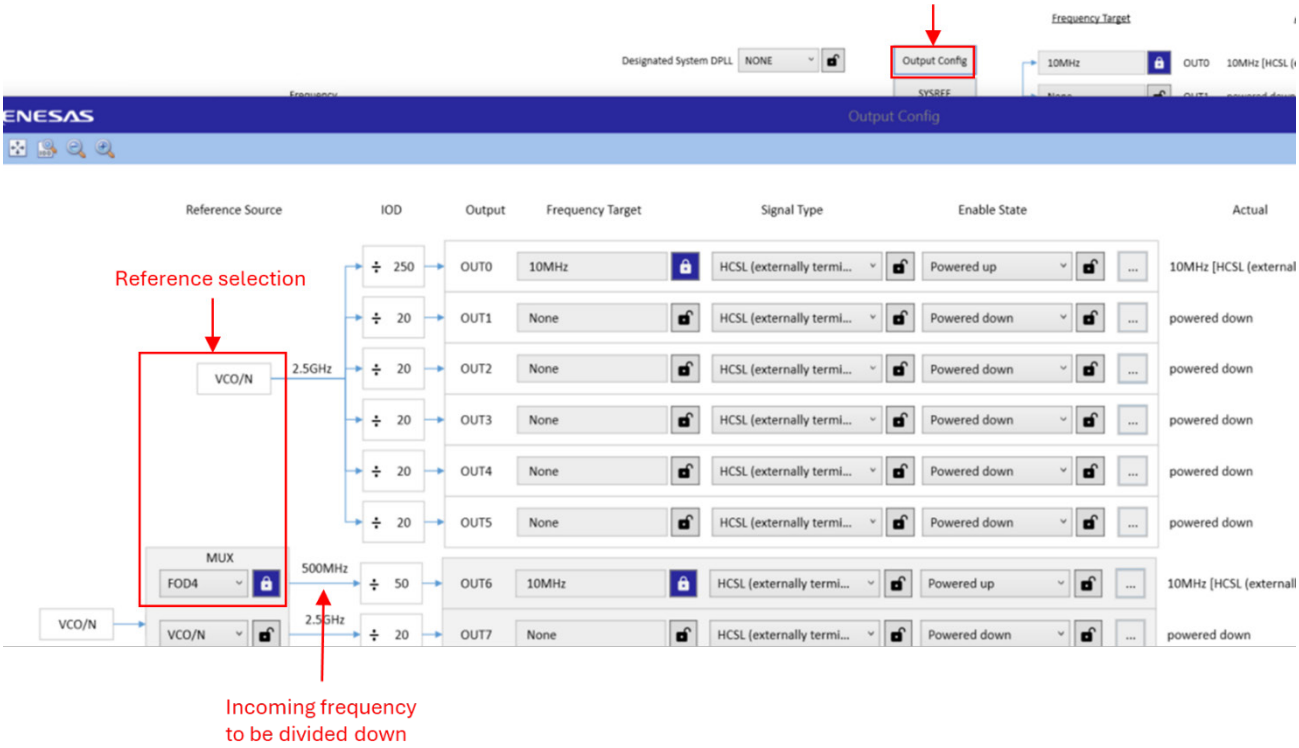


Figure 18. Outputs Block

Note: Out0 to Out5 can only reference VCO/N.

Output frequency can range between DC to 2.5GHz for differential signals and DC to 250MHz for single-ended signals. Output type can be selected between LVDS, HCSL, and CML. Outputs 12–17 can support LVCMOS.

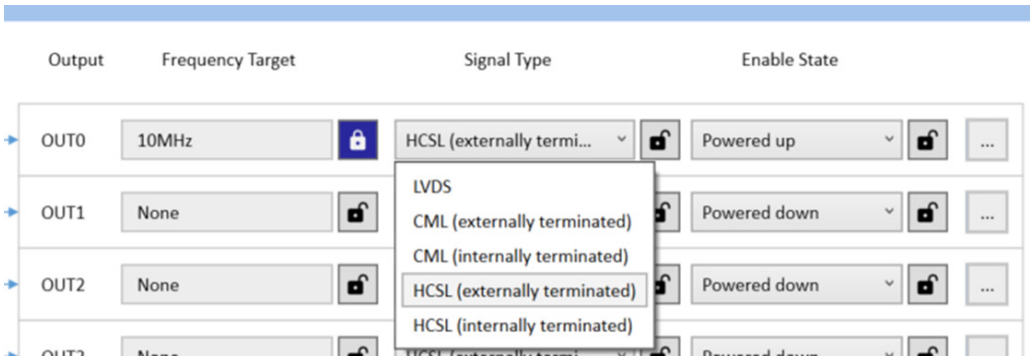


Figure 19. Output Signal Type Selection

The Advanced Block allows for configuring the terminations and voltage/amplitude settings. The OE Source Select dropdown menu chooses how the output enable is controlled, either through GPIO or register setting.

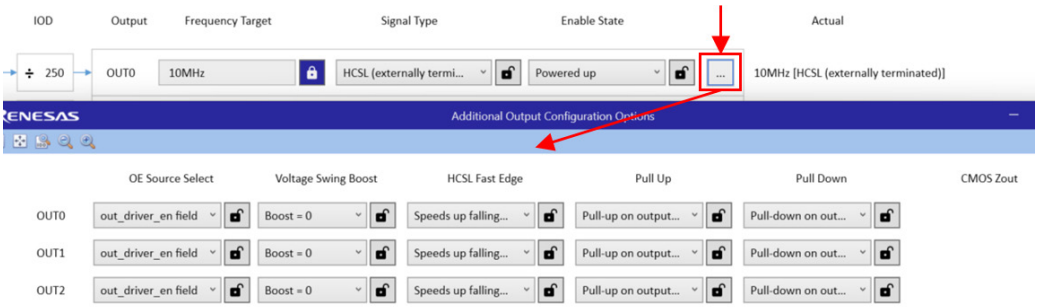


Figure 20. Output Signal Advanced Settings

7.4 FOD Block

The FOD block is used to control the fraction output dividers. The page shows settings for FOD output frequency, FOD mode, and the fractional output divider.

The FOD input reference is the VCO frequency. FOD output frequency ranges from 120MHz to 833MHz. The divider is automatically calculated by the software when the FOD frequency is set.

The FOD block also contains the input contributors to the block, as shown in the Combo Bus section. Each additional checkmark introduces a new contributor to the FOD block.

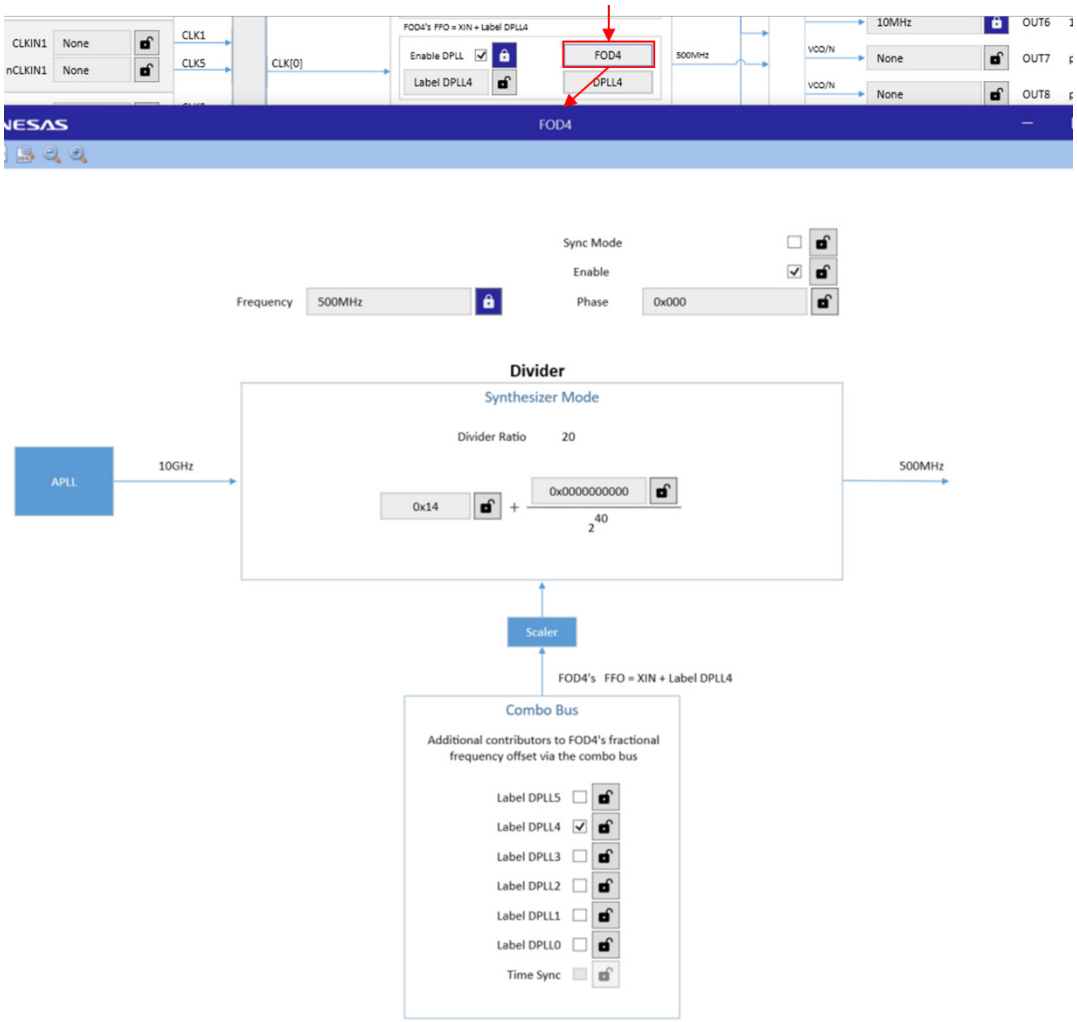


Figure 21. FOD Block

7.5 CLKIN Inputs Block

The **CLKIN**x block allows the control of the input signal type selection, frequency, and AC-coupling.

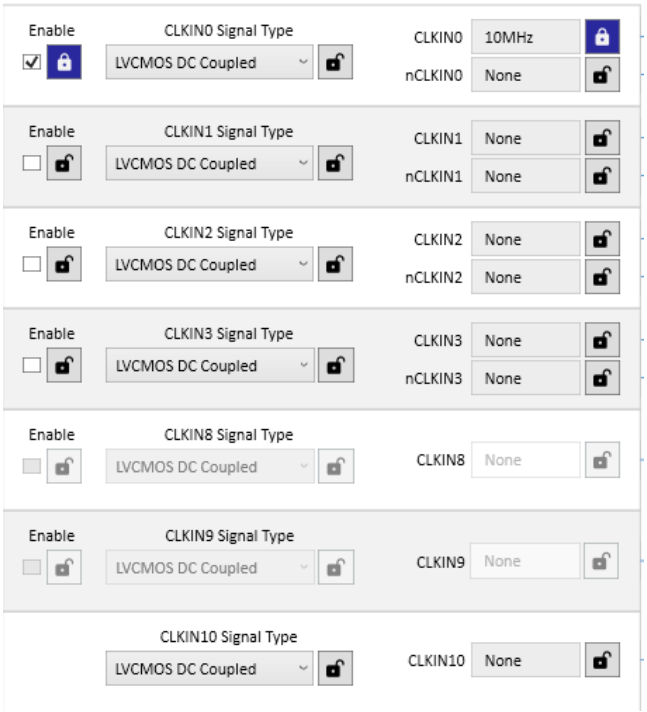


Figure 22. CLKIN Block

7.6 Input Dividers and Monitors

References must be divided down below 80MHz for the DPLL to lock to them. The input reference divider is accessible through the Input Dividers block. Clock frequency monitors are available through the Frequency Monitors block.

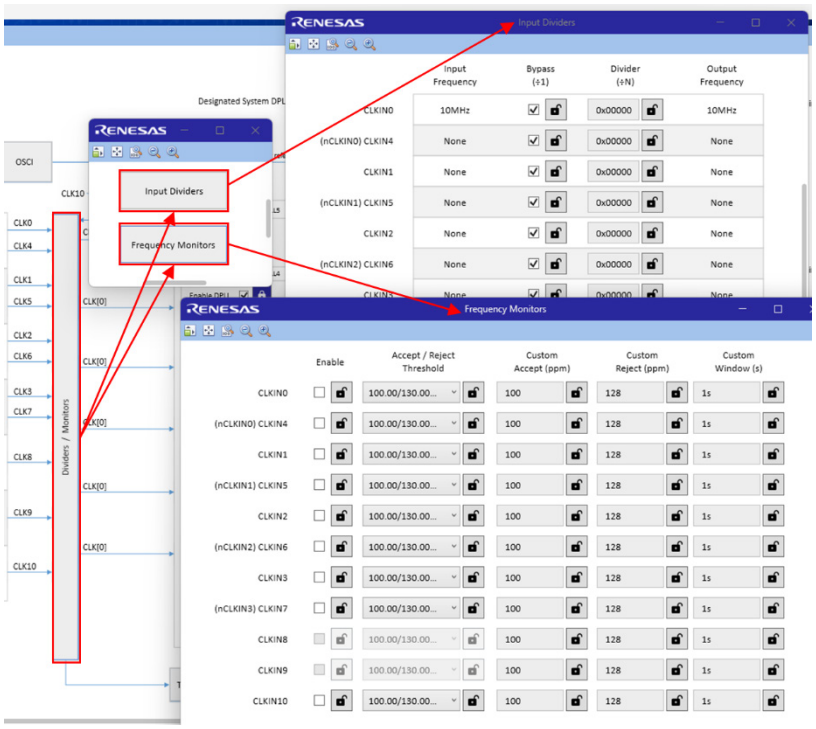


Figure 23. Input Divider and Frequency Monitor Settings

7.7 DPLL Block

The DPLL blocks contain all features pertaining to the DPLL. Clicking on the DPLL Block shows settings for reference selection, feedback selection, operation mode, and the ability to change the digital loop filter settings.

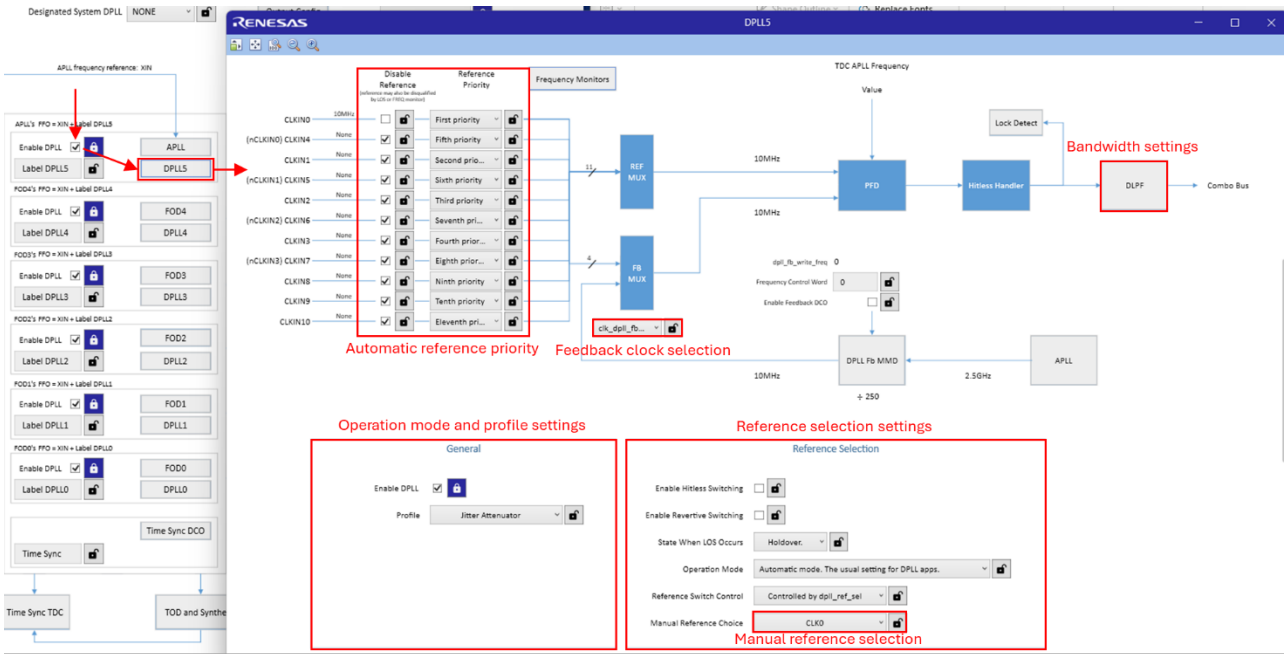


Figure 24. DPLL Block

7.8 GPIO Block

Clicking on the GPIO Block enables configuration of the GPIO function, polarity, output drive strength, and pull-up/down.

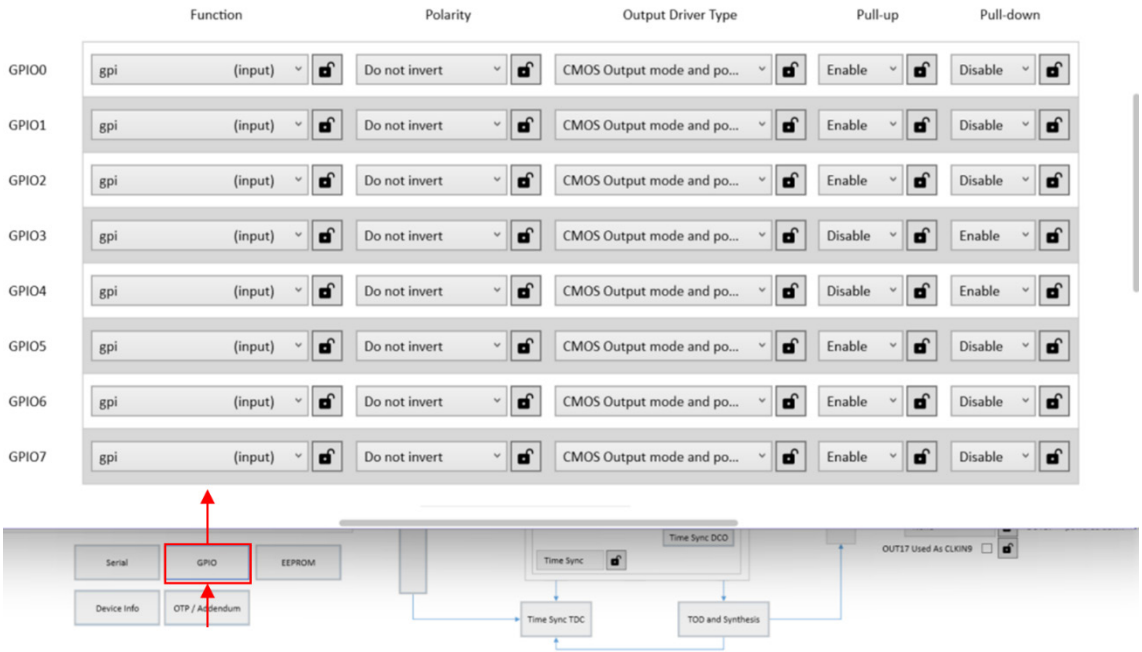


Figure 25. GPIO Block

7.9 Serial Block

The Serial Block displays settings for serial communication protocol, I²C address selection, and SPI interface type. *Note*: The RBS file serial port configuration should match the physical serial port mode on the board by setting the SPI_SEL jumper to pull-up for SPI (default) and pull-down for I²C.

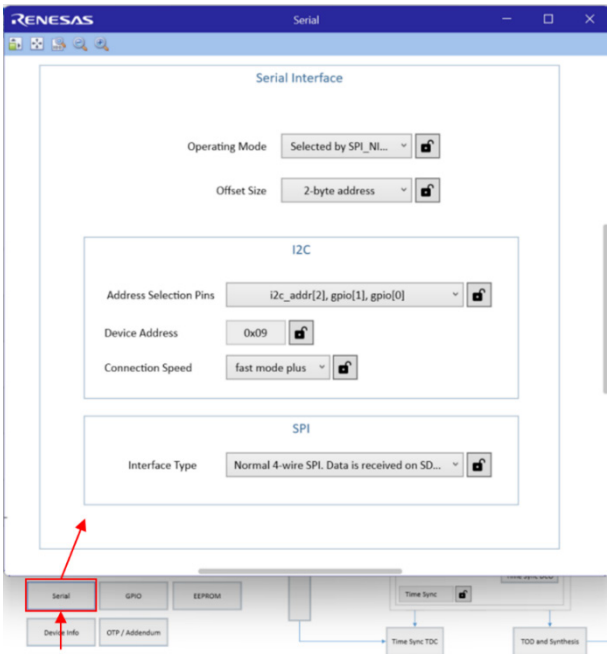


Figure 26. Serial Block

7.10 SYSREF Block

The SYSREF Block allows the configuration of SYSREF pulse type, trigger settings, pulse/pause count, and defines what outputs are considered SYSREF signals.

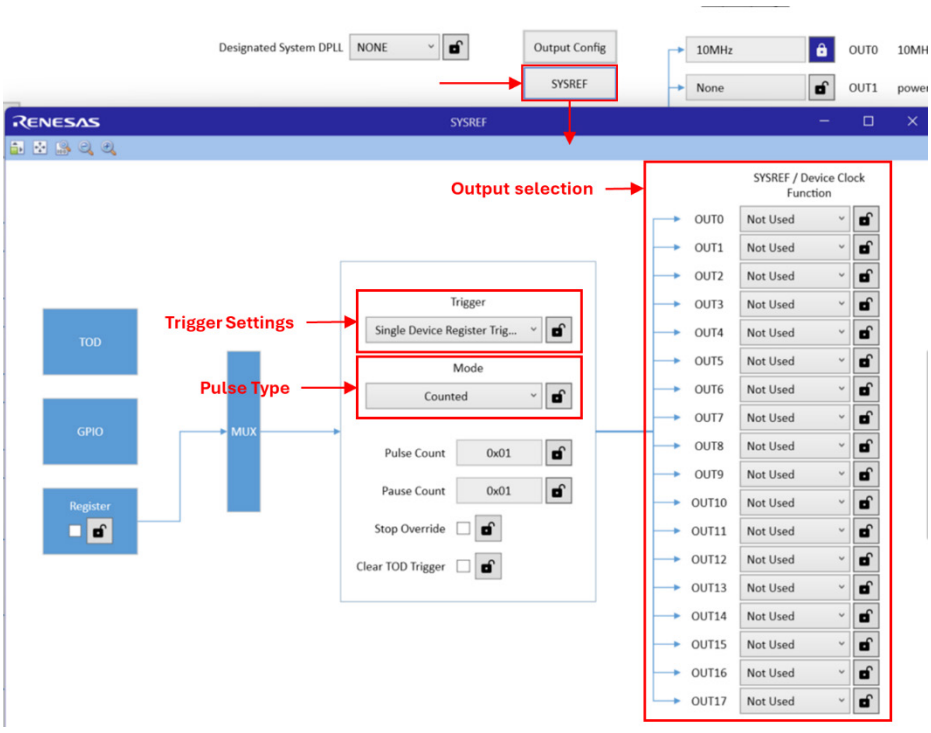


Figure 27. SYSREF Block

1. Set up a given output as either a SYSREF signal or device source, then select the trigger and pulse modes.

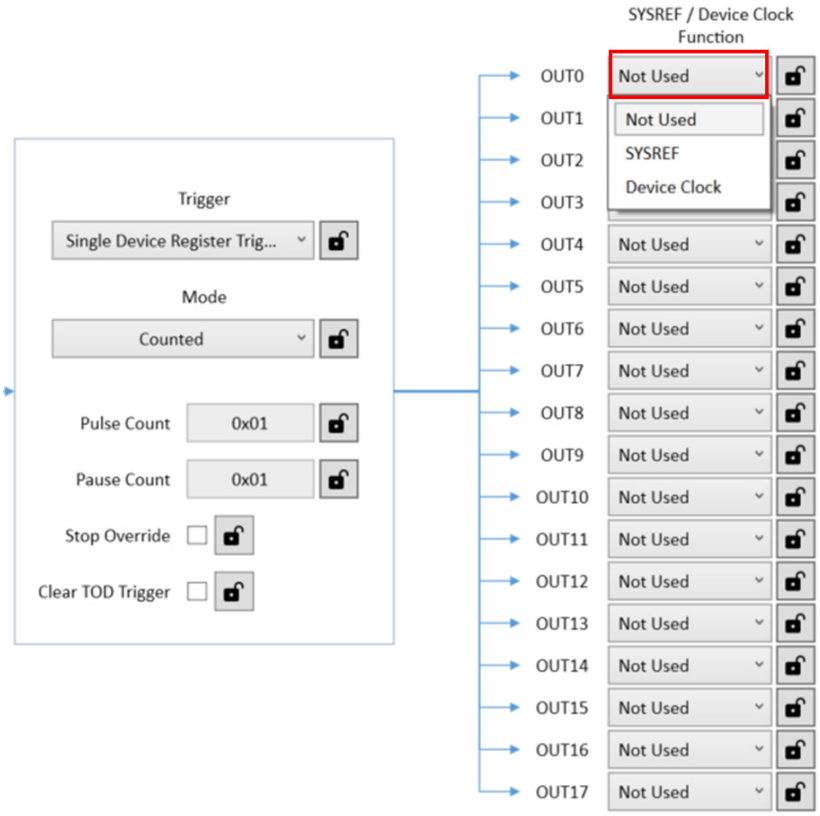


Figure 28. SYSREF Output Assignment

a. **Trigger Mode** – The source of the SYSREF trigger.
   i. **Register** – Write to the init_SYSREF bit using serial connection to trigger a SYSREF event.

      Note: For SYSREF configuration and control registers, see section 4.9 of the relevant *RC3x Programming Guide*.
   ii. **GPIO** – The SYSREF event triggers when GPIO1 sees an active input signal.

      Note: Only GPIO1 can be programmed as an input to trigger a SYSREF event. No other GPIOs have this function.
   iii. **TOD** – SYSREF is triggered with a TOD event.

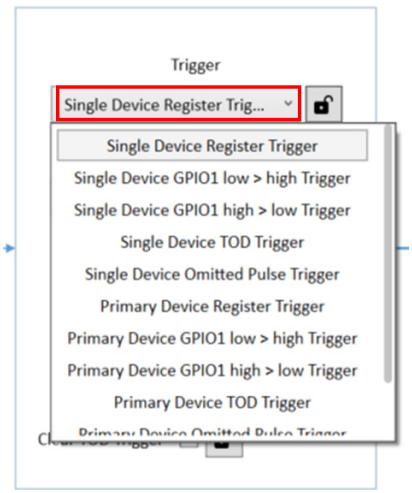


Figure 29. SYSREF Trigger Mode

b. **Pulse Mode** – The type of pulse/pause pattern generated by the SYSREF clock. Pulse mode differs between trigger types. When a register is used to trigger the SYSREF clock, then pulse mode can be configured to:

i. **Counted** – Only one pulse train is generated after the register trigger.



Figure 30. Single Pulse Train (0x10 Pulses) (7.68MHz (Green) and GPIO Trigger (Orange))

ii. **Continuous pulse/pause train** – A continuous train of pulses and pauses defined by the pulse and pause counts.

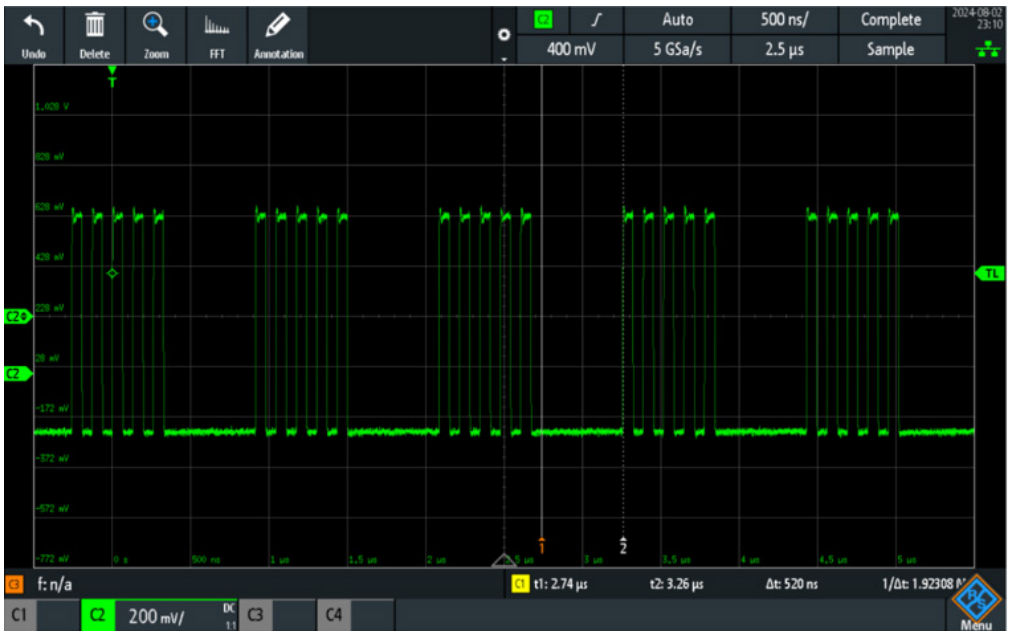


Figure 31. Continuous Pause/Pulse Train with 5 Pulses and 4 Pauses at 7.68MHz

iii. **Continuous (without pause)** – A continuous clock output until the end of the SYSREF event.

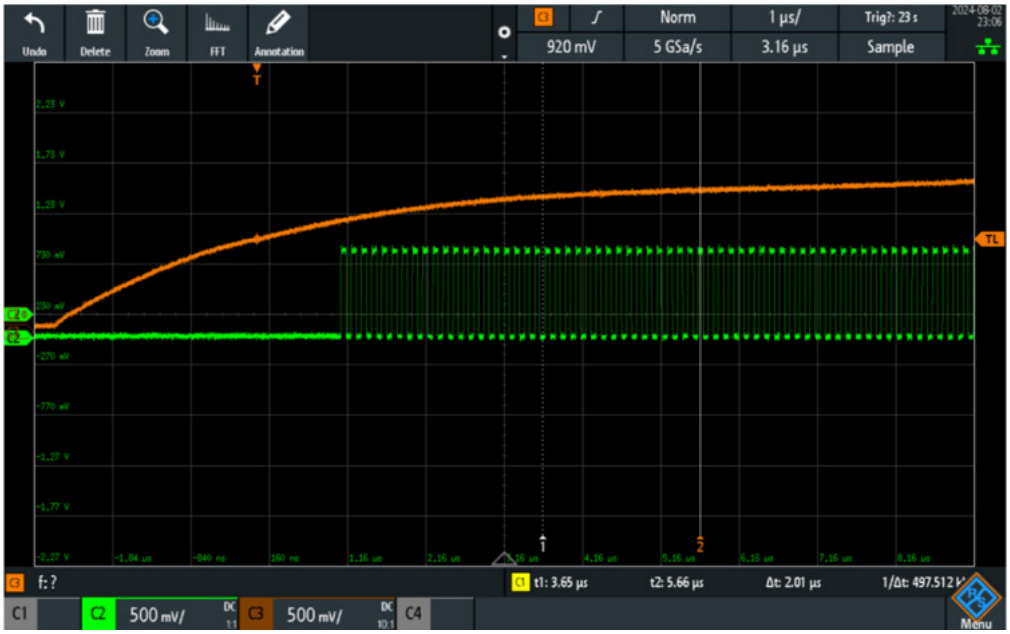


Figure 32. Continuous 7.68MHz Pulse (Green) with GPIO Dip Switch Trigger (Orange)

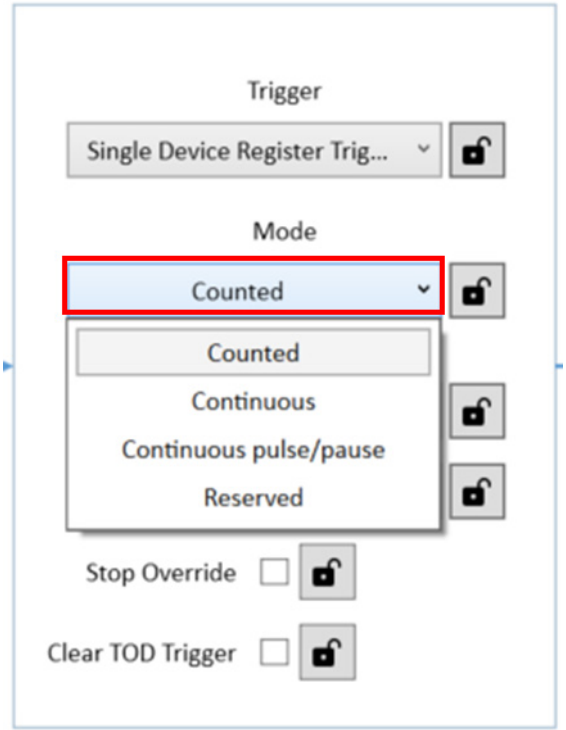


Figure 33. SYSREF Pulse Mode Register Trigger

The SYSREF signal can also be triggered by GPIO or TOD in the Pulse Mode. The pulse mode can be continuous or single pulse train depending on the trigger edge.

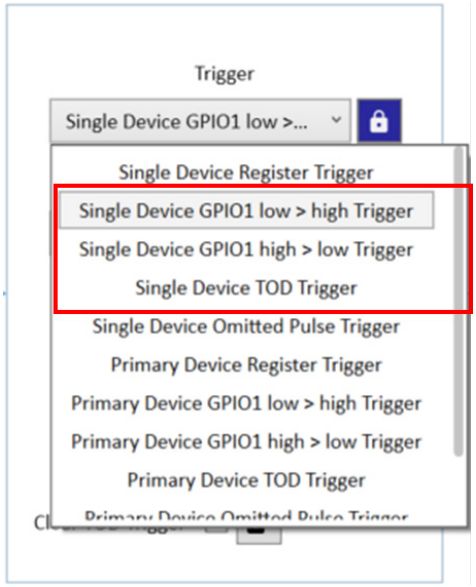


Figure 34. SYSREF Pulse Mode GPIO/TOD Trigger

Pulse count is the number of pulses in a pulse train. If single pulse train is selected, then the device will output the number of pulses denoted in pulse count before finishing the SYSREF event.

In continuous pulse/pause mode, the pulse count is the number of pulses that will be output before pausing. Then, the signal will pause for the number of pulses based on the pause count. The cycle is repeated until the sysref_init bit is set to 0.

Note: Only register trigger can be used for Continuous pulse/pause mode.

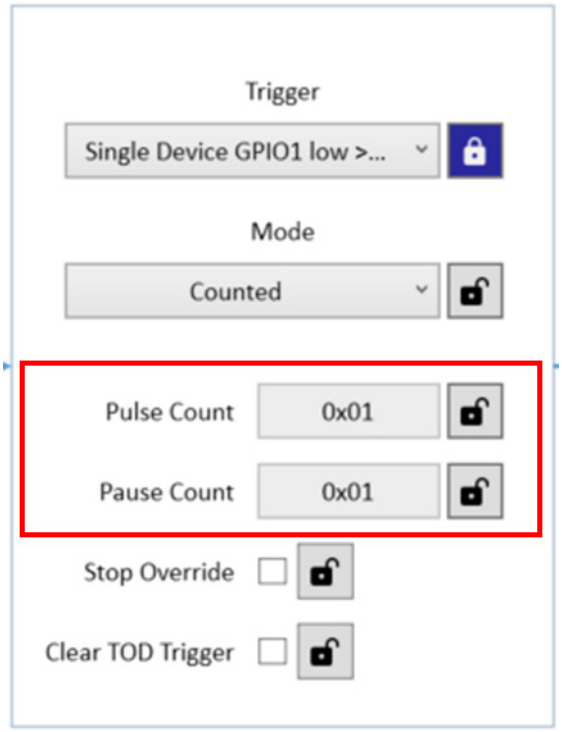


Figure 35. SYSREF Pulse and Pause Counts

When a GPIO is used as an input trigger for SYSREF, the GPIO settings must be configured. RICBox automatically configures GPIO1 as input when the GPIO trigger source is selected.

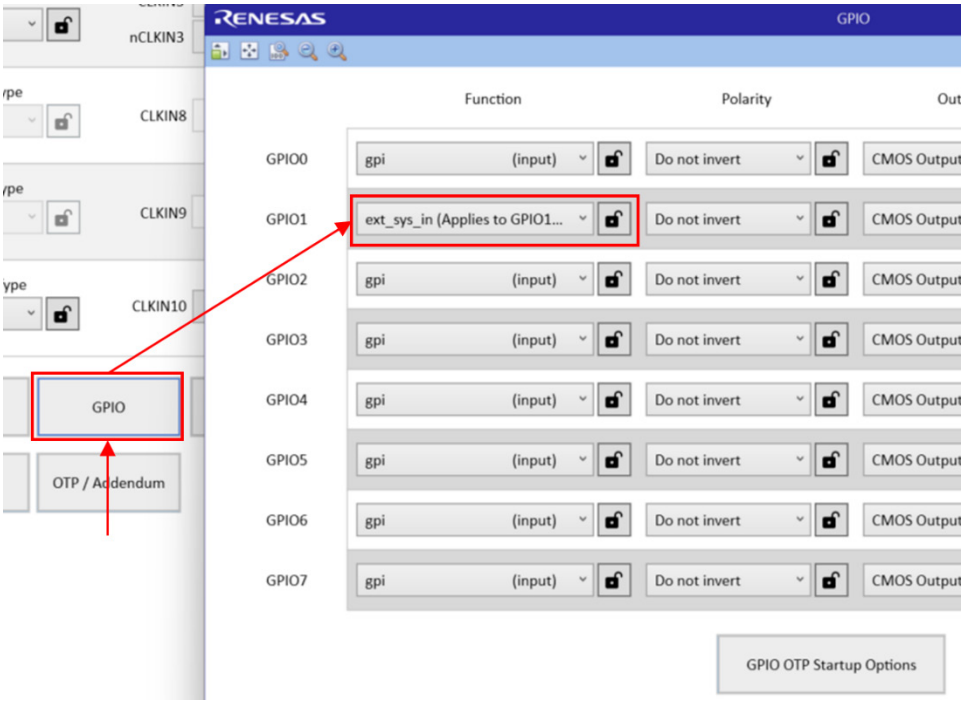


Figure 36. GPIO1 SYSREF EXT_SYS_IN

GPIO0 can be used as an external trigger output for a cascaded SYSREF signal between devices. Use the EXT_SYS_OUT setting to configure GPIO0 as SYSREF output.

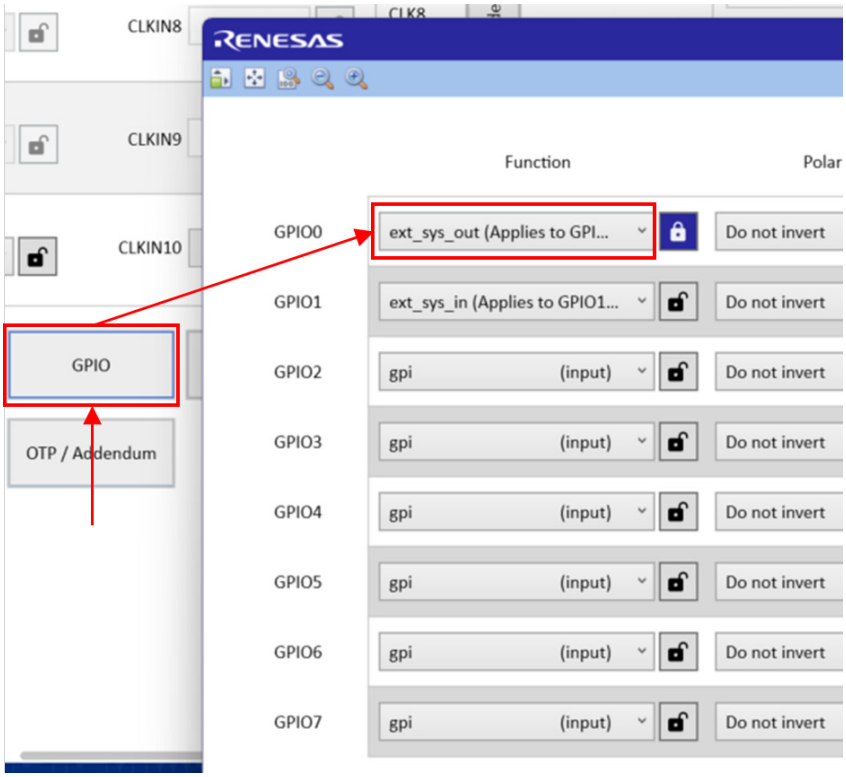


Figure 37. GPIO0 SYSREF EXT_SYS_OUT

When selecting the trigger source, there are options for primary and secondary sources. The primary source is the main device in the cascaded chain where secondary is receiving a trigger from primary device.

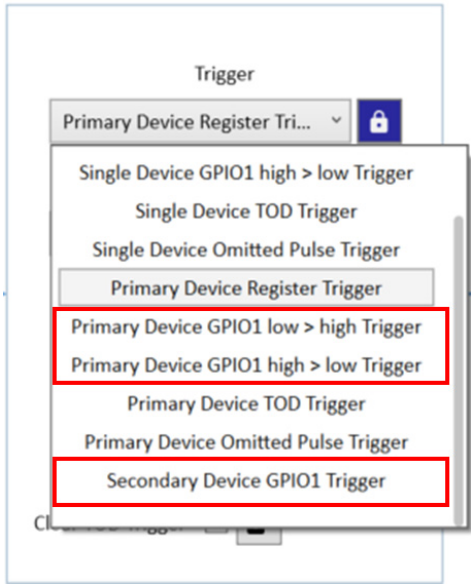


Figure 38. SYSREF Primary and Secondary Trigger Selections

Note: When any SYSREF event ends, wait at least 3 SYSREF clock periods before starting another event.

7.11 Time Sync TDC Block

1. Click the **Time Sync TDC** block in the main diagram.

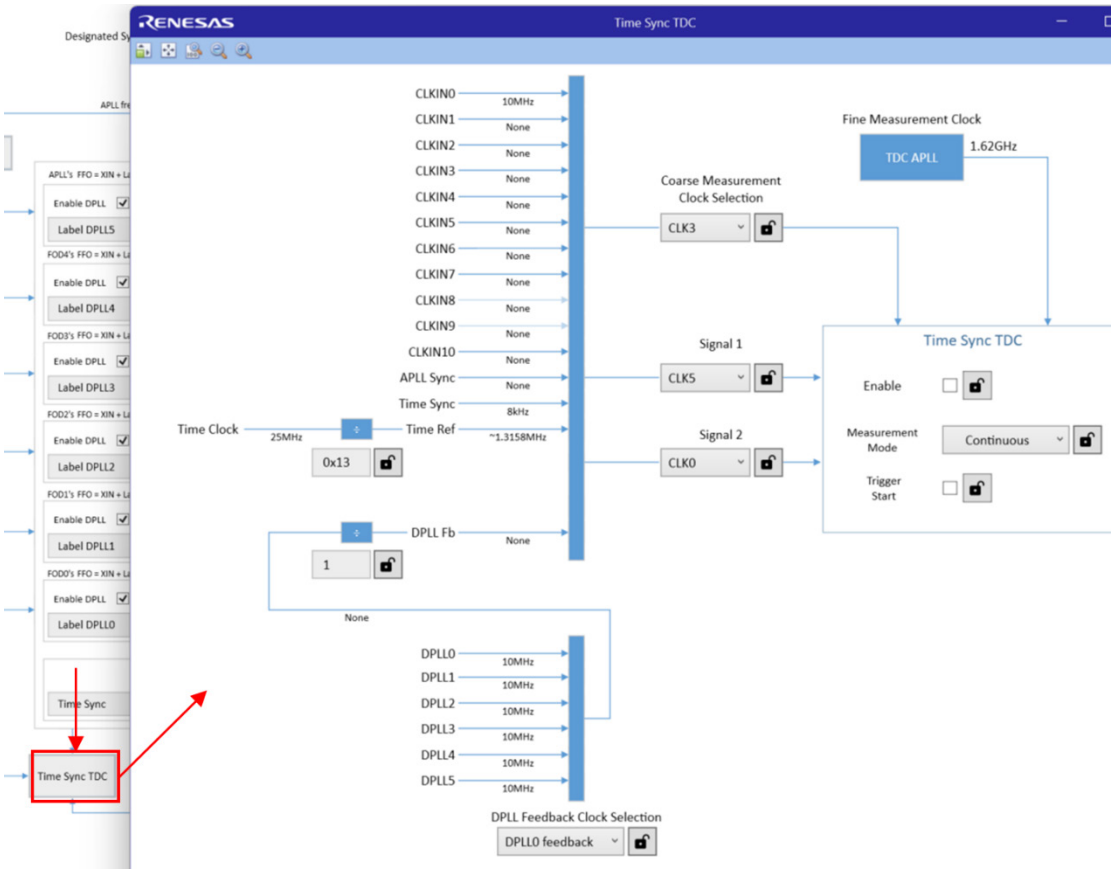


Figure 39. Time Sync TDC Block Location in the RICBox GUI

2. Enable Time Sync TDC.

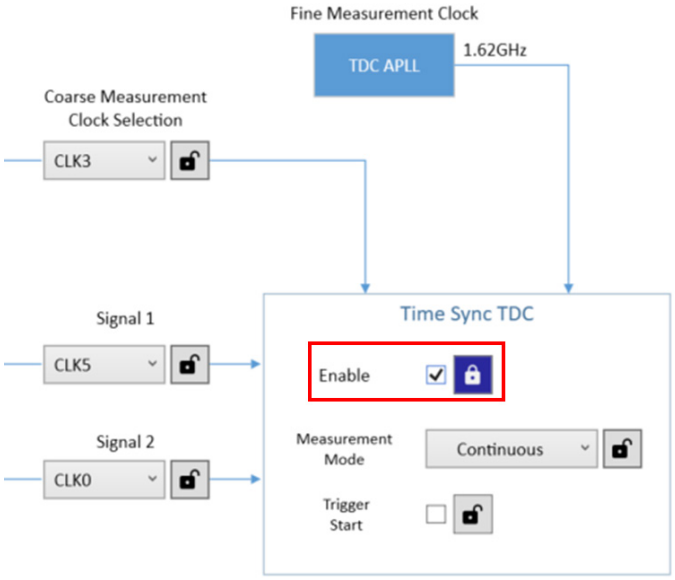


Figure 40. Time Sync TDC Enable Button

3. Select TDC Measurement Mode between one-shot and continuous.

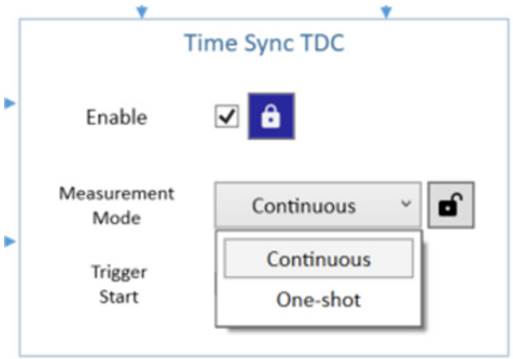


Figure 41. TDC Measurement Mode Select

4. Select input reference clocks to measure. The input clocks must be the same frequency.

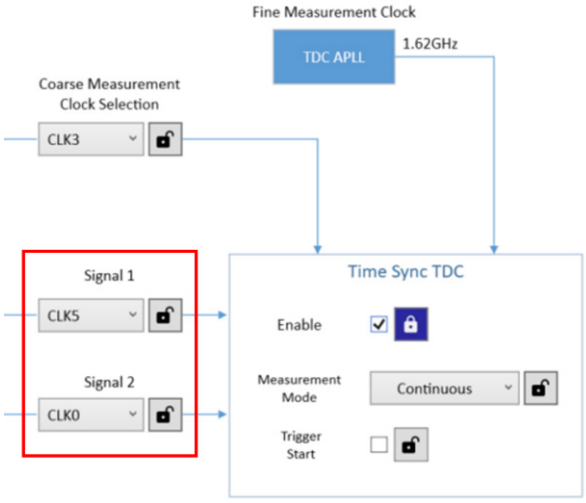


Figure 42. Time Sync TDC Reference Input Select

5. Connect to a device and program its registers with the “program” button. This step is not necessary if the program button has already been clicked prior to step 1.
6. Enable the input measurement.

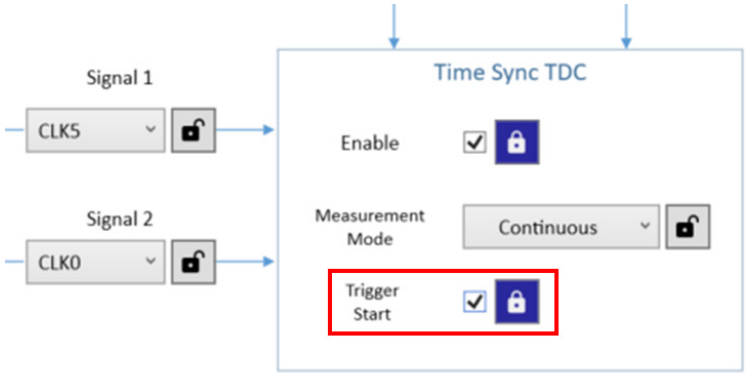


Figure 43. TDC Measurement Start Button

7. Open the RICBox command line interface (CLI) by going to tools → CLI.

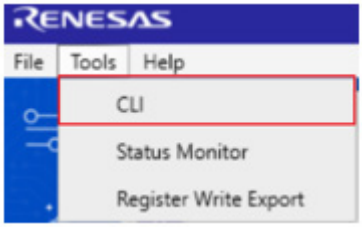


Figure 44. RICBox Command Line Interface Location

   a. Type “write TOP.STATUS.TDC_FIFO_READ_REQ.fifo_read_req 1” to load measured values to the fine and coarse value registers.
   b. Type “read TOP.STATUS.TDC_FIFO_READ.fifo_read_val_fine” to read fine measurement value.

```
> write TOP.TIME_SYNC_TDC.TDC_FIFO_READ_REQ.fifo_read_req 1
Wrote 1 byte(s) to offset 0xB2F
> read TOP.TIME_SYNC_TDC.TDC_FIFO_READ.fifo_read_val_fine
0x1ADD
```

Figure 45. RICBox Command Line Interface Register Write and Read Example

   c. Type “read TOP.STATUS.TDC_FIFO_READ.fifo_read_val_coarse” to read the coarse measurement value.

Once coarse and fine values have been read, the offset between the two input clocks can be calculated as:

$$Offset = \left(\frac{tdc_coarse_meas}{F_{TDCcoarse}} \times\right) + \left(\frac{tdc_fine_meas}{62 \times F_{TDCfine}}\right)$$

where:

- tdc_coarse_meas is read from TOP.STATUS.TDC_FIFO_READ.fifo_read_val_coarse; this value is **signed**.
- tdc_fine_meas is read from TOP.STATUS.TDC_FIFO_READ.fifo_read_val_fine; this value is **signed**.
- $F_{TDCcoarse}$ is TDC coarse measurement clock frequency.
- $F_{TDCfine}$ is the TDC fine measurement clock frequency.

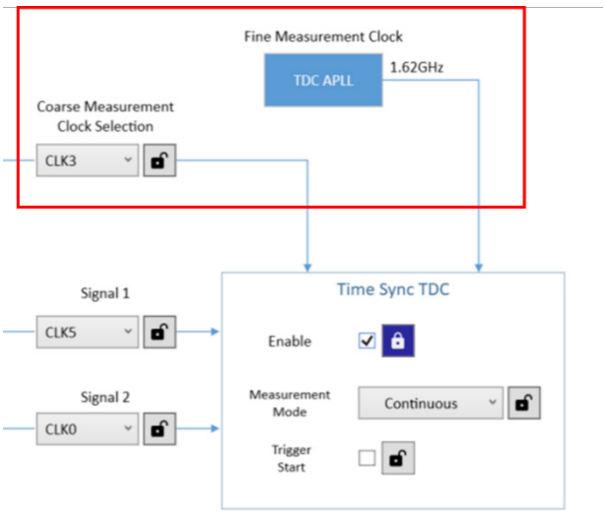


Figure 46. TDC Coarse Measurement Clock and TDC Fine Measurement Clock

8. Device Connection

Device connection can be achieved through the bottom right corner of every page.

1. To connect one of the Renesas evaluation boards, ensure the device is powered and connected to the working computer.
2. Click the **Not Connected** button in the corner of the screen. This will lead to a small pop-out page.
3. Click the connect symbol in the corner of the page to establish a connection to the device.



Figure 47. Device Connection

Note: For more information about device connection features, see section 4 of the RICBox Software Manual.

9. Common Configurable Settings

9.1 Saving/Programming EEPROM Images

1. Establish a connection to a device with the EEPROM attached.



Figure 48. Device Connection

2. Go to the EEPROM section of the block diagram.
3. Select the EEPROM Part Number and the EEPROM Address.
4. Click the **Program** button.

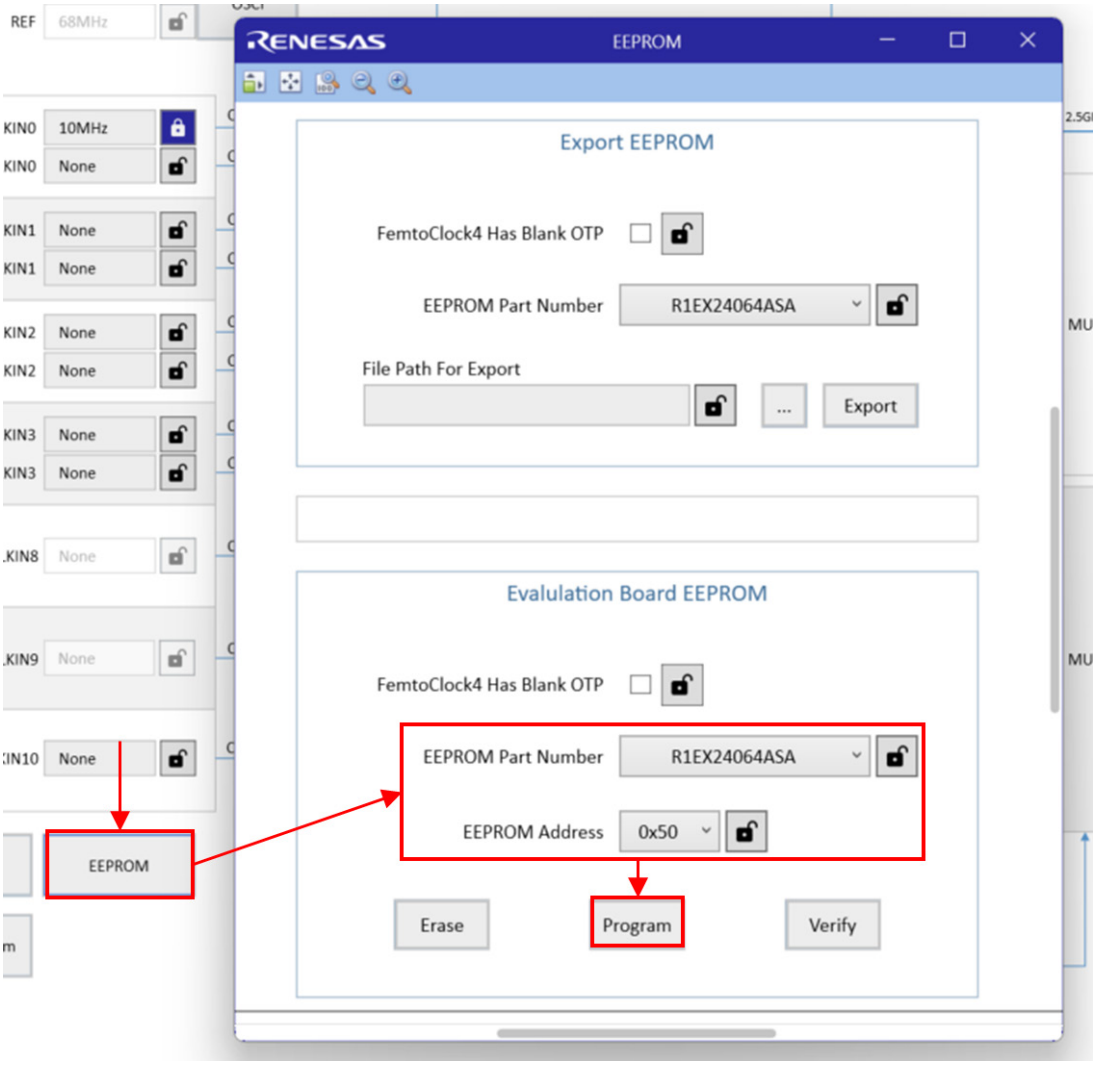


Figure 49. Programming a Connected EEPROM Device

Note: The Adding Configurations to a Settings File section highlights configuration naming. Section 13 of the RICBox Software Manual discusses multiple configuration support.

Note: FemtoClock4 software only supports programming one configuration into EEPROM at a time.

5. Choose the save location by first selecting the correct EEPROM Part Number from the Export EEPROM section.
6. Click the button next to the **File Path For Export** entry box.
7. Create a filename, then click **Save**.
8. Click the **Export** button to save the EEPROM image to the specified location.

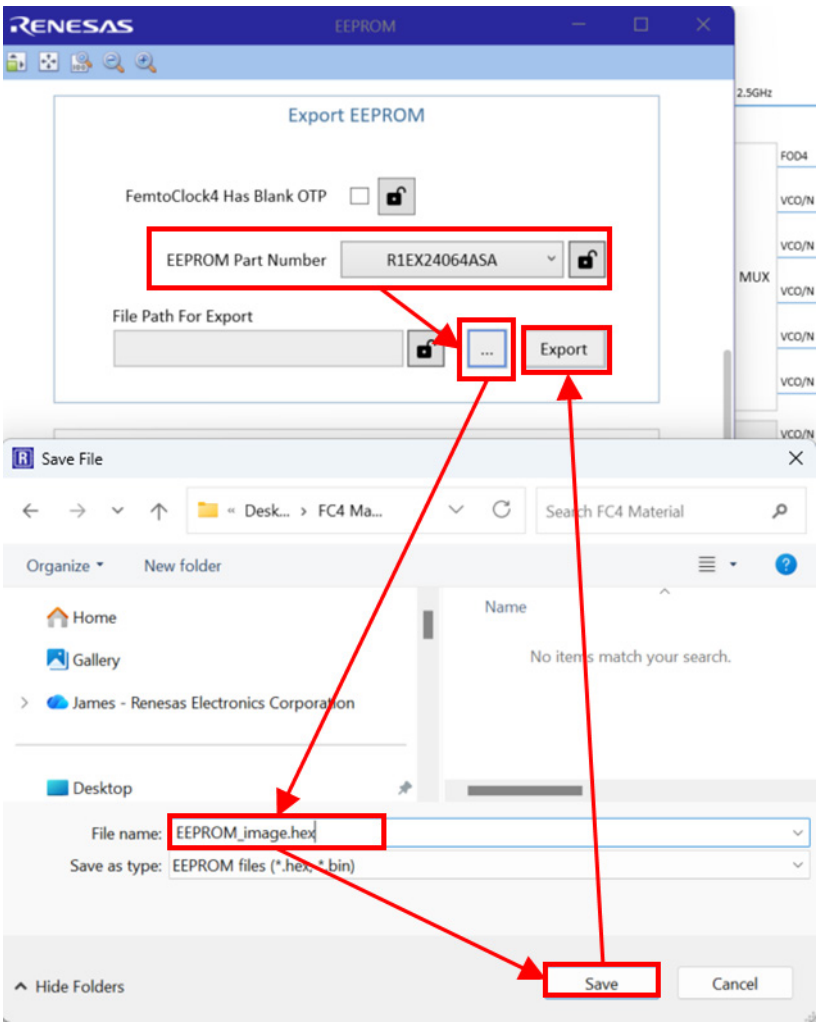


Figure 50. Saving EEPROM Image

Note: Ensure to specify the file extension as ".bin" or ".hex" when naming the file.

10. Revision History

Revision	Date	Description
1.00	Dec 11, 2025	Initial release.

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