# ClockMatrix Firmware Version 4.9.5

## Contents



## 1. Overview

This document describes changes in the functionality and register map between firmware version 4.9.5 and version 4.8.7.

**Table 1. Related Documents**

| Document Title | Document Description |
|---|---|
| Device Datasheet | Contains a functional overview of a specific device and hardware design related details including pinouts, AC and DC specifications, and applications information related to power filtering and terminations. |
| 8A3xxx Family Programming Guide v4.8 dated September 30, 2020 | Contain detailed register descriptions and address maps for all members of the family of devices. All devices use some subset of this register map. |
| 8A3xxx Family Programming Guide v4.9 dated Apr 6, 2023 | |

## 2. Firmware Version Number

The firmware version can be read from the GENERAL_STATUS registers as shown in the following table.

| Register Module Base Address: C014h | | | Firmware Version v4.8.7 | Firmware Version v4.9.5 |
|---|---|---|---|---|
| **Offset Address (Hex)** | **Individual Register Name** | **Register Description** | **Default Value** | **Default Value** |
| 010h | GENERAL_STATUS.MAJ_REL | Major release number | 09h | 09h |
| 011h | GENERAL_STATUS.MIN_REL | Minor release number | 08h | 09h |
| 012h | GENERAL_STATUS.HOTFIX_REL | Hotfix release number | 07h | 05h |

# 3. Firmware Version 4.9.5 Functions Added Since Version 4.8.7

| Issue Number | Description of Function |
|---|---|
| BRMBXR-3592 | Added a soft control and status register (SCSR) for the received time of day (TOD) value via PWM. The new register is in module SCSR_PWM_RX_INFO. |
| BRMBXR-3231<br>BRMBXR-3406<br>BRMBXR-3422<br>BRMBXR-3590<br>BRMBXR-3610<br>BRMBXR-3621<br>BRMBXR-3622<br>BRMBXR-3641 | Added support to use PWM to transmit and receive clocks that are asynchronous with the PWM carrier. |
| BRMBXR-3293 | DPLL_TRANS_CTRL registers were made accessible to the user. |
| BRMBXR-3300 | Added support to use GPIOx as a target for phase measurement with the Output TDC. |
| BRMBXR-3501<br>BRMBXR-3526 | Added option for closed-loop pull-in to the LOCK_REC_PULL_IN_EN and LOCK_ACQ_PULL_IN_EN bit fields. |
| BRMBXR-3562 | Added option for fast frame pulse switch to the FRAME_SYNC_MODE bit field. |
| BRMBXR-3594 | Added counters in the SCSRs for PWM parity errors for each PWM decoder. The new registers are in module SCSR_PWM_RX_INFO. |
| BRMBXR-3224<br>BRMBXR-3597 | Added TOD automatic update for PWM transmission. |

# 4. Improvements in Version 4.9.5 Added Since Version 4.8.7

**Issue Number: BRMBXR-3256**

| Firmware | Functional Difference |
|---|---|
| v4.8.7 | When a DPLL is in GPIO slave mode with GPIO slave active, then reference switches will be done using hitless reference switching. The DPLL will not align the phase of its outputs with the phase of the new reference.<br>When a DPLL is placed into GPIO slave mode it does not automatically align its outputs with the phase of its reference. |
| v4.9.5 | When a DPLL is in GPIO slave mode with GPIO slave active, then reference switches will not be done using hitless reference switching. The DPLL will align the phase of its outputs with the phase of the new reference.<br>When a DPLL is placed into GPIO slave mode it automatically aligns its outputs with the phase of its reference. |

**Issue Number: BRMBXR-3301**

| Firmware | Functional Difference |
|---|---|
| v4.8.7 | PWM receivers cannot receive all 128 bytes of payload if the carrier frequency is lower than 50kHz. |
| v4.9.5 | PWM receivers can receive 128 bytes with 8kHz carrier or higher. |

| Issue Number: BRMBXR-3302 | |
|---|---|
| Firmware | Functional Difference |
| v4.8.7 | If the OTP or EEPROM configuration has OUT_SYNC_DISABLE bit set to “1” then the output clock might not become active for a random interval of up to 8 seconds after power-on reset. This issue does not happen after a warm reset. |
| v4.9.5 | This issue is corrected, and the output clock starts immediately after power-on reset. |

| Issue Number: BRMBXR-3308 | |
|---|---|
| Firmware | Functional Difference |
| v4.8.7 | DPLL_0 will not switch from disabled mode to write phase mode using the PLL_MODE bit field unless DPLL_0 is reset after changing the setting of the PLL_MODE bit field. |
| v4.9.5 | This issue is corrected and DPLL_0 behaves as intended. |

| Issue Number: BRMBXR-3349 | |
|---|---|
| Firmware | Functional Difference |
| v4.8.7 | Outputs may be misaligned after the device is configured by the host. |
| v4.9.5 | This issue is corrected, and outputs are aligned after the device is configured by the host. |

| Issue Number: BRMBXR-3403 | |
|---|---|
| Firmware | Functional Difference |
| v4.8.7 | The fine phase measurement algorithm may affect the decimator value of the DPLL when the FILTER_STATUS_UPDATE_EN bit is set. |
| v4.9.5 | The decimator is controlled by the phase measurement algorithm only if the channel is in phase measurement mode. |

| Issue Number: BRMBXR-3416 | |
|---|---|
| Firmware | Functional Difference |
| v4.8.7 | When a channel is in Phase Measurement mode and the frequency of the channel FOD is set to zero Hz; if a new reference input is selected, valid phase measurement data will not be available for 10s. |
| v4.9.5 | When a new reference input is selected for phase measurement the result is updated immediately after the measurement is finished, without any additional delay. |

| Issue Number: BRMBXR-3427 | |
|---|---|
| Firmware | Functional Difference |
| v4.8.7 | If the input reference is qualified when a DPLL is restarted, then the feedback divider might not be aligned properly with the Master Divider. |
| v4.9.5 | This issue is corrected, and the feedback divider will be properly aligned with the Master Divider. |

| Issue Number: BRMBXR-3431 | |
|---|---|
| **Firmware** | **Functional Difference** |
| v4.8.7 | If two consecutive DPLL restart events occur within 1ms then subsequent reference switching instructions may not be accepted by the DPLL state machine. |
| v4.9.5 | This issue is corrected, and reference switching instructions are accepted by the DPLL state machine. |

| Issue Number: BRMBXR-3512 | |
|---|---|
| **Firmware** | **Functional Difference** |
| v4.8.7 | The TOD read command register TOD_READ_TRIGGER is cleared before the TOD value is updated by the device. This was considered an improper sequence since the self clearing TOD_READ_TRIGGER indicates to the user that the command is completed. However, the TOD value is updated immediately after the TOD_READ_TRIGGER is cleared, so there was no chance of an error. |
| v4.9.5 | The TOD read command register TOD_READ_TRIGGER is cleared after the TOD value is updated by the device. This is considered the proper sequence and there is still no chance of an error. |

| Issue Number: BRMBXR-3523 | |
|---|---|
| **Firmware** | **Functional Difference** |
| v4.8.7 | Satellite channels do not align properly when they are in phase measurement mode. |
| v4.9.5 | This issue is corrected, satellite channels align properly when they are in phase measurement mode. |

| Issue Number: BRMBXR-3535 | |
|---|---|
| **Firmware** | **Functional Difference** |
| v4.8.7 | The outputs of a channel in phase measurement mode are affected when new inputs are selected for phase measurement. |
| v4.9.5 | This issue is corrected, the outputs of a channel in phase measurement mode are not affected when new inputs are selected for phase measurement. |

| Issue Number: BRMBXR-3553 | |
|---|---|
| **Firmware** | **Functional Difference** |
| v4.8.7 | When a channel is configured as a “satellite channel” it is controlled by an internal automatic alignment algorithm that maintains alignment between the satellite channel and its source channel. On rare occasions, the automatic alignment algorithm can apply an unintended and small FFO to a satellite channel for up to 35 minutes. |
| v4.9.5 | The satellite channels and automatic alignment algorithm operate as intended. |

| Issue Number: BRMBXR-3555 | |
|---|---|
| **Firmware** | **Functional Difference** |
| v4.8.7 | When a DISQUAL_TIMER bit field is set to 1.25ms the reference monitor may generate false alarms. |
| v4.9.5 | The issue is corrected and the reference monitors operate as intended. |

| Issue Number: BRMBXR-3598 | |
|---|---|
| **Firmware** | **Functional Difference** |
| v4.8.7 | For coarse phase measurement mode, the output of the TDC is filtered to improve measurement accuracy. The filtering is done by both the decimator filter and the loop filter. The device automatically detects steps in the filtered measured phase and opens the decimator bandwidth to respond more quickly. |
| v4.9.5 | For coarse phase measurement mode, the output of the TDC is filtered to improve measurement accuracy. The filtering is done by the decimator filter only. The device automatically detects steps in the filtered measured phase and opens the decimator bandwidth to respond more quickly. |

| Issue Number: BRMBXR-3599 | |
|---|---|
| **Firmware** | **Functional Difference** |
| v4.8.7 | For coarse phase measurement mode, the phase measurement values are provided to the user in both the DPLLx_FILTER_STATUS field and the DPLLx_PHASE_STATUS field. |
| v4.9.5 | For coarse phase measurement mode, the phase measurement values are provided to the user in the DPLLx_PHASE_STATUS field only. In this mode, the DPLLx_FILTER_STATUS field remains available to the user according to its description in the programming guide. |

| Issue Number: BRMBXR-3636 | |
|---|---|
| **Firmware** | **Functional Difference** |
| v4.8.7 | The DPLL phase pull-in procedure does not pull-in the phase offset when DPLL_PHASE_PULL_IN_OFFSET is 1 ns and the DPLL_PHASE_PULL_IN_SLOPE_LIMIT is 1ppb. |
| v4.9.5 | The DPLL phase pull-in procedure does pull-in the phase offset when DPLL_PHASE_PULL_IN_OFFSET is 1 ns and the DPLL_PHASE_PULL_IN_SLOPE_LIMIT is 1ppb. |

| Issue Number: BRMBXR-3644 | |
|---|---|
| **Firmware** | **Functional Difference** |
| v4.8.7 | When tod_frame_access_en = 1, if TOD frames are not discarded by the user, then over the course of many hours, TOD frames can accumulate in the receive FIFO. |
| v4.9.5 | When tod_frame_access_en = 1, TOD frames cannot accumulate in the receive FIFO. |

# 5. Renesas Internal Documentation

| Issue Number | Description |
|---|---|
| BRMBXR-3289<br>BRMBXR-3291<br>BRMBXR-3294<br>BRMBXR-3321<br>BRMBXR-3333<br>BRMBXR-3334<br>BRMBXR-3338<br>BRMBXR-3445<br>BRMBXR-3456<br>BRMBXR-3458<br>BRMBXR-3500<br>BRMBXR-3515<br>BRMBXR-3539<br>BRMBXR-3567<br>BRMBXR-3573<br>BRMBXR-3619<br>BRMBXR-3627 | These issues are related to Renesas documentation and interim firmware versions. |

# 6. Register Differences Between Version 4.8.7 and Version 4.9.5

| Register Module Base Address: C014h | | |
|---|---|---|
| **Offset Address (Hex)** | **Individual Register Name** | **Change** |
| 011h | GENERAL_STATUS. MIN_REL | Default value is 9. |
| 012h | GENERAL_STATUS. HOTFIX_REL | Default value is 5. |

| Register Module Base Address: C03Ch | | |
|---|---|---|
| **Offset Address (Hex)** | **Individual Register Name** | **Change** |
| 022h | STATUS.DPLL0_REF_STAT.dpll0_input | Added option 0x1C = PWM sync phase (CLK28) |

| Register Module Base Address: C3B0h | | |
|---|---|---|
| Offset Address (Hex) | Individual Register Name | Change |
| 004h | DPLL_0.DPLL_CTRL_2.frame_sync_mode | Added new option, 3 = fast frame pulse switch. |
| 023h | DPLL_0.DPLL_FASTLOCK_CFG_0.lock_rec_pull_in_en<br>DPLL_0.DPLL_FASTLOCK_CFG_0.lock_rec_phase_snap_en<br>DPLL_0.DPLL_FASTLOCK_CFG_0.lock_acq_pull_in_en<br>DPLL_0.DPLL_FASTLOCK_CFG_0.lock_acq_phase_snap_en | Redefined these bits. |
| 026h | DPLL_0.DPLL_FASTLOCK_PSL | Redefined this register. |

| Register Module Base Address: CB00h | | |
|---|---|---|
| Offset Address (Hex) | Individual Register Name | Change |
| 004h | PWM_ENCODER_0.PWM_ENCODER_CMD.tod_auto_update | New bit. |

| Register Module Base Address: CB40h | | |
|---|---|---|
| Offset Address (Hex) | Individual Register Name | Change |
| 005h | PWM_DECODER_0.PWM_DECODER_CMD.tod_frame_access_en | Redefined this bit. |

| Register Module Base Address: CBCCh | | |
|---|---|---|
| Offset Address (Hex) | Individual Register Name | Change |
| 000h | TOD_0.TOD_CFG.tod_out_sync_disable | Redefined this bit. |

| Register Module Base Address: CC90h | | |
|---|---|---|
| Offset Address (Hex) | Individual Register Name | Change |
| 00Eh | TOD_READ_SECONDARY_0.TOD_READ_SECONDARY_CMD | Revised the TRIGGER description above the Bit Field Locations and Descriptions table for this register. |

| Register Module Base Address: CD20h | | |
|---|---|---|
| Offset Address (Hex) | Individual Register Name | Change |
| 004h | INPUT_TDC.INPUT_TDC_FBD_CTRL.fdb_user_config_en | Redefined this bit. |

| Register Module Base Address: CD80h | | |
|---|---|---|
| **Offset Address (Hex)** | **Individual Register Name** | **Change** |
| 000h | PWM_SYNC_ENCODER_0.PWM_SYNC_ENCODER_PAYLOAD_CNFG | New register. |
| 001h | PWM_SYNC_ENCODER_0.PWM_SYNC_ENCODER_PAYLOAD_SQUELCH_CNFG | New register. |
| 002h | PWM_SYNC_ENCODER_0.PWM_SYNC_ENCODER_CMD | New register. |

| Register Module Base Address: CE00h | | |
|---|---|---|
| **Offset Address (Hex)** | **Individual Register Name** | **Change** |
| 000h | PWM_SYNC_DECODER_0.PWM_SYNC_DECODER_PAYLOAD_CNFG_0 | New register. |
| 001h | PWM_SYNC_DECODER_0.PWM_SYNC_DECODER_PAYLOAD_CNFG_1 | New register. |
| 002h | PWM_SYNC_DECODER_0.PWM_SYNC_DECODER_PAYLOAD_CNFG_2 | New register. |
| 003h | PWM_SYNC_DECODER_0.PWM_SYNC_DECODER_PAYLOAD_CNFG_3 | New register. |
| 004h | PWM_SYNC_DECODER_0.PWM_SYNC_DECODER_CMD | New register. |

| Register Module Base Address: CE80h | | |
|---|---|---|
| **Offset Address (Hex)** | **Individual Register Name** | **Change** |
| 000h | PWM_RX_INFO.PWM_TOD | New register. |
| 00Ch | PWM_RX_INFO.PWM_DECODER0_ERRORS | New register. |
| 010h | PWM_RX_INFO.PWM_DECODER1_ERRORS | New register. |
| 014h | PWM_RX_INFO.PWM_DECODER2_ERRORS | New register. |
| 018h | PWM_RX_INFO.PWM_DECODER3_ERRORS | New register. |
| 01Ch | PWM_RX_INFO.PWM_DECODER4_ERRORS | New register. |
| 020h | PWM_RX_INFO.PWM_DECODER5_ERRORS | New register. |
| 024h | PWM_RX_INFO.PWM_DECODER6_ERRORS | New register. |
| 028h | PWM_RX_INFO.PWM_DECODER7_ERRORS | New register. |
| 02Ch | PWM_RX_INFO.PWM_DECODER8_ERRORS | New register. |
| 030h | PWM_RX_INFO.PWM_DECODER9_ERRORS | New register. |
| 034h | PWM_RX_INFO.PWM_DECODER10_ERRORS | New register. |
| 038h | PWM_RX_INFO.PWM_DECODER11_ERRORS | New register. |
| 03Ch | PWM_RX_INFO.PWM_DECODER12_ERRORS | New register. |
| 040h | PWM_RX_INFO.PWM_DECODER13_ERRORS | New register. |
| 044h | PWM_RX_INFO.PWM_DECODER14_ERRORS | New register. |
| 048h | PWM_RX_INFO.PWM_DECODER15_ERRORS | New register. |
| 04Ch | PWM_RX_INFO.PWM_SYNC_DECODER0_S QUELCH_STATUS | New register. |
| 04Dh | PWM_RX_INFO.PWM_SYNC_DECODER1_S QUELCH_STATUS | New register. |

| Register Module Base Address: CE80h (Cont.) | | |
|---|---|---|
| Offset Address (Hex) | Individual Register Name | Change |
| 04Eh | PWM_RX_INFO.PWM_SYNC_DECODER2_S QUELCH_STATUS | New register. |
| 04Fh | PWM_RX_INFO.PWM_SYNC_DECODER3_S QUELCH_STATUS | New register. |
| 050h | PWM_RX_INFO.PWM_SYNC_DECODER4_S QUELCH_STATUS | New register. |
| 051h | PWM_RX_INFO.PWM_SYNC_DECODER5_S QUELCH_STATUS | New register. |
| 052h | PWM_RX_INFO.PWM_SYNC_DECODER6_S QUELCH_STATUS | New register. |
| 053h | PWM_RX_INFO.PWM_SYNC_DECODER7_S QUELCH_STATUS | New register. |
| 054h | PWM_RX_INFO.PWM_SYNC_DECODER8_S QUELCH_STATUS | New register. |
| 055h | PWM_RX_INFO.PWM_SYNC_DECODER9_S QUELCH_STATUS | New register. |
| 056h | PWM_RX_INFO.PWM_SYNC_DECODER10_S QUELCH_STATUS | New register. |
| 057h | PWM_RX_INFO.PWM_SYNC_DECODER11_S QUELCH_STATUS | New register. |
| 058h | PWM_RX_INFO.PWM_SYNC_DECODER12_S QUELCH_STATUS | New register. |
| 059h | PWM_RX_INFO.PWM_SYNC_DECODER13_S QUELCH_STATUS | New register. |
| 05Ah | PWM_RX_INFO.PWM_SYNC_DECODER14_S QUELCH_STATUS | New register. |
| 05Bh | PWM_RX_INFO.PWM_SYNC_DECODER15_S QUELCH_STATUS | New register. |

# 7. Revision History

| Revision | Date | Description |
|---|---|---|
| 1.00 | Apr 19, 2023 | Initial release. |

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