Register Descriptions

The register descriptions section describes the behavior and function of the customer-programmable non-volatile-memory registers in the 9FGV100x family of clock generators. Table 1 showcases the products under the 9FGV100x family.

Table 1. 9FGV100x Family Products

Product	Description	Package
9FGV1001	2 Ref outputs, 4 Diff outputs with 1 Integer output divider	24 pins
9FGV1002	2 Ref outputs, 4 Diff outputs with 1 Fractional output divider	24 pins
9FGV1004	2 Ref outputs, 2 Diff outputs with individual Integer output dividers and 2 Diff outputs with 1 Fractional output divider	24 pins

For details of product operation, refer to the product datasheet.

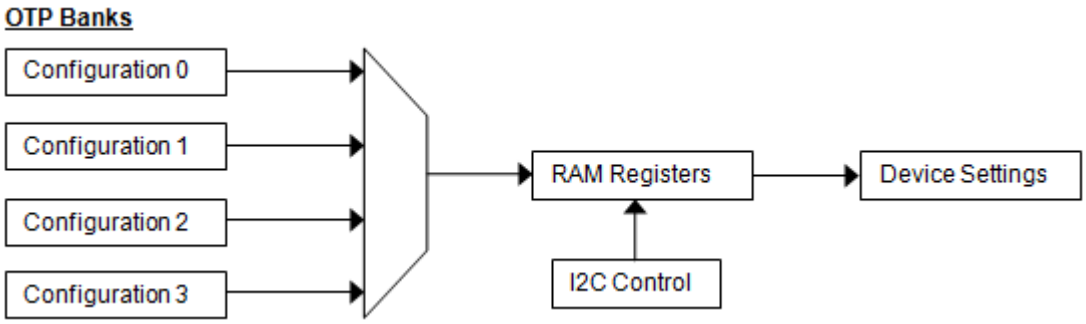
9FGV100x Clock Generator Register Set

The device contains volatile (RAM) 8-bit registers and non-volatile 8-bit registers (Figure 1). The non-volatile registers are One-Time Programmable (OTP) and will be pre-programmed at the factory with a custom dash-code configuration.

The device operates according to settings in the RAM registers. At power-up a pre-programmed configuration is transferred from OTP to RAM registers. The device behavior can then be modified by reprogramming the RAM registers through I2C.

The device can start up in “I2C mode” or in “Hardware Select Mode”, depending upon the status of the REF0_SEL_I2C# pin at power up. Also see the datasheet. I2C access is only possible when the device has started up in I2C mode. Startup in I2C mode is default when no pull-up is added to the REF0_SEL_I2C# pin. Pre-programming settings determine which of the 4 OTP banks is loaded into RAM registers at power up in I2C mode. Using I2C commands the configuration can be changed and there are also commands to reload a configuration from a different OTP bank.

Figure 1. Register Maps



User Configuration Table Selection

At power up, the voltage at REF0_SEL_I2C# pin 23 is latched by the device and used to select the state of the SEL0/SCL and SEL1/SDA pins (Table 2).

When a weak pull up (10kΩ) is placed on REF0_SEL_I2C#, the SEL0/SCL and SEL1/SDA pins will be configured as hardware select inputs, SEL0 and SEL1. Connecting SEL0 and SEL1 to VDDD and/or GND selects one of 4 configuration register sets, CFG0 through CFG3, which is then loaded into the non-volatile configuration registers to configure the clock synthesizer. The CFG0 through CFG3 configurations are preprogrammed at the factory according to customer specifications and assigned a specific (dash) part number.

When a weak pull down is placed on REF0_SEL_I2C# (or when it is left floating to use internal pulldown), the pins SEL0 and SEL1 will be configured as a I^2C interface's SDA and SCL slave bus. Configuration register set CFG0 is commonly loaded into the non-volatile configuration registers to configure the clock synthesizer but the device can be configured to load any of the other configurations. The host system can use the I^2C bus to update the volatile RAM registers to change the configuration, and to read status registers.

Table 2. Power-Up Setting of Hardware Select Pin vs I^2C Mode, and Default OTP Configuration Register

REF0_SEL_I2C# Strap at Power Up	SEL1/SDA pin	SEL0/SCL pin	Function
10kΩ pullup	0	0	OTP bank CFG0 used to initialize RAM configuration registers
	0	1	OTP bank CFG1 used to initialize RAM configuration registers
	1	0	OTP bank CFG2 used to initialize RAM configuration registers
	1	1	OTP bank CFG3 used to initialize RAM configuration registers
10kΩ pulldown or floating	SDA	SCL	I^2C bus enabled to access registers OTP bank CFG0 used to initialize RAM configuration registers

I^2C Interface and Register Access

When powered up in I^2C mode, the device allows access to internal RAM registers. The default device address is 0xD0 for 8 bits or 0x68 for 7 bits. The device can be preprogrammed for addresses in the range 0xD0-D2-D4-D6 for 8 bits or 0x68-69-6A-6B for 7 bits. The device acts as a slave device on the I^2C bus using one of the four I^2C addresses to allow multiple devices to be used in the system. The interface accepts byte-oriented block write and block read operations. Two address bytes specify the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP signal is received, at which point, all data received in the block write will be written simultaneously in the registers.

For full electrical I^2C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 100kΩ typical.

Figure 2. I^2C Interface and Register Access

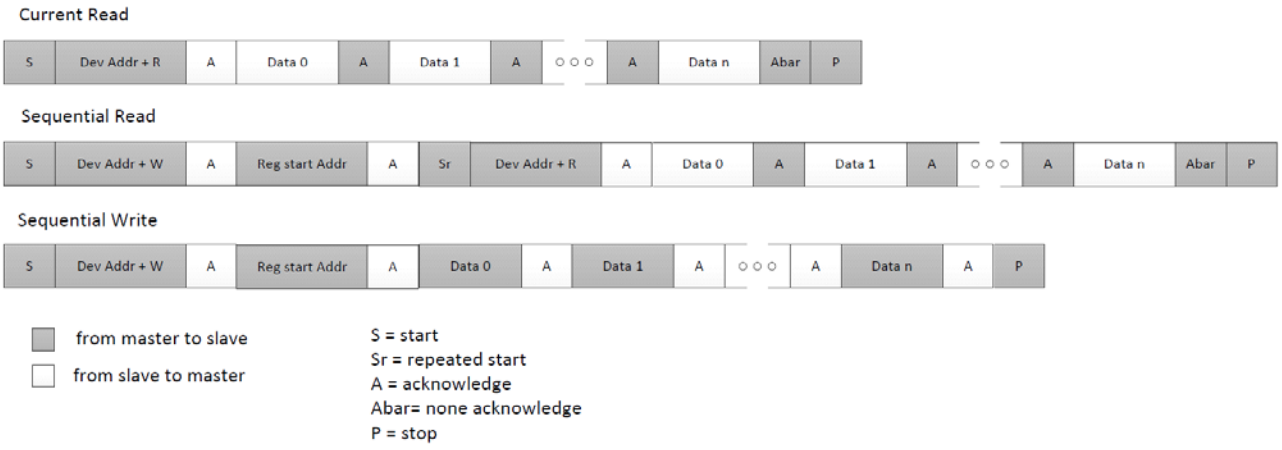


Table 3. RAM Overview

Register Address	Function Explanation
0x00	Device / I2C settings
0x01	REF Outputs settings
0x02	OUT3 output settings
0x03	
0x04	
0x05	OUT2 output settings
0x06	
0x07	
0x08	OUT1 output settings
0x09	
0x0A	
0x0B	OUT0 output settings
0x0C	
0x0D	
0x0E	Crystal Oscillator settings
0x0F	
0x10	FOD Spread Spectrum settings
0x11	
0x12	FOD Integer Value
0x13	FOD Fractional Value
0x14	
0x15	FOD Spread Spectrum settings
0x16	
0x17	FOD Miscellaneous
0x18	
0x19	
0x1A	PLL Miscellaneous
0x1B	
0x1C	PLL Loop Filter settings
0x1D	
0x1E	
0x1F	PLL Feedback Divider Value
0x20	Integer Output Divider Values
0x21	
0x22	
0x23	Reserved
0x24	Spread Spectrum Jitter Attenuator settings
0x25	Miscellaneous Device settings

RAM Register Map

Note1: To be able to read this info you already need to know the device address.

Note 2: These two bits show the configuration number 0~3 that will be loaded from OTP into registers at power up. When changing these bits through I2C you instruct the chip to load another configuration from OTP. This is useful for switching between OTP configurations when in I2C mode. This method is also used to step through each configuration for reading back OTP contents.

Table 4. RAM Register Map

Register Address		Register Bit	Function Explanation
Decimal	Hex		
00	0x00	7	Device preprogrammed? 0 = No , 1 = Yes
		[6..5]	I^2C Device address. 00=0xD0 / 0x68, 01=0xD2 / 0x69, 10=0xD4 / 0x6A, 11=0xD6 / 0x6B (1)
		[4..2]	Reserved
		[1..0]	Load Configuration number at power up. (2)
01	0x01	[7..6]	Enable REF outputs: 0x = Both REF0 and REF1 disabled (unused) 10 = REF0 enabled, REF1 disabled (unused) 11 = Both REF0 and REF1 enabled
		5	Reserved
		4	Behavior when REF is unused: 0 = Logic “0”, 1 = High Impedance (Tri-State)
		[3..2]	REF outputs Power Supply Voltage: 00=01=1.8V, 10=2.5V, 11=3.3V
		[1..0]	Reserved
02	0x02	7	Enable OUT3: 0 = Disabled (unused) , 1 = Enabled
		[6..4]	OUT3 Configuration: 000 = LPHCSL , Low Power HCSL 001 = CMOS1 , Single ended CMOS on true output pin. 011 = LVDS 100 = CMOS2 , Single ended CMOS on complementary output pin. 101 = CMOSD , Differential CMOS 111 = CMOSP , Two single ended CMOS outputs, in phase 010 and 110 are not used.
		[3..2]	OUT3 Power Supply Voltage: 00=01=1.8V, 10=2.5V, 11=3.3V
		[1..0]	Reserved
03	0x03	7	Reserved
		6	Behavior when OUT3 is unused: 0 = Logic “0”, 1 = High Impedance (Tri-State)
		5	OUT3 LPHCSL Slew Rate Control: 0 = Slow , 1 = Fast
		4	OUT3 LPHCSL Impedance Control: 0 = 85Ω Differential , 1 = 100Ω Differential
		[3..0]	OUT3 LPHCSL Amplitude Control: 650mVpp at 0000 ~ 950mVpp at 1111.
04	0x04	7	Reserved
		[6..4]	OUT3 LVDS Common Mode Control: 8uA at 000 ~ 11.5uA at 111
		3	Reserved
		[2..0]	OUT3 LVDS Amplitude Control: 30uA at 000 ~ 65uA at 111

Register Address		Register Bit	Function Explanation
Decimal	Hex		
05	0x05	7	Enable OUT2: 0 = Disabled (unused) , 1 = Enabled
		[6..4]	OUT2 Configuration: 000 = LPHCSL , Low Power HCSL 001 = CMOS1 , Single ended CMOS on true output pin. 011 = LVDS 100 = CMOS2 , Single ended CMOS on complementary output pin. 101 = CMOSD , Differential CMOS 111 = CMOSP , Two single ended CMOS outputs, in phase 010 and 110 are not used.
		[3..2]	OUT2 Power Supply Voltage: 00=01=1.8V, 10=2.5V, 11=3.3V
		[1..0]	Reserved
06	0x06	7	Reserved
		6	Behavior when OUT2 is unused: 0 = Logic “0”, 1 = High Impedance (Tri-State)
		5	OUT2 LPHCSL Slew Rate Control: 0 = Slow , 1 = Fast
		4	OUT2 LPHCSL Impedance Control: 0 = 85Ω Differential , 1 = 100Ω Differential
		[3..0]	OUT2 LPHCSL Amplitude Control: 650mVpp at 0000 ~ 950mVpp at 1111.
07	0x07	7	Reserved
		[6..4]	OUT2 LVDS Common Mode Control: 8uA at 000 ~ 11.5uA at 111
		3	Reserved
		[2..0]	OUT2 LVDS Amplitude Control: 30uA at 000 ~ 65uA at 111
08	0x08	7	Enable OUT1: 0 = Disabled (unused) , 1 = Enabled
		[6..4]	OUT1 Configuration: 000 = LPHCSL , Low Power HCSL 001 = CMOS1 , Single ended CMOS on true output pin. 011 = LVDS 100 = CMOS2 , Single ended CMOS on complementary output pin. 101 = CMOSD , Differential CMOS 111 = CMOSP , Two single ended CMOS outputs, in phase 010 and 110 are not used.
		[3..2]	OUT1 Power Supply Voltage: 00=01=1.8V, 10=2.5V, 11=3.3V
		[1..0]	Reserved
09	0x09	7	Reserved
		6	Behavior when OUT1 is unused: 0 = Logic “0”, 1 = High Impedance (Tri-State)
		5	OUT1 LPHCSL Slew Rate Control: 0 = Slow , 1 = Fast
		4	OUT1 LPHCSL Impedance Control: 0 = 85Ω Differential , 1 = 100Ω Differential
		[3..0]	OUT1 LPHCSL Amplitude Control: 650mVpp at 0000 ~ 950mVpp at 1111.
10	0x0A	7	Reserved
		[6..4]	OUT1 LVDS Common Mode Control: 8uA at 000 ~ 11.5uA at 111
		3	Reserved
		[2..0]	OUT1 LVDS Amplitude Control: 30uA at 000 ~ 65uA at 111

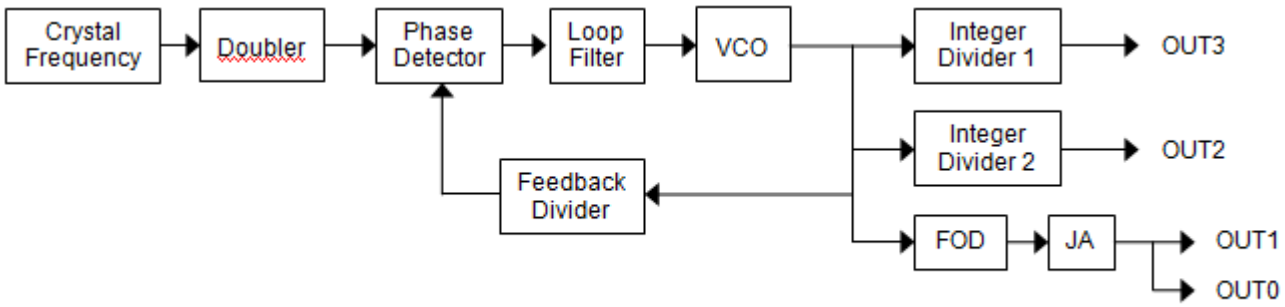
Register Address		Register Bit	Function Explanation
Decimal	Hex		
11	0x0B	7	Enable OUT0: 0 = Disabled (unused) , 1 = Enabled
		[6..4]	OUT0 Configuration: 000 = LPHCSL , Low Power HCSL 001 = CMOS1 , Single ended CMOS on true output pin. 011 = LVDS 100 = CMOS2 , Single ended CMOS on complementary output pin. 101 = CMOSD , Differential CMOS 111 = CMOSP , Two single ended CMOS outputs, in phase 010 and 110 are not used.
		[3..2]	OUT0 Power Supply Voltage: 00=01=1.8V, 10=2.5V, 11=3.3V
		[1..0]	Reserved
12	0x0C	7	Reserved
		6	Behavior when OUT0 is unused: 0 = Logic “0”, 1 = High Impedance (Tri-State)
		5	OUT0 LPHCSL Slew Rate Control: 0 = Slow , 1 = Fast
		4	OUT0 LPHCSL Impedance Control: 0 = 85Ω Differential , 1 = 100Ω Differential
		[3..0]	OUT0 LPHCSL Amplitude Control: 650mVpp at 0000 ~ 950mVpp at 1111.
13	0x0D	7	Reserved
		[6..4]	OUT0 LVDS Common Mode Control: 8uA at 000 ~ 11.5uA at 111
		3	Reserved
		[2..0]	OUT0 LVDS Amplitude Control: 30uA at 000 ~ 65uA at 111
14	0x0E	7	Crystal Oscillator LDO: 0 = Disabled , 1 = Enabled
		6	Reserved
		[5..0]	Crystal Oscillator X1 pin capacitance: Cap (pF) = 10 + 0.44 * Bits[4..0] + 7.04 * Bit[5] Appendix 3: Crystal Load Capacitance Registers for Crystal Oscillator Load Capacitance configuration.
15	0x0F	7	Crystal Oscillator Circuit: 0 = Disabled , 1 = Enabled
		6	Reserved
		[5..0]	Crystal Oscillator X2 pin capacitance: Cap (pF) = 10 + 0.44 * Bits[4..0] + 7.04 * Bit[5]
16	0x10	7	FOD Spread Spectrum: 0 = Disabled , 1 = Enabled
		[6..4]	Reserved
		[3..0]	FOD Spread Spectrum Period, bits [11..8]. See Appendix 2 for Spread Spectrum configuration
17	0x11	[7..0]	FOD Spread Spectrum Period, bits [7..0]
18	0x12	[7..0]	FOD Integer Value. See Appendix 1 for Fractional Divider configuration
19	0x13	[7..0]	FOD Fractional Value, bits [15..8]
20	0x14	[7..0]	FOD Fractional Value, bits [7..0]
21	0x15	[7..0]	FOD Spread Spectrum Step, bits [15..8]
22	0x16	[7..0]	FOD Spread Spectrum Step, bits [7..0]
23	0x17	[7..0]	Reserved

Register Address		Register Bit	Function Explanation
Decimal	Hex		
24	0x18	7	FOD Reset-B: 0 = Hold FOD in Reset Mode , 1 = Release FOD. Toggle to 0 and back to 1 to apply a reset or restart of the FOD.
		[6..2]	Reserved
		1	FOD Integer Mode: 0 = Use fractional settings for a fractional output divider value. 1 = Run output divider in Integer Mode in case the output division is an integer, for the best performance.
		0	Enable FOD: 0 = FOD is Disabled , 1 = FOD is Enabled.
25	0x19	[7..0]	Reserved
26	0x1A	7	PLL, VCO Band Calibration Start. Toggle to 0 and back to 1 to trigger a calibration. The calibration engages at the moment the bit moves from 0 to 1. The calibration finds the optimum VCO band for the current VCO frequency.
		6	Override VCO Band: 0 = Use Calibrated VCO Band , 1 = Use VCO Band value in bits [5..0].
		[5..0]	VCO Band Value. See bit 6.
27	0x1B	7	Enable VCO: 0 = VCO Disabled , 1 = VCO Enabled
		6	Enable Charge Pump: 0 = CP Disabled , 1 = CP Enabled.
		5	Enable PLL Bias: 0 = PLL Bias Disabled , 1 = PLL Bias Enabled
		4	Bypass 3rd Pole in Loop Filter: 0 = Use 3rd Pole , 1 = 3rd Pole Bypassed
		[3..0]	Reserved
28	0x1C	[7..4]	Loop Filter R-zero value
		[3..0]	Reserved
29	0x1D	[7..0]	Reserved
30	0x1E	[7..4]	Reserved
		[3..0]	Charge Pump Current
31	0x1F	[7..0]	PLL Feedback Divider Value.
32	0x20	[7..0]	Integer Divider value for OUT3, bits [7..0]
33	0x21	[7..0]	Integer Divider value for OUT2, bits [7..0]
34	0x22	[7..4]	Integer Divider value for OUT2, bits [11..8]
		[3..0]	Integer Divider value for OUT3, bits [11..8]
35	0x23	[7..0]	Reserved
36	0x24	[7..3]	Reserved
		2	Spread Spectrum Jitter Attenuator: 0 = Disabled , 1 = Enabled
		[1..0]	SS Jitter Attenuator configuration. See Appendix 2: Fractional Output Divider and Spread Spectrum.

Register Address		Register Bit	Function Explanation
Decimal	Hex		
37	0x25	7	Reserved
		6	Enable Integer Output Dividers: 0 = Disabled , 1 = Enabled
		5	Enable Crystal Frequency Doubler: 0 = Disabled , 1 = Enabled
		4	Reserved
		3	OUT3 Integer Divider Enable: 0 = Disabled , 1 = Enabled
		2	OUT2 Integer Divider Enable: 0 = Disabled , 1 = Enabled
		[1..0]	Reserved

Block Diagrams

Figure 3. 9FGV1004 Block Diagram



"FOD" is Fractional Output Divider and "JA" is Jitter Attenuator for use with Spread Spectrum only.

Figure 4. 9FGV1002 Block Diagram

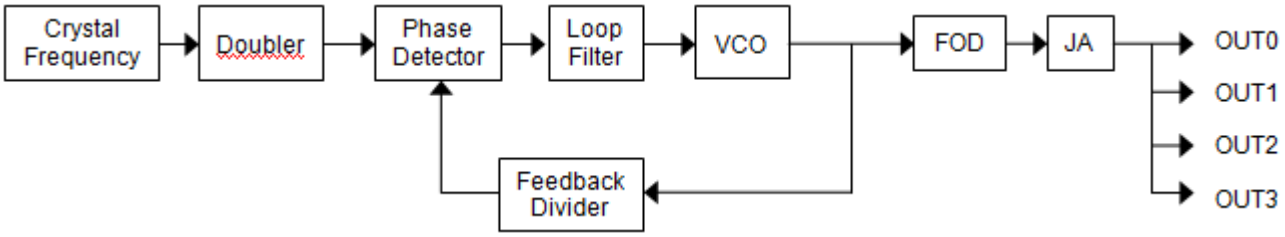
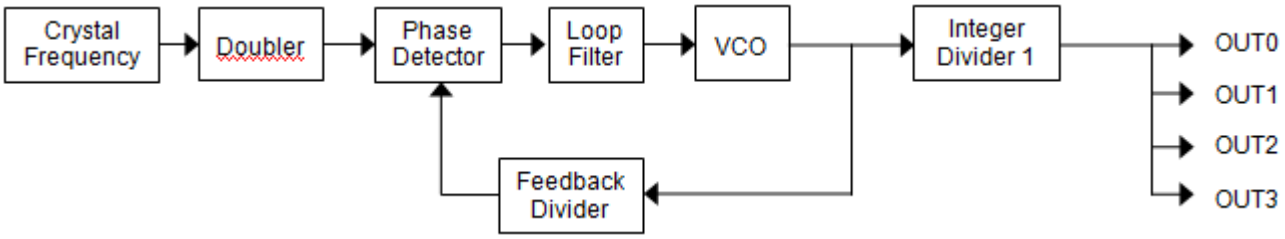


Figure 5. 9FGV1001 Block Diagram



Equations

$F_{VCO} = F_{CRYSTAL} \times$ Feedback Divider (see register 0x1F)

9FGV1004: $F_{OUT3} = F_{VCO}$ / Integer Divider 1 (see registers 0x20 and 0x22)

$F_{OUT2} = F_{VCO}$ / Integer Divider 2 (see registers 0x21 and 0x22)

$F_{OUT0} = F_{OUT1} = F_{VCO} \times$ JA Multiplier / (2 × FOD) (see registers 0x10 ~ 0x18 and 0x24)

9FGV1002: $F_{OUT0} = F_{OUT1} = F_{OUT2} = F_{OUT3} = F_{VCO} \times$ JA Multiplier / (2 × FOD) (see registers 0x10 ~ 0x18 and 0x24)

9FGV1001: $F_{OUT0} = F_{OUT1} = F_{OUT2} = F_{OUT3} = F_{VCO}$ / Integer Divider 1 (see registers 0x20 and 0x22)

Limits

$F_{CRYSTAL}$: 10MHz ~ 40MHz

F_{VCO}: 2300MHz ~ 2600MHz

Integer Divider 1 and 2: 8 ~ 4095

FOD: 4 ~ 255

Appendix 1: Fractional Output Divider Configuration

The Fractional Output Divider (FOD) is composed of an 8 bit integer portion (address 0x12) and a 16 bit fractional portion (addresses 0x13 and 0x14).

FOD value P = INT(P) + FRAC(P) = F_{VCO} / (2 × F_{OUT}) (1)

FOD Integer [7..0] = DEC2HEX(INT(P)) (2)

The FOD divides the VCO frequency F_{VCO} down to the desired output frequency F_{OUT}. Please note the additional /2 between the VCO and the FOD.

Convert FRAC(P) to hex with Eq.2 where ROUND2INT means to round to the nearest integer. The round-off error of P in ppm is the output frequency error in ppm.

FOD Fraction [15..0] = DEC2HEX(ROUND2INT(2^{16}×FRAC(P))) (3)

Example: If the VCO is 2500MHz and the desired output frequency is 148.5MHz, the FOD value is 2500/(2×148.5)=8.4175084.

The integer portion is 8 so address 0x12 will be 08-hex.

The fractional portion is 0.4175084.

FOD Fraction [15..0] = DEC2HEX(ROUND2INT(2^{16}×0.4175084) = DEC2HEX(ROUND2INT(27361.83))

= DEC2HEX(27362) = 6A E2

Address 0x13 = 6A-hex and address 0x14 = E2-hex.

There is a small error from the rounding. The actual FOD value is 8 + 27362 / 2^{16} = 8.4175110.

The rounding error is 8.4175110 / 8.4175084 - 1 = 0.31ppm.

Appendix 2: Fractional Output Divider and Spread Spectrum

Spread spectrum capability is contained within the Fractional-N output divider associated with OUT0 and OUT1. When applied, triangle wave modulation of any spread spectrum amount, SS%AMT up to ±2.5% center spread and -5% down spread between 30 and 63kHz may be generated, independent of the output clock frequency. Six variables define Spread Spectrum in the FOD (see Table 5).

Table 5. Spread Spectrum Variables in the FOD

Name	Function	RAM Register	Note
SS Enable	Spread spectrum control enable	0x10 [7]	When SS-Enable = 0, contents of Period and Step registers are Don't Care. When SS-Enable = 1, the SS Jitter Attenuator will also enable.
FOD Integer	Integer portion of the FOD value P	0x12 [7..0]	See equations 4 and 5 below.
FOD Fraction	Fractional portion of the FOD value P	0x13 [7..0] = Fraction [15..8] 0x14 [7..0] = Fraction [7..0]	See equations 4 and 5 below.
SS Period	Spread spectrum modulation period	0x10 [3..0] = Period [11..8] 0x11 [7..0] = Period [7..0]	Total 12 bits for the Period Defined as half the reciprocal of the modulation frequency and measured in cycles of the FOD output frequency. See equation 6 below.
SS Step	Modulation step size	0x15 [7..0] = Step [15..8] 0x16 [7..0] = Step [7..0]	Sets the time rate of change or time slope of the output clock frequency. See equation 8 below.
SS Jitter Attenuator	Jitter Attenuator Configuration	0x24 [1..0] = JA [1..0]	The SS Jitter Attenuator needs to be configured based upon the FOD output frequency. The JA may divide down or multiply up the frequency to the output.

Table 6. Spread Spectrum Jitter Attenuator Configuration

Output Frequency	JA [1..0]	Frequency Multiplier	FOD Frequency
15MHz ~ 30MHz	00	× 0.25	60MHz ~ 120MHz
60MHz ~ 120MHz	01	× 1	60MHz ~ 120MHz
120.0001MHz ~ 150MHz	10	× 1.25	96.0001MHz ~ 120MHz
150.0001MHz ~ 300MHz	11	× 2	75.0001MHz ~ 150MHz

Make sure to adjust the FOD output frequency based upon the Frequency Multiplier value of the Jitter Attenuator. This is only needed when Spread Spectrum is enabled. Please consult the factory for output frequencies not covered by the ranges in Table 6.

Equations

Calculate the FOD output frequency from the desired clock output frequency and the Jitter Attenuator Frequency Multiplier:

FOD $F_{OUT} = F_{CLOCK}$ / Multiplier

To calculate the spread spectrum registers, first determine the value in decimal of the FOD output divider P. The value of P needs to be offset so F_{VCO} / (2×P) is the bottom point of the triangle modulation wave. For Down Spread the value of P is offset with the Spread percentage and for Center Spread the value of P is offset with half of the Spread percentage.

Down Spread:

FOD value P = INT(P) + FRAC(P) = (1 + SS% / 100) × (F_{VCO} / (2 × F_{OUT})) (4)

See equations 2 and 3 in Appendix 1: Fractional Output Divider Configuration for address 0x12, 0x13 and 0x14 settings.

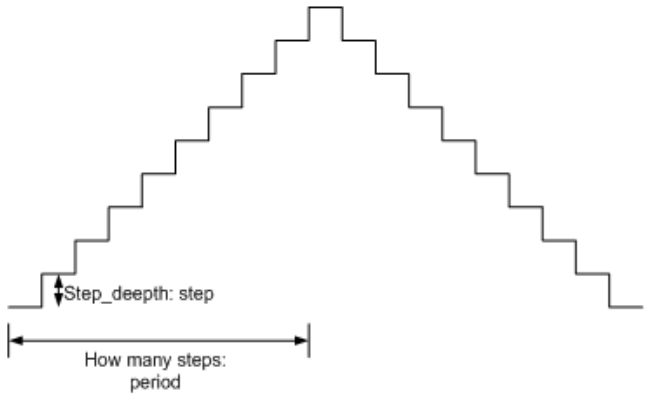
Center Spread:

FOD value P = INT(P) + FRAC(P) = (1 + SS% / 200) × (F_{VCO} / (2 × FOUT)) (5)

Please note that the SS% value is the peak-to-peak value so with +/-1.0% center spread, the SS% value is 2.0%

Consider one cycle of down spread triangular modulation; the FOD value is ramped down linearly from the P value followed by a linear ramp back up to the value of P. The modulated value of the FOD is always smaller than or equal to the value of P.

Figure 6. Spread Step and Period



The SS modulation Period is defined as the amount of time steps it takes for the triangle to move from its lowest to its highest point. The Period is essentially half of the modulation cycle or modulation rate. One time step is defined as one cycle of the output frequency FOUT. The Period register setting needs to be half of the Period decimal value so essentially ¼ of the modulation cycle.

Period (decimal) = F_{OUT} / (2×F_{SS}) (6)

Period [11..0] = DEC2HEX(ROUND2INT(Period(decimal) / 2)) (7)

Given the required Spread percentage and the Period value, we can calculate the Step size:

Step (decimal) = (SS% / 100) × P / Period (8)

Step [15..0] = DEC2HEX(ROUND2INT(2^{24} × Step(decimal))) (9)

Example 1 with Down Spread :

F_{VCO}=2500MHz, F_{CLOCK}=100MHz with -0.5% Down Spread and 31.5KHz Modulation Rate.

At 100MHz the JA Multiplier is 1 so $F_{OUT} = F_{CLOCK}$ and the JA setting is JA[1..0] = 01 binary.

FOD value P = (1 + SS% / 100) × (F_{VCO} / (2 × F_{OUT})) = (1 + 0.5/100) × (2500 / (2×100)) = 1.005 × 12.5 = 12.5625

FOD Integer [7..0] = DEC2HEX(12) = 0C-hex

FOD Fraction [15..0] = DEC2HEX(ROUND2INT(216×0.5625)) = DEC2HEX(ROUND2INT(36864)) = 90 00 hex

Period (decimal) = FOUT / (2×F_{SS}) = 100 / (2×0.0315) = 1587.3016

Period [11:0] = DEC2HEX(ROUND2INT(Period(decimal) / 2)) = DEC2HEX(794) = 3 1A hex

Step (decimal) = (SS% / 100) × P / Period = (0.5 / 100) × 12.5625 / 1587.3016 = 3.95719×10^{-5}

Step [15..0] = DEC2HEX(ROUND2INT(2^{24} × Step(decimal))) = DEC2HEX(664) = 02 98 hex

Example 2 with Center Spread :

F_{VCO}=2500MHz, F_{OUT}=27MHz with +/-1.0% Center Spread and 31.5KHz Modulation Rate.

At 27MHz the JA Multiplier is 0.25 so $F_{OUT} = 4 \times F_{CLOCK}$ = 108MHz and the JA setting is JA[1..0] = 00 binary.

FOD value P = (1 + SS% / 200) × (F_{VCO} / (2 × F_{OUT})) = (1 + 2.0/200) × (2500 / (2×108)) = 1.01 × 11.574074 = 11.689815

FOD Integer [7..0] = DEC2HEX(11) = 0B-hex

FOD Fraction [15..0] = DEC2HEX(ROUND2INT(2^{16}×0.689815)) = DEC2HEX(ROUND2INT(45207.7)) = B0 98 hex

Period (decimal) = FOUT / (2×F_{SS}) = 108 / (2×0.0315) = 1714.2857

Period [11:0] = DEC2HEX(ROUND2INT(Period(decimal) / 2)) = DEC2HEX(857) = 3 59 hex

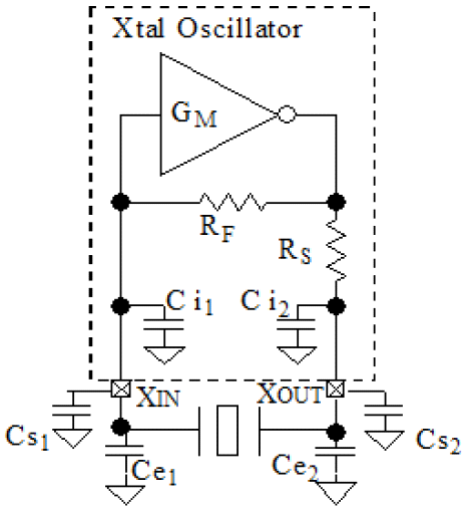
Step (decimal) = (SS% / 100) × P / Period = (2.0 / 100) × 11.689815 / 1714.2857 = 1.363812×10^{-4}

Step [15..0] = DEC2HEX(ROUND2INT(2^{24} × Step(decimal))) = DEC2HEX(2288) = 08 F0 hex

Appendix 3: Crystal Load Capacitance Registers

Registers 0x0E and 0x0F contain Crystal X1 and X2 Load capacitor settings that are used to add load capacitance to X1 and X2 (a.k.a. XIN and XOUT) respectively.

Figure 7. Crystal Oscillator Circuit



Ci1 and Ci2 are on-chip capacitors that are programmable.

Cs is stray capacitance in the PCB and Ce is external capacitors for frequency fine tuning or for achieving load capacitance values beyond the range of the on-chip programmability. Please consult the factory when adding Ce capacitors. The oscillator gain reduces with added capacitance and there may be crystal oscillator startup issues when adding too much capacitance.

All these capacitors combined make the load capacitance for the crystal. Capacitance on pin XIN or X1: Cx1 = Ci1+Cs1+Ce1

Capacitance on pin XOUT or X2: Cx2 = Ci2+Cs2+Ce2

Total Crystal Load Capacitance CL = Cx1×Cx2 / (Cx1+Cx2)

For optimum balance and oscillator gain it is recommended to design Cx1 = Cx2. In that case CL = Cx1 / 2 = Cx2 / 2.

The capacitance per pin X1 or X2 is: Cap (pF) = 10 + 0.44 * Bits[4..0] + 7.04 * Bit[5]

This includes an estimated Cs1 = Cs2 = 1.5pF.

When designing Cx1 = Cx2, the formula for CL is: CL (pF) = 5 + 0.22 × Bits[4..0] + 3.52 × Bit[5]

The minimum CL value at Cx1 = Cx2 = '00 0000'-binary = 5.0pF

The maximum CL value at Cx1 = Cx2 = '11 1111'-binary = 5 + 0.22 × 31 + 3.52 × 1 = 15.34pF (not counting Ce)

Example: For a crystal CL of 8pF, the registers can be programmed as follows:

CL (pF) = 5 + 0.22 × 14 + 3.52 × 0 = 8.08pF (nearest to 8.0pF)

So for CL = 8pF the recommended settings are Cx1[5..0] = Cx2[5..0] = 14 or '00 1110'-binary

Registers 0x0E = 0x0F = 8E-hex (= '1000 1110' binary)

Revision History

Table 7. Revision History

Revision Date	Description of Change
November 18, 2016	Initial release

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