



Networking & Communications Timing Division  
**82V3910 WANPLL – Application Programmer’s  
Interface Reference Manual**

**82V3910 WANPLL – Application Programmer’s Interface  
Reference Manual**

Version 1.1

September 23, 2013

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1.0	May 23, 2013	Initial release.
1.1	September 23, 2013	- Add support for APLL pre-divider value 1. - Update Ethernet FEC frequency configuration.

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# Chapter 1

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# Chapter 4

## Module Documentation

### 4.1 DPLL Private header file

Functions in this group are related to DPLL provisioning.

#### Data Structures

- struct [T\\_IDTPathConfiguration](#)  
*Structure containing output path configuration.*

#### Macros

- #define [SonetGigEthSel\\_NUMMAX](#) 2  
*Constant defining number of instances of SonetGigEth selectors.*

#### Enumerations

- enum [T\\_idtT0DpllSelectorA](#) {  
[T0DpllSelA\\_16E1](#), [T0DpllSelA\\_16T1](#), [T0DpllSelA\\_GSM](#), [T0DpllSelA\\_OBSAI](#),  
[T0DpllSelA\\_MAX](#) }  
*Enumerated type listing T0 DPLL selector A options.*
- enum [T\\_idtT0DpllSelectorB](#) {  
[T0DpllSelB\\_12E1](#), [T0DpllSelB\\_GPS](#), [T0DpllSelB\\_E3](#), [T0DpllSelB\\_T3](#),  
[T0DpllSelB\\_MAX](#) }  
*Enumerated type listing T0 DPLL selector B options.*
- enum [T\\_idtT4DpllSelectorA](#) {  
[T4DpllSelA\\_16E1](#), [T4DpllSelA\\_16T1](#), [T4DpllSelA\\_GSM](#), [T4DpllSelA\\_GPS](#),  
[T4DpllSelA\\_MAX](#) }  
*Enumerated type listing T4 DPLL selector A options.*
- enum [T\\_idtT4DpllSelectorB](#) {  
[T4DpllSelB\\_12E1](#), [T4DpllSelB\\_24T1](#), [T4DpllSelB\\_E3](#), [T4DpllSelB\\_T3](#),  
[T4DpllSelB\\_MAX](#) }  
*Enumerated type listing T4 DPLL selector B options.*
- enum [T\\_idtSonetGigEthSelector](#) {  
[SonetGigEthSel\\_T0DpllSonet](#) = 0, [SonetGigEthSel\\_T4DpllSonet](#) = 4, [SonetGigEthSel\\_T0Dpll10GbE](#) = 8,  
[SonetGigEthSel\\_T0Dpll10GbE\\_6664](#) = 9,  
[SonetGigEthSel\\_T4Dpll10GbE](#) = 12, [SonetGigEthSel\\_T4Dpll10GbE\\_6664](#) = 13, [SonetGigEthSel\\_MAX](#) }  
*Enumerated type listing Sonet/GigE path selection options.*

## Variables

- const [T\\_IDTPathConfiguration](#) `IDTDpll_pathConfigurationNULL_c`  
*Output path configuration no path constant.*
- const [T\\_idtSonetGigEthSelector](#) `IDTDpll_sonetGigEthPathConfig2Bitfield [Dpll_MAX][SonetGigEthOutput_MAX]`  
*Table to translate from Sonet/GigE path configuration to bitfield value.*

### 4.1.1 Detailed Description

Functions in this group are related to DPLL provisioning.

### 4.1.2 Macro Definition Documentation

#### 4.1.2.1 #define SonetGigEthSel\_NUMMAX 2

Constant defining number of instances of SonetGigEth selectors.

Definition at line 111 of file Dpll.h.

### 4.1.3 Enumeration Type Documentation

#### 4.1.3.1 enum T\_idtSonetGigEthSelector

Enumerated type listing Sonet/GigE path selection options.

Enumerator

***SonetGigEthSel\_T0DpllSonet*** From T0, 622.08MHz  
***SonetGigEthSel\_T4DpllSonet*** From T4, 622.08MHz  
***SonetGigEthSel\_T0Dpll10GbE*** From T0, 625.00MHz  
***SonetGigEthSel\_T0Dpll10GbE\_6664*** From T0, 625\*66/64MHz  
***SonetGigEthSel\_T4Dpll10GbE*** From T4, 625.00MHz  
***SonetGigEthSel\_T4Dpll10GbE\_6664*** From T4, 625\*66/64MHz  
***SonetGigEthSel\_MAX***

Definition at line 98 of file Dpll.h.

#### 4.1.3.2 enum T\_idtT0DpllSelectorA

Enumerated type listing T0 DPLL selector A options.

Enumerator

***T0DpllSelA\_16E1*** 32.768MHz  
***T0DpllSelA\_16T1*** 24.704MHz  
***T0DpllSelA\_GSM*** 26MHz  
***T0DpllSelA\_OBSAI*** 30.72MHz  
***T0DpllSelA\_MAX***

Definition at line 58 of file Dpll.h.

## 4.1.3.3 enum T\_idtT0DpllSelectorB

Enumerated type listing T0 DPLL selector B options.

Enumerator

```
T0DpllSelB_12E1 24.576MHz
T0DpllSelB_GPS GPS
T0DpllSelB_E3 34.368MHz
T0DpllSelB_T3 44.736MHz
T0DpllSelB_MAX
```

Definition at line 68 of file Dpll.h.

## 4.1.3.4 enum T\_idtT4DpllSelectorA

Enumerated type listing T4 DPLL selector A options.

Enumerator

```
T4DpllSelA_16E1 32.768MHz
T4DpllSelA_16T1 24.704MHz
T4DpllSelA_GSM 26MHz
T4DpllSelA_GPS GPS
T4DpllSelA_MAX
```

Definition at line 78 of file Dpll.h.

## 4.1.3.5 enum T\_idtT4DpllSelectorB

Enumerated type listing T4 DPLL selector B options.

Enumerator

```
T4DpllSelB_12E1 24.576MHz
T4DpllSelB_24T1 37.056MHz
T4DpllSelB_E3 34.368MHz
T4DpllSelB_T3 44.736MHz
T4DpllSelB_MAX
```

Definition at line 88 of file Dpll.h.

## 4.1.4 Variable Documentation

## 4.1.4.1 const T\_IDTPathConfiguration IDTDpll\_pathConfigurationNULL\_c

Output path configuration no path constant.

Definition at line 62 of file DpllCnfg.c.

## 4.1.4.2 const T\_idtSonetGigEthSelector IDTDpll\_sonetGigEthPathConfig2Bitfield[Dpll\_MAX][SonetGigEthOutput\_MAX]

Table to translate from Sonet/GigE path configuration to bitfield value.

Definition at line 91 of file DpllCnfg.c.

## 4.2 DPLL Function Module

Functions in this group are related to DPPL provisioning.

### Macros

- #define `DCO_PPT2DCOUNTS` 11  
*Conversion from parts per trillion to register unit value for DCO offset.*
- #define `DCO_MAX_PPT` 92274677  
*Max DCO value.*
- #define `DCO_MIN_PPT` -92274688  
*Max DCO value.*
- #define `IDT_TRANSLATE_EXT_TO_INT_DPLL`(hdlr, ext, internal)  
*Utility macro to check if DPLL instance is supported and to translated from DPLL instance to DPLL type.*

### Enumerations

- enum `T_idtFreqMonFactor` {  
`FreqMonFactor_0p0032` = 0, `FreqMonFactor_0p0064` = 1, `FreqMonFactor_0p0127` = 2, `FreqMonFactor_0p0257` = 3,  
`FreqMonFactor_0p0514` = 4, `FreqMonFactor_0p1030` = 5, `FreqMonFactor_0p2060` = 6, `FreqMonFactor_0p4120` = 7,  
`FreqMonFactor_0p8230` = 8, `FreqMonFactor_1p6460` = 9, `FreqMonFactor_3p2920` = 10, `FreqMonFactor_3p8100` = 11,  
`FreqMonFactor_4p6000` = 12, `FreqMonFactor_MAX` }  
*Enumerated list indicating frequency monitoring factor.*
- enum `T_idtBandwidthLimitStage` { `dpIIBandwidthLimitStart`, `dpIIBandwidthLimitAcquire`, `dpIIBandwidthLimitLocked`, `dpIIBandwidthLimit_MAX` }  
*Enumerated list used for selecting bandwidth limiting stages.*
- enum `T_idtDampingFactor` {  
`DampingFactor_1p2` = 1, `DampingFactor_2p5` = 2, `DampingFactor_5` = 3, `DampingFactor_10` = 4,  
`DampingFactor_20` = 5, `DampingFactor_MAX` }  
*Enumerated list showing options for bandwidth damping factor.*
- enum `T_idtDpllBandwidth` {  
`dpIIBandwidth_0p5mHz` = 0, `dpIIBandwidth_1mHz` = 1, `dpIIBandwidth_2mHz` = 2, `dpIIBandwidth_4mHz` = 3,  
`dpIIBandwidth_8mHz` = 4, `dpIIBandwidth_15mHz` = 5, `dpIIBandwidth_30mHz` = 6, `dpIIBandwidth_60mHz` = 7,  
`dpIIBandwidth_0p1Hz` = 8, `dpIIBandwidth_0p3Hz` = 9, `dpIIBandwidth_0p6Hz` = 10, `dpIIBandwidth_1p2Hz` = 11,  
`dpIIBandwidth_2p5Hz` = 12, `dpIIBandwidth_4Hz` = 13, `dpIIBandwidth_8Hz` = 14, `dpIIBandwidth_18Hz` = 15,  
`dpIIBandwidth_35Hz` = 16, `dpIIBandwidth_70Hz` = 17, `dpIIBandwidth_560Hz` = 18, `dpIIBandwidth_MAX` }  
*List of options for DPLL bandwidth.*
- enum `T_idtPhaseSlope` {  
`phaseSlope_gr1244st3` = 0, `phaseSlope_gr1244st3e` = 1, `phaseSlope_gr813` = 2, `phaseSlope_noLimit` = 3,  
`phaseSlope_MAX` }  
*Enumerated type listing phase slope.*
- enum `T_idtDpllOperMode` {  
`Automatic_Mode` = 0, `Force_FreeRun_Mode` = 1, `Force_Holdover_Mode` = 2, `Force_Locked_Mode` = 4,  
`Force_Pre_Locked2_Mode` = 5, `Force_Pre_Locked_Mode` = 6, `Force_Lost_Phase_Mode` = 7, `Dco_Mode` = 8,  
`DpllOperMode_MAX` }  
*Enumerated type for DPLL operation mode.*

- enum `T_idtCoarsePhaseLimit` {  
`coarsePhaseLimit_1 = 0, coarsePhaseLimit_3 = 1, coarsePhaseLimit_7 = 2, coarsePhaseLimit_15 = 3,`  
`coarsePhaseLimit_31 = 4, coarsePhaseLimit_63 = 5, coarsePhaseLimit_127 = 6, coarsePhaseLimit_255 =`  
`7,`  
`coarsePhaseLimit_511 = 8, coarsePhaseLimit_1023 = 9, coarsePhaseLimit_MAX }`  
*Enumerated type listing coarse phase limits.*
- enum `T_idtFinePhaseLimit` {  
`finePhaseLimit_45_90degree = 1, finePhaseLimit_90_180degree = 2, finePhaseLimit_180_360degree = 3,`  
`finePhaseLimit_20_25nanosec = 4,`  
`finePhaseLimit_60_65nanosec = 5, finePhaseLimit_120_125nanosec = 6, finePhaseLimit_950_955nanosec`  
`= 7, finePhaseLimit_MAX }`  
*Enumerated type listing fine phase limits.*
- enum `T_idtDpllHoldover` {  
`Holdover_Instantaneous = 0, Holdover_Slow_Average = 2, Holdover_Fast_Average = 3, Holdover_Manual =`  
`4,`  
`Holdover_MAX }`  
*Enumerated type listing holdover modes.*
- enum `T_idtTemp_holdover` {  
`Temp_Same_As_Full_Holdover = 0, Temp_Holdover_Instantaneous = 1, Temp_Holdover_Fast_Average = 2,`  
`Temp_Holdover_Slow_Average = 3,`  
`Temp_Holdover_MAX }`  
*Enumerated type listing temp-holdover modes.*
- enum `T_idtOperDpllMode` {  
`OperDpllMode_FreeRun = 1, OperDpllMode_HoldOver = 2, OperDpllMode_Locked = 4, OperDpllMode_Pre-`  
`Locked2 = 5,`  
`OperDpllMode_PreLocked = 6, OperDpllMode_LostPhase = 7 }`  
*Enumerated type listing DPLL operational modes.*
- enum `T_idtSonetGigEthOutput` { `SonetGigEthOutput_Sonet, SonetGigEthOutput_10GbE, SonetGigEth-`  
`Output_10GbE_6664, SonetGigEthOutput_MAX }`  
*Enumerated type listing possible Sonet/GigE output frequencies.*
- enum `T_idtDpllOutputSelectorA` {  
`DPLLOutputSelA_16E1, DPLLOutputSelA_16T1, DPLLOutputSelA_GSM, DPLLOutputSelA_OBSAI,`  
`DPLLOutputSelA_GPS, DPLLOutputSelA_MAX }`  
*Enumerated type listing DPLL selector A paths.*
- enum `T_idtDpllOutputSelectorB` {  
`DPLLOutputSelB_12E1, DPLLOutputSelB_GPS, DPLLOutputSelB_E3, DPLLOutputSelB_T3,`  
`DPLLOutputSelB_24T1, DPLLOutputSelB_MAX }`  
*Enumerated type listing DPLL selector B paths.*
- enum `T_idtDpllPpsPhasePostion` { `PpsPhasePostion_0degree, PpsPhasePostion_50ns, PpsPhasePostion_-`  
`100ns, PpsPhasePostion_MAX }`  
*Enumerated type listing PPS phase options.*
- enum `T_idtDpllPpsPulseWidth` {  
`PpsPulseWidth_0pt5sec, PpsPulseWidth_10ns, PpsPulseWidth_200ns, PpsPulseWidth_400ns,`  
`PpsPulseWidth_800ns, PpsPulseWidth_1us, PpsPulseWidth_20us, PpsPulseWidth_50us,`  
`PpsPulseWidth_100us, PpsPulseWidth_200us, PpsPulseWidth_1pt2ms, PpsPulseWidth_800us,`  
`PpsPulseWidth_MAX }`  
*Enumerated type listing PPS pulse width.*

## Functions

- `T_idtDpllType IDTDpll_GetTypeOfDpll` (`T_idtDrvHdlr hdlr, T_idtDpllInstance nDpll`)  
*Function to determine type of DPLL give a DPLL instance.*
- `void IDTDpll_SetAutoSelInput` (`T_idtDrvHdlr hdlr, T_idtDpllInstance nDpll, T_osUjnt8 mode`)  
*Set the DPLL as automatic reference clock selection.*

- T\_osUInt8 [IDTDpll\\_GetAutoSelInput](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Get automatic input selection status.*
- void [IDTDpll\\_SetForceSelInput](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_osUInt8 nInputNo)  
*Set the DPLL to force to lock to a specified reference clock.*
- T\_osUInt8 [IDTDpll\\_GetForceSelInput](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Set the DPLL to force to lock to a specified reference clock.*
- T\_osUInt8 [IDTDpll\\_Get1stPriorityInput](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Get input number of a valid clock with the highest priority.*
- T\_osUInt8 [IDTDpll\\_Get2ndPriorityInput](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Get input number of a valid clock with the second highest priority.*
- T\_osUInt8 [IDTDpll\\_Get3rdPriorityInput](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Get input number of a valid clock with the third highest priority.*
- T\_osUInt8 [IDTDpll\\_GetCurrentSelectInput](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Get the current selected input clock.*
- void [IDTDpll\\_SetDpllOperMod](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_idtDpllOperMode nMode)  
*Set DPLL working at the specified operating mode.*
- T\_idtDpllOperMode [IDTDpll\\_GetDpllOperMod](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Set DPLL working at the specified operating mode.*
- T\_osUInt8 [IDTDpll\\_IsDpllLocked](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Inquire if the DPLL is in lock state.*
- void [IDTDpll\\_SetBandWidthDamping](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_idtBandwidthLimitStage stage, T\_idtDpllBandwidth nBandWidth, T\_idtDampingFactor nDamping)  
*Set the bandwidth and damping factor used for bandwidth limiting.*
- void [IDTDpll\\_GetBandWidthDamping](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_idtBandwidthLimitStage stage, T\_idtDpllBandwidth \*nBandWidth\_p, T\_idtDampingFactor \*nDamping\_p)  
*Get configured bandwidth and damping factor for bandwidth limiting.*
- void [IDTDpll\\_SetAutoSelBandWidth](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_osUInt8 nEnable)  
*Set device to select a suitable bandwidth and damping factor automatically.*
- T\_osUInt8 [IDTDpll\\_GetAutoSelBandWidth](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Get auto bandwidth/damping factor status automatically.*
- void [IDTDpll\\_SetDpllFrozen](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_osUInt8 nEnable)  
*Set DPLL integral path value frozen.*
- T\_osUInt8 [IDTDpll\\_GetDpllFrozen](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Get DPLL integral path value frozen.*
- void [IDTDpll\\_SetPhaseCoarseDetector](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_osUInt8 nEnable, T\_osUInt8 nWide, T\_osUInt8 nMultiPhase, T\_osUInt8 nMultiPh8kEn)  
*Set the coarse phase lose detector enable.*
- void [IDTDpll\\_GetPhaseCoarseDetector](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_osUInt8 \*nEnable\_p, T\_osUInt8 \*nWide\_p, T\_osUInt8 \*nMultiPhase\_p, T\_osUInt8 \*nMultiPh8kEn\_p)  
*Set the coarse phase lose detector enable.*
- void [IDTDpll\\_SetPhaseCoarseLimit](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_idtCoarsePhaseLimit nLimit)  
*Set the limitation of the coarse phase lose detector.*
- T\_idtCoarsePhaseLimit [IDTDpll\\_GetPhaseCoarseLimit](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Get the limitation of the coarse phase lose detector.*
- void [IDTDpll\\_SetPhaseFineDetectorEnable](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_osUInt8 nEnable)  
*Set the fine phase lose detector enable.*
- T\_osUInt8 [IDTDpll\\_GetPhaseFineDetectorEnable](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Get the fine phase lose detector enable.*
- void [IDTDpll\\_SetPhaseFineLimit](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_idtFinePhaseLimit nLimit)

- Set the limitation of the fine phase lose detector.*

  - `T_idtFinePhaseLimit IDTDppll_GetPhaseFineLimit` (`T_idtDrvHdlr hdlr`, `T_idtDppllInstance nDppll`)
- Set the limitation of the fine phase lose detector.*

  - `void IDTDppll_SetFastLossSwitch` (`T_idtDrvHdlr hdlr`, `T_osUInt8 nEnable`)
- Set reference clock switch if a fast loss occurs.*

  - `T_osUInt8 IDTDppll_GetFastLossSwitch` (`T_idtDrvHdlr hdlr`)
- Get reference clock switch if a fast loss occurs.*

  - `void IDTDppll_SetHoldoverMode` (`T_idtDrvHdlr hdlr`, `T_idtDppllInstance nDppll`, `T_idtDppllHoldover nMode`, `T_osUInt8 nReadMode`)
- Set calculation mode of holdover frequency and read back mode.*

  - `void IDTDppll_GetHoldoverMode` (`T_idtDrvHdlr hdlr`, `T_idtDppllInstance nDppll`, `T_idtDppllHoldover *nMode_p`, `T_osUInt8 *nReadMode_p`)
- Get calculation mode of holdover frequency and read back mode.*

  - `void IDTDppll_SetTempHoldoverMode` (`T_idtDrvHdlr hdlr`, `T_idtDppllInstance nDppll`, `T_idtTemp_holdover n-Mode`)
- Set calculation mode of temporary holdover frequency.*

  - `T_idtTemp_holdover IDTDppll_GetTempHoldoverMode` (`T_idtDrvHdlr hdlr`, `T_idtDppllInstance nDppll`)
- Set calculation mode of temporary holdover frequency.*

  - `long IDTDppll_GetHoldoverFreq` (`T_idtDrvHdlr hdlr`, `T_idtDppllInstance nDppll`)
- Get holdover frequency offset (in parts per trillion). In DCO mode, this function returns current DCO offset (in parts per trillion).*

  - `void IDTDppll_SetHoldoverFreq` (`T_idtDrvHdlr hdlr`, `T_idtDppllInstance nDppll`, `long pptOffset`)
- Set DCO frequency to device. Note this function should only be called when DCO mode is enabled.*

  - `long IDTDppll_GetCurrentDppllFreqOffset` (`T_idtDrvHdlr hdlr`, `T_idtDppllInstance nDppll`)
- Get current frequency offset of DPLL in parts per trillion (PPT)*

  - `void IDTDppll_SetDppllSoftAlarmLimit` (`T_idtDrvHdlr hdlr`, `T_idtDppllInstance nDppll`, `T_osUInt8 nLimit`)
- Set the limitation of Soft alarm of DPLL.*

  - `T_osUInt8 IDTDppll_GetDppllSoftAlarmLimit` (`T_idtDrvHdlr hdlr`, `T_idtDppllInstance nDppll`)
- Get the limitation of Soft alarm of DPLL.*

  - `void IDTDppll_SetDppllHardAlarmLimit` (`T_idtDrvHdlr hdlr`, `T_idtDppllInstance nDppll`, `T_osUInt16 nLimit`)
- Set the limitation of Hard alarm of DPLL.*

  - `T_osUInt16 IDTDppll_GetDppllHardAlarmLimit` (`T_idtDrvHdlr hdlr`, `T_idtDppllInstance nDppll`)
- Get the limitation of Hard alarm of DPLL.*

  - `void IDTDppll_SetDppllHardAlarmEnable` (`T_idtDrvHdlr hdlr`, `T_osUInt8 nEnable`)
- Set DPLL in unlocked state when a Hard alarm raised.*

  - `T_osUInt8 IDTDppll_GetDppllHardAlarmEnable` (`T_idtDrvHdlr hdlr`)
- Get DPLL in unlocked state when a Hard alarm raised.*

  - `T_osUInt16 IDTDppll_GetCurrentPhaseError` (`T_idtDrvHdlr hdlr`, `T_idtDppllInstance nDppll`)
- Get the current phase error of DPLL.*

  - `void IDTDppll_SetSonetGigEthOutputPath` (`T_idtDrvHdlr hdlr`, `T_osUInt8 instance`, `T_idtDppllInstance inputDppll`, `T_idtSonetGigEthOutput outputFreq`)
- Set Sonet/GigE path configuration.*

  - `void IDTDppll_GetSonetGigEthOutputPath` (`T_idtDrvHdlr hdlr`, `T_osUInt8 instance`, `T_idtDppllInstance *inputDppll_p`, `T_idtSonetGigEthOutput *outputFreq_p`)
- Retrieve Sonet/GigE path configuration.*

  - `void IDTDppll_SetDppllOutputPathSelectorA` (`T_idtDrvHdlr hdlr`, `T_idtDppllInstance nDppll`, `T_idtDppllOutput-SelectorA path`)
- Set DPLL output path selector A.*

  - `T_idtDppllOutputSelectorA IDTDppll_GetDppllOutputPathSelectorA` (`T_idtDrvHdlr hdlr`, `T_idtDppllInstance nDppll`)
- Get DPLL output path selector A.*

- void `IDTDpll_SetDpllOutputPathSelectorB` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_idtDpllOutputSelectorB` path)
  - Set DPLL output path selector B.*
- `T_idtDpllOutputSelectorB` `IDTDpll_GetDpllOutputPathSelectorB` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)
  - Get DPLL output path selector B.*
- void `IDTDpll_SetDpllEthPathEnable` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_osUInt8` nDisable)
  - Set ETH Enable/Disable.*
- `T_osUInt8` `IDTDpll_GetDpllEthPathEnable` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)
  - Get ETH Enable/Disable.*
- void `IDTDpll_SetDpllSelBPathEnable` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_osUInt8` nDisable)
  - Set DPLL output path selector B Enable/Disable.*
- `T_osUInt8` `IDTDpll_GetDpllSelBPathEnable` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)
  - Get DPLL output path selector B Enable/Disable.*
- void `IDTDpll_SetDpll16E116T1Enable` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_osUInt8` nDisable)
  - Set 16E1/16T1 Enable/Disable.*
- `T_osUInt8` `IDTDpll_GetDpll16E116T1Enable` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)
  - Get 16E1/16T1 Enable/Disable.*
- void `IDTDpll_SetDpllSelAPathEnable` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_osUInt8` nDisable)
  - Set DPLL output path selector A Enable/Disable.*
- `T_osUInt8` `IDTDpll_GetDpllSelAPathEnable` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)
  - Set DPLL output path selector A Enable/Disable.*
- void `IDTDpll_SetFrequencyMonitoringFactor` (`T_idtDrvHdlr` hdlr, `T_idtFreqMonFactor` freqMonFactor)
  - Function to set the frequency monitoring factor. Hard and soft alarm thresholds use this factor as their base unit.*
- `T_idtFreqMonFactor` `IDTDpll_GetFrequencyMonitoringFactor` (`T_idtDrvHdlr` hdlr)
  - Function to get the frequency monitoring factor. Hard and soft alarm thresholds use this factor as their base unit.*
- void `IDTDpll_SetHardAlarmThreshold` (`T_idtDrvHdlr` hdlr, `T_osUInt8` accepting, `T_osUInt8` rejecting)
  - Set the frequency hard alarm accepting thresholds of reference clock monitoring.*
- void `IDTDpll_GetHardAlarmThreshold` (`T_idtDrvHdlr` hdlr, `T_osUInt8` \*accepting\_p, `T_osUInt8` \*rejecting\_p)
  - Get the frequency hard alarm accepting thresholds of reference clock monitoring.*
- void `IDTDpll_SetSoftAlarmThreshold` (`T_idtDrvHdlr` hdlr, `T_osUInt8` accepting, `T_osUInt8` rejecting)
  - Set the frequency soft alarm accepting thresholds of reference clock monitoring.*
- void `IDTDpll_GetSoftAlarmThreshold` (`T_idtDrvHdlr` hdlr, `T_osUInt8` \*accepting\_p, `T_osUInt8` \*rejecting\_p)
  - Get the frequency soft alarm accepting thresholds of reference clock monitoring.*
- void `IDTDpll_SetIcpCtrl` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_osUInt8` nIcp)
  - Set charge pump control.*
- `T_osUInt8` `IDTDpll_GetIcpCtrl` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)
  - Get charge pump control.*
- void `IDTDpll_SetPhaseSlope` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_idtPhaseSlope` nPhaseSlope)
  - Set DPLL phase slope for DPLLs.*
- `T_idtPhaseSlope` `IDTDpll_GetPhaseSlope` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)
  - Get DPLL phase slope for DPLLs.*
- void `IDTDpll_SetPpsFastLock` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nEnableFreq, `T_osUInt8` nEnablePhase)
  - Enable/Disable 1 PPS fast lock.*
- void `IDTDpll_GetPpsFastLock` (`T_idtDrvHdlr` hdlr, `T_osUInt8` \*nEnableFreq\_p, `T_osUInt8` \*nEnablePhase\_p)
  - Get enable/disable 1 PPS fast lock status.*
- void `IDTDpll_SetPhaseTransient` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nEnable)
  - Set the configuration when phase transient occurs.*
- `T_osUInt8` `IDTDpll_GetPhaseTransient` (`T_idtDrvHdlr` hdlr)



*Get the configuration when phase transient occurs.*

- void [IDTDpll\\_SetHitlessSwitchingFeature](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nEnable, T\_osUInt8 nFrozen)

*Set the configuration of hitless switching feature.*

- void [IDTDpll\\_GetHitlessSwitchingFeature](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 \*nEnable\_p, T\_osUInt8 \*nFrozen\_p)

*Get the configuration of hitless switching feature.*

- void [IDTDpll\\_SetPhaseOffset](#) (T\_idtDrvHdlr hdlr, T\_osUInt16 nOffset)

*Set the phase offset value.*

- T\_osUInt16 [IDTDpll\\_GetPhaseOffset](#) (T\_idtDrvHdlr hdlr)

*Get the phase offset value.*

- void [IDTDpll\\_SetPpsPhase](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_idtDpllPpsPhasePostion nPhase, T\_idtDpllPpsPulseWidth nPulse)

*Set PPS phase and pulse for DPLL.*

- void [IDTDpll\\_GetPpsPhase](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_idtDpllPpsPhasePostion \*nPhase\_p, T\_idtDpllPpsPulseWidth \*nPulse\_p)

*Get PPS phase and pulse for DPLL.*

### 4.2.1 Detailed Description

Functions in this group are related to DPPL provisioning.

### 4.2.2 Macro Definition Documentation

#### 4.2.2.1 #define DCO\_MAX\_PPT 92274677

Max DCO value.

#### See Also

[IDTDpll\\_SetHoldoverFreq/IDTDpll\\_GetHoldoverFreq](#)

Definition at line 262 of file DpllCnfg.h.

#### 4.2.2.2 #define DCO\_MIN\_PPT -92274688

Max DCO value.

#### See Also

[IDTDpll\\_SetHoldoverFreq/IDTDpll\\_GetHoldoverFreq](#)

Definition at line 266 of file DpllCnfg.h.

#### 4.2.2.3 #define DCO\_PPT2DCOUNITS 11

Conversion from parts per trillion to register unit value for DCO offset.

Definition at line 258 of file DpllCnfg.h.

#### 4.2.2.4 #define IDT\_TRANSLATE\_EXT\_TO\_INT\_DPLL( *hdr*, *ext*, *internal* )

##### Value:

```
do {
    OS_ASSERT((ext)<DPLL_INSTANCE_MAX);
    OS_ASSERTS((hdr->deviceConfig_m->pllExt2IntXlate_ma[(ext)]<Dpll_MAX), \
        ("Unsupported DPLL instance %d\n", (ext))); \
    internal = hdr->deviceConfig_m->pllExt2IntXlate_ma[(ext)]; \
} while(0)
```

Utility macro to check if DPLL instance is supported and to translated from DPLL instance to DPLL type.

##### Parameters

<i>hdr</i>	Device driver handle
<i>ext</i>	External DPLL instance number (0..N)
<i>internal</i>	Internal DPLL instance

Definition at line 304 of file DpllCnfg.h.

### 4.2.3 Enumeration Type Documentation

#### 4.2.3.1 enum T\_idtBandwidthLimitStage

Enumerated list used for selecting bandwidth limiting stages.

##### Enumerator

***dpllBandwidthLimitStart*** Start stage bandwidth limiting stage  
***dpllBandwidthLimitAcquire*** Acquire stage bandwidth limiting stage  
***dpllBandwidthLimitLocked*** Locked stage bandwidth limiting stage  
***dpllBandwidthLimit\_MAX***

Definition at line 79 of file DpllCnfg.h.

#### 4.2.3.2 enum T\_idtCoarsePhaseLimit

Enumerated type listing coarse phase limits.

##### Enumerator

***coarsePhaseLimit\_1*** +/- 1 UI  
***coarsePhaseLimit\_3*** +/- 3 UI  
***coarsePhaseLimit\_7*** +/- 7 UI  
***coarsePhaseLimit\_15*** +/- 15 UI  
***coarsePhaseLimit\_31*** +/- 31 UI  
***coarsePhaseLimit\_63*** +/- 63 UI  
***coarsePhaseLimit\_127*** +/- 127 UI  
***coarsePhaseLimit\_255*** +/- 255 UI  
***coarsePhaseLimit\_511*** +/- 511 UI  
***coarsePhaseLimit\_1023*** +/- 1023 UI (Only valid for T0)  
***coarsePhaseLimit\_MAX***

Definition at line 159 of file DpllCnfg.h.

## 4.2.3.3 enum T\_idtDampingFactor

Enumerated list showing options for bandwidth damping factor.

Enumerator

***DampingFactor\_1p2*** 1.2  
***DampingFactor\_2p5*** 2.5  
***DampingFactor\_5*** 5  
***DampingFactor\_10*** 10  
***DampingFactor\_20*** 20  
***DampingFactor\_MAX***

Definition at line 91 of file DpllCnfg.h.

## 4.2.3.4 enum T\_idtDpllBandwidth

List of options for DPLL bandwidth.

Enumerator

***dpllBandwidth\_0p5mHz*** 0.5 mHz  
***dpllBandwidth\_1mHz*** 1 mHz  
***dpllBandwidth\_2mHz*** 2 mHz  
***dpllBandwidth\_4mHz*** 4 mHz  
***dpllBandwidth\_8mHz*** 8 mHz  
***dpllBandwidth\_15mHz*** 15 mHz  
***dpllBandwidth\_30mHz*** 30 mHz  
***dpllBandwidth\_60mHz*** 60 mHz  
***dpllBandwidth\_0p1Hz*** 0.1 Hz  
***dpllBandwidth\_0p3Hz*** 0.3 Hz  
***dpllBandwidth\_0p6Hz*** 0.6 Hz  
***dpllBandwidth\_1p2Hz*** 1.2 Hz  
***dpllBandwidth\_2p5Hz*** 2.5 Hz  
***dpllBandwidth\_4Hz*** 4 Hz  
***dpllBandwidth\_8Hz*** 8 Hz  
***dpllBandwidth\_18Hz*** 18 Hz  
***dpllBandwidth\_35Hz*** 35 Hz  
***dpllBandwidth\_70Hz*** 70 Hz  
***dpllBandwidth\_560Hz*** 560 Hz  
***dpllBandwidth\_MAX***

Definition at line 104 of file DpllCnfg.h.

#### 4.2.3.5 enum T\_idtDpllHoldover

Enumerated type listing holdover modes.

Enumerator

***Holdover\_Instantaneous*** Automatic instantaneous mode  
***Holdover\_Slow\_Average*** Automatic slow average mode  
***Holdover\_Fast\_Average*** Automatic fast average mode  
***Holdover\_Manual*** Manual mode  
***Holdover\_MAX***

Definition at line 191 of file DpllCnfg.h.

#### 4.2.3.6 enum T\_idtDpllOperMode

Enumerated type for DPLL operation mode.

Enumerator

***Automatic\_Mode*** Automatic mode  
***Force\_FreeRun\_Mode*** Force to Free-Run mode  
***Force\_Holdover\_Mode*** Force to Holdover mode  
***Force\_Locked\_Mode*** Force to Locked mode  
***Force\_Pre\_Locked2\_Mode*** Force to Pre-Locked2 mode  
***Force\_Pre\_Locked\_Mode*** Force to Pre-Lock mode  
***Force\_Lost\_Phase\_Mode*** Force to Lost-Phase mode  
***Dco\_Mode*** DCO mode  
***DpllOperMode\_MAX***

Definition at line 143 of file DpllCnfg.h.

#### 4.2.3.7 enum T\_idtDpllOutputSelectorA

Enumerated type listing DPLL selector A paths.

Enumerator

***DPLLOutputSelA\_16E1*** 16E1 Output path  
***DPLLOutputSelA\_16T1*** 16T1 Output path  
***DPLLOutputSelA\_GSM*** GSM Output path  
***DPLLOutputSelA\_OBSAI*** OBSAI Output path  
***DPLLOutputSelA\_GPS*** GPS Output path  
***DPLLOutputSelA\_MAX***

Definition at line 235 of file DpllCnfg.h.

## 4.2.3.8 enum T\_idtDpllOutputSelectorB

Enumerated type listing DPLL selector B paths.

Enumerator

***DPLLOutputSelB\_12E1*** 12E1 Output path  
***DPLLOutputSelB\_GPS*** GPS Output path  
***DPLLOutputSelB\_E3*** E3 Output path  
***DPLLOutputSelB\_T3*** T3 Output path  
***DPLLOutputSelB\_24T1*** 24T1 Output path  
***DPLLOutputSelB\_MAX***

Definition at line 247 of file DpllCnfg.h.

## 4.2.3.9 enum T\_idtDpllPpsPhasePostion

Enumerated type listing PPS phase options.

Enumerator

***PpsPhasePostion\_0degree*** 0 degrees  
***PpsPhasePostion\_50ns*** 50 nanoseconds  
***PpsPhasePostion\_100ns*** 100 nanaoseconds  
***PpsPhasePostion\_MAX***

Definition at line 271 of file DpllCnfg.h.

## 4.2.3.10 enum T\_idtDpllPpsPulseWidth

Enumerated type listing PPS pulse width.

Enumerator

***PpsPulseWidth\_0pt5sec*** 0.5 seconds  
***PpsPulseWidth\_10ns*** 10 nanoseconds  
***PpsPulseWidth\_200ns*** 200 nanoseconds  
***PpsPulseWidth\_400ns*** 400 nanoseconds  
***PpsPulseWidth\_800ns*** 800 nanoseconds  
***PpsPulseWidth\_1us*** 1 microsecond  
***PpsPulseWidth\_20us*** 20 microseconds  
***PpsPulseWidth\_50us*** 20 microseconds  
***PpsPulseWidth\_100us*** 100 microseconds  
***PpsPulseWidth\_200us*** 200 microseconds  
***PpsPulseWidth\_1pt2ms***  
***PpsPulseWidth\_800us*** 1.2 miliseonds 800 microseconds  
***PpsPulseWidth\_MAX***

Definition at line 281 of file DpllCnfg.h.

#### 4.2.3.11 enum T\_idtFinePhaseLimit

Enumerated type listing fine phase limits.

Enumerator

***finePhaseLimit\_45\_90degree*** +/- 45-90 degrees  
***finePhaseLimit\_90\_180degree*** +/- 90-180 degrees  
***finePhaseLimit\_180\_360degree*** +/- 180-360 degrees  
***finePhaseLimit\_20\_25nanosec*** +/- 20-25 nanoseconds  
***finePhaseLimit\_60\_65nanosec*** +/- 60-65 nanoseconds  
***finePhaseLimit\_120\_125nanosec*** +/- 120-125 nanoseconds  
***finePhaseLimit\_950\_955nanosec*** +/- 950-955 nanoseconds  
***finePhaseLimit\_MAX***

Definition at line 178 of file DpllCnfg.h.

#### 4.2.3.12 enum T\_idtFreqMonFactor

Enumerated list indicating frequency monitoring factor.

Enumerator

***FreqMonFactor\_0p0032*** 0.0032 ppm  
***FreqMonFactor\_0p0064*** 0.0064 ppm  
***FreqMonFactor\_0p0127*** 0.0127 ppm  
***FreqMonFactor\_0p0257*** 0.0257 ppm  
***FreqMonFactor\_0p0514*** 0.0514 ppm  
***FreqMonFactor\_0p1030*** 0.103 ppm  
***FreqMonFactor\_0p2060*** 0.206 ppm  
***FreqMonFactor\_0p4120*** 0.412 ppm  
***FreqMonFactor\_0p8230*** 0.823 ppm  
***FreqMonFactor\_1p6460*** 1.646 ppm  
***FreqMonFactor\_3p2920*** 3.292 ppm  
***FreqMonFactor\_3p8100*** 3.81 ppm  
***FreqMonFactor\_4p6000*** 4.6 ppm  
***FreqMonFactor\_MAX***

Definition at line 58 of file DpllCnfg.h.

#### 4.2.3.13 enum T\_idtOperDpllMode

Enumerated type listing DPLL operational modes.

Enumerator

***OperDpllMode\_FreeRun*** Free-Run Mode  
***OperDpllMode\_HoldOver*** HoldOver Mode  
***OperDpllMode\_Locked*** Locked Mode  
***OperDpllMode\_PreLocked2*** Pre-Locked 2 Mode  
***OperDpllMode\_PreLocked*** Pre-Locked Mode  
***OperDpllMode\_LostPhase*** Lost Phase Mode

Definition at line 211 of file DpllCnfg.h.

## 4.2.3.14 enum T\_idtPhaseSlope

Enumerated type listing phase slope.

Enumerator

***phaseSlope\_gr1244st3*** GR-1244 Stratum3 61us/s  
***phaseSlope\_gr1244st3e*** GR-1244 Stratum3E, G2-253 Stratum 3 (855ns/s)  
***phaseSlope\_gr813*** GR-813,G.8262 (7.5us/s)  
***phaseSlope\_noLimit*** No limit  
***phaseSlope\_MAX***

Definition at line 131 of file DpllCnfg.h.

## 4.2.3.15 enum T\_idtSonetGigEthOutput

Enumerated type listing possible Sonet/GigE output frequencies.

Enumerator

***SonetGigEthOutput\_Sonet*** SONET/SDH 622.08MHz output  
***SonetGigEthOutput\_10GbE*** Ethernet 625 MHz output  
***SonetGigEthOutput\_10GbE\_6664*** Ethernet OTN 625(66/64) MHz output  
***SonetGigEthOutput\_MAX***

Definition at line 224 of file DpllCnfg.h.

## 4.2.3.16 enum T\_idtTemp\_holdover

Enumerated type listing temp-holdover modes.

Enumerator

***Temp\_Same\_As\_Full\_Holdover*** Same as the DPLL holdover mode  
***Temp\_Holdover\_Instantaneous*** Automatic instantaneous  
***Temp\_Holdover\_Fast\_Average*** Automatic fast average  
***Temp\_Holdover\_Slow\_Average*** Automatic slow average  
***Temp\_Holdover\_MAX***

Definition at line 201 of file DpllCnfg.h.

## 4.2.4 Function Documentation

4.2.4.1 T\_osUInt8 IDTDpll\_Get1stPriorityInput ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Get input number of a valid clock with the highest priority.

Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

**Returns**

nInput The number of input clock with highest priority

Definition at line 296 of file DpllCnfg.c.

#### 4.2.4.2 T\_osUInt8 IDTDpll.Get2ndPriorityInput ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Get input number of a valid clock with the second highest priority.

**Parameters**

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

**Returns**

nInput The number of input clock with second highest priority

Definition at line 318 of file DpllCnfg.c.

#### 4.2.4.3 T\_osUInt8 IDTDpll.Get3rdPriorityInput ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Get input number of a valid clock with the third highest priority.

**Parameters**

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

**Returns**

nInput The number of input clock with third highest priority

Definition at line 340 of file DpllCnfg.c.

#### 4.2.4.4 T\_osUInt8 IDTDpll.GetAutoSelBandWidth ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Get auto bandwidth/damping factor status automatically.

**Parameters**

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

**Returns**

0-manual bandwidth/damping factor mode, 1-automatic bandwidth/damping factor mode

Definition at line 723 of file DpllCnfg.c.

#### 4.2.4.5 T\_osUInt8 IDTDpll.GetAutoSelInput ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Get automatic input selection status.



## Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

## Returns

0-In manual mode, 1-In auto mode

Definition at line 218 of file DpllCnfg.c.

4.2.4.6 void IDTDpll\_GetBandWidthDamping ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_idtBandwidthLimitStage *stage*, T\_idtDpllBandwidth \* *nBandWidth\_p*, T\_idtDampingFactor \* *nDamping\_p* )

Get configured bandwidth and damping factor for bandwidth limiting.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>stage</i>	Bandwidth stage
<i>nBandWidth_p</i>	the bandwidth of DPLL <ul style="list-style-type: none"> <li>• dpllBandwidth_0p5mHz - 0.5 mHz</li> <li>• dpllBandwidth_1mHz - 1 mHz</li> <li>• dpllBandwidth_2mHz - 2 mHz</li> <li>• dpllBandwidth_4mHz - 4 mHz</li> <li>• dpllBandwidth_8mHz - 8 mHz</li> <li>• dpllBandwidth_15mHz - 15 mHz</li> <li>• dpllBandwidth_30mHz - 30 mHz</li> <li>• dpllBandwidth_60mHz - 60 mHz</li> <li>• dpllBandwidth_0p1Hz - 0.1 Hz</li> <li>• dpllBandwidth_0p3Hz - 0.3 Hz</li> <li>• dpllBandwidth_0p6Hz - 0.6 Hz</li> <li>• dpllBandwidth_1p2Hz - 1.2 Hz</li> <li>• dpllBandwidth_2p5Hz - 2.5 Hz</li> <li>• dpllBandwidth_4Hz - 4 Hz</li> <li>• dpllBandwidth_8Hz - 8 Hz</li> <li>• dpllBandwidth_18Hz - 18 Hz</li> <li>• dpllBandwidth_35Hz - 35 Hz</li> <li>• dpllBandwidth_70Hz - 70 Hz</li> <li>• dpllBandwidth_560Hz - 560 Hz</li> </ul>
<i>nDamping_p</i>	the damping factor of DPLL <ul style="list-style-type: none"> <li>• DampingFactor_1p2 - 1.2</li> <li>• DampingFactor_2p5 - 2.5</li> <li>• DampingFactor_5 - 5</li> <li>• DampingFactor_10 - 10</li> <li>• DampingFactor_20 - 20</li> </ul>

Definition at line 639 of file DpllCnfg.c.

#### 4.2.4.7 long IDTDpll\_GetCurrentDpllFreqOffset ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Get current frequency offset of DPLL in parts per trillion (PPT)

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

##### Returns

Frequency offset in parts per trillion

Definition at line 1347 of file DpllCnfg.c.

#### 4.2.4.8 T\_osUInt16 IDTDpll\_GetCurrentPhaseError ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Get the current phase error of DPLL.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

##### Returns

nError: a 2' complement signed integer represents current phase error. It is a multiple, the real phase error is:  
nError \* 0.0014

Definition at line 1510 of file DpllCnfg.c.

#### 4.2.4.9 T\_osUInt8 IDTDpll\_GetCurrentSelectInput ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Get the current selected input clock.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

##### Returns

nInput the number of selected input clock

Definition at line 362 of file DpllCnfg.c.

#### 4.2.4.10 T\_osUInt8 IDTDpll\_GetDpll16E116T1Enable ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Get 16E1/16T1 Enable/Disable.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

**Returns**

- 0= Enable
- 1= Disable

Definition at line 1992 of file DpllCnfg.c.

#### 4.2.4.11 T\_osUInt8 IDTDpll\_GetDpllEthPathEnable ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Get ETH Enable/Disable.

**Parameters**

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

**Returns**

- 0= Enable
- 1= Disable

Definition at line 1846 of file DpllCnfg.c.

#### 4.2.4.12 T\_osUInt8 IDTDpll\_GetDpllFrozen ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Get DPLL integral path value frozen.

**Parameters**

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

**Returns**

- 0= Disable the integral path frozen
- 1= Enable the integral path frozen

Definition at line 780 of file DpllCnfg.c.

#### 4.2.4.13 T\_osUInt8 IDTDpll\_GetDpllHardAlarmEnable ( T\_idtDrvHdlr *hdlr* )

Get DPLL in unlocked state when a Hard alarm raised.

**Parameters**

<i>hdlr</i>	Device driver handler
-------------	-----------------------

**Returns**

- 0= Ignore Hard alarm, DPLL continues operation
- 1= DPLL is unlock if Hard alarm raised

Definition at line 1495 of file DpllCnfg.c.

#### 4.2.4.14 T\_osUint16 IDTDpll\_GetDpllHardAlarmLimit ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Get the limitation of Hard alarm of DPLL.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

##### Returns

a 2' complement signed integer represents limitation of hard alarm. It is a multiple, the real limitation is: nLimit \* 0.0014

Definition at line 1458 of file DpllCnfg.c.

#### 4.2.4.15 T\_idtDpllOperMode IDTDpll\_GetDpllOperMod ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Set DPLL working at the specified operating mode.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

##### Returns

nMode

- Automatic\_Mode = Automatic mode
- Force\_FreeRun\_Mode = Force to Free-Run mode
- Force\_Holdover\_Mode = Force to Holdover mode
- Force\_Locked\_Mode = Force to Locked mode
- Force\_Pre\_Locked2\_Mode = Force to Pre-Locked2 mode
- Force\_Pre\_Locked\_Mode = Force to Pre-Lock mode
- Force\_Lost\_Phase\_Mode = Force to Lost-Phase mode
- Dco\_Mode = DCO mode

Definition at line 454 of file DpllCnfg.c.

#### 4.2.4.16 T\_idtDpllOutputSelectorA IDTDpll\_GetDpllOutputPathSelectorA ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Get DPLL output path selector A.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

##### Returns

DPLL selector path

Definition at line 1687 of file DpllCnfg.c.

4.2.4.17 T\_idtDpllOutputSelectorB IDTDpll\_GetDpllOutputPathSelectorB ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Get DPLL output path selector B.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

## Returns

DPLL selector path

Definition at line 1771 of file DpllCnfg.c.

4.2.4.18 T\_osUInt8 IDTDpll\_GetDpllSelAPathEnable ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Set DPLL output path selector A Enable/Disable.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

## Returns

- 0= Enable
- 1= Disable

Definition at line 2064 of file DpllCnfg.c.

4.2.4.19 T\_osUInt8 IDTDpll\_GetDpllSelBPathEnable ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Get DPLL output path selector B Enable/Disable.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

## Returns

- 0= Enable
- 1= Disable

Definition at line 1920 of file DpllCnfg.c.

4.2.4.20 T\_osUInt8 IDTDpll\_GetDpllSoftAlarmLimit ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Get the limitation of Soft alarm of DPLL.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

**Returns**

a 2' complement signed integer represents limitation of soft alarm. It is a multiple, the real limitation is:  $nLimit * 0.724$

Definition at line 1410 of file DpllCnfg.c.

**4.2.4.21 T\_osUInt8 IDTDpll\_GetFastLossSwitch ( T\_idtDrvHdlr hdlr )**

Get reference clock switch if a fast loss occurs.

**Parameters**

<i>hdlr</i>	Device driver handler
-------------	-----------------------

**Returns**

- 0= Disable switch, DPLL enters temporary holdover state
- 1= Enable switch, DPLL enters Phase-loss state

Definition at line 1116 of file DpllCnfg.c.

**4.2.4.22 T\_osUInt8 IDTDpll\_GetForceSellInput ( T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll )**

Set the DPLL to force to lock to a specified reference clock.

**Parameters**

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

**Returns**

Port number of selected input clock

Definition at line 271 of file DpllCnfg.c.

**4.2.4.23 T\_idtFreqMonFactor IDTDpll\_GetFrequencyMonitoringFactor ( T\_idtDrvHdlr hdlr )**

Function to get the frequency monitoring factor. Hard and soft alarm thresholds use this factor as their base unit.

**Parameters**

<i>hdlr</i>	Device driver handler
-------------	-----------------------

**Returns**

Frequency monitoring factor value.

- FreqMonFactor\_0p0032 - 0.0032 ppm
- FreqMonFactor\_0p0064 - 0.0064 ppm
- FreqMonFactor\_0p0127 - 0.0127 ppm
- FreqMonFactor\_0p0257 - 0.0257 ppm
- FreqMonFactor\_0p0514 - 0.0514 ppm
- FreqMonFactor\_0p1030 - 0.103 ppm

- FreqMonFactor\_0p2060 - 0.206 ppm
- FreqMonFactor\_0p4120 - 0.412 ppm
- FreqMonFactor\_0p8230 - 0.823 ppm
- FreqMonFactor\_1p6460 - 1.646 ppm
- FreqMonFactor\_3p2920 - 3.29 ppm
- FreqMonFactor\_3p8100 - 3.81 ppm
- FreqMonFactor\_4p6000 - 4.6 ppm

Definition at line 2146 of file DpllCnfg.c.

#### 4.2.4.24 void IDTDpll\_GetHardAlarmThreshold ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 \* *accepting\_p*, T\_osUInt8 \* *rejecting\_p* )

Get the frequency hard alarm accepting thresholds of reference clock monitoring.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>accepting_p</i>	Accepting threshold (ppm) is a multiple of frequency monitoring factor value. Accepting Threshold = (AcceptingValue + 1)*(FreqMonFactor)
<i>rejecting_p</i>	Rejecting threshold (ppm) is a multiple of frequency monitoring factor value. Rejecting Threshold = (RejectingValue + 1)*(FreqMonFactor)

Definition at line 2195 of file DpllCnfg.c.

#### 4.2.4.25 void IDTDpll\_GetHitlessSwitchingFeature ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 \* *nEnable\_p*, T\_osUInt8 \* *nFrozen\_p* )

Get the configuration of hitless switching feature.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nEnable_p</i>	<ul style="list-style-type: none"> <li>• 0= Disable the hitless switching feature;</li> <li>• 1= Enable the hitless switching feature;</li> </ul>
<i>nFrozen_p</i>	<ul style="list-style-type: none"> <li>• 0= hitless switching feature is not frozen;</li> <li>• 1= HS feature is frozen, ignore the further hitless switching events</li> </ul>

Definition at line 2546 of file DpllCnfg.c.

#### 4.2.4.26 long IDTDpll\_GetHoldoverFreq ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Get holdover frequency offset (in parts per trillion). In DCO mode, this function returns current DCO offset (in parts per trillion).

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

**Returns**

Parts per trillion

Definition at line 1255 of file DpllCnfg.c.

4.2.4.27 void IDTDpll\_GetHoldoverMode ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_idtDpllHoldover \* *nMode\_p*, T\_osUInt8 \* *nReadMode\_p* )

Get calculation mode of holdover frequency and read back mode.

**Parameters**

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>nMode_p</i>	<ul style="list-style-type: none"> <li>• Holdover_Instantaneous = automatic instantaneous mode</li> <li>• Holdover_Slow_Average = automatic slow average</li> <li>• Holdover_Fast_Average = Automatic fast average</li> <li>• Holdover_Manual = Manual</li> </ul>
<i>nReadMode_p</i>	<ul style="list-style-type: none"> <li>• 0= Don't read value from device</li> <li>• 1= Read value calculated by device back to the holdover frequency register(0x5D,0x5E and 0x5F)</li> </ul>

Definition at line 1176 of file DpllCnfg.c.

4.2.4.28 T\_osUInt8 IDTDpll\_GetIcpCtrl ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Get charge pump control.

**Parameters**

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

**Returns**

Charge pump current selection ( 0 - 0x1F ); 10 = 40uA;

Definition at line 2312 of file DpllCnfg.c.

4.2.4.29 void IDTDpll\_GetPhaseCoarseDetector ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_osUInt8 \* *nEnable\_p*, T\_osUInt8 \* *nWide\_p*, T\_osUInt8 \* *nMultiPhase\_p*, T\_osUInt8 \* *nMultiPh8kEn\_p* )

Set the coarse phase lose detector enable.

**Parameters**

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance



<i>nEnable_p</i>	<ul style="list-style-type: none"> <li>• 0= Disable the coarse phase detector</li> <li>• 1= Enable the coarse phase detector</li> </ul>
<i>nWide_p</i>	<ul style="list-style-type: none"> <li>• 0= Wide range disable</li> <li>• 1= Wide range enable</li> </ul>
<i>nMultiPhase_p</i>	<ul style="list-style-type: none"> <li>• 0= Limit to +/- 1UI</li> <li>• 1= Limit to PH_LOS_COARSE_LIMT register</li> </ul>
<i>nMultiPh8kEn_p</i>	<ul style="list-style-type: none"> <li>• 0= Limit to +/- 1UI when reference clock 8/4/2KHz clock</li> <li>• 1= Limit to PH_LOS_COARSE_LIMT register</li> </ul>

Definition at line 876 of file DpllCnfg.c.

#### 4.2.4.30 T\_idtCoarsePhaseLimit IDTDpll\_GetPhaseCoarseLimit ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Get the limitation of the coarse phase lose detector.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

##### Returns

Limitation of coarse phase loss detector.

- coarsePhaseLimit\_1 - +/- 1 UI
- coarsePhaseLimit\_3 - +/- 3 UI
- coarsePhaseLimit\_7 - +/- 7 UI
- coarsePhaseLimit\_15 - +/- 15 UI
- coarsePhaseLimit\_31 - +/- 31 UI
- coarsePhaseLimit\_63 - +/- 63 UI
- coarsePhaseLimit\_127 - +/- 127 UI
- coarsePhaseLimit\_255 - +/- 255 UI
- coarsePhaseLimit\_511 - +/- 511 UI
- coarsePhaseLimit\_1023 - +/- 1023 UI T0 only

Definition at line 968 of file DpllCnfg.c.

#### 4.2.4.31 T\_osUint8 IDTDpll\_GetPhaseFineDetectorEnable ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Get the fine phase lose detector enable.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

**Returns**

- 0= Disable the fine phase detector
- 1= Enable the fine phase detector

Definition at line 1016 of file DpllCnfg.c.

#### 4.2.4.32 T\_idtFinePhaseLimit IDTDpll\_GetPhaseFineLimit ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Set the limitation of the fine phase lose detector.

**Parameters**

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

**Returns**

Limitation of fine phase loss detector

- finePhaseLimit\_45\_90degree = +/- 45-90 degrees
- finePhaseLimit\_90\_180degree = +/- 90-180 degrees
- finePhaseLimit\_180\_360degree = +/- 180-360 degrees
- finePhaseLimit\_20\_25nanosec = +/- 20-25 nanoseconds
- finePhaseLimit\_60\_65nanosec = +/- 60-65 nanoseconds
- finePhaseLimit\_120\_125nanosec = +/- 120-125 nanoseconds
- finePhaseLimit\_950\_955nanosec = +/- 950-955 nanoseconds

Definition at line 1077 of file DpllCnfg.c.

#### 4.2.4.33 T\_osUInt16 IDTDpll\_GetPhaseOffset ( T\_idtDrvHdlr *hdlr* )

Get the phase offset value.

**Parameters**

<i>hdlr</i>	Device driver handler
-------------	-----------------------

**Returns**

Phase offset= nOffset \* 0x61 ns;

Definition at line 2584 of file DpllCnfg.c.

#### 4.2.4.34 T\_idtPhaseSlope IDTDpll\_GetPhaseSlope ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Get DPLL phase slope for DPLLs.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

## Returns

Phase slope

- phaseSlope\_gr1244st3 = GR-1244 ST3 (61us/s)
- phaseSlope\_gr1244st3e = GR-1244 ST2,3E,ST3 (855ns/s)
- phaseSlope\_gr813 = GR-813,G.8262 (7.5us/s)
- phaseSlope\_noLimit = No limitation

Definition at line 2397 of file DpllCnfg.c.

4.2.4.35 T\_osUInt8 IDTDpll\_GetPhaseTransient ( T\_idtDrvHdlr *hdlr* )

Get the configuration when phase transient occurs.

## Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

## Returns

- 0= Disable the phase transient monitor
- 1= Enable the phase transient monitor

Definition at line 2503 of file DpllCnfg.c.

4.2.4.36 void IDTDpll\_GetPpsFastLock ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 \* *nEnableFreq\_p*, T\_osUInt8 \* *nEnablePhase\_p* )

Get enable/disable 1 PPS fast lock status.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nEnableFreq_p</i>	Enable (1) / Disable (0) frequency locking
<i>nEnablePhase_p</i>	Enable (1) / Disable (0) phase locking

Definition at line 2461 of file DpllCnfg.c.

4.2.4.37 void IDTDpll\_GetPpsPhase ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_idtDpllPpsPhasePostion \* *nPhase\_p*, T\_idtDpllPpsPulseWidth \* *nPulse\_p* )

Get PPS phase and pulse for DPLL.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>nPhase_p</i>	Phase position

## See Also

[T\\_idtDpllPpsPhasePostion](#)

## Parameters

<i>nPulse_p</i>	Pulse width
-----------------	-------------

## See Also

[T\\_idtDpllPpsPulseWidth](#)

Definition at line 2661 of file DpllCnfg.c.

4.2.4.38 void IDTDpll\_GetSoftAlarmThreshold ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 \* *accepting\_p*, T\_osUInt8 \* *rejecting\_p* )

Get the frequency soft alarm accepting thresholds of reference clock monitoring.

## Parameters

<i>hdlr</i>	Device driver handler
<i>accepting_p</i>	Accepting threshold (ppm) is a multiple of frequency monitoring factor value. Accepting Threshold = (AcceptingValue + 1)*(FreqMonFactor)
<i>rejecting_p</i>	Rejecting threshold (ppm) is a multiple of frequency monitoring factor value. Rejecting Threshold = (RejectingValue + 1)*(FreqMonFactor)

Definition at line 2249 of file DpllCnfg.c.

4.2.4.39 void IDTDpll\_GetSonetGigEthOutputPath ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *instance*, T\_idtDpllInstance \* *inputDpll\_p*, T\_idtSonetGigEthOutput \* *outputFreq\_p* )

Retrieve Sonet/GigE path configuration.

## Parameters

<i>hdlr</i>	Device driver handler
<i>instance</i>	Sonet/GigE path instance 0..1
<i>inputDpll_p</i>	Provisioned DPLL instance of Sonet/GigE path
<i>outputFreq_p</i>	Provisioned output frequency of Sonet/GigE path

Definition at line 1609 of file DpllCnfg.c.

4.2.4.40 T\_idtTemp\_holdover IDTDpll\_GetTempHoldoverMode ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Set calculation mode of temporary holdover frequency.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

## Returns

- Temp\_Same\_As\_Full\_Holdover = Same as the DPLL holdover mode
- Temp\_Holdover\_Instantaneous = Automatic instantaneous mode
- Temp\_Holdover\_Fast\_Average = Automatic fast average

- Temp\_Holdover\_Slow\_Average = Automatic slow average

Definition at line 1234 of file DpllCnfg.c.

#### 4.2.4.41 T\_idtDpllType IDTDpll\_GetTypeOfDpll ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Function to determine type of DPLL give a DPLL instance.

This functions is useful in determining supported features of each DPLL

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

##### Returns

Dpll\_T0- T0 DPLL, Dpll\_T4- T4 DPLL, Dpll\_MAX- DPLL instance not supported

Definition at line 176 of file DpllCnfg.c.

#### 4.2.4.42 T\_osUInt8 IDTDpll\_IsDpllLocked ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

Inquire if the DPLL is in lock state.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

##### Returns

nState

- 0= DPLL is in unlocked state
- 1= DPLL is in locked state

Definition at line 498 of file DpllCnfg.c.

#### 4.2.4.43 void IDTDpll\_SetAutoSelBandWidth ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_osUInt8 *nEnable* )

Set device to select a suitable bandwidth and damping factor automatically.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>nEnable</i>	<ul style="list-style-type: none"> <li>• 0= Only locked bandwidth and damping factor selected</li> <li>• 1= enable automatic selection</li> </ul>

Definition at line 694 of file DpllCnfg.c.

#### 4.2.4.44 void IDTDpll\_SetAutoSellInput ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_osUInt8 *mode* )

Set the DPLL as automatic reference clock selection.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>mode</i>	0-In manual mode, 1-In auto mode

Definition at line 190 of file DpllCnfg.c.

#### 4.2.4.45 void IDTDpll\_SetBandWidthDamping ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_idtBandwidthLimitStage *stage*, T\_idtDpllBandwidth *nBandWidth*, T\_idtDampingFactor *nDamping* )

Set the bandwidth and damping factor used for bandwidth limiting.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>stage</i>	Bandwidth stage
<i>nBandWidth</i>	<p>the bandwidth of DPLL</p> <ul style="list-style-type: none"> <li>• <i>dppllBandwidth_0p5mHz</i> - 0.5 mHz</li> <li>• <i>dppllBandwidth_1mHz</i> - 1 mHz</li> <li>• <i>dppllBandwidth_2mHz</i> - 2 mHz</li> <li>• <i>dppllBandwidth_4mHz</i> - 4 mHz</li> <li>• <i>dppllBandwidth_8mHz</i> - 8 mHz</li> <li>• <i>dppllBandwidth_15mHz</i> - 15 mHz</li> <li>• <i>dppllBandwidth_30mHz</i> - 30 mHz</li> <li>• <i>dppllBandwidth_60mHz</i> - 60 mHz</li> <li>• <i>dppllBandwidth_0p1Hz</i> - 0.1 Hz</li> <li>• <i>dppllBandwidth_0p3Hz</i> - 0.3 Hz</li> <li>• <i>dppllBandwidth_0p6Hz</i> - 0.6 Hz</li> <li>• <i>dppllBandwidth_1p2Hz</i> - 1.2 Hz</li> <li>• <i>dppllBandwidth_2p5Hz</i> - 2.5 Hz</li> <li>• <i>dppllBandwidth_4Hz</i> - 4 Hz</li> <li>• <i>dppllBandwidth_8Hz</i> - 8 Hz</li> <li>• <i>dppllBandwidth_18Hz</i> - 18 Hz</li> <li>• <i>dppllBandwidth_35Hz</i> - 35 Hz</li> <li>• <i>dppllBandwidth_70Hz</i> - 70 Hz</li> <li>• <i>dppllBandwidth_560Hz</i> - 560 Hz</li> </ul>
<i>nDamping</i>	<p>the damping factor of DPLL</p> <ul style="list-style-type: none"> <li>• <i>DampingFactor_1p2</i> - 1.2</li> <li>• <i>DampingFactor_2p5</i> - 2.5</li> <li>• <i>DampingFactor_5</i> - 5</li> <li>• <i>DampingFactor_10</i> - 10</li> <li>• <i>DampingFactor_20</i> - 20</li> </ul>

Definition at line 550 of file DpllCnfg.c.

4.2.4.46 void IDTDpll\_SetDpll16E116T1Enable ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_osUInt8 *nDisable* )

Set 16E1/16T1 Enable/Disable.

Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>nDisable</i>	<ul style="list-style-type: none"> <li>• 0= Enable</li> <li>• 1= Disable</li> </ul>

Definition at line 1956 of file DpllCnfg.c.

4.2.4.47 void IDTDpll\_SetDpllEthPathEnable ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_osUInt8 *nDisable* )

Set ETH Enable/Disable.

Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>nDisable</i>	<ul style="list-style-type: none"> <li>• 0= Enable</li> <li>• 1= Disable</li> </ul>

Definition at line 1810 of file DpllCnfg.c.

4.2.4.48 void IDTDpll\_SetDpllFrozen ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_osUInt8 *nEnable* )

Set DPLL integral path value frozen.

Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>nEnable</i>	<ul style="list-style-type: none"> <li>• 0= Disable the integral path frozen</li> <li>• 1= Enable the integral path frozen</li> </ul>

Definition at line 750 of file DpllCnfg.c.

4.2.4.49 void IDTDpll\_SetDpllHardAlarmEnable ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nEnable* )

Set DPLL in unlocked state when a Hard alarm raised.

Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

<i>nEnable</i>	<ul style="list-style-type: none"> <li>• 0= Ignore Hard alarm, DPLL continues operation</li> <li>• 1= DPLL is unlock if Hard alarm raised</li> </ul>
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Definition at line 1479 of file DpllCnfg.c.

4.2.4.50 void IDTDpll\_SetDpllHardAlarmLimit ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_osUint16 *nLimit* )

Set the limitation of Hard alarm of DPLL.

#### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>nLimit</i>	A 2' complement signed integer represents limitation of hard alarm. It is a multiple, the real limitation is: $nLimit * 0.0014$

Definition at line 1430 of file DpllCnfg.c.

4.2.4.51 void IDTDpll\_SetDpllOperMod ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_idtDpllOperMode *nMode* )

Set DPLL working at the specified operating mode.

#### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>nMode</i>	<ul style="list-style-type: none"> <li>• Automatic_Mode = Automatic mode</li> <li>• Force_FreeRun_Mode = Force to Free-Run mode</li> <li>• Force_Holdover_Mode = Force to Holdover mode</li> <li>• Force_Locked_Mode = Force to Locked mode</li> <li>• Force_Pre_Locked2_Mode = Force to Pre-Locked2 mode</li> <li>• Force_Pre_Locked_Mode = Force to Pre-Lock mode</li> <li>• Force_Lost_Phase_Mode = Force to Lost-Phase mode</li> <li>• Dco_Mode = DCO mode</li> </ul>

Definition at line 390 of file DpllCnfg.c.

4.2.4.52 void IDTDpll\_SetDpllOutputPathSelectorA ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_idtDpllOutputSelectorA *path* )

Set DPLL output path selector A.

#### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>path</i>	DPLL selector path



Definition at line 1646 of file DpllCnfg.c.

4.2.4.53 void IDTDpll\_SetDpllOutputPathSelectorB ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_idtDpllOutputSelectorB *path* )

Set DPLL output path selector B.

Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>path</i>	DPLL selector path

Definition at line 1724 of file DpllCnfg.c.

4.2.4.54 void IDTDpll\_SetDpllSelAPathEnable ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_osUInt8 *nDisable* )

Set DPLL output path selector A Enable/Disable.

Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>nDisable</i>	<ul style="list-style-type: none"> <li>• 0= Enable</li> <li>• 1= Disable</li> </ul>

Definition at line 2028 of file DpllCnfg.c.

4.2.4.55 void IDTDpll\_SetDpllSelBPathEnable ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_osUInt8 *nDisable* )

Set DPLL output path selector B Enable/Disable.

Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>nDisable</i>	<ul style="list-style-type: none"> <li>• 0= Enable</li> <li>• 1= Disable</li> </ul>

Definition at line 1884 of file DpllCnfg.c.

4.2.4.56 void IDTDpll\_SetDpllSoftAlarmLimit ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_osUInt8 *nLimit* )

Set the limitation of Soft alarm of DPLL.

Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>nLimit</i>	A 2' complement signed integer represents limitation of soft alarm. It is a multiple, the real limitation is: $nLimit * 0.724$

Definition at line 1386 of file DpllCnfg.c.

4.2.4.57 void IDTDpll\_SetFastLossSwitch ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nEnable* )

Set reference clock switch if a fast loss occurs.

Parameters

<i>hdlr</i>	Device driver handler
<i>nEnable</i>	<ul style="list-style-type: none"> <li>• 0= Disable switch, DPLL enters temporary holdover state</li> <li>• 1= Enable switch, DPLL enters Phase-loss state</li> </ul>

Definition at line 1100 of file DpllCnfg.c.

4.2.4.58 void IDTDpll\_SetForceSelInput ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_osUInt8 *nInputNo* )

Set the DPLL to force to lock to a specified reference clock.

Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>nInputNo</i>	The number of a specified input clock

Definition at line 243 of file DpllCnfg.c.

4.2.4.59 void IDTDpll\_SetFrequencyMonitoringFactor ( T\_idtDrvHdlr *hdlr*, T\_idtFreqMonFactor *freqMonFactor* )

Function to set the frequency monitoring factor. Hard and soft alarm thresholds use this factor as their base unit.

Parameters

<i>hdlr</i>	Device driver handler
<i>freqMonFactor</i>	<p>Frequency monitoring factor value.</p> <ul style="list-style-type: none"> <li>• FreqMonFactor_0p0032 - 0.0032 ppm</li> <li>• FreqMonFactor_0p0064 - 0.0064 ppm</li> <li>• FreqMonFactor_0p0127 - 0.0127 ppm</li> <li>• FreqMonFactor_0p0257 - 0.0257 ppm</li> <li>• FreqMonFactor_0p0514 - 0.0514 ppm</li> <li>• FreqMonFactor_0p1030 - 0.103 ppm</li> <li>• FreqMonFactor_0p2060 - 0.206 ppm</li> <li>• FreqMonFactor_0p4120 - 0.412 ppm</li> <li>• FreqMonFactor_0p8230 - 0.823 ppm</li> <li>• FreqMonFactor_1p6460 - 1.646 ppm</li> <li>• FreqMonFactor_3p2920 - 3.29 ppm</li> <li>• FreqMonFactor_3p8100 - 3.81 ppm</li> <li>• FreqMonFactor_4p6000 - 4.6 ppm</li> </ul>

Definition at line 2114 of file DpllCnfg.c.

4.2.4.60 void IDTDpll\_SetHardAlarmThreshold ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *accepting*, T\_osUInt8 *rejecting* )

Set the frequency hard alarm accepting thresholds of reference clock monitoring.

## Parameters

<i>hdlr</i>	Device driver handler
<i>accepting</i>	Accepting threshold (ppm) is a multiple of frequency monitoring factor value. Accepting Threshold = (AcceptingValue + 1)*(FreqMonFactor)
<i>rejecting</i>	Rejecting threshold (ppm) is a multiple of frequency monitoring factor value. Rejecting Threshold = (RejectingValue + 1)*(FreqMonFactor)

Definition at line 2166 of file DpllCnfg.c.

4.2.4.61 void IDTDpll\_SetHitlessSwitchingFeature ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nEnable*, T\_osUInt8 *nFrozen* )

Set the configuration of hitless switching feature.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nEnable</i>	<ul style="list-style-type: none"> <li>• 0= Disable the hitless switching feature;</li> <li>• 1= Enable the hitless switching feature;</li> </ul>
<i>nFrozen</i>	<ul style="list-style-type: none"> <li>• 0= hitless switching feature is not frozen;</li> <li>• 1= HS feature is frozen, ignore the further hitless switching events</li> </ul>

Definition at line 2521 of file DpllCnfg.c.

4.2.4.62 void IDTDpll\_SetHoldoverFreq ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, long *pptOffset* )

Set DCO frequency to device. Note this function should only be called when DCO mode is enabled.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>pptOffset</i>	Parts per trillion offset.

Definition at line 1295 of file DpllCnfg.c.

4.2.4.63 void IDTDpll\_SetHoldoverMode ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_idtDpllHoldover *nMode*, T\_osUInt8 *nReadMode* )

Set calculation mode of holdover frequency and read back mode.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>nMode</i>	<ul style="list-style-type: none"> <li>• Holdover_ Instantaneous = automatic instantaneous mode</li> <li>• Holdover_ Slow_ Average = automatic slow average</li> <li>• Holdover_ Fast_ Average = Automatic fast average</li> <li>• Holdover_ Manual = Manual</li> </ul>
<i>nReadMode</i>	<ul style="list-style-type: none"> <li>• 0= Don't read value from device</li> <li>• 1= Read value calculated by device back to the holdover frequency register(0x5D,0x5E and 0x5F)</li> </ul>

Definition at line 1136 of file DpllCnfg.c.

4.2.4.64 void IDTDpll.SetIcpCtrl ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_osUInt8 *nIcp* )

Set charge pump control.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>nIcp</i>	Charge pump current selection ( 0 - 0x1F ); 10 = 40uA;

Definition at line 2269 of file DpllCnfg.c.

4.2.4.65 void IDTDpll.SetPhaseCoarseDetector ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_osUInt8 *nEnable*, T\_osUInt8 *nWide*, T\_osUInt8 *nMultiPhase*, T\_osUInt8 *nMultiPh8kEn* )

Set the coarse phase lose detector enable.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>nEnable</i>	<ul style="list-style-type: none"> <li>• 0= Disable the coarse phase detector</li> <li>• 1= Enable the coarse phase detector</li> </ul>
<i>nWide</i>	<ul style="list-style-type: none"> <li>• 0= Wide range disable</li> <li>• 1= Wide range enable</li> </ul>
<i>nMultiPhase</i>	<ul style="list-style-type: none"> <li>• 0= Limit to +/- 1UI</li> <li>• 1= Limit to PH_LOS_COARSE_LIMT register</li> </ul>

<i>nMultiPh8kEn</i>	<ul style="list-style-type: none"> <li>• 0= Limit to +/- 1UI when reference clock 8/4/2KHz clock</li> <li>• 1= Limit to PH_LOS_COARSE_LIMT register</li> </ul>
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Definition at line 813 of file DpllCnfg.c.

4.2.4.66 void IDTDpll\_SetPhaseCoarseLimit ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_idtCoarsePhaseLimit *nLimit* )

Set the limitation of the coarse phase lose detector.

#### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>nLimit</i>	Limitation of coarse phase loss detector. <ul style="list-style-type: none"> <li>• coarsePhaseLimit_1 - +/- 1 UI</li> <li>• coarsePhaseLimit_3 - +/- 3 UI</li> <li>• coarsePhaseLimit_7 - +/- 7 UI</li> <li>• coarsePhaseLimit_15 - +/- 15 UI</li> <li>• coarsePhaseLimit_31 - +/- 31 UI</li> <li>• coarsePhaseLimit_63 - +/- 63 UI</li> <li>• coarsePhaseLimit_127 - +/- 127 UI</li> <li>• coarsePhaseLimit_255 - +/- 255 UI</li> <li>• coarsePhaseLimit_511 - +/- 511 UI</li> <li>• coarsePhaseLimit_1023 - +/- 1023 UI T0 only</li> </ul>

Definition at line 934 of file DpllCnfg.c.

4.2.4.67 void IDTDpll\_SetPhaseFineDetectorEnable ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_osUInt8 *nEnable* )

Set the fine phase lose detector enable.

#### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>nEnable</i>	<ul style="list-style-type: none"> <li>• 0= Disable the fine phase detector</li> <li>• 1= Enable the fine phase detector</li> </ul>

Definition at line 991 of file DpllCnfg.c.

4.2.4.68 void IDTDpll\_SetPhaseFineLimit ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_idtFinePhaseLimit *nLimit* )

Set the limitation of the fine phase lose detector.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>nLimit</i>	Limitation of fine phase loss detector <ul style="list-style-type: none"> <li>• finePhaseLimit_45_90degree = +/- 45-90 degrees</li> <li>• finePhaseLimit_90_180degree = +/- 90-180 degrees</li> <li>• finePhaseLimit_180_360degree = +/- 180-360 degrees</li> <li>• finePhaseLimit_20_25nanosec = +/- 20-25 nanoseconds</li> <li>• finePhaseLimit_60_65nanosec = +/- 60-65 nanoseconds</li> <li>• finePhaseLimit_120_125nanosec = +/- 120-125 nanoseconds</li> <li>• finePhaseLimit_950_955nanosec = +/- 950-955 nanoseconds</li> </ul>

Definition at line 1045 of file DpllCnfg.c.

#### 4.2.4.69 void IDTDpll\_SetPhaseOffset ( T\_idtDrvHdlr *hdlr*, T\_osUInt16 *nOffset* )

Set the phase offset value.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nOffset</i>	Phase offset= $nOffset * 0x61$ ns;

Definition at line 2566 of file DpllCnfg.c.

#### 4.2.4.70 void IDTDpll\_SetPhaseSlope ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_idtPhaseSlope *nPhaseSlope* )

Set DPLL phase slope for DPLLs.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>nPhaseSlope</i>	<ul style="list-style-type: none"> <li>• phaseSlope_gr1244st3 = GR-1244 ST3 (61us/s)</li> <li>• phaseSlope_gr1244st3e = GR-1244 ST2,3E,ST3 (855ns/s)</li> <li>• phaseSlope_gr813 = GR-813,G.8262 (7.5us/s)</li> <li>• phaseSlope_noLimit = No limitation</li> </ul>

Definition at line 2351 of file DpllCnfg.c.

#### 4.2.4.71 void IDTDpll\_SetPhaseTransient ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nEnable* )

Set the configuration when phase transient occurs.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nEnable</i>	<ul style="list-style-type: none"> <li>• 0= Disable the phase transient monitor</li> <li>• 1= Enable the phase transient monitor</li> </ul>

Definition at line 2486 of file DpllCnfg.c.

4.2.4.72 void IDTDpll\_SetPpsFastLock ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nEnableFreq*, T\_osUInt8 *nEnablePhase* )

Enable/Disable 1 PPS fast lock.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nEnableFreq</i>	Enable (1) / Disable (0) frequency locking
<i>nEnablePhase</i>	Enable (1) / Disable (0) phase locking

Definition at line 2433 of file DpllCnfg.c.

4.2.4.73 void IDTDpll\_SetPpsPhase ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_idtDpllPpsPhasePostion *nPhase*, T\_idtDpllPpsPulseWidth *nPulse* )

Set PPS phase and pulse for DPLL.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>nPhase</i>	Phase position

## See Also

[T\\_idtDpllPpsPhasePostion](#)

## Parameters

<i>nPulse</i>	Pulse width
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## See Also

[T\\_idtDpllPpsPulseWidth](#)

Definition at line 2605 of file DpllCnfg.c.

4.2.4.74 void IDTDpll\_SetSoftAlarmThreshold ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *accepting*, T\_osUInt8 *rejecting* )

Set the frequency soft alarm accepting thresholds of reference clock monitoring.

## Parameters

<i>hdlr</i>	Device driver handler
<i>accepting</i>	Accepting threshold (ppm) is a multiple of frequency monitoring factor value. Accepting Threshold = (AcceptingValue + 1)*(FreqMonFactor)

<i>rejecting</i>	Rejecting threshold (ppm) is a multiple of frequency monitoring factor value. Rejecting Threshold = (RejectingValue + 1)*(FreqMonFactor)
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Definition at line 2220 of file DpllCnfg.c.

4.2.4.75 void IDTDpll.SetSonetGigEthOutputPath ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *instance*, T\_idtDpllInstance *inputDpll*, T\_idtSonetGigEthOutput *outputFreq* )

Set Sonet/GigE path configuration.

#### Parameters

<i>hdlr</i>	Device driver handler
<i>instance</i>	Sonet/GigE path instance 0..1
<i>inputDpll</i>	Dpll instance
<i>outputFreq</i>	Output frequency

Definition at line 1535 of file DpllCnfg.c.

4.2.4.76 void IDTDpll.SetTempHoldoverMode ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll*, T\_idtTemp\_holdover *nMode* )

Set calculation mode of temporary holdover frequency.

#### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance
<i>nMode</i>	<ul style="list-style-type: none"> <li>• Temp_Same_As_Full_Holdover = Same as the DPLL holdover mode</li> <li>• Temp_Holdover_Instantaneous = Automatic instantaneous mode</li> <li>• Temp_Holdover_Fast_Average = Automatic fast average</li> <li>• Temp_Holdover_Slow_Average = Automatic slow average</li> </ul>

Definition at line 1209 of file DpllCnfg.c.



## 4.3 General Function Module

Functions in this group are related to device wide provisioning and status.

### Data Structures

- struct [T\\_idtI2CtransData](#)  
*I2C address translation information used internally by the driver.*

### Macros

- #define [Activate\\_Edge\\_Rising](#) 0
- #define [Activate\\_Edge\\_Falling](#) 1
- #define [INT\\_Active\\_Low](#) 0
- #define [INT\\_Active\\_High](#) 1
- #define [NOMINAL\\_PPT\\_TO\\_2COMPL](#)(ppt) (T\_osUInt32)(((ppt)\*10)/884)  
*Conversion from parts per trillion to register unit value for nominal (oscillator) offset.*
- #define [NOMINAL\\_2COMPL\\_TO\\_PPT](#)(twoCompl) (long)((((twoCompl)\*884)/10)  
*Conversion from parts per trillion to register unit value for nominal (oscillator) offset.*
- #define [NOMINAL\\_MAX\\_PPT](#) 94893  
*Maximum oscillator offset value.*
- #define [NOMINAL\\_MIN\\_PPT](#) -94893  
*Minimum oscillator offset value.*

### Enumerations

- enum [networkType\\_t](#) { [Network\\_SDH](#) = 0, [Network\\_SONET](#) = 1, [Network\\_MAX](#) }
- Enumerated type listing types of selectable network type.
- enum [phaseTimeoutMultiplier\\_t](#) {  
[phaseTimeoutMultiplier\\_2](#) = 0, [phaseTimeoutMultiplier\\_4](#) = 1, [phaseTimeoutMultiplier\\_8](#) = 2, [phaseTimeoutMultiplier\\_16](#) = 3,  
[phaseTimeoutMultiplier\\_MAX](#) }
- Enumerated type listing phase alarm timeout multipliers.

### Functions

- T\_osUInt16 [IDTGeneral\\_GetDeviceID](#) (T\_idtDrvHdlr hdlr)  
*Get ID number of the device.*
- void [IDTGeneral\\_SetOscFreqOffset](#) (T\_idtDrvHdlr hdlr, long pptOffset)  
*Set compensation to the oscillator offset.*
- long [IDTGeneral\\_GetOscFreqOffset](#) (T\_idtDrvHdlr hdlr)  
*Get compensated oscillator offset.*
- void [IDTGeneral\\_SetNetworkType](#) (T\_idtDrvHdlr hdlr, [networkType\\_t](#) nType)  
*Set the network type, SDH or SONET.*
- [networkType\\_t](#) [IDTGeneral\\_GetNetworkType](#) (T\_idtDrvHdlr hdlr)  
*Get the network type, SDH or SONET.*
- void [IDTGeneral\\_SetRevertiveMode](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nEnable)  
*Set the device running in Revertive mode or not.*
- T\_osUInt8 [IDTGeneral\\_GetRevertiveMode](#) (T\_idtDrvHdlr hdlr)  
*Get the device running in Revertive mode or not.*

- void [IDTGeneral\\_SetTimeoutValue](#) (T\_idtDrvHdlr hdlr, [phaseTimeoutMultiplier\\_t](#) nMultiFactor, T\_osUInt8 nTimeout)  
*Set the value of time out of phase alarm Timeout(second)= nMultiFactor \* nTimeout.*
- void [IDTGeneral\\_GetTimeoutValue](#) (T\_idtDrvHdlr hdlr, [phaseTimeoutMultiplier\\_t](#) \*nMultiFactor\_p, T\_osUInt8 \*nTimeout\_p)  
*Get the value of time out of phase alarm Timeout(second)= nMultiFactor \* nTimeout.*
- void [IDTGeneral\\_SetOscActiveEdge](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nEdge)  
*Set the activate edge of main oscillator.*
- T\_osUInt8 [IDTGeneral\\_GetOscActiveEdge](#) (T\_idtDrvHdlr hdlr)  
*Get the activate edge of main oscillator.*
- void [IDTGeneral\\_SetProtectMode](#) (T\_idtDrvHdlr hdlr)  
*Enable protected register access mode.*
- void [IDTGeneral\\_SetSingleUnprotectMode](#) (T\_idtDrvHdlr hdlr)  
*Set single access register access mode.*
- void [IDTGeneral\\_SetFullyUnprotectMode](#) (T\_idtDrvHdlr hdlr)  
*Set fully un-protected register access mode.*
- void [IDTGeneral\\_SetFlagOnTDO](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nEnable)  
*Set TDO pin to indicate the fail of selected clock.*
- T\_osUInt8 [IDTGeneral\\_GetFlagOnTDO](#) (T\_idtDrvHdlr hdlr)  
*Get TDO pin to indicate the fail of selected clock.*
- void [IDTGeneral\\_SetUltraFastSwitch](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nEnable)  
*Set Ultra-fast-switch enable or not.*
- T\_osUInt8 [IDTGeneral\\_GetUltraFastSwitch](#) (T\_idtDrvHdlr hdlr)  
*Get Ultra-fast-switch enable or not.*
- void [IDTGeneral\\_SetHardAlarm](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nEnable)  
*Set Hard-alarm enable when the input exceeds the threshold.*
- T\_osUInt8 [IDTGeneral\\_GetHardAlarm](#) (T\_idtDrvHdlr hdlr)  
*Get Hard-alarm enable when the input exceeds the threshold.*
- T\_osUInt8 [IDTGeneral\\_i2cTranslate](#) (T\_osUInt8 i2cAddr, void \*transData)  
*I2C address translation function used internally by the driver.*
- void [IDTGeneral\\_InitDeviceCommon](#) (T\_idtDrvHdlr hdlr)
- T\_idtDrvHdlr [IDTGeneral\\_InitDriverCommon](#) (const char \*name, [T\\_idtDrvAccess](#) drvAccess, [T\\_idtDeviceType](#) deviceType, const [T\\_idtDrvDeviceConfig](#) \*deviceConfig, int useHighLevelApi)
- void [IDTGeneral\\_DeInitDriver](#) (T\_idtDrvHdlr hdlr)  
*De-initialize driver handler.*

### 4.3.1 Detailed Description

Functions in this group are related to device wide provisioning and status.

### 4.3.2 Macro Definition Documentation

#### 4.3.2.1 #define Activate\_Edge\_Falling 1

Definition at line 85 of file General.h.

#### 4.3.2.2 #define Activate\_Edge\_Rising 0

Definition at line 84 of file General.h.

#### 4.3.2.3 #define INT\_Active\_High 1

Definition at line 89 of file General.h.

#### 4.3.2.4 #define INT\_Active\_Low 0

Definition at line 88 of file General.h.

#### 4.3.2.5 #define NOMINAL\_2COMPL\_TO\_PPT( *twoCompl* ) (long)(((twoCompl)\*884)/10)

Conversion from parts per trillion to register unit value for nominal (oscillator) offset.

Definition at line 97 of file General.h.

#### 4.3.2.6 #define NOMINAL\_MAX\_PPT 94893

Maximum oscillator offset value.

Definition at line 100 of file General.h.

#### 4.3.2.7 #define NOMINAL\_MIN\_PPT -94893

Minimum oscillator offset value.

Definition at line 103 of file General.h.

#### 4.3.2.8 #define NOMINAL\_PPT\_TO\_2COMPL( *ppt* ) (T\_osUInt32)(((ppt)\*10)/884)

Conversion from parts per trillion to register unit value for nominal (oscillator) offset.

Definition at line 93 of file General.h.

### 4.3.3 Enumeration Type Documentation

#### 4.3.3.1 enum networkType\_t

Enumerated type listing types of selectable network type.

Enumerator

***Network\_SDH*** SDH network

***Network\_SONET*** SONET network

***Network\_MAX***

Definition at line 58 of file General.h.

#### 4.3.3.2 enum phaseTimeoutMultiplier\_t

Enumerated type listing phase alarm timeout multipliers.

Enumerator

***phaseTimeoutMultiplier\_2*** 2x Multiplier

***phaseTimeoutMultiplier\_4*** 4x Multiplier

***phaseTimeoutMultiplier\_8*** 8x Multiplier  
***phaseTimeoutMultiplier\_16*** 18x Multiplier  
***phaseTimeoutMultiplier\_MAX***

Definition at line 66 of file General.h.

#### 4.3.4 Function Documentation

##### 4.3.4.1 void IDTGeneral\_DeInitDriver ( T\_idtDrvHdlr *hdlr* )

De-initialize driver handler.

De-allocates handler. Handler is invalid after calling this function

###### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 568 of file General.c.

##### 4.3.4.2 T\_osUInt16 IDTGeneral\_GetDeviceID ( T\_idtDrvHdlr *hdlr* )

Get ID number of the device.

###### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

###### Returns

16-bit ID number

Definition at line 58 of file General.c.

##### 4.3.4.3 T\_osUInt8 IDTGeneral\_GetFlagOnTDO ( T\_idtDrvHdlr *hdlr* )

Get TDO pin to indicate the fail of selected clock.

###### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

###### Returns

- 0= Not enable to use TDO pin
- 1= enable to use the pin;

Definition at line 354 of file General.c.

##### 4.3.4.4 T\_osUInt8 IDTGeneral\_GetHardAlarm ( T\_idtDrvHdlr *hdlr* )

Get Hard-alarm enable when the input exceeds the threshold.

## Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

## Returns

- 0= Disable Hard-alarm feature
- 1= Enable the feature

Definition at line 414 of file General.c.

**4.3.4.5 networkType\_t IDTGeneral\_GetNetworkType ( T\_idtDrvHdlr *hdlr* )**

Get the network type, SDH or SONET.

## Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

## Returns

nType

- Network\_SDH = SDH network
- Network\_SONET = SONET network

Definition at line 172 of file General.c.

**4.3.4.6 T\_osUInt8 IDTGeneral\_GetOscActiveEdge ( T\_idtDrvHdlr *hdlr* )**

Get the activate edge of main oscillator.

## Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

## Returns

- 0= Rising edge is activate edge
- 1= Falling edge is activate edge

Definition at line 286 of file General.c.

**4.3.4.7 long IDTGeneral\_GetOscFreqOffset ( T\_idtDrvHdlr *hdlr* )**

Get compensated oscillator offset.

## Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

## Returns

Crystal oscillator frequency offset (in parts per trillion)

Definition at line 117 of file General.c.

#### 4.3.4.8 T\_osUInt8 IDTGeneral\_GetRevertiveMode ( T\_idtDrvHdlr hdlr )

Get the device running in Revertive mode or not.

##### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

##### Returns

nEnable

- 0= Works in Non-Revertive mode
- 1= Works in Revertive mode

Definition at line 203 of file General.c.

#### 4.3.4.9 void IDTGeneral\_GetTimeoutValue ( T\_idtDrvHdlr hdlr, phaseTimeoutMultiplier\_t \* nMultiFactor\_p, T\_osUInt8 \* nTimeout\_p )

Get the value of time out of phase alarm Timeout(second)= nMultiFactor \* nTimeout.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nMultiFactor_p</i>	<ul style="list-style-type: none"> <li>• phaseTimeoutMultiplier_2 - Multiple 2</li> <li>• phaseTimeoutMultiplier_4 - Multiple 4</li> <li>• phaseTimeoutMultiplier_8 - Multiple 8</li> <li>• phaseTimeoutMultiplier_16 - Multiple 16</li> </ul>
<i>nTimeout_p</i>	a 6-bit unsigned integer, unit is second;

Definition at line 252 of file General.c.

#### 4.3.4.10 T\_osUInt8 IDTGeneral\_GetUltraFastSwitch ( T\_idtDrvHdlr hdlr )

Get Ultra-fast-switch enable or not.

##### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

##### Returns

- 0= The feature is disabled
- 1= The feature is enabled

Definition at line 384 of file General.c.

#### 4.3.4.11 T\_osUInt8 IDTGeneral\_i2cTranslate ( T\_osUInt8 i2cAddr, void \* transData )

I2C address translation function used internally by the driver.

## Parameters

<i>i2cAddr</i>	I2C slave address
<i>transData</i>	Translation information

## Returns

Translated address

Definition at line 428 of file General.c.

4.3.4.12 void IDTGeneral\_InitDeviceCommon ( T\_idtDrvHdlr *hdlr* )

Definition at line 455 of file General.c.

4.3.4.13 T\_idtDrvHdlr IDTGeneral\_InitDriverCommon ( const char \* *name*, T\_idtDrvAccess *drvAccess*, T\_idtDeviceType *deviceType*, const T\_idtDrvDeviceConfig \* *deviceConfig*, int *useHighLevelApi* )

Definition at line 508 of file General.c.

4.3.4.14 void IDTGeneral\_SetFlagOnTDO ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nEnable* )

Set TDO pin to indicate the fail of selected clock.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nEnable</i>	<ul style="list-style-type: none"> <li>• 0= Not enable to use TDO pin</li> <li>• 1= enable to use the pin;</li> </ul>

Definition at line 338 of file General.c.

4.3.4.15 void IDTGeneral\_SetFullyUnprotectMode ( T\_idtDrvHdlr *hdlr* )

Set fully un-protected register access mode.

## Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 324 of file General.c.

4.3.4.16 void IDTGeneral\_SetHardAlarm ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nEnable* )

Set Hard-alarm enable when the input exceeds the threshold.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nEnable</i>	<ul style="list-style-type: none"> <li>• 0= Disable Hard-alarm feature</li> <li>• 1= Enable the feature</li> </ul>

Definition at line 398 of file General.c.

4.3.4.17 void IDTGeneral\_SetNetworkType ( T\_idtDrvHdlr *hdlr*, networkType\_t *nType* )

Set the network type, SDH or SONET.

Parameters

<i>hdlr</i>	Device driver handler
<i>nType</i>	<ul style="list-style-type: none"> <li>• Network_SDH = SDH network</li> <li>• Network_SONET = SONET network</li> </ul>

Definition at line 152 of file General.c.

4.3.4.18 void IDTGeneral\_SetOscActiveEdge ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nEdge* )

Set the activate edge of main oscillator.

Parameters

<i>hdlr</i>	Device driver handler
<i>nEdge</i>	<ul style="list-style-type: none"> <li>• 0= Rising edge is activate edge</li> <li>• 1= Falling edge is activate edge</li> </ul>

Definition at line 270 of file General.c.

4.3.4.19 void IDTGeneral\_SetOscFreqOffset ( T\_idtDrvHdlr *hdlr*, long *pptOffset* )

Set compensation to the oscillator offset.

Parameters

<i>hdlr</i>	Device driver handler
<i>pptOffset</i>	Crystal oscillator frequency offset (in parts per trillion)

Definition at line 78 of file General.c.

4.3.4.20 void IDTGeneral\_SetProtectMode ( T\_idtDrvHdlr *hdlr* )

Enable protected register access mode.

Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 298 of file General.c.

4.3.4.21 void IDTGeneral\_SetRevertiveMode ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nEnable* )

Set the device running in Revertive mode or not.



## Parameters

<i>hdlr</i>	Device driver handler
<i>nEnable</i>	<ul style="list-style-type: none"> <li>• 0= Works in Non-Revertive mode</li> <li>• 1= Works in Revertive mode</li> </ul>

Definition at line 186 of file General.c.

#### 4.3.4.22 void IDTGeneral\_SetSingleUnprotectMode ( T\_idtDrvHdlr *hdlr* )

Set single access register access mode.

## Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 311 of file General.c.

#### 4.3.4.23 void IDTGeneral\_SetTimeoutValue ( T\_idtDrvHdlr *hdlr*, phaseTimeoutMultiplier\_t *nMultiFactor*, T\_osUInt8 *nTimeout* )

Set the value of time out of phase alarm Timeout(second)= *nMultiFactor* \* *nTimeout*.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nMultiFactor</i>	<ul style="list-style-type: none"> <li>• phaseTimeoutMultiplier_2 - Multiple 2</li> <li>• phaseTimeoutMultiplier_4 - Multiple 4</li> <li>• phaseTimeoutMultiplier_8 - Multiple 8</li> <li>• phaseTimeoutMultiplier_16 - Multiple 16</li> </ul>
<i>nTimeout</i>	a 6-bit unsigned integer, unit is second;

Definition at line 221 of file General.c.

#### 4.3.4.24 void IDTGeneral\_SetUltraFastSwitch ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nEnable* )

Set Ultra-fast-switch enable or not.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nEnable</i>	<ul style="list-style-type: none"> <li>• 0= The feature is disabled</li> <li>• 1= The feature is enabled</li> </ul>

Definition at line 368 of file General.c.

## 4.4 Hardware Abstraction Layer Module

Functions in this group are related to hardware abstraction layer.

### Macros

- #define `IDT_HAL_USE_MACRO` 0
- #define `IDTHAL_ModifyBitfield`(regVal, mask, lsb, data)  
*Define function to set bitfield value of read data from device.*
- #define `IDTHAL_GetBitfield`(regVal, mask, lsb) (((regVal) & (mask)) >> (lsb))  
*Define function to get bitfield value of read data from device.*

### Functions

- void `IDTHAL_WriteBitfield` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset, T\_osUInt8 mask, T\_osUInt8 lsb, T\_osUInt8 data)  
*Define function to write a bitfield to a device.*
- void `IDTHAL_WriteBitfield_Ext` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset, T\_osUInt8 mask, T\_osUInt8 lsb, T\_osUInt8 data)  
*Define function to write a bitfield to a device.*
- T\_osUInt8 `IDTHAL_ReadBitfield` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset, T\_osUInt8 mask, T\_osUInt8 lsb)  
*Define function to read a bitfield from device.*
- T\_osUInt8 `IDTHAL_ReadBitfield_Ext` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset, T\_osUInt8 mask, T\_osUInt8 lsb)  
*Define function to read a bitfield from device.*
- T\_osUInt8 `IDTHal_Read` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset)  
*Function to read from device.*
- void `IDTHal_Write` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset, T\_osUInt8 data)  
*Define function to write to device.*
- T\_osUInt8 `IDTHal_Read_Ext` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset)  
*Function to read from device apll address space.*
- void `IDTHal_Write_Ext` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset, T\_osUInt8 data)  
*Function to write to device apll address space.*

#### 4.4.1 Detailed Description

Functions in this group are related to hardware abstraction layer.

#### 4.4.2 Macro Definition Documentation

##### 4.4.2.1 #define IDT\_HAL\_USE\_MACRO 0

Definition at line 53 of file Hal.h.

##### 4.4.2.2 #define IDTHAL\_GetBitfield( regVal, mask, lsb ) (((regVal) & (mask)) >> (lsb))

Define function to get bitfield value of read data from device.

This macro function can be used after a register is read from a device. This macro **doesn't** access the device.

#### Parameters

<i>regVal</i>	register data value.
<i>mask</i>	Bitfield mask
<i>lsb</i>	Least significant bit

Definition at line 80 of file Hal.h.

#### 4.4.2.3 #define IDTHAL\_ModifyBitfield( *regVal*, *mask*, *lsb*, *data* )

##### Value:

```
regVal = ((regVal & ~(mask)) |
          ((data) << (lsb)) & (mask))
```

Define function to set bitfield value of read data from device.

This macro function can be used after a register is read from a device. This macro **doesn't** access the device.

##### Parameters

<i>regVal</i>	register data value.
<i>mask</i>	Bitfield mask
<i>lsb</i>	Least significant bit
<i>data</i>	Bit field data to set

Definition at line 66 of file Hal.h.

#### 4.4.3 Function Documentation

##### 4.4.3.1 T\_osUInt8 IDTHal\_Read ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *offset* )

Function to read from device.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>offset</i>	Register address offset

Function to read from device.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>offset</i>	Register address offset

Definition at line 152 of file Hal.c.

##### 4.4.3.2 T\_osUInt8 IDTHal\_Read.Ext ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *offset* )

Function to read from device apll address space.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>offset</i>	Register address offset

Definition at line 209 of file Hal.c.

##### 4.4.3.3 T\_osUInt8 IDTHAL\_ReadBitfield ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *offset*, T\_osUInt8 *mask*, T\_osUInt8 *lsb* )

Define function to read a bitfield from device.

**Parameters**

<i>hdlr</i>	Device driver handler
<i>offset</i>	Register address offset
<i>mask</i>	Bitfield mask
<i>lsb</i>	Least significant bit

**Returns**

Bit field value

Definition at line 108 of file Hal.c.

#### 4.4.3.4 T\_osUInt8 IDTHAL\_ReadBitfield\_Ext ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *offset*, T\_osUInt8 *mask*, T\_osUInt8 *lsb* )

Define function to read a bitfield from device.

**Parameters**

<i>hdlr</i>	Device driver handler
<i>offset</i>	Register address offset
<i>mask</i>	Bitfield mask
<i>lsb</i>	Least significant bit

**Returns**

Bit field value

Definition at line 131 of file Hal.c.

#### 4.4.3.5 void IDTHal\_Write ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *offset*, T\_osUInt8 *data* )

Define function to write to device.

**Parameters**

<i>hdlr</i>	Device driver handler
<i>offset</i>	Register address offset
<i>data</i>	Data to write

Define function to write to device.

**Parameters**

<i>hdlr</i>	Device driver handler
<i>offset</i>	Register address offset
<i>data</i>	Data to write

Definition at line 181 of file Hal.c.

#### 4.4.3.6 void IDTHal\_Write\_Ext ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *offset*, T\_osUInt8 *data* )

Function to write to device apll address space.

## Parameters

<i>hdlr</i>	Device driver handler
<i>offset</i>	Register address offset
<i>data</i>	Data to write

Definition at line 238 of file Hal.c.

4.4.3.7 void IDTHAL\_WriteBitfield ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *offset*, T\_osUInt8 *mask*, T\_osUInt8 *lsb*, T\_osUInt8 *data* )

Define function to write a bitfield to a device.

## Parameters

<i>hdlr</i>	Device driver handler
<i>offset</i>	Register address offset
<i>mask</i>	Bitfield mask
<i>lsb</i>	Least significant bit
<i>data</i>	Bit field data to write

Definition at line 60 of file Hal.c.

4.4.3.8 void IDTHAL\_WriteBitfield\_Ext ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *offset*, T\_osUInt8 *mask*, T\_osUInt8 *lsb*, T\_osUInt8 *data* )

Define function to write a bitfield to a device.

## Parameters

<i>hdlr</i>	Device driver handler
<i>offset</i>	Register address offset
<i>mask</i>	Bitfield mask
<i>lsb</i>	Least significant bit
<i>data</i>	Bit field data to write

Definition at line 84 of file Hal.c.

## 4.5 Input Function Module

Functions in this group are related to input port provisioning.

### Macros

- #define `Input_Phase_Lock_Alarm` 1
- #define `Input_No_Activity_Alarm` 2
- #define `Input_Freq_Hard_Alarm` 4
- #define `IDT_TRANSLATE_EXT_TO_INT_INPORT`(hdlr, ext, internal)  
*Utility macro to check if input port is supported and to translated from external port to internal port.*
- #define `IDT_EXT_INPORT_POPULATED`(hdlr, ext) (hdlr->deviceConfig\_m->inputExt2IntXlate\_ma[(ext)])  
*Utility macro to check if input port is populated.*

### Enumerations

- enum `T_idtInputDividerMux` { `Divider_Bypass` = 0, `Divider_Lock8k` = 1, `Divider_DivN` = 2, `Divider_MAX` }  
*Enumerated type listing input divider modes.*
- enum `T_idtHighFrequencyDivisor` { `HF_Bypass` = 0, `HF_Divide_4` = 1, `HF_Divide_5` = 2, `HF_MAX` }  
*Enumerated type listing high frequency (> 155.52MHz) dividers.*
- enum `T_idtInputFrequencyBitfieldValue` {  
`Freq_8K` = 0, `Freq_1544M` = 1, `Freq_2048M` = 1, `Freq_648M` = 2,  
`Freq_1944M` = 3, `Freq_2592M` = 4, `Freq_3888M` = 5, `Freq_2K` = 9,  
`Freq_4K` = 10, `Freq_1PPS` = 11, `Freq_625M` = 12, `Freq_10M` = 13,  
`Freq_MAX` }  
*Enumerated type listing input frequencies.*
- enum `T_idtInputFrequencyFamily` {  
`InFreqFamily_8K` = 0, `InFreqFamily_1544M` = 1, `InFreqFamily_2048M` = 2, `InFreqFamily_648M` = 3,  
`InFreqFamily_1944M` = 4, `InFreqFamily_2592M` = 5, `InFreqFamily_3888M` = 6, `InFreqFamily_2K` = 7,  
`InFreqFamily_4K` = 8, `InFreqFamily_1PPS` = 9, `InFreqFamily_625M` = 10, `InFreqFamily_10M` = 11,  
`InFreqFamily_MAX` }  
*Enumerated type listing input frequency families.*
- enum `T_idtAmiInputFrequencyBitFieldValue` { `AmiFreq_64kHzPlus8kHz`, `AmiFreq_64kHzPlus400Hz`, `AmiFreq_MAX` }  
*Enumerated type listing AMI Input frequencies.*
- enum `T_idtInputSyncFreq` {  
`SYNC_8kHz`, `SYNC_1PPS`, `SYNC_4kHz`, `SYNC_2kHz`,  
`SYNC_MAX` }  
*Enumerated type listing possible input sync frequencies.*
- enum `T_externalSyncSampling` {  
`externalSyncSampling_onTarget`, `externalSyncSampling_0dot5Early`, `externalSyncSampling_1dot0Late`,  
`externalSyncSampling_0dot5Late`,  
`externalSyncSampling_MAX` }  
*Enumerated type listing sampling of input external sync.*
- enum `T_externalSyncEdge` { `externalSyncEdge_FallingEdge`, `externalSyncEdge_RisingEdge`, `externalSyncEdge_MAX` }  
*Enumerated type listing possible external sync alignment options.*
- enum `T_externalSyncAlarmRange` {  
`externalSyncAlarmRange_1`, `externalSyncAlarmRange_2`, `externalSyncAlarmRange_3`, `externalSyncAlarmRange_4`,  
`externalSyncAlarmRange_5`, `externalSyncAlarmRange_6`, `externalSyncAlarmRange_7`, `externalSyncAlarmRange_8`,  
`externalSyncAlarmRange_MAX` }

*Enumerate type listing ranges for external sync alarm.*

- enum `T_externalSyncBypass` { `externalSyncBypass_ExSync1`, `externalSyncBypass_AutoSel`, `externalSyncBypass_MAX` }

*Enumerated type listing output synchronization with respect to.*

- enum `T_externalSyncEnable` { `externalSyncEnable_Disable`, `externalSyncEnable_Enable`, `externalSyncEnable_Auto`, `externalSyncEnable_MAX` }

*Enumerated type listing enable options for external input sync.*

## Functions

- void `IDTInput_SetPriority` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo, `T_idtDpllInstance` nDpll, `T_osUInt8` nPriority)
 

*Set specified port to the priority.*
- `T_osUInt8` `IDTInput_GetPriority` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo, `T_idtDpllInstance` nDpll)
 

*Get the current priority of the specified port.*
- void `IDTInput_SetInputFrequency` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo, `T_idtInputFrequencyBitfieldValue` nFrequency)
 

*Set the frequency of the input clock at the specified port.*
- `T_idtInputFrequencyBitfieldValue` `IDTInput_GetInputFrequency` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo)
 

*Get frequency of the input clock at the specified port.*
- void `IDTInput_SetAmiInputFrequency` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo, `T_idtAmiInputFrequencyBitFieldValue` amiSignal)
 

*Provision AMI signal for input port.*
- `T_idtAmiInputFrequencyBitFieldValue` `IDTInput_GetAmiInputFrequency` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo)
 

*Function to retrieve AMI input frequency for input port.*
- void `IDTInput_SetActivityMonitor` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo, `T_osUInt8` nBucket)
 

*Select one of the four activity monitor configurations for the specified input port.*
- `T_osUInt8` `IDTInput_GetActivityMonitor` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo)
 

*Retrieve selected activity monitoring configuration.*
- void `IDTInput_SetBucketConfig` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nBucket, `T_osUInt8` nUpper, `T_osUInt8` nLower, `T_osUInt8` nSize, `T_osUInt8` nDecay)
 

*Set the configuration to Leaky Bucket activity monitoring.*
- void `IDTInput_GetBucketConfig` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nBucket, `T_osUInt8` \*nUpper\_p, `T_osUInt8` \*nLower\_p, `T_osUInt8` \*nSize\_p, `T_osUInt8` \*nDecay\_p)
 

*Get activity monitoring configuration (Leaky Bucket)*
- void `IDTInput_SetPreDivider` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo, `T_idtInputDividerMux` nDivider)
 

*Assign a pre-divider for the specified input.*
- `T_idtInputDividerMux` `IDTInput_GetPreDivider` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo)
 

*Get configured input port pre-divider.*
- void `IDTInput_SetDivisionFactor` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo, `T_osUInt16` iFactor)
 

*Set the dividen factor to pre-divider assigned to a certain input.*
- `T_osUInt16` `IDTInput_GetDivisionFactor` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo)
 

*Get the dividen factor to pre-divider assigned to a certain input.*
- void `IDTInput_SetInputHFdivider` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo, `T_idtHighFrequencyDivisor` nUsage)
 

*Set the usage of high frequency (> 155.52MHz) divider.*
- `T_idtHighFrequencyDivisor` `IDTInput_GetInputHFdivider` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo)
 

*Get high frequency configuration divider.*
- `T_osUInt8` `IDTInput_GetInputFreqOffset` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo)
 

*Get the frequency offset of the specified input clock. The returned value is updated every 16 seconds.*
- `T_osUInt8` `IDTInput_GetInputClockStatus` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo)

- Get the status of a specified input clock.*

  - `T_osUInt8 IDTInput_GetInputClockValidation` (`T_idtDrvHdlr hdlr`, `T_osUInt8 nInputNo`)

*Get the clock validation status of an input port.*
- `void IDTInput_EnableAllInputs` (`T_idtDrvHdlr hdlr`)

*Enable to select anyone of input clocks.*
- `void IDTInput_DisableAllInputs` (`T_idtDrvHdlr hdlr`)

*Disable to select anyone of input clocks.*
- `void IDTInput_SetInputEnable` (`T_idtDrvHdlr hdlr`, `T_osUInt8 nInputNo`, `T_osUInt8 enable`)

*Enable/Disable selected input.*
- `T_osUInt8 IDTInput_GetInputEnable` (`T_idtDrvHdlr hdlr`, `T_osUInt8 nInputNo`)

*Retrieve enable/disable status of selected input.*
- `void IDTInput_SetSyncFrequency` (`T_idtDrvHdlr hdlr`, `T_idtInputSyncFreq syncFreq`)

*Function to select input external sync frequency.*
- `T_idtInputSyncFreq IDTInput_GetSyncFrequency` (`T_idtDrvHdlr hdlr`)

*Function to retrieve select input external sync frequency.*
- `void IDTInput_SetSyncSampling` (`T_idtDrvHdlr hdlr`, `T_osUInt8 exSyncN`, `T_externalSyncSampling sampling`)

*Function to provision sampling configuration for external sync.*
- `T_externalSyncSampling IDTInput_GetSyncSampling` (`T_idtDrvHdlr hdlr`, `T_osUInt8 exSyncN`)

*Function to retrieve sampling configuration for external sync.*
- `void IDTInput_SetSyncEdge` (`T_idtDrvHdlr hdlr`, `T_externalSyncEdge edge`)

*Function to provision synchronization alignment.*
- `T_externalSyncEdge IDTInput_GetSyncEdge` (`T_idtDrvHdlr hdlr`)

*Function to retrieve synchronization alignment.*
- `void IDTInput_SetSyncAlarmRange` (`T_idtDrvHdlr hdlr`, `T_externalSyncAlarmRange range`)

*Function to provision the sync allowable range before alarming.*
- `T_externalSyncAlarmRange IDTInput_GetSyncAlarmRange` (`T_idtDrvHdlr hdlr`)

*Function to retrieve the sync allowable range before alarming.*
- `void IDTInput_SetSyncBypass` (`T_idtDrvHdlr hdlr`, `T_externalSyncBypass bypass`)

*Function to provision sync bypass mode.*
- `T_externalSyncBypass IDTInput_GetSyncBypass` (`T_idtDrvHdlr hdlr`)

*Function to retrieve sync bypass mode.*
- `void IDTInput_SetSyncEnable` (`T_idtDrvHdlr hdlr`, `T_externalSyncEnable enable`)

*Function to provision enable mode for input external sync.*
- `T_externalSyncEnable IDTInput_GetSyncEnable` (`T_idtDrvHdlr hdlr`)

*Function to retrieve external sync enable mode.*
- `T_idtInputFrequencyFamily IDTInput_InFreqBitValue2Family` (`T_idtDrvHdlr hdlr`, `T_idtInputFrequencyBitfield-Value inFreqBitValue`)

*Translate input frequency bit value to input frequency family.*

#### 4.5.1 Detailed Description

Functions in this group are related to input port provisioning. This module also include frequency monitoring controls too.



## 4.5.2 Macro Definition Documentation

### 4.5.2.1 #define IDT\_EXT\_INPORT\_POPULATED( *hdlr*, *ext* ) (hdlr->deviceConfig\_m->inputExt2IntXlate\_ma[(ext)])

Utility macro to check if input port is populated.

#### Parameters

<i>hdlr</i>	Device driver handle
<i>ext</i>	External input port number

#### Returns

a positive number - populated, 0 - not populated

Definition at line 223 of file Input.h.

### 4.5.2.2 #define IDT\_TRANSLATE\_EXT\_TO\_INT\_INPORT( *hdlr*, *ext*, *internal* )

#### Value:

```
do {
    OS_ASSERT((ext) <= IDT_DRV_MAX_INPUT);
    OS_ASSERT((ext) > 0);
    OS_ASSERTS(hdlr->deviceConfig_m->inputExt2IntXlate_ma[(ext)],
               ("Unsupported input port %d\n", (ext)));
    internal = hdlr->deviceConfig_m->inputExt2IntXlate_ma[(ext)];
} while(0)
```

Utility macro to check if input port is supported and to translated from external port to internal port.

#### Parameters

<i>hdlr</i>	Device driver handle
<i>ext</i>	External input port number
<i>internal</i>	Internal input number

Definition at line 208 of file Input.h.

### 4.5.2.3 #define Input\_Freq\_Hard\_Alarm 4

Definition at line 79 of file Input.h.

### 4.5.2.4 #define Input\_No\_Activity\_Alarm 2

Definition at line 78 of file Input.h.

### 4.5.2.5 #define Input\_Phase\_Lock\_Alarm 1

Definition at line 77 of file Input.h.

## 4.5.3 Enumeration Type Documentation

### 4.5.3.1 enum T\_externalSyncAlarmRange

Enumerate type listing ranges for external sync alarm.

Enumerator

***externalSyncAlarmRange\_1*** +/- 1 UI range  
***externalSyncAlarmRange\_2*** +/- 2 UI range  
***externalSyncAlarmRange\_3*** +/- 3 UI range  
***externalSyncAlarmRange\_4*** +/- 4 UI range  
***externalSyncAlarmRange\_5*** +/- 5 UI range  
***externalSyncAlarmRange\_6*** +/- 6 UI range  
***externalSyncAlarmRange\_7*** +/- 7 UI range  
***externalSyncAlarmRange\_8*** +/- 8 UI range  
***externalSyncAlarmRange\_MAX***

Definition at line 161 of file Input.h.

#### 4.5.3.2 enum T\_externalSyncBypass

Enumerated type listing output synchronization with respect to.

Enumerator

***externalSyncBypass\_ExSync1*** Synchronized to external sync 1  
***externalSyncBypass\_AutoSel*** Auto synchronize using DPLL #1. If DPLL #1 select IN1 or IN4 then synchronize to external sync1 If DPLL #1 select IN2 then synchronize to external sync 2. If no input selected by DPLL #1, external sync are not synchronized  
***externalSyncBypass\_MAX***

Definition at line 176 of file Input.h.

#### 4.5.3.3 enum T\_externalSyncEdge

Enumerated type listing possible external sync alignment options.

Enumerator

***externalSyncEdge\_FallingEdge*** External sync align to falling edge  
***externalSyncEdge\_RisingEdge*** External sync align to rising edge  
***externalSyncEdge\_MAX***

Definition at line 151 of file Input.h.

#### 4.5.3.4 enum T\_externalSyncEnable

Enumerated type listing enable options for external input sync.

Enumerator

***externalSyncEnable\_Disable*** Disable external sync  
***externalSyncEnable\_Enable*** Enable external sync  
***externalSyncEnable\_Auto*** Enable/Disable external sync based on DPLL #1 locking to (internal) input 4  
***externalSyncEnable\_MAX***

Definition at line 193 of file Input.h.

## 4.5.3.5 enum T\_externalSyncSampling

Enumerated type listing sampling of input external sync.

Enumerator

**externalSyncSampling\_onTarget** On target (0 UI)  
**externalSyncSampling\_0dot5Early** 0.5 UI early  
**externalSyncSampling\_1dot0Late** 1.0 UI late  
**externalSyncSampling\_0dot5Late** 0.5 UI late  
**externalSyncSampling\_MAX**

Definition at line 139 of file Input.h.

## 4.5.3.6 enum T\_idtAmiInputFrequencyBitFieldValue

Enumerated type listing AMI Input frequencies.

Enumerator

**AmiFreq\_64kHzPlus8kHz** 64 kHz + 8 kHz signal  
**AmiFreq\_64kHzPlus400Hz** 64 kHz + 400 Hz signal  
**AmiFreq\_MAX**

Definition at line 118 of file Input.h.

## 4.5.3.7 enum T\_idtHighFrequencyDivisor

Enumerated type listing high frequency (>155.52MHz) dividers.

Enumerator

**HF\_Bypass** Bypass high frequency divider  
**HF\_Divide\_4** HF Divide by 4  
**HF\_Divide\_5** HF Divide by 5  
**HF\_MAX**

Definition at line 68 of file Input.h.

## 4.5.3.8 enum T\_idtInputDividerMux

Enumerated type listing input divider modes.

Enumerator

**Divider\_Bypass** Bypass divider mode  
**Divider\_Lock8k** Lock 8kHz divider mode  
**Divider\_DivN** Divide by N (DivN) mode  
**Divider\_MAX**

Definition at line 59 of file Input.h.

#### 4.5.3.9 enum T\_idtInputFrequencyBitfieldValue

Enumerated type listing input frequencies.

Enumerator

*Freq\_8K*

*Freq\_1544M*

*Freq\_2048M*

*Freq\_648M*

*Freq\_1944M*

*Freq\_2592M*

*Freq\_3888M*

*Freq\_2K*

*Freq\_4K*

*Freq\_1PPS*

*Freq\_625M*

*Freq\_10M*

*Freq\_MAX*

Definition at line 82 of file Input.h.

#### 4.5.3.10 enum T\_idtInputFrequencyFamily

Enumerated type listing input frequency families.

Enumerator

*InFreqFamily\_8K*

*InFreqFamily\_1544M*

*InFreqFamily\_2048M*

*InFreqFamily\_648M*

*InFreqFamily\_1944M*

*InFreqFamily\_2592M*

*InFreqFamily\_3888M*

*InFreqFamily\_2K*

*InFreqFamily\_4K*

*InFreqFamily\_1PPS*

*InFreqFamily\_625M*

*InFreqFamily\_10M*

*InFreqFamily\_MAX*

Definition at line 100 of file Input.h.

## 4.5.3.11 enum T\_idtInputSyncFreq

Enumerated type listing possible input sync frequencies.

Enumerator

**SYNC\_8kHz** 8 kHz sync input  
**SYNC\_1PPS** 1 PPS sync input  
**SYNC\_4kHz** 4 kHz sync input  
**SYNC\_2kHz** 2 kHz sync input  
**SYNC\_MAX**

Definition at line 128 of file Input.h.

## 4.5.4 Function Documentation

4.5.4.1 void IDTInput\_DisableAllInputs ( T\_idtDrvHdlr *hdlr* )

Disable to select anyone of input clocks.

Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 790 of file Input.c.

4.5.4.2 void IDTInput\_EnableAllInputs ( T\_idtDrvHdlr *hdlr* )

Enable to select anyone of input clocks.

Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 771 of file Input.c.

4.5.4.3 T\_osUInt8 IDTInput\_GetActivityMonitor ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nInputNo* )

Retrieve selected activity monitoring configuration.

Parameters

<i>hdlr</i>	Device driver handler
<i>nInputNo</i>	the specified port

Returns

nBucket the bucket number assigned to the specified port.

- 0= bucket 0, controlled by the registers from 31H to 34H
- 1= bucket 1, controlled by the registers from 35H to 38H
- 2= bucket 2, controlled by the registers from 39H to 3cH
- 3= bucket 3, controlled by the registers from 3dH to 40H

Definition at line 363 of file Input.c.

#### 4.5.4.4 T\_idtAmiInputFrequencyBitFieldValue IDTInput\_GetAmiInputFrequency ( T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo )

Function to retrieve AMI input frequency for input port.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nInputNo</i>	the specified input port number

##### Returns

AMI input frequency

Definition at line 1238 of file Input.c.

#### 4.5.4.5 void IDTInput\_GetBucketConfig ( T\_idtDrvHdlr hdlr, T\_osUInt8 nBucket, T\_osUInt8 \* nUpper\_p, T\_osUInt8 \* nLower\_p, T\_osUInt8 \* nSize\_p, T\_osUInt8 \* nDecay\_p )

Get activity monitoring configuration (Leaky Bucket)

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nBucket</i>	the bucket number to provision 0-3
<i>nUpper_p</i>	Upper threshold of Leaky Bucket
<i>nLower_p</i>	Lower threshold of Leaky Bucket
<i>nSize_p</i>	Bucket size of Leaky Bucket
<i>nDecay_p</i>	Decay rate of Leaky bucket <ul style="list-style-type: none"> <li>• 0x0 = Bucket decrease by 1 in every 128 ms</li> <li>• 0x1 = Bucket decrease by 1 in every 256 ms</li> <li>• 0x2 = Bucket decrease by 1 in every 512 ms</li> <li>• 0x3 = Bucket decrease by 1 in every 1024 ms</li> </ul>

Definition at line 431 of file Input.c.

#### 4.5.4.6 T\_osUInt16 IDTInput\_GetDivisionFactor ( T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo )

Get the dividen factor to pre-divider assigned to a certain input.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nInputNo</i>	the input port number to which the pre-divider

##### Returns

division factor as a preset of the specified divider (24 bit 2's compliment)

Definition at line 568 of file Input.c.

#### 4.5.4.7 T\_osUInt8 IDTInput\_GetInputClockStatus ( T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo )

Get the status of a specified input clock.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nInputNo</i>	number of the input clock

## Returns

nStatus.Bit0: =1, Phase lock alarm. =0, No phase lock alarm. nStatus.Bit1: =1, Clock no-activity alarm. =0, No clock no-activity alarm. nStatus.Bit2: =1, Clock frequency hard alarm. =0, No clock frequency hard alarm.

Definition at line 710 of file Input.c.

4.5.4.8 T\_osUInt8 IDTInput\_GetInputClockValidation ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nInputNo* )

Get the clock validation status of an input port.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nInputNo</i>	Input port

## Returns

0-Invalid clock, 1-Valid clock

Definition at line 738 of file Input.c.

4.5.4.9 T\_osUInt8 IDTInput\_GetInputEnable ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nInputNo* )

Retrieve enable/disable status of selected input.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nInputNo</i>	number of the input clock

## Returns

enable 1-Disable 0-Enable input port

Definition at line 849 of file Input.c.

4.5.4.10 T\_osUInt8 IDTInput\_GetInputFreqOffset ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nInputNo* )

Get the frequency offset of the specified input clock. The returned value is updated every 16 seconds.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nInputNo</i>	number of the input clock whose frequency offset is returned.

## Returns

Frequency offset

Definition at line 675 of file Input.c.

#### 4.5.4.11 T\_idtInputFrequencyBitfieldValue IDTInput\_GetInputFrequency ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nInputNo* )

Get frequency of the input clock at the specified port.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nInputNo</i>	the specified input port number

##### Returns

nFrequency code of input clock frequency.

- Freq\_8K= 8 kHz
- Freq\_1544M/Freq\_2048M= 1.544/2.048 MHz
- Freq\_648M= 6.48 MHz
- Freq\_1944M= 19.44 MHz
- Freq\_2592M= 25.92 MHz
- Freq\_3888M= 38.88 MHz
- Freq\_2K= 2 kHz
- Freq\_4K= 4 kHz
- Freq\_1PPS= 1 PPS
- Freq\_625M= 6.25 MHz
- Freq\_10M= 10 MHz

Definition at line 299 of file Input.c.

#### 4.5.4.12 T\_idtHighFrequencyDivisor IDTInput\_GetInputHFdivider ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nInputNo* )

Get high frequency configuration divider.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nInputNo</i>	Input port number

##### Returns

- HF\_Bypass : The HF divider is bypassed
- HF\_Divide\_4 : The HF divider's division factor is 4
- HF\_Divide\_5 : The HF divider's division factor is 5

Definition at line 640 of file Input.c.

#### 4.5.4.13 T\_idtInputDividerMux IDTInput\_GetPreDivider ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nInputNo* )

Get configured input port pre-divider.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nInputNo</i>	the specified input port number



**Returns**

pre-divider assigned to the specified input

- 0 = bypass both dividers
- 1 = Lock-8k divider
- 2 = DivN divider

Definition at line 502 of file Input.c.

#### 4.5.4.14 T\_osUInt8 IDTInput.GetPriority ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nInputNo*, T\_idtDpllInstance *nDpll* )

Get the current priority of the specified port.

**Parameters**

<i>hdlr</i>	Device driver handler
<i>nInputNo</i>	Input port number (consult data sheet for valid port numbers)
<i>nDpll</i>	DPLL instance

**Returns**

Priority of the port

Definition at line 211 of file Input.c.

#### 4.5.4.15 T\_externalSyncAlarmRange IDTInput.GetSyncAlarmRange ( T\_idtDrvHdlr *hdlr* )

Function to retrieve the sync allowable range before alarming.

**Parameters**

<i>hdlr</i>	Device driver handler
-------------	-----------------------

**Returns**

Allowable range

Definition at line 1053 of file Input.c.

#### 4.5.4.16 T\_externalSyncBypass IDTInput.GetSyncBypass ( T\_idtDrvHdlr *hdlr* )

Function to retrieve sync bypass mode.

**Parameters**

<i>hdlr</i>	Device driver handler
-------------	-----------------------

**Returns**

Bypass mode

Definition at line 1091 of file Input.c.

#### 4.5.4.17 T\_externalSyncEdge IDTInput\_GetSyncEdge ( T\_idtDrvHdlr hdlr )

Function to retrieve synchronization alignment.

##### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

##### Returns

Edge to synchronize against

Definition at line 1014 of file Input.c.

#### 4.5.4.18 T\_externalSyncEnable IDTInput\_GetSyncEnable ( T\_idtDrvHdlr hdlr )

Function to retrieve external sync enable mode.

##### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

##### Returns

Enable mode

Definition at line 1165 of file Input.c.

#### 4.5.4.19 T\_idtInputSyncFreq IDTInput\_GetSyncFrequency ( T\_idtDrvHdlr hdlr )

Function to retrieve select input external sync frequency.

##### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

##### Returns

Input external sync

Definition at line 902 of file Input.c.

#### 4.5.4.20 T\_externalSyncSampling IDTInput\_GetSyncSampling ( T\_idtDrvHdlr hdlr, T\_osUInt8 exSyncN )

Function to retrieve sampling configuration for external sync.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>exSyncN</i>	External sync (1-EXT SYNC1, 2-EX SYNC2)

##### Returns

Sampling configuration

Definition at line 957 of file Input.c.

4.5.4.21 `T_idtInputFrequencyFamily IDTInput.InFreqBitValue2Family ( T_idtDrvHdlr hdlr,  
T_idtInputFrequencyBitfieldValue inFreqBitValue )`

Translate input frequency bit value to input frequency family.

Parameters

<i>hdlr</i>	Device driver handler
<i>inFreqBitValue</i>	Input frequency bit value

Returns

Input frequency family

Definition at line 95 of file Input.c.

4.5.4.22 `void IDTInput.SetActivityMonitor ( T_idtDrvHdlr hdlr, T_osUInt8 nInputNo, T_osUInt8 nBucket )`

Select one of the four activity monitor configurations for the specified input port.

Parameters

<i>hdlr</i>	Device driver handler
<i>nInputNo</i>	the specified port
<i>nBucket</i>	the bucket number assigned to the specified port. <ul style="list-style-type: none"> <li>• 0= bucket 0, controlled by the registers from 31H to 34H</li> <li>• 1= bucket 1, controlled by the registers from 35H to 38H</li> <li>• 2= bucket 2, controlled by the registers from 39H to 3cH</li> <li>• 3= bucket 3, controlled by the registers from 3dH to 40H</li> </ul>

Definition at line 329 of file Input.c.

4.5.4.23 `void IDTInput.SetAmiInputFrequency ( T_idtDrvHdlr hdlr, T_osUInt8 nInputNo, T_idtAmiInputFrequencyBit-  
FieldValue amiSignal )`

Provision AMI signal for input port.

Parameters

<i>hdlr</i>	Device driver handler
<i>nInputNo</i>	the specified input port number
<i>amiSignal</i>	AMI signal <ul style="list-style-type: none"> <li>• AmiFreq_64kHzPlus8kHz= 64 kHz + 8 kHz signal</li> <li>• AmiFreq_64kHzPlus400Hz= 64 kHz + 400 Hz signal</li> </ul>

Definition at line 1195 of file Input.c.

4.5.4.24 `void IDTInput.SetBucketConfig ( T_idtDrvHdlr hdlr, T_osUInt8 nBucket, T_osUInt8 nUpper, T_osUInt8 nLower,  
T_osUInt8 nSize, T_osUInt8 nDecay )`

Set the configuration to Leaky Bucket activity monitoring.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nBucket</i>	the bucket number to provision 0-3
<i>nUpper</i>	Upper threshold of Leaky Bucket
<i>nLower</i>	Lower threshold of Leaky Bucket
<i>nSize</i>	Bucket size of Leaky Bucket
<i>nDecay</i>	Decay rate of Leaky bucket <ul style="list-style-type: none"> <li>• 0x0 = Bucket decrease by 1 in every 128 ms</li> <li>• 0x1 = Bucket decrease by 1 in every 256 ms</li> <li>• 0x2 = Bucket decrease by 1 in every 512 ms</li> <li>• 0x3 = Bucket decrease by 1 in every 1024 ms</li> </ul>

Definition at line 393 of file Input.c.

#### 4.5.4.25 void IDTInput\_SetDivisionFactor ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nInputNo*, T\_osUInt16 *nFactor* )

Set the dividen factor to pre-divider assigned to a certain input.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nInputNo</i>	the input port number to which the pre-divider
<i>nFactor</i>	division factor as a preset of the specified divider

Definition at line 531 of file Input.c.

#### 4.5.4.26 void IDTInput\_SetInputEnable ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nInputNo*, T\_osUInt8 *enable* )

Enable/Disable selected input.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nInputNo</i>	number of the input clock
<i>enable</i>	1-Disable 0-Enable input port

Definition at line 811 of file Input.c.

#### 4.5.4.27 void IDTInput\_SetInputFrequency ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nInputNo*, T\_idtInputFrequencyBitfieldValue *nFrequency* )

Set the frequency of the input clock at the specified port.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nInputNo</i>	the specified input port number
<i>nFrequency</i>	code of input clock frequency. <ul style="list-style-type: none"> <li>• Freq_8K= 8 kHz</li> <li>• Freq_1544M/Freq_2048M= 1.544/2.048 MHz</li> <li>• Freq_648M= 6.48 MHz</li> <li>• Freq_1944M= 19.44 MHz</li> <li>• Freq_2592M= 25.92 MHz</li> <li>• Freq_3888M= 38.88 MHz</li> <li>• Freq_2K= 2 kHz</li> <li>• Freq_4K= 4 kHz</li> <li>• Freq_1PPS= 1 PPS</li> <li>• Freq_625M= 6.25 MHz</li> <li>• Freq_10M= 10 MHz</li> </ul>

Definition at line 255 of file Input.c.

#### 4.5.4.28 void IDTInput\_SetInputHFdivider ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nInputNo*, T\_idtHighFrequencyDivisor *nUsage* )

Set the usage of high frequency (> 155.52MHz) divider.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nInputNo</i>	Input port number
<i>nUsage</i>	<ul style="list-style-type: none"> <li>• HF_Bypass : The HF divider is bypassed</li> <li>• HF_Divide_4 : The HF divider's division factor is 4</li> <li>• HF_Divide_5 : The HF divider's division factor is 5</li> </ul>

Definition at line 600 of file Input.c.

#### 4.5.4.29 void IDTInput\_SetPreDivider ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nInputNo*, T\_idtInputDividerMux *nDivider* )

Assign a pre-divider for the specified input.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nInputNo</i>	the specified input port number
<i>nDivider</i>	pre-divider assigned to the specified input <ul style="list-style-type: none"> <li>• 0 = bypass both dividers</li> <li>• 1 = Lock-8k divider</li> <li>• 2 = DivN divider</li> </ul>

Definition at line 466 of file Input.c.

4.5.4.30 void IDTInput\_SetPriority ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nInputNo*, T\_idtDpllInstance *nDpll*, T\_osUInt8 *nPriority* )

Set specified port to the priority.

Parameters

<i>hdlr</i>	Device driver handler
<i>nInputNo</i>	Input port number (consult data sheet for valid port numbers)
<i>nDpll</i>	DPLL instance
<i>nPriority</i>	the priority of the specified port

Definition at line 170 of file Input.c.

4.5.4.31 void IDTInput\_SetSyncAlarmRange ( T\_idtDrvHdlr *hdlr*, T\_externalSyncAlarmRange *range* )

Function to provision the sync allowable range before alarming.

Parameters

<i>hdlr</i>	Device driver handler
<i>range</i>	Allowable range

Definition at line 1030 of file Input.c.

4.5.4.32 void IDTInput\_SetSyncBypass ( T\_idtDrvHdlr *hdlr*, T\_externalSyncBypass *bypass* )

Function to provision sync bypass mode.

Parameters

<i>hdlr</i>	Device driver handler
<i>bypass</i>	Bypass mode

Definition at line 1069 of file Input.c.

4.5.4.33 void IDTInput\_SetSyncEdge ( T\_idtDrvHdlr *hdlr*, T\_externalSyncEdge *edge* )

Function to provision synchronization alignment.

Parameters

<i>hdlr</i>	Device driver handler
<i>edge</i>	Edge to synchronize against

Definition at line 992 of file Input.c.

4.5.4.34 void IDTInput\_SetSyncEnable ( T\_idtDrvHdlr *hdlr*, T\_externalSyncEnable *enable* )

Function to provision enable mode for input external sync.

Parameters

<i>hdlr</i>	Device driver handler
<i>enable</i>	Enable mode

Definition at line 1106 of file Input.c.

4.5.4.35 void IDTInput\_SetSyncFrequency ( T\_idtDrvHdlr *hdlr*, T\_idtInputSyncFreq *syncFreq* )

Function to select input external sync frequency.

Parameters

<i>hdlr</i>	Device driver handler
<i>syncFreq</i>	Input external sync

Definition at line 881 of file Input.c.

4.5.4.36 void IDTInput\_SetSyncSampling ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *exSyncN*, T\_externalSyncSampling *sampling* )

Function to provision sampling configuration for external sync.

Parameters

<i>hdlr</i>	Device driver handler
<i>exSyncN</i>	External sync (1-EXT SYNC1, 2-EX SYNC2)
<i>sampling</i>	Sampling configuration

Definition at line 918 of file Input.c.

## 4.6 Output Function Module

Functions in this group are related to output port provisioning.

### Macros

- #define `IDT_TRANSLATE_EXT_TO_INT_OUTPORT`(hdlr, ext, internal)  
*Utility macro to check if output port is supported and to translated from external port to internal port.*
- #define `IDT_EXT_OUTPORT_POPULATED`(hdlr, ext) (hdlr->deviceConfig\_m->outputExt2IntXlate\_ma[(ext)])  
*Utility macro to check if output port is populated.*

### Enumerations

- enum `T_outputPathType` {  
`OutputPath_SonetGigEth`, `OutputPath_7776kHz`, `OutputPath_Eth`, `OutputPath_16E1_16T1`,  
`OutputPath_12E1_E3_T3`, `OutputPath_GSM_16E1_16T1`, `OutputPath_GPS`, `OutputPath_OBSAI`,  
`OutputPath_24T1`, `OutputPath_MAX` }  
*Enumerated type listing possible output port sources (from DPLL(s)) This enumerated type is used in conjunction with DPLL instance to select output DPLL frequency to output dividers. The following table outlines.*
- enum `T_outputInterface` {  
`OUTPUTIF_AMI`, `OUTPUTIF_CMOS`, `OUTPUTIF_LVDS`, `OUTPUTIF_PECL`,  
`OUTPUTIF_MAX` }  
*Enumerated type listing type of supported output port interfaces.*
- enum `T_frameSync` { `frameSync_FRSYNC`, `frameSync_MFRSYNC`, `frameSync_MAX` }  
*Enumerated type listing supported frame syncs.*

### Functions

- void `IDTOutput_SetOutputConfig` (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN, T\_idtDpllInstance nDpll, T\_outputPathType nPath, T\_osUInt8 nFactor, T\_idtApllConfigPerOutput \*aplConfig)  
*Set the configuration of Output port.*
- void `IDTOutput_GetOutputConfig` (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN, T\_idtDpllInstance \*nDpll\_p, T\_outputPathType \*nPath\_p, T\_osUInt8 \*nFactor\_p, T\_idtApllConfigPerOutput \*aplConfig)  
*Get the configuration of Output port.*
- void `IDTOutput_SetOutputInvert` (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN, T\_osUInt8 invert)  
*Set the specified output port to generate a invert signal.*
- T\_osUInt8 `IDTOutput_GetOutputInvert` (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN)  
*Get output signal inversion status.*
- void `IDTOutput_SetOutputEnable` (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN, T\_osUInt8 nEnable)  
*Enable/Disable output port. Consult data sheet for supported ports.*
- T\_osUInt8 `IDTOutput_GetOutputEnable` (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN)  
*Get enable/disable status of output port. Consult data sheet for supported ports.*
- void `IDTOutput_SetOutputInterface` (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN, T\_outputInterface outIf)  
*Set output port interface type. Consult data sheet for supported interfaces per port.*
- T\_outputInterface `IDTOutput_GetOutputInterface` (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN)  
*Get output port interface type. Consult data sheet for supported interfaces per port.*
- void `IDTOutput_SetFrameSync` (T\_idtDrvHdlr hdlr, T\_frameSync frameSync, T\_osUInt8 enable, T\_osUInt8 invert, T\_osUInt8 pulse)  
*Function to control output frame syncs.*
- void `IDTOutput_GetFrameSync` (T\_idtDrvHdlr hdlr, T\_frameSync frameSync, T\_osUInt8 \*enable\_p, T\_osUInt8 \*invert\_p, T\_osUInt8 \*pulse\_p)



- Function to retrieve output frame sync configuration.*

  - void `IDTOutput_SetFrameSyncPulseEdge` (T\_idtDrvHdlr hdlr, T\_osUInt8 isRisingEdge)

*Function provision trigger for frame sync pulses.*
- T\_osUInt8 `IDTOutput_GetFrameSyncPulseEdge` (T\_idtDrvHdlr hdlr)

*Function retrieve trigger for frame sync pulses.*
- void `IDTOutput_DisableApIInput` (T\_idtDrvHdlr hdlr, T\_idtOutputApIConfig outputApIConfig)

*Function disables APLL input.*
- void `IDTOutput_DisableAllIntOutput` (T\_idtDrvHdlr hdlr)

*Function disables all internal outputs.*

### 4.6.1 Detailed Description

Functions in this group are related to output port provisioning.

### 4.6.2 Macro Definition Documentation

#### 4.6.2.1 #define IDT\_EXT\_OUTPORT\_POPULATED( hdlr, ext ) (hdlr->deviceConfig\_m->outputExt2IntXlate\_ma[(ext)])

Utility macro to check if output port is populated.

#### Parameters

<i>hdlr</i>	Device driver handle
<i>ext</i>	External output port number

#### Returns

a positive number - populated, 0 - not populated

Definition at line 79 of file Output.h.

#### 4.6.2.2 #define IDT\_TRANSLATE\_EXT\_TO\_INT\_OUTPORT( hdlr, ext, internal )

#### Value:

```
do {
    OS_ASSERT((ext)<=IDT_DRV_MAX_OUTPUT);
    OS_ASSERT((ext)>0);
    OS_ASSERTS(hdlr->deviceConfig_m->outputExt2IntXlate_ma[(ext)], \
        ("Unsupported output port %d\n", (ext)));
    internal = hdlr->deviceConfig_m->outputExt2IntXlate_ma[(ext)];
} while(0)
```

Utility macro to check if output port is supported and to translated from external port to internal port.

#### Parameters

<i>hdlr</i>	Device driver handle
<i>ext</i>	External output port number
<i>internal</i>	Internal output number

Definition at line 64 of file Output.h.

### 4.6.3 Enumeration Type Documentation

#### 4.6.3.1 enum T\_frameSync

Enumerated type listing supported frame syncs.

Enumerator

**frameSync\_FRSYNC** FR Sync (8 kHz / 1 PPS)  
**frameSync\_MFRSYNC** MFR Sync (2kHz / 1 PPS)  
**frameSync\_MAX**

Definition at line 121 of file Output.h.

#### 4.6.3.2 enum T\_outputInterface

Enumerated type listing type of supported output port interfaces.

Enumerator

**OUTPUTIF\_AMI** AMI  
**OUTPUTIF\_CMOS** CMOS  
**OUTPUTIF\_LVDS** LVDS  
**OUTPUTIF\_PECL** PECL  
**OUTPUTIF\_MAX**

Definition at line 110 of file Output.h.

#### 4.6.3.3 enum T\_outputPathType

Enumerated type listing possible output port sources (from DPLL(s)) This enumerated type is used in conjunction with DPLL instance to select output DPLL frequency to output dividers. The following table outlines.

Enumerator

**OutputPath\_SonetGigEth** From corresponding Sonet/GigE path  
**OutputPath\_7776kHz** From SONET/SDH path 77.76MHz  
**OutputPath\_Eth** From Ethernet path 25MHz  
**OutputPath\_16E1\_16T1** From 16E1/16T1 path 32.768MHz/24.704MHz  
**OutputPath\_12E1\_E3\_T3** From 12E1/E3/T3 path 24.576MHz/34.368MHz/44.736MHz  
**OutputPath\_GSM\_16E1\_16T1** From GSM/16E1/16T1 path 26MHz/32.768MHz/16.384MHz  
**OutputPath\_GPS** From GPS path 40MHz  
**OutputPath\_OBSAI** From OBSAI path 30.72MHz  
**OutputPath\_24T1** From 24T1 path 37.056MHz  
**OutputPath\_MAX**

Definition at line 89 of file Output.h.

### 4.6.4 Function Documentation

#### 4.6.4.1 void IDTOutput\_DisableAllIntOutput ( T\_idtDrvHdr hdlr )

Function disables all internal outputs.

Should ONLY be called from device init function to disable internal outputs for better jitter performance

## Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 1030 of file Output.c.

#### 4.6.4.2 void IDTOutput\_DisableApIInput ( T\_idtDrvHdlr *hdlr*, T\_idtOutputApIConfig *outputApIConfig* )

Function disables APLL input.

Only valid for output path has APLL configured

## Parameters

<i>hdlr</i>	Device driver handler
<i>outputApIConfig</i>	APLL output path configuration

Definition at line 1004 of file Output.c.

#### 4.6.4.3 void IDTOutput\_GetFrameSync ( T\_idtDrvHdlr *hdlr*, T\_frameSync *frameSync*, T\_osUInt8 \* *enable\_p*, T\_osUInt8 \* *invert\_p*, T\_osUInt8 \* *pulse\_p* )

Function to retrieve output frame sync configuration.

## Parameters

<i>hdlr</i>	Device driver handler
<i>frameSync</i>	Select between FR and MFR frame syncs
<i>enable_p</i>	Enable frame sync
<i>invert_p</i>	Invert output frame sync (0-noninverted, 1-invert)
<i>pulse_p</i>	Select between clock (50:50 clock cycle) or pulse (dictated by IN3) (0-clock, 1-pulse)

Definition at line 919 of file Output.c.

#### 4.6.4.4 T\_osUInt8 IDTOutput\_GetFrameSyncPulseEdge ( T\_idtDrvHdlr *hdlr* )

Function retrieve trigger for frame sync pulses.

Only valid for frame syncs when provisioned for pulse.

## Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

## Returns

Frame sync pulse triggered by rising edge (0-falling edge, 1-rising edge)

Definition at line 986 of file Output.c.

#### 4.6.4.5 T\_outputInterface IDTOutput\_GetOutputInterface ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nOutN* )

Get output port interface type. Consult data sheet for supported interfaces per port.

## Parameters

<i>hdlr</i>	Device driver handler
<i>nOutN</i>	Output port number

**Returns**

Interface type.

Definition at line 793 of file Output.c.

4.6.4.6 void IDTOutput\_GetOutputConfig ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nOutN*, T\_idtDpllInstance \* *nDpll\_p*, T\_outputPathType \* *nPath\_p*, T\_osUInt8 \* *nFactor\_p*, T\_idtApplConfigPerOutput \* *applConfig* )

Get the configuration of Output port.

**Parameters**

<i>hdlr</i>	Device driver handler
<i>nOutN</i>	Output port that want to be used
<i>nDpll_p</i>	DPLL instance
<i>nPath_p</i>	Select a specified path as input of output divider
<i>nFactor_p</i>	Dividen factor of a certain output divider. Look up the table in datasheet
<i>applConfig</i>	APLL configuration. Set to NULL if the output port does not go through APLL.

Definition at line 405 of file Output.c.

4.6.4.7 T\_osUInt8 IDTOutput\_GetOutputEnable ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nOutN* )

Get enable/disable status of output port. Consult data sheet for supported ports.

**Parameters**

<i>hdlr</i>	Device driver handler
<i>nOutN</i>	Output port that want to be used

**Returns**

nEnable

- 0=Disable port
- 1=Enable port

Definition at line 653 of file Output.c.

4.6.4.8 T\_osUInt8 IDTOutput\_GetOutputInvert ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nOutN* )

Get output signal inversion status.

**Parameters**

<i>hdlr</i>	Device driver handler
<i>nOutN</i>	Output port that want to be used

**Returns**

0-do no invert, 1-invert output signal

Definition at line 555 of file Output.c.

4.6.4.9 void IDTOutput\_SetFrameSync ( T\_idtDrvHdlr *hdlr*, T\_frameSync *frameSync*, T\_osUInt8 *enable*, T\_osUInt8 *invert*, T\_osUInt8 *pulse* )

Function to control output frame syncs.

Parameters

<i>hdlr</i>	Device driver handler
<i>frameSync</i>	Select between FR and MFR frame syncs
<i>enable</i>	Enable frame sync
<i>invert</i>	Invert output frame sync (0-noninverted, 1-invert)
<i>pulse</i>	Select between clock (50:50 clock cycle) or pulse (dictated by IN3) (0-clock, 1-pulse)

Definition at line 860 of file Output.c.

4.6.4.10 void IDTOutput\_SetFrameSyncPulseEdge ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *isRisingEdge* )

Function provision trigger for frame sync pulses.

Only valid for frame syncs when provisioned for pulse.

Parameters

<i>hdlr</i>	Device driver handler
<i>isRisingEdge</i>	Frame sync pulse triggered by rising edge.

Definition at line 962 of file Output.c.

4.6.4.11 void IDTOutput\_SetOutputInterface ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nOutN*, T\_outputInterface *outIf* )

Set output port interface type. Consult data sheet for supported interfaces per port.

Parameters

<i>hdlr</i>	Device driver handler
<i>nOutN</i>	Output port number
<i>outIf</i>	Interface type.

Definition at line 706 of file Output.c.

4.6.4.12 void IDTOutput\_SetOutputConfig ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nOutN*, T\_idtDpllInstance *nDpll*, T\_outputPathType *nPath*, T\_osUInt8 *nFactor*, T\_idtApllConfigPerOutput \* *apllConfig* )

Set the configuration of Output port.

Parameters

<i>hdlr</i>	Device driver handler
<i>nOutN</i>	Output port that want to be used
<i>nDpll</i>	DPLL instance
<i>nPath</i>	Select a specified path as input of output divider
<i>nFactor</i>	Dividen factor of a certain output divider. Look up the table in datasheet
<i>apllConfig</i>	APLL configuration

Definition at line 182 of file Output.c.

4.6.4.13 void IDTOutput.SetOutputEnable ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nOutN*, T\_osUInt8 *nEnable* )

Enable/Disable output port. Consult data sheet for supported ports.

Parameters

<i>hdlr</i>	Device driver handler
<i>nOutN</i>	Output port that want to be used
<i>nEnable</i>	<ul style="list-style-type: none"> <li>• 0=Disable port</li> <li>• 1=Enable port</li> </ul>

Definition at line 596 of file Output.c.

4.6.4.14 void IDTOutput.SetOutputInvert ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nOutN*, T\_osUInt8 *invert* )

Set the specified output port to generate a invert signal.

Parameters

<i>hdlr</i>	Device driver handler
<i>nOutN</i>	Output port that want to be used
<i>invert</i>	0-do no invert, 1-invert output signal

Definition at line 506 of file Output.c.

## 4.7 Register definitions

### Enumerations

- enum {
  - REG\_ID\_LOW = 0x00, REG\_ID\_HIGH = 0x01, REG\_MPU\_PIN\_STS = 0x02, REG\_NOMINAL\_FREQ\_LO-  
W\_CNFG = 0x04,
  - REG\_NOMINAL\_FREQ\_MID\_CNFG = 0x05, REG\_NOMINAL\_FREQ\_HIGH\_CNFG = 0x06, REG\_T4\_T0\_  
SEL\_CNFG = 0x07, REG\_PHASE\_ALARM\_TIME\_OUT\_CNFG = 0x08,
  - REG\_INPUT\_MODE\_CNFG = 0x09, REG\_DIFFERENTIAL\_IN\_OUT\_CNFG = 0x0A, REG\_MON\_SW\_HS-  
\_CNFG = 0x0B, REG\_INTERRUPT\_CNFG = 0x0C,
  - REG\_INTERRUPTS1\_STS = 0x0D, REG\_INTERRUPTS2\_STS = 0x0E, REG\_INTERRUPTS3\_STS = 0x0F,  
REG\_INTERRUPTS1\_MASK\_CNFG = 0x10,
  - REG\_INTERRUPTS2\_MASK\_CNFG = 0x11, REG\_INTERRUPTS3\_MASK\_CNFG = 0x12, REG\_MS\_SL\_  
CTRL\_CNFG = 0x13, REG\_IN1\_CNFG = 0x14,
  - REG\_IN2\_CNFG = 0x15, REG\_IN3\_CNFG = 0x16, REG\_IN4\_CNFG = 0x17, REG\_IN5\_IN6\_HF\_DIV\_CN-  
FG = 0x18,
  - REG\_IN5\_CNFG = 0x19, REG\_IN6\_CNFG = 0x1A, REG\_IN7\_CNFG = 0x1B, REG\_IN8\_CNFG = 0x1C,  
REG\_IN9\_CNFG = 0x1D, REG\_IN10\_CNFG = 0x1E, REG\_IN11\_CNFG = 0x1F, REG\_IN12\_CNFG = 0x20,  
REG\_IN13\_CNFG = 0x21, REG\_IN14\_CNFG = 0x22, REG\_PRE\_DIV\_CH\_CNFG = 0x23, REG\_PRE\_DIV-  
N\_LOW\_CNFG = 0x24,
  - REG\_PRE\_DIVN\_HIGH\_CNFG = 0x25, REG\_IN1\_IN2\_SEL\_PRIORITY\_CNFG = 0x26, REG\_IN3\_IN4\_S-  
EL\_PRIORITY\_CNFG = 0x27, REG\_IN5\_IN6\_SEL\_PRIORITY\_CNFG = 0x28,
  - REG\_IN7\_IN8\_SEL\_PRIORITY\_CNFG = 0x29, REG\_IN9\_IN10\_SEL\_PRIORITY\_CNFG = 0x2A, REG\_I-  
N11\_IN12\_SEL\_PRIORITY\_CNFG = 0x2B, REG\_IN13\_IN14\_SEL\_PRIORITY\_CNFG = 0x2C,
  - REG\_PAGE\_POINTER\_CNFG = 0x2D, REG\_FREQ\_MON\_FACTOR\_CNFG = 0x2E, REG\_HARD\_FREQ-  
\_MON\_THRESHOLD\_CNFG = 0x2F, REG\_SOFT\_FREQ\_MON\_THRESHOLD\_CNFG = 0x30,
  - REG\_UPPER\_THRESHOLD\_0\_CNFG = 0x31, REG\_LOWER\_THRESHOLD\_0\_CNFG = 0x32, REG\_BU-  
CKET\_SIZE\_0\_CNFG = 0x33, REG\_DECAY\_RATE\_0\_CNFG = 0x34,
  - REG\_UPPER\_THRESHOLD\_1\_CNFG = 0x35, REG\_LOWER\_THRESHOLD\_1\_CNFG = 0x36, REG\_BU-  
CKET\_SIZE\_1\_CNFG = 0x37, REG\_DECAY\_RATE\_1\_CNFG = 0x38,
  - REG\_UPPER\_THRESHOLD\_2\_CNFG = 0x39, REG\_LOWER\_THRESHOLD\_2\_CNFG = 0x3A, REG\_BU-  
CKET\_SIZE\_2\_CNFG = 0x3B, REG\_DECAY\_RATE\_2\_CNFG = 0x3C,
  - REG\_UPPER\_THRESHOLD\_3\_CNFG = 0x3D, REG\_LOWER\_THRESHOLD\_3\_CNFG = 0x3E, REG\_BU-  
CKET\_SIZE\_3\_CNFG = 0x3F, REG\_DECAY\_RATE\_3\_CNFG = 0x40,
  - REG\_IN\_FREQ\_READ\_CH\_CNFG = 0x41, REG\_IN\_FREQ\_READ\_STS = 0x42, REG\_IN1\_IN2\_STS =  
0x43, REG\_IN3\_IN4\_STS = 0x44,
  - REG\_IN5\_IN6\_STS = 0x45, REG\_IN7\_IN8\_STS = 0x46, REG\_IN9\_IN10\_STS = 0x47, REG\_IN11\_IN12\_S-  
TS = 0x48,
  - REG\_IN13\_IN14\_STS = 0x49, REG\_INPUT\_VALID1\_STS = 0x4A, REG\_INPUT\_VALID2\_STS = 0x4B,  
REG\_REMOTE\_INPUT\_VALID1\_CNFG = 0x4C,
  - REG\_REMOTE\_INPUT\_VALID2\_CNFG = 0x4D, REG\_PRIORITY\_TABLE1\_STS = 0x4E, REG\_PRIORITY-  
\_TABLE2\_STS = 0x4F, REG\_T0\_INPUT\_SEL\_CNFG = 0x50,
  - REG\_T4\_INPUT\_SEL\_CNFG = 0x51, REG\_OPERATING\_STS = 0x52, REG\_T0\_OPERATION\_MODE\_C-  
NFG = 0x53, REG\_T4\_OPERATION\_MODE\_CNFG = 0x54,
  - REG\_T0\_DPLL\_APLL\_PATH\_CNFG = 0x55, REG\_T0\_DPLL\_START\_BW\_DAMPING\_CNFG = 0x56, R-  
EG\_T0\_DPLL\_ACQ\_BW\_DAMPING\_CNFG = 0x57, REG\_T0\_DPLL\_LOCKED\_BW\_DAMPING\_CNFG =  
0x58,
  - REG\_T0\_BW\_OVERSHOOT\_CNFG = 0x59, REG\_PHASE\_LOSS\_COARSE\_LIMIT\_CNFG = 0x5A, REG-  
\_PHASE\_LOSS\_FINE\_LIMIT\_CNFG = 0x5B, REG\_T0\_HOLDOVER\_MODE\_CNFG = 0x5C,
  - REG\_HOLDOVER\_FREQ\_LOW\_CNFG = 0x5D, REG\_HOLDOVER\_FREQ\_MID\_CNFG = 0x5E, REG\_HO-  
LDOVER\_FREQ\_HIGH\_CNFG = 0x5F, REG\_T4\_DPLL\_APLL\_PATH\_CNFG = 0x60,
  - REG\_T4\_DPLL\_LOCKED\_BW\_DAMPING\_CNFG = 0x61, REG\_CURRENT\_FREQ\_LOW\_STS = 0x62,  
REG\_CURRENT\_FREQ\_MID\_STS = 0x63, REG\_CURRENT\_FREQ\_HIGH\_STS = 0x64,
  - REG\_DPLL\_FREQ\_SOFT\_LIMIT\_CNFG = 0x65, REG\_DPLL\_FREQ\_HARD\_LIMIT\_LOW\_CNFG = 0x66,  
REG\_DPLL\_FREQ\_HARD\_LIMIT\_MID\_CNFG = 0x67, REG\_CURRENT\_DPLL\_PHASE\_LOW\_STS =  
0x68,
  - REG\_CURRENT\_DPLL\_PHASE\_HIGH\_STS = 0x69, REG\_OUT1\_FREQ\_CNFG = 0x6B, REG\_OUT2\_FR-

EQ\_CNFG = 0x6C, REG\_OUT3\_FREQ\_CNFG = 0x6D,  
 REG\_OUT4\_FREQ\_CNFG = 0x6E, REG\_OUT5\_FREQ\_CNFG = 0x6F, REG\_OUT6\_FREQ\_CNFG = 0x70,  
 REG\_OUT7\_FREQ\_CNFG = 0x71,  
 REG\_OUT8\_FREQ\_CNFG = 0x72, REG\_OUT9\_FREQ\_CNFG = 0x73, REG\_FR\_MFR\_SYNC\_CNFG =  
 0x74, REG\_PHASE\_MON\_CNFG = 0x78,  
 REG\_PHASE\_OFFSET\_LOW\_CNFG = 0x7A, REG\_PHASE\_OFFSET\_HIGH\_CNFG = 0x7B, REG\_SYNC\_  
 \_MONITOR\_CNFG = 0x7C, REG\_SYNC\_PHASE\_CNFG = 0x7D,  
 REG\_PROTECTION\_CNFG = 0x7E, REG\_MPU\_SEL\_CNFG = 0x7F, REG\_DFS\_OFF\_CNFG = 0x30, RE-  
 G\_T0\_PPS\_CNFG = 0x31,  
 REG\_PH\_SLOPE\_CNFG = 0x32, REG\_T0\_ICP\_CTRL\_CNFG = 0x33, REG\_T4\_ICP\_CTRL\_CNFG = 0x34,  
 REG\_T4\_PPS\_CNFG = 0x3E,  
 BF\_ID\_A\_SIZE = 8, BF\_ID\_A\_MASK = 0xFF, BF\_ID\_A\_LSB = 0, BF\_ID\_B\_SIZE = 8,  
 BF\_ID\_B\_MASK = 0xFF, BF\_ID\_B\_LSB = 0, BF\_MPU\_PIN\_STS\_SIZE = 1, BF\_MPU\_PIN\_STS\_MASK =  
 0x01,  
 BF\_MPU\_PIN\_STS\_LSB = 0, BF\_NOMINAL\_FREQ\_VALUE\_A\_SIZE = 8, BF\_NOMINAL\_FREQ\_VALUE\_  
 \_A\_MASK = 0xFF, BF\_NOMINAL\_FREQ\_VALUE\_A\_LSB = 0,  
 BF\_NOMINAL\_FREQ\_VALUE\_B\_SIZE = 8, BF\_NOMINAL\_FREQ\_VALUE\_B\_MASK = 0xFF, BF\_NOMIN-  
 AL\_FREQ\_VALUE\_B\_LSB = 0, BF\_NOMINAL\_FREQ\_VALUE\_C\_SIZE = 8,  
 BF\_NOMINAL\_FREQ\_VALUE\_C\_MASK = 0xFF, BF\_NOMINAL\_FREQ\_VALUE\_C\_LSB = 0, BF\_T4\_T0\_S-  
 SEL\_SIZE = 1, BF\_T4\_T0\_SEL\_MASK = 0x10,  
 BF\_T4\_T0\_SEL\_LSB = 4, BF\_MULTI\_FACTOR\_SIZE = 2, BF\_MULTI\_FACTOR\_MASK = 0xC0, BF\_MUL-  
 TI\_FACTOR\_LSB = 6,  
 BF\_TIMEOUT\_VALUE\_SIZE = 6, BF\_TIMEOUT\_VALUE\_MASK = 0x3F, BF\_TIMEOUT\_VALUE\_LSB = 0,  
 BF\_AUTO\_EXT\_SYNC\_EN\_SIZE = 1,  
 BF\_AUTO\_EXT\_SYNC\_EN\_MASK = 0x80, BF\_AUTO\_EXT\_SYNC\_EN\_LSB = 7, BF\_EXT\_SYNC\_EN\_SI-  
 ZE = 1, BF\_EXT\_SYNC\_EN\_MASK = 0x40,  
 BF\_EXT\_SYNC\_EN\_LSB = 6, BF\_PH\_ALARM\_TIMEOUT\_SIZE = 1, BF\_PH\_ALARM\_TIMEOUT\_MASK =  
 0x20, BF\_PH\_ALARM\_TIMEOUT\_LSB = 5,  
 BF\_SYNC\_FREQ\_SIZE = 2, BF\_SYNC\_FREQ\_MASK = 0x18, BF\_SYNC\_FREQ\_LSB = 3, BF\_IN\_SONE-  
 T\_SDH\_SIZE = 1,  
 BF\_IN\_SONET\_SDH\_MASK = 0x04, BF\_IN\_SONET\_SDH\_LSB = 2, BF\_MASTER\_SLAVE\_SIZE = 1, BF\_  
 \_MASTER\_SLAVE\_MASK = 0x02,  
 BF\_MASTER\_SLAVE\_LSB = 1, BF\_REVERTIVE\_MODE\_SIZE = 1, BF\_REVERTIVE\_MODE\_MASK =  
 0x01, BF\_REVERTIVE\_MODE\_LSB = 0,  
 BF\_OSC\_EDGE\_SIZE = 1, BF\_OSC\_EDGE\_MASK = 0x04, BF\_OSC\_EDGE\_LSB = 2, BF\_OUT7\_PECL\_  
 LVDS\_SIZE = 1,  
 BF\_OUT7\_PECL\_LVDS\_MASK = 0x02, BF\_OUT7\_PECL\_LVDS\_LSB = 1, BF\_OUT6\_PECL\_LVDS\_SIZE  
 = 1, BF\_OUT6\_PECL\_LVDS\_MASK = 0x01,  
 BF\_OUT6\_PECL\_LVDS\_LSB = 0, BF\_FREQ\_MON\_CLK\_SIZE = 1, BF\_FREQ\_MON\_CLK\_MASK = 0x80,  
 BF\_FREQ\_MON\_CLK\_LSB = 7,  
 BF\_LOS\_FLAG\_TO\_TDO\_SIZE = 1, BF\_LOS\_FLAG\_TO\_TDO\_MASK = 0x40, BF\_LOS\_FLAG\_TO\_TDO\_  
 \_LSB = 6, BF\_ULTR\_FAST\_SW\_SIZE = 1,  
 BF\_ULTR\_FAST\_SW\_MASK = 0x20, BF\_ULTR\_FAST\_SW\_LSB = 5, BF\_EXT\_SW\_SIZE = 1, BF\_EXT\_S-  
 W\_MASK = 0x10,  
 BF\_EXT\_SW\_LSB = 4, BF\_HS\_FREZ\_SIZE = 1, BF\_HS\_FREZ\_MASK = 0x08, BF\_HS\_FREZ\_LSB = 3,  
 BF\_HS\_EN\_SIZE = 1, BF\_HS\_EN\_MASK = 0x04, BF\_HS\_EN\_LSB = 2, BF\_FREQ\_MON\_HARD\_EN\_SIZE  
 = 1,  
 BF\_FREQ\_MON\_HARD\_EN\_MASK = 0x01, BF\_FREQ\_MON\_HARD\_EN\_LSB = 0, BF\_HZ\_EN\_SIZE = 1,  
 BF\_HZ\_EN\_MASK = 0x02,  
 BF\_HZ\_EN\_LSB = 1, BF\_INT\_POL\_SIZE = 1, BF\_INT\_POL\_MASK = 0x01, BF\_INT\_POL\_LSB = 0,  
 BF\_IN8\_SIZE = 1, BF\_IN8\_MASK = 0x80, BF\_IN8\_LSB = 7, BF\_IN7\_SIZE = 1,  
 BF\_IN7\_MASK = 0x40, BF\_IN7\_LSB = 6, BF\_IN6\_SIZE = 1, BF\_IN6\_MASK = 0x20,  
 BF\_IN6\_LSB = 5, BF\_IN5\_SIZE = 1, BF\_IN5\_MASK = 0x10, BF\_IN5\_LSB = 4,  
 BF\_IN4\_SIZE = 1, BF\_IN4\_MASK = 0x08, BF\_IN4\_LSB = 3, BF\_IN3\_SIZE = 1,  
 BF\_IN3\_MASK = 0x04, BF\_IN3\_LSB = 2, BF\_IN2\_SIZE = 1, BF\_IN2\_MASK = 0x02,  
 BF\_IN2\_LSB = 1, BF\_IN1\_SIZE = 1, BF\_IN1\_MASK = 0x01, BF\_IN1\_LSB = 0,  
 BF\_T0\_OPERATING\_MODE\_STS\_SIZE = 1, BF\_T0\_OPERATING\_MODE\_STS\_MASK = 0x80, BF\_T0\_



OPERATING\_MODE\_STS\_LSB = 7, BF\_TO\_MAIN\_REF\_FAIL\_SIZE = 1,  
 BF\_TO\_MAIN\_REF\_FAIL\_MASK = 0x40, BF\_TO\_MAIN\_REF\_FAIL\_LSB = 6, BF\_IN14\_SIZE = 1, BF\_IN14\_MASK = 0x20,  
 BF\_IN14\_LSB = 5, BF\_IN13\_SIZE = 1, BF\_IN13\_MASK = 0x10, BF\_IN13\_LSB = 4,  
 BF\_IN12\_SIZE = 1, BF\_IN12\_MASK = 0x08, BF\_IN12\_LSB = 3, BF\_IN11\_SIZE = 1,  
 BF\_IN11\_MASK = 0x04, BF\_IN11\_LSB = 2, BF\_IN10\_SIZE = 1, BF\_IN10\_MASK = 0x02,  
 BF\_IN10\_LSB = 1, BF\_IN9\_SIZE = 1, BF\_IN9\_MASK = 0x01, BF\_IN9\_LSB = 0,  
 BF\_EX\_SYNC\_ALARM\_SIZE = 1, BF\_EX\_SYNC\_ALARM\_MASK = 0x80, BF\_EX\_SYNC\_ALARM\_LSB = 7, BF\_T4\_STS\_SIZE = 1,  
 BF\_T4\_STS\_MASK = 0x40, BF\_T4\_STS\_LSB = 6, BF\_INPUT\_TO\_T4\_SIZE = 1, BF\_INPUT\_TO\_T4\_MASK = 0x10,  
 BF\_INPUT\_TO\_T4\_LSB = 4, BF\_AMI2\_VIOL\_SIZE = 1, BF\_AMI2\_VIOL\_MASK = 0x08, BF\_AMI2\_VIOL\_LSB = 3,  
 BF\_AMI2\_LOS\_SIZE = 1, BF\_AMI2\_LOS\_MASK = 0x04, BF\_AMI2\_LOS\_LSB = 2, BF\_AMI1\_VIOL\_SIZE = 1,  
 BF\_AMI1\_VIOL\_MASK = 0x02, BF\_AMI1\_VIOL\_LSB = 1, BF\_AMI1\_LOS\_SIZE = 1, BF\_AMI1\_LOS\_MASK = 0x01,  
 BF\_AMI1\_LOS\_LSB = 0, BF\_PPS\_FAST\_FREQ\_LOCK\_EN\_SIZE = 1, BF\_PPS\_FAST\_FREQ\_LOCK\_EN\_MASK = 0x10, BF\_PPS\_FAST\_FREQ\_LOCK\_EN\_LSB = 4,  
 BF\_PPS\_FAST\_PH\_LOCK\_EN\_SIZE = 1, BF\_PPS\_FAST\_PH\_LOCK\_EN\_MASK = 0x08, BF\_PPS\_FAST\_PH\_LOCK\_EN\_LSB = 3, BF\_MS\_SL\_CTRL\_SIZE = 1,  
 BF\_MS\_SL\_CTRL\_MASK = 0x01, BF\_MS\_SL\_CTRL\_LSB = 0, BF\_400HZ\_SEL\_SIZE = 1, BF\_400HZ\_SEL\_MASK = 0x40,  
 BF\_400HZ\_SEL\_LSB = 6, BF\_BUCKET\_SEL\_SIZE = 2, BF\_BUCKET\_SEL\_MASK = 0x30, BF\_BUCKET\_SEL\_LSB = 4,  
 BF\_IN\_FREQ\_SIZE = 4, BF\_IN\_FREQ\_MASK = 0x0F, BF\_IN\_FREQ\_LSB = 0, BF\_DIRECT\_DIV\_SIZE = 1, BF\_DIRECT\_DIV\_MASK = 0x80, BF\_DIRECT\_DIV\_LSB = 7, BF\_LOCK\_8K\_SIZE = 1, BF\_LOCK\_8K\_MASK = 0x40,  
 BF\_LOCK\_8K\_LSB = 6, BF\_IN6\_DIV\_SIZE = 2, BF\_IN6\_DIV\_MASK = 0xC0, BF\_IN6\_DIV\_LSB = 6, BF\_IN5\_DIV\_SIZE = 2, BF\_IN5\_DIV\_MASK = 0x03, BF\_IN5\_DIV\_LSB = 0, BF\_PRE\_DIV\_CH\_VALUE\_SIZE = 4,  
 BF\_PRE\_DIV\_CH\_VALUE\_MASK = 0x0F, BF\_PRE\_DIV\_CH\_VALUE\_LSB = 0, BF\_PRE\_DIVN\_VALUE\_A\_SIZE = 8, BF\_PRE\_DIVN\_VALUE\_A\_MASK = 0xFF,  
 BF\_PRE\_DIVN\_VALUE\_A\_LSB = 0, BF\_PRE\_DIVN\_VALUE\_B\_SIZE = 7, BF\_PRE\_DIVN\_VALUE\_B\_MASK = 0x7F, BF\_PRE\_DIVN\_VALUE\_B\_LSB = 0,  
 BF\_IN2\_SEL\_PRIORITY\_SIZE = 4, BF\_IN2\_SEL\_PRIORITY\_MASK = 0xF0, BF\_IN2\_SEL\_PRIORITY\_LSB = 4, BF\_IN1\_SEL\_PRIORITY\_SIZE = 4,  
 BF\_IN1\_SEL\_PRIORITY\_MASK = 0x0F, BF\_IN1\_SEL\_PRIORITY\_LSB = 0, BF\_IN4\_SEL\_PRIORITY\_SIZE = 4, BF\_IN4\_SEL\_PRIORITY\_MASK = 0xF0,  
 BF\_IN4\_SEL\_PRIORITY\_LSB = 4, BF\_IN3\_SEL\_PRIORITY\_SIZE = 4, BF\_IN3\_SEL\_PRIORITY\_MASK = 0x0F, BF\_IN3\_SEL\_PRIORITY\_LSB = 0,  
 BF\_IN6\_SEL\_PRIORITY\_SIZE = 4, BF\_IN6\_SEL\_PRIORITY\_MASK = 0xF0, BF\_IN6\_SEL\_PRIORITY\_LSB = 4, BF\_IN5\_SEL\_PRIORITY\_SIZE = 4,  
 BF\_IN5\_SEL\_PRIORITY\_MASK = 0x0F, BF\_IN5\_SEL\_PRIORITY\_LSB = 0, BF\_IN8\_SEL\_PRIORITY\_SIZE = 4, BF\_IN8\_SEL\_PRIORITY\_MASK = 0xF0,  
 BF\_IN8\_SEL\_PRIORITY\_LSB = 4, BF\_IN7\_SEL\_PRIORITY\_SIZE = 4, BF\_IN7\_SEL\_PRIORITY\_MASK = 0x0F, BF\_IN7\_SEL\_PRIORITY\_LSB = 0,  
 BF\_IN10\_SEL\_PRIORITY\_SIZE = 4, BF\_IN10\_SEL\_PRIORITY\_MASK = 0xF0, BF\_IN10\_SEL\_PRIORITY\_LSB = 4, BF\_IN9\_SEL\_PRIORITY\_SIZE = 4,  
 BF\_IN9\_SEL\_PRIORITY\_MASK = 0x0F, BF\_IN9\_SEL\_PRIORITY\_LSB = 0, BF\_IN12\_SEL\_PRIORITY\_SIZE = 4, BF\_IN12\_SEL\_PRIORITY\_MASK = 0xF0,  
 BF\_IN12\_SEL\_PRIORITY\_LSB = 4, BF\_IN11\_SEL\_PRIORITY\_SIZE = 4, BF\_IN11\_SEL\_PRIORITY\_MASK = 0x0F, BF\_IN11\_SEL\_PRIORITY\_LSB = 0,  
 BF\_IN14\_SEL\_PRIORITY\_SIZE = 4, BF\_IN14\_SEL\_PRIORITY\_MASK = 0xF0, BF\_IN14\_SEL\_PRIORITY\_LSB = 4, BF\_IN13\_SEL\_PRIORITY\_SIZE = 4,  
 BF\_IN13\_SEL\_PRIORITY\_MASK = 0x0F, BF\_IN13\_SEL\_PRIORITY\_LSB = 0, BF\_PAGE\_POINTER\_SIZE = 1, BF\_PAGE\_POINTER\_MASK = 0x01,  
 BF\_PAGE\_POINTER\_LSB = 0, BF\_FREQ\_MON\_FACTOR\_SIZE = 4, BF\_FREQ\_MON\_FACTOR\_MASK =

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0x0F, BF_FREQ_MON_FACTOR_LSB = 0,
BF_HARD_FREQ_MON_THRESHOLD_A_SIZE = 4, BF_HARD_FREQ_MON_THRESHOLD_A_MASK =
0xF0, BF_HARD_FREQ_MON_THRESHOLD_A_LSB = 4, BF_HARD_FREQ_MON_THRESHOLD_B_SIZE
= 4,
BF_HARD_FREQ_MON_THRESHOLD_B_MASK = 0x0F, BF_HARD_FREQ_MON_THRESHOLD_B_LSB
= 0, BF_SOFT_FREQ_MON_THRESHOLD_A_SIZE = 4, BF_SOFT_FREQ_MON_THRESHOLD_A_MASK
= 0xF0,
BF_SOFT_FREQ_MON_THRESHOLD_A_LSB = 4, BF_SOFT_FREQ_MON_THRESHOLD_B_SIZE = 4,
BF_SOFT_FREQ_MON_THRESHOLD_B_MASK = 0x0F, BF_SOFT_FREQ_MON_THRESHOLD_B_LSB =
0,
BF_UPPER_THRESHOLD_DATA_SIZE = 8, BF_UPPER_THRESHOLD_DATA_MASK = 0xFF, BF_UPPE
R_THRESHOLD_DATA_LSB = 0, BF_LOWER_THRESHOLD_DATA_SIZE = 8,
BF_LOWER_THRESHOLD_DATA_MASK = 0xFF, BF_LOWER_THRESHOLD_DATA_LSB = 0, BF_BUCK
ET_SIZE_DATA_SIZE = 8, BF_BUCKET_SIZE_DATA_MASK = 0xFF,
BF_BUCKET_SIZE_DATA_LSB = 0, BF_DECAY_RATE_DATA_SIZE = 2, BF_DECAY_RATE_DATA_MA
SK = 0x03, BF_DECAY_RATE_DATA_LSB = 0,
BF_IN_FREQ_READ_CH_SIZE = 4, BF_IN_FREQ_READ_CH_MASK = 0x0F, BF_IN_FREQ_READ_CH_
LSB = 0, BF_IN_FREQ_VALUE_SIZE = 8,
BF_IN_FREQ_VALUE_MASK = 0xFF, BF_IN_FREQ_VALUE_LSB = 0, BF_IN2_FREQ_SOFT_ALARM_SI
ZE = 1, BF_IN2_FREQ_SOFT_ALARM_MASK = 0x80,
BF_IN2_FREQ_SOFT_ALARM_LSB = 7, BF_IN2_FREQ_HARD_ALARM_SIZE = 1, BF_IN2_FREQ_HAR
D_ALARM_MASK = 0x40, BF_IN2_FREQ_HARD_ALARM_LSB = 6,
BF_IN2_NO_ACTIVITY_ALARM_SIZE = 1, BF_IN2_NO_ACTIVITY_ALARM_MASK = 0x20, BF_IN2_NO_
ACTIVITY_ALARM_LSB = 5, BF_IN2_PH_LOCK_ALARM_SIZE = 1,
BF_IN2_PH_LOCK_ALARM_MASK = 0x10, BF_IN2_PH_LOCK_ALARM_LSB = 4, BF_IN1_FREQ_SOFT_
_ALARM_SIZE = 1, BF_IN1_FREQ_SOFT_ALARM_MASK = 0x08,
BF_IN1_FREQ_SOFT_ALARM_LSB = 3, BF_IN1_FREQ_HARD_ALARM_SIZE = 1, BF_IN1_FREQ_HAR
D_ALARM_MASK = 0x04, BF_IN1_FREQ_HARD_ALARM_LSB = 2,
BF_IN1_NO_ACTIVITY_ALARM_SIZE = 1, BF_IN1_NO_ACTIVITY_ALARM_MASK = 0x02, BF_IN1_NO_
ACTIVITY_ALARM_LSB = 1, BF_IN1_PH_LOCK_ALARM_SIZE = 1,
BF_IN1_PH_LOCK_ALARM_MASK = 0x01, BF_IN1_PH_LOCK_ALARM_LSB = 0, BF_IN4_FREQ_SOFT_
_ALARM_SIZE = 1, BF_IN4_FREQ_SOFT_ALARM_MASK = 0x80,
BF_IN4_FREQ_SOFT_ALARM_LSB = 7, BF_IN4_FREQ_HARD_ALARM_SIZE = 1, BF_IN4_FREQ_HAR
D_ALARM_MASK = 0x40, BF_IN4_FREQ_HARD_ALARM_LSB = 6,
BF_IN4_NO_ACTIVITY_ALARM_SIZE = 1, BF_IN4_NO_ACTIVITY_ALARM_MASK = 0x20, BF_IN4_NO_
ACTIVITY_ALARM_LSB = 5, BF_IN4_PH_LOCK_ALARM_SIZE = 1,
BF_IN4_PH_LOCK_ALARM_MASK = 0x10, BF_IN4_PH_LOCK_ALARM_LSB = 4, BF_IN3_FREQ_SOFT_
_ALARM_SIZE = 1, BF_IN3_FREQ_SOFT_ALARM_MASK = 0x08,
BF_IN3_FREQ_SOFT_ALARM_LSB = 3, BF_IN3_FREQ_HARD_ALARM_SIZE = 1, BF_IN3_FREQ_HAR
D_ALARM_MASK = 0x04, BF_IN3_FREQ_HARD_ALARM_LSB = 2,
BF_IN3_NO_ACTIVITY_ALARM_SIZE = 1, BF_IN3_NO_ACTIVITY_ALARM_MASK = 0x02, BF_IN3_NO_
ACTIVITY_ALARM_LSB = 1, BF_IN3_PH_LOCK_ALARM_SIZE = 1,
BF_IN3_PH_LOCK_ALARM_MASK = 0x01, BF_IN3_PH_LOCK_ALARM_LSB = 0, BF_IN6_FREQ_SOFT_
_ALARM_SIZE = 1, BF_IN6_FREQ_SOFT_ALARM_MASK = 0x80,
BF_IN6_FREQ_SOFT_ALARM_LSB = 7, BF_IN6_FREQ_HARD_ALARM_SIZE = 1, BF_IN6_FREQ_HAR
D_ALARM_MASK = 0x40, BF_IN6_FREQ_HARD_ALARM_LSB = 6,
BF_IN6_NO_ACTIVITY_ALARM_SIZE = 1, BF_IN6_NO_ACTIVITY_ALARM_MASK = 0x20, BF_IN6_NO_
ACTIVITY_ALARM_LSB = 5, BF_IN6_PH_LOCK_ALARM_SIZE = 1,
BF_IN6_PH_LOCK_ALARM_MASK = 0x10, BF_IN6_PH_LOCK_ALARM_LSB = 4, BF_IN5_FREQ_SOFT_
_ALARM_SIZE = 1, BF_IN5_FREQ_SOFT_ALARM_MASK = 0x08,
BF_IN5_FREQ_SOFT_ALARM_LSB = 3, BF_IN5_FREQ_HARD_ALARM_SIZE = 1, BF_IN5_FREQ_HAR
D_ALARM_MASK = 0x04, BF_IN5_FREQ_HARD_ALARM_LSB = 2,
BF_IN5_NO_ACTIVITY_ALARM_SIZE = 1, BF_IN5_NO_ACTIVITY_ALARM_MASK = 0x02, BF_IN5_NO_
ACTIVITY_ALARM_LSB = 1, BF_IN5_PH_LOCK_ALARM_SIZE = 1,
BF_IN5_PH_LOCK_ALARM_MASK = 0x01, BF_IN5_PH_LOCK_ALARM_LSB = 0, BF_IN8_FREQ_SOFT_
_ALARM_SIZE = 1, BF_IN8_FREQ_SOFT_ALARM_MASK = 0x80,
BF_IN8_FREQ_SOFT_ALARM_LSB = 7, BF_IN8_FREQ_HARD_ALARM_SIZE = 1, BF_IN8_FREQ_HAR

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D\_ALARM\_MASK = 0x40, BF\_IN8\_FREQ\_HARD\_ALARM\_LSB = 6,  
 BF\_IN8\_NO\_ACTIVITY\_ALARM\_SIZE = 1, BF\_IN8\_NO\_ACTIVITY\_ALARM\_MASK = 0x20, BF\_IN8\_NO\_ -  
 ACTIVITY\_ALARM\_LSB = 5, BF\_IN8\_PH\_LOCK\_ALARM\_SIZE = 1,  
 BF\_IN8\_PH\_LOCK\_ALARM\_MASK = 0x10, BF\_IN8\_PH\_LOCK\_ALARM\_LSB = 4, BF\_IN7\_FREQ\_SOFT -  
 \_ALARM\_SIZE = 1, BF\_IN7\_FREQ\_SOFT\_ALARM\_MASK = 0x08,  
 BF\_IN7\_FREQ\_SOFT\_ALARM\_LSB = 3, BF\_IN7\_FREQ\_HARD\_ALARM\_SIZE = 1, BF\_IN7\_FREQ\_HAR -  
 D\_ALARM\_MASK = 0x04, BF\_IN7\_FREQ\_HARD\_ALARM\_LSB = 2,  
 BF\_IN7\_NO\_ACTIVITY\_ALARM\_SIZE = 1, BF\_IN7\_NO\_ACTIVITY\_ALARM\_MASK = 0x02, BF\_IN7\_NO\_ -  
 ACTIVITY\_ALARM\_LSB = 1, BF\_IN7\_PH\_LOCK\_ALARM\_SIZE = 1,  
 BF\_IN7\_PH\_LOCK\_ALARM\_MASK = 0x01, BF\_IN7\_PH\_LOCK\_ALARM\_LSB = 0, BF\_IN10\_FREQ\_SOF -  
 T\_ALARM\_SIZE = 1, BF\_IN10\_FREQ\_SOFT\_ALARM\_MASK = 0x80,  
 BF\_IN10\_FREQ\_SOFT\_ALARM\_LSB = 7, BF\_IN10\_FREQ\_HARD\_ALARM\_SIZE = 1, BF\_IN10\_FREQ\_H -  
 ARD\_ALARM\_MASK = 0x40, BF\_IN10\_FREQ\_HARD\_ALARM\_LSB = 6,  
 BF\_IN10\_NO\_ACTIVITY\_ALARM\_SIZE = 1, BF\_IN10\_NO\_ACTIVITY\_ALARM\_MASK = 0x20, BF\_IN10\_ -  
 NO\_ACTIVITY\_ALARM\_LSB = 5, BF\_IN10\_PH\_LOCK\_ALARM\_SIZE = 1,  
 BF\_IN10\_PH\_LOCK\_ALARM\_MASK = 0x10, BF\_IN10\_PH\_LOCK\_ALARM\_LSB = 4, BF\_IN9\_FREQ\_SO -  
 FT\_ALARM\_SIZE = 1, BF\_IN9\_FREQ\_SOFT\_ALARM\_MASK = 0x08,  
 BF\_IN9\_FREQ\_SOFT\_ALARM\_LSB = 3, BF\_IN9\_FREQ\_HARD\_ALARM\_SIZE = 1, BF\_IN9\_FREQ\_HAR -  
 D\_ALARM\_MASK = 0x04, BF\_IN9\_FREQ\_HARD\_ALARM\_LSB = 2,  
 BF\_IN9\_NO\_ACTIVITY\_ALARM\_SIZE = 1, BF\_IN9\_NO\_ACTIVITY\_ALARM\_MASK = 0x02, BF\_IN9\_NO\_ -  
 ACTIVITY\_ALARM\_LSB = 1, BF\_IN9\_PH\_LOCK\_ALARM\_SIZE = 1,  
 BF\_IN9\_PH\_LOCK\_ALARM\_MASK = 0x01, BF\_IN9\_PH\_LOCK\_ALARM\_LSB = 0, BF\_IN12\_FREQ\_SOF -  
 T\_ALARM\_SIZE = 1, BF\_IN12\_FREQ\_SOFT\_ALARM\_MASK = 0x80,  
 BF\_IN12\_FREQ\_SOFT\_ALARM\_LSB = 7, BF\_IN12\_FREQ\_HARD\_ALARM\_SIZE = 1, BF\_IN12\_FREQ\_H -  
 ARD\_ALARM\_MASK = 0x40, BF\_IN12\_FREQ\_HARD\_ALARM\_LSB = 6,  
 BF\_IN12\_NO\_ACTIVITY\_ALARM\_SIZE = 1, BF\_IN12\_NO\_ACTIVITY\_ALARM\_MASK = 0x20, BF\_IN12\_ -  
 NO\_ACTIVITY\_ALARM\_LSB = 5, BF\_IN12\_PH\_LOCK\_ALARM\_SIZE = 1,  
 BF\_IN12\_PH\_LOCK\_ALARM\_MASK = 0x10, BF\_IN12\_PH\_LOCK\_ALARM\_LSB = 4, BF\_IN11\_FREQ\_S -  
 OFT\_ALARM\_SIZE = 1, BF\_IN11\_FREQ\_SOFT\_ALARM\_MASK = 0x08,  
 BF\_IN11\_FREQ\_SOFT\_ALARM\_LSB = 3, BF\_IN11\_FREQ\_HARD\_ALARM\_SIZE = 1, BF\_IN11\_FREQ\_H -  
 ARD\_ALARM\_MASK = 0x04, BF\_IN11\_FREQ\_HARD\_ALARM\_LSB = 2,  
 BF\_IN11\_NO\_ACTIVITY\_ALARM\_SIZE = 1, BF\_IN11\_NO\_ACTIVITY\_ALARM\_MASK = 0x02, BF\_IN11\_ -  
 NO\_ACTIVITY\_ALARM\_LSB = 1, BF\_IN11\_PH\_LOCK\_ALARM\_SIZE = 1,  
 BF\_IN11\_PH\_LOCK\_ALARM\_MASK = 0x01, BF\_IN11\_PH\_LOCK\_ALARM\_LSB = 0, BF\_IN14\_FREQ\_S -  
 OFT\_ALARM\_SIZE = 1, BF\_IN14\_FREQ\_SOFT\_ALARM\_MASK = 0x80,  
 BF\_IN14\_FREQ\_SOFT\_ALARM\_LSB = 7, BF\_IN14\_FREQ\_HARD\_ALARM\_SIZE = 1, BF\_IN14\_FREQ\_H -  
 ARD\_ALARM\_MASK = 0x40, BF\_IN14\_FREQ\_HARD\_ALARM\_LSB = 6,  
 BF\_IN14\_NO\_ACTIVITY\_ALARM\_SIZE = 1, BF\_IN14\_NO\_ACTIVITY\_ALARM\_MASK = 0x20, BF\_IN14\_ -  
 NO\_ACTIVITY\_ALARM\_LSB = 5, BF\_IN14\_PH\_LOCK\_ALARM\_SIZE = 1,  
 BF\_IN14\_PH\_LOCK\_ALARM\_MASK = 0x10, BF\_IN14\_PH\_LOCK\_ALARM\_LSB = 4, BF\_IN13\_FREQ\_S -  
 OFT\_ALARM\_SIZE = 1, BF\_IN13\_FREQ\_SOFT\_ALARM\_MASK = 0x08,  
 BF\_IN13\_FREQ\_SOFT\_ALARM\_LSB = 3, BF\_IN13\_FREQ\_HARD\_ALARM\_SIZE = 1, BF\_IN13\_FREQ\_H -  
 ARD\_ALARM\_MASK = 0x04, BF\_IN13\_FREQ\_HARD\_ALARM\_LSB = 2,  
 BF\_IN13\_NO\_ACTIVITY\_ALARM\_SIZE = 1, BF\_IN13\_NO\_ACTIVITY\_ALARM\_MASK = 0x02, BF\_IN13\_ -  
 NO\_ACTIVITY\_ALARM\_LSB = 1, BF\_IN13\_PH\_LOCK\_ALARM\_SIZE = 1,  
 BF\_IN13\_PH\_LOCK\_ALARM\_MASK = 0x01, BF\_IN13\_PH\_LOCK\_ALARM\_LSB = 0, BF\_HIGHEST\_PRI -  
 ORITY\_VALIDATED\_SIZE = 4, BF\_HIGHEST\_PRIORITY\_VALIDATED\_MASK = 0xF0,  
 BF\_HIGHEST\_PRIORITY\_VALIDATED\_LSB = 4, BF\_CURRENTLY\_SELECTED\_INPUTS\_SIZE = 4, BF\_ -  
 CURRENTLY\_SELECTED\_INPUTS\_MASK = 0x0F, BF\_CURRENTLY\_SELECTED\_INPUTS\_LSB = 0,  
 BF\_THIRD\_HIGHEST\_PRIORITY\_VALIDATED\_SIZE = 4, BF\_THIRD\_HIGHEST\_PRIORITY\_VALIDATE -  
 D\_MASK = 0xF0, BF\_THIRD\_HIGHEST\_PRIORITY\_VALIDATED\_LSB = 4, BF\_SECOND\_HIGHEST\_PRI -  
 ORITY\_VALIDATED\_SIZE = 4,  
 BF\_SECOND\_HIGHEST\_PRIORITY\_VALIDATED\_MASK = 0x0F, BF\_SECOND\_HIGHEST\_PRIORITY\_V -  
 ALIDATED\_LSB = 0, BF\_T0\_INPUT\_SEL\_SIZE = 4, BF\_T0\_INPUT\_SEL\_MASK = 0x0F,  
 BF\_T0\_INPUT\_SEL\_LSB = 0, BF\_T4\_LOCK\_T0\_SIZE = 1, BF\_T4\_LOCK\_T0\_MASK = 0x40, BF\_T4\_LOC -  
 K\_T0\_LSB = 6,  
 BF\_T0\_FOR\_T4\_SIZE = 1, BF\_T0\_FOR\_T4\_MASK = 0x20, BF\_T0\_FOR\_T4\_LSB = 5, BF\_T4\_TEST\_T0\_ -

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PH_SIZE = 1,
BF_T4_TEST_T0_PH_MASK = 0x10, BF_T4_TEST_T0_PH_LSB = 4, BF_T4_INPUT_SEL_SIZE = 4, BF_T4_INPUT_SEL_MASK = 0x0F,
BF_T4_INPUT_SEL_LSB = 0, BF_EX_SYNC_ALARM_MON_SIZE = 1, BF_EX_SYNC_ALARM_MON_MASK = 0x80, BF_EX_SYNC_ALARM_MON_LSB = 7,
BF_T4_DPLL_LOCK_SIZE = 1, BF_T4_DPLL_LOCK_MASK = 0x40, BF_T4_DPLL_LOCK_LSB = 6, BF_T0_DPLL_SOFT_FREQ_ALARM_SIZE = 1,
BF_T0_DPLL_SOFT_FREQ_ALARM_MASK = 0x20, BF_T0_DPLL_SOFT_FREQ_ALARM_LSB = 5, BF_T4_DPLL_SOFT_FREQ_ALARM_SIZE = 1, BF_T4_DPLL_SOFT_FREQ_ALARM_MASK = 0x10,
BF_T4_DPLL_SOFT_FREQ_ALARM_LSB = 4, BF_T0_DPLL_LOCK_SIZE = 1, BF_T0_DPLL_LOCK_MASK = 0x08, BF_T0_DPLL_LOCK_LSB = 3,
BF_T0_DPLL_OPERATING_MODE_SIZE = 3, BF_T0_DPLL_OPERATING_MODE_MASK = 0x07, BF_T0_DPLL_OPERATING_MODE_LSB = 0, BF_T0_WDCO_SIZE = 1,
BF_T0_WDCO_MASK = 0x08, BF_T0_WDCO_LSB = 3, BF_T0_OPERATING_MODE_SIZE = 3, BF_T0_OPERATING_MODE_MASK = 0x07,
BF_T0_OPERATING_MODE_LSB = 0, BF_T4_WDCO_SIZE = 1, BF_T4_WDCO_MASK = 0x08, BF_T4_WDCO_LSB = 3,
BF_T4_OPERATING_MODE_SIZE = 3, BF_T4_OPERATING_MODE_MASK = 0x07, BF_T4_OPERATING_MODE_LSB = 0, BF_T0_APLL_PATH_SIZE = 4,
BF_T0_APLL_PATH_MASK = 0xF0, BF_T0_APLL_PATH_LSB = 4, BF_T0_GSM_OBSAI_16E1_16T1_SEL_SIZE = 2, BF_T0_GSM_OBSAI_16E1_16T1_SEL_MASK = 0x0C,
BF_T0_GSM_OBSAI_16E1_16T1_SEL_LSB = 2, BF_T0_12E1_GPS_E3_T3_SEL_SIZE = 2, BF_T0_12E1_GPS_E3_T3_SEL_MASK = 0x03, BF_T0_12E1_GPS_E3_T3_SEL_LSB = 0,
BF_T0_DPLL_START_DAMPING_SIZE = 3, BF_T0_DPLL_START_DAMPING_MASK = 0xE0, BF_T0_DPLL_START_DAMPING_LSB = 5, BF_T0_DPLL_START_BW_SIZE = 5,
BF_T0_DPLL_START_BW_MASK = 0x1F, BF_T0_DPLL_START_BW_LSB = 0, BF_T0_DPLL_ACQ_DAMPING_SIZE = 3, BF_T0_DPLL_ACQ_DAMPING_MASK = 0xE0,
BF_T0_DPLL_ACQ_DAMPING_LSB = 5, BF_T0_DPLL_ACQ_BW_SIZE = 5, BF_T0_DPLL_ACQ_BW_MASK = 0x1F, BF_T0_DPLL_ACQ_BW_LSB = 0,
BF_T0_DPLL_LOCKED_DAMPING_SIZE = 3, BF_T0_DPLL_LOCKED_DAMPING_MASK = 0xE0, BF_T0_DPLL_LOCKED_DAMPING_LSB = 5, BF_T0_DPLL_LOCKED_BW_SIZE = 5,
BF_T0_DPLL_LOCKED_BW_MASK = 0x1F, BF_T0_DPLL_LOCKED_BW_LSB = 0, BF_AUTO_BW_SEL_SIZE = 1, BF_AUTO_BW_SEL_MASK = 0x80,
BF_AUTO_BW_SEL_LSB = 7, BF_T0_LIMIT_SIZE = 1, BF_T0_LIMIT_MASK = 0x08, BF_T0_LIMIT_LSB = 3,
BF_COARSE_PH_LOS_LIMT_EN_SIZE = 1, BF_COARSE_PH_LOS_LIMT_EN_MASK = 0x80, BF_COARSE_PH_LOS_LIMT_EN_LSB = 7, BF_WIDE_EN_SIZE = 1,
BF_WIDE_EN_MASK = 0x40, BF_WIDE_EN_LSB = 6, BF_MULTI_PH_APP_SIZE = 1, BF_MULTI_PH_APP_MASK = 0x20,
BF_MULTI_PH_APP_LSB = 5, BF_MULTI_PH_8K_4K_2K_EN_SIZE = 1, BF_MULTI_PH_8K_4K_2K_EN_MASK = 0x10, BF_MULTI_PH_8K_4K_2K_EN_LSB = 4,
BF_PH_LOS_COARSE_LIMT_SIZE = 4, BF_PH_LOS_COARSE_LIMT_MASK = 0x0F, BF_PH_LOS_COARSE_LIMT_LSB = 0, BF_FINE_PH_LOS_LIMT_EN_SIZE = 1,
BF_FINE_PH_LOS_LIMT_EN_MASK = 0x80, BF_FINE_PH_LOS_LIMT_EN_LSB = 7, BF_FAST_LOS_SW_SIZE = 1, BF_FAST_LOS_SW_MASK = 0x40,
BF_FAST_LOS_SW_LSB = 6, BF_PH_LOS_FINE_LIMT_SIZE = 3, BF_PH_LOS_FINE_LIMT_MASK = 0x07, BF_PH_LOS_FINE_LIMT_LSB = 0,
BF_MAN_HOLDOVER_SIZE = 1, BF_MAN_HOLDOVER_MASK = 0x80, BF_MAN_HOLDOVER_LSB = 7, BF_AUTO_AVG_SIZE = 1,
BF_AUTO_AVG_MASK = 0x40, BF_AUTO_AVG_LSB = 6, BF_FAST_AVG_SIZE = 1, BF_FAST_AVG_MASK = 0x20,
BF_FAST_AVG_LSB = 5, BF_READ_AVG_SIZE = 1, BF_READ_AVG_MASK = 0x10, BF_READ_AVG_LSB = 4,
BF_TEMP_HOLDOVER_MODE_SIZE = 2, BF_TEMP_HOLDOVER_MODE_MASK = 0x0C, BF_TEMP_HOLDOVER_MODE_LSB = 2, BF_HOLDOVER_FREQ_A_SIZE = 8,
BF_HOLDOVER_FREQ_A_MASK = 0xFF, BF_HOLDOVER_FREQ_A_LSB = 0, BF_HOLDOVER_FREQ_B_SIZE = 8, BF_HOLDOVER_FREQ_B_MASK = 0xFF,
BF_HOLDOVER_FREQ_B_LSB = 0, BF_HOLDOVER_FREQ_C_SIZE = 8, BF_HOLDOVER_FREQ_C_MASK = 0xFF,
BF_HOLDOVER_FREQ_C_LSB = 0,

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ASK = 0xFF, BF_HOLD OVER_FREQ_C_LSB = 0,
BF_T4_APLL_PATH_SIZE = 4, BF_T4_APLL_PATH_MASK = 0xF0, BF_T4_APLL_PATH_LSB = 4, BF_
T4_GSM_OBSAI_16E1_16T1_SEL_SIZE = 2,
BF_T4_GSM_OBSAI_16E1_16T1_SEL_MASK = 0x0C, BF_T4_GSM_OBSAI_16E1_16T1_SEL_LSB = 2,
BF_T4_12E1_GPS_E3_T3_SEL_SIZE = 2, BF_T4_12E1_GPS_E3_T3_SEL_MASK = 0x03,
BF_T4_12E1_GPS_E3_T3_SEL_LSB = 0, BF_T4_DPLL_LOCKED_DAMPING_SIZE = 3, BF_T4_DPLL_L
OCKED_DAMPING_MASK = 0xE0, BF_T4_DPLL_LOCKED_DAMPING_LSB = 5,
BF_T4_DPLL_LOCKED_BW_SIZE = 2, BF_T4_DPLL_LOCKED_BW_MASK = 0x03, BF_T4_DPLL_LOCK
ED_BW_LSB = 0, BF_CURRENT_DPLL_FREQ_A_SIZE = 8,
BF_CURRENT_DPLL_FREQ_A_MASK = 0xFF, BF_CURRENT_DPLL_FREQ_A_LSB = 0, BF_CURRENT_
_DPLL_FREQ_B_SIZE = 8, BF_CURRENT_DPLL_FREQ_B_MASK = 0xFF,
BF_CURRENT_DPLL_FREQ_B_LSB = 0, BF_CURRENT_DPLL_FREQ_C_SIZE = 8, BF_CURRENT_DP
LL_FREQ_C_MASK = 0xFF, BF_CURRENT_DPLL_FREQ_C_LSB = 0,
BF_FREQ_LIMT_PH_LOS_SIZE = 1, BF_FREQ_LIMT_PH_LOS_MASK = 0x80, BF_FREQ_LIMT_PH_LO
S_LSB = 7, BF_DPLL_FREQ_SOFT_LIMT_SIZE = 7,
BF_DPLL_FREQ_SOFT_LIMT_MASK = 0x7F, BF_DPLL_FREQ_SOFT_LIMT_LSB = 0, BF_DPLL_FREQ_
HARD_LIMT_A_SIZE = 8, BF_DPLL_FREQ_HARD_LIMT_A_MASK = 0xFF,
BF_DPLL_FREQ_HARD_LIMT_A_LSB = 0, BF_DPLL_FREQ_HARD_LIMT_B_SIZE = 8, BF_DPLL_FRE
Q_HARD_LIMT_B_MASK = 0xFF, BF_DPLL_FREQ_HARD_LIMT_B_LSB = 0,
BF_CURRENT_PH_DATA_A_SIZE = 8, BF_CURRENT_PH_DATA_A_MASK = 0xFF, BF_CURRENT_PH_
_DATA_A_LSB = 0, BF_CURRENT_PH_DATA_B_SIZE = 8,
BF_CURRENT_PH_DATA_B_MASK = 0xFF, BF_CURRENT_PH_DATA_B_LSB = 0, BF_OUT1_PATH_S
EL_SIZE = 4, BF_OUT1_PATH_SEL_MASK = 0xF0,
BF_OUT1_PATH_SEL_LSB = 4, BF_OUT1_DIVIDER_SIZE = 4, BF_OUT1_DIVIDER_MASK = 0x0F, BF_
OUT1_DIVIDER_LSB = 0,
BF_OUT2_PATH_SEL_SIZE = 4, BF_OUT2_PATH_SEL_MASK = 0xF0, BF_OUT2_PATH_SEL_LSB = 4,
BF_OUT2_DIVIDER_SIZE = 4,
BF_OUT2_DIVIDER_MASK = 0x0F, BF_OUT2_DIVIDER_LSB = 0, BF_OUT3_PATH_SEL_SIZE = 4, BF_
OUT3_PATH_SEL_MASK = 0xF0,
BF_OUT3_PATH_SEL_LSB = 4, BF_OUT3_DIVIDER_SIZE = 4, BF_OUT3_DIVIDER_MASK = 0x0F, BF_
OUT3_DIVIDER_LSB = 0,
BF_OUT4_PATH_SEL_SIZE = 4, BF_OUT4_PATH_SEL_MASK = 0xF0, BF_OUT4_PATH_SEL_LSB = 4,
BF_OUT4_DIVIDER_SIZE = 4,
BF_OUT4_DIVIDER_MASK = 0x0F, BF_OUT4_DIVIDER_LSB = 0, BF_OUT5_PATH_SEL_SIZE = 4, BF_
OUT5_PATH_SEL_MASK = 0xF0,
BF_OUT5_PATH_SEL_LSB = 4, BF_OUT5_DIVIDER_SIZE = 4, BF_OUT5_DIVIDER_MASK = 0x0F, BF_
OUT5_DIVIDER_LSB = 0,
BF_OUT6_PATH_SEL_SIZE = 4, BF_OUT6_PATH_SEL_MASK = 0xF0, BF_OUT6_PATH_SEL_LSB = 4,
BF_OUT6_DIVIDER_SIZE = 4,
BF_OUT6_DIVIDER_MASK = 0x0F, BF_OUT6_DIVIDER_LSB = 0, BF_OUT7_PATH_SEL_SIZE = 4, BF_
OUT7_PATH_SEL_MASK = 0xF0,
BF_OUT7_PATH_SEL_LSB = 4, BF_OUT7_DIVIDER_SIZE = 4, BF_OUT7_DIVIDER_MASK = 0x0F, BF_
OUT7_DIVIDER_LSB = 0,
BF_OUT8_PATH_SEL_SIZE = 1, BF_OUT8_PATH_SEL_MASK = 0x80, BF_OUT8_PATH_SEL_LSB = 7,
BF_OUT8_EN_SIZE = 1,
BF_OUT8_EN_MASK = 0x40, BF_OUT8_EN_LSB = 6, BF_T4_INPUT_FAIL_SIZE = 1, BF_T4_INPUT_FA
IL_MASK = 0x20,
BF_T4_INPUT_FAIL_LSB = 5, BF_AMI_OUT_DUTY_SIZE = 1, BF_AMI_OUT_DUTY_MASK = 0x10, BF_
AMI_OUT_DUTY_LSB = 4,
BF_400HZ_OUT_SEL_SIZE = 1, BF_400HZ_OUT_SEL_MASK = 0x08, BF_400HZ_OUT_SEL_LSB = 3,
BF_OUT9_INV_SIZE = 1,
BF_OUT9_INV_MASK = 0x04, BF_OUT9_INV_LSB = 2, BF_OUT7_INV_SIZE = 1, BF_OUT7_INV_MASK
= 0x02,
BF_OUT7_INV_LSB = 1, BF_OUT6_INV_SIZE = 1, BF_OUT6_INV_MASK = 0x01, BF_OUT6_INV_LSB =
0,
BF_OUT9_PATH_SEL_SIZE = 1, BF_OUT9_PATH_SEL_MASK = 0x80, BF_OUT9_PATH_SEL_LSB = 7,
BF_OUT9_EN_SIZE = 1,
BF_OUT9_EN_MASK = 0x40, BF_OUT9_EN_LSB = 6, BF_OUT5_INV_SIZE = 1, BF_OUT5_INV_MASK =

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0x10,
BF_OUT5_INV_LSB = 4, BF_OUT4_INV_SIZE = 1, BF_OUT4_INV_MASK = 0x08, BF_OUT4_INV_LSB =
3,
BF_OUT3_INV_SIZE = 1, BF_OUT3_INV_MASK = 0x04, BF_OUT3_INV_LSB = 2, BF_OUT2_INV_SIZE =
1,
BF_OUT2_INV_MASK = 0x02, BF_OUT2_INV_LSB = 1, BF_OUT1_INV_SIZE = 1, BF_OUT1_INV_MASK
= 0x01,
BF_OUT1_INV_LSB = 0, BF_IN_2K_4K_8K_INV_SIZE = 1, BF_IN_2K_4K_8K_INV_MASK = 0x80, BF_IN-
_2K_4K_8K_INV_LSB = 7,
BF_8K_EN_SIZE = 1, BF_8K_EN_MASK = 0x40, BF_8K_EN_LSB = 6, BF_2K_EN_SIZE = 1,
BF_2K_EN_MASK = 0x20, BF_2K_EN_LSB = 5, BF_2K_8K_PUL_POSITION_SIZE = 1, BF_2K_8K_PUL_-
POSITION_MASK = 0x10,
BF_2K_8K_PUL_POSITION_LSB = 4, BF_8K_INV_SIZE = 1, BF_8K_INV_MASK = 0x08, BF_8K_INV_LSB
= 3,
BF_8K_PUL_SIZE = 1, BF_8K_PUL_MASK = 0x04, BF_8K_PUL_LSB = 2, BF_2K_INV_SIZE = 1,
BF_2K_INV_MASK = 0x02, BF_2K_INV_LSB = 1, BF_2K_PUL_SIZE = 1, BF_2K_PUL_MASK = 0x01,
BF_2K_PUL_LSB = 0, BF_IN_NOISE_WINDOW_SIZE = 1, BF_IN_NOISE_WINDOW_MASK = 0x80, BF_I-
N_NOISE_WINDOW_LSB = 7,
BF_PH_OFFSET_A_SIZE = 8, BF_PH_OFFSET_A_MASK = 0xFF, BF_PH_OFFSET_A_LSB = 0, BF_PH_-
OFFSET_EN_SIZE = 1,
BF_PH_OFFSET_EN_MASK = 0x80, BF_PH_OFFSET_EN_LSB = 7, BF_PH_OFFSET_B_SIZE = 2, BF_-
PH_OFFSET_B_MASK = 0x03,
BF_PH_OFFSET_B_LSB = 0, BF_SYNC_BYPASS_SIZE = 1, BF_SYNC_BYPASS_MASK = 0x80, BF_SY-
NC_BYPASS_LSB = 7,
BF_SYNC_MON_LIMT_SIZE = 3, BF_SYNC_MON_LIMT_MASK = 0x70, BF_SYNC_MON_LIMT_LSB = 4,
BF_SYNC_EDGE_SIZE = 1,
BF_SYNC_EDGE_MASK = 0x40, BF_SYNC_EDGE_LSB = 6, BF_SYNC_PH2_SIZE = 2, BF_SYNC_PH2-
_MASK = 0x0C,
BF_SYNC_PH2_LSB = 2, BF_SYNC_PH1_SIZE = 2, BF_SYNC_PH1_MASK = 0x03, BF_SYNC_PH1_LSB
= 0,
BF_PROTECTION_DATA_SIZE = 8, BF_PROTECTION_DATA_MASK = 0xFF, BF_PROTECTION_DATA_-
_LSB = 0, BF_MPU_SEL_CNFG_SIZE = 3,
BF_MPU_SEL_CNFG_MASK = 0x07, BF_MPU_SEL_CNFG_LSB = 0, BF_T0_DFS_OFF_3_SIZE = 1,
BF_T0_DFS_OFF_3_MASK = 0x80,
BF_T0_DFS_OFF_3_LSB = 7, BF_T0_DFS_OFF_2_SIZE = 1, BF_T0_DFS_OFF_2_MASK = 0x40, BF_-
T0_DFS_OFF_2_LSB = 6,
BF_T0_DFS_OFF_1_SIZE = 1, BF_T0_DFS_OFF_1_MASK = 0x20, BF_T0_DFS_OFF_1_LSB = 5, BF_-
T0_DFS_OFF_0_SIZE = 1,
BF_T0_DFS_OFF_0_MASK = 0x10, BF_T0_DFS_OFF_0_LSB = 4, BF_T4_DFS_OFF_3_SIZE = 1, BF_-
T4_DFS_OFF_3_MASK = 0x08,
BF_T4_DFS_OFF_3_LSB = 3, BF_T4_DFS_OFF_2_SIZE = 1, BF_T4_DFS_OFF_2_MASK = 0x04, BF_-
T4_DFS_OFF_2_LSB = 2,
BF_T4_DFS_OFF_1_SIZE = 1, BF_T4_DFS_OFF_1_MASK = 0x02, BF_T4_DFS_OFF_1_LSB = 1, BF_-
T4_DFS_OFF_0_SIZE = 1,
BF_T4_DFS_OFF_0_MASK = 0x01, BF_T4_DFS_OFF_0_LSB = 0, BF_PPS_PHASE_SIZE = 2, BF_PPS-
_PHASE_MASK = 0x30,
BF_PPS_PHASE_LSB = 4, BF_PPS_PULSE_SIZE = 4, BF_PPS_PULSE_MASK = 0x0F, BF_PPS_PULS-
E_LSB = 0,
BF_T0_PH_SLOPE_SIZE = 2, BF_T0_PH_SLOPE_MASK = 0x0C, BF_T0_PH_SLOPE_LSB = 2, BF_T4_-
PH_SLOPE_SIZE = 2,
BF_T4_PH_SLOPE_MASK = 0x03, BF_T4_PH_SLOPE_LSB = 0, BF_ICP_CTRL_CODE_SIZE = 5, BF_IC-
P_CTRL_CODE_MASK = 0x1F,
BF_ICP_CTRL_CODE_LSB = 0, REGMAP_MAX }

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*Enumerated type listing register offsets and bit field constants.*

• enum {

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REG_CONTROL = 0x00, REG_CLK_SEL = 0x01, REG_PDSELO_LSB = 0x02, REG_PDSELO_MSB = 0x03,
REG_PDSEL1_LSB = 0x04, REG_PDSEL1_MSB = 0x05, REG_M0_LSB = 0x06, REG_M0_MSB = 0x07,
REG_M1_LSB = 0x08, REG_M1_MSB = 0x09, REG_ODBSELA0 = 0x0A, REG_ODBSELA1 = 0x0B,
REG_ODBSELB0 = 0x0C, REG_ODBSELB1 = 0x0D, REG_VCXO_SEL = 0x0E, REG_CONFIG_QA = 0x0F,
REG_CONFIG_QB = 0x10, BF_CONFIG_SIZE = 1, BF_CONFIG_MASK = 0x02, BF_CONFIG_LSB = 1,
BF_CLK_SEL_SIZE = 1, BF_CLK_SEL_MASK = 0x01, BF_CLK_SEL_LSB = 0, BF_PDSELO_LSB_SIZE =
8,
BF_PDSELO_LSB_MASK = 0xFF, BF_PDSELO_LSB_LSB = 0, BF_PDSELO_MSB_SIZE = 7, BF_PDSELO-
_MSB_MASK = 0x7F,
BF_PDSELO_MSB_LSB = 0, BF_PDSEL1_LSB_SIZE = 8, BF_PDSEL1_LSB_MASK = 0xFF, BF_PDSEL1-
_LSB_LSB = 0,
BF_PDSEL1_MSB_SIZE = 7, BF_PDSEL1_MSB_MASK = 0x7F, BF_PDSEL1_MSB_LSB = 0, BF_M0_LS-
B_SIZE = 8,
BF_M0_LSB_MASK = 0xFF, BF_M0_LSB_LSB = 0, BF_M0_MSB_SIZE = 7, BF_M0_MSB_MASK = 0x7F,
BF_M0_MSB_LSB = 0, BF_M1_LSB_SIZE = 8, BF_M1_LSB_MASK = 0xFF, BF_M1_LSB_LSB = 0,
BF_M1_MSB_SIZE = 7, BF_M1_MSB_MASK = 0x7F, BF_M1_MSB_LSB = 0, BF_ODBSELA0_SIZE = 3,
BF_ODBSELA0_MASK = 0x07, BF_ODBSELA0_LSB = 0, BF_ODBSELA1_SIZE = 3, BF_ODBSELA1_MA-
SK = 0x07,
BF_ODBSELA1_LSB = 0, BF_ODBSELB0_SIZE = 3, BF_ODBSELB0_MASK = 0x07, BF_ODBSELB0_LSB
= 0,
BF_ODBSELB1_SIZE = 3, BF_ODBSELB1_MASK = 0x07, BF_ODBSELB1_LSB = 0, BF_SEL_DOUBLE_-
SIZE = 1,
BF_SEL_DOUBLE_MASK = 0x80, BF_SEL_DOUBLE_LSB = 7, BF_MR_SYNC_SIZE = 1, BF_MR_SYNC-
_MASK = 0x40,
BF_MR_SYNC_LSB = 6, BF_BYPASS_SIZE = 1, BF_BYPASS_MASK = 0x20, BF_BYPASS_LSB = 5,
BF_SHUTOFF_SIZE = 1, BF_SHUTOFF_MASK = 0x10, BF_SHUTOFF_LSB = 4, BF_VCXO_SEL_SIZE =
1,
BF_VCXO_SEL_MASK = 0x01, BF_VCXO_SEL_LSB = 0, BF_LVDS_QA_SIZE = 1, BF_LVDS_QA_MASK
= 0x02,
BF_LVDS_QA_LSB = 1, BF_OE_A_SIZE = 1, BF_OE_A_MASK = 0x01, BF_OE_A_LSB = 0,
BF_LVDS_QB_SIZE = 1, BF_LVDS_QB_MASK = 0x02, BF_LVDS_QB_LSB = 1, BF_OE_B_SIZE = 1,
BF_OE_B_MASK = 0x01, BF_OE_B_LSB = 0, REGMAP_APLL_MAX }

```

*Enumerated type listing register offsets and bit field constants.*

#### 4.7.1 Detailed Description

#### 4.7.2 Enumeration Type Documentation

##### 4.7.2.1 anonymous enum

Enumerated type listing register offsets and bit field constants.

##### Enumerator

**REG\_ID\_LOW** Device ID Register 1, Low byte

**REG\_ID\_HIGH** Device ID Register 2, High byte

**REG\_MPU\_PIN\_STS** MPU Pin Status Register

**REG\_NOMINAL\_FREQ\_LOW\_CNFG** Crystal Oscillator Frequency Offset Calibration Configuration Register  
1,value[7:0]

**REG\_NOMINAL\_FREQ\_MID\_CNFG** Crystal Oscillator Frequency Offset Calibration Configuration Register  
2,value[15:8]

**REG\_NOMINAL\_FREQ\_HIGH\_CNFG** Crystal Oscillator Frequency Offset Calibration Configuration Register  
3,value[23:16]

**REG\_T4\_T0\_SEL\_CNFG** T0/T4 Register Selection Configuration

**REG\_PHASE\_ALARM\_TIME\_OUT\_CNFG** Phase Lock Alarm Time Out Configuration Register



**REG\_INPUT\_MODE\_CNFG** Input Mode Control Register

**REG\_DIFFERENTIAL\_IN\_OUT\_CNFG** Differential Input/Output Port Configuration Register

**REG\_MON\_SW\_HS\_CNFG** Frequency Monitoring, Master Clock Switch, Input Clock Switch, HS Configuration Register

**REG\_INTERRUPT\_CNFG** Interrupt Configuration Register

**REG\_INTERRUPTS1\_STS** Interrupt Status Register 1

**REG\_INTERRUPTS2\_STS** Interrupt Status Register 2

**REG\_INTERRUPTS3\_STS** Interrupt Status Register 3

**REG\_INTERRUPTS1\_MASK\_CNFG** Interrupt Mask Register 1

**REG\_INTERRUPTS2\_MASK\_CNFG** Interrupt Mask Register 2

**REG\_INTERRUPTS3\_MASK\_CNFG** Interrupt Mask Register 3

**REG\_MS\_SL\_CTRL\_CNFG** Master Slave Control

**REG\_IN1\_CNFG** Input 1 Configuration Register

**REG\_IN2\_CNFG** Input 2 Configuration Register

**REG\_IN3\_CNFG** Input 3 Configuration Register

**REG\_IN4\_CNFG** Input 4 Configuration Register

**REG\_IN5\_IN6\_HF\_DIV\_CNFG** Input 5 and Input 6 High Frequency divider Configuration Register

**REG\_IN5\_CNFG** Input 5 Configuration Register

**REG\_IN6\_CNFG** Input 6 Configuration Register

**REG\_IN7\_CNFG** Input 7 Configuration Register

**REG\_IN8\_CNFG** Input 8 Configuration Register

**REG\_IN9\_CNFG** Input 9 Configuration Register

**REG\_IN10\_CNFG** Input 10 Configuration Register

**REG\_IN11\_CNFG** Input 11 Configuration Register

**REG\_IN12\_CNFG** Input 12 Configuration Register

**REG\_IN13\_CNFG** Input 13 Configuration Register

**REG\_IN14\_CNFG** Input 14 Configuration Register

**REG\_PRE\_DIV\_CH\_CNFG** Input Clock Select for Frequency division Configuration Register

**REG\_PRE\_DIVN\_LOW\_CNFG** DivN Divider Configuration Register 1, Low byte

**REG\_PRE\_DIVN\_HIGH\_CNFG** DivN Divider Configuration Register 2, High byte

**REG\_IN1\_IN2\_SEL\_PRIORITY\_CNFG** Input 1 and Input 2 Priority Configuration Register

**REG\_IN3\_IN4\_SEL\_PRIORITY\_CNFG** Input 3 and Input 4 Priority Configuration Register

**REG\_IN5\_IN6\_SEL\_PRIORITY\_CNFG** Input 5 and Input 6 Priority Configuration Register

**REG\_IN7\_IN8\_SEL\_PRIORITY\_CNFG** Input 7 and Input 8 Priority Configuration Register

**REG\_IN9\_IN10\_SEL\_PRIORITY\_CNFG** Input 9 and Input 10 Priority Configuration Register

**REG\_IN11\_IN12\_SEL\_PRIORITY\_CNFG** Input 11 and Input 12 Priority Configuration Register

**REG\_IN13\_IN14\_SEL\_PRIORITY\_CNFG** Input 13 and Input 14 Priority Configuration Register

**REG\_PAGE\_POINTER\_CNFG** Page Pointer Configuration Register

**REG\_FREQ\_MON\_FACTOR\_CNFG** Frequency Monitor Factor Configuration Register

**REG\_HARD\_FREQ\_MON\_THRESHOLD\_CNFG** Hard Frequency Alarm Threshold for the Non-Selected Input Clocks Configuration Register

**REG\_SOFT\_FREQ\_MON\_THRESHOLD\_CNFG** Soft Frequency Alarm Threshold for the Selected Input Clock Configuration Register

**REG\_UPPER\_THRESHOLD\_0\_CNFG** Upper Threshold 0 Configuration Register

**REG\_LOWER\_THRESHOLD\_0\_CNFG** Lower Threshold 0 Configuration Register



**REG\_BUCKET\_SIZE\_0\_CNFG** Leaky Bucket Size 0 Configuration Register  
**REG\_DECAY\_RATE\_0\_CNFG** Decay Rate 0 Configuration Register  
**REG\_UPPER\_THRESHOLD\_1\_CNFG** Upper Threshold 1 Configuration Register  
**REG\_LOWER\_THRESHOLD\_1\_CNFG** Lower Threshold 1 Configuration Register  
**REG\_BUCKET\_SIZE\_1\_CNFG** Leaky Bucket Size 1 Configuration Register  
**REG\_DECAY\_RATE\_1\_CNFG** Decay Rate 1 Configuration Register  
**REG\_UPPER\_THRESHOLD\_2\_CNFG** Upper Threshold 2 Configuration Register  
**REG\_LOWER\_THRESHOLD\_2\_CNFG** Lower Threshold 2 Configuration Register  
**REG\_BUCKET\_SIZE\_2\_CNFG** Leaky Bucket Size 2 Configuration Register  
**REG\_DECAY\_RATE\_2\_CNFG** Decay Rate 2 Configuration Register  
**REG\_UPPER\_THRESHOLD\_3\_CNFG** Upper Threshold 3 Configuration Register  
**REG\_LOWER\_THRESHOLD\_3\_CNFG** Lower Threshold 3 Configuration Register  
**REG\_BUCKET\_SIZE\_3\_CNFG** Leaky Bucket Size 3 Configuration Register  
**REG\_DECAY\_RATE\_3\_CNFG** Decay Rate 3 Configuration Register  
**REG\_IN\_FREQ\_READ\_CH\_CNFG** Input Clock Selection for Frequency Monitoring Result Read Register  
**REG\_IN\_FREQ\_READ\_STS** Input Clock Frequency Offset Register  
**REG\_IN1\_IN2\_STS** Input 1 and Input 2 Status Register  
**REG\_IN3\_IN4\_STS** Input 3 and Input 4 Status Register  
**REG\_IN5\_IN6\_STS** Input 5 and Input 6 Status Register  
**REG\_IN7\_IN8\_STS** Input 7 and Input 8 Status Register  
**REG\_IN9\_IN10\_STS** Input 9 and Input 10 Status Register  
**REG\_IN11\_IN12\_STS** Input 11 and Input 12 Status Register  
**REG\_IN13\_IN14\_STS** Input 13 and Input 14 Status Register  
**REG\_INPUT\_VALID1\_STS** Input Clock Validation Register 1  
**REG\_INPUT\_VALID2\_STS** Input Clock Validation Register 2  
**REG\_REMOTE\_INPUT\_VALID1\_CNFG** Remote Input Clock Validation Register 1  
**REG\_REMOTE\_INPUT\_VALID2\_CNFG** Remote Input Clock Validation Register 2  
**REG\_PRIORITY\_TABLE1\_STS** The Highest Priority Valid Input Clock and the Selected Input Clock Register  
  
**REG\_PRIORITY\_TABLE2\_STS** The Second Highest Priority Valid Input Clock and the Selected Input Clock Register  
**REG\_T0\_INPUT\_SEL\_CNFG** T0 Input Clock Selection Configuration Register  
**REG\_T4\_INPUT\_SEL\_CNFG** T4 Input Clock Selection Configuration Register  
**REG\_OPERATING\_STS** Operating Status Register  
**REG\_T0\_OPERATION\_MODE\_CNFG** T0 DPLL Operation Mode Selection Register  
**REG\_T4\_OPERATION\_MODE\_CNFG** T4 DPLL Operation Mode Selection Register  
**REG\_T0\_DPLL\_APLL\_PATH\_CNFG** T0 DPLL APLL Path Configuration Register  
**REG\_T0\_DPLL\_START\_BW\_DAMPING\_CNFG** T0 DPLL Start Bandwidth and Damping Factor Configuration Register  
**REG\_T0\_DPLL\_ACQ\_BW\_DAMPING\_CNFG** T0 DPLL Acquisition Bandwidth and Damping Factor Configuration Register  
**REG\_T0\_DPLL\_LOCKED\_BW\_DAMPING\_CNFG** T0 DPLL Locked Bandwidth and Damping Factor Configuration Register  
**REG\_T0\_BW\_OVERSHOOT\_CNFG** T0 DPLL Bandwidth Overshoot Configuration Register  
**REG\_PHASE\_LOSS\_COARSE\_LIMIT\_CNFG** Coarse Phase Lock Detector Configuration Register  
**REG\_PHASE\_LOSS\_FINE\_LIMIT\_CNFG** Fine Phase Lock Detector Configuration Register

**REG\_T0\_HOLDOVER\_MODE\_CNFG** T0 DPLL Holdover Mode Configuration Register  
**REG\_HOLDOVER\_FREQ\_LOW\_CNFG** DPLL Holdover Frequency Register 1  
**REG\_HOLDOVER\_FREQ\_MID\_CNFG** DPLL Holdover Frequency Register 2  
**REG\_HOLDOVER\_FREQ\_HIGH\_CNFG** DPLL Holdover Frequency Register 3  
**REG\_T4\_DPLL\_APLL\_PATH\_CNFG** T4 DPLL APLL Path Configuration Register  
**REG\_T4\_DPLL\_LOCKED\_BW\_DAMPING\_CNFG** T4 DPLL Locked Bandwidth and Damping Factor Configuration Register  
**REG\_CURRENT\_FREQ\_LOW\_STS** DPLL Current Frequency Register 1  
**REG\_CURRENT\_FREQ\_MID\_STS** DPLL Current Frequency Register 2  
**REG\_CURRENT\_FREQ\_HIGH\_STS** DPLL Current Frequency Register 3  
**REG\_DPLL\_FREQ\_SOFT\_LIMIT\_CNFG** DPLL Soft Frequency Alarm Limit Configuration Register  
**REG\_DPLL\_FREQ\_HARD\_LIMIT\_LOW\_CNFG** DPLL Hard Frequency Alarm Limit Configuration Register 1  
  
**REG\_DPLL\_FREQ\_HARD\_LIMIT\_MID\_CNFG** DPLL Hard Frequency Alarm Limit Configuration Register 2  
**REG\_CURRENT\_DPLL\_PHASE\_LOW\_STS** Current DPLL Phase Register 1  
**REG\_CURRENT\_DPLL\_PHASE\_HIGH\_STS** Current DPLL Phase Register 2  
**REG\_OUT1\_FREQ\_CNFG** Output 1 Configuration Register  
**REG\_OUT2\_FREQ\_CNFG** Output 2 Configuration Register  
**REG\_OUT3\_FREQ\_CNFG** Output 3 Configuration Register  
**REG\_OUT4\_FREQ\_CNFG** Output 4 Configuration Register  
**REG\_OUT5\_FREQ\_CNFG** Output 5 Configuration Register  
**REG\_OUT6\_FREQ\_CNFG** APLL 1 Clock Frequency Configuration  
**REG\_OUT7\_FREQ\_CNFG** APLL 2 Clock Frequency Configuration  
**REG\_OUT8\_FREQ\_CNFG** Output 8 Configuration Register  
**REG\_OUT9\_FREQ\_CNFG** Output 9 Configuration Register  
**REG\_FR\_MFR\_SYNC\_CNFG** Frame Sync and Multi-frame Sync Output Configuration Register  
**REG\_PHASE\_MON\_CNFG** Phase Transient Monitor Configuration Register  
**REG\_PHASE\_OFFSET\_LOW\_CNFG** Phase Offset Control Register 1  
**REG\_PHASE\_OFFSET\_HIGH\_CNFG** Phase Offset Control Register 2  
**REG\_SYNC\_MONITOR\_CNFG** Sync Monitor Configuration Register  
**REG\_SYNC\_PHASE\_CNFG** Sync Phase Configuration Register  
**REG\_PROTECTION\_CNFG** Registers Access Mode Selection Register  
**REG\_MPU\_SEL\_CNFG** MPU Interface Mode Selection Register  
**REG\_DFS\_OFF\_CNFG** Digital Frequency Synthesizer Configuration Register  
**REG\_T0\_PPS\_CNFG** T0 1 Pulse Per Second Configuration Register  
**REG\_PH\_SLOPE\_CNFG** Phase Slope limiting Register  
**REG\_T0\_ICP\_CTRL\_CNFG** T0 APLL Charge Pump Current Configuration Register  
**REG\_T4\_ICP\_CTRL\_CNFG** T4 APLL Charge Pump Current Configuration Register  
**REG\_T4\_PPS\_CNFG** T4 1 Pulse Per Second Configuration Register  
**BF\_ID\_A\_SIZE** ID\_LOW  
**BF\_ID\_A\_MASK**  
**BF\_ID\_A\_LSB**  
**BF\_ID\_B\_SIZE** ID\_HIGH  
**BF\_ID\_B\_MASK**  
**BF\_ID\_B\_LSB**

**BF\_MPU\_PIN\_STS\_SIZE** MPU\_PIN\_STS  
**BF\_MPU\_PIN\_STS\_MASK**  
**BF\_MPU\_PIN\_STS\_LSB**  
**BF\_NOMINAL\_FREQ\_VALUE\_A\_SIZE** NOMINAL\_FREQ\_LOW\_CNFG  
**BF\_NOMINAL\_FREQ\_VALUE\_A\_MASK**  
**BF\_NOMINAL\_FREQ\_VALUE\_A\_LSB**  
**BF\_NOMINAL\_FREQ\_VALUE\_B\_SIZE** NOMINAL\_FREQ\_MID\_CNFG  
**BF\_NOMINAL\_FREQ\_VALUE\_B\_MASK**  
**BF\_NOMINAL\_FREQ\_VALUE\_B\_LSB**  
**BF\_NOMINAL\_FREQ\_VALUE\_C\_SIZE** NOMINAL\_FREQ\_HIGH\_CNFG  
**BF\_NOMINAL\_FREQ\_VALUE\_C\_MASK**  
**BF\_NOMINAL\_FREQ\_VALUE\_C\_LSB**  
**BF\_T4\_T0\_SEL\_SIZE** T4\_T0\_SEL\_CNFG  
**BF\_T4\_T0\_SEL\_MASK**  
**BF\_T4\_T0\_SEL\_LSB**  
**BF\_MULTI\_FACTOR\_SIZE** PHASE\_ALARM\_TIME\_OUT\_CNFG  
**BF\_MULTI\_FACTOR\_MASK**  
**BF\_MULTI\_FACTOR\_LSB**  
**BF\_TIMEOUT\_VALUE\_SIZE** PHASE\_ALARM\_TIME\_OUT\_CNFG  
**BF\_TIMEOUT\_VALUE\_MASK**  
**BF\_TIMEOUT\_VALUE\_LSB**  
**BF\_AUTO\_EXT\_SYNC\_EN\_SIZE** INPUT\_MODE\_CNFG  
**BF\_AUTO\_EXT\_SYNC\_EN\_MASK**  
**BF\_AUTO\_EXT\_SYNC\_EN\_LSB**  
**BF\_EXT\_SYNC\_EN\_SIZE** INPUT\_MODE\_CNFG  
**BF\_EXT\_SYNC\_EN\_MASK**  
**BF\_EXT\_SYNC\_EN\_LSB**  
**BF\_PH\_ALARM\_TIMEOUT\_SIZE** INPUT\_MODE\_CNFG  
**BF\_PH\_ALARM\_TIMEOUT\_MASK**  
**BF\_PH\_ALARM\_TIMEOUT\_LSB**  
**BF\_SYNC\_FREQ\_SIZE** INPUT\_MODE\_CNFG  
**BF\_SYNC\_FREQ\_MASK**  
**BF\_SYNC\_FREQ\_LSB**  
**BF\_IN\_SONET\_SDH\_SIZE** INPUT\_MODE\_CNFG  
**BF\_IN\_SONET\_SDH\_MASK**  
**BF\_IN\_SONET\_SDH\_LSB**  
**BF\_MASTER\_SLAVE\_SIZE** INPUT\_MODE\_CNFG  
**BF\_MASTER\_SLAVE\_MASK**  
**BF\_MASTER\_SLAVE\_LSB**  
**BF\_REVERTIVE\_MODE\_SIZE** INPUT\_MODE\_CNFG  
**BF\_REVERTIVE\_MODE\_MASK**  
**BF\_REVERTIVE\_MODE\_LSB**  
**BF\_OSC\_EDGE\_SIZE** DIFFERENTIAL\_IN\_OUT\_CNFG  
**BF\_OSC\_EDGE\_MASK**  
**BF\_OSC\_EDGE\_LSB**

***BF\_OUT7\_PECL\_LVDS\_SIZE*** DIFFERENTIAL\_IN\_OUT\_CNFG  
***BF\_OUT7\_PECL\_LVDS\_MASK***  
***BF\_OUT7\_PECL\_LVDS\_LSB***  
***BF\_OUT6\_PECL\_LVDS\_SIZE*** DIFFERENTIAL\_IN\_OUT\_CNFG  
***BF\_OUT6\_PECL\_LVDS\_MASK***  
***BF\_OUT6\_PECL\_LVDS\_LSB***  
***BF\_FREQ\_MON\_CLK\_SIZE*** MON\_SW\_HS\_CNFG  
***BF\_FREQ\_MON\_CLK\_MASK***  
***BF\_FREQ\_MON\_CLK\_LSB***  
***BF\_LOS\_FLAG\_TO\_TDO\_SIZE*** MON\_SW\_HS\_CNFG  
***BF\_LOS\_FLAG\_TO\_TDO\_MASK***  
***BF\_LOS\_FLAG\_TO\_TDO\_LSB***  
***BF\_ULTR\_FAST\_SW\_SIZE*** MON\_SW\_HS\_CNFG  
***BF\_ULTR\_FAST\_SW\_MASK***  
***BF\_ULTR\_FAST\_SW\_LSB***  
***BF\_EXT\_SW\_SIZE*** MON\_SW\_HS\_CNFG  
***BF\_EXT\_SW\_MASK***  
***BF\_EXT\_SW\_LSB***  
***BF\_HS\_FREZ\_SIZE*** MON\_SW\_HS\_CNFG  
***BF\_HS\_FREZ\_MASK***  
***BF\_HS\_FREZ\_LSB***  
***BF\_HS\_EN\_SIZE*** MON\_SW\_HS\_CNFG  
***BF\_HS\_EN\_MASK***  
***BF\_HS\_EN\_LSB***  
***BF\_FREQ\_MON\_HARD\_EN\_SIZE*** MON\_SW\_HS\_CNFG  
***BF\_FREQ\_MON\_HARD\_EN\_MASK***  
***BF\_FREQ\_MON\_HARD\_EN\_LSB***  
***BF\_HZ\_EN\_SIZE*** INTERRUPT\_CNFG  
***BF\_HZ\_EN\_MASK***  
***BF\_HZ\_EN\_LSB***  
***BF\_INT\_POL\_SIZE*** INTERRUPT\_CNFG  
***BF\_INT\_POL\_MASK***  
***BF\_INT\_POL\_LSB***  
***BF\_IN8\_SIZE*** INTERRUPTS1\_STS INTERRUPTS1\_MASK\_CNFG INPUT\_VALID1\_STS REMOTE\_INPUT-  
VALID1\_CNFG  
***BF\_IN8\_MASK***  
***BF\_IN8\_LSB***  
***BF\_IN7\_SIZE*** INTERRUPTS1\_STS INTERRUPTS1\_MASK\_CNFG INPUT\_VALID1\_STS REMOTE\_INPUT-  
VALID1\_CNFG  
***BF\_IN7\_MASK***  
***BF\_IN7\_LSB***  
***BF\_IN6\_SIZE*** INTERRUPTS1\_STS INTERRUPTS1\_MASK\_CNFG INPUT\_VALID1\_STS REMOTE\_INPUT-  
VALID1\_CNFG  
***BF\_IN6\_MASK***  
***BF\_IN6\_LSB***

**BF\_IN5\_SIZE** INTERRUPTS1\_STS INTERRUPTS1\_MASK\_CNFG INPUT\_VALID1\_STS REMOTE\_INPUT\_VALID1\_CNFG

**BF\_IN5\_MASK**

**BF\_IN5\_LSB**

**BF\_IN4\_SIZE** INTERRUPTS1\_STS INTERRUPTS1\_MASK\_CNFG INPUT\_VALID1\_STS REMOTE\_INPUT\_VALID1\_CNFG

**BF\_IN4\_MASK**

**BF\_IN4\_LSB**

**BF\_IN3\_SIZE** INTERRUPTS1\_STS INTERRUPTS1\_MASK\_CNFG INPUT\_VALID1\_STS REMOTE\_INPUT\_VALID1\_CNFG

**BF\_IN3\_MASK**

**BF\_IN3\_LSB**

**BF\_IN2\_SIZE** INTERRUPTS1\_STS INTERRUPTS1\_MASK\_CNFG INPUT\_VALID1\_STS REMOTE\_INPUT\_VALID1\_CNFG

**BF\_IN2\_MASK**

**BF\_IN2\_LSB**

**BF\_IN1\_SIZE** INTERRUPTS1\_STS INTERRUPTS1\_MASK\_CNFG INPUT\_VALID1\_STS REMOTE\_INPUT\_VALID1\_CNFG

**BF\_IN1\_MASK**

**BF\_IN1\_LSB**

**BF\_T0\_OPERATING\_MODE\_STS\_SIZE** INTERRUPTS2\_STS INTERRUPTS2\_MASK\_CNFG

**BF\_T0\_OPERATING\_MODE\_STS\_MASK**

**BF\_T0\_OPERATING\_MODE\_STS\_LSB**

**BF\_T0\_MAIN\_REF\_FAIL\_SIZE** INTERRUPTS2\_STS INTERRUPTS2\_MASK\_CNFG

**BF\_T0\_MAIN\_REF\_FAIL\_MASK**

**BF\_T0\_MAIN\_REF\_FAIL\_LSB**

**BF\_IN14\_SIZE** INTERRUPTS2\_STS INTERRUPTS2\_MASK\_CNFG INPUT\_VALID2\_STS REMOTE\_INPUT\_VALID2\_CNFG

**BF\_IN14\_MASK**

**BF\_IN14\_LSB**

**BF\_IN13\_SIZE** INTERRUPTS2\_STS INTERRUPTS2\_MASK\_CNFG INPUT\_VALID2\_STS REMOTE\_INPUT\_VALID2\_CNFG

**BF\_IN13\_MASK**

**BF\_IN13\_LSB**

**BF\_IN12\_SIZE** INTERRUPTS2\_STS INTERRUPTS2\_MASK\_CNFG INPUT\_VALID2\_STS REMOTE\_INPUT\_VALID2\_CNFG

**BF\_IN12\_MASK**

**BF\_IN12\_LSB**

**BF\_IN11\_SIZE** INTERRUPTS2\_STS INTERRUPTS2\_MASK\_CNFG INPUT\_VALID2\_STS REMOTE\_INPUT\_VALID2\_CNFG

**BF\_IN11\_MASK**

**BF\_IN11\_LSB**

**BF\_IN10\_SIZE** INTERRUPTS2\_STS INTERRUPTS2\_MASK\_CNFG INPUT\_VALID2\_STS REMOTE\_INPUT\_VALID2\_CNFG

**BF\_IN10\_MASK**

**BF\_IN10\_LSB**

**BF\_IN9\_SIZE** INTERRUPTS2\_STS INTERRUPTS2\_MASK\_CNFG INPUT\_VALID2\_STS REMOTE\_INPUT\_VALID2\_CNFG

**BF\_IN9\_MASK**  
**BF\_IN9\_LSB**  
**BF\_EX\_SYNC\_ALARM\_SIZE** INTERRUPTS3\_STS INTERRUPTS3\_MASK\_CNFG  
**BF\_EX\_SYNC\_ALARM\_MASK**  
**BF\_EX\_SYNC\_ALARM\_LSB**  
**BF\_T4\_STS\_SIZE** INTERRUPTS3\_STS INTERRUPTS3\_MASK\_CNFG  
**BF\_T4\_STS\_MASK**  
**BF\_T4\_STS\_LSB**  
**BF\_INPUT\_TO\_T4\_SIZE** INTERRUPTS3\_STS INTERRUPTS3\_MASK\_CNFG  
**BF\_INPUT\_TO\_T4\_MASK**  
**BF\_INPUT\_TO\_T4\_LSB**  
**BF\_AMI2\_VIOL\_SIZE** INTERRUPTS3\_STS INTERRUPTS3\_MASK\_CNFG  
**BF\_AMI2\_VIOL\_MASK**  
**BF\_AMI2\_VIOL\_LSB**  
**BF\_AMI2\_LOS\_SIZE** INTERRUPTS3\_STS INTERRUPTS3\_MASK\_CNFG  
**BF\_AMI2\_LOS\_MASK**  
**BF\_AMI2\_LOS\_LSB**  
**BF\_AMI1\_VIOL\_SIZE** INTERRUPTS3\_STS INTERRUPTS3\_MASK\_CNFG  
**BF\_AMI1\_VIOL\_MASK**  
**BF\_AMI1\_VIOL\_LSB**  
**BF\_AMI1\_LOS\_SIZE** INTERRUPTS3\_STS INTERRUPTS3\_MASK\_CNFG  
**BF\_AMI1\_LOS\_MASK**  
**BF\_AMI1\_LOS\_LSB**  
**BF\_PPS\_FAST\_FREQ\_LOCK\_EN\_SIZE** MS\_SL\_CTRL\_CNFG  
**BF\_PPS\_FAST\_FREQ\_LOCK\_EN\_MASK**  
**BF\_PPS\_FAST\_FREQ\_LOCK\_EN\_LSB**  
**BF\_PPS\_FAST\_PH\_LOCK\_EN\_SIZE** MS\_SL\_CTRL\_CNFG  
**BF\_PPS\_FAST\_PH\_LOCK\_EN\_MASK**  
**BF\_PPS\_FAST\_PH\_LOCK\_EN\_LSB**  
**BF\_MS\_SL\_CTRL\_SIZE** MS\_SL\_CTRL\_CNFG  
**BF\_MS\_SL\_CTRL\_MASK**  
**BF\_MS\_SL\_CTRL\_LSB**  
**BF\_400HZ\_SEL\_SIZE** IN1\_CNFG IN2\_CNFG  
**BF\_400HZ\_SEL\_MASK**  
**BF\_400HZ\_SEL\_LSB**  
**BF\_BUCKET\_SEL\_SIZE** IN1\_CNFG IN2\_CNFG IN3\_CNFG IN4\_CNFG IN5\_CNFG IN6\_CNFG IN7\_CNFG  
 IN8\_CNFG IN9\_CNFG IN10\_CNFG IN11\_CNFG IN12\_CNFG IN13\_CNFG IN14\_CNFG  
**BF\_BUCKET\_SEL\_MASK**  
**BF\_BUCKET\_SEL\_LSB**  
**BF\_IN\_FREQ\_SIZE** IN1\_CNFG IN2\_CNFG IN3\_CNFG IN4\_CNFG IN5\_CNFG IN6\_CNFG IN7\_CNFG IN8-  
 \_CNFG IN9\_CNFG IN10\_CNFG IN11\_CNFG IN12\_CNFG IN13\_CNFG IN14\_CNFG  
**BF\_IN\_FREQ\_MASK**  
**BF\_IN\_FREQ\_LSB**  
**BF\_DIRECT\_DIV\_SIZE** IN3\_CNFG IN4\_CNFG IN5\_CNFG IN6\_CNFG IN7\_CNFG IN8\_CNFG IN9\_CNFG  
 IN10\_CNFG IN11\_CNFG IN12\_CNFG IN13\_CNFG IN14\_CNFG

***BF\_DIRECT\_DIV\_MASK***

***BF\_DIRECT\_DIV\_LSB***

***BF\_LOCK\_8K\_SIZE*** IN3\_CNFG IN4\_CNFG IN5\_CNFG IN6\_CNFG IN7\_CNFG IN8\_CNFG IN9\_CNFG I-  
N10\_CNFG IN11\_CNFG IN12\_CNFG IN13\_CNFG IN14\_CNFG

***BF\_LOCK\_8K\_MASK***

***BF\_LOCK\_8K\_LSB***

***BF\_IN6\_DIV\_SIZE*** IN5\_IN6\_HF\_DIV\_CNFG

***BF\_IN6\_DIV\_MASK***

***BF\_IN6\_DIV\_LSB***

***BF\_IN5\_DIV\_SIZE*** IN5\_IN6\_HF\_DIV\_CNFG

***BF\_IN5\_DIV\_MASK***

***BF\_IN5\_DIV\_LSB***

***BF\_PRE\_DIV\_CH\_VALUE\_SIZE*** PRE\_DIV\_CH\_CNFG

***BF\_PRE\_DIV\_CH\_VALUE\_MASK***

***BF\_PRE\_DIV\_CH\_VALUE\_LSB***

***BF\_PRE\_DIVN\_VALUE\_A\_SIZE*** PRE\_DIVN\_LOW\_CNFG

***BF\_PRE\_DIVN\_VALUE\_A\_MASK***

***BF\_PRE\_DIVN\_VALUE\_A\_LSB***

***BF\_PRE\_DIVN\_VALUE\_B\_SIZE*** PRE\_DIVN\_HIGH\_CNFG

***BF\_PRE\_DIVN\_VALUE\_B\_MASK***

***BF\_PRE\_DIVN\_VALUE\_B\_LSB***

***BF\_IN2\_SEL\_PRIORITY\_SIZE*** IN1\_IN2\_SEL\_PRIORITY\_CNFG

***BF\_IN2\_SEL\_PRIORITY\_MASK***

***BF\_IN2\_SEL\_PRIORITY\_LSB***

***BF\_IN1\_SEL\_PRIORITY\_SIZE*** IN1\_IN2\_SEL\_PRIORITY\_CNFG

***BF\_IN1\_SEL\_PRIORITY\_MASK***

***BF\_IN1\_SEL\_PRIORITY\_LSB***

***BF\_IN4\_SEL\_PRIORITY\_SIZE*** IN3\_IN4\_SEL\_PRIORITY\_CNFG

***BF\_IN4\_SEL\_PRIORITY\_MASK***

***BF\_IN4\_SEL\_PRIORITY\_LSB***

***BF\_IN3\_SEL\_PRIORITY\_SIZE*** IN3\_IN4\_SEL\_PRIORITY\_CNFG

***BF\_IN3\_SEL\_PRIORITY\_MASK***

***BF\_IN3\_SEL\_PRIORITY\_LSB***

***BF\_IN6\_SEL\_PRIORITY\_SIZE*** IN5\_IN6\_SEL\_PRIORITY\_CNFG

***BF\_IN6\_SEL\_PRIORITY\_MASK***

***BF\_IN6\_SEL\_PRIORITY\_LSB***

***BF\_IN5\_SEL\_PRIORITY\_SIZE*** IN5\_IN6\_SEL\_PRIORITY\_CNFG

***BF\_IN5\_SEL\_PRIORITY\_MASK***

***BF\_IN5\_SEL\_PRIORITY\_LSB***

***BF\_IN8\_SEL\_PRIORITY\_SIZE*** IN7\_IN8\_SEL\_PRIORITY\_CNFG

***BF\_IN8\_SEL\_PRIORITY\_MASK***

***BF\_IN8\_SEL\_PRIORITY\_LSB***

***BF\_IN7\_SEL\_PRIORITY\_SIZE*** IN7\_IN8\_SEL\_PRIORITY\_CNFG

***BF\_IN7\_SEL\_PRIORITY\_MASK***

***BF\_IN7\_SEL\_PRIORITY\_LSB***

***BF\_IN10\_SEL\_PRIORITY\_SIZE*** IN9\_IN10\_SEL\_PRIORITY\_CNFG  
***BF\_IN10\_SEL\_PRIORITY\_MASK***  
***BF\_IN10\_SEL\_PRIORITY\_LSB***  
***BF\_IN9\_SEL\_PRIORITY\_SIZE*** IN9\_IN10\_SEL\_PRIORITY\_CNFG  
***BF\_IN9\_SEL\_PRIORITY\_MASK***  
***BF\_IN9\_SEL\_PRIORITY\_LSB***  
***BF\_IN12\_SEL\_PRIORITY\_SIZE*** IN11\_IN12\_SEL\_PRIORITY\_CNFG  
***BF\_IN12\_SEL\_PRIORITY\_MASK***  
***BF\_IN12\_SEL\_PRIORITY\_LSB***  
***BF\_IN11\_SEL\_PRIORITY\_SIZE*** IN11\_IN12\_SEL\_PRIORITY\_CNFG  
***BF\_IN11\_SEL\_PRIORITY\_MASK***  
***BF\_IN11\_SEL\_PRIORITY\_LSB***  
***BF\_IN14\_SEL\_PRIORITY\_SIZE*** IN13\_IN14\_SEL\_PRIORITY\_CNFG  
***BF\_IN14\_SEL\_PRIORITY\_MASK***  
***BF\_IN14\_SEL\_PRIORITY\_LSB***  
***BF\_IN13\_SEL\_PRIORITY\_SIZE*** IN13\_IN14\_SEL\_PRIORITY\_CNFG  
***BF\_IN13\_SEL\_PRIORITY\_MASK***  
***BF\_IN13\_SEL\_PRIORITY\_LSB***  
***BF\_PAGE\_POINTER\_SIZE*** PAGE\_POINTER\_CNFG  
***BF\_PAGE\_POINTER\_MASK***  
***BF\_PAGE\_POINTER\_LSB***  
***BF\_FREQ\_MON\_FACTOR\_SIZE*** FREQ\_MON\_FACTOR\_CNFG  
***BF\_FREQ\_MON\_FACTOR\_MASK***  
***BF\_FREQ\_MON\_FACTOR\_LSB***  
***BF\_HARD\_FREQ\_MON\_THRESHOLD\_A\_SIZE*** HARD\_FREQ\_MON\_THRESHOLD\_CNFG  
***BF\_HARD\_FREQ\_MON\_THRESHOLD\_A\_MASK***  
***BF\_HARD\_FREQ\_MON\_THRESHOLD\_A\_LSB***  
***BF\_HARD\_FREQ\_MON\_THRESHOLD\_B\_SIZE*** HARD\_FREQ\_MON\_THRESHOLD\_CNFG  
***BF\_HARD\_FREQ\_MON\_THRESHOLD\_B\_MASK***  
***BF\_HARD\_FREQ\_MON\_THRESHOLD\_B\_LSB***  
***BF\_SOFT\_FREQ\_MON\_THRESHOLD\_A\_SIZE*** SOFT\_FREQ\_MON\_THRESHOLD\_CNFG  
***BF\_SOFT\_FREQ\_MON\_THRESHOLD\_A\_MASK***  
***BF\_SOFT\_FREQ\_MON\_THRESHOLD\_A\_LSB***  
***BF\_SOFT\_FREQ\_MON\_THRESHOLD\_B\_SIZE*** SOFT\_FREQ\_MON\_THRESHOLD\_CNFG  
***BF\_SOFT\_FREQ\_MON\_THRESHOLD\_B\_MASK***  
***BF\_SOFT\_FREQ\_MON\_THRESHOLD\_B\_LSB***  
***BF\_UPPER\_THRESHOLD\_DATA\_SIZE*** UPPER\_THRESHOLD\_0\_CNFG UPPER\_THRESHOLD\_1\_CNFG  
 UPPER\_THRESHOLD\_2\_CNFG UPPER\_THRESHOLD\_3\_CNFG  
***BF\_UPPER\_THRESHOLD\_DATA\_MASK***  
***BF\_UPPER\_THRESHOLD\_DATA\_LSB***  
***BF\_LOWER\_THRESHOLD\_DATA\_SIZE*** LOWER\_THRESHOLD\_0\_CNFG LOWER\_THRESHOLD\_1\_CN-  
 FG LOWER\_THRESHOLD\_2\_CNFG LOWER\_THRESHOLD\_3\_CNFG  
***BF\_LOWER\_THRESHOLD\_DATA\_MASK***  
***BF\_LOWER\_THRESHOLD\_DATA\_LSB***



***BF\_BUCKET\_SIZE\_DATA\_SIZE*** BUCKET\_SIZE\_0\_CNFG BUCKET\_SIZE\_1\_CNFG BUCKET\_SIZE\_2\_CNFG BUCKET\_SIZE\_3\_CNFG  
***BF\_BUCKET\_SIZE\_DATA\_MASK***  
***BF\_BUCKET\_SIZE\_DATA\_LSB***  
***BF\_DECAY\_RATE\_DATA\_SIZE*** DECAY\_RATE\_0\_CNFG DECAY\_RATE\_1\_CNFG DECAY\_RATE\_2\_CNFG DECAY\_RATE\_3\_CNFG  
***BF\_DECAY\_RATE\_DATA\_MASK***  
***BF\_DECAY\_RATE\_DATA\_LSB***  
***BF\_IN\_FREQ\_READ\_CH\_SIZE*** IN\_FREQ\_READ\_CH\_CNFG  
***BF\_IN\_FREQ\_READ\_CH\_MASK***  
***BF\_IN\_FREQ\_READ\_CH\_LSB***  
***BF\_IN\_FREQ\_VALUE\_SIZE*** IN\_FREQ\_READ\_STS  
***BF\_IN\_FREQ\_VALUE\_MASK***  
***BF\_IN\_FREQ\_VALUE\_LSB***  
***BF\_IN2\_FREQ\_SOFT\_ALARM\_SIZE*** IN1\_IN2\_STS  
***BF\_IN2\_FREQ\_SOFT\_ALARM\_MASK***  
***BF\_IN2\_FREQ\_SOFT\_ALARM\_LSB***  
***BF\_IN2\_FREQ\_HARD\_ALARM\_SIZE*** IN1\_IN2\_STS  
***BF\_IN2\_FREQ\_HARD\_ALARM\_MASK***  
***BF\_IN2\_FREQ\_HARD\_ALARM\_LSB***  
***BF\_IN2\_NO\_ACTIVITY\_ALARM\_SIZE*** IN1\_IN2\_STS  
***BF\_IN2\_NO\_ACTIVITY\_ALARM\_MASK***  
***BF\_IN2\_NO\_ACTIVITY\_ALARM\_LSB***  
***BF\_IN2\_PH\_LOCK\_ALARM\_SIZE*** IN1\_IN2\_STS  
***BF\_IN2\_PH\_LOCK\_ALARM\_MASK***  
***BF\_IN2\_PH\_LOCK\_ALARM\_LSB***  
***BF\_IN1\_FREQ\_SOFT\_ALARM\_SIZE*** IN1\_IN2\_STS  
***BF\_IN1\_FREQ\_SOFT\_ALARM\_MASK***  
***BF\_IN1\_FREQ\_SOFT\_ALARM\_LSB***  
***BF\_IN1\_FREQ\_HARD\_ALARM\_SIZE*** IN1\_IN2\_STS  
***BF\_IN1\_FREQ\_HARD\_ALARM\_MASK***  
***BF\_IN1\_FREQ\_HARD\_ALARM\_LSB***  
***BF\_IN1\_NO\_ACTIVITY\_ALARM\_SIZE*** IN1\_IN2\_STS  
***BF\_IN1\_NO\_ACTIVITY\_ALARM\_MASK***  
***BF\_IN1\_NO\_ACTIVITY\_ALARM\_LSB***  
***BF\_IN1\_PH\_LOCK\_ALARM\_SIZE*** IN1\_IN2\_STS  
***BF\_IN1\_PH\_LOCK\_ALARM\_MASK***  
***BF\_IN1\_PH\_LOCK\_ALARM\_LSB***  
***BF\_IN4\_FREQ\_SOFT\_ALARM\_SIZE*** IN3\_IN4\_STS  
***BF\_IN4\_FREQ\_SOFT\_ALARM\_MASK***  
***BF\_IN4\_FREQ\_SOFT\_ALARM\_LSB***  
***BF\_IN4\_FREQ\_HARD\_ALARM\_SIZE*** IN3\_IN4\_STS  
***BF\_IN4\_FREQ\_HARD\_ALARM\_MASK***  
***BF\_IN4\_FREQ\_HARD\_ALARM\_LSB***  
***BF\_IN4\_NO\_ACTIVITY\_ALARM\_SIZE*** IN3\_IN4\_STS

**BF\_IN4\_NO\_ACTIVITY\_ALARM\_MASK**  
**BF\_IN4\_NO\_ACTIVITY\_ALARM\_LSB**  
**BF\_IN4\_PH\_LOCK\_ALARM\_SIZE** IN3\_IN4\_STS  
**BF\_IN4\_PH\_LOCK\_ALARM\_MASK**  
**BF\_IN4\_PH\_LOCK\_ALARM\_LSB**  
**BF\_IN3\_FREQ\_SOFT\_ALARM\_SIZE** IN3\_IN4\_STS  
**BF\_IN3\_FREQ\_SOFT\_ALARM\_MASK**  
**BF\_IN3\_FREQ\_SOFT\_ALARM\_LSB**  
**BF\_IN3\_FREQ\_HARD\_ALARM\_SIZE** IN3\_IN4\_STS  
**BF\_IN3\_FREQ\_HARD\_ALARM\_MASK**  
**BF\_IN3\_FREQ\_HARD\_ALARM\_LSB**  
**BF\_IN3\_NO\_ACTIVITY\_ALARM\_SIZE** IN3\_IN4\_STS  
**BF\_IN3\_NO\_ACTIVITY\_ALARM\_MASK**  
**BF\_IN3\_NO\_ACTIVITY\_ALARM\_LSB**  
**BF\_IN3\_PH\_LOCK\_ALARM\_SIZE** IN3\_IN4\_STS  
**BF\_IN3\_PH\_LOCK\_ALARM\_MASK**  
**BF\_IN3\_PH\_LOCK\_ALARM\_LSB**  
**BF\_IN6\_FREQ\_SOFT\_ALARM\_SIZE** IN5\_IN6\_STS  
**BF\_IN6\_FREQ\_SOFT\_ALARM\_MASK**  
**BF\_IN6\_FREQ\_SOFT\_ALARM\_LSB**  
**BF\_IN6\_FREQ\_HARD\_ALARM\_SIZE** IN5\_IN6\_STS  
**BF\_IN6\_FREQ\_HARD\_ALARM\_MASK**  
**BF\_IN6\_FREQ\_HARD\_ALARM\_LSB**  
**BF\_IN6\_NO\_ACTIVITY\_ALARM\_SIZE** IN5\_IN6\_STS  
**BF\_IN6\_NO\_ACTIVITY\_ALARM\_MASK**  
**BF\_IN6\_NO\_ACTIVITY\_ALARM\_LSB**  
**BF\_IN6\_PH\_LOCK\_ALARM\_SIZE** IN5\_IN6\_STS  
**BF\_IN6\_PH\_LOCK\_ALARM\_MASK**  
**BF\_IN6\_PH\_LOCK\_ALARM\_LSB**  
**BF\_IN5\_FREQ\_SOFT\_ALARM\_SIZE** IN5\_IN6\_STS  
**BF\_IN5\_FREQ\_SOFT\_ALARM\_MASK**  
**BF\_IN5\_FREQ\_SOFT\_ALARM\_LSB**  
**BF\_IN5\_FREQ\_HARD\_ALARM\_SIZE** IN5\_IN6\_STS  
**BF\_IN5\_FREQ\_HARD\_ALARM\_MASK**  
**BF\_IN5\_FREQ\_HARD\_ALARM\_LSB**  
**BF\_IN5\_NO\_ACTIVITY\_ALARM\_SIZE** IN5\_IN6\_STS  
**BF\_IN5\_NO\_ACTIVITY\_ALARM\_MASK**  
**BF\_IN5\_NO\_ACTIVITY\_ALARM\_LSB**  
**BF\_IN5\_PH\_LOCK\_ALARM\_SIZE** IN5\_IN6\_STS  
**BF\_IN5\_PH\_LOCK\_ALARM\_MASK**  
**BF\_IN5\_PH\_LOCK\_ALARM\_LSB**  
**BF\_IN8\_FREQ\_SOFT\_ALARM\_SIZE** IN7\_IN8\_STS  
**BF\_IN8\_FREQ\_SOFT\_ALARM\_MASK**  
**BF\_IN8\_FREQ\_SOFT\_ALARM\_LSB**  
**BF\_IN8\_FREQ\_HARD\_ALARM\_SIZE** IN7\_IN8\_STS

***BF\_IN8\_FREQ\_HARD\_ALARM\_MASK***  
***BF\_IN8\_FREQ\_HARD\_ALARM\_LSB***  
***BF\_IN8\_NO\_ACTIVITY\_ALARM\_SIZE*** IN7\_IN8\_STS  
***BF\_IN8\_NO\_ACTIVITY\_ALARM\_MASK***  
***BF\_IN8\_NO\_ACTIVITY\_ALARM\_LSB***  
***BF\_IN8\_PH\_LOCK\_ALARM\_SIZE*** IN7\_IN8\_STS  
***BF\_IN8\_PH\_LOCK\_ALARM\_MASK***  
***BF\_IN8\_PH\_LOCK\_ALARM\_LSB***  
***BF\_IN7\_FREQ\_SOFT\_ALARM\_SIZE*** IN7\_IN8\_STS  
***BF\_IN7\_FREQ\_SOFT\_ALARM\_MASK***  
***BF\_IN7\_FREQ\_SOFT\_ALARM\_LSB***  
***BF\_IN7\_FREQ\_HARD\_ALARM\_SIZE*** IN7\_IN8\_STS  
***BF\_IN7\_FREQ\_HARD\_ALARM\_MASK***  
***BF\_IN7\_FREQ\_HARD\_ALARM\_LSB***  
***BF\_IN7\_NO\_ACTIVITY\_ALARM\_SIZE*** IN7\_IN8\_STS  
***BF\_IN7\_NO\_ACTIVITY\_ALARM\_MASK***  
***BF\_IN7\_NO\_ACTIVITY\_ALARM\_LSB***  
***BF\_IN7\_PH\_LOCK\_ALARM\_SIZE*** IN7\_IN8\_STS  
***BF\_IN7\_PH\_LOCK\_ALARM\_MASK***  
***BF\_IN7\_PH\_LOCK\_ALARM\_LSB***  
***BF\_IN10\_FREQ\_SOFT\_ALARM\_SIZE*** IN9\_IN10\_STS  
***BF\_IN10\_FREQ\_SOFT\_ALARM\_MASK***  
***BF\_IN10\_FREQ\_SOFT\_ALARM\_LSB***  
***BF\_IN10\_FREQ\_HARD\_ALARM\_SIZE*** IN9\_IN10\_STS  
***BF\_IN10\_FREQ\_HARD\_ALARM\_MASK***  
***BF\_IN10\_FREQ\_HARD\_ALARM\_LSB***  
***BF\_IN10\_NO\_ACTIVITY\_ALARM\_SIZE*** IN9\_IN10\_STS  
***BF\_IN10\_NO\_ACTIVITY\_ALARM\_MASK***  
***BF\_IN10\_NO\_ACTIVITY\_ALARM\_LSB***  
***BF\_IN10\_PH\_LOCK\_ALARM\_SIZE*** IN9\_IN10\_STS  
***BF\_IN10\_PH\_LOCK\_ALARM\_MASK***  
***BF\_IN10\_PH\_LOCK\_ALARM\_LSB***  
***BF\_IN9\_FREQ\_SOFT\_ALARM\_SIZE*** IN9\_IN10\_STS  
***BF\_IN9\_FREQ\_SOFT\_ALARM\_MASK***  
***BF\_IN9\_FREQ\_SOFT\_ALARM\_LSB***  
***BF\_IN9\_FREQ\_HARD\_ALARM\_SIZE*** IN9\_IN10\_STS  
***BF\_IN9\_FREQ\_HARD\_ALARM\_MASK***  
***BF\_IN9\_FREQ\_HARD\_ALARM\_LSB***  
***BF\_IN9\_NO\_ACTIVITY\_ALARM\_SIZE*** IN9\_IN10\_STS  
***BF\_IN9\_NO\_ACTIVITY\_ALARM\_MASK***  
***BF\_IN9\_NO\_ACTIVITY\_ALARM\_LSB***  
***BF\_IN9\_PH\_LOCK\_ALARM\_SIZE*** IN9\_IN10\_STS  
***BF\_IN9\_PH\_LOCK\_ALARM\_MASK***  
***BF\_IN9\_PH\_LOCK\_ALARM\_LSB***  
***BF\_IN12\_FREQ\_SOFT\_ALARM\_SIZE*** IN11\_IN12\_STS

***BF\_IN12\_FREQ\_SOFT\_ALARM\_MASK***  
***BF\_IN12\_FREQ\_SOFT\_ALARM\_LSB***  
***BF\_IN12\_FREQ\_HARD\_ALARM\_SIZE*** IN11\_IN12\_STS  
***BF\_IN12\_FREQ\_HARD\_ALARM\_MASK***  
***BF\_IN12\_FREQ\_HARD\_ALARM\_LSB***  
***BF\_IN12\_NO\_ACTIVITY\_ALARM\_SIZE*** IN11\_IN12\_STS  
***BF\_IN12\_NO\_ACTIVITY\_ALARM\_MASK***  
***BF\_IN12\_NO\_ACTIVITY\_ALARM\_LSB***  
***BF\_IN12\_PH\_LOCK\_ALARM\_SIZE*** IN11\_IN12\_STS  
***BF\_IN12\_PH\_LOCK\_ALARM\_MASK***  
***BF\_IN12\_PH\_LOCK\_ALARM\_LSB***  
***BF\_IN11\_FREQ\_SOFT\_ALARM\_SIZE*** IN11\_IN12\_STS  
***BF\_IN11\_FREQ\_SOFT\_ALARM\_MASK***  
***BF\_IN11\_FREQ\_SOFT\_ALARM\_LSB***  
***BF\_IN11\_FREQ\_HARD\_ALARM\_SIZE*** IN11\_IN12\_STS  
***BF\_IN11\_FREQ\_HARD\_ALARM\_MASK***  
***BF\_IN11\_FREQ\_HARD\_ALARM\_LSB***  
***BF\_IN11\_NO\_ACTIVITY\_ALARM\_SIZE*** IN11\_IN12\_STS  
***BF\_IN11\_NO\_ACTIVITY\_ALARM\_MASK***  
***BF\_IN11\_NO\_ACTIVITY\_ALARM\_LSB***  
***BF\_IN11\_PH\_LOCK\_ALARM\_SIZE*** IN11\_IN12\_STS  
***BF\_IN11\_PH\_LOCK\_ALARM\_MASK***  
***BF\_IN11\_PH\_LOCK\_ALARM\_LSB***  
***BF\_IN14\_FREQ\_SOFT\_ALARM\_SIZE*** IN13\_IN14\_STS  
***BF\_IN14\_FREQ\_SOFT\_ALARM\_MASK***  
***BF\_IN14\_FREQ\_SOFT\_ALARM\_LSB***  
***BF\_IN14\_FREQ\_HARD\_ALARM\_SIZE*** IN13\_IN14\_STS  
***BF\_IN14\_FREQ\_HARD\_ALARM\_MASK***  
***BF\_IN14\_FREQ\_HARD\_ALARM\_LSB***  
***BF\_IN14\_NO\_ACTIVITY\_ALARM\_SIZE*** IN13\_IN14\_STS  
***BF\_IN14\_NO\_ACTIVITY\_ALARM\_MASK***  
***BF\_IN14\_NO\_ACTIVITY\_ALARM\_LSB***  
***BF\_IN14\_PH\_LOCK\_ALARM\_SIZE*** IN13\_IN14\_STS  
***BF\_IN14\_PH\_LOCK\_ALARM\_MASK***  
***BF\_IN14\_PH\_LOCK\_ALARM\_LSB***  
***BF\_IN13\_FREQ\_SOFT\_ALARM\_SIZE*** IN13\_IN14\_STS  
***BF\_IN13\_FREQ\_SOFT\_ALARM\_MASK***  
***BF\_IN13\_FREQ\_SOFT\_ALARM\_LSB***  
***BF\_IN13\_FREQ\_HARD\_ALARM\_SIZE*** IN13\_IN14\_STS  
***BF\_IN13\_FREQ\_HARD\_ALARM\_MASK***  
***BF\_IN13\_FREQ\_HARD\_ALARM\_LSB***  
***BF\_IN13\_NO\_ACTIVITY\_ALARM\_SIZE*** IN13\_IN14\_STS  
***BF\_IN13\_NO\_ACTIVITY\_ALARM\_MASK***  
***BF\_IN13\_NO\_ACTIVITY\_ALARM\_LSB***  
***BF\_IN13\_PH\_LOCK\_ALARM\_SIZE*** IN13\_IN14\_STS

**BF\_IN13\_PH\_LOCK\_ALARM\_MASK**  
**BF\_IN13\_PH\_LOCK\_ALARM\_LSB**  
**BF\_HIGHEST\_PRIORITY\_VALIDATED\_SIZE** PRIORITY\_TABLE1\_STS  
**BF\_HIGHEST\_PRIORITY\_VALIDATED\_MASK**  
**BF\_HIGHEST\_PRIORITY\_VALIDATED\_LSB**  
**BF\_CURRENTLY\_SELECTED\_INPUTS\_SIZE** PRIORITY\_TABLE1\_STS  
**BF\_CURRENTLY\_SELECTED\_INPUTS\_MASK**  
**BF\_CURRENTLY\_SELECTED\_INPUTS\_LSB**  
**BF\_THIRD\_HIGHEST\_PRIORITY\_VALIDATED\_SIZE** PRIORITY\_TABLE2\_STS  
**BF\_THIRD\_HIGHEST\_PRIORITY\_VALIDATED\_MASK**  
**BF\_THIRD\_HIGHEST\_PRIORITY\_VALIDATED\_LSB**  
**BF\_SECOND\_HIGHEST\_PRIORITY\_VALIDATED\_SIZE** PRIORITY\_TABLE2\_STS  
**BF\_SECOND\_HIGHEST\_PRIORITY\_VALIDATED\_MASK**  
**BF\_SECOND\_HIGHEST\_PRIORITY\_VALIDATED\_LSB**  
**BF\_T0\_INPUT\_SEL\_SIZE** T0\_INPUT\_SEL\_CNFG  
**BF\_T0\_INPUT\_SEL\_MASK**  
**BF\_T0\_INPUT\_SEL\_LSB**  
**BF\_T4\_LOCK\_T0\_SIZE** T4\_INPUT\_SEL\_CNFG  
**BF\_T4\_LOCK\_T0\_MASK**  
**BF\_T4\_LOCK\_T0\_LSB**  
**BF\_T0\_FOR\_T4\_SIZE** T4\_INPUT\_SEL\_CNFG  
**BF\_T0\_FOR\_T4\_MASK**  
**BF\_T0\_FOR\_T4\_LSB**  
**BF\_T4\_TEST\_T0\_PH\_SIZE** T4\_INPUT\_SEL\_CNFG  
**BF\_T4\_TEST\_T0\_PH\_MASK**  
**BF\_T4\_TEST\_T0\_PH\_LSB**  
**BF\_T4\_INPUT\_SEL\_SIZE** T4\_INPUT\_SEL\_CNFG  
**BF\_T4\_INPUT\_SEL\_MASK**  
**BF\_T4\_INPUT\_SEL\_LSB**  
**BF\_EX\_SYNC\_ALARM\_MON\_SIZE** OPERATING\_STS  
**BF\_EX\_SYNC\_ALARM\_MON\_MASK**  
**BF\_EX\_SYNC\_ALARM\_MON\_LSB**  
**BF\_T4\_DPLL\_LOCK\_SIZE** OPERATING\_STS  
**BF\_T4\_DPLL\_LOCK\_MASK**  
**BF\_T4\_DPLL\_LOCK\_LSB**  
**BF\_T0\_DPLL\_SOFT\_FREQ\_ALARM\_SIZE** OPERATING\_STS  
**BF\_T0\_DPLL\_SOFT\_FREQ\_ALARM\_MASK**  
**BF\_T0\_DPLL\_SOFT\_FREQ\_ALARM\_LSB**  
**BF\_T4\_DPLL\_SOFT\_FREQ\_ALARM\_SIZE** OPERATING\_STS  
**BF\_T4\_DPLL\_SOFT\_FREQ\_ALARM\_MASK**  
**BF\_T4\_DPLL\_SOFT\_FREQ\_ALARM\_LSB**  
**BF\_T0\_DPLL\_LOCK\_SIZE** OPERATING\_STS  
**BF\_T0\_DPLL\_LOCK\_MASK**  
**BF\_T0\_DPLL\_LOCK\_LSB**  
**BF\_T0\_DPLL\_OPERATING\_MODE\_SIZE** OPERATING\_STS

***BF\_T0\_DPLL\_OPERATING\_MODE\_MASK***  
***BF\_T0\_DPLL\_OPERATING\_MODE\_LSB***  
***BF\_T0\_WDCO\_SIZE*** T0\_OPERATION\_MODE\_CNFG  
***BF\_T0\_WDCO\_MASK***  
***BF\_T0\_WDCO\_LSB***  
***BF\_T0\_OPERATING\_MODE\_SIZE*** T0\_OPERATION\_MODE\_CNFG  
***BF\_T0\_OPERATING\_MODE\_MASK***  
***BF\_T0\_OPERATING\_MODE\_LSB***  
***BF\_T4\_WDCO\_SIZE*** T4\_OPERATION\_MODE\_CNFG  
***BF\_T4\_WDCO\_MASK***  
***BF\_T4\_WDCO\_LSB***  
***BF\_T4\_OPERATING\_MODE\_SIZE*** T4\_OPERATION\_MODE\_CNFG  
***BF\_T4\_OPERATING\_MODE\_MASK***  
***BF\_T4\_OPERATING\_MODE\_LSB***  
***BF\_T0\_APLL\_PATH\_SIZE*** T0\_DPLL\_APLL\_PATH\_CNFG  
***BF\_T0\_APLL\_PATH\_MASK***  
***BF\_T0\_APLL\_PATH\_LSB***  
***BF\_T0\_GSM\_OBSAI\_16E1\_16T1\_SEL\_SIZE*** T0\_DPLL\_APLL\_PATH\_CNFG  
***BF\_T0\_GSM\_OBSAI\_16E1\_16T1\_SEL\_MASK***  
***BF\_T0\_GSM\_OBSAI\_16E1\_16T1\_SEL\_LSB***  
***BF\_T0\_12E1\_GPS\_E3\_T3\_SEL\_SIZE*** T0\_DPLL\_APLL\_PATH\_CNFG  
***BF\_T0\_12E1\_GPS\_E3\_T3\_SEL\_MASK***  
***BF\_T0\_12E1\_GPS\_E3\_T3\_SEL\_LSB***  
***BF\_T0\_DPLL\_START\_DAMPING\_SIZE*** T0\_DPLL\_START\_BW\_DAMPING\_CNFG  
***BF\_T0\_DPLL\_START\_DAMPING\_MASK***  
***BF\_T0\_DPLL\_START\_DAMPING\_LSB***  
***BF\_T0\_DPLL\_START\_BW\_SIZE*** T0\_DPLL\_START\_BW\_DAMPING\_CNFG  
***BF\_T0\_DPLL\_START\_BW\_MASK***  
***BF\_T0\_DPLL\_START\_BW\_LSB***  
***BF\_T0\_DPLL\_ACQ\_DAMPING\_SIZE*** T0\_DPLL\_ACQ\_BW\_DAMPING\_CNFG  
***BF\_T0\_DPLL\_ACQ\_DAMPING\_MASK***  
***BF\_T0\_DPLL\_ACQ\_DAMPING\_LSB***  
***BF\_T0\_DPLL\_ACQ\_BW\_SIZE*** T0\_DPLL\_ACQ\_BW\_DAMPING\_CNFG  
***BF\_T0\_DPLL\_ACQ\_BW\_MASK***  
***BF\_T0\_DPLL\_ACQ\_BW\_LSB***  
***BF\_T0\_DPLL\_LOCKED\_DAMPING\_SIZE*** T0\_DPLL\_LOCKED\_BW\_DAMPING\_CNFG  
***BF\_T0\_DPLL\_LOCKED\_DAMPING\_MASK***  
***BF\_T0\_DPLL\_LOCKED\_DAMPING\_LSB***  
***BF\_T0\_DPLL\_LOCKED\_BW\_SIZE*** T0\_DPLL\_LOCKED\_BW\_DAMPING\_CNFG  
***BF\_T0\_DPLL\_LOCKED\_BW\_MASK***  
***BF\_T0\_DPLL\_LOCKED\_BW\_LSB***  
***BF\_AUTO\_BW\_SEL\_SIZE*** T0\_BW\_OVERSHOOT\_CNFG  
***BF\_AUTO\_BW\_SEL\_MASK***  
***BF\_AUTO\_BW\_SEL\_LSB***  
***BF\_T0\_LIMIT\_SIZE*** T0\_BW\_OVERSHOOT\_CNFG

***BF\_T0\_LIMIT\_MASK***  
***BF\_T0\_LIMIT\_LSB***  
***BF\_COARSE\_PH\_LOS\_LIMT\_EN\_SIZE*** PHASE\_LOSS\_COARSE\_LIMIT\_CNFG  
***BF\_COARSE\_PH\_LOS\_LIMT\_EN\_MASK***  
***BF\_COARSE\_PH\_LOS\_LIMT\_EN\_LSB***  
***BF\_WIDE\_EN\_SIZE*** PHASE\_LOSS\_COARSE\_LIMIT\_CNFG  
***BF\_WIDE\_EN\_MASK***  
***BF\_WIDE\_EN\_LSB***  
***BF\_MULTI\_PH\_APP\_SIZE*** PHASE\_LOSS\_COARSE\_LIMIT\_CNFG  
***BF\_MULTI\_PH\_APP\_MASK***  
***BF\_MULTI\_PH\_APP\_LSB***  
***BF\_MULTI\_PH\_8K\_4K\_2K\_EN\_SIZE*** PHASE\_LOSS\_COARSE\_LIMIT\_CNFG  
***BF\_MULTI\_PH\_8K\_4K\_2K\_EN\_MASK***  
***BF\_MULTI\_PH\_8K\_4K\_2K\_EN\_LSB***  
***BF\_PH\_LOS\_COARSE\_LIMT\_SIZE*** PHASE\_LOSS\_COARSE\_LIMIT\_CNFG  
***BF\_PH\_LOS\_COARSE\_LIMT\_MASK***  
***BF\_PH\_LOS\_COARSE\_LIMT\_LSB***  
***BF\_FINE\_PH\_LOS\_LIMT\_EN\_SIZE*** PHASE\_LOSS\_FINE\_LIMIT\_CNFG  
***BF\_FINE\_PH\_LOS\_LIMT\_EN\_MASK***  
***BF\_FINE\_PH\_LOS\_LIMT\_EN\_LSB***  
***BF\_FAST\_LOS\_SW\_SIZE*** PHASE\_LOSS\_FINE\_LIMIT\_CNFG  
***BF\_FAST\_LOS\_SW\_MASK***  
***BF\_FAST\_LOS\_SW\_LSB***  
***BF\_PH\_LOS\_FINE\_LIMT\_SIZE*** PHASE\_LOSS\_FINE\_LIMIT\_CNFG  
***BF\_PH\_LOS\_FINE\_LIMT\_MASK***  
***BF\_PH\_LOS\_FINE\_LIMT\_LSB***  
***BF\_MAN\_HOLDOVER\_SIZE*** T0\_HOLDOVER\_MODE\_CNFG  
***BF\_MAN\_HOLDOVER\_MASK***  
***BF\_MAN\_HOLDOVER\_LSB***  
***BF\_AUTO\_AVG\_SIZE*** T0\_HOLDOVER\_MODE\_CNFG  
***BF\_AUTO\_AVG\_MASK***  
***BF\_AUTO\_AVG\_LSB***  
***BF\_FAST\_AVG\_SIZE*** T0\_HOLDOVER\_MODE\_CNFG  
***BF\_FAST\_AVG\_MASK***  
***BF\_FAST\_AVG\_LSB***  
***BF\_READ\_AVG\_SIZE*** T0\_HOLDOVER\_MODE\_CNFG  
***BF\_READ\_AVG\_MASK***  
***BF\_READ\_AVG\_LSB***  
***BF\_TEMP\_HOLDOVER\_MODE\_SIZE*** T0\_HOLDOVER\_MODE\_CNFG  
***BF\_TEMP\_HOLDOVER\_MODE\_MASK***  
***BF\_TEMP\_HOLDOVER\_MODE\_LSB***  
***BF\_HOLDOVER\_FREQ\_A\_SIZE*** HOLDOVER\_FREQ\_LOW\_CNFG  
***BF\_HOLDOVER\_FREQ\_A\_MASK***  
***BF\_HOLDOVER\_FREQ\_A\_LSB***  
***BF\_HOLDOVER\_FREQ\_B\_SIZE*** HOLDOVER\_FREQ\_MID\_CNFG

**BF\_HOLDOVER\_FREQ\_B\_MASK**  
**BF\_HOLDOVER\_FREQ\_B\_LSB**  
**BF\_HOLDOVER\_FREQ\_C\_SIZE** HOLDOVER\_FREQ\_HIGH\_CNFG  
**BF\_HOLDOVER\_FREQ\_C\_MASK**  
**BF\_HOLDOVER\_FREQ\_C\_LSB**  
**BF\_T4\_APLL\_PATH\_SIZE** T4\_DPLL\_APLL\_PATH\_CNFG  
**BF\_T4\_APLL\_PATH\_MASK**  
**BF\_T4\_APLL\_PATH\_LSB**  
**BF\_T4\_GSM\_OBSAI\_16E1\_16T1\_SEL\_SIZE** T4\_DPLL\_APLL\_PATH\_CNFG  
**BF\_T4\_GSM\_OBSAI\_16E1\_16T1\_SEL\_MASK**  
**BF\_T4\_GSM\_OBSAI\_16E1\_16T1\_SEL\_LSB**  
**BF\_T4\_12E1\_GPS\_E3\_T3\_SEL\_SIZE** T4\_DPLL\_APLL\_PATH\_CNFG  
**BF\_T4\_12E1\_GPS\_E3\_T3\_SEL\_MASK**  
**BF\_T4\_12E1\_GPS\_E3\_T3\_SEL\_LSB**  
**BF\_T4\_DPLL\_LOCKED\_DAMPING\_SIZE** T4\_DPLL\_LOCKED\_BW\_DAMPING\_CNFG  
**BF\_T4\_DPLL\_LOCKED\_DAMPING\_MASK**  
**BF\_T4\_DPLL\_LOCKED\_DAMPING\_LSB**  
**BF\_T4\_DPLL\_LOCKED\_BW\_SIZE** T4\_DPLL\_LOCKED\_BW\_DAMPING\_CNFG  
**BF\_T4\_DPLL\_LOCKED\_BW\_MASK**  
**BF\_T4\_DPLL\_LOCKED\_BW\_LSB**  
**BF\_CURRENT\_DPLL\_FREQ\_A\_SIZE** CURRENT\_FREQ\_LOW\_STS  
**BF\_CURRENT\_DPLL\_FREQ\_A\_MASK**  
**BF\_CURRENT\_DPLL\_FREQ\_A\_LSB**  
**BF\_CURRENT\_DPLL\_FREQ\_B\_SIZE** CURRENT\_FREQ\_MID\_STS  
**BF\_CURRENT\_DPLL\_FREQ\_B\_MASK**  
**BF\_CURRENT\_DPLL\_FREQ\_B\_LSB**  
**BF\_CURRENT\_DPLL\_FREQ\_C\_SIZE** CURRENT\_FREQ\_HIGH\_STS  
**BF\_CURRENT\_DPLL\_FREQ\_C\_MASK**  
**BF\_CURRENT\_DPLL\_FREQ\_C\_LSB**  
**BF\_FREQ\_LIMT\_PH\_LOS\_SIZE** DPLL\_FREQ\_SOFT\_LIMIT\_CNFG  
**BF\_FREQ\_LIMT\_PH\_LOS\_MASK**  
**BF\_FREQ\_LIMT\_PH\_LOS\_LSB**  
**BF\_DPLL\_FREQ\_SOFT\_LIMT\_SIZE** DPLL\_FREQ\_SOFT\_LIMIT\_CNFG  
**BF\_DPLL\_FREQ\_SOFT\_LIMT\_MASK**  
**BF\_DPLL\_FREQ\_SOFT\_LIMT\_LSB**  
**BF\_DPLL\_FREQ\_HARD\_LIMT\_A\_SIZE** DPLL\_FREQ\_HARD\_LIMIT\_LOW\_CNFG  
**BF\_DPLL\_FREQ\_HARD\_LIMT\_A\_MASK**  
**BF\_DPLL\_FREQ\_HARD\_LIMT\_A\_LSB**  
**BF\_DPLL\_FREQ\_HARD\_LIMT\_B\_SIZE** DPLL\_FREQ\_HARD\_LIMIT\_MID\_CNFG  
**BF\_DPLL\_FREQ\_HARD\_LIMT\_B\_MASK**  
**BF\_DPLL\_FREQ\_HARD\_LIMT\_B\_LSB**  
**BF\_CURRENT\_PH\_DATA\_A\_SIZE** CURRENT\_DPLL\_PHASE\_LOW\_STS  
**BF\_CURRENT\_PH\_DATA\_A\_MASK**  
**BF\_CURRENT\_PH\_DATA\_A\_LSB**  
**BF\_CURRENT\_PH\_DATA\_B\_SIZE** CURRENT\_DPLL\_PHASE\_HIGH\_STS



***BF\_CURRENT\_PH\_DATA\_B\_MASK***  
***BF\_CURRENT\_PH\_DATA\_B\_LSB***  
***BF\_OUT1\_PATH\_SEL\_SIZE*** OUT1\_FREQ\_CNFG  
***BF\_OUT1\_PATH\_SEL\_MASK***  
***BF\_OUT1\_PATH\_SEL\_LSB***  
***BF\_OUT1\_DIVIDER\_SIZE*** OUT1\_FREQ\_CNFG  
***BF\_OUT1\_DIVIDER\_MASK***  
***BF\_OUT1\_DIVIDER\_LSB***  
***BF\_OUT2\_PATH\_SEL\_SIZE*** OUT2\_FREQ\_CNFG  
***BF\_OUT2\_PATH\_SEL\_MASK***  
***BF\_OUT2\_PATH\_SEL\_LSB***  
***BF\_OUT2\_DIVIDER\_SIZE*** OUT2\_FREQ\_CNFG  
***BF\_OUT2\_DIVIDER\_MASK***  
***BF\_OUT2\_DIVIDER\_LSB***  
***BF\_OUT3\_PATH\_SEL\_SIZE*** OUT3\_FREQ\_CNFG  
***BF\_OUT3\_PATH\_SEL\_MASK***  
***BF\_OUT3\_PATH\_SEL\_LSB***  
***BF\_OUT3\_DIVIDER\_SIZE*** OUT3\_FREQ\_CNFG  
***BF\_OUT3\_DIVIDER\_MASK***  
***BF\_OUT3\_DIVIDER\_LSB***  
***BF\_OUT4\_PATH\_SEL\_SIZE*** OUT4\_FREQ\_CNFG  
***BF\_OUT4\_PATH\_SEL\_MASK***  
***BF\_OUT4\_PATH\_SEL\_LSB***  
***BF\_OUT4\_DIVIDER\_SIZE*** OUT4\_FREQ\_CNFG  
***BF\_OUT4\_DIVIDER\_MASK***  
***BF\_OUT4\_DIVIDER\_LSB***  
***BF\_OUT5\_PATH\_SEL\_SIZE*** OUT5\_FREQ\_CNFG  
***BF\_OUT5\_PATH\_SEL\_MASK***  
***BF\_OUT5\_PATH\_SEL\_LSB***  
***BF\_OUT5\_DIVIDER\_SIZE*** OUT5\_FREQ\_CNFG  
***BF\_OUT5\_DIVIDER\_MASK***  
***BF\_OUT5\_DIVIDER\_LSB***  
***BF\_OUT6\_PATH\_SEL\_SIZE*** OUT6\_FREQ\_CNFG  
***BF\_OUT6\_PATH\_SEL\_MASK***  
***BF\_OUT6\_PATH\_SEL\_LSB***  
***BF\_OUT6\_DIVIDER\_SIZE*** OUT6\_FREQ\_CNFG  
***BF\_OUT6\_DIVIDER\_MASK***  
***BF\_OUT6\_DIVIDER\_LSB***  
***BF\_OUT7\_PATH\_SEL\_SIZE*** OUT7\_FREQ\_CNFG  
***BF\_OUT7\_PATH\_SEL\_MASK***  
***BF\_OUT7\_PATH\_SEL\_LSB***  
***BF\_OUT7\_DIVIDER\_SIZE*** OUT7\_FREQ\_CNFG  
***BF\_OUT7\_DIVIDER\_MASK***  
***BF\_OUT7\_DIVIDER\_LSB***  
***BF\_OUT8\_PATH\_SEL\_SIZE*** OUT8\_FREQ\_CNFG

***BF\_OUT8\_PATH\_SEL\_MASK***  
***BF\_OUT8\_PATH\_SEL\_LSB***  
***BF\_OUT8\_EN\_SIZE*** OUT8\_FREQ\_CNFG  
***BF\_OUT8\_EN\_MASK***  
***BF\_OUT8\_EN\_LSB***  
***BF\_T4\_INPUT\_FAIL\_SIZE*** OUT8\_FREQ\_CNFG OUT9\_FREQ\_CNFG  
***BF\_T4\_INPUT\_FAIL\_MASK***  
***BF\_T4\_INPUT\_FAIL\_LSB***  
***BF\_AMI\_OUT\_DUTY\_SIZE*** OUT8\_FREQ\_CNFG  
***BF\_AMI\_OUT\_DUTY\_MASK***  
***BF\_AMI\_OUT\_DUTY\_LSB***  
***BF\_400HZ\_OUT\_SEL\_SIZE*** OUT8\_FREQ\_CNFG  
***BF\_400HZ\_OUT\_SEL\_MASK***  
***BF\_400HZ\_OUT\_SEL\_LSB***  
***BF\_OUT9\_INV\_SIZE*** OUT8\_FREQ\_CNFG  
***BF\_OUT9\_INV\_MASK***  
***BF\_OUT9\_INV\_LSB***  
***BF\_OUT7\_INV\_SIZE*** OUT8\_FREQ\_CNFG  
***BF\_OUT7\_INV\_MASK***  
***BF\_OUT7\_INV\_LSB***  
***BF\_OUT6\_INV\_SIZE*** OUT8\_FREQ\_CNFG  
***BF\_OUT6\_INV\_MASK***  
***BF\_OUT6\_INV\_LSB***  
***BF\_OUT9\_PATH\_SEL\_SIZE*** OUT9\_FREQ\_CNFG  
***BF\_OUT9\_PATH\_SEL\_MASK***  
***BF\_OUT9\_PATH\_SEL\_LSB***  
***BF\_OUT9\_EN\_SIZE*** OUT9\_FREQ\_CNFG  
***BF\_OUT9\_EN\_MASK***  
***BF\_OUT9\_EN\_LSB***  
***BF\_OUT5\_INV\_SIZE*** OUT9\_FREQ\_CNFG  
***BF\_OUT5\_INV\_MASK***  
***BF\_OUT5\_INV\_LSB***  
***BF\_OUT4\_INV\_SIZE*** OUT9\_FREQ\_CNFG  
***BF\_OUT4\_INV\_MASK***  
***BF\_OUT4\_INV\_LSB***  
***BF\_OUT3\_INV\_SIZE*** OUT9\_FREQ\_CNFG  
***BF\_OUT3\_INV\_MASK***  
***BF\_OUT3\_INV\_LSB***  
***BF\_OUT2\_INV\_SIZE*** OUT9\_FREQ\_CNFG  
***BF\_OUT2\_INV\_MASK***  
***BF\_OUT2\_INV\_LSB***  
***BF\_OUT1\_INV\_SIZE*** OUT9\_FREQ\_CNFG  
***BF\_OUT1\_INV\_MASK***  
***BF\_OUT1\_INV\_LSB***  
***BF\_IN\_2K\_4K\_8K\_INV\_SIZE*** FR\_MFR\_SYNC\_CNFG

***BF\_IN\_2K\_4K\_8K\_INV\_MASK***  
***BF\_IN\_2K\_4K\_8K\_INV\_LSB***  
***BF\_8K\_EN\_SIZE*** FR\_MFR\_SYNC\_CNFG  
***BF\_8K\_EN\_MASK***  
***BF\_8K\_EN\_LSB***  
***BF\_2K\_EN\_SIZE*** FR\_MFR\_SYNC\_CNFG  
***BF\_2K\_EN\_MASK***  
***BF\_2K\_EN\_LSB***  
***BF\_2K\_8K\_PUL\_POSITION\_SIZE*** FR\_MFR\_SYNC\_CNFG  
***BF\_2K\_8K\_PUL\_POSITION\_MASK***  
***BF\_2K\_8K\_PUL\_POSITION\_LSB***  
***BF\_8K\_INV\_SIZE*** FR\_MFR\_SYNC\_CNFG  
***BF\_8K\_INV\_MASK***  
***BF\_8K\_INV\_LSB***  
***BF\_8K\_PUL\_SIZE*** FR\_MFR\_SYNC\_CNFG  
***BF\_8K\_PUL\_MASK***  
***BF\_8K\_PUL\_LSB***  
***BF\_2K\_INV\_SIZE*** FR\_MFR\_SYNC\_CNFG  
***BF\_2K\_INV\_MASK***  
***BF\_2K\_INV\_LSB***  
***BF\_2K\_PUL\_SIZE*** FR\_MFR\_SYNC\_CNFG  
***BF\_2K\_PUL\_MASK***  
***BF\_2K\_PUL\_LSB***  
***BF\_IN\_NOISE\_WINDOW\_SIZE*** PHASE\_MON\_CNFG  
***BF\_IN\_NOISE\_WINDOW\_MASK***  
***BF\_IN\_NOISE\_WINDOW\_LSB***  
***BF\_PH\_OFFSET\_A\_SIZE*** PHASE\_OFFSET\_LOW\_CNFG  
***BF\_PH\_OFFSET\_A\_MASK***  
***BF\_PH\_OFFSET\_A\_LSB***  
***BF\_PH\_OFFSET\_EN\_SIZE*** PHASE\_OFFSET\_HIGH\_CNFG  
***BF\_PH\_OFFSET\_EN\_MASK***  
***BF\_PH\_OFFSET\_EN\_LSB***  
***BF\_PH\_OFFSET\_B\_SIZE*** PHASE\_OFFSET\_HIGH\_CNFG  
***BF\_PH\_OFFSET\_B\_MASK***  
***BF\_PH\_OFFSET\_B\_LSB***  
***BF\_SYNC\_BYPASS\_SIZE*** SYNC\_MONITOR\_CNFG  
***BF\_SYNC\_BYPASS\_MASK***  
***BF\_SYNC\_BYPASS\_LSB***  
***BF\_SYNC\_MON\_LIMT\_SIZE*** SYNC\_MONITOR\_CNFG  
***BF\_SYNC\_MON\_LIMT\_MASK***  
***BF\_SYNC\_MON\_LIMT\_LSB***  
***BF\_SYNC\_EDGE\_SIZE*** SYNC\_PHASE\_CNFG  
***BF\_SYNC\_EDGE\_MASK***  
***BF\_SYNC\_EDGE\_LSB***  
***BF\_SYNC\_PH2\_SIZE*** SYNC\_PHASE\_CNFG

***BF\_SYNC\_PH2\_MASK***  
***BF\_SYNC\_PH2\_LSB***  
***BF\_SYNC\_PH1\_SIZE*** SYNC\_PHASE\_CNFG  
***BF\_SYNC\_PH1\_MASK***  
***BF\_SYNC\_PH1\_LSB***  
***BF\_PROTECTION\_DATA\_SIZE*** PROTECTION\_CNFG  
***BF\_PROTECTION\_DATA\_MASK***  
***BF\_PROTECTION\_DATA\_LSB***  
***BF\_MPU\_SEL\_CNFG\_SIZE*** MPU\_SEL\_CNFG  
***BF\_MPU\_SEL\_CNFG\_MASK***  
***BF\_MPU\_SEL\_CNFG\_LSB***  
***BF\_T0\_DFS\_OFF\_3\_SIZE*** DFS\_OFF\_CNFG  
***BF\_T0\_DFS\_OFF\_3\_MASK***  
***BF\_T0\_DFS\_OFF\_3\_LSB***  
***BF\_T0\_DFS\_OFF\_2\_SIZE*** DFS\_OFF\_CNFG  
***BF\_T0\_DFS\_OFF\_2\_MASK***  
***BF\_T0\_DFS\_OFF\_2\_LSB***  
***BF\_T0\_DFS\_OFF\_1\_SIZE*** DFS\_OFF\_CNFG  
***BF\_T0\_DFS\_OFF\_1\_MASK***  
***BF\_T0\_DFS\_OFF\_1\_LSB***  
***BF\_T0\_DFS\_OFF\_0\_SIZE*** DFS\_OFF\_CNFG  
***BF\_T0\_DFS\_OFF\_0\_MASK***  
***BF\_T0\_DFS\_OFF\_0\_LSB***  
***BF\_T4\_DFS\_OFF\_3\_SIZE*** DFS\_OFF\_CNFG  
***BF\_T4\_DFS\_OFF\_3\_MASK***  
***BF\_T4\_DFS\_OFF\_3\_LSB***  
***BF\_T4\_DFS\_OFF\_2\_SIZE*** DFS\_OFF\_CNFG  
***BF\_T4\_DFS\_OFF\_2\_MASK***  
***BF\_T4\_DFS\_OFF\_2\_LSB***  
***BF\_T4\_DFS\_OFF\_1\_SIZE*** DFS\_OFF\_CNFG  
***BF\_T4\_DFS\_OFF\_1\_MASK***  
***BF\_T4\_DFS\_OFF\_1\_LSB***  
***BF\_T4\_DFS\_OFF\_0\_SIZE*** DFS\_OFF\_CNFG  
***BF\_T4\_DFS\_OFF\_0\_MASK***  
***BF\_T4\_DFS\_OFF\_0\_LSB***  
***BF\_PPS\_PHASE\_SIZE*** T0\_PPS\_CNFG T4\_PPS\_CNFG  
***BF\_PPS\_PHASE\_MASK***  
***BF\_PPS\_PHASE\_LSB***  
***BF\_PPS\_PULSE\_SIZE*** T0\_PPS\_CNFG T4\_PPS\_CNFG  
***BF\_PPS\_PULSE\_MASK***  
***BF\_PPS\_PULSE\_LSB***  
***BF\_T0\_PH\_SLOPE\_SIZE*** PH\_SLOPE\_CNFG  
***BF\_T0\_PH\_SLOPE\_MASK***  
***BF\_T0\_PH\_SLOPE\_LSB***  
***BF\_T4\_PH\_SLOPE\_SIZE*** PH\_SLOPE\_CNFG

***BF\_T4\_PH\_SLOPE\_MASK***  
***BF\_T4\_PH\_SLOPE\_LSB***  
***BF\_ICP\_CTRL\_CODE\_SIZE*** T0\_ICP\_CTRL\_CNFG T4\_ICP\_CTRL\_CNFG  
***BF\_ICP\_CTRL\_CODE\_MASK***  
***BF\_ICP\_CTRL\_CODE\_LSB***  
***REGMAP\_MAX***

Definition at line 55 of file RegisterDef.h.

#### 4.7.2.2 anonymous enum

Enumerated type listing register offsets and bit field constants.

##### Enumerator

***REG\_CONTROL*** General Control Register  
***REG\_CLK\_SEL*** Input Clock Select  
***REG\_PDSEL0\_LSB*** Configuration 0 Pre-divider LSB  
***REG\_PDSEL0\_MSB*** Configuration 0 Pre-divider MSB  
***REG\_PDSEL1\_LSB*** Configuration 1 Pre-divider LSB  
***REG\_PDSEL1\_MSB*** Configuration 1 Pre-divider MSB  
***REG\_M0\_LSB*** Configuration 0 Feedback divider LSB  
***REG\_M0\_MSB*** Configuration 0 Feedback divider MSB  
***REG\_M1\_LSB*** Configuration 1 Feedback divider LSB  
***REG\_M1\_MSB*** Configuration 1 Feedback divider MSB  
***REG\_ODBSELA0*** QA Output Divider Config 0  
***REG\_ODBSELA1*** QA Output Divider Config 1  
***REG\_ODBSELB0*** QB Output Divider Config 0  
***REG\_ODBSELB1*** QB Output Divider Config 1  
***REG\_VCXO\_SEL*** VCXO Crystal Select  
***REG\_CONFIG\_QA*** Output Configuration QA  
***REG\_CONFIG\_QB*** Output Configuration QB  
***BF\_CONFIG\_SIZE*** CONTROL  
***BF\_CONFIG\_MASK***  
***BF\_CONFIG\_LSB***  
***BF\_CLK\_SEL\_SIZE*** CLK\_SEL  
***BF\_CLK\_SEL\_MASK***  
***BF\_CLK\_SEL\_LSB***  
***BF\_PDSEL0\_LSB\_SIZE*** PDSEL0\_LSB  
***BF\_PDSEL0\_LSB\_MASK***  
***BF\_PDSEL0\_LSB\_LSB***  
***BF\_PDSEL0\_MSB\_SIZE*** PDSEL0\_MSB  
***BF\_PDSEL0\_MSB\_MASK***  
***BF\_PDSEL0\_MSB\_LSB***  
***BF\_PDSEL1\_LSB\_SIZE*** PDSEL1\_LSB  
***BF\_PDSEL1\_LSB\_MASK***  
***BF\_PDSEL1\_LSB\_LSB***

***BF\_PDSEL1\_MSB\_SIZE*** PDSEL1\_MSB  
***BF\_PDSEL1\_MSB\_MASK***  
***BF\_PDSEL1\_MSB\_LSB***  
***BF\_M0\_LSB\_SIZE*** M0\_LSB  
***BF\_M0\_LSB\_MASK***  
***BF\_M0\_LSB\_LSB***  
***BF\_M0\_MSB\_SIZE*** M0\_MSB  
***BF\_M0\_MSB\_MASK***  
***BF\_M0\_MSB\_LSB***  
***BF\_M1\_LSB\_SIZE*** M1\_LSB  
***BF\_M1\_LSB\_MASK***  
***BF\_M1\_LSB\_LSB***  
***BF\_M1\_MSB\_SIZE*** M1\_MSB  
***BF\_M1\_MSB\_MASK***  
***BF\_M1\_MSB\_LSB***  
***BF\_ODBSELA0\_SIZE*** ODBSELA0  
***BF\_ODBSELA0\_MASK***  
***BF\_ODBSELA0\_LSB***  
***BF\_ODBSELA1\_SIZE*** ODBSELA1  
***BF\_ODBSELA1\_MASK***  
***BF\_ODBSELA1\_LSB***  
***BF\_ODBSELB0\_SIZE*** ODBSELB0  
***BF\_ODBSELB0\_MASK***  
***BF\_ODBSELB0\_LSB***  
***BF\_ODBSELB1\_SIZE*** ODBSELB1  
***BF\_ODBSELB1\_MASK***  
***BF\_ODBSELB1\_LSB***  
***BF\_SEL\_DOUBLE\_SIZE*** VCXO\_SEL  
***BF\_SEL\_DOUBLE\_MASK***  
***BF\_SEL\_DOUBLE\_LSB***  
***BF\_MR\_SYNC\_SIZE*** VCXO\_SEL  
***BF\_MR\_SYNC\_MASK***  
***BF\_MR\_SYNC\_LSB***  
***BF\_BYPASS\_SIZE*** VCXO\_SEL  
***BF\_BYPASS\_MASK***  
***BF\_BYPASS\_LSB***  
***BF\_SHUTOFF\_SIZE*** VCXO\_SEL  
***BF\_SHUTOFF\_MASK***  
***BF\_SHUTOFF\_LSB***  
***BF\_VCXO\_SEL\_SIZE*** VCXO\_SEL  
***BF\_VCXO\_SEL\_MASK***  
***BF\_VCXO\_SEL\_LSB***  
***BF\_LVDS\_QA\_SIZE*** CONFIG\_QA  
***BF\_LVDS\_QA\_MASK***  
***BF\_LVDS\_QA\_LSB***

***BF\_OE\_A\_SIZE*** CONFIG\_QA  
***BF\_OE\_A\_MASK***  
***BF\_OE\_A\_LSB***  
***BF\_LVDS\_QB\_SIZE*** CONFIG\_QB  
***BF\_LVDS\_QB\_MASK***  
***BF\_LVDS\_QB\_LSB***  
***BF\_OE\_B\_SIZE*** CONFIG\_QB  
***BF\_OE\_B\_MASK***  
***BF\_OE\_B\_LSB***  
***REGMAP\_APLL\_MAX***

Definition at line 55 of file ApIIRegDef.h.

## 4.8 ApI1 Function Module

Functions in this group are related to APLL provisioning.

### Data Structures

- struct [T\\_idtApI1ConfigPerOutput](#)  
*Structure containing APLL per output configuration.*
- struct [T\\_idtApI1Config](#)  
*Structure containing APLL full configuration.*
- struct [T\\_idtApI1FreqMapping](#)  
*Type definition for mapping output frequency to APLL configuration.*
- struct [T\\_idtApI1Xtal](#)  
*Structure containing APLL crystal id and frequency information.*

### Macros

- #define [IDT\\_GET\\_OUTPUT\\_APLL\\_CONFIG](#)(hdlr, output, outputApI1)  
*Utility macro to translate output port to APLL instance.*
- #define [IDT\\_APLL\\_API\\_LOG\\_HEADER](#)
- #define [IDT\\_APLL\\_API\\_LOG\\_ERR](#)(fmt)
- #define [IDT\\_APLL\\_API\\_LOG\\_INFO](#)(fmt)
- #define [IDT\\_APLL\\_API\\_LOG\\_DEBUG](#)(fmt)
- #define [IDT\\_APLL\\_API\\_TRACE](#)(fmt) OS\_TRACE(fmt)
- #define [INVALID\\_DIVIDER\\_VALUE](#) (0xFFFF)  
*Define constant indicating invalid divider value.*

### Typedefs

- typedef T\_osUInt16 [T\\_idtApI1DividerValue](#)  
*Type define for APLL divider value.*
- typedef T\_osUInt8 [T\\_idtApI1RegAddr](#)  
*Type define for APLL register address.*
- typedef T\_osUInt8 [T\\_idtApI1RegMask](#)  
*Type define for APLL register value mask.*
- typedef T\_osUInt8 [T\\_idtApI1RegVal](#)  
*Type define for APLL register value.*

### Enumerations

- enum [T\\_idtApI1InputFreqType](#) {  
APLL\_INPUT\_FREQ\_19440KHz, APLL\_INPUT\_FREQ\_25000KHz, APLL\_INPUT\_FREQ\_77760KHz, APLL\_INPUT\_FREQ\_125000KHz,  
APLL\_INPUT\_FREQ\_155520KHz, APLL\_INPUT\_FREQ\_25781\_DOT\_25KHz, APLL\_INPUT\_FREQ\_312500KHz, APLL\_INPUT\_FREQ\_128906\_DOT\_25KHz,  
APLL\_INPUT\_FREQ\_156250KHz, APLL\_INPUT\_FREQ\_8KHz, APLL\_INPUT\_FREQ\_MAX }  
*Enumerated type listing supported input frequencies.*



- enum `T_idtApIIOutputFreqType` {  
`APLL_OUTPUT_FREQ_24883_DOT_2KHz`, `APLL_OUTPUT_FREQ_25000KHz`, `APLL_OUTPUT_FREQ_25781_DOT_25KHz`, `APLL_OUTPUT_FREQ_77760KHz`,  
`APLL_OUTPUT_FREQ_78125KHz`, `APLL_OUTPUT_FREQ_80566_DOT_40625KHz`, `APLL_OUTPUT_FREQ_124416KHz`, `APLL_OUTPUT_FREQ_125000KHz`,  
`APLL_OUTPUT_FREQ_128906_DOT_25KHz`, `APLL_OUTPUT_FREQ_155520KHz`, `APLL_OUTPUT_FREQ_156250KHz`, `APLL_OUTPUT_FREQ_161132_DOT_8125KHz`,  
`APLL_OUTPUT_FREQ_311040KHz`, `APLL_OUTPUT_FREQ_312500KHz`, `APLL_OUTPUT_FREQ_322265_DOT_625KHz`, `APLL_OUTPUT_FREQ_622080KHz`,  
`APLL_OUTPUT_FREQ_625000KHz`, `APLL_OUTPUT_FREQ_644531_DOT_25KHz`, `APLL_OUTPUT_FREQ_MAX` }  
*Enumerated type listing supported output frequencies.*
- enum `T_idtApIIId` { `APLL_INST_1`, `APLL_INST_2`, `APLL_INST_MAX` }  
*Enumerated type listing APLL instance within device.*
- enum `T_idtApIIAccessType` { `APLL_ACCESS_I2C`, `APLL_ACCESS_SIM`, `APLL_ACCESS_MAX` }  
*Enumerated type listing supported access methods.*
- enum `T_idtApIIConfigSel` { `APLL_CONFIG0 = 0`, `APLL_CONFIG1 = 1`, `APLL_CONFIG_MAX` }  
*Enumerated type listing possible configuration for each APLL.*
- enum `T_idtApIIInputClkSrc` { `APLL_CLK_SEL_EXTERNAL`, `APLL_CLK_SEL_INTERNAL`, `APLL_CLK_SEL_MAX` }  
*Enumerated type listing input ports.*
- enum `T_idtApIIOutput` { `APLL_OUTPUT_QA`, `APLL_OUTPUT_QB`, `APLL_OUTPUT_MAX` }  
*Enumerated type listing output ports.*
- enum `T_idtApIIOutputEn` { `APLL_OUTPUT_DISABLE`, `APLL_OUTPUT_ENABLE`, `APLL_OUTPUT_EN_MAX` }  
*Enumerated type listing output port status (enable/disable)*
- enum `T_idtApIIOutputSigType` { `APLL_OUT_SIG_LVPECL`, `APLL_OUT_SIG_LVDS`, `APLL_OUT_SIG_MAX` }  
*Enumerated type listing output signal type.*
- enum `T_idtApIIOutputSupportedType` { `APLL_OUT_QA_ONLY`, `APLL_OUT_QB_ONLY`, `APLL_OUT_QA_OR_QB`, `APLL_OUT_MAX` }  
*Enumerated type listing frequency supported by the output.*
- enum `T_idtApIIQaDiv` {  
`APLL_QA_ODSEL_DIV_25 = 0`, `APLL_QA_ODSEL_DIV_5 = 1`, `APLL_QA_ODSEL_DIV_4 = 2`, `APLL_QA_ODSEL_DIV_2 = 3`,  
`APLL_QA_ODSEL_DIV_1 = 4`, `APLL_QA_ODSEL_DIV_MAX` }  
*Enumerated type listing output port A divider values.*
- enum `T_idtApIIQbDiv` {  
`APLL_QB_ODSEL_DIV_8 = 0`, `APLL_QB_ODSEL_DIV_5 = 1`, `APLL_QB_ODSEL_DIV_4 = 2`, `APLL_QB_ODSEL_DIV_2 = 3`,  
`APLL_QB_ODSEL_DIV_1 = 4`, `APLL_QB_ODSEL_DIV_MAX` }  
*Enumerated type listing output port B divider values.*
- enum `T_idtApIIFreqDoublersSel` { `APLL_FREQ_SEL_SINGLE = 0`, `APLL_FREQ_SEL_DOUBLE = 1`, `APLL_FREQ_SEL_MAX` }  
*Enumerated type listing feedback frequency doubling values.*
- enum `T_idtApIIXtalId` {  
`APLL_XTAL_1_APLL1`, `APLL_XTAL_2_APLL2`, `APLL_XTAL_3_APLL1`, `APLL_XTAL_4_APLL2`,  
`APLL_XTAL_MAX` }  
*Enumerated type listing crystals.*
- enum `T_idtApIIXtalType` { `APLL_XTAL_FREQ_25000KHz`, `APLL_XTAL_FREQ_25781_DOT_25KHz`, `APLL_XTAL_FREQ_24883_DOT_2KHz`, `APLL_XTAL_FREQ_MAX` }  
*Enumerated type listing support crystal frequencies.*
- enum `T_idtApIIMasterResetSync` { `APLL_OUT_MR_SYNC = 0`, `APLL_IN_MR_SYNC = 1`, `APLL_MR_SYNC_MAX` }

*Enumerated type listing Device master reset sync status.*

- enum `T_idtApplBypass` { `APLL_BYPASS_NORMAL_OP` = 0, `APLL_BYPASS_BYPASS` = 1, `APLL_BYPASS_MAX` }

*Enumerated type listing Appl bypass status/setting.*

- enum `T_idtApplShutoff` { `APLL_SHUTOFF_NORMAL_OP` = 0, `APLL_SHUTOFF_SHUTOFF` = 1, `APLL_SHUTOFF_MAX` }

*Enumerated type listing Appl shutoff status/setting.*

## Functions

- void `IDTApl_SetApplConfigPerOutput` (`T_idtDrvHdlr` hdlr, `T_idtApplId` applId, `T_idtApplOutput` output, `T_idtApplConfigPerOutput` \*applConfigPerOutput)  
*Set APLL per output configuration.*
- void `IDTApl_GetApplConfigPerOutput` (`T_idtDrvHdlr` hdlr, `T_idtApplId` applId, `T_idtApplOutput` output, `T_idtApplConfigPerOutput` \*applConfigPerOutput)  
*Get APLL per output configuration.*
- void `IDTApl_SetApplConfig` (`T_idtDrvHdlr` hdlr, `T_idtApplId` applId, `T_idtApplConfig` \*applConfig)  
*Set APLL full configuration.*
- void `IDTApl_GetApplConfig` (`T_idtDrvHdlr` hdlr, `T_idtApplId` applId, `T_idtApplConfig` \*applConfig)  
*Get APLL full configuration.*
- `outputFrequency_t` `IDTApl_ApllInput2DpllOutput` (`T_idtApplInputFreqType` appllInputFreq)  
*Translate APLL input frequency to DPLL output frequency.*
- `T_idtApplOutputFreqType` `IDTApl_DpllOutput2ApplOutput` (`outputFrequency_t` dpllOutput)  
*Translate DPLL output frequency to APLL output frequency.*
- const `T_idtApplFreqMapping` \* `IDTApl_GetApplFreqTableEntry` (`T_idtDrvHdlr` hdlr, `T_idtOutputApplConfig` outputAppl, `outputFrequency_t` nOutFreq)  
*Get APLL frequency configuration table entry based on the output frequency.*
- `T_idtApplConfigSel` `IDTApl_GetNonActiveApplConfig` (`T_idtDrvHdlr` hdlr, `T_idtApplId` applId)  
*Get non-active APLL configuration.*
- void `IDTApl_Switch2NonActiveApplConfig` (`T_idtDrvHdlr` hdlr, `T_idtApplId` applId)  
*Switch to non-active APLL configuration.*
- `T_idtApplXtalId` `IDTApl_GetXtalIdFromXtalFreq` (`T_idtDrvHdlr` hdlr, `T_idtApplId` applId, `T_idtApplXtalType` appllVcxoFreq)  
*Get APLL configured crystal ID from crystal frequency.*
- `T_osBool` `IDTApl_XtalConfigured` (`T_idtDrvHdlr` hdlr, `T_idtApplId` applId)  
*Checks if there is any XTAL configured for the APLL.*
- `T_osBool` `IDTApl_ValidXtalInput` (const `T_idtDrvDeviceConfig` \*deviceConfig, `T_idtApplXtal` \*xtalList, `T_osUInt8` numberOfXtal)  
*Checks if there is input XTAL information is valid for the device.*
- `T_idtApplXtal` \* `IDTApl_GetSupportedXtal` (const `T_idtDrvDeviceConfig` \*deviceConfig, `T_osUInt8` \*numberOfXtal)  
*Return supported xtal configuration by the device.*
- `T_idtApplConfigSel` `IDTApl_GetConfigSel` (`T_idtDrvHdlr` hdlr, `T_idtApplId` appllInstId)  
*Function to retrieve APLL configuration.*
- void `IDTApl_SetConfigSel` (`T_idtDrvHdlr` hdlr, `T_idtApplId` appllInstId, `T_idtApplConfigSel` applConfig)  
*Function to provision APLL based on input configuration.*
- `T_idtApplInputClkSrc` `IDTApl_GetInputClkSrc` (`T_idtDrvHdlr` hdlr, `T_idtApplId` appllInstId)  
*Function to retrieve selected APLL input frequency source (external/internal)*
- void `IDTApl_SetInputClkSrc` (`T_idtDrvHdlr` hdlr, `T_idtApplId` appllInstId, `T_idtApplInputClkSrc` inputClk)  
*Function to provision APLL input frequency source (external/internal)*
- `T_idtApplDividerValue` `IDTApl_GetPreDiv` (`T_idtDrvHdlr` hdlr, `T_idtApplId` appllInstId, `T_idtApplConfigSel` applConfig)

- Function to retrieve pre- (input) divider value.*

  - void `IDTApll_GetPreDivRange` (`T_idtDrvHdlr` hdlr, `T_idtApllDividerValue` \*minDiv, `T_idtApllDividerValue` \*maxDiv)
- Function to retrieve pre- (input) divisor range.*

  - void `IDTApll_SetPreDiv` (`T_idtDrvHdlr` hdlr, `T_idtApllId` apIIInstId, `T_idtApllConfigSel` apIIConfig, `T_idtApllDividerValue` div)
- Function to provision pre- (input) divider value.*

  - `T_idtApllDividerValue` `IDTApll_GetFeedbackDiv` (`T_idtDrvHdlr` hdlr, `T_idtApllId` apIIInstId, `T_idtApllConfigSel` apIIConfig)
- Function to retrieve feedback (oscillator) divider value.*

  - void `IDTApll_GetFeedbackDivRange` (`T_idtDrvHdlr` hdlr, `T_idtApllDividerValue` \*minDiv, `T_idtApllDividerValue` \*maxDiv)
- Function to retrieve feedback (oscillator) divisor range.*

  - void `IDTApll_SetFeedbackDiv` (`T_idtDrvHdlr` hdlr, `T_idtApllId` apIIInstId, `T_idtApllConfigSel` apIIConfig, `T_idtApllDividerValue` div)
- Function to provision feedback (oscillator) divider value.*

  - `T_idtApllQaDiv` `IDTApll_GetQaDiv` (`T_idtDrvHdlr` hdlr, `T_idtApllId` apIIInstId, `T_idtApllConfigSel` apIIConfig)
- Function to retrieve output port A divisor.*

  - void `IDTApll_SetQaDiv` (`T_idtDrvHdlr` hdlr, `T_idtApllId` apIIInstId, `T_idtApllConfigSel` apIIConfig, `T_idtApllQaDiv` div)
- Function to provision output port A divisor.*

  - `T_idtApllQaDiv` `IDTApll_GetQbDiv` (`T_idtDrvHdlr` hdlr, `T_idtApllId` apIIInstId, `T_idtApllConfigSel` apIIConfig)
- Function to retrieve output port B divisor.*

  - void `IDTApll_SetQbDiv` (`T_idtDrvHdlr` hdlr, `T_idtApllId` apIIInstId, `T_idtApllConfigSel` apIIConfig, `T_idtApllQbDiv` div)
- Function to provision output port B divisor.*

  - `T_idtApllFreqDoublerSel` `IDTApll_GetFreqDoublerSel` (`T_idtDrvHdlr` hdlr, `T_idtApllId` apIIInstId)
- Function to retrieve whether feedback frequency doubling is enabled.*

  - void `IDTApll_SetFreqDoublerSel` (`T_idtDrvHdlr` hdlr, `T_idtApllId` apIIInstId, `T_idtApllFreqDoublerSel` doubler)
- Function to enable/disable feedback frequency doubling.*

  - `T_idtApllXtalId` `IDTApll_GetXtalId` (`T_idtDrvHdlr` hdlr, `T_idtApllId` apIIInstId)
- Function to retrieve oscillator currently used.*

  - void `IDTApll_SetXtalId` (`T_idtDrvHdlr` hdlr, `T_idtApllId` apIIInstId, `T_idtApllXtalId` xtal)
- Function to select oscillator.*

  - `T_idtApllOutputSigType` `IDTApll_GetOutputSigType` (`T_idtDrvHdlr` hdlr, `T_idtApllId` apIIInstId, `T_idtApllOutput` output)
- Function to retrieve output port signal type.*

  - void `IDTApll_SetOutputSigType` (`T_idtDrvHdlr` hdlr, `T_idtApllId` apIIInstId, `T_idtApllOutput` output, `T_idtApllOutputSigType` outputSigType)
- Function to provision output port signal type.*

  - `T_idtApllOutputEn` `IDTApll_GetOutputEnState` (`T_idtDrvHdlr` hdlr, `T_idtApllId` apIIInstId, `T_idtApllOutput` output)
- Function to retrieve output port status (enable/disable)*

  - void `IDTApll_SetOutputEnState` (`T_idtDrvHdlr` hdlr, `T_idtApllId` apIIInstId, `T_idtApllOutput` output, `T_idtApllOutputEn` enable)
- Function to control (enable/disable) output port.*

  - `T_idtApllMasterResetSync` `IDTApll_GetMasterResetSync` (`T_idtDrvHdlr` hdlr, `T_idtApllId` apIIInstId)
- Function to retrieve reset status of device.*

  - void `IDTApll_SetMasterResetSync` (`T_idtDrvHdlr` hdlr, `T_idtApllId` apIIInstId, `T_idtApllMasterResetSync` reset)
- Function to reset APLL.*

  - `T_idtApllBypass` `IDTApll_GetBypass` (`T_idtDrvHdlr` hdlr, `T_idtApllId` apIIInstId)

*Function to retrieve bypass status of device.*

- void `IDTApl_SetBypass` (`T_idtDrvHdlr` hdlr, `T_idtAplIld` aplIInstId, `T_idtAplBypass` bypass)

*Function to set APLL bypass setting.*

- `T_idtAplShutoff` `IDTApl_GetShutoff` (`T_idtDrvHdlr` hdlr, `T_idtAplIld` aplIInstId)

*Function to retrieve shutoff status of device.*

- void `IDTApl_SetShutoff` (`T_idtDrvHdlr` hdlr, `T_idtAplIld` aplIInstId, `T_idtAplShutoff` shutoff)

*Function to set APLL shutoff setting.*

- const `T_idtAplFreqMapping` \* `IDTApl_GetConfigListByFreq` (`T_idtAplOutputFreqType` aplOutputFreq)

*Function to retrieve output configuration given an output frequency.*

- const `T_idtAplFreqMapping` \* `IDTApl_GetConfigListByXtalType` (`T_idtAplXtalType` aplXtalFreq)

*Function to retrieve output configuration given the oscillator type (frequency)*

- `T_osBool` `IDTApl_NullFreqTableEntry` (const `T_idtAplFreqMapping` \*aplFreqMapping)

*Function to check whether the input APLL frequency mapping is NULL (not configured)*

- const `T_idtAplFreqMapping` \* `IDTApl_GetCurrentAplFreqConfig` (`T_idtAplIld` aplIld, `T_idtAplOutput` output)

*Function to retrieve the current APLL frequency mapping configuration for the output.*

### 4.8.1 Detailed Description

Functions in this group are related to APLL provisioning.

### 4.8.2 Macro Definition Documentation

#### 4.8.2.1 #define IDT\_APLL\_API\_LOG\_DEBUG( fmt )

**Value:**

```
do { \
    OS_LOGGER(9, (IDT_APLL_API_LOG_HEADER)); \
    OS_LOGGER(9, fmt); \
} while (0)
```

Definition at line 65 of file `AplLogging.h`.

#### 4.8.2.2 #define IDT\_APLL\_API\_LOG\_ERR( fmt )

**Value:**

```
do { \
    OS_ERROR(fmt); \
} while(0)
```

Definition at line 52 of file `AplLogging.h`.

#### 4.8.2.3 #define IDT\_APLL\_API\_LOG\_HEADER

**Value:**

```
"[File: %s, Line: %d, Function: %s] ", \
    __FILE__, __LINE__, __FUNCTION__
```

Definition at line 47 of file `AplLogging.h`.

4.8.2.4 #define IDT\_APLL\_API\_LOG\_INFO( *fmt* )**Value:**

```
do { \
    OS_LOGGER(5, (IDT_APLL_API_LOG_HEADER)); \
    OS_LOGGER(5, fmt); \
} while(0)
```

Definition at line 58 of file ApIILogging.h.

4.8.2.5 #define IDT\_APLL\_API\_TRACE( *fmt* ) OS\_TRACE(*fmt*)

Definition at line 72 of file ApIILogging.h.

4.8.2.6 #define IDT\_GET\_OUTPUT\_APLL\_CONFIG( *hdr*, *output*, *outputApII* )**Value:**

```
do {
    OS_ASSERT((output) <= IDT_DRV_MAX_OUTPUT); \
    OS_ASSERT((output) > 0); \
    outputApII = hdr->deviceConfig_m->outPutApIIConfig[output]; \
} while(0)
```

Utility macro to translate output port to APLL instance.

**Parameters**

<i>hdr</i>	Device driver handle
<i>output</i>	External output port number
<i>outputApII</i>	APLL instance

Definition at line 60 of file ApII.h.

## 4.8.2.7 #define INVALID\_DIVIDER\_VALUE (0xFFFF)

Define constant indicating invalid divider value.

Definition at line 49 of file ApIITypeDef.h.

## 4.8.3 Typedef Documentation

## 4.8.3.1 typedef T\_osUInt16 T\_idtApIIDividerValue

Type define for APLL divider value.

Definition at line 224 of file ApIITypeDef.h.

## 4.8.3.2 typedef T\_osUInt8 T\_idtApIIRegAddr

Type define for APLL register address.

Definition at line 229 of file ApIITypeDef.h.

#### 4.8.3.3 typedef T\_osUInt8 T\_idtApIRegMask

Type define for APLL register value mask.

Definition at line 234 of file ApITypeDef.h.

#### 4.8.3.4 typedef T\_osUInt8 T\_idtApIRegVal

Type define for APLL register value.

Definition at line 239 of file ApITypeDef.h.

### 4.8.4 Enumeration Type Documentation

#### 4.8.4.1 enum T\_idtApIAccessType

Enumerated type listing supported access methods.

Enumerator

***APLL\_ACCESS\_I2C*** Device access through I2C

***APLL\_ACCESS\_SIM*** Simulated device

***APLL\_ACCESS\_MAX***

Definition at line 64 of file ApITypeDef.h.

#### 4.8.4.2 enum T\_idtApIBypass

Enumerated type listing ApI bypass status/setting.

Enumerator

***APLL\_BYPASS\_NORMAL\_OP*** ApI in normal operation

***APLL\_BYPASS\_BYPASS*** ApI bypass VCXO and connect selected clock input to output A and B

***APLL\_BYPASS\_MAX***

Definition at line 204 of file ApITypeDef.h.

#### 4.8.4.3 enum T\_idtApIConfigSel

Enumerated type listing possible configuration for each APLL.

Enumerator

***APLL\_CONFIG0*** Configuration #1

***APLL\_CONFIG1*** Configuration #2

***APLL\_CONFIG\_MAX***

Definition at line 74 of file ApITypeDef.h.

## 4.8.4.4 enum T\_idtApIIFreqDoublersel

Enumerated type listing feedback frequency doubling values.

Enumerator

***APLL\_FREQ\_SEL\_SINGLE*** Feedback frequency not doubled  
***APLL\_FREQ\_SEL\_DOUBLE*** Feedback frequency doubled  
***APLL\_FREQ\_SEL\_MAX***

Definition at line 161 of file ApIITypeDef.h.

## 4.8.4.5 enum T\_idtApIIId

Enumerated type listing APLL instance within device.

Enumerator

***APLL\_INST\_1*** APLL #1  
***APLL\_INST\_2*** APLL #2  
***APLL\_INST\_MAX***

Definition at line 54 of file ApIITypeDef.h.

## 4.8.4.6 enum T\_idtApIIInputClkSrc

Enumerated type listing input ports.

Enumerator

***APLL\_CLK\_SEL\_EXTERNAL*** External clock source  
***APLL\_CLK\_SEL\_INTERNAL*** Internal clock source  
***APLL\_CLK\_SEL\_MAX***

Definition at line 84 of file ApIITypeDef.h.

## 4.8.4.7 enum T\_idtApIIInputFreqType

Enumerated type listing supported input frequencies.

Enumerator

***APLL\_INPUT\_FREQ\_19440KHz*** 19.4 MHz  
***APLL\_INPUT\_FREQ\_25000KHz*** 25.0 MHz  
***APLL\_INPUT\_FREQ\_77760KHz*** 77.76 MHz  
***APLL\_INPUT\_FREQ\_125000KHz*** 125 MHz  
***APLL\_INPUT\_FREQ\_155520KHz*** 155.52 MHz  
***APLL\_INPUT\_FREQ\_25781\_DOT\_25KHz*** 25.78125 MHz  
***APLL\_INPUT\_FREQ\_312500KHz*** 312.5 MHz  
***APLL\_INPUT\_FREQ\_128906\_DOT\_25KHz*** 128.90625 MHz  
***APLL\_INPUT\_FREQ\_156250KHz*** 156.25 MHz  
***APLL\_INPUT\_FREQ\_8KHz*** 8 KHz  
***APLL\_INPUT\_FREQ\_MAX***

Definition at line 56 of file ApIIFreqProfile.h.

#### 4.8.4.8 enum T\_idtApIIMasterResetSync

Enumerated type listing Device master reset sync status.

Enumerator

***APLL\_OUT\_MR\_SYNC*** Device out of master reset sync (normal operation)  
***APLL\_IN\_MR\_SYNC*** Device in master reset sync  
***APLL\_MR\_SYNC\_MAX***

Definition at line 194 of file ApIITypeDef.h.

#### 4.8.4.9 enum T\_idtApIIOutput

Enumerated type listing output ports.

Enumerator

***APLL\_OUTPUT\_QA*** Output port A  
***APLL\_OUTPUT\_QB*** Output port B  
***APLL\_OUTPUT\_MAX***

Definition at line 94 of file ApIITypeDef.h.

#### 4.8.4.10 enum T\_idtApIIOutputEn

Enumerated type listing output port status (enable/disable)

Enumerator

***APLL\_OUTPUT\_DISABLE*** Disable output port  
***APLL\_OUTPUT\_ENABLE*** Enable output port  
***APLL\_OUTPUT\_EN\_MAX***

Definition at line 104 of file ApIITypeDef.h.

#### 4.8.4.11 enum T\_idtApIIOutputFreqType

Enumerated type listing supported output frequencies.

Enumerator

***APLL\_OUTPUT\_FREQ\_24883\_DOT\_2KHz*** 24.8832 MHz  
***APLL\_OUTPUT\_FREQ\_25000KHz*** 25.0 MHz  
***APLL\_OUTPUT\_FREQ\_25781\_DOT\_25KHz*** 25.78125 MHz  
***APLL\_OUTPUT\_FREQ\_77760KHz*** 77.76 MHz  
***APLL\_OUTPUT\_FREQ\_78125KHz*** 78.125 MHz  
***APLL\_OUTPUT\_FREQ\_80566\_DOT\_40625KHz*** 80.56640625 MHz  
***APLL\_OUTPUT\_FREQ\_124416KHz*** 124.416 MHz  
***APLL\_OUTPUT\_FREQ\_125000KHz*** 125.0 MHz  
***APLL\_OUTPUT\_FREQ\_128906\_DOT\_25KHz*** 128.90625 MHz  
***APLL\_OUTPUT\_FREQ\_155520KHz*** 155.52 MHz



***APLL\_OUTPUT\_FREQ\_156250KHz*** 156.250 MHz  
***APLL\_OUTPUT\_FREQ\_161132\_DOT\_8125KHz*** 161.1328125 MHz  
***APLL\_OUTPUT\_FREQ\_311040KHz*** 311.040 MHz  
***APLL\_OUTPUT\_FREQ\_312500KHz*** 312.50 MHz  
***APLL\_OUTPUT\_FREQ\_322265\_DOT\_625KHz*** 322.265625 MHz  
***APLL\_OUTPUT\_FREQ\_622080KHz*** 622.080 MHz  
***APLL\_OUTPUT\_FREQ\_625000KHz*** 625.0 MHz  
***APLL\_OUTPUT\_FREQ\_644531\_DOT\_25KHz*** 644.53125 MHz  
***APLL\_OUTPUT\_FREQ\_MAX***

Definition at line 74 of file ApIIFreqProfile.h.

#### 4.8.4.12 enum T\_idtApIIOutputSigType

Enumerated type listing output signal type.

Enumerator

***APLL\_OUT\_SIG\_LVPECL*** LVPECL output signal type  
***APLL\_OUT\_SIG\_LVDS*** LVDS output signal type  
***APLL\_OUT\_SIG\_MAX***

Definition at line 114 of file ApIITypeDef.h.

#### 4.8.4.13 enum T\_idtApIIOutputSupportedType

Enumerated type listing frequency supported by the output.

Enumerator

***APLL\_OUT\_QA\_ONLY*** Frequency only supported by output port A  
***APLL\_OUT\_QB\_ONLY*** Frequency only supported by output port B  
***APLL\_OUT\_QA\_OR\_QB*** Frequency supported by both output port A and B  
***APLL\_OUT\_MAX***

Definition at line 124 of file ApIITypeDef.h.

#### 4.8.4.14 enum T\_idtApIIQaDiv

Enumerated type listing output port A divider values.

Enumerator

***APLL\_QA\_ODSEL\_DIV\_25*** Output A divider 25  
***APLL\_QA\_ODSEL\_DIV\_5*** Output A divider 5  
***APLL\_QA\_ODSEL\_DIV\_4*** Output A divider 4  
***APLL\_QA\_ODSEL\_DIV\_2*** Output A divider 2  
***APLL\_QA\_ODSEL\_DIV\_1*** Output A divider 1  
***APLL\_QA\_ODSEL\_DIV\_MAX***

Definition at line 135 of file ApIITypeDef.h.

## 4.8.4.15 enum T\_idtApIIQbDiv

Enumerated type listing output port B divider values.

Enumerator

***APLL\_QB\_ODSEL\_DIV\_8*** Output B divider 8  
***APLL\_QB\_ODSEL\_DIV\_5*** Output B divider 5  
***APLL\_QB\_ODSEL\_DIV\_4*** Output B divider 4  
***APLL\_QB\_ODSEL\_DIV\_2*** Output B divider 2  
***APLL\_QB\_ODSEL\_DIV\_1*** Output B divider 1  
***APLL\_QB\_ODSEL\_DIV\_MAX***

Definition at line 148 of file ApIITypeDef.h.

## 4.8.4.16 enum T\_idtApIIShutoff

Enumerated type listing ApII shutoff status/setting.

Enumerator

***APLL\_SHUTOFF\_NORMAL\_OP*** ApII in normal operation  
***APLL\_SHUTOFF\_SHUTOFF*** VCXO current is shut off and Outputs are squelched  
***APLL\_SHUTOFF\_MAX***

Definition at line 214 of file ApIITypeDef.h.

## 4.8.4.17 enum T\_idtApII XtalId

Enumerated type listing crystals.

Enumerator

***APLL\_XTAL\_1\_APLL1*** XTAL1 connects to APPL1  
***APLL\_XTAL\_2\_APLL2*** XTAL2 connects to APPL2  
***APLL\_XTAL\_3\_APLL1*** XTAL3 connects to APPL1  
***APLL\_XTAL\_4\_APLL2*** XTAL4 connects to APPL2  
***APLL\_XTAL\_MAX***

Definition at line 171 of file ApIITypeDef.h.

## 4.8.4.18 enum T\_idtApII XtalType

Enumerated type listing support crystal frequencies.

Enumerator

***APLL\_XTAL\_FREQ\_25000KHz*** Ethernet (25 MHz)  
***APLL\_XTAL\_FREQ\_25781\_DOT\_25KHz*** Ethernet FEC (25.78125 MHz)  
***APLL\_XTAL\_FREQ\_24883\_DOT\_2KHz*** SONET/SDH (24.8832 MHz)  
***APLL\_XTAL\_FREQ\_MAX***

Definition at line 183 of file ApIITypeDef.h.

### 4.8.5 Function Documentation

#### 4.8.5.1 `outputFrequency_t` IDTAplI\_AplIInput2DplIOutput ( `T_idtAplIInputFreqType` *apIIInputFreq* )

Translate APLL input frequency to DPLL output frequency.

##### Parameters

<i>apIIInputFreq</i>	APLL input frequency
----------------------	----------------------

##### Returns

DPLL output frequency

Definition at line 474 of file ApII.c.

#### 4.8.5.2 `T_idtAplIOutputFreqType` IDTAplI\_DplIOutput2AplIOutput ( `outputFrequency_t` *dplIOutput* )

Translate DPLL output frequency to APLL output frequency.

##### Parameters

<i>dplIOutput</i>	DPLL output frequency
-------------------	-----------------------

##### Returns

APLL output frequency

Definition at line 533 of file ApII.c.

#### 4.8.5.3 `void` IDTAplI\_GetAplIConfig ( `T_idtDrvHdlr` *hdlr*, `T_idtAplIIId` *apIIInstId*, `T_idtAplIConfig *` *apIIConfig* )

Get APLL full configuration.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>apIIInstId</i>	APLL instance
<i>apIIConfig</i>	APLL configuration

Definition at line 416 of file ApII.c.

#### 4.8.5.4 `void` IDTAplI\_GetAplIConfigPerOutput ( `T_idtDrvHdlr` *hdlr*, `T_idtAplIIId` *apIIInstId*, `T_idtAplIOutput` *output*, `T_idtAplIConfigPerOutput *` *apIIConfigPerOutput* )

Get APLL per output configuration.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>apIIInstId</i>	APLL instance
<i>output</i>	Output port
<i>apIIConfigPer-Output</i>	APLL per port configuration

Definition at line 318 of file ApII.c.

4.8.5.5 `const T_idtApIIFreqMapping* IDTAplI_GetApIIFreqTableEntry ( T_idtDrvHdlr hdlr, T_idtOutputApIIFreq outputApIIFreq, outputFrequency_t nOutFreq )`

Get APLL frequency configuration table entry based on the output frequency.

#### Parameters

<i>hdlr</i>	Device driver handler
<i>outputApIIFreq</i>	Output APLL configuration
<i>nOutFreq</i>	Output frequency

#### Returns

APLL frequency configuration

Definition at line 627 of file ApIIFreq.c.

4.8.5.6 `T_idtApIIBypass IDTAplI_GetBypass ( T_idtDrvHdlr hdlr, T_idtApIIFreq apIIFreq )`

Function to retrieve bypass status of device.

#### Parameters

<i>hdlr</i>	Device driver handler
<i>apIIFreq</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>

#### Returns

Bypass status

- APLL\_BYPASS\_NORMAL\_OP - Normal operation
- APLL\_BYPASS\_BYPASS - Bypass VCXO, connect input to output

Definition at line 1359 of file ApIIFreq.c.

4.8.5.7 `const T_idtApIIFreqMapping* IDTAplI_GetConfigListByFreq ( T_idtApIIFreqType apIIFreqType, apIIFreq apIIFreq )`

Function to retrieve output configuration given an output frequency.

#### Parameters

<i>apIIFreq</i>	Output frequency
-----------------	------------------

#### Returns

Output configuration

Definition at line 545 of file ApIIFreqProfile.c.

4.8.5.8 `const T_idtApIIFreqMapping* IDTAplI_GetConfigListByXtalType ( T_idtApIIFreqType apIIFreqType, apIIFreq apIIFreq )`

Function to retrieve output configuration given the oscillator type (frequency)

## Parameters

<i>apllVcxoFreq</i>	Oscillator type (frequency)
---------------------	-----------------------------

## Returns

Output configuration

Definition at line 564 of file ApIIFreqProfile.c.

4.8.5.9 **T\_idtApIIConfigSel** IDTApll\_GetConfigSel ( T\_idtDrvHdlr *hdlr*, T\_idtApIIId *apllInstId* )

Function to retrieve APLL configuration.

## Parameters

<i>hdlr</i>	Device driver handler
<i>apllInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>

## Returns

APLL configuration

- APLL\_CONFIG0 - configuration 0
- APLL\_CONFIG1 - configuration 1

Definition at line 219 of file ApIIApi.c.

4.8.5.10 **const T\_idtApIIFreqMapping\*** IDTApll\_GetCurrentApIIFreqConfig ( T\_idtApIIId *apllId*, T\_idtApIIOutput *output* )

Function to retrieve the current APLL frequency mapping configuration for the output.

## Parameters

<i>apllId</i>	APLL instance
<i>output</i>	APLL output

## Returns

APLL frequency mapping configuration

Definition at line 604 of file ApIIFreqProfile.c.

4.8.5.11 **T\_idtApIIDividerValue** IDTApll\_GetFeedbackDiv ( T\_idtDrvHdlr *hdlr*, T\_idtApIIId *apllInstId*, T\_idtApIIConfigSel *apllConfig* )

Function to retrieve feedback (oscillator) divider value.

## Parameters

<i>hdr</i>	Device driver handler
<i>apllInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>
<i>apllConfig</i>	APLL configuration <ul style="list-style-type: none"> <li>• APLL_CONFIG0 - configuration 0</li> <li>• APLL_CONFIG1 - configuration 1</li> </ul>

## Returns

Divisor value

Definition at line 525 of file ApllApi.c.

4.8.5.12 void IDTApll\_GetFeedbackDivRange ( T\_idtDrvHdr *hdr*, T\_idtApllDividerValue \* *minDiv*, T\_idtApllDividerValue \* *maxDiv* )

Function to retrieve feedback (oscillator) divisor range.

## Parameters

<i>hdr</i>	Device driver handler
<i>minDiv</i>	minimum divisor
<i>maxDiv</i>	maximum divisor

Definition at line 502 of file ApllApi.c.

4.8.5.13 T\_idtApllFreqDoublerSel IDTApll\_GetFreqDoublerSel ( T\_idtDrvHdr *hdr*, T\_idtApllId *apllInstId* )

Function to retrieve whether feedback frequency doubling is enabled.

## Parameters

<i>hdr</i>	Device driver handler
<i>apllInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>

## Returns

Feedback frequency doubling value

- APLL\_FREQ\_SEL\_SINGLE - Feedback frequency not doubled
- APLL\_FREQ\_SEL\_DOUBLE - Feedback frequency doubled

Definition at line 890 of file ApllApi.c.

4.8.5.14 T\_idtApllInputClkSrc IDTApll\_GetInputClkSrc ( T\_idtDrvHdr *hdr*, T\_idtApllId *apllInstId* )

Function to retrieve selected APLL input frequency source (external/internal)

## Parameters

<i>hdr</i>	Device driver handler
<i>apllInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>

## Returns

Input clock source for APLL

- APLL\_CLK\_SEL\_EXTERNAL - external clock source
- APLL\_CLK\_SEL\_INTERNAL - internal clock source

Definition at line 287 of file ApllApi.c.

#### 4.8.5.15 T\_idtApllMasterResetSync IDTApll.GetMasterResetSync ( T\_idtDrvHdr *hdr*, T\_idtApllId *apllInstId* )

Function to retrieve reset status of device.

## Parameters

<i>hdr</i>	Device driver handler
<i>apllInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>

## Returns

Master reset sync

- APLL\_OUT\_MR\_SYNC - Normal operation
- APLL\_IN\_MR\_SYNC - In master sync reset

Definition at line 1291 of file ApllApi.c.

#### 4.8.5.16 T\_idtApllConfigSel IDTApll.GetNonActiveApllConfig ( T\_idtDrvHdr *hdr*, T\_idtApllId *apllInst* )

Get non-active APLL configuration.

## Parameters

<i>hdr</i>	Device driver handler
<i>apllInst</i>	APLL instance

**Returns**

Non-active APLL configuration

Definition at line 706 of file ApI.c.

#### 4.8.5.17 T\_idtApIOutputEn IDTAplI.GetOutputEnState ( T\_idtDrvHdlr *hdlr*, T\_idtApIId *apIInstId*, T\_idtApIOutput *output* )

Function to retrieve output port status (enable/disable)

**Parameters**

<i>hdlr</i>	Device driver handler
<i>apIInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>
<i>output</i>	Output port <ul style="list-style-type: none"> <li>• APLL_OUTPUT_QA - Output port A</li> <li>• APLL_OUTPUT_QB - Output port B</li> </ul>

**Returns**

Enable /Disable output port

- APLL\_OUTPUT\_DISABLE - Disable output
- APLL\_OUTPUT\_ENABLE - Enable output

Definition at line 1146 of file ApIApi.c.

#### 4.8.5.18 T\_idtApIOutputSigType IDTAplI.GetOutputSigType ( T\_idtDrvHdlr *hdlr*, T\_idtApIId *apIInstId*, T\_idtApIOutput *output* )

Function to retrieve output port signal type.

**Parameters**

<i>hdlr</i>	Device driver handler
<i>apIInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>
<i>output</i>	Output port <ul style="list-style-type: none"> <li>• APLL_OUTPUT_QA - Output port A</li> <li>• APLL_OUTPUT_QB - Output port B</li> </ul>

**Returns**

output signal type

- APLL\_OUT\_SIG\_LVPECL - Output LVPECL signal
- APLL\_OUT\_SIG\_LVDS - Output LVDS signal



Definition at line 1035 of file ApIIApi.c.

#### 4.8.5.19 T\_idtApIIDividerValue IDTAplI\_GetPreDiv ( T\_idtDrvHdlr *hdlr*, T\_idtApIIId *apIIInstId*, T\_idtApIIConfigSel *apIIConfig* )

Function to retrieve pre- (input) divider value.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>apIIInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>
<i>apIIConfig</i>	APLL configuration <ul style="list-style-type: none"> <li>• APLL_CONFIG0 - configuration 0</li> <li>• APLL_CONFIG1 - configuration 1</li> </ul>

##### Returns

Divisor value

Definition at line 356 of file ApIIApi.c.

#### 4.8.5.20 void IDTAplI\_GetPreDivRange ( T\_idtDrvHdlr *hdlr*, T\_idtApIIDividerValue \* *minDiv*, T\_idtApIIDividerValue \* *maxDiv* )

Function to retrieve pre- (input) divisor range.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>minDiv</i>	minimum divisor
<i>maxDiv</i>	maximum divisor

##### Note

Divisor "1" is also a valid divisor

Definition at line 415 of file ApIIApi.c.

#### 4.8.5.21 T\_idtApIIQaDiv IDTAplI\_GetQaDiv ( T\_idtDrvHdlr *hdlr*, T\_idtApIIId *apIIInstId*, T\_idtApIIConfigSel *config* )

Function to retrieve output port A divisor.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>apIIInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>

<i>config</i>	APLL configuration <ul style="list-style-type: none"> <li>• APLL_CONFIG0 - configuration 0</li> <li>• APLL_CONFIG1 - configuration 1</li> </ul>
---------------	---

**Returns**

Output divider assigned to output port A

- APLL\_QA\_ODSEL\_DIV\_25 - divide by 25
- APLL\_QA\_ODSEL\_DIV\_5 - divide by 5
- APLL\_QA\_ODSEL\_DIV\_4 - divide by 4
- APLL\_QA\_ODSEL\_DIV\_2 - divide by 2
- APLL\_QA\_ODSEL\_DIV\_1 - divide by 1

Definition at line 662 of file AplApi.c.

#### 4.8.5.22 T\_idtAplQaDiv IDTApl\_GetQbDiv ( T\_idtDrvHdlr *hdlr*, T\_idtAplIld *apllInstId*, T\_idtAplConfigSel *config* )

Function to retrieve output port B divisor.

**Parameters**

<i>hdlr</i>	Device driver handler
<i>apllInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>
<i>config</i>	APLL configuration <ul style="list-style-type: none"> <li>• APLL_CONFIG0 - configuration 0</li> <li>• APLL_CONFIG1 - configuration 1</li> </ul>

**Returns**

Output divider assigned to output port B

- APLL\_QB\_ODSEL\_DIV\_8 - divide by 8
- APLL\_QB\_ODSEL\_DIV\_5 - divide by 5
- APLL\_QB\_ODSEL\_DIV\_4 - divide by 4
- APLL\_QB\_ODSEL\_DIV\_2 - divide by 2
- APLL\_QB\_ODSEL\_DIV\_1 - divide by 1

Definition at line 779 of file AplApi.c.

#### 4.8.5.23 T\_idtAplIshutoff IDTApl\_GetShutoff ( T\_idtDrvHdlr *hdlr*, T\_idtAplIld *apllInstId* )

Function to retrieve shutoff status of device.

## Parameters

<i>hdr</i>	Device driver handler
<i>apllInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>

## Returns

Shutoff status

- APLL\_SHUTOFF\_NORMAL\_OP - Normal operation
- APLL\_SHUTOFF\_SHUTOFF - VCXO shutoff

Definition at line 1427 of file ApIIApi.c.

#### 4.8.5.24 T\_idtApIIxTal\* IDTAplI\_GetSupportedXtal ( const T\_idtDrvDeviceConfig \* deviceConfig, T\_osUInt8 \* numberOfXtal )

Return supported xtal configuration by the device.

## Parameters

<i>deviceConfig</i>	APLL device configuration
<i>numberOfXtal</i>	Number of xtal configuration in the returned list

## Returns

The list of supported XTAL configuration

Caller needs to free the list after finishing using it.

Definition at line 899 of file ApII.c.

#### 4.8.5.25 T\_idtApIIxTalId IDTAplI\_GetXtalId ( T\_idtDrvHdr *hdr*, T\_idtApIIId *apllInstId* )

Function to retrieve oscillator currently used.

## Parameters

<i>hdr</i>	Device driver handler
<i>apllInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>

## Returns

current oscillator used

- APLL\_XTAL\_1\_APLL1 - XTAL1 for APLL1
- APLL\_XTAL\_2\_APLL2 - XTAL2 for APLL2
- APLL\_XTAL\_3\_APLL1 - XTAL3 for APLL1
- APLL\_XTAL\_4\_APLL2 - XTAL4 for APLL2

Definition at line 960 of file ApIIApi.c.

#### 4.8.5.26 T\_idtApIIXtalId IDTApl\_GetXtalIdFromXtalFreq ( T\_idtDrvHdlr *hdlr*, T\_idtApIIId *apIIInst*, T\_idtApIIXtalType *apIIVcxoFreq* )

Get APLL configured crystal ID from crystal frequency.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>apIIInst</i>	APLL instance
<i>apIIVcxoFreq</i>	Crytal frequency

##### Returns

Crytal ID

Definition at line 753 of file ApI.c.

#### 4.8.5.27 T\_osBool IDTApl\_NullFreqTableEntry ( const T\_idtApIIFreqMapping \* *apIIFreqConfig* )

Function to check whether the input APLL frequency mapping is NULL (not configured)

##### Parameters

<i>apIIFreqConfig</i>	APLL frequency mapping configuration
-----------------------	--------------------------------------

##### Returns

E\_osTrue - not configured, E\_osFalse - configured

Definition at line 583 of file ApIIFreqProfile.c.

#### 4.8.5.28 void IDTApl\_SetApIConfig ( T\_idtDrvHdlr *hdlr*, T\_idtApIIId *apIIInstId*, T\_idtApIConfig \* *apIConfig* )

Set APLL full configuration.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>apIIInstId</i>	APLL instance
<i>apIConfig</i>	APLL configuration

Definition at line 357 of file ApI.c.

#### 4.8.5.29 void IDTApl\_SetApIConfigPerOutput ( T\_idtDrvHdlr *hdlr*, T\_idtApIIId *apIIInstId*, T\_idtApIIOOutput *output*, T\_idtApIConfigPerOutput \* *apIConfigPerOutput* )

Set APLL per output configuration.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>apIIInstId</i>	APLL instance
<i>output</i>	Output port
<i>apIConfigPerOutput</i>	APLL per port configuration

Definition at line 272 of file ApII.c.

4.8.5.30 void IDTAplI.SetBypass ( T\_idtDrvHdlr *hdlr*, T\_idtApIIId *apIIInstId*, T\_idtApIIBypass *bypass* )

Function to set APLL bypass setting.

Parameters

<i>hdlr</i>	Device driver handler
<i>apIIInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>
<i>bypass</i>	Value to set bypass <ul style="list-style-type: none"> <li>• APLL_BYPASS_NORMAL_OP - Normal operation</li> <li>• APLL_BYPASS_BYPASS - Bypass VCXO, connect input to output</li> </ul>

Definition at line 1322 of file ApIIApi.c.

4.8.5.31 void IDTAplI.SetConfigSel ( T\_idtDrvHdlr *hdlr*, T\_idtApIIId *apIIInstId*, T\_idtApIIConfigSel *apIIConfig* )

Function to provision APLL based on input configuration.

Parameters

<i>hdlr</i>	Device driver handler
<i>apIIInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>
<i>apIIConfig</i>	APLL configuration <ul style="list-style-type: none"> <li>• APLL_CONFIG0 - configuration 0</li> <li>• APLL_CONFIG1 - configuration 1</li> </ul>

Definition at line 250 of file ApIIApi.c.

4.8.5.32 void IDTAplI.SetFeedbackDiv ( T\_idtDrvHdlr *hdlr*, T\_idtApIIId *apIIInstId*, T\_idtApIIConfigSel *apIIConfig*, T\_idtApIIDividerValue *div* )

Function to provision feedback (oscillator) divider value.

## Parameters

<i>hdr</i>	Device driver handler
<i>apllInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>
<i>apllConfig</i>	APLL configuration <ul style="list-style-type: none"> <li>• APLL_CONFIG0 - configuration 0</li> <li>• APLL_CONFIG1 - configuration 1</li> </ul>
<i>div</i>	Divisor value

Definition at line 588 of file ApllApi.c.

#### 4.8.5.33 void IDTApll\_SetFreqDoublersel ( T\_idtDrvHdr *hdr*, T\_idtApllId *apllInstId*, T\_idtApllFreqDoublersel *doublers* )

Function to enable/disable feedback frequency doubling.

## Parameters

<i>hdr</i>	Device driver handler
<i>apllInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>
<i>doublers</i>	Feedback frequency doubling value <ul style="list-style-type: none"> <li>• APLL_FREQ_SEL_SINGLE - Feedback frequency not doubled</li> <li>• APLL_FREQ_SEL_DOUBLE - Feedback frequency doubled</li> </ul>

Definition at line 921 of file ApllApi.c.

#### 4.8.5.34 void IDTApll\_SetInputClkSrc ( T\_idtDrvHdr *hdr*, T\_idtApllId *apllInstId*, T\_idtApllInputClkSrc *inputClk* )

Function to provision APLL input frequency source (external/internal)

## Parameters

<i>hdr</i>	Device driver handler
<i>apllInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>
<i>inputClk</i>	Input clock source for APLL <ul style="list-style-type: none"> <li>• APLL_CLK_SEL_EXTERNAL - external clock source</li> <li>• APLL_CLK_SEL_INTERNAL - internal clock source</li> </ul>

Definition at line 318 of file ApllApi.c.

4.8.5.35 void IDTAplI\_SetMasterResetSync ( T\_idtDrvHdlr *hdlr*, T\_idtAplIId *apIiInstId*, T\_idtAplIMasterResetSync *reset* )

Function to reset APLL.

Parameters

<i>hdlr</i>	Device driver handler
<i>apIiInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>
<i>reset</i>	Value to set master reset sync <ul style="list-style-type: none"> <li>• APLL_OUT_MR_SYNC - Normal operation</li> <li>• APLL_IN_MR_SYNC - In master sync reset</li> </ul>

Definition at line 1254 of file ApIiApi.c.

4.8.5.36 void IDTAplI\_SetOutputEnState ( T\_idtDrvHdlr *hdlr*, T\_idtAplIId *apIiInstId*, T\_idtAplIOutput *output*, T\_idtAplIOutputEn *enable* )

Function to control (enable/disable) output port.

Parameters

<i>hdlr</i>	Device driver handler
<i>apIiInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>
<i>output</i>	Output port <ul style="list-style-type: none"> <li>• APLL_OUTPUT_QA - Output port A</li> <li>• APLL_OUTPUT_QB - Output port B</li> </ul>
<i>enable</i>	Enable /Disable output <ul style="list-style-type: none"> <li>• APLL_OUTPUT_DISABLE - Disable output</li> <li>• APLL_OUTPUT_ENABLE - Enable output</li> </ul>

Definition at line 1199 of file ApIiApi.c.

4.8.5.37 void IDTAplI\_SetOutputSigType ( T\_idtDrvHdlr *hdlr*, T\_idtAplIId *apIiInstId*, T\_idtAplIOutput *output*, T\_idtAplIOutputSigType *outputSigType* )

Function to provision output port signal type.

Parameters

<i>hdlr</i>	Device driver handler
<i>apIiInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>

<i>output</i>	Output port <ul style="list-style-type: none"> <li>• APLL_OUTPUT_QA - Output port A</li> <li>• APLL_OUTPUT_QB - Output port B</li> </ul>
<i>outputSigType</i>	output signal type <ul style="list-style-type: none"> <li>• APLL_OUT_SIG_LVPECL - Output LVPECL signal</li> <li>• APLL_OUT_SIG_LVDS - Output LVDS signal</li> </ul>

Definition at line 1088 of file AplApi.c.

4.8.5.38 void IDTAplI.SetPreDiv ( T\_idtDrvHdlr *hdlr*, T\_idtAplIId *apllInstId*, T\_idtAplIConfigSel *apllConfig*, T\_idtAplIDividerValue *div* )

Function to provision pre- (input) divider value.

#### Parameters

<i>hdlr</i>	Device driver handler
<i>apllInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>
<i>apllConfig</i>	APLL configuration <ul style="list-style-type: none"> <li>• APLL_CONFIG0 - configuration 0</li> <li>• APLL_CONFIG1 - configuration 1</li> </ul>
<i>div</i>	Divisor value

Definition at line 438 of file AplApi.c.

4.8.5.39 void IDTAplI.SetQaDiv ( T\_idtDrvHdlr *hdlr*, T\_idtAplIId *apllInstId*, T\_idtAplIConfigSel *config*, T\_idtAplIQaDiv *div* )

Function to provision output port A divisor.



## Parameters

<i>hdr</i>	Device driver handler
<i>apllInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>
<i>config</i>	APLL configuration <ul style="list-style-type: none"> <li>• APLL_CONFIG0 - configuration 0</li> <li>• APLL_CONFIG1 - configuration 1</li> </ul>
<i>div</i>	Divisor value <ul style="list-style-type: none"> <li>• APLL_QA_ODSEL_DIV_25 - divide by 25</li> <li>• APLL_QA_ODSEL_DIV_5 - divide by 5</li> <li>• APLL_QA_ODSEL_DIV_4 - divide by 4</li> <li>• APLL_QA_ODSEL_DIV_2 - divide by 2</li> <li>• APLL_QA_ODSEL_DIV_1 - divide by 1</li> </ul>

Definition at line 718 of file ApIIApi.c.

4.8.5.40 void IDTApll\_SetQbDiv ( T\_idtDrvHdr *hdr*, T\_idtApIIId *apllInstId*, T\_idtApIIConfigSel *config*, T\_idtApIIQbDiv *div* )

Function to provision output port B divisor.

## Parameters

<i>hdr</i>	Device driver handler
<i>apllInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>
<i>config</i>	APLL configuration <ul style="list-style-type: none"> <li>• APLL_CONFIG0 - configuration 0</li> <li>• APLL_CONFIG1 - configuration 1</li> </ul>
<i>div</i>	Divisor value <ul style="list-style-type: none"> <li>• APLL_QB_ODSEL_DIV_8 - divide by 8</li> <li>• APLL_QB_ODSEL_DIV_5 - divide by 5</li> <li>• APLL_QB_ODSEL_DIV_4 - divide by 4</li> <li>• APLL_QB_ODSEL_DIV_2 - divide by 2</li> <li>• APLL_QB_ODSEL_DIV_1 - divide by 1</li> </ul>

Definition at line 835 of file ApIIApi.c.

4.8.5.41 void IDTApll\_SetShutoff ( T\_idtDrvHdr *hdr*, T\_idtApIIId *apllInstId*, T\_idtApIIShutoff *shutoff* )

Function to set APLL shutoff setting.

## Parameters

<i>hdr</i>	Device driver handler
<i>apllInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>
<i>shutoff</i>	Value to set shutoff <ul style="list-style-type: none"> <li>• APLL_SHUTOFF_NORMAL_OP - Normal operation</li> <li>• APLL_SHUTOFF_SHUTOFF - VCXO shutoff</li> </ul>

Definition at line 1390 of file ApIApi.c.

#### 4.8.5.42 void IDTApll\_SetXtalId ( T\_idtDrvHdlr *hdr*, T\_idtApllId *apllInstId*, T\_idtApllXtalId *xtal* )

Function to select oscillator.

## Parameters

<i>hdr</i>	Device driver handler
<i>apllInstId</i>	APLL instance <ul style="list-style-type: none"> <li>• APLL_INST_1 - APLL #1</li> <li>• APLL_INST_2 - APLL #2</li> </ul>
<i>xtal</i>	Oscillator to select <ul style="list-style-type: none"> <li>• APLL_XTAL_1_APLL1 - XTAL1 for APLL1</li> <li>• APLL_XTAL_2_APLL2 - XTAL2 for APLL2</li> <li>• APLL_XTAL_3_APLL1 - XTAL3 for APLL1</li> <li>• APLL_XTAL_4_APLL2 - XTAL4 for APLL2</li> </ul>

Definition at line 991 of file ApIApi.c.

#### 4.8.5.43 void IDTApll\_Switch2NonActiveAplIConfig ( T\_idtDrvHdlr *hdr*, T\_idtApllId *apllId* )

Switch to non-active APLL configuration.

## Parameters

<i>hdr</i>	Device driver handler
<i>apllId</i>	APLL instance

Definition at line 733 of file ApI.c.

#### 4.8.5.44 T\_osBool IDTApll\_ValidXtalInput ( const T\_idtDrvDeviceConfig \* *deviceConfig*, T\_idtApllXtal \* *xtalList*, T\_osUInt8 *numberOfXtal* )

Checks if there is input XTAL information is valid for the device.

## Parameters

<i>deviceConfig</i>	APLL device configuration
<i>xtalList</i>	List of XTAL information for the device
<i>numberOfXtal</i>	Number of XTAL in the xtalList

**Returns**

TRUE, if input XTAL information is valid; FALSE, otherwise

Definition at line 834 of file ApII.c.

**4.8.5.45 T\_osBool IDTApII\_XtalConfigured ( T\_idtDrvHdlr *hdlr*, T\_idtApIIId *apIIId* )**

Checks if there is any XTAL configured for the APLL.

**Parameters**

<i>hdlr</i>	Device driver handler
<i>apIIId</i>	APLL instance

**Returns**

TRUE, if there is at least one XTAL configured; FALSE, otherwise

Definition at line 790 of file ApII.c.



## Chapter 5

# Data Structure Documentation

### 5.1 bucketReg\_t Struct Reference

Structure used to store leaky bucket register offsets.

#### Data Fields

- T\_osUInt8 [upperThreshReg\\_m](#)
- T\_osUInt8 [lowerThreshReg\\_m](#)
- T\_osUInt8 [bucketSizeReg\\_m](#)
- T\_osUInt8 [decayRateReg\\_m](#)

#### 5.1.1 Detailed Description

Structure used to store leaky bucket register offsets.

Definition at line 47 of file Input.c.

#### 5.1.2 Field Documentation

##### 5.1.2.1 T\_osUInt8 bucketSizeReg\_m

Bucket size register offset

Definition at line 51 of file Input.c.

##### 5.1.2.2 T\_osUInt8 decayRateReg\_m

Decay rate register offset

Definition at line 52 of file Input.c.

##### 5.1.2.3 T\_osUInt8 lowerThreshReg\_m

Lower threshold register offset

Definition at line 50 of file Input.c.

#### 5.1.2.4 T\_osUInt8 upperThreshReg\_m

Upper threshold register offset

Definition at line 49 of file Input.c.

The documentation for this struct was generated from the following file:

- [common/src/Input.c](#)

## 5.2 T\_idtApIIConfig::fbDiv\_s Struct Reference

```
#include <ApI1.h>
```

### Data Fields

- [T\\_idtApIIDividerValue fbDivConfig0](#)
- [T\\_idtApIIDividerValue fbDivConfig1](#)

#### 5.2.1 Detailed Description

Definition at line 95 of file ApI1.h.

#### 5.2.2 Field Documentation

##### 5.2.2.1 T\_idtApIIDividerValue fbDivConfig0

APLL feedback divider value for configuration 0

Definition at line 97 of file ApI1.h.

##### 5.2.2.2 T\_idtApIIDividerValue fbDivConfig1

APLL feedback divider value for configuration 1

Definition at line 98 of file ApI1.h.

The documentation for this struct was generated from the following file:

- [common/include/ApI1.h](#)

## 5.3 globalArgs\_t Struct Reference

Structure to define program command line arguments.

### Data Fields

- T\_osUInt32 [modes\\_m](#)
- char [filename\\_ma](#) [SAMPLE\_MAX\_FILENAME]
- T\_osUInt32 [inputFreq\\_m](#) [IDT\_DRV\_MAX\_INPUT]
- [outputFrequency\\_t](#) [outFreq\\_m](#) [IDT\_DRV\_MAX\_OUTPUT]
- T\_idtDpllType [dpll\\_m](#) [IDT\_DRV\_MAX\_OUTPUT]

- T\_osUInt8 [isSim\\_m](#)
- T\_osUInt8 [dcoMode\\_m](#)
- long [offset\\_m](#)
- T\_osUInt8 [numberOfXtal](#)
- T\_idtApplXtal \* [xtalList](#)
- T\_DpllProfile [dpllProfile\\_ma](#) [DPLL\_INSTANCE\_MAX]
- T\_osUInt8 [sampleConfig\\_m](#)
- T\_osUInt8 [regOffset\\_m](#)
- T\_osUInt8 [regValue\\_m](#)

### 5.3.1 Detailed Description

Structure to define program command line arguments.

Definition at line 127 of file main.c.

### 5.3.2 Field Documentation

#### 5.3.2.1 T\_osUInt8 dcoMode\_m

Enable/Disable

DCO mode

Definition at line 143 of file main.c.

#### 5.3.2.2 T\_idtDpllType dpll\_m[IDT\_DRV\_MAX\_OUTPUT]

Select DPLL T0 / T4

Definition at line 138 of file main.c.

#### 5.3.2.3 T\_DpllProfile dpllProfile\_ma[DPLL\_INSTANCE\_MAX]

Dpll Profile

Definition at line 148 of file main.c.

#### 5.3.2.4 char filename\_ma[SAMPLE\_MAX\_FILENAME]

File name for

load/store

Definition at line 130 of file main.c.

#### 5.3.2.5 T\_osUInt32 inputFreq\_m[IDT\_DRV\_MAX\_INPUT]

Input frequency (kHz)

Definition at line 132 of file main.c.

### 5.3.2.6 T\_osUInt8 isSim\_m

Switch to

simulated mode

Definition at line 141 of file main.c.

### 5.3.2.7 T\_osUInt32 modes\_m

Operation modes

for program

Definition at line 128 of file main.c.

### 5.3.2.8 T\_osUInt8 numberOfXtal

Number APLL external Xtals

Definition at line 146 of file main.c.

### 5.3.2.9 long offset\_m

DCO Offset

Definition at line 145 of file main.c.

### 5.3.2.10 outputFrequency\_t outFreq\_m[IDT\_DRV\_MAX\_OUTPUT]

Output frequency (enum)

Definition at line 135 of file main.c.

### 5.3.2.11 T\_osUInt8 regOffset\_m

register offset

Definition at line 151 of file main.c.

### 5.3.2.12 T\_osUInt8 regValue\_m

register value

Definition at line 152 of file main.c.

### 5.3.2.13 T\_osUInt8 sampleConfig\_m

Sample configuration

Definition at line 150 of file main.c.

### 5.3.2.14 T\_idtApIIXtal\* xtalList

APLL external Xtal list

Definition at line 147 of file main.c.



The documentation for this struct was generated from the following file:

- 82V3910/sample/src/main.c

## 5.4 T\_idtApllConfig::outputConfig\_s Struct Reference

```
#include <Apl1.h>
```

### Data Structures

- struct [qaConfig\\_s](#)
- struct [qbConfig\\_s](#)

### Data Fields

- struct [T\\_idtApllConfig::outputConfig\\_s::qaConfig\\_s](#) qaConfig
- struct [T\\_idtApllConfig::outputConfig\\_s::qbConfig\\_s](#) qbConfig

#### 5.4.1 Detailed Description

Definition at line 118 of file Apl1.h.

#### 5.4.2 Field Documentation

5.4.2.1 struct [T\\_idtApllConfig::outputConfig\\_s::qaConfig\\_s](#) qaConfig

5.4.2.2 struct [T\\_idtApllConfig::outputConfig\\_s::qbConfig\\_s](#) qbConfig

The documentation for this struct was generated from the following file:

- common/include/Apl1.h

## 5.5 T\_idtApllConfig::outputDiv\_s Struct Reference

```
#include <Apl1.h>
```

### Data Structures

- struct [qaDiv\\_s](#)
- struct [qbDiv\\_s](#)

### Data Fields

- struct [T\\_idtApllConfig::outputDiv\\_s::qaDiv\\_s](#) qaDiv
- struct [T\\_idtApllConfig::outputDiv\\_s::qbDiv\\_s](#) qbDiv

### 5.5.1 Detailed Description

Definition at line 100 of file AplI.h.

### 5.5.2 Field Documentation

5.5.2.1 struct T\_idtAplIConfig::outputDiv\_s::qaDiv\_s qaDiv

5.5.2.2 struct T\_idtAplIConfig::outputDiv\_s::qbDiv\_s qbDiv

The documentation for this struct was generated from the following file:

- [common/include/AplI.h](#)

## 5.6 pathSelectorConfig\_t Struct Reference

Structure containing select configuration. Used to translate between frequency and output path configuration.

```
#include <outputFreq_priv.h>
```

### Data Fields

- [pathSelectors\\_t selector\\_m](#)
- int [value\\_m](#)
- T\_osUInt8 [outputDivider\\_m](#)
- T\_osUInt8 [outputPathSelector\\_m](#)
- T\_osUInt8 [instance\\_m](#)

### 5.6.1 Detailed Description

Structure containing select configuration. Used to translate between frequency and output path configuration.

Definition at line 69 of file outputFreq\_priv.h.

### 5.6.2 Field Documentation

5.6.2.1 T\_osUInt8 instance\_m

instance of this configuration

Definition at line 74 of file outputFreq\_priv.h.

5.6.2.2 T\_osUInt8 outputDivider\_m

Output divider value

Definition at line 72 of file outputFreq\_priv.h.

5.6.2.3 T\_osUInt8 outputPathSelector\_m

Output path selector

Definition at line 73 of file outputFreq\_priv.h.

#### 5.6.2.4 pathSelectors\_t selector\_m

Path selector

Definition at line 70 of file outputFreq\_priv.h.

#### 5.6.2.5 int value\_m

Path selector value

Definition at line 71 of file outputFreq\_priv.h.

The documentation for this struct was generated from the following file:

- [common/hlapi/include/outputFreq\\_priv.h](#)

## 5.7 pathSelectorIndex\_t Struct Reference

Structure to index to path selector configs.

```
#include <outputFreq_priv.h>
```

### Data Fields

- int [start\\_m](#)
- int [size\\_m](#)

### 5.7.1 Detailed Description

Structure to index to path selector configs.

Definition at line 78 of file outputFreq\_priv.h.

### 5.7.2 Field Documentation

#### 5.7.2.1 int size\_m

Number of entries

Definition at line 80 of file outputFreq\_priv.h.

#### 5.7.2.2 int start\_m

Start index

Definition at line 79 of file outputFreq\_priv.h.

The documentation for this struct was generated from the following file:

- [common/hlapi/include/outputFreq\\_priv.h](#)

## 5.8 T\_idtApllConfig::preDiv\_s Struct Reference

```
#include <Apl1.h>
```

## Data Fields

- [T\\_idtApIldividerValue preDivConfig0](#)
- [T\\_idtApIldividerValue preDivConfig1](#)

### 5.8.1 Detailed Description

Definition at line 90 of file ApI.h.

### 5.8.2 Field Documentation

#### 5.8.2.1 T\_idtApIldividerValue preDivConfig0

APLL pre-divider value for configuration 0

Definition at line 92 of file ApI.h.

#### 5.8.2.2 T\_idtApIldividerValue preDivConfig1

APLL pre-divider value for configuration 1

Definition at line 93 of file ApI.h.

The documentation for this struct was generated from the following file:

- [common/include/ApI.h](#)

## 5.9 T\_idtApIConfig::outputConfig\_s::qaConfig\_s Struct Reference

```
#include <ApI.h>
```

## Data Fields

- [T\\_idtApIOutputSigType outputSigType](#)
- [T\\_idtApIOutputEn enOutput](#)

### 5.9.1 Detailed Description

Definition at line 120 of file ApI.h.

### 5.9.2 Field Documentation

#### 5.9.2.1 T\_idtApIOutputEn enOutput

APLL QA output enable

Definition at line 123 of file ApI.h.

### 5.9.2.2 T\_idtApIOutputSigType outputSigType

APLL QA output signal type

Definition at line 122 of file ApI.h.

The documentation for this struct was generated from the following file:

- [common/include/ApI.h](#)

## 5.10 T\_idtApIConfig::outputDiv\_s::qaDiv\_s Struct Reference

```
#include <ApI.h>
```

### Data Fields

- [T\\_idtApIDividerValue outputDivConfig0](#)
- [T\\_idtApIDividerValue outputDivConfig1](#)

### 5.10.1 Detailed Description

Definition at line 102 of file ApI.h.

### 5.10.2 Field Documentation

#### 5.10.2.1 T\_idtApIDividerValue outputDivConfig0

APLL QA output divider value for configuration 0

Definition at line 104 of file ApI.h.

#### 5.10.2.2 T\_idtApIDividerValue outputDivConfig1

APLL QB output divider value for configuration 1

Definition at line 105 of file ApI.h.

The documentation for this struct was generated from the following file:

- [common/include/ApI.h](#)

## 5.11 T\_idtApIConfig::outputConfig\_s::qbConfig\_s Struct Reference

```
#include <ApI.h>
```

### Data Fields

- [T\\_idtApIOutputSigType outputSigType](#)
- [T\\_idtApIOutputEn enOutput](#)

### 5.11.1 Detailed Description

Definition at line 125 of file ApI.h.

## 5.11.2 Field Documentation

### 5.11.2.1 T\_idtApIOutputEn enOutput

APLL QB output enable

Definition at line 128 of file ApI.h.

### 5.11.2.2 T\_idtApIOutputSigType outputSigType

APLL QB output signal type

Definition at line 127 of file ApI.h.

The documentation for this struct was generated from the following file:

- [common/include/ApI.h](#)

## 5.12 T\_idtApIConfig::outputDiv\_s::qbDiv\_s Struct Reference

```
#include <ApI.h>
```

### Data Fields

- [T\\_idtApIDividerValue outputDivConfig0](#)
- [T\\_idtApIDividerValue outputDivConfig1](#)

### 5.12.1 Detailed Description

Definition at line 107 of file ApI.h.

### 5.12.2 Field Documentation

#### 5.12.2.1 T\_idtApIDividerValue outputDivConfig0

APLL QB output divider value for configuration 0

Definition at line 109 of file ApI.h.

#### 5.12.2.2 T\_idtApIDividerValue outputDivConfig1

APLL QB output divider value for configuration 1

Definition at line 110 of file ApI.h.

The documentation for this struct was generated from the following file:

- [common/include/ApI.h](#)

## 5.13 T\_apIOutputFrequencyEntry Struct Reference

Structure used to translate APLL configuration and output port frequency.

## Data Fields

- [T\\_idtApIDividerValue apIDivVal\\_m](#)
- [outputFrequency\\_t frequencies\\_m \[APLL\\_XTAL\\_FREQ\\_MAX\]](#)

### 5.13.1 Detailed Description

Structure used to translate APLL configuration and output port frequency.

Definition at line 67 of file outputFreqString.c.

### 5.13.2 Field Documentation

#### 5.13.2.1 T\_idtApIDividerValue apIDivVal\_m

Divider value

Definition at line 68 of file outputFreqString.c.

#### 5.13.2.2 outputFrequency\_t frequencies\_m[APLL\_XTAL\_FREQ\_MAX]

Definition at line 71 of file outputFreqString.c.

The documentation for this struct was generated from the following file:

- [common/hlapi/src/outputFreqString.c](#)

## 5.14 T\_idtApIConfig Struct Reference

Structure containing APLL full configuration.

```
#include <ApI.h>
```

## Data Structures

- struct [fbDiv\\_s](#)
- struct [outputConfig\\_s](#)
- struct [outputDiv\\_s](#)
- struct [preDiv\\_s](#)

## Data Fields

- [T\\_idtApIConfigSel apICfg](#)
- [T\\_idtApIInputClkSrc inputClk](#)
- struct [T\\_idtApIConfig::preDiv\\_s](#) preDiv
- struct [T\\_idtApIConfig::fbDiv\\_s](#) fbDiv
- struct [T\\_idtApIConfig::outputDiv\\_s](#) outputDiv
- [T\\_idtApIFreqDoublerSel dbleSel](#)
- [T\\_idtApIMasterResetSync mrSync](#)
- [T\\_idtApIBypass byPass](#)
- [T\\_idtApIShutoff shutOff](#)
- [T\\_idtApIXtalId xtal](#)
- struct [T\\_idtApIConfig::outputConfig\\_s](#) outputConfig

### 5.14.1 Detailed Description

Structure containing APLL full configuration.

Definition at line 86 of file Apll.h.

### 5.14.2 Field Documentation

#### 5.14.2.1 T\_idtApIConfigSel apIICfg

APLL stored register configuration selection

Definition at line 88 of file Apll.h.

#### 5.14.2.2 T\_idtApIIBypass byPass

APLL bypass configuration

Definition at line 115 of file Apll.h.

#### 5.14.2.3 T\_idtApIIFreqDoublersel dbleSel

APLL frequency doubler in feedback path

Definition at line 113 of file Apll.h.

#### 5.14.2.4 struct T\_idtApIConfig::fbDiv\_s fbDiv

#### 5.14.2.5 T\_idtApIInputClkSrc inputClk

APLL sourced clock selection

Definition at line 89 of file Apll.h.

#### 5.14.2.6 T\_idtApIIMasterResetSync mrSync

APLL Master reset sync

Definition at line 114 of file Apll.h.

#### 5.14.2.7 struct T\_idtApIConfig::outputConfig\_s outputConfig

#### 5.14.2.8 struct T\_idtApIConfig::outputDiv\_s outputDiv

#### 5.14.2.9 struct T\_idtApIConfig::preDiv\_s preDiv

#### 5.14.2.10 T\_idtApIIShutoff shutOff

APLL shut off mode

Definition at line 116 of file Apll.h.

#### 5.14.2.11 T\_idtApIIXtalId xtal

APLL crystal selection



Definition at line 117 of file ApI.h.

The documentation for this struct was generated from the following file:

- [common/include/ApI.h](#)

## 5.15 T\_idtApIConfigPerOutput Struct Reference

Structure containing APLL per output configuration.

```
#include <ApI.h>
```

### Data Fields

- [T\\_idtApIConfigSel](#) apIcFg
- [T\\_idtApIInputClkSrc](#) inputClk
- [T\\_idtApIDividerValue](#) preDiv
- [T\\_idtApIDividerValue](#) fbDiv
- [T\\_idtApIDividerValue](#) outputDiv
- [T\\_idtApIFreqDoublerSel](#) dbleSel
- [T\\_idtApIXtalId](#) xtal
- [T\\_idtApIOutputSigType](#) sigType
- [T\\_idtApIOutputEn](#) enOutput

### 5.15.1 Detailed Description

Structure containing APLL per output configuration.

Definition at line 70 of file ApI.h.

### 5.15.2 Field Documentation

#### 5.15.2.1 T\_idtApIConfigSel apIcFg

APLL stored register configuration selection

Definition at line 72 of file ApI.h.

#### 5.15.2.2 T\_idtApIFreqDoublerSel dbleSel

APLL frequency doubler in feedback path

Definition at line 77 of file ApI.h.

#### 5.15.2.3 T\_idtApIOutputEn enOutput

APLL output enable

Definition at line 80 of file ApI.h.

#### 5.15.2.4 T\_idtApIDividerValue fbDiv

APLL feedback divider value

Definition at line 75 of file ApI.h.

### 5.15.2.5 T\_idtApIInputClkSrc inputClk

APLL sourced clock selection

Definition at line 73 of file ApI.h.

### 5.15.2.6 T\_idtApIDividerValue outputDiv

APLL output divider value

Definition at line 76 of file ApI.h.

### 5.15.2.7 T\_idtApIDividerValue preDiv

APLL pre-divider value

Definition at line 74 of file ApI.h.

### 5.15.2.8 T\_idtApIOutputSigType sigType

APLL output signal configuration

Definition at line 79 of file ApI.h.

### 5.15.2.9 T\_idtApIXtalId xtal

APLL crystal selection

Definition at line 78 of file ApI.h.

The documentation for this struct was generated from the following file:

- [common/include/ApI.h](#)

## 5.16 T\_idtApIFreqMapping Struct Reference

Type definition for mapping output frequency to APLL configuration.

```
#include <ApIIFreqProfile.h>
```

### Data Fields

- [T\\_idtApIInputFreqType apIInputFreq](#)
- [T\\_idtApIDividerValue apIPreDivider](#)
- [T\\_idtApIDividerValue apIFbDivider](#)
- [T\\_idtApIXtalType apIXtalFreq](#)
- [T\\_idtApIDividerValue apIOutputDivider](#)
- [T\\_idtApIOutputFreqType apIOutputFreq](#)
- [T\\_idtApIOutputSupportedType apIOutputs](#)

### 5.16.1 Detailed Description

Type definition for mapping output frequency to APLL configuration.

Definition at line 100 of file ApIIFreqProfile.h.

## 5.16.2 Field Documentation

### 5.16.2.1 T\_idtApIIDividerValue apIFbDivider

Feedback (oscillator) divider

Definition at line 104 of file ApIFreqProfile.h.

### 5.16.2.2 T\_idtApIInputFreqType apIInputFreq

Input frequency

Definition at line 102 of file ApIFreqProfile.h.

### 5.16.2.3 T\_idtApIDividerValue apIOutputDivider

Output divider

Definition at line 106 of file ApIFreqProfile.h.

### 5.16.2.4 T\_idtApIOutputFreqType apIOutputFreq

Output frequency type

Definition at line 107 of file ApIFreqProfile.h.

### 5.16.2.5 T\_idtApIOutputSupportedType apIOutputs

Output supported (A or B or both)

Definition at line 108 of file ApIFreqProfile.h.

### 5.16.2.6 T\_idtApIDividerValue apIPreDivider

Pre- (input) divider

Definition at line 103 of file ApIFreqProfile.h.

### 5.16.2.7 T\_idtApIIXtalType apIIXtalFreq

Oscillator type

Definition at line 105 of file ApIFreqProfile.h.

The documentation for this struct was generated from the following file:

- [apI/include/ApIFreqProfile.h](#)

## 5.17 T\_idtApIIXtal Struct Reference

Structure containing APLL crystal id and frequency information.

```
#include <ApITypeDef.h>
```

## Data Fields

- [T\\_idtApIIXtalId aplIIXtalId](#)
- [T\\_idtApIIXtalType aplIIXtalFreq](#)

### 5.17.1 Detailed Description

Structure containing APLL crystal id and frequency information.

Definition at line 244 of file ApIITypeDef.h.

### 5.17.2 Field Documentation

#### 5.17.2.1 T\_idtApIIXtalType aplIIXtalFreq

APLL crystal frequency

Definition at line 247 of file ApIITypeDef.h.

#### 5.17.2.2 T\_idtApIIXtalId aplIIXtalId

APLL crystal ID

Definition at line 246 of file ApIITypeDef.h.

The documentation for this struct was generated from the following file:

- [apll/include/ApIITypeDef.h](#)

## 5.18 T\_idtApIIXtalList Struct Reference

Wrapper structure containing APLL crystal id and frequency information.

```
#include <access.h>
```

## Data Fields

- int [xtal1ApI1](#)
- [T\\_idtApIIXtalType xtal1ApI1Freq](#)
- int [xtal3ApI1](#)
- [T\\_idtApIIXtalType xtal3ApI1Freq](#)
- int [xtal2ApI2](#)
- [T\\_idtApIIXtalType xtal2ApI2Freq](#)
- int [xtal4ApI2](#)
- [T\\_idtApIIXtalType xtal4ApI2Freq](#)

### 5.18.1 Detailed Description

Wrapper structure containing APLL crystal id and frequency information.

This structure is used for TCL extension library

Definition at line 50 of file access.h.

## 5.18.2 Field Documentation

### 5.18.2.1 int xtal1ApI1

APLL1 XTAL1 flag

Definition at line 52 of file access.h.

### 5.18.2.2 T\_idtApIIXtalType xtal1ApI1Freq

APLL1 XTAL1 Frequency

Definition at line 53 of file access.h.

### 5.18.2.3 int xtal2ApI2

APLL2 XTAL2 flag

Definition at line 56 of file access.h.

### 5.18.2.4 T\_idtApIIXtalType xtal2ApI2Freq

APLL2 XTAL2 Frequency

Definition at line 57 of file access.h.

### 5.18.2.5 int xtal3ApI1

APLL1 XTAL3 flag

Definition at line 54 of file access.h.

### 5.18.2.6 T\_idtApIIXtalType xtal3ApI1Freq

APLL1 XTAL3 Frequency

Definition at line 55 of file access.h.

### 5.18.2.7 int xtal4ApI2

APLL2 XTAL4 flag

Definition at line 58 of file access.h.

### 5.18.2.8 T\_idtApIIXtalType xtal4ApI2Freq

APLL2 XTAL4 Frequency

Definition at line 59 of file access.h.

The documentation for this struct was generated from the following file:

- 82V3910/sample/include/[access.h](#)

## 5.19 T\_idtDrvAccess Struct Reference

Initialization structure detailing device access information for device driver.

```
#include <Define.h>
```

### Data Fields

- [T\\_idtAccessInitFunc initFunc\\_m](#)
- [T\\_idtAccessDelInitFunc deinitFunc\\_m](#)
- [T\\_idtReadFunc readFunc\\_m](#)
- [T\\_idtWriteFunc writeFunc\\_m](#)
- void \* [userData\\_m](#)

### 5.19.1 Detailed Description

Initialization structure detailing device access information for device driver.

Definition at line 193 of file Define.h.

### 5.19.2 Field Documentation

#### 5.19.2.1 T\_idtAccessDelInitFunc deinitFunc\_m

Access deinitialization

Definition at line 196 of file Define.h.

#### 5.19.2.2 T\_idtAccessInitFunc initFunc\_m

Access initialization

Definition at line 195 of file Define.h.

#### 5.19.2.3 T\_idtReadFunc readFunc\_m

Read function

Definition at line 197 of file Define.h.

#### 5.19.2.4 void\* userData\_m

Extra user data

Definition at line 199 of file Define.h.

#### 5.19.2.5 T\_idtWriteFunc writeFunc\_m

Write function

Definition at line 198 of file Define.h.

The documentation for this struct was generated from the following file:

- [common/include/Define.h](#)

## 5.20 T\_idtDrvDeviceConfig Struct Reference

Device type/variant information.

```
#include <Define.h>
```

### Data Fields

- T\_osUInt8 [inputExt2IntXlate\\_ma](#) [IDT\_DRV\_MAX\_INPUT+1]
- T\_osUInt8 [inSyncXlate\\_ma](#) [2]
- T\_osUInt8 [outputExt2IntXlate\\_ma](#) [IDT\_DRV\_MAX\_OUTPUT+1]
- [T\\_idtOutputApplConfig](#) [outPutApplConfig](#) [IDT\_DRV\_MAX\_OUTPUT+1]
- T\_osUInt8 [outSyntXlate\\_ma](#) [2]
- T\_osUInt8 [numberOfSonetGigEthPath\\_m](#)
- T\_osUInt8 [numberOfAppl\\_m](#)
- T\_osUInt8 [populatedAppl\\_ma](#) [APLL\_INST\_MAX]
- T\_osUInt8 [pllExt2IntXlate\\_ma](#) [DPLL\_INSTANCE\_MAX]
- T\_osUInt8 [pllInt2ExtXlate\\_ma](#) [DPLL\_INSTANCE\_MAX]
- [T\\_idtDpllType](#) [t0PllMode\\_m](#)
- T\_osUInt8 [dcoModeSupport\\_ma](#) [DPLL\_INSTANCE\_MAX]
- T\_osUInt8 [phaseSlopeLimiting\\_ma](#) [DPLL\_INSTANCE\_MAX]
- T\_osUInt8 [maxNumXtalPerAppl\\_m](#)
- T\_osUInt8 [supportedXtalId\\_ma](#) [APLL\_XTAL\_MAX]
- T\_osUInt8 [supportedXtalFreq\\_ma](#) [APLL\_XTAL\_MAX][APLL\_XTAL\_FREQ\_MAX]
- [T\\_idtInputFreqValid](#) [inputFreqValidFunc\\_m](#)
- [T\\_idtOutputFreqValid](#) [outputFreqValidFunc\\_m](#)

### 5.20.1 Detailed Description

Device type/variant information.

This data structure contains device variant information.

Definition at line 219 of file Define.h.

### 5.20.2 Field Documentation

#### 5.20.2.1 T\_osUInt8 dcoModeSupport\_ma[DPLL\_INSTANCE\_MAX]

DPLL support DCO mode

Definition at line 232 of file Define.h.

#### 5.20.2.2 T\_osUInt8 inputExt2IntXlate\_ma[IDT\_DRV\_MAX\_INPUT+1]

Input translation table (external to internal)

Definition at line 221 of file Define.h.

#### 5.20.2.3 T\_idtInputFreqValid inputFreqValidFunc\_m

Input frequency validation function

Definition at line 237 of file Define.h.

#### 5.20.2.4 T\_osUInt8 inSyncXlate\_ma[2]

Input sync translation table

Definition at line 222 of file Define.h.

#### 5.20.2.5 T\_osUInt8 maxNumXtalPerAppl\_m

Maximum number of XTALs per APLL

Definition at line 234 of file Define.h.

#### 5.20.2.6 T\_osUInt8 numberOfAppl\_m

Number of APLLs

Definition at line 227 of file Define.h.

#### 5.20.2.7 T\_osUInt8 numberOfSonetGigEthPath\_m

Number of Sonet GigE path

Definition at line 226 of file Define.h.

#### 5.20.2.8 T\_idtOutputApplConfig outPutApplConfig[IDT\_DRV\_MAX\_OUTPUT+1]

Output APLL configuration

Definition at line 224 of file Define.h.

#### 5.20.2.9 T\_osUInt8 outputExt2IntXlate\_ma[IDT\_DRV\_MAX\_OUTPUT+1]

Output translation table (external to internal)

Definition at line 223 of file Define.h.

#### 5.20.2.10 T\_idtOuputFreqValid outputFreqValidFunc\_m

Output frequency validation function

Definition at line 238 of file Define.h.

#### 5.20.2.11 T\_osUInt8 outSyntXlate\_ma[2]

Output sync translation table

Definition at line 225 of file Define.h.

#### 5.20.2.12 T\_osUInt8 phaseSlopeLimiting\_ma[DPLL\_INSTANCE\_MAX]

DPLL support phase slope limiting

Definition at line 233 of file Define.h.



## 5.20.2.13 T\_osUInt8 pllExt2IntXlate\_ma[DPLL\_INSTANCE\_MAX]

DPLL translation table (external to internal)

Definition at line 229 of file Define.h.

## 5.20.2.14 T\_osUInt8 pllInt2ExtXlate\_ma[DPLL\_INSTANCE\_MAX]

DPLL translation table (internal to external)

Definition at line 230 of file Define.h.

## 5.20.2.15 T\_osUInt8 populatedAppl\_ma[APLL\_INST\_MAX]

Populated APLL(s)

Definition at line 228 of file Define.h.

## 5.20.2.16 T\_osUInt8 supportedXtalFreq\_ma[APLL\_XTAL\_MAX][APLL\_XTAL\_FREQ\_MAX]

Supported XTAL frequency

Definition at line 236 of file Define.h.

## 5.20.2.17 T\_osUInt8 supportedXtalId\_ma[APLL\_XTAL\_MAX]

Supported XTAL id

Definition at line 235 of file Define.h.

## 5.20.2.18 T\_idtDpllType t0PllMode\_m

If T0 exists, T0 mode

Definition at line 231 of file Define.h.

The documentation for this struct was generated from the following file:

- [common/include/Define.h](#)

## 5.21 T\_idtDrvHdlr Struct Reference

Device driver handler.

```
#include <Define.h>
```

### Data Fields

- const char \* [name\\_m](#)
- [T\\_idtDeviceType](#) [deviceType\\_m](#)
- [T\\_idtDrvAccess](#) [drvAccess\\_m](#)
- const [T\\_idtDrvDeviceConfig](#) \* [deviceConfig\\_m](#)
- [T\\_osUInt8](#) [numberOfApplXtal\\_m](#)
- [T\\_idtApplXtal](#) [xtalList](#) [[IDT\\_DRV\\_MAX\\_APLL\\_XTAL](#)]
- struct [S\\_IDTPathConfiguration](#) \* [currOutPathCfg\\_mp](#)

- void \* [dpllI2CTransData\\_mp](#)
- void \* [apllI2CTransData\\_mp](#)
- [T\\_idtI2CAddrTransFunc i2cAddrTransFunc\\_m](#)
- [T\\_osUInt8 i2cAddr](#)

### 5.21.1 Detailed Description

Device driver handler.

All device driver functions have driver handlers as an input parameter. This handler allows the device driver to support an unlimited number devices.

Definition at line 255 of file Define.h.

### 5.21.2 Field Documentation

#### 5.21.2.1 void\* [apllI2CTransData\\_mp](#)

Helper data for translating I2C address mapping to apll register space

Definition at line 265 of file Define.h.

#### 5.21.2.2 struct [S\\_IDTPathConfiguration\\* currOutPathCfg\\_mp](#)

Current output path configuration - used by high level API code. Basic driver doesn't require this.

Definition at line 263 of file Define.h.

#### 5.21.2.3 const [T\\_idtDrvDeviceConfig\\* deviceConfig\\_m](#)

Device configuration

Definition at line 260 of file Define.h.

#### 5.21.2.4 [T\\_idtDeviceType deviceType\\_m](#)

Device Type

Definition at line 258 of file Define.h.

#### 5.21.2.5 void\* [dpllI2CTransData\\_mp](#)

Helper data for translating I2C address mapping to dpll register space

Definition at line 264 of file Define.h.

#### 5.21.2.6 [T\\_idtDrvAccess drvAccess\\_m](#)

Device access functions

Definition at line 259 of file Define.h.

#### 5.21.2.7 [T\\_osUInt8 i2cAddr](#)

7-bit unshifted i2c slave address for PLL

Definition at line 267 of file Define.h.

### 5.21.2.8 T\_idtI2CaddrTransFunc i2cAddrTransFunc\_m

Function to translate I2C address

Definition at line 266 of file Define.h.

### 5.21.2.9 const char\* name\_m

Name of driver instance

Definition at line 257 of file Define.h.

### 5.21.2.10 T\_osUInt8 numberOfApllXtal\_m

Number of APLL XTALs

Definition at line 261 of file Define.h.

### 5.21.2.11 T\_idtApllXtal xtalList[IDT\_DRV\_MAX\_APLL\_XTAL]

List of APLL XTALs

Definition at line 262 of file Define.h.

The documentation for this struct was generated from the following file:

- [common/include/Define.h](#)

## 5.22 T\_IDTFreq2bfVal Struct Reference

Structure to contain translation information for frequency to bitfield value.

### Data Fields

- T\_osUInt32 [freq\\_m](#)
- T\_idtInputFrequencyBitfieldValue [bfVal\\_m](#)

### 5.22.1 Detailed Description

Structure to contain translation information for frequency to bitfield value.

Definition at line 50 of file inputFreq.c.

### 5.22.2 Field Documentation

#### 5.22.2.1 T\_idtInputFrequencyBitfieldValue bfVal\_m

Bitfield value

Definition at line 52 of file inputFreq.c.

### 5.22.2.2 T\_osUInt32 freq\_m

Frequency (in Hz)

Definition at line 51 of file inputFreq.c.

The documentation for this struct was generated from the following file:

- [common/hlapi/src/inputFreq.c](#)

## 5.23 T\_idtHfDivEntry Struct Reference

Structure to use as high frequency (HF) divider information.

### Data Fields

- [T\\_osUInt8 divValue\\_m](#)
- [T\\_idtHighFrequencyDivisor hfDivValue\\_m](#)

### 5.23.1 Detailed Description

Structure to use as high frequency (HF) divider information.

Definition at line 58 of file inputFreq.c.

### 5.23.2 Field Documentation

#### 5.23.2.1 T\_osUInt8 divValue\_m

Divisor value

Definition at line 59 of file inputFreq.c.

#### 5.23.2.2 T\_idtHighFrequencyDivisor hfDivValue\_m

```
HF divisor bit field
```

value

Definition at line 60 of file inputFreq.c.

The documentation for this struct was generated from the following file:

- [common/hlapi/src/inputFreq.c](#)

## 5.24 T\_idtI2CtransData Struct Reference

I2C address translation information used internally by the driver.

```
#include <General.h>
```

### Data Fields

- [T\\_osUInt8 bitLocation](#)
- [T\\_osUInt8 bitValue](#)

### 5.24.1 Detailed Description

I2C address translation information used internally by the driver.

Definition at line 78 of file General.h.

### 5.24.2 Field Documentation

#### 5.24.2.1 T\_osUInt8 bitLocation

Definition at line 80 of file General.h.

#### 5.24.2.2 T\_osUInt8 bitValue

Definition at line 81 of file General.h.

The documentation for this struct was generated from the following file:

- [common/include/General.h](#)

## 5.25 T\_idtOutputApIConfig Struct Reference

Structure containing APLL inforatmion.

```
#include <Define.h>
```

### Data Fields

- [T\\_idtApIId apIInst](#)
- [T\\_osUInt8 apIInput](#)
- [T\\_idtApIOutput apIOutput](#)
- [T\\_osUInt8 extOutput](#)

### 5.25.1 Detailed Description

Structure containing APLL inforatmion.

Definition at line 205 of file Define.h.

### 5.25.2 Field Documentation

#### 5.25.2.1 T\_osUInt8 apIInput

APLL input port number

Definition at line 208 of file Define.h.

#### 5.25.2.2 T\_idtApIId apIInst

APLL instanace ID

Definition at line 207 of file Define.h.

### 5.25.2.3 T\_idtApIOutput apIOutput

APLL output port number

Definition at line 209 of file Define.h.

### 5.25.2.4 T\_osUInt8 extOutput

External output port number

Definition at line 210 of file Define.h.

The documentation for this struct was generated from the following file:

- [common/include/Define.h](#)

## 5.26 T\_IDTPathConfiguration Struct Reference

Structure containing output path configuration.

```
#include <Dpll.h>
```

### Data Fields

- [networkType\\_t networkType\\_m](#)
- [T\\_idtDpllOutputSelectorA T0SelA\\_m](#)
- [T\\_idtDpllOutputSelectorB T0SelB\\_m](#)
- [T\\_idtDpllOutputSelectorA T4SelA\\_m](#)
- [T\\_idtDpllOutputSelectorB T4SelB\\_m](#)
- [T\\_idtSonetGigEthOutput sonetGigEthSel\\_ma \[SonetGigEthSel\\_NUMMAX\]](#)

### 5.26.1 Detailed Description

Structure containing output path configuration.

Definition at line 114 of file Dpll.h.

### 5.26.2 Field Documentation

#### 5.26.2.1 networkType\_t networkType\_m

Network type

Definition at line 115 of file Dpll.h.

#### 5.26.2.2 T\_idtSonetGigEthOutput sonetGigEthSel\_ma[SonetGigEthSel\_NUMMAX]

Sonet/GigE Output Path Selector

Definition at line 122 of file Dpll.h.

#### 5.26.2.3 T\_idtDpllOutputSelectorA T0SelA\_m

T0 Output Path Selector A

Definition at line 116 of file Dpll.h.

#### 5.26.2.4 T\_idtDpllOutputSelectorB T0SelB\_m

T0 Output Path Selector B

Definition at line 117 of file Dpll.h.

#### 5.26.2.5 T\_idtDpllOutputSelectorA T4SelA\_m

T4 Output Path Selector A

Definition at line 118 of file Dpll.h.

#### 5.26.2.6 T\_idtDpllOutputSelectorB T4SelB\_m

T4 Output Path Selector B

Definition at line 119 of file Dpll.h.

The documentation for this struct was generated from the following file:

- [common/include/Dpll.h](#)

## 5.27 T\_idtSonetGigEthBitfield2PathConfig Struct Reference

Structure Translate from Sonet/GigE bitfield to path configuration.

### Data Fields

- [T\\_idtDpllInstance inputDpll\\_m](#)
- [T\\_idtSonetGigEthOutput outputFreq\\_m](#)

### 5.27.1 Detailed Description

Structure Translate from Sonet/GigE bitfield to path configuration.

Definition at line 51 of file DpllCnfg.c.

### 5.27.2 Field Documentation

#### 5.27.2.1 T\_idtDpllInstance inputDpll\_m

input DPLL type

Definition at line 53 of file DpllCnfg.c.

#### 5.27.2.2 T\_idtSonetGigEthOutput outputFreq\_m

output frequency

Definition at line 54 of file DpllCnfg.c.

The documentation for this struct was generated from the following file:

- [common/src/DpllCnfg.c](#)

## 5.28 T\_SampleConfigEntry Struct Reference

Sample configuration information.

### Data Fields

- [T\\_SampleConfigFunc configFunction\\_m](#)
- [T\\_SampleConfigDescrFunc configDescription\\_m](#)

### 5.28.1 Detailed Description

Sample configuration information.

Definition at line 75 of file main.c.

### 5.28.2 Field Documentation

#### 5.28.2.1 T\_SampleConfigDescrFunc configDescription\_m

Function to output description

Definition at line 77 of file main.c.

#### 5.28.2.2 T\_SampleConfigFunc configFunction\_m

Function to configure

Definition at line 76 of file main.c.

The documentation for this struct was generated from the following file:

- 82V3910/sample/src/[main.c](#)



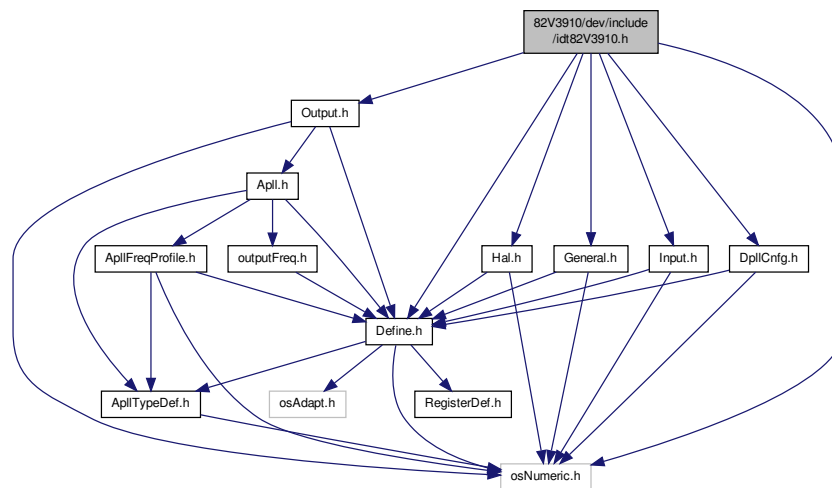
## Chapter 6

# File Documentation

### 6.1 82V3910/dev/include/idt82V3910.h File Reference

```
#include "General.h"  
#include "Define.h"  
#include "Input.h"  
#include "Output.h"  
#include "DpllCnfg.h"  
#include "Hal.h"  
#include "osNumeric.h"
```

Include dependency graph for idt82V3910.h:



### Functions

- void `IDTGeneral_InitDevice` (`T_idtDrvHdlr` hdlr)

*Initialize the device to its power on defaults.*

- `T_idtDrvHdlr` `IDTGeneral_InitDriver` (const char \*name, `T_idtDrvAccess` drvAccess, `T_idtDeviceType` deviceType, `T_idtApplXtal` \*xtalList, `T_osUInt8` numberOfXtal, `T_osUInt8` i2cAddr, int useHighLevelApi)

*Initialize device driver.*

## 6.1.1 Function Documentation

### 6.1.1.1 void IDTGeneral\_InitDevice ( T\_idtDrvHdlr *hdlr* )

Initialize the device to its power on defaults.

This function is optionally called. This function is required only after power on to initialize device registers to know states. For "warm" restarts skip this function.

#### Parameters

<i>hdlr</i>	Device driver handle
-------------	----------------------

Definition at line 101 of file 82V3910.c.

### 6.1.1.2 T\_idtDrvHdlr IDTGeneral\_InitDriver ( const char \* *name*, T\_idtDrvAccess *drvAccess*, T\_idtDeviceType *deviceType*, T\_idtApIIXtal \* *xtalList*, T\_osUInt8 *numberOfXtal*, T\_osUInt8 *i2cAddr*, int *useHighLevelApi* )

Initialize device driver.

This function creates a driver handler used as reference to a specific device. It does not perform any device access.

The *isHighLevelApi* determines whether device driver initializes high level APIs.

#### Parameters

<i>name</i>	Name of device (ex. "myDev")
<i>drvAccess</i>	Device access data.

#### See Also

*drvAccess\_t* structure information

#### Parameters

<i>deviceType</i>	What supported device
<i>xtalList</i>	A list of crystal(s) connected to APLL(s), set this parameter to NULL if there is no XTAL connected to APLL
<i>numberOfXtal</i>	Number of crystal(s) in the <i>xtalList</i> , set this parameter to 0 if <i>xtalList</i> is NULL
<i>i2cAddr</i>	7-bit unmodified i2c slave address
<i>useHighLevelApi</i>	0-Don't use high level API, 1-high level API enabled.

#### Returns

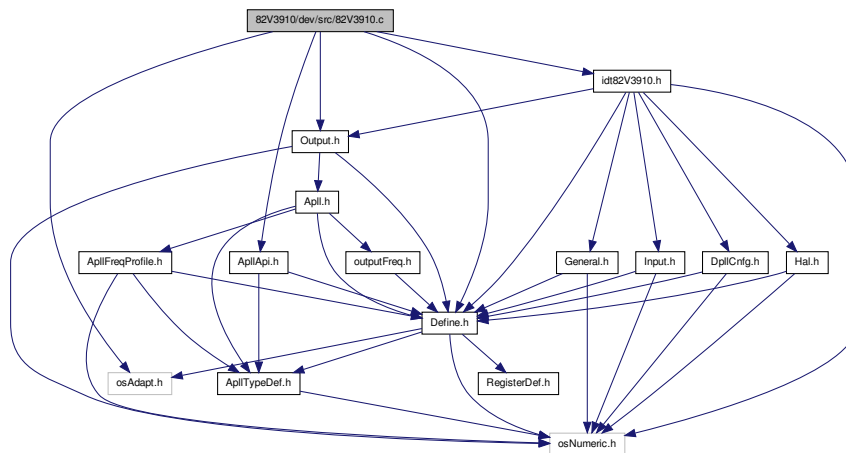
Device driver handler (used in all APIs)

Definition at line 167 of file 82V3910.c.

## 6.2 82V3910/dev/src/82V3910.c File Reference

```
#include "osAdapt.h"
#include "idt82V3910.h"
#include "Define.h"
#include "ApIApi.h"
#include "Output.h"
```

Include dependency graph for 82V3910.c:



## Functions

- void [IDTGeneral\\_InitDevice](#) (T\_idtDrvHdlr hdlr)  
*Initialize the device to its power on defaults.*
- T\_idtDrvHdlr [IDTGeneral\\_InitDriver](#) (const char \*name, T\_idtDrvAccess drvAccess, T\_idtDeviceType deviceType, T\_idtAplIXtal \*xtalList, T\_osUInt8 numberOfXtal, T\_osUInt8 i2cAddr, int useHighLevelApi)  
*Initialize device driver.*

## Variables

- const [T\\_idtDrvDeviceConfig](#) [idt82V3910Config](#)  
*Specific device profile.*

### 6.2.1 Function Documentation

#### 6.2.1.1 void IDTGeneral\_InitDevice ( T\_idtDrvHdlr hdlr )

Initialize the device to its power on defaults.

This function is optionally called. This function is required only after power on to initialize device registers to know states. For "warm" restarts skip this function.

#### Parameters

<i>hdlr</i>	Device driver handle
-------------	----------------------

Definition at line 101 of file 82V3910.c.

#### 6.2.1.2 T\_idtDrvHdlr IDTGeneral\_InitDriver ( const char \* name, T\_idtDrvAccess drvAccess, T\_idtDeviceType deviceType, T\_idtAplIXtal \* xtalList, T\_osUInt8 numberOfXtal, T\_osUInt8 i2cAddr, int useHighLevelApi )

Initialize device driver.

This function creates a driver handler used as reference to a specific device. It does not perform any device access.

The `isHighLevelApi` determines whether device driver initializes high level APIs.

#### Parameters

<i>name</i>	Name of device (ex. "myDev")
<i>drvAccess</i>	Device access data.

#### See Also

`drvAccess_t` structure information

#### Parameters

<i>deviceType</i>	What supported device
<i>xtalList</i>	A list of crystal(s) connected to APLL(s), set this parameter to NULL if there is no XTAL connected to APLL
<i>numberOfXtal</i>	Number of crystal(s) in the <code>xtalList</code> , set this parameter to 0 if <code>xtalList</code> is NULL
<i>i2cAddr</i>	7-bit unmodified i2c slave address
<i>useHighLevelApi</i>	0-Don't use high level API, 1-high level API enabled.

#### Returns

Device driver handler (used in all APIs)

Definition at line 167 of file `82V3910.c`.

## 6.2.2 Variable Documentation

### 6.2.2.1 `const T_idtDrvDeviceConfig idt82V3910Config`

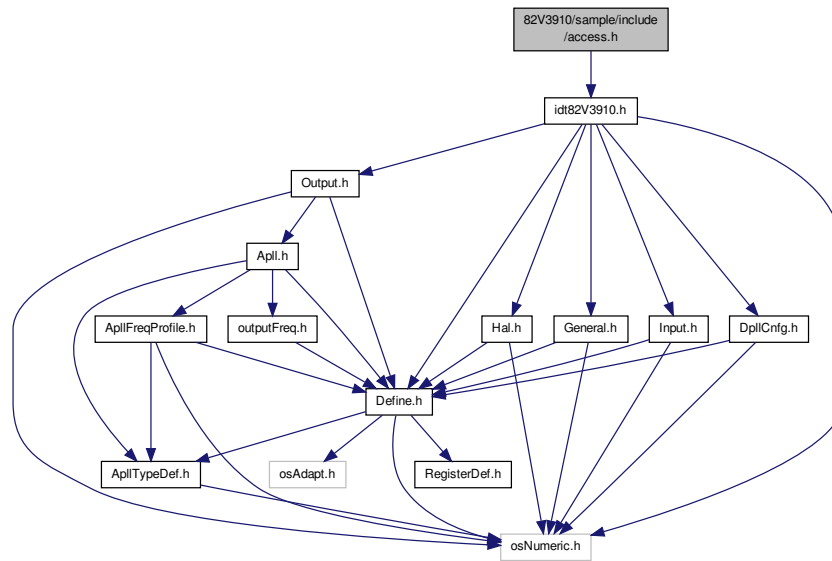
Specific device profile.

Definition at line 50 of file `82V3910.c`.

## 6.3 `82V3910/sample/include/access.h` File Reference

```
#include "idt82V3910.h"
```

Include dependency graph for access.h:



## Data Structures

- struct [T\\_idtApplXtalList](#)

*Wrapper structure containing APLL crystal id and frequency information.*

## Functions

- [T\\_idtDrvHdlr IDTSample\\_InitDriverI2c](#) ([T\\_idtApplXtalList](#) \*vcxoList, [T\\_osUInt8](#) coreI2CAddr)  
*IDTSample\_InitDriverI2c Utility function to initialize device driver for I2C access.*
- [T\\_idtDrvHdlr IDTSample\\_InitDriverSimulator](#) ([T\\_idtApplXtalList](#) \*vcxoList, [T\\_osUInt8](#) coreI2CAddr)  
*Utility function to initialize device driver for simulator access.*
- void [IDTSample\\_ResetXtalList](#) ([T\\_idtApplXtalList](#) \*vcxoList)  
*Utility function to reset APLL XTAL list to unconfigured value.*
- void [IDTSample\\_SetLogVerbosity](#) (int level)  
*Utility function to change log verbosity level access.*
- int [IDTSample\\_GetLogVerbosity](#) (void)  
*Utility function to get current log verbosity level.*

### 6.3.1 Function Documentation

#### 6.3.1.1 int IDTSample\_GetLogVerbosity ( void )

Utility function to get current log verbosity level.

This function is used for TCL extension library

Definition at line 326 of file access.c.

### 6.3.1.2 T\_idtDrvHdlr IDTSample\_InitDriverI2c ( T\_idtApIIXtalList \* *xtalList*, T\_osUInt8 *coreI2CAAddr* )

IDTSample\_InitDriverI2c Utility function to initialize device driver for I2C access.

This function is used for TCL extension library

#### Parameters

<i>xtalList</i>	List of XTAL
<i>coreI2CAAddr</i>	Device I2C address

#### Returns

Device driver handle

Definition at line 161 of file access.c.

### 6.3.1.3 T\_idtDrvHdlr IDTSample\_InitDriverSimulator ( T\_idtApIIXtalList \* *xtalList*, T\_osUInt8 *coreI2CAAddr* )

Utility function to initialize device driver for simulator access.

This function is used for TCL extension library

#### Parameters

<i>xtalList</i>	List of XTAL
<i>coreI2CAAddr</i>	Device I2C address

#### Returns

Device driver handle

Definition at line 229 of file access.c.

### 6.3.1.4 void IDTSample\_ResetXtalList ( T\_idtApIIXtalList \* *xtalList* )

Utility function to reset APLL XTAL list to unconfigured value.

This function is used for TCL extension library

#### Parameters

<i>xtalList</i>	List of XTAL
-----------------	--------------

Definition at line 296 of file access.c.

### 6.3.1.5 void IDTSample\_SetLogVerbosity ( int *level* )

Utility function to change log verbosity level access.

This function is used for TCL extension library

#### Parameters

<i>level</i>	Log verbosity level
--------------	---------------------

Definition at line 316 of file access.c.

## 6.4 82V3910/sample/include/loadstore.h File Reference

### Functions

- void [IDTSample\\_SaveRgfFile](#) (T\_idtDrvHdlr hdlr, char \*filename)  
*Function to output register contents of a device to standard IO or to a file.*
- void [IDTSample\\_LoadRgfFile](#) (T\_idtDrvHdlr hdlr, char \*filename)  
*Function to read in a file and program device registers.*

### 6.4.1 Function Documentation

#### 6.4.1.1 void IDTSample\_LoadRgfFile ( T\_idtDrvHdlr hdlr, char \* filename )

Function to read in a file and program device registers.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>filename</i>	Input file name to load register settings from.

Definition at line 124 of file loadstore.c.

#### 6.4.1.2 void IDTSample\_SaveRgfFile ( T\_idtDrvHdlr hdlr, char \* filename )

Function to output register contents of a device to standard IO or to a file.

##### Parameters

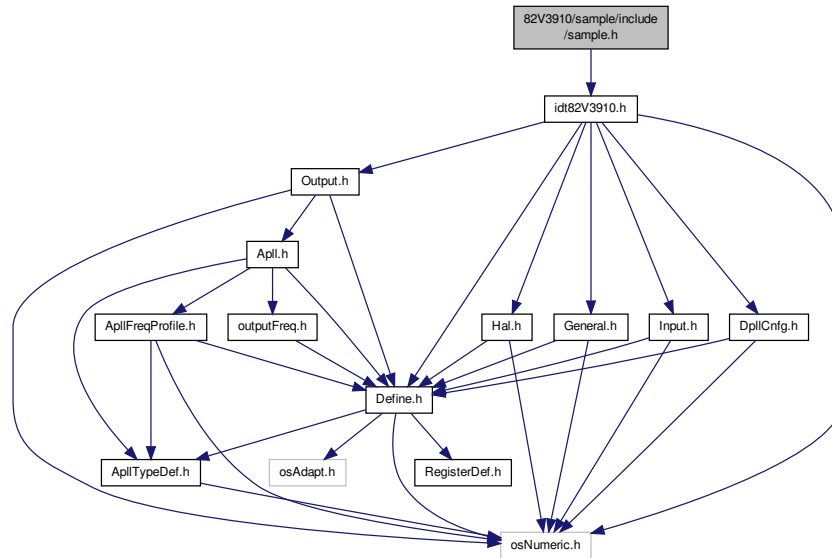
<i>hdlr</i>	Device driver handler
<i>filename</i>	Output file name, NULL for standard IO

Definition at line 94 of file loadstore.c.

## 6.5 82V3910/sample/include/sample.h File Reference

```
#include "idt82V3910.h"
```

Include dependency graph for sample.h:



### Functions

- void [IDTSample\\_ConfigureSampleConfig1](#) (T\_idtDrvHdlr hdlr)  
*Sample configuration 1.*
- void [IDTSample\\_ConfigureSampleConfig2](#) (T\_idtDrvHdlr hdlr)  
*Sample configuration 2.*
- void [IDTSample\\_ConfigureSampleConfig3](#) (T\_idtDrvHdlr hdlr)  
*Sample configuration 3.*
- void [IDTSample\\_ConfigureSampleConfig4](#) (T\_idtDrvHdlr hdlr)  
*Sample configuration 4.*
- void [IDTSample\\_ConfigureSampleConfig5](#) (T\_idtDrvHdlr hdlr)  
*Sample configuration 5.*
- void [IDTSample\\_Configure1Pps](#) (T\_idtDrvHdlr hdlr)  
*Sample configuration 1PPS.*
- void [IDTSample\\_Configure1PpsHoldover](#) (T\_idtDrvHdlr hdlr)  
*Sample configuration for 1PPS holdover issue.*
- void [IDTSample\\_ConfigureDcoMode](#) (T\_idtDrvHdlr hdlr)  
*Function to configure device for DCO mode.*
- void [IDTSample\\_SetCombinedDcoOffset](#) (T\_idtDrvHdlr hdlr, long pptOffset)  
*Function to set combined DCO offset value. It uses both DCO (holdover) and nominal offsets.*
- long [IDTSample\\_GetCombinedDcoOffset](#) (T\_idtDrvHdlr hdlr)  
*Function to get combined DCO offset value. It uses both DCO (holdover) and nominal offsets.*



## 6.5.1 Function Documentation

### 6.5.1.1 void IDTSample\_Configure1Pps ( T\_idtDrvHdlr *hdlr* )

Sample configuration 1PPS.

```
IN3 (1PPS) -> T0 -> OUT3 (1PPS)
```

#### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 420 of file sample.c.

### 6.5.1.2 void IDTSample\_Configure1PpsHoldover ( T\_idtDrvHdlr *hdlr* )

Sample configuration for 1PPS holdover issue.

#### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 449 of file sample.c.

### 6.5.1.3 void IDTSample\_ConfigureDcoMode ( T\_idtDrvHdlr *hdlr* )

Function to configure device for DCO mode.

#### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 480 of file sample.c.

### 6.5.1.4 void IDTSample\_ConfigureSampleConfig1 ( T\_idtDrvHdlr *hdlr* )

Sample configuration 1.

```
IN3 (25 MHz) -> T0 +-> OUT1 (25 MHz)
                +-> OUT6 (156.25 MHz)
```

#### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 46 of file sample.c.

### 6.5.1.5 void IDTSample\_ConfigureSampleConfig2 ( T\_idtDrvHdlr *hdlr* )

Sample configuration 2.

```
IN3 (25 MHz) -> T0 +-> OUT1 (25 MHz)
                +-> OUT3 (8 kHz)
                +-> OUT5 (125 MHz)
```

**Parameters**

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 98 of file sample.c.

**6.5.1.6 void IDTSample\_ConfigureSampleConfig3 ( T\_idtDrvHdlr *hdlr* )**

Sample configuration 3.

```
IN3 (25 MHz) -> T0 +-> OUT1 (25 MHz)
                +-> OUT3 (10 MHz)
                +-> OUT5 (1 PPS)
```

**Parameters**

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 154 of file sample.c.

**6.5.1.7 void IDTSample\_ConfigureSampleConfig4 ( T\_idtDrvHdlr *hdlr* )**

Sample configuration 4.

```
Inputs: IN3 (10MHz), IN4 (1.544MHz), IN5 (25MHz), IN6 (8KHz), IN7 (8KHz),
        IN8 (156.25MHz), IN9 (156.25MHz), IN10 (25MHz), IN11 (25MHz)
Outputs: OUT1 (1.544MHz), OUT3 (10MHz), OUT4 (25MHz), OUT7 (156.25MHz),
        OUT10 (156.25MHz), OUT11 (156.25MHz)
T0 Profile: G.8262 Option 2
T4 Profile: Default
XTAL1/2: 25MHz
```

**Parameters**

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 226 of file sample.c.

**6.5.1.8 void IDTSample\_ConfigureSampleConfig5 ( T\_idtDrvHdlr *hdlr* )**

Sample configuration 5.

```
Carbon copy of IDTSample_ConfigureSampleConfig4,
except there is no input and DPLL is in free-run
mode (default).
```

**Parameters**

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 339 of file sample.c.

**6.5.1.9 long IDTSample\_GetCombinedDcoOffset ( T\_idtDrvHdlr *hdlr* )**

Function to get combined DCO offset value. It uses both DCO (holdover) and nominal offsets.

## Parameters

<i>hdr</i>	Device driver handler
------------	-----------------------

## Returns

Parts per trillion offset

Definition at line 542 of file sample.c.

6.5.1.10 void IDTSample\_SetCombinedDcoOffset ( T\_idtDrvHdr *hdr*, long *pptOffset* )

Function to set combined DCO offset value. It uses both DCO (holdover) and nominal offsets.

## Parameters

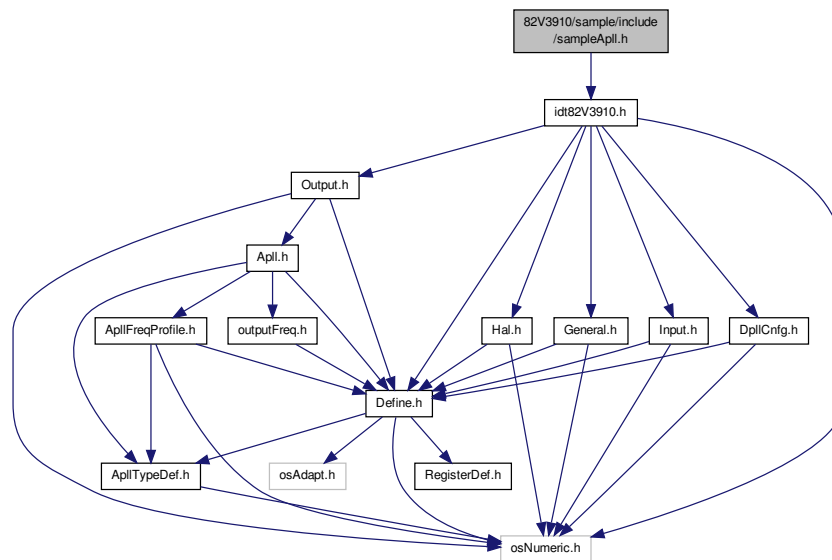
<i>hdr</i>	Device driver handler
<i>pptOffset</i>	Parts per trillion offset

Definition at line 492 of file sample.c.

## 6.6 82V3910/sample/include/sampleAppl.h File Reference

```
#include "idt82V3910.h"
```

Include dependency graph for sampleAppl.h:



## Functions

- void [IDTSample\\_ConfigureSampleConfigOutput6\\_156\\_dot\\_25MHz](#) (T\_idtDrvHdr *hdr*)  
Sample configuration for 156.25MHz output at port 6.
- void [IDTSample\\_ConfigureSampleConfigOutput7\\_77\\_dot\\_76MHz](#) (T\_idtDrvHdr *hdr*)  
Sample configuration for 77.76 MHz output at port 7.

- void [IDTSample\\_ConfigureSampleConfigureOutput10\\_25\\_MHz](#) (T\_idtDrvHdlr hdlr)  
Sample configuration for 25MHz output at port 10.
- void [IDTSample\\_SyncE\\_WAN](#) (T\_idtDrvHdlr hdlr)  
Sample configuration for SyncE WAN application.
- void [IDTSample\\_Sonet](#) (T\_idtDrvHdlr hdlr)  
Sample configuration for SONET application.
- void [IDTSample\\_DualMode](#) (T\_idtDrvHdlr hdlr)  
Sample configuration for dual mode application.
- void [IDTSample\\_SyncE\\_Sonet](#) (T\_idtDrvHdlr hdlr)  
Sample configuration for SyncE SONET application.
- void [IDTSample\\_SyncE\\_LAN](#) (T\_idtDrvHdlr hdlr)  
Sample configuration for SyncE LAN application.
- void [IDTSample\\_GPS\\_1PPS](#) (T\_idtDrvHdlr hdlr)  
Sample configuration for GPS 1PPS application.
- void [IDTSample\\_GPS](#) (T\_idtDrvHdlr hdlr)  
Sample configuration for GPS application.

## 6.6.1 Function Documentation

### 6.6.1.1 void IDTSample\_ConfigureSampleConfigOutput6\_156\_dot\_25MHz ( T\_idtDrvHdlr hdlr )

Sample configuration for 156.25MHz output at port 6.

```
IN3 (25 MHz) -> T0 +-> OUT6 (Ethernet, 156.25 MHz)
```

#### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 47 of file sampleAppl.c.

### 6.6.1.2 void IDTSample\_ConfigureSampleConfigureOutput10\_25\_MHz ( T\_idtDrvHdlr hdlr )

Sample configuration for 25MHz output at port 10.

```
IN3 (25 MHz) -> T0 +-> OUT10 (Ethernet, 25 MHz)
```

#### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 125 of file sampleAppl.c.

### 6.6.1.3 void IDTSample\_ConfigureSampleConfigureOutput7\_77\_dot\_76MHz ( T\_idtDrvHdlr hdlr )

Sample configuration for 77.76 MHz output at port 7.

```
IN3 (25 MHz) -> T0 +-> OUT7 (SONET, 77.76 MHz)
```

#### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 86 of file sampleAppl.c.

#### 6.6.1.4 void IDTSample\_DualMode ( T\_idtDrvHdlr *hdlr* )

Sample configuration for dual mode application.

```
Inputs: IN3 (19.44MHz), IN5 (155.52MHz), IN14 (1.544MHz)
T0 Profile: ST3 SONET
T4 Profile: default
Select XTAL3: done automatically by IDTH1Api_ConfigureOutput function
              based on the output frequency. To manually select XTAL,
              call SetJaXtalId function.
Outputs: OUT1 (19.44MHz), OUT6 (155.52MHz), OUT7 (77.76MHz), OUT9 (1.544MHz)
T0: IN3, IN5, IN14 -> OUT1, OUT6, OUT7 (IN14 is highest priority)
T4: IN3, IN5 -> OUT9
APLL1 XTAL1 at 25MHz & XTAL3 at 24.8832MHz
```

#### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 410 of file sampleAppl.c.

#### 6.6.1.5 void IDTSample\_GPS ( T\_idtDrvHdlr *hdlr* )

Sample configuration for GPS application.

```
Inputs: IN3 (10MHz), IN4 (10MHz), EX_SYNC1 (1PPS), EX_SYNC2 (1PPS)
T0 Profile: BITS / SSU (Wideband) - default
Outputs: OUT1 (25MHz), OUT2 (19.44MHz), OUT3 (10MHz), OUT4 (1PPS),
         OUT6 (25MHz), OUT7 (156.25MHz), OUT9 (1.544MHz), OUT10 (155.52MHz),
         OUT11 (77.76MHz), FRSYNC_8K_1PPS (1PPS), MFRSYNC_2K_1PPS (1PPS)
APLL1 XTAL1 = 25MHz & APLL2 XTAL2 = 24.8832MHz
```

#### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 1013 of file sampleAppl.c.

#### 6.6.1.6 void IDTSample\_GPS\_1PPS ( T\_idtDrvHdlr *hdlr* )

Sample configuration for GPS 1PPS application.

```
Inputs: IN3 (1PPS), IN5 (1PPS)
T0 Profile: GPS (15mHz)
Outputs: OUT1 (25MHz), OUT2 (19.44MHz), OUT3 (10MHz), OUT4 (1PPS),
         OUT6 (25MHz), OUT7 (156.25MHz), OUT9 (2.048MHz),
         OUT10 (155.52MHz), OUT11 (77.76MHz)
APLL1 XTAL1 at 25MHz & APLL2 XTAL2 at 24.8832MHz
```

#### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 835 of file sampleAppl.c.

### 6.6.1.7 void IDTSample\_Sonet ( T\_idtDrvHdlr hdlr )

Sample configuration for SONET application.

```
Inputs: IN3 (19.44MHz), IN5 (155.52MHz), IN14 (1.544MHz)
T0 Profile: ST3 SONET
T4 Profile: default
Outputs: OUT1 (19.44MHz), OUT9 (1.544MHz), OUT10 (155.52MHz)
T0: IN3, IN5, IN14 -> OUT1, OUT10 (IN14 is highest priority)
T4: IN3, IN5 -> OUT9
APLL2 XTAL2 at 24.8832MHz
```

#### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 294 of file sampleAppl.c.

### 6.6.1.8 void IDTSample\_SyncE\_LAN ( T\_idtDrvHdlr hdlr )

Sample configuration for SyncE LAN application.

```
Inputs: IN3 (25MHz), IN14 (2.048MHz)
T0 Profile: G.8262 Option 2
T4 Profile: BITS / SSU (Wideband)
Outputs: OUT1 (25MHz), OUT10 (25.78125), OUT11 (161.1328125MHz), OUT9 (2.048MHz)
T0: IN3, IN14 -> OUT1, OUT10, OUT11 (IN14 is highest priority)
T4: IN3 -> OUT9
APLL2 XTAL4 at 25.78125MHz
```

#### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 720 of file sampleAppl.c.

### 6.6.1.9 void IDTSample\_SyncE\_Sonet ( T\_idtDrvHdlr hdlr )

Sample configuration for SyncE SONET application.

```
Inputs: IN3 (25MHz) , IN5 (156.25MHz), IN6 (155.52MHz), IN7 (19.44MHz), IN14 (1.544MHz)
T0 Profile: G.8262 Option 2
T4 Profile: BITS / SSU (Wideband) - default
Outputs: OUT1 (25MHz), OUT2 (19.44MHz), OUT6 (25MHz), OUT7 (156.25MHz),
        OUT9 (1.544MHz), OUT10 (155.52MHz), OUT11 (77.76MHz)
T0: IN3, IN5, IN6, IN7, IN14 -> OUT1, OUT2, OUT6, OUT7, OUT10, OUT11 (IN14 is highest priority)
T4: IN3, IN5, IN6, IN7 -> OUT9
APLL1 XTAL1 at 25MHz & APLL2 XTAL2 at 24.8832MHz
```

#### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 534 of file sampleAppl.c.

### 6.6.1.10 void IDTSample\_SyncE\_WAN ( T\_idtDrvHdlr hdlr )

Sample configuration for SyncE WAN application.

```

Inputs: IN3 (25MHz), IN5 (156.25MHz), IN14 (1.544MHz)
T0 Profile: G.8262 Option 2
T4 Profile: Default
Outputs: OUT1 (25MHz), OUT6 (25MHz), OUT7 (156.25MHz), OUT9 (1.544MHz)
T0: IN3, IN5, IN14 -> OUT1, OUT10, OUT11 (IN14 has highest priority)
T4: IN3, IN5 -> OUT9
APLL1 XTAL1 at 25MHz

```

#### Parameters

<i>hdr</i>	Device driver handler
------------	-----------------------

Definition at line 170 of file sampleApl.c.

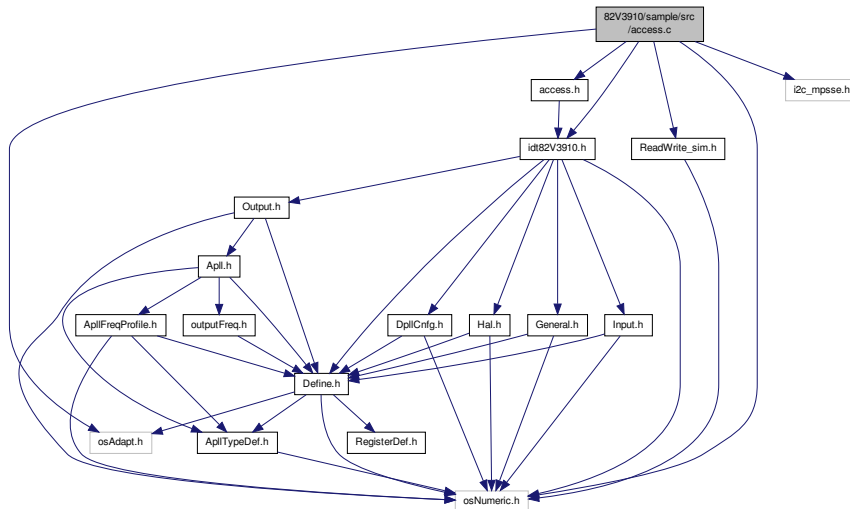
## 6.7 82V3910/sample/src/access.c File Reference

```

#include "osNumeric.h"
#include "osAdapt.h"
#include "idt82V3910.h"
#include "access.h"
#include "ReadWrite_sim.h"
#include "i2c_mpsse.h"

```

Include dependency graph for access.c:



#### Functions

- void [Init\\_SimWrapper](#) (void \*usrData)  
Function to wrap both common and APLL HAL initialization functions.
- void [DelInit\\_SimWrapper](#) (void \*usrData)  
Function to wrap both common and APLL HAL deinitialization functions.
- T\_osUInt8 [ReadByte\\_SimWrapper](#) (void \*usrData, T\_osUInt8 devAddr, T\_osUInt8 nAddr)  
Function to wrap both common and APLL HAL read register functions.
- void [WriteByte\\_SimWrapper](#) (void \*usrData, T\_osUInt8 devAddr, T\_osUInt8 nAddr, T\_osUInt8 nData)  
Function to wrap both common and APLL HAL write register functions.
- T\_idtDrvHdr [IDTSample\\_InitDriverI2c](#) (T\_idtAplXtalList \*xtalList, T\_osUInt8 coreI2CAddr)

*IDTSample\_InitDriverI2c* Utility function to initialize device driver for I2C access.

- T\_idtDrvHdlr [IDTSample\\_InitDriverSimulator](#) (T\_idtApIIXtalList \*xtalList, T\_osUInt8 coreI2CAddr)

*Utility function to initialize device driver for simulator access.*

- void [IDTSample\\_ResetXtalList](#) (T\_idtApIIXtalList \*xtalList)

*Utility function to reset APLL XTAL list to unconfigured value.*

- void [IDTSample\\_SetLogVerbosity](#) (int level)

*Utility function to change log verbosity level access.*

- int [IDTSample\\_GetLogVerbosity](#) (void)

*Utility function to get current log verbosity level.*

## Variables

- const [T\\_idtDrvAccess I2cAccessMethods](#)
- const [T\\_idtDrvAccess SimAccessMethods](#)

## 6.7.1 Function Documentation

### 6.7.1.1 void Delnit\_SimWrapper ( void \* usrData )

Function to wrap both common and APLL HAL deinitialization functions.

#### Parameters

<i>usrData</i>	User data optionally used for de-initialization
----------------	---

Definition at line 116 of file access.c.

### 6.7.1.2 int IDTSample\_GetLogVerbosity ( void )

Utility function to get current log verbosity level.

This function is used for TCL extension library

Definition at line 326 of file access.c.

### 6.7.1.3 T\_idtDrvHdlr IDTSample\_InitDriverI2c ( T\_idtApIIXtalList \* xtalList, T\_osUInt8 coreI2CAddr )

*IDTSample\_InitDriverI2c* Utility function to initialize device driver for I2C access.

This function is used for TCL extension library

#### Parameters

<i>xtalList</i>	List of XTAL
<i>coreI2CAddr</i>	Device I2C address

#### Returns

Device driver handle

Definition at line 161 of file access.c.

### 6.7.1.4 T\_idtDrvHdlr IDTSample\_InitDriverSimulator ( T\_idtApIIXtalList \* xtalList, T\_osUInt8 coreI2CAddr )

Utility function to initialize device driver for simulator access.



This function is used for TCL extension library

#### Parameters

<i>xtalList</i>	List of XTAL
<i>coreI2CAAddr</i>	Device I2C address

#### Returns

Device driver handle

Definition at line 229 of file access.c.

#### 6.7.1.5 void IDTSample\_ResetXtalList ( T\_idtApIIXtalList \* *xtalList* )

Utility function to reset APLL XTAL list to unconfigured value.

This function is used for TCL extension library

#### Parameters

<i>xtalList</i>	List of XTAL
-----------------	--------------

Definition at line 296 of file access.c.

#### 6.7.1.6 void IDTSample\_SetLogVerbosity ( int *level* )

Utility function to change log verbosity level access.

This function is used for TCL extension library

#### Parameters

<i>level</i>	Log verbosity level
--------------	---------------------

Definition at line 316 of file access.c.

#### 6.7.1.7 void Init\_SimWrapper ( void \* *usrData* )

Function to wrap both common and APLL HAL initialization functions.

#### Parameters

<i>usrData</i>	User data optionally used for initialization.
----------------	---

Definition at line 106 of file access.c.

#### 6.7.1.8 T\_osUInt8 ReadByte\_SimWrapper ( void \* *usrData*, T\_osUInt8 *devAddr*, T\_osUInt8 *nAddr* )

Function to wrap both common and APLL HAL read register functions.

#### Parameters

<i>usrData</i>	User data optionally used for reading registers
<i>devAddr</i>	Device Address (I2C addr)
<i>nAddr</i>	Register offset

**Returns**

Read register

Definition at line 129 of file access.c.

### 6.7.1.9 void WriteByte\_SimWrapper ( void \* *usrData*, T\_osUInt8 *devAddr*, T\_osUInt8 *nAddr*, T\_osUInt8 *nData* )

Function to wrap both common and APLL HAL write register functions.

**Parameters**

<i>usrData</i>	User data optionally used for writing registers
<i>devAddr</i>	Device Address (I2C addr)
<i>nAddr</i>	Register offset
<i>nData</i>	Register value to write

Definition at line 144 of file access.c.

## 6.7.2 Variable Documentation

### 6.7.2.1 const T\_idtDrvAccess I2cAccessMethods

**Initial value:**

```
= {
    i2c_init,
    i2c_deinit,
    i2c_read_byte,
    i2c_write_byte,
    NULL
}
```

Definition at line 79 of file access.c.

### 6.7.2.2 const T\_idtDrvAccess SimAccessMethods

**Initial value:**

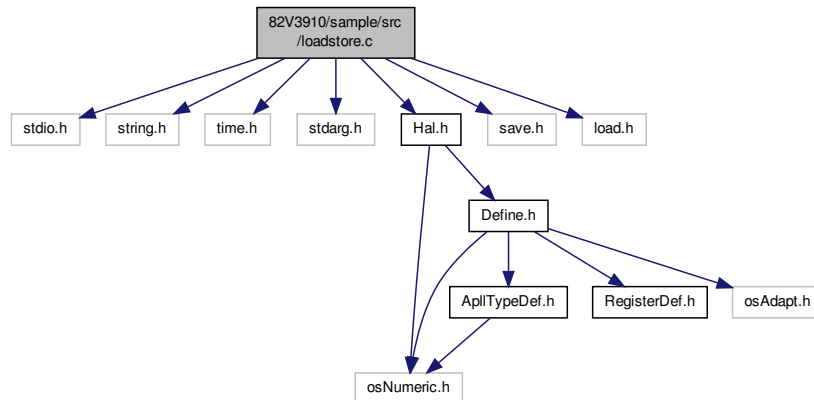
```
= {
    Init_SimWrapper,
    DeInit_SimWrapper,
    ReadByte_SimWrapper,
    WriteByte_SimWrapper,
    NULL
}
```

Definition at line 89 of file access.c.

## 6.8 82V3910/sample/src/loadstore.c File Reference

```
#include <stdio.h>
#include <string.h>
#include <time.h>
#include <stdarg.h>
#include "Hal.h"
#include "save.h"
#include "load.h"
```

Include dependency graph for loadstore.c:



## Functions

- void [IDTSample\\_SaveRgfFile](#) (T\_idtDrvHdlr hdlr, char \*filename)  
Function to output register contents of a device to standard IO or to a file.
- void [IDTSample\\_LoadRgfFile](#) (T\_idtDrvHdlr hdlr, char \*filename)  
Function to read in a file and program device registers.

### 6.8.1 Function Documentation

#### 6.8.1.1 void IDTSample\_LoadRgfFile ( T\_idtDrvHdlr hdlr, char \* filename )

Function to read in a file and program device registers.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>filename</i>	Input file name to load register settings from.

Definition at line 124 of file loadstore.c.

#### 6.8.1.2 void IDTSample\_SaveRgfFile ( T\_idtDrvHdlr hdlr, char \* filename )

Function to output register contents of a device to standard IO or to a file.

##### Parameters

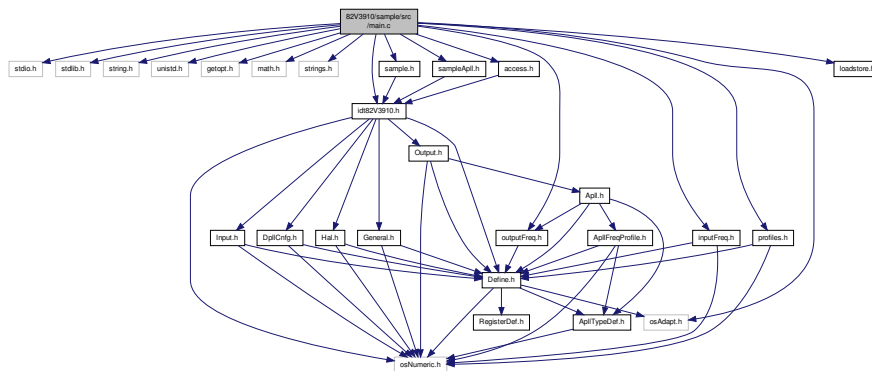
<i>hdlr</i>	Device driver handler
<i>filename</i>	Output file name, NULL for standard IO

Definition at line 94 of file loadstore.c.

## 6.9 82V3910/sample/src/main.c File Reference

```
#include <stdio.h>
#include <stdlib.h>
#include <string.h>
#include <unistd.h>
#include <getopt.h>
#include <math.h>
#include <strings.h>
#include "idt82V3910.h"
#include "osAdapt.h"
#include "sample.h"
#include "sampleAppl.h"
#include "inputFreq.h"
#include "outputFreq.h"
#include "profiles.h"
#include "loadstore.h"
#include "access.h"
```

Include dependency graph for main.c:



### Data Structures

- struct [T\\_SampleConfigEntry](#)  
*Sample configuration information.*
- struct [globalArgs\\_t](#)  
*Structure to define program command line arguments.*

### Macros

- #define [MODE\\_None](#) (0)
- #define [MODE\\_Load](#) (1<<0)
- #define [MODE\\_Save](#) (1<<1)
- #define [MODE\\_Input](#) (1<<2)
- #define [MODE\\_Output](#) (1<<3)
- #define [MODE\\_DpllProfile](#) (1<<4)
- #define [MODE\\_Sample](#) (1<<5)
- #define [MODE\\_Read](#) (1<<6)
- #define [MODE\\_Write](#) (1<<7)
- #define [SAMPLE\\_MAX\\_FILENAME](#) 50
- #define [no\\_argument](#) 0

- #define [required\\_argument](#) 1
- #define [optional\\_argument](#) 2

## Typedefs

- typedef void(\* [T\\_DpllProfileFunc](#) )(T\_idtDrvHdlr hdlr, [T\\_idtDpllInstance](#) nDpll)  
*Function typedef for DPLL profile provisioning.*
- typedef void(\* [T\\_SampleConfigFunc](#) )(T\_idtDrvHdlr hdlr)  
*Function typedef for sample configurations.*
- typedef void(\* [T\\_SampleConfigDescrFunc](#) )(void)  
*Function typedef for sample configuration descriptions.*

## Enumerations

- enum [T\\_DpllProfile](#) {  
[DpllProfile\\_GR253](#), [DpllProfile\\_GR1244](#), [DpllProfile\\_SMC](#), [DpllProfile\\_G8262Option1](#),  
[DpllProfile\\_G8262Option2](#), [DpllProfile\\_G813Option1](#), [DpllProfile\\_G813Option2](#), [DpllProfile\\_1PPS](#),  
[DpllProfile\\_MAX](#) }  
*List of possible DPLL profiles.*

## Functions

- void [IDTSample\\_DumpRegistersRgf](#) (char \*filename)
- void [printHelp](#) (void)
- int [processCmdLineArguments](#) (int argc, char \*argv[], [globalArgs\\_t](#) \*gblArgs)
- int [main](#) (int argc, char \*argv[])

## Variables

- [globalArgs\\_t](#) globalArgs
- int [simDebugFlag](#)
- const char \* [IDTHIApi\\_Frequency2String\\_c](#) [[OutFreq\\_MAX](#)]

### 6.9.1 Macro Definition Documentation

#### 6.9.1.1 #define MODE\_DpllProfile (1<<4)

Provision DPLL profile mode

Definition at line 111 of file main.c.

#### 6.9.1.2 #define MODE\_Input (1<<2)

Provision input port mode

Definition at line 105 of file main.c.

#### 6.9.1.3 #define MODE\_Load (1<<0)

Load from file mode

Definition at line 99 of file main.c.

**6.9.1.4 #define MODE\_None (0)**

No-op mode

Definition at line 96 of file main.c.

**6.9.1.5 #define MODE\_Output (1<<3)**

Provision output port mode

Definition at line 108 of file main.c.

**6.9.1.6 #define MODE\_Read (1<<6)**

Read register mode

Definition at line 117 of file main.c.

**6.9.1.7 #define MODE\_Sample (1<<5)**

Sample configuration mode

Definition at line 114 of file main.c.

**6.9.1.8 #define MODE\_Save (1<<1)**

Save to file mode

Definition at line 102 of file main.c.

**6.9.1.9 #define MODE\_Write (1<<7)**

Read register mode

Definition at line 120 of file main.c.

**6.9.1.10 #define no\_argument 0**

Definition at line 155 of file main.c.

**6.9.1.11 #define optional\_argument 2**

Definition at line 157 of file main.c.

**6.9.1.12 #define required\_argument 1**

Definition at line 156 of file main.c.

**6.9.1.13 #define SAMPLE\_MAX\_FILENAME 50**

Max filename size

Definition at line 123 of file main.c.

## 6.9.2 Typedef Documentation

### 6.9.2.1 typedef void(\* T\_DpllProfileFunc)(T\_idtDrvHdr hdr, T\_idtDpllInstance nDpll)

Function typedef for DPLL profile provisioning.

Definition at line 59 of file main.c.

### 6.9.2.2 typedef void(\* T\_SampleConfigDescrFunc)(void)

Function typedef for sample configuration descriptions.

Definition at line 70 of file main.c.

### 6.9.2.3 typedef void(\* T\_SampleConfigFunc)(T\_idtDrvHdr hdr)

Function typedef for sample configurations.

Definition at line 65 of file main.c.

## 6.9.3 Enumeration Type Documentation

### 6.9.3.1 enum T\_DpllProfile

List of possible DPLL profiles.

Enumerator

***DpllProfile\_GR253*** GR-253 (SONET) Stratum 3 DPLL Profile

***DpllProfile\_GR1244*** GR-1244 Stratum 3 DPLL Profile

***DpllProfile\_SMC*** SMC DPLL Profile

***DpllProfile\_G8262Option1*** G-8262 Option 1 DPLL Profile

***DpllProfile\_G8262Option2*** G-8262 Option 2 DPLL Profile

***DpllProfile\_G813Option1*** G-813 Option 1 DPLL Profile

***DpllProfile\_G813Option2*** G-813 Option 2 DPLL Profile

***DpllProfile\_1PPS*** 1 PPS DPLL Profile

***DpllProfile\_MAX***

Definition at line 83 of file main.c.

## 6.9.4 Function Documentation

### 6.9.4.1 void IDTSample\_DumpRegistersRgf ( char \* filename )

### 6.9.4.2 int main ( int argc, char \* argv[] )

Definition at line 641 of file main.c.

### 6.9.4.3 void printHelp ( void )

Definition at line 257 of file main.c.





- void [IDTSample\\_ConfigureSampleConfig3](#) (T\_idtDrvHdlr hdlr)  
*Sample configuration 3.*
- void [IDTSample\\_ConfigureSampleConfig4](#) (T\_idtDrvHdlr hdlr)  
*Sample configuration 4.*
- void [IDTSample\\_ConfigureSampleConfig5](#) (T\_idtDrvHdlr hdlr)  
*Sample configuration 5.*
- void [IDTSample\\_Configure1Pps](#) (T\_idtDrvHdlr hdlr)  
*Sample configuration 1PPS.*
- void [IDTSample\\_Configure1PpsHoldover](#) (T\_idtDrvHdlr hdlr)  
*Sample configuration for 1PPS holdover issue.*
- void [IDTSample\\_ConfigureDcoMode](#) (T\_idtDrvHdlr hdlr)  
*Function to configure device for DCO mode.*
- void [IDTSample\\_SetCombinedDcoOffset](#) (T\_idtDrvHdlr hdlr, long pptOffset)  
*Function to set combined DCO offset value. It uses both DCO (holdover) and nominal offsets.*
- long [IDTSample\\_GetCombinedDcoOffset](#) (T\_idtDrvHdlr hdlr)  
*Function to get combined DCO offset value. It uses both DCO (holdover) and nominal offsets.*

## 6.10.1 Function Documentation

### 6.10.1.1 void IDTSample\_Configure1Pps ( T\_idtDrvHdlr hdlr )

Sample configuration 1PPS.

```
IN3 (1PPS) -> T0 -> OUT3 (1PPS)
```

#### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 420 of file sample.c.

### 6.10.1.2 void IDTSample\_Configure1PpsHoldover ( T\_idtDrvHdlr hdlr )

Sample configuration for 1PPS holdover issue.

#### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 449 of file sample.c.

### 6.10.1.3 void IDTSample\_ConfigureDcoMode ( T\_idtDrvHdlr hdlr )

Function to configure device for DCO mode.

#### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 480 of file sample.c.

#### 6.10.1.4 void IDTSample\_ConfigureSampleConfig1 ( T\_idtDrvHdlr *hdlr* )

Sample configuration 1.

```
IN3 (25 MHz) -> T0 +-> OUT1 (25 MHz)
                +-> OUT6 (156.25 MHz)
```

##### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 46 of file sample.c.

#### 6.10.1.5 void IDTSample\_ConfigureSampleConfig2 ( T\_idtDrvHdlr *hdlr* )

Sample configuration 2.

```
IN3 (25 MHz) -> T0 +-> OUT1 (25 MHz)
                +-> OUT3 (8 kHz)
                +-> OUT5 (125 MHz)
```

##### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 98 of file sample.c.

#### 6.10.1.6 void IDTSample\_ConfigureSampleConfig3 ( T\_idtDrvHdlr *hdlr* )

Sample configuration 3.

```
IN3 (25 MHz) -> T0 +-> OUT1 (25 MHz)
                +-> OUT3 (10 MHz)
                +-> OUT5 (1 PPS)
```

##### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 154 of file sample.c.

#### 6.10.1.7 void IDTSample\_ConfigureSampleConfig4 ( T\_idtDrvHdlr *hdlr* )

Sample configuration 4.

```
Inputs: IN3 (10MHz), IN4 (1.544MHz), IN5 (25MHz), IN6 (8KHz), IN7 (8KHz),
        IN8 (156.25MHz), IN9 (156.25MHz), IN10 (25MHz), IN11 (25MHz)
Outputs: OUT1 (1.544MHz), OUT3 (10MHz), OUT4 (25MHz), OUT7 (156.25MHz),
        OUT10 (156.25MHz), OUT11 (156.25MHz)
T0 Profile: G.8262 Option 2
T4 Profile: Default
XTAL1/2: 25MHz
```

##### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 226 of file sample.c.

#### 6.10.1.8 void IDTSample\_ConfigureSampleConfig5 ( T\_idtDrvHdlr *hdlr* )

Sample configuration 5.

Carbon copy of IDTSample\_ConfigureSampleConfig4, except there is no input and DPLL is in free-run mode (default).

##### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 339 of file sample.c.

#### 6.10.1.9 long IDTSample\_GetCombinedDcoOffset ( T\_idtDrvHdlr *hdlr* )

Function to get combined DCO offset value. It uses both DCO (holdover) and nominal offsets.

##### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

##### Returns

Parts per trillion offset

Definition at line 542 of file sample.c.

#### 6.10.1.10 void IDTSample\_SetCombinedDcoOffset ( T\_idtDrvHdlr *hdlr*, long *pptOffset* )

Function to set combined DCO offset value. It uses both DCO (holdover) and nominal offsets.

##### Parameters

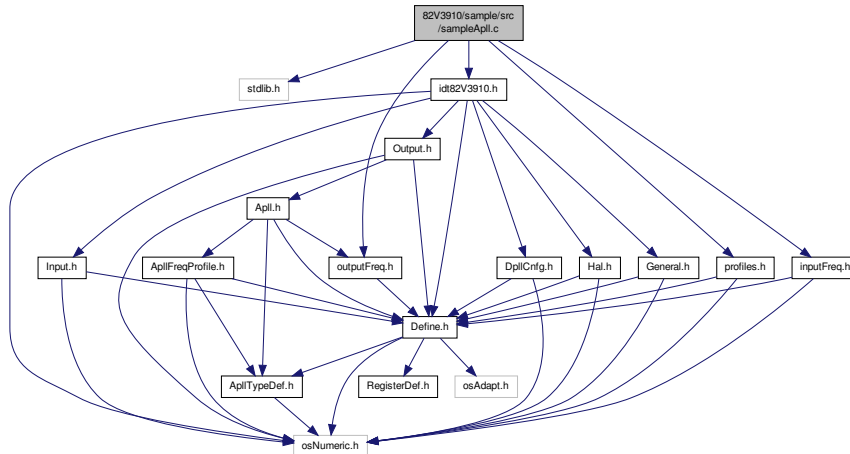
<i>hdlr</i>	Device driver handler
<i>pptOffset</i>	Parts per trillion offset

Definition at line 492 of file sample.c.

## 6.11 82V3910/sample/src/sampleAppl.c File Reference

```
#include <stdlib.h>
#include "idt82V3910.h"
#include "profiles.h"
#include "inputFreq.h"
#include "outputFreq.h"
```

Include dependency graph for sampleAppl.c:



## Functions

- void [IDTSample\\_ConfigureSampleConfigOutput6\\_156\\_dot\\_25MHz](#) (T\_idtDrvHdlr hdlr)  
Sample configuration for 156.25MHz output at port 6.
- void [IDTSample\\_ConfigureSampleConfigureOutput7\\_77\\_dot\\_76MHz](#) (T\_idtDrvHdlr hdlr)  
Sample configuration for 77.76 MHz output at port 7.
- void [IDTSample\\_ConfigureSampleConfigureOutput10\\_25\\_MHz](#) (T\_idtDrvHdlr hdlr)  
Sample configuration for 25MHz output at port 10.
- void [IDTSample\\_SyncE\\_WAN](#) (T\_idtDrvHdlr hdlr)  
Sample configuration for SyncE WAN application.
- void [IDTSample\\_Sonet](#) (T\_idtDrvHdlr hdlr)  
Sample configuration for SONET application.
- void [IDTSample\\_DualMode](#) (T\_idtDrvHdlr hdlr)  
Sample configuration for dual mode application.
- void [IDTSample\\_SyncE\\_Sonet](#) (T\_idtDrvHdlr hdlr)  
Sample configuration for SyncE SONET application.
- void [IDTSample\\_SyncE\\_LAN](#) (T\_idtDrvHdlr hdlr)  
Sample configuration for SyncE LAN application.
- void [IDTSample\\_GPS\\_1PPS](#) (T\_idtDrvHdlr hdlr)  
Sample configuration for GPS 1PPS application.
- void [IDTSample\\_GPS](#) (T\_idtDrvHdlr hdlr)  
Sample configuration for GPS application.

### 6.11.1 Function Documentation

#### 6.11.1.1 void IDTSample\_ConfigureSampleConfigOutput6\_156\_dot\_25MHz ( T\_idtDrvHdlr hdlr )

Sample configuration for 156.25MHz output at port 6.

```
IN3 (25 MHz) -> T0 +-> OUT6 (Ethernet, 156.25 MHz)
```

#### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 47 of file sampleAppl.c.

#### 6.11.1.2 void IDTSample\_ConfigureSampleConfigureOutput10\_25\_MHz ( T\_idtDrvHdlr *hdlr* )

Sample configuration for 25MHz output at port 10.

```
IN3 (25 MHz) -> T0 +-> OUT10 (Ethernet, 25 MHz)
```

#### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 125 of file sampleAppl.c.

#### 6.11.1.3 void IDTSample\_ConfigureSampleConfigureOutput7\_77\_dot\_76MHz ( T\_idtDrvHdlr *hdlr* )

Sample configuration for 77.76 MHz output at port 7.

```
IN3 (25 MHz) -> T0 +-> OUT7 (SONET, 77.76 MHz)
```

#### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 86 of file sampleAppl.c.

#### 6.11.1.4 void IDTSample\_DualMode ( T\_idtDrvHdlr *hdlr* )

Sample configuration for dual mode application.

```
Inputs: IN3 (19.44MHz), IN5 (155.52MHz), IN14 (1.544MHz)
T0 Profile: ST3 SONET
T4 Profile: default
Select XTAL3: done automatically by IDTH1Api_ConfigureOutput function
              based on the output frequency. To manually select XTAL,
              call SetJaXtalId function.
Outputs: OUT1 (19.44MHz), OUT6 (155.52MHz), OUT7 (77.76MHz), OUT9 (1.544MHz)
T0: IN3, IN5, IN14 -> OUT1, OUT6, OUT7 (IN14 is highest priority)
T4: IN3, IN5 -> OUT9
APLL1 XTAL1 at 25MHz & XTAL3 at 24.8832MHz
```

#### Parameters

<i>hdlr</i>	Device driver handler
-------------	-----------------------

Definition at line 410 of file sampleAppl.c.

#### 6.11.1.5 void IDTSample\_GPS ( T\_idtDrvHdlr *hdlr* )

Sample configuration for GPS application.

```
Inputs: IN3 (10MHz), IN4 (10MHz), EX_SYNC1 (1PPS), EX_SYNC2 (1PPS)
```

T0 Profile: BITS / SSU (Wideband) - default  
 Outputs: OUT1 (25MHz), OUT2 (19.44MHz), OUT3 (10MHz), OUT4 (1PPS),  
           OUT6 (25MHz), OUT7 (156.25MHz), OUT9 (1.544MHz), OUT10 (155.52MHz),  
           OUT11 (77.76MHz), FRSYNC\_8K\_1PPS (1PPS), MFRSYNC\_2K\_1PPS (1PPS)  
 APLL1 XTAL1 = 25MHz & APLL2 XTAL2 = 24.8832MHz

#### Parameters

<i>hdr</i>	Device driver handler
------------	-----------------------

Definition at line 1013 of file sampleAppl.c.

#### 6.11.1.6 void IDTSample\_GPS\_1PPS ( T\_idtDrvHdr *hdr* )

Sample configuration for GPS 1PPS application.

Inputs: IN3 (1PPS), IN5 (1PPS)  
 T0 Profile: GPS (15mHz)  
 Outputs: OUT1 (25MHz), OUT2 (19.44MHz), OUT3 (10MHz), OUT4 (1PPS),  
           OUT6 (25MHz), OUT7 (156.25MHz), OUT9 (2.048MHz),  
           OUT10 (155.52MHz), OUT11 (77.76MHz)  
 APLL1 XTAL1 at 25MHz & APLL2 XTAL2 at 24.8832MHz

#### Parameters

<i>hdr</i>	Device driver handler
------------	-----------------------

Definition at line 835 of file sampleAppl.c.

#### 6.11.1.7 void IDTSample\_Sonet ( T\_idtDrvHdr *hdr* )

Sample configuration for SONET application.

Inputs: IN3 (19.44MHz), IN5 (155.52MHz), IN14 (1.544MHz)  
 T0 Profile: ST3 SONET  
 T4 Profile: default  
 Outputs: OUT1 (19.44MHz), OUT9 (1.544MHz), OUT10 (155.52MHz)  
 T0: IN3, IN5, IN14 -> OUT1, OUT10 (IN14 is highest priority)  
 T4: IN3, IN5 -> OUT9  
 APLL2 XTAL2 at 24.8832MHz

#### Parameters

<i>hdr</i>	Device driver handler
------------	-----------------------

Definition at line 294 of file sampleAppl.c.

#### 6.11.1.8 void IDTSample\_SyncE\_LAN ( T\_idtDrvHdr *hdr* )

Sample configuration for SyncE LAN application.

Inputs: IN3 (25MHz), IN14 (2.048MHz)  
 T0 Profile: G.8262 Option 2  
 T4 Profile: BITS / SSU (Wideband)  
 Outputs: OUT1 (25MHz), OUT10 (25.78125), OUT11 (161.1328125MHz), OUT9 (2.048MHz)  
 T0: IN3, IN14 -> OUT1, OUT10, OUT11 (IN14 is highest priority)  
 T4: IN3 -> OUT9  
 APLL2 XTAL4 at 25.78125MHz

**Parameters**

<i>hdr</i>	Device driver handler
------------	-----------------------

Definition at line 720 of file sampleApl.c.

**6.11.1.9 void IDTSample\_SyncE\_Sonet ( T\_idtDrvHdr *hdr* )**

Sample configuration for SyncE SONET application.

```
Inputs: IN3 (25MHz) , IN5 (156.25MHz), IN6 (155.52MHz), IN7 (19.44MHz), IN14 (1.544MHz)
T0 Profile: G.8262 Option 2
T4 Profile: BITS / SSU (Wideband) - default
Outputs: OUT1 (25MHz), OUT2 (19.44MHz), OUT6 (25MHz), OUT7 (156.25MHz),
         OUT9 (1.544MHz), OUT10 (155.52MHz), OUT11 (77.76MHz)
T0: IN3, IN5, IN6, IN7, IN14 -> OUT1, OUT2, OUT6, OUT7, OUT10, OUT11 (IN14 is highest priority)
T4: IN3, IN5, IN6, IN7 -> OUT9
APLL1 XTAL1 at 25MHz & APLL2 XTAL2 at 24.8832MHz
```

**Parameters**

<i>hdr</i>	Device driver handler
------------	-----------------------

Definition at line 534 of file sampleApl.c.

**6.11.1.10 void IDTSample\_SyncE\_WAN ( T\_idtDrvHdr *hdr* )**

Sample configuration for SyncE WAN application.

```
Inputs: IN3 (25MHz), IN5 (156.25MHz), IN14 (1.544MHz)
T0 Profile: G.8262 Option 2
T4 Profile: Default
Outputs: OUT1 (25MHz), OUT6 (25MHz), OUT7 (156.25MHz), OUT9 (1.544MHz)
T0: IN3, IN5, IN14 -> OUT1, OUT10, OUT11 (IN14 has highest priority)
T4: IN3, IN5 -> OUT9
APLL1 XTAL1 at 25MHz
```

**Parameters**

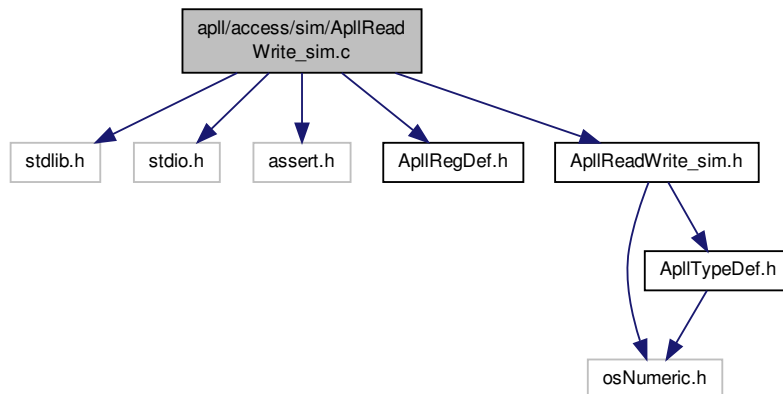
<i>hdr</i>	Device driver handler
------------	-----------------------

Definition at line 170 of file sampleApl.c.

**6.12 apll/access/sim/ApllReadWrite\_sim.c File Reference**

```
#include <stdlib.h>
#include <stdio.h>
#include <assert.h>
#include "ApllRegDef.h"
#include "ApllReadWrite_sim.h"
```

Include dependency graph for `ApllReadWrite_sim.c`:



## Macros

- `#define SIM_REG_MAP_SIZE (0x11)`

## Functions

- `void ApllInit_Sim (void *usrData)`
- `void ApllDelnit_Sim (void *usrData)`
- `T_osUInt8 ApllRead_Sim (void *usrData, T_osUInt8 deviceAddr, T_idtApllRegAddr nAddr)`
- `void ApllWrite_Sim (void *usrData, T_osUInt8 deviceAddr, T_idtApllRegAddr nAddr, T_idtApllRegVal data)`

## Variables

- `T_idtApllRegVal simulatedRegMapApll0 [SIM_REG_MAP_SIZE]`
- `T_idtApllRegVal simulatedRegMapApll1 [SIM_REG_MAP_SIZE]`

### 6.12.1 Macro Definition Documentation

#### 6.12.1.1 `#define SIM_REG_MAP_SIZE (0x11)`

Definition at line 41 of file `ApllReadWrite_sim.c`.

### 6.12.2 Function Documentation

#### 6.12.2.1 `void ApllDelnit_Sim ( void * usrData )`

Definition at line 62 of file `ApllReadWrite_sim.c`.

#### 6.12.2.2 `void ApllInit.Sim ( void * usrData )`

Definition at line 57 of file `ApllReadWrite_sim.c`.



6.12.2.3 T\_osUInt8 ApIIRead\_Sim ( void \* *usrData*, T\_osUInt8 *deviceAddr*, T\_idtApIIRegAddr *nAddr* )

Definition at line 67 of file ApIIReadWrite\_sim.c.

6.12.2.4 void ApIIWrite\_Sim ( void \* *usrData*, T\_osUInt8 *deviceAddr*, T\_idtApIIRegAddr *nAddr*, T\_idtApIIRegVal *data* )

Definition at line 82 of file ApIIReadWrite\_sim.c.

## 6.12.3 Variable Documentation

6.12.3.1 T\_idtApIIRegVal simulatedRegMapApII0[SIM\_REG\_MAP\_SIZE]

### Initial value:

```
= {
    0x00, 0x01, 0x0c, 0x35, 0x0c,
    0x35, 0x0c, 0x35, 0x0c, 0x35,
    0x00, 0x00, 0x00, 0x00, 0x00,
    0x00, 0x00
}
```

Definition at line 43 of file ApIIReadWrite\_sim.c.

6.12.3.2 T\_idtApIIRegVal simulatedRegMapApII1[SIM\_REG\_MAP\_SIZE]

### Initial value:

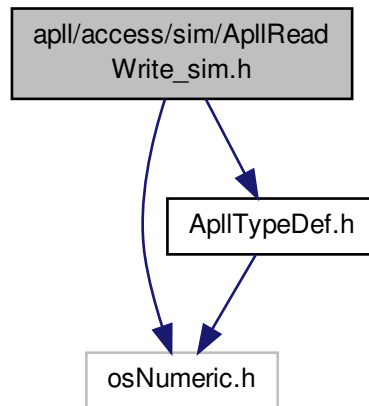
```
= {
    0x00, 0x01, 0x0c, 0x35, 0x0c,
    0x35, 0x0c, 0x35, 0x0c, 0x35,
    0x00, 0x00, 0x00, 0x00, 0x00,
    0x00, 0x00
}
```

Definition at line 50 of file ApIIReadWrite\_sim.c.

## 6.13 apII/access/sim/ApIIReadWrite\_sim.h File Reference

```
#include "osNumeric.h"
#include "ApIITypeDef.h"
```

Include dependency graph for ApIIReadWrite\_sim.h:



## Functions

- T\_osUInt8 [ApIIRead\\_Sim](#) (void \*usrData, T\_osUInt8 deviceAddr, T\_idtApIIRegAddr nAddr)
- void [ApIIRWrite\\_Sim](#) (void \*usrData, T\_osUInt8 deviceAddr, T\_idtApIIRegAddr nAddr, T\_idtApIIRegVal data)
- void [ApIIRInit\\_Sim](#) (void \*userData)
- void [ApIIRDelnit\\_Sim](#) (void \*userData)

### 6.13.1 Function Documentation

#### 6.13.1.1 void ApIIRDelnit\_Sim ( void \* userData )

Definition at line 62 of file ApIIReadWrite\_sim.c.

#### 6.13.1.2 void ApIIRInit\_Sim ( void \* userData )

Definition at line 57 of file ApIIReadWrite\_sim.c.

#### 6.13.1.3 T\_osUInt8 ApIIRead\_Sim ( void \* usrData, T\_osUInt8 deviceAddr, T\_idtApIIRegAddr nAddr )

Definition at line 67 of file ApIIReadWrite\_sim.c.

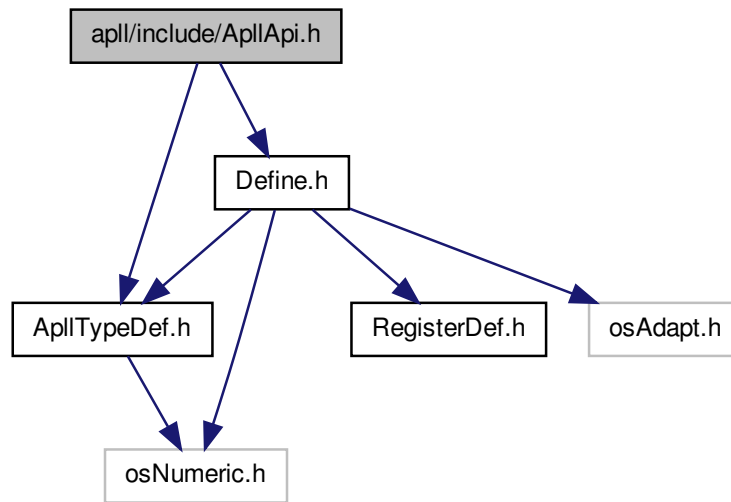
#### 6.13.1.4 void ApIIRWrite\_Sim ( void \* usrData, T\_osUInt8 deviceAddr, T\_idtApIIRegAddr nAddr, T\_idtApIIRegVal data )

Definition at line 82 of file ApIIReadWrite\_sim.c.

## 6.14 apIIR/include/ApIIRApi.h File Reference

```
#include "Define.h"
#include "ApIIRTypeDef.h"
```

Include dependency graph for ApllApi.h:



## Functions

- [T\\_idtApllConfigSel IDTApll\\_GetConfigSel](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllInstId)  
*Function to retrieve APLL configuration.*
- void [IDTApll\\_SetConfigSel](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllInstId, T\_idtApllConfigSel apllConfig)  
*Function to provision APLL based on input configuration.*
- [T\\_idtApllInputClkSrc IDTApll\\_GetInputClkSrc](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllInstId)  
*Function to retrieve selected APLL input frequency source (external/internal)*
- void [IDTApll\\_SetInputClkSrc](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllInstId, T\_idtApllInputClkSrc inputClk)  
*Function to provision APLL input frequency source (external/internal)*
- [T\\_idtApllDividerValue IDTApll\\_GetPreDiv](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllInstId, T\_idtApllConfigSel apllConfig)  
*Function to retrieve pre- (input) divider value.*
- void [IDTApll\\_GetPreDivRange](#) (T\_idtDrvHdlr hdlr, T\_idtApllDividerValue \*minDiv, T\_idtApllDividerValue \*maxDiv)  
*Function to retrieve pre- (input) divisor range.*
- void [IDTApll\\_SetPreDiv](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllInstId, T\_idtApllConfigSel apllConfig, T\_idtApllDividerValue div)  
*Function to provision pre- (input) divider value.*
- [T\\_idtApllDividerValue IDTApll\\_GetFeedbackDiv](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllInstId, T\_idtApllConfigSel apllConfig)  
*Function to retrieve feedback (oscillator) divider value.*
- void [IDTApll\\_GetFeedbackDivRange](#) (T\_idtDrvHdlr hdlr, T\_idtApllDividerValue \*minDiv, T\_idtApllDividerValue \*maxDiv)  
*Function to retrieve feedback (oscillator) divisor range.*
- void [IDTApll\\_SetFeedbackDiv](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllInstId, T\_idtApllConfigSel apllConfig, T\_idtApllDividerValue div)  
*Function to provision feedback (oscillator) divider value.*

- [T\\_idtApplQaDiv IDTApl\\_GetQaDiv](#) (T\_idtDrvHdlr hdlr, [T\\_idtApplId](#) apIInstId, [T\\_idtApplConfigSel](#) apIConfig)
 

*Function to retrieve output port A divisor.*
- void [IDTApl\\_SetQaDiv](#) (T\_idtDrvHdlr hdlr, [T\\_idtApplId](#) apIInstId, [T\\_idtApplConfigSel](#) apIConfig, [T\\_idtApplQaDiv](#) div)
 

*Function to provision output port A divisor.*
- [T\\_idtApplQaDiv IDTApl\\_GetQbDiv](#) (T\_idtDrvHdlr hdlr, [T\\_idtApplId](#) apIInstId, [T\\_idtApplConfigSel](#) apIConfig)
 

*Function to retrieve output port B divisor.*
- void [IDTApl\\_SetQbDiv](#) (T\_idtDrvHdlr hdlr, [T\\_idtApplId](#) apIInstId, [T\\_idtApplConfigSel](#) apIConfig, [T\\_idtApplQbDiv](#) div)
 

*Function to provision output port B divisor.*
- [T\\_idtApplFreqDoublerSel IDTApl\\_GetFreqDoublerSel](#) (T\_idtDrvHdlr hdlr, [T\\_idtApplId](#) apIInstId)
 

*Function to retrieve whether feedback frequency doubling is enabled.*
- void [IDTApl\\_SetFreqDoublerSel](#) (T\_idtDrvHdlr hdlr, [T\\_idtApplId](#) apIInstId, [T\\_idtApplFreqDoublerSel](#) doubler)
 

*Function to enable/disable feedback frequency doubling.*
- [T\\_idtApplXtalId IDTApl\\_GetXtalId](#) (T\_idtDrvHdlr hdlr, [T\\_idtApplId](#) apIInstId)
 

*Function to retrieve oscillator currently used.*
- void [IDTApl\\_SetXtalId](#) (T\_idtDrvHdlr hdlr, [T\\_idtApplId](#) apIInstId, [T\\_idtApplXtalId](#) xtal)
 

*Function to select oscillator.*
- [T\\_idtApplOutputSigType IDTApl\\_GetOutputSigType](#) (T\_idtDrvHdlr hdlr, [T\\_idtApplId](#) apIInstId, [T\\_idtApplOutput](#) output)
 

*Function to retrieve output port signal type.*
- void [IDTApl\\_SetOutputSigType](#) (T\_idtDrvHdlr hdlr, [T\\_idtApplId](#) apIInstId, [T\\_idtApplOutput](#) output, [T\\_idtApplOutputSigType](#) outputSigType)
 

*Function to provision output port signal type.*
- [T\\_idtApplOutputEn IDTApl\\_GetOutputEnState](#) (T\_idtDrvHdlr hdlr, [T\\_idtApplId](#) apIInstId, [T\\_idtApplOutput](#) output)
 

*Function to retrieve output port status (enable/disable)*
- void [IDTApl\\_SetOutputEnState](#) (T\_idtDrvHdlr hdlr, [T\\_idtApplId](#) apIInstId, [T\\_idtApplOutput](#) output, [T\\_idtApplOutputEn](#) enable)
 

*Function to control (enable/disable) output port.*
- [T\\_idtApplMasterResetSync IDTApl\\_GetMasterResetSync](#) (T\_idtDrvHdlr hdlr, [T\\_idtApplId](#) apIInstId)
 

*Function to retrieve reset status of device.*
- void [IDTApl\\_SetMasterResetSync](#) (T\_idtDrvHdlr hdlr, [T\\_idtApplId](#) apIInstId, [T\\_idtApplMasterResetSync](#) reset)
 

*Function to reset APLL.*
- [T\\_idtApplBypass IDTApl\\_GetBypass](#) (T\_idtDrvHdlr hdlr, [T\\_idtApplId](#) apIInstId)
 

*Function to retrieve bypass status of device.*
- void [IDTApl\\_SetBypass](#) (T\_idtDrvHdlr hdlr, [T\\_idtApplId](#) apIInstId, [T\\_idtApplBypass](#) bypass)
 

*Function to set APLL bypass setting.*
- [T\\_idtApplShutoff IDTApl\\_GetShutoff](#) (T\_idtDrvHdlr hdlr, [T\\_idtApplId](#) apIInstId)
 

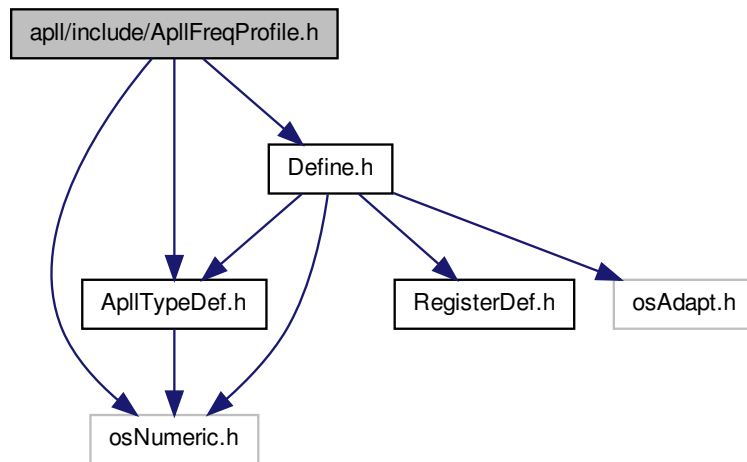
*Function to retrieve shutoff status of device.*
- void [IDTApl\\_SetShutoff](#) (T\_idtDrvHdlr hdlr, [T\\_idtApplId](#) apIInstId, [T\\_idtApplShutoff](#) shutoff)
 

*Function to set APLL shutoff setting.*

## 6.15 apI/include/ApIFreqProfile.h File Reference

```
#include "osNumeric.h"
#include "Define.h"
#include "ApITypeDef.h"
```

Include dependency graph for ApllFreqProfile.h:



## Data Structures

- struct [T\\_idtApllFreqMapping](#)

*Type definition for mapping output frequency to APLL configuration.*

## Enumerations

- enum [T\\_idtApllInputFreqType](#) {  
 APLL\_INPUT\_FREQ\_19440KHz, APLL\_INPUT\_FREQ\_25000KHz, APLL\_INPUT\_FREQ\_77760KHz, APLL\_INPUT\_FREQ\_125000KHz,  
 APLL\_INPUT\_FREQ\_155520KHz, APLL\_INPUT\_FREQ\_25781\_DOT\_25KHz, APLL\_INPUT\_FREQ\_312500KHz, APLL\_INPUT\_FREQ\_128906\_DOT\_25KHz,  
 APLL\_INPUT\_FREQ\_156250KHz, APLL\_INPUT\_FREQ\_8KHz, APLL\_INPUT\_FREQ\_MAX }

*Enumerated type listing supported input frequencies.*

- enum [T\\_idtApllOutputFreqType](#) {  
 APLL\_OUTPUT\_FREQ\_24883\_DOT\_2KHz, APLL\_OUTPUT\_FREQ\_25000KHz, APLL\_OUTPUT\_FREQ\_25781\_DOT\_25KHz, APLL\_OUTPUT\_FREQ\_77760KHz,  
 APLL\_OUTPUT\_FREQ\_78125KHz, APLL\_OUTPUT\_FREQ\_80566\_DOT\_40625KHz, APLL\_OUTPUT\_FREQ\_124416KHz, APLL\_OUTPUT\_FREQ\_125000KHz,  
 APLL\_OUTPUT\_FREQ\_128906\_DOT\_25KHz, APLL\_OUTPUT\_FREQ\_155520KHz, APLL\_OUTPUT\_FREQ\_156250KHz, APLL\_OUTPUT\_FREQ\_161132\_DOT\_8125KHz,  
 APLL\_OUTPUT\_FREQ\_311040KHz, APLL\_OUTPUT\_FREQ\_312500KHz, APLL\_OUTPUT\_FREQ\_322265\_DOT\_625KHz, APLL\_OUTPUT\_FREQ\_622080KHz,  
 APLL\_OUTPUT\_FREQ\_625000KHz, APLL\_OUTPUT\_FREQ\_644531\_DOT\_25KHz, APLL\_OUTPUT\_FREQ\_MAX }

*Enumerated type listing supported output frequencies.*

## Functions

- const [T\\_idtApllFreqMapping](#) \* [IDTApll\\_GetConfigListByFreq](#) ([T\\_idtApllOutputFreqType](#) apllOutputFreq)

*Function to retrieve output configuration given an output frequency.*

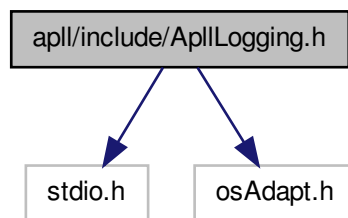
- const `T_idtApIIFreqMapping * IDTAplI_GetConfigListByXtalType (T_idtApIIXtalType apIIXtalFreq)`  
*Function to retrieve output configuration given the oscillator type (frequency)*
- `T_osBool IDTAplI_NullFreqTableEntry (const T_idtApIIFreqMapping *apIIFreqMapping)`  
*Function to check whether the input APLL frequency mapping is NULL (not configured)*
- const `T_idtApIIFreqMapping * IDTAplI_GetCurrentApIIFreqConfig (T_idtApIId apIId, T_idtApIOutput output)`  
*Function to retrieve the current APLL frequency mapping configuration for the output.*

## 6.16 apI/include/ApIILogging.h File Reference

```
#include <stdio.h>
```

```
#include "osAdapt.h"
```

Include dependency graph for ApIILogging.h:



### Macros

- `#define IDT_APLL_API_LOG_HEADER`
- `#define IDT_APLL_API_LOG_ERR(fmt)`
- `#define IDT_APLL_API_LOG_INFO(fmt)`
- `#define IDT_APLL_API_LOG_DEBUG(fmt)`
- `#define IDT_APLL_API_TRACE(fmt) OS_TRACE(fmt)`

## 6.17 apI/include/ApIRegDef.h File Reference

### Enumerations

- enum {  
`REG_CONTROL = 0x00, REG_CLK_SEL = 0x01, REG_PDSEL0_LSB = 0x02, REG_PDSEL0_MSB = 0x03,`  
`REG_PDSEL1_LSB = 0x04, REG_PDSEL1_MSB = 0x05, REG_M0_LSB = 0x06, REG_M0_MSB = 0x07,`  
`REG_M1_LSB = 0x08, REG_M1_MSB = 0x09, REG_ODBSELA0 = 0x0A, REG_ODBSELA1 = 0x0B,`  
`REG_ODBSELB0 = 0x0C, REG_ODBSELB1 = 0x0D, REG_VCXO_SEL = 0x0E, REG_CONFIG_QA = 0x0F,`  
`REG_CONFIG_QB = 0x10, BF_CONFIG_SIZE = 1, BF_CONFIG_MASK = 0x02, BF_CONFIG_LSB = 1,`  
`BF_CLK_SEL_SIZE = 1, BF_CLK_SEL_MASK = 0x01, BF_CLK_SEL_LSB = 0, BF_PDSEL0_LSB_SIZE =`  
`8,`  
`BF_PDSEL0_LSB_MASK = 0xFF, BF_PDSEL0_LSB_LSB = 0, BF_PDSEL0_MSB_SIZE = 7, BF_PDSEL0-`  
`_MSB_MASK = 0x7F,`  
`BF_PDSEL0_MSB_LSB = 0, BF_PDSEL1_LSB_SIZE = 8, BF_PDSEL1_LSB_MASK = 0xFF, BF_PDSEL1-`

```

_LSB_LSB = 0,
BF_PDSEL1_MSB_SIZE = 7, BF_PDSEL1_MSB_MASK = 0x7F, BF_PDSEL1_MSB_LSB = 0, BF_M0_LSB_SIZE = 8,
BF_M0_LSB_MASK = 0xFF, BF_M0_LSB_LSB = 0, BF_M0_MSB_SIZE = 7, BF_M0_MSB_MASK = 0x7F,
BF_M0_MSB_LSB = 0, BF_M1_LSB_SIZE = 8, BF_M1_LSB_MASK = 0xFF, BF_M1_LSB_LSB = 0,
BF_M1_MSB_SIZE = 7, BF_M1_MSB_MASK = 0x7F, BF_M1_MSB_LSB = 0, BF_ODBSELA0_SIZE = 3,
BF_ODBSELA0_MASK = 0x07, BF_ODBSELA0_LSB = 0, BF_ODBSELA1_SIZE = 3, BF_ODBSELA1_MASK = 0x07,
BF_ODBSELA1_LSB = 0, BF_ODBSELB0_SIZE = 3, BF_ODBSELB0_MASK = 0x07, BF_ODBSELB0_LSB = 0,
BF_ODBSELB1_SIZE = 3, BF_ODBSELB1_MASK = 0x07, BF_ODBSELB1_LSB = 0, BF_SEL_DOUBLE_SIZE = 1,
BF_SEL_DOUBLE_MASK = 0x80, BF_SEL_DOUBLE_LSB = 7, BF_MR_SYNC_SIZE = 1, BF_MR_SYNC_MASK = 0x40,
BF_MR_SYNC_LSB = 6, BF_BYPASS_SIZE = 1, BF_BYPASS_MASK = 0x20, BF_BYPASS_LSB = 5,
BF_SHUTOFF_SIZE = 1, BF_SHUTOFF_MASK = 0x10, BF_SHUTOFF_LSB = 4, BF_VCXO_SEL_SIZE = 1,
BF_VCXO_SEL_MASK = 0x01, BF_VCXO_SEL_LSB = 0, BF_LVDS_QA_SIZE = 1, BF_LVDS_QA_MASK = 0x02,
BF_LVDS_QA_LSB = 1, BF_OE_A_SIZE = 1, BF_OE_A_MASK = 0x01, BF_OE_A_LSB = 0,
BF_LVDS_QB_SIZE = 1, BF_LVDS_QB_MASK = 0x02, BF_LVDS_QB_LSB = 1, BF_OE_B_SIZE = 1,
BF_OE_B_MASK = 0x01, BF_OE_B_LSB = 0, REGMAP_APLL_MAX }

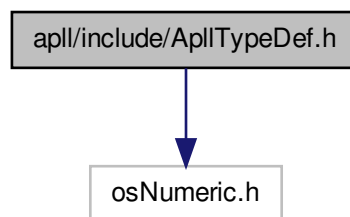
```

*Enumerated type listing register offsets and bit field constants.*

## 6.18 apll/include/ApllTypeDef.h File Reference

```
#include "osNumeric.h"
```

Include dependency graph for ApllTypeDef.h:



### Data Structures

- struct [T\\_idtApllXtal](#)

*Structure containing APLL crystal id and frequency information.*

### Macros

- #define [INVALID\\_DIVIDER\\_VALUE](#) (0xFFFF)

*Define constant indicating invalid divider value.*

## Typedefs

- typedef T\_osUInt16 [T\\_idtApllDividerValue](#)  
*Type define for APLL divider value.*
- typedef T\_osUInt8 [T\\_idtApllRegAddr](#)  
*Type define for APLL register address.*
- typedef T\_osUInt8 [T\\_idtApllRegMask](#)  
*Type define for APLL register value mask.*
- typedef T\_osUInt8 [T\\_idtApllRegVal](#)  
*Type define for APLL register value.*

## Enumerations

- enum [T\\_idtApllId](#) { [APLL\\_INST\\_1](#), [APLL\\_INST\\_2](#), [APLL\\_INST\\_MAX](#) }  
*Enumerated type listing APLL instance within device.*
- enum [T\\_idtApllAccessType](#) { [APLL\\_ACCESS\\_I2C](#), [APLL\\_ACCESS\\_SIM](#), [APLL\\_ACCESS\\_MAX](#) }  
*Enumerated type listing supported access methods.*
- enum [T\\_idtApllConfigSel](#) { [APLL\\_CONFIG0](#) = 0, [APLL\\_CONFIG1](#) = 1, [APLL\\_CONFIG\\_MAX](#) }  
*Enumerated type listing possible configuration for each APLL.*
- enum [T\\_idtApllInputClkSrc](#) { [APLL\\_CLK\\_SEL\\_EXTERNAL](#), [APLL\\_CLK\\_SEL\\_INTERNAL](#), [APLL\\_CLK\\_SEL\\_MAX](#) }  
*Enumerated type listing input ports.*
- enum [T\\_idtApllOutput](#) { [APLL\\_OUTPUT\\_QA](#), [APLL\\_OUTPUT\\_QB](#), [APLL\\_OUTPUT\\_MAX](#) }  
*Enumerated type listing output ports.*
- enum [T\\_idtApllOutputEn](#) { [APLL\\_OUTPUT\\_DISABLE](#), [APLL\\_OUTPUT\\_ENABLE](#), [APLL\\_OUTPUT\\_EN\\_MAX](#) }  
*Enumerated type listing output port status (enable/disable)*
- enum [T\\_idtApllOutputSigType](#) { [APLL\\_OUT\\_SIG\\_LVPECL](#), [APLL\\_OUT\\_SIG\\_LVDS](#), [APLL\\_OUT\\_SIG\\_MAX](#) }  
*Enumerated type listing output signal type.*
- enum [T\\_idtApllOutputSupportedType](#) { [APLL\\_OUT\\_QA\\_ONLY](#), [APLL\\_OUT\\_QB\\_ONLY](#), [APLL\\_OUT\\_QA\\_OR\\_QB](#), [APLL\\_OUT\\_MAX](#) }  
*Enumerated type listing frequency supported by the output.*
- enum [T\\_idtApllQaDiv](#) { [APLL\\_QA\\_ODSEL\\_DIV\\_25](#) = 0, [APLL\\_QA\\_ODSEL\\_DIV\\_5](#) = 1, [APLL\\_QA\\_ODSEL\\_DIV\\_4](#) = 2, [APLL\\_QA\\_ODSEL\\_DIV\\_2](#) = 3, [APLL\\_QA\\_ODSEL\\_DIV\\_1](#) = 4, [APLL\\_QA\\_ODSEL\\_DIV\\_MAX](#) }  
*Enumerated type listing output port A divider values.*
- enum [T\\_idtApllQbDiv](#) { [APLL\\_QB\\_ODSEL\\_DIV\\_8](#) = 0, [APLL\\_QB\\_ODSEL\\_DIV\\_5](#) = 1, [APLL\\_QB\\_ODSEL\\_DIV\\_4](#) = 2, [APLL\\_QB\\_ODSEL\\_DIV\\_2](#) = 3, [APLL\\_QB\\_ODSEL\\_DIV\\_1](#) = 4, [APLL\\_QB\\_ODSEL\\_DIV\\_MAX](#) }  
*Enumerated type listing output port B divider values.*
- enum [T\\_idtApllFreqDoublSel](#) { [APLL\\_FREQ\\_SEL\\_SINGLE](#) = 0, [APLL\\_FREQ\\_SEL\\_DOUBLE](#) = 1, [APLL\\_FREQ\\_SEL\\_MAX](#) }  
*Enumerated type listing feedback frequency doubling values.*
- enum [T\\_idtApllXtalId](#) { [APLL\\_XTAL\\_1\\_APLL1](#), [APLL\\_XTAL\\_2\\_APLL2](#), [APLL\\_XTAL\\_3\\_APLL1](#), [APLL\\_XTAL\\_4\\_APLL2](#), [APLL\\_XTAL\\_MAX](#) }  
*Enumerated type listing crystals.*
- enum [T\\_idtApllXtalType](#) { [APLL\\_XTAL\\_FREQ\\_25000KHz](#), [APLL\\_XTAL\\_FREQ\\_25781\\_DOT\\_25KHz](#), [APLL\\_XTAL\\_FREQ\\_24883\\_DOT\\_2KHz](#), [APLL\\_XTAL\\_FREQ\\_MAX](#) }



Enumerated type listing support crystal frequencies.

- enum `T_idtApllMasterResetSync` { `APLL_OUT_MR_SYNC` = 0, `APLL_IN_MR_SYNC` = 1, `APLL_MR_SYNC_MAX` }

Enumerated type listing Device master reset sync status.

- enum `T_idtApllBypass` { `APLL_BYPASS_NORMAL_OP` = 0, `APLL_BYPASS_BYPASS` = 1, `APLL_BYPASS_MAX` }

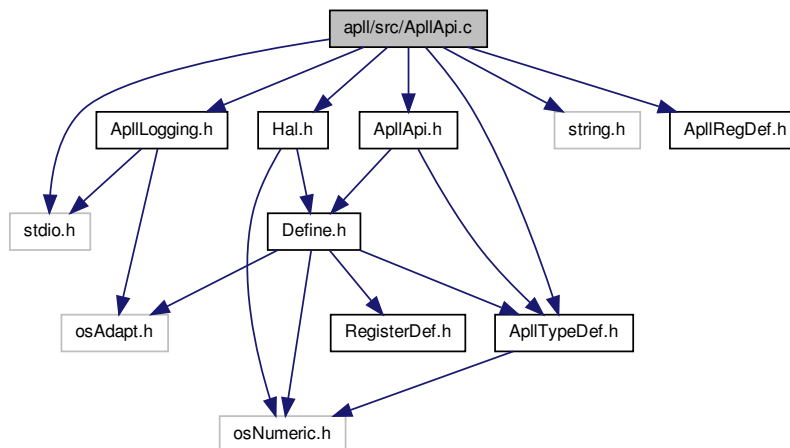
Enumerated type listing Apll bypass status/setting.

- enum `T_idtApllShutoff` { `APLL_SHUTOFF_NORMAL_OP` = 0, `APLL_SHUTOFF_SHUTOFF` = 1, `APLL_SHUTOFF_MAX` }

Enumerated type listing Apll shutoff status/setting.

## 6.19 apll/src/ApllApi.c File Reference

```
#include <stdio.h>
#include <string.h>
#include "Hal.h"
#include "ApllRegDef.h"
#include "ApllTypeDef.h"
#include "ApllApi.h"
#include "ApllLogging.h"
Include dependency graph for ApllApi.c:
```



### Macros

- #define `APLL_DIVIDER_LSB(val)` `((val)&0x00FF)`
- #define `APLL_DIVIDER_MSB(val)` `((val)&0x7F00)>>8)`
- #define `APLL_DIVIDER_VAL(Isb, msb)` `((msb)<<8|(Isb))`
- #define `APLL_PRE_DIV_LSB(val)` `APLL_DIVIDER_LSB(val)`
- #define `APLL_PRE_DIV_MSB(val)` `APLL_DIVIDER_MSB(val)`
- #define `APLL_PRE_DIV_VAL(Isb, msb)` `APLL_DIVIDER_VAL(Isb, msb)`
- #define `APLL_FB_DIV_LSB(val)` `APLL_DIVIDER_LSB(val)`
- #define `APLL_FB_DIV_MSB(val)` `APLL_DIVIDER_MSB(val)`
- #define `APLL_FB_DIV_VAL(Isb, msb)` `APLL_DIVIDER_VAL(Isb, msb)`
- #define `APLL_PRE_DIV_MIN` `(0x0004)`

- #define `APLL_PRE_DIV_MAX` (0x7FFF)
- #define `APLL_FB_DIV_MIN` (0x0005)
- #define `APLL_FB_DIV_MAX` (0x7FFF)
- #define `APLL1_REG_HIGH_BIT` (0)
- #define `APLL2_REG_HIGH_BIT` (1)
- #define `APLL_REG_HIGH_BIT_OFFSET` (7)
- #define `APLL_REG_OFFSET`(apllInstId, base)  
*Utility macro to translate APLL register address.*
- #define `APLL1_REG_VALID_OFFSET`(offset) ((offset >= `REG_CONTROL`) && (offset <= `REG_CONFIG_QB`))  
*Utility macro to sanity check APLL #1 register address.*
- #define `APLL2_REG_VALID_OFFSET`(offset)  
*Utility macro to translate APLL #2 register address.*
- #define `INVALID_XTAL_SEL_VALUE` (0xFF)

## Functions

- `T_idtApplConfigSel IDTApl_GetConfigSel` (T\_idtDrvHdlr hdlr, T\_idtApplId apllInstId)  
*Function to retrieve APLL configuration.*
- void `IDTApl_SetConfigSel` (T\_idtDrvHdlr hdlr, T\_idtApplId apllInstId, T\_idtApplConfigSel apllConfig)  
*Function to provision APLL based on input configuration.*
- `T_idtApplInputClkSrc IDTApl_GetInputClkSrc` (T\_idtDrvHdlr hdlr, T\_idtApplId apllInstId)  
*Function to retrieve selected APLL input frequency source (external/internal)*
- void `IDTApl_SetInputClkSrc` (T\_idtDrvHdlr hdlr, T\_idtApplId apllInstId, T\_idtApplInputClkSrc inputClk)  
*Function to provision APLL input frequency source (external/internal)*
- `T_idtApplDividerValue IDTApl_GetPreDiv` (T\_idtDrvHdlr hdlr, T\_idtApplId apllInstId, T\_idtApplConfigSel apllConfig)  
*Function to retrieve pre- (input) divider value.*
- void `IDTApl_GetPreDivRange` (T\_idtDrvHdlr hdlr, T\_idtApplDividerValue \*minDiv, T\_idtApplDividerValue \*maxDiv)  
*Function to retrieve pre- (input) divisor range.*
- void `IDTApl_SetPreDiv` (T\_idtDrvHdlr hdlr, T\_idtApplId apllInstId, T\_idtApplConfigSel apllConfig, T\_idtApplDividerValue div)  
*Function to provision pre- (input) divider value.*
- void `IDTApl_GetFeedbackDivRange` (T\_idtDrvHdlr hdlr, T\_idtApplDividerValue \*minDiv, T\_idtApplDividerValue \*maxDiv)  
*Function to retrieve feedback (oscillator) divisor range.*
- `T_idtApplDividerValue IDTApl_GetFeedbackDiv` (T\_idtDrvHdlr hdlr, T\_idtApplId apllInstId, T\_idtApplConfigSel apllConfig)  
*Function to retrieve feedback (oscillator) divider value.*
- void `IDTApl_SetFeedbackDiv` (T\_idtDrvHdlr hdlr, T\_idtApplId apllInstId, T\_idtApplConfigSel apllConfig, T\_idtApplDividerValue div)  
*Function to provision feedback (oscillator) divider value.*
- `T_idtApplQaDiv IDTApl_GetQaDiv` (T\_idtDrvHdlr hdlr, T\_idtApplId apllInstId, T\_idtApplConfigSel config)  
*Function to retrieve output port A divisor.*
- void `IDTApl_SetQaDiv` (T\_idtDrvHdlr hdlr, T\_idtApplId apllInstId, T\_idtApplConfigSel config, T\_idtApplQaDiv div)  
*Function to provision output port A divisor.*
- `T_idtApplQbDiv IDTApl_GetQbDiv` (T\_idtDrvHdlr hdlr, T\_idtApplId apllInstId, T\_idtApplConfigSel config)  
*Function to retrieve output port B divisor.*
- void `IDTApl_SetQbDiv` (T\_idtDrvHdlr hdlr, T\_idtApplId apllInstId, T\_idtApplConfigSel config, T\_idtApplQbDiv div)

- Function to provision output port B divisor.*

  - [T\\_idtApllFreqDoublerSel](#) [IDTApll\\_GetFreqDoublerSel](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllInstId)

*Function to retrieve whether feedback frequency doubling is enabled.*

  - void [IDTApll\\_SetFreqDoublerSel](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllInstId, T\_idtApllFreqDoublerSel doubler)

*Function to enable/disable feedback frequency doubling.*

  - [T\\_idtApllXtalId](#) [IDTApll\\_GetXtalId](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllInstId)

*Function to retrieve oscillator currently used.*

  - void [IDTApll\\_SetXtalId](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllInstId, T\_idtApllXtalId xtal)

*Function to select oscillator.*

  - [T\\_idtApllOutputSigType](#) [IDTApll\\_GetOutputSigType](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllInstId, T\_idtApllOutput output)

*Function to retrieve output port signal type.*

  - void [IDTApll\\_SetOutputSigType](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllInstId, T\_idtApllOutput output, T\_idtApllOutputSigType outputSigType)

*Function to provision output port signal type.*

  - [T\\_idtApllOutputEn](#) [IDTApll\\_GetOutputEnState](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllInstId, T\_idtApllOutput output)

*Function to retrieve output port status (enable/disable)*

  - void [IDTApll\\_SetOutputEnState](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllInstId, T\_idtApllOutput output, T\_idtApllOutputEn enable)

*Function to control (enable/disable) output port.*

  - void [IDTApll\\_SetMasterResetSync](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllInstId, T\_idtApllMasterResetSync reset)

*Function to reset APLL.*

  - [T\\_idtApllMasterResetSync](#) [IDTApll\\_GetMasterResetSync](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllInstId)

*Function to retrieve reset status of device.*

  - void [IDTApll\\_SetBypass](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllInstId, T\_idtApllBypass bypass)

*Function to set APLL bypass setting.*

  - [T\\_idtApllBypass](#) [IDTApll\\_GetBypass](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllInstId)

*Function to retrieve bypass status of device.*

  - void [IDTApll\\_SetShutoff](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllInstId, T\_idtApllShutoff shutoff)

*Function to set APLL shutoff setting.*

  - [T\\_idtApllShutoff](#) [IDTApll\\_GetShutoff](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllInstId)

*Function to retrieve shutoff status of device.*

## 6.19.1 Macro Definition Documentation

### 6.19.1.1 #define APLL1\_REG\_HIGH\_BIT (0)

Definition at line 61 of file ApllApi.c.

### 6.19.1.2 #define APLL1\_REG\_VALID\_OFFSET( offset ) ((offset >= REG\_CONTROL) && (offset <= REG\_CONFIG\_QB))

Utility macro to sanity check APLL #1 register address.

#### Parameters

<i>offset</i>	APLL register address
---------------	-----------------------

Definition at line 78 of file ApllApi.c.

6.19.1.3 `#define APLL2_REG_HIGH_BIT(1)`

Definition at line 62 of file ApIiApi.c.

6.19.1.4 `#define APLL2_REG_VALID_OFFSET( offset )`**Value:**

```
(offset >= APLL_REG_OFFSET(APLL_INST_2, REG_CONTROL)) && \
 (offset <= APLL_REG_OFFSET(APLL_INST_2, \
 REG_CONFIG_QB))
```

Utility macro to translate APLL #2 register address.

**Parameters**

<i>offset</i>	APLL register base address
---------------	----------------------------

Definition at line 85 of file ApIiApi.c.

6.19.1.5 `#define APLL_DIVIDER_LSB( val ) ((val)&0x00FF)`

Definition at line 45 of file ApIiApi.c.

6.19.1.6 `#define APLL_DIVIDER_MSB( val ) (((val)&0x7F00)>>8)`

Definition at line 46 of file ApIiApi.c.

6.19.1.7 `#define APLL_DIVIDER_VAL( lsb, msb ) ((msb)<<8|(lsb))`

Definition at line 47 of file ApIiApi.c.

6.19.1.8 `#define APLL_FB_DIV_LSB( val ) APLL_DIVIDER_LSB(val)`

Definition at line 52 of file ApIiApi.c.

6.19.1.9 `#define APLL_FB_DIV_MAX(0x7FFF)`

Definition at line 59 of file ApIiApi.c.

6.19.1.10 `#define APLL_FB_DIV_MIN(0x0005)`

Definition at line 58 of file ApIiApi.c.

6.19.1.11 `#define APLL_FB_DIV_MSB( val ) APLL_DIVIDER_MSB(val)`

Definition at line 53 of file ApIiApi.c.

6.19.1.12 `#define APLL_FB_DIV_VAL( lsb, msb ) APLL_DIVIDER_VAL(lsb, msb)`

Definition at line 54 of file ApIiApi.c.

6.19.1.13 `#define APLL_PRE_DIV_LSB( val ) APLL_DIVIDER_LSB(val)`

Definition at line 49 of file ApllApi.c.

6.19.1.14 `#define APLL_PRE_DIV_MAX (0x7FFF)`

Definition at line 57 of file ApllApi.c.

6.19.1.15 `#define APLL_PRE_DIV_MIN (0x0004)`

Definition at line 56 of file ApllApi.c.

6.19.1.16 `#define APLL_PRE_DIV_MSB( val ) APLL_DIVIDER_MSB(val)`

Definition at line 50 of file ApllApi.c.

6.19.1.17 `#define APLL_PRE_DIV_VAL( lsb, msb ) APLL_DIVIDER_VAL(lsb, msb)`

Definition at line 51 of file ApllApi.c.

6.19.1.18 `#define APLL_REG_HIGH_BIT_OFFSET (7)`

Definition at line 63 of file ApllApi.c.

6.19.1.19 `#define APLL_REG_OFFSET( apllInstId, base )`

**Value:**

```
(apllInstId == APLL_INST_1) ? (base) : \
    (base | (APLL2_REG_HIGH_BIT << APLL_REG_HIGH_BIT_OFFSET))
```

Utility macro to translate APLL register address.

**Parameters**

<i>apllInstId</i>	APLL instance
<i>base</i>	APLL register base address

Definition at line 70 of file ApllApi.c.

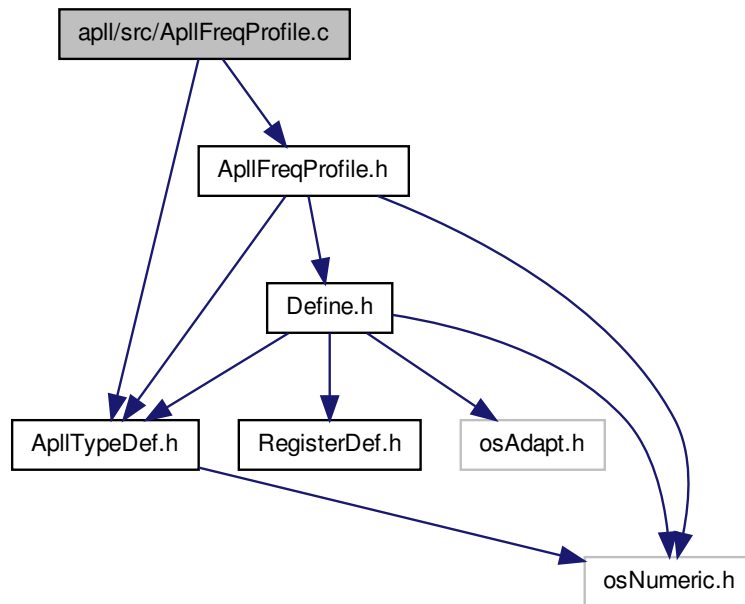
6.19.1.20 `#define INVALID_XTAL_SEL_VALUE (0xFF)`

Definition at line 89 of file ApllApi.c.

## 6.20 apll/src/ApllFreqProfile.c File Reference

```
#include "ApllTypeDef.h"
#include "ApllFreqProfile.h"
```

Include dependency graph for AplIFreqProfile.c:



## Macros

- #define [APLL\\_PRE\\_DIV\\_ETH](#) (19525)
- #define [APLL\\_PRE\\_DIV\\_SONET](#) (9775)
- #define [APLL\\_PRE\\_DIV\\_ETH\\_FEC](#) (15625)
- #define [APLL\\_FB\\_DIV\\_ETH](#) (3124)
- #define [APLL\\_FB\\_DIV\\_SONET](#) (3128)
- #define [APLL\\_FB\\_DIV\\_ETH\\_FEC](#) (3125)
- #define [APLL\\_OUTPUT\\_DIV\\_1](#) (1)
- #define [APLL\\_OUTPUT\\_DIV\\_2](#) (2)
- #define [APLL\\_OUTPUT\\_DIV\\_4](#) (4)
- #define [APLL\\_OUTPUT\\_DIV\\_5](#) (5)
- #define [APLL\\_OUTPUT\\_DIV\\_8](#) (8)
- #define [APLL\\_OUTPUT\\_DIV\\_25](#) (25)
- #define [MAX\\_CONFIG\\_COMBO\\_PER\\_FREQ](#) (1)
- #define [MAX\\_CONFIG\\_COMBO\\_PER\\_VCXO\\_TYPE](#) (6)
- #define [NULL\\_APLL\\_FREQ\\_TABLE\\_ENTRY](#)

*Utility marco for initializing NULL APLL configuration entry.*

## Functions

- `const T_idtAplIFreqMapping * IDTAplIFreq_GetConfigListByFreq (T_idtAplIFreqOutputFreqType aplIFreqOutputFreq)`  
*Function to retrieve output configuration given an output frequency.*
- `const T_idtAplIFreqMapping * IDTAplIFreq_GetConfigListByXtalType (T_idtAplIFreqXtalType aplIFreqVcxoFreq)`  
*Function to retrieve output configuration given the oscillator type (frequency)*
- `T_osBool IDTAplIFreq_NullFreqTableEntry (const T_idtAplIFreqMapping *aplIFreqConfig)`

*Function to check whether the input APLL frequency mapping is NULL (not configured)*

- const `T_idtApIIFreqMapping` \* `IDTApl_GetCurrentApIIFreqConfig` (`T_idtApIIId` apIIId, `T_idtApIIOutput` output)

*Function to retrieve the current APLL frequency mapping configuration for the output.*

## 6.20.1 Macro Definition Documentation

### 6.20.1.1 #define APLL\_FB\_DIV\_ETH (3124)

Definition at line 45 of file `ApIIFreqProfile.c`.

### 6.20.1.2 #define APLL\_FB\_DIV\_ETH\_FEC (3125)

Definition at line 47 of file `ApIIFreqProfile.c`.

### 6.20.1.3 #define APLL\_FB\_DIV\_SONET (3128)

Definition at line 46 of file `ApIIFreqProfile.c`.

### 6.20.1.4 #define APLL\_OUTPUT\_DIV\_1 (1)

Definition at line 50 of file `ApIIFreqProfile.c`.

### 6.20.1.5 #define APLL\_OUTPUT\_DIV\_2 (2)

Definition at line 51 of file `ApIIFreqProfile.c`.

### 6.20.1.6 #define APLL\_OUTPUT\_DIV\_25 (25)

Definition at line 55 of file `ApIIFreqProfile.c`.

### 6.20.1.7 #define APLL\_OUTPUT\_DIV\_4 (4)

Definition at line 52 of file `ApIIFreqProfile.c`.

### 6.20.1.8 #define APLL\_OUTPUT\_DIV\_5 (5)

Definition at line 53 of file `ApIIFreqProfile.c`.

### 6.20.1.9 #define APLL\_OUTPUT\_DIV\_8 (8)

Definition at line 54 of file `ApIIFreqProfile.c`.

### 6.20.1.10 #define APLL\_PRE\_DIV\_ETH (19525)

Definition at line 40 of file `ApIIFreqProfile.c`.

### 6.20.1.11 #define APLL\_PRE\_DIV\_ETH\_FEC (15625)

Definition at line 42 of file `ApIIFreqProfile.c`.

**6.20.1.12 #define APLL\_PRE\_DIV\_SONET (9775)**

Definition at line 41 of file ApIIFreqProfile.c.

**6.20.1.13 #define MAX\_CONFIG\_COMBO\_PER\_FREQ (1)**

Definition at line 57 of file ApIIFreqProfile.c.

**6.20.1.14 #define MAX\_CONFIG\_COMBO\_PER\_VC XO\_TYPE (6)**

Definition at line 58 of file ApIIFreqProfile.c.

**6.20.1.15 #define NULL\_APLL\_FREQ\_TABLE\_ENTRY****Value:**

```
{
    APLL_INPUT_FREQ_MAX,      \
    0,                        \
    0,                        \
    APLL_XTAL_FREQ_MAX,      \
    0,                        \
    APLL_OUTPUT_FREQ_MAX,    \
    APLL_OUT_MAX              \
}
```

Utility marco for initializing NULL APLL configuration entry.

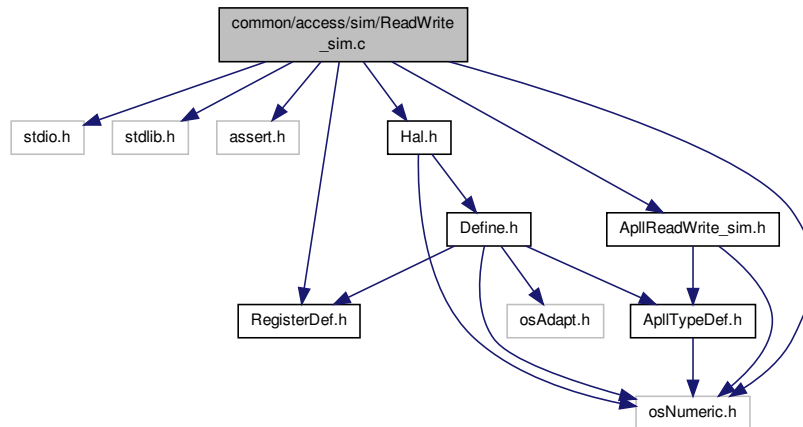
Definition at line 63 of file ApIIFreqProfile.c.

**6.21 common/access/sim/ReadWrite\_sim.c File Reference**

```
#include <stdio.h>
#include <stdlib.h>
#include <assert.h>
#include "RegisterDef.h"
#include "osNumeric.h"
#include "Hal.h"
#include "ApllReadWrite_sim.h"
```



Include dependency graph for ReadWrite\_sim.c:



## Macros

- `#define DRV_MEMMAP_SIZE 0x80`
- `#define NONE_APLL_REG_SPACE_FLAG 0x01`

## Functions

- void `Init_Sim` (void \*usrData)
- void `DelInit_Sim` (void \*usrData)
- T\_osUInt8 `RDByte_Sim` (void \*usrData, T\_osUInt8 devAddr, T\_osUInt8 nAddr)
- void `WRByte_Sim` (void \*usrData, T\_osUInt8 devAddr, T\_osUInt8 nAddr, T\_osUInt8 nData)

## Variables

- int `simDebugFlag` = 0
- T\_osUInt8 `simulatedMemMap` [2][`DRV_MEMMAP_SIZE`]
- T\_osUInt8 `dplOverlayRegisters` []
- T\_osUInt8 `page1Registers` []

### 6.21.1 Macro Definition Documentation

#### 6.21.1.1 `#define DRV_MEMMAP_SIZE 0x80`

Definition at line 45 of file `ReadWrite_sim.c`.

#### 6.21.1.2 `#define NONE_APLL_REG_SPACE_FLAG 0x01`

Definition at line 46 of file `ReadWrite_sim.c`.

## 6.21.2 Function Documentation

### 6.21.2.1 void Delnit\_Sim ( void \* *usrData* )

Definition at line 162 of file ReadWrite\_sim.c.

### 6.21.2.2 void Init\_Sim ( void \* *usrData* )

Definition at line 157 of file ReadWrite\_sim.c.

### 6.21.2.3 T\_osUInt8 RDByte\_Sim ( void \* *usrData*, T\_osUInt8 *devAddr*, T\_osUInt8 *nAddr* )

Definition at line 167 of file ReadWrite\_sim.c.

### 6.21.2.4 void WRByte\_Sim ( void \* *usrData*, T\_osUInt8 *devAddr*, T\_osUInt8 *nAddr*, T\_osUInt8 *nData* )

Definition at line 222 of file ReadWrite\_sim.c.

## 6.21.3 Variable Documentation

### 6.21.3.1 T\_osUInt8 dpllOverlayRegisters[]

#### Initial value:

```
= {
    REG_IN1_IN2_SEL_PRIORITY_CNFG,
    REG_IN3_IN4_SEL_PRIORITY_CNFG,
    REG_IN5_IN6_SEL_PRIORITY_CNFG,
    REG_IN7_IN8_SEL_PRIORITY_CNFG,
    REG_IN9_IN10_SEL_PRIORITY_CNFG,
    REG_IN11_IN12_SEL_PRIORITY_CNFG,
    REG_IN13_IN14_SEL_PRIORITY_CNFG,
    REG_PRIORITY_TABLE1_STS,
    REG_PRIORITY_TABLE2_STS,
    REG_PHASE_LOSS_COARSE_LIMIT_CNFG,
    REG_PHASE_LOSS_FINE_LIMIT_CNFG,
    REG_HOLDOVER_FREQ_LOW_CNFG,
    REG_HOLDOVER_FREQ_MID_CNFG,
    REG_HOLDOVER_FREQ_HIGH_CNFG,
    REG_CURRENT_FREQ_LOW_STS,
    REG_CURRENT_FREQ_MID_STS,
    REG_CURRENT_FREQ_HIGH_STS,
    REG_CURRENT_DPLL_PHASE_LOW_STS,
    REG_CURRENT_DPLL_PHASE_HIGH_STS
}
```

Definition at line 90 of file ReadWrite\_sim.c.

### 6.21.3.2 T\_osUInt8 page1Registers[]

#### Initial value:

```
= {
    REG_DFS_OFF_CNFG,
    REG_T0_PPS_CNFG,
    REG_PH_SLOPE_CNFG,
    REG_T0_ICP_CTRL_CNFG,
    REG_T4_ICP_CTRL_CNFG,
    REG_T4_PPS_CNFG
}
```

Definition at line 139 of file ReadWrite\_sim.c.

6.21.3.3 int simDebugFlag = 0

Definition at line 48 of file ReadWrite\_sim.c.

6.21.3.4 T\_osUInt8 simulatedMemMap[2][DRV\_MEMMAP\_SIZE]

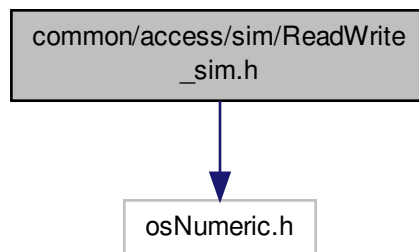
Reset values for device

Definition at line 51 of file ReadWrite\_sim.c.

## 6.22 common/access/sim/ReadWrite\_sim.h File Reference

```
#include "osNumeric.h"
```

Include dependency graph for ReadWrite\_sim.h:



### Functions

- void [Init\\_Sim](#) (void \*usrData)
- void [DelInit\\_Sim](#) (void \*usrData)
- T\_osUInt8 [RDByte\\_Sim](#) (void \*usrData, T\_osUInt8 devAddr, T\_osUInt8 nAddr)
- void [WRByte\\_Sim](#) (void \*usrData, T\_osUInt8 devAddr, T\_osUInt8 nAddr, T\_osUInt8 nData)

#### 6.22.1 Function Documentation

6.22.1.1 void [DelInit\\_Sim](#) ( void \* *usrData* )

Definition at line 162 of file ReadWrite\_sim.c.

6.22.1.2 void [Init\\_Sim](#) ( void \* *usrData* )

Definition at line 157 of file ReadWrite\_sim.c.

6.22.1.3 T\_osUInt8 [RDByte\\_Sim](#) ( void \* *usrData*, T\_osUInt8 *devAddr*, T\_osUInt8 *nAddr* )

Definition at line 167 of file ReadWrite\_sim.c.

6.22.1.4 void WRByte\_Sim ( void \* usrData, T\_osUInt8 devAddr, T\_osUInt8 nAddr, T\_osUInt8 nData )

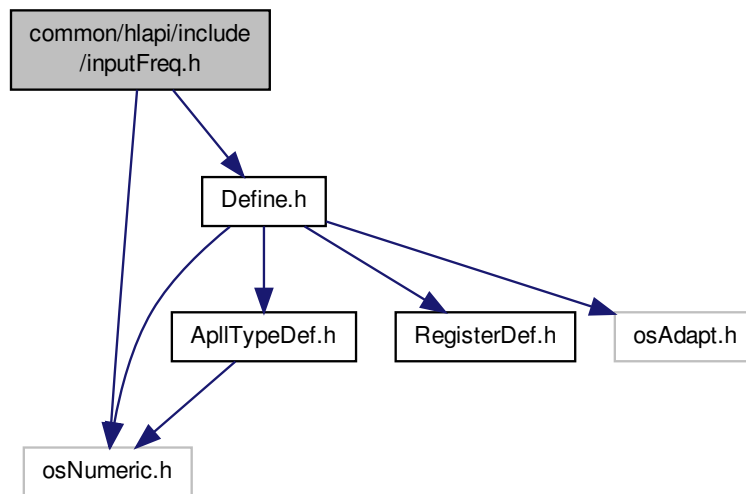
Definition at line 222 of file ReadWrite\_sim.c.

## 6.23 common/hlapi/include/inputFreq.h File Reference

```
#include "osNumeric.h"
```

```
#include "Define.h"
```

Include dependency graph for inputFreq.h:



### Functions

- void [IDTHIApi\\_ConfigureInput1PPS](#) ( T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo)  
*Function to provision input port for 1PPS (1 Hz)*
- void [IDTHIApi\\_ConfigureInputAmi](#) ( T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo, [T\\_idtAmiInputFrequencyBitFieldValue](#) amiSignal)  
*Function to provision input AMI port.*
- void [IDTHIApi\\_ConfigureInputFrequency](#) ( T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo, T\_osUInt32 nFrequency)  
*Function to provision input port.*
- void [IDTHIApi\\_DisableAllInputPriorities](#) ( T\_idtDrvHdlr hdlr)  
*Function to disable all inputs priorities.*

### 6.23.1 Function Documentation

6.23.1.1 void [IDTHIApi\\_ConfigureInput1PPS](#) ( T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo )

Function to provision input port for 1PPS (1 Hz)

Provision input for 1PPS (1 Hz)

## Parameters

<i>hdlr</i>	driver handler
<i>nInputNo</i>	input port number

Definition at line 180 of file inputFreq.c.

#### 6.23.1.2 void IDTHIApi\_ConfigureInputAmi ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nInputNo*, T\_idtAmiInputFrequencyBitFieldValue *amiSignal* )

Function to provision input AMI port.

Provision AMI input

## Parameters

<i>hdlr</i>	driver handler
<i>nInputNo</i>	input port number
<i>amiSignal</i>	Selected AMI signal /see T_idtAmiInputFrequencyBitFieldValue

Definition at line 222 of file inputFreq.c.

#### 6.23.1.3 void IDTHIApi\_ConfigureInputFrequency ( T\_idtDrvHdlr *hdlr*, T\_osUInt8 *nInputNo*, T\_osUInt32 *nFrequency* )

Function to provision input port.

Provision input port specify input frequency

## Parameters

<i>hdlr</i>	driver handler
<i>nInputNo</i>	input port number
<i>nFrequency</i>	input frequency (in kHz)

Definition at line 357 of file inputFreq.c.

#### 6.23.1.4 void IDTHIApi\_DisableAllInputPriorities ( T\_idtDrvHdlr *hdlr* )

Function to disable all inputs priorities.

Provision disable all input priorities

This is different to enabling inputs. Input priorities are used by DPLLs to select input ports to lock to. Disable input priorities tells DPLLs to ignore all inputs.

Use this function when a custom priority is desired. This functions will clear all input priorities first. Input priorities can then be set by calling IDTInput\_SetPriority function.

## Parameters

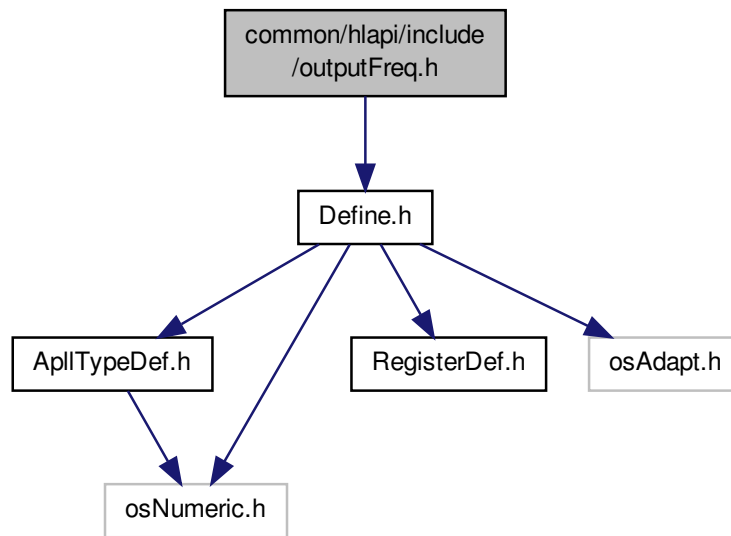
<i>hdlr</i>	Device driver handle
-------------	----------------------

Definition at line 470 of file inputFreq.c.

## 6.24 common/hlapi/include/outputFreq.h File Reference

```
#include "Define.h"
```

Include dependency graph for outputFreq.h:



## Enumerations

- enum `outputFrequency_t` {  
`OutFreq_Invalid`, `OutFreq_64k`, `OutFreq_8k`, `OutFreq_2k`,  
`OutFreq_400`, `OutFreq_1`, `OutFreq_24576k`, `OutFreq_12288k`,  
`OutFreq_6144k`, `OutFreq_4096k`, `OutFreq_2048k`, `OutFreq_32768k`,  
`OutFreq_16384k`, `OutFreq_8192k`, `OutFreq_24704k`, `OutFreq_12352k`,  
`OutFreq_6176k`, `OutFreq_3088k`, `OutFreq_1544k`, `OutFreq_34368k`,  
`OutFreq_44736k`, `OutFreq_26000k`, `OutFreq_13000k`, `OutFreq_30720k`,  
`OutFreq_15360k`, `OutFreq_7680k`, `OutFreq_3840k`, `OutFreq_37056k`,  
`OutFreq_18528k`, `OutFreq_9264k`, `OutFreq_4632k`, `OutFreq_40000k`,  
`OutFreq_20000k`, `OutFreq_10000k`, `OutFreq_5000k`, `OutFreq_622080k`,  
`OutFreq_625000k`, `OutFreq_625000k_66_64`, `OutFreq_311040k`, `OutFreq_312500k`,  
`OutFreq_312500k_66_64`, `OutFreq_155520k`, `OutFreq_156250k`, `OutFreq_156250k_66_64`,  
`OutFreq_77760k`, `OutFreq_51840k`, `OutFreq_38880k`, `OutFreq_25920k`,  
`OutFreq_125000k`, `OutFreq_125000k_66_64`, `OutFreq_19440k`, `OutFreq_25000k`,  
`OutFreq_25000k_66_64`, `OutFreq_6480k`, `OutFreq_24883_DOT_2k`, `OutFreq_78125k`,  
`OutFreq_78125k_66_64`, `OutFreq_124416k`, `OutFreq_MAX` }  
*Enumerated type listing output frequencies.*
- enum `T_sonetGigeMode` { `sonetGigeMode_Matching`, `sonetGigeMode_AllFromDpll1`, `sonetGigeMode_AllFromDpll2`, `sonetGigeMode_MAX` }  
*Enumerated type listing sonetGige modes.*

## Functions

- int `IDTHIApi_ConfigureOutput` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nOutN, `outputFrequency_t` nOutFreq, `T_idtDpllInstance` dpIInstance, `T_sonetGigeMode` sonetGigeMode, `T_idtApIConfigSel` apIConfSel, `T_idtApIOutputSigType` apIOutputSigType, `T_idtApIInputClkSrc` apIClkSource)  
*Function to provision output port.*

- void [IDTHIApi\\_DisableAllOutputs](#) (T\_idtDrvHdlr hdlr)  
*Function to disable all outputs.*
- void [IDTHIApi\\_ClearProvisioning](#) (T\_idtDrvHdlr hdlr)  
*Function to clear saved provisioning used by high level API.*
- void [IDTHIApi\\_PrintOutput](#) (T\_idtDrvHdlr hdlr)
- void [IDTHIApi\\_PrintInput](#) (T\_idtDrvHdlr hdlr)

## 6.24.1 Enumeration Type Documentation

### 6.24.1.1 enum outputFrequency\_t

Enumerated type listing output frequencies.

Enumerator

- OutFreq\_Invalid** Output frequency invalid
- OutFreq\_64k** Output frequency is 64 kHz
- OutFreq\_8k** Output frequency is 8 kHz
- OutFreq\_2k** Output frequency is 2 kHz
- OutFreq\_400** Output frequency is 400 Hz
- OutFreq\_1** Output frequency is 1 Hz (1 PPS)
- OutFreq\_24576k** Output frequency is 24.576 MHz
- OutFreq\_12288k** Output frequency is 12.288 MHz
- OutFreq\_6144k** Output frequency is 6.144 MHz
- OutFreq\_4096k** Output frequency is 4.096 MHz
- OutFreq\_2048k** Output frequency is 2.048 MHz
- OutFreq\_32768k** Output frequency is 32.768 MHz
- OutFreq\_16384k** Output frequency is 16.384MHz
- OutFreq\_8192k** Output frequency is 8.192 MHz
- OutFreq\_24704k** Output frequency is 24.704 MHz
- OutFreq\_12352k** Output frequency is 12.352 MHz
- OutFreq\_6176k** Output frequency is 6.176 MHz
- OutFreq\_3088k** Output frequency is 3.088 MHz
- OutFreq\_1544k** Output frequency is 1.544 MHz
- OutFreq\_34368k** Output frequency is 34.368 MHz
- OutFreq\_44736k** Output frequency is 44.736 MHz
- OutFreq\_26000k** Output frequency is 26 MHz
- OutFreq\_13000k** Output frequency is 13 MHz
- OutFreq\_30720k** Output frequency is 30.72 MHz
- OutFreq\_15360k** Output frequency is 15.36 MHz
- OutFreq\_7680k** Output frequency is 7.68 MHz
- OutFreq\_3840k** Output frequency is 3.84 MHz
- OutFreq\_37056k** Output frequency is 37.056 MHz
- OutFreq\_18528k** Output frequency is 18.528 MHz
- OutFreq\_9264k** Output frequency is 9.264 MHz
- OutFreq\_4632k** Output frequency is 4.632 MHz
- OutFreq\_40000k** Output frequency is 40 MHz

**OutFreq\_20000k** Output frequency is 20 MHz  
**OutFreq\_10000k** Output frequency is 10 MHz  
**OutFreq\_5000k** Output frequency is 5 MHz  
**OutFreq\_622080k** Output frequency is 622.08 MHz  
**OutFreq\_625000k** Output frequency is 625 MHz  
**OutFreq\_625000k\_66\_64** Output frequency is  $625 \times (66/64)$  MHz  
**OutFreq\_311040k** Output frequency is 311.04 MHz  
**OutFreq\_312500k** Output frequency is 312.5 MHz  
**OutFreq\_312500k\_66\_64** Output frequency is  $312.5 \times (66/64)$  MHz  
**OutFreq\_155520k** Output frequency is 155.52 MHz  
**OutFreq\_156250k** Output frequency is 156.25 MHz  
**OutFreq\_156250k\_66\_64** Output frequency is  $156.25 \times (66/64)$  MHz  
**OutFreq\_77760k** Output frequency is 77.76 MHz  
**OutFreq\_51840k** Output frequency is 51.84 MHz  
**OutFreq\_38880k** Output frequency is 38.88 MHz  
**OutFreq\_25920k** Output frequency is 25.92 MHz  
**OutFreq\_125000k** Output frequency is 125 MHz  
**OutFreq\_125000k\_66\_64** Output frequency is  $125 \times (66/64)$  MHz  
**OutFreq\_19440k** Output frequency is 19.44 MHz  
**OutFreq\_25000k** Output frequency is 25 MHz  
**OutFreq\_25000k\_66\_64** Output frequency is  $25 \times (66/64)$  MHz  
**OutFreq\_6480k** Output frequency is 6.48 MHz  
**OutFreq\_24883\_DOT\_2k** Output frequency is 24.8832 MHz  
**OutFreq\_78125k** Output frequency is 78.125 MHz  
**OutFreq\_78125k\_66\_64** Output frequency is 80.56640625 MHz  
**OutFreq\_124416k** Output frequency is 124.416 MHz  
**OutFreq\_MAX**

Definition at line 46 of file outputFreq.h.

#### 6.24.1.2 enum T\_sonetGigeMode

Enumerated type listing sonetGige modes.

Enumerator

**sonetGigeMode\_Matching** DPLL #1 to APLL #1 and DPLL #2 to APLL #2  
**sonetGigeMode\_AllFromDpll1** DPLL #1 to APLL #1 and DPLL #1 to APLL #2  
**sonetGigeMode\_AllFromDpll2** DPLL #2 to APLL #1 and DPLL #2 to APLL #2  
**sonetGigeMode\_MAX**

Definition at line 113 of file outputFreq.h.

### 6.24.2 Function Documentation

#### 6.24.2.1 void IDTHIApi\_ClearProvisioning ( T\_idtDrvHdlr hdlr )

Function to clear saved provisioning used by high level API.

Parameters



<i>hdr</i>	Device driver handle
------------	----------------------

Definition at line 1464 of file outputFreq.c.

```
6.24.2.2 int IDTHIApi_ConfigureOutput ( T_idtDrvHdr hdr, T_osUInt8 nOutN, outputFrequency_t nOutFreq,
T_idtDpllInstance dpllInstance, T_sonetGigeMode sonetGigeMode, T_idtApllConfigSel aplConfSel,
T_idtApllOutputSigType aplOutputSigType, T_idtApllInputClkSrc aplClkSource )
```

Function to provision output port.

Provision output port specifying output frequency and DPLL to use

#### Parameters

<i>hdr</i>	driver handler
<i>nOutN</i>	Output port (1-11)
<i>nOutFreq</i>	Output frequency /see outputFrequency_t for list of supported frequencies
<i>dpllInstance</i>	Dpll Instance (DPLL_INSTANCE_1, DPLL_INSTANCE_2, specify DPLL_INSTANCE_MAX for no specific DPLL)
<i>sonetGigeMode</i>	sonetGige mux configuration.

#### See Also

[T\\_sonetGigeMode](#) This parameter and [dpllInstance](#) determine what output path(s) software may use to generate specified output frequency. The following table illustrates the available paths,

<a href="#">dpllInstance</a>	<a href="#">sonetGigeMode</a>	Avail. Paths
<a href="#">DPLL_INSTANCE_1</a>	Matching	DPLL#1->SonetGigEth#1 only
<a href="#">DPLL_INSTANCE_2</a>	Matching	DPLL#2->SonetGigEth#2 only
<a href="#">DPLL_INSTANCE_MAX</a>	Matching	DPLL#1->SonetGigEth#1 or DPLL#2->SonetGigEth#2
<a href="#">DPLL_INSTANCE_1</a>	AllFromDpll1	DPLL#1->SonetGigEth#1 only
<a href="#">DPLL_INSTANCE_2</a>	AllFromDpll1	DPLL#1->SonetGigEth#2 only
<a href="#">DPLL_INSTANCE_MAX</a>	AllFromDpll1	DPLL#1->SonetGigEth#1 or DPLL#1->SonetGigEth#2
<a href="#">DPLL_INSTANCE_1</a>	AllFromDpll2	DPLL#2->SonetGigEth#1 only
<a href="#">DPLL_INSTANCE_2</a>	AllFromDpll2	DPLL#2->SonetGigEth#2 only
<a href="#">DPLL_INSTANCE_MAX</a>	AllFromDpll2	DPLL#2->SonetGigEth#1 or DPLL#2->SonetGigEth#2

#### Parameters

<i>aplConfSel</i>	Selects the APLL configuration, set to APLL_CONFIG_MAX if output port does not go through APLL, OR if you want to program backup APLL configuration
<i>aplOutputSigType</i>	APLL output signal type, set to APLL_OUT_SIG_MAX if output port does not go through APLL

<i>apllClkSource</i>	APLL clock source (internal or external), set to APLL_CLK_SEL_MAX if output port does not go through APLL
----------------------	---

**Returns**

0-OK, 1-Error, unable to configure output path mux

Definition at line 1261 of file outputFreq.c.

**6.24.2.3 void IDTHIApi.DisableAllOutputs ( T\_idtDrvHdlr *hdlr* )**

Function to disable all outputs.

**Parameters**

<i>hdlr</i>	driver handler
-------------	----------------

Definition at line 1443 of file outputFreq.c.

**6.24.2.4 void IDTHIApi.PrintInput ( T\_idtDrvHdlr *hdlr* )**

Definition at line 948 of file outputFreqString.c.

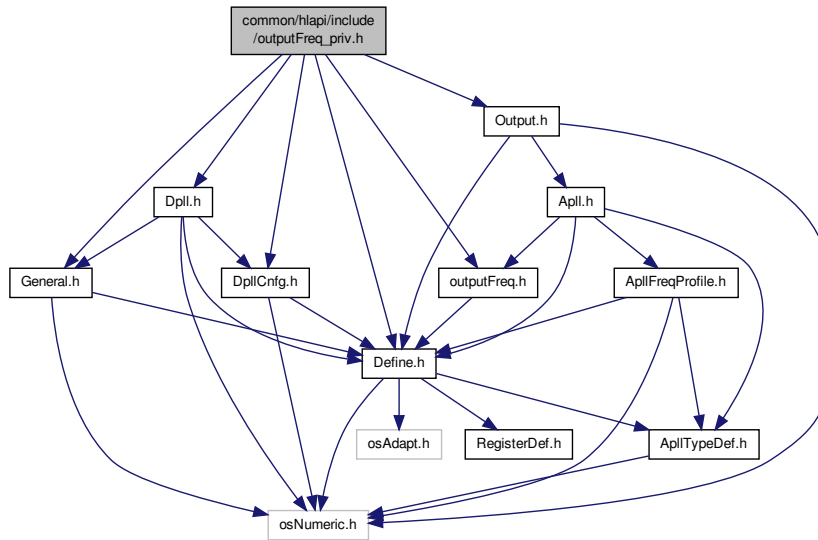
**6.24.2.5 void IDTHIApi.PrintOutput ( T\_idtDrvHdlr *hdlr* )**

Definition at line 1011 of file outputFreqString.c.

**6.25 common/hlapi/include/outputFreq\_priv.h File Reference**

```
#include "Define.h"
#include "General.h"
#include "DpllCnfg.h"
#include "Output.h"
#include "Dpll.h"
#include "outputFreq.h"
```

Include dependency graph for outputFreq\_priv.h:



## Data Structures

- struct [pathSelectorConfig\\_t](#)  
*Structure containing select configuration. Used to translate between frequency and output path configuration.*
- struct [pathSelectorIndex\\_t](#)  
*Structure to index to path selector configs.*

## Macros

- #define [SET\\_BIT](#)(array, bit, set) array[bit] = set  
*set a bit within a bit array*
- #define [CHECK\\_BIT](#)(array, bit) (array[bit] != [OutFreq\\_Invalid](#))  
*check a bit within a bit array*

## Typedefs

- typedef int [validFreq\\_t](#) [[OutFreq\\_MAX](#)]  
*Array type for storing frequency usage.*

## Enumerations

- enum [pathSelectors\\_t](#) {  
[Selector\\_Network](#), [Selector\\_T0DpllSelA](#), [Selector\\_T0DpllSelB](#), [Selector\\_T4DpllSelA](#),  
[Selector\\_T4DpllSelB](#), [Selector\\_SonetGigEth](#), [Selector\\_Any](#), [Selector\\_MAX](#) }  
*Enumerated type listing output path selectors.*

## Functions

- void `IDTHIApi_ConvertFromFreqListToFreqArray` (`outputFrequency_t` frequencies[], `validFreq_t` validFrequencies)
 

*Convert from a frequency list to frequency array.*
- void `IDTHIApi_ApplyFrequencies` (const `outputFrequency_t` \*frequencies, `validFreq_t` validFrequencies, int value)
 

*Function to set status of frequency in frequency array.*
- int `IDTHIApi_IsFreqArrayInFreqList` (const `outputFrequency_t` \*frequencies, `validFreq_t` validFrequencies)
- int `IDTHIApi_IsFrequencyInFreqList` (`outputFrequency_t` frequency, const `outputFrequency_t` validFrequencies[])
 

*Function to verify that frequency is within frequency list.*
- void `IDTHIApi_PrintAvailFrequencies` (`validFreq_t` frequencyArray)
 

*Function to print frequency array in string format.*
- void `IDTHIApi_PrintFrequencyList` (const `outputFrequency_t` frequencies[])
 

*Function to print frequency list in string format.*
- void `IDTHIApi_PrintConfiguration` (`T_IDTPathConfiguration` pathConfig)
 

*Function to print output path configuration to a string format.*
- void `IDTHIApi_PrintOption` (`pathSelectorConfig_t` option, `T_osUInt8` printPort)
 

*Function to print output path configuration option to string format.*
- void `IDTHIApi_PrintSelectedOutputPath` (`T_outputPathType` nPath)
 

*Function to display selected output port path.*
- void `IDTHIApi_PrintOutputHwConfig` (`networkType_t` network, `T_osUInt8` nOutN, `T_osUInt8` internalPort, `T_osUInt8` isEnabled, `T_osUInt8` hasApI, `T_idtApIldividerValue` apIldivVal, `T_idtApIIXtalType` xtalType, `T_osUInt8` outDiv, `T_outputPathType` outPath, `T_idtDpIInstance` dpIInstOrSonetGigEthInst, `T_idtDpIInstance` sonetGigEthInput, `T_idtSonetGigEthOutput` sonetGigEthMode, `T_idtDpIOutputSelectorA` dpISelA, `T_idtDpIOutputSelectorB` dpISelB)

## Variables

- const char \* `IDTHIApi_Frequency2String_c` [`OutFreq_MAX`]

### 6.25.1 Macro Definition Documentation

#### 6.25.1.1 `#define CHECK_BIT( array, bit ) (array[bit] != OutFreq_Invalid)`

check a bit within a bit array

Definition at line 89 of file `outputFreq_priv.h`.

#### 6.25.1.2 `#define SET_BIT( array, bit, set ) array[bit] = set`

set a bit within a bit array

Definition at line 85 of file `outputFreq_priv.h`.

### 6.25.2 Typedef Documentation

#### 6.25.2.1 `typedef int validFreq_t[OutFreq_MAX]`

Array type for storing frequency usage.

Definition at line 104 of file `outputFreq_priv.h`.

### 6.25.3 Enumeration Type Documentation

#### 6.25.3.1 enum pathSelectors\_t

Enumerated type listing output path selectors.

Enumerator

- Selector\_Network** Network selector (SDH/SONET)
- Selector\_T0DpllSelA** T0 Dpll selector A (16E1/16T1/GSM/OBSAI)
- Selector\_T0DpllSelB** T0 Dpll selector B (12E1/GPS/E3/T3)
- Selector\_T4DpllSelA** T4 Dpll selector A (16E1/16T1/GSM/GPS)
- Selector\_T4DpllSelB** T4 Dpll selector B (12E1/24T1/E3/T3)
- Selector\_SonetGigEth** APLL selector (T0 622/T4 622/T0 625/ T4 625/T0 625(66/64)/ T4 625(66/64))
- Selector\_Any** For 77.76 / Eth always available frequencies
- Selector\_MAX**

Definition at line 53 of file outputFreq\_priv.h.

### 6.25.4 Function Documentation

#### 6.25.4.1 void IDTHIApi.ApplyFrequencies ( const outputFrequency\_t \* frequencies, validFreq\_t validFrequencies, int value )

Function to set status of frequency in frequency array.

Parameters

<i>frequencies</i>	Constant frequency list
<i>validFrequencies</i>	
<i>value</i>	Status to set for frequency array

Definition at line 79 of file outputFreqUtil.c.

#### 6.25.4.2 void IDTHIApi.ConvertFromFreqListToFreqArray ( outputFrequency\_t frequencies[], validFreq\_t validFrequencies )

Convert from a frequency list to frequency array.

Parameters

<i>frequencies</i>	Frequency list to convert
<i>validFrequencies</i>	Output frequency array

Definition at line 57 of file outputFreqUtil.c.

#### 6.25.4.3 int IDTHIApi.IsFreqArrayInFreqList ( const outputFrequency\_t \* frequencies, validFreq\_t validFrequencies )

#### 6.25.4.4 int IDTHIApi.IsFrequencyInFreqList ( outputFrequency\_t frequency, const outputFrequency\_t validFrequencies[] )

Function to verify that frequency is within frequency list.

## Parameters

<i>frequency</i>	Frequency to check
<i>validFrequencies</i>	Frequency list to check against

## Returns

1-Frequency is in list, 0-Frequency is not in list

Definition at line 124 of file outputFreqUtil.c.

#### 6.25.4.5 void IDTHIApi.PrintAvailFrequencies ( validFreq\_t frequencyArray )

Function to print frequency array in string format.

## Parameters

<i>frequencyArray</i>	Frequency array
-----------------------	-----------------

Definition at line 317 of file outputFreqString.c.

#### 6.25.4.6 void IDTHIApi.PrintConfiguration ( T\_IDTPathConfiguration pathConfig )

Function to print output path configuration to a string format.

## Parameters

<i>pathConfig</i>	Output path config
-------------------	--------------------

Definition at line 358 of file outputFreqString.c.

#### 6.25.4.7 void IDTHIApi.PrintFrequencyList ( const outputFrequency\_t frequencies[] )

Function to print frequency list in string format.

## Parameters

<i>frequencies</i>	Frequency list
--------------------	----------------

Definition at line 339 of file outputFreqString.c.

#### 6.25.4.8 void IDTHIApi.PrintOption ( pathSelectorConfig\_t option, T\_osUInt8 printPort )

Function to print output path configuration option to string format.

## Parameters

<i>option</i>	Output path configuration option.
<i>printPort</i>	Flag to indicate whether port information is also displayed

Definition at line 387 of file outputFreqString.c.

6.25.4.9 void IDTHIApi\_PrintOutputHwConfig ( networkType\_t network, T\_osUInt8 nOutN, T\_osUInt8 internalPort, T\_osUInt8 isEnabled, T\_osUInt8 hasAplI, T\_idtAplIDividerValue aplIDivVal, T\_idtAplIXtalType xtalType, T\_osUInt8 outDiv, T\_outputPathType outPath, T\_idtDpllInstance dpllInstOrSonetGigEthInst, T\_idtDpllInstance sonetGigEthInput, T\_idtSonetGigEthOutput sonetGigEthMode, T\_idtDpllOutputSelectorA dpllSelA, T\_idtDpllOutputSelectorB dpllSelB )

Definition at line 581 of file outputFreqString.c.

6.25.4.10 void IDTHIApi\_PrintSelectedOutputPath ( T\_outputPathType nPath )

Function to display selected output port path.

#### Parameters

<i>nPath</i>	output port path
--------------	------------------

Definition at line 443 of file outputFreqString.c.

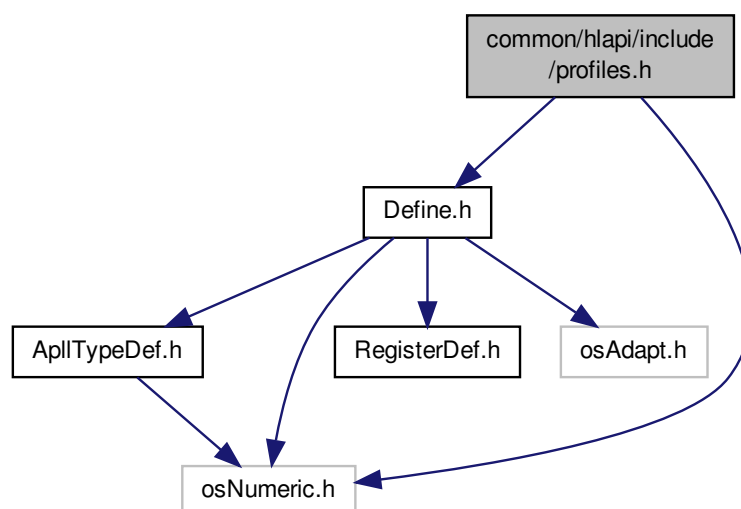
## 6.25.5 Variable Documentation

6.25.5.1 const char\* IDTHIApi\_Frequency2String\_c[OutFreq\_MAX]

Definition at line 77 of file outputFreqString.c.

## 6.26 common/hlapi/include/profiles.h File Reference

```
#include "Define.h"
#include "osNumeric.h"
Include dependency graph for profiles.h:
```



## Functions

- void `IDTHIApi_gr253SonetStratum3` (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
DPLL configuration for GR-253 (SONET) Stratum 3.
- void `IDTHIApi_gr1244Stratum3` (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
DPLL configuration for GR-1244 Stratum 3.
- void `IDTHIApi_smc` (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
DPLL configuration for SMC.
- void `IDTHIApi_g8262EecOption1` (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
DPLL configuration for G-8262 Option 1.
- void `IDTHIApi_g8262EecOption2` (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
DPLL configuration for G-8262 Option 2.
- void `IDTHIApi_g813Option1` (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
DPLL configuration for G-813 Option 1.
- void `IDTHIApi_g813Option2` (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
DPLL configuration for G-813 Option 2.
- void `IDTHIApi_pps` (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
DPLL configuration for 1 pulse per second (PPS)
- void `IDTHIApi_wideband` (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
DPLL configuration for wideband.

### 6.26.1 Function Documentation

#### 6.26.1.1 void IDTHIApi\_g813Option1 ( T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll )

DPLL configuration for G-813 Option 1.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

Definition at line 396 of file profiles.c.

#### 6.26.1.2 void IDTHIApi\_g813Option2 ( T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll )

DPLL configuration for G-813 Option 2.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

Definition at line 408 of file profiles.c.

#### 6.26.1.3 void IDTHIApi\_g8262EecOption1 ( T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll )

DPLL configuration for G-8262 Option 1.

##### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance



Definition at line 258 of file profiles.c.

6.26.1.4 void IDTHIApi\_g8262EecOption2 ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

DPLL configuration for G-8262 Option 2.

Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

Definition at line 327 of file profiles.c.

6.26.1.5 void IDTHIApi\_gr1244Stratum3 ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

DPLL configuration for GR-1244 Stratum 3.

Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

Definition at line 120 of file profiles.c.

6.26.1.6 void IDTHIApi\_gr253SonetStratum3 ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

DPLL configuration for GR-253 (SONET) Stratum 3.

Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

Definition at line 51 of file profiles.c.

6.26.1.7 void IDTHIApi\_pps ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

DPLL configuration for 1 pulse per second (PPS)

Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

Definition at line 421 of file profiles.c.

6.26.1.8 void IDTHIApi\_smc ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

DPLL configuration for SMC.

Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

Definition at line 189 of file profiles.c.

### 6.26.1.9 void IDTHIApi\_wideband ( T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll )

DPLL configuration for wideband.

#### Parameters

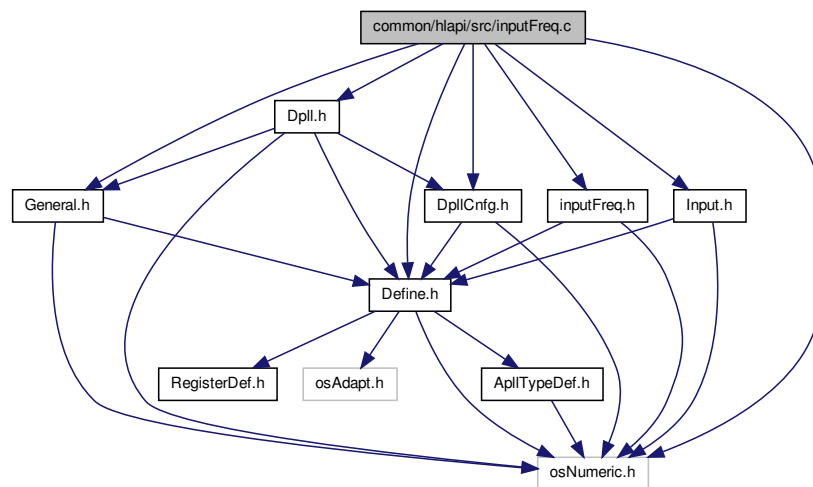
<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

Definition at line 523 of file profiles.c.

## 6.27 common/hlapi/src/inputFreq.c File Reference

```
#include "osNumeric.h"
#include "Define.h"
#include "Input.h"
#include "General.h"
#include "DpllCnfg.h"
#include "Dpll.h"
#include "inputFreq.h"
```

Include dependency graph for inputFreq.c:



### Data Structures

- struct [T\\_IDTFreq2bfVal](#)  
Structure to contain translation information for frequency to bitfield value.
- struct [T\\_idtHfDivEntry](#)  
Structure to use as high frequency (HF) divider information.

### Functions

- void [IDTHIApi\\_ConfigureInput1PPS](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo)

*Function to provision input port for 1PPS (1 Hz)*

- void [IDTHIApi\\_ConfigureInputAmi](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo, T\_idtAmiInputFrequencyBitFieldValue amiSignal)

*Function to provision input AMI port.*

- void [IDTHIApi\\_ConfigureInputFrequency](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo, T\_osUInt32 nFrequency)

*Function to provision input port.*

- void [IDTHIApi\\_DisableAllInputPriorities](#) (T\_idtDrvHdlr hdlr)

*Function to disable all inputs priorities.*

## 6.27.1 Function Documentation

### 6.27.1.1 void IDTHIApi\_ConfigureInput1PPS ( T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo )

Function to provision input port for 1PPS (1 Hz)

#### Parameters

<i>hdlr</i>	driver handler
<i>nInputNo</i>	input port number

Definition at line 180 of file inputFreq.c.

### 6.27.1.2 void IDTHIApi\_ConfigureInputAmi ( T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo, T\_idtAmiInputFrequencyBitFieldValue amiSignal )

Function to provision input AMI port.

#### Parameters

<i>hdlr</i>	driver handler
<i>nInputNo</i>	input port number
<i>amiSignal</i>	Selected AMI signal /see T_idtAmiInputFrequencyBitFieldValue

Definition at line 222 of file inputFreq.c.

### 6.27.1.3 void IDTHIApi\_ConfigureInputFrequency ( T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo, T\_osUInt32 nFrequency )

Function to provision input port.

#### Parameters

<i>hdlr</i>	driver handler
<i>nInputNo</i>	input port number
<i>nFrequency</i>	input frequency (in kHz)

Definition at line 357 of file inputFreq.c.

### 6.27.1.4 void IDTHIApi\_DisableAllInputPriorities ( T\_idtDrvHdlr hdlr )

Function to disable all inputs priorities.

This is different to enabling inputs. Input priorities are used by DLLs to select input ports to lock to. Disable input priorities tells DLLs to ignore all inputs.

Use this function when a custom priority is desired. This functions will clear all input priorities first. Input priorities

can then be set by calling `IDTInput_SetPriority` function.

#### Parameters

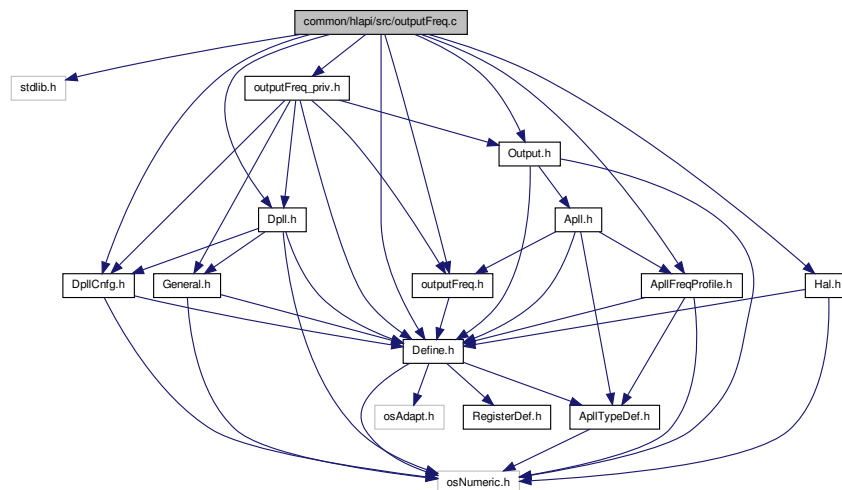
<i>hdr</i>	Device driver handle
------------	----------------------

Definition at line 470 of file `inputFreq.c`.

## 6.28 common/hlapi/src/outputFreq.c File Reference

```
#include <stdlib.h>
#include "Define.h"
#include "Dpll.h"
#include "Hal.h"
#include "Output.h"
#include "DpllCnfg.h"
#include "outputFreq.h"
#include "outputFreq_priv.h"
#include "ApplFreqProfile.h"
#include "Appl.h"
#include "ApplTypeDef.h"
#include "RegisterDef.h"
#include "osAdapt.h"
#include "osNumeric.h"
```

Include dependency graph for `outputFreq.c`:



### Macros

- `#define MAX_SUPPORTED_FREQUENCIES 9`
- `#define OUTMUX_ENTRY(sel, selval, div, path, inst) { Selector_##sel, selval, div, OutputPath_##path, inst }`

*Macro to reduce size of output path configuration entries. Used to reduce size of table so that it fits inside 80 columns.*

### Functions

- `void IDTHIApi_RetrieveOutputPathMuxFromHardware (T_idtDrvHdlr hdlr, T_IDTPathConfiguration *path-Config_p)`

*Function to retrieve output path configuration from hardware.*

- int [IDTHIApi\\_ConfigureOutput](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN, [outputFrequency\\_t](#) nOutFreq, [T\\_idtDpll-Instance](#) dpllInstance, [T\\_sonetGigeMode](#) sonetGigeMode, [T\\_idtApIConfSel](#) apIConfSel, [T\\_idtApIOutput-SigType](#) apIOutputSigType, [T\\_idtApIInputClkSrc](#) apIClkSource)  
*Function to provision output port.*
- void [IDTHIApi\\_DisableAllOutputs](#) (T\_idtDrvHdlr hdlr)  
*Function to disable all outputs.*
- void [IDTHIApi\\_ClearProvisioning](#) (T\_idtDrvHdlr hdlr)  
*Function to clear saved provisioning used by high level API.*

## 6.28.1 Macro Definition Documentation

### 6.28.1.1 #define MAX\_SUPPORTED\_FREQUENCIES 9

Definition at line 53 of file outputFreq.c.

### 6.28.1.2 #define OUTMUX\_ENTRY( sel, selval, div, path, inst ) { Selector\_##sel, selval, div, OutputPath\_##path, inst }

Macro to reduce size of output path configuration entries. Used to reduce size of table so that it fits inside 80 columns.

Definition at line 61 of file outputFreq.c.

## 6.28.2 Function Documentation

### 6.28.2.1 void IDTHIApi\_ClearProvisioning ( T\_idtDrvHdlr hdlr )

Function to clear saved provisioning used by high level API.

#### Parameters

<i>hdlr</i>	Device driver handle
-------------	----------------------

Definition at line 1464 of file outputFreq.c.

### 6.28.2.2 int IDTHIApi\_ConfigureOutput ( T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN, [outputFrequency\\_t](#) nOutFreq, [T\\_idtDpllInstance](#) dpIInstance, [T\\_sonetGigeMode](#) sonetGigeMode, [T\\_idtApIConfSel](#) apIConfSel, [T\\_idtApIOutputSigType](#) apIOutputSigType, [T\\_idtApIInputClkSrc](#) apIClkSource )

Function to provision output port.

#### Parameters

<i>hdlr</i>	driver handler
<i>nOutN</i>	Output port (1-11)
<i>nOutFreq</i>	Output frequency /see <a href="#">outputFrequency_t</a> for list of supported frequencies
<i>dpIInstance</i>	Dpll Instance (DPLL_INSTANCE_1, DPLL_INSTANCE_2, specify DPLL_INSTANCE_MAX for no specific DPLL)
<i>sonetGigeMode</i>	sonetGige mux configuration.

#### See Also

[T\\_sonetGigeMode](#) This parameter and [dpIInstance](#) determine what output path(s) software may use to generate specified output frequency. The following table illustrates the available paths,

dppllInstance	sonetGigeMode	Avail. Paths
DPLL_INSTANCE_1	Matching	DPLL#1->SonetGigEth#1 only
DPLL_INSTANCE_2	Matching	DPLL#2->SonetGigEth#2 only
DPLL_INSTANCE_MAX	Matching	DPLL#1->SonetGigEth#1 or DPLL#2->SonetGigEth#2
DPLL_INSTANCE_1	AllFromDpll1	DPLL#1->SonetGigEth#1 only
DPLL_INSTANCE_2	AllFromDpll1	DPLL#1->SonetGigEth#2 only
DPLL_INSTANCE_MAX	AllFromDpll1	DPLL#1->SonetGigEth#1 or DPLL#1->SonetGigEth#2
DPLL_INSTANCE_1	AllFromDpll2	DPLL#2->SonetGigEth#1 only
DPLL_INSTANCE_2	AllFromDpll2	DPLL#2->SonetGigEth#2 only
DPLL_INSTANCE_MAX	AllFromDpll2	DPLL#2->SonetGigEth#1 or DPLL#2->SonetGigEth#2

#### Parameters

<i>apllConfSel</i>	Selects the APLL configuration, set to APLL_CONFIG_MAX if output port does not go through APLL, <i>OR</i> if you want to program backup APLL configuration
<i>apllOutputSig-Type</i>	APLL output signal type, set to APLL_OUT_SIG_MAX if output port does not go through APLL
<i>apllClkSource</i>	APLL clock source (internal or external), set to APLL_CLK_SEL_MAX if output port does not go through APLL

#### Returns

0-OK, 1-Error, unable to configure output path mux

Definition at line 1261 of file outputFreq.c.

#### 6.28.2.3 void IDTHIApi\_DisableAllOutputs ( T\_idtDrvHdlr *hdlr* )

Function to disable all outputs.

#### Parameters

<i>hdlr</i>	driver handler
-------------	----------------

Definition at line 1443 of file outputFreq.c.

#### 6.28.2.4 void IDTHIApi\_RetrieveOutputPathMuxFromHardware ( T\_idtDrvHdlr *hdlr*, T\_IDTPathConfiguration \* *pathConfig\_p* )

Function to retrieve output path configuration from hardware.

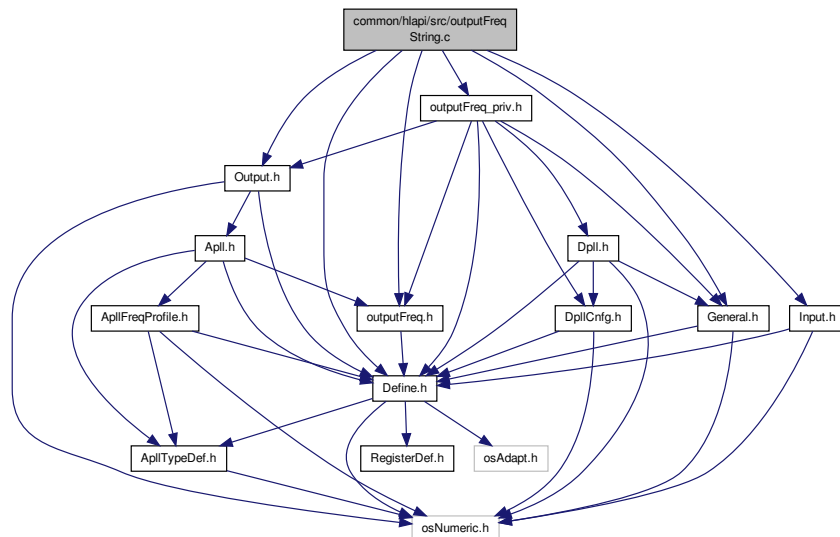
## Parameters

<i>hdr</i>	Device driver handler
<i>pathConfig_p</i>	Output path configuration

Definition at line 282 of file outputFreq.c.

## 6.29 common/hlapi/src/outputFreqString.c File Reference

```
#include "Define.h"
#include "Output.h"
#include "Input.h"
#include "General.h"
#include "outputFreq.h"
#include "outputFreq_priv.h"
Include dependency graph for outputFreqString.c:
```



## Data Structures

- struct [T\\_apllOutputFrequencyEntry](#)

*Structure used to translate APLL configuration and output port frequency.*

## Enumerations

- enum [T\\_outFreqLookupIdx](#) {  
[outFreqLookupIdx\\_Dpll77p76](#), [outFreqLookupIdx\\_Dpll12E1](#), [outFreqLookupIdx\\_Dpll16E1](#), [outFreqLookupIdx\\_Dpll16T1](#),  
[outFreqLookupIdx\\_DpllE3](#), [outFreqLookupIdx\\_DpllT3](#), [outFreqLookupIdx\\_DpllGsm](#), [outFreqLookupIdx\\_DpllObsai](#),  
[outFreqLookupIdx\\_DpllEth](#), [outFreqLookupIdx\\_Dpll24T1](#), [outFreqLookupIdx\\_DpllGps](#), [outFreqLookupIdx\\_SonetGigEthSonet](#),  
[outFreqLookupIdx\\_SonetGigEthEth](#), [outFreqLookupIdx\\_SonetGigEthFec](#), [outFreqLookupIdx\\_MAX](#) }

## Functions

- void [IDTHIApi\\_PrintAvailFrequencies](#) ([validFreq\\_t](#) frequencyArray)  
*Function to print frequency array in string format.*
- void [IDTHIApi\\_PrintFrequencyList](#) (const [outputFrequency\\_t](#) frequencies[])  
*Function to print frequency list in string format.*
- void [IDTHIApi\\_PrintConfiguration](#) ([T\\_IDTPathConfiguration](#) pathConfig)  
*Function to print output path configuration to a string format.*
- void [IDTHIApi\\_PrintOption](#) ([pathSelectorConfig\\_t](#) option, [T\\_osUInt8](#) printPort)  
*Function to print output path configuration option to string format.*
- void [IDTHIApi\\_PrintSelectedOutputPath](#) ([T\\_outputPathType](#) nPath)  
*Function to display selected output port path.*
- void [IDTHIApi\\_PrintOutputHwConfig](#) ([networkType\\_t](#) network, [T\\_osUInt8](#) nOutN, [T\\_osUInt8](#) internalPort, [T\\_osUInt8](#) isEnabled, [T\\_osUInt8](#) hasApI, [T\\_idtApIDividerValue](#) apIldivVal, [T\\_idtApIXtalType](#) xtalType, [T\\_osUInt8](#) outDiv, [T\\_outputPathType](#) outputPath, [T\\_idtDpllInstance](#) dpllInstOrSonetGigEthInst, [T\\_idtDpllInstance](#) sonetGigEthInput, [T\\_idtSonetGigEthOutput](#) sonetGigeMode, [T\\_idtDpllOutputSelectorA](#) dpllSelA, [T\\_idtDpllOutputSelectorB](#) dpllSelB)
- void [IDTHIApi\\_PrintInputHwConfig](#) ([T\\_osUInt8](#) nInputN, [T\\_osUInt8](#) internalPort, [networkType\\_t](#) networkType, [T\\_osUInt8](#) isEnabled, [T\\_idtHighFrequencyDivisor](#) nUsage, [T\\_osUInt16](#) nFactor, [T\\_idtInputDividerMux](#) nDivider, [T\\_idtInputFrequencyBitfieldValue](#) nFrequency, [T\\_osUInt8](#) numberOfDpll, [T\\_osUInt8](#) priorities[])
- void [IDTHIApi\\_PrintInput](#) ([T\\_idtDrvHdlr](#) hdlr)
- void [IDTHIApi\\_PrintOutput](#) ([T\\_idtDrvHdlr](#) hdlr)

## Variables

- const char \* [IDTHIApi\\_Frequency2String\\_c](#) [[OutFreq\\_MAX](#)]

## 6.29.1 Enumeration Type Documentation

### 6.29.1.1 enum [T\\_outFreqLookupIdx](#)

#### Enumerator

**[outFreqLookupIdx\\_Dpll77p76](#)** DPLL 77.76MHz  
**[outFreqLookupIdx\\_Dpll12E1](#)** DPLL 12E1  
**[outFreqLookupIdx\\_Dpll16E1](#)** DPLL 16E1  
**[outFreqLookupIdx\\_Dpll16T1](#)** DPLL 16T1  
**[outFreqLookupIdx\\_DpllE3](#)** DPLL E3  
**[outFreqLookupIdx\\_DpllT3](#)** DPLL T3  
**[outFreqLookupIdx\\_DpllGsm](#)** DPLL GSM  
**[outFreqLookupIdx\\_DpllObsai](#)** DPLL OBSAI  
**[outFreqLookupIdx\\_DpllEth](#)** DPLL 24T1  
**[outFreqLookupIdx\\_Dpll24T1](#)** DPLL 24T1  
**[outFreqLookupIdx\\_DpllGps](#)** DPLL GPS  
**[outFreqLookupIdx\\_SonetGigEthSonet](#)** SONET/GIGE SONET  
**[outFreqLookupIdx\\_SonetGigEthEth](#)** SONET/GIGE ETH  
**[outFreqLookupIdx\\_SonetGigEthFec](#)** SONET/GIGE FEC  
**[outFreqLookupIdx\\_MAX](#)**

Definition at line 45 of file [outputFreqString.c](#).



## 6.29.2 Function Documentation

### 6.29.2.1 void IDTHIApi.PrintAvailFrequencies ( validFreq\_t frequencyArray )

Function to print frequency array in string format.

#### Parameters

<i>frequencyArray</i>	Frequency array
-----------------------	-----------------

Definition at line 317 of file outputFreqString.c.

### 6.29.2.2 void IDTHIApi.PrintConfiguration ( T\_IDTPathConfiguration pathConfig )

Function to print output path configuration to a string format.

#### Parameters

<i>pathConfig</i>	Output path config
-------------------	--------------------

Definition at line 358 of file outputFreqString.c.

### 6.29.2.3 void IDTHIApi.PrintFrequencyList ( const outputFrequency\_t frequencies[] )

Function to print frequency list in string format.

#### Parameters

<i>frequencies</i>	Frequency list
--------------------	----------------

Definition at line 339 of file outputFreqString.c.

### 6.29.2.4 void IDTHIApi.PrintInput ( T\_idtDrvHdlr hdlr )

Definition at line 948 of file outputFreqString.c.

### 6.29.2.5 void IDTHIApi.PrintInputHwConfig ( T\_osUInt8 nInputN, T\_osUInt8 internalPort, networkType\_t networkType, T\_osUInt8 isEnabled, T\_idtHighFrequencyDivisor nUsage, T\_osUInt16 nFactor, T\_idtInputDividerMux nDivider, T\_idtInputFrequencyBitfieldValue nFrequency, T\_osUInt8 numberOfDpll, T\_osUInt8 priorities[] )

Definition at line 773 of file outputFreqString.c.

### 6.29.2.6 void IDTHIApi.PrintOption ( pathSelectorConfig\_t option, T\_osUInt8 printPort )

Function to print output path configuration option to string format.

#### Parameters

<i>option</i>	Output path configuration option.
<i>printPort</i>	Flag to indicate whether port information is also displayed

Definition at line 387 of file outputFreqString.c.

6.29.2.7 void IDTHIApi\_PrintOutput ( T\_idtDrvHdlr *hdlr* )

Definition at line 1011 of file outputFreqString.c.

6.29.2.8 void IDTHIApi\_PrintOutputHwConfig ( networkType\_t *network*, T\_osUInt8 *nOutN*, T\_osUInt8 *internalPort*, T\_osUInt8 *isEnabled*, T\_osUInt8 *hasAppl*, T\_idtApIldividerValue *apIldivVal*, T\_idtApIXtalType *xtalType*, T\_osUInt8 *outDiv*, T\_outputPathType *outPath*, T\_idtDpIIInstance *dpIIInstOrSonetGigEthInst*, T\_idtDpIIInstance *sonetGigEthInput*, T\_idtSonetGigEthOutput *sonetGigEthMode*, T\_idtDpIIOutputSelectorA *dpIISelA*, T\_idtDpIIOutputSelectorB *dpIISelB* )

Definition at line 581 of file outputFreqString.c.

6.29.2.9 void IDTHIApi\_PrintSelectedOutputPath ( T\_outputPathType *nPath* )

Function to display selected output port path.

#### Parameters

<i>nPath</i>	output port path
--------------	------------------

Definition at line 443 of file outputFreqString.c.

### 6.29.3 Variable Documentation

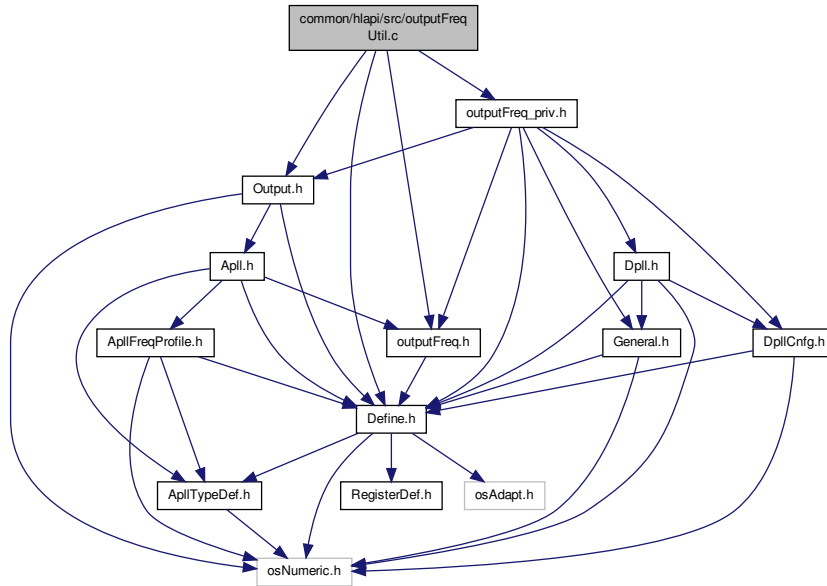
6.29.3.1 const char\* IDTHIApi\_Frequency2String\_c[OutFreq\_MAX]

Definition at line 77 of file outputFreqString.c.

## 6.30 common/hlapi/src/outputFreqUtil.c File Reference

```
#include "Define.h"
#include "Output.h"
#include "outputFreq.h"
#include "outputFreq_priv.h"
```

Include dependency graph for outputFreqUtil.c:



**Functions**

- void [IDTHIApi\\_ConvertFromFreqListToFreqArray](#) (outputFrequency\_t frequencies[], validFreq\_t validFrequencies)  
 Convert from a frequency list to frequency array.
- void [IDTHIApi\\_ApplyFrequencies](#) (const outputFrequency\_t \*frequencies, validFreq\_t validFrequencies, int value)  
 Function to set status of frequency in frequency array.
- int [IDTHIApi\\_IsFreqArrayInFreqList](#) (const outputFrequency\_t frequencies[], validFreq\_t validFrequencies)  
 Function to compare group of frequencies with used frequency list.
- int [IDTHIApi\\_IsFrequencyInFreqList](#) (outputFrequency\_t frequency, const outputFrequency\_t validFrequencies[])  
 Function to verify that frequency is within frequency list.

**6.30.1 Function Documentation**

6.30.1.1 void [IDTHIApi\\_ApplyFrequencies](#) ( const outputFrequency\_t \* frequencies, validFreq\_t validFrequencies, int value )

Function to set status of frequency in frequency array.

**Parameters**

<i>frequencies</i>	Constant frequency list
<i>validFrequencies</i>	
<i>value</i>	Status to set for frequency array

Definition at line 79 of file outputFreqUtil.c.

6.30.1.2 void IDTHIApi.ConvertFromFreqListToFreqArray ( outputFrequency\_t frequencies[], validFreq\_t validFrequencies )

Convert from a frequency list to frequency array.

Parameters

<i>frequencies</i>	Frequency list to convert
<i>validFrequencies</i>	Output frequency array

Definition at line 57 of file outputFreqUtil.c.

6.30.1.3 int IDTHIApi.IsFreqArrayInFreqList ( const outputFrequency\_t frequencies[], validFreq\_t validFrequencies )

Function to compare group of frequencies with used frequency list.

Parameters

<i>frequencies</i>	List to frequencies to check for
<i>validFrequencies</i>	List of frequencies to check against

Returns

0-Not in frequency list, 1-All in frequency list

Definition at line 100 of file outputFreqUtil.c.

6.30.1.4 int IDTHIApi.IsFrequencyInFreqList ( outputFrequency\_t frequency, const outputFrequency\_t validFrequencies[] )

Function to verify that frequency is within frequency list.

Parameters

<i>frequency</i>	Frequency to check
<i>validFrequencies</i>	Frequency list to check against

Returns

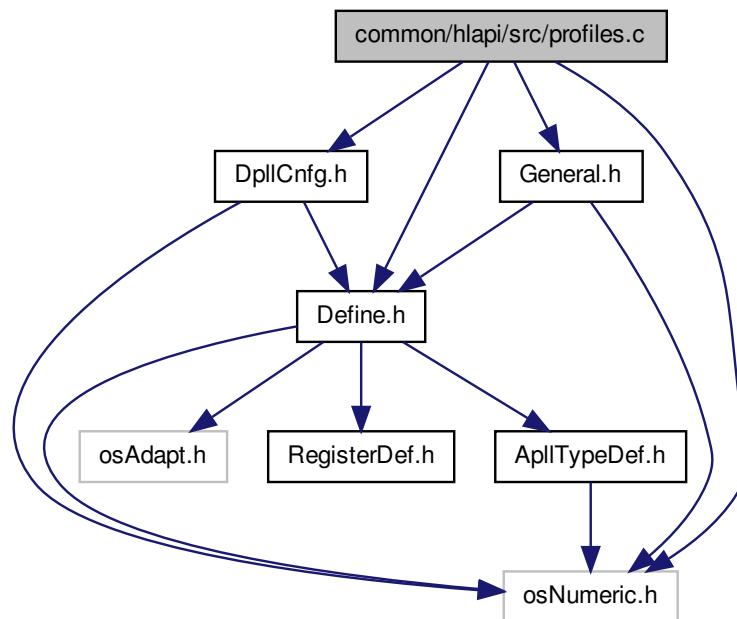
1-Frequency is in list, 0-Frequency is not in list

Definition at line 124 of file outputFreqUtil.c.

## 6.31 common/hlapi/src/profiles.c File Reference

```
#include "Define.h"
#include "osNumeric.h"
#include "DpllCnfg.h"
#include "General.h"
```

Include dependency graph for profiles.c:



## Functions

- void [IDTHIApi\\_gr253SonetStratum3](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
DPLL configuration for GR-253 (SONET) Stratum 3.
- void [IDTHIApi\\_gr1244Stratum3](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
DPLL configuration for GR-1244 Stratum 3.
- void [IDTHIApi\\_smc](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
DPLL configuration for SMC.
- void [IDTHIApi\\_g8262EecOption1](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
DPLL configuration for G-8262 Option 1.
- void [IDTHIApi\\_g8262EecOption2](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
DPLL configuration for G-8262 Option 2.
- void [IDTHIApi\\_g813Option1](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
DPLL configuration for G-813 Option 1.
- void [IDTHIApi\\_g813Option2](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
DPLL configuration for G-813 Option 2.
- void [IDTHIApi\\_pps](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
DPLL configuration for 1 pulse per second (PPS)
- void [IDTHIApi\\_wideband](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
DPLL configuration for wideband.

### 6.31.1 Detailed Description

This sample file contains DPLL configurations used to conform to various standards.

Definition in file [profiles.c](#).

## 6.31.2 Function Documentation

### 6.31.2.1 void IDTHIApi\_g813Option1 ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

DPLL configuration for G-813 Option 1.

#### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

Definition at line 396 of file profiles.c.

### 6.31.2.2 void IDTHIApi\_g813Option2 ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

DPLL configuration for G-813 Option 2.

#### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

Definition at line 408 of file profiles.c.

### 6.31.2.3 void IDTHIApi\_g8262EecOption1 ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

DPLL configuration for G-8262 Option 1.

#### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

Definition at line 258 of file profiles.c.

### 6.31.2.4 void IDTHIApi\_g8262EecOption2 ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

DPLL configuration for G-8262 Option 2.

#### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

Definition at line 327 of file profiles.c.

### 6.31.2.5 void IDTHIApi\_gr1244Stratum3 ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

DPLL configuration for GR-1244 Stratum 3.

#### Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

Definition at line 120 of file profiles.c.

6.31.2.6 void IDTHIApi\_gr253SonetStratum3 ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

DPLL configuration for GR-253 (SONET) Stratum 3.

Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

Definition at line 51 of file profiles.c.

6.31.2.7 void IDTHIApi\_pps ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

DPLL configuration for 1 pulse per second (PPS)

Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

Definition at line 421 of file profiles.c.

6.31.2.8 void IDTHIApi\_smc ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

DPLL configuration for SMC.

Parameters

<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

Definition at line 189 of file profiles.c.

6.31.2.9 void IDTHIApi\_wideband ( T\_idtDrvHdlr *hdlr*, T\_idtDpllInstance *nDpll* )

DPLL configuration for wideband.

Parameters

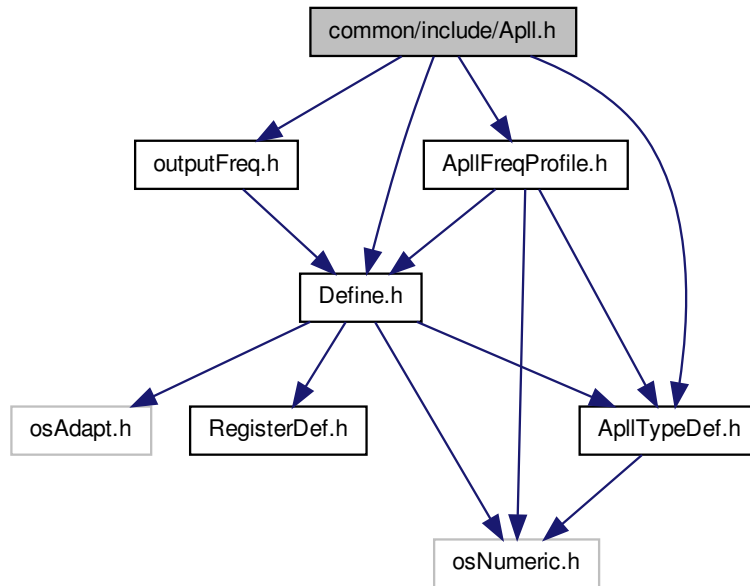
<i>hdlr</i>	Device driver handler
<i>nDpll</i>	DPLL instance

Definition at line 523 of file profiles.c.

## 6.32 common/include/Apll.h File Reference

```
#include "Define.h"
#include "outputFreq.h"
#include "ApllTypeDef.h"
#include "ApllFreqProfile.h"
```

Include dependency graph for ApI.h:



## Data Structures

- struct [T\\_idtApIConfigPerOutput](#)  
*Structure containing APLL per output configuration.*
- struct [T\\_idtApIConfig](#)  
*Structure containing APLL full configuration.*
- struct [T\\_idtApIConfig::preDiv\\_s](#)
- struct [T\\_idtApIConfig::fbDiv\\_s](#)
- struct [T\\_idtApIConfig::outputDiv\\_s](#)
- struct [T\\_idtApIConfig::outputDiv\\_s::qaDiv\\_s](#)
- struct [T\\_idtApIConfig::outputDiv\\_s::qbDiv\\_s](#)
- struct [T\\_idtApIConfig::outputConfig\\_s](#)
- struct [T\\_idtApIConfig::outputConfig\\_s::qaConfig\\_s](#)
- struct [T\\_idtApIConfig::outputConfig\\_s::qbConfig\\_s](#)

## Macros

- #define [IDT\\_GET\\_OUTPUT\\_APLL\\_CONFIG](#)(hdlr, output, outputApI)  
*Utility macro to translate output port to APLL instance.*

## Functions

- void [IDTApI\\_SetApIConfigPerOutput](#) (T\_idtDrvHdlr hdlr, T\_idtApIIId apIIId, T\_idtApIOutput output, T\_idtApIConfigPerOutput \*apIConfigPerOutput)  
*Set APLL per output configuration.*

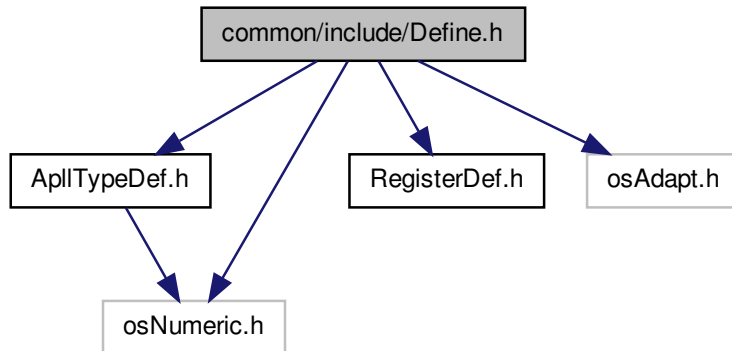


- void [IDTApl\\_GetApllConfigPerOutput](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllId, T\_idtApllOutput output, T\_idtApllConfigPerOutput \*apllConfigPerOutput)  
*Get APLL per output configuration.*
- void [IDTApl\\_SetApllConfig](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllId, T\_idtApllConfig \*apllConfig)  
*Set APLL full configuration.*
- void [IDTApl\\_GetApllConfig](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllId, T\_idtApllConfig \*apllConfig)  
*Get APLL full configuration.*
- [outputFrequency\\_t IDTApl\\_ApllInput2DpllOutput](#) (T\_idtApllInputFreqType apllInputFreq)  
*Translate APLL input frequency to DPLL output frequency.*
- [T\\_idtApllOutputFreqType IDTApl\\_DpllOutput2ApllOutput](#) (outputFrequency\_t dpllOutput)  
*Translate DPLL output frequency to APLL output frequency.*
- const [T\\_idtApllFreqMapping \\* IDTApl\\_GetApllFreqTableEntry](#) (T\_idtDrvHdlr hdlr, T\_idtOutputApllConfig outputApll, outputFrequency\_t nOutFreq)  
*Get APLL frequency configuration table entry based on the output frequency.*
- [T\\_idtApllConfigSel IDTApl\\_GetNonActiveApllConfig](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllId)  
*Get non-active APLL configuration.*
- void [IDTApl\\_Switch2NonActiveApllConfig](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllId)  
*Switch to non-active APLL configuration.*
- [T\\_idtApllXtalId IDTApl\\_GetXtalIdFromXtalFreq](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllId, T\_idtApllXtalType apllVcxoFreq)  
*Get APLL configured crystal ID from crystal frequency.*
- T\_osBool [IDTApl\\_XtalConfigured](#) (T\_idtDrvHdlr hdlr, T\_idtApllId apllId)  
*Checks if there is any XTAL configured for the APLL.*
- T\_osBool [IDTApl\\_ValidXtalInput](#) (const T\_idtDrvDeviceConfig \*deviceConfig, T\_idtApllXtal \*xtalList, T\_osUInt8 numberOfXtal)  
*Checks if there is input XTAL information is valid for the device.*
- [T\\_idtApllXtal \\* IDTApl\\_GetSupportedXtal](#) (const T\_idtDrvDeviceConfig \*deviceConfig, T\_osUInt8 \*numberOfXtal)  
*Return supported xtal configuration by the device.*

## 6.33 common/include/Define.h File Reference

```
#include "ApllTypeDef.h"
#include "RegisterDef.h"
#include "osAdapt.h"
#include "osNumeric.h"
```

Include dependency graph for Define.h:



## Data Structures

- struct [T\\_idtDrvAccess](#)  
*Initialization structure detailing device access information for device driver.*
- struct [T\\_idtOutputApplConfig](#)  
*Structure containing APLL information.*
- struct [T\\_idtDrvDeviceConfig](#)  
*Device type/variant information.*
- struct [T\\_idtDrvHdlr](#)  
*Device driver handler.*

## Macros

- #define [MPU\\_I2C\\_MODE](#) 0x00
- #define [MPU\\_SERIAL\\_MODE](#) 0x01
- #define [NULL\\_APLL\\_CONFIG](#)  
*Utility macro to set APLL configuration to NULL for the output path that does not have APLL.*
- #define [APLL\\_CONFIGURED](#)(applConfig)  
*Utility macro to check if APLL is configured.*
- #define [IDT\\_DRV\\_MAX\\_INPUT](#) 14  
*Define maximum number of supported inputs.*
- #define [IDT\\_DRV\\_MAX\\_OUTPUT](#) 11  
*Define maximum number of supported outputs.*
- #define [IDT\\_DRV\\_MAX\\_APLL\\_XTAL](#) 4  
*Define maximum number of APLL XTALs per device.*
- #define [IDT\\_DRV\\_MAX\\_XTAL\\_PER\\_APLL](#) 2  
*Define maximum number of XTALs per APLL.*

## Typedefs

- typedef T\_osUInt8(\* [T\\_idtReadFunc](#) )(void \*usrData, T\_osUInt8 deviceAddr, T\_osUInt8 addrOff)  
*Function type for reading from i2c device.*
- typedef void(\* [T\\_idtWriteFunc](#) )(void \*usrData, T\_osUInt8 deviceAddr, T\_osUInt8 addrOff, T\_osUInt8 data)  
*Function type for writing to i2c device.*
- typedef void(\* [T\\_idtAccessInitFunc](#) )(void \*userData)  
*Function type to initialize device access.*
- typedef void(\* [T\\_idtAccessDeInitFunc](#) )(void \*userData)  
*Function type to deinitialize device access.*
- typedef T\_osUInt8(\* [T\\_idtI2CAddrTransFunc](#) )(T\_osUInt8 i2cAddr, void \*transData)  
*Function type to translate i2c address used internally by the driver.*
- typedef T\_osBool(\* [T\\_idtInputFreqValid](#) )(T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo, T\_osUInt32 nFrequency, void \*auxData)  
*Function type to sanity check the input frequency.*
- typedef T\_osBool(\* [T\\_idtOutputFreqValid](#) )(T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN, T\_osUInt32 nOutFreq, void \*auxData)  
*Function type to sanity check the output frequency.*

## Enumerations

- enum [T\\_idtDpllType](#) { [Dpll\\_T0](#) = 0, [Dpll\\_T4](#) = 1, [Dpll\\_MAX](#) }  
*Enumerated type for selecting DPLLs (T0 or T4)*
- enum [T\\_idtDeviceType](#) {  
[IDT\\_82V3910](#), [IDT\\_82V3911](#), [IDT\\_82V33930](#), [IDT\\_8V89316](#),  
[IDT\\_8V89317](#), [IDT\\_DEVICE\\_MAX](#) }  
*Enumerated type listing supported device(s)*
- enum [T\\_idtDpllInstance](#) { [DPLL\\_INSTANCE\\_1](#), [DPLL\\_INSTANCE\\_2](#), [DPLL\\_INSTANCE\\_MAX](#) }  
*Define maximum number of supported DPLLs.*

### 6.33.1 Macro Definition Documentation

#### 6.33.1.1 #define APLL\_CONFIGURED( *apllConfig* )

##### Value:

```
((apllConfig.apllInst != APLL\_INST\_MAX) && \
 (apllConfig.apllInput) && \
 (apllConfig.apllOutput != APLL\_OUTPUT\_MAX) && \
 (apllConfig.extOutput)) \
? 1 : 0
```

Utility macro to check if APLL is configured.

##### Parameters

<i>apllConfig</i>	APLL configuration
-------------------	--------------------

Definition at line 81 of file Define.h.

#### 6.33.1.2 #define IDT\_DRV\_MAX\_APLL\_XTAL 4

Define maximum number of APLL XTALs per device.

Definition at line 110 of file Define.h.

**6.33.1.3 #define IDT\_DRV\_MAX\_INPUT 14**

Define maximum number of supported inputs.

Definition at line 104 of file Define.h.

**6.33.1.4 #define IDT\_DRV\_MAX\_OUTPUT 11**

Define maximum number of supported outputs.

Definition at line 107 of file Define.h.

**6.33.1.5 #define IDT\_DRV\_MAX\_XTAL\_PER\_APLL 2**

Define maximum number of XTALs per APLL.

Definition at line 113 of file Define.h.

**6.33.1.6 #define MPU\_I2C\_MODE 0x00**

Definition at line 62 of file Define.h.

**6.33.1.7 #define MPU\_SERIAL\_MODE 0x01**

Definition at line 63 of file Define.h.

**6.33.1.8 #define NULL\_APLL\_CONFIG****Value:**

```
{
    APLL_INST_MAX,    //
    0,                //
    APLL_OUTPUT_MAX, //
    0,                //
}
```

Utility macro to set APLL configuration to NULL for the output path that does not have APLL.

Definition at line 69 of file Define.h.

**6.33.2 Typedef Documentation****6.33.2.1 typedef void(\* T\_idtAccessDeInitFunc)(void \*userData)**

Function type to deinitialize device access.

Optional binding for device access

**Parameters**

<i>userData</i>	optional user data passed to deinitialization function
-----------------	--

Definition at line 156 of file Define.h.

## 6.33.2.2 typedef void(\* T\_idtAccessInitFunc)(void \*userData)

Function type to initialize device access.

Optional binding for device access

## Parameters

<i>userData</i>	optional user data passed to initialization function
-----------------	--

Definition at line 147 of file Define.h.

## 6.33.2.3 typedef T\_osUInt8(\* T\_idtl2CaddrTransFunc)(T\_osUInt8 i2cAddr, void \*transData)

Function type to translate i2c address used internally by the driver.

## Parameters

<i>i2cAddr</i>	7-bit unshifted i2c slave address for the WAN PLL
<i>transData</i>	Helper data for translating

## Returns

Translated i2c address used internally by the device driver

Definition at line 164 of file Define.h.

## 6.33.2.4 typedef T\_osBool(\* T\_idtlInputFreqValid)(T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo, T\_osUInt32 nFrequency, void \*auxData)

Function type to sanity check the input frequency.

## Parameters

<i>hdlr</i>	driver handler
<i>nInputNo</i>	input port number
<i>nFrequency</i>	input frequency (in Hz)
<i>auxData</i>	auxiliary data (optional)

## Returns

E\_osTrue - nFrequency is supported, E\_osFalse - nFrequency is not supported

Definition at line 175 of file Define.h.

## 6.33.2.5 typedef T\_osBool(\* T\_idtOuputFreqValid)(T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN, T\_osUInt32 nOutFreq, void \*auxData)

Function type to sanity check the output frequency.

## Parameters

<i>hdlr</i>	driver handler
<i>nOutN</i>	output port number
<i>nOutFreq</i>	Output frequency /see outputFrequency_t for list of supported frequencies
<i>auxData</i>	auxiliary data (optional)

**Returns**

E\_osTrue - nOutFreq is supported, E\_osFalse - nOutFreq is not supported

Definition at line 187 of file Define.h.

### 6.33.2.6 typedef T\_osUInt8(\* T\_idtReadFunc)(void \*usrData, T\_osUInt8 deviceAddr, T\_osUInt8 addrOff)

Function type for reading from i2c device.

**Parameters**

<i>usrData</i>	optional data passed to write function
<i>deviceAddr</i>	device address for bus that requires slave address (e.g. i2c)
<i>addrOff</i>	address offset

**Returns**

read data

Definition at line 129 of file Define.h.

### 6.33.2.7 typedef void(\* T\_idtWriteFunc)(void \*usrData, T\_osUInt8 deviceAddr, T\_osUInt8 addrOff, T\_osUInt8 data)

Function type to writing to i2c device.

**Parameters**

<i>usrData</i>	optional user data passed to read function
<i>deviceAddr</i>	for bus that requires slave address (e.g. i2c)
<i>addrOff</i>	address offset
<i>data</i>	data to write

Definition at line 138 of file Define.h.

## 6.33.3 Enumeration Type Documentation

### 6.33.3.1 enum T\_idtDeviceType

Enumerated type listing supported device(s)

**Enumerator**

**IDT\_82V3910** 82V3910  
**IDT\_82V3911** 82V3911  
**IDT\_82V33930** 82V33930  
**IDT\_8V89316** 8V89316  
**IDT\_8V89317** 8V89317  
**IDT\_DEVICE\_MAX**

Definition at line 93 of file Define.h.

### 6.33.3.2 enum T\_idtDpllInstance

Define maximum number of supported DPLLs.

## Enumerator

**DPLL\_INSTANCE\_1** DPLL instance #1  
**DPLL\_INSTANCE\_2** DPLL instance #2  
**DPLL\_INSTANCE\_MAX**

Definition at line 116 of file Define.h.

## 6.33.3.3 enum T\_idtDpllType

Enumerated type for selecting DPLLs (T0 or T4)

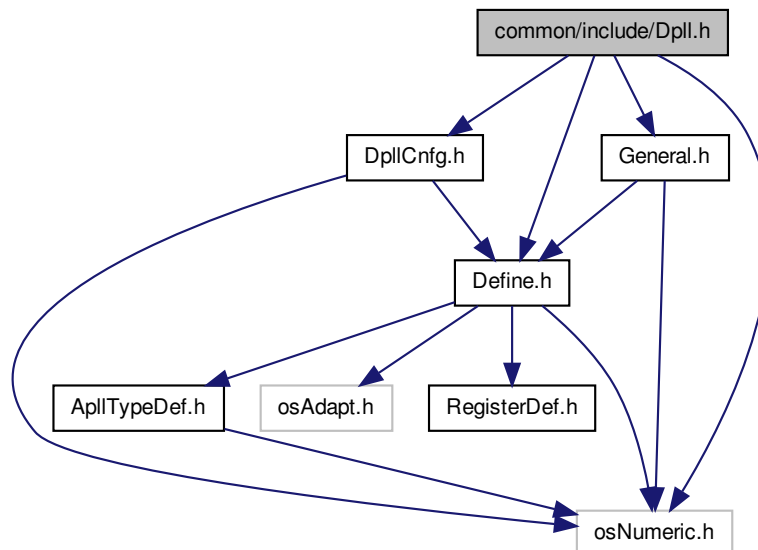
## Enumerator

**Dpll\_T0** Select T0 DPLL  
**Dpll\_T4** Select T4 DPLL  
**Dpll\_MAX**

Definition at line 53 of file Define.h.

## 6.34 common/include/Dpll.h File Reference

```
#include "osNumeric.h"
#include "Define.h"
#include "DpllCnfg.h"
#include "General.h"
Include dependency graph for Dpll.h:
```



## Data Structures

- struct [T\\_IDTPathConfiguration](#)

*Structure containing output path configuration.*

## Macros

- `#define SonetGigEthSel_NUMMAX 2`

*Constant defining number of instances of SonetGigEth selectors.*

## Enumerations

- enum `T_idtT0DpllSelectorA` {  
`T0DpllSelA_16E1, T0DpllSelA_16T1, T0DpllSelA_GSM, T0DpllSelA_OBSAI,`  
`T0DpllSelA_MAX` }

*Enumerated type listing T0 DPLL selector A options.*

- enum `T_idtT0DpllSelectorB` {  
`T0DpllSelB_12E1, T0DpllSelB_GPS, T0DpllSelB_E3, T0DpllSelB_T3,`  
`T0DpllSelB_MAX` }

*Enumerated type listing T0 DPLL selector B options.*

- enum `T_idtT4DpllSelectorA` {  
`T4DpllSelA_16E1, T4DpllSelA_16T1, T4DpllSelA_GSM, T4DpllSelA_GPS,`  
`T4DpllSelA_MAX` }

*Enumerated type listing T4 DPLL selector A options.*

- enum `T_idtT4DpllSelectorB` {  
`T4DpllSelB_12E1, T4DpllSelB_24T1, T4DpllSelB_E3, T4DpllSelB_T3,`  
`T4DpllSelB_MAX` }

*Enumerated type listing T4 DPLL selector B options.*

- enum `T_idtSonetGigEthSelector` {  
`SonetGigEthSel_T0DpllSonet = 0, SonetGigEthSel_T4DpllSonet = 4, SonetGigEthSel_T0Dpll10GbE = 8,`  
`SonetGigEthSel_T0Dpll10GbE_6664 = 9,`  
`SonetGigEthSel_T4Dpll10GbE = 12, SonetGigEthSel_T4Dpll10GbE_6664 = 13, SonetGigEthSel_MAX` }

*Enumerated type listing Sonet/GigE path selection options.*

## Variables

- const `T_IDTPathConfiguration IDTDpll_pathConfigurationNULL_c`

*Output path configuration no path constant.*

- const `T_idtSonetGigEthSelector IDTDpll_sonetGigEthPathConfig2Bitfield [Dpll_MAX][SonetGigEthOutput_MAX]`

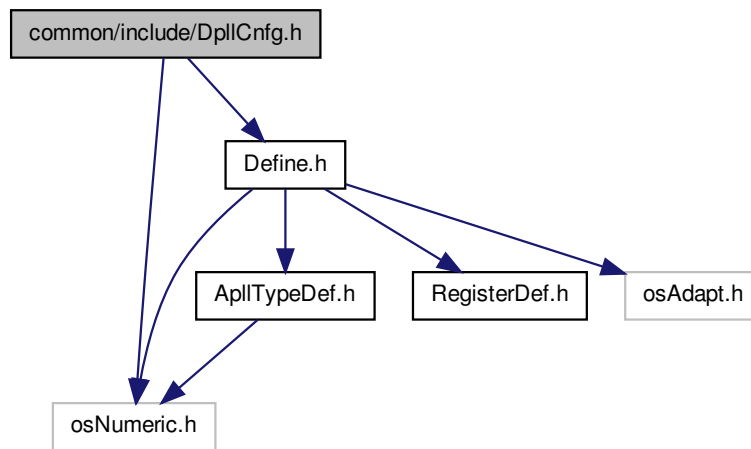
*Table to translate from Sonet/GigE path configuration to bitfield value.*

## 6.35 common/include/DpllCnfg.h File Reference

```
#include "osNumeric.h"
#include "Define.h"
```



Include dependency graph for DpllCnfg.h:



## Macros

- `#define DCO_PPT2DCOUNTS 11`  
*Conversion from parts per trillion to register unit value for DCO offset.*
- `#define DCO_MAX_PPT 92274677`  
*Max DCO value.*
- `#define DCO_MIN_PPT -92274688`  
*Max DCO value.*
- `#define IDT_TRANSLATE_EXT_TO_INT_DPLL(hdlr, ext, internal)`  
*Utility macro to check if DPLL instance is supported and to translated from DPLL instance to DPLL type.*

## Enumerations

- `enum T_idtFreqMonFactor {`  
`FreqMonFactor_0p0032 = 0, FreqMonFactor_0p0064 = 1, FreqMonFactor_0p0127 = 2, FreqMonFactor_0p0257 = 3,`  
`FreqMonFactor_0p0514 = 4, FreqMonFactor_0p1030 = 5, FreqMonFactor_0p2060 = 6, FreqMonFactor_0p4120 = 7,`  
`FreqMonFactor_0p8230 = 8, FreqMonFactor_1p6460 = 9, FreqMonFactor_3p2920 = 10, FreqMonFactor_3p8100 = 11,`  
`FreqMonFactor_4p6000 = 12, FreqMonFactor_MAX }`  
*Enumerated list indicating frequency monitoring factor.*
- `enum T_idtBandwidthLimitStage { dpllBandwidthLimitStart, dpllBandwidthLimitAcquire, dpllBandwidthLimitLocked, dpllBandwidthLimit_MAX }`  
*Enumerated list used for selecting bandwidth limiting stages.*
- `enum T_idtDampingFactor {`  
`DampingFactor_1p2 = 1, DampingFactor_2p5 = 2, DampingFactor_5 = 3, DampingFactor_10 = 4,`  
`DampingFactor_20 = 5, DampingFactor_MAX }`  
*Enumerated list showing options for bandwidth damping factor.*

- enum `T_idtDpllBandwidth` {  
`dpllBandwidth_0p5mHz = 0, dpllBandwidth_1mHz = 1, dpllBandwidth_2mHz = 2, dpllBandwidth_4mHz = 3,`  
`dpllBandwidth_8mHz = 4, dpllBandwidth_15mHz = 5, dpllBandwidth_30mHz = 6, dpllBandwidth_60mHz = 7,`  
`dpllBandwidth_0p1Hz = 8, dpllBandwidth_0p3Hz = 9, dpllBandwidth_0p6Hz = 10, dpllBandwidth_1p2Hz =`  
`11,`  
`dpllBandwidth_2p5Hz = 12, dpllBandwidth_4Hz = 13, dpllBandwidth_8Hz = 14, dpllBandwidth_18Hz = 15,`  
`dpllBandwidth_35Hz = 16, dpllBandwidth_70Hz = 17, dpllBandwidth_560Hz = 18, dpllBandwidth_MAX }`  
*List of options for DPLL bandwidth.*
- enum `T_idtPhaseSlope` {  
`phaseSlope_gr1244st3 = 0, phaseSlope_gr1244st3e = 1, phaseSlope_gr813 = 2, phaseSlope_noLimit = 3,`  
`phaseSlope_MAX }`  
*Enumerated type listing phase slope.*
- enum `T_idtDpllOperMode` {  
`Automatic_Mode = 0, Force_FreeRun_Mode = 1, Force_Holdover_Mode = 2, Force_Locked_Mode = 4,`  
`Force_Pre_Locked2_Mode = 5, Force_Pre_Locked_Mode = 6, Force_Lost_Phase_Mode = 7, Dco_Mode =`  
`8,`  
`DpllOperMode_MAX }`  
*Enumerated type for DPLL operation mode.*
- enum `T_idtCoarsePhaseLimit` {  
`coarsePhaseLimit_1 = 0, coarsePhaseLimit_3 = 1, coarsePhaseLimit_7 = 2, coarsePhaseLimit_15 = 3,`  
`coarsePhaseLimit_31 = 4, coarsePhaseLimit_63 = 5, coarsePhaseLimit_127 = 6, coarsePhaseLimit_255 =`  
`7,`  
`coarsePhaseLimit_511 = 8, coarsePhaseLimit_1023 = 9, coarsePhaseLimit_MAX }`  
*Enumerated type listing coarse phase limits.*
- enum `T_idtFinePhaseLimit` {  
`finePhaseLimit_45_90degree = 1, finePhaseLimit_90_180degree = 2, finePhaseLimit_180_360degree = 3,`  
`finePhaseLimit_20_25nanosec = 4,`  
`finePhaseLimit_60_65nanosec = 5, finePhaseLimit_120_125nanosec = 6, finePhaseLimit_950_955nanosec`  
`= 7, finePhaseLimit_MAX }`  
*Enumerated type listing fine phase limits.*
- enum `T_idtDpllHoldover` {  
`Holdover_Instantaneous = 0, Holdover_Slow_Average = 2, Holdover_Fast_Average = 3, Holdover_Manual =`  
`4,`  
`Holdover_MAX }`  
*Enumerated type listing holdover modes.*
- enum `T_idtTemp_holdover` {  
`Temp_Same_As_Full_Holdover = 0, Temp_Holdover_Instantaneous = 1, Temp_Holdover_Fast_Average = 2,`  
`Temp_Holdover_Slow_Average = 3,`  
`Temp_Holdover_MAX }`  
*Enumerated type listing temp-holdover modes.*
- enum `T_idtOperDpllMode` {  
`OperDpllMode_FreeRun = 1, OperDpllMode_HoldOver = 2, OperDpllMode_Locked = 4, OperDpllMode_Pre-`  
`Locked2 = 5,`  
`OperDpllMode_PreLocked = 6, OperDpllMode_LostPhase = 7 }`  
*Enumerated type listing DPLL operational modes.*
- enum `T_idtSonetGigEthOutput` { `SonetGigEthOutput_Sonet, SonetGigEthOutput_10GbE, SonetGigEth-`  
`Output_10GbE_6664, SonetGigEthOutput_MAX }`  
*Enumerated type listing possible Sonet/GigE output frequencies.*
- enum `T_idtDpllOutputSelectorA` {  
`DPLLOutputSelA_16E1, DPLLOutputSelA_16T1, DPLLOutputSelA_GSM, DPLLOutputSelA_OBSAI,`  
`DPLLOutputSelA_GPS, DPLLOutputSelA_MAX }`  
*Enumerated type listing DPLL selector A paths.*
- enum `T_idtDpllOutputSelectorB` {  
`DPLLOutputSelB_12E1, DPLLOutputSelB_GPS, DPLLOutputSelB_E3, DPLLOutputSelB_T3,`  
`DPLLOutputSelB_24T1, DPLLOutputSelB_MAX }`

*Enumerated type listing DPLL selector B paths.*

- enum `T_idtDpllPpsPhasePostion` { `PpsPhasePostion_0degree`, `PpsPhasePostion_50ns`, `PpsPhasePostion_100ns`, `PpsPhasePostion_MAX` }

*Enumerated type listing PPS phase options.*

- enum `T_idtDpllPpsPulseWidth` { `PpsPulseWidth_0pt5sec`, `PpsPulseWidth_10ns`, `PpsPulseWidth_200ns`, `PpsPulseWidth_400ns`, `PpsPulseWidth_800ns`, `PpsPulseWidth_1us`, `PpsPulseWidth_20us`, `PpsPulseWidth_50us`, `PpsPulseWidth_100us`, `PpsPulseWidth_200us`, `PpsPulseWidth_1pt2ms`, `PpsPulseWidth_800us`, `PpsPulseWidth_MAX` }

*Enumerated type listing PPS pulse width.*

## Functions

- `T_idtDpllType` `IDTDpll_GetTypeOfDpll` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)  
*Function to determine type of DPLL give a DPLL instance.*
- void `IDTDpll_SetAutoSelInput` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_osUInt8` mode)  
*Set the DPLL as automatic reference clock selection.*
- `T_osUInt8` `IDTDpll_GetAutoSelInput` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)  
*Get automatic input selection status.*
- void `IDTDpll_SetForceSelInput` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_osUInt8` nInputNo)  
*Set the DPLL to force to lock to a specified reference clock.*
- `T_osUInt8` `IDTDpll_GetForceSelInput` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)  
*Set the DPLL to force to lock to a specified reference clock.*
- `T_osUInt8` `IDTDpll_Get1stPriorityInput` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)  
*Get input number of a valid clock with the highest priority.*
- `T_osUInt8` `IDTDpll_Get2ndPriorityInput` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)  
*Get input number of a valid clock with the second highest priority.*
- `T_osUInt8` `IDTDpll_Get3rdPriorityInput` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)  
*Get input number of a valid clock with the third highest priority.*
- `T_osUInt8` `IDTDpll_GetCurrentSelectInput` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)  
*Get the current selected input clock.*
- void `IDTDpll_SetDpllOperMod` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_idtDpllOperMode` nMode)  
*Set DPLL working at the specified operating mode.*
- `T_idtDpllOperMode` `IDTDpll_GetDpllOperMod` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)  
*Set DPLL working at the specified operating mode.*
- `T_osUInt8` `IDTDpll_IsDpllLocked` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)  
*Inquire if the DPLL is in lock state.*
- void `IDTDpll_SetBandWidthDamping` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_idtBandwidthLimitStage` stage, `T_idtDpllBandwidth` nBandWidth, `T_idtDampingFactor` nDamping)  
*Set the bandwidth and damping factor used for bandwidth limiting.*
- void `IDTDpll_GetBandWidthDamping` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_idtBandwidthLimitStage` stage, `T_idtDpllBandwidth` \*nBandWidth\_p, `T_idtDampingFactor` \*nDamping\_p)  
*Get configured bandwidth and damping factor for bandwidth limiting.*
- void `IDTDpll_SetAutoSelBandWidth` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_osUInt8` nEnable)  
*Set device to select a suitable bandwidth and damping factor automatically.*
- `T_osUInt8` `IDTDpll_GetAutoSelBandWidth` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)  
*Get auto bandwidth/damping factor status automatically.*
- void `IDTDpll_SetDpllFrozen` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_osUInt8` nEnable)  
*Set DPLL integral path value frozen.*
- `T_osUInt8` `IDTDpll_GetDpllFrozen` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)  
*Get DPLL integral path value frozen.*

- void `IDTDpll_SetPhaseCoarseDetector` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_osUInt8` nEnable, `T_osUInt8` nWide, `T_osUInt8` nMultiPhase, `T_osUInt8` nMultiPh8kEn)
  - Set the coarse phase lose detector enable.*
- void `IDTDpll_GetPhaseCoarseDetector` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_osUInt8` \*nEnable\_p, `T_osUInt8` \*nWide\_p, `T_osUInt8` \*nMultiPhase\_p, `T_osUInt8` \*nMultiPh8kEn\_p)
  - Set the coarse phase lose detector enable.*
- void `IDTDpll_SetPhaseCoarseLimit` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_idtCoarsePhaseLimit` nLimit)
  - Set the limitation of the coarse phase lose detector.*
- `T_idtCoarsePhaseLimit` `IDTDpll_GetPhaseCoarseLimit` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)
  - Get the limitation of the coarse phase lose detector.*
- void `IDTDpll_SetPhaseFineDetectorEnable` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_osUInt8` nEnable)
  - Set the fine phase lose detector enable.*
- `T_osUInt8` `IDTDpll_GetPhaseFineDetectorEnable` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)
  - Get the fine phase lose detector enable.*
- void `IDTDpll_SetPhaseFineLimit` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_idtFinePhaseLimit` nLimit)
  - Set the limitation of the fine phase lose detector.*
- `T_idtFinePhaseLimit` `IDTDpll_GetPhaseFineLimit` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)
  - Set the limitation of the fine phase lose detector.*
- void `IDTDpll_SetFastLossSwitch` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nEnable)
  - Set reference clock switch if a fast loss occurs.*
- `T_osUInt8` `IDTDpll_GetFastLossSwitch` (`T_idtDrvHdlr` hdlr)
  - Get reference clock switch if a fast loss occurs.*
- void `IDTDpll_SetHoldoverMode` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_idtDpllHoldover` nMode, `T_osUInt8` nReadMode)
  - Set calculation mode of holdover frequency and read back mode.*
- void `IDTDpll_GetHoldoverMode` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_idtDpllHoldover` \*nMode\_p, `T_osUInt8` \*nReadMode\_p)
  - Get calculation mode of holdover frequency and read back mode.*
- void `IDTDpll_SetTempHoldoverMode` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_idtTemp_holdover` nMode)
  - Set calculation mode of temporary holdover frequency.*
- `T_idtTemp_holdover` `IDTDpll_GetTempHoldoverMode` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)
  - Set calculation mode of temporary holdover frequency.*
- long `IDTDpll_GetHoldoverFreq` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)
  - Get holdover frequency offset (in parts per trillion). In DCO mode, this function returns current DCO offset (in parts per trillion).*
- void `IDTDpll_SetHoldoverFreq` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, long pptOffset)
  - Set DCO frequency to device. Note this function should only be called when DCO mode is enabled.*
- long `IDTDpll_GetCurrentDpllFreqOffset` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)
  - Get current frequency offset of DPLL in parts per trillion (PPT)*
- void `IDTDpll_SetDpllSoftAlarmLimit` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_osUInt8` nLimit)
  - Set the limitation of Soft alarm of DPLL.*
- `T_osUInt8` `IDTDpll_GetDpllSoftAlarmLimit` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)
  - Get the limitation of Soft alarm of DPLL.*
- void `IDTDpll_SetDpllHardAlarmLimit` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_osUInt16` nLimit)
  - Set the limitation of Hard alarm of DPLL.*
- `T_osUInt16` `IDTDpll_GetDpllHardAlarmLimit` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)
  - Get the limitation of Hard alarm of DPLL.*
- void `IDTDpll_SetDpllHardAlarmEnable` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nEnable)
  - Set DPLL in unlocked state when a Hard alarm raised.*

- T\_osUInt8 [IDTDpll\\_GetDpllHardAlarmEnable](#) (T\_idtDrvHdlr hdlr)  
*Get DPLL in unlocked state when a Hard alarm raised.*
- T\_osUInt16 [IDTDpll\\_GetCurrentPhaseError](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Get the current phase error of DPLL.*
- void [IDTDpll\\_SetSonetGigEthOutputPath](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 instance, T\_idtDpllInstance inputDpll, T\_idtSonetGigEthOutput outputFreq)  
*Set Sonet/GigE path configuration.*
- void [IDTDpll\\_GetSonetGigEthOutputPath](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 instance, T\_idtDpllInstance \*inputDpll\_p, T\_idtSonetGigEthOutput \*outputFreq\_p)  
*Retrieve Sonet/GigE path configuration.*
- void [IDTDpll\\_SetDpllOutputPathSelectorA](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_idtDpllOutputSelectorA path)  
*Set DPLL output path selector A.*
- T\_idtDpllOutputSelectorA [IDTDpll\\_GetDpllOutputPathSelectorA](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Get DPLL output path selector A.*
- void [IDTDpll\\_SetDpllOutputPathSelectorB](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_idtDpllOutputSelectorB path)  
*Set DPLL output path selector B.*
- T\_idtDpllOutputSelectorB [IDTDpll\\_GetDpllOutputPathSelectorB](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Get DPLL output path selector B.*
- void [IDTDpll\\_SetDpllEthPathEnable](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_osUInt8 nDisable)  
*Set ETH Enable/Disable.*
- T\_osUInt8 [IDTDpll\\_GetDpllEthPathEnable](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Get ETH Enable/Disable.*
- void [IDTDpll\\_SetDpllSelBPathEnable](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_osUInt8 nDisable)  
*Set DPLL output path selector B Enable/Disable.*
- T\_osUInt8 [IDTDpll\\_GetDpllSelBPathEnable](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Get DPLL output path selector B Enable/Disable.*
- void [IDTDpll\\_SetDpll16E116T1Enable](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_osUInt8 nDisable)  
*Set 16E1/16T1 Enable/Disable.*
- T\_osUInt8 [IDTDpll\\_GetDpll16E116T1Enable](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Get 16E1/16T1 Enable/Disable.*
- void [IDTDpll\\_SetDpllSelAPathEnable](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_osUInt8 nDisable)  
*Set DPLL output path selector A Enable/Disable.*
- T\_osUInt8 [IDTDpll\\_GetDpllSelAPathEnable](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Set DPLL output path selector A Enable/Disable.*
- void [IDTDpll\\_SetFrequencyMonitoringFactor](#) (T\_idtDrvHdlr hdlr, T\_idtFreqMonFactor freqMonFactor)  
*Function to set the frequency monitoring factor. Hard and soft alarm thresholds use this factor as their base unit.*
- T\_idtFreqMonFactor [IDTDpll\\_GetFrequencyMonitoringFactor](#) (T\_idtDrvHdlr hdlr)  
*Function to get the frequency monitoring factor. Hard and soft alarm thresholds use this factor as their base unit.*
- void [IDTDpll\\_SetHardAlarmThreshold](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 accepting, T\_osUInt8 rejecting)  
*Set the frequency hard alarm accepting thresholds of reference clock monitoring.*
- void [IDTDpll\\_GetHardAlarmThreshold](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 \*accepting\_p, T\_osUInt8 \*rejecting\_p)  
*Get the frequency hard alarm accepting thresholds of reference clock monitoring.*
- void [IDTDpll\\_SetSoftAlarmThreshold](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 accepting, T\_osUInt8 rejecting)  
*Set the frequency soft alarm accepting thresholds of reference clock monitoring.*
- void [IDTDpll\\_GetSoftAlarmThreshold](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 \*accepting\_p, T\_osUInt8 \*rejecting\_p)  
*Get the frequency soft alarm accepting thresholds of reference clock monitoring.*
- void [IDTDpll\\_SetIcpCtrl](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_osUInt8 nIcp)

*Set charge pump control.*

- T\_osUInt8 [IDTDpll\\_GetIcpCtrl](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)

*Get charge pump control.*

- void [IDTDpll\\_SetPhaseSlope](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_idtPhaseSlope nPhaseSlope)

*Set DPLL phase slope for DPLLs.*

- T\_idtPhaseSlope [IDTDpll\\_GetPhaseSlope](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)

*Get DPLL phase slope for DPLLs.*

- void [IDTDpll\\_SetPpsFastLock](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nEnableFreq, T\_osUInt8 nEnablePhase)

*Enable/Disable 1 PPS fast lock.*

- void [IDTDpll\\_GetPpsFastLock](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 \*nEnableFreq\_p, T\_osUInt8 \*nEnablePhase\_p)

*Get enable/disable 1 PPS fast lock status.*

- void [IDTDpll\\_SetPhaseTransient](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nEnable)

*Set the configuration when phase transient occurs.*

- T\_osUInt8 [IDTDpll\\_GetPhaseTransient](#) (T\_idtDrvHdlr hdlr)

*Get the configuration when phase transient occurs.*

- void [IDTDpll\\_SetHitlessSwitchingFeature](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nEnable, T\_osUInt8 nFrozen)

*Set the configuration of hitless switching feature.*

- void [IDTDpll\\_GetHitlessSwitchingFeature](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 \*nEnable\_p, T\_osUInt8 \*nFrozen\_p)

*Get the configuration of hitless switching feature.*

- void [IDTDpll\\_SetPhaseOffset](#) (T\_idtDrvHdlr hdlr, T\_osUInt16 nOffset)

*Set the phase offset value.*

- T\_osUInt16 [IDTDpll\\_GetPhaseOffset](#) (T\_idtDrvHdlr hdlr)

*Get the phase offset value.*

- void [IDTDpll\\_SetPpsPhase](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_idtDpllPpsPhasePostion nPhase, T\_idtDpllPpsPulseWidth nPulse)

*Set PPS phase and pulse for DPLL.*

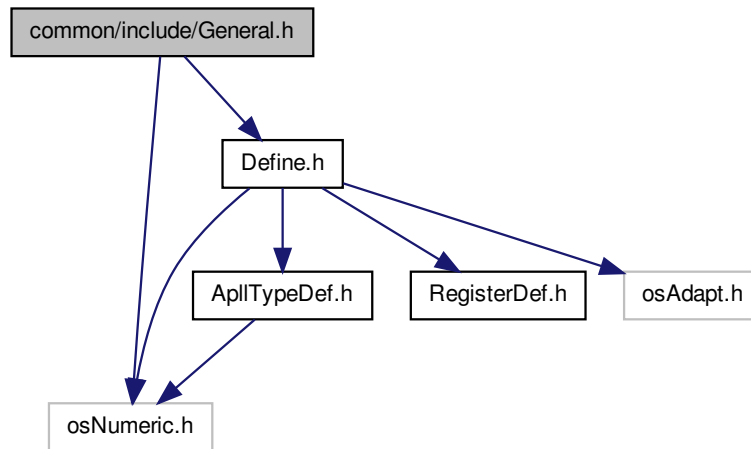
- void [IDTDpll\\_GetPpsPhase](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_idtDpllPpsPhasePostion \*nPhase\_p, T\_idtDpllPpsPulseWidth \*nPulse\_p)

*Get PPS phase and pulse for DPLL.*

## 6.36 common/include/General.h File Reference

```
#include "osNumeric.h"
#include "Define.h"
```

Include dependency graph for General.h:



## Data Structures

- struct [T\\_idtl2CtransData](#)  
*I2C address translation information used internally by the driver.*

## Macros

- `#define Activate_Edge_Rising 0`
- `#define Activate_Edge_Falling 1`
- `#define INT_Active_Low 0`
- `#define INT_Active_High 1`
- `#define NOMINAL_PPT_TO_2COMPL(ppt) (T_osUint32)(((ppt)*10)/884)`  
*Conversion from parts per trillion to register unit value for nominal (oscillator) offset.*
- `#define NOMINAL_2COMPL_TO_PPT(twoCompl) (long)((((twoCompl)*884)/10)`  
*Conversion from parts per trillion to register unit value for nominal (oscillator) offset.*
- `#define NOMINAL_MAX_PPT 94893`  
*Maximum oscillator offset value.*
- `#define NOMINAL_MIN_PPT -94893`  
*Minimum oscillator offset value.*

## Enumerations

- enum `networkType_t` { `Network_SDH = 0`, `Network_SONET = 1`, `Network_MAX` }  
*Enumerated type listing types of selectable network type.*
- enum `phaseTimeoutMultiplier_t` { `phaseTimeoutMultiplier_2 = 0`, `phaseTimeoutMultiplier_4 = 1`, `phaseTimeoutMultiplier_8 = 2`, `phaseTimeoutMultiplier_16 = 3`, `phaseTimeoutMultiplier_MAX` }  
*Enumerated type listing phase alarm timeout multipliers.*

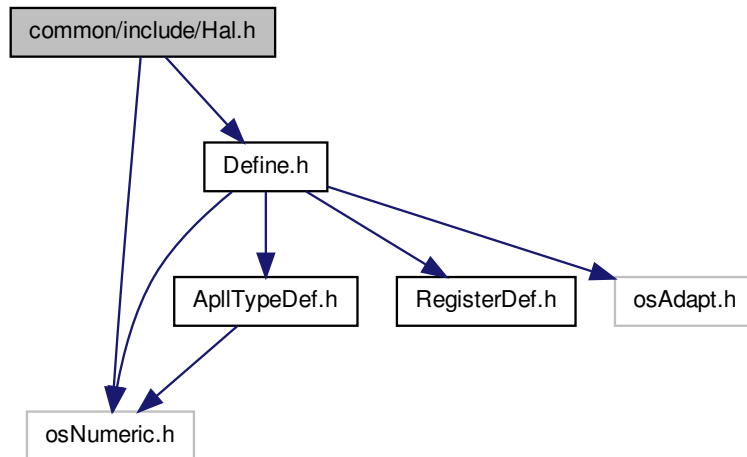
## Functions

- T\_osUInt16 [IDTGeneral\\_GetDeviceID](#) (T\_idtDrvHdlr hdlr)  
*Get ID number of the device.*
- void [IDTGeneral\\_SetOscFreqOffset](#) (T\_idtDrvHdlr hdlr, long pptOffset)  
*Set compensation to the oscillator offset.*
- long [IDTGeneral\\_GetOscFreqOffset](#) (T\_idtDrvHdlr hdlr)  
*Get compensated oscillator offset.*
- void [IDTGeneral\\_SetNetworkType](#) (T\_idtDrvHdlr hdlr, [networkType\\_t](#) nType)  
*Set the network type, SDH or SONET.*
- [networkType\\_t](#) [IDTGeneral\\_GetNetworkType](#) (T\_idtDrvHdlr hdlr)  
*Get the network type, SDH or SONET.*
- void [IDTGeneral\\_SetRevertiveMode](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nEnable)  
*Set the device running in Revertive mode or not.*
- T\_osUInt8 [IDTGeneral\\_GetRevertiveMode](#) (T\_idtDrvHdlr hdlr)  
*Get the device running in Revertive mode or not.*
- void [IDTGeneral\\_SetTimeoutValue](#) (T\_idtDrvHdlr hdlr, [phaseTimeoutMultiplier\\_t](#) nMultiFactor, T\_osUInt8 nTimeout)  
*Set the value of time out of phase alarm  $Timeout(second) = nMultiFactor * nTimeout$ .*
- void [IDTGeneral\\_GetTimeoutValue](#) (T\_idtDrvHdlr hdlr, [phaseTimeoutMultiplier\\_t](#) \*nMultiFactor\_p, T\_osUInt8 \*nTimeout\_p)  
*Get the value of time out of phase alarm  $Timeout(second) = nMultiFactor * nTimeout$ .*
- void [IDTGeneral\\_SetOscActiveEdge](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nEdge)  
*Set the activate edge of main oscillator.*
- T\_osUInt8 [IDTGeneral\\_GetOscActiveEdge](#) (T\_idtDrvHdlr hdlr)  
*Get the activate edge of main oscillator.*
- void [IDTGeneral\\_SetProtectMode](#) (T\_idtDrvHdlr hdlr)  
*Enable protected register access mode.*
- void [IDTGeneral\\_SetSingleUnprotectMode](#) (T\_idtDrvHdlr hdlr)  
*Set single access register access mode.*
- void [IDTGeneral\\_SetFullyUnprotectMode](#) (T\_idtDrvHdlr hdlr)  
*Set fully un-protected register access mode.*
- void [IDTGeneral\\_SetFlagOnTDO](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nEnable)  
*Set TDO pin to indicate the fail of selected clock.*
- T\_osUInt8 [IDTGeneral\\_GetFlagOnTDO](#) (T\_idtDrvHdlr hdlr)  
*Get TDO pin to indicate the fail of selected clock.*
- void [IDTGeneral\\_SetUltraFastSwitch](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nEnable)  
*Set Ultra-fast-switch enable or not.*
- T\_osUInt8 [IDTGeneral\\_GetUltraFastSwitch](#) (T\_idtDrvHdlr hdlr)  
*Get Ultra-fast-switch enable or not.*
- void [IDTGeneral\\_SetHardAlarm](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nEnable)  
*Set Hard-alarm enable when the input exceeds the threshold.*
- T\_osUInt8 [IDTGeneral\\_GetHardAlarm](#) (T\_idtDrvHdlr hdlr)  
*Get Hard-alarm enable when the input exceeds the threshold.*
- T\_osUInt8 [IDTGeneral\\_i2cTranslate](#) (T\_osUInt8 i2cAddr, void \*transData)  
*I2C address translation function used internally by the driver.*
- void [IDTGeneral\\_InitDeviceCommon](#) (T\_idtDrvHdlr hdlr)
- T\_idtDrvHdlr [IDTGeneral\\_InitDriverCommon](#) (const char \*name, [T\\_idtDrvAccess](#) drvAccess, [T\\_idtDeviceType](#) deviceType, const [T\\_idtDrvDeviceConfig](#) \*deviceConfig, int useHighLevelApi)
- void [IDTGeneral\\_DeInitDriver](#) (T\_idtDrvHdlr hdlr)  
*De-initialize driver handler.*



## 6.37 common/include/Hal.h File Reference

```
#include "osNumeric.h"
#include "Define.h"
Include dependency graph for Hal.h:
```



### Macros

- #define `IDT_HAL_USE_MACRO` 0
- #define `IDTHAL_ModifyBitfield`(regVal, mask, lsb, data)  
*Define function to set bitfield value of read data from device.*
- #define `IDTHAL_GetBitfield`(regVal, mask, lsb) (((regVal) & (mask)) >> (lsb))  
*Define function to get bitfield value of read data from device.*

### Functions

- void `IDTHAL_WriteBitfield` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset, T\_osUInt8 mask, T\_osUInt8 lsb, T\_osUInt8 data)  
*Define function to write a bitfield to a device.*
- void `IDTHAL_WriteBitfield_Ext` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset, T\_osUInt8 mask, T\_osUInt8 lsb, T\_osUInt8 data)  
*Define function to write a bitfield to a device.*
- T\_osUInt8 `IDTHAL_ReadBitfield` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset, T\_osUInt8 mask, T\_osUInt8 lsb)  
*Define function to read a bitfield from device.*
- T\_osUInt8 `IDTHAL_ReadBitfield_Ext` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset, T\_osUInt8 mask, T\_osUInt8 lsb)  
*Define function to read a bitfield from device.*
- T\_osUInt8 `IDTHal_Read` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset)  
*Function to read from device.*
- void `IDTHal_Write` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset, T\_osUInt8 data)  
*Define function to write to device.*
- T\_osUInt8 `IDTHal_Read_Ext` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset)  
*Function to read from device apll address space.*

- void `IDTHal_Write_Ext` (`T_idtDrvHdlr` hdlr, `T_osUInt8` offset, `T_osUInt8` data)

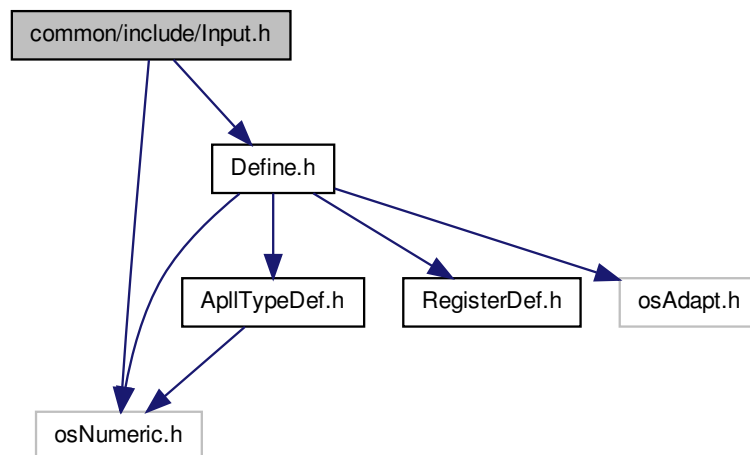
*Function to write to device apll address space.*

## 6.38 common/include/Input.h File Reference

```
#include "osNumeric.h"
```

```
#include "Define.h"
```

Include dependency graph for Input.h:



## Macros

- `#define Input_Phase_Lock_Alarm` 1
- `#define Input_No_Activity_Alarm` 2
- `#define Input_Freq_Hard_Alarm` 4
- `#define IDT_TRANSLATE_EXT_TO_INT_INPORT`(hdlr, ext, internal)  
*Utility macro to check if input port is supported and to translated from external port to internal port.*
- `#define IDT_EXT_INPORT_POPULATED`(hdlr, ext) (hdlr->deviceConfig\_m->inputExt2IntXlate\_ma[(ext)])  
*Utility macro to check if input port is populated.*

## Enumerations

- enum `T_idtInputDividerMux` { `Divider_Bypass` = 0, `Divider_Lock8k` = 1, `Divider_DivN` = 2, `Divider_MAX` }  
*Enumerated type listing input divider modes.*
- enum `T_idtHighFrequencyDivisor` { `HF_Bypass` = 0, `HF_Divide_4` = 1, `HF_Divide_5` = 2, `HF_MAX` }  
*Enumerated type listing high frequency (> 155.52MHz) dividers.*
- enum `T_idtInputFrequencyBitfieldValue` {  
`Freq_8K` = 0, `Freq_1544M` = 1, `Freq_2048M` = 1, `Freq_648M` = 2,  
`Freq_1944M` = 3, `Freq_2592M` = 4, `Freq_3888M` = 5, `Freq_2K` = 9,  
`Freq_4K` = 10, `Freq_1PPS` = 11, `Freq_625M` = 12, `Freq_10M` = 13,  
`Freq_MAX` }  
*Enumerated type listing input frequencies.*

- enum `T_idtInputFrequencyFamily` {  
`InFreqFamily_8K = 0, InFreqFamily_1544M = 1, InFreqFamily_2048M = 2, InFreqFamily_648M = 3,`  
`InFreqFamily_1944M = 4, InFreqFamily_2592M = 5, InFreqFamily_3888M = 6, InFreqFamily_2K = 7,`  
`InFreqFamily_4K = 8, InFreqFamily_1PPS = 9, InFreqFamily_625M = 10, InFreqFamily_10M = 11,`  
`InFreqFamily_MAX }`  
*Enumerated type listing input frequency families.*
- enum `T_idtAmiInputFrequencyBitFieldValue` { `AmiFreq_64kHzPlus8kHz, AmiFreq_64kHzPlus400Hz, AmiFreq_MAX` }  
*Enumerated type listing AMI Input frequencies.*
- enum `T_idtInputSyncFreq` {  
`SYNC_8kHz, SYNC_1PPS, SYNC_4kHz, SYNC_2kHz,`  
`SYNC_MAX }`  
*Enumerated type listing possible input sync frequencies.*
- enum `T_externalSyncSampling` {  
`externalSyncSampling_onTarget, externalSyncSampling_0dot5Early, externalSyncSampling_1dot0Late,`  
`externalSyncSampling_0dot5Late,`  
`externalSyncSampling_MAX }`  
*Enumerated type listing sampling of input external sync.*
- enum `T_externalSyncEdge` { `externalSyncEdge_FallingEdge, externalSyncEdge_RisingEdge, externalSyncEdge_MAX` }  
*Enumerated type listing possible external sync alignment options.*
- enum `T_externalSyncAlarmRange` {  
`externalSyncAlarmRange_1, externalSyncAlarmRange_2, externalSyncAlarmRange_3, externalSyncAlarmRange_4,`  
`externalSyncAlarmRange_5, externalSyncAlarmRange_6, externalSyncAlarmRange_7, externalSyncAlarmRange_8,`  
`externalSyncAlarmRange_MAX }`  
*Enumerate type listing ranges for external sync alarm.*
- enum `T_externalSyncBypass` { `externalSyncBypass_ExSync1, externalSyncBypass_AutoSel, externalSyncBypass_MAX` }  
*Enumerated type listing output synchronization with respect to.*
- enum `T_externalSyncEnable` { `externalSyncEnable_Disable, externalSyncEnable_Enable, externalSyncEnable_Auto, externalSyncEnable_MAX` }  
*Enumerated type listing enable options for external input sync.*

## Functions

- void `IDTInput_SetPriority` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo, `T_idtDpllInstance` nDpll, `T_osUInt8` nPriority)  
*Set specified port to the priority.*
- `T_osUInt8` `IDTInput_GetPriority` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo, `T_idtDpllInstance` nDpll)  
*Get the current priority of the specified port.*
- void `IDTInput_SetInputFrequency` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo, `T_idtInputFrequencyBitFieldValue` nFrequency)  
*Set the frequency of the input clock at the specified port.*
- `T_idtInputFrequencyBitFieldValue` `IDTInput_GetInputFrequency` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo)  
*Get frequency of the input clock at the specified port.*
- void `IDTInput_SetAmiInputFrequency` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo, `T_idtAmiInputFrequencyBitFieldValue` amiSignal)  
*Provision AMI signal for input port.*
- `T_idtAmiInputFrequencyBitFieldValue` `IDTInput_GetAmiInputFrequency` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo)  
*Function to retrieve AMI input frequency for input port.*

- void [IDTInput\\_SetActivityMonitor](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo, T\_osUInt8 nBucket)  
*Select one of the four activity monitor configurations for the specified input port.*
- T\_osUInt8 [IDTInput\\_GetActivityMonitor](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo)  
*Retrieve selected activity monitoring configuration.*
- void [IDTInput\\_SetBucketConfig](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nBucket, T\_osUInt8 nUpper, T\_osUInt8 nLower, T\_osUInt8 nSize, T\_osUInt8 nDecay)  
*Set the configuration to Leaky Bucket activity monitoring.*
- void [IDTInput\\_GetBucketConfig](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nBucket, T\_osUInt8 \*nUpper\_p, T\_osUInt8 \*nLower\_p, T\_osUInt8 \*nSize\_p, T\_osUInt8 \*nDecay\_p)  
*Get activity monitoring configuration (Leaky Bucket)*
- void [IDTInput\\_SetPreDivider](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo, [T\\_idtInputDividerMux](#) nDivider)  
*Assign a pre-divider for the specified input.*
- [T\\_idtInputDividerMux](#) [IDTInput\\_GetPreDivider](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo)  
*Get configured input port pre-divider.*
- void [IDTInput\\_SetDivisionFactor](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo, T\_osUInt16 iFactor)  
*Set the dividen factor to pre-divider assigned to a certain input.*
- T\_osUInt16 [IDTInput\\_GetDivisionFactor](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo)  
*Get the dividen factor to pre-divider assigned to a certain input.*
- void [IDTInput\\_SetInputHFdivider](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo, [T\\_idtHighFrequencyDivisor](#) nUsage)  
*Set the usage of high frequency (> 155.52MHz) divider.*
- [T\\_idtHighFrequencyDivisor](#) [IDTInput\\_GetInputHFdivider](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo)  
*Get high frequency configuration divider.*
- T\_osUInt8 [IDTInput\\_GetInputFreqOffset](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo)  
*Get the frequency offset of the specified input clock. The returned value is updated every 16 seconds.*
- T\_osUInt8 [IDTInput\\_GetInputClockStatus](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo)  
*Get the status of a specified input clock.*
- T\_osUInt8 [IDTInput\\_GetInputClockValidation](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo)  
*Get the clock validation status of an input port.*
- void [IDTInput\\_EnableAllInputs](#) (T\_idtDrvHdlr hdlr)  
*Enable to select anyone of input clocks.*
- void [IDTInput\\_DisableAllInputs](#) (T\_idtDrvHdlr hdlr)  
*Disable to select anyone of input clocks.*
- void [IDTInput\\_SetInputEnable](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo, T\_osUInt8 enable)  
*Enable/Disable selected input.*
- T\_osUInt8 [IDTInput\\_GetInputEnable](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo)  
*Retrieve enable/disable status of selected input.*
- void [IDTInput\\_SetSyncFrequency](#) (T\_idtDrvHdlr hdlr, [T\\_idtInputSyncFreq](#) syncFreq)  
*Function to select input external sync frequency.*
- [T\\_idtInputSyncFreq](#) [IDTInput\\_GetSyncFrequency](#) (T\_idtDrvHdlr hdlr)  
*Function to retrieve select input external sync frequency.*
- void [IDTInput\\_SetSyncSampling](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 exSyncN, [T\\_externalSyncSampling](#) sampling)  
*Function to provision sampling configuration for external sync.*
- [T\\_externalSyncSampling](#) [IDTInput\\_GetSyncSampling](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 exSyncN)  
*Function to retrieve sampling configuration for external sync.*
- void [IDTInput\\_SetSyncEdge](#) (T\_idtDrvHdlr hdlr, [T\\_externalSyncEdge](#) edge)  
*Function to provision synchronization alignment.*
- [T\\_externalSyncEdge](#) [IDTInput\\_GetSyncEdge](#) (T\_idtDrvHdlr hdlr)  
*Function to retrieve synchronization alignment.*
- void [IDTInput\\_SetSyncAlarmRange](#) (T\_idtDrvHdlr hdlr, [T\\_externalSyncAlarmRange](#) range)

- Function to provision the sync allowable range before alarming.*

• [T\\_externalSyncAlarmRange IDTInput\\_GetSyncAlarmRange](#) (T\_idtDrvHdlr hdlr)

*Function to retrieve the sync allowable range before alarming.*
- void [IDTInput\\_SetSyncBypass](#) (T\_idtDrvHdlr hdlr, [T\\_externalSyncBypass](#) bypass)

*Function to provision sync bypass mode.*
- [T\\_externalSyncBypass IDTInput\\_GetSyncBypass](#) (T\_idtDrvHdlr hdlr)

*Function to retrieve sync bypass mode.*
- void [IDTInput\\_SetSyncEnable](#) (T\_idtDrvHdlr hdlr, [T\\_externalSyncEnable](#) enable)

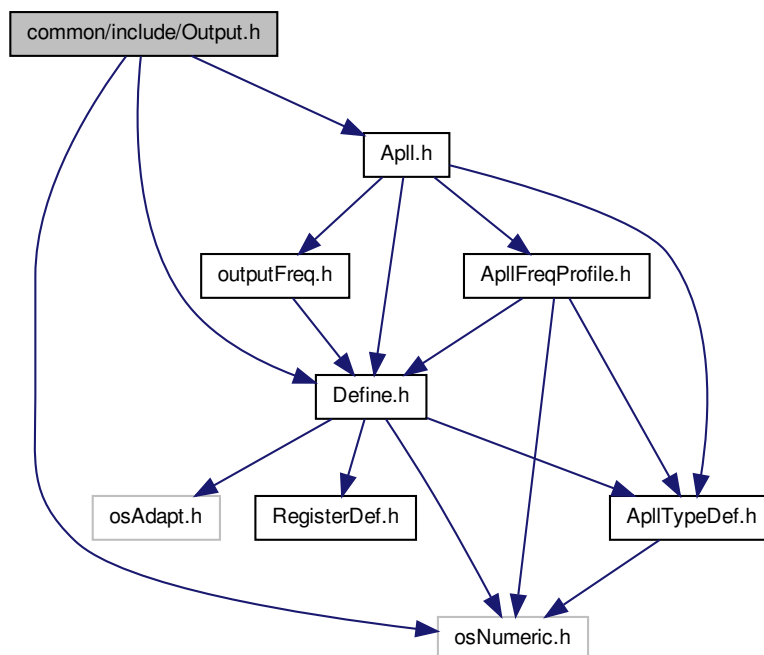
*Function to provision enable mode for input external sync.*
- [T\\_externalSyncEnable IDTInput\\_GetSyncEnable](#) (T\_idtDrvHdlr hdlr)

*Function to retrieve external sync enable mode.*
- [T\\_idtInputFrequencyFamily IDTInput\\_InFreqBitValue2Family](#) (T\_idtDrvHdlr hdlr, [T\\_idtInputFrequencyBitfield-Value](#) inFreqBitValue)

*Translate input frequency bit value to input frequency family.*

## 6.39 common/include/Output.h File Reference

```
#include "osNumeric.h"
#include "Define.h"
#include "Appl.h"
Include dependency graph for Output.h:
```



### Macros

- `#define` [IDT\\_TRANSLATE\\_EXT\\_TO\\_INT\\_OUTPORT](#)(hdlr, ext, internal)

*Utility macro to check if output port is supported and to translated from external port to internal port.*

- #define `IDT_EXT_OUTPORT_POPULATED`(hdlr, ext) (hdlr->deviceConfig\_m->outputExt2IntXlate\_ma[(ext)])  
Utility macro to check if output port is populated.

## Enumerations

- enum `T_outputPathType` {  
`OutputPath_SonetGigEth`, `OutputPath_7776kHz`, `OutputPath_Eth`, `OutputPath_16E1_16T1`,  
`OutputPath_12E1_E3_T3`, `OutputPath_GSM_16E1_16T1`, `OutputPath_GPS`, `OutputPath_OBSAI`,  
`OutputPath_24T1`, `OutputPath_MAX` }  
Enumerated type listing possible output port sources (from DPLL(s)) This enumerated type is used in conjunction with DPLL instance to select output DPLL frequency to output dividers. The following table outlines.
- enum `T_outputInterface` {  
`OUTPUTIF_AMI`, `OUTPUTIF_CMOS`, `OUTPUTIF_LVDS`, `OUTPUTIF_PECL`,  
`OUTPUTIF_MAX` }  
Enumerated type listing type of supported output port interfaces.
- enum `T_frameSync` { `frameSync_FRSYNC`, `frameSync_MFRSYNC`, `frameSync_MAX` }  
Enumerated type listing supported frame syncs.

## Functions

- void `IDTOutput_SetOutputConfig` (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN, T\_idtDpllInstance nDpll, T\_outputPathType nPath, T\_osUInt8 nFactor, T\_idtApllConfigPerOutput \*apllConfig)  
Set the configuration of Output port.
- void `IDTOutput_GetOutputConfig` (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN, T\_idtDpllInstance \*nDpll\_p, T\_outputPathType \*nPath\_p, T\_osUInt8 \*nFactor\_p, T\_idtApllConfigPerOutput \*apllConfig)  
Get the configuration of Output port.
- void `IDTOutput_SetOutputInvert` (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN, T\_osUInt8 invert)  
Set the specified output port to generate a invert signal.
- T\_osUInt8 `IDTOutput_GetOutputInvert` (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN)  
Get output signal inversion status.
- void `IDTOutput_SetOutputEnable` (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN, T\_osUInt8 nEnable)  
Enable/Disable output port. Consult data sheet for supported ports.
- T\_osUInt8 `IDTOutput_GetOutputEnable` (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN)  
Get enable/disable status of output port. Consult data sheet for supported ports.
- void `IDTOutput_SetOutputInterface` (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN, T\_outputInterface outIf)  
Set output port interface type. Consult data sheet for supported interfaces per port.
- T\_outputInterface `IDTOutput_GetOutputInterface` (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN)  
Get output port interface type. Consult data sheet for supported interfaces per port.
- void `IDTOutput_SetFrameSync` (T\_idtDrvHdlr hdlr, T\_frameSync frameSync, T\_osUInt8 enable, T\_osUInt8 invert, T\_osUInt8 pulse)  
Function to control output frame syncs.
- void `IDTOutput_GetFrameSync` (T\_idtDrvHdlr hdlr, T\_frameSync frameSync, T\_osUInt8 \*enable\_p, T\_osUInt8 \*invert\_p, T\_osUInt8 \*pulse\_p)  
Function to retrieve output frame sync configuration.
- void `IDTOutput_SetFrameSyncPulseEdge` (T\_idtDrvHdlr hdlr, T\_osUInt8 isRisingEdge)  
Function provision trigger for frame sync pulses.
- T\_osUInt8 `IDTOutput_GetFrameSyncPulseEdge` (T\_idtDrvHdlr hdlr)  
Function retrieve trigger for frame sync pulses.
- void `IDTOutput_DisableApllInput` (T\_idtDrvHdlr hdlr, T\_idtOutputApllConfig outputApllConfig)  
Function disables APLL input.
- void `IDTOutput_DisableAllIntOutput` (T\_idtDrvHdlr hdlr)  
Function disables all internal outputs.

## 6.40 common/include/RegisterDef.h File Reference

This header file contains register and bitfield information for accessing device.

### Enumerations

- enum {
  - REG\_ID\_LOW = 0x00, REG\_ID\_HIGH = 0x01, REG\_MPU\_PIN\_STS = 0x02, REG\_NOMINAL\_FREQ\_LO-  
W\_CNFG = 0x04,
  - REG\_NOMINAL\_FREQ\_MID\_CNFG = 0x05, REG\_NOMINAL\_FREQ\_HIGH\_CNFG = 0x06, REG\_T4\_T0\_  
SEL\_CNFG = 0x07, REG\_PHASE\_ALARM\_TIME\_OUT\_CNFG = 0x08,
  - REG\_INPUT\_MODE\_CNFG = 0x09, REG\_DIFFERENTIAL\_IN\_OUT\_CNFG = 0x0A, REG\_MON\_SW\_HS-  
\_CNFG = 0x0B, REG\_INTERRUPT\_CNFG = 0x0C,
  - REG\_INTERRUPTS1\_STS = 0x0D, REG\_INTERRUPTS2\_STS = 0x0E, REG\_INTERRUPTS3\_STS = 0x0F,  
REG\_INTERRUPTS1\_MASK\_CNFG = 0x10,
  - REG\_INTERRUPTS2\_MASK\_CNFG = 0x11, REG\_INTERRUPTS3\_MASK\_CNFG = 0x12, REG\_MS\_SL\_  
CTRL\_CNFG = 0x13, REG\_IN1\_CNFG = 0x14,
  - REG\_IN2\_CNFG = 0x15, REG\_IN3\_CNFG = 0x16, REG\_IN4\_CNFG = 0x17, REG\_IN5\_IN6\_HF\_DIV\_CN-  
FG = 0x18,
  - REG\_IN5\_CNFG = 0x19, REG\_IN6\_CNFG = 0x1A, REG\_IN7\_CNFG = 0x1B, REG\_IN8\_CNFG = 0x1C,  
REG\_IN9\_CNFG = 0x1D, REG\_IN10\_CNFG = 0x1E, REG\_IN11\_CNFG = 0x1F, REG\_IN12\_CNFG = 0x20,  
REG\_IN13\_CNFG = 0x21, REG\_IN14\_CNFG = 0x22, REG\_PRE\_DIV\_CH\_CNFG = 0x23, REG\_PRE\_DIV-  
N\_LOW\_CNFG = 0x24,
  - REG\_PRE\_DIVN\_HIGH\_CNFG = 0x25, REG\_IN1\_IN2\_SEL\_PRIORITY\_CNFG = 0x26, REG\_IN3\_IN4\_S-  
EL\_PRIORITY\_CNFG = 0x27, REG\_IN5\_IN6\_SEL\_PRIORITY\_CNFG = 0x28,
  - REG\_IN7\_IN8\_SEL\_PRIORITY\_CNFG = 0x29, REG\_IN9\_IN10\_SEL\_PRIORITY\_CNFG = 0x2A, REG\_I-  
N11\_IN12\_SEL\_PRIORITY\_CNFG = 0x2B, REG\_IN13\_IN14\_SEL\_PRIORITY\_CNFG = 0x2C,
  - REG\_PAGE\_POINTER\_CNFG = 0x2D, REG\_FREQ\_MON\_FACTOR\_CNFG = 0x2E, REG\_HARD\_FREQ-  
\_MON\_THRESHOLD\_CNFG = 0x2F, REG\_SOFT\_FREQ\_MON\_THRESHOLD\_CNFG = 0x30,
  - REG\_UPPER\_THRESHOLD\_0\_CNFG = 0x31, REG\_LOWER\_THRESHOLD\_0\_CNFG = 0x32, REG\_BU-  
CKET\_SIZE\_0\_CNFG = 0x33, REG\_DECAY\_RATE\_0\_CNFG = 0x34,
  - REG\_UPPER\_THRESHOLD\_1\_CNFG = 0x35, REG\_LOWER\_THRESHOLD\_1\_CNFG = 0x36, REG\_BU-  
CKET\_SIZE\_1\_CNFG = 0x37, REG\_DECAY\_RATE\_1\_CNFG = 0x38,
  - REG\_UPPER\_THRESHOLD\_2\_CNFG = 0x39, REG\_LOWER\_THRESHOLD\_2\_CNFG = 0x3A, REG\_BU-  
CKET\_SIZE\_2\_CNFG = 0x3B, REG\_DECAY\_RATE\_2\_CNFG = 0x3C,
  - REG\_UPPER\_THRESHOLD\_3\_CNFG = 0x3D, REG\_LOWER\_THRESHOLD\_3\_CNFG = 0x3E, REG\_BU-  
CKET\_SIZE\_3\_CNFG = 0x3F, REG\_DECAY\_RATE\_3\_CNFG = 0x40,
  - REG\_IN\_FREQ\_READ\_CH\_CNFG = 0x41, REG\_IN\_FREQ\_READ\_STS = 0x42, REG\_IN1\_IN2\_STS =  
0x43, REG\_IN3\_IN4\_STS = 0x44,
  - REG\_IN5\_IN6\_STS = 0x45, REG\_IN7\_IN8\_STS = 0x46, REG\_IN9\_IN10\_STS = 0x47, REG\_IN11\_IN12\_S-  
TS = 0x48,
  - REG\_IN13\_IN14\_STS = 0x49, REG\_INPUT\_VALID1\_STS = 0x4A, REG\_INPUT\_VALID2\_STS = 0x4B,  
REG\_REMOTE\_INPUT\_VALID1\_CNFG = 0x4C,
  - REG\_REMOTE\_INPUT\_VALID2\_CNFG = 0x4D, REG\_PRIORITY\_TABLE1\_STS = 0x4E, REG\_PRIORITY-  
\_TABLE2\_STS = 0x4F, REG\_T0\_INPUT\_SEL\_CNFG = 0x50,
  - REG\_T4\_INPUT\_SEL\_CNFG = 0x51, REG\_OPERATING\_STS = 0x52, REG\_T0\_OPERATION\_MODE\_C-  
NFG = 0x53, REG\_T4\_OPERATION\_MODE\_CNFG = 0x54,
  - REG\_T0\_DPLL\_APLL\_PATH\_CNFG = 0x55, REG\_T0\_DPLL\_START\_BW\_DAMPING\_CNFG = 0x56, R-  
EG\_T0\_DPLL\_ACQ\_BW\_DAMPING\_CNFG = 0x57, REG\_T0\_DPLL\_LOCKED\_BW\_DAMPING\_CNFG =  
0x58,
  - REG\_T0\_BW\_OVERSHOOT\_CNFG = 0x59, REG\_PHASE\_LOSS\_COARSE\_LIMIT\_CNFG = 0x5A, REG-  
\_PHASE\_LOSS\_FINE\_LIMIT\_CNFG = 0x5B, REG\_T0\_HOLDOVER\_MODE\_CNFG = 0x5C,
  - REG\_HOLDOVER\_FREQ\_LOW\_CNFG = 0x5D, REG\_HOLDOVER\_FREQ\_MID\_CNFG = 0x5E, REG\_HO-  
LDOVER\_FREQ\_HIGH\_CNFG = 0x5F, REG\_T4\_DPLL\_APLL\_PATH\_CNFG = 0x60,
  - REG\_T4\_DPLL\_LOCKED\_BW\_DAMPING\_CNFG = 0x61, REG\_CURRENT\_FREQ\_LOW\_STS = 0x62,  
REG\_CURRENT\_FREQ\_MID\_STS = 0x63, REG\_CURRENT\_FREQ\_HIGH\_STS = 0x64,
  - REG\_DPLL\_FREQ\_SOFT\_LIMIT\_CNFG = 0x65, REG\_DPLL\_FREQ\_HARD\_LIMIT\_LOW\_CNFG = 0x66,

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REG_DPLL_FREQ_HARD_LIMIT_MID_CNFG = 0x67, REG_CURRENT_DPLL_PHASE_LOW_STS =
0x68,
REG_CURRENT_DPLL_PHASE_HIGH_STS = 0x69, REG_OUT1_FREQ_CNFG = 0x6B, REG_OUT2_FR-
EQ_CNFG = 0x6C, REG_OUT3_FREQ_CNFG = 0x6D,
REG_OUT4_FREQ_CNFG = 0x6E, REG_OUT5_FREQ_CNFG = 0x6F, REG_OUT6_FREQ_CNFG = 0x70,
REG_OUT7_FREQ_CNFG = 0x71,
REG_OUT8_FREQ_CNFG = 0x72, REG_OUT9_FREQ_CNFG = 0x73, REG_FR_MFR_SYNC_CNFG =
0x74, REG_PHASE_MON_CNFG = 0x78,
REG_PHASE_OFFSET_LOW_CNFG = 0x7A, REG_PHASE_OFFSET_HIGH_CNFG = 0x7B, REG_SYNC-
_MONITOR_CNFG = 0x7C, REG_SYNC_PHASE_CNFG = 0x7D,
REG_PROTECTION_CNFG = 0x7E, REG_MPU_SEL_CNFG = 0x7F, REG_DFS_OFF_CNFG = 0x30, RE-
G_T0_PPS_CNFG = 0x31,
REG_PH_SLOPE_CNFG = 0x32, REG_T0_ICP_CTRL_CNFG = 0x33, REG_T4_ICP_CTRL_CNFG = 0x34,
REG_T4_PPS_CNFG = 0x3E,
BF_ID_A_SIZE = 8, BF_ID_A_MASK = 0xFF, BF_ID_A_LSB = 0, BF_ID_B_SIZE = 8,
BF_ID_B_MASK = 0xFF, BF_ID_B_LSB = 0, BF_MPU_PIN_STS_SIZE = 1, BF_MPU_PIN_STS_MASK =
0x01,
BF_MPU_PIN_STS_LSB = 0, BF_NOMINAL_FREQ_VALUE_A_SIZE = 8, BF_NOMINAL_FREQ_VALUE_-
A_MASK = 0xFF, BF_NOMINAL_FREQ_VALUE_A_LSB = 0,
BF_NOMINAL_FREQ_VALUE_B_SIZE = 8, BF_NOMINAL_FREQ_VALUE_B_MASK = 0xFF, BF_NOMIN-
AL_FREQ_VALUE_B_LSB = 0, BF_NOMINAL_FREQ_VALUE_C_SIZE = 8,
BF_NOMINAL_FREQ_VALUE_C_MASK = 0xFF, BF_NOMINAL_FREQ_VALUE_C_LSB = 0, BF_T4_T0_S-
EL_SIZE = 1, BF_T4_T0_SEL_MASK = 0x10,
BF_T4_T0_SEL_LSB = 4, BF_MULTI_FACTOR_SIZE = 2, BF_MULTI_FACTOR_MASK = 0xC0, BF_MUL-
TI_FACTOR_LSB = 6,
BF_TIMEOUT_VALUE_SIZE = 6, BF_TIMEOUT_VALUE_MASK = 0x3F, BF_TIMEOUT_VALUE_LSB = 0,
BF_AUTO_EXT_SYNC_EN_SIZE = 1,
BF_AUTO_EXT_SYNC_EN_MASK = 0x80, BF_AUTO_EXT_SYNC_EN_LSB = 7, BF_EXT_SYNC_EN_SI-
ZE = 1, BF_EXT_SYNC_EN_MASK = 0x40,
BF_EXT_SYNC_EN_LSB = 6, BF_PH_ALARM_TIMEOUT_SIZE = 1, BF_PH_ALARM_TIMEOUT_MASK =
0x20, BF_PH_ALARM_TIMEOUT_LSB = 5,
BF_SYNC_FREQ_SIZE = 2, BF_SYNC_FREQ_MASK = 0x18, BF_SYNC_FREQ_LSB = 3, BF_IN_SONE-
T_SDH_SIZE = 1,
BF_IN_SONET_SDH_MASK = 0x04, BF_IN_SONET_SDH_LSB = 2, BF_MASTER_SLAVE_SIZE = 1, BF_-
MASTER_SLAVE_MASK = 0x02,
BF_MASTER_SLAVE_LSB = 1, BF_REVERTIVE_MODE_SIZE = 1, BF_REVERTIVE_MODE_MASK =
0x01, BF_REVERTIVE_MODE_LSB = 0,
BF_OSC_EDGE_SIZE = 1, BF_OSC_EDGE_MASK = 0x04, BF_OSC_EDGE_LSB = 2, BF_OUT7_PECL_-
LVDS_SIZE = 1,
BF_OUT7_PECL_LVDS_MASK = 0x02, BF_OUT7_PECL_LVDS_LSB = 1, BF_OUT6_PECL_LVDS_SIZE
= 1, BF_OUT6_PECL_LVDS_MASK = 0x01,
BF_OUT6_PECL_LVDS_LSB = 0, BF_FREQ_MON_CLK_SIZE = 1, BF_FREQ_MON_CLK_MASK = 0x80,
BF_FREQ_MON_CLK_LSB = 7,
BF_LOS_FLAG_TO_TDO_SIZE = 1, BF_LOS_FLAG_TO_TDO_MASK = 0x40, BF_LOS_FLAG_TO_TDO-
_LSB = 6, BF_ULTR_FAST_SW_SIZE = 1,
BF_ULTR_FAST_SW_MASK = 0x20, BF_ULTR_FAST_SW_LSB = 5, BF_EXT_SW_SIZE = 1, BF_EXT_S-
W_MASK = 0x10,
BF_EXT_SW_LSB = 4, BF_HS_FREZ_SIZE = 1, BF_HS_FREZ_MASK = 0x08, BF_HS_FREZ_LSB = 3,
BF_HS_EN_SIZE = 1, BF_HS_EN_MASK = 0x04, BF_HS_EN_LSB = 2, BF_FREQ_MON_HARD_EN_SIZE
= 1,
BF_FREQ_MON_HARD_EN_MASK = 0x01, BF_FREQ_MON_HARD_EN_LSB = 0, BF_HZ_EN_SIZE = 1,

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BF_HZ_EN_MASK = 0x02,
BF_HZ_EN_LSB = 1, BF_INT_POL_SIZE = 1, BF_INT_POL_MASK = 0x01, BF_INT_POL_LSB = 0,
BF_IN8_SIZE = 1, BF_IN8_MASK = 0x80, BF_IN8_LSB = 7, BF_IN7_SIZE = 1,
BF_IN7_MASK = 0x40, BF_IN7_LSB = 6, BF_IN6_SIZE = 1, BF_IN6_MASK = 0x20,
BF_IN6_LSB = 5, BF_IN5_SIZE = 1, BF_IN5_MASK = 0x10, BF_IN5_LSB = 4,
BF_IN4_SIZE = 1, BF_IN4_MASK = 0x08, BF_IN4_LSB = 3, BF_IN3_SIZE = 1,
BF_IN3_MASK = 0x04, BF_IN3_LSB = 2, BF_IN2_SIZE = 1, BF_IN2_MASK = 0x02,
BF_IN2_LSB = 1, BF_IN1_SIZE = 1, BF_IN1_MASK = 0x01, BF_IN1_LSB = 0,
BF_TO_OPERATING_MODE_STS_SIZE = 1, BF_TO_OPERATING_MODE_STS_MASK = 0x80, BF_TO_
OPERATING_MODE_STS_LSB = 7, BF_TO_MAIN_REF_FAIL_SIZE = 1,
BF_TO_MAIN_REF_FAIL_MASK = 0x40, BF_TO_MAIN_REF_FAIL_LSB = 6, BF_IN14_SIZE = 1, BF_IN14_
_MASK = 0x20,
BF_IN14_LSB = 5, BF_IN13_SIZE = 1, BF_IN13_MASK = 0x10, BF_IN13_LSB = 4,
BF_IN12_SIZE = 1, BF_IN12_MASK = 0x08, BF_IN12_LSB = 3, BF_IN11_SIZE = 1,
BF_IN11_MASK = 0x04, BF_IN11_LSB = 2, BF_IN10_SIZE = 1, BF_IN10_MASK = 0x02,
BF_IN10_LSB = 1, BF_IN9_SIZE = 1, BF_IN9_MASK = 0x01, BF_IN9_LSB = 0,
BF_EX_SYNC_ALARM_SIZE = 1, BF_EX_SYNC_ALARM_MASK = 0x80, BF_EX_SYNC_ALARM_LSB =
7, BF_T4_STS_SIZE = 1,
BF_T4_STS_MASK = 0x40, BF_T4_STS_LSB = 6, BF_INPUT_TO_T4_SIZE = 1, BF_INPUT_TO_T4_MA
SK = 0x10,
BF_INPUT_TO_T4_LSB = 4, BF_AMI2_VIOL_SIZE = 1, BF_AMI2_VIOL_MASK = 0x08, BF_AMI2_VIOL_
_LSB = 3,
BF_AMI2_LOS_SIZE = 1, BF_AMI2_LOS_MASK = 0x04, BF_AMI2_LOS_LSB = 2, BF_AMI1_VIOL_SIZE =
1,
BF_AMI1_VIOL_MASK = 0x02, BF_AMI1_VIOL_LSB = 1, BF_AMI1_LOS_SIZE = 1, BF_AMI1_LOS_MASK
= 0x01,
BF_AMI1_LOS_LSB = 0, BF_PPS_FAST_FREQ_LOCK_EN_SIZE = 1, BF_PPS_FAST_FREQ_LOCK_EN_
_MASK = 0x10, BF_PPS_FAST_FREQ_LOCK_EN_LSB = 4,
BF_PPS_FAST_PH_LOCK_EN_SIZE = 1, BF_PPS_FAST_PH_LOCK_EN_MASK = 0x08, BF_PPS_FAST_
_PH_LOCK_EN_LSB = 3, BF_MS_SL_CTRL_SIZE = 1,
BF_MS_SL_CTRL_MASK = 0x01, BF_MS_SL_CTRL_LSB = 0, BF_400HZ_SEL_SIZE = 1, BF_400HZ_SE
L_MASK = 0x40,
BF_400HZ_SEL_LSB = 6, BF_BUCKET_SEL_SIZE = 2, BF_BUCKET_SEL_MASK = 0x30, BF_BUCKET_
_SEL_LSB = 4,
BF_IN_FREQ_SIZE = 4, BF_IN_FREQ_MASK = 0x0F, BF_IN_FREQ_LSB = 0, BF_DIRECT_DIV_SIZE = 1,
BF_DIRECT_DIV_MASK = 0x80, BF_DIRECT_DIV_LSB = 7, BF_LOCK_8K_SIZE = 1, BF_LOCK_8K_MA
SK = 0x40,
BF_LOCK_8K_LSB = 6, BF_IN6_DIV_SIZE = 2, BF_IN6_DIV_MASK = 0xC0, BF_IN6_DIV_LSB = 6,
BF_IN5_DIV_SIZE = 2, BF_IN5_DIV_MASK = 0x03, BF_IN5_DIV_LSB = 0, BF_PRE_DIV_CH_VALUE_SI
ZE = 4,
BF_PRE_DIV_CH_VALUE_MASK = 0x0F, BF_PRE_DIV_CH_VALUE_LSB = 0, BF_PRE_DIVN_VALUE_
A_SIZE = 8, BF_PRE_DIVN_VALUE_A_MASK = 0xFF,
BF_PRE_DIVN_VALUE_A_LSB = 0, BF_PRE_DIVN_VALUE_B_SIZE = 7, BF_PRE_DIVN_VALUE_B_MA
SK = 0x7F, BF_PRE_DIVN_VALUE_B_LSB = 0,
BF_IN2_SEL_PRIORITY_SIZE = 4, BF_IN2_SEL_PRIORITY_MASK = 0xF0, BF_IN2_SEL_PRIORITY_LS
B = 4, BF_IN1_SEL_PRIORITY_SIZE = 4,
BF_IN1_SEL_PRIORITY_MASK = 0x0F, BF_IN1_SEL_PRIORITY_LSB = 0, BF_IN4_SEL_PRIORITY_SIZE
= 4, BF_IN4_SEL_PRIORITY_MASK = 0xF0,
BF_IN4_SEL_PRIORITY_LSB = 4, BF_IN3_SEL_PRIORITY_SIZE = 4, BF_IN3_SEL_PRIORITY_MASK =
0x0F, BF_IN3_SEL_PRIORITY_LSB = 0,
BF_IN6_SEL_PRIORITY_SIZE = 4, BF_IN6_SEL_PRIORITY_MASK = 0xF0, BF_IN6_SEL_PRIORITY_LS
B = 4, BF_IN5_SEL_PRIORITY_SIZE = 4,
BF_IN5_SEL_PRIORITY_MASK = 0x0F, BF_IN5_SEL_PRIORITY_LSB = 0, BF_IN8_SEL_PRIORITY_SIZE
= 4, BF_IN8_SEL_PRIORITY_MASK = 0xF0,
BF_IN8_SEL_PRIORITY_LSB = 4, BF_IN7_SEL_PRIORITY_SIZE = 4, BF_IN7_SEL_PRIORITY_MASK =
0x0F, BF_IN7_SEL_PRIORITY_LSB = 0,
BF_IN10_SEL_PRIORITY_SIZE = 4, BF_IN10_SEL_PRIORITY_MASK = 0xF0, BF_IN10_SEL_PRIORITY_

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_LSB = 4, BF_IN9_SEL_PRIORITY_SIZE = 4,
BF_IN9_SEL_PRIORITY_MASK = 0x0F, BF_IN9_SEL_PRIORITY_LSB = 0, BF_IN12_SEL_PRIORITY_SIZE = 4, BF_IN12_SEL_PRIORITY_MASK = 0xF0,
BF_IN12_SEL_PRIORITY_LSB = 4, BF_IN11_SEL_PRIORITY_SIZE = 4, BF_IN11_SEL_PRIORITY_MASK = 0x0F, BF_IN11_SEL_PRIORITY_LSB = 0,
BF_IN14_SEL_PRIORITY_SIZE = 4, BF_IN14_SEL_PRIORITY_MASK = 0xF0, BF_IN14_SEL_PRIORITY_LSB = 4, BF_IN13_SEL_PRIORITY_SIZE = 4,
BF_IN13_SEL_PRIORITY_MASK = 0x0F, BF_IN13_SEL_PRIORITY_LSB = 0, BF_PAGE_POINTER_SIZE = 1, BF_PAGE_POINTER_MASK = 0x01,
BF_PAGE_POINTER_LSB = 0, BF_FREQ_MON_FACTOR_SIZE = 4, BF_FREQ_MON_FACTOR_MASK = 0x0F, BF_FREQ_MON_FACTOR_LSB = 0,
BF_HARD_FREQ_MON_THRESHOLD_A_SIZE = 4, BF_HARD_FREQ_MON_THRESHOLD_A_MASK = 0xF0, BF_HARD_FREQ_MON_THRESHOLD_A_LSB = 4, BF_HARD_FREQ_MON_THRESHOLD_B_SIZE = 4,
BF_HARD_FREQ_MON_THRESHOLD_B_MASK = 0x0F, BF_HARD_FREQ_MON_THRESHOLD_B_LSB = 0, BF_SOFT_FREQ_MON_THRESHOLD_A_SIZE = 4, BF_SOFT_FREQ_MON_THRESHOLD_A_MASK = 0xF0,
BF_SOFT_FREQ_MON_THRESHOLD_A_LSB = 4, BF_SOFT_FREQ_MON_THRESHOLD_B_SIZE = 4, BF_SOFT_FREQ_MON_THRESHOLD_B_MASK = 0x0F, BF_SOFT_FREQ_MON_THRESHOLD_B_LSB = 0,
BF_UPPER_THRESHOLD_DATA_SIZE = 8, BF_UPPER_THRESHOLD_DATA_MASK = 0xFF, BF_UPPER_THRESHOLD_DATA_LSB = 0, BF_LOWER_THRESHOLD_DATA_SIZE = 8,
BF_LOWER_THRESHOLD_DATA_MASK = 0xFF, BF_LOWER_THRESHOLD_DATA_LSB = 0, BF_BUCKET_SIZE_DATA_SIZE = 8, BF_BUCKET_SIZE_DATA_MASK = 0xFF,
BF_BUCKET_SIZE_DATA_LSB = 0, BF_DECAY_RATE_DATA_SIZE = 2, BF_DECAY_RATE_DATA_MASK = 0x03, BF_DECAY_RATE_DATA_LSB = 0,
BF_IN_FREQ_READ_CH_SIZE = 4, BF_IN_FREQ_READ_CH_MASK = 0x0F, BF_IN_FREQ_READ_CH_LSB = 0, BF_IN_FREQ_VALUE_SIZE = 8,
BF_IN_FREQ_VALUE_MASK = 0xFF, BF_IN_FREQ_VALUE_LSB = 0, BF_IN2_FREQ_SOFT_ALARM_SIZE = 1, BF_IN2_FREQ_SOFT_ALARM_MASK = 0x80,
BF_IN2_FREQ_SOFT_ALARM_LSB = 7, BF_IN2_FREQ_HARD_ALARM_SIZE = 1, BF_IN2_FREQ_HARD_ALARM_MASK = 0x40, BF_IN2_FREQ_HARD_ALARM_LSB = 6,
BF_IN2_NO_ACTIVITY_ALARM_SIZE = 1, BF_IN2_NO_ACTIVITY_ALARM_MASK = 0x20, BF_IN2_NO_ACTIVITY_ALARM_LSB = 5, BF_IN2_PH_LOCK_ALARM_SIZE = 1,
BF_IN2_PH_LOCK_ALARM_MASK = 0x10, BF_IN2_PH_LOCK_ALARM_LSB = 4, BF_IN1_FREQ_SOFT_ALARM_SIZE = 1, BF_IN1_FREQ_SOFT_ALARM_MASK = 0x08,
BF_IN1_FREQ_SOFT_ALARM_LSB = 3, BF_IN1_FREQ_HARD_ALARM_SIZE = 1, BF_IN1_FREQ_HARD_ALARM_MASK = 0x04, BF_IN1_FREQ_HARD_ALARM_LSB = 2,
BF_IN1_NO_ACTIVITY_ALARM_SIZE = 1, BF_IN1_NO_ACTIVITY_ALARM_MASK = 0x02, BF_IN1_NO_ACTIVITY_ALARM_LSB = 1, BF_IN1_PH_LOCK_ALARM_SIZE = 1,
BF_IN1_PH_LOCK_ALARM_MASK = 0x01, BF_IN1_PH_LOCK_ALARM_LSB = 0, BF_IN4_FREQ_SOFT_ALARM_SIZE = 1, BF_IN4_FREQ_SOFT_ALARM_MASK = 0x80,
BF_IN4_FREQ_SOFT_ALARM_LSB = 7, BF_IN4_FREQ_HARD_ALARM_SIZE = 1, BF_IN4_FREQ_HARD_ALARM_MASK = 0x40, BF_IN4_FREQ_HARD_ALARM_LSB = 6,
BF_IN4_NO_ACTIVITY_ALARM_SIZE = 1, BF_IN4_NO_ACTIVITY_ALARM_MASK = 0x20, BF_IN4_NO_ACTIVITY_ALARM_LSB = 5, BF_IN4_PH_LOCK_ALARM_SIZE = 1,
BF_IN4_PH_LOCK_ALARM_MASK = 0x10, BF_IN4_PH_LOCK_ALARM_LSB = 4, BF_IN3_FREQ_SOFT_ALARM_SIZE = 1, BF_IN3_FREQ_SOFT_ALARM_MASK = 0x08,
BF_IN3_FREQ_SOFT_ALARM_LSB = 3, BF_IN3_FREQ_HARD_ALARM_SIZE = 1, BF_IN3_FREQ_HARD_ALARM_MASK = 0x04, BF_IN3_FREQ_HARD_ALARM_LSB = 2,
BF_IN3_NO_ACTIVITY_ALARM_SIZE = 1, BF_IN3_NO_ACTIVITY_ALARM_MASK = 0x02, BF_IN3_NO_ACTIVITY_ALARM_LSB = 1, BF_IN3_PH_LOCK_ALARM_SIZE = 1,
BF_IN3_PH_LOCK_ALARM_MASK = 0x01, BF_IN3_PH_LOCK_ALARM_LSB = 0, BF_IN6_FREQ_SOFT_ALARM_SIZE = 1, BF_IN6_FREQ_SOFT_ALARM_MASK = 0x80,
BF_IN6_FREQ_SOFT_ALARM_LSB = 7, BF_IN6_FREQ_HARD_ALARM_SIZE = 1, BF_IN6_FREQ_HARD_ALARM_MASK = 0x40, BF_IN6_FREQ_HARD_ALARM_LSB = 6,
BF_IN6_NO_ACTIVITY_ALARM_SIZE = 1, BF_IN6_NO_ACTIVITY_ALARM_MASK = 0x20, BF_IN6_NO_

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ACTIVITY_ALARM_LSB = 5, BF_IN6_PH_LOCK_ALARM_SIZE = 1,
BF_IN6_PH_LOCK_ALARM_MASK = 0x10, BF_IN6_PH_LOCK_ALARM_LSB = 4, BF_IN5_FREQ_SOFT_
_ALARM_SIZE = 1, BF_IN5_FREQ_SOFT_ALARM_MASK = 0x08,
BF_IN5_FREQ_SOFT_ALARM_LSB = 3, BF_IN5_FREQ_HARD_ALARM_SIZE = 1, BF_IN5_FREQ_HAR_
D_ALARM_MASK = 0x04, BF_IN5_FREQ_HARD_ALARM_LSB = 2,
BF_IN5_NO_ACTIVITY_ALARM_SIZE = 1, BF_IN5_NO_ACTIVITY_ALARM_MASK = 0x02, BF_IN5_NO_
ACTIVITY_ALARM_LSB = 1, BF_IN5_PH_LOCK_ALARM_SIZE = 1,
BF_IN5_PH_LOCK_ALARM_MASK = 0x01, BF_IN5_PH_LOCK_ALARM_LSB = 0, BF_IN8_FREQ_SOFT_
_ALARM_SIZE = 1, BF_IN8_FREQ_SOFT_ALARM_MASK = 0x80,
BF_IN8_FREQ_SOFT_ALARM_LSB = 7, BF_IN8_FREQ_HARD_ALARM_SIZE = 1, BF_IN8_FREQ_HAR_
D_ALARM_MASK = 0x40, BF_IN8_FREQ_HARD_ALARM_LSB = 6,
BF_IN8_NO_ACTIVITY_ALARM_SIZE = 1, BF_IN8_NO_ACTIVITY_ALARM_MASK = 0x20, BF_IN8_NO_
ACTIVITY_ALARM_LSB = 5, BF_IN8_PH_LOCK_ALARM_SIZE = 1,
BF_IN8_PH_LOCK_ALARM_MASK = 0x10, BF_IN8_PH_LOCK_ALARM_LSB = 4, BF_IN7_FREQ_SOFT_
_ALARM_SIZE = 1, BF_IN7_FREQ_SOFT_ALARM_MASK = 0x08,
BF_IN7_FREQ_SOFT_ALARM_LSB = 3, BF_IN7_FREQ_HARD_ALARM_SIZE = 1, BF_IN7_FREQ_HAR_
D_ALARM_MASK = 0x04, BF_IN7_FREQ_HARD_ALARM_LSB = 2,
BF_IN7_NO_ACTIVITY_ALARM_SIZE = 1, BF_IN7_NO_ACTIVITY_ALARM_MASK = 0x02, BF_IN7_NO_
ACTIVITY_ALARM_LSB = 1, BF_IN7_PH_LOCK_ALARM_SIZE = 1,
BF_IN7_PH_LOCK_ALARM_MASK = 0x01, BF_IN7_PH_LOCK_ALARM_LSB = 0, BF_IN10_FREQ_SOF_
T_ALARM_SIZE = 1, BF_IN10_FREQ_SOFT_ALARM_MASK = 0x80,
BF_IN10_FREQ_SOFT_ALARM_LSB = 7, BF_IN10_FREQ_HARD_ALARM_SIZE = 1, BF_IN10_FREQ_H_
ARD_ALARM_MASK = 0x40, BF_IN10_FREQ_HARD_ALARM_LSB = 6,
BF_IN10_NO_ACTIVITY_ALARM_SIZE = 1, BF_IN10_NO_ACTIVITY_ALARM_MASK = 0x20, BF_IN10_
NO_ACTIVITY_ALARM_LSB = 5, BF_IN10_PH_LOCK_ALARM_SIZE = 1,
BF_IN10_PH_LOCK_ALARM_MASK = 0x10, BF_IN10_PH_LOCK_ALARM_LSB = 4, BF_IN9_FREQ_SO_
FT_ALARM_SIZE = 1, BF_IN9_FREQ_SOFT_ALARM_MASK = 0x08,
BF_IN9_FREQ_SOFT_ALARM_LSB = 3, BF_IN9_FREQ_HARD_ALARM_SIZE = 1, BF_IN9_FREQ_HAR_
D_ALARM_MASK = 0x04, BF_IN9_FREQ_HARD_ALARM_LSB = 2,
BF_IN9_NO_ACTIVITY_ALARM_SIZE = 1, BF_IN9_NO_ACTIVITY_ALARM_MASK = 0x02, BF_IN9_NO_
ACTIVITY_ALARM_LSB = 1, BF_IN9_PH_LOCK_ALARM_SIZE = 1,
BF_IN9_PH_LOCK_ALARM_MASK = 0x01, BF_IN9_PH_LOCK_ALARM_LSB = 0, BF_IN12_FREQ_SOF_
T_ALARM_SIZE = 1, BF_IN12_FREQ_SOFT_ALARM_MASK = 0x80,
BF_IN12_FREQ_SOFT_ALARM_LSB = 7, BF_IN12_FREQ_HARD_ALARM_SIZE = 1, BF_IN12_FREQ_H_
ARD_ALARM_MASK = 0x40, BF_IN12_FREQ_HARD_ALARM_LSB = 6,
BF_IN12_NO_ACTIVITY_ALARM_SIZE = 1, BF_IN12_NO_ACTIVITY_ALARM_MASK = 0x20, BF_IN12_
NO_ACTIVITY_ALARM_LSB = 5, BF_IN12_PH_LOCK_ALARM_SIZE = 1,
BF_IN12_PH_LOCK_ALARM_MASK = 0x10, BF_IN12_PH_LOCK_ALARM_LSB = 4, BF_IN11_FREQ_S_
OFT_ALARM_SIZE = 1, BF_IN11_FREQ_SOFT_ALARM_MASK = 0x08,
BF_IN11_FREQ_SOFT_ALARM_LSB = 3, BF_IN11_FREQ_HARD_ALARM_SIZE = 1, BF_IN11_FREQ_H_
ARD_ALARM_MASK = 0x04, BF_IN11_FREQ_HARD_ALARM_LSB = 2,
BF_IN11_NO_ACTIVITY_ALARM_SIZE = 1, BF_IN11_NO_ACTIVITY_ALARM_MASK = 0x02, BF_IN11_
NO_ACTIVITY_ALARM_LSB = 1, BF_IN11_PH_LOCK_ALARM_SIZE = 1,
BF_IN11_PH_LOCK_ALARM_MASK = 0x01, BF_IN11_PH_LOCK_ALARM_LSB = 0, BF_IN14_FREQ_S_
OFT_ALARM_SIZE = 1, BF_IN14_FREQ_SOFT_ALARM_MASK = 0x80,
BF_IN14_FREQ_SOFT_ALARM_LSB = 7, BF_IN14_FREQ_HARD_ALARM_SIZE = 1, BF_IN14_FREQ_H_
ARD_ALARM_MASK = 0x40, BF_IN14_FREQ_HARD_ALARM_LSB = 6,
BF_IN14_NO_ACTIVITY_ALARM_SIZE = 1, BF_IN14_NO_ACTIVITY_ALARM_MASK = 0x20, BF_IN14_
NO_ACTIVITY_ALARM_LSB = 5, BF_IN14_PH_LOCK_ALARM_SIZE = 1,
BF_IN14_PH_LOCK_ALARM_MASK = 0x10, BF_IN14_PH_LOCK_ALARM_LSB = 4, BF_IN13_FREQ_S_
OFT_ALARM_SIZE = 1, BF_IN13_FREQ_SOFT_ALARM_MASK = 0x08,
BF_IN13_FREQ_SOFT_ALARM_LSB = 3, BF_IN13_FREQ_HARD_ALARM_SIZE = 1, BF_IN13_FREQ_H_
ARD_ALARM_MASK = 0x04, BF_IN13_FREQ_HARD_ALARM_LSB = 2,
BF_IN13_NO_ACTIVITY_ALARM_SIZE = 1, BF_IN13_NO_ACTIVITY_ALARM_MASK = 0x02, BF_IN13_
NO_ACTIVITY_ALARM_LSB = 1, BF_IN13_PH_LOCK_ALARM_SIZE = 1,
BF_IN13_PH_LOCK_ALARM_MASK = 0x01, BF_IN13_PH_LOCK_ALARM_LSB = 0, BF_HIGHEST_PRI_
ORITY_VALIDATED_SIZE = 4, BF_HIGHEST_PRIORITY_VALIDATED_MASK = 0xF0,
BF_HIGHEST_PRIORITY_VALIDATED_LSB = 4, BF_CURRENTLY_SELECTED_INPUTS_SIZE = 4, BF_

```

CURRENTLY\_SELECTED\_INPUTS\_MASK = 0x0F, BF\_CURRENTLY\_SELECTED\_INPUTS\_LSB = 0,  
 BF\_THIRD\_HIGHEST\_PRIORITY\_VALIDATED\_SIZE = 4, BF\_THIRD\_HIGHEST\_PRIORITY\_VALIDATE-  
 D\_MASK = 0xF0, BF\_THIRD\_HIGHEST\_PRIORITY\_VALIDATED\_LSB = 4, BF\_SECOND\_HIGHEST\_PRI-  
 ORITY\_VALIDATED\_SIZE = 4,  
 BF\_SECOND\_HIGHEST\_PRIORITY\_VALIDATED\_MASK = 0x0F, BF\_SECOND\_HIGHEST\_PRIORITY\_V-  
 ALIDATED\_LSB = 0, BF\_T0\_INPUT\_SEL\_SIZE = 4, BF\_T0\_INPUT\_SEL\_MASK = 0x0F,  
 BF\_T0\_INPUT\_SEL\_LSB = 0, BF\_T4\_LOCK\_T0\_SIZE = 1, BF\_T4\_LOCK\_T0\_MASK = 0x40, BF\_T4\_LOC-  
 K\_T0\_LSB = 6,  
 BF\_T0\_FOR\_T4\_SIZE = 1, BF\_T0\_FOR\_T4\_MASK = 0x20, BF\_T0\_FOR\_T4\_LSB = 5, BF\_T4\_TEST\_T0\_-  
 PH\_SIZE = 1,  
 BF\_T4\_TEST\_T0\_PH\_MASK = 0x10, BF\_T4\_TEST\_T0\_PH\_LSB = 4, BF\_T4\_INPUT\_SEL\_SIZE = 4, BF\_-  
 T4\_INPUT\_SEL\_MASK = 0x0F,  
 BF\_T4\_INPUT\_SEL\_LSB = 0, BF\_EX\_SYNC\_ALARM\_MON\_SIZE = 1, BF\_EX\_SYNC\_ALARM\_MON\_M-  
 ASK = 0x80, BF\_EX\_SYNC\_ALARM\_MON\_LSB = 7,  
 BF\_T4\_DPLL\_LOCK\_SIZE = 1, BF\_T4\_DPLL\_LOCK\_MASK = 0x40, BF\_T4\_DPLL\_LOCK\_LSB = 6, BF\_-  
 T0\_DPLL\_SOFT\_FREQ\_ALARM\_SIZE = 1,  
 BF\_T0\_DPLL\_SOFT\_FREQ\_ALARM\_MASK = 0x20, BF\_T0\_DPLL\_SOFT\_FREQ\_ALARM\_LSB = 5, BF\_-  
 T4\_DPLL\_SOFT\_FREQ\_ALARM\_SIZE = 1, BF\_T4\_DPLL\_SOFT\_FREQ\_ALARM\_MASK = 0x10,  
 BF\_T4\_DPLL\_SOFT\_FREQ\_ALARM\_LSB = 4, BF\_T0\_DPLL\_LOCK\_SIZE = 1, BF\_T0\_DPLL\_LOCK\_MA-  
 SK = 0x08, BF\_T0\_DPLL\_LOCK\_LSB = 3,  
 BF\_T0\_DPLL\_OPERATING\_MODE\_SIZE = 3, BF\_T0\_DPLL\_OPERATING\_MODE\_MASK = 0x07, BF\_T0\_-  
 DPLL\_OPERATING\_MODE\_LSB = 0, BF\_T0\_WDCO\_SIZE = 1,  
 BF\_T0\_WDCO\_MASK = 0x08, BF\_T0\_WDCO\_LSB = 3, BF\_T0\_OPERATING\_MODE\_SIZE = 3, BF\_T0\_-  
 OPERATING\_MODE\_MASK = 0x07,  
 BF\_T0\_OPERATING\_MODE\_LSB = 0, BF\_T4\_WDCO\_SIZE = 1, BF\_T4\_WDCO\_MASK = 0x08, BF\_T4\_-  
 WDCO\_LSB = 3,  
 BF\_T4\_OPERATING\_MODE\_SIZE = 3, BF\_T4\_OPERATING\_MODE\_MASK = 0x07, BF\_T4\_OPERATIN-  
 G\_MODE\_LSB = 0, BF\_T0\_APLL\_PATH\_SIZE = 4,  
 BF\_T0\_APLL\_PATH\_MASK = 0xF0, BF\_T0\_APLL\_PATH\_LSB = 4, BF\_T0\_GSM\_OBSAI\_16E1\_16T1\_SE-  
 L\_SIZE = 2, BF\_T0\_GSM\_OBSAI\_16E1\_16T1\_SEL\_MASK = 0x0C,  
 BF\_T0\_GSM\_OBSAI\_16E1\_16T1\_SEL\_LSB = 2, BF\_T0\_12E1\_GPS\_E3\_T3\_SEL\_SIZE = 2, BF\_T0\_12-  
 E1\_GPS\_E3\_T3\_SEL\_MASK = 0x03, BF\_T0\_12E1\_GPS\_E3\_T3\_SEL\_LSB = 0,  
 BF\_T0\_DPLL\_START\_DAMPING\_SIZE = 3, BF\_T0\_DPLL\_START\_DAMPING\_MASK = 0xE0, BF\_T0\_D-  
 PLL\_START\_DAMPING\_LSB = 5, BF\_T0\_DPLL\_START\_BW\_SIZE = 5,  
 BF\_T0\_DPLL\_START\_BW\_MASK = 0x1F, BF\_T0\_DPLL\_START\_BW\_LSB = 0, BF\_T0\_DPLL\_ACQ\_DAM-  
 PING\_SIZE = 3, BF\_T0\_DPLL\_ACQ\_DAMPING\_MASK = 0xE0,  
 BF\_T0\_DPLL\_ACQ\_DAMPING\_LSB = 5, BF\_T0\_DPLL\_ACQ\_BW\_SIZE = 5, BF\_T0\_DPLL\_ACQ\_BW\_M-  
 ASK = 0x1F, BF\_T0\_DPLL\_ACQ\_BW\_LSB = 0,  
 BF\_T0\_DPLL\_LOCKED\_DAMPING\_SIZE = 3, BF\_T0\_DPLL\_LOCKED\_DAMPING\_MASK = 0xE0, BF\_T0\_-  
 DPLL\_LOCKED\_DAMPING\_LSB = 5, BF\_T0\_DPLL\_LOCKED\_BW\_SIZE = 5,  
 BF\_T0\_DPLL\_LOCKED\_BW\_MASK = 0x1F, BF\_T0\_DPLL\_LOCKED\_BW\_LSB = 0, BF\_AUTO\_BW\_SEL\_-  
 SIZE = 1, BF\_AUTO\_BW\_SEL\_MASK = 0x80,  
 BF\_AUTO\_BW\_SEL\_LSB = 7, BF\_T0\_LIMIT\_SIZE = 1, BF\_T0\_LIMIT\_MASK = 0x08, BF\_T0\_LIMIT\_LSB =  
 3,  
 BF\_COARSE\_PH\_LOS\_LIMT\_EN\_SIZE = 1, BF\_COARSE\_PH\_LOS\_LIMT\_EN\_MASK = 0x80, BF\_COA-  
 RSE\_PH\_LOS\_LIMT\_EN\_LSB = 7, BF\_WIDE\_EN\_SIZE = 1,  
 BF\_WIDE\_EN\_MASK = 0x40, BF\_WIDE\_EN\_LSB = 6, BF\_MULTI\_PH\_APP\_SIZE = 1, BF\_MULTI\_PH\_A-  
 PP\_MASK = 0x20,  
 BF\_MULTI\_PH\_APP\_LSB = 5, BF\_MULTI\_PH\_8K\_4K\_2K\_EN\_SIZE = 1, BF\_MULTI\_PH\_8K\_4K\_2K\_EN-  
 MASK = 0x10, BF\_MULTI\_PH\_8K\_4K\_2K\_EN\_LSB = 4,  
 BF\_PH\_LOS\_COARSE\_LIMT\_SIZE = 4, BF\_PH\_LOS\_COARSE\_LIMT\_MASK = 0x0F, BF\_PH\_LOS\_COA-  
 RSE\_LIMT\_LSB = 0, BF\_FINE\_PH\_LOS\_LIMT\_EN\_SIZE = 1,  
 BF\_FINE\_PH\_LOS\_LIMT\_EN\_MASK = 0x80, BF\_FINE\_PH\_LOS\_LIMT\_EN\_LSB = 7, BF\_FAST\_LOS\_S-  
 W\_SIZE = 1, BF\_FAST\_LOS\_SW\_MASK = 0x40,  
 BF\_FAST\_LOS\_SW\_LSB = 6, BF\_PH\_LOS\_FINE\_LIMT\_SIZE = 3, BF\_PH\_LOS\_FINE\_LIMT\_MASK =  
 0x07, BF\_PH\_LOS\_FINE\_LIMT\_LSB = 0,  
 BF\_MAN\_HOLDOVER\_SIZE = 1, BF\_MAN\_HOLDOVER\_MASK = 0x80, BF\_MAN\_HOLDOVER\_LSB = 7,

```

BF_AUTO_AVG_SIZE = 1,
BF_AUTO_AVG_MASK = 0x40, BF_AUTO_AVG_LSB = 6, BF_FAST_AVG_SIZE = 1, BF_FAST_AVG_M-
ASK = 0x20,
BF_FAST_AVG_LSB = 5, BF_READ_AVG_SIZE = 1, BF_READ_AVG_MASK = 0x10, BF_READ_AVG_L-
SB = 4,
BF_TEMP_HOLD OVER_MODE_SIZE = 2, BF_TEMP_HOLD OVER_MODE_MASK = 0x0C, BF_TEMP_H-
OLD OVER_MODE_LSB = 2, BF_HOLD OVER_FREQ_A_SIZE = 8,
BF_HOLD OVER_FREQ_A_MASK = 0xFF, BF_HOLD OVER_FREQ_A_LSB = 0, BF_HOLD OVER_FREQ_-
B_SIZE = 8, BF_HOLD OVER_FREQ_B_MASK = 0xFF,
BF_HOLD OVER_FREQ_B_LSB = 0, BF_HOLD OVER_FREQ_C_SIZE = 8, BF_HOLD OVER_FREQ_C_M-
ASK = 0xFF, BF_HOLD OVER_FREQ_C_LSB = 0,
BF_T4_APLL_PATH_SIZE = 4, BF_T4_APLL_PATH_MASK = 0xF0, BF_T4_APLL_PATH_LSB = 4, BF_-
T4_GSM_OBSAI_16E1_16T1_SEL_SIZE = 2,
BF_T4_GSM_OBSAI_16E1_16T1_SEL_MASK = 0x0C, BF_T4_GSM_OBSAI_16E1_16T1_SEL_LSB = 2,
BF_T4_12E1_GPS_E3_T3_SEL_SIZE = 2, BF_T4_12E1_GPS_E3_T3_SEL_MASK = 0x03,
BF_T4_12E1_GPS_E3_T3_SEL_LSB = 0, BF_T4_DPLL_LOCKED_DAMPING_SIZE = 3, BF_T4_DPLL_L-
OCKED_DAMPING_MASK = 0xE0, BF_T4_DPLL_LOCKED_DAMPING_LSB = 5,
BF_T4_DPLL_LOCKED_BW_SIZE = 2, BF_T4_DPLL_LOCKED_BW_MASK = 0x03, BF_T4_DPLL_LOCK-
ED_BW_LSB = 0, BF_CURRENT_DPLL_FREQ_A_SIZE = 8,
BF_CURRENT_DPLL_FREQ_A_MASK = 0xFF, BF_CURRENT_DPLL_FREQ_A_LSB = 0, BF_CURRENT-
_DPLL_FREQ_B_SIZE = 8, BF_CURRENT_DPLL_FREQ_B_MASK = 0xFF,
BF_CURRENT_DPLL_FREQ_B_LSB = 0, BF_CURRENT_DPLL_FREQ_C_SIZE = 8, BF_CURRENT_DP-
LL_FREQ_C_MASK = 0xFF, BF_CURRENT_DPLL_FREQ_C_LSB = 0,
BF_FREQ_LIMT_PH_LOS_SIZE = 1, BF_FREQ_LIMT_PH_LOS_MASK = 0x80, BF_FREQ_LIMT_PH_LO-
S_LSB = 7, BF_DPLL_FREQ_SOFT_LIMT_SIZE = 7,
BF_DPLL_FREQ_SOFT_LIMT_MASK = 0x7F, BF_DPLL_FREQ_SOFT_LIMT_LSB = 0, BF_DPLL_FREQ_-
HARD_LIMT_A_SIZE = 8, BF_DPLL_FREQ_HARD_LIMT_A_MASK = 0xFF,
BF_DPLL_FREQ_HARD_LIMT_A_LSB = 0, BF_DPLL_FREQ_HARD_LIMT_B_SIZE = 8, BF_DPLL_FRE-
Q_HARD_LIMT_B_MASK = 0xFF, BF_DPLL_FREQ_HARD_LIMT_B_LSB = 0,
BF_CURRENT_PH_DATA_A_SIZE = 8, BF_CURRENT_PH_DATA_A_MASK = 0xFF, BF_CURRENT_PH-
_DATA_A_LSB = 0, BF_CURRENT_PH_DATA_B_SIZE = 8,
BF_CURRENT_PH_DATA_B_MASK = 0xFF, BF_CURRENT_PH_DATA_B_LSB = 0, BF_OUT1_PATH_S-
EL_SIZE = 4, BF_OUT1_PATH_SEL_MASK = 0xF0,
BF_OUT1_PATH_SEL_LSB = 4, BF_OUT1_DIVIDER_SIZE = 4, BF_OUT1_DIVIDER_MASK = 0x0F, BF_-
OUT1_DIVIDER_LSB = 0,
BF_OUT2_PATH_SEL_SIZE = 4, BF_OUT2_PATH_SEL_MASK = 0xF0, BF_OUT2_PATH_SEL_LSB = 4,
BF_OUT2_DIVIDER_SIZE = 4,
BF_OUT2_DIVIDER_MASK = 0x0F, BF_OUT2_DIVIDER_LSB = 0, BF_OUT3_PATH_SEL_SIZE = 4, BF_-
OUT3_PATH_SEL_MASK = 0xF0,
BF_OUT3_PATH_SEL_LSB = 4, BF_OUT3_DIVIDER_SIZE = 4, BF_OUT3_DIVIDER_MASK = 0x0F, BF_-
OUT3_DIVIDER_LSB = 0,
BF_OUT4_PATH_SEL_SIZE = 4, BF_OUT4_PATH_SEL_MASK = 0xF0, BF_OUT4_PATH_SEL_LSB = 4,
BF_OUT4_DIVIDER_SIZE = 4,
BF_OUT4_DIVIDER_MASK = 0x0F, BF_OUT4_DIVIDER_LSB = 0, BF_OUT5_PATH_SEL_SIZE = 4, BF_-
OUT5_PATH_SEL_MASK = 0xF0,
BF_OUT5_PATH_SEL_LSB = 4, BF_OUT5_DIVIDER_SIZE = 4, BF_OUT5_DIVIDER_MASK = 0x0F, BF_-
OUT5_DIVIDER_LSB = 0,
BF_OUT6_PATH_SEL_SIZE = 4, BF_OUT6_PATH_SEL_MASK = 0xF0, BF_OUT6_PATH_SEL_LSB = 4,
BF_OUT6_DIVIDER_SIZE = 4,
BF_OUT6_DIVIDER_MASK = 0x0F, BF_OUT6_DIVIDER_LSB = 0, BF_OUT7_PATH_SEL_SIZE = 4, BF_-
OUT7_PATH_SEL_MASK = 0xF0,
BF_OUT7_PATH_SEL_LSB = 4, BF_OUT7_DIVIDER_SIZE = 4, BF_OUT7_DIVIDER_MASK = 0x0F, BF_-
OUT7_DIVIDER_LSB = 0,
BF_OUT8_PATH_SEL_SIZE = 1, BF_OUT8_PATH_SEL_MASK = 0x80, BF_OUT8_PATH_SEL_LSB = 7,
BF_OUT8_EN_SIZE = 1,
BF_OUT8_EN_MASK = 0x40, BF_OUT8_EN_LSB = 6, BF_T4_INPUT_FAIL_SIZE = 1, BF_T4_INPUT_FA-
IL_MASK = 0x20,
BF_T4_INPUT_FAIL_LSB = 5, BF_AMI_OUT_DUTY_SIZE = 1, BF_AMI_OUT_DUTY_MASK = 0x10, BF_-

```

```

AMI_OUT_DUTY_LSB = 4,
BF_400HZ_OUT_SEL_SIZE = 1, BF_400HZ_OUT_SEL_MASK = 0x08, BF_400HZ_OUT_SEL_LSB = 3,
BF_OUT9_INV_SIZE = 1,
BF_OUT9_INV_MASK = 0x04, BF_OUT9_INV_LSB = 2, BF_OUT7_INV_SIZE = 1, BF_OUT7_INV_MASK
= 0x02,
BF_OUT7_INV_LSB = 1, BF_OUT6_INV_SIZE = 1, BF_OUT6_INV_MASK = 0x01, BF_OUT6_INV_LSB =
0,
BF_OUT9_PATH_SEL_SIZE = 1, BF_OUT9_PATH_SEL_MASK = 0x80, BF_OUT9_PATH_SEL_LSB = 7,
BF_OUT9_EN_SIZE = 1,
BF_OUT9_EN_MASK = 0x40, BF_OUT9_EN_LSB = 6, BF_OUT5_INV_SIZE = 1, BF_OUT5_INV_MASK =
0x10,
BF_OUT5_INV_LSB = 4, BF_OUT4_INV_SIZE = 1, BF_OUT4_INV_MASK = 0x08, BF_OUT4_INV_LSB =
3,
BF_OUT3_INV_SIZE = 1, BF_OUT3_INV_MASK = 0x04, BF_OUT3_INV_LSB = 2, BF_OUT2_INV_SIZE =
1,
BF_OUT2_INV_MASK = 0x02, BF_OUT2_INV_LSB = 1, BF_OUT1_INV_SIZE = 1, BF_OUT1_INV_MASK
= 0x01,
BF_OUT1_INV_LSB = 0, BF_IN_2K_4K_8K_INV_SIZE = 1, BF_IN_2K_4K_8K_INV_MASK = 0x80, BF_IN-
_2K_4K_8K_INV_LSB = 7,
BF_8K_EN_SIZE = 1, BF_8K_EN_MASK = 0x40, BF_8K_EN_LSB = 6, BF_2K_EN_SIZE = 1,
BF_2K_EN_MASK = 0x20, BF_2K_EN_LSB = 5, BF_2K_8K_PUL_POSITION_SIZE = 1, BF_2K_8K_PUL_-
POSITION_MASK = 0x10,
BF_2K_8K_PUL_POSITION_LSB = 4, BF_8K_INV_SIZE = 1, BF_8K_INV_MASK = 0x08, BF_8K_INV_LSB
= 3,
BF_8K_PUL_SIZE = 1, BF_8K_PUL_MASK = 0x04, BF_8K_PUL_LSB = 2, BF_2K_INV_SIZE = 1,
BF_2K_INV_MASK = 0x02, BF_2K_INV_LSB = 1, BF_2K_PUL_SIZE = 1, BF_2K_PUL_MASK = 0x01,
BF_2K_PUL_LSB = 0, BF_IN_NOISE_WINDOW_SIZE = 1, BF_IN_NOISE_WINDOW_MASK = 0x80, BF_I-
N_NOISE_WINDOW_LSB = 7,
BF_PH_OFFSET_A_SIZE = 8, BF_PH_OFFSET_A_MASK = 0xFF, BF_PH_OFFSET_A_LSB = 0, BF_PH_-
OFFSET_EN_SIZE = 1,
BF_PH_OFFSET_EN_MASK = 0x80, BF_PH_OFFSET_EN_LSB = 7, BF_PH_OFFSET_B_SIZE = 2, BF_-
PH_OFFSET_B_MASK = 0x03,
BF_PH_OFFSET_B_LSB = 0, BF_SYNC_BYPASS_SIZE = 1, BF_SYNC_BYPASS_MASK = 0x80, BF_SY-
NC_BYPASS_LSB = 7,
BF_SYNC_MON_LIMT_SIZE = 3, BF_SYNC_MON_LIMT_MASK = 0x70, BF_SYNC_MON_LIMT_LSB = 4,
BF_SYNC_EDGE_SIZE = 1,
BF_SYNC_EDGE_MASK = 0x40, BF_SYNC_EDGE_LSB = 6, BF_SYNC_PH2_SIZE = 2, BF_SYNC_PH2-
_MASK = 0x0C,
BF_SYNC_PH2_LSB = 2, BF_SYNC_PH1_SIZE = 2, BF_SYNC_PH1_MASK = 0x03, BF_SYNC_PH1_LSB
= 0,
BF_PROTECTION_DATA_SIZE = 8, BF_PROTECTION_DATA_MASK = 0xFF, BF_PROTECTION_DATA-
_LSB = 0, BF_MPU_SEL_CNFG_SIZE = 3,
BF_MPU_SEL_CNFG_MASK = 0x07, BF_MPU_SEL_CNFG_LSB = 0, BF_T0_DFS_OFF_3_SIZE = 1,
BF_T0_DFS_OFF_3_MASK = 0x80,
BF_T0_DFS_OFF_3_LSB = 7, BF_T0_DFS_OFF_2_SIZE = 1, BF_T0_DFS_OFF_2_MASK = 0x40, BF_-
T0_DFS_OFF_2_LSB = 6,
BF_T0_DFS_OFF_1_SIZE = 1, BF_T0_DFS_OFF_1_MASK = 0x20, BF_T0_DFS_OFF_1_LSB = 5, BF_-
T0_DFS_OFF_0_SIZE = 1,
BF_T0_DFS_OFF_0_MASK = 0x10, BF_T0_DFS_OFF_0_LSB = 4, BF_T4_DFS_OFF_3_SIZE = 1, BF_-
T4_DFS_OFF_3_MASK = 0x08,
BF_T4_DFS_OFF_3_LSB = 3, BF_T4_DFS_OFF_2_SIZE = 1, BF_T4_DFS_OFF_2_MASK = 0x04, BF_-
T4_DFS_OFF_2_LSB = 2,
BF_T4_DFS_OFF_1_SIZE = 1, BF_T4_DFS_OFF_1_MASK = 0x02, BF_T4_DFS_OFF_1_LSB = 1, BF_-
T4_DFS_OFF_0_SIZE = 1,
BF_T4_DFS_OFF_0_MASK = 0x01, BF_T4_DFS_OFF_0_LSB = 0, BF_PPS_PHASE_SIZE = 2, BF_PPS-
_PHASE_MASK = 0x30,
BF_PPS_PHASE_LSB = 4, BF_PPS_PULSE_SIZE = 4, BF_PPS_PULSE_MASK = 0x0F, BF_PPS_PULS-

```

```

E_LSB = 0,
BF_T0_PH_SLOPE_SIZE = 2, BF_T0_PH_SLOPE_MASK = 0x0C, BF_T0_PH_SLOPE_LSB = 2, BF_T4_
PH_SLOPE_SIZE = 2,
BF_T4_PH_SLOPE_MASK = 0x03, BF_T4_PH_SLOPE_LSB = 0, BF_ICP_CTRL_CODE_SIZE = 5, BF_IC
P_CTRL_CODE_MASK = 0x1F,
BF_ICP_CTRL_CODE_LSB = 0, REGMAP_MAX }

```

*Enumerated type listing register offsets and bit field constants.*

### 6.40.1 Detailed Description

This header file contains register and bitfield information for accessing device.

#### See Also

Datasheet for detailed register descriptions.

Definition in file [RegisterDef.h](#).

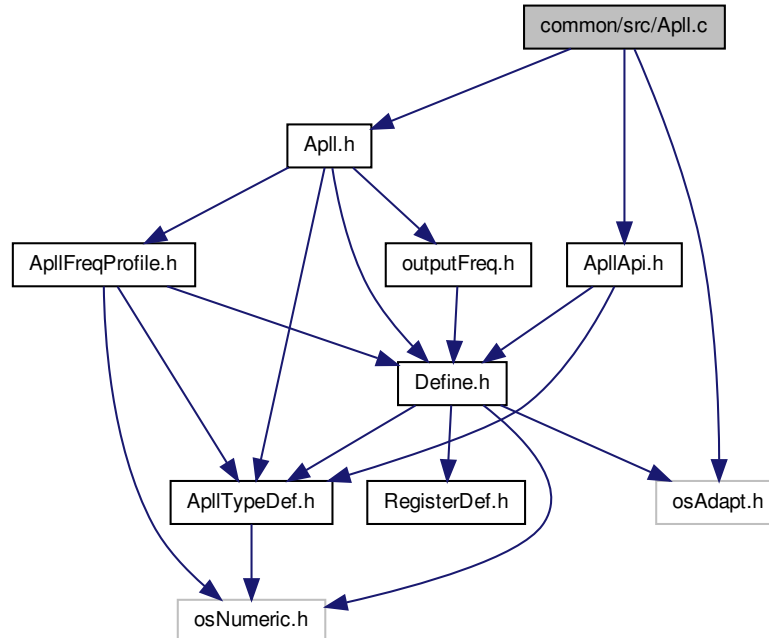
## 6.41 common/src/Apl.c File Reference

```

#include "Apl1.h"
#include "Apl1Api.h"
#include "osAdapt.h"

```

Include dependency graph for Apl.c:



### Functions

- void [IDTApl\\_SetAplConfigPerOutput](#) (T\_idtDrvHdlr hdlr, T\_idtAplId aplInstId, T\_idtAplOutput output, T\_idtAplConfigPerOutput \*aplConfigPerOutput)



*Set APLL per output configuration.*

- void `IDTApll_GetApllConfigPerOutput` (`T_idtDrvHdlr` hdlr, `T_idtApllId` appllInstId, `T_idtApllOutput` output, `T_idtApllConfigPerOutput` \*appllConfigPerOutput)

*Get APLL per output configuration.*

- void `IDTApll_SetApllConfig` (`T_idtDrvHdlr` hdlr, `T_idtApllId` appllInstId, `T_idtApllConfig` \*appllConfig)

*Set APLL full configuration.*

- void `IDTApll_GetApllConfig` (`T_idtDrvHdlr` hdlr, `T_idtApllId` appllInstId, `T_idtApllConfig` \*appllConfig)

*Get APLL full configuration.*

- `outputFrequency_t` `IDTApll_ApllInput2DpllOutput` (`T_idtApllInputFreqType` appllInputFreq)

*Translate APLL input frequency to DPLL output frequency.*

- `T_idtApllOutputFreqType` `IDTApll_DpllOutput2ApllOutput` (`outputFrequency_t` dpllOutput)

*Translate DPLL output frequency to APLL output frequency.*

- const `T_idtApllFreqMapping` \* `IDTApll_GetApllFreqTableEntry` (`T_idtDrvHdlr` hdlr, `T_idtOutputApllConfig` outputApll, `outputFrequency_t` nOutFreq)

*Get APLL frequency configuration table entry based on the output frequency.*

- `T_idtApllConfigSel` `IDTApll_GetNonActiveApllConfig` (`T_idtDrvHdlr` hdlr, `T_idtApllId` appllInst)

*Get non-active APLL configuration.*

- void `IDTApll_Switch2NonActiveApllConfig` (`T_idtDrvHdlr` hdlr, `T_idtApllId` appllId)

*Switch to non-active APLL configuration.*

- `T_idtApllXtalId` `IDTApll_GetXtalIdFromXtalFreq` (`T_idtDrvHdlr` hdlr, `T_idtApllId` appllInst, `T_idtApllXtalType` appllVcxoFreq)

*Get APLL configured crystal ID from crystal frequency.*

- `T_osBool` `IDTApll_XtalConfigured` (`T_idtDrvHdlr` hdlr, `T_idtApllId` appllId)

*Checks if there is any XTAL configured for the APLL.*

- `T_osBool` `IDTApll_ValidXtalInput` (const `T_idtDrvDeviceConfig` \*deviceConfig, `T_idtApllXtal` \*xtalList, `T_osUInt8` numberOfXtal)

*Checks if there is input XTAL information is valid for the device.*

- `T_idtApllXtal` \* `IDTApll_GetSupportedXtal` (const `T_idtDrvDeviceConfig` \*deviceConfig, `T_osUInt8` \*numberOfXtal)

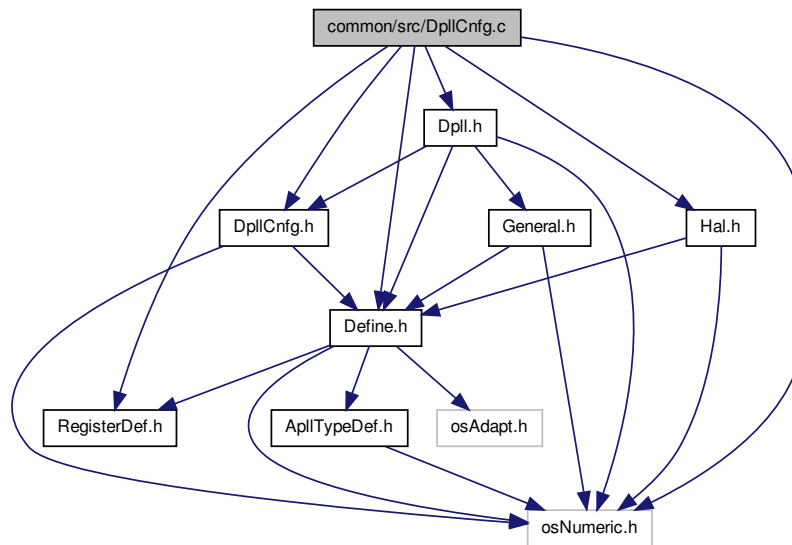
*Return supported xtal configuration by the device.*

## 6.42 common/src/DpllCnfg.c File Reference

```
#include "osNumeric.h"
#include "Define.h"
#include "Hal.h"
#include "DpllCnfg.h"
#include "RegisterDef.h"
#include "Dpll.h"
```



Include dependency graph for DpllCnfg.c:



## Data Structures

- struct [T\\_idtSonetGigEthBitfield2PathConfig](#)  
Structure Translate from Sonet/GigE bitfield to path configuration.

## Macros

- #define [INVALID\\_REGISTER\\_OFFSET](#) ((T\_osUInt8)(-1))  
Tag used to indicating invalid register offset.

## Functions

- [T\\_idtDpllType IDTDpll\\_GetTypeOfDpll](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
Function to determine type of DPLL give a DPLL instance.
- void [IDTDpll\\_SetAutoSelInput](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_osUInt8 mode)  
Set the DPLL as automatic reference clock selection.
- T\_osUInt8 [IDTDpll\\_GetAutoSelInput](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
Get automatic input selection status.
- void [IDTDpll\\_SetForceSelInput](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_osUInt8 nInputNo)  
Set the DPLL to force to lock to a specified reference clock.
- T\_osUInt8 [IDTDpll\\_GetForceSelInput](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
Set the DPLL to force to lock to a specified reference clock.
- T\_osUInt8 [IDTDpll\\_Get1stPriorityInput](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
Get input number of a valid clock with the highest priority.
- T\_osUInt8 [IDTDpll\\_Get2ndPriorityInput](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
Get input number of a valid clock with the second highest priority.
- T\_osUInt8 [IDTDpll\\_Get3rdPriorityInput](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
Get input number of a valid clock with the third highest priority.

- `T_osUInt8 IDTDpll_GetCurrentSelectInput` (`T_idtDrvHdlr hdlr`, `T_idtDpllInstance nDpll`)  
*Get the current selected input clock.*
- `void IDTDpll_SetDpllOperMod` (`T_idtDrvHdlr hdlr`, `T_idtDpllInstance nDpll`, `T_idtDpllOperMode nMode`)  
*Set DPLL working at the specified operating mode.*
- `T_idtDpllOperMode IDTDpll_GetDpllOperMod` (`T_idtDrvHdlr hdlr`, `T_idtDpllInstance nDpll`)  
*Set DPLL working at the specified operating mode.*
- `T_osUInt8 IDTDpll_IsDpllLocked` (`T_idtDrvHdlr hdlr`, `T_idtDpllInstance nDpll`)  
*Inquire if the DPLL is in lock state.*
- `void IDTDpll_SetBandWidthDamping` (`T_idtDrvHdlr hdlr`, `T_idtDpllInstance nDpll`, `T_idtBandwidthLimitStage stage`, `T_idtDpllBandwidth nBandWidth`, `T_idtDampingFactor nDamping`)  
*Set the bandwidth and damping factor used for bandwidth limiting.*
- `void IDTDpll_GetBandWidthDamping` (`T_idtDrvHdlr hdlr`, `T_idtDpllInstance nDpll`, `T_idtBandwidthLimitStage stage`, `T_idtDpllBandwidth *nBandWidth_p`, `T_idtDampingFactor *nDamping_p`)  
*Get configured bandwidth and damping factor for bandwidth limiting.*
- `void IDTDpll_SetAutoSelBandWidth` (`T_idtDrvHdlr hdlr`, `T_idtDpllInstance nDpll`, `T_osUInt8 nEnable`)  
*Set device to select a suitable bandwidth and damping factor automatically.*
- `T_osUInt8 IDTDpll_GetAutoSelBandWidth` (`T_idtDrvHdlr hdlr`, `T_idtDpllInstance nDpll`)  
*Get auto bandwidth/damping factor status automatically.*
- `void IDTDpll_SetDpllFrozen` (`T_idtDrvHdlr hdlr`, `T_idtDpllInstance nDpll`, `T_osUInt8 nEnable`)  
*Set DPLL integral path value frozen.*
- `T_osUInt8 IDTDpll_GetDpllFrozen` (`T_idtDrvHdlr hdlr`, `T_idtDpllInstance nDpll`)  
*Get DPLL integral path value frozen.*
- `void IDTDpll_SetPhaseCoarseDetector` (`T_idtDrvHdlr hdlr`, `T_idtDpllInstance nDpll`, `T_osUInt8 nEnable`, `T_osUInt8 nWide`, `T_osUInt8 nMultiPhase`, `T_osUInt8 nMultiPh8kEn`)  
*Set the coarse phase lose detector enable.*
- `void IDTDpll_GetPhaseCoarseDetector` (`T_idtDrvHdlr hdlr`, `T_idtDpllInstance nDpll`, `T_osUInt8 *nEnable_p`, `T_osUInt8 *nWide_p`, `T_osUInt8 *nMultiPhase_p`, `T_osUInt8 *nMultiPh8kEn_p`)  
*Set the coarse phase lose detector enable.*
- `void IDTDpll_SetPhaseCoarseLimit` (`T_idtDrvHdlr hdlr`, `T_idtDpllInstance nDpll`, `T_idtCoarsePhaseLimit nLimit`)  
*Set the limitation of the coarse phase lose detector.*
- `T_idtCoarsePhaseLimit IDTDpll_GetPhaseCoarseLimit` (`T_idtDrvHdlr hdlr`, `T_idtDpllInstance nDpll`)  
*Get the limitation of the coarse phase lose detector.*
- `void IDTDpll_SetPhaseFineDetectorEnable` (`T_idtDrvHdlr hdlr`, `T_idtDpllInstance nDpll`, `T_osUInt8 nEnable`)  
*Set the fine phase lose detector enable.*
- `T_osUInt8 IDTDpll_GetPhaseFineDetectorEnable` (`T_idtDrvHdlr hdlr`, `T_idtDpllInstance nDpll`)  
*Get the fine phase lose detector enable.*
- `void IDTDpll_SetPhaseFineLimit` (`T_idtDrvHdlr hdlr`, `T_idtDpllInstance nDpll`, `T_idtFinePhaseLimit nLimit`)  
*Set the limitation of the fine phase lose detector.*
- `T_idtFinePhaseLimit IDTDpll_GetPhaseFineLimit` (`T_idtDrvHdlr hdlr`, `T_idtDpllInstance nDpll`)  
*Set the limitation of the fine phase lose detector.*
- `void IDTDpll_SetFastLossSwitch` (`T_idtDrvHdlr hdlr`, `T_osUInt8 nEnable`)  
*Set reference clock switch if a fast loss occurs.*
- `T_osUInt8 IDTDpll_GetFastLossSwitch` (`T_idtDrvHdlr hdlr`)  
*Get reference clock switch if a fast loss occurs.*
- `void IDTDpll_SetHoldoverMode` (`T_idtDrvHdlr hdlr`, `T_idtDpllInstance nDpll`, `T_idtDpllHoldover nMode`, `T_osUInt8 nReadMode`)  
*Set calculation mode of holdover frequency and read back mode.*
- `void IDTDpll_GetHoldoverMode` (`T_idtDrvHdlr hdlr`, `T_idtDpllInstance nDpll`, `T_idtDpllHoldover *nMode_p`, `T_osUInt8 *nReadMode_p`)  
*Get calculation mode of holdover frequency and read back mode.*

- void `IDTDpll_SetTempHoldoverMode` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_idtTemp_holdover` n-Mode)  
*Set calculation mode of temporary holdover frequency.*
- `T_idtTemp_holdover` `IDTDpll_GetTempHoldoverMode` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)  
*Set calculation mode of temporary holdover frequency.*
- long `IDTDpll_GetHoldoverFreq` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)  
*Get holdover frequency offset (in parts per trillion). In DCO mode, this function returns current DCO offset (in parts per trillion).*
- void `IDTDpll_SetHoldoverFreq` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, long pptOffset)  
*Set DCO frequency to device. Note this function should only be called when DCO mode is enabled.*
- long `IDTDpll_GetCurrentDpllFreqOffset` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)  
*Get current frequency offset of DPLL in parts per trillion (PPT)*
- void `IDTDpll_SetDpllSoftAlarmLimit` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_osUInt8` nLimit)  
*Set the limitation of Soft alarm of DPLL.*
- `T_osUInt8` `IDTDpll_GetDpllSoftAlarmLimit` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)  
*Get the limitation of Soft alarm of DPLL.*
- void `IDTDpll_SetDpllHardAlarmLimit` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_osUInt16` nLimit)  
*Set the limitation of Hard alarm of DPLL.*
- `T_osUInt16` `IDTDpll_GetDpllHardAlarmLimit` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)  
*Get the limitation of Hard alarm of DPLL.*
- void `IDTDpll_SetDpllHardAlarmEnable` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nEnable)  
*Set DPLL in unlocked state when a Hard alarm raised.*
- `T_osUInt8` `IDTDpll_GetDpllHardAlarmEnable` (`T_idtDrvHdlr` hdlr)  
*Get DPLL in unlocked state when a Hard alarm raised.*
- `T_osUInt16` `IDTDpll_GetCurrentPhaseError` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)  
*Get the current phase error of DPLL.*
- void `IDTDpll_SetSonetGigEthOutputPath` (`T_idtDrvHdlr` hdlr, `T_osUInt8` instance, `T_idtDpllInstance` inputDpll, `T_idtSonetGigEthOutput` outputFreq)  
*Set Sonet/GigE path configuration.*
- void `IDTDpll_GetSonetGigEthOutputPath` (`T_idtDrvHdlr` hdlr, `T_osUInt8` instance, `T_idtDpllInstance` \*inputDpll\_p, `T_idtSonetGigEthOutput` \*outputFreq\_p)  
*Retrieve Sonet/GigE path configuration.*
- void `IDTDpll_SetDpllOutputPathSelectorA` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_idtDpllOutputSelectorA` path)  
*Set DPLL output path selector A.*
- `T_idtDpllOutputSelectorA` `IDTDpll_GetDpllOutputPathSelectorA` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)  
*Get DPLL output path selector A.*
- void `IDTDpll_SetDpllOutputPathSelectorB` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_idtDpllOutputSelectorB` path)  
*Set DPLL output path selector B.*
- `T_idtDpllOutputSelectorB` `IDTDpll_GetDpllOutputPathSelectorB` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)  
*Get DPLL output path selector B.*
- void `IDTDpll_SetDpllEthPathEnable` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_osUInt8` nDisable)  
*Set ETH Enable/Disable.*
- `T_osUInt8` `IDTDpll_GetDpllEthPathEnable` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)  
*Get ETH Enable/Disable.*
- void `IDTDpll_SetDpllSelBPathEnable` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll, `T_osUInt8` nDisable)  
*Set DPLL output path selector B Enable/Disable.*
- `T_osUInt8` `IDTDpll_GetDpllSelBPathEnable` (`T_idtDrvHdlr` hdlr, `T_idtDpllInstance` nDpll)  
*Get DPLL output path selector B Enable/Disable.*

- void [IDTDpll\\_SetDpll16E116T1Enable](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_osUInt8 nDisable)  
*Set 16E1/16T1 Enable/Disable.*
- T\_osUInt8 [IDTDpll\\_GetDpll16E116T1Enable](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Get 16E1/16T1 Enable/Disable.*
- void [IDTDpll\\_SetDpllSelAPathEnable](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_osUInt8 nDisable)  
*Set DPLL output path selector A Enable/Disable.*
- T\_osUInt8 [IDTDpll\\_GetDpllSelAPathEnable](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Set DPLL output path selector A Enable/Disable.*
- void [IDTDpll\\_SetFrequencyMonitoringFactor](#) (T\_idtDrvHdlr hdlr, T\_idtFreqMonFactor freqMonFactor)  
*Function to set the frequency monitoring factor. Hard and soft alarm thresholds use this factor as their base unit.*
- T\_idtFreqMonFactor [IDTDpll\\_GetFrequencyMonitoringFactor](#) (T\_idtDrvHdlr hdlr)  
*Function to get the frequency monitoring factor. Hard and soft alarm thresholds use this factor as their base unit.*
- void [IDTDpll\\_SetHardAlarmThreshold](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 accepting, T\_osUInt8 rejecting)  
*Set the frequency hard alarm accepting thresholds of reference clock monitoring.*
- void [IDTDpll\\_GetHardAlarmThreshold](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 \*accepting\_p, T\_osUInt8 \*rejecting\_p)  
*Get the frequency hard alarm accepting thresholds of reference clock monitoring.*
- void [IDTDpll\\_SetSoftAlarmThreshold](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 accepting, T\_osUInt8 rejecting)  
*Set the frequency soft alarm accepting thresholds of reference clock monitoring.*
- void [IDTDpll\\_GetSoftAlarmThreshold](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 \*accepting\_p, T\_osUInt8 \*rejecting\_p)  
*Get the frequency soft alarm accepting thresholds of reference clock monitoring.*
- void [IDTDpll\\_SetIcpCtrl](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_osUInt8 nlcp)  
*Set charge pump control.*
- T\_osUInt8 [IDTDpll\\_GetIcpCtrl](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Get charge pump control.*
- void [IDTDpll\\_SetPhaseSlope](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_idtPhaseSlope nPhaseSlope)  
*Set DPLL phase slope for DPLLs.*
- T\_idtPhaseSlope [IDTDpll\\_GetPhaseSlope](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll)  
*Get DPLL phase slope for DPLLs.*
- void [IDTDpll\\_SetPpsFastLock](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nEnableFreq, T\_osUInt8 nEnablePhase)  
*Enable/Disable 1 PPS fast lock.*
- void [IDTDpll\\_GetPpsFastLock](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 \*nEnableFreq\_p, T\_osUInt8 \*nEnablePhase\_p)  
*Get enable/disable 1 PPS fast lock status.*
- void [IDTDpll\\_SetPhaseTransient](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nEnable)  
*Set the configuration when phase transient occurs.*
- T\_osUInt8 [IDTDpll\\_GetPhaseTransient](#) (T\_idtDrvHdlr hdlr)  
*Get the configuration when phase transient occurs.*
- void [IDTDpll\\_SetHitlessSwitchingFeature](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nEnable, T\_osUInt8 nFrozen)  
*Set the configuration of hitless switching feature.*
- void [IDTDpll\\_GetHitlessSwitchingFeature](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 \*nEnable\_p, T\_osUInt8 \*nFrozen\_p)  
*Get the configuration of hitless switching feature.*
- void [IDTDpll\\_SetPhaseOffset](#) (T\_idtDrvHdlr hdlr, T\_osUInt16 nOffset)  
*Set the phase offset value.*
- T\_osUInt16 [IDTDpll\\_GetPhaseOffset](#) (T\_idtDrvHdlr hdlr)  
*Get the phase offset value.*
- void [IDTDpll\\_SetPpsPhase](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_idtDpllPpsPhasePostion nPhase, T\_idtDpllPpsPulseWidth nPulse)  
*Set PPS phase and pulse for DPLL.*
- void [IDTDpll\\_GetPpsPhase](#) (T\_idtDrvHdlr hdlr, T\_idtDpllInstance nDpll, T\_idtDpllPpsPhasePostion \*nPhase\_p, T\_idtDpllPpsPulseWidth \*nPulse\_p)  
*Get PPS phase and pulse for DPLL.*

## Variables

- const [T\\_IDTPathConfiguration](#) [IDTDpll\\_pathConfigurationNULL\\_c](#)  
*Invalid output path configuration.*
- const [T\\_osUInt8](#) [IDTDpll\\_bandwidthLimitRegisters\\_a](#) [[Dpll\\_MAX](#)][[dpllBandwidthLimit\\_MAX](#)]  
*Structure used to determine which register to access for bandwidth limiting.*
- const [T\\_idtSonetGigEthSelector](#) [IDTDpll\\_sonetGigEthPathConfig2Bitfield](#) [[Dpll\\_MAX](#)][[SonetGigEthOutput\\_MAX](#)]  
*Table to translate from Sonet/GigE path configuration to bitfield value.*

### 6.42.1 Macro Definition Documentation

#### 6.42.1.1 #define INVALID\_REGISTER\_OFFSET ((T\_osUInt8)(-1))

Tag used to indicating invalid register offset.

Definition at line 46 of file `DpllCnfg.c`.

### 6.42.2 Variable Documentation

#### 6.42.2.1 const T\_osUInt8 IDTDpll\_bandwidthLimitRegisters\_a[Dpll\_MAX][dpllBandwidthLimit\_MAX]

##### Initial value:

```
=
{
    {
        REG_T0_DPLL_START_BW_DAMPING_CNFG,
        REG_T0_DPLL_ACQ_BW_DAMPING_CNFG,
        REG_T0_DPLL_LOCKED_BW_DAMPING_CNFG
    },
    {
        INVALID_REGISTER_OFFSET,
        INVALID_REGISTER_OFFSET,
        REG_T4_DPLL_LOCKED_BW_DAMPING_CNFG
    }
}
```

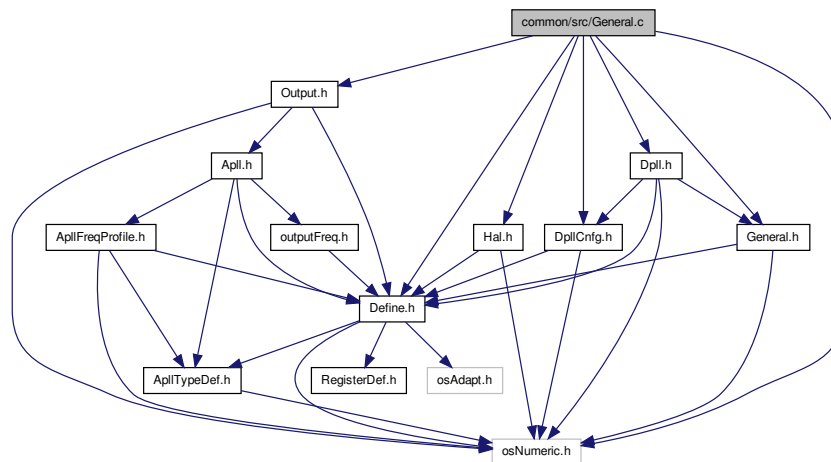
Structure used to determine which register to access for bandwidth limiting.

Definition at line 75 of file `DpllCnfg.c`.

## 6.43 common/src/General.c File Reference

```
#include "osNumeric.h"
#include "Define.h"
#include "Hal.h"
#include "DpllCnfg.h"
#include "Dpll.h"
#include "General.h"
#include "Output.h"
```

Include dependency graph for General.c:



## Functions

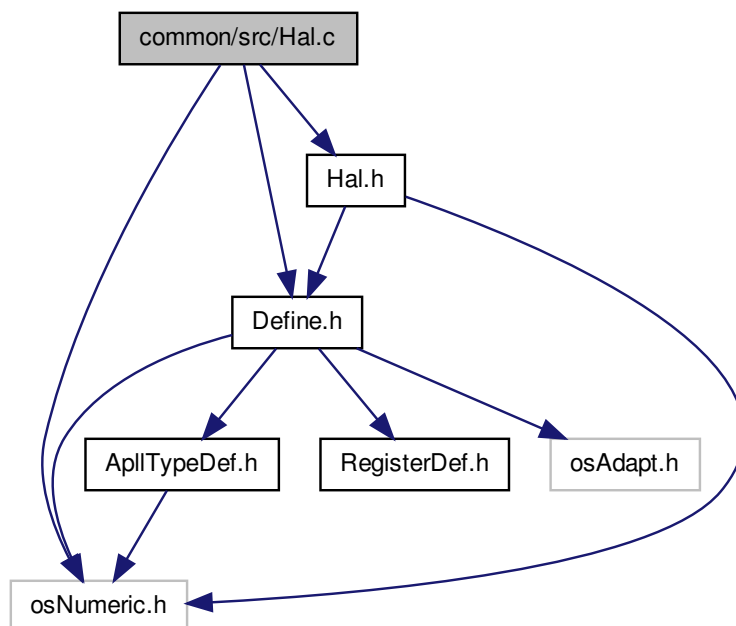
- `T_osUInt16 IDTGeneral_GetDeviceID (T_idtDrvHdlr hdlr)`  
*Get ID number of the device.*
- `void IDTGeneral_SetOscFreqOffset (T_idtDrvHdlr hdlr, long pptOffset)`  
*Set compensation to the oscillator offset.*
- `long IDTGeneral_GetOscFreqOffset (T_idtDrvHdlr hdlr)`  
*Get compensated oscillator offset.*
- `void IDTGeneral_SetNetworkType (T_idtDrvHdlr hdlr, networkType_t nType)`  
*Set the network type, SDH or SONET.*
- `networkType_t IDTGeneral_GetNetworkType (T_idtDrvHdlr hdlr)`  
*Get the network type, SDH or SONET.*
- `void IDTGeneral_SetRevertiveMode (T_idtDrvHdlr hdlr, T_osUInt8 nEnable)`  
*Set the device running in Revertive mode or not.*
- `T_osUInt8 IDTGeneral_GetRevertiveMode (T_idtDrvHdlr hdlr)`  
*Get the device running in Revertive mode or not.*
- `void IDTGeneral_SetTimeoutValue (T_idtDrvHdlr hdlr, phaseTimeoutMultiplier_t nMultiFactor, T_osUInt8 nTimeout)`  
*Set the value of time out of phase alarm  $Timeout(second) = nMultiFactor * nTimeout$ .*
- `void IDTGeneral_GetTimeoutValue (T_idtDrvHdlr hdlr, phaseTimeoutMultiplier_t *nMultiFactor_p, T_osUInt8 *nTimeout_p)`  
*Get the value of time out of phase alarm  $Timeout(second) = nMultiFactor * nTimeout$ .*
- `void IDTGeneral_SetOscActiveEdge (T_idtDrvHdlr hdlr, T_osUInt8 nEdge)`  
*Set the activate edge of main oscillator.*
- `T_osUInt8 IDTGeneral_GetOscActiveEdge (T_idtDrvHdlr hdlr)`  
*Get the activate edge of main oscillator.*
- `void IDTGeneral_SetProtectMode (T_idtDrvHdlr hdlr)`  
*Enable protected register access mode.*
- `void IDTGeneral_SetSingleUnprotectMode (T_idtDrvHdlr hdlr)`  
*Set single access register access mode.*
- `void IDTGeneral_SetFullyUnprotectMode (T_idtDrvHdlr hdlr)`  
*Set fully un-protected register access mode.*

- void `IDTGeneral_SetFlagOnTDO` (`T_idtDrvHdlr hdlr`, `T_osUInt8 nEnable`)  
*Set TDO pin to indicate the fail of selected clock.*
- `T_osUInt8 IDTGeneral_GetFlagOnTDO` (`T_idtDrvHdlr hdlr`)  
*Get TDO pin to indicate the fail of selected clock.*
- void `IDTGeneral_SetUltraFastSwitch` (`T_idtDrvHdlr hdlr`, `T_osUInt8 nEnable`)  
*Set Ultra-fast-switch enable or not.*
- `T_osUInt8 IDTGeneral_GetUltraFastSwitch` (`T_idtDrvHdlr hdlr`)  
*Get Ultra-fast-switch enable or not.*
- void `IDTGeneral_SetHardAlarm` (`T_idtDrvHdlr hdlr`, `T_osUInt8 nEnable`)  
*Set Hard-alarm enable when the input exceeds the threshold.*
- `T_osUInt8 IDTGeneral_GetHardAlarm` (`T_idtDrvHdlr hdlr`)  
*Get Hard-alarm enable when the input exceeds the threshold.*
- `T_osUInt8 IDTGeneral_i2cTranslate` (`T_osUInt8 i2cAddr`, `void *transData`)  
*I2C address translation function used internally by the driver.*
- void `IDTGeneral_InitDeviceCommon` (`T_idtDrvHdlr hdlr`)
- `T_idtDrvHdlr IDTGeneral_InitDriverCommon` (`const char *name`, `T_idtDrvAccess drvAccess`, `T_idtDeviceType deviceType`, `const T_idtDrvDeviceConfig *deviceConfig`, `int useHighLevelApi`)
- void `IDTGeneral_DelInitDriver` (`T_idtDrvHdlr hdlr`)  
*De-initialize driver handler.*

## 6.44 common/src/Hal.c File Reference

```
#include "osNumeric.h"
#include "Define.h"
#include "Hal.h"
```

Include dependency graph for Hal.c:



## Macros

- #define `DEBUG_IDT_HAL`

## Functions

- void `IDTHAL_WriteBitfield` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset, T\_osUInt8 mask, T\_osUInt8 lsb, T\_osUInt8 data)

*Define function to write a bitfield to a device.*

- void `IDTHAL_WriteBitfield_Ext` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset, T\_osUInt8 mask, T\_osUInt8 lsb, T\_osUInt8 data)

*Define function to write a bitfield to a device.*

- T\_osUInt8 `IDTHAL_ReadBitfield` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset, T\_osUInt8 mask, T\_osUInt8 lsb)

*Define function to read a bitfield from device.*

- T\_osUInt8 `IDTHAL_ReadBitfield_Ext` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset, T\_osUInt8 mask, T\_osUInt8 lsb)

*Define function to read a bitfield from device.*

- T\_osUInt8 `IDTHal_Read` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset)

*Function to read from device address space.*

- void `IDTHal_Write` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset, T\_osUInt8 data)

*Function to write to device address space.*

- T\_osUInt8 `IDTHal_Read_Ext` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset)

*Function to read from device apll address space.*

- void `IDTHal_Write_Ext` (T\_idtDrvHdlr hdlr, T\_osUInt8 offset, T\_osUInt8 data)

*Function to write to device apll address space.*

### 6.44.1 Macro Definition Documentation

#### 6.44.1.1 #define `DEBUG_IDT_HAL`

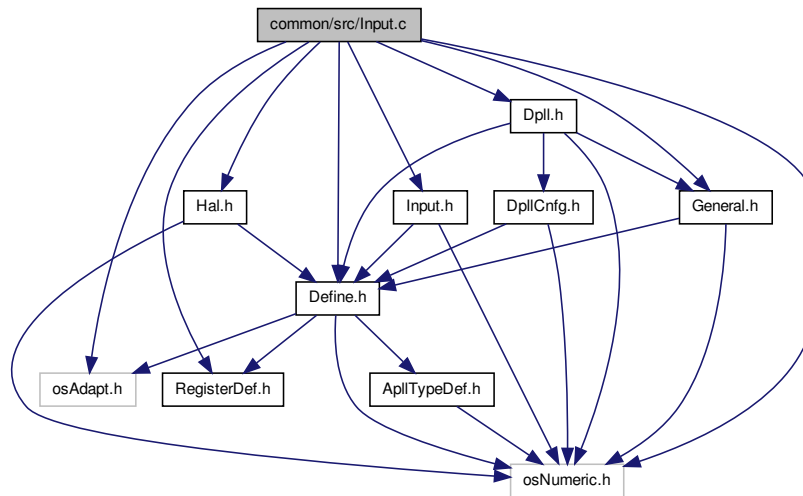
Definition at line 41 of file Hal.c.

## 6.45 common/src/Input.c File Reference

```
#include "osNumeric.h"
#include "osAdapt.h"
#include "Define.h"
#include "Hal.h"
#include "General.h"
#include "Input.h"
#include "Dpll.h"
#include "RegisterDef.h"
```



Include dependency graph for Input.c:



## Data Structures

- struct [bucketReg\\_t](#)  
Structure used to store leaky bucket register offsets.

## Functions

- [T\\_idtInputFrequencyFamily IDTInput\\_InFreqBitValue2Family](#) (T\_idtDrvHdlr hdlr, T\_idtInputFrequencyBitfieldValue inFreqBitValue)  
Translate input frequency bit value to input frequency family.
- void [IDTInput\\_SetPriority](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo, T\_idtDpllInstance nDpll, T\_osUInt8 nPriority)  
Set specified port to the priority.
- T\_osUInt8 [IDTInput\\_GetPriority](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo, T\_idtDpllInstance nDpll)  
Get the current priority of the specified port.
- void [IDTInput\\_SetInputFrequency](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo, T\_idtInputFrequencyBitfieldValue nFrequency)  
Set the frequency of the input clock at the specified port.
- [T\\_idtInputFrequencyBitfieldValue IDTInput\\_GetInputFrequency](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo)  
Get frequency of the input clock at the specified port.
- void [IDTInput\\_SetActivityMonitor](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo, T\_osUInt8 nBucket)  
Select one of the four activity monitor configurations for the specified input port.
- T\_osUInt8 [IDTInput\\_GetActivityMonitor](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo)  
Retrieve selected activity monitoring configuration.
- void [IDTInput\\_SetBucketConfig](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nBucket, T\_osUInt8 nUpper, T\_osUInt8 nLower, T\_osUInt8 nSize, T\_osUInt8 nDecay)  
Set the configuration to Leaky Bucket activity monitoring.
- void [IDTInput\\_GetBucketConfig](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nBucket, T\_osUInt8 \*nUpper\_p, T\_osUInt8 \*nLower\_p, T\_osUInt8 \*nSize\_p, T\_osUInt8 \*nDecay\_p)  
Get activity monitoring configuration (Leaky Bucket)

- void [IDTInput\\_SetPreDivider](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo, [T\\_idtInputDividerMux](#) nDivider)  
*Assign a pre-divider for the specified input.*
- [T\\_idtInputDividerMux IDTInput\\_GetPreDivider](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo)  
*Get configured input port pre-divider.*
- void [IDTInput\\_SetDivisionFactor](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo, T\_osUInt16 nFactor)  
*Set the dividen factor to pre-divider assigned to a certain input.*
- T\_osUInt16 [IDTInput\\_GetDivisionFactor](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo)  
*Get the dividen factor to pre-divider assigned to a certain input.*
- void [IDTInput\\_SetInputHFdivider](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo, [T\\_idtHighFrequencyDivisor](#) n-Usage)  
*Set the usage of high frequency (> 155.52MHz) divider.*
- [T\\_idtHighFrequencyDivisor IDTInput\\_GetInputHFdivider](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo)  
*Get high frequency configuration divider.*
- T\_osUInt8 [IDTInput\\_GetInputFreqOffset](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo)  
*Get the frequency offset of the specified input clock. The returned value is updated every 16 seconds.*
- T\_osUInt8 [IDTInput\\_GetInputClockStatus](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo)  
*Get the status of a specified input clock.*
- T\_osUInt8 [IDTInput\\_GetInputClockValidation](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo)  
*Get the clock validation status of an input port.*
- void [IDTInput\\_EnableAllInputs](#) (T\_idtDrvHdlr hdlr)  
*Enable to select anyone of input clocks.*
- void [IDTInput\\_DisableAllInputs](#) (T\_idtDrvHdlr hdlr)  
*Disable to select anyone of input clocks.*
- void [IDTInput\\_SetInputEnable](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo, T\_osUInt8 enable)  
*Enable/Disable selected input.*
- T\_osUInt8 [IDTInput\\_GetInputEnable](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nInputNo)  
*Retrieve enable/disable status of selected input.*
- void [IDTInput\\_SetSyncFrequency](#) (T\_idtDrvHdlr hdlr, [T\\_idtInputSyncFreq](#) syncFreq)  
*Function to select input external sync frequency.*
- [T\\_idtInputSyncFreq IDTInput\\_GetSyncFrequency](#) (T\_idtDrvHdlr hdlr)  
*Function to retrieve select input external sync frequency.*
- void [IDTInput\\_SetSyncSampling](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 exSyncN, [T\\_externalSyncSampling](#) sampling)  
*Function to provision sampling configuration for external sync.*
- [T\\_externalSyncSampling IDTInput\\_GetSyncSampling](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 exSyncN)  
*Function to retrieve sampling configuration for external sync.*
- void [IDTInput\\_SetSyncEdge](#) (T\_idtDrvHdlr hdlr, [T\\_externalSyncEdge](#) edge)  
*Function to provision synchronization alignment.*
- [T\\_externalSyncEdge IDTInput\\_GetSyncEdge](#) (T\_idtDrvHdlr hdlr)  
*Function to retrieve synchronization alignment.*
- void [IDTInput\\_SetSyncAlarmRange](#) (T\_idtDrvHdlr hdlr, [T\\_externalSyncAlarmRange](#) range)  
*Function to provision the sync allowable range before alarming.*
- [T\\_externalSyncAlarmRange IDTInput\\_GetSyncAlarmRange](#) (T\_idtDrvHdlr hdlr)  
*Function to retrieve the sync allowable range before alarming.*
- void [IDTInput\\_SetSyncBypass](#) (T\_idtDrvHdlr hdlr, [T\\_externalSyncBypass](#) bypass)  
*Function to provision sync bypass mode.*
- [T\\_externalSyncBypass IDTInput\\_GetSyncBypass](#) (T\_idtDrvHdlr hdlr)  
*Function to retrieve sync bypass mode.*
- void [IDTInput\\_SetSyncEnable](#) (T\_idtDrvHdlr hdlr, [T\\_externalSyncEnable](#) enable)  
*Function to provision enable mode for input external sync.*
- [T\\_externalSyncEnable IDTInput\\_GetSyncEnable](#) (T\_idtDrvHdlr hdlr)

*Function to retrieve external sync enable mode.*

- void `IDTInput_SetAmiInputFrequency` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo, `T_idtAmiInputFrequencyBitFieldValue` amiSignal)

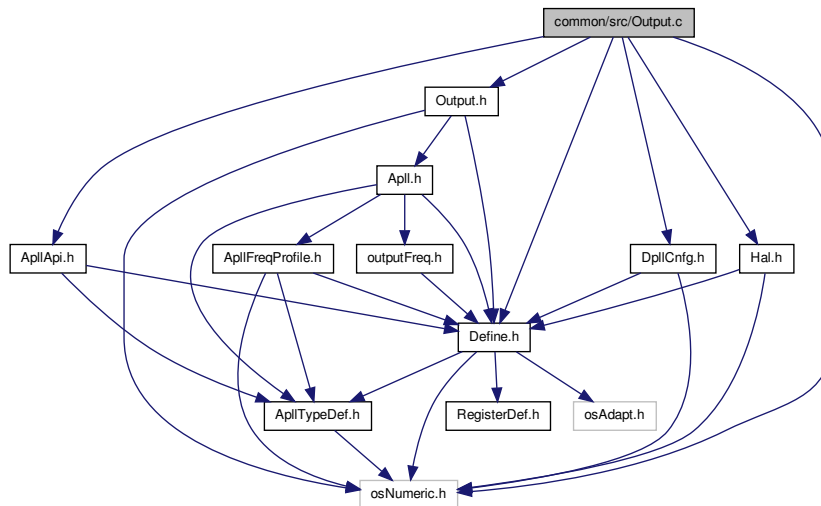
*Provision AMI signal for input port.*

- `T_idtAmiInputFrequencyBitFieldValue` `IDTInput_GetAmiInputFrequency` (`T_idtDrvHdlr` hdlr, `T_osUInt8` nInputNo)

*Function to retrieve AMI input frequency for input port.*

## 6.46 common/src/Output.c File Reference

```
#include "osNumeric.h"
#include "Define.h"
#include "Hal.h"
#include "Output.h"
#include "DpllCnfg.h"
#include "ApIApi.h"
Include dependency graph for Output.c:
```



## Enumerations

- enum `T_idtOutputPathBfVal` {  
`OutputPathBfVal_T0SonetGigEth` = 0, `OutputPathBfVal_T0Dpll_Eth` = 3, `OutputPathBfVal_T0Dpll_7776kHz`  
 = 4, `OutputPathBfVal_T0Dpll_12E1_GPS_E3_T3` = 5,  
`OutputPathBfVal_T0Dpll_16E1_16T1` = 6, `OutputPathBfVal_T0Dpll_GSM_OBSAI_16E1_16T1` = 7, `Output-`  
`PathBfVal_T4SonetGigEth` = 8, `OutputPathBfVal_T4Dpll_Eth` = 11,  
`OutputPathBfVal_T4Dpll_7776kHz` = 12, `OutputPathBfVal_T4Dpll_12E1_24T1_E3_T3` = 13, `OutputPathBf-`  
`Val_T4Dpll_16E1_16T1` = 14, `OutputPathBfVal_T4Dpll_GSM_GPS_16E1_16T1` = 15,  
`OutputPathBfVal_NULL`, `OutputPathBfVal_MAX` = `OutputPathBfVal_NULL` }

*Enumerated type listing possible output path selections.*

- enum { `OUTPUTIF_AMI_MASK` = 1<<`OUTPUTIF_AMI`, `OUTPUTIF_CMOS_MASK` = 1<<`OUTPUTIF_CMOS`, `OUTPUTIF_LVDS_MASK` = 1<<`OUTPUTIF_LVDS`, `OUTPUTIF_PECL_MASK` = 1<<`OUTPUTIF_-PECL` }

*Enumerated type supported output port interfaces in bit mask format.*

## Functions

- void [IDTOutput\\_SetOutputConfig](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN, T\_idtDpllInstance nDpll, T\_outputPathType nPath, T\_osUInt8 nFactor, T\_idtApllConfigPerOutput \*aplConfig)
 

*Set the configuration of Output port.*
- void [IDTOutput\\_GetOutputConfig](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN, T\_idtDpllInstance \*nDpll\_p, T\_outputPathType \*nPath\_p, T\_osUInt8 \*nFactor\_p, T\_idtApllConfigPerOutput \*aplConfig)
 

*Get the configuration of Output port.*
- void [IDTOutput\\_SetOutputInvert](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN, T\_osUInt8 invert)
 

*Set the specified output port to generate a invert signal.*
- T\_osUInt8 [IDTOutput\\_GetOutputInvert](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN)
 

*Get output signal inversion status.*
- void [IDTOutput\\_SetOutputEnable](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN, T\_osUInt8 nEnable)
 

*Enable/Disable output port. Consult data sheet for supported ports.*
- T\_osUInt8 [IDTOutput\\_GetOutputEnable](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN)
 

*Get enable/disable status of output port. Consult data sheet for supported ports.*
- void [IDTOutput\\_SetOutputInterface](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN, T\_outputInterface outIf)
 

*Set output port interface type. Consult data sheet for supported interfaces per port.*
- T\_outputInterface [IDTOutput\\_GetOutputInterface](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 nOutN)
 

*Get output port interface type. Consult data sheet for supported interfaces per port.*
- void [IDTOutput\\_SetFrameSync](#) (T\_idtDrvHdlr hdlr, T\_frameSync frameSync, T\_osUInt8 enable, T\_osUInt8 invert, T\_osUInt8 pulse)
 

*Function to control output frame syncs.*
- void [IDTOutput\\_GetFrameSync](#) (T\_idtDrvHdlr hdlr, T\_frameSync frameSync, T\_osUInt8 \*enable\_p, T\_osUInt8 \*invert\_p, T\_osUInt8 \*pulse\_p)
 

*Function to retrieve output frame sync configuration.*
- void [IDTOutput\\_SetFrameSyncPulseEdge](#) (T\_idtDrvHdlr hdlr, T\_osUInt8 isRisingEdge)
 

*Function provision trigger for frame sync pulses.*
- T\_osUInt8 [IDTOutput\\_GetFrameSyncPulseEdge](#) (T\_idtDrvHdlr hdlr)
 

*Function retrieve trigger for frame sync pulses.*
- void [IDTOutput\\_DisableApllInput](#) (T\_idtDrvHdlr hdlr, T\_idtOutputApllConfig outputApllConfig)
 

*Function disables APLL input.*
- void [IDTOutput\\_DisableAllIntOutput](#) (T\_idtDrvHdlr hdlr)
 

*Function disables all internal outputs.*

### 6.46.1 Enumeration Type Documentation

#### 6.46.1.1 anonymous enum

Enumerated type supported output port interfaces in bit mask format.

#### Enumerator

- OUTPUTIF\_AMI\_MASK** AMI Interface mask
- OUTPUTIF\_CMOS\_MASK** CMOS Interface mask
- OUTPUTIF\_LVDS\_MASK** LVDS Interface mask
- OUTPUTIF\_PECL\_MASK** PECL Interface mask

Definition at line 78 of file Output.c.

## 6.46.1.2 enum T\_idtOutputPathBfVal

Enumerated type listing possible output path selections.

## Enumerator

***OutputPathBfVal\_T0SonetGigEth*** From T0 Sonet/GigE path  
***OutputPathBfVal\_T0Dpll\_Eth*** From T0 DPLL ETH path  
***OutputPathBfVal\_T0Dpll\_7776kHz*** From T0 DPLL 77.76 MHz path  
***OutputPathBfVal\_T0Dpll\_12E1\_GPS\_E3\_T3*** From T0 DPLL 12E1/GPS/E3/T3 path  
***OutputPathBfVal\_T0Dpll\_16E1\_16T1*** From T0 DPLL 16E1/16T1 path  
***OutputPathBfVal\_T0Dpll\_GSM\_OBSAI\_16E1\_16T1*** From T0 DPLL GSM/OBSAI/16E1/16T1 path  
***OutputPathBfVal\_T4SonetGigEth*** From T4 Sonet/GigE path  
***OutputPathBfVal\_T4Dpll\_Eth*** From T4 DPLL ETH path  
***OutputPathBfVal\_T4Dpll\_7776kHz*** From T4 DPLL 77.76 MHz path  
***OutputPathBfVal\_T4Dpll\_12E1\_24T1\_E3\_T3*** From T4 DPLL 12E1/E3/T3/24T1 path  
***OutputPathBfVal\_T4Dpll\_16E1\_16T1*** From T4 DPLL 16E1/16T1 path  
***OutputPathBfVal\_T4Dpll\_GSM\_GPS\_16E1\_16T1*** From T4 DPLL GSM/GPS/16E1/16T1 path  
***OutputPathBfVal\_NULL*** Not supported  
***OutputPathBfVal\_MAX***

Definition at line 48 of file Output.c.

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