

RL78 Family C Compiler Package (CC-RL)

R20UT3475EJ0300 Rev. 3.00 May 31, 2019

How to Divide Boot and Flash Areas

Introduction

This document describes the processing necessary to divide a program into boot and flash areas when using the C compiler for the RL78 family (CC-RL).

Versions of Tools with which Correct Operation has been Confirmed

The following tools and versions were used for the descriptions in this document.

- C compiler for the RL78 family (CC-RL): V1.08.00
- e² studio integrated development environment: V7.3.0
- CS+ for CC integrated development environment: V8.01.00

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1. Overview

1.1 Dividing the Boot and Flash Areas

The purpose of dividing the boot and flash areas is to ensure that only the program in the flash area can be modified without reconfiguring the program in the boot area.



Figure 1 Divided Areas on System

Note: In this document, the boot area is defined as an area that cannot be modified following design of the system while the flash area is defined as an area that can be modified or replaced on the system.

To divide the boot and flash areas, create two projects, one to be used as the boot area project and the other to be used as the flash area project. These projects must satisfy the following conditions.

- The variables and functions in the boot area are accessible from the flash area.
 - The linker option -FSymbol should be used for the boot area project so that externally defined symbols will be output in a file.
- The above externally defined symbol file should be specified as a target of building in the flash area project.
- The functions in the flash area can be called from the boot area through a function table.
 - When calling functions in the flash area, the boot area project should call the address of each branch instruction for a function that is specified in the function table.
 - A table of branch instructions for functions to be called from the boot area project should be created in the flash area project.



Figure 2 References to Variables and Functions between the Boot and Flash Areas



1.2 Allocating the Boot and Flash Areas

Allocate the boot and flash areas as follows.



Figure 3 Example of Allocating the Boot and Flash Areas

1.3 Procedures for Creating the Boot Area and Flash Area Projects

Follow the procedures below to create the boot area and flash area projects.

- 1. Creating the boot area project
 - A. Create boot area programs in the source file.
 - B. Specify the necessary linker options.
 - C. Build the boot area project before the flash area project because the boot area project is required for building the flash area project.
- 2. Creating the flash area project
 - A. Create flash area programs in the source files.
 - B. Specify the necessary linker options.



1.4 Overview of Build Processing for the Boot and Flash Areas

Figure 4 shows an overview of build processing for the boot and flash areas.





2. Common Processing for the Boot and Flash Areas

2.1 Creating projects

2.1.1 e² studio

1. Create projects

Create a boot area project and a flash area project by following the procedures given in section 1.3, Procedures for Creating the Boot and Flash Areas.

Place a tick in the "boot" checkbox to configure the flash area project to allow reference to the boot area project from the flash area project when the flash area project is built. In such cases, the boot area project is built before the flash area project.

e ² Properties for flash	-		×
 Properties for flash type filter text Resource Builders C/C++ Build C/C++ General MCU Project References Renesas QE Run/Debug Settings Task Repository 	Project References Projects may refer to other projects in the workspace. Use this page to specify what other projects are referenced Project references for 'flash': ✓ ✓ ▶ boot	- □	* *
?	Apply and Close	Cancel	

Figure 5 Setting the Flash Area Project to Allow Reference to the Boot Area Project



2. Add files as targets of building

- A. Add the following files to the boot area project as targets of building.
 - extern_ftable.asm
 - ftable.inc
 - ocdmon_ce.asm
- B. Add the following files to the flash area project as targets of building.
 - boot.fsy (this file is generated after the boot area project is built)
 - ftable.asm
 - ftable.inc
 - int.c
 - sub_mot.txt



Figure 6 Example of Creating Projects with the e² studio



2.1.2 CS+

1. Create projects

Create the flash area project as the main project and the boot area project as a sub-project*.

Note: The build order in CS+ should be [Sub-project] -> [Main project].

The boot area program will not be modified once it is created. Therefore, when creating the secondor a later generation flash area project, the sub-project can be deleted.

2. Exclude the automatically generated file from the targets of building Exclude the following file from the boot area and flash area projects.

- main.c
- 3. Add files as targets of building
 - A. Add the following files to the boot area project.
 - boot.c
 - extern_ftable.asm
 - ftable.inc
 - ocdmon_ce.asm
 - B. Add the following files to the flash area project.
 - flash.c
 - ftable.asm
 - ftable.inc
 - int.c
 - boot.fsy







2.2 Creating a common program for the boot and flash areas

2.2.1 Address definition file for the branch table (assembly language)

- Create ftable.inc, which is the address definition file for the branch table for reference from both the boot and flash areas.
 - FLASH_TABLE: Start address of the branch table
 - INTERRUPT_OFFSET: Size of the interrupt area in the branch table

Example: ftable.inc

		QU	0x2000
INTERR	TERRUPT_OFFSET .E	ΩQ	0x100

2.3 Hex files for the boot and flash areas

File names used in this document are listed below (output procedures are described later).

- Hex file for the boot and flash areas combined: boot_flash.mot
- Hex file for the flash area: flash2000_ffff.mot
- Hex file for the boot area: boot0000_1fff.mot

Note: A load module file (*.abs) is separately generated for each of the boot and flash areas.





2.4 Initialization procedure

Figure 9 shows the initialization procedure.



Figure 9 Initialization Procedure



3. Boot Area

3.1 Creating boot area programs

The following steps are required for boot area programs.

- Modifying the startup routine
- Modifying hdwinit.asm and stkinit.asm
- Creating the program such that the on-chip debug area is secured
- Creating a file for resolving the function addresses in the branch table

3.1.1 Modifying the startup routine (cstart.asm)

The procedure for modifying the startup routine (cstart.asm) is given below.

1. Add inclusion of the address definition file for the branch table.

Example: Modifying cstart.asm (1/6)

```
$IFNDEF __RENESAS_VERSION__
__RENESAS_VERSION__.EQU 0x01000000
$ENDIF
$INCLUDE "ftable.inc"
```

2. Comment out the conditional assembly control instructions to make the definition of the .stack_bss section valid.

Example: Modifying cstart.asm (2/6)

```
;$IF (__RENESAS_VERSION__ < 0x01010000); for CC-RL V1.00
;------
; stack area
;------; !!! [CAUTION]!!!
; Set up stack size suitable for a project.
.SECTION .stack_bss, BSS
_stackend:
   .DS 0x200
_stacktop:
;$ENDIF</pre>
```

3. Modify the section name to exclude it from the target of the -FSymbol option (which is used to output externally defined symbols).

Example: Modifying cstart.asm (3/6)



4. Comment out the conditional assembly control instructions to specify the explicitly allocated .stack_bss section as the stack pointer.

Example: Modifying cstart.asm (4/6)

```
;-----
 ; setting the stack pointer
 ;-----
;$IF (__RENESAS_VERSION__ >= 0x01010000)
; MOVW SP, #LOWW( STACK ADDR START)
;$ELSE ; for CC-RL V1.00
 MOVW SP, #LOWW ( stacktop)
;$ENDIF
```

5. Modify the main function call to the call to the main function for the boot area, and add a branch instruction to the flash area startup routine.

Example: Modifying cstart.asm (5/6)

```
;-----
; call main function
;-----
CALL !! boot main ; main();
BR !!FLASH TABLE
```

6. Comment out the definition of the .const section when no mirror source area is included in the boot area.

Example: Modifying cstart.asm (6/6)

```
; section
;------
$IF ( RENESAS VERSION >= 0x01010000)
.SECTION .RLIB, TEXTF
.L section RLIB:
.SECTION .SLIB, TEXTF
.L section SLIB:
$ENDIF
.SECTION .textf, TEXTF
.L section textf:
;.SECTION .const, CONST
;.L section const:
```



3.1.2 Modifying hdwinit.asm and stkinit.asm

Modify the section name to exclude it from the target of the -FSymbol option (which is used to output externally defined symbols).

Example: Modifying hdwinit.asm and stkinit.asm

.btextf .CSEG TEXTF

3.1.3 Creating the program such that the on-chip debug area is secured (ocdrom_ce.asm)

To use the on-chip debugging function, specific memory areas are required to be empty (filled with 0xff).

Specifying the -debug_monitor option of the linker leads to the generation of a load module file in which the addresses 0x0002 to 0x0003, 0x00ce to 0x00d7, and the last 512 bytes of ROM are filled with 0xff (set up according to the information in the device file specified with the -device option).

Since the last 512 bytes of ROM are part of the flash area, make the following settings for the boot area.

- Addresses 0x0002 to 0x0003 Specify 0xffff with the linker option -VECTN.
- Addresses 0x00ce to 0x00d7
 Make definitions in the assembly source (see the following program).

Example: ocdrom_ce.asm

```
MON_CE .CSEG AT 0x00ce
.DB8 0xffffffffffffff
.DB2 0xffff
```

- Last 512 bytes of ROM Allocate this area through the flash area project.
- 3.1.4 Creating a file for resolving the function addresses in the branch table (extern_ftable.asm)
- Define symbols for resolving the addresses for the branch table to be used to call functions in the flash area from the boot area.
- Register this file in the project.

Example: Creating extern_ftable.asm

```
$INCLUDE "ftable.inc"
.public_f1
_f1 .equ (FLASH_TABLE + INTERRUPT_OFFSET + (0 * 4))
.public_f2
f2 .equ (FLASH_TABLE + INTERRUPT_OFFSET + (1 * 4))
```



3.2 Specifying boot area options

Make the following option settings for the boot area.

- Output of a file for the externally defined symbols
- Specify the section allocation
- Specify a vector for branching to the interrupt function in the flash area
- Make necessary settings for the on-chip debugging function
- Specify hex file output only to the boot area address range

3.2.1 Output of a file for the externally defined symbols

The externally defined symbols need to be output to a file so that the flash area project has access to the variables and functions in the boot area.

Register all target sections with the -FSymbol option.

Example: e² studio

 $[Properties] \rightarrow [C/C++ Build] \rightarrow [Settings] \rightarrow [Tool Settings] tabbed page$

 \rightarrow [Linker] \rightarrow [Output] \rightarrow [Section that outputs external defined symbols to the file]



Figure 10 Example of Option Setting with the e² studio



Example: CS+

 $[\text{CC-RL} (\text{Build Tool})] {\rightarrow} [\text{Link Options}] \text{ tabbed page}$

 \rightarrow [Section] \rightarrow [Section that outputs external defined symbols to the file]

Property	- x
CC-RL Property	- +
✓ Section	^
Layout sections automatically	Yes(-AUTO_SECTION_LAYOUT)
Section start address	
 Section that outputs external defined symbols to the file 	Section that outputs external defined symbols to the file[10]
[00]	.constf
[01]	text
[02]	textf
[03]	.const
[04]	lbss
[05]	.sbss
[06]	.data
[07]	.sdata
[08]	.RLIB
1091	SLIB
> ROM to RAM mapped section	ROM to RAM mapped section[2]
> Verify	
> Message	
> Others	✓
[01]	
Specifies the section that outputs external defined symbols to the file in the format of	f " <section name="">", one per line.</section>
This option corresponds to the -FSymbol option of the rlink command.	
Common Options / Compile Options / Assemble Options Link Option	IS Hex Output Options / I/O Header File Generation Options /

Figure 11 Example of Option Setting with CS+



3.2.2 Specifying the section allocation

Specify the section allocation in the boot area with the linker option -start. Make sure that the sections do not overlap those in the flash area.

In addition, specify the stack area section.

Example: e² studio

 $[Properties] \rightarrow [C/C++ Build] \rightarrow [Settings] \rightarrow [Tool Settings] tabbed page$

 \rightarrow [Linker] \rightarrow [Section] \rightarrow [Section Viewer]

e ² Properties for boot					
type filter text	Settings				(→ → -
 > Resource Builders > C/C++ Build Build Variables Environment Logging Settings Tool Chain Editor > C/C++ General > MCU Project References 	Configuration: HardwareD Tool Settings Toolchai Stress Common Stress Compiler Stress Assembler Stress Linker	in Device 🎤 Build	ns automatically	 ✓ Manage Conf 	rigurations
Renesas QE Run/Debug Settings > Task Repository	 Input Advanced List Optimization Section Device Output Advanced Miscellaneous User Sector 		Section Name btext btext .btextf .RLIB .text .SLIB .textf .constf	Add Section New Overlay	
?		0x000FE900	.data .sdata .stack bss .dataR .bss	Remove Section Move Up Move Down	cancel
		0x000FFE20	·	Browse	
				OK Cancel	

Figure 12 Example of Option Setting with the e² studio



Example: CS+

[CC-RL (Build Tool)]→[Link Options] tabbed page

 \rightarrow [Section] \rightarrow [Section start address]

✓ CC-RL Property					₽ - +	
✓ Section					^	
Layout sections automatically	Layout sections automatically Yes(-AUTO_SECTION_LAYOUT)					
Section start address	.btext,.btex	tftext,.RLIB,.SLI	IB,.textf,.constf,.da	ta,.sdata/000D8,.s	tack_bss,.data	
 Section that outputs external defined symbols to the file [00] [01] 	Section Settings			×		
[01]	Address	Section		Add		
[02]	0x000D8	.btext	L I	_		
[04]		.btextf		Modify		
[05]	l		[New Overlag		
[06]		.text	l	New <u>O</u> verlay		
[07]		.RLIB		Remove		
[00]		.SLIB	L			
> ROM to RAM mapped section		.textf		Up Down		
> Verify		.constf				
> Message		.data				
> Others					~	
Section start address		.sdata				
Specify the section start address.	0xFE900	.stack_bss				
This option corresponds to the -STARt option of the rlink command.		.dataR				
		.bss				
Common Options / Compile Options / Assemble Options / Link O	0xFFE20	.sdataR		Import		
		.sbss	[<u>E</u> xport		
		ОК	Cancel	<u>H</u> elp		

Figure 13 Example of Option Setting with CS+



3.2.3 Specifying a vector for branching to the interrupt function in the flash area Specify the address in the branch table with the linker option -VECTN.

Example: e² studio

[Properties]→[C/C++ Build]→[Settings]→[Tool Settings] tabbed page

 \rightarrow [Linker] \rightarrow [Output] \rightarrow [Address setting for specified area of vector table]

 \rightarrow 8=0x2010 (to specify 0x2010 for address 8)

e ² Properties for boot				_	×
type filter text	Settings			⇔ - ⊲	> - -
 > Resource Builders > C/C++ Build Build Variables Environment Logging Settings Tool Chain Editor > C/C++ General > MCU Project References Renesas QE Run/Debug Settings > Task Repository 	 Linker Iput Advanced List Optimization Section Device Output Advanced Miscellaneous User Secton 	Output debug information Compress debug information Delete local symbol name information Reduce memory occupancy of linker Fill with padding data at the end of a section Address setting for unused vector area Generate divided vector table section Address setting for specified area of vector table 8=0x2010 ROM to RAM mapped section		1 중 중 ·	
?			Apply and Close	Cano	:el

Figure 14 Example of Option Setting with the e² studio

Example: CS+

[CC-RL (Build Tool)]→[Link Options] tabbed page

→[Output Code]→[Address setting for specified area of vector table]

 \rightarrow 8=2010 (to specify 0x2010 for address 8)

-	CC-RL Property	- 4	+				
	Device Output Code		^				
	Specify execution start address	No					
		No	- 10				
	Fill with padding data at the end of a section						
~	Address setting for specified area of vector table	Address setting for specified area of vector table[2]					
	[0]	2=ffff					
	[1]	8=2010					
	Address setting for unused vector area		-				
	Generate function list used for detecting illegal indirect function call	No					
	Split vector table sections	No					
>	List		~				
Device Common Options / Compile Options / Assemble Options / Hex Output Options / I/O Header File Generation Options /							

Figure 15 Example of Option Setting with CS+



3.2.4 Making necessary settings for the on-chip debugging function

- 1. Allocate the area of addresses 0x0002 and 0x0003 with the linker option -VECTN (if you are using the e2 studio, this area is automatically allocated).
- 2. Set the linker option –OCDBG to be enabled and specify the value for the on-chip debug option byte.

Example: e² studio

 $[Properties] \rightarrow [C/C++ Build] \rightarrow [Settings] \rightarrow [Tool Settings] tabbed page$

 \rightarrow [Linker] \rightarrow [Device] \rightarrow [Set enable/disable on-chip debug by link option]

Note: If you are using a hardware-debug build configuration (i.e. with "E1/E2", "E2", or "E2 Lite" selected as the debugger hardware), deselect the [Secure memory area of OCD monitor] checkbox.

e ² Properties for boot			_		×
type filter text	Settings			⇔ - ⇒	• •
 > Resource Builders > C/C++ Build Build Variables Environment Logging Settings Tool Chain Editor > C/C++ General > MCU Project References Renesas QE Run/Debug Settings > Task Repository 	 > Son Common > Son Compiler > Son Assembler > Son Assembler > Son Linker > Son Input > Advanced > Ust > Optimization > Section > Section > Device > Son Output > Advanced > Miscellaneous > User > Son Converter 	Check specifications of de	CD monitor O5E00-05FFF FFFFEF o debug by link option 85 None e when a section is allocated to the RAM area allocation that crosses (64KB-1) boundary potation of sections	월 춘I 윤I	
?			Apply and Close	Cance	I

Figure 16 Example of Option Setting with the e² studio



Example: CS+

[CC-RL (Build Tool)]→[Link Options] tabbed page

- \rightarrow [Device] \rightarrow [Option byte values for OCD]
- \rightarrow [Section] \rightarrow [Address setting for specified area of vector table]
- \rightarrow 2=ffff (to set 0xffff at address 2)

×	CC-RL Property		م 1	-	+
~	Device				^
	Set enable/disable on-chip debug by link option	Yes(-OCDBG)			
	Option byte values for OCD	HEX 85			
	Set debug monitor area	No			
	Set user option byte	Yes(-USER_OPT_BYTE)			
	User option byte value	HEX FFFFEF			
	Control allocation to self RAM area	No			
~	Output Code				
	Specify execution start address	No			
	Fill with padding data at the end of a section	No			
× ا	Address setting for specified area of vector table	Address setting for specified area of vector table[2]		_	
	[0]	2=ffff			
	[1]	8=2010			
	Address setting for unused vector area				×
De	vice				
\setminus	Common Options 🖌 Compile Options 🧹 Assemble Options 🔪 Link O	ptions 🔏 Hex Output Options 🧹 I/O Header File Generation Options			•

Figure 17 Example of Option Setting with CS+



3.2.5 Specifying hex file output only to the boot area address range

Specify the output file name and output addresses.

Example: e² studio

 $[Properties] \rightarrow [C/C++ Build] \rightarrow [Settings] \rightarrow [Tool Settings] tabbed page$

- →[Converter]→[Output]
- \rightarrow Select the [Output hex file] checkbox.
- \rightarrow Select [Motorola S-record file] as the output file format.
- \rightarrow Specify the output file name and output addresses in [Division output file].



Figure 18 Example of Option Setting with the e² studio

Example: CS+

[CC-RL (Build Tool)]→[Hex Output Options] tabbed page

→[Output File]→Specify the output file name and output addresses in [Division output file].

~	CC-RL Property		₽ - +				
	Output hex file	Yes	^				
	Output folder	%BuildModeName%					
	Output file name	%ProjectName%.mot					
	Load address	HEX					
~	Division output file	Division output file[1]					
	[0]	%BuildModeName%\boot0000_1fff.	mot=0000-1fff				
×	THEX FORMAL		•				
Division output file Specify the division hex file in the format of " <file name="">={<start address="">-<end address=""> <section name="">[]][/<load address="">]", one per line. ([/<load address="">] can be specified in case of CC-RL V1.07.00 or later and the [Hex file format] property is Intel HEX file or Motorola S-record file.) Specifies the <start address=""> and <end address=""> in hexadecimal without 0x. The default extensions depends on [Hex file format]property when extension omitted</end></start></load></load></section></end></start></file>							
\setminus	Common Options 🖌 Compile Options 🖌 Assemble Options 🖌 Link Op	otions Hex Output Options	I/O Header File Generation Options /				

Figure 19 Example of Option Setting with CS+



4. Flash Area

4.1 Creating flash area programs

The following steps are required for flash area programs.

- Modifying the startup routine
- Creating a branch table program
- Defining an interrupt function

4.1.1 Modifying the startup routine (cstart.asm)

Comment out the stack pointer settings. The stack pointer specified in the boot area startup routine should be used; a stack pointer must not be specified again in the flash area.

Example: cstart.asm

```
;-----
; setting the stack pointer
;------
;$IF (__RENESAS_VERSION__ >= 0x01010000)
; MOVW SP,#LOWW(_STACK_ADDR_START)
;$ELSE ; for CC-RL V1.00
; MOVW SP,#LOWW(_stacktop)
;$ENDIF
```

4.1.2 Creating a branch table program (ftable.asm)

At the addresses called from the boot area, write instructions for branching to the function addresses in the flash area.

Example: ftable.asm





4.1.3 Defining an interrupt function

- The interrupt vector should be defined in the boot area project.
- Do not specify the vector address (vect) with the #pragma interrupt directive in the flash area.

Example: int.c

```
#include "iodefine.h"
#pragma interrupt int_INTPO
volatile char f;
void int_INTPO(void)
{
    f = 1;
}
```

4.2 Specifying flash area options

Make the following option settings for the flash area.

- Register the externally defined symbol file with the project
- Specify the section allocation
- Specify hex file output only to the flash area address range
- Combine the hex files for the boot and flash areas

4.2.1 Registering the externally defined symbol file with the project

Register the externally defined symbol file created in the boot area with the project to allow access to the variables and functions in the boot area.

Example: e² studio

If you are using the e² studio, build the boot area project and then manually register the externally defined symbol file (boot.fsy) created in the boot area with the flash area project.



Figure 20 Example of Option Setting with the e² studio



Example: CS+

If you are using CS+, building the boot area project will automatically register the externally defined symbol file (boot.fsy) with the flash area project.



Figure 21 Example of Option Setting with CS+



4.2.2 Specifying the section allocation

Specify the section allocation in the flash area with the linker option -start.

- Make sure that the sections do not overlap those in the boot area.
- Do not allocate anything to the branch table area.

Example: e² studio

 $[Properties] \rightarrow [C/C++ Build] \rightarrow [Settings] \rightarrow [Tool Settings] tabbed page$

 \rightarrow [Linker] \rightarrow [Section] \rightarrow [Section Viewer]

Address	Section Name	
0x00002200	.const	
	.text	
	.data	
	.sdata	Add Section
	.RLIB	
	.SLIB	New Overlay
	.textf	Remove Section
	.constf	Move Up
0x000FEC00	.dataR	Move Down
	.bss	movebown
0x000FFE80	.stataR	
	.sbss	
	Carlat	
Override Linke	rschpt	
		Browse
Imp	ort Export Re-Apply	

Figure 22 Example of Option Setting with the e² studio



Example: CS+

[CC-RL (Build Tool)]→[Link Options] tabbed page

 \rightarrow [Section] \rightarrow [Section start address]

Section Setting	JS		×
Address	Section		<u>A</u> dd
0x02200	.const		Modify
	.text		<u>In</u> ouny
	.RLIB		New <u>O</u> verlay
	.SLIB		Remove
	.textf		
	.constf		<u>U</u> p <u>D</u> own
	.data		
	.sdata		
0xFEC00	.dataR		
	.bss		
0xFFE80	.sdataR		Import
	.sbss		<u>E</u> xport
·	ОК	Cancel	<u>H</u> elp

Figure 23 Example of Option Setting with CS+



4.2.3 Specifying hex file output only to the flash area address range

Specify the output file name and output addresses.

Example: e² studio

 $[Properties] \rightarrow [C/C++ Build] \rightarrow [Settings] \rightarrow [Tool Settings] tabbed page$

- \rightarrow [Converter] \rightarrow [Output]
- \rightarrow Select the [Output hex file] checkbox.
- \rightarrow Select [Motorola S-record file] as the output file format.

 \rightarrow Specify the output file name and output addresses in [Division output file].

e ² Properties for flash		×
type filter text	Settings $\Leftrightarrow \checkmark \Rightarrow \checkmark$	•
 Resource Builders C/C++ Build Build Variables Environment Logging Settinger 	Configuration: HardwareDebug [Active] Manage Configurations Tool Settings Toolchain Device Pailed Steps Build Artifact Binary Parsers Settor Parsers	*
Settings Tool Chain Editor C/C++ General MCU Project References Renesas QE Run/Debug Settings Task Repository	> So Common	
?	Apply and Close Cancel	>

Figure 24 Example of Option Setting with the e² studio

Example: CS+

[CC-RL (Build Tool)]→[Hex Output Options] tabbed page

 \rightarrow [Output File] \rightarrow Specify the output file name and output addresses in [Division output file].

-	ζ,	CC-RL Property	â 🖉 – +		
•	~	Output File	A		
		Output hex file	Yes		
		Output folder	%BuildModeName%		
		Output file name	%ProjectName%.mot		
	_	Load address	HEX		
ŀ	~	Division output file	Division output file[1]		
L		[0]	%BuildModeName%\flash2000_ffff.mot=2000+ffff		
		Hex Format	· · · · · · · · · · · · · · · · · · ·		
S E	Division output file Specify the division hex file in the format of " <file name="">={<start address=""><end address=""> <section name="">[]{/<load address="">]", one per line. ([/<load address="">] can be specified in case of CC-RL V1.07.00 or later and the [Hex file format] property is Intel HEX file or Motorola S-record file.) Specifies the <start address=""> and <end address=""> in hexadecimal without 0x</end></start></load></load></section></end></start></file>				
$\left[\right]$	С	ommon Options 🖌 Compile Options 🤺 Assemble Options 🖌 Link Op	otions \lambda Hex Output Options 👌 I/O Header File Generation Options 🖉 🔻 🔻		

Figure 25 Example of Option Setting with CS+



4.2.4 Combining the hex files for the boot and flash areas

To combine the hex files for the boot and flash areas into one file, add the linker execution step after the build processing.

Example: e² studio

e ² Properties for flash		— 🗆	×	
type filter text	Settings	<> ▼ 0	⇒	,
 > Resource Builders > C/C++ Build Build Variables Environment Logging Settings Tool Chain Editor > C/C++ General > MCU Project References Renesas QE Run/Debug Settings > Task Repository 	Tool Settings Toolchain Device Perebuild Steps Pre-build steps Command(s):	S Error Parser		~
?	Apply and Cl	lose Can	icel	

Figure 26 Example of Option Setting with the e² studio

Example: CS+

[CC-RL (Build Tool)]→[Common Options] tabbed page→[Others]

 \rightarrow Add the command to execute the linker ("%MicomToolPath%¥CC-RL¥V1.08.00¥bin¥rlink.exe" - subcommand=sub_mot.txt) to [Commands executed after build processing].

•

Figure 27 Example of Option Setting with CS+



Specify the input hex files, their format, and the output file name in the subcommand file for input to the linker.

Example: sub_mot.txt (e² studio)

```
-input=..¥..¥boot¥HardwareDebug¥boot0000_1fff.mot
-input=flash2000 ffff.mot
-form=stype
-output=boot flash.mot
```

Example: sub_mot.txt (CS+)

```
-input=.¥boot¥DefaultBuild¥boot0000 1fff.mot
-input=.¥DefaultBuild¥flash2000 ffff.mot
-form=stype
-output=.¥DefaultBuild¥boot flash.mot
```



5. Debugging Tool

5.1 Downloading to Debugging Tool

Two load module files (*.abs) are generated; one for each of the boot and flash areas. Download both of the load module files to the debugging tool.

Example: e² studio

 $[Debug] \rightarrow [Debug \ Configurations] \rightarrow [flash \ Hardware Debug] \rightarrow [Startup] \ tabbed \ page$

 \rightarrow [Load image and symbols]

Add the load module file for the boot area to the project for the flash area.

e ² Debug Configurations					×	
Create, manage, and run configurations					-	
😢 [Main]: Program does not exist					JOr -	
					,	
	Name: flash HardwareDebug					
type filter text	🖺 Main 🕸 Debugger 🍺 Star	tup 🔲 🛄 Common 🖥	Source			
C/C++ Application	Initialization Commands					
EASE Script	Reset and Delay (seconds):	3				
C GDB Hardware Debugging C GDB OpenOCD Debugging						
GDB Simulator Debugging (RH850)						
Java Applet Java Application					~	
🕞 Launch Group	Load image and symbols					
Launch Group (Deprecated) Remote Application	Filename	Load type	Offset (hex)	On connect	Add	
Semote Debugger	Program Binary [flash.x]	Image and Symbols		Yes		
Remote Java Application	✓ boot.x [C:\Users\toolgi	Image and Symbols	0	No	Edit	
✓ C [™] Renesas GDB Hardware Debugging C [™] boot HardwareDebug					Remove	
c* flash HardwareDebug					Move up	
C [®] Renesas Linux Application C [®] Renesas Simulator Debugging (RX, RL78)					Move down	
Target Communication Framework						
	Runtime Ontions					
Filter matched 19 of 21 items					Re <u>v</u> ert Appl <u>v</u>	
(?)					Debug Close	
e ² Debug - flash/src/cstart.asm - e2 studio				*Note o	on e² studio	
File Edit Navigate Search Project Renesas Vi → → → → → → → → → → → → → → → → → → →		ə 1 🖓 1 🔏 1 🗩 🕹				
			ee.		ot.x to "No" when ting the debugging	
					ownload it after	
🎄 Debug 🛛 🚺 🔩 🖛 💷 🏦	ê 🖏 🕹			connec	tion.	
▲ C [×] flash HardwareDe	All on-connect modules					
All on-connect	modules					
≡ start()			4			
C:/Renesas/e. Clear symbol ta	ble		- 1			
Program Binary	[boot.x] [Image and Symi	ools, 0x0]				

Figure 28 Example of Option Setting with the e² studio



Example: CS+

[RL78 Simulator (Debug Tool)]→[Download File Settings] tabbed page

 \rightarrow [Download] \rightarrow [Download files]

Add the load module file for the boot area to the project for the flash area.

RL78 Simulator Property		P - +
✓ Download		
> Download files	[2]	
CPU Reset after download	Download Files	×
Automatic change method of event setting position	Download file list:	Download file property:
> Debug Information	flash.abs	
	boot.abs	File \boot \Default Build \boot .abs
		Down File type Load module file
		Download object Yes Download symbol informatic Yes
		Generate the information for Yes
		File
		Specify the file to be downloaded.
Download files	<u>A</u> dd <u>R</u> emove	
Specifies the file to be downloaded. The download file dialog box is opened		
		OK Cancel <u>H</u> elp
Connect Settings / Debug Tool Settings / Download File Setting	us 🖉 Hook Transaction Sett	******
Connect Settings Debug Tool Settings Download File Setting	IS A HOOK Transaction Set	ungs /

Figure 29 Example of Option Setting with CS+



6. Sample Programs

The following pages show examples of boot and flash area programs that were created through the procedures described in earlier sections.

6.1 Sample program for the boot area (boot.c)

```
#include "iodefine.h"/* SFR definition file */
#pragma interrupt int INTP1(vect=INTP1) /* Interrupt definition in the boot
area */
int boot a = 0x12;
int boot b = 0x34;
extern int f1(int); /* Prototype declaration of a function in the flash area
*/
extern int f2(int); /* Prototype declaration of a function in the flash area
*/
void boot main(void) /* Main function in the boot area \ */
{
 /* Main processing in the boot area */
}
void boot func (void)
{
 boot_a = f1(boot_a); /* Call of a function in the flash area */
 boot_b = f2(boot_b); /* Call of a function in the flash area */
}
void int INTP1 (void) /* Interrupt processing in the boot area */
{
 boot a = 1;
}
```



6.2 Sample program for the flash area (flash.c)

```
#include "iodefine.h"/* SFR definition file */
int flash a, b;
extern int boot_a, boot_b; /* Functions defined in the boot area */
extern void boot_func(void); /* Function defined in the boot area */
int f1(int a)
{
return (++a);
}
int f2(int b)
{
return (--b);
}
{
boot_a++;  /* Access to a variable in the boot area */
boot_b++;  /* Access to a variable in the boot area */
boot func(); /* Access to a variable in the boot area */
}
```



Revision History

		Descriptio	Description	
Rev.	Date	Page	Summary	
1.00		-	New release	
2.00		All	Changed the format of this document	
		P3, P29, P32, P47	Updated the version numbers of tools	
		P32, P33	Corrected the values to be specified with the -VECTN option	
		P40	Corrected the branch instruction to the _int_INTP0 label	
3.00	1	All	Changed the format of this document	
			Updated the version numbers of tools	



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(Rev.4.0-1 November 2017)

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