User Manual

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RH850 Evaluation Platform

RH850/V1R-M-292BGA PiggyBack board

RH850-V1RM-292PIN-PB-T1-V1

Renesas Electronics
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Chapter 1 Introduction

The RH850/V1R-M Application Board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics 32-bit RH850/V1R-M microcontroller. The PiggyBack board (RH850-V1RM-292PIN-PB-T1-V1) can be used as a standalone board, or can be mated with a mainboard (e.g. Y-RH850-X1X-MB-T1-V1) for extended functionality.

Main features:

- Socket for mounting of device
- Standalone operation of the board
- Direct supply of device voltage (typ. 3.3V and 1.25V)
- Device programming capability
- Device debugging capability
- Pin headers for direct access to each functional device pin
- Reset button
- MainOSC circuitry
- Connectors to MainBoard
- Operating temperature from 0°C to +40°C

This document describes the functionality provided by the PiggyBack board and guides the user through its operation.

For details regarding the operation of the microcontroller, refer to the RH850/V1R-M User's Manual.

Chapter 2 Overview

2.1 Overview

Figures 1 and 2 provide a schematic view of the PiggyBack board.

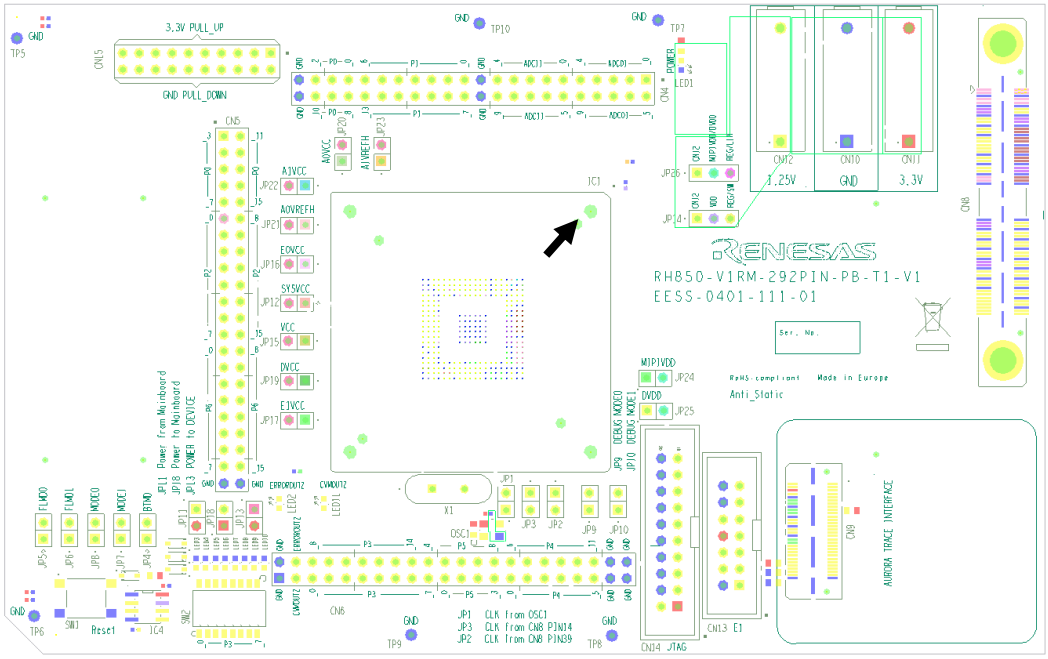


Figure 1 PiggyBack Board Schematic Top View

The black arrow denotes the position of socket pin #1.

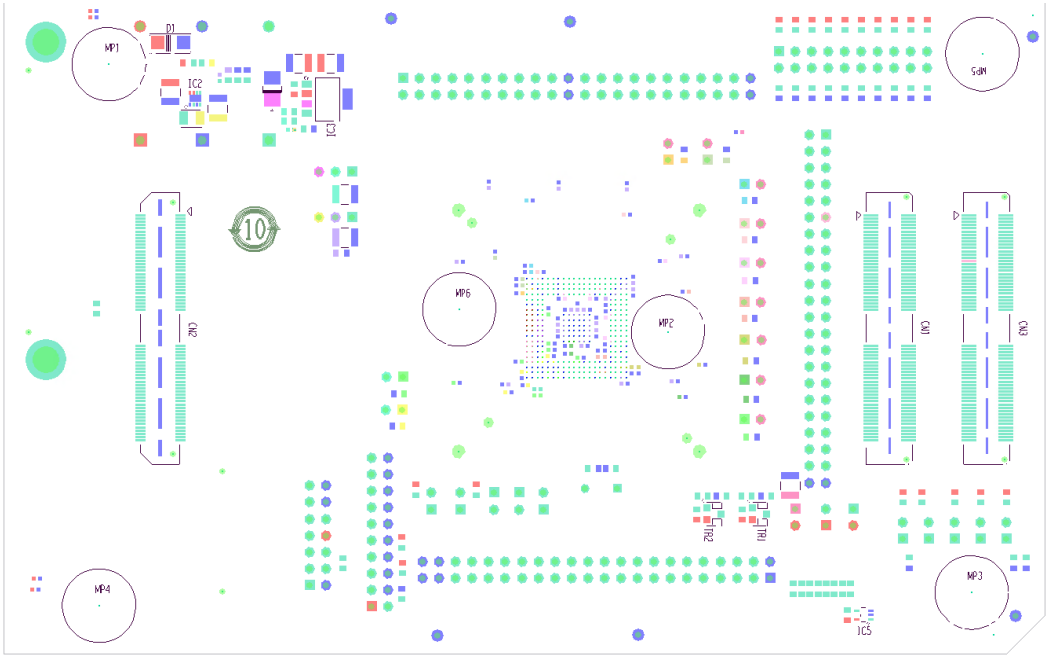


Figure 2 PiggyBack Board Schematic Bottom View

2.2 Mounting of the device

The board is designed for use with the following device:

RH850/V1R-M in BGA292 package.

The device must be placed inside the socket IC1. To insert the device align the corner of the device package marked with a white triangle with the pin #1 of the socket. The pin #1 of the socket is marked with a circle near to the “IC1” label (see also black arrow in Figure 1).

First insert the device into the socket with closed mount. Then press down the lid of the socket until the device slips into the socket and finally release the lid.

CAUTION: *Please follow the mounting instruction carefully as described. Otherwise the device might get damaged.*

Chapter 3 Power supply

3.1 Board power connection

For operation of the device, a supply voltage must be connected to the board. There are several possibilities to power the device.

Within this document the following voltages are considered as ‘typical’ connections:

- 3.3V
- 1.25V

Direct voltage supply

Two different voltages can be supplied to the board.

The following connectors are available to supply those voltages directly:

- Three 4mm ‘banana-type’ connectors:
  - Two red connectors for voltages *3.3V* (CN11) and *1.25V* (CN12).
  - A black connector for ground (GND) connection (CN10).
  Note: The three connectors are supplied with the board but not assembled.

For details about voltage distribution, refer to **Chapter 3.2 ‘Voltage distribution’**.

Supply by MainBoard

In case the PiggyBack board is mounted on a MainBoard, the voltage *3.3V* is supplied by the on-board regulator of the MainBoard.

CAUTION: *Do not supply 3.3V directly to the PiggyBack board in case it is mounted on the MainBoard.*

For each of the voltages, *3.3V* and *1.25V* a green LED is available to signal that the related voltage is available on the PiggyBack board. The corresponding LEDs are placed directly beneath the connectors of the related voltage.

3.2 Voltage distribution

The table below shows the required device power supply pins. For detailed explanation of their function, please refer to the user documentation of the device.

Voltage domain
VDD
MIPIVDDD
DVDD
VCC
SYSVCC
E0VCC
E1VCC
A0VCC
A0VREFH
A1VCC
A1VREFH
DVCC

Additional one power supply for the MainBoard can be selected:

Supply voltage	Function
VDDIOF	IO supply voltage for components located on a connected mainboard.

The following figure shows the configurable voltage distribution on the PiggyBack board.

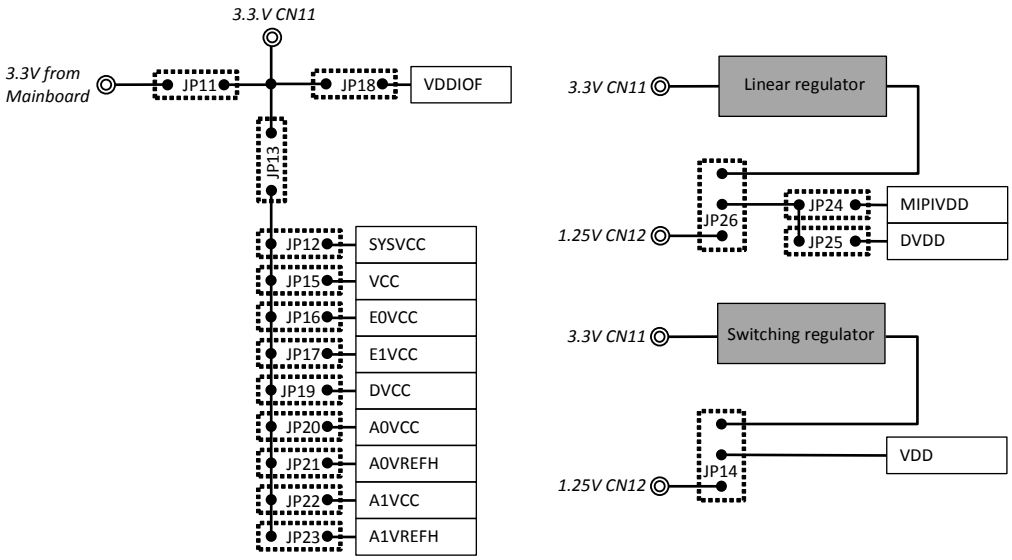


Figure 3 Voltage Distribution on the PiggyBack Board

- All power supply lines can be interrupted by jumpers. This provides the possibility to measure the current consumption of each individual power domain of the device.
- The IO supply voltage for the Mainboard (VDDIOF) can be connected via jumper JP18 to *Voltage1*, if the PiggyBack board is mounted on a MainBoard.
- VDD can be powered either directly from the ‘banana-type’ connector (*Voltage2* – CN12) or by on-board voltage regulators. Thereby the DPS device can be operated with one single voltage supply (*Voltage1)*. The source for VDD is selectable by jumper JP14.

Chapter 4 Clock sources

One external crystal oscillator for the device clock supply is provided with the board.

4.1 MainOsc

A crystal or ceramic resonator can be mounted on socket X1.

A 40MHz oscillator is supplied with the board.

4.2 Programmable Oscillator

It is possible to mount a programmable crystal oscillator on the PiggyBack board at OSC1. The available footprint and circuitry is designed for a SG-8002CE programmable crystal oscillator from Epson Toyocom. The output from this oscillator can be connected to port X1 of the device via jumper JP1. The SG-8002CE is neither mounted nor provided with the board. For details about the available circuitry refer to Error! Reference source not found. **‘**Error! Reference urce not found.**’**. A resonator mounted on socket X1 must not be used in parallel to another clock source.

4.3 Clock from the MIPI CSI2 Interface

It is possible to use a high speed clock source from a CSI2-transmitter. For this purpose the jumpers JP2 and JP3 are provided. For details about the operation and usage of the CSI2-clock please refer to the **Section 16 ‘MIPI-CSI2 (MCSIA)’** of **RH850/V1R-M User’s Manual**.

Chapter 5 Debug and Programming interface

For connection of the microcontroller debug and flash programming tools, the connectors CN13 (E1 emulator) and CN14 (JTAG), with 14 and 20 pins respectively, are provided. The board also allows the programmer to trace and debug via AURORA Trace Interface (CN9).

The signal connection of the debug and programming interfaces are shown in the table below:

V1R-M device pin	E1 emulator pin	DSP JTAG pin	AURORA IF pin
RESETZ	13*	15*	4*
P4_6 (RESETOUTZ)	-	-	19
FLMD0	4	-	-
FLMD1 (P4_5)	-	-	-
JP0_0	7	5	7
JP0_1	5	13	9
JP0_2	1	9+11	3
JP0_3	9	7	5
JP0_4	3	3	11
JP0_5	11	-	15
JP0_6	-	-	13
JP0_7	-	-	17
P4_0 (DEBUG_MODE0)	-	-	-
P4_1 (DEBUG_MODE1)	-	-	-
AURORES1Z	-	-	54
AURORES2Z	-	-	52
MSYNZ	-	-	50

5.1 Debug and Programming interface (E1 Emulator)

The signal connection of the E1 Emulator (14-pin connector CN13) is shown in the table below:

Device Port	CN13 Pin #	CN13 Pin #	Device Port
JP0_2	1	2	GND
JP0_4	3	4	FLMD0
JP0_1	5	6	NC
JP0_0	7	8	E1VCC
JP0_3	9	10	NC
JP0_5	11	12	GND
RESETZ	13	14	GND

5.2 Debug and Trace (AURORA Interface)

The signal connection of the AURORA Trace Interface (60-pin connector CN9) is shown in the table below:

Direction/Level	Device Port	CN9 Pin #	CN9 Pin#	Device Port	Direction/Level
-	-	1	2	-	-
input / E1VCC(3.3V)	JP0_2 (TCK)	3	4	See RESET chapter	bidir / SYSVCC(3.3V)
input / E1VCC(3.3V)	JP0_3 (TMS)	5	6	E1VCC (3.3V)	E1VCC (3.3V)
input / E1VCC(3.3V)	JP0_0 (TDI)	7	8	-	-
output / E1VCC(3.3V)	JP0_1 (TDO)	9	10	GND	-
input / E1VCC(3.3V)	JP0_4 (TRSTZ)	11	12	TODP0	output / diff (DVCC 3.3V)
output / E1VCC(3.3V)	JP0_6 (EVTOZ)	13	14	TODN0	output / diff (DVCC 3.3V)
output / E1VCC(3.3V)	JP0_5 (RDYZ)	15	16	GND	-
input / E1VCC(3.3V)	JP0_7 (EVTIZ)	17	18	TODP1	output / diff (DVCC 3.3V)
output / E1VCC(3.3V)	P4_6 (RESETOUTZ)	19	20	TODN1	output / diff (DVCC 3.3V)
-	-	21	22	GND	-
-	-	23	24	-	-
-	-	25	26	-	-
-	-	27	28	GND	-
-	-	29	30	-	-
-	-	31	32	-	-
-	-	33	34	GND	-
-	-	35	36	CICREFP	input / diff (DVCC 3.3V)
-	-	37	38	CICREFN	input / diff (DVCC 3.3V)
-	-	39	40	-	-
-	-	41	42	-	-
-	-	43	44	-	-
-	-	45	46	-	-
-	-	47	48	-	-
-	-	49	50	MSYNZ	input / E1VCC(3.3V)
-	-	51	52	AURORES2Z	input / E1VCC(3.3V)
-	-	53	54	AURORES1Z	input / E1VCC(3.3V)
-	-	55	56	-	-
-	-	57	58	-	-
-	GND	59	60	GND	-

5.3 JTAG Debug (DSP)

The signal connection of the JTAG interface (20-pin connector CN14) is shown in the table below:

Device Port	CN14 Pin #	CN14 Pin #	Device Port
E1VCC	1	2	-
JP0_4 (TRSTZ)	3	4	GND
JP0_0 (TDI)	5	6	GND
JP0_3 (TMS)	7	8	GND
JP0_2 (TCK)	9	10	GND
JP0_2 (TCK)	11	12	GND
JP0_1 (TDO)	13	14	GND
See RESET chapter	15	16	GND
-	17	18	GND
-	19	20	GND

The debug system supports following modes by the jumpers JP9 (DEBUG_MODE1) and JP10 (DEBUG_MODE0). The supported debugging modes are shown in the table below:

DEBUG_MODE1	DEBUG_MODE0	Mode	
0	0	Chain mode	RH850 and DSP are connected as a chain
0	1	RH850 mode	Debug target is RH850
1	0	DSP mode	Debug target is DSP
1	1	-	Setting is prohibited

For more details about available debug modes please refer to the **Section 34 'On-chip Debug Unit (OCD)'** of **RH850/V1R-M User's Manual**.

Chapter 6 Connectors for ports of device

Connection to each functional pin of the device is possible via the connectors CN4 to CN6. For detailed explanation of their function, please refer to the user documentation of the device.

The following signals/device ports are not available at the connectors CN4 to CN6:

Device Port
TODP0
TODN0
TODP1
TODN1
CICREFP
CICREFN
AUDATA0
AUDATA1
AUDATA2
AUDATA3
AUDCK
AUDSYNCZ
AUDRSTZ
MIPIxDPy
MIPIxDNy
MIPIxCPy
MIPIxCNy

CAUTION: *The pin headers are directly connected to the pins of the device, therefore special care must be taken to avoid any electrostatic or other damage to the device.*

6.1 GPIO and ADC connections

Three 44-pin connectors (CN4, CN5 and CN6) are available to access GPIO and ADC ports of V1R-M. For details about their purpose and usage please refer to **Section 2 'Pin Functions'** and **Section 30 'AD Converter'** of **RH850/V1R-M User's Manual**.

6.1.1 Connector CN4

Device Port	CN4 Pin #	CN4 Pin#	Device Port
ADC0I0	1	2	ADC0I5
ADC0I1	3	4	ADC0I6
ADC0I2	5	6	ADC0I7
ADC0I3	7	8	ADC0I8
ADC0I4	9	10	ADC0I9
ADC1I0	11	12	ADC1I5
ADC1I1	13	14	ADC1I6
ADC1I2	15	16	ADC1I7
ADC1I3	17	18	ADC1I8
ADC1I4	19	20	ADC1I9
GND	21	22	GND
P1_0	23	24	P1_7
P1_1	25	26	P1_8
P1_2	27	28	P1_9
P1_3	29	30	P1_10
P1_4	31	32	P1_11
P1_5	33	34	P1_12
P1_6	35	36	P1_13
P0_0	37	38	P0_8
P0_1	39	40	P0_9
P0_2	41	42	P0_10
GND	43	44	GND

6.1.2 Connector CN5

Device Port	CN5 Pin #	CN5 Pin#	Device Port
P0_3	1	2	P0_11
P0_4	3	4	P0_12
P0_5	5	6	P0_13
P0_6	7	8	P0_14
P0_7	9	10	P0_15
P2_0	11	12	P2_8
P2_1	13	14	P2_9
P2_2	15	16	P2_10
P2_3	17	18	P2_11
P2_4	19	20	P2_12
P2_5	21	22	P2_13
P2_6	23	24	P2_14
P2_7	25	26	P2_15
P6_0	27	28	P6_8
P6_1	29	30	P6_9
P6_2	31	32	P6_10
P6_3	33	34	P6_11
P6_4	35	36	P6_12
P6_5	37	38	P6_13
P6_6	39	40	P6_14
P6_7	41	42	P6_15
GND	43	44	GND

6.1.3 Connector CN6

Device Port	CN6 Pin #	CN6 Pin#	Device Port
GND	1	2	GND
CVMOUTZ	3	4	ERROROUTZ
P3_0	5	6	P3_8
P3_1	7	8	P3_9
P3_2	9	10	P3_10
P3_3	11	12	P3_11
P3_4	13	14	P3_12
P3_5	15	16	P3_13
P3_6	17	18	P3_14
P3_7	19	20	P5_4
P5_0	21	22	P5_5
P5_1	23	24	P5_6
P5_2	25	26	P5_7
P5_3	27	28	P5_8
P4_0	29	30	P4_6
P4_1	31	32	P4_7
P4_2	33	34	P4_8
P4_3	35	36	P4_9
P4_4	37	38	P4_10
P4_5	39	40	P4_11
GND	41	42	GND
GND	43	44	GND

6.2 Push button for RESET

In order to issue a RESET to the device, the push-button SW1 is available.

6.3 Mode Selection

The PiggyBack Board gives the possibility to configure the following mode pins:

- FLMD0 via jumper JP5
- FLMD1 via jumper JP6
- MODE0 via jumper JP8
- MODE1 via jumper JP7

To apply “High” to the mode pins, the corresponding jumper must be shorted.

Note: The mode pins FLMD0 und FLMD1 are connected to pull-down resistors, therefore they are “Low” by default (when the jumpers JP5 and JP6 are not shorted)

CAUTION: *Be careful in configuration of mode related pins, as wrong configuration can cause irregular behavior of the devices. Be sure to check the corresponding User Manual, for details, which modes can be selected for the device.*

6.4 TFT touch screen display

When using the MainBoard RH850-X1X-MB-T2-V2, it is possible to interface to a TFT display and a touch controller. For details, refer to the MainBoard documentation. The signals used to interface are as follows:

Device Port	Display function	Shield pin	Mainboard Pin
P6_4	RESETZ	RESETZ	DIGIO[4]
P4_8	TFT_DC	D9 (/D6)	PWM[25]
P2_0	SPI_SCK	D13 / SPI_SCK	PWM[28]
P2_1	SPI_MOSI	D11 / SPI_MOSI	PWM[27]
P2_3	SPI_MISO	D12 / SPI_MISO	PWM[29]
P2_9	SPI_SS_TFT	D10 / SPI_SS (/D5)	PWM[20]
P2_6	SPI_SS_TOUCH_R	D8	PWM[21]
P4_9	SPI_SS_microSD	D4	PWM[09]
P4_10	I2C_SCL_TOUCH_C	A5 / SCL	IIC0_SCL
P4_11	I2C_SDA_TOUCH_C	A4 / SDA	IIC0_SDA
P3_11	(INT_TOUCH)	D7	PWM[38]

6.5 Connectors to MainBoard

Three connectors (CN1, CN2 and CN3) are available to connect the PiggyBack board to a MainBoard. Regarding the function on the MainBoard, please refer to User Manuals of supported MainBoards.

6.5.1 Connector CN1

Pin	Function on MainBoard	Device Port		Pin	Function on MainBoard	Device Port
1	5.0V	-		2	5.0V	-
3	5.0V	-		4	5.0V	-
5	RESETZ	See RESET		6	NMI	P3_14
7	WAKE	-		8	-	-
9	INT0	P3_8		10	INT1	P3_9
11	- (INT2)	P3_10		12	- (INT3)	P3_11
13	-	-		14	-	-
15	UART0_TX	P5_4		16	UART1_TX	-
17	UART0_RX	P5_5		18	UART1_RX	-
19	LIN0_TX	P5_4		20	LIN1_TX	-
21	LIN0_RX	P5_5		22	LIN1_RX	-
23	IIC0_SCL	P4_10		24	IIC1_SCL	-
25	IIC0_SDA	P4_11		26	IIC1_SDA	-
27	CAN0_TX	P5_1		28	CAN1_TX	P5_6
29	CAN0_RX	P5_0		30	CAN1_RX	P5_7
31	SENT0_IN	-		32	SENT1_IN	-
33	SENT0_OUT	-		34	SENT1_OUT	-
35	PSI50_RX	-		36	PSI51_RX	-
37	PSI50_TX	-		38	PSI51_TX	-
39	PSI50_SYNC	-		40	PSI51_SYNC	-
41	FLX0_TX	P0_14		42	FLX0_TXENZ	P1_0
43	FLX0_RX	P0_3		44	-	-
45	FLX1_TX	P0_13		46	FLX1_TXENZ	P1_5
47	FLX1_RX	P0_2		48	FLX_RESERVED	-
49	-	-		50	-	-
51	ETH0_MDIO	P0_8		52	ETH0_MDC	P0_7
53	ETH0_RXD0	P0_3		54	ETH0_TXD0	P0_12
55	ETH0_RXD1	P0_2		56	ETH0_TXD1	P1_2
57	ETH0_RXD2	P1_5		58	ETH0_TXD2	P0_14
59	ETH0_RXD3	P1_0		60	ETH0_TXD3	P0_13
61	ETH0_RXDCLK	P1_4		62	ETH0_TXCLK	P1_3
63	ETH0_RXER	P0_4		64	ETH0_TXER	P0_15
65	ETH0_CRS	P0_5		66	ETH0_TXEN	P0_1
67	ETH0_RXDV	P0_11		68	ETH0_COL	P0_6
69	ETH0_RESETZ	P0_10		70	ETH0_LINK	P0_9
71	-	-		72	-	-

73	USB0F_DM	-		74	USB0H_DM	-
75	USB0F_DP	-		76	USB0H_DP	-
77	-	-		78	-	-
79	-	-		80	-	-
81	-	-		82	-	-
83	-	-		84	-	-
85	DIGIO_0	P6_0		86	DIGIO_1	P6_1
87	DIGIO_2	P6_2		88	DIGIO_3	P6_3
89	DIGIO_4	P6_4		90	DIGIO_5	P6_5
91	DIGIO_6	P6_6		92	DIGIO_7	P6_7
93	DIGIO_8	P6_8		94	DIGIO_9	P6_9
95	DIGIO_10	P6_10		96	DIGIO_11	P6_11
97	DIGIO_12	P6_12		98	DIGIO_13	P6_13
99	DIGIO_14	P6_14		100	DIGIO_15	P6_15
101	-	-		102	-	-
103	MUX0	-		104	MUX1	-
105	MUX2	-		106	-	-
107	ADC0	ADC0I0		108	ADC1	ADC0I1
109	ADC2	ADC0I2		110	ADC3	ADC0I3
111	ADC4	ADC0I4		112	ADC5	ADC0I5
113	ADC6	ADC0I6		114	ADC7	ADC0I7
115	VDDIOF	3.3V		116	VDDIOF	3.3V
117	3.3V	3.3V		118	3.3V	3.3V
119	3.3V	3.3V		120	3.3V	3.3V

6.5.2 Connector CN2

Pin	Function on MainBoard	Device Port		Pin	Function on MainBoard	Device Port
1	CAN2_TX	P5_2		2	CAN3_TX	-
3	CAN2_RX	P5_3		4	CAN3_RX	-
5	CAN4_TX	-		6	CAN5_TX	-
7	CAN4_RX	-		8	CAN5_RX	-
9	LIN2_TX	-		10	LIN3_TX	-
11	LIN2_RX	-		12	LIN3_RX	-
13	LIN4_TX	-		14	LIN5_TX	-
15	LIN4_RX	-		16	LIN5_RX	-
17	LIN6_TX	-		18	LIN7_TX	-
19	LIN6_RX	-		20	LIN7_RX	-
21	LIN8_TX	-		22	LIN9_TX	-
23	LIN8_RX	-		24	LIN9_RX	-
25	LIN10_TX	-		26	LIN11_TX	-
27	LIN10_RX	-		28	LIN11_RX	-
29	LIN12_TX	-		30	LIN13_TX	-
31	LIN12_RX	-		32	LIN13_RX	-

33	LIN14_TX	-		34	LIN15_TX	-
35	LIN14_RX	-		36	LIN15_RX	-
37	-	-		38	-	-
39	-	-		40	-	-
41	MLB_CLK	-		42	MLB_RESET	-
43	MLB_SIG	-		44	MLB_DAT	-
45	-	-		46	-	-
47	CAN6_TX	-		48	CAN7_TX	-
49	CAN6_RX	-		50	CAN7_RX	-
51	-	-		52	-	-
53	-	-		54	-	-
55	-	-		56	-	-
57	-	-		58	-	-
59	-	-		60	-	-
61	-	-		62	-	-
63	-	-		64	-	-
65	-	-		66	-	-
67	-	-		68	-	-
69	-	-		70	-	-
71	-	-		72	-	-
73	-	-		74	-	-
75	-	-		76	-	-
77	-	-		78	-	-
79	-	-		80	-	-
81	-	-		82	-	-
83	-	-		84	-	-
85	-	-		86	-	-
87	-	-		88	-	-
89	-	-		90	-	-
91	-	-		92	-	-
93	-	-		94	-	-
95	-	-		96	-	-
97	-	-		98	-	-
99	-	-		100	-	-
101	-	-		102	-	-
103	-	-		104	-	-
105	-	-		106	-	-
107	-	-		108	-	-
109	-	-		110	-	-
111	-	-		112	-	-
113	-	-		114	-	-
115	-	-		116	-	-
117	-	-		118	-	-
119	-	-		120	-	-

6.5.3 Connector CN3

Pin	Function on MainBoard	Device Port		Pin	Function on MainBoard	Device Port
1	PWM[00]	-		2	PWM[01]	-
3	PWM[02]	-		4	PWM[03]	-
5	PWM[04]	-		6	PWM[05]	-
7	PWM[06]	-		8	PWM[07]	-
9	PWM[08]	-		10	PWM[09]	P4_9
11	PWM[10]	-		12	PWM[11]	-
13	PWM[12]	-		14	PWM[13]	-
15	PWM[14]	-		16	PWM[15]	-
17	PWM[16]	-		18	PWM[17]	-
19	PWM[18]	-		20	PWM[19]	-
21	PWM[20]	P2_9		22	PWM[21]	P2_6
23	PWM[22]	-		24	PWM[23]	-
25	PWM[24]	-		26	PWM[25]	P4_8
27	PWM[26]	-		28	PWM[27]	P2_1
29	PWM[28]	P2_0		30	PWM[29]	P2_3
31	PWM[30]	-		32	PWM[31]	-
33	PWM[32]	-		34	PWM[33]	-
35	PWM[34]	-		36	PWM[35]	-
37	PWM[36]	-		38	PWM[37]	-
39	PWM[38]	P3_11		40	PWM[39]	-
41	PWM[40]	-		42	PWM[41]	-
43	PWM[42]	-		44	PWM[43]	-
45	PWM[44]	-		46	PWM[45]	-
47	PWM[46]	-		48	PWM[47]	-
49	PWM[48]	-		50	PWM[49]	-
51	PWM[50]	-		52	PWM[51]	-
53	PWM[52]	-		54	PWM[53]	-
55	PWM[54]	-		56	PWM[55]	-
57	PWM[56]	-		58	PWM[57]	-
59	PWM[58]	-		60	PWM[59]	-
61	PWM[60]	-		62	PWM[61]	-
63	PWM[62]	-		64	PWM[63]	-
65	PWM[64]	-		66	PWM[65]	-
67	PWM[66]	-		68	PWM[67]	-
69	PWM[68]	-		70	PWM[69]	-
71	PWM[70]	-		72	PWM[71]	-
73	PWM[72]	-		74	PWM[73]	-
75	PWM[74]	-		76	PWM[75]	-
77	PWM[76]	-		78	PWM[77]	-
79	PWM[78]	-		80	PWM[79]	-
81	PWMADC[00]	-		82	PWMADC[01]	-

83	PWMADC[02]	-		84	PWMADC[03]	-
85	PWMADC[04]	-		86	PWMADC[05]	-
87	PWMADC[06]	-		88	PWMADC[07]	-
89	PWMADC[08]	-		90	PWMADC[09]	-
91	PWMADC[10]	-		92	PWMADC[11]	-
93	PWMADC[12]	-		94	PWMADC[13]	-
95	PWMADC[14]	-		96	PWMADC[15]	-
97	NC	-		98	NC	-
99	NC	-		100	NC	-
101	NC	-		102	NC	-
103	NC	-		104	NC	-
105	NC	-		106	NC	-
107	NC	-		108	NC	-
109	NC	-		110	NC	-
111	NC	-		112	NC	-
113	NC	-		114	NC	-
115	NC	-		116	NC	-
117	NC	-		118	NC	-
119	NC	-		120	NC	-

Chapter 7 Additional circuitry

7.1 MIPI CSI2 and HS-SPI connector

The PiggyBack board has the MIPI CSI2 connector (CN8) for connecting a CSI2 source. The connector for HS-SPI slaves/counterparts is shared with the MIPI CSI connector. The pinout is shown in the table below:

Pin	Group	MCU Port	MCU Function	Direction	Level
1	CSI2 ch2	MIPI1DN2	MIPI1DN2	I	(CSI2)
3	CSI2 ch2	MIPI1DP2	MIPI1DP2	I	(CSI2)
5	Power	GND	GND	P	0V
7	CSI2 ch2	MIPI1DN3	MIPI1DN3	I	(CSI2)
9	CSI2 ch2	MIPI1DP3	MIPI1DP3	I	(CSI2)
11	Power	GND	GND	P	0V
13	CSI2 ch3	MIPI2DN1	MIPI2DN1	I	(CSI2)
15	CSI2 ch3	MIPI2DP1	MIPI2DP1	I	(CSI2)
17	Power	GND	GND	P	0V
19	SPI ch3	P1_10	HSPI0_SPCK	O	3.3V
21	SPI ch3	P1_9	HSPI0_RX	I	3.3V
23	Power	GND	GND	P	0V
25	SPI ch3	P1_13	HSPI0_SSL0	O	3.3V
27	SPI ch3	P1_6	HSPI0_TX	O	3.3V
29	Power	GND	GND	P	0V
31	NC	NC	-	-	-
33	NC	NC	-	-	-
35	NC	NC	-	-	-
37	NC	NC	-	-	-
39	System	X1, via 0-ohm	X1	I	3.3V
41	Power	GND	GND	P	0V
43	GPIO	P6_0	GPIO	IO	3.3V
45	GPIO	P6_1	GPIO	IO	3.3V
47	Power	GND	GND	P	0V
49	GPIO	P4_10	GPIO	IO	3.3V
51	GPIO	P4_11	GPIO	IO	3.3V
53	Power	GND	GND	P	0V
55	CSI2 ch2	MIPI1DNCK	MIPI1DNCK	I	(CSI2)
57	CSI2 ch2	MIPI1DPCK	MIPI1DPCK	I	(CSI2)
59	Power	GND	GND	P	0V
61	Power	GND	GND	P	0V
63	CSI2 ch3	MIPI2DN2	MIPI2DN2	I	(CSI2)
65	CSI2 ch3	MIPI2DP2	MIPI2DP2	I	(CSI2)
67	Power	GND	GND	P	0V
69	GPIO	P6_2	GPIO	IO	3.3V
71	GPIO	P6_3	GPIO	IO	3.3V
73	Power	GND	GND	P	0V
75	GPIO	P6_5	GPIO	IO	3.3V
77	GPIO	P6_6	GPIO	IO	3.3V

79	Power	GND	GND	P	0V
81	GPIO	P6_7	GPIO	IO	3.3V
83	GPIO	P6_8	GPIO	IO	3.3V
85	Power	GND	GND	P	0V
87	CSI2 ch3	MIPI2DN3	MIPI2DN3	I	(CSI2)
89	CSI2 ch3	MIPI2DP3	MIPI2DP3	I	(CSI2)
91	Power	GND	GND	P	0V
93	GPIO	P4_4	GPIO	IO	3.3V
95	GPIO	P4_7	GPIO	IO	3.3V
97	Power	GND	GND	P	0V
99	GPIO	P6_9	GPIO	IO	3.3V
101	GPIO	P6_10	GPIO	IO	3.3V
103	Power	GND	GND	P	0V
105	System	P2_2	GPIO	O	3.3V
107	System	P2_10	GPIO	O	3.3V
109	System	P2_12	GPIO	O	3.3V
111	System	P1_8	GPIO	O	3.3V
113	System	P1_11	GPIO	IO, OD	3.3V
115	System	P2_4	GPIO	O	3.3V
117	NC	NC	-	-	-
119	Board detect	(to CN-pin16)	-	O	3.3V
2	CSI2 ch2	MIPI1DN0	MIPI1DN0	I	(CSI2)
4	CSI2 ch2	MIPI1DP0	MIPI1DP0	I	(CSI2)
6	Power	GND	GND	P	0V
8	CSI2 ch2	MIPI1DN1	MIPI1DN1	I	(CSI2)
10	CSI2 ch2	MIPI1DP1	MIPI1DP1	I	(CSI2)
12	Power	GND	GND	P	0V
14	System	X1, via 0-ohm	X1	I	3.3V
16	Power	(to CN-pin119)	-	PI	3.3V
18	Power	GND	GND	P	0V
20	CSI2 ch3	MIPI2DN0	MIPI2DN0	I	(CSI2)
22	CSI2 ch3	MIPI2DP0	MIPI2DP0	I	(CSI2)
24	Power	GND	GND	P	0V
26	CSI2 ch1	MIPI0DN3	MIPI0DN3	I	(CSI2)
28	CSI2 ch1	MIPI0DP3	MIPI0DP3	I	(CSI2)
30	Power	GND	GND	P	0V
32	CSI2 ch1	MIPI0DN2	MIPI0DN2	I	(CSI2)
34	CSI2 ch1	MIPI0DP2	MIPI0DP2	I	(CSI2)
36	Power	GND	GND	P	0V
38	CSI2 ch1	MIPI0DN1	MIPI0DN1	I	(CSI2)
40	CSI2 ch1	MIPI0DP1	MIPI0DP1	I	(CSI2)
42	Power	GND	GND	P	0V
44	CSI2 ch1	MIPI0DN0	MIPI0DN0	I	(CSI2)
46	CSI2 ch1	MIPI0DP0	MIPI0DP0	I	(CSI2)
48	Power	GND	GND	P	0V
50	CSI2 ch3	MIPI2DNCK	MIPI2DNCK	I	(CSI2)
52	CSI2 ch3	MIPI2DPCK	MIPI2DPCK	I	(CSI2)
54	Power	GND	GND	P	0V

56	CSI2 ch1	MIPI0DNCK	MIPI0DNCK	I	(CSI2)
58	CSI2 ch1	MIPI0DPCK	MIPI0DPCK	I	(CSI2)
60	Power	GND	GND	P	0V
62	Power	GND	GND	P	0V
64	SPI ch2	P1_12	HSPI1_RX	I	3.3V
66	SPI ch2	P3_9	INTP9	I	3.3V
68	Power	GND	GND	P	0V
70	SPI ch2	P2_7	HSPI1_SSL0	O	3.3V
72	SPI ch2	P2_8	HSPI1_TX	O	3.3V
74	Power	GND	GND	P	0V
76	SPI ch2	P1_7	HSPI1_SPCK	O	3.3V
78	SPI ch1	P2_14	HSPI0_RX	I	3.3V
80	Power	GND	GND	P	0V
82	SPI ch1	P3_8	INTP8	I	3.3V
84	SPI ch1	P2_11	HSPI0_SSL0	O	3.3V
86	Power	GND	GND	P	0V
88	SPI ch1	P2_15	HSPI0_TX	O	3.3V
90	SPI ch1	P2_13	HSPI0_SPCK	O	3.3V
92	Power	GND	GND	P	0V
94	UART ch1	P5_5	RLIN30RX	I	3.3V
96	UART ch1	P5_4	RLIN30TX	O	3.3V
98	Power	GND	GND	P	0V
100	GPIO	P6_11	GPIO	IO	3.3V
102	GPIO	P6_12	GPIO	IO	3.3V
104	Power	GND	GND	P	0V
106	GPIO	P1_1	GPIO	IO	3.3V
108	GPIO	P3_12	GPIO	IO	3.3V
110	Power	GND	GND	P	0V
112	GPIO	P6_13	GPIO	IO	3.3V
114	GPIO	P6_14	GPIO	IO	3.3V
116	Power	GND	GND	P	0V
118	GPIO	P6_15	GPIO	IO	3.3V
120	GPIO	P5_8	GPIO	IO	3.3V

7.2 Signaling for CVMOUTZ and ERROROUTZ

Two red LEDs, LED2 and LED11 are available two indicate a “low” output signal from CVMOUTZ and ERROROUTZ, respectively.

7.3 Pin Headers for Pull-Down and Pull-Up

A connector CN15 is available to enable easy connection to Voltage1 (3.3V) or GND via pull-up or pull-down resistances, respectively.

Hereby uneven pins from 1 to 19 (in total ten) are configured as pull-up pin headers, while the even numbers from 2 to 20 (in total ten) can be used for pull-down.

By connecting device port pins from CN4 – 6 to CN15 it is therefore possible to pull a desired port pin to “Low” or “High”.

7.4 GPIO LEDs

There are 8 LEDs (LED3 – LED10) connected to GPIO port P3 (pins 7:0) of the device. It is possible to enable or disable function of the LEDs with the switch SW2. Connections between GPIO LEDs and pins of the switch are shown in the table below:

GPIO Pin	LED Designator	DIP Switch SW2
P3_0	LED3	S1
P3_1	LED4	S2
P3_2	LED5	S3
P3_3	LED6	S4
P3_4	LED7	S5
P3_5	LED8	S6
P3_6	LED9	S7
P3_7	LED10	S8

Note: for the Y-RH850-V1RM-292PIN-PB-T1-V1 boards with serial numbers

0001, 0004, 0005, 0007, 0010, 0013, 0014, 0015, 0016, 0021, 0023, 0024, 0026, 0027, 0028, 0029, 0030, 0031, 0032, 0033

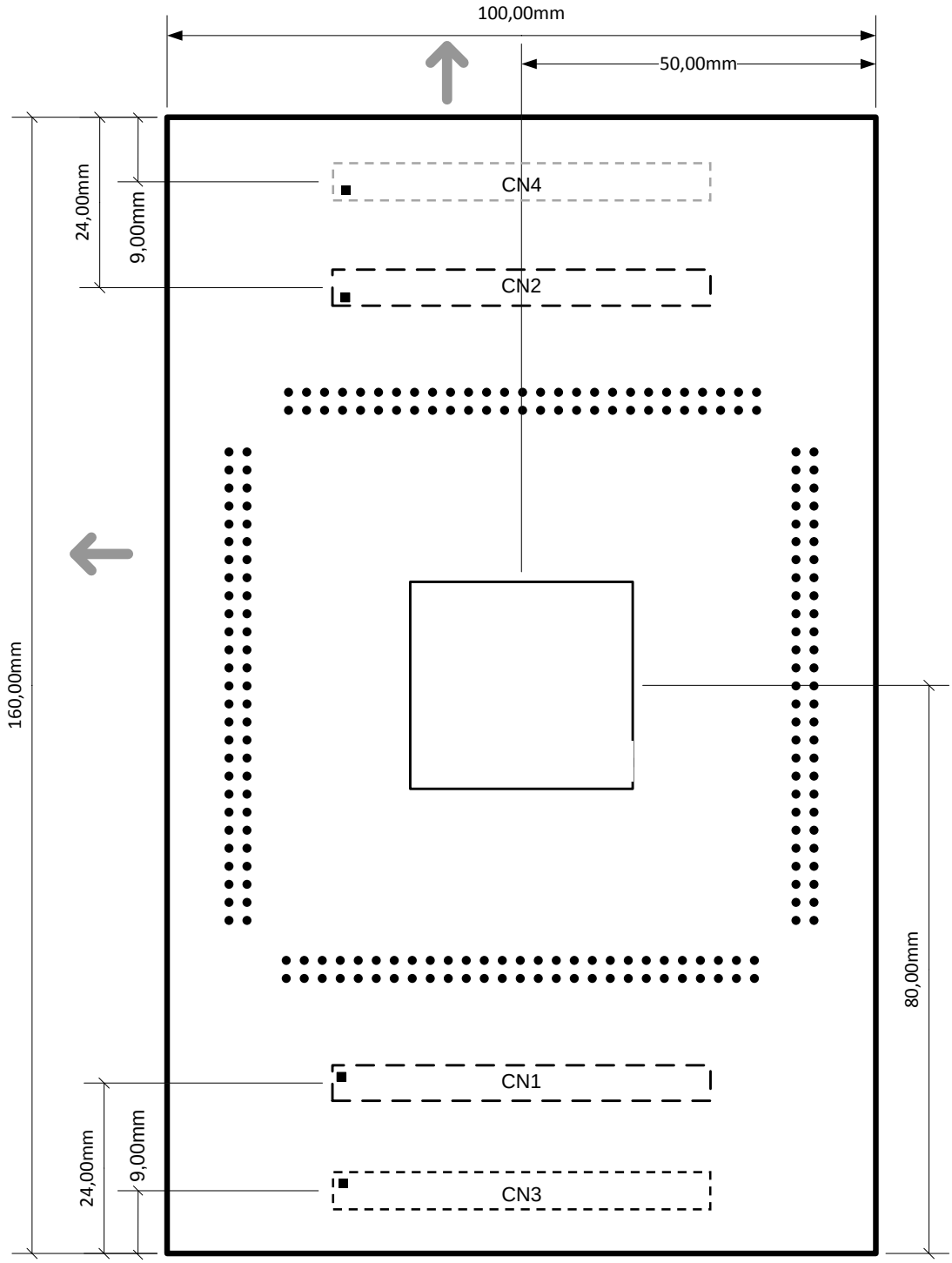
there is different SW2 switch order corresponding to the GPIO LEDs:

GPIO Pin	LED Designator	DIP Switch SW2
P3_0	LED3	S8
P3_1	LED4	S7
P3_2	LED5	S6
P3_3	LED6	S5
P3_4	LED7	S4
P3_5	LED8	S3
P3_6	LED9	S2
P3_7	LED10	S1

Chapter 8 Precautions

No limitations are known at the release of this document.

Chapter 9 Mechanical dimensions



Chapter 10 Revision History

The table provides information about the major changes of the document versions.

Date	Version	Description
2016-02-15	1.0	Initial release
2016-08-18	1.01	Added a note for boards with the reverse order of the GPIO LEDs switch

Appendix A Schematic

CAUTION: *The schematic shown in this document is not intended to be used as a reference for mass production. Any usage in an application design is in sole responsibility of the customer.*

The following components described in the schematic are provided with but not mounted on the board:

- Standard 4mm power lab sockets
  - CN10
  - CN11
  - CN12

REV	COMMENT	DATE	DRAWN BY
1.00	Release	06/12/2015	R.Romes

Device Socket and Connectors

header row 2.54mm

header 44way CN4

header 44way CN5

header 44way CN6

CVMOUTZ

ERROROUTZ

RH850/V1RM 292BGA

P0<15..0>
P1<13..0>
P2<15..0>
P3<14..0>
P4<11..0>
P5<8..0>
P6<15..0>
JP0<7..0>
ADC0I<9..0>
ADC1I<9..0>

VDD 1.25V
MIPIVDD 1.25V
DVDD 1.25V
E0VCC 3.3V
E1VCC 3.3V
DVCC 3.3V
VCC 3.3V
SYSVCC 3.3V
A0VCC 3.3V
A1VCC 3.3V
A0VREFH 3.3V
A1VREFH 3.3V

Ports
JTAG I/F
ADC
Sys Ctrl
Camera I/F
Trace I/F

RH850_V1RM-292bga+enp_socket
IC1

CVMOUTZ
ERROROUTZ
FLMD0
RESET_Z
RESETZ

MIPI0DP[3..0]
MIPI0DN[3..0]
MIPI0DPCK
MIPI0DNCK
MIPI1DP[3..0]
MIPI1DN[3..0]
MIPI1DPCK
MIPI1DNCK
MIPI2DP[3..0]
MIPI2DN[3..0]
MIPI2DPCK
MIPI2DNCK

TODP[1..0]
TODN[1..0]
MSYNZ
AURORESZ2
AURORESZ1

CICREFP
CICREFN

SG8002CE-40MHz
OSC1
OE CLK
GND VCC
1K0 R1
C20 100n
JP1 JP2 JP3
X1
40.000 MHz + socket
18pF
C21 4.7p
C23 4.7p
X1_B
X1_C

VSS[34..1]
OSCVSS[2..1]
MIPIVSS0[9..1]
EVSS[5..1]
DVSS[15..1]
A0VSS[6..1]
A1VSS[5..1]

plane decoupling
C66 C67 C68 C69 C70 C71 C72 C73 470p 470p 470p 470p 470p 100p 100p 10n
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 470p 100n 100n 470p 100n 100n 470p 470p 100n 100n 100n 470p
C13 C14 C15 C16 100n 100n 100n 100n
C17 C18 C19 100n 100n 100n
C22 C24 100n 100n
C25 100n
C26 C27 100n 100n
C28 100n
C29 100n
C30 C31 C32 C33 100n 100n 100n 100n
C35 C37 100n 100n
C38 C39 100n 100n
C40 C41 100n 100n

MIPI CSI2 i/f

QSH-060-01-L-D-A-RT1
CN8

MIPI1DN<2>
MIPI1DP<2>
MIPI1DN<3>
MIPI1DP<3>
MIPI2DN<1>
MIPI2DP<1>
P1<10>
P1<9>
P1<13>
P1<6>
X1_C
P6<0>
P6<1>
P4<10>
P4<11>
MIPI1DNCK
MIPI1DPCK
MIPI2DN<2>
MIPI2DP<2>
P6<2>
P6<3>
P6<5>
P6<6>
P6<7>
P6<8>
MIPI2DN<3>
MIPI2DP<3>
P4<4>
P4<7>
P6<9>
P6<10>
P2<2>
P2<10>
P2<12>
P1<8>
P1<11>
P2<4>
BOARD_DET
MIPI1DN<0>
MIPI1DP<0>
MIPI1DN<1>
MIPI1DP<1>
X1_B
BOARD_DET
MIPI2DN<0>
MIPI2DP<0>
MIPI0DN<3>
MIPI0DP<3>
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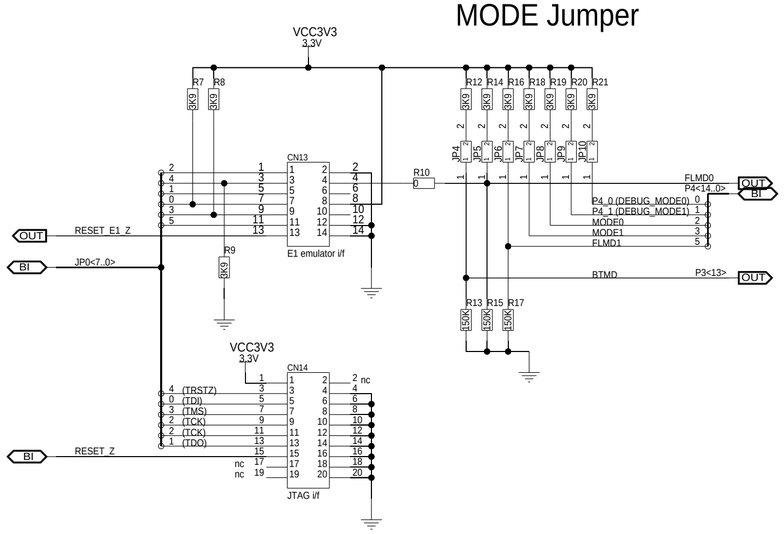
MIPI0DP<1>
MIPI0DN<0>
MIPI0DP<0>
MIPI2DNCK
MIPI2DPCK
MIPI0DNCK
MIPI0DPCK
P1<12>
P3<9>
P2<7>
P2<8>
P1<7>
P2<14>
P3<8>
P2<11>
P2<15>
P2<13>
P5<5>
P5<4>
P6<11>
P6<12>
P1<1>
P3<12>
P6<13>
P6<14>
P6<15>
P5<8>

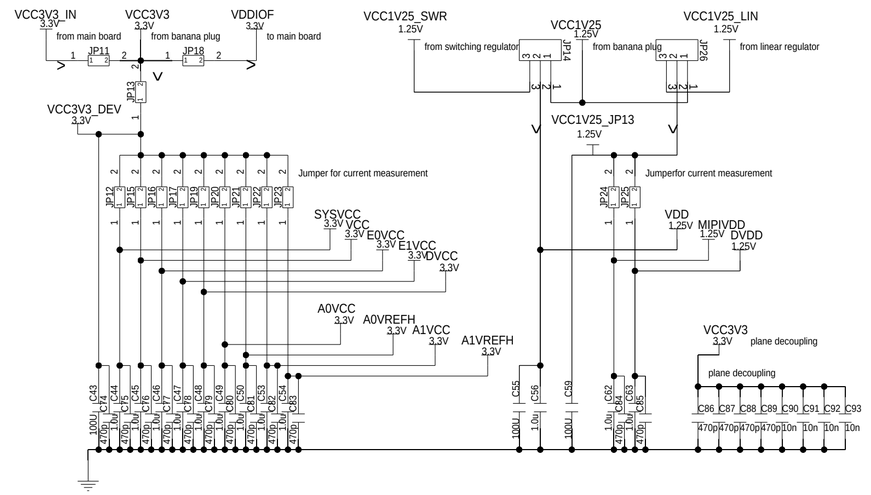
AURORA Trace i/f

VCC3V3 3.3V
R3 6K9
R4 6K9
QTH-030-01-L-D-A
CN9
(TCK)
(TMS)
(TDI)
(TDO)
(TRSTZ)
(EVTOZ)
(RDYZ)
(EVTIZ)
(RESETOUTZ)
P4<6>
JP0<7..0>
RESET_Z
TODP<1..0>
TODN<1..0>
CICREFP
CICREFN
MSYNZ
AURORESZ<2..1>
R5 6K9
R6 6K9

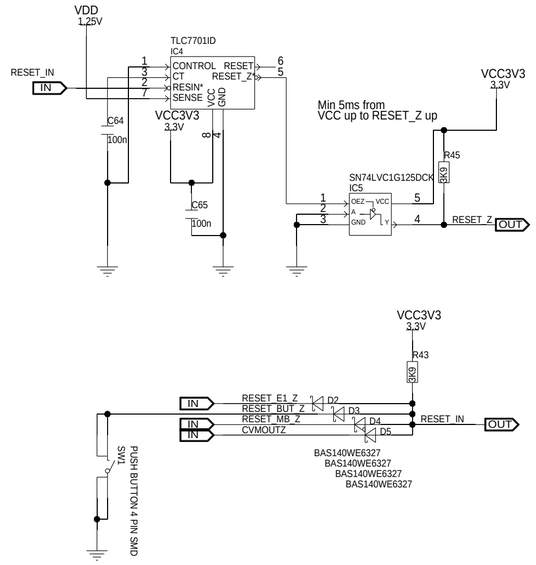
Debug & Program I/F



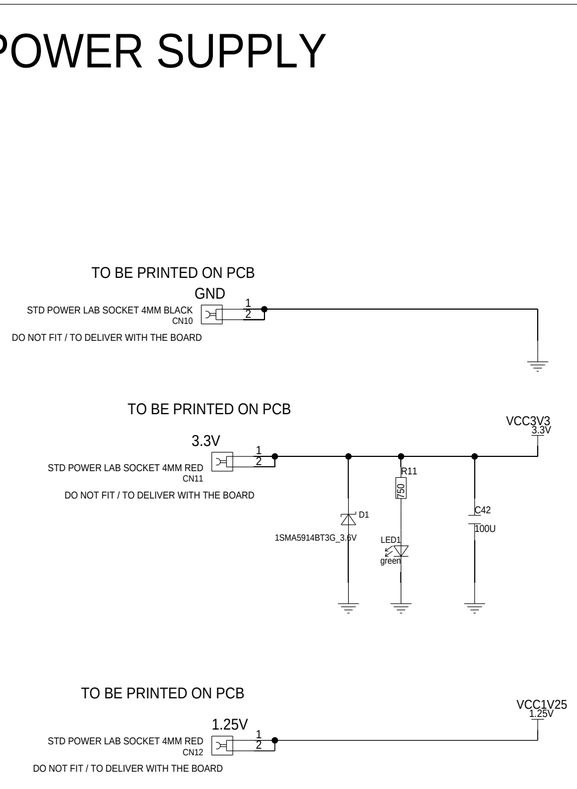
VOLTAGE DISTRIBUTION



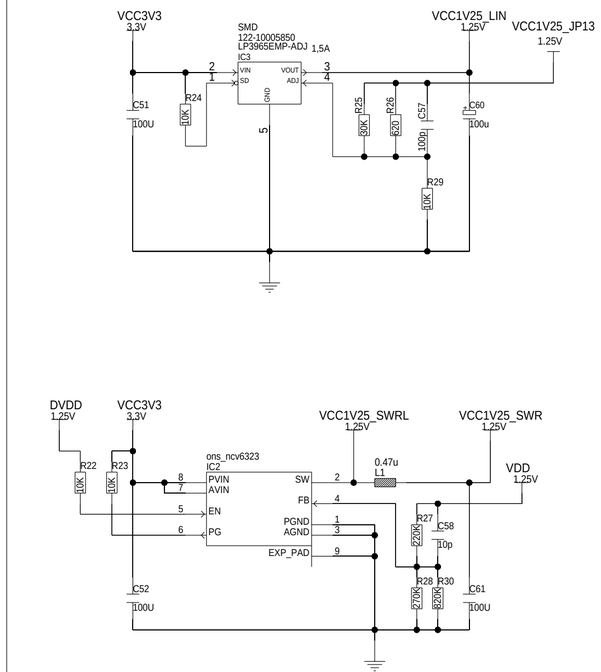
PUSH BUTTON FOR RESET



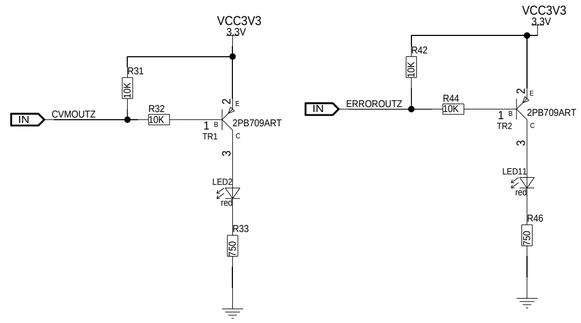
POWER SUPPLY



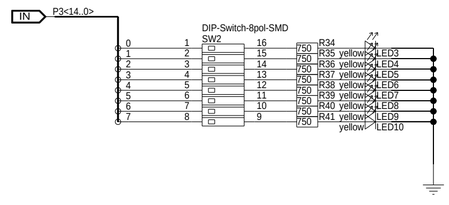
VOLTAGE REGULATOR



LED - CVMOUTZ&ERROROUTZ



LED - P3<7..0>



RENESAS Electronics Europe GmbH

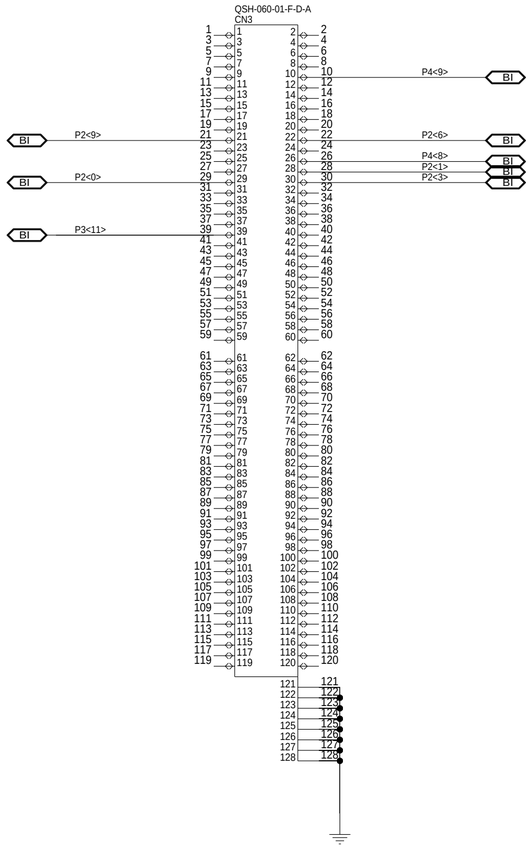
Title: RH850-V1RM-292PIN-PB-T1-V1

Size: A2 | Document Number: EESS-0400-111-01

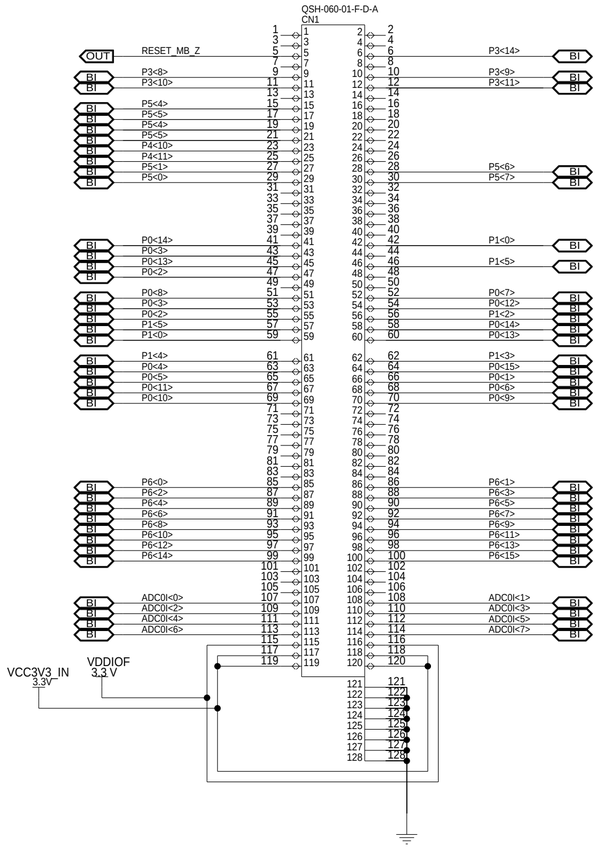
Date: Thu Jan 07 14:06:50 2016 | PAGE 2 OF 3 | 1.00inwork

CONNECT TO MAIN BOARD

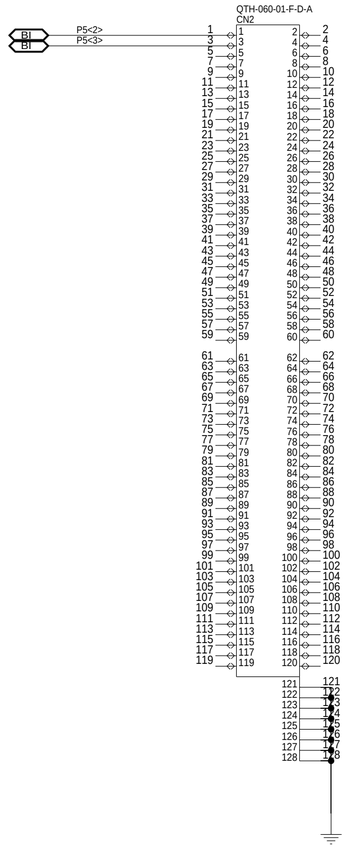
CONNECTOR3



CONNECTOR1



CONNECTOR2



FUDUCIALS

TOP

- TP11 FIDUCIAL_1MM
- TP12 FIDUCIAL_1MM

BOTTOM

- TP14 FIDUCIAL_1MM
- TP15 FIDUCIAL_1MM

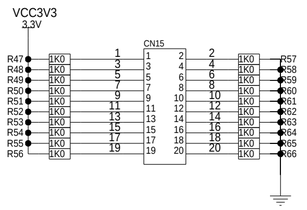
GND TEST POINT

- TP5 GND-TESTPOINT
- TP6 GND-TESTPOINT
- TP7 GND-TESTPOINT
- TP8 GND-TESTPOINT
- TP9 GND-TESTPOINT
- TP10 GND-TESTPOINT

RUBBER FEET

- BLACK MP1
- BLACK MP2
- BLACK MP3
- BLACK MP4
- BLACK MP5
- BLACK MP6

PULL UP PULL DOWN Connector



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