VersaClock7 PCB Layout Guidelines

PCB layout is a physical realization of the circuit designs. Good board layout practices will improve the electrical performance by controlling crosstalk and ensuring signal integrity. In addition, layout plays a fundamental role in meeting EMC emissions and immunity requirements.

This document provides information and recommendations to aid in the design and layout of PCB circuitry using VersaClock7 (VC7) devices. It contains information for generic PCB layout and some particular considerations for VC7 devices.

Contents

1. Layer Stack-Up

A PCB consists of multiple layers of copper (foil) and isolation materials laminated together. PCB layer stack-up design refers to the layer arrangement of copper and dielectric material layers with the total number of layers and the thickness of each layer taking into considerations.

Planning optimal multilayer stack-up is one of the most critical factors in determining electromagnetic compatibility performance of a PCB. A well-designed layer stack-up can both minimize the radiation and stay robust from external noise sources.

The following two diagrams illustrate the significance and relationships of signal impedance and EMC control with the PCB layer stack-up.

A signal trace that is suspended over a ground plane with a dielectric layer between them is call a microstrip. Its impedance is determined by a number of factors in the PCB and its stack-up arrangement:

- Signal trace width
- Thickness of the trace (thickness of copper layer)
- Distance between the two traces if it is a differential pair
- Thickness of the dielectric layer between a microstrip and the ground plane under the dielectric layer
- Dielectric constant Er

The following figure shows the calculation of a differential pair's impedance on the top layer of a PCB stack-up [1].

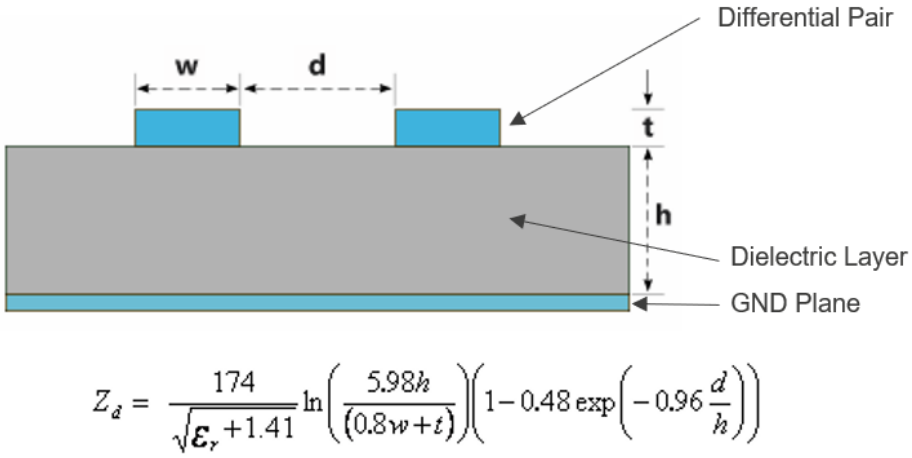

Figure 1. Signal Impedance with Respect of PCB Stack-Up

When a signal trace changes layers, the above factors affecting trace impedance change as well. Caution must be exercised in order to keep the signal impedance continuous to avoid signal integrity impairments.

Another signal type is called a stripline signal, which is one sandwiched between two dielectric material layers. A stripline signal trace impedance is similarly related to these factors but with a different calculation formula (not provided).

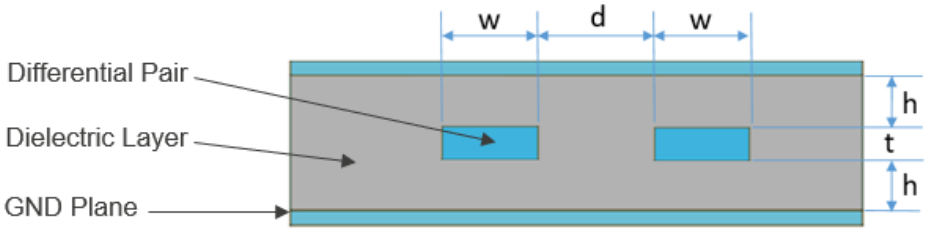

Figure 2. Stripline Signals Embedded in Dielectric Layer between Two GND Layers

It is worth noting that stripline signals are in between two GND plane layers. This minimizes crosstalk between the stripline signals and signals outside this layer. This is why an optimal stack-up design will enhance EMC performance of a PCB design.

Layer stack-up is a universal requirement for any PCB design, not just for VC7 devices. The following stack-up example is a board stack-up used for our VC7 Evaluation Board. The following comments are specific to this board layer stack-up:

- A 10-layer board is planned
- 6 layers are dedicated to copper planes – 4 ground planes and 2 power planes. This generous number of ground and power planes will help the board's EMC performance.
  Note: Depending on signal density, not every PCB board can dedicate such an abundant number of copper planes.
- Every signal layer must have an adjacent copper plane layer (ground or power plane) as return current paths for the signals on that layer.
- Megtron-6 material of different thickness are chosen as the dielectric layers between copper layers. Megtron-6 material demonstrates a very low loss at signal frequency < 2GHz. Given the clock frequencies in VC7 devices, FR4 material should be adequate.
- Total board thinness is 62mil, which is the most common board thickness.

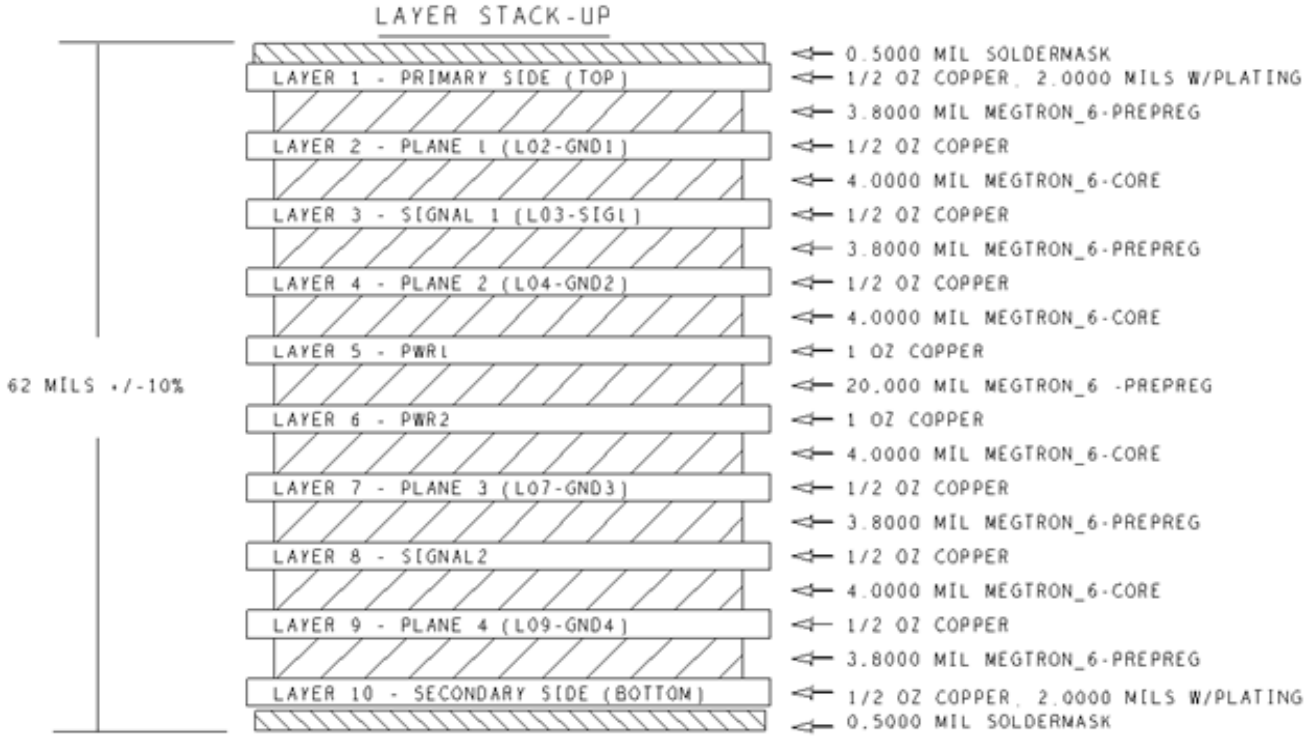

Figure 3. VC7 EVB Layer Stack-Up [2]

- From the above stack-up, Layer 3 (signal layer) is sandwiched between Layer 2 (GND plane) and Layer 4 (GND plane). Thus, Layer 3 is the preferred layer to route critical signals as noise and cross-talks are minimalized. This is also true for Layer 8.
- Copper layer thickness is defined by weight of copper (e.g., ½ oz of copper, or 1oz of copper). The thickness of copper layer of 1oz is the thickness of copper when 1oz of copper is spread evenly across a square foot, which is 0.35mm or 350mil (see the following figure).

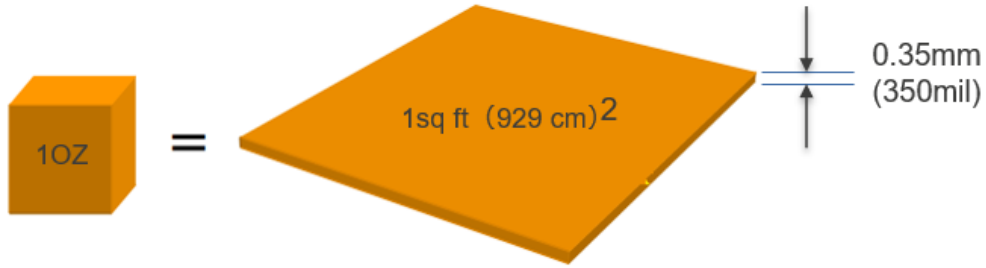

Figure 4. Copper Weight (Foil Thickness)

2. Placement

The optimal placement of the VC7 device and its neighboring components is specific to each design. The following general recommendations are provided for the designer to consider:

- Place the VC7 device/crystal away from switching power supply circuit.
- Place and orient the VC7 device for convenient routing of input and output clock traces.
- For crystal placement and routing recommendations, see “Crystal Placement and Handling”.
- For decoupling capacitor placement and routing recommendations, see “Power Supply Trace and Power Filtering Layout”.

3. Crystal Placement and Handling

Xin/Xout are the crystal oscillator circuit interface pins. Consider the following recommendations when using a crystal:

- Place the crystal as close to the IC pins as possible to minimize Xin/Xout trace length. The purpose of doing so is to minimize parasitic capacitance and interference. For the same reason, avoid using vias in Xin/Xout traces.
- When using capacitors on each crystal pin to set the load capacitance value, connect the ground side of the two capacitors close together and close to the IC ground connection. The reason is to minimize noise coupling from the ground plane. The VC7 devices have internal capacitors. It is preferred to use internal capacitance to avoid using external capacitors. When doing so, configure the internal capacitance based on crystal’s load capacitance (CL) in the spec. Avoid overloading or underloading the crystal.
- Treat the crystal component area as a “keep out area” for signal routing on other layers.
- Rout Xin and Xout traces as non-coupled high impedance traces. Separate them by at least 3x the trace width.
- Xin can be overdriven by a single-ended LVCMOS signal, or an AC-coupled signal lead from a differential pair, provided that the signal amplitude remain between 500mV and 1.2V and a slew rate of at least 0.2V/ns. In this case, the VC7’s internal capacitance should be configured to a minimum value. In the following schematics, place the signal termination resistor close to Xin pin.

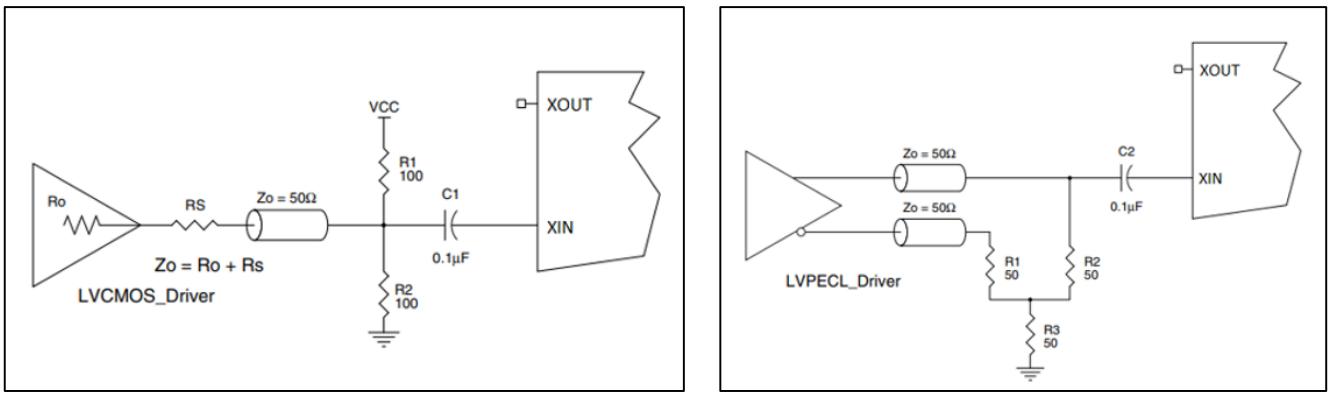

Figure 5. XIN Overdrive with an LVCMOS or an LVPECL Clock Source

4. VC7 Device Electrical and Thermal Pad Handling

VC7 devices come with an ePad – a ground island directly beneath the device on the same layer the IC is soldered on the PCB. The ePad is both a grounding pad and a thermal relief pad for the device. ePad patterns are different in different part numbers. Separate discussions on ePad handing are included in the following sections.

4.1 RC21008A/RC31008A – 40-LGA [3]

- Device land pattern is shown below:
  - PCB pad width: 0.20mm
  - PCB pad length: 0.45mm
    - Toe extension (beyond package edge): 0.05mm
    - Heel extension (toward package center): 0mm
- Stencil recommendations (Unit: mm):
  - Thickness: 0.125
  - Aperture for thermal pads: 0.84 × 0.84 (x9, each aperture centered on corresponding land pattern of each pad)
  - Aperture for pins: 0.22 × 0.58 (x40, heel coincides with package pin heel)
- Via placement and connections:
  - Place a thermal/ground via on each thermal pad.
  - This implementation is called via-in-pad, which is the option for this package because there is no extra space for the vias outside of pads.

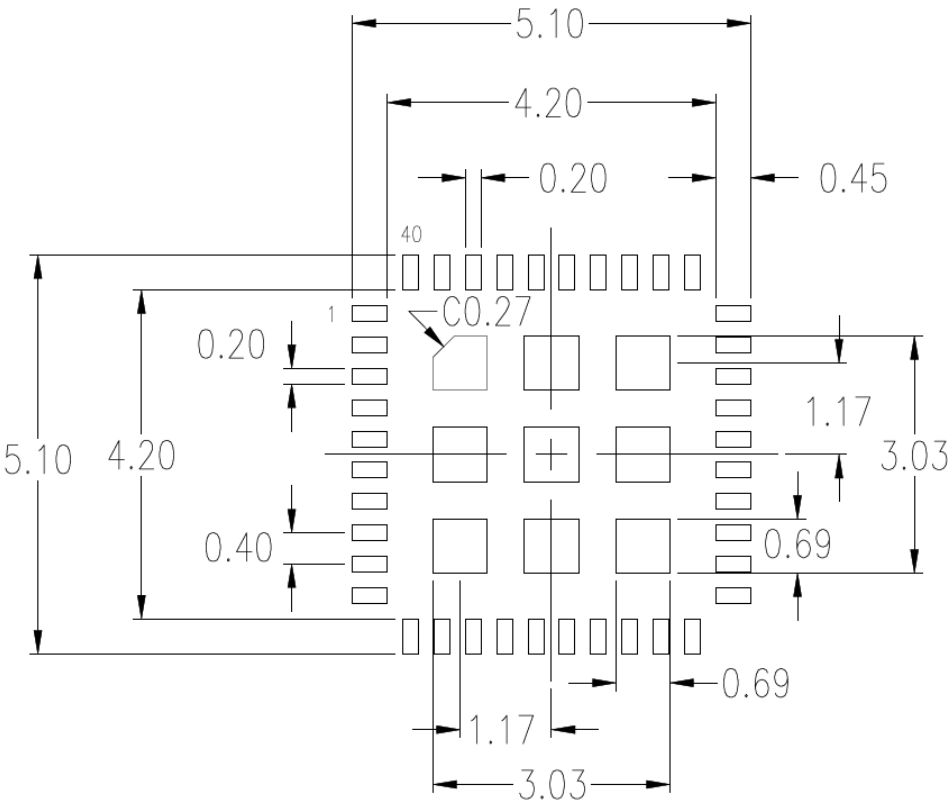

Figure 6. 40-LGA Land Pattern Dimensions

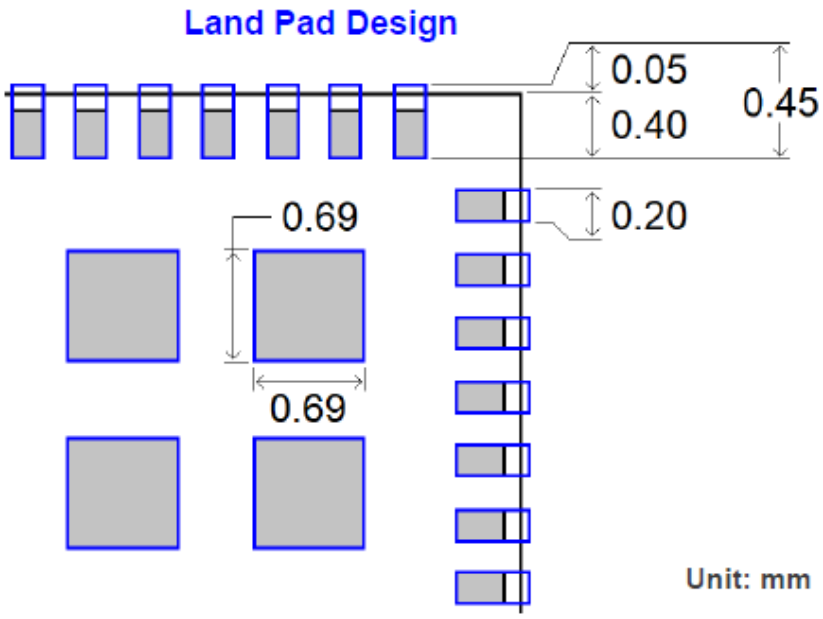

Figure 7. Layout Land Pattern Recommendations for RC21008AQ

4.2 RC21012A/RC21012A – QFN-48 [4]

- Device land pattern is shown below
  - PCB pad width: 0.20mm
  - PCB pad length: 0.55mm
    - Toe extension (beyond package edge): 0.05mm
    - Heel extension (toward package center): 0mm
- Stencil recommendations (Unit: mm)
  - Thickness: 0.125
  - Aperture for thermal pads: 2.3 × 2.3 (x4, 200um gap between apertures; centered on land pad).
    Note: We recommend 4x 2.3 × 2.3 mm solder paste pads instead of a big, single pad to avoid excessive copper.
  - Aperture for pins: 0.20 × 0.58 (x48, heel coincides with package pin heel)
- Via placement and connections:
  - Place as many thermal/ground vias as fit in each of the 4 split pads.
  - This implementation is called via-in-pad, which is the option for this package as there is no extra space for the vias outside of pads.

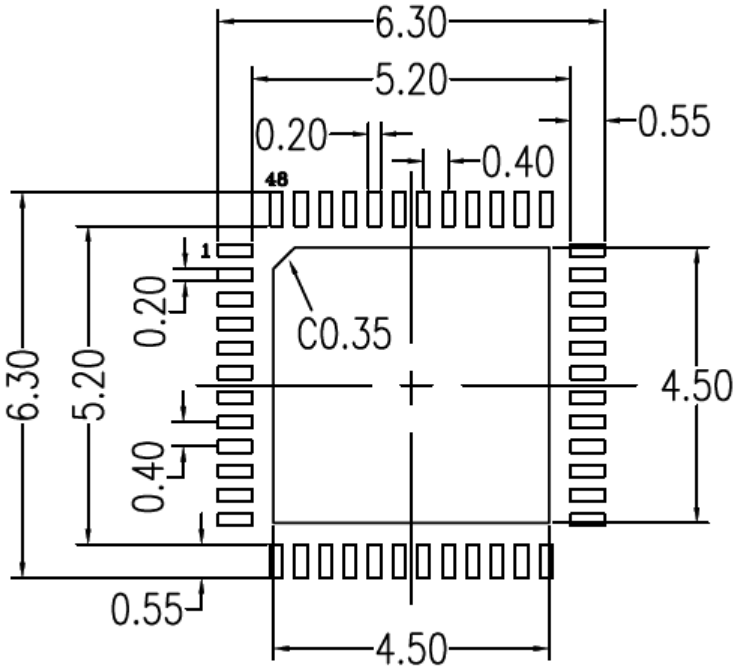

Figure 8. QFN-48 Land Pattern Dimensions

4.3 RC21005A/RC21005AQ – 32-LGA [5]

- Device land pattern is shown below.
- Stencil recommendations (Unit: mm)
  - Thickness: 0.125
  - Aperture for thermal pads: 0.60 × 0.55 (x4, each aperture vertex closes to the aggregate center of the pattern. Four apertures should be aligned with the corresponding vertex of the land pad)
  - Aperture for pins: 0.22 × 0.68 (x32, heel coincides with package pin heel)
- Via placement and connections:
  - Place thermal/ground via in space close to each thermal pad.
  - Connect each via with a thermal pattern with a trace for a low impedance connection. Via size and trace width are per each design's DCR.

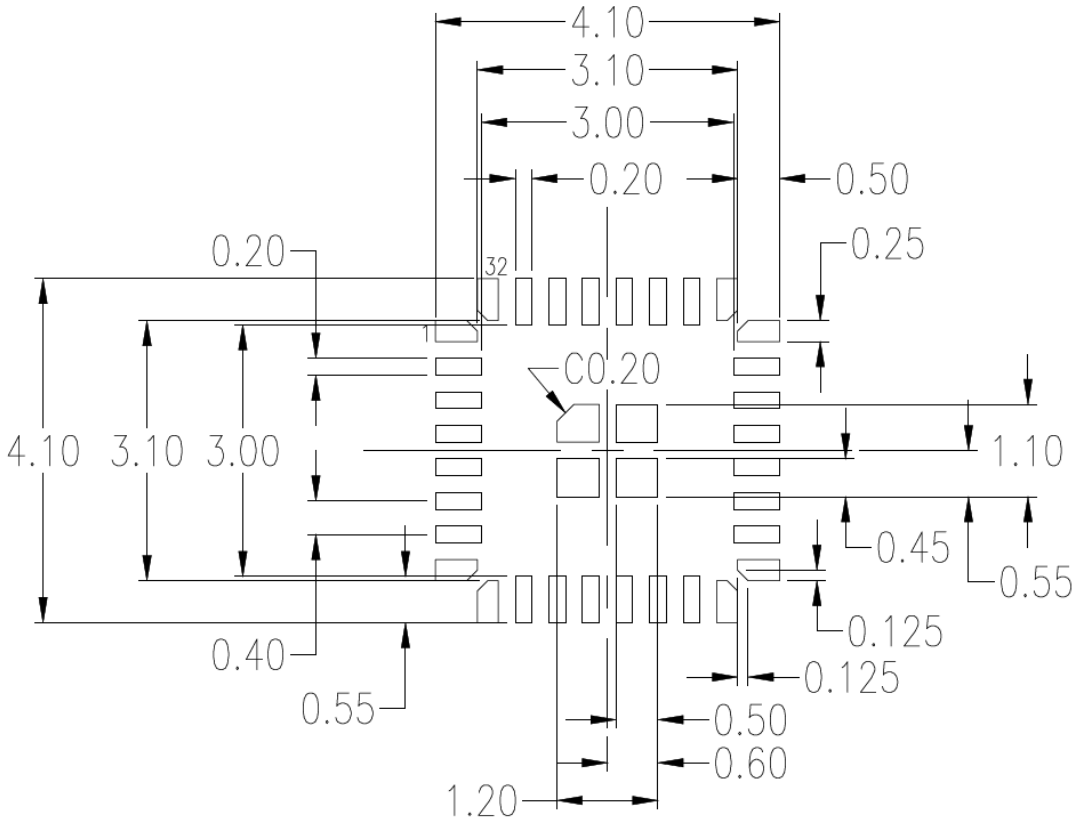

Figure 9. 32-LGA Land Pattern Dimensions

5. Trace Routing

Routing a PCB board with VC7 devices should follow the generic engineering practice of PCB routing rules. Routing recommendations are summarized in the following sections.

5.1 Single-Ended Routing

- Keep clock traces as straight as possible. Use arc-shaped (or 45 degree) traces instead of right-angle or even sharp-angle bending.

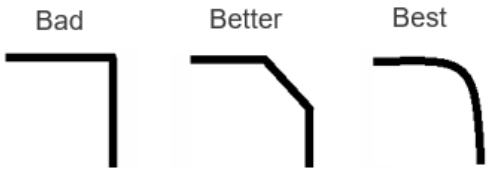

Figure 10. Trace Bending

- Do not use multiple signal layers for clock signals (i.e., to avoid changing layers).
- Do not use vias in clock transmission lines (i.e., to avoid changing layers). Vias can cause impedance mismatch impairing signal integrity.
- Always route clock signals (and any signal in that matter) on a layer that has an immediately adjacent ground layer as a return current path.
- As a classic routing pitfall, avoid routing a signal across a cut-out/slit on the reference plane. If unavoidable, use a stitching capacitor (i.e., 0.1uF) to provide a return current path as follows.

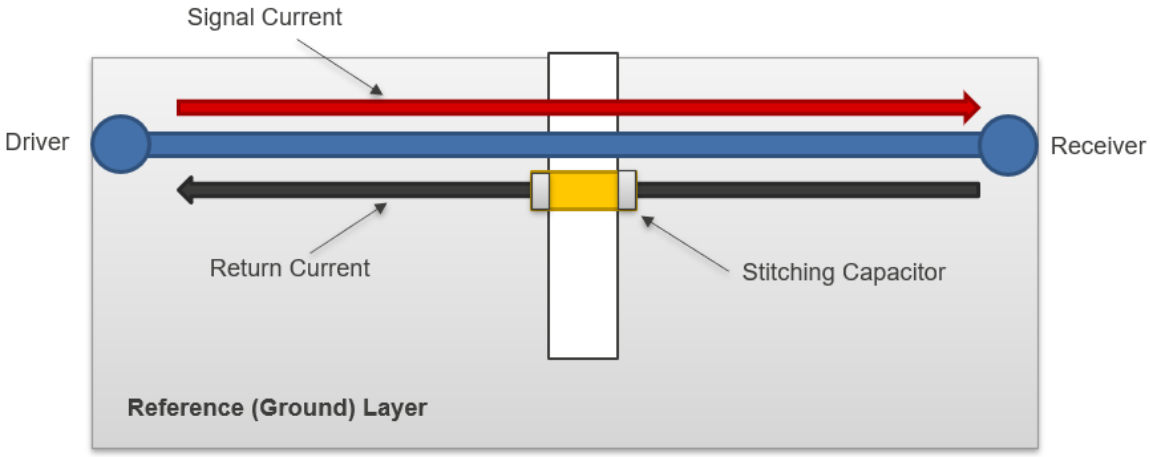

Figure 11. Using a Stitching Capacitor Where Passing a Ground Plane Slit

5.2 Differential (Clock) Pair Routing

Differential traces should always be routed together (side-by-side). This keeps any noise injection into the signal pair a true common-mode noise which gets rejected by the receiver. In a real PCB routing, consider the following points as additional recommendations.

- Keep both leads of a differential pair the same length so that signals arrive at the receiver at the same time. Use “phase matching bumps” to the lead that is shorter than the other lead to make both signal leads the same length. Remember to compensate at the end where length deficit takes place as shown below.

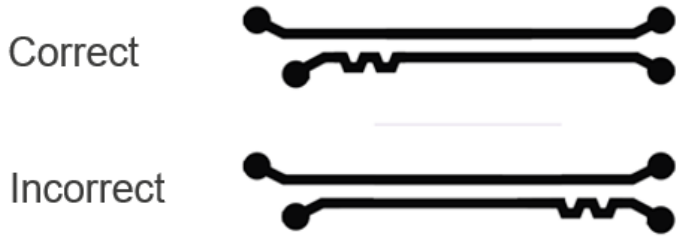

Figure 12. Adding Phase Compensation Bumps in a Differential Pair

- If ac-coupling capacitors are used, place the coupling capacitors in a way that the differential pair can be routed symmetrically as shown below.

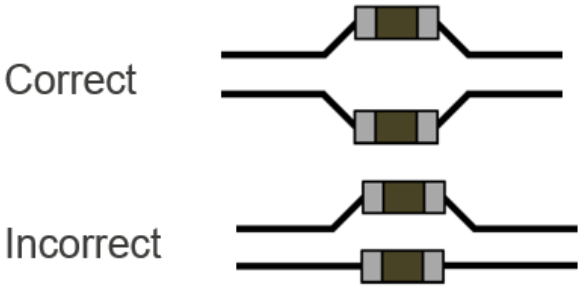

Figure 13. Symmetrical Placement of Series Components in a Differential Pair

- To avoid a non-related component on the board, avoid encompassing the component within the differential pair. Rather route the differential pair away from the component together as in the following diagram.

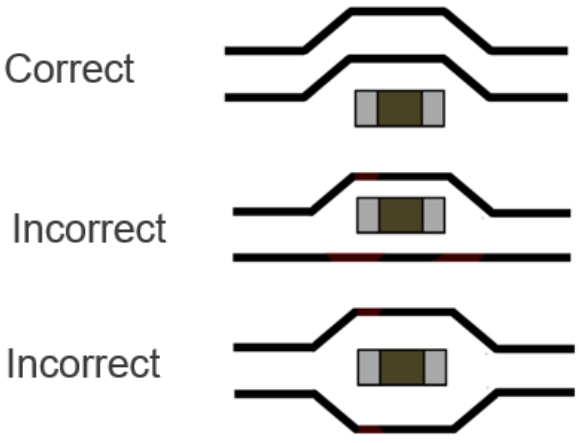

Figure 14. Avoid Encompassing an Unrelated Component in a Differential Pair

- Changing layers when routing differential pairs is not uncommon. When that happens, place a pair of ground vias close to the signal vias, respectively, to provide a return current path.

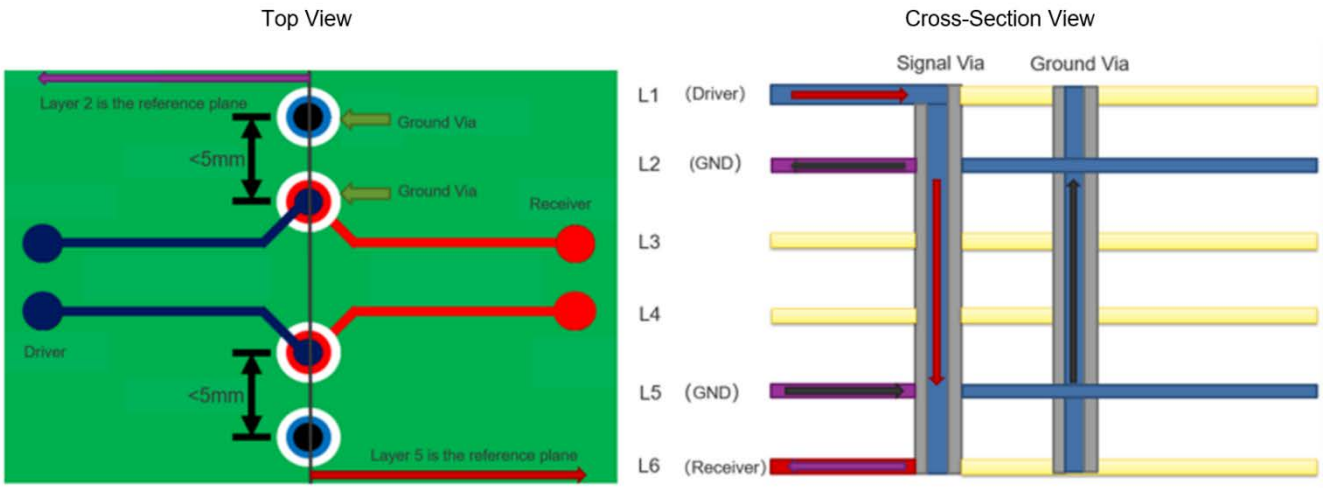

Figure 15. Ground Vias Added Close to Signal Vias when Signal Changes Layers

- Route differential pairs vertically in two adjacent layers. Avoid routing a power trace close to, and in parallel of, signal traces.
- When via stub becomes a signal integrity concern, use back drill (in PCB manufacturing stage). In the following figure, a differential pair changes layers from L1 to L2 leaving a via stub equivalent to the thickness from L2 to L6 (assuming a 6-layer board). Back drill is to drill off the copper barrel (wall of the via) from L2 to L6, which is illustrated in the figure. There is a cost adder to back-drilling. Balance the performance requirement versus the cost added.

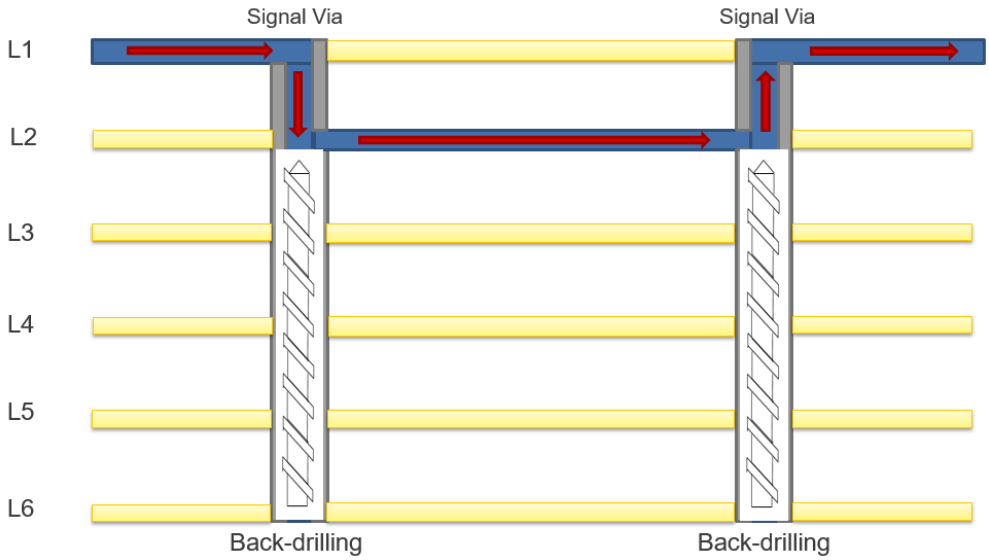

Figure 16. Back Drill

- When a differential pair changes layers, make sure the impedance is maintained in a different layer. Due to the different dielectric layer thickness, this may mean a change of trace width of the differential pair in a different layer, which may not always be feasible. Because of that, it is preferred that routing a differential pair on the same layer if possible.

6. Power Supply Trace and Power Filtering Layout

Power filtering is one of the most important measures to prevent power supply noises from coupling to the device outputs, adversely affecting performance, especially when using switched power supplies. Usually we recommend power supply filtering with a parallel combination of bulk, decoupling, and bypass capacitors as displayed in the following figure.

Bulk capacitors are usually large size capacitors. They are used for limiting surge currents in the power supply. In a power supply design, multiple types of regulators (linear and switching) are often used to shift voltage levels and to reject power supply ripples. Power supply decoupling is achieved with a ferrite bead (and/or a small value series resistor) and decoupling capacitors forming a pi-shape low pass filter topology.

Bypass capacitors are often small size capacitors and are recommended to place them close to the device to shunt high-frequency noises to ground. They are used together with bulk decoupling capacitors to provide a clean power to the device.

A pi-shape power filtering topology used in the VC7 Evaluation Board (see Figure 1 in the *VersaClock7 Power Supply Filtering Recommendations*) can achieve a noise attenuation across the frequency spectrum as shown below. For more information about power supply filtering recommendations, see the application note titled *VersaClock7 Power Supply Filtering Recommendations*.

The following list contains layout recommendations for power supply traces and power supply filtering:

- Do not overlay power traces from the two power players.
- Do not run power traces parallel/adjacent for long stretches, even if they are of different layers.
- Cross power traces from different layers at 90 degrees if the crossing is necessary.
- Keep power traces as thick as possible (while keeping a generous spacing to adjacent power traces) for lower resistance and inductance.
- Space power traces further apart where possible.
- VDDA is most sensitive to noise. VDDD is digital domain supply, thus the noisiest. Use separate power filtering for VDDA and VDDD, and space them apart in layout.
- VDDO traces supply different output drivers. Use separate power filtering rail for each VDDO trace. VDDO traces supplying the same output frequencies can share a single power filtering.
- Place a bypass capacitor (0.1uF) as close as possible to a power pin. Place the decoupling capacitor on the same layer as QFN/LGA device.
- Place bypass capacitors on the same layer as the device.
- Use a ground via for each bypass capacitor. Do not share a ground via for more than one bypass capacitor.
- Use low-inductive pad designs [7] as shown below.

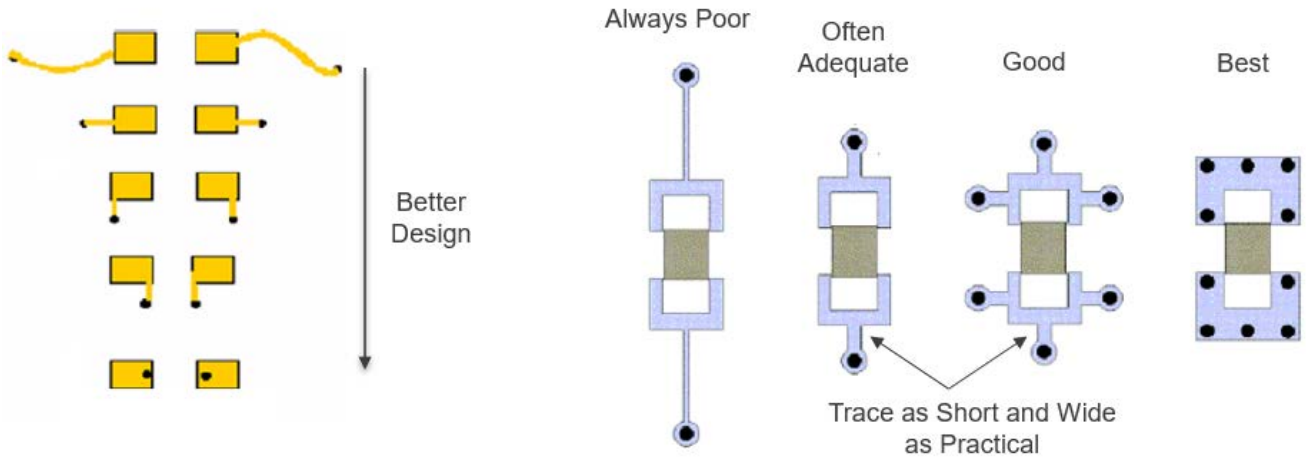

Figure 17. Decoupling Capacitor Pad Design

7. References

1. IPC-D-317A
2. RC21008A/RC31008A-EVK Layout
3. REN_PSC-4864-01_20201208
4. REN_PSC-4212-05_20190510
5. REN_PSC-4889-02_20220114
6. AN-909 PCB Layout Considerations for Designing IDT VersaClock 3S, 5 and 6 Clock Products
7. AN-376 LIU PCB Layout Guide

8. Revision History

Revision	Date	Description
1.00	Aug 4, 2022	Initial release.

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