NEC

# User's Manual

# V850ES/DJ2

## 32-bit System in Package Microcontroller

## Hardware

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## µPD70F3325

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## NOTES FOR CMOS DEVICES

**① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN).

**② HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

**③ PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

**④ STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

**⑤ POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

**⑥ INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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# Preface

**Readers**

This manual is intented for users who want to understand the functions of the V850ES/DJ2.

**Purpose**

This manual presents the hardware manual of the V850ES/DJ2.
This User's Manual is an extension of the F_Series User's Manual.

F_Series Items:

For all of the items regarding the FG2 please refer to the F_Series User's Manual/Data sheet (U17215EJ2V0UD00 (2nd edition) and further releases).

MTRC of D_Series:

In this User's Manual/Data Sheet all of the MTRC relevant items and the internal connection or pinout of the D_Series device are regarded.

**Organization**

This system specification describes the following sections:

- Pin function
- Port function
- Internal peripheral function
- Electrical target specification

**Legend**

Symbols and notation are used as follows:

| | | |
|---|---|---|
| Weight in data notation | : | Left is high-order column, right is low order column |
| Active low notation | : | $\overline{xxx}$ (pin or signal name is over-scored) or /xxx (slash before signal name) |
| Memory map address: | : | High order at high stage and low order at low stage |
| **Note** | : | Explanation of (Note) in the text |
| **Caution** | : | Item deserving extra attention |
| **Remark** | : | Supplementary explanation to the text |
| Numeric notation | : | Binary . . . xxxx or xxxB<br>Decimal . . . xxxx<br>Hexadecimal . . . xxxxH or 0x xxxx |

Prefixes representing powers of 2 (address space, memory capacity)

K (kilo): $2^{10} = 1024$

M (mega): $2^{20} = 1024^2 = 1,048,576$

G (giga): $2^{30} = 1024^3 = 1,073,741,824$

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# Chapter 1 Introduction

The V850ES/DJ2 is a product of the NEC's V850 D_Series Series of single-chip microcontroller designed for application with up to 6 stepper motor channels.
It provides low-power operation for real-time control applications especial for automotive Dashboard applications.

## 1.1 General

The V850ES/DJ2 is a 32-bit System in Package (SiP) microcontroller that includes a V850ES CPU core device of the F_Series (V850ES/FG2) and a Meter Controller/Driver (MTRC) in one package.

The F_Series includes peripheral functions such as ROM/RAM, a timer/counter, serial interfaces, and an A/D converter.
In addition to high real-time response characteristics and 1-clock-pitch basic instructions, the V850ES/FG2 features multiply instructions, saturated operation instructions, bit manipulation instructions, etc., realised by a hardware multiplier, as optimum instructions for digital servo control applications. Moreover, as a real-time control system, the V850ES/FG2 enables extremely high cost-performance for applications that require a low power consumption, such as automotive applications.
For an overview of the V850ES/FG2 refer to "V850ES/FG2 Introduction" on page 25.

The integrated MTRC supplies a meter controller driver macro for up to 6 stepper motor channels and GPIOs. Via the dedicated interface the controlling will be handled with a dedicated protocol.
For this internal interface the 3-wire serial interface CSIB1 of the V850ES/DG2 device is used for the serial communication and the PCM0 port of the V850ES/FG2 device is used as the CS function for the MTRC.

## 1.2 Features (V850ES/D_Series)

***Table 1-1: Features (V850ES/D_Series)***

| Part Number | Name | V850ES/FG2 device | Pin | Internal Memory | | CAN | SM |
|---|---|---|---|---|---|---|---|
| | | | | Flash (KB) | RAM (KB) | | |
| µPD70F3325 | V850ES/DJ2 | µPD70F3235(A)/FG2 | 144 | 256 | 12 | 2 | 6 |

**Note:** In the following the product term V850ES/Fx2 is used for V850ES/FG2, unless otherwise noted.

## 1.3 About the Subject of this User's Manual

This User's Manual is an extension of the F_Series User's Manual.

F_Series Items:
For all of the items regarding the V850ES/DG2 please refer to the F_Series User's Manual/Data Sheet (U17215EJ2V0UD00 (2nd edition) and further releases).

MTRC of D_Series:
In this User's Manual/Data Sheet all of the MTRC relevant items and the internal connection or pinout of the D_Series device are regarded.

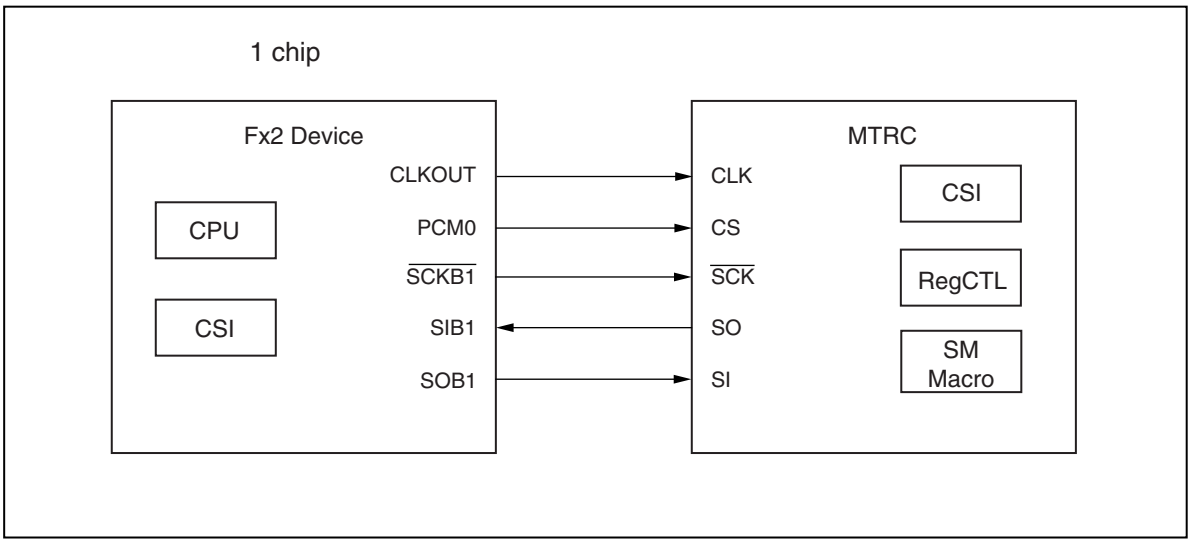
## 1.4 Internal Connection

The following pins of the V850ES/Fx2 device are connected to the MTRC:

- CSI I/F: SIB1, SOB1, $\overline{\text{SCKB1}}$
- Chip select: PCM0 as CS

### 1.4.1 System in Package (SiP)

***Figure 1-1: D_Series SiP***



## 1.5 Communication Between the V850ES/Fx2 and MTRC

The clocked synchronous serial interface CSIB1 of the V850ES/Fx2 device is used for the communication with the MTRC.

The communication I/F of the MTRC is fixed to the following settings:

- I/F: CSI
- Mode: Slave mode
- Data length: 8-bits
  (support continuous data transfer,
  therefore the V850ES/Fx2 CSIB1 can use 16-bit data length)
- Transfer: MSB first
- Transmission: transmission/reception mode

### 1.5.1 Communication

The software for the communication between the V850ES/Fx2 device and the MTRC has to manage the I/F of the CSIB1 and the PCM0 pin as chip select signal.

The CSI1B of the V850ES/Fx2 device has been set to master mode, because the MTRC CSI is always in slave mode. Therefore it is necessary, that the CSIB1 sends dummy data if the V850ES/Fx2 device wants to read data from the MTRC.

The MTRC CSI is always in 8-bit mode but is capable of continuous data transfer. Therefore the 16-bit mode of the CSIB1 can be used for faster communication for example.

### 1.5.2 Internal and external communication via CSIB1

In case the PMT4 pins are operated in alternate function mode (PMCMT4n = 1), the function of the PMT40 to PMT42 (EXCSIB1 pins) ports is further controlled by the PCM0/CS signal:

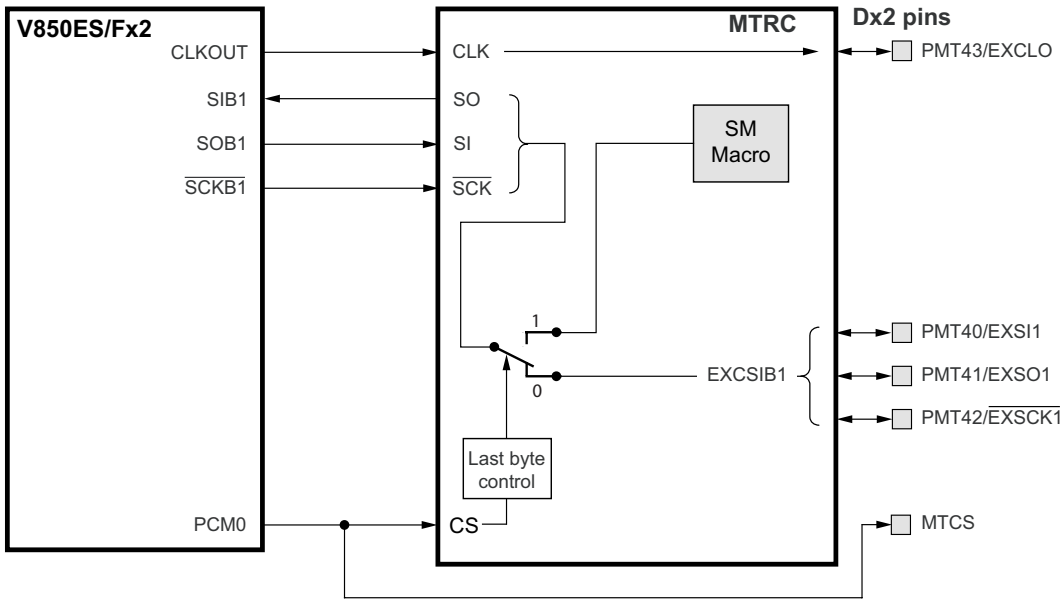
- PMCMT4n = 1, PCM0/CS = 0:
  PMT40 to PMT42 (EXCSIB1) provide the function of the V850ES/Fx2's CSIB1 interface pins. Thus if no communication between the V850ES/Fx2 and the MTRC is ongoing, the V850ES/Fx2 can connect to an external device via the CSIB1 interface.
  A special "Last byte control" circuit ensures, that an ongoing CSIB data transfer between the V850ES/Fx2 and an external device is not interrupted by setting PCM0/CS = 1. CSIB1 and EXCSIB1 is disconnected only after data transfer is completed.

- PMCMT4n = 1, PCM0/CS = 0:
  PMT40 to PMT42 have no function.

The MTCS pin reflects the status of PCM0/CS, and therefore the mode of the EXCSIB1 pins.

If PMT40 to PMT42 are in port mode (PMCMT4n = 0), they are controlled by the PMT4 control registers.

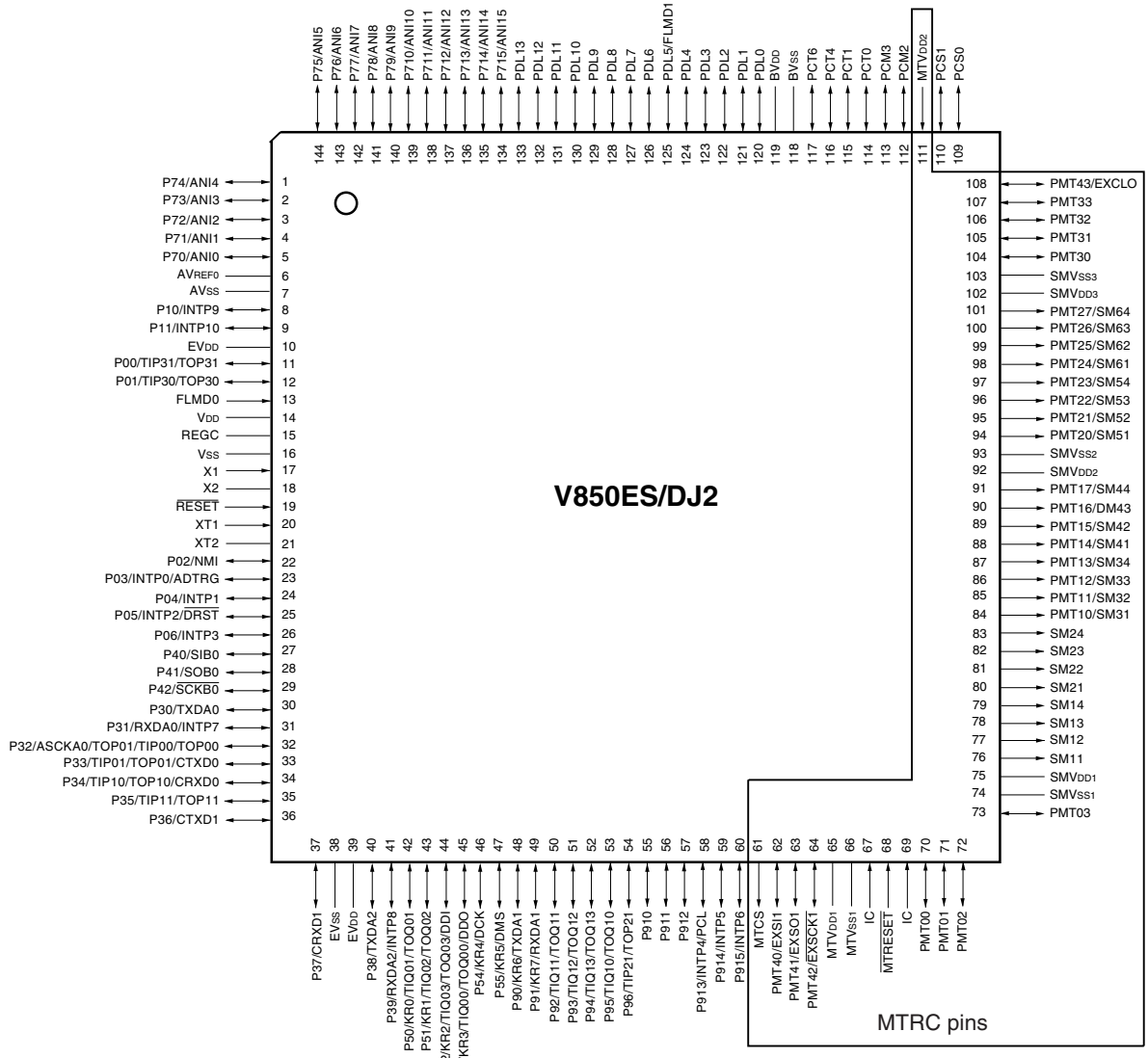
***Figure 1-2: CS Functionality***




| PCM0/CS MTCS | EXCSIB1 signals |
|---|---|
| 1 | EXCSIB1 signals have no function |
| 0 | EXCSIB1 signals have the function of the V850ES/Fx2's CSIB1 interface pins |

## 1.6 Pinout of DJ2

***Figure 1-3: Pinout of DJ2***

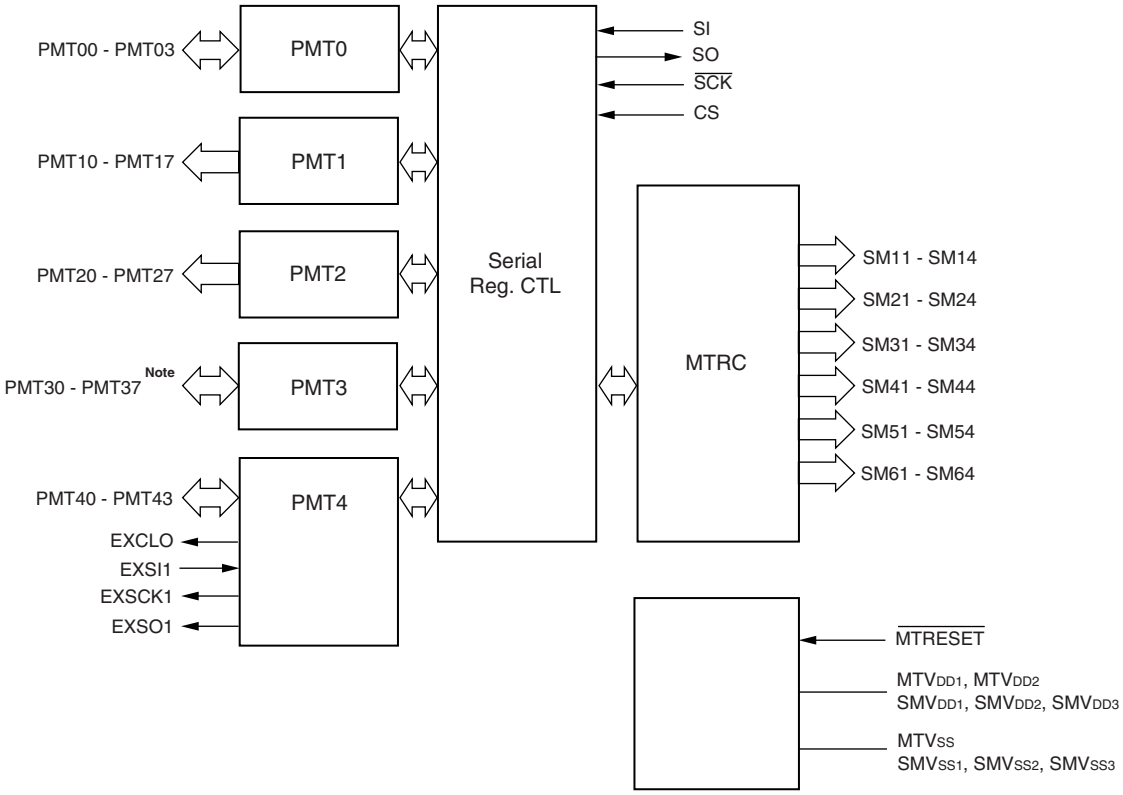


## 1.7 Overview of MTRC Functions

***Table 1-2: Overview of MTRC Functions***

| | | |
|---|---|---|
| Operating Frequency | | Max. 16 MHz (typ. 8 MHz) |
| Meter Driver | | 360° × 6 channels |
| Ports | I/O | 16 |
| | O | 16 |
| Connection between V850ES/Fx2 device and MTRC | | 3-Wire Serial Interface (CSI) slave mode, 8-bit, single/continuous mode |
| Power Supply voltage range | | 4.0 V to 5.5 V |

***Figure 1-4: Block Diagram of the MTRC***




**Note:** I/O ports of PMT3 are used in the V850ES/DJ2 as follows:

- V850ES/DJ2, 144-pin: PMT30-PMT33

## 1.8 Peripheral I/O Registers

***Table 1-3: Peripheral I/O Registers***

| Address | Register Name | Symbol | Initial Value After Reset | Access | | | R/W |
|---|---|---|---|---|---|---|---|
| | | | | 1-bit | 8-bit | 16-bit | |
| 00H | Compare Register 10 | MCMP10 | 00H | | × | | R/W |
| 01H | Compare Register 11 | MCMP11 | 00H | | × | | R/W |
| 02H | Compare Control Register 1 | MCMPC1 | 00H | | × | | R/W |
| 03H | Compare Register 20 | MCMP20 | 00H | | × | | R/W |
| 04H | Compare Register 21 | MCMP21 | 00H | | × | | R/W |
| 05H | Compare Control Register 2 | MCMPC2 | 00H | | × | | R/W |
| 06H | Compare Register 30 | MCMP30 | 00H | | × | | R/W |
| 07H | Compare Register 31 | MCMP31 | 00H | | × | | R/W |
| 08H | Compare Control Register 3 | MCMPC3 | 00H | | × | | R/W |
| 09H | Compare Register 40 | MCMP40 | 00H | | × | | R/W |
| 0AH | Compare Register 41 | MCMP41 | 00H | | × | | R/W |
| 0BH | Compare Control Register 4 | MCMPC4 | 00H | | × | | R/W |
| 0CH | Compare Register 50 | MCMP50 | 00H | | × | | R/W |
| 0DH | Compare Register 51 | MCMP51 | 00H | | × | | R/W |
| 0EH | Compare Control Register 5 | MCMPC5 | 00H | | × | | R/W |
| 0FH | Compare Register 60 | MCMP60 | 00H | | × | | R/W |
| 10H | Compare Register 61 | MCMP61 | 00H | | × | | R/W |
| 11H | Compare Control Register 6 | MCMPC6 | 00H | | × | | R/W |
| 12H | Timer Mode Control Register 0 | MCNTC0 | 00H | | × | | R/W |
| 13H | Timer Mode Control Register 1 | MCNTC1 | 00H | | × | | R/W |
| 20H | Port MT0 | PMT0 | Undefined | | × | | R/W |
| 21H | Port MT1 | PMT1 | Undefined | | × | | R/W |
| 22H | Port MT2 | PMT2 | Undefined | | × | | R/W |
| 23H | Port MT3 | PMT3 | Undefined | | × | | R/W |
| 24H | Port MT4 | PMT4 | Undefined | | × | | R/W |
| 25H | Port MT0 Mode Register | PMMT0 | FFH | | × | | R/W |
| 26H | Port MT1 Mode Register | PMMT1 | FFH | | × | | R/W |
| 27H | Port MT2 Mode Register | PMMT2 | FFH | | × | | R/W |
| 28H | Port MT3 Mode Register | PMMT3 | FFH | | × | | R/W |
| 29H | Port MT4 Mode Register | PMMT4 | FFH | | × | | R/W |
| 2AH | Port MT1 Mode Control Register | PMCMT1 | 00H | | × | | R/W |
| 2BH | Port MT2 Mode Control Register | PMCMT2 | 00H | | × | | R/W |
| 2CH | Port MT4 Mode Control Register | PMCMT4 | 00H | | × | | R/W |
| 2DH | SM1SM2 Mode Control Register | SM12MC | 00H | | × | | R/W |
| 2EH | Ring Oscillator Control Register | MRCTL | 50H | | × | | R/W |
| 31H | Calibration Register | MRCAL | 10H | | × | | R/W |

**[MEMO]**

# Chapter 2 V850ES/FG2 Introduction

The V850ES/FG2 is one of the products of NEC Electronics' V850 Series of single-chip microcontrollers for real-time control.

The V850ES/FG2 is a 32-bit single-chip microcontroller that includes the V850ES CPU core and integrate peripheral functions such as ROM/RAM, DMA controller, and timers/counters. These microcontrollers also incorporate a CAN (Controller Area Network) as an automotive LAN.

In addition to highly real-time responsive, 1-clock-pitch basic instructions, this microcontroller have instructions ideal for digital servo applications, such as multiplication instructions using a hardware multiplier, sum-of-products operation instructions, and bit manipulation instructions. This microcontroller can also realize a real-time control system that is highly cost effective and can be used in automotive instrumentation fields.

- Number of instructions: 83
- Minimum instruction execution time: 50 ns (main clock ($f_{XX}$) = 20 MHz)
- General-purpose registers: 32 bits × 32
- Power-on clear function
- Low-voltage detection function
- Ring-OSC: 200 kHz (TYP.)
- Interrupts/exceptions
  Non-maskable interrupts
  Maskable interrupts
- I/O lines: I/O ports: 84
- Timer/counters
  16-bit interval timer M (TMM): 1 ch
  16-bit timer/event counter P (TMP): 4 ch
  16-bit timer/event counter Q (TMQ): 2 ch
- Watch timer: 1 ch
- Watchdog timer 2: 1 ch
- Serial interface (SIO)
  Asynchronous serial interface A (UART)
  3-wire variable-length serial interface B (CSIB)
- CAN controller: 2 ch
- A/D converter: 10-bit resolution: 16 ch

- Clock generator

  Main clock/subclock operation
  CPU clock in seven steps ($f_{XX}$, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/32$, $f_{XT}$)
  Clock-through mode/PLL mode selectable

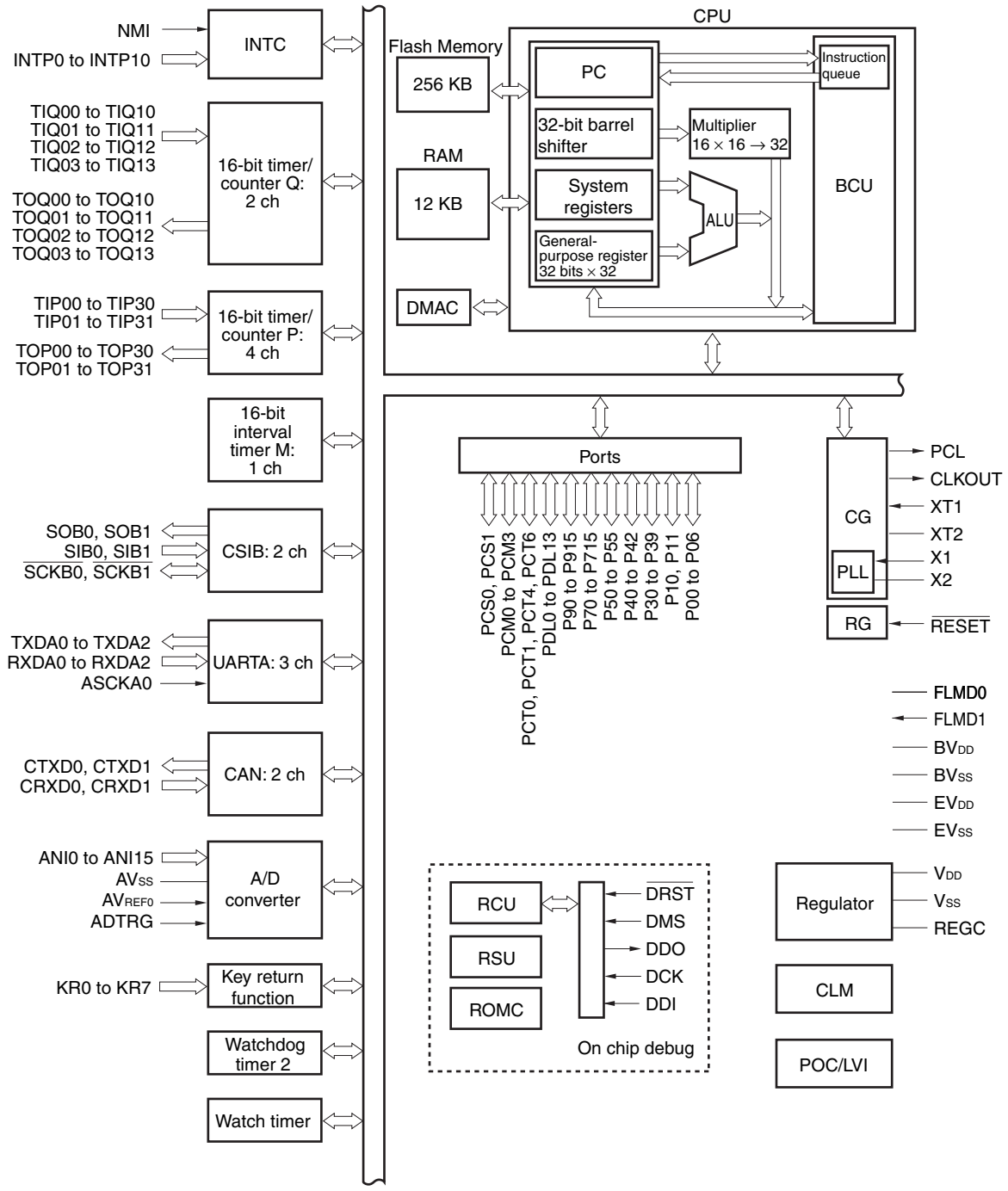
- Power save function

  -HALT
  -IDLE1
  -IDLE2
  -software STOP
  -subclock
  -sub-IDLE modes

**Pin identification**

| | | | |
|---|---|---|---|
| ADTRG: | A/D trigger input | PCM0 to PCM3: | Port CM |
| ANI0 to ANI15: | Analog input | PCS0, PCS1: | Port CS |
| ASCKA0: | Asynchronous serial clock | PCT0, PCT1, | |
| $AV_{REF0}$: | Analog reference voltage | PCT4, PCT6: | Port CT |
| $AV_{SS}$: | Analog $V_{SS}$ | PDL0 to PDL13: | Port DL |
| $BV_{DD}$: | Power supply for bus interface | REGC: | Regulator control |
| $BV_{SS}$: | Ground for bus interface | RESET: | Reset |
| CLKOUT: | Clock output | RXDA0 to RXDA2: | Receive data |
| CRXD0, CRXD1: | Receive data for controller area network | SCKB0, SCKB1: | Serial clock |
| CTXD0, CTXD1: | Transmit data for controller area network | SIB0, SIB1: | Serial input |
| DCK: | Debug clock | SOB0, SOB1: | Serial output |
| DDI: | Debug data input | TIP00, TIP01, | |
| DDO: | Debug data output | TIP10, TIP11, | |
| DMS: | Debug mode select | TIP20, TIP21, | |
| DRST: | Debug reset | TIP30, TIP31, | |
| $EV_{DD}$: | Power supply for port | TIQ00 to TIQ03, | |
| $EV_{SS}$: | Ground for port | TIQ10 to TIQ13: | Timer input |
| FLMD0, FLMD1: | Flash programming mode | TOP00, TOP01, | |
| INTP0 to INTP10: | Interrupt request from peripherals | TOP10, TOP11, | |
| KR0 to KR7: | Key return | TOP20, TOP21, | |
| NMI: | Non-maskable interrupt request | TOP30, TOP31, | |
| P00 to P06: | Port 0 | TOQ01 to TOQ03, | |
| P10, P11: | Port 1 | TOQ11 to TOQ13: | Timer output |
| P30 to P39: | Port 3 | TXDA0 to TXDA2: | Transmit data |
| P40 to P42: | Port 4 | $V_{DD}$: | Power supply |
| P50 to P55: | Port 5 | $V_{SS}$: | Ground |
| P70 to P715: | Port 7 | X1, X2: | Crystal for main clock |
| P90 to P915: | Port 9 | XT1, XT2: | Crystal for subclock |
| PCL: | Programmable clock output | | |

*Figure 2-1: V850ES/FG2 - µPD70F3235 Block Diagram*



## 2.1 Pin Functions

This section explains the names and functions of the pins of the V850ES/FG2.

Three I/O buffer power supplies, $AV_{REF0}$, $BV_{DD}$ and $EV_{DD}$, are available. The relationship between the power supplies and the pins is shown below.

***Table 2-1: Pin I/O Buffer Power Supplies (V850ES/FG2)***

| Power Supply | Corresponding Pin |
|---|---|
| $AV_{REF0}$ | Port 7 |
| $EV_{DD}$ | Port 0, Port 1, Port 3, Port 4, Port 5, Port 9, RESET |
| $BV_{DD}$ | Port CM, Port CS, Port CT, Port DL |

***Table 2-2: Pin List (Port Pins)***

| Pin Name | I/O | Function | Alternate Function |
|---|---|---|---|
| P00 | I/O | Port 0<br>7-bit I/O port<br>Input/output can be specified in 1-bit units. | TIP31/TOP31 |
| P01 | | | TIP30/TOP30 |
| P02 | | | NMI |
| P03 | | | INTP0/ADTRG |
| P04 | | | INTP1 |
| P05 | | | INTP2/DRST |
| P06 | | | INTP3 |
| P10 | I/O | Port 1<br>2-bit I/O port<br>Input/output can be specified in 1-bit units. | INTP9 |
| P11 | | | INTP10 |
| P30 | I/O | Port 3<br>10-bit I/O port<br>Input/output can be specified in 1-bit units. | TXDA0 |
| P31 | | | RXDA0/INTP7 |
| P32 | | | ASCKA0/TIP00/TOP00/ TOP01 |
| P33 | | | TIP01/TOP01/CTXD0 |
| P34 | | | TIP10/TOP10/CRXD0 |
| P35 | | | TIP11/TOP11 |
| P36 | | | CTXD1 |
| P37 | | | CRXD1 |
| P38 | | | TXDA2 |
| P39 | | | RXDA2/INTP8 |
| P40 | I/O | Port 4<br>3-bit I/O port<br>Input/output can be specified in 1-bit units. | SIB0 |
| P41 | | | SOB0 |
| P42 | | | SCKB0 |

***Table 2-2: Pin List (Port Pins) (Continued)***

| Pin Name | I/O | Function | Alternate Function |
|---|---|---|---|
| P50 | I/O | Port 5<br>6-bit I/O port<br>Input/output can be specified in 1-bit units. | KR0/TIQ01/TOQ01 |
| P51 | | | KR1/TIQ02/TOQ02 |
| P52 | | | KR2/TIQ03/TOQ03/DDI |
| P53 | | | KR3/TIQ00/TOQ00/DDO |
| P54 | | | KR4/DCK |
| P55 | | | KR5/DMS |
| P70 to P715 | I/O | Port 7<br>16-bit I/O port<br>Input/output can be specified in 1-bit units. | ANI0 to ANI15 |
| P90 | I/O | Port 9<br>16-bit I/O port<br>Input/output can be specified in 1-bit units. | KR6/TXDA1 |
| P91 | | | KR7/RXDA1 |
| P92 | | | TIQ11/TOQ11 |
| P93 | | | TIQ12/TOQ12 |
| P94 | | | TIQ13/TOQ13 |
| P95 | | | TIQ10/TOQ10 |
| P96 | | | TIP21/TOP21 |
| P97 | | | SIB1/TIP20/TOP20 |
| P98 | | | SOB1 |
| P99 | | | SCKB1 |
| P910 | | | - |
| P911 | | | - |
| P912 | | | - |
| P913 | | | INTP4/PCL |
| P914 | | | INTP5 |
| P915 | | | INTP6 |
| PCM0 | I/O | Port CM<br>4-bit I/O port<br>Input/output can be specified in 1-bit units. | - |
| PCM1 | | | CLKOUT |
| PCM2, PCM3 | | | - |
| PCS0, PCS1 | I/O | Port CS<br>2-bit I/O port<br>Input/output can be specified in 1-bit units. | - |
| PCT0, PCT1, PCT4, PCT6 | I/O | Port CT<br>4-bit I/O port<br>Input/output can be specified in 1-bit units. | - |
| | | | - |
| PDL0 to PDL4 | I/O | Port DL<br>14-bit I/O port<br>Input/output can be specified in 1-bit units. | - |
| PDL5 | | | FLMD1 |
| PDL6 to PDL13 | | | - |

***Table 2-3: Pin List (Non-Port Pins)***

| Pin Name | I/O | Function | Alternate Function |
|---|---|---|---|
| NMI | Input | External interrupt input (non-maskable, with analog noise eliminated) | P02 |
| INTP0 | Input | External interrupt request input (maskable, with analog noise eliminated) | P03/ADTRG |
| INTP1 | | | P04 |
| INTP2 | | | P05/DRST |
| INTP3 | | | P06 |
| INTP4 | | | P913/PCL |
| INTP5 | | | P914 |
| INTP6 | | | P915 |
| INTP7 | | | P31/RXDA0 |
| INTP8 | | | P39/RXDA2 |
| INTP9 | | | P10 |
| INTP10 | | | P11 |
| TIP00 | Input | External event/clock input (TMP00) | P32/ASCKA0/TOP00/TOP01 |
| TIP01 | | External event/clock input (TMP01) | P33/TOP01/CTXD0 |
| TIP10 | | External event/clock input (TMP10) | P34/TOP10/CRXD0 |
| TIP11 | | External event/clock input (TMP11) | P35/TOP11 |
| TIP20 | | External event/clock input (TMP20) | P97/SIB1/TOP20 |
| TIP21 | | External event/clock input (TMP21) | P96/TOP21 |
| TIP30 | | External event/clock input (TMP30) | P01/TOP30 |
| TIP31 | | External event/clock input (TMP31) | P00/TOP31 |
| TOP00 | Output | Timer output (TMP00) | P32/ASCKA0/TIP00/TOP01 |
| TOP01 | | Timer output (TMP01) | P32/ASCKA0/TIP00/TOP00 |
| | | | P33/TIP01/CTXD0 |
| TOP10 | | Timer output (TMP10) | P34/TIP10/CRXD0 |
| TOP11 | | Timer output (TMP11) | P35/TIP11 |
| TOP20 | | Timer output (TMP20) | P97/SIB1/TIP20 |
| TOP21 | | Timer output (TMP21) | P96/TIP21 |
| TOP30 | | Timer output (TMP30) | P01/TIP30 |
| TOP31 | | Timer output (TMP31) | P00/TIP31 |
| TIQ00 | Input | External event/clock input (TMQ00) | P53/KR3/TOQ00/DDO |
| TIQ01 | | External event input (TMQ01) | P50/KR0/TOQ01 |
| TIQ02 | | External event input (TMQ02) | P51/KR1/TOQ02 |
| TIQ03 | | External event input (TMQ03) | P52/KR2/TOQ03/DDI |
| TIQ10 | | External event input (TMQ10) | P95/TOQ10 |
| TIQ11 | | External event input (TMQ11) | P92/TOQ11 |
| TIQ12 | | External event input (TMQ12) | P93/TOQ12 |
| TIQ13 | | External event input (TMQ13) | P94/TOQ13 |

***Table 2-3: Pin List (Non-Port Pins) (Continued)***

| Pin Name | I/O | Function | Alternate Function |
|---|---|---|---|
| TOQ00 | Output | Timer output (TMQ00) | P53/KR3/TIQ00/DDO |
| TOQ01 | | Timer output (TMQ01) | P50/KR0/TIQ01 |
| TOQ02 | | Timer output (TMQ02) | P51/KR1/TIQ02 |
| TOQ03 | | Timer output (TMQ03) | P52/KR2/TIQ03/DDI |
| TOQ10 | | Timer output (TMQ10) | P95/TIQ10 |
| TOQ11 | | Timer output (TMQ11) | P92/TIQ11 |
| TOQ12 | | Timer output (TMQ12) | P93/TIQ12 |
| TOQ13 | | Timer output (TMQ13) | P94/TIQ13 |
| SIB0 | Input | Serial receive data input (CSIB0) | P40 |
| SIB1 | | Serial receive data input (CSIB1) | P97/TIP20/TOP20 |
| SOB0 | Output | Serial transmit data output (CSIB0) | P41 |
| SOB1 | | Serial transmit data output (CSIB1) | P98 |
| SCKB0 | I/O | Serial clock I/O (CSIB0) | P42 |
| SCKB1 | | Serial clock I/O (CSIB1) | P99 |
| RXDA0 | Input | Serial receive data input (UARTA0) | P31/INTP7 |
| RXDA1 | | Serial receive data input (UARTA1) | P91/KR7 |
| RXDA2 | | Serial receive data input (UARTA2) | P39/INTP8 |
| TXDA0 | Output | Serial transmit data output (UARTA0) | P30 |
| TXDA1 | | Serial transmit data output (UARTA1) | P90/KR6 |
| TXDA2 | | Serial transmit data output (UARTA2) | P38 |
| ASCKA0 | Input | Baud rate clock input to UARTA0 | P32/TIP00/TOP00/TOP01 |
| CRXD0 | Input | CAN receive data input (CAN0) | P34/TIP10/TOP10 |
| CRXD1 | | CAN receive data input (CAN1) | P37 |
| CTXD0 | Output | CAN transmit data output (CAN0) | P33/TIP01/TOP01 |
| CTXD1 | | CAN transmit data output (CAN1) | P36 |
| ANI0 to ANI15 | Input | Analog voltage input to A/D converter | P70 to P715 |
| $AV_{REF0}$ | Input | Reference voltage input to A/D converter (same potential as $V_{DD}$) | – |
| $AV_{SS}$ | – | Ground potential for A/D and D/A converters (same potential as $V_{SS}$) | – |
| ADTRG | Input | A/D converter external trigger input | P03/INTP0 |
| KR0 | Input | Key interrupt input | P50/TIQ01/TOQ01 |
| KR1 | | | P51/TIQ02/TOQ02 |
| KR2 | | | P52/TIQ03/TOQ03/DDI |
| KR3 | | | P53/TIQ00/TOQ00/DDO |
| KR4 | | | P54/DCK |
| KR5 | | | P55/DMS |
| KR6 | | | P90/TXDA1 |
| KR7 | | | P91/RXDA1 |
| DMS | Input | Debug mode select | P55/KR5 |
| DDI | Input | Debug data input | P52/KR2/TIQ03/TOQ03 |
| DDO | Output | Debug data output | P53/KR3/TIQ00/TOQ00 |

***Table 2-3: Pin List (Non-Port Pins) (Continued)***

| Pin Name | I/O | Function | Alternate Function |
|---|---|---|---|
| DCK | Input | Debug clock input | P54/KR4 |
| DRST | Input | Debug reset input | P05/INTP2 |
| FLMD0 | Input | Flash programming mode setting pins | - |
| FLMD1 | | | PDL5 |
| CLKOUT | Output | Internal system clock output | PCM1 |
| PCL | Output | Clock output (timing output of X1 input clock and sub-clock) | P913/INTP4 |
| REGC | - | Regulator output stabilizing capacitor connection | - |
| RESET | Input | System reset input | - |
| X1 | Input | Main clock resonator connection | - |
| X2 | - | | - |
| XT1 | Input | Subclock resonator connection | - |
| XT2 | - | | - |
| $V_{DD}$ | - | Positive power supply pin for internal circuitry | - |
| $V_{SS}$ | - | Ground potential for internal circuitry | - |
| $EV_{DD}$ | - | Positive power supply pin for external circuitry (same potential as $V_{DD}$) | - |
| $EV_{SS}$ | - | Ground potential for external circuitry (same potential as $V_{SS}$) | - |
| $BV_{DD}$ | - | Positive power supply pin for external circuitry (same potential as $V_{DD}$) | - |
| $BV_{SS}$ | - | Ground potential for external circuitry (same potential as $V_{SS}$) | - |

***Table 2-4: Pin I/O Circuit Types and Recommended Connection of Unused Pins***

| Pin | I/O Circuit Type | Recommended Connection |
|---|---|---|
| P00/TIP31/TOP31 | 5-W | Input: Independently connect to EVDD or EVSS via a resistor<br>Output: Leave open |
| P01/TIP30/TOP30 | | |
| P02/NMI | | |
| P03/INTP0/ADTRG | | |
| P04/INTP1 | | |
| P05/INTP2/DRST | 5-AF | Input: Independently connect to EVSS via a resistor<br>Output: Leave open |
| P06/INTP3 | 5-W | Input: Independently connect to EVDD or EVSS via a resistor<br>Output: Leave open |
| P10/INTP9 | 5-W | Input: Independently connect to EVDD or EVSS via a resistor<br>Output: Leave open |
| P11/INTP10 | | |
| P30/TXDA0 | 5-A | Input: Independently connect to EVDD or EVSS via a resistor<br>Output: Leave open |
| P31/RXDA0/INTP7 | 5-W | |
| P32/ASCKA0/TIP00/TOP00/TOP01 | | |
| P33/TIP01/TOP01/CTXD0 | | |
| P34/TIP10/TOP10/CRXD0 | | |
| P35/TIP11/TOP11 | | |
| P36/CTXD1 | 5-A | |
| P37/CRXD1 | 5-W | |
| P38/TXDA2 | 5-A | |
| P39/RXDA2/INTP8 | 5-W | |
| P40/SIB0 | 5-W | Input: Independently connect to EVDD or EVSS via a resistor<br>Output: Leave open |
| P41/SOB0 | 5-A | |
| P42/SCKB0 | 5-W | |
| P50/KR0/TIQ01/TOQ01 | 5-W | Input: Independently connect to EVDD or EVSS via a resistor<br>Output: Leave open |
| P51/KR1/TIQ02/TOQ02 | | |
| P52/KR2/TIQ03/TOQ03/DDI | | |
| P53/KR3/TIQ00/TOQ00/DDO | | |
| P54/KR4/DCK | | |
| P55/KR5/DMS | | |
| P70/ANI0 to P711/ANI11 | 11-G | Input: Independently connect to AVREF0 or AVSS via a resistor<br>Output: Leave open |
| P712/ANI12 to P715/ANI15 | | |
| P90/KR6/TXDA1 | 5-W | Input: Independently connect to EVDD or EVSS via a resistor<br>Output: Leave open |
| P91/KR7/RXDA1 | | |
| P92/TIQ11/TOQ11 | | |
| P93/TIQ12/TOQ12 | | |
| P94/TIQ13/TOQ13 | | |
| P95/TIQ10/TOQ10 | | |

***Table 2-4: Pin I/O Circuit Types and Recommended Connection of Unused Pins (Continued)***

| | | |
|---|---|---|
| P96/TIP21/TOP21 | 5-W | Input: Independently connect to EVDD or EVSS via a resistor<br>Output: Leave open |
| P97/SIB1/TIP20/TOP20 | | |
| P98/SOB1 | 5-A | |
| P99/SCKB1 | 5-W | |
| P910 | 5-A | |
| P911 | | |
| P912 | | |
| P913/INTP4/PCL | 5-W | |
| P914/INTP5 | | |
| P915/INTP6 | | |
| PCM0 | 5 | Input: Independently connect to BVDD or BVSS via a resistor<br>Output: Leave open |
| PCM1/CLKOUT | | |
| PCM2, PCM3 | | |
| PCS0, PCS1 | 5 | Input: Independently connect to BVDD or BVSS via a resistor<br>Output: Leave open |
| PCT0, PCT1, PCT4, PCT6 | 5 | Input: Independently connect to BVDD or BVSS via a resistor<br>Output: Leave open |
| PDL0 to PDL4 | 5 | Input: Independently connect to BVDD or BVSS via a resistor<br>Output: Leave open |
| PDL5/ FLMD1 | | |
| PDL6 to AD13 | | |
| AVREF0 | - | Directly connect to VDD |
| AVSS | - | - |
| FLMD0[a] | - | Directly connect to VSS |
| REGC | - | - |
| RESET | 2 | - |
| X1 | - | - |
| X2 | - | - |
| XT1 | 16 | Connect to VSS via a resistor |
| XT2 | 16 | Leave open |
| VDD | - | - |
| VSS | - | - |
| BVDD | - | - |
| BVSS | - | - |
| EVDD | - | - |
| EVSS | - | - |

a. If noise that exceeds the noise elimination width is input to the RESET pin during self programming, the flash on-board mode may be entered depending on the capacitance charge end timing when a capacitor is connected to the FLMD0 pin. Therefore, do not connect a capacitor to the FLMD0 pin.

***Figure 2-2: Pin I/O Circuit Types (1/2)***

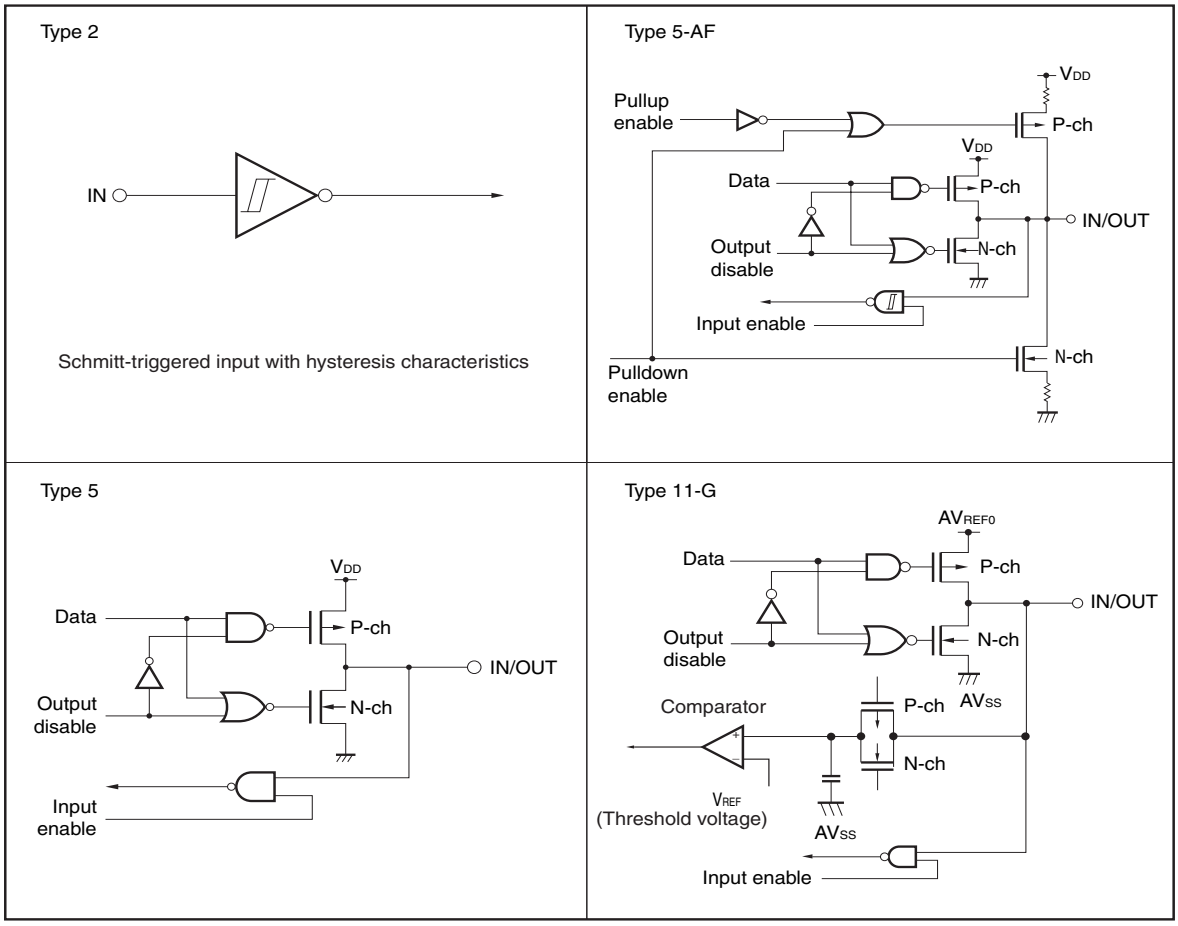
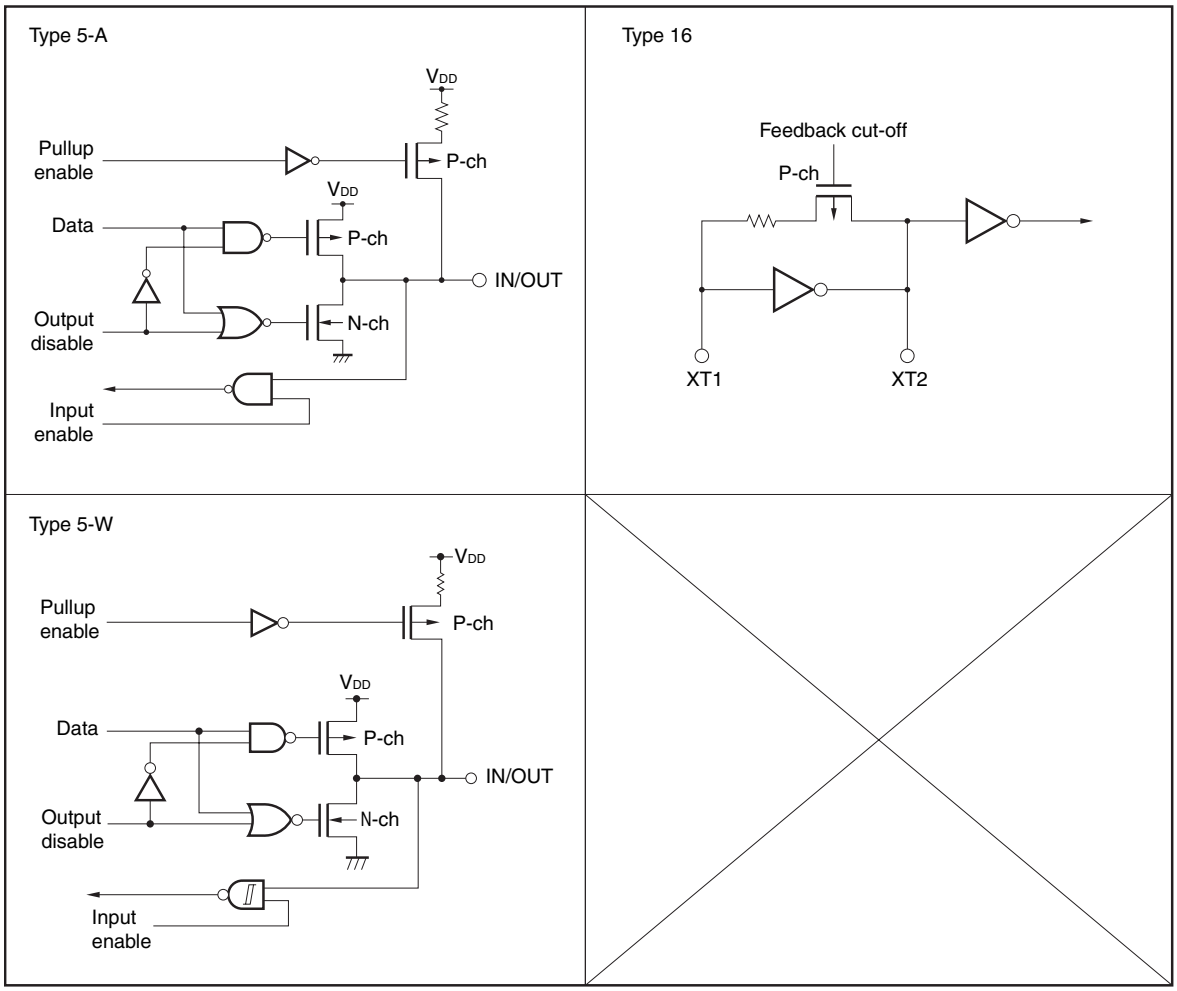


***Figure 2-3: Figure 2-1. Pin I/O Circuit Types (2/2)***



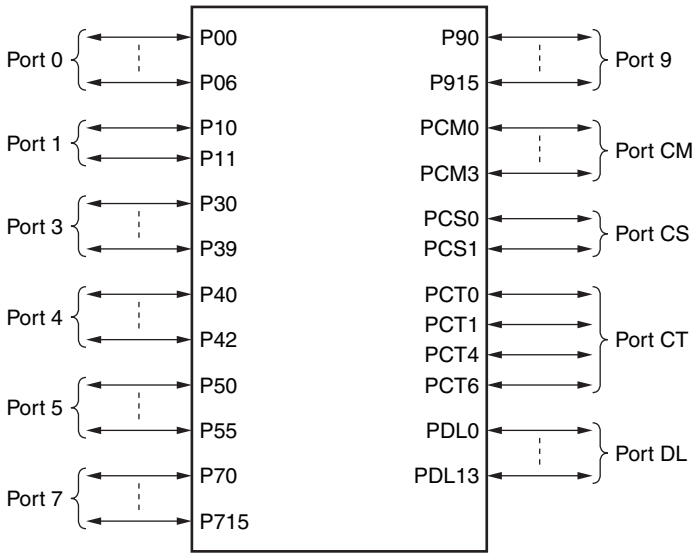
## 2.2 Port Functions

### Features

- I/O ports: 84
- Port pins function alternately as other peripheral-function I/O pins
- Can be set in input or output mode in 1-bit units.

The V850ES/FG2 has a total of 84 I/O ports, ports 0, 1, 3 to 5, 7, 9, CM, CS, CT, and DL. The port configuration is shown below.

***Figure 2-4: Port Configuration***



## 2.3 CPU Functions

Based on the RISC architecture, the CPU of the V850ES/FG2 executes most of the instructions in one clock under control of a five-stage pipeline.

**Features**

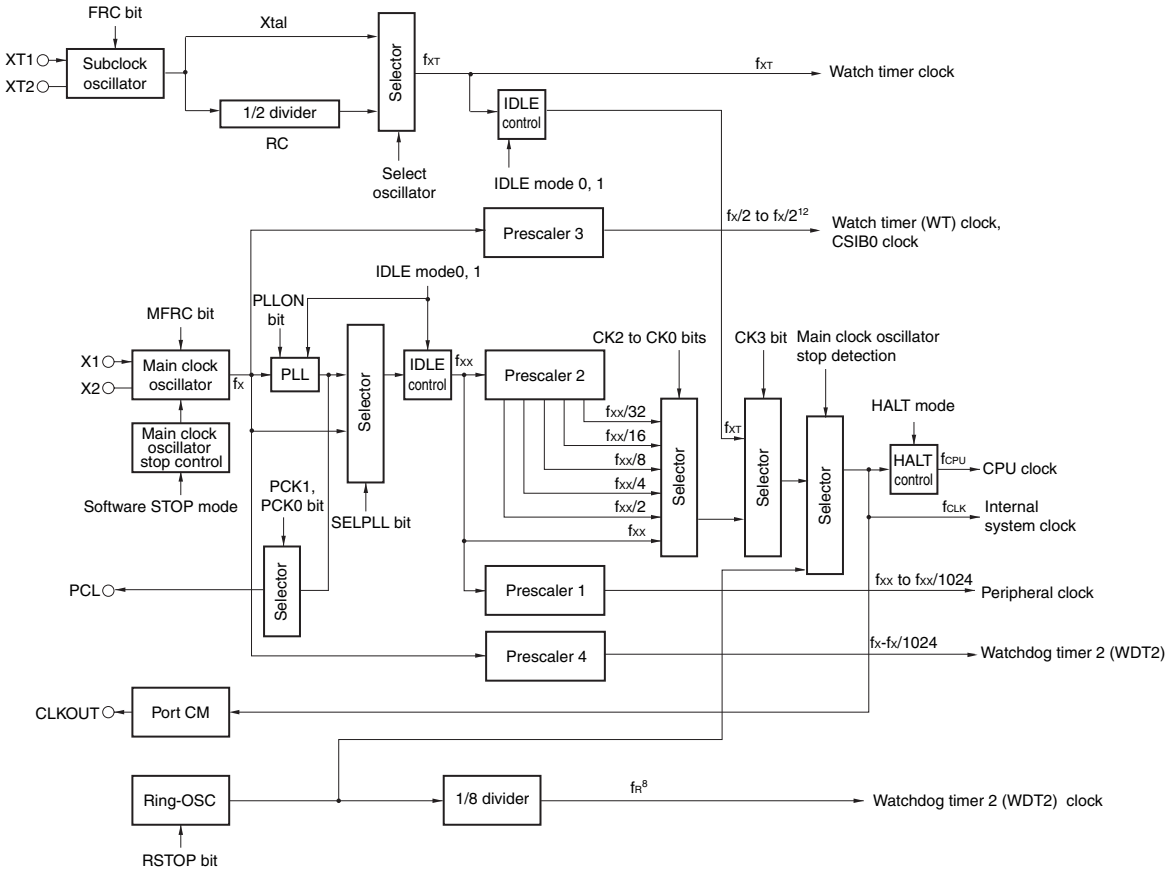
- Minimum instruction execution time: 50 ns (at 20 MHz operation)
- Memory space
  - Program space: 64 MB, linear
  - Data space: 4 GB, linear
- General-purpose registers: 32 bits × 32
- Internal 32-bit architecture
- Five-stage pipeline control
- Multiplication/division instructions
- Saturation operation instructions
- 32-bit shift instructions: 1 clock
- Load/store instructions with long/short format
- Four types of bit manipulation instructions
  - SET1
  - CLR1
  - NOT1
  - TST1

## 2.4 Clock Generation Function

The following clock generation functions are available.

- Main clock oscillator
- In clock-through mode
  $f_X$ = 4 to 5 MHz ($f_{XX}$ = 4 to 5 MHz)
- In PLL (Phase Locked Loop) mode
  $f_X$ = 4 to 5 MHz ($f_{XX}$ = 16 to 20 MHz)
- Subclock oscillator (sub-resonator)
- 32.768 kHz
- 20 kHz (RCR = 390 kΩ, C = 47 pF)
- Multiply (×4) function via PLL (Phase Locked Loop)
- Clock-trough mode/PLL mode selectable
- Ring OSC
- $f_R$ = 100 to 400 kHz
- Internal system clock generation
- 7 steps ($f_{XX}$, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/32$, $f_{XT}$)
- Peripheral clock generation
- Clock output function
- Programmable clock output (PCL) function

***Figure 2-5: Clock Generator***



## 2.5 16-bit Timer/event Counter P

The V850ES/FG2 includes 16-bit timer/event counter P (TMP0 to TMP3).

**Features**

Timer P (TMP) is a 16-bit timer/event counter that can be used in various ways.
TMP can perform the following operations.

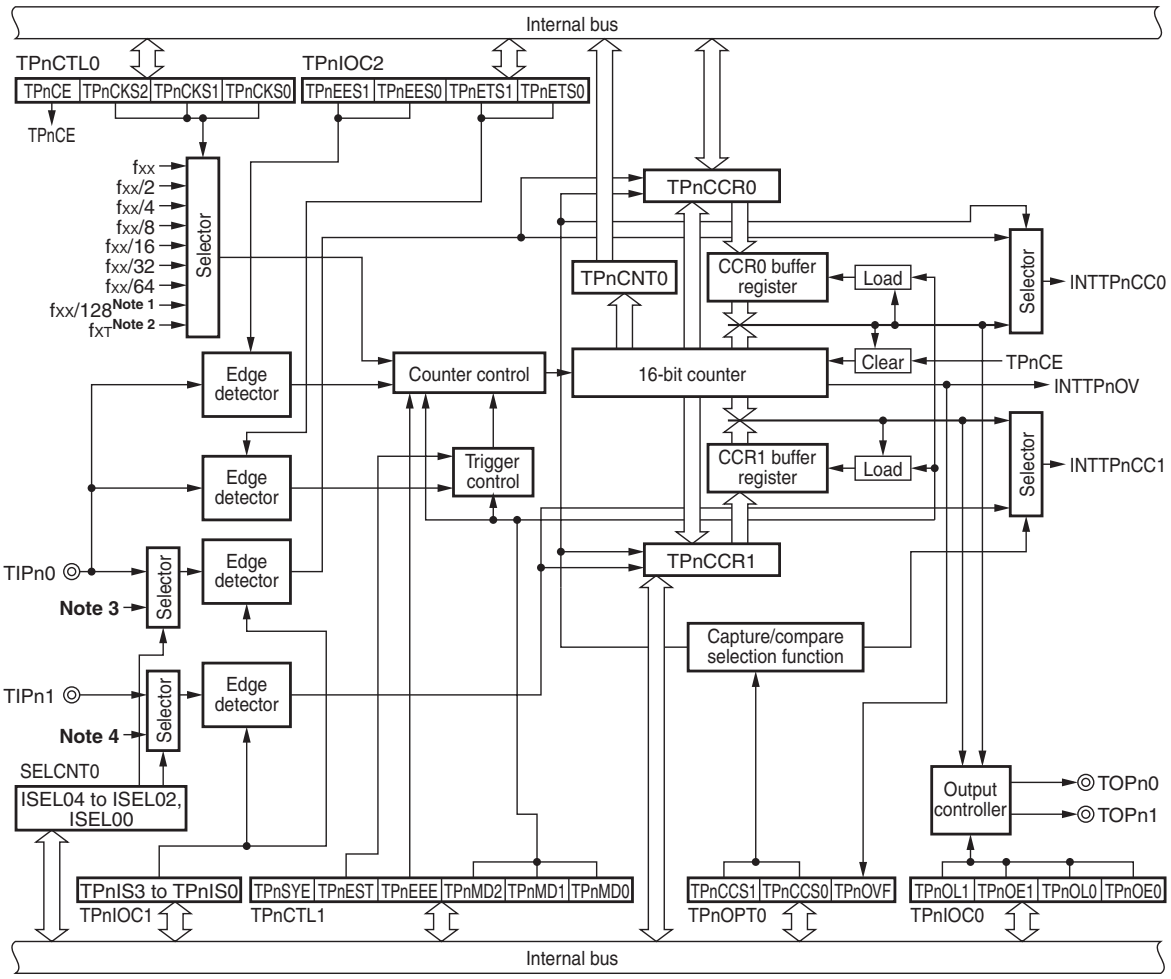
- PWM output
- Interval timer
- External event counter (operation disabled when clock is stopped)
- One-shot pulse output
- Pulse width measurement function
- Timer synchronized operation function
- Free-running function
- External trigger pulse output function

Functional Outline

- Capture trigger input signal × 2
- External trigger input signal × 1
- Clock selection × 8
- External event count input × 1
- Readable counter × 1
- Capture/compare reload register × 2
- Capture/compare match interrupt × 2
- Timer output (TOPn0, TOPn1) × 2

**Remark:** n = 0 to 3

***Figure 2-6: Figure 6-1. Block Diagram of Timer P***




**Notes: 1.** TMP0, TMP2

**2.** TMP1, TMP3 (when main clock is stopped, count operation by subclock cannot be performed.)

**3.** TSOUT signal of CAN0 block (TMP0)
RXDA0 pin (TMP1)

**4.** INTTM0EQ0 interrupt of TMM block or TSOUT signal of CAN1 block (TMP0)
RXDA1 pin (TMP1)

**Remark:** n = 0 to 3

## 2.6 16-bit Timer/event Counter Q

The V850ES/FG2 includes 16-bit timer/event counter Q (TMQ0, TMQ1).

**Features**

Timer Q (TMQ) is a 16-bit timer/event counter that can be used in various ways.
TMQ can perform the following operations.

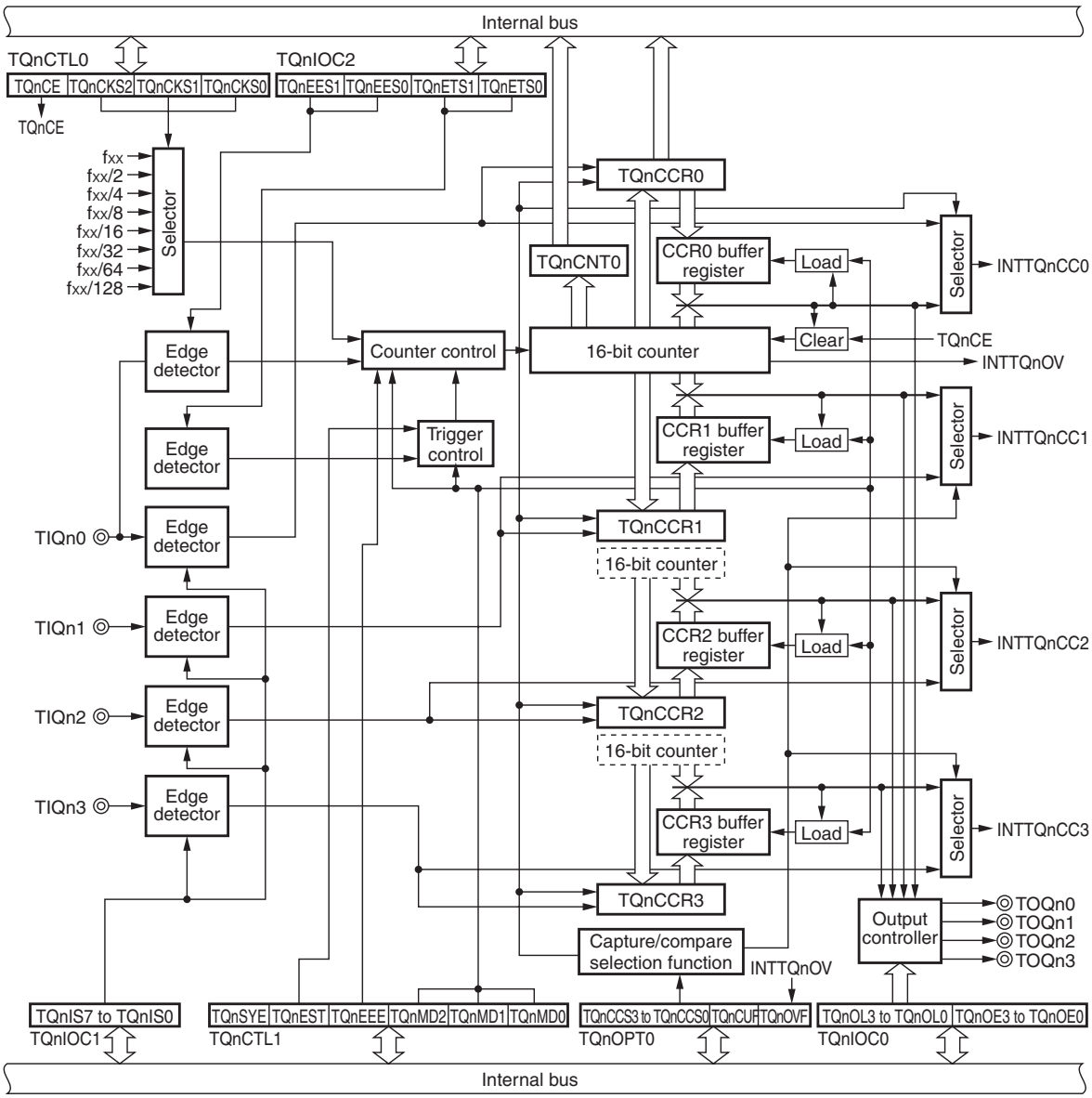
- PWM output
- Interval timer
- External event counter (operation disabled when clock is stopped)
- One-shot pulse output
- Pulse width measurement function
- Triangular wave PWM output
- Timer synchronized operation function

Functional Outline

- Capture trigger input signal × 4
- External trigger input signal × 1
- Clock selection × 8
- External event count input × 1
- Readable counter × 1
- Capture/compare reload register × 4
- Capture/compare match interrupt × 4
- Timer output (TOQn0 to TOQn3) × 4

**Remark:** n = 0, 1

***Figure 2-7: Figure 7-1. Block Diagram of Timer Q***




**Remark:** n = 0, 1

## 2.7 16-bit Interval Timer M

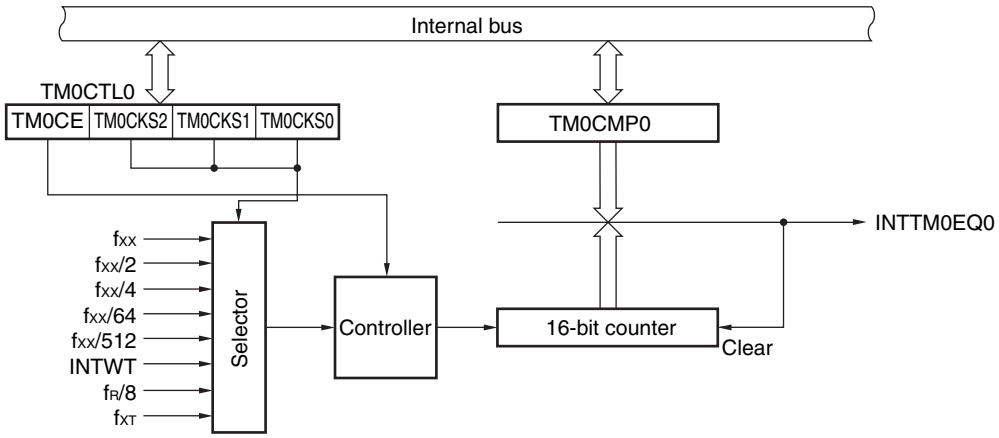
The V850ES/FG2 includes 16-bit interval timer M (TMM0).

**Features**

Timer M (TMM) supports only a clear & start mode. It does not support a free-running mode. To use timer M in a manner equivalent to in the free-running mode, set the compare register to FFFFH and start the 16-bit counter. A match interrupt will occur when the timer overflows.

- Interval function
- Clock selection × 8
- Simple counter × 1
  (The simple counter is a counter that does not use a counter read buffer. This counter cannot be read during timer count operation.)
- Simple compare × 1
  (The simple compare register is a register that does not use a compare write buffer. No data can be written to this compare register during timer count operation.)
- Compare match interrupt × 1

***Figure 2-8: Block Diagram of Timer M***



## 2.8 Watch Timer Functions

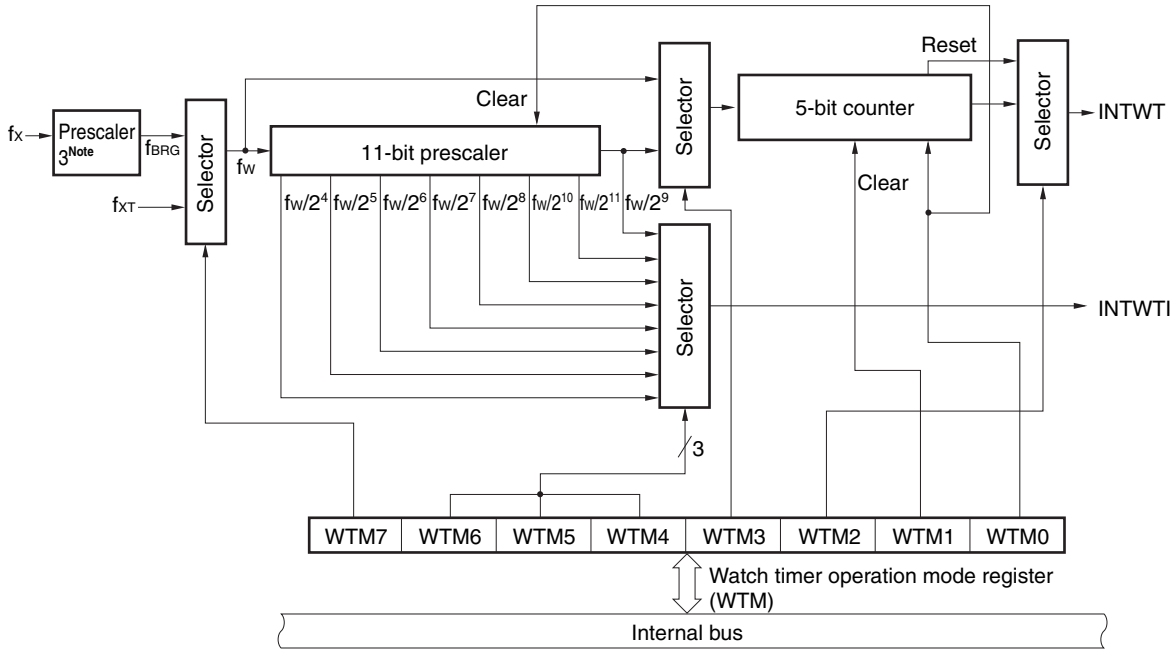
### Features

The watch timer has the following functions.

- Watch timer
- Interval timer

The watch timer and interval timer functions can be used at the same time.

***Figure 2-9: Block Diagram of Watch Timer***




**Note:** For details of prescaler 3, see Figure 2-10 “Block Diagram of Prescaler 3”.

**Remarks:** **1.** $f_{BRG}$:Prescaler 3 output frequency

**2.** $f_X$:Oscillation frequency

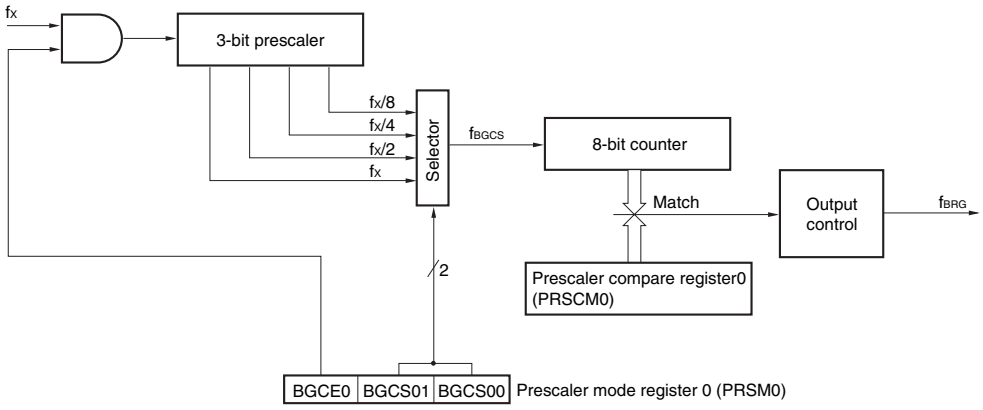
**3.** $f_{XT}$:Subclock frequency

**4.** $f_W$:Watch timer clock frequency

**5.** INTWT:Watch timer interrupt

**6.** INTWTI:Interval timer interrupt

***Figure 2-10: Block Diagram of Prescaler 3***




**Remark:** $f_{BGCS}$:Prescaler 3 count clock frequency

**1.** $f_{BRG}$:Prescaler 3 output frequency

**2.** $f_X$:Oscillation frequency

## 2.9 Functions of Watchdog Timer 2

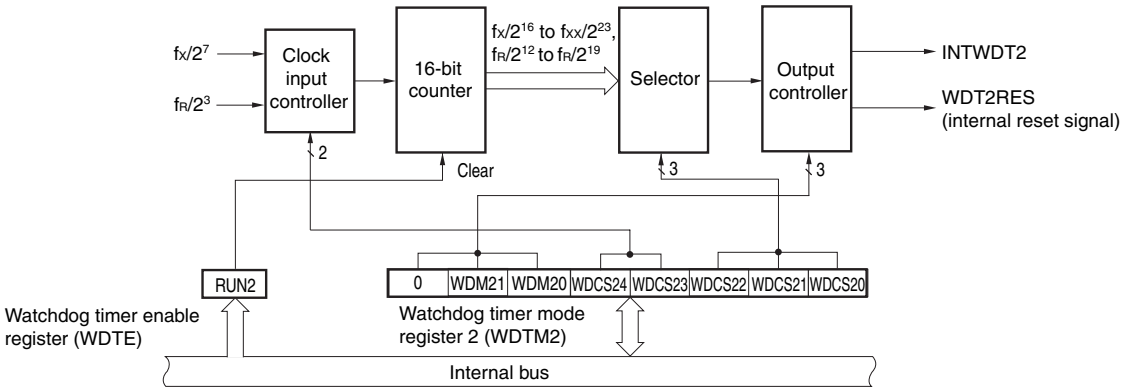
### Features

Watchdog timer 2 has the following functions.

- Default-start watchdog timer
  - →Reset mode: Reset operation upon overflow of watchdog timer 2 (generation of WDT2RES signal)
  - →Non-maskable interrupt request mode: NMI operation upon overflow of watchdog timer 2 (generation of INTWDT2 signal)**Note**
- Input selectable from main clock and Ring-OSC as the source clock

**Note:** Restoring using the RETI instruction following non-maskable interrupt servicing due to a non-maskable interrupt request signal (INTWDT2) is not possible. Therefore, following completion of interrupt servicing, perform a system reset.

***Figure 2-11: Block Diagram of Watchdog Timer 2***




**Remarks:** **1.** $f_X$: Oscillation frequency

**2.** $f_R$: Ring-OSC clock frequency

**3.** INTWDT2: Non-maskable interrupt request signal from watchdog timer 2

**4.** WDT2RES: Watchdog timer 2 reset signal

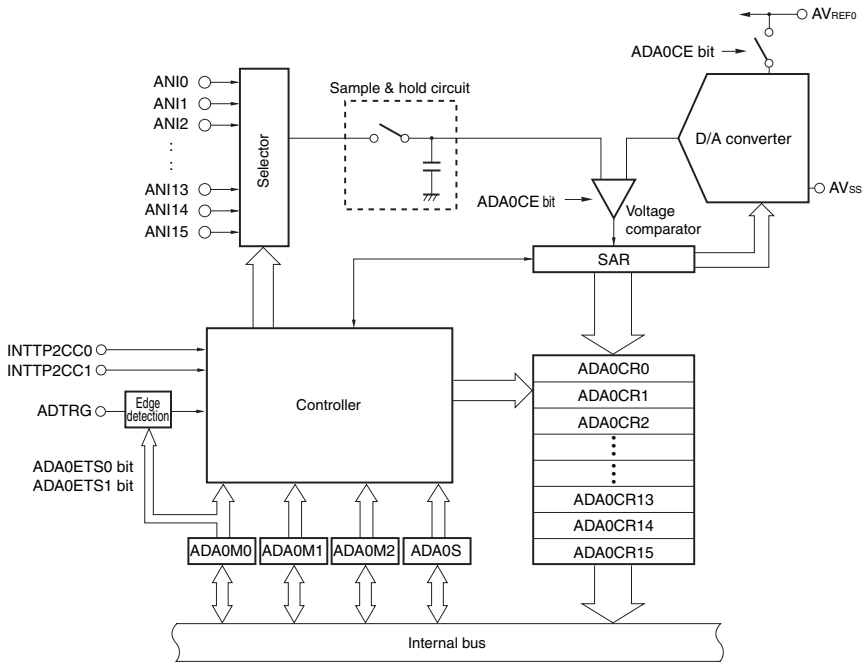
## 2.10 A/D Converter

### Features

The A/D converter converts analog input signals into digital values, has a resolution of 10 bits, and can handle 16 analog input signal channels (ANI0 to ANI15).
The A/D converter has the following features.

- 10-bit resolution
- 16 channels
- Successive approximation method
- Operating voltage: $AV_{REF0}$ = 4.0 to 5.5 V
- Analog input voltage: 0 V to $AV_{REF0}$
- The following functions are provided as operation modes.
  - Continuous select mode
  - Continuous scan mode
  - One-shot scan mode
- The following functions are provided as trigger modes.
  - Software trigger mode
  - External trigger mode (external, 1)
  - Timer trigger mode
- Power-fail monitor function (conversion result compare function)

***Figure 2-12: Block Diagram of A/D Converter***



## 2.11 Asynchronous Serial Interface A (UARTA)

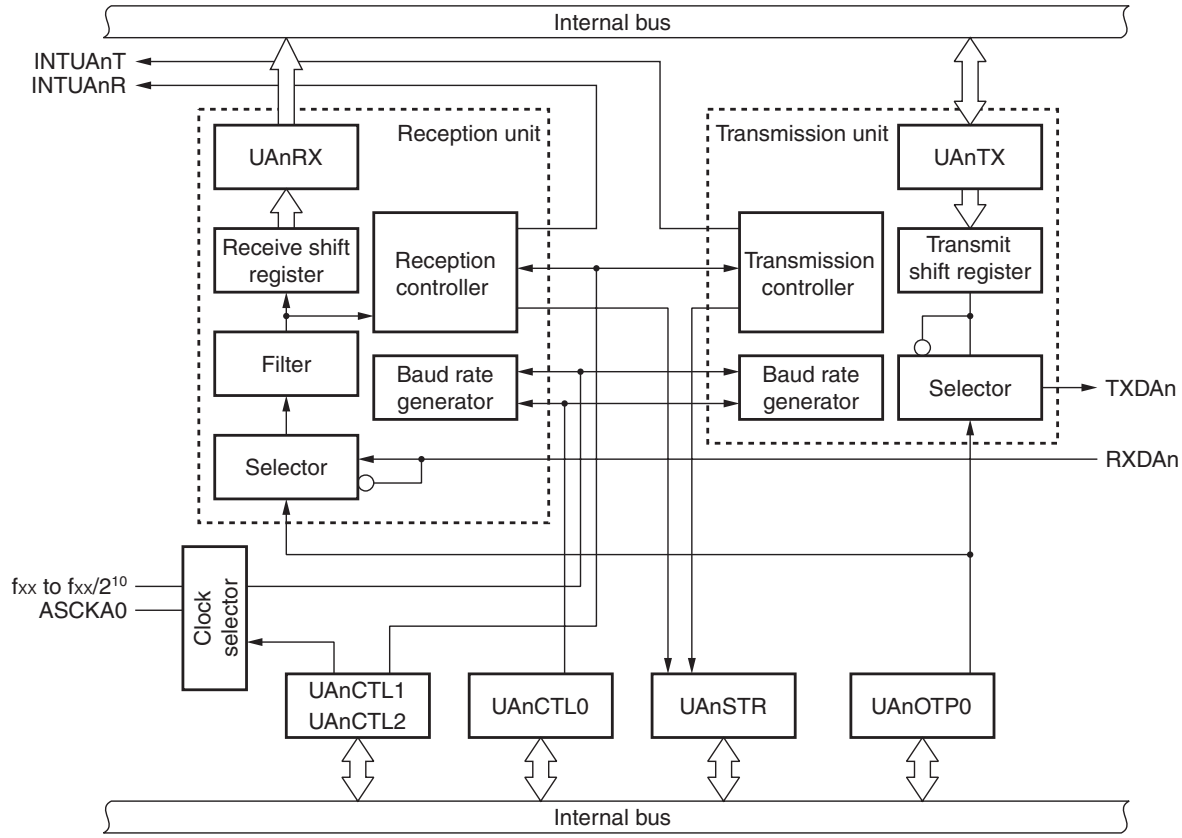
The V850ES/FG2 includes asynchronous serial interface A (UARTA).

**Features**

- Transfer rate: 300 bps to 312.5 kbps (using internal system clock of 20 MHz and dedicated baud rate generator)
- Full-duplex communication
  - UARTA receive data register n (UAnRX)
  - UARTA transmit data register n (UAnTX)
- 2-pin configurationTXDAn:
  - Output pin of transmit data
  - RXDAn: Input pin of receive data
- Reception error detection function
  - Parity error
  - Framing error
  - Overrun error
- Interrupt sources: 2 types
  - Reception complete interrupt (INTUAnR): An interrupt is generated in the reception enabled status by ORing three types of reception errors. It is also generated when receive data is transferred from the shift register to receive buffer register n after completion of serial transfer.
  - Transmission enable interrupt (INTUAnT): Generated when transmit data is transferred from the transmit buffer register to the shift register in the transmission enabled status.
- Character length of transmit/receive data is specified by the UAnCTL0 register.
- Character length: 7 or 8 bits
- Parity function: Odd, even, 0, none
- Transmission stop bit: 1 or 2 bits
- Dedicated baud rate generator
- MSB/LSB first transfer selectable
- Transmit/receive data reversible
- 13 to 20 bits selectable for SBF (Sync Break Field) transmission in LIN (Local Interconnect Network) communication format
- 11 or more bits recognizable for SBF reception in LIN communication format
- SBF reception flag

**Remark:** n = 0 to 2

***Figure 2-13: Block Diagram of Asynchronous Serial Interface A***




**Remark:** n = 0 to 2

## 2.12 3-Wire Serial Interface (CSIB)

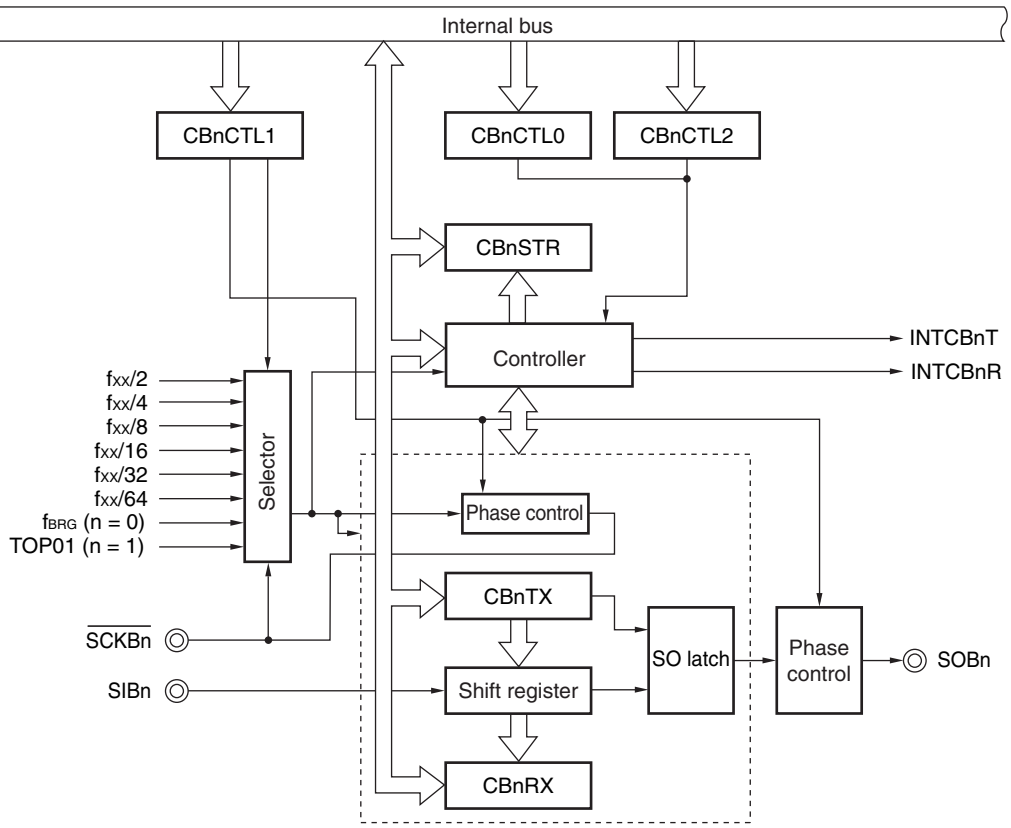
The V850ES/FG2 includes a 3-wire serial interface (CSIB).

**Features**

- Master mode and slave mode selectable
- 3-wire serial interface for 8-bit to 16-bit transfer
- Interrupt request signals (INTCBnT and INTCBnR)
- Serial clock and data phase selectable
- Transfer data length selectable from 8 to 16 bits in 1-bit units
- Data transfer with MSB- or LSB-first selectable
- 3-wireSOBn:
  - Serial data output
  - SIBn:Serial data input
  - SCKBn:Serial clock I/O
- Transmission mode, reception mode, and transmission/reception mode selectable

**Remark:** n = 0, 1

***Figure 2-14: Block Diagram of 3-Wire Serial Interface***




**Remark:** n = 0, 1

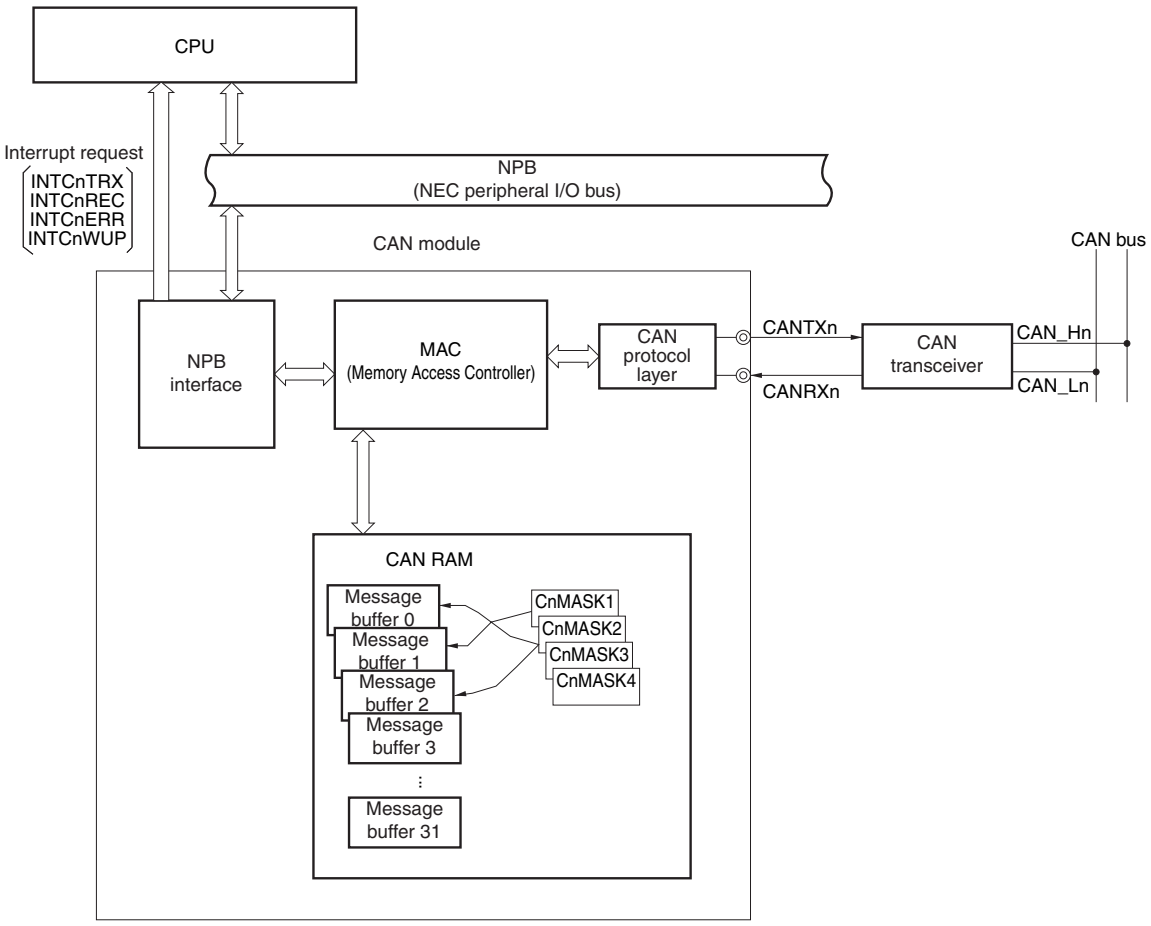
## 2.13 CAN Controller

This product features an on-chip 2-channel CAN (Controller Area Network) controller that complies with the CAN protocol as standardized in ISO 11898. The number of channels varies depending on the product as shown below.

**Features**

- Compliant with ISO 11898 and tested according to ISO/DIS 16845 (CAN conformance test)
- Standard frame and extended frame transmission/reception enabled
- Transfer rate: 1 Mbps max. (CAN clock input ≥ 8 MHz)
- 32 message buffers × 2 channels
- Receive/transmit history list function
- Automatic block transmission function
- Multi-buffer receive block function
- Mask setting of four patterns is possible for each channel

***Figure 2-15: Block Diagram of CAN Module***




**Remark:** n = 0, 1

## 2.14 Interrupt/Exception Processing Function

The V850ES/FG2 is provided with a dedicated interrupt controller (INTC) for interrupt servicing.
An interrupt is an event that occurs independently of program execution, and an exception is an event whose occurrence is dependent on program execution.
The V850ES/FG2 can process interrupt request signals from the on-chip peripheral hardware and external sources. Moreover, exception processing can be started by the TRAP instruction (software exception) or by generation of an exception event (i.e. fetching of an illegal opcode) (exception trap).

**Features**

- Interrupts
  - Non-maskable interrupts: 1 source
  - Maskable interrupts: External: 11, Internal: 50 sources
    - 8 levels of programmable priorities (maskable interrupts)
    - Multiple interrupt control according to priority
    - Masks can be specified for each maskable interrupt request
  - Noise elimination, edge detection, and valid edge specification for external interrupt request signals
  - Exceptions
    - Software exceptions: 32 sources
    - Exception trap: 2 sources (illegal opcode exception, debug trap)

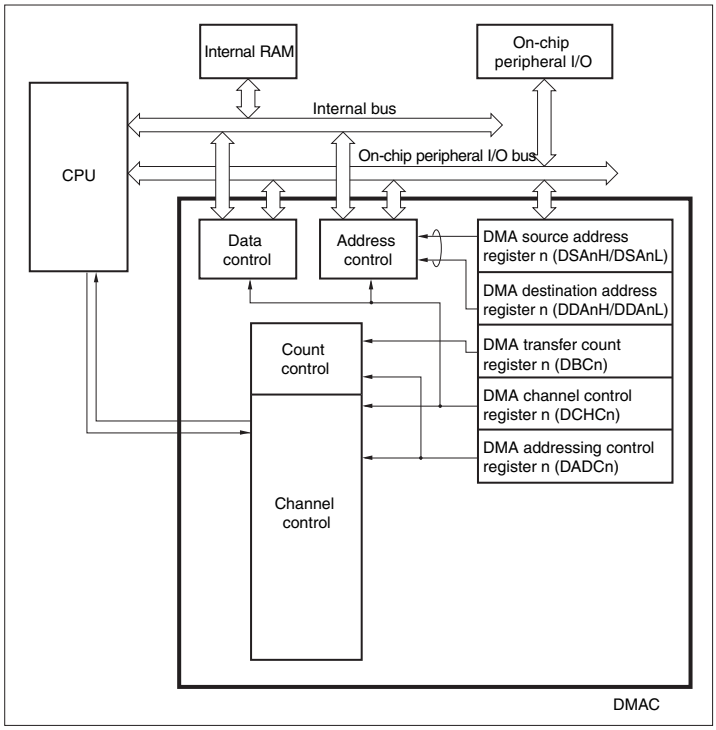
## 2.15 DMA Controller (DMAC)

The V850ES/FG2 incorporates a direct memory access (DMA) controller (DMAC) that executes and controls DMA transfer. The V850ES/FG2 incorporates four independent DMA channels.
The DMAC controls data transfer between memory and I/O, between memories, or between I/Os based on DMA requests issued by the on-chip peripheral I/O (serial interface, real-time pulse unit, and A/D converter), interrupts from external input pins, or software triggers (memory refers to internal RAM or external memory).

**Features**

- 4 independent DMA channels
- Transfer unit: 8/16 bits
- Maximum transfer count: 65,536 ($2^{16}$)
- Transfer type: Two-cycle transfer
- Transfer mode: Single transfer mode
- Transfer requests
  - Request by interrupts from on-chip peripheral I/O (serial interface, timer/counter, A/D converter) or interrupts from external input pin
  - Requests by software trigger
- Transfer targets
  - Peripheral I/O ⇔ Peripheral I/O
  - Peripheral I/O ⇔ Internal RAM

***Figure 2-16: Block Diagram of DMA Controller***




**Remark:** n = 0 to 3

## 2.16 Key Interrupt Function

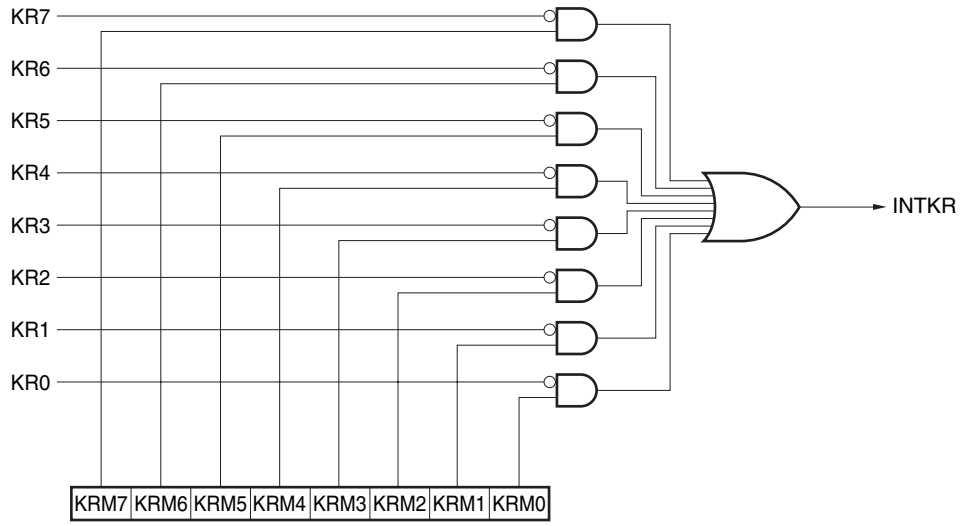
### Features

A key interrupt request signal (INTKR) can be generated by inputting a falling edge to the eight key input pins (KR0 to KR7) by setting the key return mode register (KRM).

***Table 2-5: Assignment of Key Return Detection Pins***

| Flag | Pin Description |
|---|---|
| KRM0 | Controls KR0 signal in 1-bit units |
| KRM1 | Controls KR1 signal in 1-bit units |
| KRM2 | Controls KR2 signal in 1-bit units |
| KRM3 | Controls KR3 signal in 1-bit units |
| KRM4 | Controls KR4 signal in 1-bit units |
| KRM5 | Controls KR5 signal in 1-bit units |
| KRM6 | Controls KR6 signal in 1-bit units |
| KRM7 | Controls KR7 signal in 1-bit units |

***Figure 2-17: Key Return Block Diagram***



## 2.17 Standby Function

### Overview

The power consumption of the system can be effectively reduced by using the standby modes in combination and selecting the appropriate mode for the application. The available standby modes are listed below.

***Table 2-6: Standby Modes***

| Mode | Functional Outline |
|---|---|
| HALT mode | Mode in which only the operating clock of the CPU is stopped |
| IDLE1 mode | Mode in which all the internal operations of the chip except the oscillator, PLL[a], and flash memory are stopped |
| IDLE2 mode | Mode in which all the internal operations of the chip except the oscillator are stopped |
| Software STOP mode | Mode in which all the internal operations of the chip except the subclock oscillator are stopped |
| Subclock operation mode | Mode in which the subclock is used as the internal system clock |
| Sub-IDLE mode | Mode in which all the internal operations of the chip except the oscillator, PLL[a], and flash memory are stopped, in the subclock operation mode |

a. The PLL holds the previous operating status (in clock-through mode or PLL mode).

## 2.18 Reset Function

The reset function is outlined below.

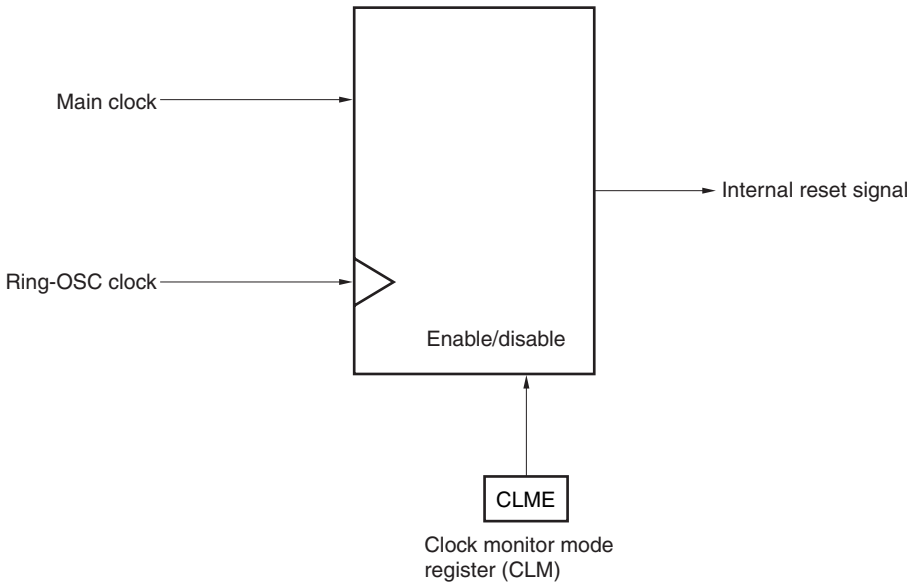
- Reset function by RESET pin input
- Reset function by overflow of watchdog timer 2 (WDT2RES)
- System reset by low voltage detector (LVI)
- System reset by clock monitor (CLM)

## 2.19 Clock Monitor

The clock monitor samples the main clock by using the on-chip Ring-OSC and generates a reset request signal when oscillation of the main clock is stopped.
Once the operation of the clock monitor has been enabled by an operation enable flag, it cannot be cleared to 0 by any means other than reset.
The clock monitor automatically stops under the following conditions.

- While oscillation stabilization time is being counted after software STOP mode is released
- When the main clock is stopped (MCK bit of the PCC register = 1 during subclock operation, or CLS bit of the PCC register = 0 during main clock operation)
- When the sampling clock is stopped (Ring-OSC)
- When the CPU operates with Ring-OSC

***Figure 2-18: CLM Block Diagram***



## 2.20 Low-voltage Detector

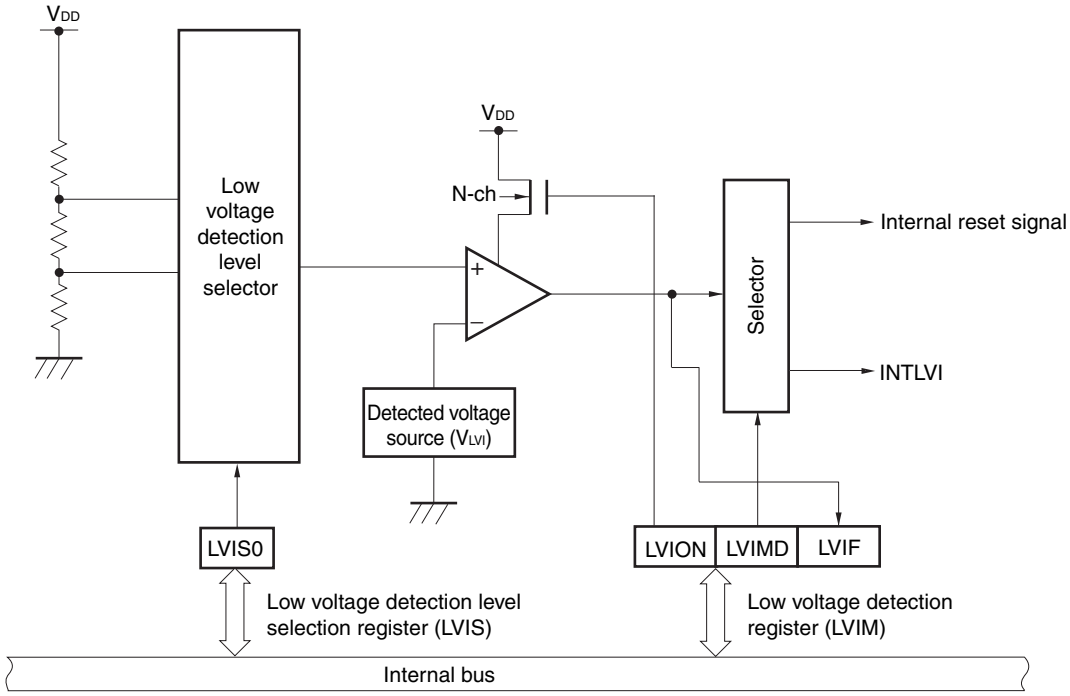
### Features

The low-voltage detector (LVI) has the following functions.

- Compares the supply voltage ($V_{DD}$) and detected voltage ($V_{LVII}$) and generates an internal interrupt signal or internal reset signal when $V_{DD} < V_{LVI}$.
- The level of the supply voltage to be detected can be changed by software (in two steps).
- Interrupt or reset signal can be selected by software.
- Can operate in STOP mode too.
- Operation can be stopped by software.

If the low-voltage detector is used to generate a reset signal, bit 0 (LVIRF) of the reset source flag register (RESF) is set to 1 when the reset signal is generated.

***Figure 2-19: Block Diagram of Low-Voltage Detector***

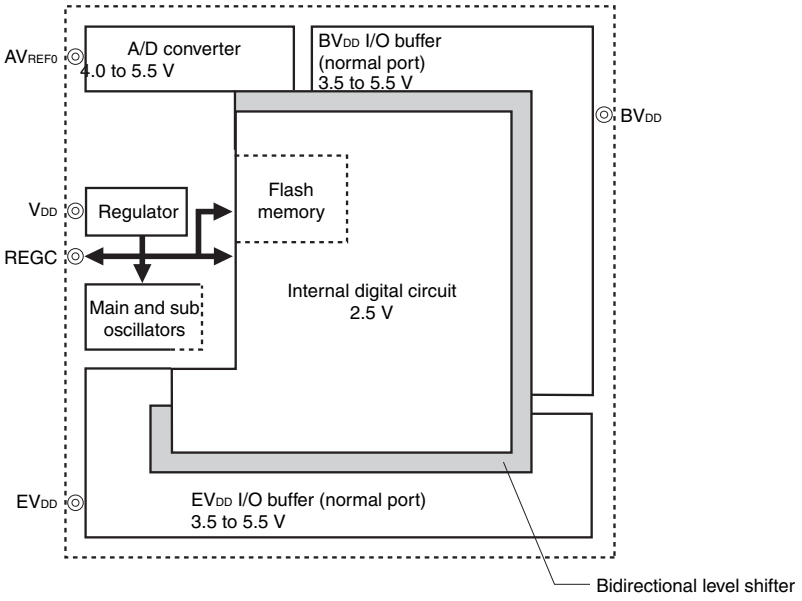


## 2.21 Voltage Regulator

### Features

This product has an on-chip regulator to lower the power consumption and noise.
This regulator supplies a voltage lower than the supply voltage $V_{DD}$ to the oscillator block and internal logic circuits (except the A/D converter and I/O buffers). The output voltage of the regulator is set to 2.5 V (±0.2 V).

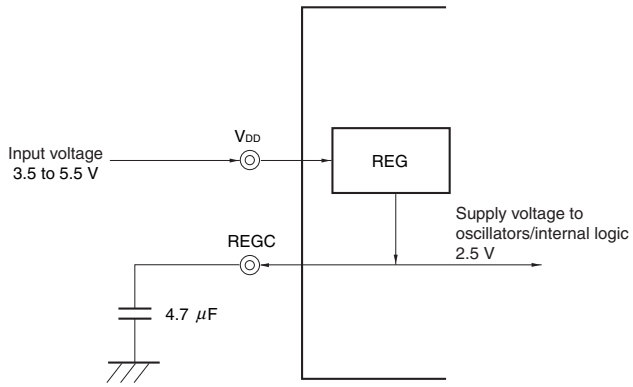
***Figure 2-20: Regulator***




The regulator of this product operates in all operation modes (normal operation, HALT, IDLE1, IDLE2, STOP, and sub-IDLE modes, and during reset).
To stabilize the output voltage of the regulator, connect a capacitor (4.7 μF**Note**) to the REGC pin.

**Note:** Connect the REGC pin as illustrated below.

***Figure 2-21: Connection of REGC Pin (REGC = Capacitance)***



## 2.22 Flash Memory

The following products are flash memory versions of the V850ES/FG2.

**Caution: There are differences in the amount of noise tolerance and noise radiation between flash memory versions and mask ROM versions. When considering changing from a flash memory version to a mask ROM version during the process from experimental manufacturing to mass production, make sure to sufficiently evaluate commercial samples (CS) (not engineering samples (ES)) of the mask ROM versions.**

**μPD70F3235 On-chip 256 KB flash memory**
When fetching an instruction, 4 bytes of the flash memory can be accessed in 1 clock in the same manner as the mask ROM versions.
The flash memory can be written mounted on the target board (on-board write), by connecting a dedicated flash programmer to the target system.
Flash memory is commonly used in the following development environments and applications.

- For altering software after solder-mounting the V850ES/FG2 on the target system
- For differentiating software in small-scale production of various models.
- For data adjustment when starting mass production

**Features**

- 4-byte/1-clock access (for instruction fetch access)
- Batch erase or block unit erase
- Communication with dedicated flash programmer via serial interface
- Erase/write voltage: Can be erased or written using a single power supply.
- On-board programming
- Flash memory programming by self writing

**Erasure unit**
The units in which the 256 KB flash memory can be erased are as follows.

**(1)Batch erasure**
The areas of flash memory xx000000H to xx03FFFFH can be erased at the same time.

**(2)Block erasure**
The flash memory can be erased in block units.
Block 0: 56 KB
Block 1: 8 KB
Block 2: 56 KB
Block 3: 8 KB
Block 4: 56 KB
Block 5: 56 KB
Block 6: 8 KB
Block 7: 8 KB
Block 8: 32 KB

## 2.23 ROM Mask Options Function

### Mask Options (Flash ROM Product)

The flash memory versions in this product series have an option data area where a block subject to mask options is specified.
When writing a program to a flash memory version, be sure to set the option data corresponding to the following option in the program at address 007AH as default data.
The data in this area cannot be rewritten during program execution.

***Table 2-7: Mask Options***

| Address | Set Value | Setting |
|---|---|---|
| 007AH | 00H | Ring-OSC:Can be stopped.<br>WDT2:Count clock can be selected.<br>Overflow signal can be selected from INTWDT2 or WDT2RES.<br>Subclock:Crystal resonator connection |
| | 01H | Ring-OSC:Cannot be stopped.<br>WDT2:Count clock can be selected.<br>Overflow signal can be selected from INTWDT2 or WDT2RES.<br>Subclock:Crystal resonator connection |
| | 02H | Ring-OSC:Can be stopped.<br>WDT2:Count clock is fixed to Ring-OSC.<br>Overflow signal is fixed to WDT2RES.<br>Subclock:Crystal resonator connection |
| | 03H | Ring-OSC:Cannot be stopped.<br>WDT2:Count clock is fixed to Ring-OSC.<br>Overflow signal is fixed to WDT2RES.<br>Subclock:Crystal resonator connection |
| | C0H | Ring-OSC:Can be stopped.<br>WDT2:Count clock can be selected.<br>Overflow signal can be selected from INTWDT2 or WDT2RES.<br>Subclock:RC oscillation connection |
| | C1H | Ring-OSC:Cannot be stopped.<br>WDT2:Count clock can be selected.<br>Overflow signal can be selected from INTWDT2 or WDT2RES.<br>Subclock:RC oscillation connection |
| | C2H | Ring-OSC:Can be stopped.<br>WDT2:Count clock is fixed to Ring-OSC.<br>Overflow signal is fixed to WDT2RES.<br>Subclock:RC oscillation connection |
| | C3H | Ring-OSC:Cannot be stopped.<br>WDT2:Count clock is fixed to Ring-OSC.<br>Overflow signal is fixed to WDT2RES.<br>Subclock:RC oscillation connection |

**Caution: Do not make any settings other than the above.**

## 2.24 On-chip Debug Unit (Flash Memory Versions only)

The V850ES/FG2 includes an on-chip debug unit. By connecting an N-Wire emulator, on-chip debugging can be executed with the V850ES/FG2 alone.

**Caution: The following debug functions are supported by the V850ES/FG2, and whether they are usable or not differs depending on the debugger. For details of the debugging function, refer to the user's manual of the debugger to be used.**

**Functional Outline**
The on-chip debug unit of the V850ES/FG2 is RCU1 (Run Control Unit 1).

**Debug interface**
Communication with the host machine is established by using the DRST, DCK, DMS, DDI, and DDO signals via an N-Wire emulator. The communication specifications of N-Wire are used for the interface.

**On-chip debug**
On-chip debugging can be executed by preparing wiring and a connector for on-chip debugging on the target system. An N-Wire emulator is used as the connector that connects the emulator.
Clear the OCDM0 bit of the OCDM register (special register) to 0 when you use on-chip debug mode.

**Forced reset function**
The V850ES/FG2 can be forcibly reset.

**Break reset function**
The CPU can be started in the debug mode immediately after reset of the CPU is released.

**Forced break function**
Execution of the user program can be forcibly aborted (however, the illegal operation code exception handler (first address: 00000060H) cannot be used).

**Hardware break function**
Two breakpoints for instruction and access can be used. The instruction breakpoint can abort program execution at any address. The access breakpoint can abort program execution by data access to any address.

**Software break function**
Up to four software breakpoints can be set in the internal ROM area. The number of software breakpoints that can be set in the RAM area differs depending on the debugger to be used.

**Debug monitor function**
A memory space for debugging that is different from the user memory space is used during debugging (background monitor mode). The user program can be executed starting from any address.
While execution of the user program is aborted, the user resources (such as memory and I/O) can be read and written, and the user program can be downloaded.

**Mask function**
Each signal can be masked.
The correspondence with the mask functions of the debugger (ID850NWC) for the N-Wire emulator (IE-V850E1-CD-NW) of NEC Electronics is shown below.

- NMI0 mask function: NMI pin
- NMI1 mask function: WDT2 interrupt
- NMI2 mask function: –
- RESET mask function: RESET pin, WDT2 reset, LVI reset, clock monitor reset

**Timer function**
The execution time of the user program can be measured.

**Peripheral macro operation/stop selection function during break**
Depending on the debugger to be used, whether the peripheral macro operates or is stopped during a break can be selected.

Functions that are always stopped during break

- Clock monitor
- Watchdog timer 2

Functions that can operate or be stopped during break (however, each function cannot be selected individually)

- A/D converter
- Timer M
- Timer P
- Timer Q
- Watch timer

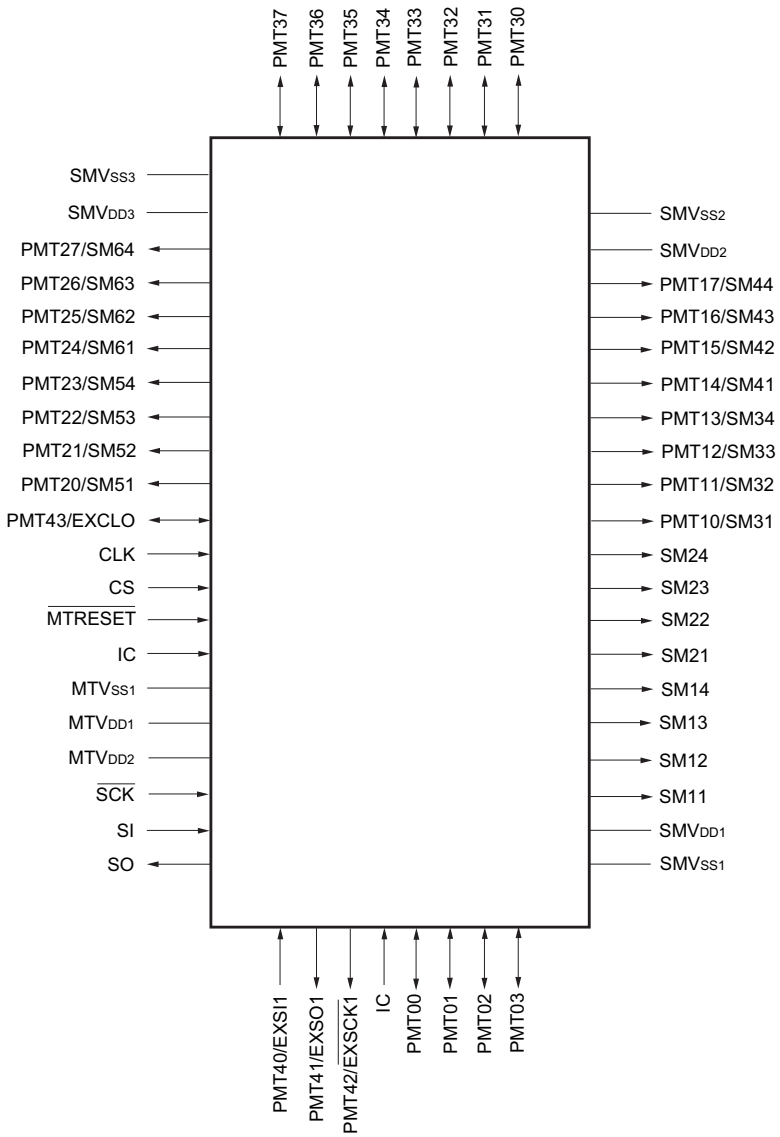
Peripheral functions that continue operating during break (functions that cannot be stopped)

- Peripheral functions other than above

# Chapter 3 Pin Function of MTRC

## 3.1 Pin Configuration (Top View)

***Figure 3-1: Pinout of MTRC***



## 3.2 List of Pin Functions

***Table 3-1: List of Pin Functions (1/2)***

| Symbol | IO | Function | Connection |
|---|---|---|---|
| PMT00 | IO | I/O Port | External |
| PMT01 | IO | I/O Port | External |
| PMT02 | IO | I/O Port | External |
| PMT03 | IO | I/O Port | External |
| SM11 | O - Hi-Z | Meter1 PWM Output Signal (sin+) | External |
| SM12 | O - Hi-Z | Meter1 PWM Output Signal (sin-) | External |
| SM13 | O - Hi-Z | Meter1 PWM Output Signal (cos+) | External |
| SM14 | O - Hi-Z | Meter1 PWM Output Signal (cos-) | External |
| SM21 | O - Hi-Z | Meter2 PWM Output Signal (sin+) | External |
| SM22 | O - Hi-Z | Meter2 PWM Output Signal (sin-) | External |
| SM23 | O - Hi-Z | Meter2 PWM Output Signal (cos+) | External |
| SM24 | O - Hi-Z | Meter2 PWM Output Signal (cos-) | External |
| PMT10/SM31 | O - Hi-Z / O | Output Port / Meter3 PWM Output Signal (sin+) | External |
| PMT11/SM32 | O - Hi-Z / O | Output Port / Meter3 PWM Output Signal (sin-) | External |
| PMT12/SM33 | O - Hi-Z / O | Output Port / Meter3 PWM Output Signal (cos+) | External |
| PMT13/SM34 | O - Hi-Z / O | Output Port / Meter3 PWM Output Signal (cos-) | External |
| PMT14/SM41 | O - Hi-Z / O | Output Port / Meter4 PWM Output Signal (sin+) | External |
| PMT15/SM42 | O - Hi-Z / O | Output Port / Meter4 PWM Output Signal (sin-) | External |
| PMT16/SM43 | O - Hi-Z / O | Output Port / Meter4 PWM Output Signal (cos+) | External |
| PMT17/SM44 | O - Hi-Z / O | Output Port / Meter4 PWM Output Signal (cos-) | External |
| PMT20/SM51 | O - Hi-Z / O | Output Port / Meter5 PWM Output Signal (sin+) | External |
| PMT21/SM52 | O - Hi-Z / O | Output Port / Meter5 PWM Output Signal (sin-) | External |
| PMT22/SM53 | O - Hi-Z / O | Output Port / Meter5 PWM Output Signal (cos+) | External |
| PMT23/SM54 | O - Hi-Z / O | Output Port / Meter5 PWM Output Signal (cos-) | External |
| PMT24/SM61 | O - Hi-Z / O | Output Port / Meter6 PWM Output Signal (sin+) | External |
| PMT25/SM62 | O - Hi-Z / O | Output Port / Meter6 PWM Output Signal (sin-) | External |
| PMT26/SM63 | O - Hi-Z / O | Output Port / Meter6 PWM Output Signal (cos+) | External |
| PMT27/SM64 | O - Hi-Z / O | Output Port / Meter6 PWM Output Signal (cos-) | External |
| PMT30 | IO | I/O Port | External |
| PMT31 | IO | I/O Port | External |
| PMT32 | IO | I/O Port | External |
| PMT33 | IO | I/O Port | External |
| PMT34**Caution** | IO | I/O Port | Internal[a] |
| PMT35**Caution** | IO | I/O Port | Internal[a] |
| PMT36**Caution** | IO | I/O Port | Internal[a] |
| PMT37**Caution** | IO | I/O Port | Internal[a] |
| PMT40/EXSI1 | IO/I | I/O Port / Expand Pin for SI | External |
| PMT41/EXSO1 | IO/O | I/O Port / Expand Pin for SO | External |

*Table 3-1: List of Pin Functions (2/2)*

| Symbol | IO | Function | Connection |
|---|---|---|---|
| PMT42/$\overline{\text{EXSCK1}}$ | IO/O | I/O Port / Expand Pin for $\overline{\text{SCK}}$ | External |
| PMT43/EXCLO | IO/O | I/O Port / Expand Pin for System Clock | External |
| SMVDD1 | | Power Supply Input Voltage for Meter1, Meter2 | External |
| SMVSS1 | | Ground Potential for Meter1, Meter2 | External |
| SMVDD2 | | Power Supply Input Voltage for Meter3, Meter4 | External |
| SMVSS2 | | Ground Potential for Meter3, Meter4 | External |
| SMVDD3 | | Power Supply Input Voltage for Meter5, Meter6 | External |
| SMVSS3 | | Ground Potential for Meter5, Meter6 | External |
| CLK | I | System Clock Input | Internal to FG2 |
| CS | I | Serial Access Enable | Internal to FG2 |
| MTCS | O | PCM0 pin of FG2 device (PCM0 has to be configured to output for internal communication) | External from FG2 |
| $\overline{\text{MTRESET}}$ | I | Reset Input | External |
| MTVSS | | Ground Potential (Digital Unit) | External |
| MTVDD | | Power Supply Input Voltage (Digital Unit) | External |
| $\overline{\text{SCK}}$ | I | Serial Clock Input | Internal to FG2 |
| SI | I | Serial Data Input | Internal to FG2 |
| SO | O | Serial Data Output | Internal to FG2 |

a. Internally connected, not available on external pins.

**Caution: Setting the port mode configuration for PMT34 to PMT37 requires special attention, refer to “Port MT3” on page 87.**

***Table 3-2: Recommended connection of unused pins (1/2)***

| Symbol | Alternate Function | I/O Circuit | Recommended connection |
|---|---|---|---|
| PMT00 | | A-1 | Input: Independently connect to $MTV_{DD}$ or $MTV_{SS}$ via a resistor<br>Output: Leave open |
| PMT01 | | | Input: Independently connect to $MTV_{DD}$ or $MTV_{SS}$ via a resistor<br>Output: Leave open |
| PMT02 | | | Input: Independently connect to $MTV_{DD}$ or $MTV_{SS}$ via a resistor<br>Output: Leave open |
| PMT03 | | | Input: Independently connect to $MTV_{DD}$ or $MTV_{SS}$ via a resistor<br>Output: Leave open |
| SM11 | | B-1 | Leave open |
| SM12 | | | Leave open |
| SM13 | | | Leave open |
| SM14 | | | Leave open |
| SM21 | | | Leave open |
| SM22 | | | Leave open |
| SM23 | | | Leave open |
| SM24 | | | Leave open |
| PMT10/SM31 | Meter3 PWM Output Signal (sin+) | B-2 | Leave open |
| PMT11/SM32 | Meter3 PWM Output Signal (sin-) | | Leave open |
| PMT12/SM33 | Meter3 PWM Output Signal (cos+) | | Leave open |
| PMT13/SM34 | Meter3 PWM Output Signal (cos-) | | Leave open |
| PMT14/SM41 | Meter4 PWM Output Signal (sin+) | | Leave open |
| PMT15/SM42 | Meter4 PWM Output Signal (sin-) | | Leave open |
| PMT16/SM43 | Meter4 PWM Output Signal (cos+) | | Leave open |
| PMT17/SM44 | Meter4 PWM Output Signal (cos-) | | Leave open |
| PMT20/SM51 | Meter5 PWM Output Signal (sin+) | | Leave open |
| PMT21/SM52 | Meter5 PWM Output Signal (sin-) | | Leave open |
| PMT22/SM53 | Meter5 PWM Output Signal (cos+) | | Leave open |
| PMT23/SM54 | Meter5 PWM Output Signal (cos-) | | Leave open |
| PMT24/SM61 | Meter6 PWM Output Signal (sin+) | | Leave open |
| PMT25/SM62 | Meter6 PWM Output Signal (sin-) | | Leave open |
| PMT26/SM63 | Meter6 PWM Output Signal (cos+) | | Leave open |
| PMT27/SM64 | Meter6 PWM Output Signal (cos-) | | Leave open |

***Table 3-2: Recommended connection of unused pins (2/2)***

| Symbol | Alternate Function | I/O Circuit | Recommended connection |
|---|---|---|---|
| PMT30 | | A-1 | Input: Independently connect to $MTV_{DD}$ or $MTV_{SS}$ via a resistor<br>Output: Leave open |
| PMT31 | | | Input: Independently connect to $MTV_{DD}$ or $MTV_{SS}$ via a resistor<br>Output: Leave open |
| PMT32 | | | Input: Independently connect to $MTV_{DD}$ or $MTV_{SS}$ via a resistor<br>Output: Leave open |
| PMT33 | | | Input: Independently connect to $MTV_{DD}$ or $MTV_{SS}$ via a resistor<br>Output: Leave open |
| PMT40/EXSI1 | Expand Pin for SI | D-2 | Input: Independently connect to $MTV_{DD}$ or $MTV_{SS}$ via a resistor<br>Output: Leave open |
| PMT41/EXSO1 | Expand Pin for SO | D-1 | Input: Independently connect to $MTV_{DD}$ or $MTV_{SS}$ via a resistor<br>Output: Leave open |
| $\overline{\text{PMT42/EXSCK1}}$ | $\overline{\text{Expand Pin for SCK}}$ | D-3 | Input: Independently connect to $MTV_{DD}$ or $MTV_{SS}$ via a resistor<br>Output: Leave open |
| PMT43/EXCLO | Expand Pin for System Clock | D-4 | Input: Independently connect to $MTV_{DD}$ or $MTV_{SS}$ via a resistor<br>Output: Leave open |
| SMVDD1 | | - | |
| SMVSS1 | | - | |
| SMVDD2 | | - | |
| SMVSS2 | | - | |
| SMVDD3 | | - | |
| SMVSS3 | | - | |
| $\overline{\text{CLK}}$ | | CLK[a] | internal connected |
| MTCS | | MTCS[a] | internal connected |
| $\overline{\text{MTRESET}}$ | | - | |
| $MTV_{SS}$ | | - | |
| $MTV_{DD}$ | | - | |
| $\overline{\text{SCK}}$ | | SCK[a] | internal connected |
| SI | | SI[a] | internal connected |
| SO | | SO | internal connected |
| IC1, IC2 | | - | Input: connect to $MTV_{SS}$ directly |

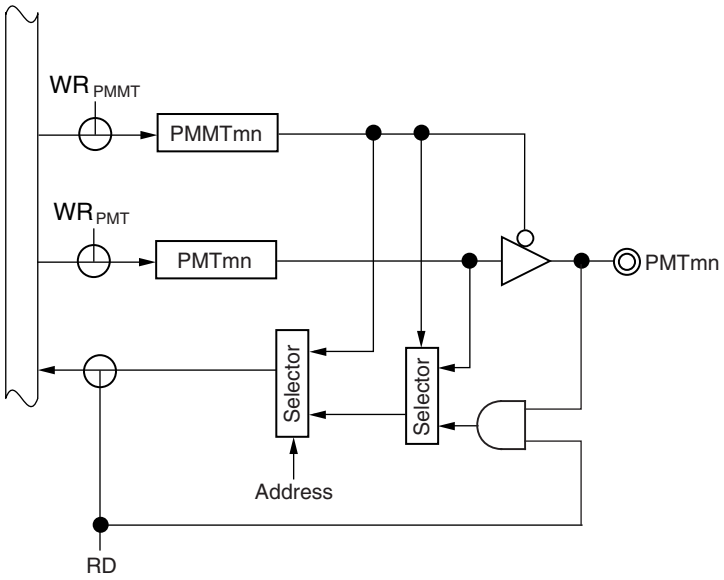
a. Some input pins of the MTRC have pull down/pull up resistors to avoid noise effects that could cause malfunction during the initialization of the FG2 device.
After $\overline{\text{MTRESET}}$ release, these resistors are active. The resistors will be deactivated after the first rising edge of the MTCS signal. They will be reactivated if $\overline{\text{MTRESET}}$ = 0.
Therefore these resistors consume some current when they are activated.

## 3.3 Pin I/O Circuits

Each type of port block diagram is as follows. Then, the type of each port is shown in each chapter.

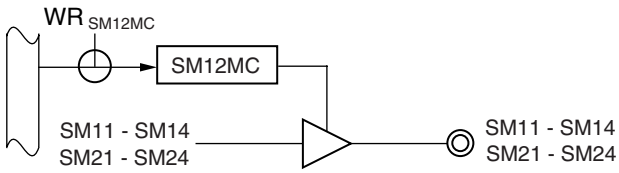
### 3.3.1 Type A-1

***Figure 3-2: Type A-1***



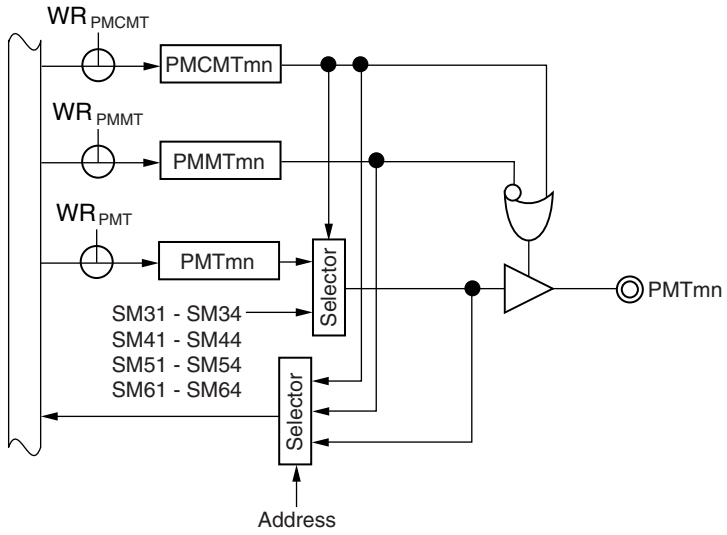

### 3.3.2 Type B-1

***Figure 3-3: Type B-1***



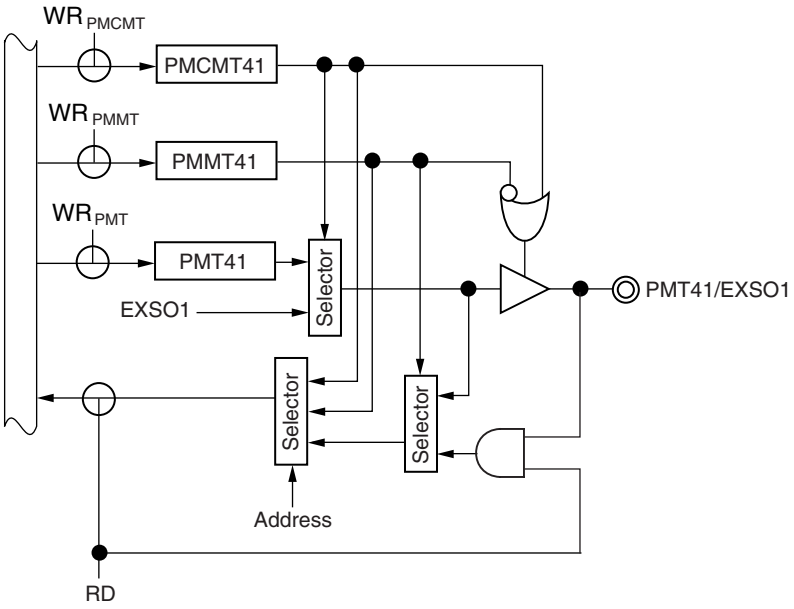
### 3.3.3 Type B-2

***Figure 3-4: Type B-2***



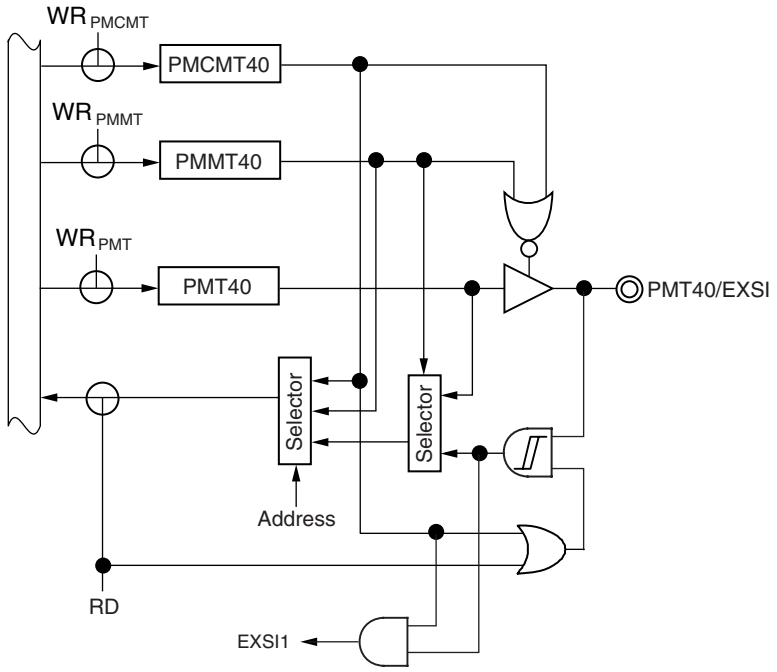

### 3.3.4 Type D-1

***Figure 3-5: Type D-1***



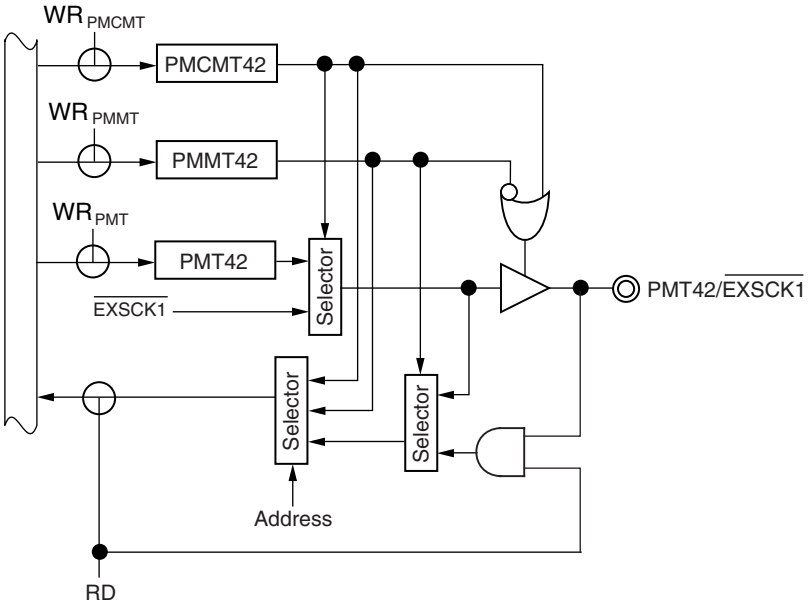
### 3.3.5 Type D-2

***Figure 3-6: Type D-2***



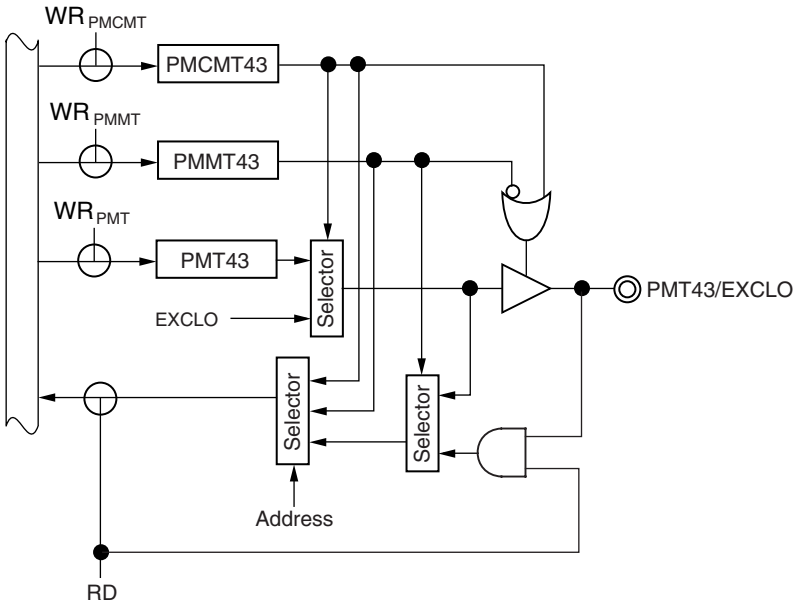

### 3.3.6 Type D-3

***Figure 3-7: Type D-3***



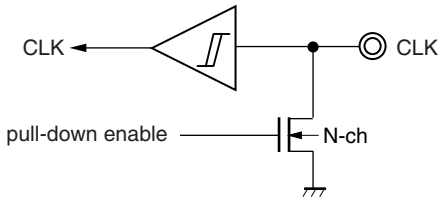
### 3.3.7 Type D-4

***Figure 3-8: Type D-4***



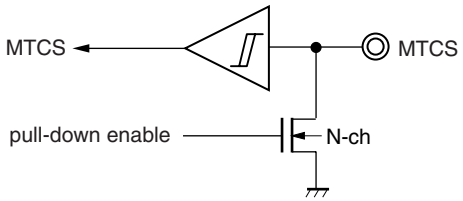

### 3.3.8 Type CLK

***Figure 3-9: Type CLK***



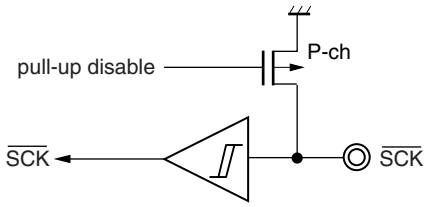

### 3.3.9 Type MTCS

***Figure 3-10: Type MTCS***



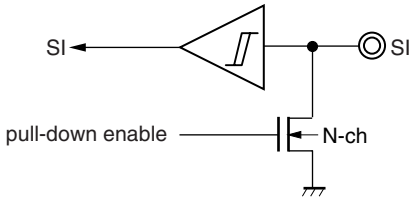
### 3.3.10 Type $\overline{\text{SCK}}$

*Figure 3-11: Type $\overline{\text{SCK}}$*



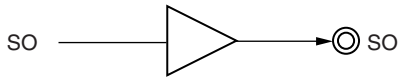

### 3.3.11 Type SI

*Figure 3-12: Type SI*




### 3.3.12 Type SO

*Figure 3-13: Type SO*



# Chapter 4 Port Functions

## 4.1 Setting Alternate Pin Functions

Set “1” to the PMCmn bit of PMCm register to set the pin to the alternate pin function.
Refer to the following table for setting the alternate pin function for every port pin.
Not any port provides alternate pin function and therefore this registers has no PMCMTmn register.
Please refer to the peripheral function chapter to get more details.

**Remark:** m = 1, 2, 4
n = 0 to 7

***Table 4-1: Alternate Pin Functions (1/2)***

| Port name | Alternate pin name | Setting value when selecting alternate function | | | |
|---|---|---|---|---|---|
| | | PMTmn | PMMTmn | PMCMTmn | Remark |
| PMT00 | – | 0/1 | 1 | - | |
| PMT01 | | | | | |
| PMT02 | | | | | |
| PMT03 | | | | | |
| PMT10 | SM31 | 0/1 | 0/1 | 1 | |
| PMT11 | SM32 | | | | |
| PMT12 | SM33 | | | | |
| PMT13 | SM34 | | | | |
| PMT14 | SM41 | | | | |
| PMT15 | SM42 | | | | |
| PMT16 | SM43 | | | | |
| PMT17 | SM44 | | | | |
| PMT20 | SM51 | 0/1 | 0/1 | 1 | |
| PMT21 | SM52 | | | | |
| PMT22 | SM53 | | | | |
| PMT23 | SM54 | | | | |
| PMT24 | SM61 | | | | |
| PMT25 | SM62 | | | | |
| PMT26 | SM63 | | | | |
| PMT27 | SM64 | | | | |
| PMT30 | – | 0/1 | 1 | - | |
| PMT31 | | | | | |
| PMT32 | | | | | |
| PMT33 | | | | | |
| PMT34 | **Caution** | | | | |
| PMT35 | | | | | |
| PMT36 | | | | | |
| PMT37 | | | | | |

*Table 4-1: Alternate Pin Functions (2/2)*

| Port name | Alternate pin name | Setting value when selecting alternate function | | | |
|---|---|---|---|---|---|
| | | PMTmn | PMMTmn | PMCMTmn | Remark |
| PMT40 | EXSI1 | 0/1 | 0/1 | 1 | Connect to SO only if MTCS = 0[a] |
| PMT41 | EXSO1 | | | | Connect to SI only if MTCS = 0 |
| PMT42 | $\overline{\text{EXSCK1}}$ | | | | Connect to $\overline{\text{SCK}}$ only if MTCS = 0 |
| PMT43 | EXCLO | | | | Connect to CLK only if MTCS = 0 |

a. The MTCS signal is identical to the V850ES/Fx2's PCM0 signal, which connects the EXCSIB1 interface to the V850ES/Fx2 CSIB1, when PCM0 = MTCS = 0.
Note that changing the internal connection of the EXCSIB1 interface pins upon a change of PCM0/MTCS may be delayed due to an ongoing CSIB1 data transfer.

**Caution: Setting the port mode configuration for PMT34 to PMT37 requires special attention, refer to "Port MT3" on page 87.**

## 4.2 Port MT0

### 4.2.1 Port MT0 functions

- 4-bit I/O Port
- Port I/O data specified in 1-bit units

***Table 4-2: Port MT0 Functions***

| Port Mode | Alternate Function | TYPE | Register | | |
|---|---|---|---|---|---|
| | | | PORT | PM | PMC |
| PMT00 | - | A-1 | × | × | - |
| PMT01 | - | A-1 | × | × | - |
| PMT02 | - | A-1 | × | × | - |
| PMT03 | - | A-1 | × | × | - |

**Remarks: 1.** PORT: Port
PM: Port mode register
PMC: Port mode control register

**2.** ×: available
-: not available

### 4.2.2 Register

**(1) Port Register 0 (PMT0)**

MTRC Port register 0 (MT0) is an 8-bit register that controls pin level read, output level write.

It can be read and written in 8-bit unit.

***Figure 4-1: Port Register 0 (PMT0) Format***

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| PMT0 | 0 | 0 | 0 | 0 | PMT03 | PMT02 | PMT01 | PMT00 | 0x20 | undefined |
| R/W | R | R | R | R | R/W | R/W | R/W | R/W | | |

| PMT0n | Output data control (n= 0 - 3) |
|---|---|
| 0 | Output 0 |
| 1 | Output 1 |

**(2) Port MT0 Mode Register 0 (PMMT0)**

This is an 8-bit register used to specify the input mode/output mode.

It can be read and written in 8-bit unit.

***Figure 4-2: Port MT0 Mode Register 0 (PMMT0) Format***

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| PMMT0 | 1 | 1 | 1 | 1 | PMMT03 | PMMT02 | PMMT01 | PMMT00 | 0x25 | 0xFF |
| R/W | R | R | R | R | R/W | R/W | R/W | R/W | | |

| PMMT0n | I/O mode control (n= 0 - 3) |
|---|---|
| 0 | Output mode |
| 1 | Input mode |

## 4.3 Port MT1

### 4.3.1 Port MT1 functions

- 8-bit output port
- Port I/O specified in 1-bit units (PMMT1 register)
- Port mode/control mode (alternate function) specified in 1-bit units (PMCMT1 register)

***Table 4-3: Port MT1 Functions***

| Port Mode | Alternate Function | TYPE | Register | | |
|---|---|---|---|---|---|
| | | | PORT | PM | PMC |
| PMT10 | SM31 | B-2 | × | × | × |
| PMT11 | SM32 | B-2 | × | × | × |
| PMT12 | SM33 | B-2 | × | × | × |
| PMT13 | SM34 | B-2 | × | × | × |
| PMT14 | SM41 | B-2 | × | × | × |
| PMT15 | SM42 | B-2 | × | × | × |
| PMT16 | SM43 | B-2 | × | × | × |
| PMT17 | SM44 | B-2 | × | × | × |

**Remarks: 1.** PORT: Port
PM: Port mode register
PMC: Port mode control register

**2.** ×: available
-: not available

### 4.3.2 Registers

**(1) Port Register 1 (PMT1)**

MTRC Port register 1 (MT1) is an 8-bit register that controls pin level read, output level write.

It can be read and written in 8-bit unit.

***Figure 4-3: Port Register 1 (PMT1) Format***

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| PMT1 | PMT17 | PMT16 | PMT15 | PMT14 | PMT13 | PMT12 | PMT11 | PMT10 | 0x21 | undefined |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

| PMT1n | Output data control (n= 0 - 7) |
|---|---|
| 0 | Output 0 |
| 1 | Output 1 |

**(2) Port Mode Register 1 (PMMT1)**

It can be read and written in 8-bit unit.

***Figure 4-4: Port Mode Register 1 (PMMT1) Format***

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| PMMT1 | PMMT17 | PMMT16 | PMMT15 | PMMT14 | PMMT13 | PMMT12 | PMMT11 | PMMT10 | 0x26 | 0xFF |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

| PMMT1n | I/O mode control (n= 0 - 7) |
|---|---|
| 0 | Output mode |
| 1 | Input mode |

**(3) Port Mode Control Register (PMCMT1)**

It can be read and written in 8-bit unit.

***Figure 4-5: Port Mode Control Register 1 (PMCMT1) Format***

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| PMCMT1 | PMCMT17 | PMCMT16 | PMCMT15 | PMCMT14 | PMCMT13 | PMCMT12 | PMCMT11 | PMCMT10 | 0x2A | 0x00 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

| PMCMT1n | PMMT1n | PMCMTn mode control (n = 0 - 7) |
|---|---|---|
| 0 | 0 | Output port |
| 0 | 1 | Hi-Z output |
| 1 | x | SM44 output (n = 7)<br>SM43 output (n = 6)<br>SM42 output (n = 5)<br>SM41 output (n = 4)<br>SM34 output (n = 3)<br>SM33 output (n = 2)<br>SM32 output (n = 1)<br>SM31 output (n = 0) |

## 4.4 Port SM1/SM2

### 4.4.1 Port SM1/SM2 functions

- 8-bit output port
- Port mode/control mode (Hi-Z output as alternate function) specified in 1-bit units (SM12MC register)

***Table 4-4: Port MT2 Functions***

| Port Mode | Alternate Function | TYPE | Register | | |
|---|---|---|---|---|---|
| | | | PORT | PM | PMC |
| Hi-Z | SM11 | B-1 | - | - | × |
| Hi-Z | SM12 | B-1 | - | - | × |
| Hi-Z | SM13 | B-1 | - | - | × |
| Hi-Z | SM14 | B-1 | - | - | × |
| Hi-Z | SM21 | B-1 | - | - | × |
| Hi-Z | SM22 | B-1 | - | - | × |
| Hi-Z | SM23 | B-1 | - | - | × |
| Hi-Z | SM24 | B-1 | - | - | × |

**Remarks: 1.** PORT: Port
PM: Port mode register
PMC: Port mode control register

**2.** ×: available
-: not available

**(1) SM1SM2 Mode Control Register (SM12MC)**

It can be read and written in 8-bit unit.

***Figure 4-6: SM1SM2 Mode Control Register (SM12MC) Format***

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| SM12MC | SM24HZC | SM23HZC | SM22HZC | SM21HZC | SM14HZC | SM13HZC | SM12HZC | SM11HZC | 0x2D | 0x00 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

| SMmnHZC | Output data control (m = 1, 2 and n = 1 - 4) |
|---|---|
| 0 | Hi-Z output |
| 1 | SMmn output |

## 4.5 Port MT2

### 4.5.1 Port MT2 functions

- 8-bit output port
- Port mode/control mode (alternate function) specified in 1-bit units (PMCMT2 register)
- Hi-Z output controllable in 1-bit units (PMMT2, PMCMT2 register)

***Table 4-5: Port MT2 Functions***

| Port Mode | Alternate Function | TYPE | Register | | |
|---|---|---|---|---|---|
| | | | PORT | PM | PMC |
| PMT20 | SM51 | B-2 | × | × | × |
| PMT21 | SM52 | B-2 | × | × | × |
| PMT22 | SM53 | B-2 | × | × | × |
| PMT23 | SM54 | B-2 | × | × | × |
| PMT24 | SM61 | B-2 | × | × | × |
| PMT25 | SM62 | B-2 | × | × | × |
| PMT26 | SM63 | B-2 | × | × | × |
| PMT27 | SM64 | B-2 | × | × | × |

**Remarks: 1.** PORT: Port
PM: Port mode register
PMC: Port mode control register

**2.** ×: available
-: not available

### 4.5.2 Registers

**(1) Port Register 2 (PMT2)**

MTRC Port register 2 (MT2) is an 8-bit register that controls pin level read, output level write.

It can be read and written in 8-bit unit.

***Figure 4-7: Port Register 2 (PMT2) Format***

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| PMT2 | PMT27 | PMT26 | PMT25 | PMT24 | PMT23 | PMT22 | PMT21 | PMT20 | 0x22 | undefined |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

| PMT2n | Output data control (n= 0 - 7) |
|---|---|
| 0 | Output 0 |
| 1 | Output 1 |

**(2) Port Mode Register 2 (PMMT2)**

It can be read and written in 8-bit unit.

***Figure 4-8: Port Mode Register 2 (PMMT2) Format***

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| PMMT2 | PMMT27 | PMMT26 | PMMT25 | PMMT24 | PMMT23 | PMMT22 | PMMT21 | PMMT20 | 0x27 | 0xFF |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

| PMMT2n | I/O mode control (n= 0 - 7) |
|---|---|
| 0 | Output mode |
| 1 | Input mode |

**(3) Port Mode Control Register 2 (PMCMT2)**

It can be read and written in 8-bit unit.

***Figure 4-9: Port Mode Control Register 2 (PMCMT2) Format***

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| PMCMT2 | PMCMT27 | PMCMT26 | PMCMT25 | PMCMT24 | PMCMT23 | PMCMT22 | PMCMT21 | PMCMT20 | 0x2B | 0x00 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

| PMCMT2n | PMMT2n | PMCMTn mode control (n = 0 - 7) |
|---|---|---|
| 0 | 0 | Output port |
| 0 | 1 | Hi-Z output |
| 1 | x | SM64 output (n = 7)<br>SM63 output (n = 6)<br>SM62 output (n = 5)<br>SM61 output (n = 4)<br>SM54 output (n = 3)<br>SM53 output (n = 2)<br>SM52 output (n = 1)<br>SM51 output (n = 0) |

## 4.6 Port MT3

### 4.6.1 Port MT3 functions

- 8-bit I/O port
- Port I/O specified in 1-bit units

***Table 4-6: Port MT3 Functions***

| Port Mode | Alternate Function | TYPE | Register | | |
|---|---|---|---|---|---|
| | | | PORT | PM | PMC |
| PMT30 | - | A-1 | × | × | - |
| PMT31 | - | A-1 | × | × | - |
| PMT32 | - | A-1 | × | × | - |
| PMT33 | - | A-1 | × | × | - |
| PMT34[Caution] | - | A-1 | × | × | - |
| PMT35[Caution] | - | A-1 | × | × | - |
| PMT36[Caution] | - | A-1 | × | × | - |
| PMT37[Caution] | - | A-1 | × | × | - |

**Caution: The ports PMT34 to PMT37 are connected internally to MTVSS.**
**The port configuration for PMT3n (n = 4 to 7) must be set as follows and must not be changed afterwards:**

- **PMMT3n = 1: port input mode (default after reset)**
- **PMT3n = 0: port output = 0**

**Remarks: 1.** PORT: Port
PM: Port mode register
PMC: Port mode control register

**2.** ×: available
-: not available

### 4.6.2 Registers

**(1) Port Register 3 (PMT3)**

MTRC Port register 3 (MT3) is an 8-bit register that controls pin level read, output level write.

It can be read and written in 8-bit unit.

***Figure 4-10: Port Register 3 (PMT3) Format***

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| PMT3 | PMT37 | PMT36 | PMT35 | PMT34 | PMT33 | PMT32 | PMT31 | PMT30 | 0x23 | undefined |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

| PMT3n[Caution] | Output data control (n= 0 - 7) |
|---|---|
| 0 | Output 0 |
| 1 | Output 1 |

**Caution: Set PMT3n = 0 for n = 4 to 7 .**

**(2) Port Mode Control Register 3 (PMMT3)**

It can be read and written in 8-bit unit.

***Figure 4-11: Port Mode Control Register 3 (PMMT3) Format***

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| PMMT3 | PMMT37 | PMMT36 | PMMT35 | PMMT34 | PMMT33 | PMMT32 | PMMT31 | PMMT30 | 0x28 | 0xFF |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

| PMMT3n[Caution] | I/O mode control (n= 0 - 7) |
|---|---|
| 0 | Output mode |
| 1 | Input mode |

**Caution: Set PMMT3n = 1 for n = 4 to 7 .**

## 4.7 Port MT4

### 4.7.1 Port MT4 functions

- 4-bit I/O port
- Port I/O specified in 1-bit units (PMMT4 register)
- Port mode/control mode (alternate function) specified in 1-bit units (PMCMT4 register)

***Table 4-7: Port MT4 Functions***

| Port Mode | Alternate Function | TYPE | Register | | |
|---|---|---|---|---|---|
| | | | PORT | PM | PMC |
| PMT40 | EXSI1 | D-2 | × | × | × |
| PMT41 | EXSO1 | D-1 | × | × | × |
| PMT42 | $\overline{\text{EXSCK1}}$ | D-3 | × | × | × |
| PMT43 | EXCLO | D-4 | × | × | × |

**Remarks: 1.** PORT: Port
PM: Port mode register
PMC: Port mode control register

**2.** ×: available
-: not available

### 4.7.2 Registers

**(1) Port Register 4 (PMT4)**

MTRC Port register 4 (MT4) is an 8-bit register that controls pin level read, output level write.

It can be read and written in 8-bit unit.

***Figure 4-12: Port Register 4 (PMT4) Format***

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| PMT4 | 0 | 0 | 0 | 0 | PMT43 | PMT42 | PMT41 | PMT40 | 0x24 | undefined |
| R/W | R | R | R | R | R/W | R/W | R/W | R/W | | |

| PMT4n | Output data control (n= 0 - 3) |
|---|---|
| 0 | Output 0 |
| 1 | Output 1 |

**(2) Port Mode Register 4 (PMMT4)**

It can be read and written in 8-bit unit.

***Figure 4-13: Port Mode Register 4 (PMMT4) Format***

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| PMMT4 | 1 | 1 | 1 | 1 | PMMT43 | PMMT42 | PMMT41 | PMMT40 | 0x29 | 0xFF |
| R/W | R | R | R | R | R/W | R/W | R/W | R/W | | |

| PMMT4n | Output data control (n= 0 - 3) |
|---|---|
| 0 | Output mode |
| 1 | Input mode |

**(3) Port Mode Control Register 4 (PMCMT4)**

It can be read and written in 8-bit unit.

***Figure 4-14: Port Mode Control Register 4 (PMCMT4) Format***

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| PMCMT4 | 0 | 0 | 0 | 0 | PMCMT43 | PMCMT42 | PMCMT41 | PMCMT40 | 0x2C | 0x00 |
| R/W | R | R | R | R | R/W | R/W | R/W | R/W | | |

| PMCMT43 | PMCMT43 mode control |
|---|---|
| 0 | I/O port |
| 1 | EXCLO output |

| PMCMT42 | PMCMT42 mode control |
|---|---|
| 0 | I/O port |
| 1 | $\overline{\text{EXSCK1}}$ output **Note** |

| PMCMT41 | PMCMT41 mode control |
|---|---|
| 0 | I/O port |
| 1 | EXSO1 output **Note** |

| PMCMT40 | PMCMT40 mode control |
|---|---|
| 0 | I/O port |
| 1 | EXSI1 Input **Note** |

**Note:** The alternate function is only available if MTCS = “0”.
When MTCS = “1”, each I/O status is as follows.

| Pin name | Status |
|---|---|
| EXSCK1 | “H” level output |
| EXSO1 | “L” level output |
| EXSI1 | Input disabled |

# Chapter 5 Clock Generator

## 5.1 Ring Oscillator

To support a high frequency clock source for the MTRC an internal high speed Ring Oscillator is implemented in the MTRC. This Ring Oscillator is controlled with SFRs to realize stop, restart and calibration.

After the release of the $\overline{\text{MTRESET}}$ pin the Ring Oscillator is stopped. It will be automatically started if the MTCS signal will be set from “0” to “1”.

**Remark:** For mass production tests the MTRC can be clocked alternatively direct from the FG2 device via the CLKOUT pin. This pin is internally connected with the CLK pin of the MTRC. Due to EME reason this mode is not useful for real applications.

### 5.1.1 Autocalibration function

At the first start of the ring oscillator it is uncalibrated and therefore significant deviations from its basic frequency (8 MHz) could be possible.
The Ring Oscillator Unit supplies an autocalibration function. With 5 specified calibration pulses at the CS pin of the MTRC (therefore PCM0/WAIT pin at the FG2) direct after MTRES release, the Ring Oscillator self-calibration unit adjusts the frequency iteratively.
The calculated calibration factor is stored in the MRCAL register. This register controls the calibration unit of the Ring Oscillator to set its frequency to 8 MHz.

### 5.1.2 Ring Oscillator states

With the Ring Oscillator 3 different states have to be separated:

- Calibration Mode
- Start-up after $\overline{\text{MTRESET}}$
- Start-up after Standby Mode release

At each state different actions are necessary to handle the Ring Oscillator. The basic separation depends on the handling of the MRCAL register.

## 5.2 Ring Oscillator Control Registers

### 5.2.1 RingOSC Control Register (MRCTL)

The MRCTL register is an 8-bit register that controls the RingOSC operation.
This register can be read or written in 8-bit units. However, bits 1 (MRCALSF) and 0 (MRCALERR) are read-only.

**Cautions: 1. After system reset has been released, the MRCALEN bit can be written only one time.**

**2. When the MRON bit = 0, the MRCLKSEL bit can't be written.**

***Figure 5-1: RingOSC Control Register (MRCTL) Format (1/2)***

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| MRCTL | MRON | MRCLKSEL | 0 | MRCALEN | 0 | 0 | MRCALSF | MRCALERR | 0x2E | 0x50 |
| After Reset | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | | |
| R/W | R/W | R/W | R | R/W | R | R | R | R | | |

| MRON | Operation / Stop of RingOSC and MRNGCTL operation control |
|---|---|
| 0 | Ring Oscillator stopped |
| 1 | Ring Oscillator enabled |

This bit will be set when MRCLKSEL = 1 and a rising edge at MTCSP pin occurs.

**Cautions: 1. After MTRESET and MTCS = "1" the MRON bit is changed from "0" to "1" by hardware.**

**2. To save power consumption the Ring Oscillator can be stopped by clearing the MRON bit to "0". After that, the MTRC has to be woken up via the PCM0/CS signal. The MRCAL register has to be updated, too.**

| MRCLKSEL | System clock selection for meter |
|---|---|
| 0 | CLK as input for clock supply by FG2 |
| 1 | internal Ring Oscillator as clock source |

**Caution: If MRON bit = "0" (Ring Oscillator stopped for power saving) no MTRC register access is possible. Therefor the MRON bit can't be set to "1" (Ring Oscillator as clock source)**

*Figure 5-1: RingOSC Control Register for the Meter (MRCTL) Format (2/2)*

| MRCALEN | Ring Oscillator frequency calibration operation control |
|---|---|
| 0 | Calibration disabled |
| 1 | Calibration enabled |

**Caution: After the $\overline{\text{MTRESET}}$ pin has been released, the MRCALEN bit can be written only one time.**

| MRCALSF | RingOSC frequency calibration operation status flag |
|---|---|
| 0 | Ring Oscillator calibration procedure is not active |
| 1 | during the Ring Oscillator calibration procedure |

The MRCALSF bit will be set to “1” when the MRON bit = 1(ring oscillator activated) and the MRCALEN bit = “1” (MTRC is set to calibration mode)
The MRCALSF bit will be reset to “0” by the following condition:

- when MRON bit = “0” (ring oscillator deactivated)
- when calibration procedure was finished successful
- when calibration error occurred with MRCALEN bit = “1”
- when MRCALEN bit = “0” (calibration register MRCAL has to be rewritten manually without automatic calibration procedure)

| MRCALERR | RingOSC frequency calibration error flag |
|---|---|
| 0 | No calibration error |
| 1 | Calibration error |

The MRCALERR bit is set to “1”, when the ring oscillator calibration is not normally executed. This will happen, when the pulse width of the calibration pulse at the MTCS pin hasn’t got the specified high and low pulse width, or the calibration temperature is not in the specified range.

When the MRON bit is set to “0” (ring oscillator stopped) the MRCALLERR bit will be reset to “0“.

### 5.2.2 RingOSC Calibration Register (MRCAL)

The MRCAL register is a 5-bit register for the RingOSC calibration operation.
This register can be read or written in 8-bit units.

This register can be set in a range of 0x01to 0x1F. The frequency of RingOSC will be increased by the MRCAL register value.

If the MRON bit = “0” and the MRCALEN bit = “1” (MRCTL register) the MRCAL register will be set to 0x10, which is the middle of its value range.

This register can be written only once:

- after $\overline{\text{MTRESET}}$ pin release:
  After setting MRON bit = 1 (done by hardware if MTCS bit = 1) and MRCALEN bit = 0 (written manually)

- after standby mode release:
  After setting MRON bit from 0 to 1 while MRCALEN bit = 0

***Figure 5-2: RingOSC Calibration Register (MRCAL) Format***

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| MRCAL | 0 | 0 | 0 | MRCAL4 | MRCAL3 | MRCAL2 | MRCAL1 | MRCAL0 | 0xXX | 0x50 |
| After Reset | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | | |
| R/W | R | R | R | R/W | R/W | R/W | R/W | R/W | | |

**Caution: When the MRON bit is set to 1 after a power save mode (MRON bit was “0”) this register has to be rewritten with the formerly stored calibration value (e.g. external EEPROM) that has followed from the frequency calibration at the specified temperature and voltage.**

## 5.3 Calibration Procedure

To calibrate the Ring Oscillator 5 specified calibration pulses of the same length at the PCM0 pin of the FG2 are necessary. To guarantee the maximum deviation of the calibrated Ring Oscillator this calibration has to be performed at the specified temperature and with the specified voltage.

After the autocalibration of the ring oscillator the calibration correction value is stored in the MRCAL register. This value has to be read out and stored in a nonvolatile memory (e.g. external EEPROM) if the ring oscillator has to be stopped for power save mode and woken up again after power save mode. This is due to the fact, that the data retention of the MRCAL register can’t be guaranteed during the time of the stopped ring oscillator.

Please see the following procedure for the autocalibration function.

***Figure 5-3: Flowchart for Frequency Calibration***

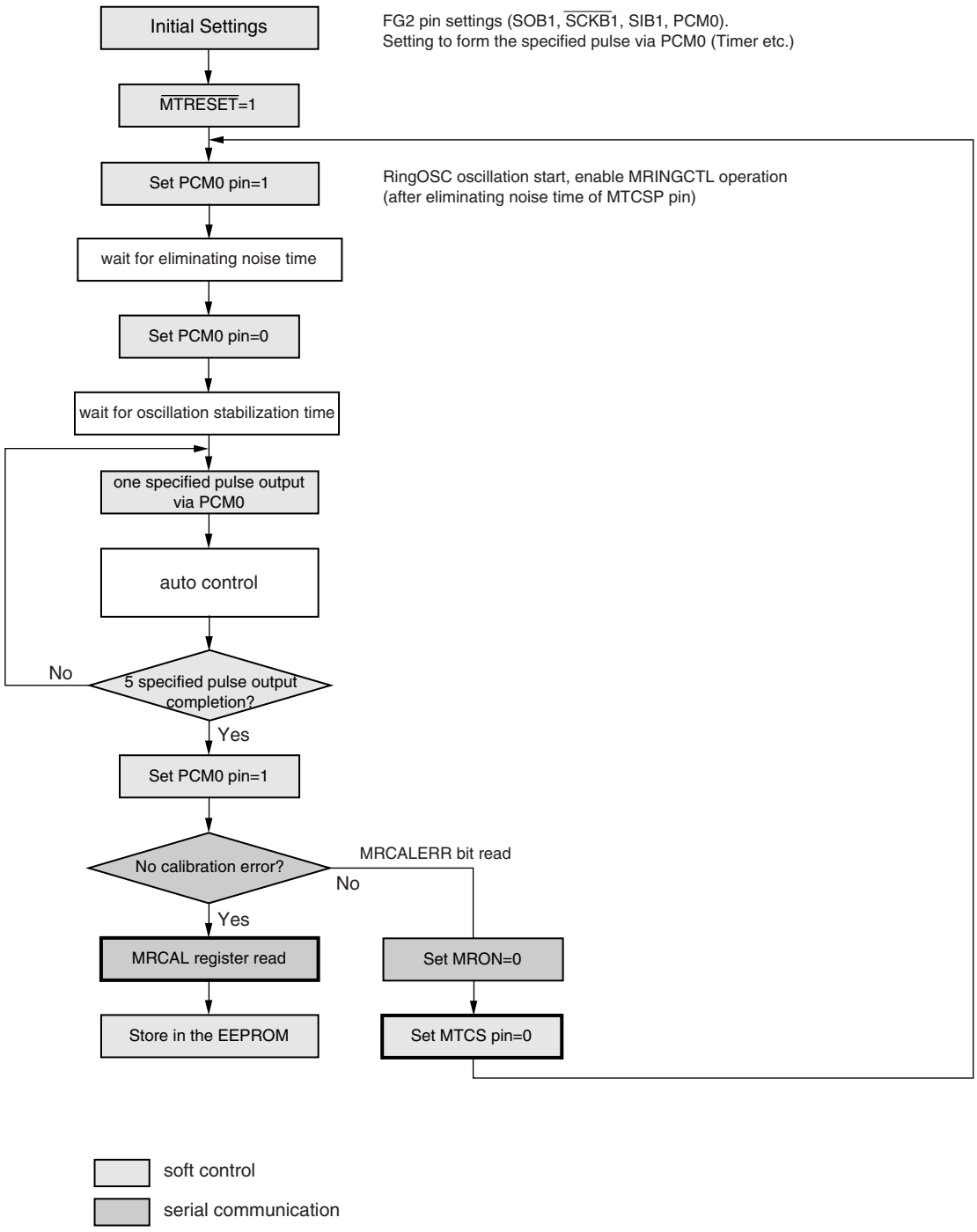
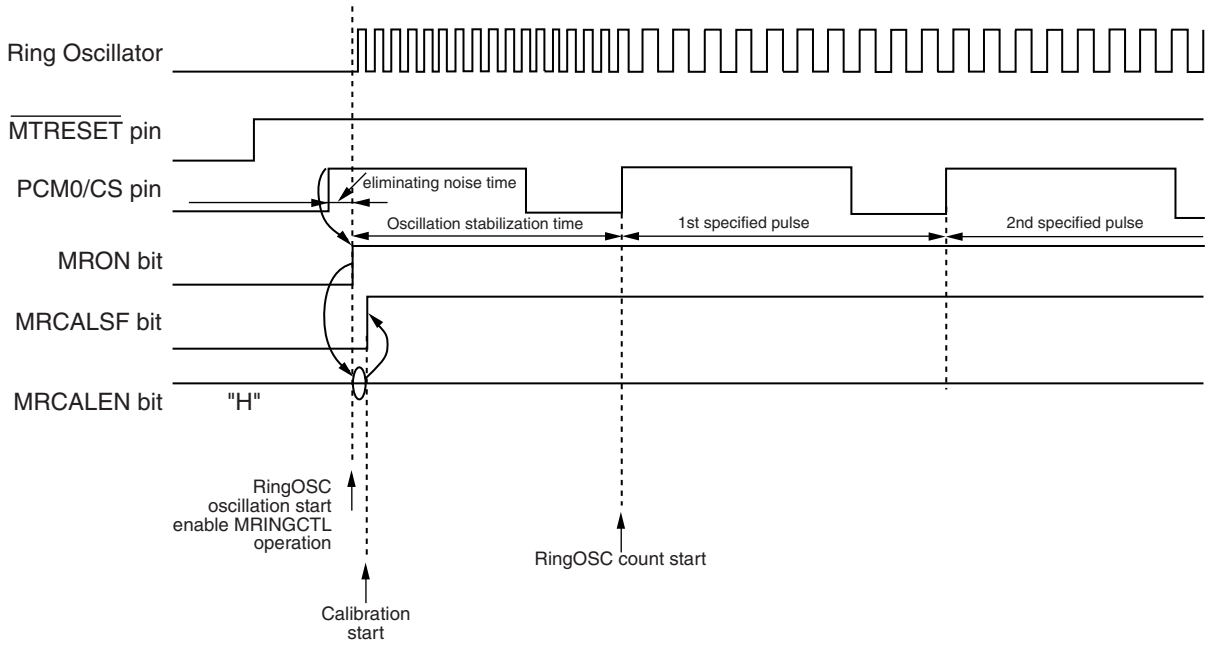


***Figure 5-4: Timing Diagram for Frequency Calibration***



## 5.4 MTRESET Release of the MTRC

If the MTRC is reset, the MRCAL register will be reset, too. Therefore the beforehand stored MRCAL register value has to be written back.
Please see the following procedure for the $\overline{\text{MTRESET}}$ Release of the MTRC.

***Figure 5-5: Flowchart for MTRESET Release***

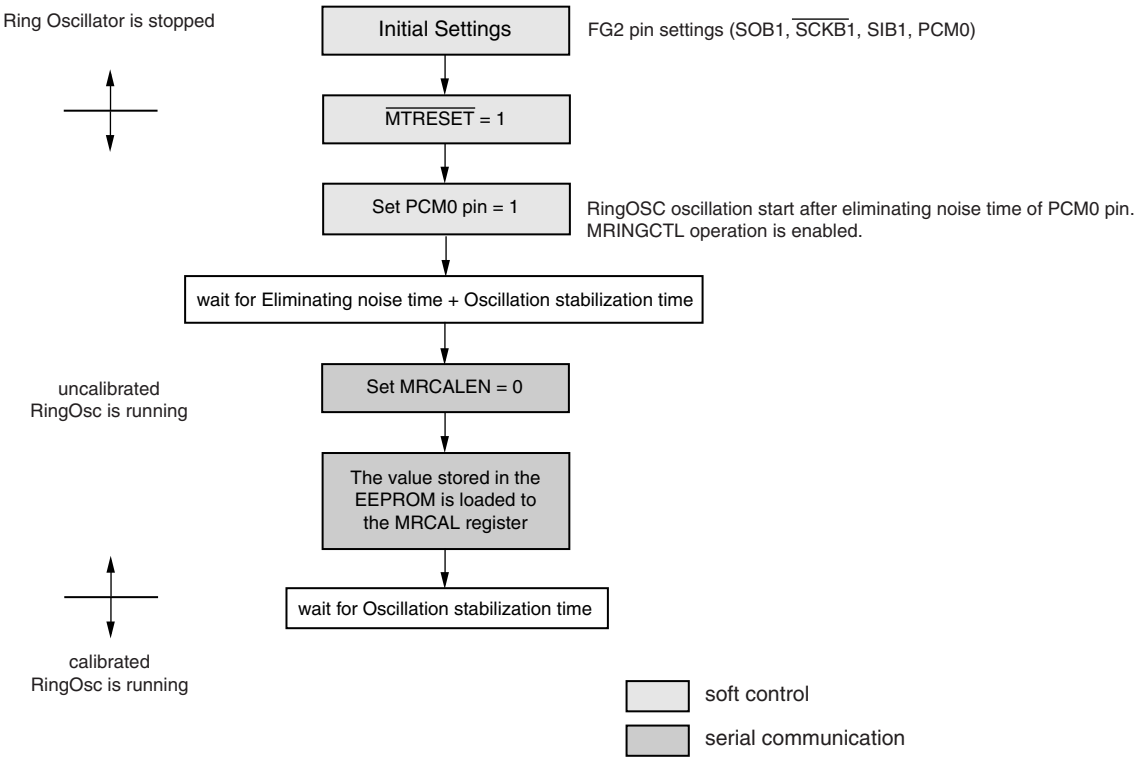
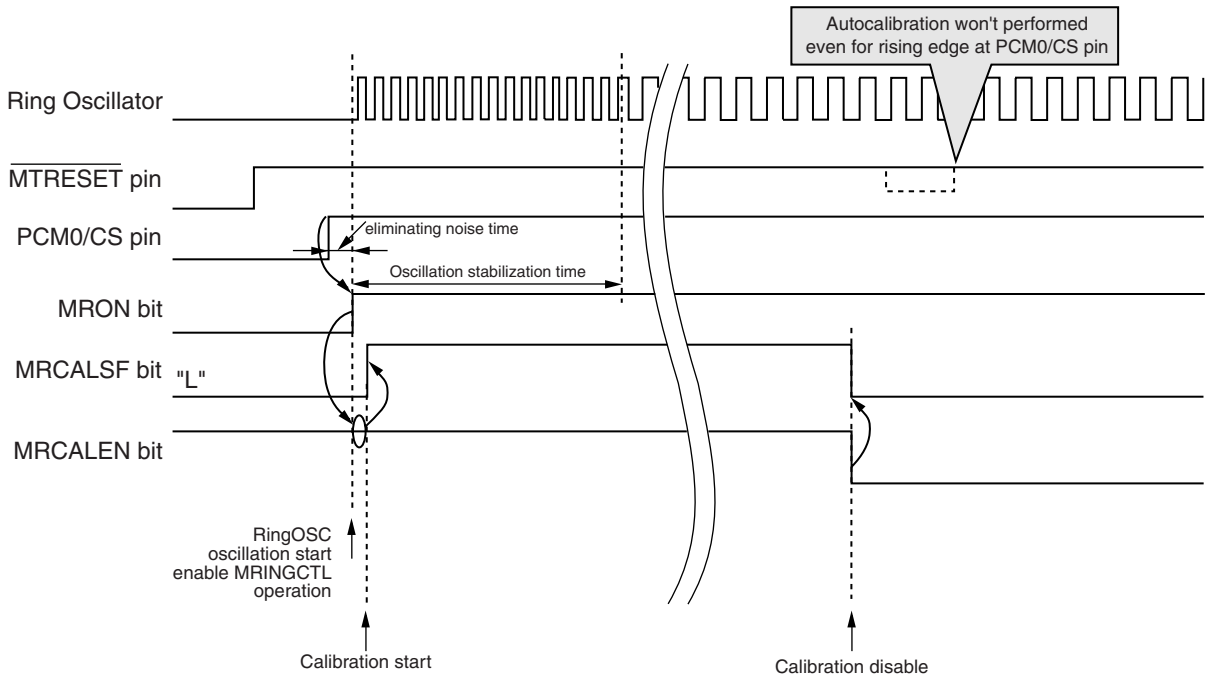


***Figure 5-6: Timing for MTRES Release***



## 5.5 Standby Mode Release of the Ring Oscillator

To save power, the ring oscillator could be switched off via setting the MRON bit of the MRCTL register = 0.
During the time of the stopped Ring Oscillator, the data retention of the MRCAL register can't be guaranteed. Therefore the before stored value of the MRCAL register (e.g. in an external EEPROM) has to be write back to the MRCAL register after the waken.
The PCM0 pin of the FG2 will wake up the Ring Oscillator from its standby mode.
To switch the Ring Oscillator on again the following procedure has to be fulfilled.

***Figure 5-7: Flowchart for Standby Mode Release***

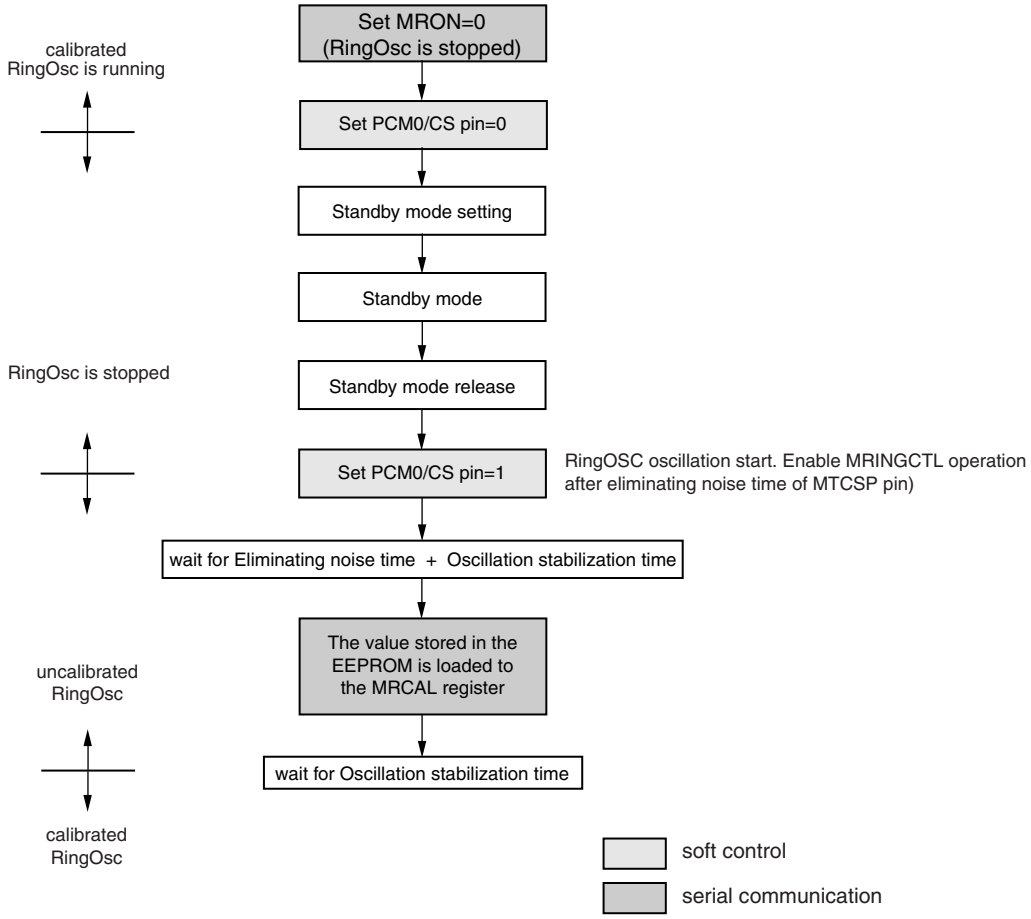
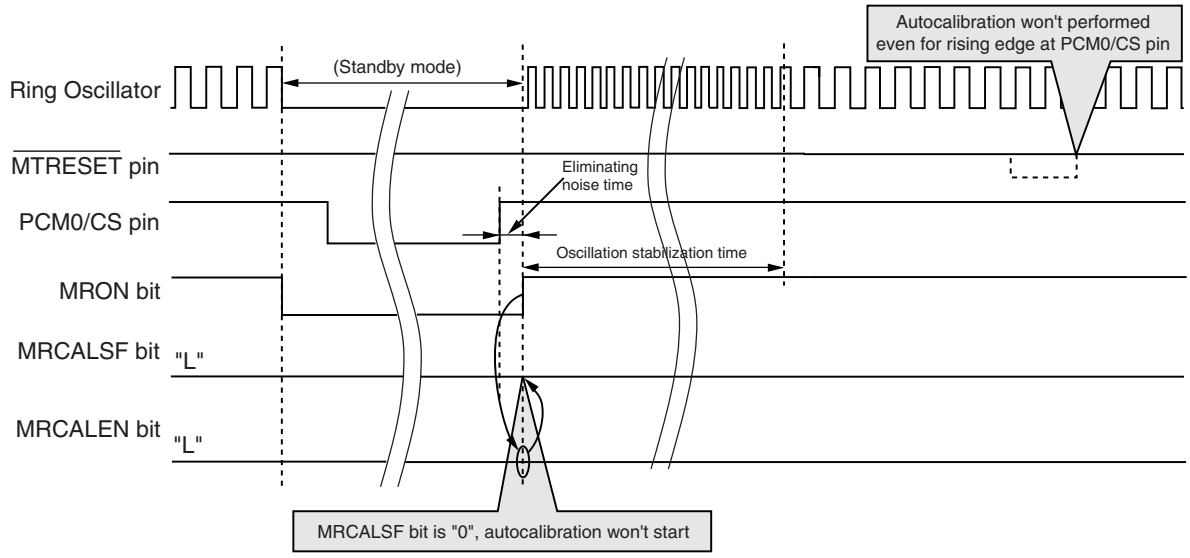


***Figure 5-8: Timing Diagram for Standby Mode Release***



## 5.6 Cautions

(1) The calibration has to be performed at the specified conditions (Temperature and Voltage). If performing at other condition, the accuracy of the ring oscillator cannot be guaranteed.

(2) The basic calibration pulse must have the specified High and Low pulse width at the PCM0/CS pin.

(3) Be sure to input 5 basic pulses.

(4) After calibration executing, the MRCALERR bit = 0 has to be checked before storing the MRCAL value (i.e. in an EEPROM). This has to be done after setting the MTCS pin = 1 and performing the 5 basic calibration pulses.

(5) If a calibration error occurs (check if after 5 basic calibration pulses the MRCALERR bit = 1), set the MRON bit to "0". After this set it to "1" again and execute the calibration once again. This can be necessary if the calibration conditions were not adhered to the calibration condition specification.

(6) The power consumption can be reduced by stopping the RingOSCs by clearing the MRON bit to “0”. Therefore the basic clock supply of the MTRC will be stopped, too. When after power save mode release the MRON bit is set to “1” again, the stored calibration value has to be written to the MRCAL register first. If this is not executed, the accuracy of the ring oscillator cannot be guaranteed.

(7) During power save mode the MTCS pin can not be used, except for power save mode release only.

(8) Be sure to set the MRCALEN bit = 0 after system reset has been released and the operation of ring oscillator has been started. If this is not done, the accuracy of the ring oscillator cannot be guaranteed.

(9) Secure the “eliminating noise time” of PCM0/CS signal and the “oscillation stabilization time of the ring oscillator” at power save mode release.

(10) Secure oscillation stabilization time of the ring oscillator before writing the stored calibration value to the MRCAL register.

(11) Do not set the MRCALEN bit = 0 when the automatic calibration is executed. (The MRCALEN bit can't be set to “1” after set to “0”. This will be done by hardware only at $\overline{\text{MTRESET}}$ = 0.)

**[MEMO]**

# Chapter 6 Serial Interface

## 6.1 Communication Protocol

The CSI of the MTRC is fixed to the following operation mode:

Communication protocol: Clocked synchronous serial interface

- Data length: 8-bits fixed
- Transfer direction: MSB first
- Transfer mode: Transmit/Receive mode
- Serial clock frequency: $f_{SCK} <= f_{Ring\ Oscillator} / 4$

**Remark:** $f_{SCK}$: Serial Interface clock
$f_{Ring\ Oscillator}$: frequency of MTRC Ring Oscillator

Communication format:

| 1st byte<br>(Command + Address) | 2nd byte to last byte<br>(Data) |
|---|---|

## 6.2 Command Table

| Instruction | Command (+ Address) | Data |
|---|---|---|
| READ | $I_7I_6A_5A_4A_3A_2A_1A_0$<br>(input) | $D_7D_6D_5D_4D_3D_2D_1D_0$<br>(output) |
| WRITE | $I_7I_6A_5A_4A_3A_2A_1A_0$<br>(input) | $D_7D_6D_5D_4D_3D_2D_1D_0$<br>(input) |

### 6.2.1 Command Byte

This is the 1st Received Data at communication start, that was sent from the FG2 device.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Command | RW | AUTO | A5 | A4 | A3 | A2 | A1 | A0 |

| RW | R/W Selection of MTRC |
|---|---|
| 0 | Read |
| 1 | Write |

| AUTO | Operation mode of Communication |
|---|---|
| 0 | Disable Continuous transfer |
| 1 | Enable Continuous transfer |

| A5 to A0 | Address |
|---|---|
| 0/1 | define address data as 6-bit format |

### 6.2.2 Data Bytes

After the Command Byte the Data Bytes follows.

When read function is selected, the MTRC outputs data which was specified by the address of the Command Byte.
When the write function is selected the FG2 device outputs data which are written to the MTRC addresses specified by the Command Byte before.

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Data | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

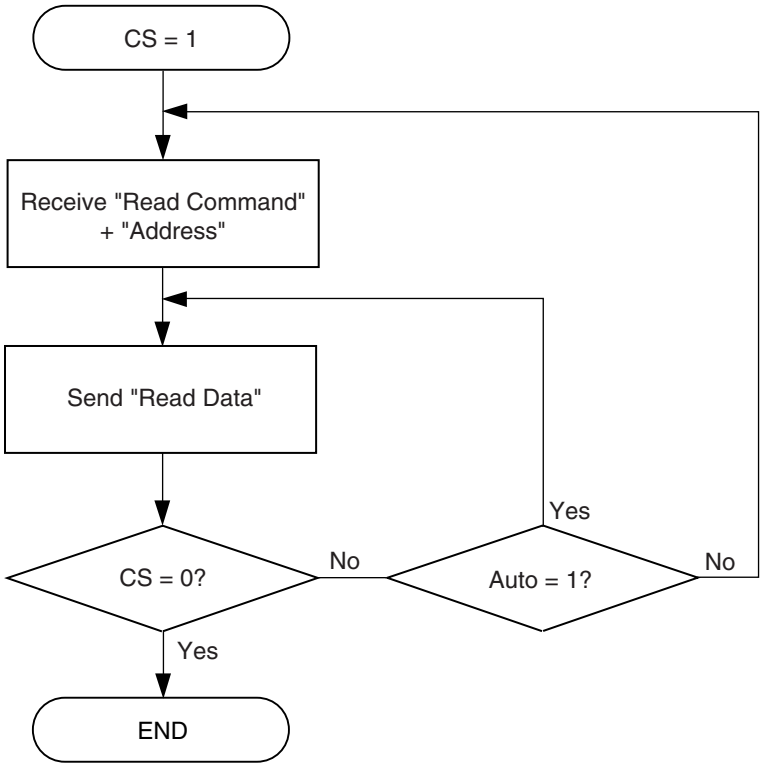
## 6.3 Serial I/F Operation

### 6.3.1 Read from MTRC operation

After PCM0/CS = “1”, the MTRC is waiting for the command byte via the SI pin. If the read command is received the MTRC outputs data via the SO pin, which were specified with the address bits A5 to A0.

When continuous transfer is selected (Auto bit of Command Byte = “1”), the MTRC outputs next data, at the incremented address via the SO pin.

***Figure 6-1: MTRC Operation Flow on Reading***



### 6.3.2 Timing of MTRC Read operation

***Figure 6-2: MTRC Read Operation (Auto=0)***

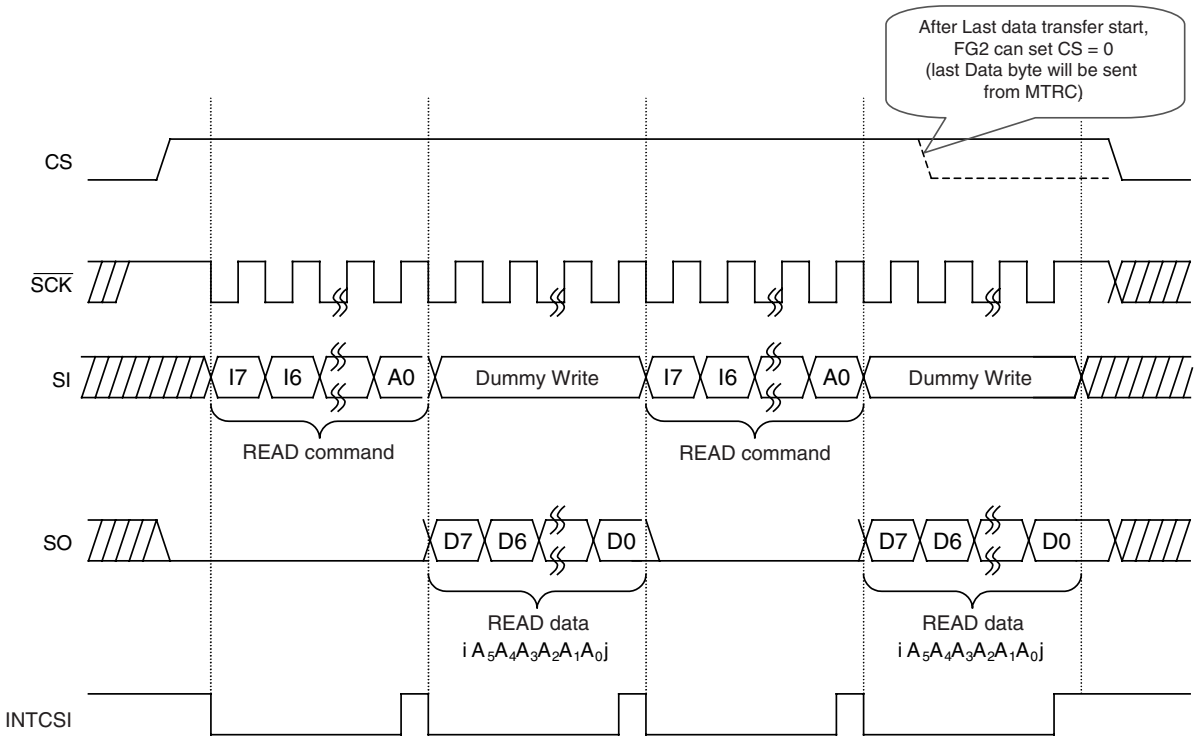
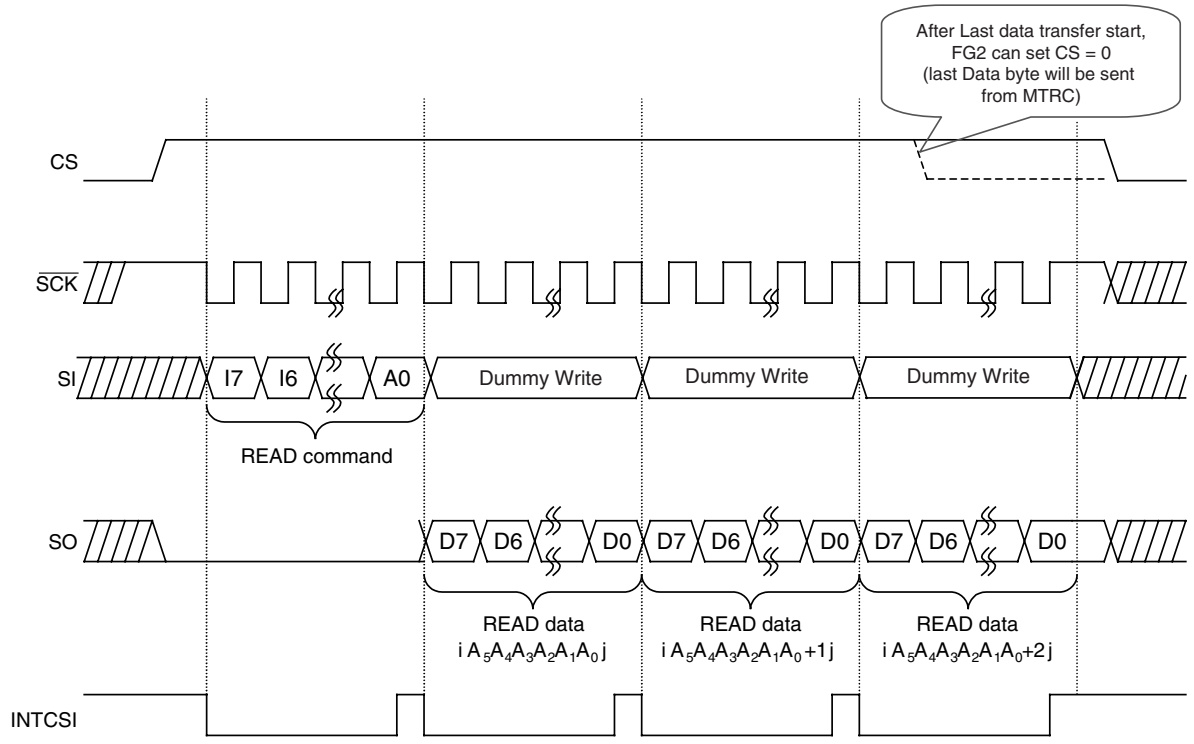


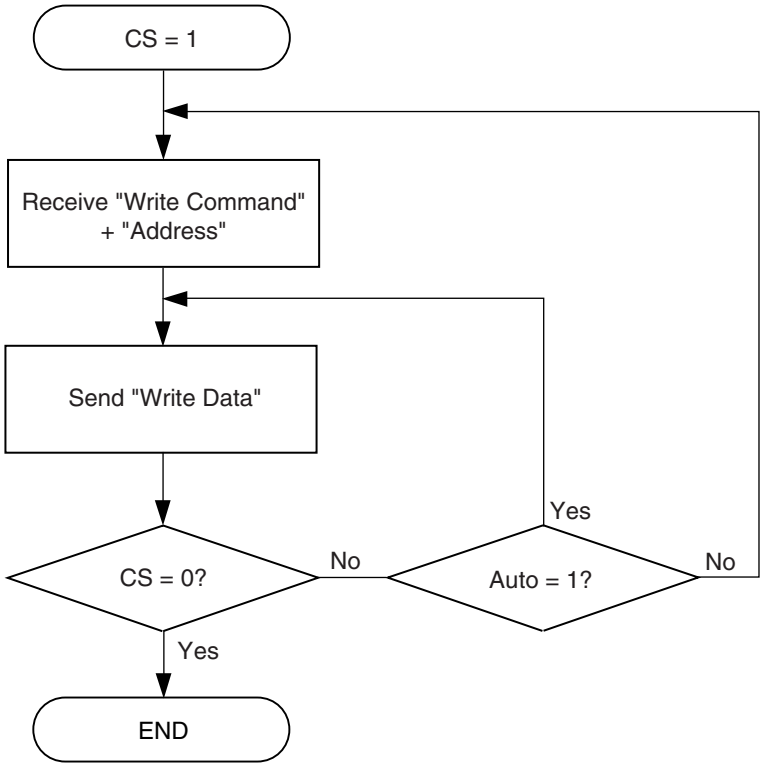

***Figure 6-3: MTRC Read Operation (Auto bit = 1)***



### 6.3.3 MTRC Write operation

After CS pin = “1", MTRC received write command/address via SI pin. After receive command, MTRC write next receive data, which is specified address.
When select continuous mode (Auto = “1”), next receive data will be written 1 incremented address. When select disable continuous mode (Auto = “0”), After receive 1 byte data, MTRC decide that next received data as command/address

***Figure 6-4: Operation Flow on MTRC Writing***



### 6.3.4 Timing of MTRC Write operation

***Figure 6-5: MTRC Write Operation (Auto bit = 0)***

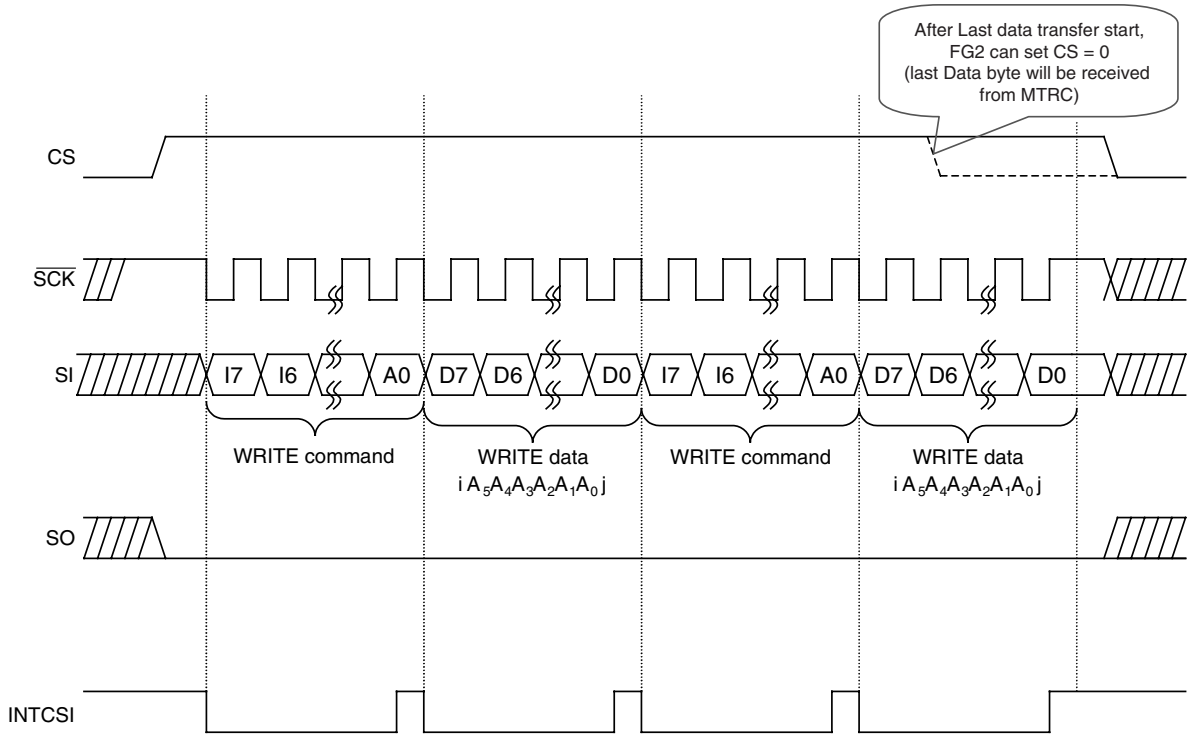
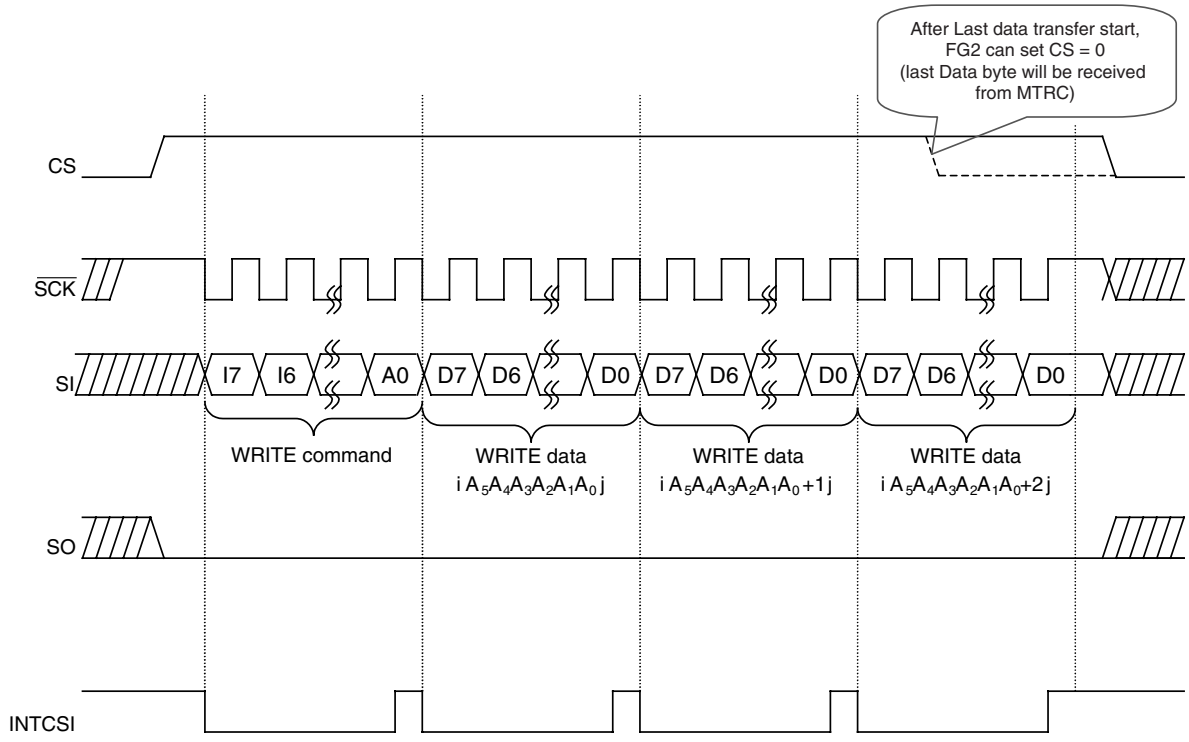



***Figure 6-6: MTRC Write Operation (Auto bit = 1)***



## 6.4 External CSIB1 Function (EXCSI1)

If the PMT4 port is configured for peripheral mode the PCM0/CS signal controls the output function of the external CSIB1 (EXCSI1) functionality. The EXCSIB1 provide the FG2 CSIB1 communication for external components, too. This function can be used, if there's no internal communication between the FG2 device and the MTRC (refer to Figure 1-2, "CS Functionality," on page 20).
With special regard to the last byte transfer of the internal communication protocol a switch control will delay the switching until the last byte was transferred between FG2 and the MTRC.

**Remarks:** **1.** If the EXCSI1 is used, and the CS is set to "0" during the last byte transfer, the EXSO1 and EXSI1 signal will be suppressed until the last Byte transfer has ended. Therefore an external component receives no signals from the last internal MTRC communication.

**2.** After the switching the last communicated signal level at SOB1 of the internal communication will remain at the EXSO1 pin.

## 6.5 Internal CSIB1 Function

### 6.5.1 Operation of Serial Interface

The communication I/F of the MTRC is fixed to the following settings:

- I/F: CSI
- Mode: Slave mode
- Data length: 8-bits
  (support continuous data transfer,
  therefore the FG2 CSIB1 can use 16-bit data length)
- Transfer: MSB first
- Transmission: transmission/reception mode
- Baudrate: maximum $f_{Ring\ Oscillator}$ / 4

**Cautions: 1. The internal ring oscillator of the MTRC is not synchronized to the CSIB1 $\overline{SCKB1}$ signal. Furthermore the MTRC needs time to process the incoming commands and data. Therefore the baudrate of the FG2 CSIB1 has to be set to maximum of $f_{Ring\ Oscillator}$ / 4.**

**2. After $\overline{MTRESET}$ release, the Ring Oscillator is uncalibrated. Therefore the maximum specified frequency deviation (especial the min. $f_{Ring\ Oscillator}$) for the uncalibrated Ring Oscillator has to be regarded.**

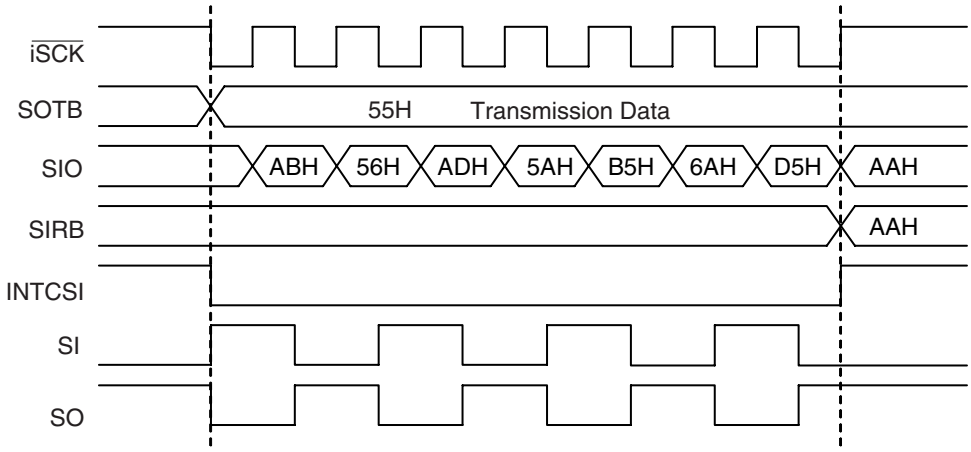
**(1) Basic operation**

The MTRC serial interface is only working in slave mode.

When iSCK clock is applied the transfer operation is started.
There's a delay between SCK of the CSIB1 from FG2 and the iSCK of the MTRC. The iSCK signal is synchronised with the MTRC Ring Oscillator. If the Ring Oscillator is stopped no communication is possible.

SIO shift operation is synchronised with the falling edge of iSCK. The data which is received via SI pin is latched.
SIO on rising edge of iSCK.

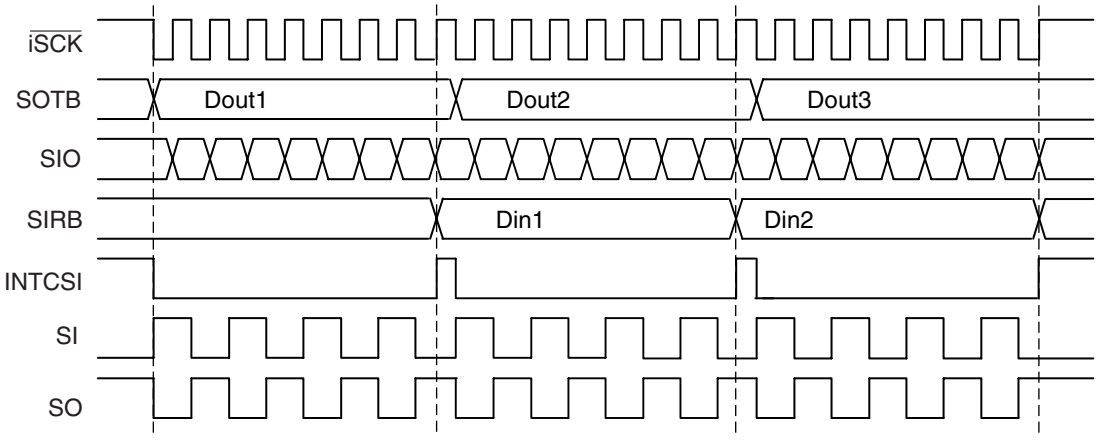
***Figure 6-7: Basic Operation***




**(2) Continuous data transfer**

In spite of the fix 8-bit mode of the MTRC CSI, it supports continuous data transfer mode.
Therefore the FG2 CSIB1 can set to 16-bit mode and continuous data transfer for the fastest communication.

***Figure 6-8: Continuous Data Transfer***



**[MEMO]**

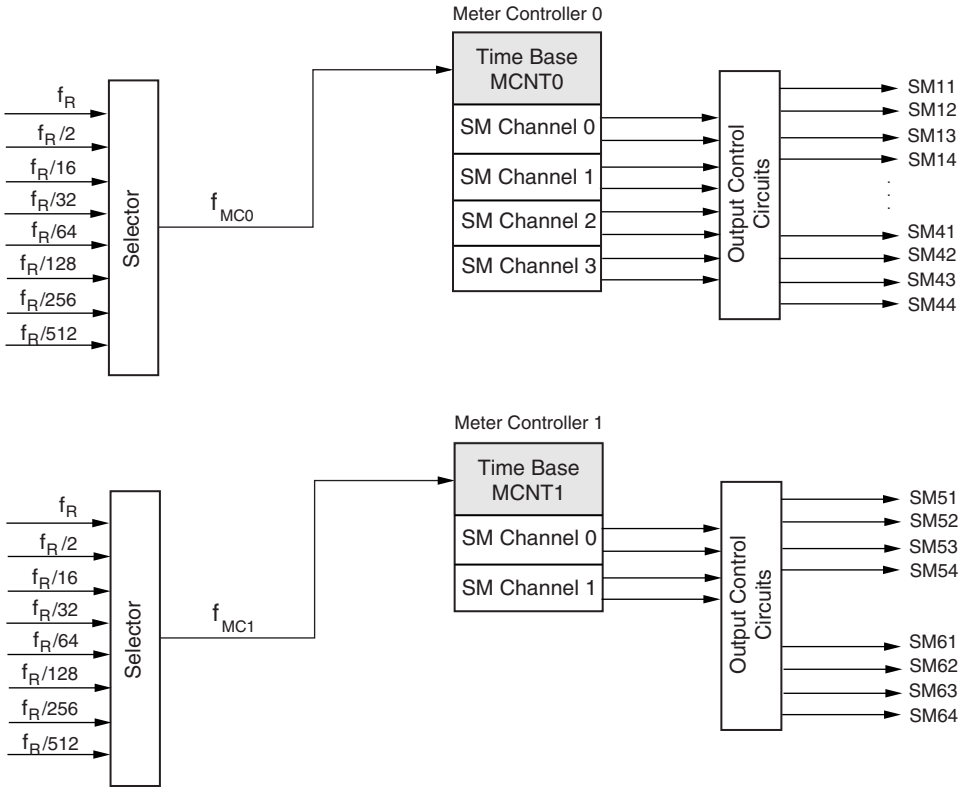
# Chapter 7 Meter Controller Driver

This MTRC has 6 × 360° type meters controllable driver.

## 7.1 Meter Controller Driver Function Outline

- 8-bit free run counter × 2
- 8-bit compare register × 12
- 8-bit +1 accuracy PWM output × 24

***Figure 7-1: Meter Controller Driver Block Diagram***



## 7.2 Register Setting

### 7.2.1 Free Running Counter m (MCNTm, m = 0, 1)

MCNTm is an 8-bit free running counter. This counter will be incremented by $f_{MCn}$ (n = 0, 1). This frequency is generated from CLK1 and the selected prescaler.
The counter starts by setting the PCEm bit =”1” of MCNTCm register.
After reaching the value FFH the counter will be overflowed and set itself to 01H.

MCNTm can’t be written or read.

***Figure 7-2: Free Running Counter MCNTm Format***

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| MCNTm | MCNTm | | | | | | | | | 00H |
| R/W | _ | | | | | | | | | |

The count value is cleared in the following cases.

- RESET = “0”
- PCEm = “0”

The relation of the duty factor for the PWM output from the SMnm pin is calculated by the following expression:

$$\text{PWM (duty)} = \text{Set value MCMPnm} / 255 \times 100\%$$

**Remark:** n = 1 to 6
m = 0, 1

### 7.2.2 Sin Compare Register n0 (MCMPn0, n = 1 to 6)

MCMPn0 is an 8-bit register, which continuously compares its value with the MCNTm value. When the two values match, a match signal of sin side of meter n is generated.
MCMP10 to MCMP40 are compared with MCNT0, MCMP50 to MCMP60 are compared with MCNT1.
MCMPn0 are in master-slave configuration. MCNTm is compared with the slave register.

Transmit from master register to slave register executes at

TENn =”1” AND when overflow occurs.

Ensure that the TENn bit =”0” (i.e. rewriting time < PWM cycle time), then set MCMPn0 and the corresponding TENn bit to 1.

The PWM pulse is not output until the first overflow occurs after the counting operation has been started, because the compare data is not transferred to the slave beforehand.

MCMPn0 is set with an 8-bit memory manipulation instruction.
The value of these register are set to 00H at MTRESET = “0”.

***Figure 7-3: Sin Compare Register MCMPn0 Format***

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| MCNPn0 | MCMPn0 | | | | | | | | **Notes** | 00H |
| R/W | R/W | | | | | | | | | |

**Note:** MCNP10 at 0x00
MCNP20 at 0x03
MCNP30 at 0x06
MCNP40 at 0x09
MCNP50 at 0x0C
MCNP60 at 0x0F

**Remark:** n = 1 to 6

### 7.2.3 Cos Compare Register n1 (MCMPn1, n = 1 to 6)

MCMPn1 is an 8-bit register, with the same functionality of the MCMPn0 register but for the cos signal. When the above two values match, a match signal of cos side of meter n is generated.
MCMP11 to MCMP41 are compared with MCNT0, MCMP51 to MCMP61 are compared with MCNT1.

For the handling of the TENn bit please refer to the MCMPn0 register

MCMPn1 is set with an 8-bit memory manipulation instruction.
The value of these register are set to 00H at $\overline{\text{MTRESET}}$ = “0”.

***Figure 7-4: Cos Compare Register MCMPn1 Format***

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| MCNPn1 | MCMPn1 | | | | | | | | **Note** | 00H |
| R/W | R/W | | | | | | | | | |

**Note:** MCNP11 at 0x01
MCNP21 at 0x04
MCNP31 at 0x07
MCNP41 at 0x0A
MCNP51 at 0x0D
MCNP61 at 0x10

**Remark:** n = 1 to 6

### 7.2.4 Compare Control Register (MCMPCn, n = 1 to 6)

MCMPCn is an 8-bit register that controls the operation of the compare register and output direction of the PWM pin. TENn bit becomes “0” automatically after finished transmission from master register to slave register.

**Caution: If the master register is written during transmit from master register to slave register, transmission data may break. Confirm that the time for rewriting the TEN bit is greater then the count period of the MCNTm counter register.**

MCMPCn is set with an 8-bit memory manipulation instruction.
MTRESET =”0” clears MCMPCn to 00H.

***Figure 7-5: Compare Control Register MCMPCn Format (1/2)***

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| MCMPCn | 0 | 0 | 0 | TENn | ADBn1 | ADBn0 | DIRn1 | DIRn0 | **Note** | 0 |
| R/W | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |

**Note:** MCMPC1 at 0x02
MCMPC2 at 0x05
MCMPC3 at 0x08
MCMPC4 at 0x0B
MCMPC5 at 0x0E
MCMPC6 at 0x11

| TENn | Enable transfer by register from master to slave |
|---|---|
| 0 | Disable data transfer from MCMPnm master to slave.<br>New data can be written. |
| 1 | Enable data transfer from MCMPnm master to slave.<br>(Data transfer is executed from master to slave when next MCNTm overflow occurs)<br>New data cannot be written. |

**Caution: Ensure that the time for rewriting the TEN bit is greater then the count period of the MCNTm counter register (PWM cycle time).**

**Remarks: 1.** TENn bit is cleared automatically after data transfer from MCMPnm master register to slave register has finished.

**2.** Don’t rewrite TENn bit when CAE bit is “0”.

*Figure 7-5: Compare Control Register MCMPCn Format (2/2)*

| ADBn1 | Control of 1-bit addition circuit (cos side of meter n) |
|---|---|
| 0 | No 1-bit addition |
| 1 | 1-bit addition |

| ADBn0 | Control of 1-bit addition circuit (sin side of meter n) |
|---|---|
| 0 | No 1-bit addition |
| 1 | 1-bit addition |

The 1-bit addition adds 1 further PWM tick to the PWM value that was set with the MCMPnm register, but only every second PWM cycle. Therefore in the average value will be only 1/2 PWM tick, which corresponds with a further bit for the resolution of the PWM value (quasi 9-bit resolution).

| DIRn1 | DIRn0 | Control of PWM output pin | | | |
|---|---|---|---|---|---|
| | | SMn1 (sin+) | SMn2 (sin-) | SMn3 (cos+) | SMn4 (cos-) |
| 0 | 0 | PWM | 0 | PWM | 0 |
| 0 | 1 | PWM | 0 | 0 | PWM |
| 1 | 0 | 0 | PWM | 0 | PWM |
| 0 | 1 | 0 | PWM | PWM | 0 |

### 7.2.5 Timer Mode Control Register (MCNTm) (m = 0, 1)

MCNTCm is an 8-bit register that controls the operation of the timer counter MCNTm. MCNTCm is set with an 8-bit memory instruction.
MTRESET =”0” clears MCNTCm to 00H.

***Figure 7-6: Timer Mode Control Register (MCNTm) Format (1/2)***

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | Initial value |
|---|---|---|---|---|---|---|---|---|---|---|
| MCNTCm | CAE[Note1] | 0 | 0 | PCEm | 0 | SMCLm2 | SMCLm1 | SMCLm0 | Note2 | 0 |
| R/W | R/W | R | R/W | R/W | R | R/W | R/W | R/W | | |

**Notes: 1.** CAE is a flag that is only available in MCNTC0.

**2.** MCNTC0 at 0x12
MCNTC1 at 0x13

**Cautions: 1. First of all, set CAE = “1” to operate this macro.**

**2. To enable the operation the PCE bit has to be set to “1”, after setting the CAE, SMCL02, SMCL01 and SMCL00 bits.**

**3. At DJ2 (6 SM channels): to set this macro into power save mode first set PCE1 = 0 then set the CAE and PCE0 bit simultaneously to “0”**

**Remark:** SMCL02, SMCL01, SMCL00 bit and CAE bit can be written at same time in purpose to decrease frequency of register access.

| CAE | Control of internal clock operation |
|---|---|
| 0 | Disables the internal clock supply |
| 1 | Enables the internal clock supply |

By setting CAE = 0 the count operation is stopped. This is used to reduce the power consumption.

**Remark:** If the CAE bit will be set to “0” the counter MCNTCn register will hold it’s value and the PWM output pin will hold its actual Level. To clear the counter and set the PWM output pin to inactive level, PCEm = 0 has to be set beforehand.

| PCEm | Timer counter operation control |
|---|---|
| 0 | Operation is stopped with clearing the timer value<br>and the associated PWM output pins will be set to Low level |
| 1 | Operation enable |

**Remarks: 1.** the CAE and PCE0 bit can be set simultaneously to “0” (same register)

**2.** If only the 4 SM channels of the MCMT0 counter are used the power consumption can be reduced by writing the CAE bit and the PCE0 bit simultaneously. In other cases set PCE1 bit = 0 beforehand.

***Figure 7-6: Timer Mode Control Register (MCNTm) Format (2/2)***

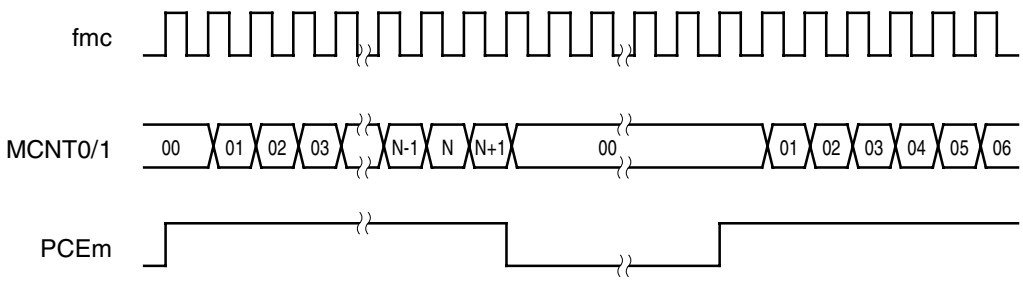
| SMCLm2 | SMCLm1 | SMCLm0 | Timer counter 1 clock selection |
|---|---|---|---|
| 0 | 0 | 0 | $f_R$ |
| 0 | 0 | 1 | $f_R$ / 2 |
| 0 | 1 | 0 | $f_R$ / 16 |
| 0 | 1 | 1 | $f_R$ / 32 |
| 1 | 0 | 0 | $f_R$ / 64 |
| 1 | 0 | 1 | $f_R$ / 128 |
| 1 | 1 | 0 | $f_R$ / 256 |
| 1 | 1 | 1 | $f_R$ / 512 |

## 7.3 Operation

### 7.3.1 Count timing

The counter is counted up by the rising edge of the $f_{MCn}$ clock signal that is selected by the SMCLm2 to 0 bits.
The counting operation is enabled or disabled by the PCEm bit of the timer mode control register.
The MCNTm register is cleared by MTRESET = “0” or PCEm = “0” and counting operation stops.
The first count cycle could include a clock error ≤ 1 $f_{MCn}$ clock due to the fact of the synchronization with the $f_{MCn}$ clock.

***Figure 7-7: Restart Timing after Counting Operation Stopped***



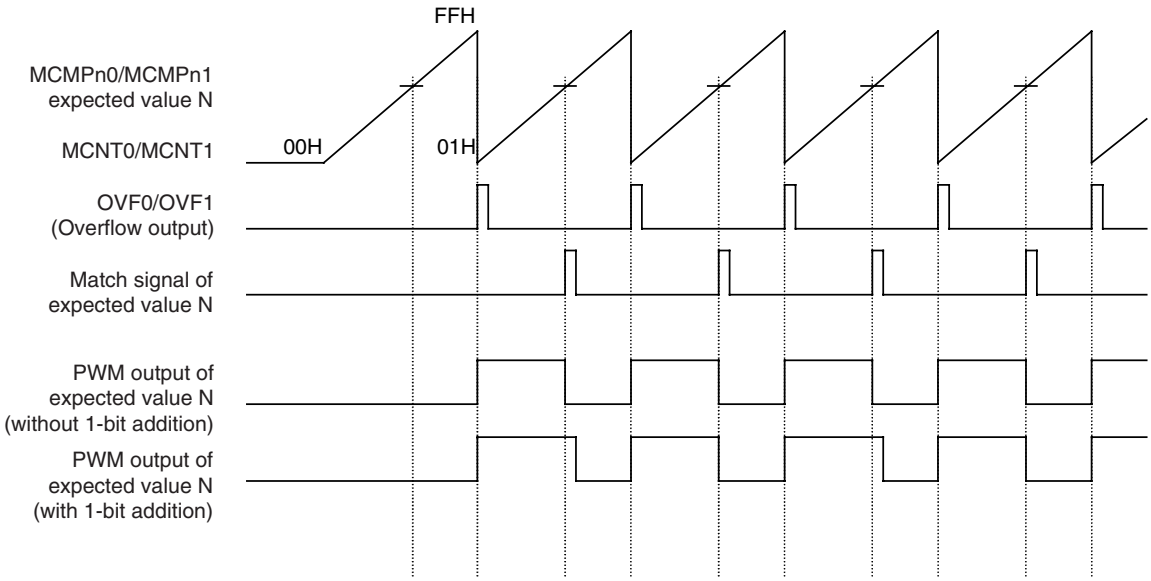

**Remark:** Counting operation starts → counting operation stops → counting operation start

### 7.3.2 Operation of 1-bit addition circuit

1-bit addition to the PWM output is activated by setting ADBn1, ADBn0 bit of the MCMPCn register to “1”.

1-bit addition mode repeats 1-bit addition/non-addition to PWM output alternately upon MCNTm overflow output, and enables the state of PWM output between current compare value N and the next compare value N+1.

***Figure 7-8: Operation of 1-bit Addition***




**Remark:** n = 1 to 6
m = 0, 1

### 7.3.3 PWM output with 1 clock shifted operation

If the output of the sin/cos signal of meter channel 1 to 4 (5 and 6) rises/falls internally as indicated by the broken line, the SM11 to SM44 (SM51 to SM64) pins always shift the rising edge of the output pin by 1 count clock of the MCNTm counter. This shifted outputs prevent high current peaks that leads to $V_{DD}$/GND fluctuating.

*Figure 7-9: Output Timing of SM11 to SM44*

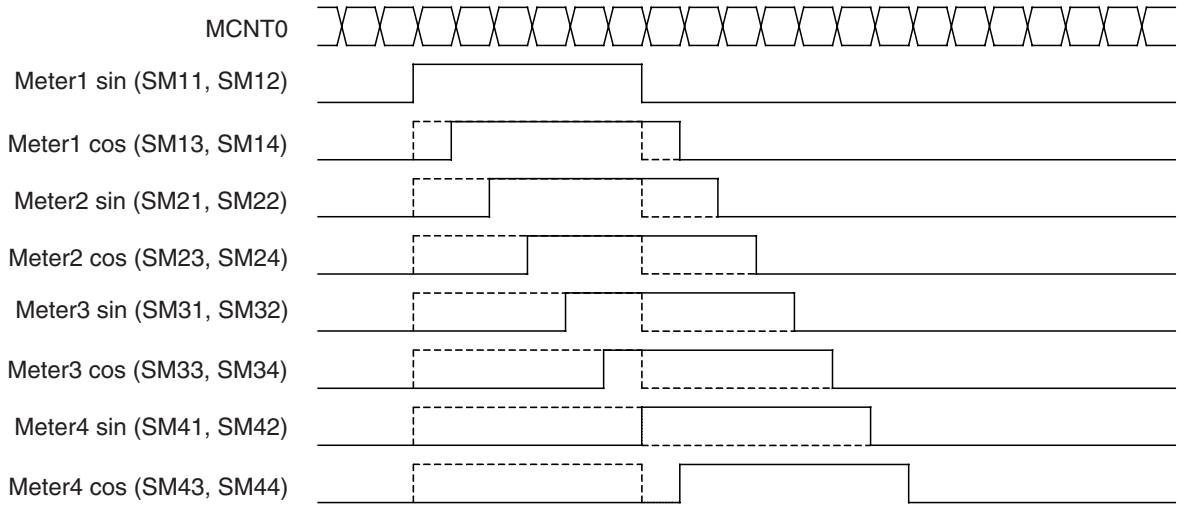
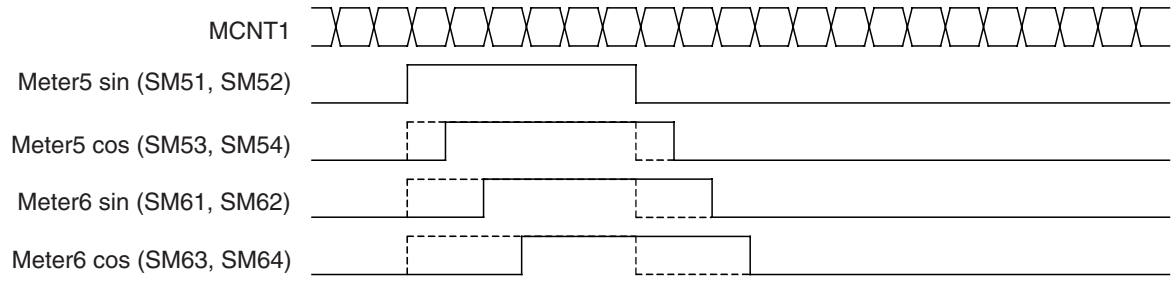
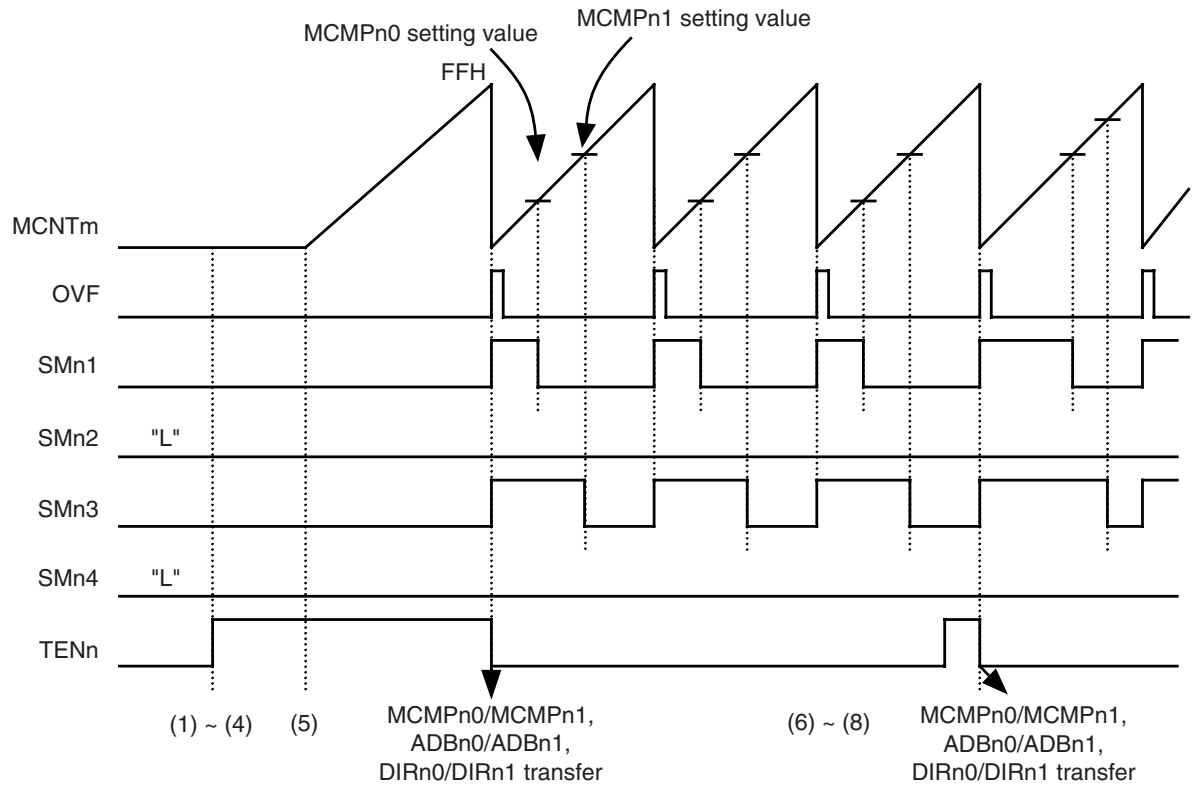



*Figure 7-10: Output Timing of SM51 to SM64*



## 7.4 Method of Using

***Figure 7-11: Using of the SM***

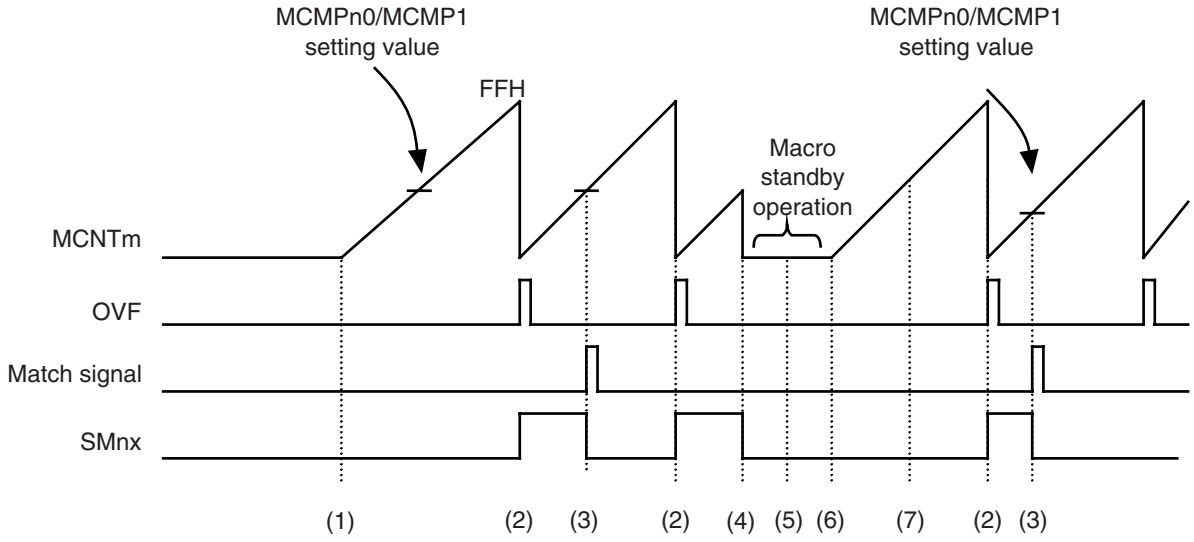



(1) Setting SM pin to output mode by Port mode register assigned to SMn1 to SMn4 output
(2) Input clock is supplied to the macro by setting CAE = “1”
(3) Set compare register MCMPn0, MCMPn1
(4) Set TENn = “1” and ADBn0/1, DIRn0/1 bits by setting compare mode control register MCMPCn.
(5) Set PCE0/1 = “1”, the counting operation/timing (with the specified counting selection) starts.
(6) Ensure that TENn = “0” (rewriting period longer than count period until overflow)
(7) Rewrite compare register MCMPn0, MCMPn1.
(8) Set TENn = “1” (ADBn1, ADBn0, DIRn1, DIRn0 can be written at the same time if necessary).

### 7.4.1 Macro Standby operation

By setting PCE1 and PCE0/CAE = “0” of MCMTCn register, the timer stops count operation and the PWM output is set to “0”. After that the macro is in power saving standby mode state.

***Figure 7-12: SM Standby Operation***




ADBn1 = 0, ADBn0 = 0, DIRn1 = 0, DIRn0 = 0

(1) PCEm = “1” is written, counting operation starts.
(2) Overflow occurs
(3) MCMPn0 or MCMPn1 match with setting value.
(4) CAE = “0" and PCEm = “0" are written, counting value is cleared & operation stops, PWM output is disabled.
(5) MCMPn0 or MCMPn1 is rewritten.
(6) CAE = “1" and PCEm = “1" are written, counting operation starts
(7) TENn = “1” is written (ADBn1, ADBn0, DIRn1, DIRn0 bits can be written at the same time if necessary)

**[MEMO]**

# Chapter 8 Reset Function

## 8.1 Separated Reset Functions

The reset functions of the FG2 and the MTRC are separated to each other. Therefore the application has to coordinate the reset states.

## 8.2 External Reset Circuitry

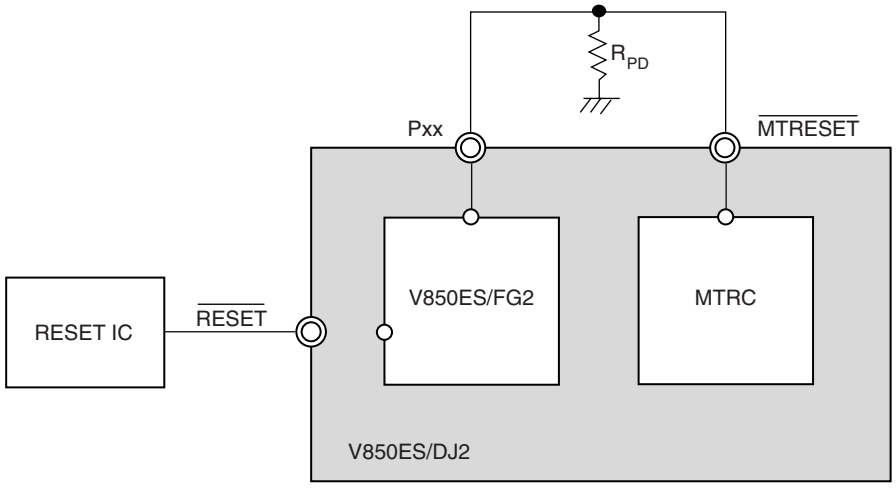
To control the Reset state of the MTRC it is recommended, to connect the $\overline{\text{MTRESET}}$ pin to an output port of the FG2.

**Remarks: 1.** It is not possible to connect the $\overline{\text{MTRESET}}$ pin of the MTRC and $\overline{\text{RESET}}$ pin of the FG2 together.
(If the FG2 comes into Reset state during a serial transmission via the CSIB1, the communication can't be restarted. Because of the independent clock supply of the MTRC, it will wait for the continuation of the broken communication. But if the Reset state of the F_Series is released, the MTRC SFRs would be re-initialized with a totally new transmission of the CSIB1 again. Therefore the communication will be left out of synchronization.)

**2.** During a Power save mode the signal at $\overline{\text{MTRESET}}$ pin should be high to remain the MTRC in operation mode (but switched off Ring Oscillator). Otherwise the MTRC will consume in reset mode more current via the PU/PD resistors at the internal connection pins.

### 8.2.1 External reset circuitry with pull-down resistor

***Figure 8-1: External Reset Circuitry with Pull-Down Resistor***

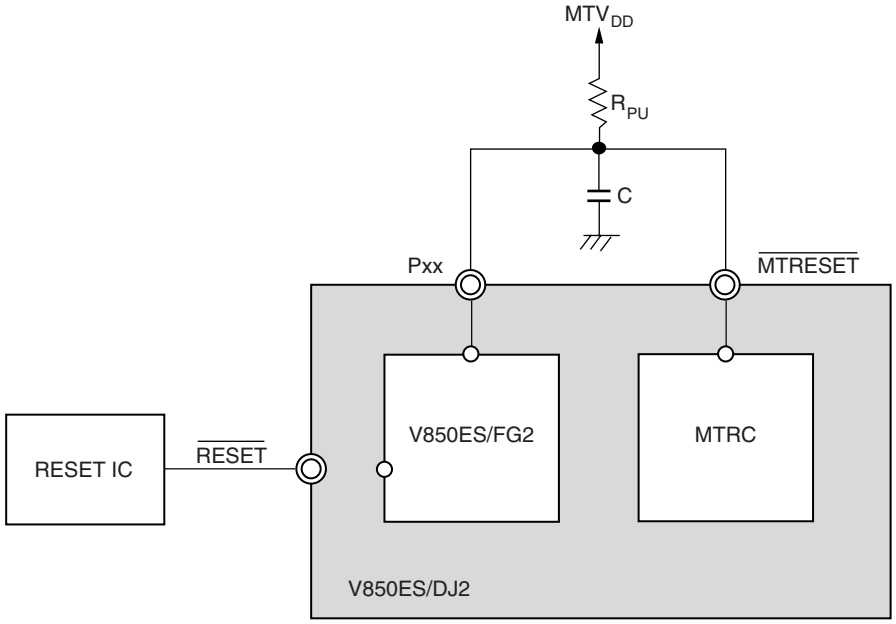



This circuitry is the best choose for safety applications, but consumes more power in power save modes.

If the FG2 will be reset via an internal (LVI or WD) or external function ($\overline{\text{RESET}}$), the Pxx pin will be set into its reset mode (input) and the pull down resistor will set the MTRC into reset state, too.
In power save mode a continuous current will be consumed via $R_{PD}$.

### 8.2.2 External reset circuitry with pull-up resistor

*Figure 8-2: External Reset Circuitry with Pull-Up Resistor*




This circuitry saves more power, but at internal reset in the FG2 device, the MTRC will be left active with its last configured settings.

If MTVDD will be applied, the signal at $\overline{\text{MTRESET}}$ pin will release the reset mode of the MTRC. The capacitor will cause a delay between MTVDD apply and MTRESET release, to ensure the minimum specified time between this points of time.

If the FG2 will be reset via an internal (LVI or WD) or external function ($\overline{\text{RESET}}$), the $P_{XX}$ port will be set into its reset mode (input) but the pull up resistor $R_{PU}$ will hold the MTRC in its normal operation mode. Therefore the last configured action (PWM signal) will remain. It has to be checked if this leads to critical application states.
After the RESET release of the FG2 device, the MTRC should be reset via $\overline{\text{MTRESET}}$ pin as soon as possible (i.e. in the start-up code).

# Chapter 9 Electrical Specification

## 9.1 Absolute Maximum Ratings ($T_A$ = 25°C)

| Parameter | Symbol | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | $V_{DD}=EV_{DD}=BV_{DD}=AV_{REF0}=MTV_{DD}=SMV_{DD}$ | | -0.3 to +6.5 | V |
| | $EV_{DD}$ | $V_{DD}=EV_{DD}=BV_{DD}=AV_{REF0}=MTV_{DD}=SMV_{DD}$ | | -0.3 to +6.5 | V |
| | $BV_{DD}$ | $V_{DD}=EV_{DD}=BV_{DD}=AV_{REF0}=MTV_{DD}=SMV_{DD}$ | | -0.3 to +6.5 | V |
| | $MTV_{DD1,2}$ | $V_{DD}=EV_{DD}=BV_{DD}=AV_{REF0}=MTV_{DD}=SMV_{DD}$ | | -0.3 to +6.5 | V |
| | $SMV_{DD1,2,3}$ | $V_{DD}=EV_{DD}=BV_{DD}=AV_{REF0}=MTV_{DD}=SMV_{DD}$ | | -0.3 to +6.5 | V |
| | $AV_{REF0}$ | $V_{DD}=EV_{DD}=BV_{DD}=AV_{REF0}=MTV_{DD}=SMV_{DD}$ | | -0.3 to +0.3 | V |
| | $V_{SS}$ | $V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=MTV_{SS}=SMV_{SS}$ | | -0.3 to +0.3 | V |
| | $EV_{SS}$ | $V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=MTV_{SS}=SMV_{SS}$ | | -0.3 to +0.3 | V |
| | $BV_{SS}$ | $V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=MTV_{SS}=SMV_{SS}$ | | -0.3 to +0.3 | V |
| | $MTV_{SS1}$ | $V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=MTV_{SS}=SMV_{SS}$ | | -0.3 to +0.3 | V |
| | $SMV_{SS1,2}$ | $V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=MTV_{SS}=SMV_{SS}$ | | -0.3 to +0.3 | V |
| | $AV_{SS}$ | $V_{SS}=EV_{SS}=BV_{SS}=AV_{SS}=MTV_{SS}=SMV_{SS}$ | | -0.3 to +0.3 | V |
| Input voltage | $V_{I1}$ | P00-P06, P10-P11, P30-P39, P40-P42, P50-P55, P90-P96, P910-P915, $\overline{\text{RESET}}$, FLMD0 | | -0.3 to $EV_{DD}$+0.3[a] | V |
| | $V_{I2}$ | PCM2-PCM3, PCS0-PCS1, PCT0, PCT1, PCT4, PCT6, PDL0-PDL13 | | -0.3 to $BV_{DD}$+0.3[a] | V |
| | $V_{I3}$ | X1, X2, XT1, XT2 | | -0.3 to $V_{RO}$[b]+0.3[a] | V |
| | $V_{I4}$ | PMT00-PMT03, PMT30-PMT35, PMT40-PMT43, $\overline{\text{MTRESET}}$ | | -0.3 to $MTV_{DD}$+0.3[a] | V |
| Analog input voltage | $V_{IAN}$ | P70-P715 | | -0.3 to $AV_{REF0}$+0.3[a] | V |
| High level output current | $I_{OH}$ | P00-P06, P10-P11, P30-P39, P40-P42, P50-P55, P90-P96, P910-P915 | 1 pin | -4 | mA |
| | | | Total | -50 | mA |
| | | P70-715 | 1 pin | -4 | mA |
| | | | Total | -20 | mA |
| | | PCM2-PCM3, PCS0-PCS1, PCT0, PCT1, PCT4, PCT6, PDL0-PDL13, MTCS | 1 pin | -4 | mA |
| | | | Total | -50 | mA |
| | | PMT10-PMT17 | 1 pin | -45 | mA |
| | | | Total | -135 | mA |
| | | PMT20-PMT27 | 1 pin | -45 | mA |
| | | | Total | -135 | mA |
| | | SM11-SM14, SM21-SM24 | 1 pin | -45 | mA |
| | | | Total | -135 | mA |
| | | PMT00-PMT03, PMT30-PMT35, PMT40-PMT43 | 1 pin | -4 | mA |
| | | | Total | -15 | mA |

| Parameter | Symbol | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Low level output current | $I_{OL}$ | P00-P06, P10-P11, P30-P39, P40-P42, P50-P55, P90-P96, P910-P915 | 1 pin | 4 | mA |
| | | | Total | 50 | mA |
| | | P70-P715 | 1 pin | 4 | mA |
| | | | Total | 20 | mA |
| | | PCM2-PCM3, PCS0-PCS1, PCT0, PCT1,PCT4, PCT6, PDL0-PDL13, MTCS | 1 pin | 4 | mA |
| | | | Total | 50 | mA |
| | | PMT10-PMT17 | 1 pin | 45 | mA |
| | | | Total | 135 | mA |
| | | SM11-SM14, SM21-SM24 | 1 pin | 45 | mA |
| | | | Total | 135 | mA |
| | | PMT00-PMT03, PMT30-PMT35, PMT40-PMT43 | 1 pin | 4 | mA |
| | | | Total | 30 | mA |
| Operating ambient temperature | $T_A$ | Normal operating mode | | -40 to +85 | °C |
| | | Flash programming mode | | -40 to +85 | |
| Storage temperature | $T_{STG}$ | | | -40 to +125 | |

a. Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.
b. $V_{RO}$ is the on-chip regulator output voltage (typ. 2.5 V)

**Cautions: 1. Avoid direct connections among the IC device output (or I/O) pins and between $V_{DD}$ or $V_{CC}$ and GND.**

**2. All $V_{DD}$ pins have to be connected externally.**

**3. All $V_{SS}$ pins have to be connected externally.**

**4. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**5. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.**

**Remark:** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

## 9.2 Capacitance

($T_A$=25°C,
$V_{DD}$=$EV_{DD}$=$BV_{DD}$=$AV_{REF0}$=$MTV_{DD}$=$SMV_{DD}$=$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$AV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input capacitance | $C_I$ | f=1 MHz, Other than unmeasured pins:0 V | | | 15 | pF |
| Input / Output capacitance | $C_{IO}$ | f=1 MHz, Other than unmeasured pins:0 V<br>PMT00-PMT03, PMT30-PMT37,<br>PMT40-PMT43 | | | 15 | pF |
| Output capacitance | $C_O$ | f=1 MHz, Other than unmeasured pins:0 V<br>Other than following pins | | | 15 | pF |
| | $C_{SMO}$ | f=1 MHz, Other than unmeasured pins:0 V<br>PMT10-PMT17, PMT20-PMT27,<br>SM11-SM14, SM21-SM24 | | | 40 | pF |

## 9.3 Operation Conditions

($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=4.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$=0 V,
$T_A$=-40 to +85°C

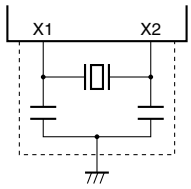
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Internal system clock frequency | $f_{CLK}$ | $V_{DD}$=5 V ± 10%<br>PLL mode (OSC=4 MHz to 5 MHz) | 16 | | 20 | MHz |
| | | $V_{DD}$ = 4.0 to 5.5 V<br>PLL mode (OSC=4 MHz) | 16 | 16 | 16 | MHz |
| | | $V_{DD}$= 4.0 to 5.5 V<br>Through-rate mode (OSC=4 MHz to 5 MHz) | 4 | | 5 | MHz |
| | | $V_{DD}$= 4.0 to 5.5 V<br>Sub-IDLE mode (Crystal)[a] | 32 | | 35 | KHz |
| | | REGC Capacity = 4.7 µF, at operation with subclock (RC resonator) | 12.5 | | 27.5 | KHz |

a. Be sure not to access peripheral, even if switched sub operation mode one time, before go sub-IDLE mode.

## 9.4 Oscillation Circuits

### 9.4.1 Main System Clock Oscillation Circuit Characteristics

($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=4.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$ =0 V,
$T_A$=-40 to +85°C)

| Resonator | Recommended circuit | Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Crystal/ Ceramic resonator |  | Oscillation frequency | | 4 | | 5 | MHz |
| | | Oscillation stabilization time[a] | After reset is released | | $2^{16}/f_X$ | | s |
| | | | After STOP mode is released | 0.5[b] | c | | ms |
| | | | After IDLE2 mode is released | 350[b] | c | | µs |

a. Time required from when $V_{DD}$ reaches oscillation voltage range (MIN.: 4.0 V) to when the crystal resonator stabilizes.
b. Stabilization time for Flash macro. Setting by OSTS resistor.
c. Depend on the setting of the oscillation stabilization time select resistor (OSTS).

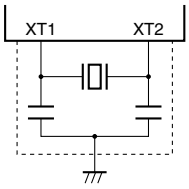
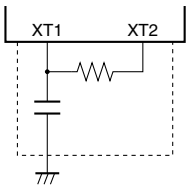
**Cautions: 1. When using the main clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.**

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as $V_{SS}$.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

**2. When the main clock is stopped and the device is operating on the subclock, wait until the oscillation stabilization time has been secured by the program before switching back to the main clock.**

### 9.4.2 Sub System Clock Oscillation Circuit Characteristics

($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=4.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$ =0 V,
$T_A$=-40 to +85°C)

| Resonator | Recommended circuit | Pyaarameter | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Crystal resonator |  | Oscillation frequency ($f_{XT}$) | | 32 | 32.768 | 35 | KHz |
| | | Oscillation stabilization time[a] | | | | 10 | μs |
| RC resonator |  | Oscillation frequency ($f_{XT}$) | R = 390 kΩ ±5%[b]<br>C = 47 pF ±10%[b] | 25 | 40 | 55 | KHz |
| | | Oscillation stabilization time[a] | | | | 100 | μs |

a. Time required from when $V_{DD}$ reaches oscillation voltage range (MIN.= 4.0 V) to when the crystal resonator stabilizes.
b. In order to avoid the influence of wiring capacity, shorten wiring as much as possible.

**Cautions: 1. When using the subclock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.**

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as $V_{SS}$.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

**2. The subclock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main clock oscillator. Particular care is therefore required with the wiring method when the subclock is used.**

### 9.4.3 MTRC Ring Oscillator Oscillation Circuit Characteristics

($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=4.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$ =0 V,
$T_A$=-40 to +85°C)

| Resonator | Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Ring Oscillator | Oscillation frequency ($f_{XR}$)[a] | | 6.8[b] | 8 | 9.2 | MHz |
| | Oscillation stabilization time[c] | | | | 20 | µs |
| calibration pulse | Calibration high pulse[d] | | | 14 | | µs |
| | calibration low pulse | | 3 | | | µs |
| MTCS | High-Level width | | 600 | | | ns |
| | Low-Level width | | 600 | | | ns |
| | analog delay for noise suppression | | 71 | 192 | | ns |

a. if calibration routine was successfully performed
b. 4 MHz if uncalibrated
c. time required when MRON bit is set from "0" to "1"
d. has to be exact the typ. value

### 9.4.4 PLL Characteristics

($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=4.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$ =0 V,
$T_A$=-40 to +85°C)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input frequency | $f_x$ | | 4 | | 5 | MHz |
| Output frequency | $f_{xx}$ | | 16 | | 20 | MHz |
| Clock time | $t_{PLL}$ | After $V_{DD}$ reaches MIN.: 3.5 V | | | 800 | µs |

### 9.4.5 µPD70F3235(A) V850FG2 Ring-OSC Characteristics

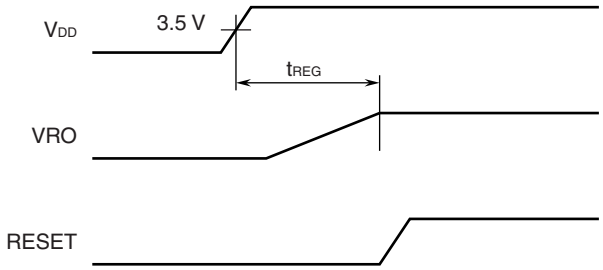
($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=4.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$ =0 V,
$T_A$=-40 to +85°C)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Output frequency | $f_r$ | | 100 | 200 | 400 | KHz |

## 9.5 Voltage Regulator Characteristics

($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=4.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$ =0 V,
$T_A$=-40 to +85°C)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input voltage | $V_{DD}$ | | 3.5 | | 5.5 | V |
| Output voltage | $V_{RO}$ | | | 2.5 | | V |
| Lock time | $t_{REG}$ | After $V_{DD}$ reaches MIN.: 3.5 V<br>Connect C = 4.7 µF ± 20% to REGC pin | | | 1 | ms |



## 9.6 DC Characteristics

### 9.6.1 Input/Output Level

($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=4.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$=0 V,
$T_A$=-40 to +85°C)

| Parameter | Symbol | Conditions | | MIN. | TYP | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| Input voltage, high | $V_{IH1}$ | P30, P34, P36-P38, P41, P911 | | 0.7 $EV_{DD}$ | | $EV_{DD}$ | V |
| | $V_{IH2}$ | P00-P06, P10-P11, P31-P33, P35, P39, P40, P42, P50-P55, P90-P96, P910, P912-P915 | | 0.8 $EV_{DD}$ | | $EV_{DD}$ | V |
| | $V_{IH3}$ | PCM2-PCM3, PCS0-PCS1, PCT0, PCT1, PCT4, PCT6, PDL0-PDL13 | | 0.7 $BV_{DD}$ | | $BV_{DD}$ | V |
| | $V_{IH4}$ | P70-P715 | | 0.7 $AV_{REF0}$ | | $AV_{REF0}$ | V |
| | $V_{IH5}$ | $\overline{RESET}$, FLMD0 | | 0.8 $EV_{DD}$ | | $EV_{DD}$ | V |
| | $V_{IH6}$ | PMT40, $\overline{MTRESET}$ | | 0.8 $MTV_{DD}$ | | $MTV_{DD}$ | V |
| | $V_{IH7}$ | PMT00-PMT03, PMT30-PMT35, PMT41-PMT43 | | 0.7 $MTV_{DD}$ | | $MTV_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | P30, P34, P36-P38, P41, P98, P911 | | $EV_{SS}$ | | 0.3 $EV_{DD}$ | V |
| | $V_{IL2}$ | P00-P06, P10-P11, P31-P33, P35, P39, P40, P42, P50-P55, P90-P96, P910, P912-P915 | | $EV_{SS}$ | | 0.2 $EV_{DD}$ | V |
| | $V_{IL3}$ | PCM2-PCM3, PCS0-PCS1, PCT0, PCT1, PCT4, PCT6, PDL0-PDL13 | | $BV_{SS}$ | | 0.3 $BV_{DD}$ | V |
| | $V_{IL4}$ | P70-P715 | | $AV_{SS}$ | | 0.3 $AV_{REF0}$ | V |
| | $V_{IL5}$ | $\overline{RESET}$, FLMD0 | | $EV_{SS}$ | | 0.2 $EV_{DD}$ | V |
| | $V_{IL6}$ | PMT40, $\overline{MTRESET}$ | | $MTV_{SS}$ | | 0.2 $MTV_{DD}$ | V |
| | $V_{IL7}$ | PMT00-PMT03, PMT30-PMT35, PMT41-PMT43 | | $MTV_{SS}$ | | 0.3 $MTV_{DD}$ | V |
| Output voltage, high | $V_{OH1}$[a] | P00-P06, P10-P11, P30-P39, P40-P42, P50-P55, P90-P96, P910-P915 | $I_{OH}$=-1.0 mA | $EV_{DD}$-1.0 | | $EV_{DD}$ | V |
| | | | $I_{OH}$=-100 µA | $EV_{DD}$-0.5 | | $EV_{DD}$ | V |
| | $V_{OH2}$[a] | PCM0-PCM3, PCS0-PCS1, PCT0, PCT1, PCT4, PCT6, PDL0-PDL13 | $I_{OH}$=-1.0 mA | $BV_{DD}$-1.0 | | $BV_{DD}$ | V |
| | | | $I_{OH}$=-100 µA | $BV_{DD}$-0.5 | | $BV_{DD}$ | V |
| | $V_{OH3}$[b] | P70-P715 | $I_{OH}$=-1.0 mA | $AV_{REF0}$ -1.0 | | $AV_{REF0}$ | V |
| | | | $I_{OH}$=-100 µA | $AV_{REF0}$ -0.5 | | $AV_{REF0}$ | V |
| Output voltage, high | $V_{OH4}$[c] | PMT10-PMT17, PMT20-PMT27, SM11-SM14, SM21-SM24 | $I_{OH}$=-27 mA ($T_A$=85°C)<br>$I_{OH}$=-30 mA ($T_A$=25°C)<br>$I_{OH}$=-40 mA ($T_A$=-40°C) | $SMV_{DD}$-0.07 | | $SMV_{DD}$ - 0.7 | V |
| | | | $I_{OH}$=-19 mA ($T_A$=85°C)<br>$I_{OH}$=-21 mA ($T_A$=25°C)<br>$I_{OH}$=-28 mA ($T_A$=-40°C) | $SMV_{DD}$-0.5 | | $SMV_{DD}$ - 0.7 | V |
| | $V_{OH5}$[d] | PMT00-PMT03, PMT30-PMT35, PMT40-PMT43 | $I_{OH}$=-1.0 mA | $MTV_{DD}$-1.0 | | $MTV_{DD}$ | V |

| Parameter | Symbol | Conditions | | MIN. | TYP | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output voltage, low | $V_{OL1}$[e] | P00-P06, P10-P11, P30-P39, P40-P42, P50-P55, P90-P96, P910-P915 | $I_{OL}$=1.0 mA | 0 | | 0.4 | V |
| | $V_{OL2}$[e] | PCM0-PCM3, PCS0-PCS1, PCT0, PCT1, PCT4, PCT6, PDL0-PDL13 | | | | | |
| | $V_{OL3}$[f] | P70-P715 | | | | | |
| | $V_{OL4}$[g] | PMT10-PMT17, PMT20-PMT27, SM11-SM14, SM21-SM24 | $I_{OL}$=27 mA ($T_A$=85°C)<br>$I_{OL}$=30 mA ($T_A$=25°C)<br>$I_{OL}$=40 mA ($T_A$=-40°C) | 0.07 | | 0.7 | V |
| | | | $I_{OH}$=19 mA ($T_A$=85°C)<br>$I_{OH}$=21 mA ($T_A$=25°C)<br>$I_{OH}$=28 mA ($T_A$=-40°C) | 0.07 | | 0.5 | V |
| | $V_{OL5}$[h] | PMT00-PMT03, PMT30-PMT35, PMT40-PMT43 | $I_{OL}$=1.0 mA | 0 | | 0.4 | V |
| Pull-up resistor | R1 | $V_I$=0 V | | 10 | 30 | 100 | KΩ |
| Pull-down resistor[i] | R2 | $V_I$=$V_{DD}$ | | 10 | 30 | 100 | KΩ |

a. Total $I_{OH}$ (Max.) is -20 mA
b. $I_{OL}$ max of $V_{OL3}$ is -16 mA.
c. $I_{OH}$ max of $V_{OH4}$ is -135 mA.
d. $I_{OH}$ max of $V_{OH5}$ is -12 mA.
e. $I_{OL}$ max of $V_{OL3}$ is 20 mA.
f. $I_{OL}$ max of $V_{OL3}$ is 16 mA.
g. $I_{OL}$ max of $V_{OL4}$ is 135 mA.
h. $I_{OL}$ max of $V_{OL5}$ is 12 mA
i. Exists only at $\overline{DRST}$ pin

### 9.6.2 Pin Leak Current

($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=4.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$=0 V,
$T_A$=-40 to +85°C)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input leakage current, high | $I_{LIH1}$ | $V_{IN}$ = $V_{DD}$ | Analog pins | | | +0.2 | μA |
| | | | Except the above | | | +0.5 | |
| Input leakage current, low | $I_{LIL1}$ | $V_{IN}$ = 0 V | Analog pins | | | −0.2 | μA |
| | | | Except the above | | | −0.5 | |
| Output leakage current, high | $I_{LOH1}$ | $V_O$ = $V_{DD}$ | Analog pins | | | +0.2 | μA |
| | | | Except the above | | | +0.5 | |
| Output leakage current, low | $I_{LOL1}$ | $V_O$ = 0 V | Analog pins | | | −0.2 | μA |
| | | | Except the above | | | −0.5 | |

**Caution: In flash memory versions, spec of FLMD0 pin is as follows.:**

- **Input leakage current, high: 2 μA**
- **Input leakage current, low: 2 μA**

### 9.6.3 Power Supply Current

($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=4.0 to 5.5 V
$AV_{REF0}$=4.0 to 5.5 V
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$=0 V
$T_A$=-40 to +85°C)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Supply current[a] | IDD1 | Operating mode | $f_{XX}$=20 MHz (OSC=5 MHz)<br>MTRC-Ring Oscillator On | | 32.5 | 50 | mA |
| | | | All peripherals stopped<br>MTRC-Ring Oscillator On | | 22 | | mA |
| | IDD2 | HALT mode | $f_{XX}$=20 MHz (OSC=5 MHz)<br>MTRC-Ring Oscillator On | | 20.5 | 33 | mA |
| | | | All peripherals stopped<br>MTRC-Ring Oscillator On | | 11 | | mA |
| | IDD3 | IDLE1 mode | $f_{XX}$=5 MHz (OSC=5 MHz)<br>PLL Off<br>MTRC-Ring Oscillator Off | | 0.6 | 0.92 | mA |
| | IDD4 | IDLE2 mode | $f_{XX}$=5 MHz (OSC=5 MHz)<br>PLL Off<br>MTRC-Ring Oscillator Off | | 0.25 | 0.72 | mA |
| | IDD5 | Sub Operation mode[b] | Crystal resonator<br>$f_{XT}$=32.768 KHz<br>RC resonator[c]<br>$f_{XT}$=40 KHz<br>MTRC-Ring Oscillator Off | | 200 | 420 | µA |
| | IDD6 | Sub IDLE mode[d] | Crystal resonator<br>$f_{XT}$=32.768 KHz<br>MTRC-Ring Oscillator Off | | 20 | 140 | µA |
| | | | RC resonator[c]<br>$f_{XT}$=40 KHz<br>MTRC-Ring Oscillator Off | | 35 | 160 | µA |
| | IDD7 | STOP mode[e] | Ring Oscillator On<br>MTRC-Ring Oscillator Off | | 15 | 85 | µA |
| | | | Ring Oscillator Off<br>MTRC-Ring Oscillator Off | | 7 | 70 | µA |

a. $V_{DD}$, $EV_{DD}$, $BV_{DD}$ and $MTV_{DD}$ total current. $AV_{REF0}$ and $SMV_{DD}$ current, port buffer current (including a current flowing in the on-chip pull-up/pull-down resistors) are not included.
b. Main Oscillator is off and Ring Oscillator is on.
c. RC Oscillator frequency is typ.40 KHz. This clock is divided (1/2) internally.
d. Main Oscillator is off.
e. Main Oscillator is off and Sub Oscillator is not used.

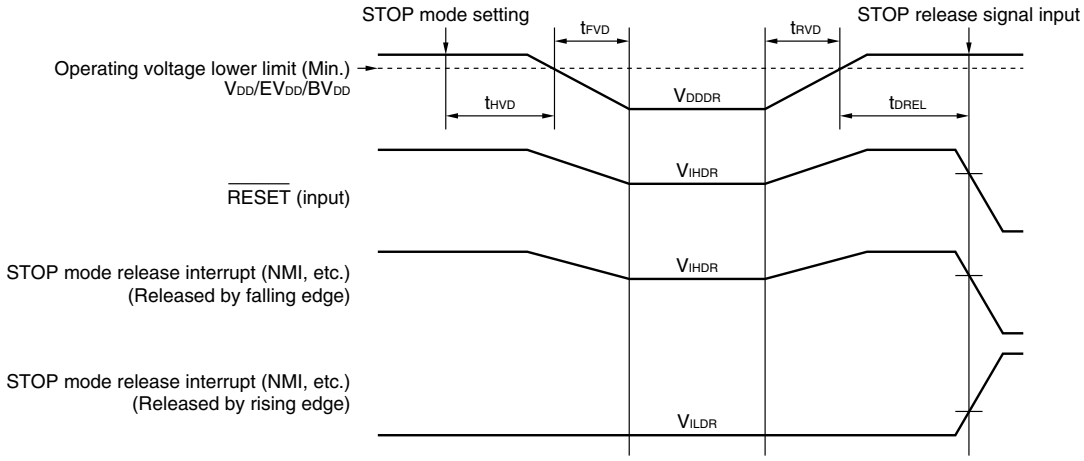
### 9.6.4 Data Retention Characteristics

($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=2.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$=0 V,
$T_A$=-40 to +85°C)

***Table 9-1: Data Retention Characteristics***

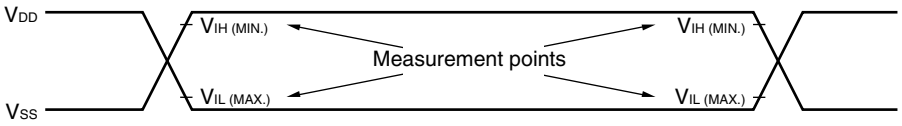
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention voltage | $V_{DDDR}$ | In STOP mode | 1.9 | | 5.5 | V |
| Data retention current | $I_{DDDR}$ | $V_{DDDR}$ = 2.0 V | | 6 | 65 | μA |
| Supply voltage rise time | $t_{RVD}$ | | 1 | | | μs |
| Supply voltage fall time | $t_{FVD}$ | | 1 | | | μs |
| Supply voltage retention time | $t_{HVD}$ | After STOP mode release | 0 | | | ms |
| STOP release signal input time | $t_{DREL}$ | After $V_{DD}$ reaches MIN.: 3.5 V | 0 | | | μs |
| Data retention input voltage, high | $V_{IHDR}$ | All input ports | 0.9$V_{DDDR}$ | | $V_{DDDR}$ | V |
| Data retention input voltage, low | $V_{ILDR}$ | All input ports | 0 | | 0.1$V_{DDDR}$ | V |

**Caution: Shifting to STOP mode and restoring from STOP mode must be performed within the rated operating range.**

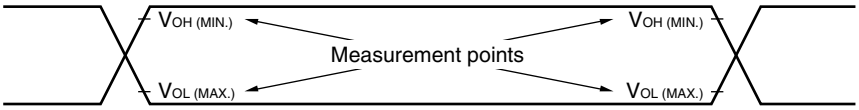


## 9.7 AC Characteristics

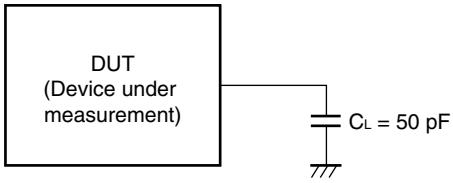
**AC Test Input Measurement Points ($V_{DD}$, $AV_{DD}$, $EV_{DD}$, $BV_{DD}$, $MTV_{DD}$, $MTV_{DD}$),**




**AC Test Output Measurement Points**




**Load Conditions**



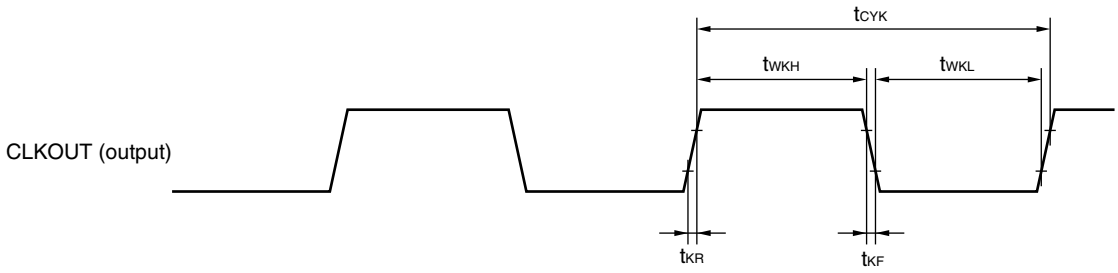

**Caution: If the load capacitance exceeds 50 pF due to the circuit configuration, bring the load capacitance of the device to 50 pF or less by inserting a buffer or by some other means.**

### 9.7.1 EXCLO output timing

($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=4.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$=0 V,
$T_A$=-40 to +85°C, $C_L$=50 pF)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| Output cycle | $t_{CYK}$ | | 62.5 ns | 8 μs | |
| High level width | $t_{WKH}$ | | $t_{CYK}$/2 - 15 | | ns |
| Low level width | $t_{WKL}$ | | $t_{CYK}$/2 - 15 | | ns |
| Rising time | $t_{KR}$ | | | 15 | ns |
| Falling time | $t_{KF}$ | | | 15 | ns |

**Clock Timing**



### 9.7.2 $\overline{\text{RESET}}$, Interrupt, FLMD0 timing

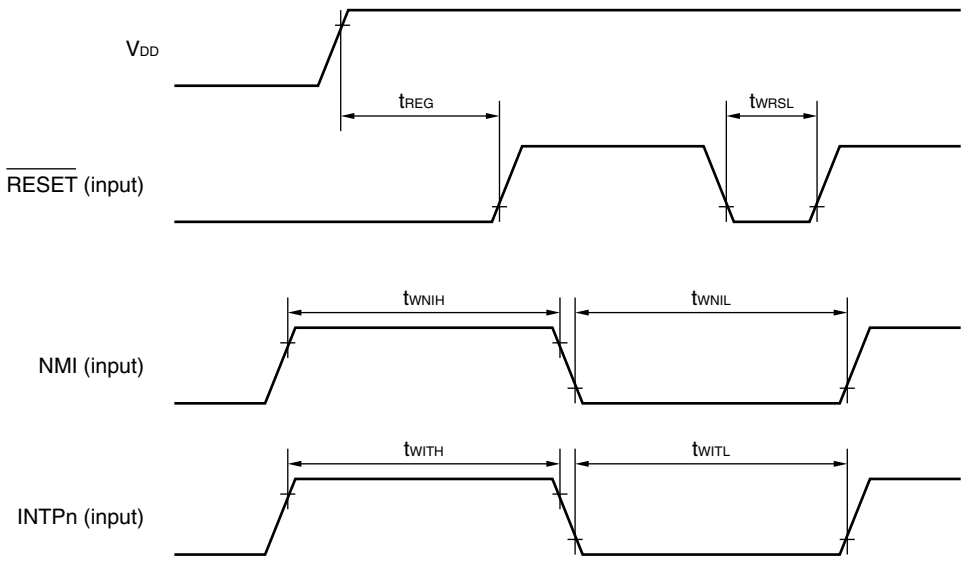
($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=4.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$=0 V,
$T_A$=-40 to +85°C, $C_L$=50 pF)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| $\overline{\text{MTRESET}}$ input low level width | $t_{WMRSL}$ | | 500 | | ns |

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| RESET low-level width | $t_{WRSL}$ | | 500 | | ns |
| NMI high-level width | $t_{WNIH}$ | Analog noise elimination | 500 | | ns |
| NMI low-level width | $t_{WNIL}$ | Analog noise elimination | 500 | | ns |
| INTPn high-level width[a] | $t_{WITH}$ | Analog noise elimination (n = 0 to 7) | 500 | | ns |
| | | Digital noise elimination (n = 3) | [b] | | ns |
| INTPn low-level width[a] | $t_{WITL}$ | Analog noise elimination (n = 0 to 7) | 500 | | ns |
| | | Digital noise elimination (n = 3) | [b] | | ns |

a. ADTRG is same spec (P03/INTP0/ADTRG). DRST is same spec (P05/INTP2/DRST).
b. 2Tsamp + 20 or 3Tsamp + 20

**Reset/Interrupt**

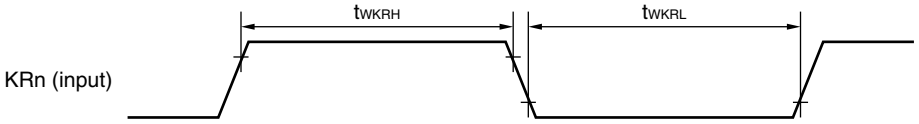



**Remark:** n = 0 to 7

### 9.7.3 Key Return timing

($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=4.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$=0 V,
$T_A$=-40 to +85°C, $C_L$=50 pF)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| KRn input high-level width | $t_{WKRH}$ | Analog noise elimination (n = 0 to 7) | 500 | | ns |
| KRn input low-level width | $t_{WKRL}$ | | 500 | | ns |



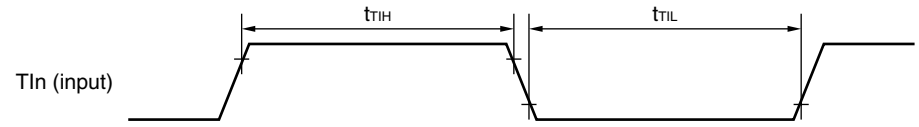

**Remark:** n = 0 to 7

### 9.7.4 Timer Input timing

($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=4.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$=0 V,
$T_A$=-40 to +85°C, $C_L$=50 pF)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| TIn high-level width | $t_{TIH}$ | TIP00, TIP01, TIP10, TIP11, TIP20, TIP21, TIP30, TIP31, TIQ00 to TIQ03, TIQ10 to TIQ13 | Note | | ns |
| TIn low-level width | $t_{TIL}$ | | Note | | ns |

**Note:** 2Tsamp + 20 or 3Tsamp + 20
Tsamp: Sampling clock for noise elimination



### 9.7.5 CSI timing

#### (1) CSIB0

##### (a) Master Mode

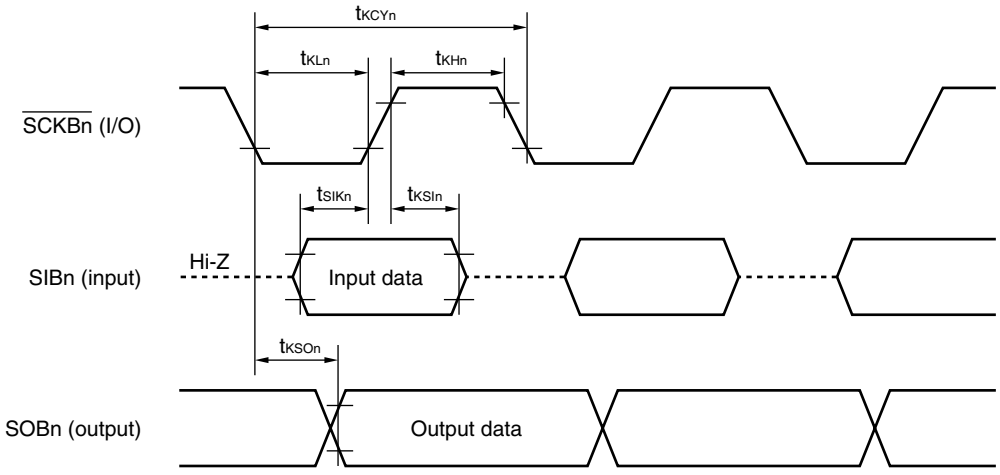
($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=4.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$=0 V,
$T_A$=-40 to +85°C, $C_L$=50 pF)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| $\overline{SCKB0}$ cycle time | $t_{KCY0}$ | | 125 | | ns |
| $\overline{SCKB0}$ high level width | $t_{KH0}$ | | $t_{KCY0}$/2-15 | | ns |
| $\overline{SCKB0}$ low level width | $t_{KL0}$ | | $t_{KCY0}$/2-15 | | ns |
| SIB0 setup time (to $\overline{SCKB0}$) | $t_{SIK0}$ | | 30 | | ns |
| SIB0 hold time (from $\overline{SCKB0}$) | $t_{KSI0}$ | | 25 | | ns |
| $\overline{SCKB0}$ to SOB0 output delay time | $t_{KSO0}$ | | | 25 | ns |

##### (b) Slave Mode

($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=4.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$=0 V,
$T_A$=-40 to +85°C, $C_L$=50 pF)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| $\overline{SCKB0}$ cycle time | $t_{KCY0}$ | | 200 | | ns |
| $\overline{SCKB0}$ high level width | $t_{KH0}$ | | 90 | | ns |
| $\overline{SCKB0}$ low level width | $t_{KL0}$ | | 90 | | ns |
| SIB0 setup time (to $\overline{SCKB0}$) | $t_{SIK0}$ | | 50 | | ns |
| SIB0 hold time (from $\overline{SCKB0}$) | $t_{KSI0}$ | | 50 | | ns |
| $\overline{SCKB0}$ to SOB0 output delay time | $t_{KSO0}$ | | | 50 | ns |



**(2) CSIB1**

CSIB1 can be only used in Master Mode.

**(a) Master Mode**

($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=4.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$=0 V,
$T_A$=-40 to +85°C, $C_L$=50 pF)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| $\overline{EXSCK1}$ cycle time | $t_{KCY1}$ | | 250/1000[a] | | ns |
| $\overline{EXSCK1}$ high level width | $t_{KH1}$ | | $t_{KCY1}$/2 - 30 | | ns |
| $\overline{EXSCK1}$ low level width | $t_{KL1}$ | | $t_{KCY1}$/2 - 30 | | ns |
| EXSI1 setup time (to $\overline{EXSCK1}$) | $t_{SIK1}$ | | 50 | | ns |
| EXSI1 hold time (from $\overline{EXSCK1}$) | $t_{KSI1}$ | | 50 | | ns |
| $\overline{EXSCK1}$ to EXSO1 output delay time | $t_{KSO1}$ | | | 50 | ns |

a. Be sure to set cycle time ($\overline{EXSCK1}$) over 4 times as the internal system clock cycle ($1/f_{CLK}$). $t_{KCY1} \geq 1/f_{CLK} \times 4$
If the CSI1 communicate with the uncalibrated MTRC ($f_{RO\_uncal}$ min. 4 MHz) $t_{KCY1}$ has to be ≥ 1000 ns

### 9.7.6 UART timing

($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=4.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$=0 V,
$T_A$=-40 to +85°C, $C_L$=50 pF)

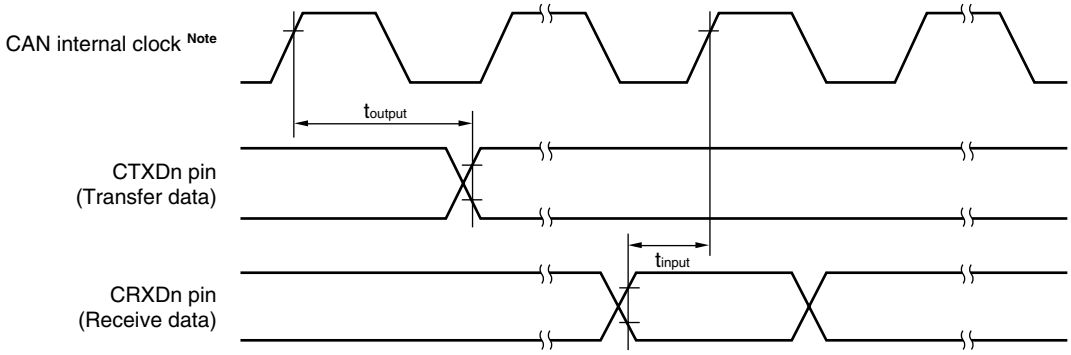
| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| Communication rate | | | | 312.5 | kbps |
| ASCK0 cycle time | | | | 10 | MHz |

### 9.7.7 CAN timing

($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=4.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$=0 V,
$T_A$=-40 to +85°C, $C_L$=50 pF)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| Transfer rate | | | | 1 | Mbps |
| Internal delay time[a] | | | | 100 | ns |

a. Internal delay time ($t_{NODE}$) = Internal transfer delay time ($t_{OUTPUT}$) + Internal receive delay time ($t_{INPUT}$).




**Note:** CAN internal clock (fCAN): CAN baud rate clock

**Remark:** n = 0, 1

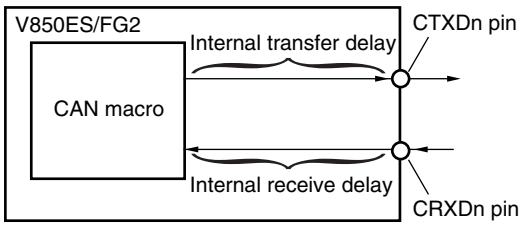



Image figure of internal delay

### 9.7.8 AD Converter

($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=4.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$=0 V,
$T_A$=-40 to +85°C, $C_L$=50 pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Resolution | | | | | 10 | bit |
| Overall error[a] | | 4.0 ≤ $AV_{REF0}$ ≤ 5.5 V | | ±0.15 | ±0.45 | %FSR |
| Conversion time | $t_{CONV}$ | | 3.1 | | 16 | μs |
| Analog input voltage | $V_{IAN}$ | | $AV_{SS}$ | | $AV_{REF0}$ | V |
| $AV_{REF0}$ current | $I_{AREF0}$ | When using A/D converter | | 5 | 10 | mA |
| | | When not using A/D converter | | 1 | 10 | μA |

a. Excluding quantization error (±0.05%FSR). Indicates the ratio to the full-scale value (%FSR).

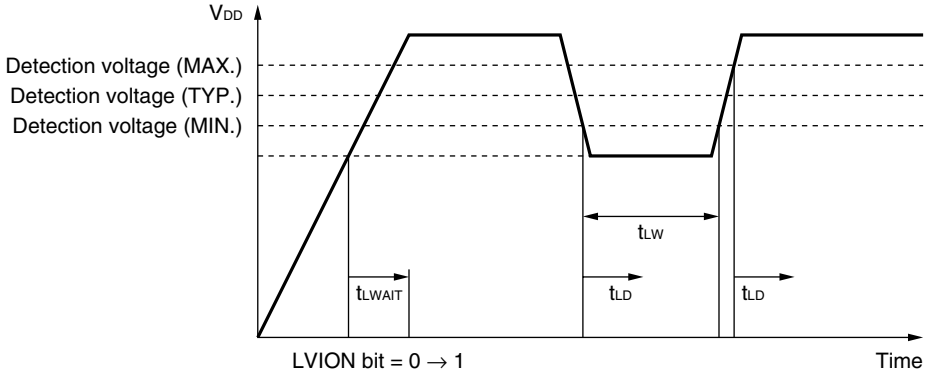
**Note:** FSR: Full Scale Range

### 9.7.9 LVI

($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=4.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$=0 V,
$T_A$=-40 to +85°C, $C_L$=50 pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection voltage | $V_{LVI0}$ | | 4.2 | 4.4 | 4.6 | V |
| | $V_{LVI1}$ | | 4.0 | 4.2 | 4.4 | V |
| Response time[a] | $t_{LD}$ | After $V_{DD}$ reaches $V_{LVI0}$/$V_{LVI1}$ (Max.). After $V_{DD}$ drops $V_{LVI0}$/$V_{LVI1}$ (Min.). | | 0.2 | 2.0 | ms |
| Minimum $V_{DD}$ width | $t_{LW}$ | | 0.2 | | | ms |
| Reference voltage stabilization wait time[b] | $t_{LWAIT}$ | After $V_{DD}$ reaches 3.5 V. After LVION bit (LVIM.bit7) = 0 →1 | | 0.1 | 0.2 | ms |

a. The time required to output an interrupt/reset after the detection voltage is detected.
b. Unnecessary when the POC function is used.

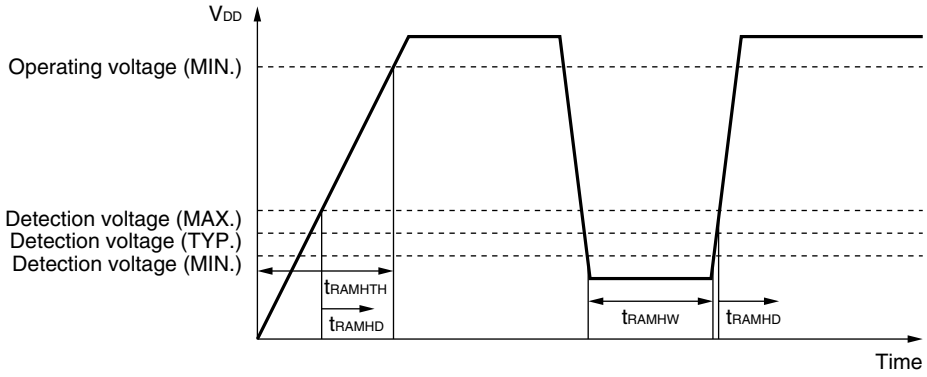


### 9.7.10 RAM retention flag

($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=4.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$=0 V,
$T_A$=-40 to +85°C, $C_L$=50 pF)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection voltage | $V_{RAMH}$ | | 1.9 | 2.0 | 2.1 | V |
| Supply voltage rise time | $t_{RAMHTH}$ | $V_{DD}$ = 0 V → 3.5 V | 0.002 | | 1,800 | ms |
| Response time[a] | $t_{RAMHD}$ | After the supply voltage reaches the detection voltage (MAX.) | | 0.2 | 2.0 | ms |
| Minimum $V_{DD}$ width | $t_{RAMHW}$ | | 0.2 | | | ms |

a. Time required to set the RAMF bit after the detection voltage is detected.



### 9.7.11 Flash Memory Programming characteristics

($V_{DD}$=$EV_{DD}$=$BV_{DD}$=$MTV_{DD}$=$SMV_{DD}$=$AV_{REF0}$=4.0 to 5.5 V,
$V_{SS}$=$EV_{SS}$=$BV_{SS}$=$MTV_{SS}$=$SMV_{SS}$=$AV_{SS}$=0 V,
$T_A$=-40 to +85°C, $C_L$=50 pF)

#### (1) Basic characteristics

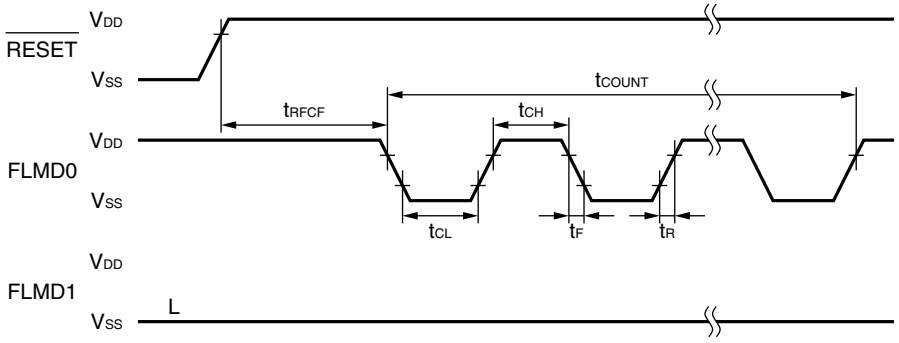
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Operating frequency | $f_{CPU}$ | | 4 | | 20 | MHz |
| Supply voltage | $V_{DD}$ | | 4.0 | | 5.5 | V |
| Number of writes | $C_{WRT}$[a] | | | | 100 | Times |
| Input voltage, high | $V_{IH}$ | FLMD0 | 0.8$EV_{DD}$ | | $EV_{DD}$ | V |
| Input voltage, low | $V_{IL}$ | FLMD0 | $EV_{SS}$ | | 0.2$EV_{DD}$ | V |
| Programming temperature | $t_{PRG}$ | | −40 | | +85 | °C |

a.The initial write when the product is shipped, any erase → write set of operations, or any programming operation is counted as one rewrite.

#### (2) Serial Write Operation Characteristics

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| FLMD0 setup time from RESET↑ | $t_{RFCF}$ | | 5000/$f_X$ + $\alpha$[a] | | | s |
| Count execution time | $t_{COUNT}$ | | | | 3 | ms |
| FLMD0 high-level width | $t_{CH}$ | | 10 | | 100 | μs |
| FLMD0 low-level width | $t_{CL}$ | | 10 | | 100 | μs |
| FLMD rise time | $t_R$ | | | | 50 | μs |
| FLMD fall time | $t_F$ | | | | 50 | μs |

a. $\alpha$ denotes the oscillation stabilization time

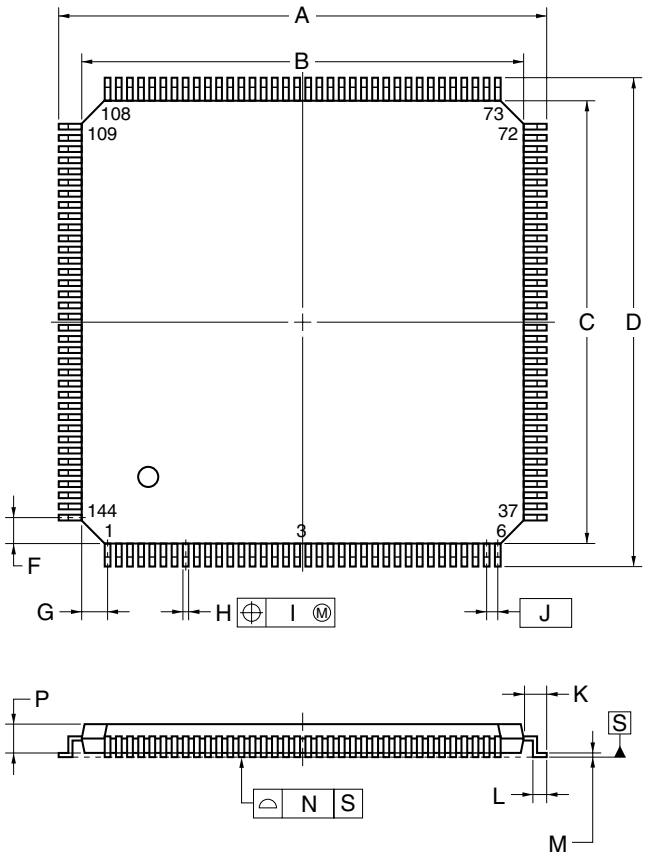


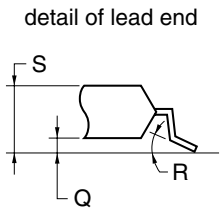
**[MEMO]**

# Chapter 10 Package Drawings

***Figure 10-1: V850ES/DJ2***

## 144-PIN PLASTIC LQFP (FINE PITCH) (20x20)




**NOTE**

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 22.0±0.2 |
| B | 20.0±0.2 |
| C | 20.0±0.2 |
| D | 22.0±0.2 |
| F | 1.25 |
| G | 1.25 |
| H | 0.22±0.05 |
| I | 0.08 |
| J | 0.5 (T.P.) |
| K | 1.0±0.2 |
| L | 0.5±0.2 |
| M | $0.17^{+0.03}_{0.07}$ |
| N | 0.08 |
| P | 1.4 |
| Q | 0.10±0.05 |
| R | $3^{\circ}{}^{+4^{\circ}}_{3^{\circ}}$ |
| S | 1.5±0.1 |

**S144GJ-50-UEN**

**[MEMO]**

# Chapter 11 Recommended Soldering Conditions

Solder this product under the following recommended conditions.
For details of the recommended soldering conditions, refer to information document Semiconductor Device:

**Mounting Technology Manual (C10535E).**

For soldering methods and conditions other than those recommended please consult NEC.

| Soldering Method | Soldering Condition | Symbol of Recommended Soldering Condition |
|---|---|---|
| Infrared reflow | Package peak temperature: 235°C | IR35-207-3 |
| Partial heating | 350°C | P350 |

**Caution: Do not use two or more soldering methods in combination (except partial heating method).**

**[MEMO]**

# Revision History

| Version | Date | Remarks |
|---|---|---|
| 1.1 | 2005/09/01 | Initial release |
| 1.2 | 2006/12/13 | Chapter 1.5.2: new description of internal and external communication via CSIB1 |
| | | Chapter 3.1: MTCS corrected to CS in MTRC pinout |
| | | Chapter 3.2: description of MTCS completed |
| | | Chapter 4.6.1: new caution: configuration of PMT34 to PMT37 |
| | | Chapter 4.6.2: new caution: configuration of PMT34 to PMT37 |
| | | Chapter 9.6.3: IDD3 condition corrected: PLL Off |

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