NEC

User's Manual

# V850E/PHO2 Traceability Data

## 32-bit Single-Chip Microcontroller

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## μPD70F3187
## μPD70F3447
## μPD76F0053

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## NOTES FOR CMOS DEVICES

**① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN).

**② HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

**③ PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

**④ STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

**⑤ POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

**⑥ INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

*For further information,*
*please contact:*


**NEC Electronics Corporation**
1753, Shimonumabe, Nakahara-ku,
Kawasaki, Kanagawa 211-8668,
Japan
Tel: 044-435-5111
http://www.necel.com/

**[America]**

**NEC Electronics America, Inc.**
2880 Scott Blvd.
Santa Clara, CA 95050-2554, U.S.A.
Tel: 408-588-6000
800-366-9782
http://www.am.necel.com/

**[Europe]**

**NEC Electronics (Europe) GmbH**
Arcadiastrasse 10
40472 Düsseldorf, Germany
Tel: 0211-65030
http://www.eu.necel.com/

**Hanover Office**
Podbielskistrasse 166 B
30177 Hannover
Tel: 0 511 33 40 2-0

**Munich Office**
Werner-Eckert-Strasse 9
81829 München
Tel: 0 89 92 10 03-0

**Stuttgart Office**
Industriestrasse 3
70565 Stuttgart
Tel: 0 711 99 01 0-0

**United Kingdom Branch**
Cygnus House, Sunrise Parkway
Linford Wood, Milton Keynes
MK14 6NP, U.K.
Tel: 01908-691-133

**Succursale Française**
9, rue Paul Dautier, B.P. 52180
78142 Velizy-Villacoublay Cédex
France
Tel: 01-3067-5800

**Sucursal en España**
Juan Esplandiu, 15
28007 Madrid, Spain
Tel: 091-504-2787

**Tyskland Filial**
Täby Centrum
Entrance S (7th floor)
18322 Täby, Sweden
Tel: 08 638 72 00

**Filiale Italiana**
Via Fabio Filzi, 25/A
20124 Milano, Italy
Tel: 02-667541

**Branch The Netherlands**
Steijgerweg 6
5616 HS Eindhoven
The Netherlands
Tel: 040 265 40 10

**[Asia & Oceania]**

**NEC Electronics (China) Co., Ltd**
7th Floor, Quantum Plaza, No. 27 ZhiChunLu Haidian
District, Beijing 100083, P.R.China
Tel: 010-8235-1155
http://www.cn.necel.com/

**NEC Electronics Shanghai Ltd.**
Room 2509-2510, Bank of China Tower,
200 Yincheng Road Central,
Pudong New Area, Shanghai P.R. China P.C:200120
Tel: 021-5888-5400
http://www.cn.necel.com/

**NEC Electronics Hong Kong Ltd.**
12/F., Cityplaza 4,
12 Taikoo Wan Road, Hong Kong
Tel: 2886-9318
http://www.hk.necel.com/

**Seoul Branch**
11F., Samik Lavied'or Bldg., 720-2,
Yeoksam-Dong, Kangnam-Ku,
Seoul, 135-080, Korea
Tel: 02-558-3737

**NEC Electronics Taiwan Ltd.**
7F, No. 363 Fu Shing North Road
Taipei, Taiwan, R. O. C.
Tel: 02-8175-9600
http://www.tw.necel.com/

**NEC Electronics Singapore Pte. Ltd.**
238A Thomson Road,
#12-08 Novena Square,
Singapore 307684
Tel: 6253-8311
http://www.sg.necel.com/


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# Introduction

**Readers**

This User's Manual is intended for users who want to understand the functionality of the V850E/PHO2 Traceability Data for devices µPD70F3187, µPD70F3447 and µPD76F0053 of the V850 core family.

**Purpose**

This User's Manual explains the background and handling of the V850E/PHO2 Traceability Data for devices µPD70F3187, µPD70F3447 and µPD76F0053 of the V850 core family.

**Organization**

This User's Manual contains the major sections:

- Description of the traceability data

**Legend**

Symbols and notation are used as follows:

| | | |
|---|---|---|
| Weight in data notation | : | Left is high-order column, right is low order column |
| Active low notation | : | $\overline{xxx}$ (pin or signal name is over-scored) or /xxx (slash before signal name) |
| Memory map address: | : | High order at high stage and low order at low stage |
| **Note** | : | Explanation of (Note) in the text |
| **Caution** | : | Information requiring particular attention |
| **Remark** | : | Supplementary explanation to the text |
| Numeric notation | : | Binary... xxxx or xxxB<br>Decimal... xxxx<br>Hexadecimal... xxxxH or 0x xxxx |

Prefixes representing powers of 2 (address space, memory capacity)

K (kilo): $2^{10} = 1024$

M (mega): $2^{20} = 1024^2 = 1,048,576$

G (giga): $2^{30} = 1024^3 = 1,073,741,824$

# Chapter 1 Overview

This Users Manual describes the format of traceability data to be used to identify and obtain device specific production data. This specification is applicable to V850E/PHO2 (µPD76F0053, µPD70F3187, µPD70F 3447).

## 1.1 Naming Conventions

Certain terms, required for the description of the traceability data are long and too complicated for good readability of the document. Therefore, special names and abbreviations will be used in the course of this document to improve the readability.

***Extra Area***

Extra Area is a separate area of the code flash that is used to store special parameter such as traceability data, trimming data etc. The access to the extra area is not granted by the application. Only a special library or the device internal firmware can read such area.

# Chapter 2 Traceability Data

The traceability data are stored at fixed addresses in the extra area of the device's flash memory.

***Figure 2-1: V850E/PHO2 Traceability Data***

| | bit31 | bit30 | bit29 | bit28 | bit27 | bit26 | bit25 | bit24 | bit23 | bit22 | bit21 | bit20 | bit19 | bit18 | bit17 | bit16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x432 | Product Code (4 last digits) | | | | | | | | | | | | | | | |

| | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x430 | Standard/Custom | 1 | Alphabet Code | | Product Version | | | | | | | | | | | |

| | bit31 | bit30 | bit29 | bit28 | bit27 | bit26 | bit25 | bit24 | bit23 | bit22 | bit21 | bit20 | bit19 | bit18 | bit17 | bit16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x422 | Plant Code | | | | Line No. | | | | Diffusion Lot No.(Year.) | | | | Diffusion Lot No.(Month. | | | |

| | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x420 | Diffusion Lot No.(4th dig.) | | | | Diffusion Lot No.(3rd dig | | | | Diffusion Lot No.(2nd dig | | | | Diffusion Lot No.(1st dig. | | | |

| | bit31 | bit30 | bit29 | bit28 | bit27 | bit26 | bit25 | bit24 | bit23 | bit22 | bit21 | bit20 | bit19 | bit18 | bit17 | bit16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x41A | Pass/Fail | | | | | | | | | | Wafer No. | | | | | |

| | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x418 | Y-Index | | | | | | | | X-Index | | | | | | | |

## 2.1 Description of the Traceability Data

### 2.1.1 X-Index

The value consist of an 8-bit value that locates the X axis of the location of the die on the wafer.

### 2.1.2 Y-Index

The value consist of an 8-bit value that locates the Y axis of the location of the die on the wafer.

### 2.1.3 Wafer No.

The value gives the wafer number as 6-bit value.

### 2.1.4 Pass/Fail

A single bit indicates whether the specific die passed or failed the production.
Pass is 1b, fail is 0b.

### 2.1.5 Diffusion Lot No.

The diffusion lot number consists of 6 groups of four bits each.
The lot number year and month consist of 4bits each having a range of 0...Fh each.
Example 09/2006 will result in 0609h.

### 2.1.6 Line number, Plant number

Give the diffusion line number of the specified production line and plant.
The diffusion line for PHO2 will be 1111b or Fh.
The plant number will be 1111b or Fh for NMS Kyushu plant.

### 2.1.7 Product version

The 12-bit wide value indicates the device version of the dedicated product.
The value is divided in three groups of four bits each.
E.g. V2.1.0 will be 0010 0001 0000b or 210h.
V2.2.0 will be 0010 0010 0000b or 220h.

### 2.1.8 Alphabet code

Defines the device suffix, e.g. V2.2 µPD76F0053A is 01b.

| Value | Definition |
|---|---|
| 00b | non |
| 01b | A |
| 10b | B |
| 11b | H |

### 2.1.9 Standard Custom marker

The single bit indicates if it is a customised or standard product.
Customised product will have a 0b, while standard products will have a 1b.

### 2.1.10 Product code (4 last digits)

The value is divided into four groups of three bits each.
E.g. uPD76F0053 will be 0000 0000 0101 0011b or 0053h.
uPD70F3187 will be 0011 0001 1000 0111b or 3187h.