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RENESAS

User's Manual

μPD98431

10/100 Mbps Ethernet™ Controller

Document No. S14054EJ4V0UM00 (4th edition)
Date Published July 2001 NS CP(K)

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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M8E 00.4

Major Revisions in This Edition

Page	Description
p.17	Modification of caution in **CHAPTER 2 (1) Register interface** HCLK.
	Modification of caution in **CHAPTER 2 (2) FIFO interface** FCLK.
p.23	Modification of description in **CHAPTER 2 (4) JTAG pins** TRST#.
p.29	Addition and modification of description in **3.4.1 (2) Appending CRC**.
p.30	Partial deletion of descriptions in **3.4.1 (3) Appending PAD**.
p.47	Modification of description in **3.7.1 (2) (b) SKIP signal**.
pp.63 to 64	**4.1 (1) Port control register map** Default value of the following registers modified. CLRT, MACC3, TIMR, RIMR, TSVREG1, TSVREG2, RSVREG, FSVREG
pp.66 to 93	**4.2 Port Setting Registers** Description of the following registers modified. MACC1, CAR1, CAR2, CAM1, MACC3, TSVREG1, TSVREG2, RSVREG, TFIC Bit name of the following register modified. MIIC Default value of the following bit modified. PTIME of the MACC3 register

The mark ★ shows major revised points.

INTRODUCTION

Target Users

This manual is intended for user engineers who wish to understand the functions of the μPD98431, and design and develop application systems using it.

Purpose

This manual explains the hardware functions of the μPD98431 in the following organization.

Organization

This manual consists of the following chapters.

- General
- Pin functions
- Functional description
- Register description
- Statistics counters
- JTAG boundary scan

How to Use This Manual

It is assumed that the readers of this manual have a general knowledge of electricity, logic circuits, and microcomputers.

To understand the overall functions of the μPD98431
→ Read this manual in the order of CONTENTS.

Conventions

Data significance	: Higher digits on the left and lower digits on the right
Active low	: XXX# (# following pin or signal name)
Memory map address	: Higher address on the top and lower address on the bottom
Note	: Footnote for item marked with **Note** in the text
Caution	: Information requiring particular attention
Remark	: Supplementary information
Numeric notation	: Binary ... XXXX or XXXXB Decimal ... XXXX Hexadecimal ... XXXXH

Prefix indicating power of 2 (address space and memory capacity):

K (kilo)	: $2^{10} = 1024$
M (mega)	: $2^{20} = 1024^2$
G (giga)	: $2^{30} = 1024^3$

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

- Data Sheet: S14150E

CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1 GENERAL

The μPD98431 is a 10/100 Mbps Ethernet controller having eight Media Access Control (MAC) ports conforming to IEEE 802.3 and IEEE 802.3u. Its main features are as follows:

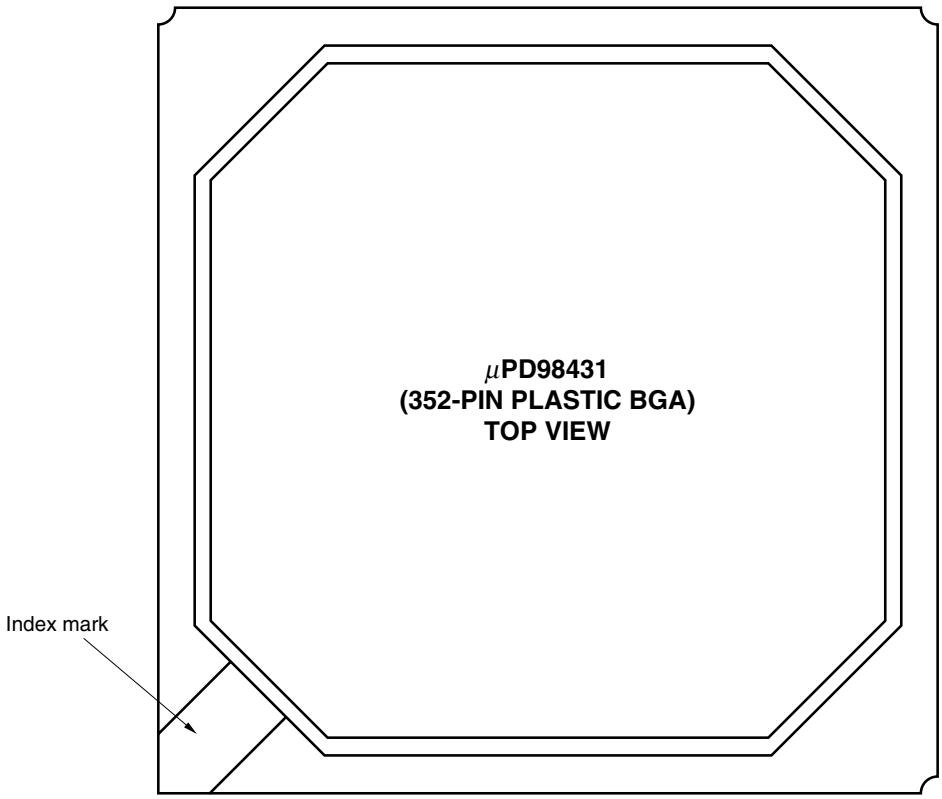
1.1 Features

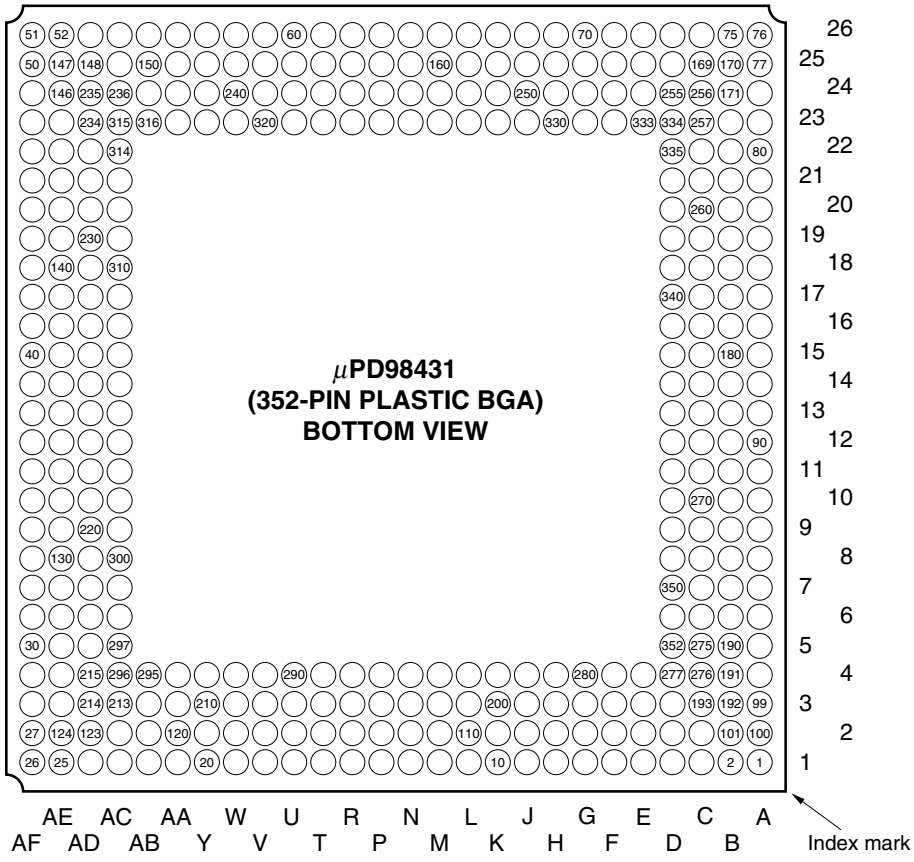
- Eight 10/100 Mbps Ethernet MAC ports conforming to IEEE 802.3 and IEEE 802.3u
- Supports MII and 10 Mbps serial interface as interface with physical layer devices
- Each port has 2K bytes of receive FIFO and 512 bytes of transmit FIFO.
- High-speed FIFO data bus interface of 32/64 bits × 66 MHz
- Full-duplex operation and IEEE 802.3x flow control
- Statistics counter supporting RMON/SNMP
- Filtering conditions can be set according to address type.
- VLAN frame detection function
- Mirror port function
- JTAG support
- Supply voltage: 3.3 V

1.2 Ordering Information

Part Number	Package
μPD98431S1-F6	352-pin plastic BGA (35 × 35)

1.3 Pin Configuration





(1/2)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1(A1)	TXFD30/FD62	51(AF26)	D28	101(B2)	TXFD27/FD59	151(AA25)	D16
2(B1)	TXFD29/FD61	52(AE26)	D27	102(C2)	TXFD28/FD60	152(Y25)	D13
3(C1)	TXFD26/FD58	53(AD26)	D24	103(D2)	TXFD24/FD56	153(W25)	D9
4(D1)	TXFD23/FD55	54(AC26)	D21	104(E2)	TXFD21/FD53	154(V25)	D6
5(E1)	TXFD20/FD52	55(AB26)	D18	105(F2)	TXFD18/FD50	155(U25)	D3
6(F1)	TXFD17/FD49	56(AA26)	D15	106(G2)	TXFD15/FD47	156(T25)	TXFBA7
7(G1)	TXFD14/FD46	57(Y26)	D12	107(H2)	TXFD11/FD43	157(R25)	TXFBA4
8(H1)	TXFD10/FD42	58(W26)	D8	108(J2)	TXFD8/FD40	158(P25)	TXFBA0
9(J1)	TXFD7/FD39	59(V26)	D5	109(K2)	TXFD5/FD37	159(N25)	TXFBA1
10(K1)	TXFD4/FD36	60(U26)	D2	110(L2)	TXFD1/FD33	160(M25)	TXFPT2
11(L1)	TXFD0/FD32	61(T26)	TXFBA6	111(M2)	RXFDQ1/FDQ1	161(L25)	TXFPT0
12(M1)	RXFDQ2/FDQ2	62(R26)	TXFBA3	112(N2)	FCLK	162(K25)	TXFDQ1
13(N1)	RXFD31/FD31	63(P26)	RXFPT2	113(P2)	RXFA	163(J25)	TXFEN#/FRW
14(P1)	RXFD30/FD30	64(N26)	RXFPT1	114(R2)	RXFD28/FD28	164(H25)	ACK#
15(R1)	RXFD29/FD29	65(M26)	RXFPT0	115(T2)	RXFD26/FD26	165(G25)	RW
16(T1)	RXFD27/FD27	66(L26)	TXFPT1	116(U2)	RXFD23/FD23	166(F25)	A8
17(U1)	RXFD24/FD24	67(K26)	TXFDQ2	117(V2)	RXFD20/FD20	167(E25)	A5
18(V1)	RXFD21/FD21	68(J26)	RXFEN#/FEN#	118(W2)	RXFD17/FD17	168(D25)	A3
19(W1)	RXFD18/FD18	69(H26)	SKIP	119(Y2)	RXFD13/FD13	169(C25)	TCK
20(Y1)	RXFD14/FD14	70(G26)	CS#	120(AA2)	RXFD10/FD10	170(B25)	TEST3
21(AA1)	RXFD11/FD11	71(F26)	A9	121(AB2)	RXFD7/FD7	171(B24)	MDIO
22(AB1)	RXFD8/FD8	72(E26)	A6	122(AC2)	RXFD5/FD5	172(B23)	TXER0
23(AC1)	RXFD4/FD4	73(D26)	A2	123(AD2)	RXFD1/FD1	173(B22)	TXD02
24(AD1)	RXFD0/FD0	74(C26)	TDO	124(AE2)	TXD43	174(B21)	TXCLK0
25(AE1)	TEST0	75(B26)	TRST#	125(AE3)	TXEN4	175(B20)	RXD03
26(AF1)	CRS4	76(A26)	TDI	126(AE4)	TXD40	176(B19)	RXD00
27(AF2)	TXER4	77(A25)	MDC	127(AE5)	RXDV4	177(B18)	CRS1
28(AF3)	TXD42	78(A24)	COL0	128(AE6)	RXD41	178(B17)	TXD12
29(AF4)	TXCLK4	79(A23)	TXEN0	129(AE7)	COL5	179(B16)	TXCLK1
30(AF5)	RXD43	80(A22)	TXD01	130(AE8)	TXEN5	180(B15)	RXD13
31(AF6)	RXD40	81(A21)	RXER0	131(AE9)	TXD51	181(B14)	RXCLK1
32(AF7)	CRS5	82(A20)	RXD02	132(AE10)	RXDV5	182(B13)	RXD10
33(AF8)	TXD53	83(A19)	RXCLK0	133(AE11)	RXD51	183(B12)	TXEN2
34(AF9)	TXD50	84(A18)	TXER1	134(AE12)	COL6	184(B11)	TXD22
35(AF10)	RXD53	85(A17)	TXD11	135(AE13)	TXD63	185(B10)	RXER2
36(AF11)	RXD50	86(A16)	RXER1	136(AE14)	TXEN6	186(B9)	RXD22
37(AF12)	CRS6	87(A15)	RXD12	137(AE15)	TXCLK6	187(B8)	RXCLK2
38(AF13)	TXD62	88(A14)	COL2	138(AE16)	RXDV6	188(B7)	TXER3
39(AF14)	TXD61	89(A13)	CRS2	139(AE17)	RXD60	189(B6)	TXD32
40(AF15)	TXD60	90(A12)	TXER2	140(AE18)	CRS7	190(B5)	TXCLK3
41(AF16)	RXER6	91(A11)	TXD23	141(AE19)	TXD73	191(B4)	RXDV3
42(AF17)	RXD61	92(A10)	TXCLK2	142(AE20)	TXD70	192(B3)	RXD30
43(AF18)	COL7	93(A9)	RXD23	143(AE21)	RXDV7	193(C3)	TXFD31/FD63
44(AF19)	TXEN7	94(A8)	RXD20	144(AE22)	RXD71	194(D3)	TXFD25/FD57
45(AF20)	TXD71	95(A7)	CRS3	145(AE23)	RXCLK7	195(E3)	TXFD22/FD54
46(AF21)	RXER7	96(A6)	TXD33	146(AE24)	TEST2	196(F3)	TXFD19/FD51
47(AF22)	RXD72	97(A5)	TXD30	147(AE25)	D25	197(G3)	TXFD16/FD48
48(AF23)	RESET#	98(A4)	RXD33	148(AD25)	D26	198(H3)	TXFD12/FD44
49(AF24)	D31	99(A3)	RXCLK3	149(AC25)	D22	199(J3)	TXFD9/FD41
50(AF25)	D30	100(A2)	TEST1	150(AB25)	D19	200(K3)	TXFD6/FD38

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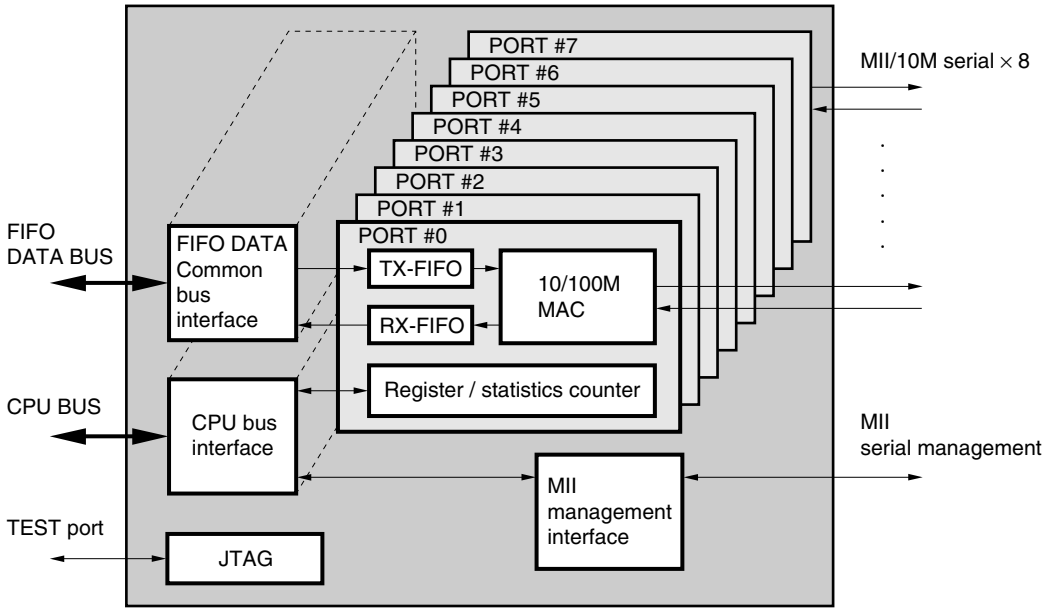
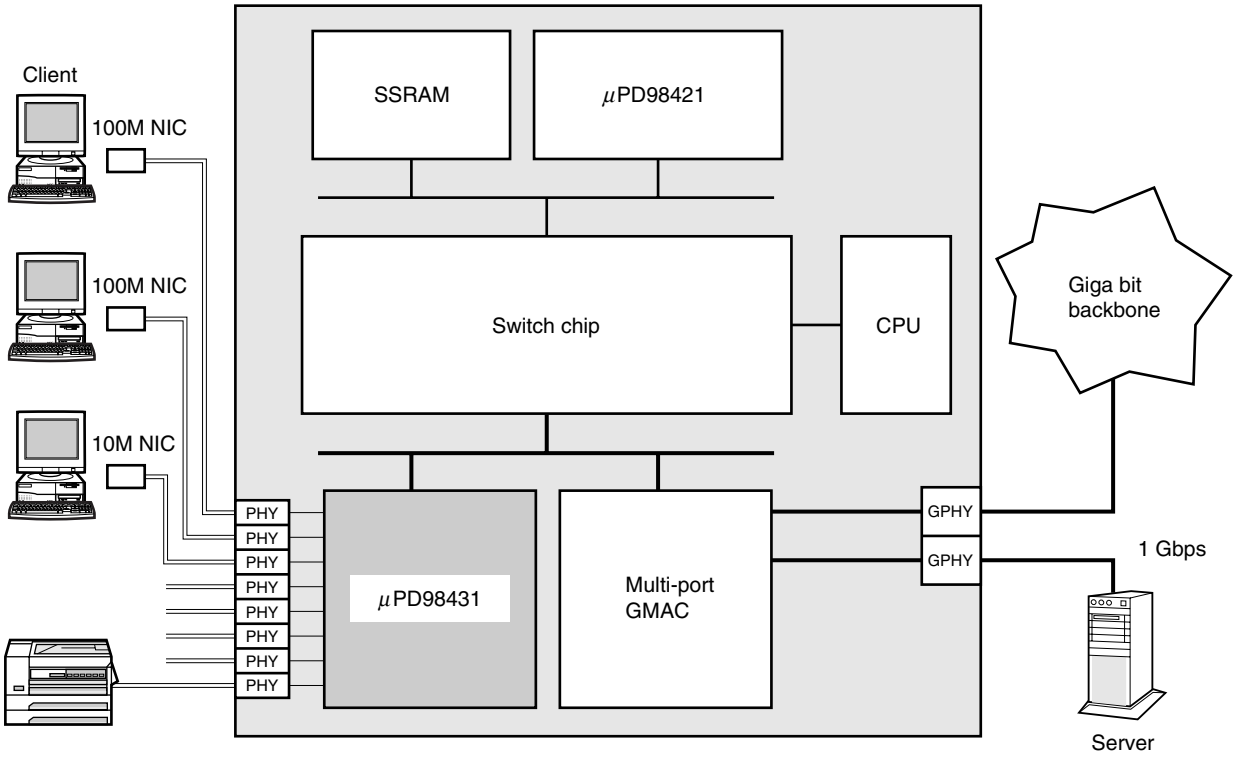
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
201(L3)	TXFD3/FD35	239(Y24)	D14	277(D4)	GND	315(AC23)	GND
202(M3)	TXFD2/FD34	240(W24)	D10	278(E4)	GND	316(AB23)	GND
203(N3)	RXFDQ0/FDQ0	241(V24)	D7	279(F4)	VDD	317(AA23)	VDD
204(P3)	RXFDQ3/FDQ3	242(U24)	D4	280(G4)	GND	318(Y23)	GND
205(R3)	RXFD25/FD25	243(T24)	D1	281(H4)	GND	319(W23)	GND
206(T3)	RXFD22/FD22	244(R24)	D0	282(J4)	TXFD13/FD45	320(V23)	D11
207(U3)	RXFD19/FD19	245(P24)	TXFBA5	283(K4)	VDD	321(U23)	VDD
208(V3)	RXFD16/FD16	246(N24)	TXFBA2	284(L4)	GND	322(T23)	GND
209(W3)	RXFD12/FD12	247(M24)	TXFDQ3	285(M4)	VDD	323(R23)	VDD
210(Y3)	RXFD9/FD9	248(L24)	TXFDQ0	286(N4)	GND	324(P23)	GND
211(AA3)	RXFD6/FD6	249(K24)	PASS	287(P4)	GND	325(N23)	GND
212(AB3)	RXFD3/FD3	250(J24)	HCLK	288(R4)	VDD	326(M23)	VDD
213(AC3)	RXFD2/FD2	251(H24)	A10	289(T4)	GND	327(L23)	GND
214(AD3)	COL4	252(G24)	A7	290(U4)	VDD	328(K23)	VDD
215(AD4)	TXD41	253(F24)	A4	291(V4)	RXFD15/FD15	329(J23)	INT#
216(AD5)	RXER4	254(E24)	A1	292(W4)	GND	330(H23)	GND
217(AD6)	RXD42	255(D24)	A0	293(Y4)	GND	331(G23)	GND
218(AD7)	RXCLK4	256(C24)	TMS	294(AA4)	VDD	332(F23)	VDD
219(AD8)	TXER5	257(C23)	CRS0	295(AB4)	GND	333(E23)	GND
220(AD9)	TXD52	258(C22)	TXD03	296(AC4)	GND	334(D23)	GND
221(AD10)	RXER5	259(C21)	TXD00	297(AC5)	VDD	335(D22)	VDD
222(AD11)	TXCLK5	260(C20)	RXDV0	298(AC6)	CLAMP	336(D21)	CLAMP
223(AD12)	RXD52	261(C19)	RXD01	299(AC7)	GND	337(D20)	GND
224(AD13)	RXCLK5	262(C18)	COL1	300(AC8)	VDD	338(D19)	VDD
225(AD14)	TXER6	263(C17)	TXD13	301(AC9)	CLAMP	339(D18)	CLAMP
226(AD15)	RXD63	264(C16)	TXEN1	302(AC10)	GND	340(D17)	GND
227(AD16)	RXCLK6	265(C15)	TXD10	303(AC11)	VDD	341(D16)	VDD
228(AD17)	TXER7	266(C14)	RXDV1	304(AC12)	CLAMP	342(D15)	CLAMP
229(AD18)	TXD72	267(C13)	RXD11	305(AC13)	GND	343(D14)	GND
230(AD19)	TXCLK7	268(C12)	TXD21	306(AC14)	RXD62	344(D13)	TXD20
231(AD20)	RXD73	269(C11)	RXDV2	307(AC15)	VDD	345(D12)	VDD
232(AD21)	RXD70	270(C10)	RXD21	308(AC16)	VDD	346(D11)	VDD
233(AD22)	TEST4	271(C9)	COL3	309(AC17)	GND	347(D10)	GND
234(AD23)	TEST5	272(C8)	TXEN3	310(AC18)	CLAMP	348(D9)	CLAMP
235(AD24)	D29	273(C7)	TXD31	311(AC19)	VDD	349(D8)	VDD
236(AC24)	D23	274(C6)	RXER3	312(AC20)	GND	350(D7)	GND
237(AB24)	D20	275(C5)	RXD32	313(AC21)	CLAMP	351(D6)	CLAMP
238(AA24)	D17	276(C4)	RXD31	314(AC22)	VDD	352(D5)	VDD

1.4 Internal Block Diagram



1.5 System Configuration Example



(1) Register interface

(1/2)

Pin Name	Pin No.	I/O	Function
CS#	70	I	Chip select. When this signal is low, the internal registers of the chip can be accessed.
RW	165	I	Host read/write. This pin is used by the host system to access the register bus. When a high level is input to this pin, the register bus is accessed for read. When a low level is input, the register bus is accessed for write.
A[10:0]	251, 71, 166, 252, 72, 167, 253, 168, 73, 254, 255	I	Register address. The address necessary for selecting a port or register to be accessed when an internal register of the μPD98431 is to be accessed is given to A[10:0]. The μPD98431 has a 32-bit register for each port. A[10:8] specifies a port, and A[7:0] specifies a register address. The relation between the setting of A[10:8] and a port number is as follows: Port 0 → A[10:8] = 000B Port 1 → A[10:8] = 001B Port 2 → A[10:8] = 010B Port 3 → A[10:8] = 011B Port 4 → A[10:8] = 100B Port 5 → A[10:8] = 101B Port 6 → A[10:8] = 110B Port 7 → A[10:8] = 111B
D[31:0]	49, 50, 235, 51, 52, 148, 147, 53, 236, 149, 54, 237, 150, 55, 238, 151, 56, 239, 152, 57, 320, 240, 153, 58, 241, 154, 59, 242, 155, 60, 243, 244	I/O, 3-state	Register data These pins form a bidirectional data bus through which the internal registers of the μPD98431 are accessed.
INT#	329	O, open drain	Interrupt signal. Interrupt request signal. This signal goes low if an interrupt source is generated. It is kept low until all the interrupt statuses are cleared if an interrupt occurs. This signal is an open-drain output signal.
RESET#	48	I	Hardware reset. Active-low asynchronous reset signal. Immediately after hardware reset, all the registers are set to their default values, and all the FIFOs and counters are cleared.
ACK#	164	O 3-state	Register data acknowledge. This signal indicates that the data on D[31:0] is valid when a register is read. When this signal is low, the data read from the register exists on D[31:0]. When a register is written, this signal indicates completion of the writing.

(2/2)

Pin Name	Pin No.	I/O	Function
HCLK	250	I	Register interface clock. This pin inputs a synchronization clock used to access a register. The maximum frequency of the input clock is 66 MHz. **Caution Make sure that the frequency of HCLK is always higher than the frequencies of RXCLK and TXCLK.**

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(2) FIFO interface

(1/3)

Pin Name	Pin No.	I/O	Function
RXFEN#/ FEN#	68	I	FIFO bus reception enable/FIFO bus enable. The function of this signal differs as follows depending on the FIFO bus mode: (1) 32-bit dual bus mode In this mode, this signal functions as RXFEN#. If this signal goes low, the receive FIFO bus interface is enabled, and data can be read from the receive FIFO. (2) 64-bit single bus mode In this mode, this signal functions as FEN#. If this signal goes low, the FIFO bus interface is enabled, and data can be read from the receive FIFO or written to the transmit FIFO.
TXFEN# FRW	163	I	FIFO bus transmission enable/FIFO bus direction The function of this signal differs as follows depending on the FIFO bus mode: (1) 32-bit dual bus mode In this mode, this signal functions as TXFEN#. If this signal goes low, the transmit FIFO bus interface is enabled, and data can be written to the transmit FIFO. (2) 64-bit single bus mode In this mode, this signal functions as FRW, and specifies the direction of FIFO bus access. While this signal is high, the FIFO bus is accessed by the receive FIFO for read. While it is low, the bus is accessed by the transmit FIFO for write.
FCLK	112	I	FIFO bus clock. The FIFO bus is synchronized with FCLK. The maximum frequency of the input clock is 66 MHz. **Caution Make sure that the frequency of HCLK is always higher than the frequencies of RXCLK and TXCLK.**

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(2/3)

Pin Name	Pin No.	I/O	Function
RXFPT[2:0]	63 to 65	O, 3-state	Receive port number. These signals indicate a port number from which receive data is output when the receive FIFO is accessed for read. The relation between RXFPT[2:0] and a port number is as follows: Port 0 → RXFPT[2:0] = 000B Port 1 → RXFPT[2:0] = 001B Port 2 → RXFPT[2:0] = 010B Port 3 → RXFPT[2:0] = 011B Port 4 → RXFPT[2:0] = 100B Port 5 → RXFPT[2:0] = 101B Port 6 → RXFPT[2:0] = 110B Port 7 → RXFPT[2:0] = 111B
TXFPT[2:0]	160, 66, 161	I	Transmit port number. These signals indicate the port number of the transmit FIFO to which transmit data is written when the transmit FIFO is accessed for write. The relation between TXFPT[2:0] and a port number is as follows: Port 0 → TXFPT[2:0] = 000B Port 1 → TXFPT[2:0] = 001B Port 2 → TXFPT[2:0] = 010B Port 3 → TXFPT[2:0] = 011B Port 4 → TXFPT[2:0] = 100B Port 5 → TXFPT[2:0] = 101B Port 6 → TXFPT[2:0] = 110B Port 7 → TXFPT[2:0] = 111B
TXFD[31:0], RXFD[31:0]/ FD[63:0]	193, 1, 2, 102, 101, 3, 194, 103, 4, 195, 104, 5, 196, 105, 6, 197, 106, 7, 282, 198, 107, 8, 199, 108, 9, 200, 109, 10, 201, 202, 110, 11, 13 to 15, 114, 16, 115, 205, 17, 116, 206, 18, 117, 207, 19, 118, 208, 291, 20, 119, 209, 21, 120, 210, 22, 121, 211, 122, 23, 212, 213, 123, 24	I, O / I/O, 3-state	32-bit transmit FIFO data bus, 32-bit receive FIFO data bus/64-bit FIFO data bus. These signals provide the data bus of the FIFO bus interface. The functions of these signals differ as follows depending on the FIFO bus mode. (1) 32-bit dual bus mode These signals function as TXFD[31:0] and RXFD[31:0]. This 64-bit data bus is divided into two unidirectional buses, TXFD[31:0] and RXFD[31:0], when the BUSWTH bit of the MISCR register is cleared to 0. (2) 64-bit single bus mode These signals function as FD[63:0]. This 64-bit data bus is used as a 64-bit bidirectional bus to access the FIFO when the BUSWTH bit of the MISCR register is set to 1.

(3/3)

Pin Name	Pin No.	I/O	Function
RXFDQ[3:0]/ FDQ[3:0]	204, 12, 111, 203	O / O/I, 3-state	Receive data attribute/FIFO bus attribute. These signals indicate the attribute of data on the FIFO bus. The functions of these signals differ as follows depending on the bus mode: (1) 32-bit dual bus mode These signals function as RXFDQ[3:0] and output the attribute of the receive data output onto RXFD[31:0] when the FIFO bus is accessed by the receive FIFO for read. For the output pattern of RXFDQ[3:0], refer to **Table 3-3**. (2) 64-bit single bus mode These signals function as FDQ[3:0] and input the attribute of the transmit data on FD[63:0] when the transmit FIFO is accessed for write. When the receive FIFO is accessed for read, the attribute of the receive data output onto FD[63:0] is output. For the input pattern and output pattern of FDQ[3:0], refer to **Tables 3-2** and **3-4**.
TXFDQ[3:0]	247, 67, 162, 248	I	Transmit data attribute. These signals indicate the attribute of the transmit data on the FIFO bus in the 32-bit dual bus mode. They indicate the attribute of the transmit data on FD[63:0] when the transmit FIFO is accessed for write. For the input pattern of TXFDQ[3:0], refer to **Table 3-1**. These signals are meaningless in the 64-bit single bus mode.
TXFBA[7:0]	156, 61, 245, 157, 62, 246, 159, 158	O, 3-state	Transmit FIFO buffer available. When these signals are high, the transmit FIFO has space to which transmit data can be written. If the quantity of the data in the transmit FIFO exceeds the value set to the TFDMH field of the TFIC register, these signals go low. A TXFBA signal is provided for each port, and TXFBA[n] is the TXFBA signal of port n.
RXFA	113	O, 3-state	Receive frame available. When this signal is high, the port indicated by RXFPT has at least one packet from the receive data stream that is ready to be transferred to the host system.
PASS	249	I	Receive frame pass. This signal is input to start transfer of the receive data currently on the FIFO bus when the bus is accessed by the receive FIFO for read.
SKIP	69	I	Receive frame skip. This signal is input to skip the port currently on the FIFO bus and read data from the next port when the FIFO bus is accessed by the receive FIFO for read.

(3) MII (Media Independent Interface)

(1/4)

Pin Name	Pin No.	I/O	Function
TXCLK[7:0]	230, 137, 222, 29, 190, 92, 179, 174	I	MII transmit clock. These pins input the transmit clock (duty: 50%) necessary for outputting data to the PHY device connected to each port. Transmit data from each port, TXD7[3:0] through TXD0[3:0], and TXEN[7:0] that indicates that the transmit data on TXD is valid are output to each port in synchronization with this clock. In the MII mode, a 2.5 MHz clock is input for 10 Mbps operation, and a 25 MHz clock is input for 100 Mbps operation. In this mode, TXD and TXEN are output in synchronization with the rising of TXCLK. In the 10 Mbps serial mode, a 10 MHz clock is input. In this mode, TXD and TXEN are output in synchronization with the rising of TXCLK. For the unused ports, fix TXCLK to high or low level.
TXD0[3:0]	258, 173, 80, 259	O	MII transmit data (port 0). These pins output transmit data to the PHY device connected to port 0. In the MII mode, transmit data of nibble width (4 bits wide) is output at the rising edge of TXCLK0. In the 10 Mbps serial mode, only TXD0[0] is used to output serial transmit data at the rising edge of TXCLK0.
TXD1[3:0]	263, 178, 85, 265	O	MII transmit data (port 1). These pins output transmit data to the PHY device connected to port 1. In the MII mode, transmit data of nibble width (4 bits wide) is output at the rising edge of TXCLK1. In the 10 Mbps serial mode, only TXD1[0] is used to output serial transmit data at the rising edge of TXCLK1.
TXD2[3:0]	91, 184, 268, 344	O	MII transmit data (port 2). These pins output transmit data to the PHY device connected to port 2. In the MII mode, transmit data of nibble width (4 bits wide) is output at the rising edge of TXCLK2. In the 10 Mbps serial mode, only TXD2[0] is used to output serial transmit data at the rising edge of TXCLK2.
TXD3[3:0]	96, 189, 273, 97	O	MII transmit data (port 3). These pins output transmit data to the PHY device connected to port 3. In the MII mode, transmit data of nibble width (4 bits wide) is output at the rising edge of TXCLK3. In the 10 Mbps serial mode, only TXD3[0] is used to output serial transmit data at the rising edge of TXCLK3.
TXD4[3:0]	124, 28, 215, 126	O	MII transmit data (port 4). These pins output transmit data to the PHY device connected to port 4. In the MII mode, transmit data of nibble width (4 bits wide) is output at the rising edge of TXCLK4. In the 10 Mbps serial mode, only TXD4[0] is used to output serial transmit data at the rising edge of TXCLK4.
TXD5[3:0]	33, 220, 131, 34	O	MII transmit data (port 5). These pins output transmit data to the PHY device connected to port 5. In the MII mode, transmit data of nibble width (4 bits wide) is output at the rising edge of TXCLK5. In the 10 Mbps serial mode, only TXD5[0] is used to output serial transmit data at the rising edge of TXCLK5.

(2/4)

Pin Name	Pin No.	I/O	Function
TXD6[3:0]	135, 38 to 40	O	MII transmit data (port 6). These pins output transmit data to the PHY device connected to port 6. In the MII mode, transmit data of nibble width (4 bits wide) is output at the rising edge of TXCLK6. In the 10 Mbps serial mode, only TXD6[0] is used to output serial transmit data at the rising edge of TXCLK6.
TXD7[3:0]	141, 229, 45, 142	O	MII transmit data (port 7). These pins output transmit data to the PHY device connected to port 7. In the MII mode, transmit data of nibble width (4 bits wide) is output at the rising edge of TXCLK7. In the 10 Mbps serial mode, only TXD7[0] is used to output serial transmit data at the rising edge of TXCLK7.
TXEN[7:0]	44, 136, 130, 125, 272, 183, 264, 79	O	MII transmit enable. These signals indicate whether the transmit data (TXD) of each port is valid. In the 10 Mbps serial mode, they remain high starting from the fist bit of a preamble, until the last bit of the transmit frame is output. In the MII mode, they remain high starting from the first nibble data indicating a preamble, until the last nibble data of the transmit frame is output.
RXCLK[7:0]	145, 227, 224, 218, 99, 187, 181, 83,	I	MII receive clock. These pins input the clock (duty: 50%) received from the PHY device. RXD7[3:0] through RXD0[3:0] that are the data received from each port, and TXEN[7:0] that indicates the existence of transmit data on TXD are output in synchronization with this clock. In the MII mode, a 2.5 MHz clock is input for 10 Mbps operation, and a 25 MHz clock is input for 100 Mbps operation. In this mode, RXD and RXDV are input at the rising edge of RXCLK. In the 10 Mbps serial mode, a 10 MHz clock is input. In this mode, RXD is input at the rising edge of RXCLK. Fix RXCLK of an unused port to the high or low level.
RXD0[3:0]	175, 82, 261, 176	I	MII receive data (port 0). These pins input data received from the PHY device connected to port 0. In the MII mode, receive data of nibble width (4 bits wide) is input at the rising edge of RXCLK0. In the 10 Mbps serial mode, only RXD0[0] is used and serial receive data is input at the rising edge of RXCLK0.
RXD1[3:0]	180, 87, 267, 182	I	MII receive data (port 1). These pins input data received from the PHY device connected to port 1. In the MII mode, receive data of nibble width (4 bits wide) is input at the rising edge of RXCLK1. In the 10 Mbps serial mode, only RXD1[0] is used and serial receive data is input at the rising edge of RXCLK1.
RXD2[3:0]	93, 186, 270, 94	I	MII receive data (port 2). These pins input data received from the PHY device connected to port 2. In the MII mode, receive data of nibble width (4 bits wide) is input at the rising edge of RXCLK2. In the 10 Mbps serial mode, only RXD2[0] is used and serial receive data is input at the rising edge of RXCLK2.

(3/4)

Pin Name	Pin No.	I/O	Function
RXD3[3:0]	98, 275, 276, 192	I	MII receive data (port 3). These pins input data received from the PHY device connected to port 3. In the MII mode, receive data of nibble width (4 bits wide) is input at the rising edge of RXCLK3. In the 10 Mbps serial mode, only RXD3[0] is used and serial receive data is input at the rising edge of RXCLK3.
RXD4[3:0]	30, 217, 128, 31	I	MII receive data (port 4). These pins input data received from the PHY device connected to port 4. In the MII mode, receive data of nibble width (4 bits wide) is input at the rising edge of RXCLK4. In the 10 Mbps serial mode, only RXD4[0] is used and serial receive data is input at the rising edge of RXCLK4.
RXD5[3:0]	35, 223, 133, 36	I	MII receive data (port 5). These pins input data received from the PHY device connected to port 5. In the MII mode, receive data of nibble width (4 bits wide) is input at the rising edge of RXCLK5. In the 10 Mbps serial mode, only RXD5[0] is used and serial receive data is input at the rising edge of RXCLK5.
RXD6[3:0]	226, 306, 42, 139	I	MII receive data (port 6). These pins input data received from the PHY device connected to port 6. In the MII mode, receive data of nibble width (4 bits wide) is input at the rising edge of RXCLK6. In the 10 Mbps serial mode, only RXD6[0] is used and serial receive data is input at the rising edge of RXCLK6.
RXD7[3:0]	231, 47, 144, 232	I	MII receive data (port 7). These pins input data received from the PHY device connected to port 7. In the MII mode, receive data of nibble width (4 bits wide) is input at the rising edge of RXCLK7. In the 10 Mbps serial mode, only RXD7[0] is used and serial receive data is input at the rising edge of RXCLK7.
CRS[7:0]	140, 37, 32, 26, 95, 89, 177, 257	I	Carrier sense. These are carrier sense signals input from the PHY device connected to each port. Fix CRS of an unused port to the low level.
RXDV[7:0]	143, 138, 132, 127, 191, 269, 266, 260	I	MII receive data valid. These signals indicate, in the MII mode, that the data on RXD is valid for each port. When these signals are high, the data on RXD is valid. Fix RXDV of an unused port to the high or low level.
COL[7:0]	43, 134, 129, 214, 271, 88, 262, 78	I	Collision detected. These pins input the collision signals detected by the PHY device connected to each port. Fix COL of an unused port to the low level.
TXER[7:0]	228, 225, 219, 27, 188, 90, 84, 172	O	MII transmit coding error. These signals indicate that an error occurs at each port of the μPD98431 during transmission.

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Pin Name	Pin No.	I/O	Function
RXER[7:0]	46, 41, 221, 216, 274, 185, 86, 81	I	MII receive error. These are input signals to detect errors occurring at each port of the PHY device during reception. Fix RXER of an unused port to the low level.
MDC	77	O	MII management data clock. This is a transfer clock for MII serial management data.
MDIO	171	I/O	MII management data input/output. This is a bidirectional MII serial management data signal.

(4) JTAG pins (These functions can be supported upon request.)

Pin Name	Pin No.	I/O	Function
TMS	256	I	JTAG test mode select. This signal controls the boundary scan state machine. This pin is internally pulled up. (pull-up resistor: 50 kΩ)
TDI	76	I	JTAG test data input. This signal is serial data input for boundary scan. This pin is internally pulled up. (pull-up resistor: 50 kΩ)
TDO	74	O 3-state	JTAG test data output. This signal is serial data output for boundary scan.
TCK	169	I	JTAG test clock. This is clock input used to synchronize test data input and output. This pin is internally pulled up. (pull-up resistor: 50 kΩ)
TRST#	75	I	JTAG reset. When this signal is deasserted low, the boundary scan operation is reset. This signal must be kept high during boundary scan operation. When not using the JTAG function, keep it low. This pin is internally pulled up. (pull-up resistor: 50 kΩ)

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(5) Test pins and power pins

Pin Name	Pin No.	I/O	Function
TEST	234, 233, 170, 146, 100, 25	I	Test pins. These pins are used to test the device. Always fix these pins to low.
VDD	279, 283, 285, 288, 290, 294, 297, 300, 303, 307, 308, 311, 314, 317, 321, 323, 326, 328, 332, 335, 338, 341, 345, 346, 349, 352	–	Power supply (+3.3 V)
GND	277, 278, 280, 281, 284, 286, 287, 289, 292, 293, 295, 296, 299, 302, 305, 309, 312, 315, 316, 318, 319, 322, 324, 325, 327, 330, 331, 333, 334, 337, 340, 343, 347, 350	–	Ground (0 V)
CLAMP	298, 301, 304, 310, 313, 336, 339, 342, 348, 351	–	Clamp power supply. This pin supplies a clamp voltage to the MII buffer circuit. Supply +5 V to this pin when an external 5 V PHY device is used. Supply +3.3 V when an external 3.3 V PHY device is used.

CHAPTER 3 FUNCTIONAL DESCRIPTION

3.1 System Configuration

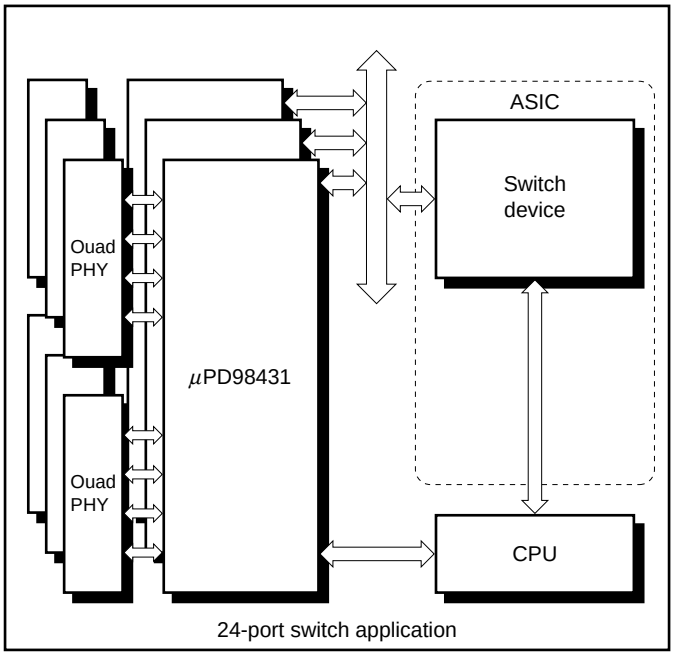
The μPD98431 is an 8-port, 10/100 Mbps Ethernet MAC (Media Access Control) having many modes and features. This device has been developed for network devices requiring multiple ports such as LAN switches and rooters.

The μPD98431 supports two network interfaces. In the MII mode, it provides an interface supporting MII (Media Independent Interface) standardized by IEEE802.3u. By connecting a PHY device supporting MII, a 10 Mbps or 100 Mbps Ethernet can be implemented. In the 10 Mbps serial interface mode, an interface with an external 10 Mbps transceiver which transmits clocked serial data can be realized. Half-duplex or full-duplex operation can be performed by all the ports of the μPD98431 and in each network interface mode.

Two system interfaces, FIFO bus interface and register bus interface, are available. The FIFO bus interface connects an upper layer with the internal FIFOs of the μPD98431. This interface has a speed of up to 66 MHz and a width of 64 bits. Each port of the μPD98431 has 2K bytes of receive FIFO and 512 bytes of transmit FIFO.

The register bus interface is used to access the control registers and statistics counter, and is not dependent on a specific CPU.

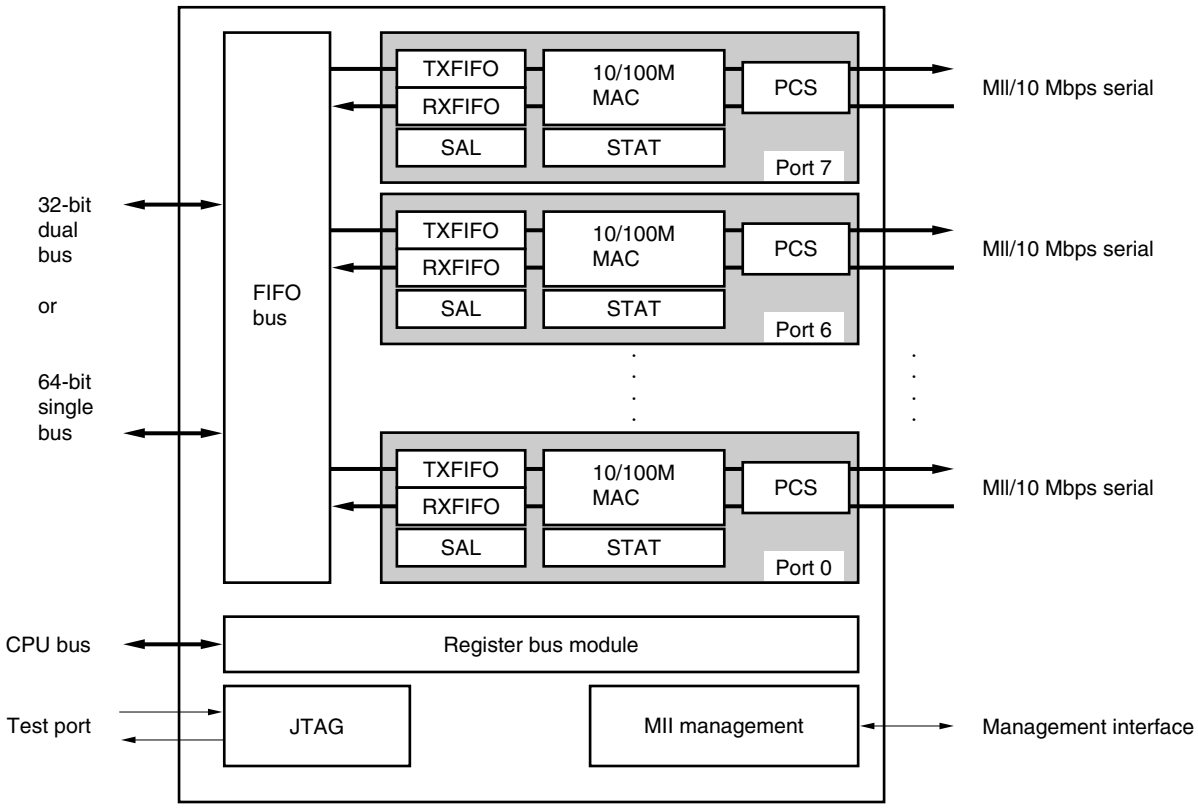
Figure 3-1. Example of System Configuration Using μPD98431



3.2 Function Blocks

The μPD98431 has an MAC module, PCS module, SAL module, STAT module, and FIFOs for each port. In addition, it also has common modules such as a FIFO bus module, MII management module, and register bus module (refer to **Figure 3-2**).

Figure 3-2. μPD98431 Functional Block Diagram



3.2.1 MAC module

The MAC module realizes a 10/100M Ethernet MAC function and is designed to connect a PHY device supporting MII. If a PCS module is connected to the MAC module, the μPD98431 can be connected to a 10BASE-T transceiver having a 10 Mbps serial interface.

The MAC module has a transmission block, reception block, and MAC control block. The transmission and reception blocks realize the Ethernet transmission and reception operations standardized by IEEE802.3 and IEEE802.3u. The MAC control block processes flow control and performs reception and transmission of the flow control frame defined by IEEE802.3x.

The MAC module not only processes data but also assists data processing by the blocks connected to it by issuing status information on reception and transmission.

3.2.2 PCS module

The PCS module implements the Physical Coding Sublayer function that is used to connect a 10 Mbps serial interface. This module is connected to the MAC module at the system side. At the network side of the PCS module, a PHY device supporting MII or 10BASE-T transceiver can be connected.

If the PCS module is set so that it connects an MII-supporting PHY device as the external device at the network side, the PCS module connects the MII signal from the MAC module to the external device as is. If the PCS module is set so that it is connected to an external device with the 10 Mbps serial bus interface, the module converts MII nibble data into serial data. In this way, the PCS module can be used to configure a 10/100BASE-TX system via MII, and a 10BASE-T system with the 10M-bps serial interface.

3.2.3 SAL (Station Address Logic) module

The SAL module detects the value in the destination address field of a receive packet, compares the address under conditions specified in advance, and reports the result of the comparison to the receive FIFO. The receive FIFO accepts or rejects the receive packet, depending on an address condition, in accordance with the report from the SAL module.

The address condition can be set for each port or by address type.

A unicast address is compared with the value of the station address register that is set in the control register of each port. In the case of a multicast address, whether all multicast packets are received or only the multicast packet selected by a hash table is received can be selected. As for a broadcast address, whether the broadcast packet is received or not can be selected.

In addition, the μPD98431 can also accept all packets for all address types. For address filtering conditions, refer to **3.5.5 Address filtering**.

3.2.4 STAT (STATistics counter) module

The μPD98431 has a statistics counter set that is useful for implementing RMON/SMNP, for each port. The STAT module implements this statistics counter set. For details of the statistics counter, refer to **3.12 Statistics Counter**.

3.2.5 Internal FIFOs

As FIFOs, the μPD98431 has a high-speed dual-port SRAM which has a capacity of 2K bytes for reception and 512 bytes for transmission for each port. The FIFOs also arbitrate the transmit/receive clock from the network side and FIFO bus clock from the system side.

3.2.6 FIFO bus module

The FIFO bus module interfaces between the internal FIFOs and upper layer. This interface has a speed of up to 66 MHz and a width of 64 bits. Two data bus modes can be selected: 64-bit single bus mode in which data can transfer bidirectionally over a 64-bit bus, and 32-bit dual bus mode in which a 32-bit transmit data bus and a 32-bit receive data bus, each of which transfers data unidirectionally, are used.

3.2.7 MII management module

The MII management module implements the MII serial management function standardized by IEEE802.3u. By using this module, the μPD98431 supplies one serial interface that is used to access PHY registers by using a MII management frame between an external MII and PHY device.

3.2.8 Register bus module

The register bus module supplies control registers that are used to set each port or the entire chip, and a register bus that is used to access the statistics counter of each port. The register bus consists of an 11-bit address bus and a 32-bit bidirectional data bus. These general-purpose buses are not dependent on a specific CPU.

3.2.9 Operating clock

The μPD98431 requires four operating clocks: transmit clock and receive clock provided by a PHY device, a clock for register access, and a clock to transfer data with the FIFO bus.

The transmission block of the MAC module reads transmit data from the transmit FIFO in synchronization with the transmit clock input from the PHY device, generates a transmit frame, and outputs it to the PHY device. In the meantime, the reception block of the MAC module receives a receive frame in synchronization with the receive clock input from the PHY device, and writes the data to the host system to the receive FIFO. As the transmit clock and receive clock, 25 MHz clocks are input for the 100 Mbps operation and 2.5 MHz clocks are input for the 10 Mbps operation.

The clock to access a register is provided in the HCLK signal. The frequency of this signal can be set in the range 66 to 25 MHz. The MDC signal used for the MII management interface is generated by dividing this HCLK signal.

The clock provided to the FIFO bus is the FCLK signal. Data is written from the host system to the internal FIFOs of the μPD98431, or read from the FIFOs to the host system in synchronization with this FCLK signal. The frequency of the FLCK signal is in the range 66 to 25 MHz.

3.3 Frame Format

In an Ethernet network, information is transmitted or received in the form of a packet or frame. The frame format used for Ethernet consists of preamble (PA), start frame delimiter (SFD), destination address (DA), source address (SA), type/length field (TYPE/LEN), data field (DATA), and frame check sequence (FCS) (refer to **Figure 3-3**).

The frame length is defined to be 64 bytes at minimum and 1518 bytes at maximum, excluding the preamble and SFD.

Figure 3-3. Ethernet/IEEE802.3 Frame Structure

PA	SFD	DA	SA	TYPE /LEN	DATA	FCS
7B	1B	6B	6B	2B	46B to 1500B	4B

B = byte

(1) Preamble and SFD

The preamble and SFD consists of the repetition of “10” for 62 bits and “11”, and indicate the beginning of each frame.

(2) Destination address

The destination address field indicates the MAC address of the destination. A unicast address, multicast address, or broadcast address is written to this field.

(3) Source address

The MAC address at the transmission source is written to the source address field.

(4) Type/length field

This field of an Ethernet frame is used to indicate a protocol type. In an IEEE802.3 frame, this field is used to indicate the length of the data field.

(5) Data field

The data field consists of 46 to 1500 bytes.

(6) Frame check sequence

The frame check sequence field is used to write 32-bit CRC (Cyclic Redundancy Check) to check transfer data.

A VLAN frame is slightly different from the normal frame in structure. In this frame, a 4-byte VLAN header is inserted immediately after the source address field. The μPD98431 has a VLAN frame detection function. If a transmit or receive frame is detected as a VLAN frame, it performs packet processing based on the length of this frame. For details, refer to **3.11 Operation for VLAN Frames**.

Figure 3-4. VLAN Frame Structure

PA	SFD	DA	SA	TPID	TCI	LEN	DATA	FCS
7B	1B	6B	6B	2B	2B	2B	42B to 1500B	4B

VLAN header

B = byte

TPID = Tag Protocol ID, TCI = Tag Control Information

3.4 Transmission Operation

The μPD98431 creates a transmit data frame based on the data given by the host system to the transmit FIFO. If a collision occurs, it executes a back-off algorithm and re-transmits the data in the transmit FIFO. Status information for each transmit packet, such as the number of transmit bytes and occurrence of errors, is written to the TSVREG1 and TSVREG2 registers on completion of transmission.

3.4.1 Creating transmit packet

Usually, the transmit data written by the host system to the transmit FIFO includes a destination address and the last valid data in the data field. The preamble, SFD, and FCS necessary for a transmit packet frame can be automatically appended by the μPD98431.

(1) Appending preamble and SFD

The μPD98431 always appends a preamble and SFD to the transmit data in the transmit FIFO and outputs the data to the network.

(2) Appending CRC

The μPD98431 can automatically calculate the value of the CRC and append it to the FCS field at the end of a packet. Whether a CRC is automatically appended or not is determined by the TXFDQ signal and the setting of
★ the CRCEN bit and the PADEN bit of the MACC1 register.

If appending a CRC is specified by the TXFDQ signal, a CRC is always automatically appended at the end of a transmit packet. If appending a CRC is not specified by the TXFDQ signal, whether a CRC is automatically appended depends on the setting of the CRCEN bit of the MACC1 register. If this CRCEN bit is 0, a CRC is not automatically appended; if it is 1, a CRC is automatically appended.

★ Also when the PADEN bit specifying to append PAD is 1, the correct CRC is always automatically appended by the μPD98431, regardless of the specification by the TXFDQ signal or setting of the CRCEN bit.

If it is specified that a CRC is not automatically appended, the value of the FCS field must be appended at the end of the transmit data stream that is written to the transmit FIFO by the upper layer.

(3) Appending PAD

If the data length of one packet written to the transmit FIFO is less than the minimum frame length of 64 bytes (68 bytes in the case of a VLAN frame), the μPD98431 automatically appends PAD to extend the data length to the minimum frame length. If the PADEN bit of the MACC1 register is set to 1 or if the appending CRC is ★ specified by the TXFDQ signal, the PAD auxiliary function is enabled.

Whether PAD is appended to a VLAN frame depends on the APD and VPD bits of the MACC2 register. For details, refer to **3.11 Operation for VLAN Frames**.

3.4.2 Starting packet transmission

Transmitting a packet to the network is started if either of the following conditions is satisfied:

- If the quantity of the data in the transmit FIFO exceeds a predetermined threshold level
- If an attribute indicating the end of data is given to TXFDQ or FDQ at the same time as the transmit data that is to be written to the transmit FIFO

The transmission start threshold level is written to the TFDWL field of the TFIC register.

If transmission is started during half-duplex operation, carrier sense is first performed to check to see if any other station on the network is transmitting data. If no other station is transmitting data, and if the gap between packets that was determined in advance when the previous data transmission was completed, or inter-packet gap is satisfied, outputting a transmit data stream to the PHY device is immediately started. If any other station is transmitting data, the μPD98431 waits until the communication ends and postpones its transmission until the inter-packet gap is satisfied.

Because the carrier sense is ignored during full-duplex operation, outputting transmit data to the PHY device is started as soon as the transmission start condition has been satisfied.

3.4.3 Setting inter-packet gap

With the μPD98431, the inter-packet gap (IPG) must be set by using a register. This gap may be back-to-back IPG that is applied when data is successively transmitted with the minimum gap width, or non-back-to-back IPG that is used in the other cases.

(1) Back-to-back IPG

The back-to-pack IPG is set by the IPGT register. The back-to-back IPG is used to transmit data successively with the minimum gap width after station transmission. At this time, the minimum gap width is written to the IPGT register. If the next transmission start condition is satisfied within the time of the minimum gap width after transmission of the station has been completed, the μPD98431 assumes back-to-back transmission and immediately outputs the next transmit data stream in the PHY device after the IPG time set in the IPGT register has elapsed.

(2) Non-back-to-back IPG

The non-back-to-back IPG set by the IPGR register is used to start outputting a transmit data stream to the PHY device after transmission by another station has been completed and the IPG time has elapsed. The non-back-to-back IPG consists of two portions. In the first half of the non-back-to-back IPG, carrier sense is performed. If a carrier is detected during this time, the IPG count is cleared. The μPD98431 waits until no carrier is detected and starts IPG count again. If no carrier is detected during the period in which carrier sense is performed, the μPD98431 immediately starts outputting a transmit data stream after the IPG period has elapsed.

The IPGR register sets the total time of the non-back-to-back IPG to the IPGR2 field, and the first half carrier sense period to the IPGR1 field.

3.4.4 Collision and retransmission

The μPD98431 automatically retransmits packets if a collision occurs, except if the number of collisions exceeds the maximum number of times set by the CLRT register or if a collision occurs after the collision window period that is also set by the CLRT register. If a collision occurs, data transmission from the transmit FIFO is stopped, and transmission of jam is started. The read point in the transmit FIFO is returned to the beginning of the transmit data. When transmission of a jam pattern has been completed, the μPD98431 stands by for transmission in accordance with the back-off algorithm. When the back-off period has expired, retransmission is automatically started.

If the number of collisions exceeds the maximum number of times set by the CLRT register or if it occurs after the collision window period set by the CLRT register, it is regarded as a network error. If this happens, the data in the transmit FIFO of the packet in which the condition occurs is cleared, and the other transmit packet data already accumulated is not affected. The occurrence of this condition causes the INT# signal to go low. If the number of collisions exceeds the maximum number of times, the ECOL bit of the TSVERG1 register is set to 1. If a collision occurs after the collision window period, the LCOL bit of the TSVREG1 register is set to 1.

The interval of retransmission is determined by the back-off algorithm, and the μPD98431 stands by for retransmission for random slot time (512-bit time). This algorithm determines coefficient r of the slot time during which the μPD98431 stands by before executing the nth retransmission, by using the following expression:

$0 \leq r < 2^n$, where n = 10 if n exceeds 10

3.4.5 End of or aborting transmission

The μPD98431 ends or aborts transmission if any of the conditions described below is satisfied. If transmission is aborted, the packet data remaining in the transmit FIFO is cleared. If transmission is aborted in the packet being written to the transmit FIFO, all the data written to the transmit FIFO after transmission was aborted are ignored until the end of data is specified by inputting the TXFDQ/FDQ signal (refer to **3.7.1 FIFO bus interface**).

Each time transmission has ended or has been aborted, the status information related to the transmission operation is reported to the TSVREG1 and TSVREG2 registers. This status information can be used as an interrupt source for the INT# signal by unmasking the interrupt by using the TIMR register.

(1) Normal completion

If data transmission is completed without problem, the TDONE bit of the TSVREG1 register is set to 1. If retransmission due to collision takes place before transmission is completed, the number of times of retransmission is reported to the TCBC field of the TSVREG1 register.

(2) Collision exceeding maximum number of times

If the number of collisions exceeds the maximum number of times set by the RETRY field of the CLRT register, transmission is aborted and the ECOL bit of the TSVREG1 register is set to 1.

(3) Occurrence of late collision

If the number of collision windows exceeds the collision window set by the LCOL field of the CLRT register, it is assumed as a late collision and transmission is aborted. If a late collision occurs, the LCOL bit of the TSVREG1 register is set to 1.

(4) Transmission excessive defer

If transmission is not started 24288-bit time after the μPD98431 tried to start transmission, it is assumed to be an excessive defer and transmission is aborted. If an excessive defer occurs, the TEDFR bit of the TSVREG1 register is set to 1.

(5) If attempt is made to transmit packet exceeding maximum packet length

If an attempt is made to transmit a packet with a length exceeding the maximum packet length set by the LMAX register, the μPD98431 continues transmission until the packet length reaches the value of the LMAX register and aborts transmission if the packet length exceeds the value of the LMAX register. If the HUGEN bit of the MACC1 register is set to 1, however, the transmit packet length limit by the LMAX register is canceled. If transmission is aborted under this condition, the TGNT bit of the TSVREG2 register is set to 1.

(6) Occurrence of transmit FIFO underrun

If all the data in the transmit FIFO has been transmitted and transmit data from the system cannot be written to the FIFO in time, the transmit FIFO underruns and transmission is aborted. If transmission is aborted because the transmit FIFO underruns, the TUDR bit of the FSVREG register is set to 1.

3.5 Reception Operation

The μPD98431 supplies receive data to the host system from the receive data stream sent from the PHY device. It detects the preamble and SFD, checks the length field, and executes CRC check. Status information on each received packet, such as the number of received bytes and occurrence of errors, is written to the RSVREG register after reception has been completed. This status information can be appended to the data stream output from the receive FIFO to the host system, depending on the setting of the MACC3 register. In addition, packet filtering can be also set depending on the address condition.

3.5.1 Detecting preamble and SFD

In the MII mode, each port recognizes data on the RXDn signal as receive data if the RXDVn signal goes high. In the 10 Mbps serial mode, the port recognizes data on RXDn[0] as receive data if the CRSn signal goes high. When recognized as receive data, the RXD data, which is serial data, is converted into parallel data inside the μPD98431. When a preamble pattern (1, 0, 1, 0 ...) is detected from the data converted into parallel data, each port waits until (1, 1) and SFD that follow the preamble pattern are detected. When the SFD is detected, the beginning of a receive packet is recognized, and storing data in the receive FIFO is started. The preamble and SFD are eliminated from the receive packet and are not stored in the receive FIFO.

3.5.2 Length field check

Each port of the μPD98431 counts the length of a receive packet, assumes the 2 bytes following the source address field to be the length field, and checks the data field length. The packet regarded as a VLAN frame regards the 2 bytes following the VLAN header as a length field. For information on how the VLAN frame is detected, refer to **3.11.1 Detecting VLAN frames**. The result of checking is reported to the host system as status information.

3.5.3 CRC check

Each port of the μPD98431 automatically calculates a 4-byte frame check sequence (FCS) from the receive packet data and compares it with the CRC data suffixed to the receive packet. The result of comparison is reported to the host system as status information.

3.5.4 Packet filtering

The μPD98431 can filter receive packets under the following conditions. Filtering can be set for each port. Two or more filtering conditions can be used in combination.

- Destination address
- Short packet: Packet with packet length of less than 64 bytes
- CRC error packet
- Control frame

For details of the procedure to filter packets by using the destination address as a condition, refer to **3.5.5 Address filtering**. Filtering for CRC error packets, control frames, and short packets can be specified by using the RFIC2 register. Depending on the setting of this register, a packet in which a CRC error has occurred, control frames, and short packets can be eliminated from the receive FIFO. All the filtering conditions may be canceled. If all of them are canceled, all the received packets are transferred to the host system.

3.5.5 Address filtering

The μPD98431 can execute filtering by using the destination address of a receive packet and eliminate a packet that does not satisfy a given condition. The address filtering condition is set using the AFR, HT1, and HT2 registers. A filtering condition can be also set for each address type of unicast address, multicast address, and broadcast address. In addition, two or more of the filtering conditions described below can be used in combination.

(1) Filtering of unicast address

The station address set by the LSA1 and LSA2 registers is used as a unicast address and is compared with the destination address of the receive packet. If the two addresses coincide, the receive packet is accumulated to the receive FIFO. Coincidence of the unicast address is detected for each receive packet, unless the PRO bit of the AFR register is set to 1.

(2) Filtering of multicast address

A multicast address is filtered in two ways. When the PRM bit of the AFR register is set to 1, all multicast packets are stored in the receive FIFO.

When the AMC bit of the AFR register is set to 1, only multicast packets that coincide with the hash table prepared by the HT1 and HT2 registers are stored in the receive FIFO. Coincidence is detected by using the hash table as shown below:

The CRC of the received multicast address is calculated. As a result, a 32-bit CRC is obtained. By using the bits 28 to 23 of this 32-bit CRC, the hash table is referenced. The following polynomial expression is used for CRC calculation.

$$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^{8} + X^{7} + X^{5} + X^{4} + X^{2} + X + 1$$

If the bit of the HT1 or HT2 register indicated by these high-order 6 bits is set to 1, the multicast packet is stored in the receive FIFO. To set the hash table, the CRC of a multicast address must be calculated and the corresponding bit must be set to 1 in advance.

(3) Filtering broadcast address

The broadcast packet is stored in the receive FIFO when the ABC bit of the AFR register is set to 1.

(4) Promiscuous mode

The promiscuous mode is set when the PRO bit of the AFR register is set to 1, and the packets of all address types are stored in the receive FIFO.

(5) Address filtering setting condition

Address filtering is set as follows:

First, set the SRXEN bit of the MACC1 register to 1. If this bit is 0, all the receive packets are ignored and not received by the receive FIFO. Next, write a station address to the LSA1 and LSA2 registers. Write a combination of the necessary filtering conditions to the AFR register. To perform conditional multicast packet reception, a hash table must be set using the HT1 and HT2 registers. When all these settings have been completed, set the SRXEN bit to 1 to enable packet reception.

3.5.6 Receive FIFO overflow

If the receive FIFO overflows while receive packets are being stored in it, storing of the data is immediately stopped. If this happens, the packets in the receive FIFO are cleared, and the data received after the overflow occurred is ignored. The overflow is reported to the host system by the FSVREG register.

3.5.7 Clearing receive FIFO

The host system can clear the contents of the receive FIFO by setting the RXFFLH bit of the MACC3 register to 1. If this bit is set while receive packets are being stored in the receive FIFO, the packet being received is discarded. If the preceding receive packet has been already stored in the receive FIFO at this time, this packet is also cleared.

3.6 Full-Duplex Operation

Each port of the μPD98431 can execute full-duplex operation and can transmit and receive packets simultaneously. If the FULLD bit of the MACC1 register is set to 1, the full-duplex operation is enabled. In this case, the COLn and CRSn signals are ignored. If the setting of the SRXEN bit of the MACC1 register is changed while the CRSn signal is high, the new value of the SRXEN bit becomes valid after the CRSn signal has gone low, regardless of the setting of the FULLD bit.

3.7 System Bus Interfaces

The μPD98431 has a FIFO bus interface and a register bus interface to interface the host system. The FIFO bus interface is used to transfer transmit/receive data between the internal FIFOs of the μPD98431 and host system. The register bus interface is used to access the internal registers and statistics counters of the μPD98431.

3.7.1 FIFO bus interface

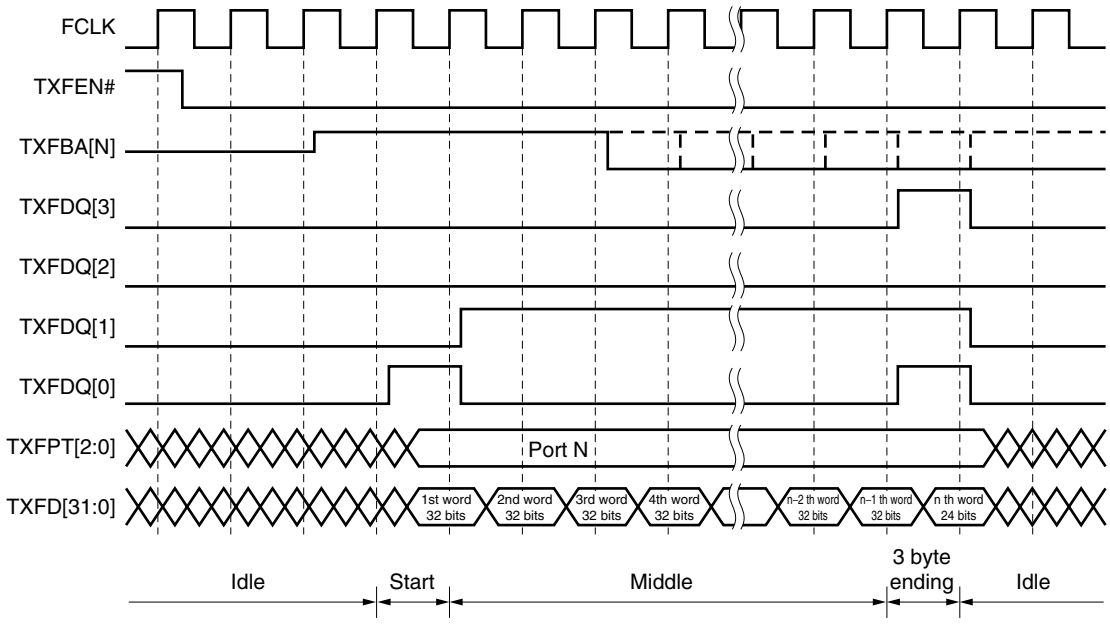
The μPD98431 has two FIFO bus interface modes: 32-bit dual bus mode and 64-bit single bus mode. In the 32-bit dual bus mode, a 32-bit transmit data bus and a 32-bit receive data bus are used so that transmit or receive data can be transferred unidirectionally. In the 64-bits single bus mode, a 64-bit bidirectional data bus is used to transfer transmit/receive data. These bus modes are selected depending on the setting of the MISCR register.

The data transfer rate of the FIFO bus interface is up to 66 MHz in both the bus modes.

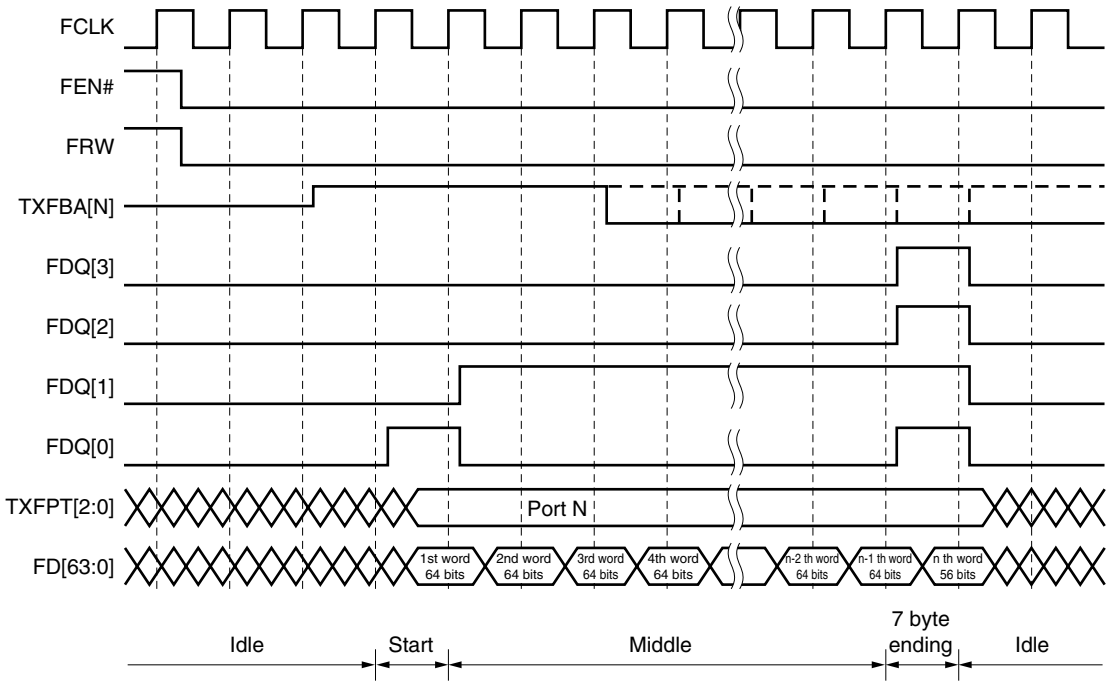
(1) Transmit FIFO bus interface operation

Figure 3-5. FIFO Interface Write Timing

(a) Example in 32-bit dual bus mode



(b) Example in 64-bit single bus mode



In the 32-bit dual bus mode, writing data to the transmit FIFO is enabled by making the TXFEN# signal low. In the 64-bit single bus mode, the FEN# and FRW signals are made low.

When these signals are asserted, the TXFBAn signal function of all the ports is enabled. Each port makes the TXFBAn signal high if the data stored in the transmit FIFO does not exceed the value set by the TFDMH field of the TFIC register. In this way, the host system can recognize that a quantity of free space set in advance is available in the transmit FIFO for each port.

When the high level of the TXFBAn signal is recognized, the host system starts writing transmit data. The host system prepares necessary data on TXFPT[2:0], TXFD[31:0], and TXFDQ[3:0] in the 32-bit dual bus mode, and on TXFPT[2:0], FD[63:0], and FDQ[3:0] in the 64-bit single bus mode.

TXFPT[2:0] are signals that specify the port number of the port that transmits packets. The host system gives the port number of the transmit FIFO to which it will write data, to these pins. TXFD[31:0] and FD[63:0] are the data buses through which data is written to the transmit FIFO in the respective bus modes. TXFDQ[3:0] and FDQ[3:0] are signals indicating the attribute of the data on the FIFO data bus, and input the attribute of the data on TXFD[31:0] or FD[64:0] in each bus mode of the host system.

The attributes of data include idle, data start, intermediate, and data end. If end data includes a fraction, this data attribute informs the μPD98431 that fraction processing is necessary. In addition, automatic appending of a CRC code can be also instructed by setting an attribute. Tables 3-1 and 3-2 show the relations between TXFDQ[3:0] and FDQ[3:0] inputs, and data attributes.

Table 3-1. TXFDQ Pins and Transmit Data Attributes (32-Bit Dual Bus)

TXFDQ pins				Data Attribute	Valid Data Byte Position	
[3]	[2]	[1]	[0]		Little Endian	Big Endian
0	0	0	0	Idle	–	–
0	0	0	1	Data start	TXFD[31:0]	TXFD[31:0]
0	0	1	0	Intermediate data	TXFD[31:0]	TXFD[31:0]
0	0	1	1	Data start (with CRC appended)	TXFD[31:0]	TXFD[31:0]
0	1	×	×	Reserved	–	–
1	0	0	0	Data end 0	TXFD[31:0]	TXFD[31:0]
1	0	0	1	Data end 1	TXFD[7:0]	TXFD[31:24]
1	0	1	0	Data end 2	TXFD[15:0]	TXFD[31:16]
1	0	1	1	Data end 3	TXFD[23:0]	TXFD[31:8]
1	1	×	×	Reserved	–	–

Table 3-2. FDQ Pins and Transmit Data Attributes (64-Bit Single Bus)

FDQ pins				Data Attribute	Valid Data Byte Position	
[3]	[2]	[1]	[0]		Little Endian	Big Endian
0	0	0	0	Idle	–	–
0	0	0	1	Data start	FD[63:0]	FD[63:0]
0	0	1	0	Intermediate data	FD[63:0]	FD[63:0]
0	0	1	1	Data start (with CRC appended)	FD[63:0]	FD[63:0]
0	1	×	×	Reserved	–	–
1	0	0	0	Data end 0	FD[63:0]	FD[63:0]
1	0	0	1	Data end 1	FD[7:0]	FD[63:56]
1	0	1	0	Data end 2	FD[15:0]	FD[63:48]
1	0	1	1	Data end 3	FD[23:0]	FD[63:40]
1	1	0	0	Data end 4	FD[31:0]	FD[63:32]
1	1	0	1	Data end 5	FD[39:0]	FD[63:24]
1	1	1	0	Data end 6	FD[47:0]	FD[63:16]
1	1	1	1	Data end 7	FD[55:0]	FD[63:8]

For details of little endian and big endian, refer to **3.7.1 (4) Little endian/big endian**.

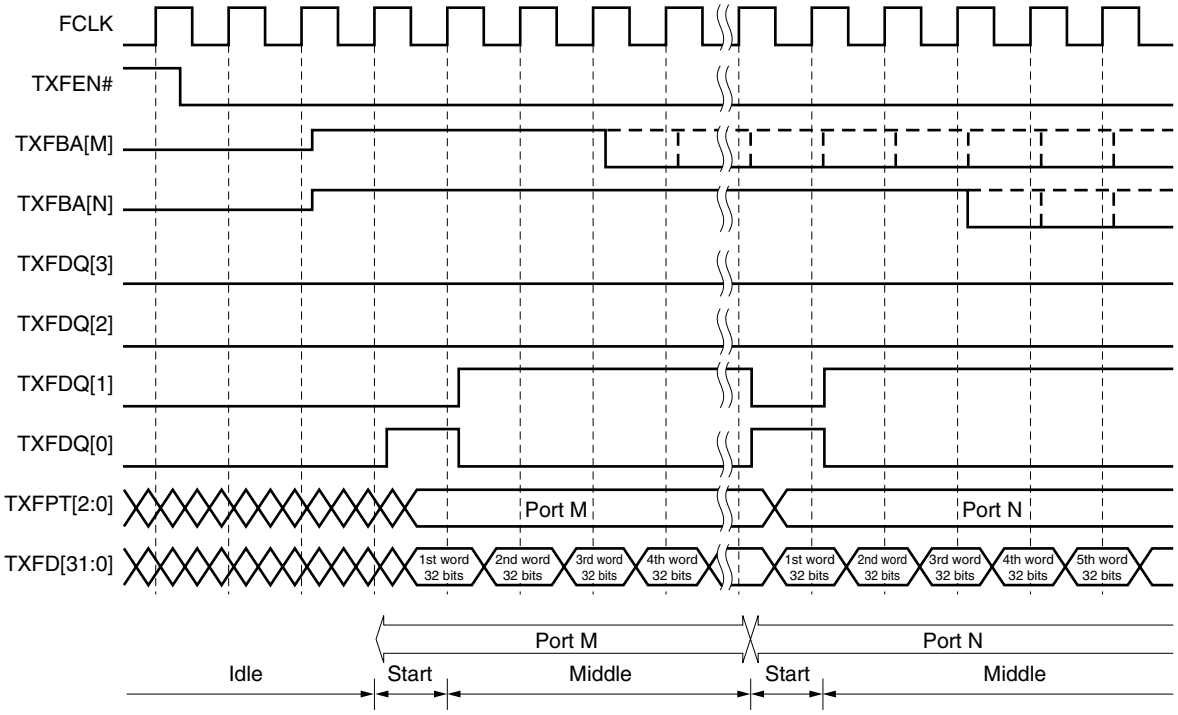
Once data start has been written, the rest of the data is written to the transmit FIFO by means of burst transfer.

If the quantity of the data in the transmit FIFO exceeds the value set to the TFDWH field of the TFIC register, the TXFBAn signal goes low. By specifying idle in the middle of burst transfer, writing to the transmit FIFO can be postponed.

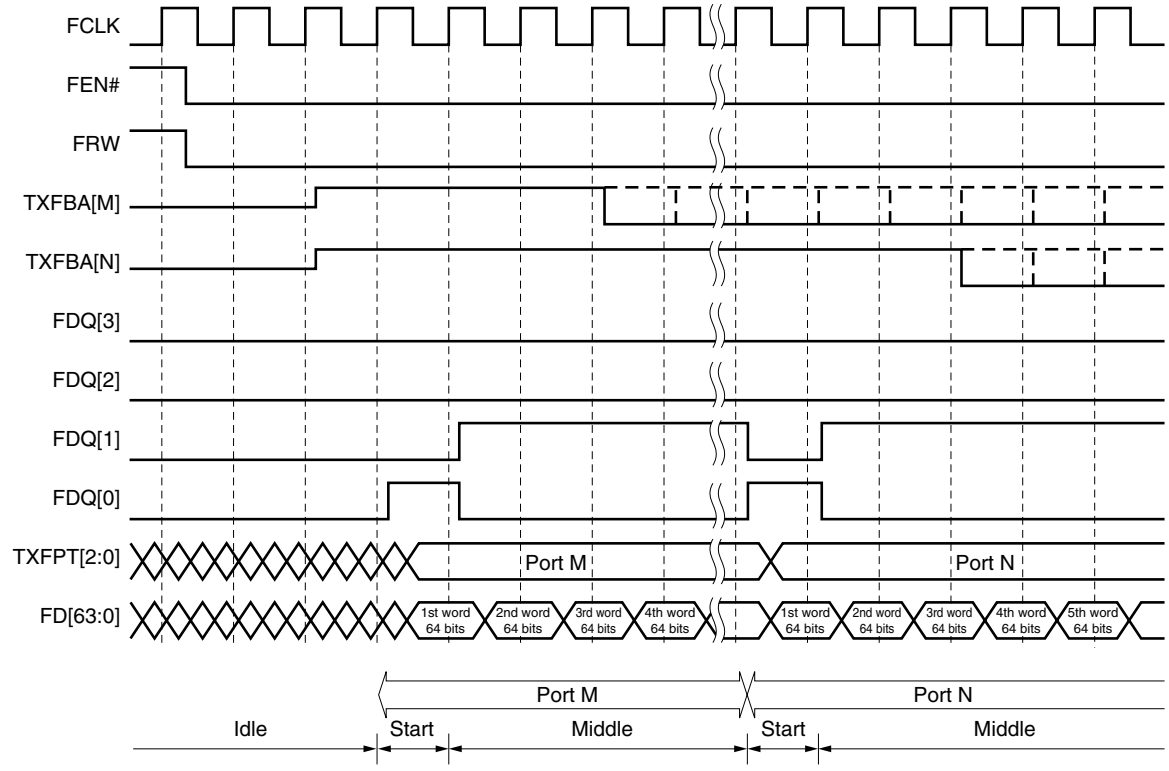
By changing TXFPT[2:0] while data is written to the transmit FIFO, the transmit data can be written to the transmit FIFO of another port. In this case, the data can be written to other port at the rising edge of FCLK immediately after TXFPT[2:0] has been changed. However, it is necessary to confirm that the TXFBA signal corresponding to the other port is high. The data stream written to the other port can be started from data having any attributes of the data start, intermediate data, and end data, so that the transmit packet can be divided into blocks and sequentially written to each of the ports. Each time a port is changed, however, the attribute of the data to be written must be correctly provided to it. Figure 3-6 shows an example of changing the port to which the transmit data is to be written using TXFPT[2:0].

Figure 3-6. Timing for Changing Transmit Data Write Port Using TXFPT[2:0]

(a) Example in 32-bit dual bus mode



(b) Example in 64-bit single bus mode



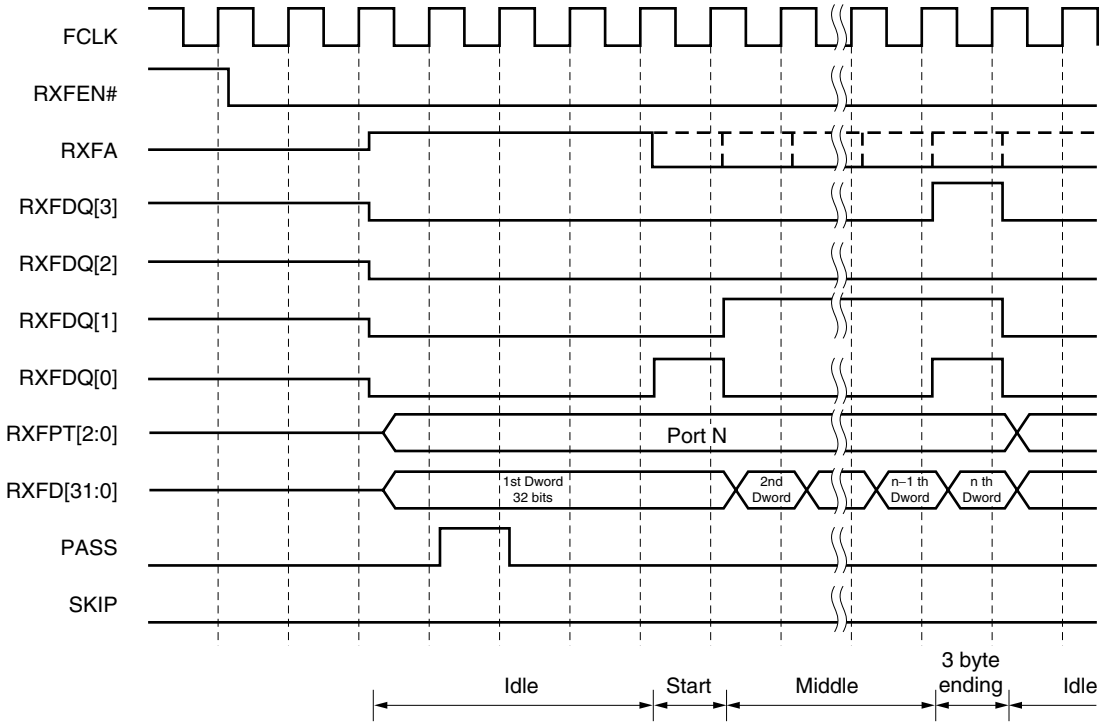
If a cause that aborts transmission of a packet (such as excessive collision or excessive defer) occurs while data is written to the transmit FIFO, the transmit packet data that has already been accumulated in the transmit FIFO is cleared. Data written to the transmit FIFO after the abortion has taken place is ignored until attribute data indicating the end of the data (EOF) is provided to the TXFDQ or FDQ pin. The host system can write the next packet after inputting EOF.

If a cause that aborts transmission occurs in the transmit packet that has been already accumulated in the transmit FIFO and is waiting to be transmitted while data is written to the transmit FIFO, transmission of that packet is canceled, and the rest of the packets in the transmit FIFO are cleared. At this time, the other packet data accumulated in the transmit FIFO or the packet data currently written are not affected.

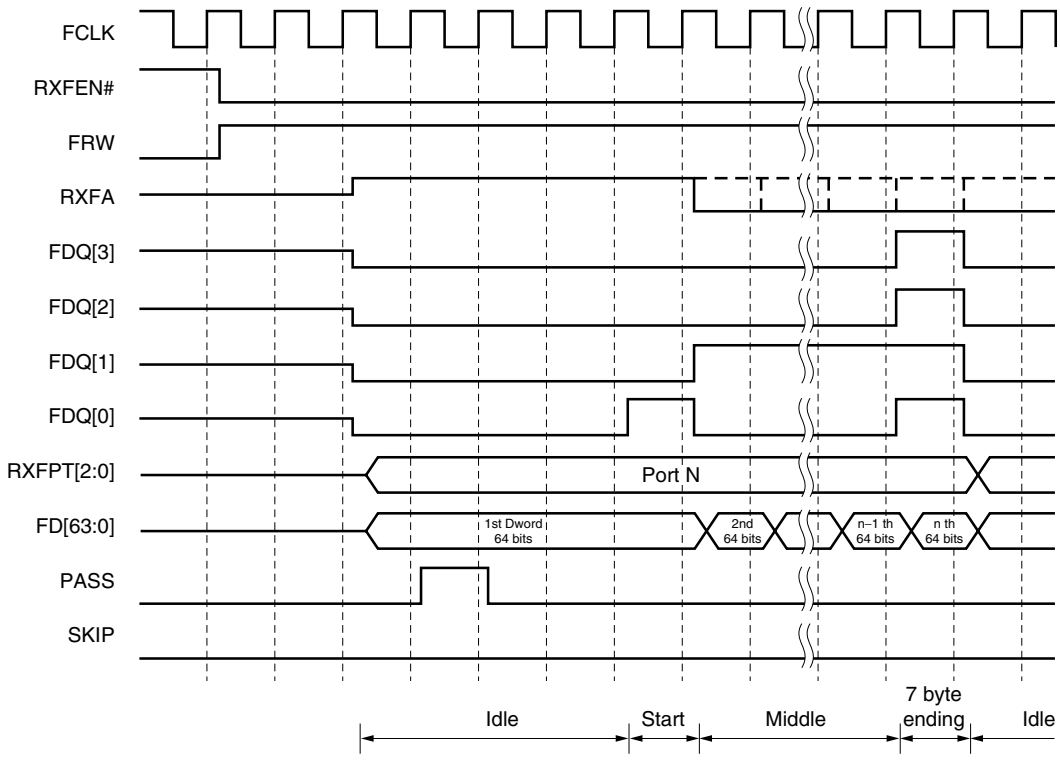
(2) Receive FIFO bus interface operation

Figure 3-7. FIFO Interface Read Timing

(a) Example in 32-bit dual bus mode



(b) Example in 64-bit single bus mode



The μPD98431 starts data transfer to the host system after reception from the network side has been completed and one packet of data has been completely stored in the receive FIFO. Data is read from the receive FIFO in the following procedure:

(a) Reading from receive FIFO

Reading data from the receive FIFO is enabled by making the RXFEN# signal low in the 32-bit dual bus mode. In the 64-bit single bus mode, it is enabled by making the FEN# signal low and the FRW signal high.

The μPD98431 starts reading the port numbers of the receive FIFOs via the FIFO bus interface. First, when reading from the receive FIFO is enabled, the μPD98431 scans the receive FIFO of each port to check to see if one packet of receive data is completely stored in the receive FIFO of any port. If one packet of data is stored in any of the receive FIFOs, the μPD98431 makes the RXFA signal high to inform the host system that it is ready to transfer the receive data. At the same time, the μPD98431 outputs the port number of the receive FIFO that is ready for data transfer, to RXFPT[2:0]. After the host system recognizes RXFPT[2:0], it must input the PASS signal to read data from the receive FIFO of the port. When the PASS signal is input, the receive data can be read from RXFD[31:0] or FD[63:0] in the burst format as a receive data stream synchronized with FCLK.

As soon as the receive data has been read, the μPD98431 outputs the data attribute on the FIFO data bus to the RXFDQ or FDQ signal in each bus mode. If a fraction occurs in the byte units at the end of the receive data, the valid byte position can be checked by using this data attribute.

Tables 3-3 and 3-4 show the relation between the RXFDQ[3:0] and FDQ[3:0] outputs, and data attribute.

Table 3-3. RXFDQ Pin and Receive Data Attribute (32-Bit Dual Bus)

RXFDQ Pin				Data Attribute	Valid Data Byte Position	
[3]	[2]	[1]	[0]		Little Endian	Big Endian
0	0	0	0	Idle	–	–
0	0	0	1	Data start	TXFD[31:0]	TXFD[31:0]
0	0	1	0	Intermediate data	TXFD[31:0]	TXFD[31:0]
0	0	1	1	Reserved	–	–
0	1	0	0	Status information (first)	TXFD[31:0]	TXFD[31:0]
0	1	0	1	Status information (last)	TXFD[31:0]	TXFD[31:0]
0	1	1	×	Reserved	–	–
1	0	0	0	Data end 0	TXFD[31:0]	TXFD[31:0]
1	0	0	1	Data end 1	TXFD[7:0]	TXFD[31:24]
1	0	1	0	Data end 2	TXFD[15:0]	TXFD[31:16]
1	0	1	1	Data end 3	TXFD[23:0]	TXFD[31:8]
1	1	×	×	Reserved	–	–

Table 3-4. FDQ Pin and Receive Data Attribute (64-Bit Single Bus)

FDQ Pin				Data Attribute	Valid Data Byte Position	
[3]	[2]	[1]	[0]		Little Endian	Big Endian
0	0	0	0	Idle	–	–
0	0	0	1	Data start	FD[63:0]	FD[63:0]
0	0	1	0	Intermediate data	FD[63:0]	FD[63:0]
0	0	1	1	Reserved	FD[63:0]	FD[63:0]
0	1	0	0	Status information (first)	FD[31:0]	FD[63:32]
0	1	0	1	Status information (last)	FD[31:0]	FD[63:32]
0	1	1	×	Reserved	–	–
1	0	0	0	Data end 0	FD[63:0]	FD[63:0]
1	0	0	1	Data end 1	FD[7:0]	FD[63:56]
1	0	1	0	Data end 2	FD[15:0]	FD[63:48]
1	0	1	1	Data end 3	FD[23:0]	FD[63:40]
1	1	0	0	Data end 4	FD[31:0]	FD[63:32]
1	1	0	1	Data end 5	FD[39:0]	FD[63:24]
1	1	1	0	Data end 6	FD[47:0]	FD[63:16]
1	1	1	1	Data end 7	FD[55:0]	FD[63:8]

For details of how to append status information, refer to **3.7.1 (2) (c) Appending status information**. For details of little endian/big endian, refer to **3.7.1 (4) Little endian/big endian**.

When reading of the one packet specified by RXFPT has been completed, the μPD98431 then makes the RXFA signal high if any of the ports is ready for reading receive data, outputs the port number to RXFPT, and waits for reading the next receive data.

The RXFA signal remains high if receive data ready to be read exists in the port indicated by RXFPT. However, the RXFA signal goes low once if control is transferred to another port by the SKIP signal while the first port is read.

The sequence in which the ports of the μPD98431 transfer receive data is predetermined. Port 0 first transfers data, followed by port 1, port 2, and so on. After port 7 has transferred data, port 0 transfers data again. If one packet of receive data has not been completely accumulated in the next port when it is selected, however, that port is skipped, and the port after the next one is selected.

Figure 3-8 shows an example of timing at which reading the next port is started after reading of the receive port from a specific port has been completed.

Figure 3-8. Timing for Changing Port After Completion of Received Data Read (1/2)

(a) Example in 32-bit dual bus mode

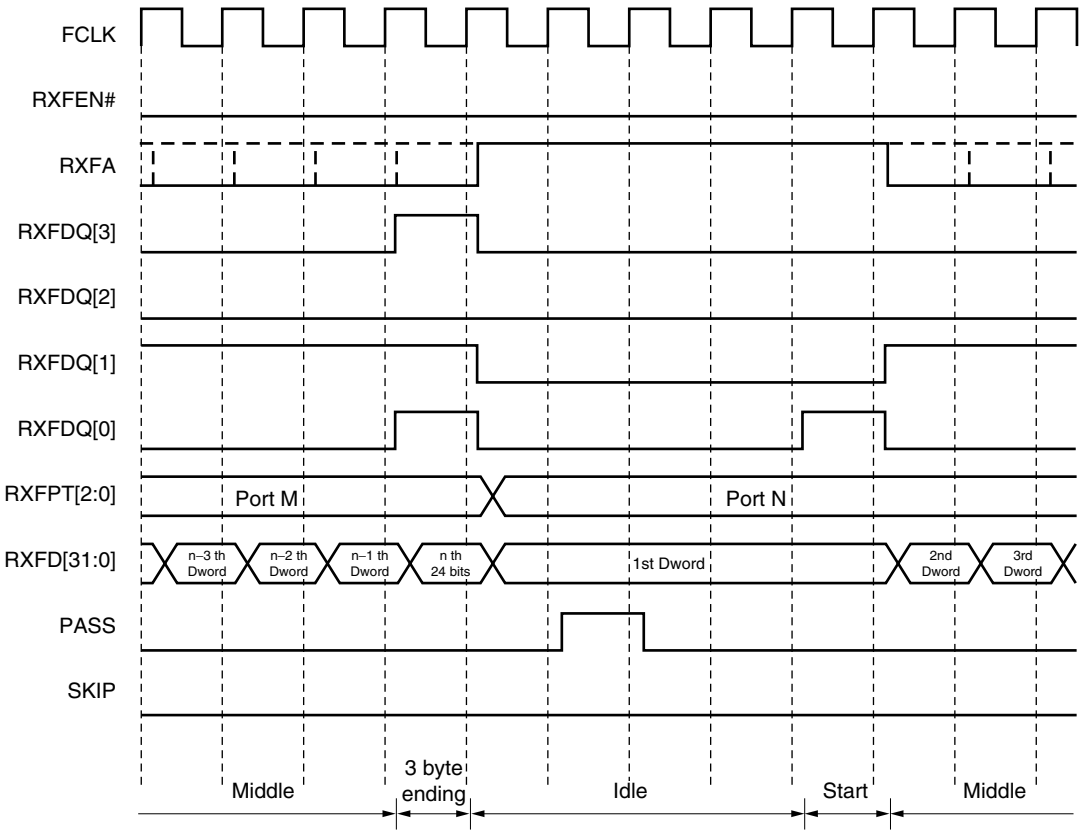
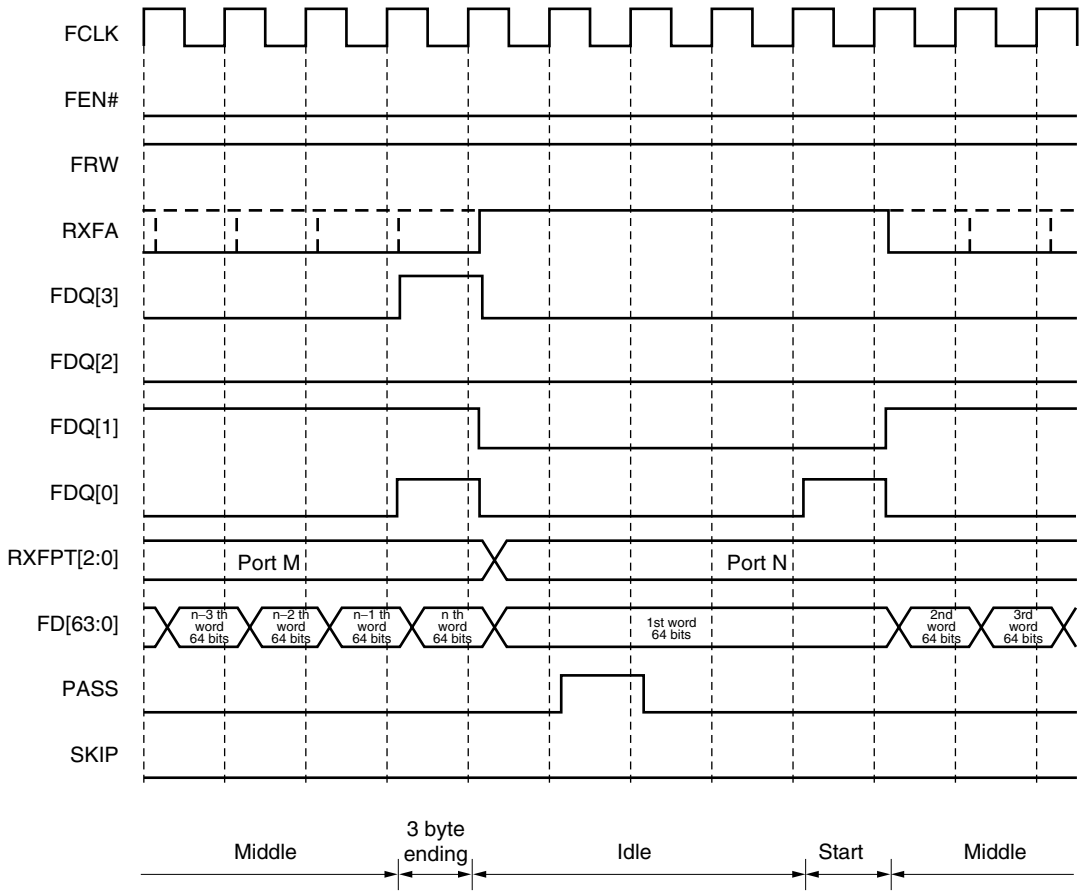


Figure 3-8. Timing for Changing Port After Completion of Received Data Read (2/2)

(b) Example in 64-bit single bus mode



The filtering condition of the receive data written from the network side to the receive FIFO can be set by using a register. If the register is set so that a packet including a CRC error, control frame, or short packet is not received, these packets are stored briefly in the receive FIFO. However, the contents of the receive FIFO are cleared when the CRC error is confirmed, and the μPD98431 does not inform the host system that it stored the packets. The same applies to address filtering. A packet that does not satisfy the filtering condition is deleted from the receive FIFO and is not transferred to the host system.

If the receive FIFO overflows, the packet being received is written to the receive FIFO. However, the data already stored in the receive FIFO after the overflow has been detected is cleared and is not transferred to the host system.

If data less than 8 bytes long is stored in the receive FIFO from the network side, the receive FIFO unconditionally deletes this data.

(b) SKIP signal

The port number of the receive FIFO whose data is read through the FIFO bus is instructed by the μPD98431. By inputting the SKIP signal when the RXFA signal goes high after reading the receive FIFO has been enabled or while receive data is being read by means of burst transfer, the host system can read being a port other than the one specified by the μPD98431.

As described above, the sequence in which receive data is transferred is predetermined, and the SKIP signal is used to forcibly change the port from which receive data is to be read next, under the instruction of the host system.

When the SKIP signal is input, the μPD98431 stops reading the receive data from the current port, outputs 0000B to the RXFDQ or FDQ pin, and enters idle status. The RXFA signal goes low once. Next, it outputs the port number of the next port that is ready for transferring receive data to the RXFPT and makes the RXFA signal high again. If the PASS signal is input from the host system at this time, data is read from the next port.

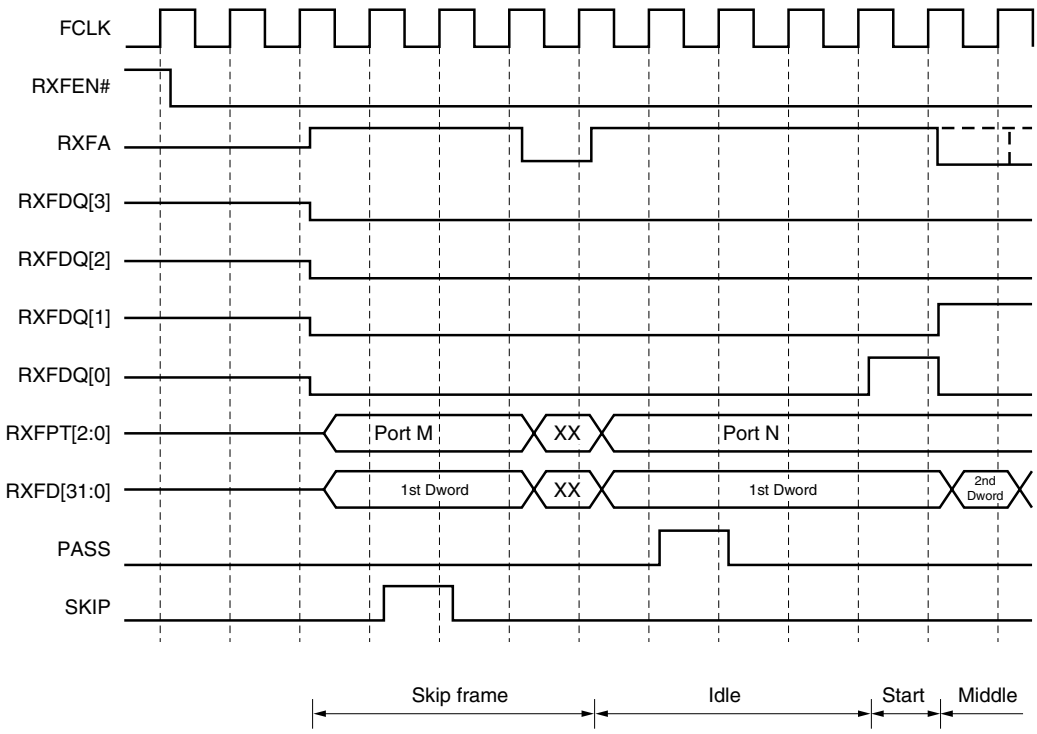
The data of the port that is skipped by the SKIP signal is retained. If reading the receive data of the other port has been completed or if the original port is selected by input of the new SKIP signal, the port that was skipped waits for input of a new PASS signal, and then starts transferring the rest of the receive data.

Figure 3-9 shows an example of selecting a port using the SKIP signal before starting to read data. In this case, a port is selected two clocks of FCLK after the SKIP signal has been detected.

Do not input the SKIP signal for the duration of two or more clocks. To skip two or more ports in a row by inputting the SKIP signal two times or more, input the next SKIP signal after confirming that the new port has been selected after inputting the first SKIP signal for the duration of one clock.

Figure 3-9. Timing for Changing Port to Be Read Using SKIP Signal (Before Port Is Read)

(a) Example in 32-bit dual bus mode



(b) Example in 64-bit single bus mode

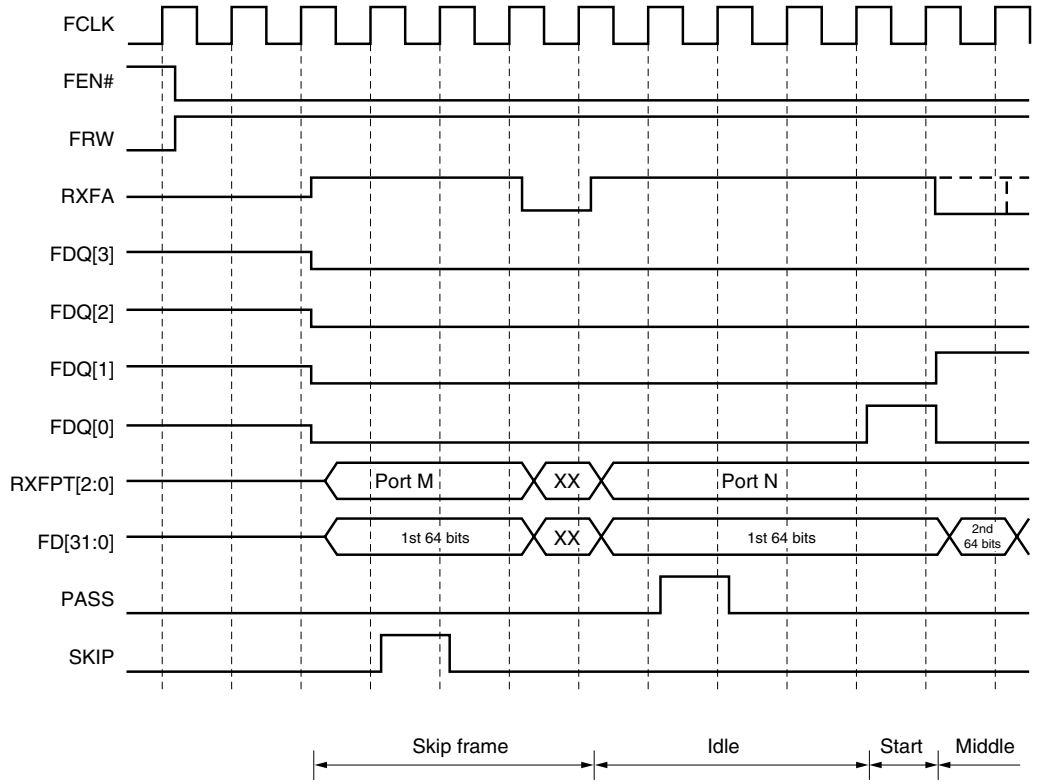


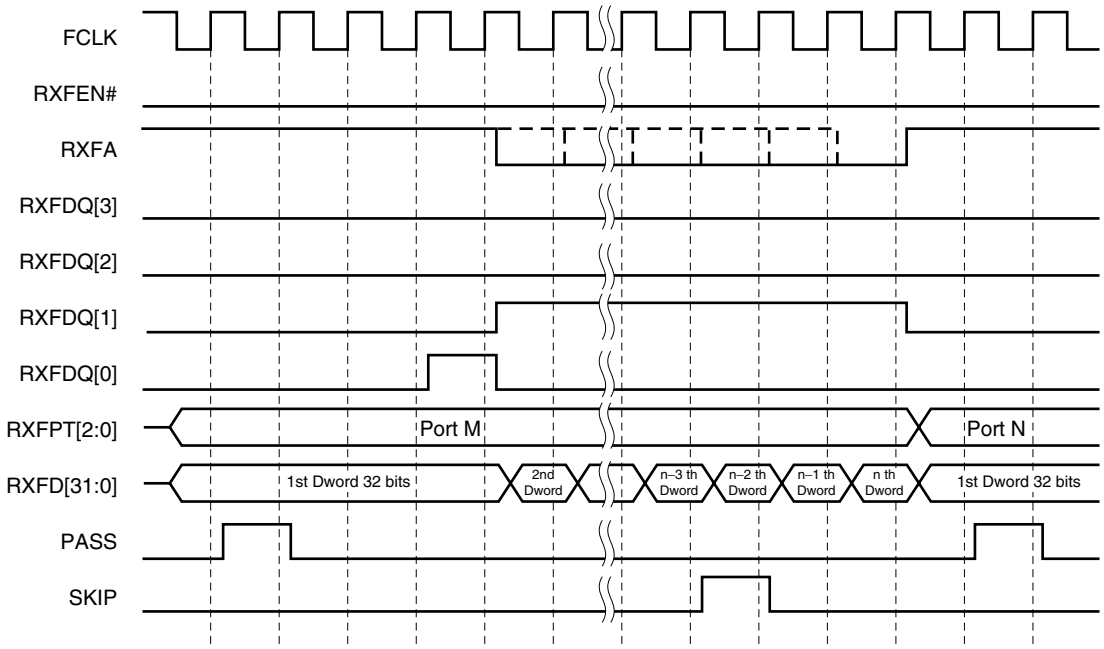
Figure 3-10 shows a timing example of changing the port by inputting the SKIP signal while the port is read. In this case, the new port is selected two clocks of FCLK after the SKIP signal has been detected. The μPD98431 outputs valid receive data for the duration of two clocks, until the new port is selected. If data is read from the port that has been skipped by the SKIP signal (if readable receive data does not exist in any other port), the original port is indicated by RXFPT[2:0] two clocks after the valid data of two clocks (refer to **Figure 3-10 (b)** and **(d)**). Because the μPD98431 is in IDLE status when the next port is indicated after the SKIP signal has been input, inputting the PASS signal is necessary for starting to read.

If the port that has been skipped by the SKIP signal is selected again, the port starts outputting receive data next to the one that was output last when the port was skipped. By using the SKIP signal, therefore, the data received by each port can be divided into blocks and read. Determine a unit in which data is to be divided and read, and input the SKIP signal in that unit until the data end attribute appears on the RXFDQ or FDQ signal. In this way, each port can be successively read in units of reading. Unlike writing data to the transmit FIFO, however, the μPD98431 specifies a port to be read.

★ Do not input the SKIP signal and the PASS signal for the duration of two or more clocks. To skip a port by inputting the SKIP signal two times or more, confirm that a new port is selected after the first SKIP signal has been input for the duration of one clock, and then input the next SKIP clock.

Figure 3-10. Timing for Changing Port to Be Read Using SKIP Signal (While Port Is Read) (1/2)

(a) Example in 32-bit dual bus mode (if the next port is not the port skipped)



(b) Example in 32-bit dual bus mode (if the next port is the port skipped)

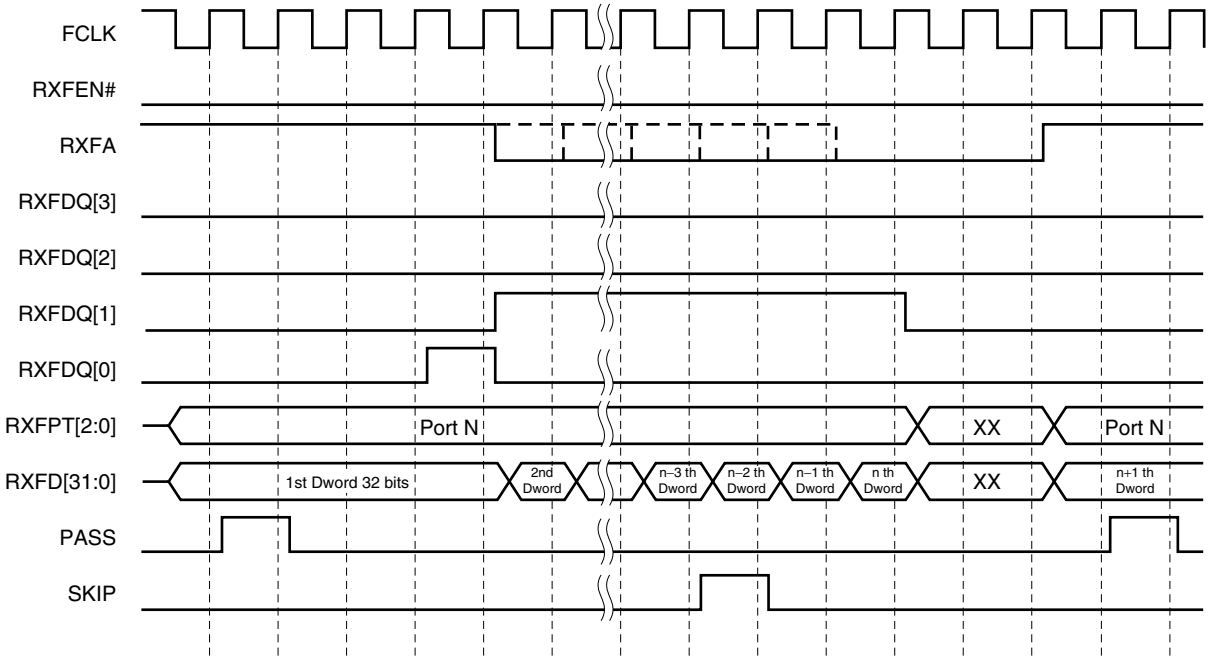
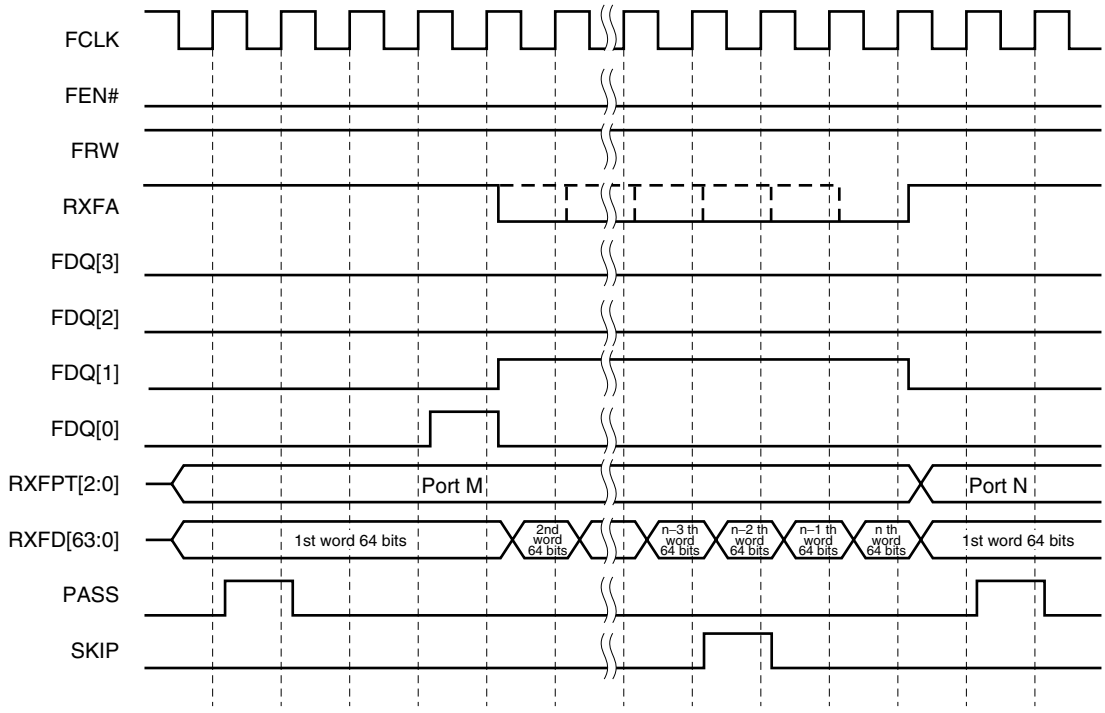
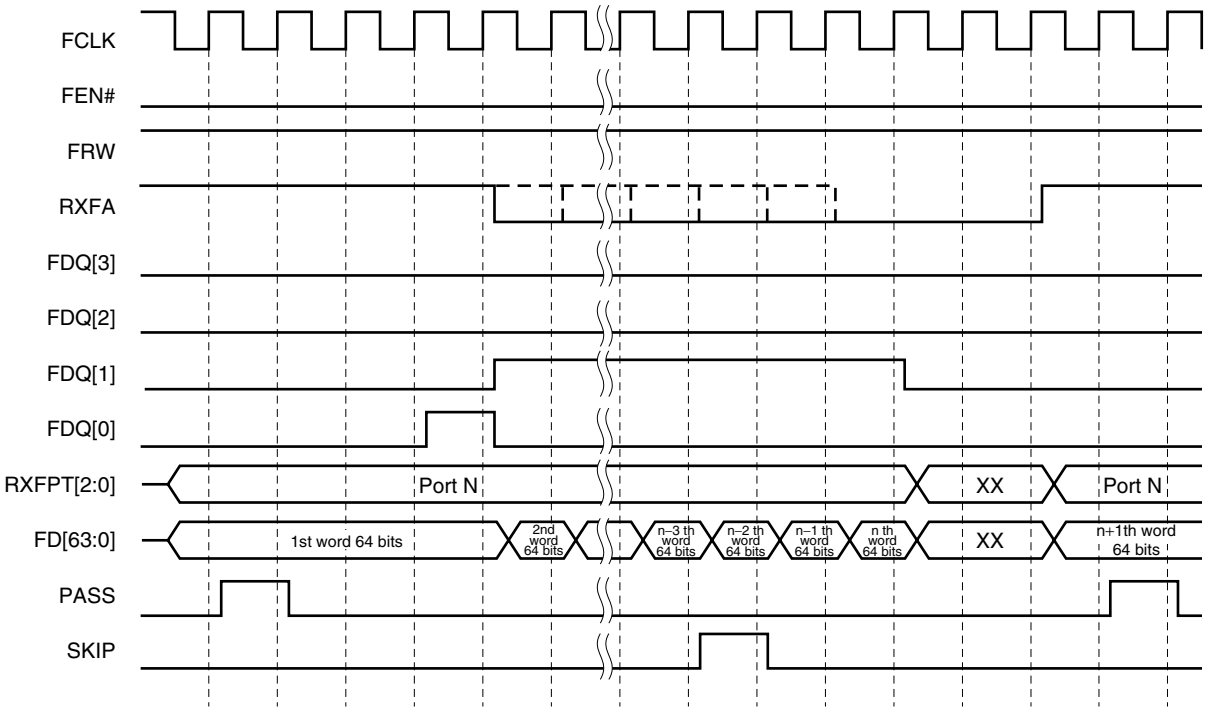


Figure 3-10. Timing for Changing Port to Be Read Using SKIP Signal (While Port Is Read) (2/2)

(c) Example in 64-bit single bus mode (if the next port is not the port skipped)



(d) Example in 64-bit single bus mode (if the next port is the port skipped)



(c) Appending status information

The μPD98431 can append the status information of a packet to the receive data stream that is read from the FIFO bus. When the APSS bit of the MACC3 register is set to 1, the status information on the packet to be read is prefixed to the receive data stream. If the APSE bit of the MACC3 register is set to 1, the status information is suffixed to the receive data stream. The status information that is appended is the contents of the RSVREG register that are updated each time a packet has been received. These contents are appended as 32-bit data.

(3) Timing for changing access direction of FIFO bus in 64-bit single bus mode

Figure 3-11 shows the timing for switching between reading receive data and writing transmit data in the 64-bit single bus mode. Be sure to deassert the FEN# signal once before switching the operation from reading to writing or vice versa.

If the FEN# signal is deasserted during a write operation, detection of deasserting the FEN# signal to the next rising edge of FCLK is assumed as valid writing.

If the FEN# signal is deasserted during a read operation, the valid data is output after detection of deasserting the FEN# signal until the FCLK rises the next time. If the data read last after the FEN# signal has been deasserted is the intermediate data of the packet being read, however, the internal operation of the chip to read data from the receive FIFO is not stopped by deasserting the FEN# signal. Consequently, the rest of the data cannot be correctly read when reading is resumed. To avoid this, confirm the end of data by completely reading the packet before deasserting the FEN# signal, or input the SKIP signal to set the FIFO bus in IDLE status and then deassert the FEN# signal.

Figure 3-11. Timing for Changing FIFO Bus Read/Write in 64-Bit Single Bus Mode (1/2)

(a) Example of timing for changing write cycle to read cycle

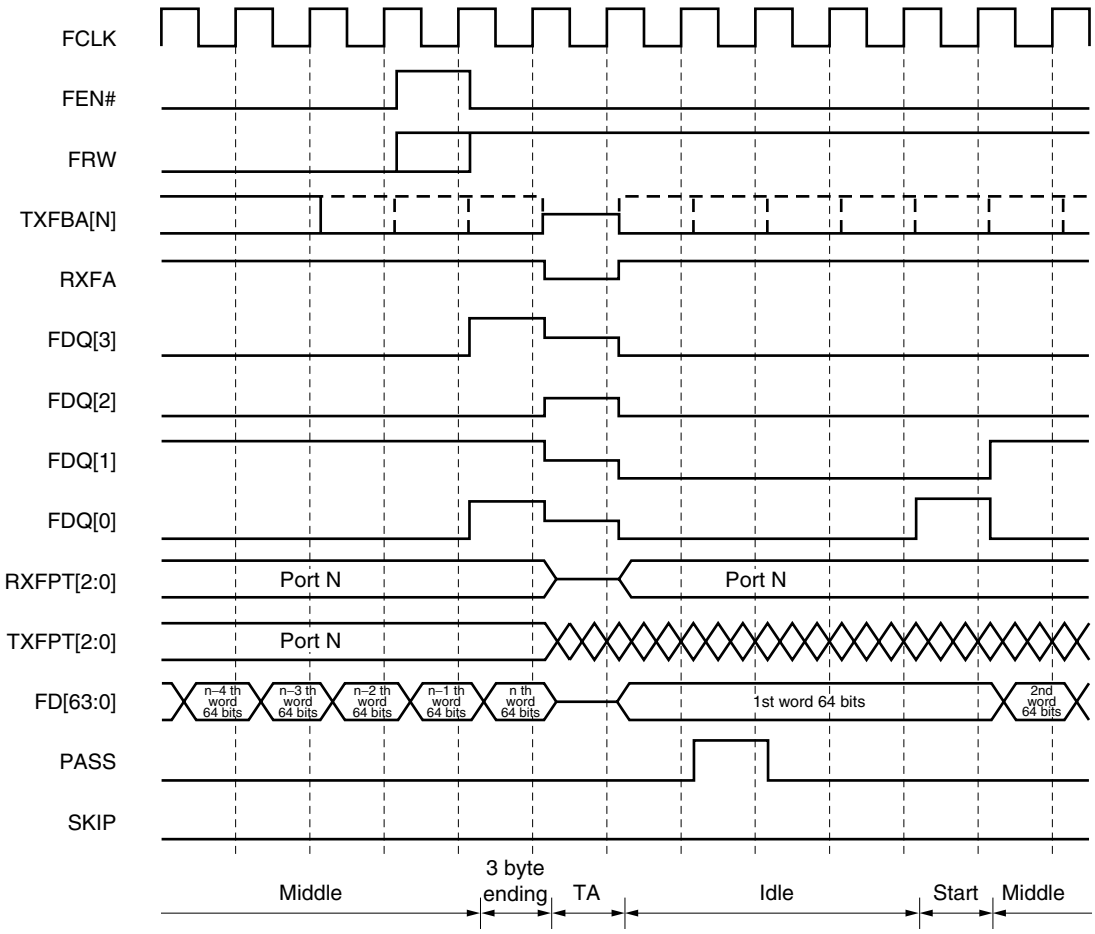
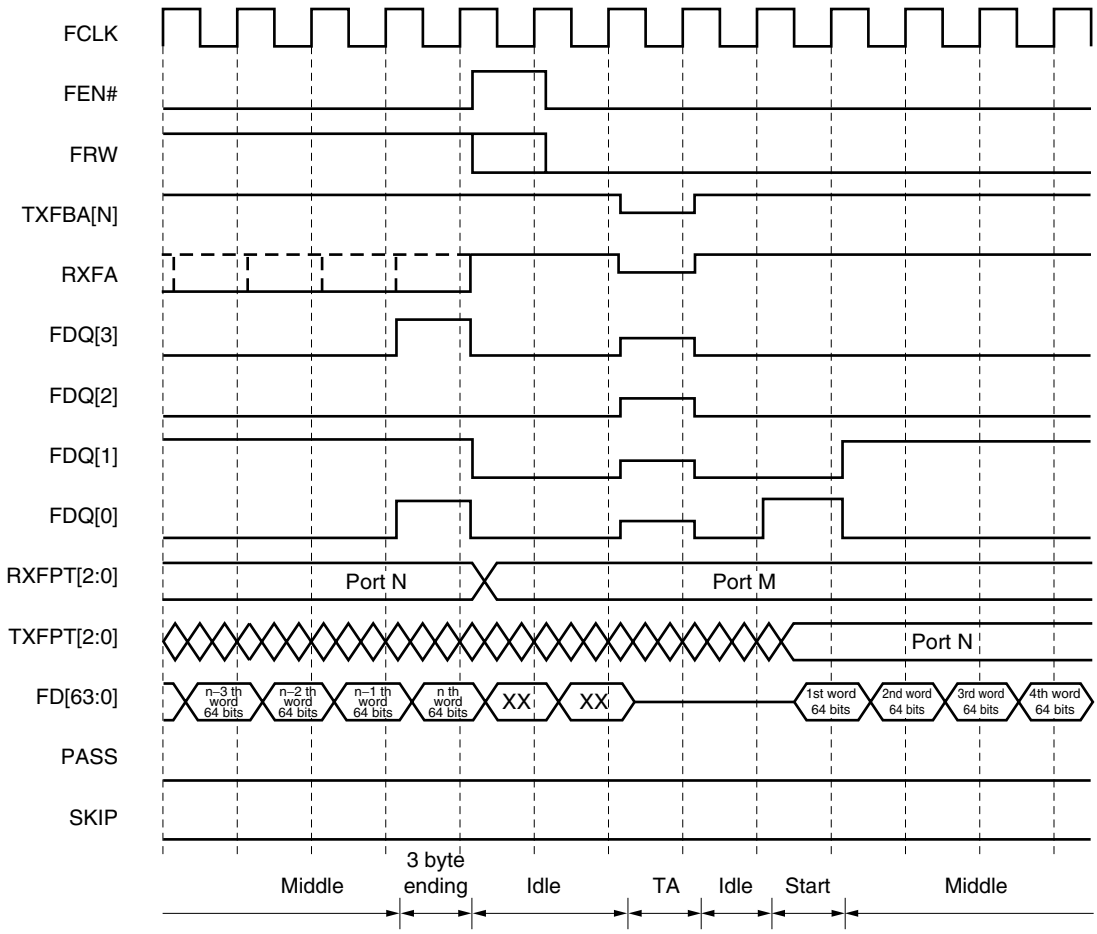


Figure 3-11. Timing for Changing FIFO Bus Read/Write in 64-Bit Single Bus Mode (2/2)

(b) Example of timing for changing read cycle to write cycle



(4) Little endian/big endian

The μPD98431 has a function to select little endian or big endian as the byte order of the transmit/receive data on the FIFO interface. Little endian or big endian is selected by using the BUSMODE bit of the MACC3 register.

In the little endian mode, data is transferred starting from the least significant byte of the data bus. In the big endian mode, data transfer starts from the most significant byte. The setting of the BUSMODE bit of the MACC3 register does not influence the byte order of the register bus interface.

3.7.2 Register bus interface

The μPD98431 provides a register bus interface via which the internal registers of the μPD98431, such as control registers and statistics counters, can be accessed. The register bus interface consists of a 32-bit bidirectional data bus and an 11-bit address bus and control signals (CS#, RW, and ACK# signals).

(1) Controlling reading/writing registers

To read an internal register of the μPD98431, the host system sets the address of the register to be read in A[10:0], and makes the RW signal high and the CS# signal low. The μPD98431 recognizes read access by the host system by checking the statuses of the RW and CS# signals. Then it makes the ACK# signal high once and reads the necessary data. When the read data is written to D[31:0], the μPD98431 makes the ACK# signal low. After the ACK# signal has gone low, the host system reads the data in D[31:0], and then returns the CS# signal to the high level. The host system must keep the statuses of the A[10:0], RW, and CS# signals until the ACK# signal has gone low and the host system reads the data. When the host system reads data and makes the CS# signal high, the μPD98431 completes the read cycle. The ACK# signal goes low for the duration of one cycle of HCLK.

To write data to an internal register of the μPD98431, the host system writes the address of the register to which data is to be written, to A[10:0], and the write data to D[31:0]. It then makes the RW and CS# signals low. When the μPD98431 recognizes the write access by the host system by checking the statuses of the RW and CS# signals, it makes the ACK# signal high once, and starts writing data to D[31:0]. After writing has been completed, the μPD98431 makes the ACK# signal low to report to the host system. The host system must keep the statuses of the A[10:0], D[31:0], RW, and CS# signals until the ACK# signal goes low and the host system has completed writing data. When writing has been completed and the host system makes the CS# signal high, the μPD98431 completes the write cycle. The ACK# signal goes low for the duration of one cycle of HCLK.

(2) Register address mapping

The registers accessed by the host system are classified as port control registers, statistics counters, and global registers. A port control register and a statistics counter are provided for each port and are used to read the setting of the operation, status information, or statistics information of each port. The global register is used to perform setting related to all the ports and is used for all the ports.

These registers are specified by the address data in A[10:0]. A[10:0] consists of two parts. The port number of the port whose register is to be accessed is written to the high-order bits, A[10:8], and the address of the register to be accessed is written to the low-order bits, A[7:0]. Figure 3-12 shows an example of relation between a port number and a register address for reference.

Figure 3-12. Register Address Bus

A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Port number			Register address							

Example: To access MACC3 register (register address: 90H) of port 3

A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	1	1	0	0	1	0	0	0	0

To access the global register, the value of A[10:8] is ignored.

The registers related to the MII management interface (MIIC, MCMD, MADR, MWTD, MRDD, and MIND registers) are valid only when the port number is set to 0.

(3) Interrupt servicing

If an interrupt occurs, the μPD98431 makes the INT# signal low to report to the host system. The sources of interrupts are as follows:

- Transmit packet status information indicated by TSVREG1 register
- Receive packet status information indicated by RSVREG register
- FIFO status information indicated in FSVREG register
- Overflow of statistics counter indicated by CAR1 and CAR2 registers

After the INT# signal has been asserted, the host system can check at which port the interrupt has occurred and by which status source the INT# signal has been asserted, by reading the STIR register. By reading the status register of the corresponding port, the host system can identify the interrupt source in detail.

If an interrupt source that asserts the INT# signal is generated in the status register provided for each port, the corresponding bit of the STIR register is set to 1. Even if the STIR register has been read, neither the status register nor the INT# signal is cleared.

An interrupt mask can be specified for each interrupt source. If an interrupt is caused by a masked source, the corresponding bit of each status register is set to 1. However, the INT# signal is not asserted, nor is the corresponding bit of the STIR register set to 1.

Each status register is automatically cleared when it is read while the SRRC bit of the MISCR register is set to 1. The INT# signal is deasserted when the status registers of all the ports (except the masked bits) have been cleared.

3.8 Network Interface

The μPD98431 has an MII (Media Independent Interface) and a 10 Mbps serial interface to interface the network. The interface to be used can be selected for each port by using the EXINT bit of the PCSC register.

3.8.1 MII (Media Independent Interface)

The MII is an interface defined by IEEE802.3u. This interface transmits or receives data independently of the media type (STP, UTP, or optical fiber) and transfer rate (10 Mbps or 100 Mbps). This interface has a data bus 4 bits (nibble) wide to transmit or receive data, and control signals. In addition, a two-wire serial interface and an MII management interface are also provided to implement access between the μPD98431 and PHY device by using the MII management frame.

The μPD98431 supports transmission/reception, nibble data bus, and control signals for each port. It is provided with one MII management interface port.

3.8.2 MII management interface

(1) MDC clock

The μPD98431 generates the MDC clock used for the MII management interface by dividing the clock input to the HCLK pin. To conform with the IEEE standard, the division ratio must be set in accordance with the HCLK input. The division ratio is set by the CLKS bit of the MIIC register. Table 3-5 shows the relation between the HCLK input and CLKS bit.

Table 3-5. CLKS Bit of MIIC Register and Frequency of HCLK

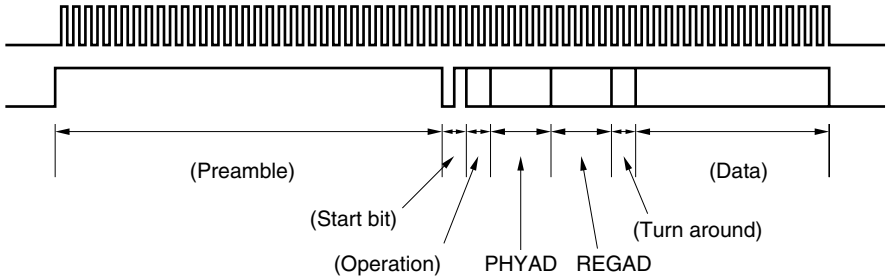
CLKS Bit of MIIC		Frequency Range of HCLK Input
Bit 3	Bit 2	
0	0	Not used
0	1	33 MHz MAX
1	0	50 MHz MAX
1	1	66 MHz MAX

The MDC is output only when a management frame is transmitted or received.

(2) MII management frame data

Figure 3-13 shows the MII management frame structure.

Figure 3-13. MII Management Frame Structure



The μPD98431 automatically generates a preamble and start bit in an MII management frame. The op code is automatically appended in accordance with reading/writing of a register of the external PHY device. PHYAD and REGAD indicate the device address of the PHY device and a register address of the PHY device, and the values set to the FIAD and RGAD fields of the MADR register are appended to PHYAD and REGAD.

Reading from the PHY device is executed when the RSTAT bit of the MCMD register is set to 1. Writing to the PHY device is executed by writing data to the CTLD field of the MWTD register.

The μPD98431 first outputs serial data from the preamble to REGAD as an MDIO signal, and after turn around, outputs the data set to the CLTD field of the MWTD register for write access. For read access, serial data is input from the MDIO signal and is written to the PRSD field of the MRDD register.

(3) Access procedure

The MII management frame is transmitted or received as follows:

First, the BUSY bit of the MIND register is checked to see if MII management access is currently in progress. If the BUSY bit is ON, the μPD98431 waits until it turns OFF. Next, the device address of the targeted external PHY device and the register address of the PHY device are written to the FIAD and RGAD fields of the MADR register, respectively.

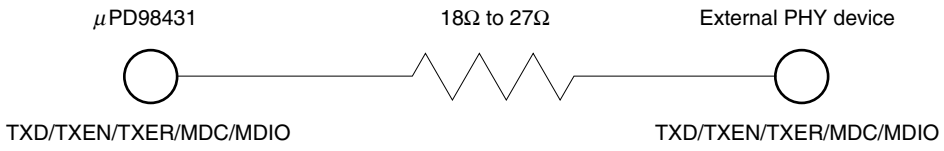
A write access is started by writing data to the CTLD field of the MWTD register. The BUSY bit turns ON when data has been written to the MWTD register, and turns OFF when the write access has been completed.

A read access is started when the RSTAT bit of the MCMD register is set to 1. When the RSTAT bit is set to 1, the BUSY bit turns ON. It turns OFF after the read access has been completed. The host system can obtain the read data by reading the PRSD field of the MRDD register after confirming that the BUSY bit has turned OFF.

3.8.3 Connecting μPD98431 MII output signal pins

To connect the MII output signals (TXD, TXEN, TXER, MDC, MDIO) to a PHY device, connect a series resistor of 18 Ω to 27 Ω to each MII output signal as shown in Figure 3-14, to make the driving capability of the MII output buffer conform to the IEEE802.3u standard.

Figure 3-14. Connecting MII Output Signal Pins



3.8.4 10 Mbps serial interface

The μPD98431 has a serial interface that connects a 10 Mbps transceiver. This interface consists of 1-bit serial data, clock, and control signals for both transmission and reception.

For the transmit interface of port n, TXCLKn, TXDn[0], and TXENn are used. To detect collision, the COLn signal is used. Transmit serial data is output from TXDn[0] at the rising edge of TXCLKn.

TXENn goes high when the data in TXDn[0] is valid.

For the receive interface of port n, RXCLKn, RXDn[0], and CRSn are used. The μPD98431 samples the receive serial data input from RXDn[0] at the rising edge of RXCLKn. If CRSn is high at this time, the μPD98431 assumes that the sampled data is valid receive data.

3.9 Flow Control

The μPD98431 implements flow control by processing the pause control frame defined by IEEE802.3x Annex31B.

The purpose of flow control is to lower the frequency at which packets are transmitted from the other terminals connected to the μPD98431 on a point-to-point basis for full-duplex operation.

When a pause control frame is received, the value of the pause timer field in the control frame is loaded to the pause timer in the MAC. If the pause timer is not 0, the next transmission is started after the time set by the pause timer has expired.

To suppress data transmission from other terminals on the network, a reserved multicast address (01-80-C2-00-00-01), pause op code, and a 16-bit pause timer value are generated and transmitted as a pause control frame.

3.9.1 Receiving control frame

The μPD98431 validates reception and detection of a control frame when the RXFC bit of the MACC1 register is 1. The pause control frame is detected by checking the destination address and op code of the type field. In order that the receive data stream is detected as a pause control frame, either the multicast address (01-80-C2-00-00-01) reserved as a destination address or the unicast address given to the MAC is necessary. In addition, 8808H is necessary for the length/type field, and the correct pause op code 0001H is necessary for the control op code field.

When the μPD98431 receives a valid pause control frame, it suppresses transmission for the duration specified by the pause timer value included in the received pause control packet.

3.9.2 Flow control pause timer

The flow control pause timer is a 16-bit timer and stores the pause timer value in the received pause control frame. If the pause timer value of the pause control frame is not 0, it indicates that a new frame should not be transmitted. If the pause timer value of the received control frame is 0, normal transmission is resumed.

If the RXFC bit of the MACC1 register is 0, the value loaded to the pause timer is ignored. The setting of the RXFC bit has nothing to do with the pause timer, and the pause timer is always updated when a valid control frame has been received. If the setting of the RXFC bit is changed, software reset must be executed by using the MCRST bit of the MACC2 register.

3.9.3 Transmitting pause control frame

The μPD98431 automatically generates and transmits a pause control frame, depending on the relation between the quantity of data in the receive FIFO and threshold values set by the RFDMH and RFDML fields of the RFIC1 register when the FLWCNT bit of the MACC3 register is 1.

When the FLWCNT bit is 1, and if the quantity of data in the receive FIFO exceeds the threshold level set by the RFDMH field, the μPD98431 automatically transmits the pause control frame. If a data frame is already being transmitted when the μPD98431 tries to transmit the pause frame, the μPD98431 waits until transmission of the data frame is completed, and then transmits the pause frame.

The pause control frame transmitted at this time is generated as follows. A reserved multicast address (01-80-C2-00-00-01) is given as a destination address by hardware, and the station address set by the LSA1 and LSA2 registers is appended as a source address. 8808H is appended to the length/type field, and a pause op code of 0001H is appended to the control op code field. In addition, the value set to the PTIME field of the MACC3 register is appended as the value of the pause timer.

After the quantity of data in the receive FIFO has exceeded the threshold value of the RFDMH field and the μPD98431 has automatically transmitted the pause control frame, the data stored in the receive FIFO is transferred to the upper layer. If the quantity of data in the receive FIFO falls below the threshold level set by the RFDML field as a result, the μPD98431 automatically generates and transmits a pause control frame with a pause timer value of 0, prompting resumption of transmission by the other party.

3.10 Back Pressure

The μPD98431 has a back pressure function. This function is valid only during half-duplex operation and is enabled if the quantity of data in the receive FIFO exceeds the threshold level set by the RFDMH field of the RFIC1 register when the BACKPE bit of the MACC3 register is 1. If packet detection is detected with this function enabled, a dummy packet is immediately transmitted, and collision is forcibly generated. When the data in the receive FIFO is transferred to the host system and if the data quantity of the receive FIFO falls below the value of the RFDMH field of the RFIC1 register as a result, this function is disabled.

3.11 Operation for VLAN Frames

The μPD98431 detects a VLAN frame by comparing the value set in advance in a register with the TPID field in a receive or transmit packet. This section explains the operation to be performed for a VLAN frame. The settings can be performed separately for each port, by using the register provided for each port.

3.11.1 Detecting VLAN frames

The μPD98431 always compares a 2-octet value of the TPID field that follows the source address in a transmit packet with the value of the VLTP register in the μPD98431. When the two values match it assumes the packet is a VLAN frame.

3.11.2 Receiving VLAN frames

If the value of the TPID field in a receive packet coincides with the value of the VLTP register, the VLAN bit of the RSVREG register is set to 1. At this time, judgment related to the receive frame size is made based on MAX: 1522 bytes, MIN: 64 bytes. If filtering is performed by using the SIFT bit of the RFIC2 register (discarding short packet), the reference packet is discarded when the data in the receive FIFO is less than 64 bytes even if the packet is recognized as a VLAN frame.

3.11.3 Transmitting VLAN frames

If the APD bit of the MACC2 register is set to 1, the length of the transmit packet that is regarded as a VLAN packet is judged based on MAX: 1522 bytes, MIN: 64 bytes. However, if the APD bit is 1 and the PADEN bit of the MACC1 register is 1, pad and CRC are automatically appended to the transmit packets regarded as VLAN packets with data of less than 68 bytes and the packets are transmitted as 68 bytes.

If a frame whose TPID field value does not coincide with the value of the VLTP register is transmitted, or if the APD bit is 0, the processing is based on the normal frame size (MAX: 1518 bytes, MIN: 64 bytes).

If the VPD bit of the MACC2 register is 1, all the packets transmitted are regarded as VLAN frames and the above operation proceeds, regardless of whether the TPID field value coincides with the VLTP register value. The setting of the VPD bit takes precedence over the setting of the APD bit.

3.12 Statistics Counters

The μPD98431 has a statistics counter set that is useful for implementing RMON and SNMP for each port. The statistics counter is a 32-bit counter and supplies the upper layer with a total of 41 pieces of information on transmission and reception.

The statistics counter counts and retains statistical parameters related to transmission/reception of packets (for details of the parameters counted, refer to **CHAPTER 5 STATISTICS COUNTERS**). The counter is μPDated each time a packet has been transmitted or received. The status information is stored in the status FIFO in the μPD98431 after an operation has been completed. Based on this information, the statistics counter is successively updated.

Each counter is cleared to 0 and continues counting if an overflow occurs. If an overflow occurs in a statistics counter, or if an overrun occurs in the status FIFO, the corresponding bit of the CAR1 or CAR2 register is set to 1, generating an interrupt. This interrupt can be masked for each counter by using the CAM1 and CAM2 registers.

The statistics counter is cleared by means of hardware reset.

3.13 Loopback

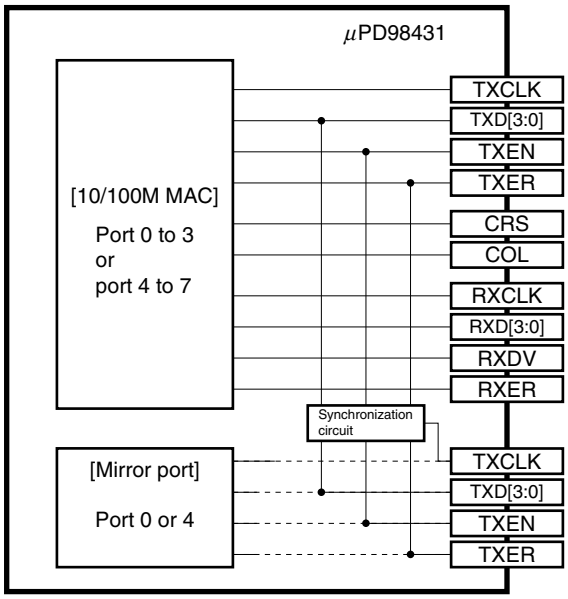
The MII transmit data stream is internally looped back as an MII receive data stream if the MACLB bit of the MACC1 register is set to 1. TXCLKn is internally connected to RXCLKn. COLn and CRSn are ignored. To use loopback, the FULLD bit of the MACC1 register must be set to 1 and the full-duplex operation mode must be set. These settings can be made for each port independently.

3.14 Mirror Port Function

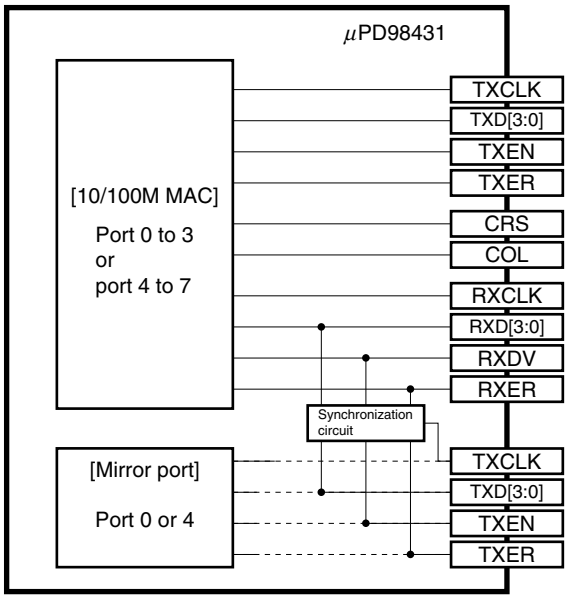
The mirror port function is used to monitor the status of a port specified by a register from a specific port. The μPD98431 outputs the receive or transmit MII data stream of a port specified by the MIRR register as the transmit MII data stream of a specific port. Refer to **Figure 3-15**.

Figure 3-15. Output of MII Data to Mirror Port

(1) Transmit MII data mirror port output



(2) Receive MII data mirror port output



Ports 1, 2, and 3 use port 0 as the mirror port. Ports 5, 6, and 7 use port 4 as the mirror port. Mirror ports 0 and 4 are enabled by setting the P0EN bit and P4EN bit of the MIRR register to 1, respectively. When the P0EN or P4EN bit is set to 1, the MII data stream of a port selected by the MP0[1:0] or MP4[1:0] field of the MIRR register is output to the corresponding mirror port as a transmit MII data stream. Whether the mirrored data stream is transmit data or receive data is selected by using the T/R0 or T/R4 bit of the MIRR register. Tables 3-6 and 3-7 show the relation between the setting of the MIRR register and the MII data stream output to the mirror port.

Table 3-6. Setting of Mirror Port 0

Mirror Port [P0EN = 1]	Port Selection MP0[1:0]	Transmission/ Reception Selection T/R0	Mirror Port 0 MII Output
Port 0	00	0	Port 0 MII receive data
	00	1	Port 0 MII transmit data
	01	0	Port 1 MII receive data
	01	1	Port 1 MII transmit data
	10	0	Port 2 MII receive data
	10	1	Port 2 MII transmit data
	11	0	Port 3 MII receive data
	11	1	Port 3 MII transmit data

Table 3-7. Setting of Mirror Port 4

Mirror Port [P4EN = 1]	Port Selection MP4[1:0]	Transmission/ Reception Selection T/R4	Mirror Port 4 MII Output
Port 4	00	0	Port 4 MII receive data
	00	1	Port 4 MII transmit data
	01	0	Port 5 MII receive data
	01	1	Port 5 MII transmit data
	10	0	Port 6 MII receive data
	10	1	Port 6 MII transmit data
	11	0	Port 7 MII receive data
	11	1	Port 7 MII transmit data

Caution The mirror port function can be used only when the selected port and mirror port are in MII mode (when the EXINT bit of the PCSC register is 0).

3.15 Low-Power Mode

The μPD98431 has a register, POWR, that reduces the power consumption if some ports are not used. By setting a bit of the POWD register to 1, clock supply to the corresponding port is cut and the power consumption is reduced.

Each bit of the POWD register can be turned ON/OFF while the μPD98431 is operating. The port corresponding to the bit of the POWD register that is set to 1 enters the sleep status and is excluded from the round-robin sequence in reception. Because the register setting before the port enters the sleep status is not held, the registers must be reset after the port has been released from the sleep status.

Because HCLK is not supplied to a sleeping port, the setting register of the port cannot be accessed while the port is sleeping. Because the register setting before the port enters sleep status is not preserved, it must be set again after sleep status has been cleared.

If sleep status is set without clearing interrupt sources, the INT# signal may remain asserted. Because the port setting register cannot be cleared as it cannot be accessed while the port is sleeping, clear the interrupt source of the corresponding port before setting the POWD register, and then set the port in sleep status.

To set the corresponding port in sleep status while data is read from the receive FIFO or written to the transmit FIFO, wait until the FIFO bus operation to the port enters the IDLE status.

If sleep status is set while data is received from or transmitted to a network, the packet being received or transmitted is canceled. Nor is the data that has been already stored to the FIFO preserved. To clear sleep status, execute software reset after releasing sleep status (refer to **3.16 (3), (4)** for details of the software reset procedure).

3.16 Notes on Using μPD98431

(1) Connection with PHY device

If the μPD98431 is connected to the PHY device of some manufacturers, a write access is not correctly completed when MII management access is made, and the data is not correctly written to the PHY register. This phenomenon has reportedly occurred with the following product:

- Broadcom BCM5208

The μPD98431 outputs MDC for the duration of 64 clocks to an MII management frame, from preamble to data. Reportedly, the PHY device in which the above phenomenon occurs does not complete a write access unless MDC is input in the "IDLE" status following the data, i.e., unless MDC is input at least for the duration of 65 clocks after preamble has been started. To avoid this phenomenon, consult each PHY device manufacturer.

(2) Automatic transmission of pause frame

If a condition in which a pause frame is automatically transmitted occurred two times or more in a short period of time, the condition that is satisfied last is assumed to be valid and the pause frame is transmitted. Depending on the case, however, the pause frame is transmitted two times in the condition that is satisfied last.

The pause frames automatically transmitted include the pause frame having the value of PTIME of the MACC3 register (PTIME pause frame) and pause frame with a pause timer value of 0 (0-pause frame). The PTIME pause frame and 0-pause frame are automatically transmitted under the following conditions:

The PTIME pause frame is transmitted if the quantity of the data in the receive FIFO exceeds the value of RFDMH of the RFIC1 register. If this condition occurs successively at short intervals, the PTIME pause frame is transmitted once by regarding only the last condition as valid. Depending on the interval at which the condition occurs, however, the PTIME pause frame is transmitted two times.

The 0 pause frame is transmitted if the quantity of the data in the receive FIFO falls below the value of RFDML of the RFIC1a register after the condition for transmitting the PTIME pause frame has been satisfied. At this time, the 0-pause frame is transmitted after the PTIME pause frame has been transmitted. If the interval at which the quantity of the data in the receive FIFO falls below the value of RFDML of the RFIC1 register is short after the PTIME pause frame transmission condition has been satisfied, transmission of the PTIME pause frame is canceled, and only the 0 pause frame is transmitted. Depending on the interval at which the condition occurs, however, the 0-pause frame is transmitted two times.

There is no measure to avoid this problem, such as external circuits or software. It is assumed that the system operates without problem because the pause frame is transmitted singly or successively in the condition that is satisfied last.

(3) Recovery from hang-up of reception/transmission

If transmission or reception is forcibly stopped because of disconnection of the cable or other reasons, the PHY device may generate the MII signal at a timing not rated. If this happens, the μPD98431 malfunctions and can no longer execute transmission or reception. If transmission or reception freezes for these reasons, only the port in which the problem has occurred can be recovered by the following steps:

<1> Detect operation status.
By using the link signal of the PHY device, detect stoppage of transmission or reception.

<2> Disable transmission or reception.
Disable reception of a new packet by clearing the SRXEN bit of the MACC1 register to 0.
Disable writing of a new packet from the high-end system.

<3> Read data remaining in receive FIFO.
Read the packet data remaining in the receive FIFO.
If a packet completely accumulated in the receive FIFO exists when reception is stopped, that packet can be read. The packet being received cannot be read. It is not necessary to read the remaining packet if it is to be discarded.

<4> Execute software reset
Execute software reset using the following procedure.

1. PCSC register: Set the PCRST bit to 1.
2. MACC2 register: Set the MCRST, RFRST, and TFRST bits to 1.
3. MACC3 register: Set the RXFFLH and TXFFLH bits to 1.
4. MACC3 register: Set the RXFFLH bit to 0.
5. MACC2 register: Set the RFRST bit to 0.
6. PCSC register: Set the PCRST bit to 0.
7. MACC2 register: Set the MCRST and TFRST bits to 0.
8. MACC3 register: Set the TXFFLH bit to 0.

Be sure to leave an interval of at least 20 TXCLK or RXCLK clocks between each step in the procedure.

<5> Resume reception.
Resume reception by setting the SRXEN bit of the MACC1 register to 1.

Recovery can also be made by executing hardware reset. In this case, however, note that all the ports are initialized.

(4) Cautions on switching settings of MACC1, MACC2, MACC3, PCSC registers

Observe the following points when switching the settings of the MACC1, MACC2, MACC3, and PCSC registers. With the exception of the SRXEN bit of the MACC1 register, the PTIME bit of the MACC3 register, and all the software reset bits, when switching the settings of the bits in the MACC1, MACC2, MACC3, and PCSC registers, be sure to execute software reset using the following procedure after setting the registers.

<1> PCSC register: Set the PCRST bit to 1.
<2> MACC2 register: Set the MCRST, RFRST, and TFRST bits to 1.
<3> MACC3 register: Set the RXFFLH and TXFFLH bits to 1.
<4> MACC3 register: Set the RXFFLH bit to 0.
<5> MACC2 register: Set the RFRST bit to 0.
<6> PCSC register: Set the PCRST bit to 0.
<7> MACC2 register: Set the MCRST and TFRST bits to 0.
<8> MACC3 register: Set the TXFFLH bit to 0.

Be sure to leave an interval of at least 20 TXCLK or RXCLK clocks between each step in the procedure.

(5) Cautions on releasing software reset of MII management interface block

When accessing the management after releasing the software reset applied to the MII management interface block via the MISRT bit of the MIIC register, be sure to wait until at least 60 HCLK clocks have elapsed before accessing the MCMD or MWTD register.

CHAPTER 4 REGISTER DESCRIPTION

4.1 Control Register Map

(1) Port control register map

(1/2)

Register Address A[7:0]	Name	Function	R/W	Default
00H	MACC1	MAC configuration register 1	R/W	00000800H
01H	MACC2	MAC configuration register 2	R/W	00000000H
02H	IPGT	Back-to-back IPG register	R/W	00000013H
03H	IPGR	Non-back-to-back IPG register	R/W	00000E13H
★ 04H	CLRT	Collision register	R/W	0000380FH
05H	LMAX	Maximum packet length register	R/W	00000600H
06H to 14H	–	Reserved	–	–
15H	LSA1	Station address register 1	R/W	00000000H
16H	LSA2	Station address register 2	R/W	00000000H
17H	PTVR	Pause timer value read register	R	00000000H
18H	–	Reserved	–	–
19H	VLTP	VLAN type register	R/W	00000000H
1AH to 1FH	–	Reserved	–	–
20H	MIIC	MII configuration register	R/W	00000000H
21H to 24H	–	Reserved	–	–
25H	MCMD	MII command register	W	00000000H
26H	MADR	MII address register	R/W	00000000H
27H	MWTD	MII write data register	R/W	00000000H
28H	MRDD	MII read data register	R	00000000H
29H	MIND	MII indicator register	R	00000000H
2AH to 31H	–	Reserved	–	–
32H	AFR	Address filter register	R/W	00000000H
33H	HT1	Hash table register 1	R/W	00000000H
34H	HT2	Hash table register 2	R/W	00000000H
35H to 36H	–	Reserved	–	–
37H	CAR1	CARRY register 1	R/W	00000000H
38H	CAR2	CARRY register 2	R/W	00000000H

Caution Do not access addresses marked “Reserved”.

(2/2)

	Register Address A[7:0]	Name	Function	R/W	Default
	39H to 4BH	–	Reserved	–	–
	4CH	CAM1	CARRY register 1 mask register	R/W	00000000H
	4DH	CAM2	CARRY register 2 mask register	R/W	00000000H
	4EH to 4FH	–	Reserved	–	–
	50H to 81H	–	Refer to **CHAPTER 5 STATISTICS COUNTERS**.	–	–
	82H to 8FH	–	Reserved	–	–
★	90H	MACC3	MAC configuration register 3	R/W	FFFF0000H
★	91H	TIMR	Transmission interrupt mask register	R/W	00000000H
★	92H	RIMR	Reception interrupt mask register	R/W	00000000H
★	93H	TSVREG1	Transmit status register 1	R	00000000H
★	94H	TSVREG2	Transmit status register 2	R	00000000H
★	95H	RSVREG	Receive status register	R	00000000H
★	96H	FSVREG	FIFO status register	R	00000000H
	97H	–	Reserved	–	–
	98H	PCSC	PCS configuration register	R/W	00000000H
	99H to 9AH	–	Reserved	–	–
	9BH	RFIC1	Receive FIFO configuration register 1	R/W	07FF0000H
	9CH	RFIC2	Receive FIFO configuration register 2	R/W	07FF0007H
	9DH	TFIC	Transmit FIFO configuration register	R/W	00FF00FFH
	9EH to F9H	–	Reserved	–	–

Caution Do not access addresses marked “Reserved”.

(2) Global register map

Register Address A[7:0]	Name	Function	R/W	Default
FAH	–	Reserved	–	–
FBH	STIR	Status information register	R	00000000H
FCH	MISCR	Bus width/interrupt setting register	R/W	00000000H
FDH	MIRR	Mirror port setting register	R/W	00000000H
FEH	–	Reserved	–	–
FFH	POWD	Power down control register	R/W	00000000H

4.2 Port Setting Registers

The port setting register is used to define the operation of each port or check the status of the port. To access the register of each port, input a port number to A[10:8] of the address bus A[10:0], and the address of the register to A[7:0].

MACC1 - MAC configuration register 1 (register address A[7:0] = 00H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	MACLB	Reserved		Reserved	RXFC	SRXEN	Reserved	PUREP	FLCHT	NOBO	Reserved	CRCEN	PADEN	FULLD	HUGEN

(1/2)

Bit	Name	Function	Default
31:15	–	Reserved. Write 0 to these bits.	–
14	MACLB	MAC loopback. When this bit is set to 1, data is looped back from the transmission block to the reception block inside MAC.	0
13:12	–	Reserved. Write 0 to these bits.	–
11	–	Reserved. Write 1 to this bit.	1
10	RXFC	Reception flow control enable. When this bit is set to 1, the pause operation is executed for the duration of the pause time set by the pause timer. The value of the pause timer is updated when a valid pause control frame is received, regardless of the setting of this bit.	0
9	SRXEN	Reception enable If this bit is set to 1, writing receive packet data from the network to the receive FIFO is enabled. If the status of this bit is changed while the CRSn signal is asserted, the new status becomes valid after the CRSn signal has been deasserted.	0
8	–	Reserved. Write 0 to this bit.	0
7	PUREP	Pure preamble. When this bit is set to 1, data other than '0101' is not enabled during preamble.	0
6	FLCHT	Length field check. When this bit is set to 1, the value of the length field and data field length are checked and reported as a status vector.	0
5	NOBO	No Back Off. When this bit is set to 1, packet transmission is always performed without back off.	0
4	–	Reserved. Write 0 to these bits.	–
3	CRCEN	CRC enable. When this bit is set to 1, a CRC is automatically suffixed to a packet.	0

(2/2)

Bit	Name	Function	Default
2	PADEN	PAD append If this bit is set to 1, padding is performed if the packet length is less than 64 bytes (68 bytes in the case of a VLAN frame). If this bit is 1, the μPD98431 automatically appends CRC regardless of the specification by the TXFDQ signal or setting of the CRCEN bit.	0
1	FULLD	Full-duplex enable. When this bit is set to 1, the full-duplex operation is performed.	0
0	HUGEN	Large packet enable. When this bit is cleared to 0, transmission or reception of a packet exceeding the value of the LMAX register is aborted. **Caution If this bit is 1, the constraint of the LMAX register is cleared. If a packet is received exceeding the upper limit of the receive FIFO set by RFUB of the RFIC2 register, a receive FIFO overrun occurs.**	0

★

Remark When switching the settings of bits other than the SRXEN bit, be sure to execute software reset after setting the registers. Refer to **3.16 (4) Cautions on switching settings of MACC1, MACC2, MACC3, PCSC registers**.

MACC2 - MAC configuration register 2 (register address A[7:0] = 01H) R/W

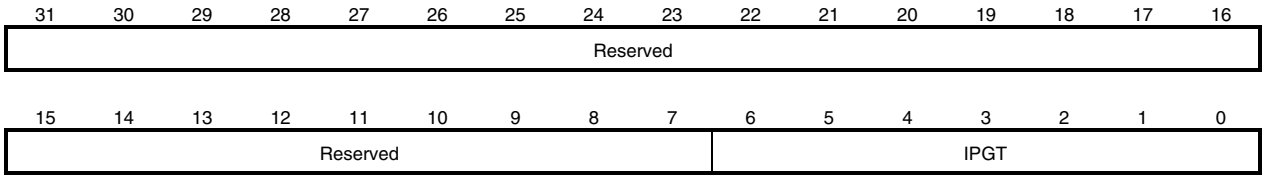
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					MCRST	RFRST	TFRST	Reserved	BPNB	APD	VPD	Reserved			

Bit	Name	Function	Default
31:11	–	Reserved. Write 0 to these bits.	–
10	MCRST	MAC control block software reset. When this bit is set to 1, software reset is executed. To clear software reset, write 0 to this bit.	0
9	RFRST	Reception block software reset. When this bit is set to 1, software reset is executed. To clear software reset, write 0 to this bit.	0
8	TFRST	Transmission block software reset. When this bit is set to 1, software reset is executed. To clear software reset, write 0 to this bit.	0
7	–	Reserved. Write 0 to this bit.	–
6	BPNB	Back Pressure No Back Off. When this bit is set to 1, only transmission after back pressure is not backed off.	0
5	APD	Auto VLAN pad. If this bit is set to 1, a transmit packet regarded as a VLAN packet is processed based on MAX: 1522 bytes, MIN: 64 bytes. However, if this bit is 1 and if the PADEN bit of the MACC1 register is also 1, pad and CRC are automatically appended to the transmit packets regarded as VLAN packets that are less than 68 bytes, and packets are transmitted as 68 bytes. The μPD98431 regards the transmit packets matching the VLAN type registered to the VLTP register as VLAN packets.	0
4	VPD	VLAN pad mode. If this bit is set to 1, all transmit packets are regarded as VLAN packets and processed based on MAX: 1522 bytes, MIN: 64 bytes. However, if this bit is 1 and if the PADEN bit of the MACC1 register is also 1, pad and CRC are automatically appended to these transmit packets that are less than 68 bytes, and packets are transmitted as 68 bytes. Setting of the VPD bit takes precedence over setting of the APD bit.	0
3:0	–	Reserved. Write 0 to these bits.	–

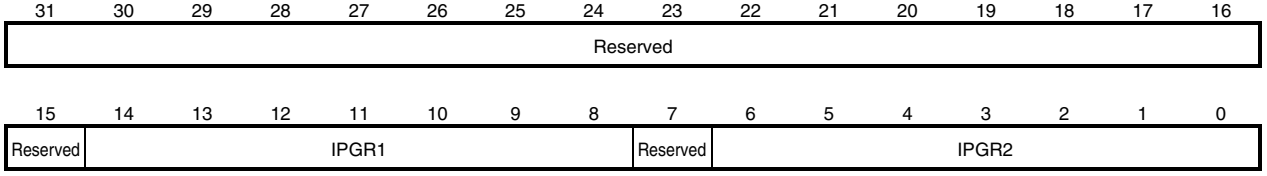
Remark When switching the settings of bits other than the software reset bits, be sure to execute software reset after setting the registers. Refer to **3.16 (4) Cautions on switching settings of MACC1, MACC2, MACC3, PCSC registers**.

IPGT - Back-to-back IPG register (register address A[7:0] = 02H) R/W



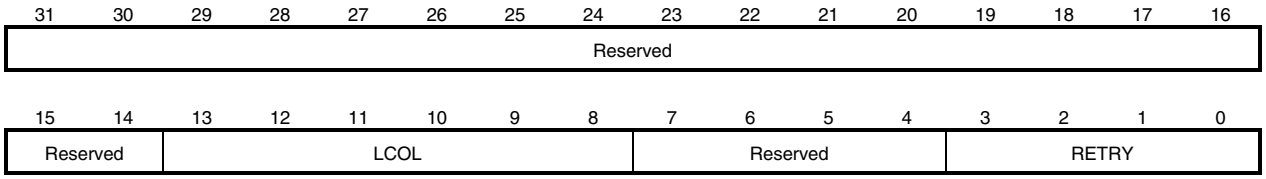
Bit	Name	Function	Default
31:7	–	Reserved. Write 0 to these bits.	–
6:0	IPGT	IPG for back-to-back. These bit set a back-to-back IPG by using the following expression: IPG = (5 + IPGT) × 4 bits time	13H

IPGR - Non-back-to-back IPG register (register address A[7:0] = 03H) R/W



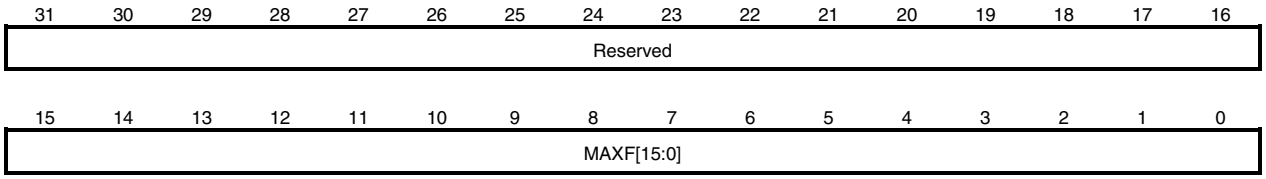
Bit	Name	Function	Default
31:15	–	Reserved. Write 0 to these bits.	–
14:8	IPGR1	Carrier sense period. This field sets the carrier sense period of the first half of a non-back-to-back IPG, by using the following expression: Carrier sense period = (2 + IPGR1) × 4 bits time	0EH
7	–	Reserved. Write 0 to this bit.	–
6:0	IPGR2	Non-back-to-back IPG. This field sets a non-back-to-back IPG by using the following expression: IGP = (5 + IPGR2) × 4 bits time The carrier sense period set by the IPGR1 field is included in the IPG set by the IPGR2 field.	13H

CLRT - Collision register (register address A[7:0] = 04H) R/W



Bit	Name	Function	Default
31:14	–	Reserved. Write 0 to these bits.	–
13:8	LCOL	Collision window. This field sets a collision window width by using the following expression: Collision window width = (LCOL + 8) × 8 bits time	38H
7:4	–	Reserved. Write 0 to these bits.	–
3:0	RETRY	Maximum number of times of retransmission in case of collision. This field sets the maximum number of times of retransmission if a collision occurs. If retransmission is not completed within the value set by this field, transmission is aborted. This value indicates the maximum number of times of collision.	0FH

LMAX - Maximum packet length register (register address A[7:0] = 05H) R/W



Bit	Name	Function	Default
31:16	–	Reserved. Write 0 to these bits.	–
15:0	MAXF	Maximum packet length (octet). MACC1 register: When the HUGEN bit is 0, the transmit/receive packet length is limited by this value. Reception : Reception is immediately aborted if the receive frame length exceeds MAXF. The data accumulated to the receive FIFO and up to MAXF is discarded. Transmission : Transmission is aborted immediately if the transmit frame length exceeds MAXF. The maximum value of MAXF is 7FFH.	0600H

LSA1 - Station address register 1 (register address A[7:0] = 15H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SA[15:0]															

Bit	Name	Function	Default
31:16	–	Reserved. Write 0 to these bits.	0
15:0	LSA1	Station address SA[47:32]. SA[47:0] are used for comparison of a source address when a pause control frame is assembled and a destination address when address filtering is used.	0

LSA2 - Station address register 2 (register address A[7:0] = 16H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SA[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SA[15:0]															

Bit	Name	Function	Default
31:0	LSA2	Station address SA[31:0].	0

PTVR - Pause timer value read register (register address A[7:0] = 17H) Read only

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTCT[15:0]															

Bit	Name	Function	Default
31:16	–	Reserved	–
15:0	PTCT	Pause timer counter. This field indicates the current value of the pause timer. **Caution This register holds a valid value while the reception control flow is enabled (while the RXFC bit of the MACC1 register is 1).**	0

VLTP - VLAN type register (register address A[7:0] = 19H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VLTP[15:0]															

Bit	Name	Function	Default
31:16	–	Reserved. Write 0 to these bits.	–
15:0	VLTP	VLAN type. This field specifies a VLAN type. Reception : The value of this field and the value of the TPID field of the receive frame are compared to detect a VLAN frame. Transmission : If the value of the TPID field of the transmit frame coincides with the value of this field when the APD bit of the MACC2 register is 1, PAD is appended to the transmit frame as a VLAN frame.	0

MIIC - MII configuration register (register address A[7:0] = 20H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
★ MIRST	Reserved											CLKS		Reserved	

Bit	Name	Function	Default
31:16	–	Reserved. Write 0 to these bits.	–
★ 15	MIRST	MII management interface block software reset. When this bit is set to 1, the MII management interface block is reset by software. Write 0 to this bit to clear the software reset.	0
14:4	–	Reserved. Write 0 to these bits.	–
3:2	CLKS	Host clock speed setting. This field selects a clock speed. Selects a clock speed in accordance with the input HCLK. Depending on this setting, HCLK is divided so that MDC is 2.5 MHz or less. 00 = Not used 01 = 33 MHz MAX 10 = 50 MHz MAX 11 = 66 MHz MAX	0
1:0	–	Reserved. Write 0 to these bits.	–

Caution When accessing this register, input 000B to A[10:8].

MCMD - MII command register (register address A[7:0] = 25H) Write only

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															RSTAT

Bit	Name	Function	Default
31:1	–	Reserved. Write 0 to these bits.	–
0	RSTAT	MII management read. When this bit is set to 1, read access by the MII management interface is executed.	0

Caution When accessing this register, input 000B to A[10:8].

MADR - MII address register (register address A[7:0] = 26H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			FIAD[4:0]					Reserved			RGAD[4:0]				

Bit	Name	Function	Default
31:13	–	Reserved. Write 0 to these bits.	–
12:8	FIAD	MII PHY address. This field sets a PHY address to select one of the 32 PHY devices.	0
7:5	–	Reserved. Write 0 to these bits.	–
4:0	RGAD	MII register address. This field selects one of the 16-bit registers of a PHY device to be accessed.	0

Caution When accessing this register, input 000B to A[10:8].

MWTD - MII write data register (register address A[7:0] = 27H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTLD[15:0]															

Bit	Name	Function	Default
31:16	–	Reserved. Write 0 to these bits.	–
15:0	CTLD	MII write data. This is a write data field used for write access by the MII management interface.	0

Caution When accessing this register, input 000B to A[10:8].

MRDD - MII read data register (register address A[7:0] = 28H) Read only

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRSD[15:0]															

Bit	Name	Function	Default
31:16	–	Reserved	–
15:0	PRSD	MII read data. This is a read data field used for read access by the MII management interface.	0

Caution When accessing this register, input 000B to A[10:8].

MIND - MII indicator register (register address A[7:0] = 29H) Read only

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															BUSY

Bit	Name	Function	Default
31:1	–	Reserved	–
0	BUSY	BUSY. This bit is set to 1 to indicate that the μPD98431 is accessed by an external PHY device via the MII management interface.	0

Caution When accessing this register, input 000B to A[10:8].

AFR - Address filter register (register address A[7:0] = 32H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												PRO	PRM	AMC	ABC

Bit	Name	Function	Default
31:4	–	Reserved. Write 0 to these bits.	–
3	PRO	Promiscuous mode. In this mode, all packets are accepted.	0
2	PRM	Multicast reception. In this mode, all multicast packets are accepted.	0
1	AMC	Conditional multicast reception. In this mode, only multicast packets that satisfy a given condition are accepted. A multicast packet that coincides with a hash table is accepted.	0
0	ABC	Broadcast reception. In this mode, broadcast packets are accepted.	0

HT1 - Hash table register 1 (register address A[7:0] = 33H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HT[63:48]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HT[47:32]															

Bit	Name	Function	Default
31:0	HT1	Hash table 1. This table is used for conditional multicast packet detection. These bits are the high-order 32 bits of the hush table, HT[63:32].	0

HT2 - Hash table register 2 (register address A[7:0] = 34H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HT[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HT[15:0]															

Bit	Name	Function	Default
31:0	HT2	Hash table 2. This table is used for conditional multicast packet detection. These bits are the low-order 32 bits of the hash table, HT[31:0].	0

CAR1 - CARRY register 1 (register address A[7:0] = 37H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C1VT	C1UT	C1BT	C1MT	C1PT	C1TB	C1MX	C11K	C1FE	C1TE	C1OT	C1SF	C1BR	C1MR	C1PR	C1RB

This register indicates that a statistics counter has overflowed. Each bit of this register corresponds to a statistics counter. When a statistics counter overflows, the corresponding bit of this register is set to 1. For details of the statistics counter, refer to **CHAPTER 5 STATISTICS COUNTERS**.

★ If this register is read when the SRRC bit of the MISCR register is set to 1, all the bits are automatically cleared.

Bit	Name	Function	Default
31:16	–	Reserved. Write 0 to these bits.	–
15	C1VT	RVBT counter carry bit	0
14	C1UT	TUCA counter carry bit	0
13	C1BT	TBCA counter carry bit	0
12	C1MT	TMCA counter carry bit	0
★ 11	C1PT	TPKT counter carry bit	0
10	C1TB	TBYT counter carry bit	0
9	C1MX	RMAX counter carry bit	0
8	C11K	R1K counter carry bit	0
7	C1FE	R511 counter carry bit	0
6	C1TF	R255 counter carry bit	0
5	C1OT	R127 counter carry bit	0
4	C1SF	R64 counter carry bit	0
3	C1BR	RBCA counter carry bit	0
★ 2	C1MR	RMCA counter carry bit	0
1	C1PR	RPKT counter carry bit	0
0	C1RB	RBYT counter carry bit	0

CAR2 - CARRY register 2 (register address A[7:0] = 38H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C2DV	Reserved								C2IM	C2CS	C2NC	C2XC	C2LC	C2MC	C2SC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2XC	C2DF	C2XF	C2TE	C2JB	C2FG	C2OV	C2UN	C2FC	C2CD	C2FO	C2AL	C2UO	C2PF	C2CF	C2RE

This register indicates that a statistics counter has overflowed. Each bit of this register corresponds to a statistics counter. When a statistics counter overflows, the corresponding bit of this register is set to 1. For details of the statistics counter, refer to **CHAPTER 5 STATISTICS COUNTERS**.

★ If this register is read when the SRRC bit of the MISCR register is set to 1, all the bits are automatically cleared.

Bit	Name	Function	Default
31	C2DV	Status vector overrun. This bit indicates that a status FIFO overrun in the statistics counter.	0
30:23	–	Reserved. Write 0 to these bits.	–
22	C2IM	TIME counter carry bit	0
21	C2CS	TCSE counter carry bit	0
20	C2NC	TNCL counter carry bit	0
19	C2XC	TXCL counter carry bit	0
18	C2LC	TLCL counter carry bit	0
17	C2MC	TMCL counter carry bit	0
16	C2SC	TSCL counter carry bit	0
15	C2XD	TXDF counter carry bit	0
14	C2DF	TDFR counter carry bit	0
13	C2XF	TXPF counter carry bit	0
12	C2TE	TFCS counter carry bit	0
11	C2JB	RBJR counter carry bit	0
10	C2FG	RFRG counter carry bit	0
9	C2OV	ROVR counter carry bit	0
8	C2UN	RUND counter carry bit	0
7	C2FC	RFCR counter carry bit	0
6	C2CD	RCDE counter carry bit	0
5	C2FO	RFLR counter carry bit	0
4	C2AL	RALN counter carry bit	0
3	C2UO	RXUO counter carry bit	0
2	C2PF	RXPF counter carry bit	0
1	C2CF	RXCF counter carry bit	0
0	C2RE	RFCS counter carry bit	0

CAM1 - CARRY register 1 mask register (register address A[7:0] = 4CH) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M1VT	M1UT	M1BT	M1MT	M1PT	M1TB	M1MX	M11K	M1FE	M1TF	M1OT	M1SF	M1BR	M1MR	M1PR	M1RB

This register masks the INT# signal that is generated when a bit of the CAR1 register is set to 1. When a bit of this register is set to 1, the corresponding bit of the CAR1 register is unmasked.

Each bit of the CAR1 register can be masked.

Bit	Name	Function	Default
31:16	–	Reserved. Write 0 to these bits.	–
15	M1VT	RVBT counter carry mask bit	0
14	M1UT	TUCA counter carry mask bit	0
13	M1BT	TBCA counter carry mask bit	0
12	M1MT	TMCA counter carry mask bit	0
★ 11	M1PT	TPKT counter carry mask bit	0
10	M1TB	TBYT counter carry mask bit	0
9	M1MX	RMAX counter carry mask bit	0
8	M11K	R1K counter carry mask bit	0
7	M1FE	R511 counter carry mask bit	0
6	M1TF	R255 counter carry mask bit	0
5	M1OT	R127 counter carry mask bit	0
4	M1SF	R64 counter carry mask bit	0
3	M1BR	RBCA counter carry mask bit	0
★ 2	M1MR	RMCA counter carry mask bit	0
1	M1PR	RPKT counter carry mask bit	0
0	M1RB	RBYT counter carry mask bit	0

CAM2 - CARRY register 2 mask register (register address A[7:0] = 4DH) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
M2DV	Reserved								M2IM	M2CS	M2NC	M2XC	M2LC	M2MC	M2SC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M2XD	M2DF	M2XF	M2TE	M2JB	M2FG	M2OV	M2UN	M2FC	M2CD	M2FO	M2AL	M2UO	M2PF	M2CF	M2RE

Bit	Name	Function	Default
31	M2DV	Status vector overrun mask bit	0
30:23	–	Reserved. Write 0 to these bits.	–
22	M2IM	TIME counter carry mask bit	0
21	M2CS	TCSE counter carry mask bit	0
20	M2NC	TNCL counter carry mask bit	0
19	M2XC	TXCL counter carry mask bit	0
18	M2LC	TLCL counter carry mask bit	0
17	M2MC	TMCL counter carry mask bit	0
16	M2SC	TSCL counter carry mask bit	0
15	M2XD	TXDF counter carry mask bit	0
14	M2DF	TDFR counter carry mask bit	0
13	M2XF	TXRF counter carry mask bit	0
12	M2TE	TFCS counter carry mask bit	0
11	M2JB	RJBR counter carry mask bit	0
10	M2FG	RFRG counter carry mask bit	0
9	M2OV	ROVR counter carry mask bit	0
8	M2UN	RUND counter carry mask bit	0
7	M2FC	RFCR counter carry mask bit	0
6	M2CD	RCDE counter carry mask bit	0
5	M2FO	RFLR counter carry mask bit	0
4	M2AL	RALN counter carry mask bit	0
3	M2UO	RXUO counter carry mask bit	0
2	M2PF	RXPF counter carry mask bit	0
1	M2CF	RXCF counter carry mask bit	0
0	M2RE	RFCS counter carry mask bit	0

MACC3 - MAC configuration register 3 (register address A[7:0] = 90H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PTIME[15:0]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									APSE	APSS	BUSMODE	BACKPE	FLWCNT	TXFFLH	RXFLH

Bit	Name	Function	Default
★ 31:16	PTIME	Pause timer value. The value of this field is used as a pause timer value when the μPD98431 generates a pause control frame.	FFFFH
15:7	–	Reserved. Write 0 to these bits.	
6	APSE	Status information append (suffix). When this bit is 1, the status information of a receive packet is suffixed to the receive data stream read from the FIFO bus.	0
5	APSS	Status information append (prefix). When this bit is 1, the status information of a receive packet is prefixed to the receive data stream read from the FIFO bus. **Caution Do not set the APSE and APSS bits to 1 at the same time.**	0
4	BUSMODE	Little endian/big endian. When this bit is 1, the byte order of the FIFO bus is big endian.	0
3	BACKPE	Back pressure enable. When this bit is 1, the back pressure function is enabled.	0
2	FLWCNT	Transmission flow control enable. When this bit is 1, automatic transmission of the pause control frame is enabled.	0
1	TXFFLH	Transmit FIFO flash. When this bit is set to 1, all the contents of the transmit FIFO are cleared. To clear this function, write 0 to this bit.	0
0	RXFFLH	Receive FIFO flash. When this bit is set to 1, all the contents of the receive FIFO are cleared. To clear this function, write 0 to this bit.	0

★ **Remark** When switching the settings of bits other than the PTIME bit, be sure to execute software reset after setting the registers. Refer to **3.16 (4) Cautions on switching settings of MACC1, MACC2, MACC3, PCSC registers**.

TIMR - Transmission interrupt mask register (register address A[7:0] = 91H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													ITFOV	ITFUN	ITWMH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICSE	ITBP	ITPP	ITPCF	ITCFR	ITGNT	ILCOL	IECOL	ITEDFR	ITDFR	ITBRO	ITMUL	ITDONE	ITFLOR	ITFLER	ITCRCE

This register masks occurrence of the INT# signal due to each cause. When each bit of this register is set to 1, the mask is cleared.

(1/2)

Bit	Name	Function	Default
31:19	–	Reserved. Write 0 to these bits.	–
18	ITFOV	Transmit FIFO overrun. When this bit is 0, the interrupt of the corresponding bit of the FSVREG register is masked.	0
17	ITFUN	Transmit FIFO underrun. When this bit is 0, the interrupt of the corresponding bit of the FSVREG register is masked.	0
16	ITWMH	Transmission full level over. When this bit is 0, the interrupt of the corresponding bit of the FSVREG register is masked.	0
15	ICSE	Carrier sense error. When this bit is 0, the interrupt of the corresponding bit of the TSVREG1 register is masked.	0
14	ITBR	Back pressure. When this bit is 0, the interrupt of the corresponding bit of the TSVREG1 register is masked.	0
13	ITPP	Transmission request during pause. When this bit is 0, the interrupt of the corresponding bit of the TSVREG1 register is masked.	0
12	ITPCF	Pause control frame transmission. When this bit is 0, the interrupt of the corresponding bit of the TSVREG1 register is masked.	0
11	ITCFR	Control frame transmission. When this bit is 0, the interrupt of the corresponding bit of the TSVREG1 register is masked.	0
10	ITGNT	Packet transmission with length exceeding LMAX. When this bit is 0, the interrupt of the corresponding bit of the TSVREG1 register is masked.	0
9	ILCOL	Late collision. When this bit is 0, the interrupt of the corresponding bit of the TSVREG1 register is masked.	0
8	IECOL	Excessive collision. When this bit is 0, the interrupt of the corresponding bit of the TSVREG1 register is masked.	0
7	ITEDFR	Excessive defer. When this bit is 0, the interrupt of the corresponding bit of the TSVREG1 register is masked.	0

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Bit	Name	Function	Default
6	ITDFR	Transmission defer. When this bit is 0, the interrupt of the corresponding bit of the TSVREG1 register is masked.	0
5	ITBRO	Broadcast packet transmission. When this bit is 0, the interrupt of the corresponding bit of the TSVREG1 register is masked.	0
4	ITMUL	Multicast packet transmission. When this bit is 0, the interrupt of the corresponding bit of the TSVREG1 register is masked.	0
3	ITDONE	End of transmission. When this bit is 0, the interrupt of the corresponding bit of the TSVREG1 register is masked.	0
2	ITFLOR	Length field check. When this bit is 0, the interrupt of the corresponding bit of the TSVREG1 register is masked.	0
1	ITFLER	Data length non-coincidence. When this bit is 0, the interrupt of the corresponding bit of the TSVREG1 register is masked.	0
0	ITCRCE	Transmit CRC error. When this bit is 0, the interrupt of the corresponding bit of the TSVREG1 register is masked.	0

RIMR - Reception interrupt mask register (register address A[7:0] = 92H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													IRFOV	IRWMH	IRWML

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRLENE	IVLAN	IUSOP	IRPCF	IRCFR	IDNB	IRBRO	IRMUL	IRXOK	IRLOR	IRLER	IRCRCE	IRCV	ICEPS	IREPS	IPAIG

This register masks occurrence of the INT# signal due to each cause. When each bit of this register is set to 1, the mask is cleared.

(1/2)

Bit	Name	Function	Default
31:19	–	Reserved. Write 0 to these bits.	–
18	IRFOV	Receive FIFO overrun. When this bit is 0, the interrupt of the corresponding bit of the FSVREG register is masked.	0
17	IRWMH	Pause frame transmission level. When this bit is 0, the interrupt of the corresponding bit of the FSVREG register is masked.	0
16	IRWML	Zero frame transmission level. When this bit is 0, the interrupt of the corresponding bit of the FSVREG register is masked.	0
15	IRLENE	Receive packet length error. When this bit is 0, the interrupt of the corresponding bit of the RSVREG register is masked.	0
14	IVLAN	VLAN frame When this bit is 0, the interrupt of the corresponding bit of the RSVREG register is masked.	0
13	IUSOP	Reception of control frame including undefined op code. When this bit is 0, the interrupt of the corresponding bit of the RSVREG register is masked.	0
12	IRPCF	Pause control frame reception. When this bit is 0, the interrupt of the corresponding bit of the RSVREG register is masked.	0
11	IRCFR	Control frame reception. When this bit is 0, the interrupt of the corresponding bit of the RSVREG register is masked.	0
10	IDNB	Dribble nibble error. When this bit is 0, the interrupt of the corresponding bit of the RSVREG register is masked.	0
9	IRBRO	Broadcast packet reception. When this bit is 0, the interrupt of the corresponding bit of the RSVREG register is masked.	0
8	IRMUL	Multicast packet reception. When this bit is 0, the interrupt of the corresponding bit of the RSVREG register is masked.	0
7	IRXOK	End of reception. When this bit is 0, the interrupt of the corresponding bit of the RSVREG register is masked.	0

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Bit	Name	Function	Default
6	IRLOR	Length field check. When this bit is 0, the interrupt of the corresponding bit of the RSVREG register is masked.	0
5	IRLER	Data length non-coincidence. When this bit is 0, the interrupt of the corresponding bit of the RSVREG register is masked.	0
4	IRCRCE	CRC error. When this bit is 0, the interrupt of the corresponding bit of the RSVREG register is masked.	0
3	IRCV	RXER detection. When this bit is 0, the interrupt of the corresponding bit of the RSVREG register is masked.	0
2	ICEPS	False Carrier detection. When this bit is 0, the interrupt of the corresponding bit of the RSVREG register is masked.	0
1	IREPS	Invalid packet reception. When this bit is 0, the interrupt of the corresponding bit of the RSVREG register is masked.	0
0	IPAIG	Invalid packet ignore. When this bit is 0, the interrupt of the corresponding bit of the RSVREG register is masked.	0

TSVREG1 - Transmit status register 1 (register address A[7:0] = 93H) Read only

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												TCBC			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSE	TBP	ITPP	TPCF	TCFR	TGNT	LCOL	ECOL	TEDFR	TDFR	TBRO	TMUL	TDONE	TFLOR	TFLER	TCRCE

This register indicates an interrupt source when the INT# signal is made low by the status of a transmit packet (except bits 31 through 16). If the interrupt of each bit occurs, the corresponding bit is set to 1 and the INT# signal is made low. If an interrupt is caused by a source masked by the TIMR register, only the corresponding bit of this register is set to 1 and the INT# signal is not made low.

This register is updated at the end of each transmission or when transmission is aborted.

If this register is read when the SRRC bit of the MISCR register is set to 1, all the bits are automatically cleared.

(1/2)

Bit	Name	Function	Default
31:20	–	Reserved. Write 0 to these bits.	–
19:16	TCBC	Collision count. This field indicates the number of collisions that have occurred until transmission is completed. This bit is cleared to 0 if transmission is aborted.	
15	CSE	Carrier sense error. When this bit is 1, it indicates that a carrier sense error has occurred during transmission.	0
14	TBP	Back pressure. When this bit is 1, it indicates that a dummy packet has been transmitted by backpressure and that a collision has occurred.	0
13	ITPP	Transmission request during pause. When this bit is 1, it indicates that transmission of the packet requested has been completed during pause. This bit is not set to 1 if the packet requested to be transmitted during pause is the pause frame automatically transmitted by the μPD98431.	0
12	TPCF	Pause control frame transmission. When this bit is 1, it indicates that a pause control frame has been transmitted.	0
11	TCFR	Control frame transmission. When this bit is 1, it indicates that a control frame has been transmitted.	0
10	TGNT	Transmission of packet of length exceeding LMAX. When this bit is 1, it indicates that a packet with a length exceeding the packet length specified by the LMAX register has been transmitted. This bit is set to 1 only when the HUGEN bit of the MACC1 register is 0.	0
9	LCOL	Late collision. When this bit is 1, it indicates that a collision exceeding the collision window set by the CLRT register has occurred.	0
8	ECOL	Excessive collision. When this bit is 1, it indicates that the number of collisions has exceeded the maximum retransmission count set by the CLRT register.	0

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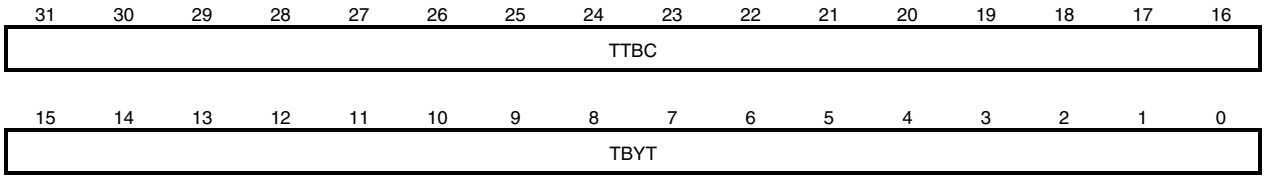
Bit	Name	Function	Default
7	TEDFR	Excessive defer. When this bit is 1, it indicates that an excessive defer (i.e., transmission is not started even after 24288 bit time) has occurred.	0
6	TDFR	Transmission defer. When this bit is 1, it indicates that a transmission delay has occurred. This bit is not set to 1 if transmission is aborted.	0
5	TBRO	Broadcast packet transmission. When this bit is 1, it indicates that a broadcast packet has been transmitted. This bit is not set to 1 if transmission is aborted.	0
★ 4	TMUL	Multicast packet transmission. When this bit is 1, it indicates that a multicast packet or broadcast packet has been transmitted. This bit is not set to 1 if transmission is aborted.	0
3	TDONE	End of transmission. When this bit is 1, it indicates that transmission has been completed normally. This bit is not set to 1 if transmission is aborted.	0
2	TFLOR	Length field check. When this bit is 1, it indicates that the value of the length field of the transmit packet exceeds 1500. This bit is not set to 1 if the FLCHT bit of the MACC1 register is 0.	0
1	TFLER	Data length non-coincidence. When this bit is 1, it indicates that the data field length of the transmit packet does not coincide with the value of the length field. This bit is not set to 1 if the FLCHT bit of the MACC1 register is 0. TFLOR is set to 1 but TFLER is not set to 1 if the value of the length field exceeds 1500.	0
0	TCRCE	Transmit CRC error. When this bit is 1, it indicates that the CRC code appended by the host to the transmit packet is not correct. This bit is not set to 1 if the CRCEN bit of the MACC1 register is 1. It is not set to 1 if transmission is aborted.	0

TSVREG2 - Transmit status register 2 (register address A[7:0] = 94H) Read only



This register indicates the number of transmit bytes per transmitted packet, and is updated at the end of each transmission or when transmission is aborted.

★ If this register is read when the SRRC bit of the MISCR register is set to 1, all the bits are automatically cleared.

Bit	Name	Function	Default
31:16	TTBC	Total transmit byte count. This field indicates the total number of bytes, including packets canceled because of occurrence of a collision, that have been transmitted before transmission is completed.	0
15:0	TBYT	Transmit byte count. This field indicates the number of bytes transmitted normally. This field does not take the correct value if transmission is aborted.	0

RSVREG - Receive status register (register address A[7:0] = 95H) Read only

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RBYT															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RLENE	VLAN	USOP	RPCF	RCFR	DBNB	RBRO	RMUL	RXOK	RLOR	RLER	RCRCE	RCV	CEPS	REPS	PAIG

This register indicates an interrupt source when the INT# signal is made low by the status of a receive packet (except bits 31 through 16). If the interrupt of each bit occurs, the corresponding bit is set to 1 and the INT# signal is made low. If an interrupt is caused by the source masked by the RIMR register, only the corresponding bit of this register is set to 1 and the INT# signal is not made low.

This register is updated each time the MAC module receives a packet.

If this register is read when the SRRC bit of the MISCR register is set to 1, all the bits are automatically cleared.

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Bit	Name	Function	Default
31:16	RBYT	Receive byte count. This field indicates the length of the received packet in byte units.	–
15	RLENE	Receive packet length error. When this bit is 1, it indicates that the length of the receive packet is less than 64 octet or greater than 1518 octet. (less than 64 octet or greater than 1522 octet in the case of VLAN)	0
14	VLAN	VLAN frame. When this bit is 1, it indicates that the VPID field of the received packet coincides with the value of the VLTP register. This bit is not set to 1 if a CRC error or RXER occurs.	0
13	USOP	Reception of control frame including undefined op code. When this bit is 1, it indicates that a control frame including an undefined op code has been received. This bit is not set to 1 if a CRC error occurs.	0
12	RPCF	Pause control frame reception. When this bit is 1, it indicates that a pause control frame has been received. This bit is not set to 1 if a CRC error occurs.	0
11	RCFR	Control frame reception. When this bit is 1, it indicates that a control frame has been received. This bit is not set to 1 if a CRC error occurs.	0
10	DBNB	Reception of a packet including dribble nibble. When this bit is 1, it indicates that a dribble nibble has occurred in the received packet.	0
9	RBRO	Broadcast packet reception. When this bit is 1, it indicates that a broadcast packet has been received.	0
8	RMUL	Multicast packet reception. When this bit is 1, it indicates reception of a multicast packet or a broadcast packet.	0
7	RXOK	End of reception When this bit is 1, it indicates that reception has been completed. This bit is not set to 1 if a CRC error or RXER occurs.	0

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Bit	Name	Function	Default
6	RLOR	Length field check. When this bit is 1, it indicates that the value of the length field of a received packet exceeds 1500. This bit is not set to 1 if the FLCHT bit of the MACC1 register is 0.	0
5	RLER	Data length non-coincidence. When this bit is 1, it indicates that the data field length of the received packet and the value of its length field do not coincide. This bit is not set to 1 if the FLCHT bit of the MACC1 register is 0. RLOR is set to 1 but RLER is not set to 1 if the value of the length field exceeds 1500.	0
4	RCRCE	CRC error. When this bit is 1, it indicates that a CRC error has occurred in the received packet.	0
3	RCV	RXER detection. When this bit is 1, it indicates that RXER has been detected.	0
2	CEPS	False Carrier detection. When this bit is 1, it indicates that False Carrier has been detected after the preceding reception.	0
1	REPS	Invalid packet reception. When this bit is 1, it indicates that an invalid packet (only preamble + SFD or packet with only 1 nibble of data) has been received after the preceding reception. The invalid packet that has set this bit to 1 is discarded in the MAC.	0
0	PAIG	Receive packet ignore. When this bit is 1, it indicates that data has been received in the following conditions after the preceding reception: • Carrier length: If a carrier length exceeding 6072 nibbles is detected • If the following packet is received with IPG being 80 bit time or less after packet reception • MACC1: Illegal preamble or SFD has been received when the PUREP bit is set. The invalid packet that has set this bit to 1 is discarded in the MAC.	0

FSVREG - FIFO status register (register address A[7:0] = 96H) Read only

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					TFOV	TFUM	TWMH	Reserved					RFOV	RWMH	RWML

This register indicates an interrupt source when the INT# signal is made low by each status (except Reserved bits). If the interrupt of each bit occurs, the corresponding bit is set to 1 and the INT# signal is made low. If an interrupt is caused by the source masked by the TIMR register or RIMR register, only the corresponding bit of this register is set to 1 and the INT# signal is not made low.

If this register is read when the SRRC bit of the MISCR register is set to 1, all the bits are automatically cleared.

Bit	Name	Function	Default
31:11	–	Reserved	–
10	TFOV	Transmit FIFO overrun. This bit is set to 1 if an overrun occurs in the transmit FIFO.	0
9	TFUN	Transmit FIFO underrun. This bit is set to 1 if an underrun occurs in the transmit FIFO.	0
8	TWMH	Transmission full level over. This bit is set to 1 if the quantity of data in the transmit FIFO exceeds the value set by the TFDMH field of the TFIC register.	0
7:3	–	Reserved	
2	RFOV	Receive FIFO overflow. If the quantity of data in the receive FIFO exceeds the value of the RFUB field of the RFIC2 register, it is assumed to be an overrun, and this bit is set to 1.	0
1	RWMH	Pause frame transmission level over. This bit is set to 1 if the quantity of data in the receive FIFO exceeds the value set by the RFDMH field of the RFIC1 register.	0
0	RWML	Zero frame transmission level. This bit is set to 1 if the quantity of data in the receive FIFO has exceeded the value set by the RFDMH field of the RFIC1 register and than fallen below the value set by the RFDML field.	0

PCSC - PCS configuration register (register address A[7:0] = 98H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												PCRST	INTLB	EXINT	ENJAE

Bit	Name	Function	Default
31:4	–	Reserved. Write 0 to these bits.	0
3	PCRST	PCS block software reset. When this bit is set to 1, software reset is executed. To clear software reset, write 0 to this bit.	0
2	INTLB	PCS loopback. When this bit is set to 1, the PCS transmit data output is looped back as PCS receive data input.	0
1	EXINT	Physical layer interface selection. This bit selects an interface with the physical layer device. When this bit is cleared to 0, the MII mode is selected; when it is set to 1, the 10 Mbps serial mode is selected.	0
0	ENJAB	Jabber protection enable. When this bit is set to 1, the jabber packet is not transmitted in the 10 Mbps serial mode.	0

Remark When switching the settings of bits other than the software reset bits, be sure to execute software reset after setting the registers. Refer to **3.16 (4) Cautions on switching settings of MACC1, MACC2, MACC3, PCSC registers**.

RFIC1 - Receive FIFO configuration register 1 (register address A[7:0] = 9BH) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					RFDMH										

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					RFDML										

Bit	Name	Function	Default
31:27	–	Reserved. Write 0 to these bits.	0
26:16	RFDMH	Pause frame transmission level. If the quantity of data in the receive FIFO exceeds the value of this field when the transmission flow control function is enabled, a pause frame having the pause timer value set by the MACC3 register is automatically transmitted.	7FFH
15:11	–	Reserved. Write 0 to these bits.	0
10:0	RFDML	Zero frame transmission level. If the transmission flow control function is enabled and if the quantity of data in the receive FIFO has once exceeded the value set to the RFDMH field and then falls below the value of this field, a control frame with a pause timer value of 0 is automatically transmitted. **Caution The relation between the set value of RFDMH and that of RFDML must be as follows:** **0 ≤ RFDML ≤ RFDMH ≤ 7FFH**	000H

Caution In the FIFO of the μPD98431, the packet data quantity is used in 4-byte units in the 32-bit bus mode and in 8-byte units in the 64-bit bus mode. If a fraction occurs at the end of a packet, the value rounded up in data units of each bus mode is regarded as the quantity of the accumulated data in the FIFO. To compare the data quantities of RFDMH, RFDML, and FIFO, each register value plus 1 data unit (4 bytes in the 32-bit bus mode or 8 bytes in the 64-bit bus mode), and the quantity of the data accumulated in the previous data units are used.

RFIC2 - Receive FIFO configuration register 2 (register address A[7:0] = 9CH) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					RFUB										

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													SIFT	DCRCE	FCRX

Bit	Name	Function	Default
31:27	–	Reserved. Write 0 to these bits.	0
26:16	RFUB	Receive FIFO upper limit setting[Note 1]. This field sets the upper limit of the receive FIFO. If the quantity of the data accumulated in the receive FIFO exceeds this value, the μPD98431 assumes that the receive FIFO has overrun. A value in a range of 40H to 7FFH can be set to this field.	7FFH
15:3	–	Reserved. Write 0 to these bits.	0
2	SIFT	Discarding short packet. When this bit is 1, a packet of less than 64 bytes is discarded. Similarly, a VLAN packet of less than 64 bytes is discarded.	1
1	DCRCE	Discarding CRC error packet[Note 2]. When this bit is 1, the packet in which a CRC error and RXER have occurred is discarded.	1
0	FCRX	Discarding control packet. When this bit is 1, the pause control frame is discarded. An undefined control frame other than the pause frame is not discarded.	1

Notes 1. In the FIFO of the μPD98431, the packet data quantity is used in 4-byte units in the 32-bit bus mode and in 8-byte units in the 64-bit bus mode. If a fraction occurs at the end of a packet, the value rounded up in data units of each bus mode is regarded as the quantity of the accumulated data in the FIFO. To compare the data quantities of RFUB and FIFO, each register value plus 1 data unit (4 bytes in the 32-bit bus mode or 8 bytes in the 64-bit bus mode) and the quantity of the data accumulated in the previous data units are used, except in the following cases:

Case 1. To prefix status information to receive data (APPS bit of MACC3 register = 1), comparison is performed by using the value of the RFUB register and the data quantity accumulated in the previous data units.

2. If a RFUB value at which a fraction of 1 to 4 bytes occurs when data is processed in 8-byte units in the 64-bit bus mode, comparison is performed by using the value truncating the fraction plus 8 bytes, 1 data unit in the 64-bit bus mode, and the data quantity accumulated in the previous data units.

2. To discard jam data received during a collision using the μPD98431, set the DCRCE bit to 1.

TFIC - Transmit FIFO configuration register (register address A[7:0] = 9DH) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved							TFDMH								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							TFDWL								

Bit	Name	Function	Default
31:25	–	Reserved. Write 0 to these bits.	0
24:16	TFDMH	Transmission full level. If the quantity of the data in the transmit FIFO is less than the value of this field, the μPD98431 makes the TXFBA[n] signal high, informing the host system that the transmit FIFO has a vacancy. If the quantity of the data in the transmit FIFO exceeds the value of this field, the TXFBA[n] signal is made low. Set a value to this field in the range 3FH to 1FFH.	0FFH
15:9	–	Reserved. Write 0 to these bits.	0
8:0	TFDWL	Transmission drain level. If the quantity of data in the transmit FIFO has exceeded the value of this field, transmission of a packet is started. Set a value to this field in the range the value of (CLRT register: LCOL + 8) to 1FFH.	0FFH

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Caution In the FIFO of the μPD98431, the packet data quantity is used in 4-byte units in the 32-bit bus mode and in 8-byte units in the 64-bit bus mode. If a fraction occurs at the end of a packet, the value rounded up in data units of each bus mode is regarded as the quantity of the accumulated data in the FIFO. To compare the data quantities of TFDMH, TFDWL, and FIFO, the data quantity accumulated in the previous data units is used.

4.3 Global Registers

The global registers are used to set and check the statuses of all the ports. When accessing a global register, only A[7:0] of the address bus A[10:0] are valid, and A[10:8] are ignored.

STIR - Status information register (register address A[7:0] = FBH) Read only

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P7TS	P7RS	P7FS	P7CA	P7TS	P7RS	P7FS	P7CA	P7TS	P7RS	P7FS	P7CA	P7TS	P7RS	P7FS	P7CA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P7TS	P7RS	P7FS	P7CA	P7TS	P7RS	P7FS	P7CA	P7RS	P7RS	P7FS	P7CA	P7TS	P7RS	P7FS	P7CA

If a bit of the TSVREG1, RSVREG, FSVREG, CAR1, or CAR2 registers of each port is set to 1, the corresponding bit of this register is set to 1. This register indicates the current status of each status register. If a status register is cleared, therefore, the corresponding bit of this register is also cleared. Even if this register is read, the status registers are not cleared nor is the INT# signal deasserted.

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Bit	Name	Function	Default
31	P7TS	Port 7 TSVREG status. This bit is set to 1 if any bit of the TSVREG1 register of port 7 is set to 1.	0
30	P7RS	Port 7 RSVREG status. This bit is set to 1 if any bit of the RSVREG register of port 7 is set to 1.	0
29	P7FS	Port 7 FSVREG status. This bit is set to 1 if any bit of the FSVREG register of port 7 is set to 1.	0
28	P7CA	Port 7 CAR status. This bit is set to 1 if any bit of the CAR1 or CAR2 register of port 7 is set to 1.	0
27	P7TS	Port 6 TSVREG status. This bit is set to 1 if any bit of the TSVREG1 register of port 6 is set to 1.	0
26	P7RS	Port 6 RSVREG status. This bit is set to 1 if any bit of the RSVREG register of port 6 is set to 1.	0
25	P7FS	Port 6 FSVREG status. This bit is set to 1 if any bit of the FSVREG register of port 6 is set to 1.	0
24	P7CA	Port 6 CAR status. This bit is set to 1 if any bit of the CAR1 or CAR2 register of port 6 is set to 1.	0
23	P7TS	Port 5 TSVREG status. This bit is set to 1 if any bit of the TSVREG1 register of port 5 is set to 1.	0
22	P7RS	Port 5 RSVREG status. This bit is set to 1 if any bit of the RSVREG register of port 5 is set to 1.	0
21	P7FS	Port 5 FSVREG status. This bit is set to 1 if any bit of the FSVREG register of port 5 is set to 1.	0
20	P7CA	Port 5 CAR status. This bit is set to 1 if any bit of the CAR1 or CAR2 register of port 5 is set to 1.	0

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Bit	Name	Function	Default
19	P7TS	Port 4 TSVREG status. This bit is set to 1 if any bit of the TSVREG1 register of port 4 is set to 1.	0
18	P7RS	Port 4 RSVREG status. This bit is set to 1 if any bit of the RSVREG register of port 4 is set to 1.	0
17	P7FS	Port 4 FSVREG status. This bit is set to 1 if any bit of the FSVREG register of port 4 is set to 1.	0
16	P7CA	Port 4 CAR status. This bit is set to 1 if any bit of the CAR1 or CAR2 register of port 4 is set to 1.	0
15	P7TS	Port 3 TSVREG status. This bit is set to 1 if any bit of the TSVREG1 register of port 3 is set to 1.	0
14	P7RS	Port 3 RSVREG status. This bit is set to 1 if any bit of the RSVREG register of port 3 is set to 1.	0
13	P7FS	Port 3 FSVREG status. This bit is set to 1 if any bit of the FSVREG register of port 3 is set to 1.	0
12	P7CA	Port 3 CAR status. This bit is set to 1 if any bit of the CAR1 or CAR2 register of port 3 is set to 1.	0
11	P7TS	Port 2 TSVREG status. This bit is set to 1 if any bit of the TSVREG1 register of port 2 is set to 1.	0
10	P7RS	Port 2 RSVREG status. This bit is set to 1 if any bit of the RSVREG register of port 2 is set to 1.	0
9	P7FS	Port 2 FSVREG status. This bit is set to 1 if any bit of the FSVREG register of port 2 is set to 1.	0
8	P7CA	Port 2 CAR status. This bit is set to 1 if any bit of the CAR1 or CAR2 register of port 2 is set to 1.	0
7	P7TS	Port 1 TSVREG status. This bit is set to 1 if any bit of the TSVREG1 register of port 1 is set to 1.	0
6	P7RS	Port 1 RSVREG status. This bit is set to 1 if any bit of the RSVREG register of port 1 is set to 1.	0
5	P7FS	Port 1 FSVREG status. This bit is set to 1 if any bit of the FSVREG register of port 1 is set to 1.	0
4	P7CA	Port 1 CAR status. This bit is set to 1 if any bit of the CAR1 or CAR2 register of port 1 is set to 1.	0
3	P7TS	Port 0 TSVREG status. This bit is set to 1 if any bit of the TSVREG1 register of port 0 is set to 1.	0
2	P7RS	Port 0 RSVREG status. This bit is set to 1 if any bit of the RSVREG register of port 0 is set to 1.	0
1	P7FS	Port 0 FSVREG status. This bit is set to 1 if any bit of the FSVREG register of port 0 is set to 1.	0
0	P7CA	Port 0 CAR status. This bit is set to 1 if any bit of the CAR1 or CAR2 register of port 0 is set to 1.	0

MISCR - FIFO bus width/interrupt setting register (register address A[7:0] = FCH) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															BUSWTH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							INTEN	Reserved							SRRC

Bit	Name	Function	Default
31:17	–	Reserved. Write 0 to these bits.	–
16	BUSWTH	FIFO bus interface data bus width. When this bit is 0, the data bus width of the FIFO bus interface is 32 bits (32-bit dual bus mode). When it is 1, the data bus width of the FIFO bus interface is 64 bits (64-bit single bus mode).	0
15:9	–	Reserved. Write 0 to these bits.	–
8	INTEN	Interrupt enable. When this bit is 1, the function of the INT# signal is enabled.	0
7:1	–	Reserved. Write 0 to these bits.	0
0	SRRC	Status register read clear setting. When this bit is 1, each status register is cleared when it is read.	0

MIRR - Mirror port setting register (register address A[7:0] = FDH) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								TR4	MP4		MP4EN	TR0	MP0		MP0EN

Bit	Name	Function	Default
31:8	–	Reserved. Write 0 to these bits.	–
7	TR4	Transmission/reception selection (mirror port: port 4). When port 4 is used as a mirror port, this bit selects which of transmission or reception is mirrored. When this bit is 1, the MII transmit data of the port specified by MP4[1:0] is output as the MII transmit data of port 4. When it is 0, the MII receive data of the port specified by MP4[1:0] is output as the MII transmit data of port 4.	0
6:5	MP4[1:0]	Port selection (mirror port: port 4). This field specifies a port mirrored by port 4. The relation between the bits of this field and ports is as follows: MP4[1:0] = 11B: Port 7 MP4[1:0] = 10B: Port 6 MP4[1:0] = 01B: Port 5 MP4[1:0] = 00B: Port 4	0
4	MP4EN	Port 4 mirroring enable. When this bit is 1, port mirroring by port 4 is enabled.	0
3	TR0	Transmission/reception selection (mirror port: port 0). When port 0 is used as a mirror port, this bit selects whether transmission or reception is mirrored. When this bit is 1, the MII transmit data of the port specified by MP0[1:0] is output as the MII transmit data of port 0. When it is 0, the MII receive data of the port specified by MP0[1:0] is output as the MII transmit data of port 0.	0
2:1	MP0[1:0]	Port selection (mirror port: port 0). This field specifies a port mirrored by port 0. The relation between the bits of this field and ports is as follows: MP0[1:0] = 11B: Port 3 MP0[1:0] = 10B: Port 2 MP0[1:0] = 01B: Port 1 MP0[1:0] = 00B: Port 0	0
0	MP0EN	Port 0 mirroring enable. When this bit is 1, port mirroring by port 0 is enabled.	0

POWD - Power down control register (register address A[7:0] = FFH) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								POWD							

Bit	Name	Function	Default
31:8	–	Reserved. Write 0 to these bits.	–
7:0	POWD	Setting of power down mode. This field sets a power down mode. By setting a bit of this field to 1, clock supply to the corresponding port in the device is cut. Bits 7 through 0 correspond to ports 7 through 0, respectively.	0

Statistics counter map

(1/2)

Register Address A[7:0]	Name	Function	R/W	Default
50H	RBYT	Byte reception counter	R/W	00000000H
51H	RPKT	Packet reception counter	R/W	00000000H
52H	RFCS	CRC error reception counter	R/W	00000000H
53H	RMCA	Multicast packet reception counter	R/W	00000000H
54H	RBCA	Broadcast packet reception counter	R/W	00000000H
55H	RXCF	Control frame reception counter	R/W	00000000H
56H	RXPF	Pause frame reception counter	R/W	00000000H
57H	RXUO	Undefined control frame reception counter	R/W	00000000H
58H	RALN	Alignment error reception counter	R/W	00000000H
59H	RFLR	Data length non-coincidence reception counter	R/W	00000000H
5AH	RCDE	Code error reception counter	R/W	00000000H
5BH	RFCR	False Carrier reception counter	R/W	00000000H
5CH	RUND	Short packet reception counter	R/W	00000000H
5DH	ROVR	Jabber packet reception counter	R/W	00000000H
5EH	RFRG	Error short packet reception counter	R/W	00000000H
5FH	RJBR	Error jabber packet reception counter	R/W	00000000H
60H	R64	64-byte frame reception counter	R/W	00000000H
61H	R127	65-to-127 byte frame reception counter	W	00000000H
62H	R255	128-to-255 byte frame reception counter	R/W	00000000H
63H	R511	256-to-511 byte frame reception counter	R/W	00000000H
64H	R1K	512-to-1023 byte frame reception counter	R/W	00000000H
65H	RMAX	1024-to-RMAX byte frame reception counter	R/W	00000000H
66H	RVBT	Valid byte reception counter	R/W	00000000H
67H to 6FH	–	Reserved	–	–
70H	TBYT	Byte transmission counter	R/W	00000000H
71H	TPKT	Packet transmission counter	R/W	00000000H
72H	TFCS	CRC error transmission counter	R/W	00000000H
73H	TMCA	Multicast packet transmission counter	R/W	00000000H
74H	TBCA	Broadcast packet transmission counter	R/W	00000000H
75H	TUCA	Unicast packet transmission counter	R/W	00000000H
76H	TXPF	Pause control frame transmission counter	R/W	00000000H
77H	TDFR	Transmission defer counter	R/W	00000000H

Caution Do not access addresses marked “Reserved”.

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Register Address A[7:0]	Name	Function	R/W	Default
78H	TXDF	Transmission excessive defer counter	R/W	00000000H
79H	TSCL	Single collision packet transmission counter	R/W	00000000H
7AH	TMCL	Multi-collision packet transmission counter	R/W	00000000H
7BH	TLCL	Late collision counter	R/W	00000000H
7CH	TXCL	Excessive collision counter	R/W	00000000H
7DH	TNCL	Total collision counter	R/W	00000000H
7EH	TCSE	Carrier sense error counter	R/W	00000000H
7FH	TIME	MAC internal error counter	R/W	00000000H
80H	RFOVR	Receive FIFO overrun counter	R/W	00000000H
81H	TFUNR	Transmit FIFO underrun counter	R/W	00000000H

Caution Do not access addresses marked “Reserved”.

RBYT - Byte reception counter (register address A[7:0] = 50H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RBYT[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RBYT[15:0]															

This counter indicates the byte count of a receive packet. It counts the number of bytes from the destination address to the FCS byte of the packet. It also counts even if an error occurs.

If a packet exceeding the length set by the LMAX register is received when the HUGEN bit of the MACC1 register is 0, the value of the LMAX register is counted as the packet length.

RPKT - Packet reception counter (register address A[7:0] = 51H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRKT[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRKT[15:0]															

This counter counts all the receive packets, including packets in which an error has occurred, all the unicast packets, all the multicast packets, and all the broadcast packets.

RFCS - CRC error reception counter (register address A[7:0] = 52H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RFCS[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFCS[15:0]															

This counter is incremented when a CRC error occurs in a receive packet.

If a packet exceeding the length set by the LMAX register is received when the HUGEN bit of the MACC1 register is 0, a CRC check is performed as soon as the set value of the LMAX register is reached, so this may be counted as the reception of a CRC error.

RMCA - Multicast packet reception counter (register address A[7:0] = 53H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RMCA[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RMCA[15:0]															

This counter counts multicast packets with a length of longer than 64 bytes and less than 1518 bytes (less than 1522 bytes in the case of a VLAN frame) when such packets have been received. Broadcast packets are not included. Note also that receive packets in which a CRC error occurred are not counted.

RBCA - Broadcast packet reception counter (register address A[7:0] = 54H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RBCA[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RBCA[15:0]															

This counter counts broadcast packets with a length of longer than 64 bytes and less than 1518 bytes (less than 1522 bytes in the case of a VLAN frame) when such packets have been received. Multicast packets are not included. Note also that receive packets in which a CRC error occurred are not counted.

RXCF - Control frame reception counter (register address A[7:0] = 55H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RXCF[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXCF[15:0]															

This counter counts received control frames, including pause frames and control frames not supported. The counter is not incremented when a CRC error has been detected.

RXPF - Pause frame reception counter (register address A[7:0] = 56H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RXPF[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXPF[15:0]															

This counter counts received valid pause control frames.

RXUO - Undefined control frame reception counter (register address A[7:0] = 57H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RXUO[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXUO[15:0]															

This counter counts received control frames including an op code other than PAUSE or pause control frames having an invalid destination address. The counter is not incremented when a CRC error has been detected.

RALN - Alignment error reception counter (register address A[7:0] = 58H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RALN[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RALN[15:0]															

This counter is incremented when a CRC error and a dribble nibble have occurred in a receive packet.

If a packet exceeding the length set by the LMAX register is received when the HUGEN bit of the MACC1 register is 0, an alignment error check is performed as soon as the set value (byte unit) of the LMAX register is reached, so this counter is not incremented.

RFLR - Data length non-coincidence reception counter (register address A[7:0] = 59H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RFLR[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFLR[15:0]															

This counter is incremented if the value of the length field of a receive packet does not coincide with the data field length of the packet actually received. It is not incremented if the value of the length field is greater than 1501 (such as when a byte equivalent to the length field is used as an Ethernet type field).

RCDE - Code error reception counter (register address A[7:0] = 5AH) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RCDE[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RCDE[15:0]															

This counter is incremented if an illegal data symbol has been detected at least once while a carrier is detected.

RFCR - False Carrier reception counter (register address A[7:0] = 5BH) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RFCR[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFCR[15:0]															

This counter counts False Carrier if it occurs in an idle state, after the next packet has been received. It is assumed that False Carrier has been generated if 1110B is input from RXD as nibble data when RXER is high level. Even if two or more False Carriers are generated between idle states, this counter counts only once.

RUND - Short packet reception counter (register address A[7:0] = 5CH) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RUND[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RUND[15:0]															

This counter is incremented if the receive packet is less than 64 bytes long and includes a valid FCS field.

ROVR - Jabber packet reception counter (register address A[7:0] = 5DH) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ROVR[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ROVR[15:0]															

This counter is incremented if the receive packet is longer than 1518 bytes (less than 1522 bytes in the case of a VLAN frame) and includes a valid FCS field.

If a packet exceeding the length set by the LMAX register is received when the HUGEN bit of the MACC1 register is 0, a CRC check is performed as soon as the set value of the LMAX register is reached, so this may not be counted as the reception of a CRC error.

RFRG - Error short packet reception counter (register address A[7:0] = 5EH) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RFRG[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFRG[15:0]															

This counter is incremented if the receive packet is less than 64 bytes long and includes a CRC error or alignment error.

RJBR - Error jabber packet reception counter (register address A[7:0] = 5FH) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RJBR[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RJBR[15:0]															

This counter is incremented if the receive packet is longer than 1518 bytes (less than 1522 bytes in the case of a VLAN frame) and includes a CRC error or alignment error.

If a packet exceeding the length set by the LMAX register is received when the HUGEN bit of the MACC1 register is 0, an alignment error check is performed as soon as the set value (byte unit) of the LMAX register is reached, so this counter may be incremented.

R64 - 64-byte frame reception counter (register address A[7:0] = 60H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R64[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R64[15:0]															

This counter is incremented if the receive packet length is 64 bytes. Packets including a CRC error, symbol error, or length/type error are also counted.

R127 - 65-to-127 byte frame reception counter (register address A[7:0] = 61H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R127[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R127[15:0]															

This counter is incremented if the receive packet length is 65 to 127 bytes. Packets including a CRC error, symbol error, or length/type error are also counted.

R255 - 128-to-255 byte frame reception counter (register address A[7:0] = 62H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R255[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R255[15:0]															

This counter is incremented if the receive packet length is 128 to 255 bytes. Packets including a CRC error, symbol error, or length/type error are also counted.

R511 - 256-to-511 byte frame reception counter (register address A[7:0] = 63H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R511[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R511[15:0]															

This counter is incremented if the receive packet length is 256 to 511 bytes. Packets including a CRC error, symbol error, or length/type error are also counted.

R1K - 512-to-1023 byte frame reception counter (register address A[7:0] = 64H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R1K[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R1K[15:0]															

This counter is incremented if the receive packet length is 512 to 1023 bytes. Packets including a CRC error, symbol error, or length/type error are also counted.

RMAX - 1024-to-RMAX byte frame reception counter (register address A[7:0] = 65H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RMAX[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RMAX[15:0]															

This counter is incremented if the receive packet length is 1024 to 1518 bytes (1024 to 1522 bytes in the case of a VLAN frame.) Packets including a CRC error, symbol error, or length/type error are also counted.

RVBT - Valid byte reception counter (register address A[7:0] = 66H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RVBT[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RVBT[15:0]															

This counter indicates the byte count of a valid packet. It counts from the destination address to the FCS byte.

TBYT - Byte transmission counter (register address A[7:0] = 70H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TBYT[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBYT[15:0]															

This counter indicates the byte count of a transmit packet. If a collision occurs before transmission has been completed or aborted, it also counts the transmit byte when the collision occurred. However, the preamble and SFD are not counted.

TPKT - Packet transmission counter (register address A[7:0] = 71H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TPKT[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPKT[15:0]															

This counter is incremented each time a packet has been transmitted, including a packet in which an error has occurred, all unicast packets, all multicast packets, and broadcast packets.

TFCS - CRC error transmission counter (register address A[7:0] = 72H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TFCS[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TFCS[15:0]															

This counter is incremented if a CRC error is detected in the FCS field that has been appended to a transmit packet.

This counter is not incremented if transmission is aborted.

TMCA - Multicast packet transmission counter (register address A[7:0] = 73H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TMCA[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMCA[15:0]															

This counter is incremented when a multicast packet has been transmitted. Broadcast packets are not included.

This counter is not incremented if transmission is aborted or if a CRC error has been detected.

TBCA - Broadcast packet transmission counter (register address A[7:0] = 74H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TBCA[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBCA[15:0]															

This counter is incremented when a broadcast packet has been transmitted. Multicast packets are not included.
This counter is not incremented if transmission is aborted or if a CRC error has been detected.

TUCA - Unicast packet transmission counter (register address A[7:0] = 75H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TICA[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TUCA[15:0]															

This counter is incremented when a unicast packet has been transmitted.
This counter is not incremented if transmission is aborted or if a CRC error has been detected.

TXPF - Pause control frame transmission counter (register address A[7:0] = 76H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TXPF[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXPF[15:0]															

This counter is incremented by the pause control frame automatic transmission function of the μPD98431 each time a pause control frame has been transmitted.

TDFR - Transmission defer counter (register address A[7:0] = 77H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TDFR[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFR[15:0]															

This counter is incremented if a transmission defer occurs because a carrier has been detected when transmission is to be started. If a collision occurs during transmission that has been started after a defer has been generated, this counter is not incremented.

TXDF - Transmission excessive defer counter (register address A[7:0] = 78H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TXDF[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXDF[15:0]															

This counter is incremented if transmission is aborted by an excessive defer.

TSCL - Single collision packet transmission counter (register address A[7:0] = 79H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSCL[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSCL[15:0]															

The value of this counter is incremented if transmission is successful after a collision has occurred once during transmission.

TMCL - Multi-collision packet transmission counter (register address A[7:0] = 7AH) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TMCL[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMCL[15:0]															

This counter is incremented if transmission is successful after multiple collisions (at least two and no more than the value set in the RETRY field of the CLRT register) occur in a single transmit operation.

TLCL - Late collision counter (register address A[7:0] = 7BH) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TLCL[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TLCL[15:0]															

This counter is incremented when late collision occurs during transmission.

TXCL - Excessive collision counter (register address A[7:0] = 7CH) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TXCL[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXCL[15:0]															

This counter is incremented if a number of collisions exceeding the value set in the RETRY field of the CLRT register occurs in a single transmit operation.

TNCL - Total collision counter (register address A[7:0] = 7DH) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TNCL[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TNCL[15:0]															

This counter counts the total number of collisions after which transmission is successful.

TCSE - Carrier sense error counter (register address A[7:0] = 7EH) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TCSE[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCSE[15:0]															

This counter is incremented if a carrier sense error occurs during transmission.

TIME - MAC internal error counter (register address A[7:0] = 7FH) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIME[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME[15:0]															

The value of this counter is incremented if an internal error of MAC occurs (transmission underrun or transmission exceeding LMAX) during transmission.

RFOVR - Receive FIFO overrun counter (register address A[7:0] = 80H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RFOVR[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFOVR[15:0]															

This counter is incremented if the receive FIFO overruns.

Caution This counter does not have a carry bit. If it overflows, this counter is cleared to 0 in the same manner as the other statistics counters.

TFUNR - Transmit FIFO underrun counter (register address A[7:0] = 81H) R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TFUNR[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TFUNR[15:0]															

This counter is incremented if the transmit FIFO underruns.

Caution This counter does not have a carry bit. If it overflows, this counter is cleared to 0 in the same manner as the other statistics counters.

CHAPTER 6 JTAG BOUNDARY SCAN

The μPD98431 has a JTAG boundary scan circuit.

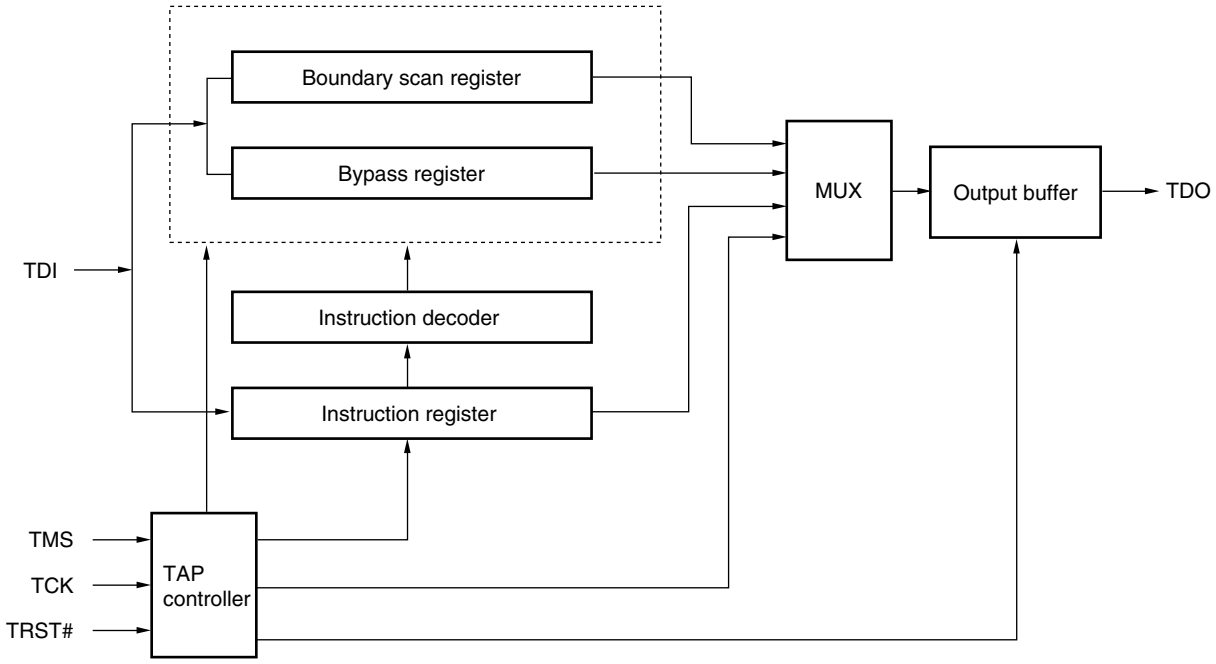
6.1 Features

- Conforms to IEEE1149.1 JTAG Boundary Scan Standard.
- Three registers dedicated to boundary scan
  - Instruction register
  - Bypass register
  - Boundary scan register
- Two instructions supported
  - BYPASS instruction
  - EXTEST instruction
  - SAMPLE/PRELOAD instruction
- Five pins dedicated to boundary scan (5 pins)
  - TCK (JTAG Test Clock)
  - TMS (JTAG Test Mode Select)
  - TDI (JTAG Test Data Input)
  - TDO (JTAG Test Data Output)
  - TRST# (JTAG Reset)

6.2 Internal Configuration of Boundary Scan Circuit

Figure 6-1 shows the block diagram of the internal JTAG boundary scan circuit of the μPD98431.

Figure 6-1. Block Diagram of Boundary Scan Circuit



6.2.1 Instruction register

The instruction register consists of a 2-bit shift register and writes instruction data from the TDI pin. The register and instruction are selected by this instruction data.

6.2.2 TAP (Test Access Port) controller

The TAP controller changes operating state by latching the signal of the TMS pin at the rising edge of the clock input to the TCK pin.

6.2.3 Bypass register

The bypass register consists of a 1-bit shift register connected between the TDI and TDO pins when the TAP controller is in Shift-DR state. If this register is selected while the TAP controller is in Shift-DR state, data is shifted to the TDO pin at the rising edge of the clock input to the TCK pin.

When this register is selected, the operation of the JTAG boundary circuit does not influence on the operation of the μPD98431.

6.2.4 Boundary scan register

The boundary scan register is located between an external pin of the μPD98431 and internal logic circuit. When this register is selected, data is latched or loaded by the instruction of the TAP controller.

If this register is selected while the TAP controller is in Shift-DR state, data is output to the TDO pin starting from the LSB at the falling edge of the clock input to the TCK pin.

6.3 Pin Function

6.3.1 TCK (JTAG Test Clock) pin

The TCK pin is used to supply a clock signal to the JTAG boundary scan circuit (such as the bypass register, instruction register, and TAP controller. This clock signal is isolated so as not to be supplied to the other internal circuits of the μPD98431.

6.3.2 TMS (JTAG Test Mode Select) pin

Input to the TMS signal is latched at the rising edge of the clock input to the TCK pin and defines the operation of the TAP controller.

6.3.3 TDI (JTAG Test Data Input) pin

The TDI pin is an input pin that inputs data to the JTAG boundary scan circuit register.

6.3.4 TDO (JTAG Test Data Output) pin

The TDO pin is an output pin that outputs data from the JTAG boundary scan circuit.

This pin changes its output at the falling edge of the clock input to the TCK pin. This pin is a three-state output pin and is controlled by the TAP controller.

6.3.5 TRST# (JTAG Reset) pin

This pin asynchronously initializes the TAP controller. This reset signal sets the μPD98431 in the normal operation mode and the boundary register in non-operation state.

6.4 Operation Description

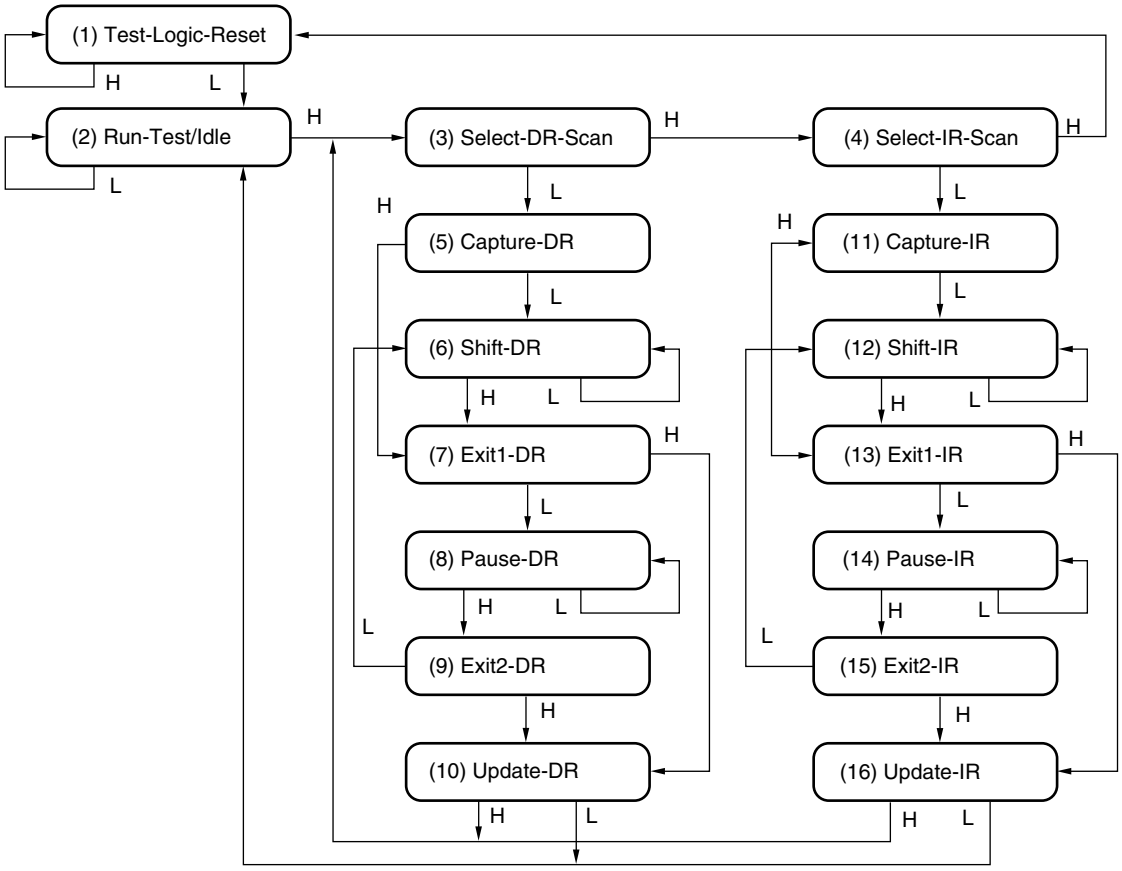
6.4.1 TAP controller

The TAP controller is a circuit having 16 states synchronized with changes of the TMS and TCK pins. Its operation is specified by IEEE Standard 1149.1.

6.4.2 TAP controller state

Figure 6-2 shows the state transition of the TAP controller. The state of the TAP controller is determined depending on the state of the TMS pin signal input at the rising edge of the clock input to the TCK pin. The operations of the instruction register, boundary scan register, and bypass register change at the rising or falling edge of the clock input to the TCK pin. (Refer to **Figure 6-3**).

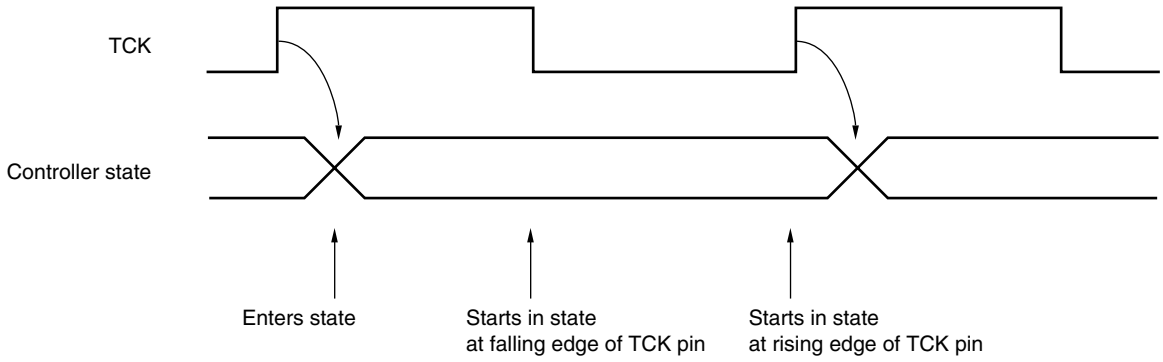
Figure 6-2. State Transition of TAP Controller



Remarks 1. "H" and "L" of the arrows indicating state transition in the above figure indicate the state of the TMS pin at the rising edge of the clock input to the TCK pin.

2. Numbers in ( ) in the above figure correspond to the explanation below.

Figure 6-3. Operation Timing in Controller State



(1) Test-Logic-Reset

The boundary scan circuit performs no operation on the μPD98431. Therefore, it does not affect the system logic of the μPD98431. This is because the bypass instruction is stored to the instruction register and executed on initialization. The TAP controller enters the Test-Logic-Reset state if the TMS pin holds the high level for the duration of at least five rising edges of the TCK pin signal, regardless of the current state of the controller. The TAP controller holds this state for the duration in which the TMS pin signal high.

If the TAP controller must be in the Test-Logic-Reset state, the controller returns to the original Test-Logic-Reset state even if a low-level signal is input once to the TMS pin by mistake (due to, for example, the influence of the external interface), if the TMS pin signal holds its high level status for the duration of three rising edges of the TCK pin signal.

The operation of the test logic does not hinder the logic operation of the μPD98431 due to the above error.

When the TAP controller exits from the Test-Logic-Reset state, the controller enters the Run-Test/Idle state. In this state, no operation is performed because the current instruction is set by the operation of the bypass register. The logic operation of the JTAG boundary scan circuit is inactive even in the Select-DR-Scan and Select-IR-Scan states.

(2) Run-Test/Idle

The TAP controller is in this state during scan operation (in Select-DR-Scan or Select-IR-Scan state). Once the controller has entered this state and if the TMS pin signal holds the low level, the controller remains in this state. The controller enters the Select-DR-Scan state if the TMS pin signal holds high level at one rising edge of the TCK pin signal.

All the test data registers (boundary register and bypass register) selected by the current instruction hold the previous status (Idle). While the TAP controller is in this state, the instruction does not change.

(3) Select-DR-Scan

This is a temporary boundary scan state. The boundary scan register and bypass register selected by the current instruction hold the previous state.

If the TMS pin signal is held low at the rising edge of the TCK pin signal while the TAP controller is in this state, the controller enters the Capture-DR state, and scan sequence to the selected registers is started.

If the TMS pin signal is held high at the rising edge of the TCK pin signal, the TAP controller enters the Select-IR-Scan state. While the controller is in this state, the instruction does not change.

(4) Select-IR-Scan

This is a temporary boundary scan state. The boundary scan register and bypass register selected by the current instruction hold the previous state.

If the TMS pin signal is held low at the rising edge of the TCK pin signal while the TAP controller is in this state, the controller enters the Capture-IR state, and scan sequence to the selected registers is started.

If the TMS pin signal is held high at the rising edge of the TCK pin signal, the TAP controller enters the Test-Logic-Reset state. While the controller is in this state, the instruction does not change.

(5) Capture-DR

In this controller state, data is loaded to the boundary scan register selected by the current instruction in parallel at the rising edge of the TCK pin signal. (In this case, load the data from the input pin of each device to the corresponding boundary scan register at the same time.) While the TAP controller is in this state, the instruction does not change.

If the TAP controller is in this state at the rising edge of the TCK pin signal, the controller enters the following state:

- If the TMS pin signal is held high: Exit1-DR state
- If the TMS pin signal is held low : Shift-DR state

(6) Shift-DR

In this controller state, TDI and TDO are connected (at either of the boundary scan register of bypass register) by the current instruction. The shift data is shifted one state at a time toward the serial output direction at each rising edge of the TCK pin signal.

The boundary scan register or bypass register selected by the current instruction holds the previous status without change if the controller is not on the serial bus (not in the Shift-DR state). While the controller is in this state, the instruction does not change.

If the TAP controller is in this state at the rising edge of the TCK pin signal, the controller enters the following state:

- If the TMS pin signal is held high: Exit1-DR state
- If the TMS pin signal is held low : Shift-DR state

(7) Exit1-DR

This is a temporary controller state. If the TMS pin signal is held high at the rising edge of the TCK pin signal with the TAP controller in this state, the controller enters the Update-DR state. This ends the scan process.

If the TMS pin signal is held low at the rising edge of the TCK pin signal, the TAP controller enters the Pause-DR state.

Both the bypass register and boundary scan register selected by the current instruction hold the previous status without change. While the TAP controller is in this state, the instruction does not change.

(8) Pause-DR

In this controller state, shifting between TDI and TDO connected by either the bypass register or boundary scan register is temporarily stopped. These registers selected by the current instruction hold the previous state without change.

The TAP controller remains in this state while the TMS pin signal is low. If the TMS pin signal is held high at the rising edge of the TCK pin signal, the TAP controller enters the Exit2-DR state. While the TAP controller is in this state, the instruction does not change.

(9) Exit2-DR

This is a temporary controller state. If the TMS pin signal is held high at the rising edge of the TCK pin signal with the TAP controller in this state, the controller enters the Update-DR state. This ends the scan process.

If the TMS pin signal is held low at the rising edge of the TCK pin signal, the TAP controller enters the Shift-DR state.

Both the bypass register and boundary scan register selected by the current instruction hold the previous status without change. While the TAP controller is in this state, the instruction does not change.

(10) Update-DR

The boundary scan register has a parallel output latch to prevent changes in parallel output (while shifted to the shift register path concatenated) by certain instructions (for example, EXTEST instruction).

In the Update-DR controller state, data is latched from the shift register to the parallel output latch of this register at the falling edge of the TCK pin signal.

The data retained latched to the parallel output latch changes depending on this controller state (the data does not change with the other controller states).

The previous states of all the shift register of the boundary scan register selected by the current instruction are retained.

While the TAP controller is in this state, the instruction does not change.

If the TMS pin signal is held high at the rising edge of the TCK pin signal with the TAP controller in this state, the controller enters the Select-DR-Scan state.

If the TMS pin signal is held low at the rising edge of the TCK signal, the TAP controller enters the Run-Test/Idle state.

(11) Capture-IR

In this controller state, the shift register loads the pattern of a fixed logic value “01(binary)” to the instruction register at the rising edge of the TCK pin signal.

The previous states of both the bypass register and boundary scan register selected by the current instruction are retained without change.

While the TAP controller is in this state, the instruction does not change.

If the TMS pin signal is held high at the rising edge of the TCK pin signal while the controller is in this state, the controller enters the Exit1-IR state.

If the TMS pin signal is held low at the rising edge of the TCK pin signal, the TAP controller enters the Shift-IR state.

(12) Shift-IR

In this controller state, TDI and TDO are connected by the shift register in the instruction register. The shift data is shift one state toward the serial output direction at each rising edge of the TCK pin signal.

The boundary scan register or bypass register selected by the current instruction holds the previous state without change.

While the TAP controller is in this state, the instruction does not change.

If the TMS pin signal is held high at the rising edge of the TCK pin signal with the TAP controller in this state, the controller enters the Exit1-IR state. If the TMS pin signal is held low, the controller remains the Shift-IR state.

(13) Exit1-IR

This is a temporary controller state. If the TMS pin signal is held high at the rising edge of the TCK pin signal, the TAP controller enters the Update-IR state. This ends the scan process.

If the TMS pin signal is held low at the rising edge of the TCK pin, the TAP controller enters the Pause-IR state.

Both the bypass register and boundary scan register selected by the current instruction retain their states without change.

While the TAP controller is in this state, the instruction does not change.

(14) Pause-IR

In this controller state, shift of the instruction register is temporarily stopped. The bypass register and boundary scan register selected by the current instruction hold the previous state without change.

While the TAP controller is in this state, the instruction does not change. The instruction register holds the current state.

While the TMS pin signal is low, the TAP controller remains in this state. If the TMS pin signal is held high at the rising edge of the TCK pin signal, the TAP controller enters the Exit2-IR state.

(15) Exit2-IR

This is a temporary controller state. If the TMS pin signal is held high at the rising edge of the TCK pin signal, the TAP controller enters the Update-IR state. This ends the scan process.

If the TMS pin signal is held low at the rising edge of the TCK pin, the TAP controller enters the Shift-IR state.

Both the bypass register and boundary scan register selected by the current instruction retain their states without change.

While the TAP controller is in this state, or while the instruction register holds the current state, the instruction does not change.

(16) Update-IR

In this controller state, the instruction shifted to the instruction register is latched to the parallel output latch from the shift register path at the falling edge of the TCK pin signal. Once a new instruction has been latched, it is used as the current instruction.

The bypass register or boundary scan register selected by the current instruction holds the previous state.

If the TMS pin signal is held high at the rising edge of the TCK pin signal while the TAP controller is in this state, the TAP controller enters the Select-DR-Scan state.

If the TMS pin signal is held low at the rising edge of the TCK pin signal, the TAP controller enters the Run-Test/Idle state.

The Pause-DR controller state in (8) and Pause-IR controller state in (14) temporarily stop shifting of data in the bypass register, the boundary scan register, or instruction register.

6.5 TAP Controller Operation

The TAP controller operates as follows.

The state of the controller is changed by either of (1) and (2) below.

(1) Rising edge of TCK pin signal
(2) TRST# pin input

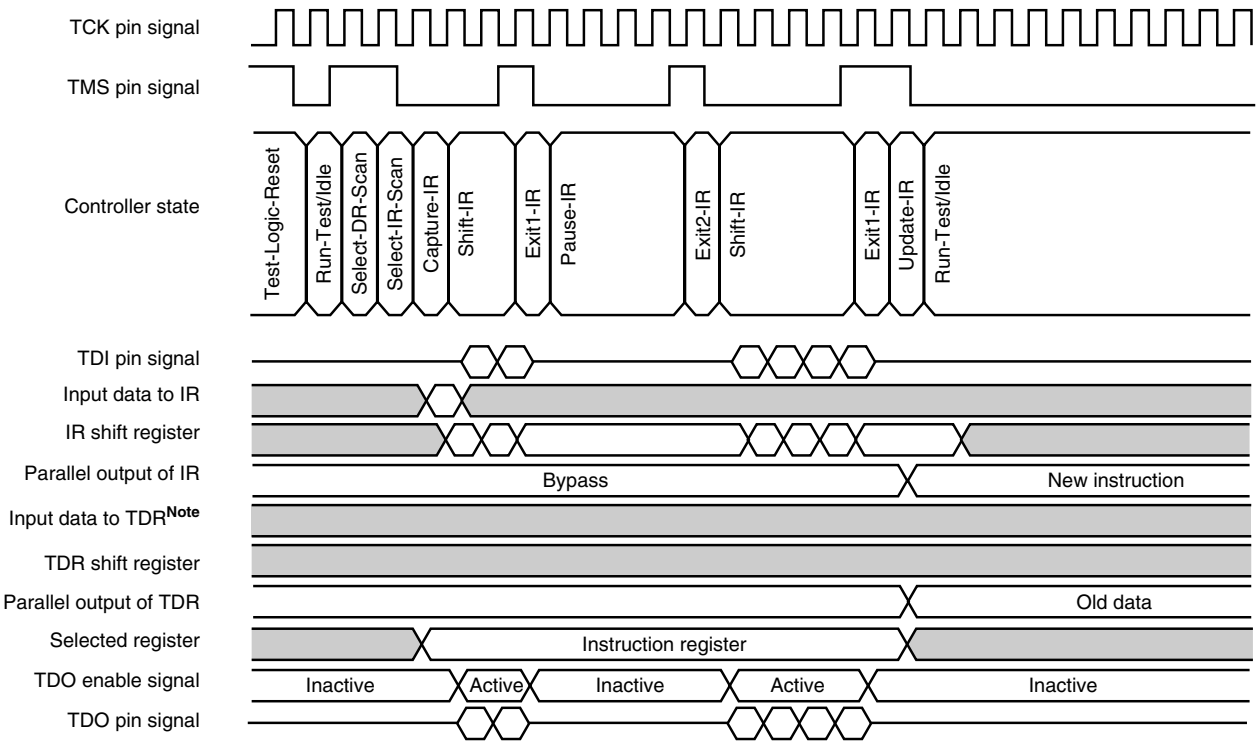
The TAP controller generates signals that control the operations of the bypass register, boundary scan register, and instruction register defined by the IEEE1149.1 JTAG Boundary Scan Standard (refer to **Figures 6-4** and **6-5**).

The TDO pin output buffer and the peripheral circuit that selects a register whose contents are to be output to the TDO pin are controlled as shown in Table 6-1. The TDO pin defined in this table changes at the falling edge of the TCK pin signal after it has entered each state.

Table 6-1. Operation in Each Controller State

Controller State	Selected Register to Be Driven to TDO Pin	TDO Pin Driver
Test-Logic-Reset	Undefined	High impedance
Run-Test/Idle		
Select-DR-Scan		
Select-IR-Scan		
Capture-IR		
Shift-IR	Instruction register	Active
Exit1-IR	Undefined	High impedance
Pause-IR		
Exit2-IR		
Update-IR		
Capture-DR		
Shift-DR	Data register (boundary scan register, bypass register)	Active
Exit1-DR	Undefined	High impedance
Pause-DR		
Exit2-DR		
Update-DR		

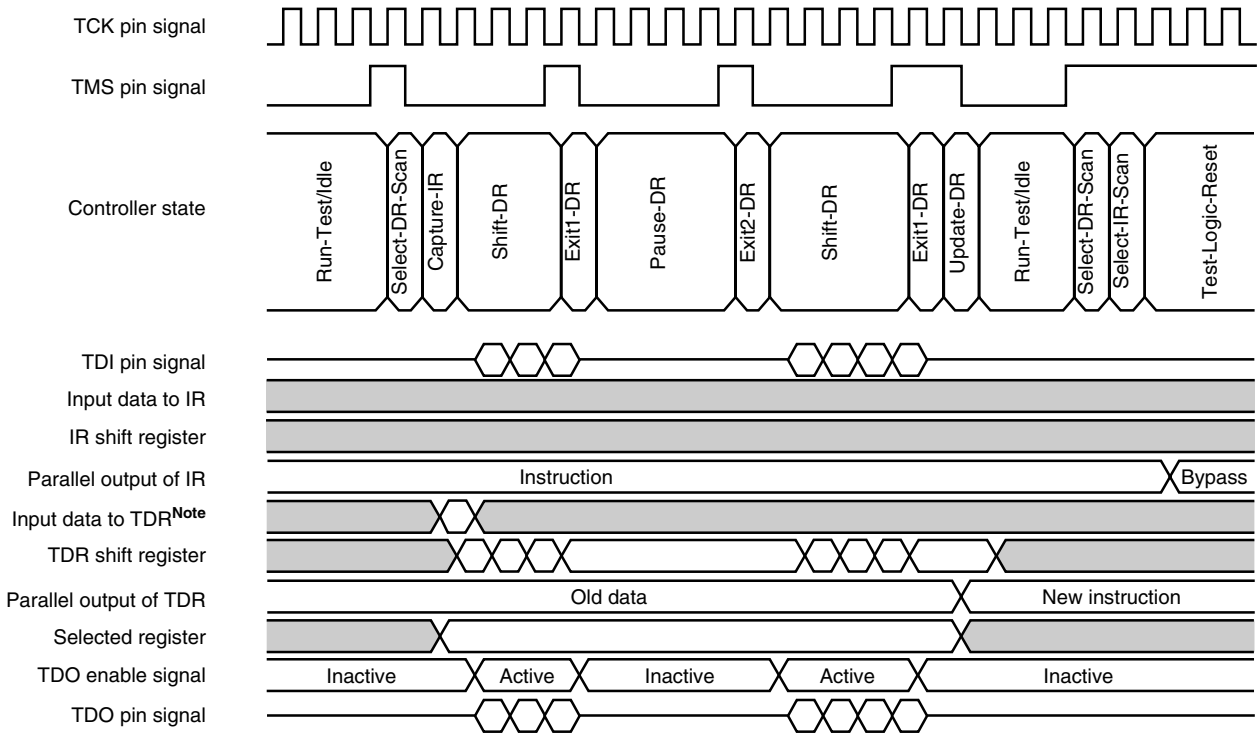
Figure 6-4. Operation of Test Logic (Instruction Scan)



Note TDR (Test Data Register): Boundary scan register and bypass register

Remark : Arbitrary or undefined

Figure 6-5. Operation of Test Logic (Data Scan)



Note TDR (Test Data Register): Boundary scan register and bypass register

Remark ▭: Arbitrary or undefined

6.6 Initializing TAP Controller

The TAP controller is initialized as follows:

(1) The TAP controller is not initialized by the operation of system input such as system reset.
(2) The TAP controller enters the Test-Logic-Reset controller state at the fifth rising edge of the TCK pin signal (while the TMS pin signal is held high).
(3) The TAP controller asynchronously enters the Test-Logic-Reset state when the TRST# signal is input.

6.7 Instruction Register

This register is defined as follows (refer to **6.2 Internal Configuration of Boundary Scan Circuit**).

(1) The instruction shifted and input to the instruction register is latched so that it changes only in the Update-IR and Test-Logic-Reset controller states.
(2) Data is not inverted since it has been serially input to the instruction register until it is serially output.
(3) A fixed binary pattern data “01” (with LSB (Least Significant Bit) being “1”) is loaded to this register cell in the Capture-IR controller state.
(4) A fixed binary pattern data “01” (with LSB being “1”) is loaded to this register cell in the Test-Logic-Reset controller state.
(5) While this register is read, data is output from the TDO pin, starting from the LSB to the MSB (Most Significant Bit), at each falling edge of the TCK pin signal.

The JTAG boundary scan circuit of the μPD98431 can support only the following two instructions depending on the data set to the instruction register.

- BYPASS instruction
- EXTEST instruction
- SAMPLE/PRELOAD instruction

Instruction Register		Supported Instruction
D1	D0	
0	0	EXTEST instruction
0	1	SAMPLE/PRELOAD instruction
1	0	Reserved
1	1	BYPASS instruction

6.7.1 BYPASS instruction

This instruction is specified by instruction data “11”. This instruction is used to select only the bypass register (to access between the TDI and TDO pins serially) in the Shift-DR controller state.

While this instruction is selected, the operation of the JTAG boundary scan circuit does not affect the operation of the μPD98431.

This bypass instruction is selected while the TAP controller is in the Test-Logic-Reset state.

6.7.2 EXTEST instruction

This instruction is specified by instruction data “00”. In the Shift-DR controller state, this instruction is used to select the boundary scan register of serial access between the TDI and TDO instructions.

- While this instruction is selected:

The states of all the signals driven from the system output pins are completely defined by the data shifted to the boundary scan register. In the Update-DR controller state, the states of all the signals are changed only by the falling edge of the TCK pin signal.

The states of all the signals input from the system input pins are loaded to the boundary scan register at the rising edge of the TCK pin signal while the TAP controller is in the Capture-DR state.

6.7.3 SAMPLE/PRELOAD instruction

This instruction is specified by instruction data “01”. This instruction is used to implement two functions: SAMPLE and PRELOAD.

Phase-out/Discontinued

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