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RENESAS

User's Manual

μPD98412

(NEASCOT-X15™)

Advanced ATM Switch LSI

Document No. S14169EJ2V0UMJ1 (2nd edition)
Date Published October 2000 N CP(K)

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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M8E 00.4

MAJOR REVISIONS IN THIS EDITION

Page	Contents
p.20-65	**CHAPTER 1 GENERAL, CHAPTER 2 PIN FUNCTIONS** CBD pins increased
	CHAPTER 3 FUNCTIONAL OUTLINE
p.141	Addition of **Caution** and **Caution 2** in **3.12.4 (2) <Procedure>**
p.153	Change to **Remark** in **3.12.7 (2)**
p.199	Addition of **Caution** in **3.20.1**
p.201	Change to **Figure 3-52**
	CHAPTER 4 INTERNAL REGISTERS
p.213	Addition to **4.3.2 MODE0 register**
P.215	Addition to function of HM field and change of bit 3 setting of EO in **4.3.3 MODE1 register**
p.258	Addition of **4.3.37 Switching mode area setting register**
p.319	Addition of **CHAPTER 7 DIFFERENCE BY STANDARD**

The mark ★ shows major revised points.

[MEMO]

PREFACE

Readers

This manual is intended for user engineers who wish to understand the functions of the μPD98412 and design application systems using it.

Purpose

This manual explains the hardware functions of the μPD98412 in the following organization.

Organization

This manual consists of the following chapters.

- General
- Pin functions
- Functional outline
- Internal registers
- JTAG boundary scan
- Examples of setting and operation
- Difference by standard

How to Read This Manual

It is assumed that the readers of this manual have a general knowledge of electricity, logic circuits, and microcomputers.

To understand the overall functions of the μPD98412
→ Read this manual in the order of Table of Contents.

Conventions

Data significance	:	Left: high-order digit, right: low-order digit
Active low	:	××××_B (_B following pin or signal name)
Memory map address	:	Top: high-order, bottom: low-order
Note	:	Explanation of part of text marked **Note**
Caution	:	Important information
Remark	:	Supplementary information
Numeric notation	:	Binary ... ×××× or ×××B Decimal ... ×××× Hexadecimal ... ××××H

Related documentation

Some of the related documents are preliminary editions but are not so specified below.

- Pamphlet : S14301E
- Data sheet : S14237E

[MEMO]

CONTENTS

LIST OF FIGURES (1/2)

LIST OF FIGURES (2/2)

LIST OF TABLES

CHAPTER 1 GENERAL

The μPD98412 (NEASCOT-X15) is an LSI integrating ATM switch functions on a single chip. It has UTOPIA Level2 interfaces and can switch 30 × 30 circuits by connecting multiple PHY devices. The μPD98412 employs a shared buffer non-blocking type switch and realizes a switch capacity of 1.5G bps by using an externally connected SRAM for buffering cells.

1.1 Features

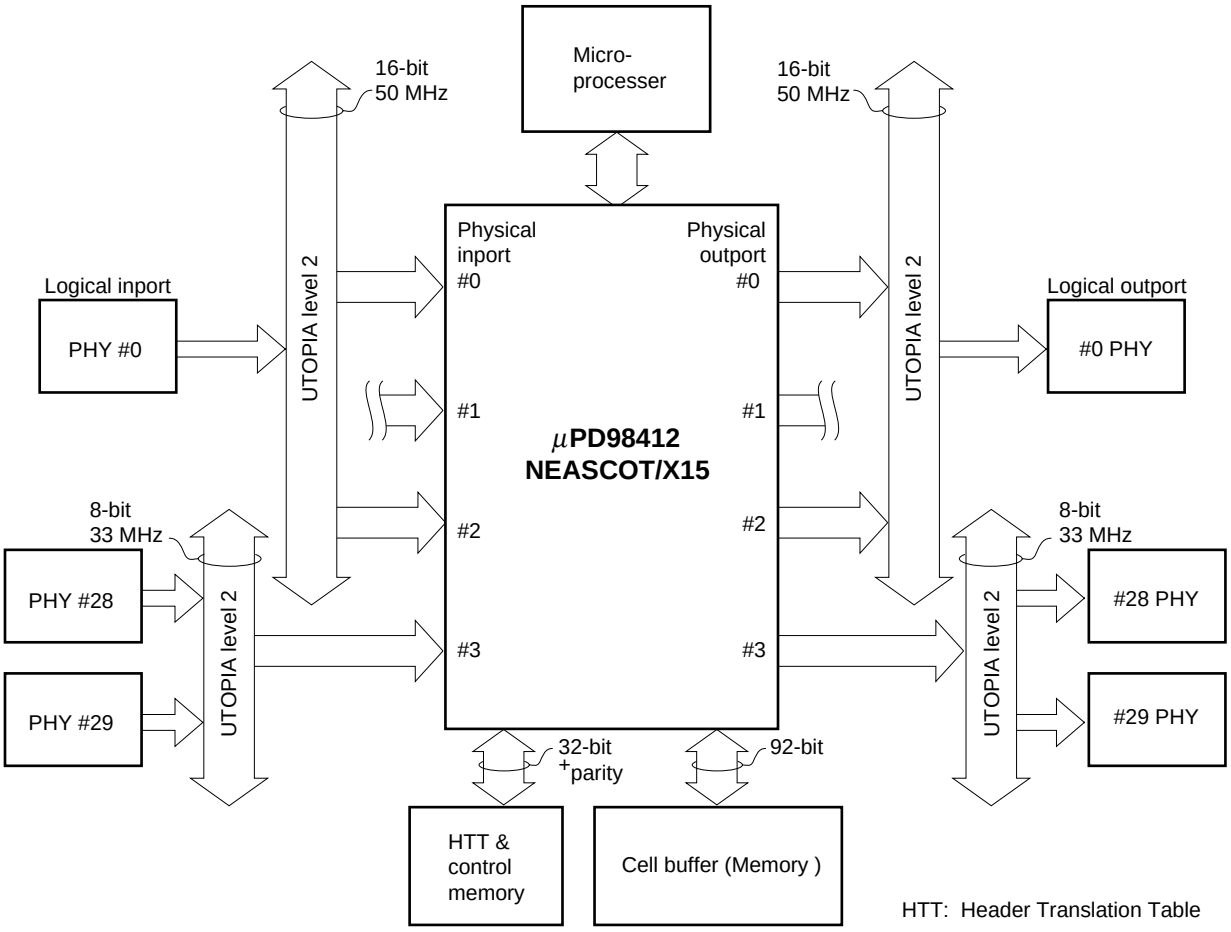
- Conforms to ATM FORUM UNI Version 3.1 & Traffic Management 4.0
- Realizes all switch functions with a single chip
- Non-blocking type with switch capacity of 1.5G bps
- UTOPIA Level2 interface allowing you to select bit widths
  (4 ports × 8 bits, 2 ports × 8 bits + 1 port × 16 bits, 2 ports × 16 bits)
- Various polling modes for UTOPIA Level2 interface
- Can switch 30 logical ports
- Multi-speed (622M bps, 155M bps, 52M bps, 25M bps, etc.)
- Microprocessor connecting port can be set for signaling processing and OAM cell processing
- Supports 16K/32K/64K uni-cast VP/VC and 1K/2K/4K multi-cast VP/VC
- Shared buffer architecture using standard SRAM
- Cell buffer capacity: 12.8K/25.6K/51.2K cells
- Supports four QOS classes (CBR, VBR, ABR, UBR)
- ABR traffic control (binary mode)
- Supports EPD (Early Packet Discard) and PPD (Partial Packet Discard)
- +3.3-V single power source (directly connectable with +5-V TTL level signals)
- Test function: Supports JTAG (IEEE 1149.1)

1.2 Ordering Information

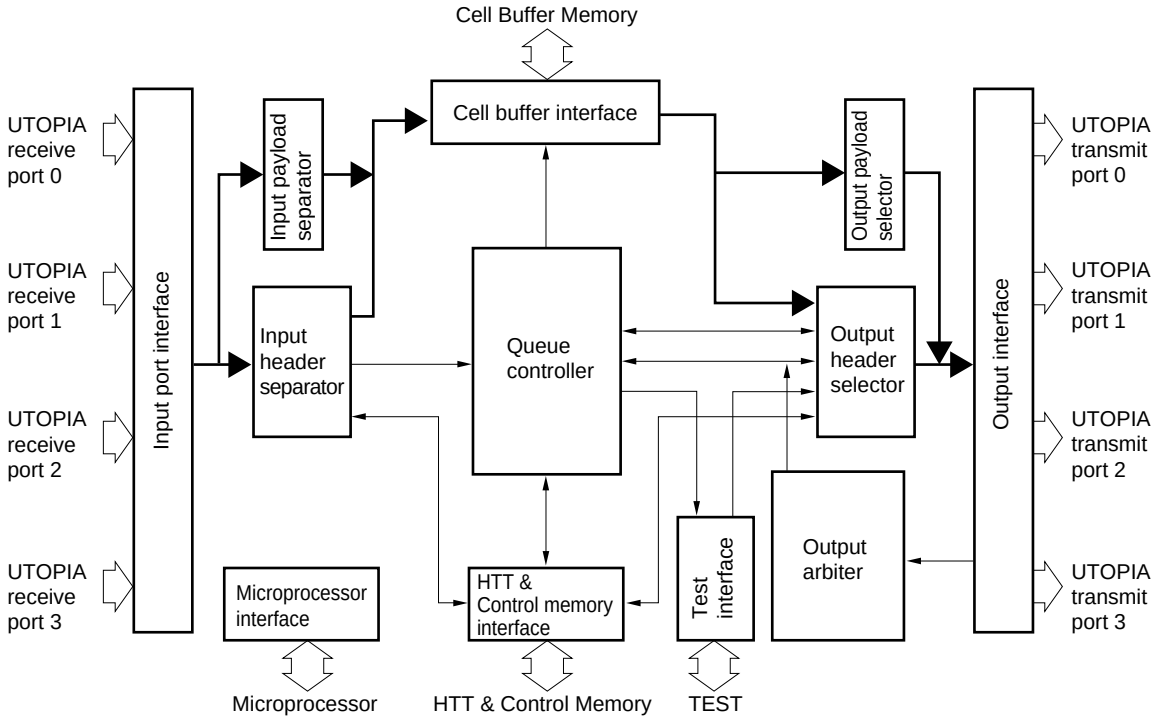
Part Number	Package
μPD98412N7-H6	576-pin tape BGA (40 × 40 mm)

1.3 Example of System Configuration (Application)

The μPD98412 can be used to realize an ATM layer cell switching function by connecting it to a microprocessor, SRAM for use as a cell buffer, and a header translation table (HTT)/SRAM for storing control information as shown below.

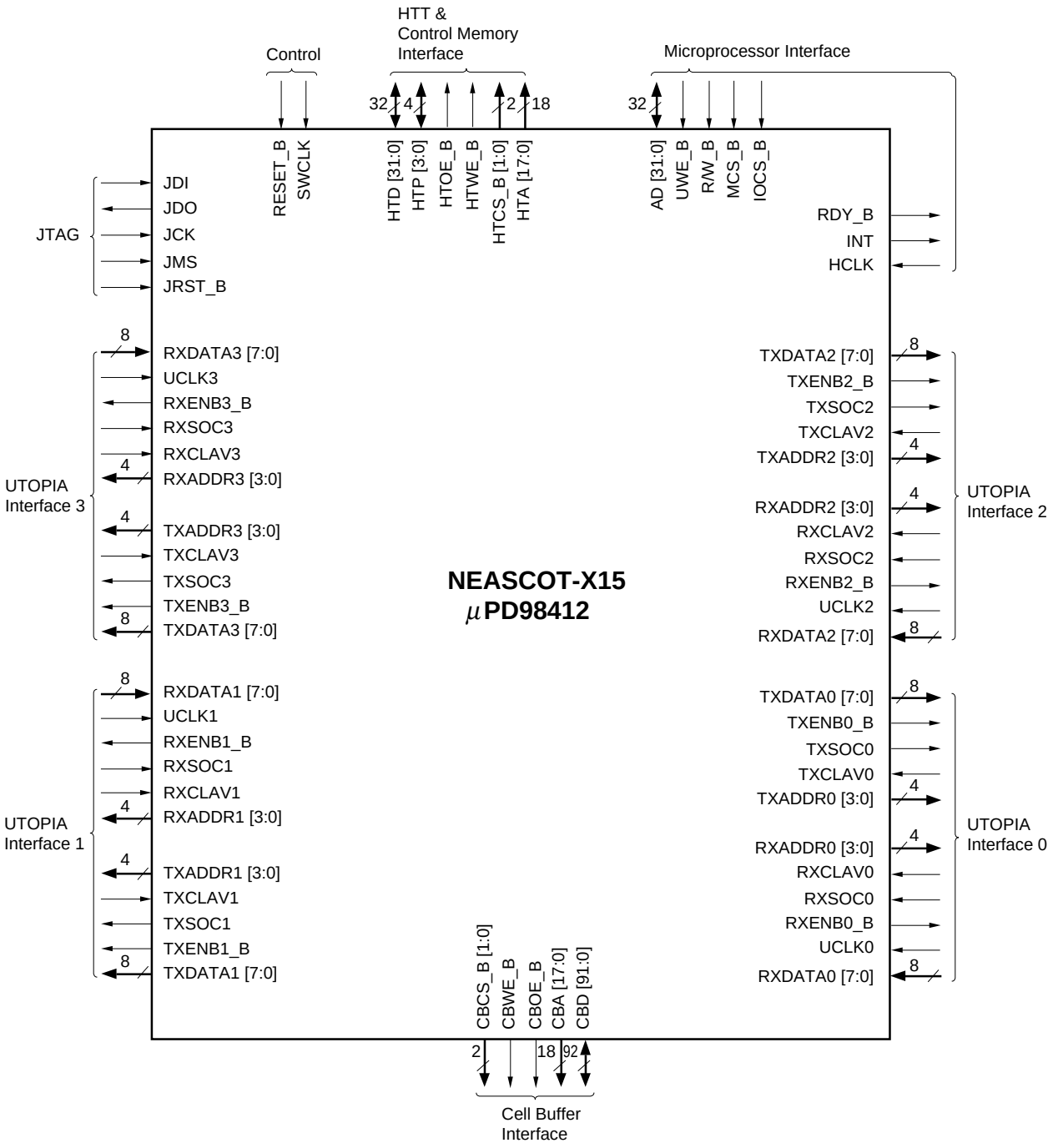


1.4 Block Diagram

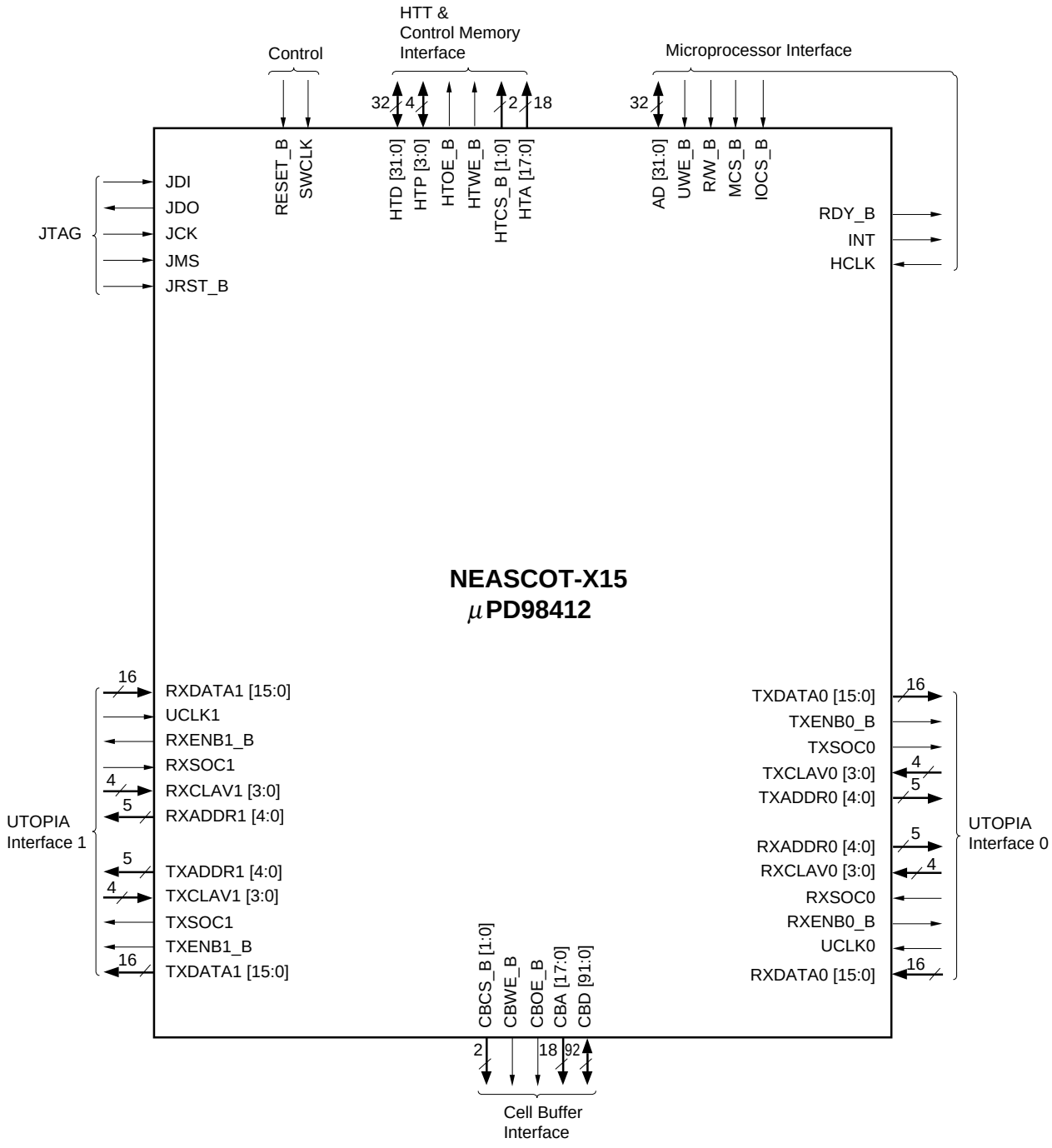


1.5 Pin Configuration

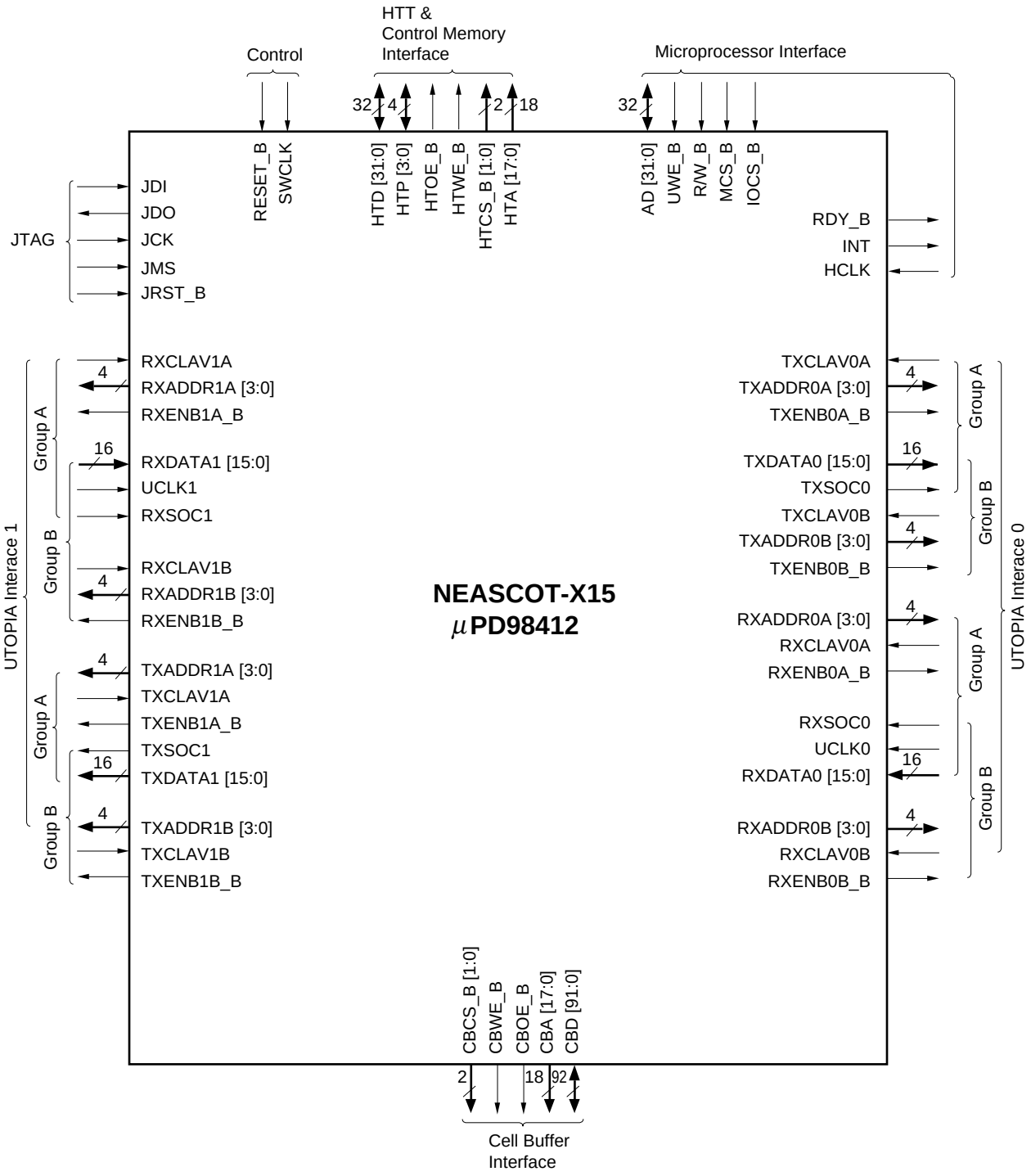
(1) 8-bit 12-PHY polling mode/15-PHY polling mode



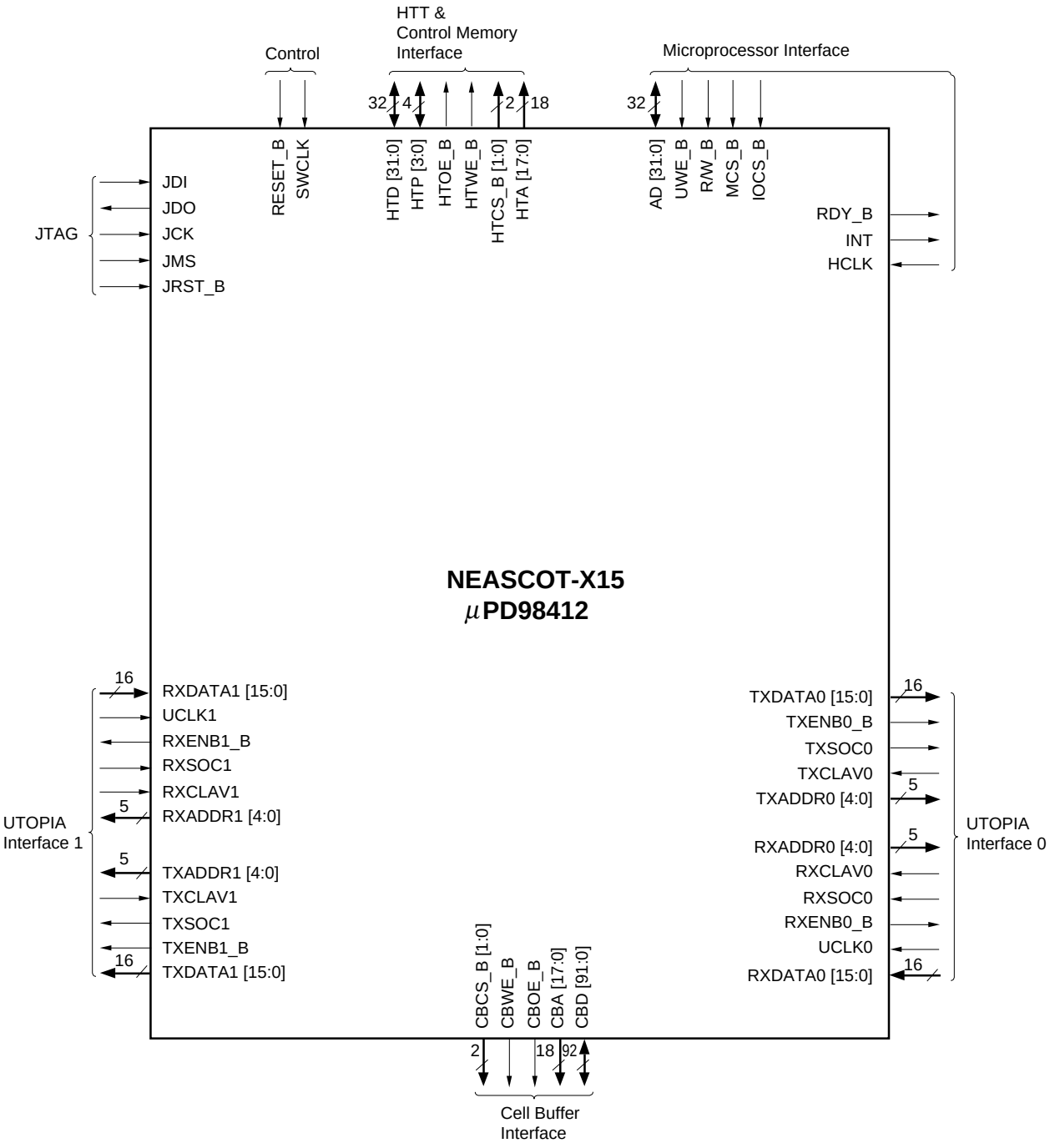
(2) 16-bit multiplexed status polling mode



(3) 16-bit 2-group weighted polling mode



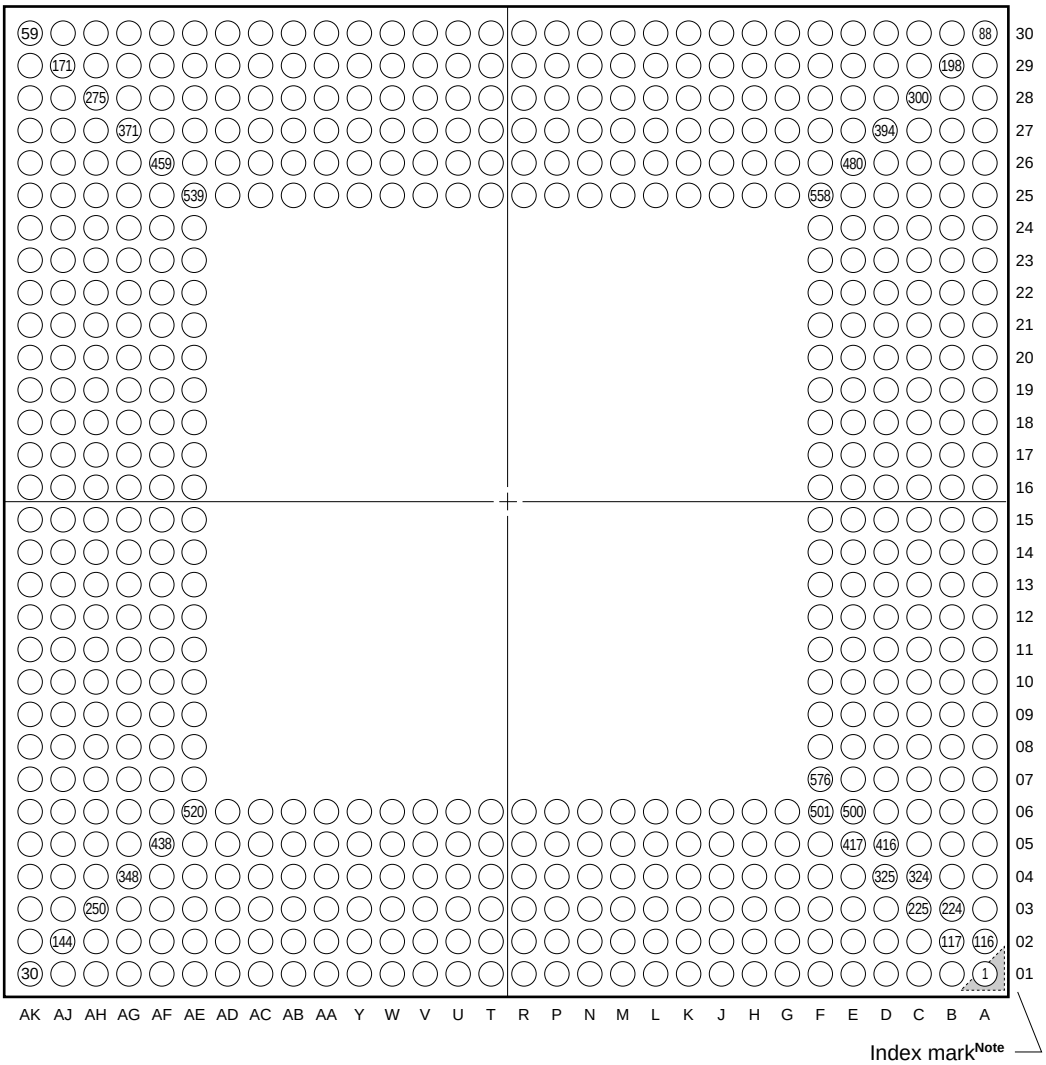
(4) 16-bit 1-group weighted polling mode



[MEMO]

2.1 Pin Configuration (Bottom View)

- **576-pin tape BGA (40 × 40 mm)**
  μPD98412N7-H6



Note The index mark is shown in Top View.

Pin name

1. Power

V_{DD} : Supply Voltage
GND : Ground

2. Memory Interface

HTA17 - HTA0 : HTT Memory Address
HTD31 - HTD0 : HTT Memory Data Bus
HTP3 - HTP0 : HTT Memory Data Bus Parity
HTCS1_B, HTCS0_B : HTT Memory Chip Select
HTWE_B : HTT Memory Write Enable
HTOE_B : HTT Memory Output Enable
CBA17 - CBA0 : Cell Buffer Memory Address
CBD91 - CBD0 : Cell Buffer Memory Data Bus
CBCS1_B, CBCS0_B : Cell Buffer Memory Chip Select
CBWE_B : Cell Buffer Memory Write Enable
CBOE_B : Cell Buffer Memory Output Enable

3. CPU Interface

IOCS_B : I/O Chip Select
MCS_B : Memory Chip Select
RDY_B : I/O Ready, Memory Ready
INT : Interrupt Request
HCLK : Host Clock
AD31 - AD00 : Address and Data
R/W_B : Read/Write
UWE_B : Upper Word Enable

4. JTAG

JDI : JTAG Data Input
JDO : JTAG Data Output
JCK : JTAG Data Clock
JMS : JTAG Mode Select
JRST_B : JTAG Reset

5. Other

SWCLK : System Clock
RESET_B : Hardware Reset
IC : Internal Connected
CG : Connect Ground
PU : Pull-up

6. UTOPIA

(1) 8-bit 12-PHY Polling Mode/15-PHY Polling Mode

UCLK0 : UTOPIA Clock
RXADDR03-RXADDR00 : Receive Address
RXDATA007-RXDATA000 : Receive Data Bus
RXSOC0 : Receive Start of Cell
RXENB0_B : Receive Enable Data Transfers
RXCLAV0 : Receive Cell Buffer Available
TXADDR03-TXADDR00 : Transmit Address
TXDATA007-TXDATA000 : Transmit Data Bus
TXSOC0 : Transmit Start of Cell
TXENB0_B : Transmit Enable Data Transfers
TXCLAV0 : Transmit Cell Buffer Available
UCLK1 : UTOPIA Clock
RXADDR13-RXADDR10 : Receive Address
RXDATA107-RXDATA100 : Receive Data Bus
RXSOC1 : Receive Start of Cell
RXENB1_B : Receive Enable Data Transfers
RXCLAV1 : Receive Cell Buffer Available
TXADDR13-TXADDR10 : Transmit Address
TXDATA107-TXDATA100 : Transmit Data Bus
TXSOC1 : Transmit Start of Cell
TXENB1_B : Transmit Enable Data Transfers
TXCLAV1 : Transmit Cell Buffer Available
UCLK2 : UTOPIA Clock
RXADDR23-RXADDR20 : Receive Address
RXDATA207-RXDATA200 : Receive Data Bus
RXSOC2 : Receive Start of Cell
RXENB2_B : Receive Enable Data Transfers
RXCLAV2 : Receive Cell Buffer Available
TXADDR23-TXADDR20 : Transmit Address
TXDATA207-TXDATA200 : Transmit Data Bus
TXSOC2 : Transmit Start of Cell
TXENB2_B : Transmit Enable Data Transfers
TXCLAV2 : Transmit Cell Buffer Available
UCLK3 : UTOPIA Clock
RXADDR33-RXADDR30 : Receive Address
RXDATA307-RXDATA300 : Receive Data Bus
RXSOC3 : Receive Start of Cell
RXENB3_B : Receive Enable Data Transfers
RXCLAV3 : Receive Cell Buffer Available
TXADDR33-TXADDR30 : Transmit Address
TXDATA307-TXDATA300 : Transmit Data Bus
TXSOC3 : Transmit Start of Cell
TXENB3_B : Transmit Enable Data Transfers
TXCLAV3 : Transmit Cell Buffer Available

(2) 16-bit Multiplexed Status Polling Mode

UCLK0 : UTOPIA Clock
RXADDR04-RXADDR00 : Receive Address
RXDATA015-RXDATA000 : Receive Data Bus
RXSOC0 : Receive Start of Cell
RXENB0_B : Receive Enable Data Transfers
RXCLAV0[3]-RXCLAV0[0] : Receive Cell Buffer Available
TXADDR04-TXADDR00 : Transmit Address
TXDATA015-TXDATA000 : Transmit Data Bus
TXSOC0 : Transmit Start of Cell
TXENB0_B : Transmit Enable Data Transfers
TXCLAV0[3]-TXCLAV0[0] : Transmit Cell Buffer Available
UCLK1 : UTOPIA Clock
RXADDR14-RXADDR10 : Receive Address
RXDATA115-RXDATA100 : Receive Data Bus
RXSOC1 : Receive Start of Cell
RXENB1_B : Receive Enable Data Transfers
RXCLAV1[3]-RXCLAV1[0] : Receive Cell Buffer Available
TXADDR14-TXADDR10 : Transmit Address
TXDATA115-TXDATA100 : Transmit Data Bus
TXSOC1 : Transmit Start of Cell
TXENB1_B : Transmit Enable Data
TXCLAV1[3]-TXCLAV1[0] : Transmit Cell Buffer Available

(3) 16-bit 2-Group Weighted Polling Mode

UCLK0 : UTOPIA Clock
RXADDR0A3-RXADDR0A0 : Receive Address
RXADDR0B3-RXADDR0B0 : Receive Address
RXDATA015-RXDATA000 : Receive Data Bus
RXSOC0 : Receive Start of Cell
RXENB0A_B, RXENB0B_B : Receive Enable Data Transfers
RXCLAV0A, RXCLAV0B : Receive Cell Buffer Available
TXADDR0A3-TXADDR0A0 : Transmit Address
TXADDR0B3-TXADDR0B0 : Transmit Address
TXDATA015-TXDATA000 : Transmit Data Bus
TXSOC0 : Transmit Start of Cell
TXENB0A_B, TXENB0B_B : Transmit Enable Data Transfers
TXCLAV0A, TXCLAV0B : Transmit Cell Buffer Available
UCLK1 : UTOPIA Clock
RXADDR1A3-RXADDR1A0 : Receive Address
RXADDR1B3-RXADDR1B0 : Receive Address
RXDATA115-RXDATA100 : Receive Data Bus
RXSOC1 : Receive Start of Cell
RXENB1A_B, RXENB1B_B : Receive Enable Data Transfers
RXCLAV1A, RXCLAV1B : Receive Cell Buffer Available
TXADDR1A3-TXADDR1A0 : Transmit Address
TXADDR1B3-TXADDR1B0 : Transmit Address
TXDATA115-TXDATA100 : Transmit Data Bus
TXSOC1 : Transmit Start of Cell
TXENB1A_B, TXENB1B_B : Transmit Enable Data Transfers
TXCLAV1A, TXCLAV1B : Transmit Cell Buffer Available

(4) 16-bit 1-Group Weighted Polling Mode

UCLK0 : UTOPIA Clock
RXADDR04-RXADDR00 : Receive Address
RXDATA015-RXDATA000 : Receive Data Bus
RXSOC0 : Receive Start of Cell
RXENB0_B : Receive Enable Data Transfers
RXCLAV0 : Receive Cell Buffer Available
TXADDR04-TXADDR00 : Transmit Address
TXDATA015-TXDATA000 : Transmit Data Bus
TXSOC0 : Transmit Start of Cell
TXENB0_B : Transmit Enable Data Transfers
TXCLAV0 : Transmit Cell Buffer Available
UCLK1 : UTOPIA Clock
RXADDR14-RXADDR10 : Receive Address
RXDATA115-RXDATA100 : Receive Data Bus
RXSOC1 : Receive Start of Cell
RXENB1_B : Receive Enable Data Transfers
RXCLAV1 : Receive Cell Buffer Available
TXADDR14-TXADDR10 : Transmit Address
TXDATA115-TXDATA100 : Transmit Data Bus
TXSOC1 : Transmit Start of Cell
TXENB1_B : Transmit Enable Data Transfers
TXCLAV1 : Transmit Cell Buffer Available

2.2 Pin Layout

(1/15)

Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
1	A01	AD30	←	←	←	I/O
2	B01	GND	←	←	←	
3	C01	AD24	←	←	←	I/O
4	D01	AD20	←	←	←	I/O
5	E01	AD16	←	←	←	I/O
6	F01	GND	←	←	←	
7	G01	AD10	←	←	←	I/O
8	H01	AD06	←	←	←	I/O
9	J01	GND	←	←	←	
10	K01	AD01	←	←	←	I/O
11	L01	HTA17	←	←	←	O
12	M01	HTA13	←	←	←	O
13	N01	HTA09	←	←	←	O
14	P01	GND	←	←	←	
15	R01	HTA06	←	←	←	O
16	T01	HTA02	←	←	←	O
17	U01	HTCS0_B	←	←	←	O
18	V01	HTD31	←	←	←	I/O
19	W01	HTD29	←	←	←	I/O
20	Y01	V_{DD}	←	←	←	
21	AA01	HTD24	←	←	←	I/O
22	AB01	HTD21	←	←	←	I/O
23	AC01	HTD17	←	←	←	I/O
24	AD01	HTP1	←	←	←	I/O
25	AE01	V_{DD}	←	←	←	
26	AF01	GND	←	←	←	
27	AG01	HTD06	←	←	←	I/O
28	AH01	HTD05	←	←	←	I/O
29	AJ01	HTD01	←	←	←	I/O
30	AK01	PU	←	←	←	I
31	AK02	V_{DD}	←	←	←	
32	AK03	GND	←	←	←	
33	AK04	JCK	←	←	←	I
34	AK05	RXDATA307	RXDATA115	RXDATA115	RXDATA115	I
35	AK06	V_{DD}	←	←	←	
36	AK07	RXDATA301	RXDATA109	RXDATA109	RXDATA109	I
37	AK08	GND	←	←	←	
38	AK09	RXCLAV3	RXCLAV1[2]	RXCLAV1B	CG	I
39	AK10	V_{DD}	←	←	←	
40	AK11	TXADDR33	IC	TXADDR1B3	IC	O

(2/15)

Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
41	AK12	CG	TXCLAV1[3]	CG	CG	I
42	AK13	TXDATA307	TXDATA115	TXDATA115	TXDATA115	O
43	AK14	V_{DD}	←	←	←	
44	AK15	TXDATA304	TXDATA112	TXDATA112	TXDATA112	O
45	AK16	TXDATA300	TXDATA108	TXDATA108	TXDATA108	O
46	AK17	RXDATA104	RXDATA104	RXDATA104	RXDATA104	I
47	AK18	RXDATA100	RXDATA100	RXDATA100	RXDATA100	I
48	AK19	UCLK1	UCLK1	UCLK1	UCLK1	I
49	AK20	RXCLAV1	RXCLAV1[0]	RXCLAV1A	RXCLAV1	I
50	AK21	RXADDR12	RXADDR12	RXADDR1A2	RXADDR12	O
51	AK22	TXADDR12	TXADDR12	TXADDR1A2	TXADDR12	O
52	AK23	TXCLAV1	TXCLAV1[0]	TXCLAV1A	TXCLAV1	I
53	AK24	TXDATA107	TXDATA107	TXDATA107	TXDATA107	O
54	AK25	TXDATA103	TXDATA103	TXDATA103	TXDATA103	O
55	AK26	CBD87	←	←	←	I/O
56	AK27	CBD84	←	←	←	I/O
57	AK28	V_{DD}	←	←	←	
58	AK29	GND	←	←	←	
59	AK30	CBD77	←	←	←	I/O
60	AJ30	GND	←	←	←	
61	AH30	V_{DD}	←	←	←	
62	AG30	CBD68	←	←	←	I/O
63	AF30	CBD64	←	←	←	I/O
64	AE30	V_{DD}	←	←	←	
65	AD30	CBD58	←	←	←	I/O
66	AC30	CBD54	←	←	←	I/O
67	AB30	V_{DD}	←	←	←	
68	AA30	CBD49	←	←	←	I/O
69	Y30	CBD47	←	←	←	I/O
70	W30	CBCS1_B	←	←	←	O
71	V30	CBA17	←	←	←	O
72	U30	V_{DD}	←	←	←	
73	T30	CBA14	←	←	←	O
74	R30	CBA10	←	←	←	O
75	P30	CBA06	←	←	←	O
76	N30	CBA02	←	←	←	O
77	M30	CBA00	←	←	←	O
78	L30	V_{DD}	←	←	←	
79	K30	CBD39	←	←	←	I/O
80	J30	CBD35	←	←	←	I/O

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
81	H30	V_{DD}	←	←	←	
82	G30	CBD29	←	←	←	I/O
83	F30	CBD25	←	←	←	I/O
84	E30	GND	←	←	←	
85	D30	CBD18	←	←	←	I/O
86	C30	V_{DD}	←	←	←	
87	B30	V_{DD}	←	←	←	
88	A30	CBD11	←	←	←	I/O
89	A29	V_{DD}	←	←	←	
90	A28	CBD05	←	←	←	I/O
91	A27	CBD01	←	←	←	I/O
92	A26	RXDATA005	RXDATA005	RXDATA005	RXDATA005	I
93	A25	RXDATA003	RXDATA003	RXDATA003	RXDATA003	I
94	A24	V_{DD}	←	←	←	
95	A23	RXCLAV0	RXCLAV0[0]	RXCLAV0A	RXCLAV0	I
96	A22	V_{DD}	←	←	←	
97	A21	TXADDR03	TXADDR03	TXADDR03	TXADDR03	O
98	A20	TXADDR01	TXADDR01	TXADDR01	TXADDR01	O
99	A19	TXSOC0	TXSOC0	TXSOC0	TXSOC0	O
100	A18	TXDATA005	TXDATA005	TXDATA005	TXDATA005	O
101	A17	GND	←	←	←	
102	A16	TXDATA001	TXDATA001	TXDATA001	TXDATA001	O
103	A15	RXDATA205	RXDATA013	RXDATA013	RXDATA013	I
104	A14	RXDATA201	RXDATA009	RXDATA009	RXDATA009	I
105	A13	RXENB2_B	IC	RXENB0B_B	IC	O
106	A12	RXCLAV2	RXCLAV0[2]	RXCLAV0B	CG	I
107	A11	RXADDR21	IC	RXADDR0B1	IC	O
108	A10	TXADDR22	IC	TXADDR0B2	IC	O
109	A09	TXCLAV2	TXCLAV0[2]	TXCLAV0B	CG	I
110	A08	GND	←	←	←	
111	A07	TXDATA203	TXDATA011	TXDATA011	TXDATA011	O
112	A06	V_{DD}	←	←	←	
113	A05	GND	←	←	←	
114	A04	R/W_B	←	←	←	I
115	A03	UWE_B	←	←	←	I
116	A02	CG	←	←	←	I
117	B02	AD29	←	←	←	I/O
118	C02	AD27	←	←	←	I/O
119	D02	V_{DD}	←	←	←	
120	E02	AD19	←	←	←	I/O

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
121	F02	AD15	←	←	←	I/O
122	G02	AD11	←	←	←	I/O
123	H02	AD09	←	←	←	I/O
124	J02	AD05	←	←	←	I/O
125	K02	AD04	←	←	←	I/O
126	L02	AD00	←	←	←	I/O
127	M02	HTA14	←	←	←	O
128	N02	HTA10	←	←	←	O
129	P02	V_{DD}	←	←	←	
130	R02	HTA05	←	←	←	O
131	T02	HTA01	←	←	←	O
132	U02	HTWE_B	←	←	←	O
133	V02	HTD30	←	←	←	I/O
134	W02	HTD26	←	←	←	I/O
135	Y02	HTD25	←	←	←	I/O
136	AA02	HTD22	←	←	←	I/O
137	AB02	HTD20	←	←	←	I/O
138	AC02	HTD16	←	←	←	I/O
139	AD02	HTD13	←	←	←	I/O
140	AE02	HTD10	←	←	←	I/O
141	AF02	HTD07	←	←	←	I/O
142	AG02	HTD02	←	←	←	I/O
143	AH02	GND	←	←	←	
144	AJ02	GND	←	←	←	
145	AJ03	CBD91	←	←	←	I/O
146	AJ04	JDO	←	←	←	O
147	AJ05	V_{DD}	←	←	←	
148	AJ06	RXDATA306	RXDATA114	RXDATA114	RXDATA114	I
149	AJ07	RXDATA302	RXDATA110	RXDATA110	RXDATA110	I
150	AJ08	RXDATA300	RXDATA108	RXDATA108	RXDATA108	I
151	AJ09	RXENB3_B	IC	RXENB1B_B	IC	O
152	AJ10	V_{DD}	←	←	←	
153	AJ11	RXADDR30	RXADDR14	RXADDR1B0	RXADDR14	O
154	AJ12	TXADDR30	TXADDR14	TXADDR1B0	TXADDR14	O
155	AJ13	TXENB3_B	IC	TXENB1B_B	IC	O
156	AJ14	GND	←	←	←	
157	AJ15	TXDATA303	TXDATA111	TXDATA111	TXDATA111	O
158	AJ16	RXDATA107	RXDATA107	RXDATA107	RXDATA107	I
159	AJ17	RXDATA103	RXDATA103	RXDATA103	RXDATA103	I
160	AJ18	V_{DD}	←	←	←	

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
161	AJ19	V_{DD}	←	←	←	
162	AJ20	GND	←	←	←	
163	AJ21	TXADDR13	TXADDR13	TXADDR1A3	TXADDR13	O
164	AJ22	TXADDR10	TXADDR10	TXADDR1A0	TXADDR10	O
165	AJ23	TXENB1_B	TXENB1_B	TXENB1A_B	TXENB1_B	O
166	AJ24	TXDATA104	TXDATA104	TXDATA104	TXDATA104	O
167	AJ25	TXDATA101	TXDATA101	TXDATA101	TXDATA101	O
168	AJ26	CBD85	←	←	←	I/O
169	AJ27	V_{DD}	←	←	←	
170	AJ28	CBD80	←	←	←	I/O
171	AJ29	CBD76	←	←	←	I/O
172	AH29	CBD74	←	←	←	I/O
173	AG29	GND	←	←	←	
174	AF29	CBD67	←	←	←	I/O
175	AE29	CBD63	←	←	←	I/O
176	AD29	CBD59	←	←	←	I/O
177	AC29	CBD57	←	←	←	I/O
178	AB29	CBD53	←	←	←	I/O
179	AA29	CBD52	←	←	←	I/O
180	Y29	CBD48	←	←	←	I/O
181	W29	CBD44	←	←	←	I/O
182	V29	CBOE_B	←	←	←	O
183	U29	GND	←	←	←	
184	T29	CBA13	←	←	←	O
185	R29	CBA09	←	←	←	O
186	P29	CBA05	←	←	←	O
187	N29	CBA01	←	←	←	O
188	M29	CBD41	←	←	←	I/O
189	L29	CBD40	←	←	←	I/O
190	K29	CBD36	←	←	←	I/O
191	J29	CBD34	←	←	←	I/O
192	H29	CBD30	←	←	←	I/O
193	G29	CBD26	←	←	←	I/O
194	F29	CBD23	←	←	←	I/O
195	E29	CBD19	←	←	←	I/O
196	D29	GND	←	←	←	
197	C29	CBD14	←	←	←	I/O
198	B29	CBD10	←	←	←	I/O
199	B28	CBD08	←	←	←	I/O
200	B27	CBD02	←	←	←	I/O

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
201	B26	CBD00	←	←	←	I/O
202	B25	RXDATA004	RXDATA004	RXDATA004	RXDATA004	I
203	B24	RXDATA000	RXDATA000	RXDATA000	RXDATA000	I
204	B23	RXENB0_B	RXENB0_B	RXENB0A_B	RXENB0_B	O
205	B22	RXADDR03	RXADDR03	RXADDR0A3	RXADDR03	O
206	B21	RXADDR02	RXADDR02	RXADDR0A2	RXADDR02	O
207	B20	TXADDR02	TXADDR02	TXADDR0A2	TXADDR02	O
208	B19	TXCLAV0	TXCLAV0[0]	TXCLAV0A	TXCLAV0	I
209	B18	TXDATA006	TXDATA006	TXDATA006	TXDATA006	O
210	B17	TXDATA002	TXDATA002	TXDATA002	TXDATA002	O
211	B16	TXDATA000	TXDATA000	TXDATA000	TXDATA000	O
212	B15	RXDATA204	RXDATA012	RXDATA012	RXDATA012	I
213	B14	RXDATA200	RXDATA008	RXDATA008	RXDATA008	I
214	B13	RXSOC2	RXLLAV0[3]	CG	CG	I
215	B12	GND	←	←	←	
216	B11	TXADDR23	IC	TXADDR0B3	IC	O
217	B10	CG	TXCLAV0[3]	CG	CG	I
218	B09	TXENB2_B	IC	TXENB0B_B	IC	O
219	B08	TXDATA204	TXDATA012	TXDATA012	TXDATA012	O
220	B07	TXDATA200	TXDATA008	TXDATA008	TXDATA008	O
221	B06	IOCS_B	←	←	←	I
222	B05	CG	←	←	←	I
223	B04	CG	←	←	←	I
224	B03	IC	←	←	←	O
225	C03	AD28	←	←	←	I/O
226	D03	AD26	←	←	←	I/O
227	E03	AD22	←	←	←	I/O
228	F03	AD18	←	←	←	I/O
229	G03	AD14	←	←	←	I/O
230	H03	V_{DD}	←	←	←	
231	J03	AD08	←	←	←	I/O
232	K03	V_{DD}	←	←	←	
233	L03	GND	←	←	←	
234	M03	HTA15	←	←	←	O
235	N03	HTA11	←	←	←	O
236	P03	HTA07	←	←	←	O
237	R03	HTA03	←	←	←	O
238	T03	HTA00	←	←	←	O
239	U03	HTOE_B	←	←	←	O
240	V03	V_{DD}	←	←	←	

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
241	W03	GND	←	←	←	
242	Y03	HTD23	←	←	←	I/O
243	AA03	V_{DD}	←	←	←	
244	AB03	GND	←	←	←	
245	AC03	HTD14	←	←	←	I/O
246	AD03	HTD11	←	←	←	I/O
247	AE03	HTP0	←	←	←	I/O
248	AF03	HTD03	←	←	←	I/O
249	AG03	HTD00	←	←	←	I/O
250	AH03	IC	←	←	←	O
251	AH04	CBD90	←	←	←	I/O
252	AH05	JDI	←	←	←	I
253	AH06	JMS	←	←	←	I
254	AH07	RXDATA305	RXDATA113	RXDATA113	RXDATA113	I
255	AH08	GND	←	←	←	
256	AH09	GND	←	←	←	
257	AH10	RXSOC3	RXCLAV1[3]	CG	CG	I
258	AH11	RXADDR31	IC	RXADDR1B1	IC	O
259	AH12	TXADDR31	IC	TXADDR1B1	IC	O
260	AH13	TXSOC3	IC	IC	IC	O
261	AH14	TXDATA305	TXDATA113	TXDATA113	TXDATA113	O
262	AH15	TXDATA301	TXDATA109	TXDATA109	TXDATA109	O
263	AH16	RXDATA106	RXDATA106	RXDATA106	RXDATA106	I
264	AH17	RXDATA102	RXDATA102	RXDATA102	RXDATA102	I
265	AH18	GND	←	←	←	
266	AH19	RXADDR13	RXADDR13	RXADDR1A3	RXADDR13	O
267	AH20	RXADDR10	RXADDR10	RXADDR1A0	RXADDR10	O
268	AH21	TXADDR11	TXADDR11	TXADDR1A1	TXADDR11	O
269	AH22	TXSOC1	TXSOC1	TXSOC1	TXSOC1	O
270	AH23	TXDATA105	TXDATA105	TXDATA105	TXDATA105	O
271	AH24	TXDATA102	TXDATA102	TXDATA102	TXDATA102	O
272	AH25	CBD86	←	←	←	I/O
273	AH26	CBD81	←	←	←	I/O
274	AH27	CBD79	←	←	←	I/O
275	AH28	CBD75	←	←	←	I/O
276	AG28	CBD73	←	←	←	I/O
277	AF28	CBD69	←	←	←	I/O
278	AE28	CBD66	←	←	←	I/O
279	AD28	CBD62	←	←	←	I/O
280	AC28	GND	←	←	←	

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
281	AB28	CBD56	←	←	←	I/O
282	AA28	GND	←	←	←	
283	Y28	V_{DD}	←	←	←	
284	W28	CBD45	←	←	←	I/O
285	V28	CBWE_B	←	←	←	O
286	U28	CBA15	←	←	←	O
287	T28	CBA11	←	←	←	O
288	R28	CBA08	←	←	←	O
289	P28	CBA04	←	←	←	O
290	N28	V_{DD}	←	←	←	
291	M28	GND	←	←	←	
292	L28	CBD37	←	←	←	I/O
293	K28	V_{DD}	←	←	←	
294	J28	CBD31	←	←	←	I/O
295	H28	CBD27	←	←	←	I/O
296	G28	CBD24	←	←	←	I/O
297	F28	CBD20	←	←	←	I/O
298	E28	CBD15	←	←	←	I/O
299	D28	CBD13	←	←	←	I/O
300	C28	CBD09	←	←	←	I/O
301	C27	CBD07	←	←	←	I/O
302	C26	CBD03	←	←	←	I/O
303	C25	RXDATA007	RXDATA007	RXDATA007	RXDATA007	I
304	C24	GND	←	←	←	
305	C23	GND	←	←	←	
306	C22	RXSOC0	RXSOC0	RXSOC0	RXSOC0	I
307	C21	GND	←	←	←	
308	C20	V_{DD}	←	←	←	
309	C19	CG	TXCLAV0[1]	CG	CG	I
310	C18	TXDATA007	TXDATA007	TXDATA007	TXDATA007	O
311	C17	TXDATA003	TXDATA003	TXDATA003	TXDATA003	O
312	C16	RXDATA206	RXDATA014	RXDATA014	RXDATA014	I
313	C15	GND	←	←	←	
314	C14	GND	←	←	←	
315	C13	V_{DD}	←	←	←	
316	C12	RXADDR20	RXADDR04	RXADDR0B0	RXADDR04	O
317	C11	TXADDR20	TXADDR04	TXADDR0B0	TXADDR04	O
318	C10	TXSOC2	IC	IC	IC	O
319	C09	TXDATA205	TXDATA013	TXDATA013	TXDATA013	O
320	C08	TXDATA201	TXDATA009	TXDATA009	TXDATA009	O

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
321	C07	CG	←	←	←	I
322	C06	RDY_B	←	←	←	O
323	C05	GND	←	←	←	
324	C04	V_{DD}	←	←	←	
325	D04	V_{DD}	←	←	←	
326	E04	AD25	←	←	←	I/O
327	F04	GND	←	←	←	
328	G04	AD17	←	←	←	I/O
329	H04	V_{DD}	←	←	←	
330	J04	GND	←	←	←	
331	K04	AD07	←	←	←	I/O
332	L04	V_{DD}	←	←	←	
333	M04	HTA16	←	←	←	O
334	N04	HTA12	←	←	←	O
335	P04	HTA08	←	←	←	O
336	R04	HTA04	←	←	←	O
337	T04	V_{DD}	←	←	←	
338	U04	HTP3	←	←	←	I/O
339	V04	GND	←	←	←	
340	W04	HTP2	←	←	←	I/O
341	Y04	GND	←	←	←	
342	AA04	V_{DD}	←	←	←	
343	AB04	HTD15	←	←	←	I/O
344	AC04	HTD12	←	←	←	I/O
345	AD04	HTD08	←	←	←	I/O
346	AE04	HTD04	←	←	←	I/O
347	AF04	RESET_B	←	←	←	I
348	AG04	IC	←	←	←	O
349	AG05	CBD89	←	←	←	I/O
350	AG06	IC	←	←	←	
351	AG07	JRST_B	←	←	←	I
352	AG08	GND	←	←	←	
353	AG09	V_{DD}	←	←	←	
354	AG10	UCLK3	CG	CG	CG	I
355	AG11	RXADDR32	IC	RXADDR1B2	IC	O
356	AG12	TXADDR32	IC	TXADDR1B2	IC	O
357	AG13	TXCLAV3	TXCLAV1[2]	TXCLAV1B	CG	I
358	AG14	TXDATA306	TXDATA114	TXDATA114	TXDATA114	O
359	AG15	TXDATA302	TXDATA110	TXDATA110	TXDATA110	O
360	AG16	V_{DD}	←	←	←	

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
361	AG17	RXDATA101	RXDATA101	RXDATA101	RXDATA101	I
362	AG18	RXENB1_B	RXENB1_B	RXENB1A_B	RXENB1_B	O
363	AG19	RXADDR11	RXADDR11	RXADDR1A1	RXADDR11	O
364	AG20	GND	←	←	←	
365	AG21	GND	←	←	←	
366	AG22	TXDATA106	TXDATA106	TXDATA106	TXDATA106	O
367	AG23	GND	←	←	←	
368	AG24	GND	←	←	←	
369	AG25	CBD82	←	←	←	I/O
370	AG26	GND	←	←	←	
371	AG27	V_{DD}	←	←	←	
372	AF27	CBD72	←	←	←	I/O
373	AE27	CBD70	←	←	←	I/O
374	AD27	CBD65	←	←	←	I/O
375	AC27	GND	←	←	←	
376	AB27	V_{DD}	←	←	←	
377	AA27	CBD55	←	←	←	I/O
378	Y27	GND	←	←	←	
379	W27	CBD46	←	←	←	I/O
380	V27	CBCS0_B	←	←	←	O
381	U27	CBA16	←	←	←	O
382	T27	CBA12	←	←	←	O
383	R27	V_{DD}	←	←	←	
384	P27	CBA03	←	←	←	O
385	N27	GND	←	←	←	
386	M27	CBD38	←	←	←	I/O
387	L27	GND	←	←	←	
388	K27	GND	←	←	←	
389	J27	CBD28	←	←	←	I/O
390	H27	GND	←	←	←	
391	G27	CBD21	←	←	←	I/O
392	F27	CBD16	←	←	←	I/O
393	E27	V_{DD}	←	←	←	
394	D27	GND	←	←	←	
395	D26	CBD06	←	←	←	I/O
396	D25	GND	←	←	←	
397	D24	RXDATA006	RXDATA006	RXDATA006	RXDATA006	I
398	D23	V_{DD}	←	←	←	
399	D22	UCLK0	UCLK0	UCLK0	UCLK0	I
400	D21	CG	RXCLAV0[1]	CG	CG	I

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
401	D20	GND	←	←	←	
402	D19	TXADDR00	TXADDR00	TXADDR0A0	TXADDR00	O
403	D18	TXENB0_B	TXENB0_B	TXENB0A_B	TXENB0_B	O
404	D17	TXDATA004	TXDATA004	TXDATA004	TXDATA004	O
405	D16	RXDATA207	RXDATA015	RXDATA015	RXDATA015	I
406	D15	V_{DD}	←	←	←	
407	D14	UCLK2	CG	CG	CG	I
408	D13	RXADDR23	IC	RXADDR0B3	IC	O
409	D12	TXADDR21	IC	TXADDR0B1	IC	O
410	D11	GND	←	←	←	
411	D10	TXDATA206	TXDATA014	TXDATA014	TXDATA014	O
412	D09	TXDATA202	TXDATA010	TXDATA010	TXDATA010	O
413	D08	GND	←	←	←	
414	D07	INT	←	←	←	O
415	D06	CG	←	←	←	I
416	D05	AD31	←	←	←	I/O
417	E05	V_{DD}	←	←	←	
418	F05	V_{DD}	←	←	←	
419	G05	AD21	←	←	←	I/O
420	H05	V_{DD}	←	←	←	
421	J05	AD12	←	←	←	I/O
422	K05	V_{DD}	←	←	←	
423	L05	AD02	←	←	←	I/O
424	M05	V_{DD}	←	←	←	
425	N05	GND	←	←	←	
426	P05	V_{DD}	←	←	←	
427	R05	V_{DD}	←	←	←	
428	T05	HTCS1_B	←	←	←	O
429	U05	V_{DD}	←	←	←	
430	V05	HTD28	←	←	←	I/O
431	W05	V_{DD}	←	←	←	
432	Y05	HTD19	←	←	←	I/O
433	AA05	V_{DD}	←	←	←	
434	AB05	GND	←	←	←	
435	AC05	V_{DD}	←	←	←	
436	AD05	V_{DD}	←	←	←	
437	AE05	SWCLK	←	←	←	I
438	AF05	V_{DD}	←	←	←	
439	AF06	CBD88	←	←	←	I/O
440	AF07	GND	←	←	←	

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
441	AF08	V_{DD}	←	←	←	
442	AF09	RXDATA303	RXDATA111	RXDATA111	RXDATA111	I
443	AF10	V_{DD}	←	←	←	
444	AF11	GND	←	←	←	
445	AF12	V_{DD}	←	←	←	
446	AF13	V_{DD}	←	←	←	
447	AF14	V_{DD}	←	←	←	
448	AF15	V_{DD}	←	←	←	
449	AF16	RXDATA105	RXDATA105	RXDATA105	RXDATA105	I
450	AF17	V_{DD}	←	←	←	
451	AF18	RXSOC1	RXSOC1	RXSOC1	RXSOC1	I
452	AF19	V_{DD}	←	←	←	
453	AF20	V_{DD}	←	←	←	
454	AF21	V_{DD}	←	←	←	
455	AF22	V_{DD}	←	←	←	
456	AF23	V_{DD}	←	←	←	
457	AF24	CBD83	←	←	←	I/O
458	AF25	V_{DD}	←	←	←	
459	AF26	V_{DD}	←	←	←	
460	AE26	GND	←	←	←	
461	AD26	V_{DD}	←	←	←	
462	AC26	V_{DD}	←	←	←	
463	AB26	CBD60	←	←	←	I/O
464	AA26	V_{DD}	←	←	←	
465	Y26	CBD50	←	←	←	I/O
466	W26	V_{DD}	←	←	←	
467	V26	V_{DD}	←	←	←	
468	U26	V_{DD}	←	←	←	
469	T26	V_{DD}	←	←	←	
470	R26	CBA07	←	←	←	O
471	P26	V_{DD}	←	←	←	
472	N26	CBD43	←	←	←	I/O
473	M26	V_{DD}	←	←	←	
474	L26	CBD33	←	←	←	I/O
475	K26	V_{DD}	←	←	←	
476	J26	V_{DD}	←	←	←	
477	H26	V_{DD}	←	←	←	
478	G26	CBD17	←	←	←	I/O
479	F26	GND	←	←	←	
480	E26	V_{DD}	←	←	←	

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
481	E25	V_{DD}	←	←	←	
482	E24	V_{DD}	←	←	←	
483	E23	V_{DD}	←	←	←	
484	E22	RXDATA001	RXDATA001	RXDATA001	RXDATA001	I
485	E21	V_{DD}	←	←	←	
486	E20	RXADDR00	RXADDR00	RXADDR0A0	RXADDR00	O
487	E19	V_{DD}	←	←	←	
488	E18	V_{DD}	←	←	←	
489	E17	V_{DD}	←	←	←	
490	E16	V_{DD}	←	←	←	
491	E15	RXDATA202	RXDATA010	RXDATA010	RXDATA010	I
492	E14	V_{DD}	←	←	←	
493	E13	RXADDR22	IC	RXADDR0B2	IC	O
494	E12	V_{DD}	←	←	←	
495	E11	V_{DD}	←	←	←	
496	E10	V_{DD}	←	←	←	
497	E09	HCLK	←	←	←	I
498	E08	V_{DD}	←	←	←	
499	E07	V_{DD}	←	←	←	
500	E06	IC	←	←	←	
501	F06	GND	←	←	←	
502	G06	AD23	←	←	←	I/O
503	H06	GND	←	←	←	
504	J06	AD13	←	←	←	I/O
505	K06	GND	←	←	←	
506	L06	AD03	←	←	←	I/O
507	M06	GND	←	←	←	
508	N06	V_{DD}	←	←	←	
509	P06	GND	←	←	←	
510	R06	GND	←	←	←	
511	T06	GND	←	←	←	
512	U06	GND	←	←	←	
513	V06	HTD27	←	←	←	I/O
514	W06	GND	←	←	←	
515	Y06	HTD18	←	←	←	I/O
516	AA06	GND	←	←	←	
517	AB06	HTD09	←	←	←	I/O
518	AC06	GND	←	←	←	
519	AD06	V_{DD}	←	←	←	
520	AE06	GND	←	←	←	

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
521	AE07	V_{DD}	←	←	←	
522	AE08	GND	←	←	←	
523	AE09	RXDATA304	RXDATA112	RXDATA112	RXDATA112	I
524	AE10	GND	←	←	←	
525	AE11	RXADDR33	IC	RXADDR1B3	IC	O
526	AE12	GND	←	←	←	
527	AE13	GND	←	←	←	
528	AE14	GND	←	←	←	
529	AE15	GND	←	←	←	
530	AE16	GND	←	←	←	
531	AE17	GND	←	←	←	
532	AE18	CG	RXCLAV1[1]	CG	CG	I
533	AE19	GND	←	←	←	
534	AE20	CG	TXCLAV1[1]	CG	CG	I
535	AE21	GND	←	←	←	
536	AE22	TXDATA100	TXDATA100	TXDATA100	TXDATA100	O
537	AE23	GND	←	←	←	
538	AE24	CBD78	←	←	←	I/O
539	AE25	GND	←	←	←	
540	AD25	CBD71	←	←	←	I/O
541	AC25	GND	←	←	←	
542	AB25	CBD61	←	←	←	I/O
543	AA25	GND	←	←	←	
544	Y25	CBD51	←	←	←	I/O
545	W25	GND	←	←	←	
546	V25	GND	←	←	←	
547	U25	GND	←	←	←	
548	T25	GND	←	←	←	
549	R25	GND	←	←	←	
550	P25	GND	←	←	←	
551	N25	CBD42	←	←	←	I/O
552	M25	GND	←	←	←	
553	L25	CBD32	←	←	←	I/O
554	K25	GND	←	←	←	
555	J25	CBD22	←	←	←	I/O
556	H25	GND	←	←	←	
557	G25	CBD12	←	←	←	I/O
558	F25	GND	←	←	←	
559	F24	CBD04	←	←	←	I/O
560	F23	GND	←	←	←	

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Pin No.	Address	12-PHY Polling Mode/ 15-PHY Polling Mode	Multiplexed Status Polling Mode	2-Group Weighted Polling Mode	1-Group Weighted Polling Mode	I/O
561	F22	RXDATA002	RXDATA002	RXDATA002	RXDATA002	I
562	F21	GND	←	←	←	
563	F20	RXADDR01	RXADDR01	RXADDR0A1	RXADDR01	O
564	F19	GND	←	←	←	
565	F18	GND	←	←	←	
566	F17	GND	←	←	←	
567	F16	GND	←	←	←	
568	F15	RXDATA203	RXDATA011	RXDATA011	RXDATA011	I
569	F14	GND	←	←	←	
570	F13	V_{DD}	←	←	←	
571	F12	GND	←	←	←	
572	F11	TXDATA207	TXDATA015	TXDATA015	TXDATA015	O
573	F10	GND	←	←	←	
574	F09	MCS_B	←	←	←	I
575	F08	GND	←	←	←	
576	F07	GND	←	←	←	

2.3 Pin Functions

Although the μPD98412 is a device operating at 3.3 V, it can be directly connected to a PHY device, CPU, and memory with a 5-V TTL interface.

2.3.1 Power supply

Table 2-1. Power Supply

Pin Name	Pin No.	I/O	Function
V_{DD}	20, 25, 31, 35, 39, 43, 57, 61, 64, 67, 72, 78, 81, 86, 87, 89, 94, 96, 112, 119, 129, 147, 152, 160, 161, 169, 230, 232, 240, 243, 283, 290, 293, 308, 315, 324, 325, 329, 332, 337, 342, 353, 360, 371, 376, 383, 393, 398, 406, 417, 418, 420, 422, 424, 426, 427, 429, 431, 433, 435, 436, 438, 441, 443, 445 - 448, 450, 452 - 456, 458, 459, 461, 462, 464, 466 - 469, 471, 473, 475 - 477, 480 - 483, 485, 487 - 490, 492, 494 - 496, 498, 499, 508, 519, 521, 570	—	These pins supply a power of +3.3 V ± 5%.
GND	2, 6, 9, 14, 26, 32, 37, 58, 60, 84, 101, 110, 113, 143, 144, 156, 162, 173, 183, 196, 215, 233, 241, 244, 255, 256, 265, 280, 282, 291, 304, 305, 307, 313, 314, 323, 327, 330, 339, 341, 352, 364, 365, 367, 368, 370, 375, 378, 385, 387, 388, 390, 394, 396, 401, 410, 413, 425, 434, 440, 444, 460, 479, 501, 503, 505, 507, 509 - 512, 514, 516, 518, 520, 522, 524, 526 - 531, 533, 535, 537, 539, 541, 543, 545 - 550, 552, 554, 556, 558, 560, 562, 564 - 567, 569, 571, 573, 575, 576	—	These are ground pins.

2.3.2 UTOPIA interface

The μPD98412 employs a UTOPIA Level2 (cell level transfer) interface between PHY layer and ATM layer. Symbol, pim number, and function are varied depending on the polling mode.

(1) 8-bit 12-PHY polling mode/15-PHY polling mode

Table 2-2. Receive Interface Signals (1/2)

Symbol	Pin No.	I/O	Function
RXADDR03 - RXADDR00	205, 206, 563, 486	O	Multi-PHY select address of receive interface 0. RXADDR03 is the MSB.
RXDATA007 - RXDATA000	303, 397, 92, 202, 93, 561, 484, 203	I	Cell data input of receive interface 0. Cell data is input from a PHY layer device in 8-bit units. The μPD98412 reads the data at the rising edge of UCLK0. RXDATA007 is the MSB.
RXSOC0	306	I	Cell transfer start signal of receive interface 0. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB0_B	204	O	Transfer enable signal of receive interface 0. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXCLAV0	95	I	Cell transfer enable signal of receive interface 0. This pin inputs a signal indicating that one or more cells to be transferred from the PHY layer device to the μPD98412 exist.
UCLK0	399	I	UTOPIA clock input of receive interface 0. Data is transferred/received at the rising edge of this clock.
RXADDR13 - RXADDR10	266, 50, 363, 267	O	Multi-PHY select address of receive interface 1. RXADDR13 is the MSB.
RXDATA107 - RXDATA100	158, 263, 449, 46, 159, 264, 361, 47	I	Cell data input of receive interface 1. Cell data is input from a PHY layer device in 8-bit units. The μPD98412 reads the data at the rising edge of UCLK1. RXDATA107 is the MSB.
RXSOC1	451	I	Cell transfer start signal of receive interface 1. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB1_B	362	O	Transfer enable signal of receive interface 1. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXCLAV1	49	I	Cell transfer enable signal of receive interface 1. This pin inputs a signal indicating that one or more cells to be transferred from the PHY layer device to the μPD98412 exist.
UCLK1	48	I	UTOPIA clock input of receive interface 1. Data is transferred/received at the rising edge of this clock.

Table 2-2. Receive Interface Signals (2/2)

Symbol	Pin No.	I/O	Function
RXADDR23 - RXADDR20	408, 493, 107, 316	O	Multi-PHY select address of receive interface 2. RXADDR23 is the MSB.
RXDATA207 - RXDATA200	405, 312, 103, 212, 568, 491, 104, 213	I	Cell data input of receive interface 2. Cell data is input from a PHY layer device in 8-bit units. The μPD98412 reads the data at the rising edge of UCLK2. RXDATA207 is the MSB.
RXSOC2	214	I	Cell transfer start signal of receive interface 2. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB2_B	105	O	Transfer enable signal of receive interface 2. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXCLAV2	106	I	Cell transfer enable signal of receive interface 2. This pin inputs a signal indicating that one or more cells to be transferred from the PHY layer device to the μPD98412 exist.
UCLK2	407	I	UTOPIA clock input of receive interface 2. Data is transferred/received at the rising edge of this clock.
RXADDR33 - RXADDR30	525, 355, 258, 153	O	Multi-PHY select address of receive interface 3. RXADDR33 is the MSB.
RXDATA307 - RXDATA300	34, 148, 254, 523, 442, 149, 36, 150	I	Cell data input of receive interface 3. Cell data is input from a PHY layer device in 8-bit units. The μPD98412 reads the data at the rising edge of UCLK3. RXDATA307 is the MSB.
RXSOC3	257	I	Cell transfer start signal of receive interface 3. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB3_B	151	O	Transfer enable signal of receive interface 3. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXCLAV3	38	I	Cell transfer enable signal of receive interface 3. This pin inputs a signal indicating that one or more cells to be transferred from the PHY layer device to the μPD98412 exist.
UCLK3	354	I	UTOPIA clock input of receive interface 3. Data is transferred/received at the rising edge of this clock.

Table 2-3. Transmit Interface Signals (1/2)

Symbol	Pin No.	I/O	Function
TXADDR03 - TXADDR00	97, 207, 98, 402	O	Multi-PHY select address of transmit interface 0. TXADDR03 is the MSB.
TXDATA007 - TXDATA000	310, 209, 100, 404, 311, 210, 102, 211	O	Cell data output of transmit interface 0. Cell data is output to a PHY layer device in 8-bit units. The μPD98412 outputs the data at the rising edge of UCLK0. TXDATA007 is the MSB. (3-state buffer)
TXSOC0	99	O	Cell transfer start signal of transmit interface 0. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)
TXENB0_B	403	O	Transfer enable signal of transmit interface 0. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXCLAV0	208	I	Cell transfer enable signal of transmit interface 0. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed.
TXADDR13 - TXADDR10	163, 51, 268, 164	O	Multi-PHY select address of transmit interface 1. TXADDR13 is the MSB.
TXDATA107 - TXDATA100	53, 366, 270, 166, 54, 271, 167, 536	O	Cell data output of transmit interface 1. Cell data is output to a PHY layer device in 8-bit units. The μPD98412 outputs the data at the rising edge of UCLK1. TXDATA107 is the MSB. (3-state buffer)
TXSOC1	269	O	Cell transfer start signal of transmit interface 1. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)
TXENB1_B	165	O	Transfer enable signal of transmit interface 1. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXCLAV1	52	I	Cell transfer enable signal of transmit interface 1. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed.

Table 2-3. Transmit Interface Signals (2/2)

Symbol	Pin No.	I/O	Function
TXADDR23 - TXADDR20	216, 108, 409, 317	O	Multi-PHY select address of transmit interface 2. TXADDR23 is the MSB.
TXDATA207 - TXDATA200	572, 411, 319, 219, 111, 412, 320, 220	O	Cell data output of transmit interface 2. Cell data is output to a PHY layer device in 8-bit units. The μPD98412 outputs the data at the rising edge of UCLK2. TXDATA207 is the MSB. (3-state buffer)
TXSOC2	318	O	Cell transfer start signal of transmit interface 2. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)
TXENB2_B	218	O	Transfer enable signal of transmit interface 2. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXCLAV2	109	I	Cell transfer enable signal of transmit interface 2. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed.
TXADDR33 - TXADDR30	40, 356, 259, 154	O	Multi-PHY select address of transmit interface 3. TXADDR33 is the MSB.
TXDATA307 - TXDATA300	42, 358, 261, 44, 157, 359, 262, 45	O	Cell data output of transmit interface 3. Cell data is output to a PHY layer device in 8-bit units. The μPD98412 outputs the data at the rising edge. TXDATA307 is the MSB. (3-state buffer)
TXSOC3	260	O	Cell transfer start signal of transmit interface 3. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)
TXENB3_B	155	O	Transfer enable signal of transmit interface 3. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXCLAV3	357	I	Cell transfer enable signal of transmit interface 3. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed.

(2) 16-bit multiplexed status polling mode

Table 2-4. Receive Interface Signals (1/2)

Symbol	Pin No.	I/O	Function
RXADDR04 - RXADDR00	316, 205, 206, 563, 486	O	Multi-PHY select address of receive interface 0. RXADDR04 is the MSB.
RXDATA015 - RXDATA000	405, 312, 103, 212, 568, 491, 104, 213, 303, 397, 92, 202, 93, 561, 484, 203	I	Cell data input of receive interface 0. Cell data is input from a PHY layer device in 16-bit units. The μPD98412 reads the data at the rising edge of UCLK0. RXDATA015 is the MSB.
RXSOC0	306	I	Cell transfer start signal of receive interface 0. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB0_B	204	O	Transfer enable signal of receive interface 0. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXCLAV0[0] - RXCLAV0[3]	95, 400, 106, 214	I	Cell transfer enable signal of receive interface 0. This pin inputs a signal indicating that one or more cells to be transferred from the PHY layer device to the μPD98412 exist. Pins to be connected (RXCLAV0[0]-[3]) differ depending on PHY address of the connected PHY device. For details, refer to **3.7 Multiplexed Status Polling Mode**.
UCLK0	399	I	UTOPIA clock input of receive interface 0. Data is transferred/received at the rising edge of this clock.

Table 2-4. Receive Interface Signals (2/2)

Symbol	Pin No.	I/O	Function
RXADDR14 - RXADDR10	153, 266, 50, 363, 267	O	Multi-PHY select address of receive interface 1. RXADDR14 is the MSB.
RXDATA115 - RXDATA100	34, 148, 254, 523, 442, 149, 36, 150, 158, 263, 449, 46, 159, 264, 361, 47	I	Cell data input of receive interface 1. Cell data is input from a PHY layer device in 16-bit units. The μPD98412 reads the data at the rising edge of UCLK1. RXDATA115 is the MSB.
RXSOC1	451	I	Cell transfer start signal of receive interface 1. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB1_B	362	O	Transfer enable signal of receive interface 1. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXCLAV1[0] - RXCLAV1[3]	49, 532, 38, 257	I	Cell transfer enable signal of receive interface 1. This pin inputs a signal indicating that one or more cells to be transferred from the PHY layer device to the μPD98412 exist. Pins to be connected (RXCLAV1[0]-[3]) differ depending on PHY address of the connected PHY device. For details, refer to **3.7 Multiplexed Status Polling Mode**.
UCLK1	48	I	UTOPIA clock input of receive interface 1. Data is transferred/received at the rising edge of this clock.

Table 2-5. Transmit Interface Signals

Symbol	Pin No.	I/O	Function
TXADDR04 - TXADDR00	317, 97, 207, 98, 402	O	Multi-PHY select address of transmit interface 0. TXADDR04 is the MSB.
TXDATA015 - TXDATA000	572, 411, 319, 219, 111, 412, 320, 220, 310, 209, 100, 404, 311, 210, 102, 211	O	Cell data output of transmit interface 0. Cell data is output to a PHY layer device in 16-bit units. The μPD98412 outputs the data at the rising edge of UCLK0. TXDATA015 is the MSB. (3-state buffer)
TXSOC0	99	O	Cell transfer start signal of transmit interface 0. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)
TXENB0_B	403	O	Transfer enable signal of transmit interface 0. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXCLAV0[0] - TXCLAV0[3]	208, 309, 109, 217	I	Cell transfer enable signal of transmit interface 0. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed. Pins to be connected (TXCLAV0[0]-[3]) differ depending on PHY address of the connected PHY device. For details, refer to **3.7 Multiplexed Status Polling Mode**.
TXADDR14 - TXADDR10	154, 163, 51, 268, 164	O	Multi-PHY select address of transmit interface 1. TXADDR14 is the MSB.
TXDATA115 - TXDATA100	42, 358, 261, 44, 157, 359, 262, 45, 53, 366, 270, 166, 54, 271, 167, 536	O	Cell data output of transmit interface 1. Cell data is output to a PHY layer device in 16-bit units. The μPD98412 outputs the data at the rising edge of UCLK1. TXDATA115 is the MSB. (3-state buffer)
TXSOC1	269	O	Cell transfer start signal of transmit interface 1. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)
TXENB1_B	165	O	Transfer enable signal of transmit interface 1. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXCLAV1[0] - TXCLAV1[3]	52, 534, 357, 41	I	Cell transfer enable signal of transmit interface 1. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed. Pins to be connected (TXCLAV1[0]-[3]) differ depending on PHY address of the connected PHY device. For details, refer to **3.7 Multiplexed Status Polling Mode**.

(3) 16-bit 2-group weighted polling mode

Table 2-6. Receive Interface Signals (1/2)

Symbol	Pin No.	I/O	Function
RXADDR0A3 - RXADDR0A0	205, 206, 563, 486	O	Multi-PHY select address of receive interface 0, group A. RXADDR0A3 is the MSB.
RXADDR0B3 - RXADDR0B0	408, 493, 107, 316	O	Multi-PHY select address of receive interface 0, group B. RXADDR0B3 is the MSB.
RXENB0A_B	204	O	Transfer enable signal of receive interface 0, group A. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXENB0B_B	105	O	Transfer enable signal of receive interface 0, group B. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXCLAV0A	95	I	Cell transfer enable signal of receive interface 0, group A. This pin inputs a signal indicating that one or more cells to be transferred from the PHY layer device to the μPD98412 exist.
RXCLAV0B	106	I	Cell transfer enable signal of receive interface 0, group B. This pin inputs a signal indicating that one or more cells to be transferred from the PHY layer device to the μPD98412 exist.
RXDATA015 - RXDATA000	405, 312, 103, 212, 568, 491, 104, 213, 303, 397, 92, 202, 93, 561, 484, 203	I	Cell data input of receive interface 0. Cell data is input from a PHY layer device in 16-bit units. The μPD98412 reads the data at the rising edge of UCLK0. RXDATA015 is the MSB.
RXSOC0	306	I	Cell transfer start signal of receive interface 0. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
UCLK0	399	I	UTOPIA clock input of receive interface 0. Data is transferred/received at the rising edge of this clock.

Table 2-6. Receive Interface Signals (2/2)

Symbol	Pin No.	I/O	Function
RXADDR1A3 - RXADDR1A0	266, 50, 363, 267	O	Multi-PHY select address of receive interface 1, group A. RXADDR1A3 is the MSB.
RXADDR1B3 - RXADDR1B0	525, 355, 258, 153	O	Multi-PHY select address of receive interface 1, group B. RXADDR1B3 is the MSB.
RXENB1A_B	362	O	Transfer enable signal of receive interface 1, group A. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXENB1B_B	151	O	Transfer enable signal of receive interface 1, group B. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXCLAV1A	49	I	Cell transfer enable signal of receive interface 1, group A. This pin inputs a signal indicating that one or more cells to be transferred from the PHY layer device to the μPD98412 exist.
RXCLAV1B	38	I	Cell transfer enable signal of receive interface 1, group B. This pin inputs a signal indicating that one or more cells to be transferred from the PHY layer device to the μPD98412 exist.
RXDATA115 - RXDATA100	34, 148, 254, 523, 442, 149, 36, 150, 158, 263, 449, 46, 159, 264, 361, 47	I	Cell data input of receive interface 1. Cell data is input from a PHY layer device in 16-bit units. The μPD98412 reads the data at the rising edge of UCLK1. RXDATA115 is the MSB.
RXSOC1	451	I	Cell transfer start signal of receive interface 1. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
UCLK1	48	I	UTOPIA clock input of receive interface 1. Data is transferred/received at the rising edge of this clock.

Table 2-7. Transmit Interface Signals (1/2)

Symbol	Pin No.	I/O	Function
TXADDR0A3 - TXADDR0A0	97, 207, 98, 402	O	Multi-PHY select address of transmit interface 0, group A. TXADDR0A3 is the MSB.
TXADDR0B3 - TXADDR0B0	216, 108, 409, 317	O	Multi-PHY select address of transmit interface 0, group B. TXADDR0B3 is the MSB.
TXENB0A_B	403	O	Transfer enable signal of transmit interface 0, group A. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXENB0B_B	218	O	Transfer enable signal of transmit interface 0, group B. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXCLAV0A	208	I	Cell transfer enable signal of transmit interface 0, group A. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed.
TXCLAV0B	109	I	Cell transfer enable signal of transmit interface 0, group B. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed.
TXDATA015 - TXDATA000	572, 411, 319, 219, 111, 412, 320, 220, 310, 209, 100, 404, 311, 210, 102, 211	O	Cell data output of transmit interface 0. Cell data is output to a PHY layer device in 16-bit units. The μPD98412 outputs the data at the rising edge of UCLK0. TXDATA015 is the MSB. (3-state buffer)
TXSOC0	99	O	Cell transfer start signal of transmit interface 0. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)

Table 2-7. Transmit Interface Signals (2/2)

Symbol	Pin No.	I/O	Function
TXADDR1A3 - TXADDR1A0	163, 51, 268, 164	O	Multi-PHY select address of transmit interface 1, group A. TXADDR1A3 is the MSB.
TXADDR1B3 - TXADDR1B0	40, 356, 259, 154	O	Multi-PHY select address of transmit interface 1, group B. TXADDR1B3 is the MSB.
TXENB1A_B	165	O	Transfer enable signal of transmit interface 1, group A. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXENB1B_B	155	O	Transfer enable signal of transmit interface 1, group B. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXCLAV1A	52	I	Cell transfer enable signal of transmit interface 1, group A. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed.
TXCLAV1B	357	I	Cell transfer enable signal of transmit interface 1, group B. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed.
TXDATA115 - TXDATA100	42, 358, 261, 44, 157, 359, 262, 45, 53, 366, 270, 166, 54, 271, 167, 536	O	Cell data output of transmit interface 1. Cell data is output to a PHY layer device in 16-bit units. The μPD98412 outputs the data at the rising edge of UCLK1. TXDATA115 is the MSB. (3-state buffer)
TXSOC1A	269	O	Cell transfer start signal of transmit interface 1. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)

(4) 16-bit 1-group weighted polling mode

Table 2-8. Receive Interface Signals (1/2)

Symbol	Pin No.	I/O	Function
RXADDR04 - RXADDR00	316, 205, 206, 563, 486	O	Multi-PHY select address of receive interface 0. RXADDR04 is the MSB.
RXDATA015 - RXDATA000	405, 312, 103, 212, 568, 491, 104, 213, 303, 397, 92, 202, 93, 561, 484, 203	I	Cell data input of receive interface 0. Cell data is input from a PHY layer device in 16-bit units. The μPD98412 reads the data at the rising edge of UCLK0. RXDATA015 is the MSB.
RXSOC0	306	I	Cell transfer start signal of receive interface 0. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB0_B	204	O	Transfer enable signal of receive interface 0. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXCLAV0	95	I	Cell transfer enable signal of receive interface 0. This pin inputs a signal indicating that one or more cells to be transferred from the PHY layer device to the μPD98412 exist.
UCLK0	399	I	UTOPIA clock input of receive interface 0. Data is transferred/received at the rising edge of this clock.

Table 2-8. Receive Interface Signals (2/2)

Symbol	Pin No.	I/O	Function
RXADDR14 - RXADDR10	153, 266, 50, 363, 267	O	Multi-PHY select address of receive interface 1. RXADDR14 is the MSB.
RXDATA115 - RXDATA100	34, 148, 254, 523, 442, 149, 36, 150, 158, 263, 449, 46, 159, 264, 361, 47	I	Cell data input of receive interface 1. Cell data is input from a PHY layer device in 16-bit units. The μPD98412 reads the data at the rising edge of UCLK1. RXDATA115 is the MSB.
RXSOC1	451	I	Cell transfer start signal of receive interface 1. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB1_B	362	O	Transfer enable signal of receive interface 1. This signal informs a PHY layer device that the μPD98412 is ready for reception in the next clock cycle.
RXCLAV1	49	I	Cell transfer enable signal of receive interface 1. This pin inputs a signal indicating that one or more cells to be transferred from the PHY layer device to the μPD98412 exist.
UCLK1	48	I	UTOPIA clock input of receive interface 1. Data is transferred/received at the rising edge of this clock.

Table 2-9. Transmit Interface Signals

Symbol	Pin No.	I/O	Function
TXADDR04 - TXADDR00	317, 97, 207, 98, 402	O	Multi-PHY select address of transmit interface 0. TXADDR04 is the MSB.
TXDATA015 - TXDATA000	572, 411, 319, 219, 111, 412, 320, 220, 310, 209, 100, 404, 311, 210, 102, 211	O	Cell data output of transmit interface 0. Cell data is output to a PHY layer device in 16-bit units. The μPD98412 outputs the data at the rising edge of UCLK0. TXDATA015 is the MSB. (3-state buffer)
TXSOC0	99	O	Cell transfer start signal of transmit interface 0. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)
TXENB0_B	403	O	Transfer enable signal of transmit interface 0. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXCLAV0	208	I	Cell transfer enable signal of transmit interface 0. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed.
TXADDR14 - TXADDR10	154, 163, 51, 268, 164	O	Multi-PHY select address of transmit interface 1. TXADDR14 is the MSB.
TXDATA115 - TXDATA100	42, 358, 261, 44, 157, 359, 262, 45, 53, 366, 270, 166, 54, 271, 167, 536	O	Cell data output of transmit interface 1. Cell data is output to a PHY layer device in 16-bit units. The μPD98412 outputs the data at the rising edge of UCLK1. TXDATA115 is the MSB. (3-state buffer)
TXSOC1	269	O	Cell transfer start signal of transmit interface 1. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)
TXENB1_B	165	O	Transfer enable signal of transmit interface 1. This signal informs a PHY layer device that the μPD98412 outputs data in the current clock cycle.
TXCLAV1	52	I	Cell transfer enable signal of transmit interface 1. This pin inputs a signal that indicates that the μPD98412 is ready to receive the next cell after transfer of the current cell is completed.

2.3.3 Memory interface signals

The μPD98412 has two types of memory interfaces. One of them is used to store a cell header translation table and an address pointer to the cell buffer to the HTT & control memory, and the other is used to store cell data to the cell buffer memory. Table 2-10 shows the interface signals of the HTT & control memory. Table 2-11 shows the interface signals of the cell buffer memory.

Table 2-10. HTT & Control Memory Interface Signals

Symbol	Pin No.	I/O	Function
HTA17 - HTA00	11, 333, 234, 127, 12, 334, 235, 128, 13, 335, 236, 15, 130, 336, 237, 16, 131, 238	O	Address output
HTD31 - HTD00	18, 133, 19, 430, 513, 134, 135, 21, 242, 136, 22, 137, 432, 515, 23, 138, 343, 245, 139, 344, 246, 140, 517, 345, 141, 27, 28, 346, 248, 142, 29, 249	I/O	Data I/O bus (32-bit/word units) (w/pull-down resistor)
HTP3 - HTP0	338, 340, 24, 247	I/O	Parity I/O (w/pull-down resistor)
HTCS1_B, HTCS0_B	428, 17	O	Chip select signal
HTWE_B	132	O	Write enable signal
HTOE_B	239	O	Output enable signal

Table 2-11. Cell Buffer Memory Interface Signals

Symbol	Pin No.	I/O	Function
CBA17 - CBA00	71, 381, 286, 73, 184, 382, 287, 74, 185, 288, 470, 75, 186, 289, 384, 76, 187, 77	O	Address output
CBD91 - CBD00	145, 251, 349, 439, 55, 272, 168, 56, 457, 369, 273, 170, 274, 538, 59, 171, 275, 172, 276, 372, 540, 373, 277, 62, 174, 278, 374, 63, 175, 279, 542, 463, 176, 65, 177, 281, 377, 66, 178, 179, 544, 465, 68, 180, 69, 379, 284, 181, 472, 551, 188, 189, 79, 386, 292, 190, 80, 191, 474, 553, 294, 192, 82, 389, 295, 193, 83, 296, 194, 555, 391, 297, 195, 85, 478, 392, 298, 197, 299, 557, 88, 198, 300, 199, 301, 395, 90, 559, 302, 200, 91, 201	I/O	Data input/output bus (92-bit/word units) (w/pull-down resistor)
CBCS1_B, CBCS0_B	70, 380	O	Chip select signal
CBWE_B	285	O	Write enable signal
CBOE_B	182	O	Output enable signal

2.3.4 Microprocessor interface signals

The μPD98412 supports a 32-bit address/data multiplexed synchronous bus type microprocessor interface.

Table 2-12. Microprocessor Interface Signals

Symbol	Pin No.	I/O	Function
IOCS_B	221	I	I/O chip select signal
MCS_B	574	I	Memory chip select signal
INT	414	O	Interrupt request signal
HCLK	497	I	Microprocessor bus clock (8 to 33 MHz)
AD31 - AD0	416, 1, 117, 225, 118, 226, 326, 3, 502, 227, 419, 4, 120, 228, 328, 5, 121, 229, 504, 421, 122, 7, 123, 231, 331, 8, 124, 125, 506, 423, 10, 126	I/O	Address/data bus
R/W_B	114	I	Read/write select signal
UWE_B	115	I	High-order word enable signal
RDY_B	322	O	Ready signal (3-state buffer)

2.3.5 JTAG

Table 2-13. JTAG Interface Signals

Symbol	Pin No.	I/O	Function
JDI	252	I	JTAG serial data input
JDO	146	O	JTAG serial data output (normally open) (3-state buffer)
JCK	33	I	JTAG serial clock input
JMS	253	I	JTAG mode select signal
JRST_B	351	I	JTAG reset signal

2.3.6 Others

Table 2-14. Other Interface Signals

Symbol	Pin No.	I/O	Function
SWCLK	437	I	System clock input (8 to 40 MHz)
RESET_B	347	I	Hardware reset signal (Schmitt input buffer)
CG	116, 222, 223, 321, 415	I	Always connect to GND.
PU	30	I	Always pull up to V_{DD}.
IC	224, 250, 348, 350, 500	O	Internally connected (always open).

2.4 Recommended Connections of Unused Pins

Table 2-15. Recommended Connections of Unused Pins

Pin Name	I/O	Recommended Connections
RXDATA***	I	Connect to GND.
RXSOC*	I	Connect to GND.
RXCLAV*	I	Connect to GND.
UCLK*	I	Connect to GND.
TXCLAV*	I	Connect to GND.
HTD31 - HTD00	I/O (w/pull-down resistor)	Open.
HTP3 - HTP0	I/O (w/pull-down resistor)	Open.
CBD91 - CBD00	I/O (w/pull-down resistor)	Open.
IOCS_B	I	Pull up to V_{DD}.
MCS_B	I	Pull up to V_{DD}.
AD31 - AD00	I/O	Pull up to V_{DD}.
R/W_B	I	Pull up to V_{DD}.
UWE_B	I	Pull up to V_{DD}.
JDI	I	Connect to GND.
JCK	I	Connect to GND.
JMS	I	Connect to GND.
JRST_B	I	Connect to GND.
All output pins	O	Open.

2.5 Pin Status at Reset

Table 2-16. Pin Status at Reset

Pin Name	I/O	Pin Status at Reset
RXADDR*	O	High level
RXENB*_B	O	High level
TXADDR*	O	High level
TXDATA***	O (3-state buffer)	Hi-Z
TXSOC*	O (3-state buffer)	Hi-Z
TXENB*_B	O	High level
HTA17 - HTA00	O	Low level
HTCS1_B, HTCS0_B	O	High level
HTWE_B	O	High level
HTOE_B	O	High level
HTP3 - HTP0	I/O (w/pull-down resistor)	Low level
HTD31 - HTD00	I/O (w/pull-down resistor)	Low level
CBD91 - CBD00	I/O (w/pull-down resistor)	Low level
CBA17 - CBA00	O	Low level
CBOE_B	O	High level
CBWE_B	O	High level
CBCS1_B, CBCS0_B	O	High level
INT	O	Low level
RDY_B	O (3-state buffer)	Hi-Z
AD31 - AD00	I/O	Hi-Z
JDO	O (3-state buffer)	Hi-Z

[MEMO]

CHAPTER 3 FUNCTIONAL OUTLINE

The μPD98412 is a shared-buffer non-blocking ATM switch which has a header translation function. Its circuit interfaces conform to UTOPIA Level2 and can connect up to 24 circuits of different rates by connecting multiple PHY devices. A header translation table is stored in external SRAM. By referencing this table, the μPD98412 can simultaneously translate headers of up to 64K connections (at the full memory capacity) during switching. The external SRAM is also used as a shared buffer to which up to 51.2K cells (at full memory capacity) can be stored.

The μPD98412 also controls transfer quality by using EPD (Early Packet Discard), PPD (Partial Packet Discard), priority cell discard control, and ABR (Available Bit Rate) traffic control features.

3.1 UTOPIA Interface

The μPD98412 employs UTOPIA interfaces conforming to UTOPIA Level2. Thes interfaces support single ATM-mutli-PHY, 8-bit data width (8-bit UTOPIA interface) and 16-bit data width (16-bit UTOPIA interface). Both the interfaces support cell-level handshaking, and do not support octet-level handshaking.

These 8-bit and 16-bit UTOIPA interfaces operate in the following modes:

8-bit UTOPIA interface

- 12-PHY polling mode (μPD98410-compatible mode. Up to 12 PHY devices can be connected.)
- 15-PHY polling mode (Up to 15 PHY devices can be connected.)

16-bit UTOPIA interface

- Multiplexed status polling mode (Up to 30 PHY devices can be connected.)
- 2-group weighted polling mode (Up to 30 PHY devices can be connected.)
- 1-group weighted polling mode (Up to 30 PHY devices can be connected.)

The μPD98412 constitutes the 16-bit UTOPIA interface by using two 8-bit UTOPIA interfaces. In addition, 8-bit UTOPIA interfaces and a 16-bit UTOPIA interface can be used together. Therefore, these interfaces can be used in the following combinations:

- Four 8-bit UTOPIA interfaces
- Two 8-bit UTOPIA interfaces and one 16-bit UTOPIA interface
- Two 16-bit UTOPIA interfaces

Ports 0 and 2 of the 8-bit UTOPIA interfaces are used for 16-bit UTOPIA interface port 0. Ports 1 and 3 of the 8-bit UTOPIA interfaces are used for 16-bit UTOPIA interface port 1.

3.1.1 Setting polling modes

The polling modes are set by using UTOPIA configuration registers (UTPCFG0 through 3). The correspondence between each UTOPIA configuration register and each UTOPIA port is as shown below.

Setting Register	When 8-Bit UTOPIA I/F Is Used	When 16-Bit UTOPIA I/F Is Used
UTPCFG0	UTOPIA8#0	UTOPIA16#0
UTPCFG1	UTOPIA8#1	UTOPIA16#1
UTPCFG2	UTOPIA8#2	Not used
UTPCFG3	UTOPIA8#3	Not used

The BW bit of the UTPCFG0 and UTPCFG1 registers is used to select the 8-bit UTOPIA interfaces or 16-bit UTOPIA interfaces.

The NPC0 through 2 fields of the UTPCFG0 through 3 registers are used to set a polling class which is the priority class of polling and selection. A polling class is selected if two or more PHY devices each having a different speed are connected to one UTOPIA interface. How the priority of polling and selection is controlled differs depending on the polling mode.

The μPD98412 is set in the 12-PHY polling mode of the 8-bit UTOPIA interfaces upon power application and immediately after reset.

3.1.2 Condition of clock frequency

Set the UTOPIA clock frequency and system clock frequency of the μPD98412, observing the following relation:

In 12-PHY polling mode of 8-bit UTOPIA I/F

System clock frequency $\geq 33/40 \times$ UTOPIA clock frequency

In other polling modes

System clock frequency $\geq 33/50 \times$ UTOPIA clock frequency

3.1.3 Effective throughput of UTOPIA interface

With the μPD98412, the effective throughput per UTOPIA interface is defined as follows:

Effective throughput per UTOPIA interface =
min (Maximum transfer rate per UTOPIA I/F, Internal processing speed per UTOPIA I/F)

The maximum transfer rates of the 8-bit UTOPIA interface and the 16-bit UTOPIA interface are calculated as follows:

- 8-bit UTOPIA interface
  - Rx side
    1) When the UH bit of the UTPCFGn register is “0” (X10-like handshake mode)
       12-PHY/15-PHY polling mode
       Maximum transfer rate per UTOPIA [Mbps] = UTOPIA clock [MHz] × 8 [bits] × 53/54
    2) When the UH bit of the UTPCFGn register is “1” (X15 handshake mode)
       15-PHY polling mode
       Maximum transfer rate per UTOPIA [Mbps] = UTOPIA clock [MHz] × 8 [bits] × 53/56
  - Tx side
    Maximum transfer rate per UTOPIA [Mbps] = UTOPIA clock [MHz] × 8 [bits] × 53/54

- 16-bit UTOPIA interface
  - Rx side
    1) When the UH bit of the UTPCFGn register is “0” (X10-like handshake mode)
       Maximum transfer rate per UTOPIA [Mbps] = UTOPIA clock [MHz] × 8 [bits] × 53/28
    2) When the UH bit of the UTPCFGn register is “1” (X15 handshake mode)
       Maximum transfer rate per UTOPIA [Mbps] = UTOPIA clock [MHz] × 8 [bits] × 53/30
  - Tx side
    Maximum transfer rate per UTOPIA [Mbps] = UTOPIA clock [MHz] × 8 [bits] × 53/28

The internal processing speed of the 8-bit UTOPIA interface and 16-bit UTOPIA interface per UTOPIA is calculated as follows:

- 8-bit UTOPIA interface
  Internal processing speed per UTOPIA [Mbps] = system clock [MHz] × 8 [bits] × 53/44
- 16-bit UTOPIA interface
  Internal processing speed per UTOPIA [Mbps] = system clock [MHz] × 8 [bits] × 53/22

Make sure that the total throughput of the PHY devices connected to one UTOPIA interface of the μPD98412 is less than the effective throughput per UTOPIA interface.

3.2 Outline of Polling

Cells are input to the μPD98412 in the following sequence:

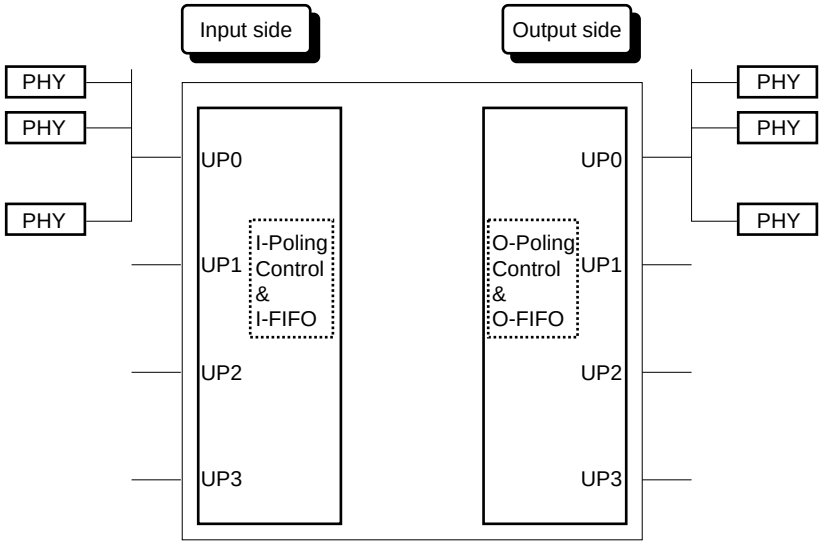
<1> The μPD98412 inquires whether a PHY device has a cell (polling).
<2> If the device has a cell, the μPD98412 inputs the cell. If not, the μPD98412 makes an inquiry to the next PHY device of those that are mapped to the logical port by the port configuration register.

Cells are output from the output queue in the following sequence:

<1> The μPD98412 inquires whether each PHY device is ready to transmit a cell (polling).
<2> Based on output rate control (shaping), cell stop information, and the result of polling in <1>, the μPD98412 determines from which output port to output a cell.
<3> Of the output queues corresponding to the logical output port determined, the μPD98412 determines the service class of the queue used to output the cell (WFQ (Weighted Fairness Queue)).

The way in which polling is used to input or output cells is explained below.
Figure 3-1 shows the related functional blocks of the μPD98412.

Figure 3-1. Functional Blocks of μPD98412



- UP0-UP3 : UTOPIA interface ports
- I/O-Polling Control : Polling control block for input and output sides
- I/O-FIFO : Input or output FIFO. A FIFO exists for each UTOPIA port and corresponds to UP0 to UP3.

Basically, cells are input or output as follows:

(Input)

- The polling control block inquires whether each PHY device is ready to transmit a cell, and determines the logical input port that inputs the cell.
- The cell is input to the I-FIFO.

(Output)

- The polling control block inquires whether each PHY device is ready to receive a cell.
- The output cell is determined based on the result of polling, shaping, and WFQ, and is stored to the O-FIFO.
- The cell is transmitted to the corresponding logical output port.

Up to 12, 15, or 30 PHY devices can be connected to one UTOPIA port, depending on the polling mode.

For the details of polling modes at the input and output sides, refer to **3.5 12-PHY Polling Mode** to **3.9 1-group weighted polling mode**.

3.3 Input Port Handshake Mode

The μPD98412 has two handshake modes for the input UTOPIA interface: X10-like handshake mode and X15 handshake mode.

3.3.1 X10-like handshake mode

The input UTOPIA interface of the μPD98412 is set in the X10-like handshake mode when the UH bit of the UTOPIA configuration register (UTPCFGn) is cleared to “0”.

When the 12-PHY polling mode is set in this X10-like handshake mode, the μPD98412 performs the same handshake operation as the μPD98410 (therefore, this mode is a μPD98410-compatible mode).

3.3.2 X15 handshake mode

The input UTOPIA interface of the μPD98412 is set in the X15 handshake mode when the UH bit of the UTPCFGn register is set to “1”.

The differences between this mode and the X10-like handshake mode are as follows:

(1) Interval between transferring continuous cells (interval between output of the end of cell - payload 48 - to output of the beginning of the next cell - header 1)

- It takes at least one clock in the X10-like handshake mode.
- It takes at least three clocks in the X15 handshake mode.

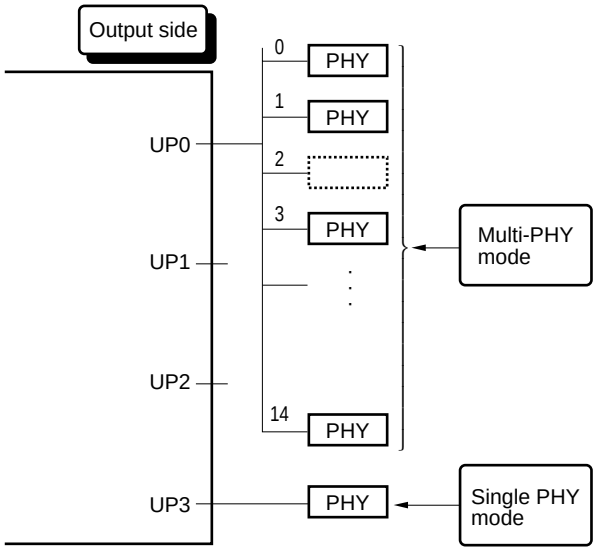
(2) Polling PHY device inputting cell

- In the X10-like handshake mode, the PHY device that is inputting a cell is not polled. If the PHY device that is to input the next cell is not determined until the clock indicating the end of a cell (payload 48 with 8-bit UTOPIA interface or payloads 47 and 48 with 16-bit UTOPIA interface) is input, the PHY device that has been inputting cells is granted the permission to input.
- In the X15 handshake mode, the PHY device that is inputting a cell is polled at the end of the cell (payload 48 with 8-bit UTOPIA interface or payloads 47 and 48 with 16-bit UTOPIA interface).

3.4 Single PHY Mode and Multi-PHY Mode

Depending on how the PHY device(s) on the output UTOPIA port side is connected, the multi-PHY mode or single PHY mode is used.

Figure 3-2. Single PHY Mode and Multi-PHY Mode



Each mode is explained below.

<1> Multi-PHY mode

In this mode, two or more PHY devices can be connected to one UTOPIA output port. Even if only one PHY device is connected, the operation in this mode is different from that in the single PHY mode.

<2> Single PHY mode

In this mode, one PHY device is connected to one UTOPIA output port.

The single PHY connection mode can be used for both the 8-bit UTOPIA interface and 16-bit UTOPIA interface. When this mode is set, the μPD98412 polls the PHY device to which a cell is transferred, when P45 (payload 45) is transferred in the case of the 8-bit UTOPIA interface or when P41 and P42 are transferred in the case of the 16-bit UTOPIA Interface, to determine whether the device is ready to receive the next cell. The other PHY devices are not polled.

Either multi-PHY mode or single PHY mode can be specified for each logical output port by using the SG bit of the port configuration (PTn) register. In the single PHY mode, one PHY device is connected to one UTOPIA output port. If two or more PHY devices are connected, the lowest logical output port number is selected.

If one UTOPIA output port is set in both the multi-PHY mode and single PHY mode, the single PHY mode takes precedence.

Cautions 1. If the setting of the SG bit of the port configuration register is changed while the μPD98412 is operating, two cells may be output to an illegal PHY device, or cell loss may occur because the result of polling does not match immediately before and after the mode is changed between single PHY and multi-PHY mode. After that, however, transmission is performed normally.

2. If mapping to the logical output port is changed by changing the setting of PHY, UPN, and EN of the port configuration register while the μPD98412 is operating, two cells may be output to an illegal PHY device, or cell loss may occur because the result of polling does not match immediately before and after the mode is changed between single PHY and multi-PHY mode. After that, however, transmission is performed normally.

3.5 12-PHY Polling Mode

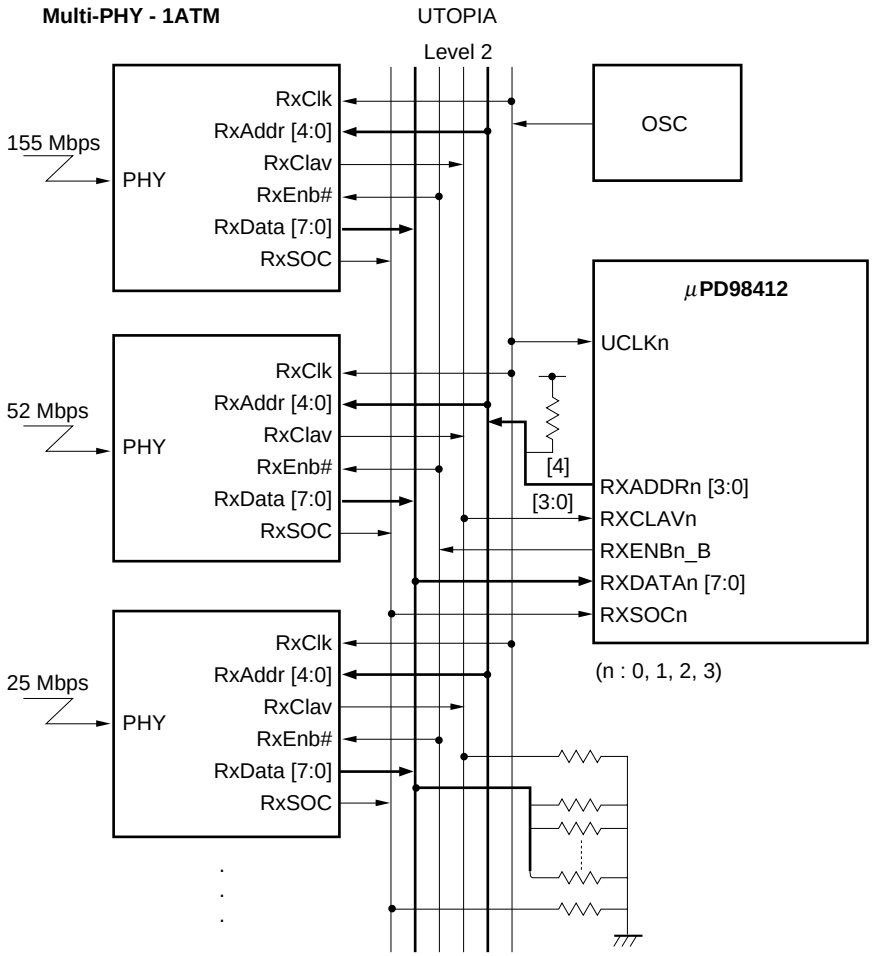
The 12-PHY polling mode can be used for the 8-bit UTOPIA interface and supports up to 12 PHY devices by means of multiple PHY connection. This mode is a μPD98410-compatible mode.

3.5.1 Input port interface

An input port is mapped to a logical input port number based on the PHY address and UTOPIA interface number, in accordance with the contents of the port configuration (PTn) register. The μPD98412 performs its internal processing by using this logical input port number.

Figure 3-3 shows an example of connecting multiple PHY devices to one UTOPIA interface.

Figure 3-3. Example of Connecting UTOPIA Receive Interface

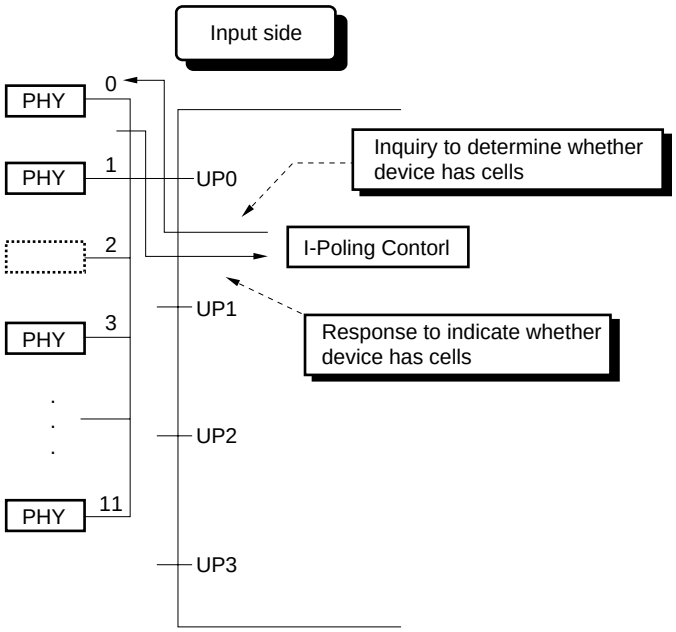


Remark Of the 5 bits of a PHY address, the low-order 4 bits are connected to the μPD98412. Pull up the highest bit. The μPD98412 outputs a PHY address of "0" through "11" for the purpose of polling.
The μPD98412 does not have an RxClk output. Supply UCLKn to the μPD98412 as a UTOPIA clock.

3.5.2 Input port cell transfer timing

(1) Basic operation

Figure 3-4. Basic Operation of Polling during Cell Input

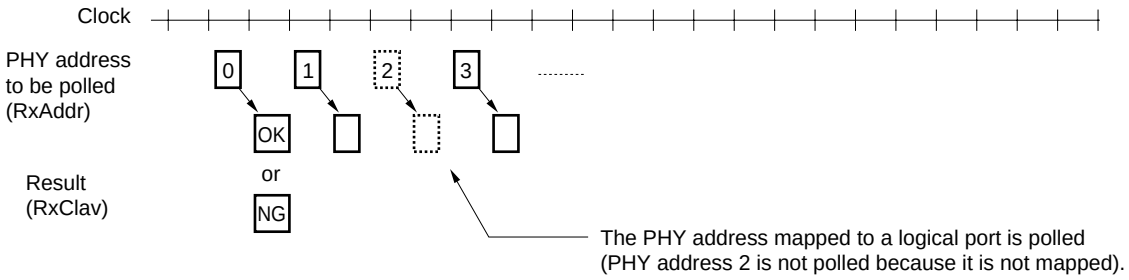


Cells are input to the μPD98412 in the following sequence:

<1> The μPD98412 inquires whether a PHY device has cells.
<2> The PHY device returns a response to indicate whether the device has cells.

This sequence is performed for a PHY device mapped to a logical port by PHY, UPN, and EN of the port configuration register. Figure 3-5 shows the relationship between the clock and polling control at this time. Polling control at the input side has no relationship with the basic operation cycle (= 54 UTOPIA clocks) units.

Figure 3-5. Relationship between Polling Control and Basic Operation Cycle (during Cell Input)

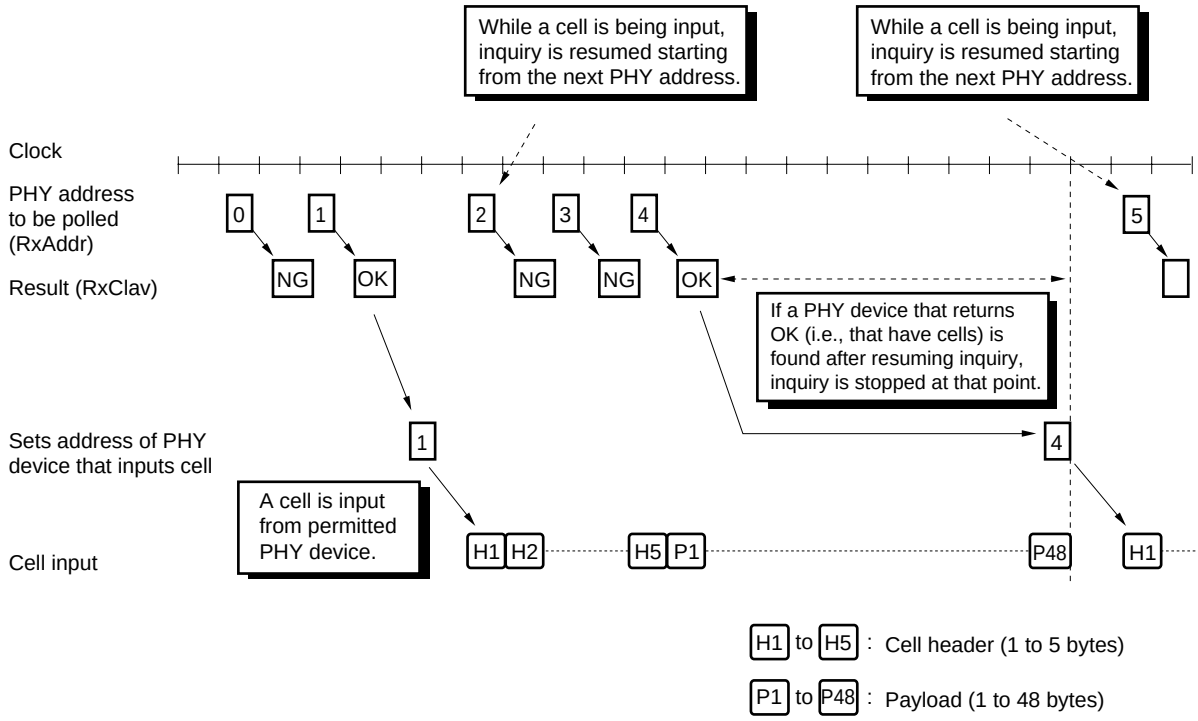


Caution Never map a PHY device that is not connected to a logical port. Otherwise, the input side polls a PHY device that does not exist, resulting in a hang up of the corresponding UTOPIA receive interface port.

(2) Cell input timing

If the result of polling is okay (i.e., if the device has cells), the cells are input as follows:

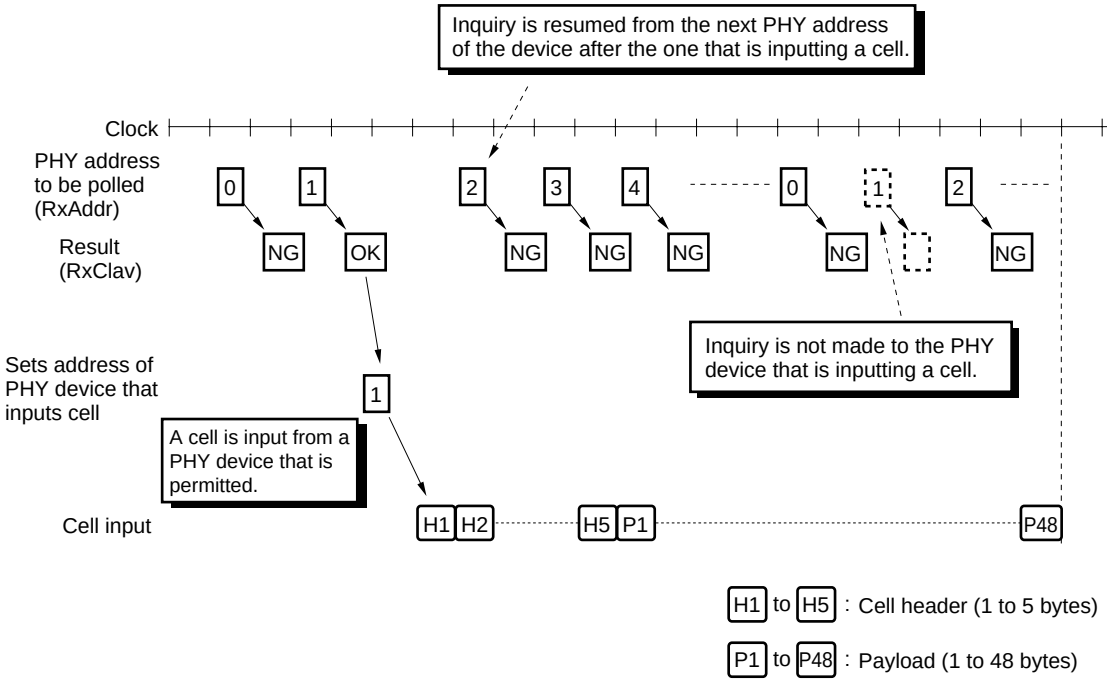
Figure 3-6. Basic Cell Input Timing 1



<Operation>

- If a PHY device returns OK in response to the inquiry, that PHY device is selected at the next clock.
- A cell is input from the selected PHY device at the clock after next.
- Inquiry is resumed at the input timing of H1. At this time, the PHY address is that of the next PHY device after the one that is inputting a cell.
- An inquiry is not made to a PHY device that is not mapped to a logical port. Nor is one made to a PHY device that is inputting a cell (refer to **Figure 3-7**).
- If another PHY device that returns OK in response to the inquiry is found while one PHY device is inputting a cell, the inquiry is stopped at that point.
- The PHY device that is to input a cell next is selected at the input timing of P48.
- Inquiry is resumed from the input timing of H1. The PHY address at this time is that of the next PHY device after the one that is inputting a cell.

Figure 3-7. Basic Cell Input Timing 2



(3) Control of continuous input

When only one PHY device is connected to one UTPIA input port, if the μPD98412 does not make an inquiry to the PHY device that is inputting the cells. As a result, the interval between inputting a cell and inputting the next cell is widened as shown in Figure 3-8, reducing the transfer rate. For this reason, the μPD98412 permits the PHY device that has been inputting cells to continue inputting if the PHY device that is to input a cell next is not determined until the clock of P48 is input.

Figure 3-8. Drop in Transfer Rate during Continuous Input

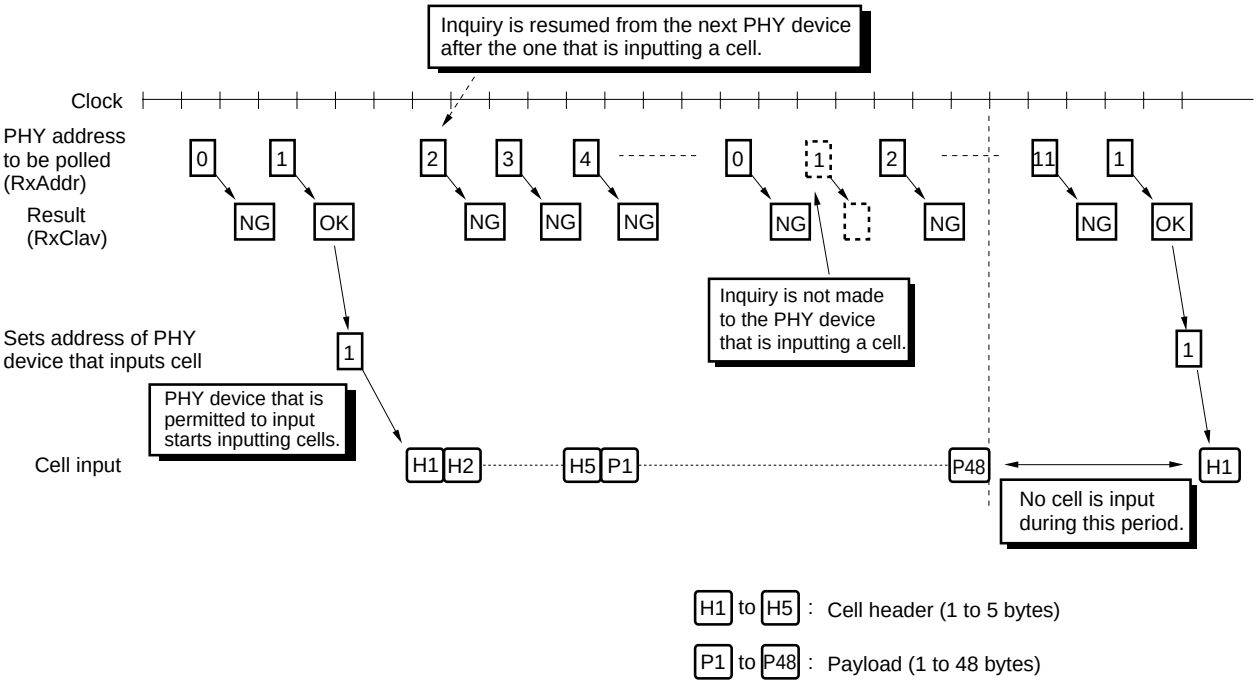
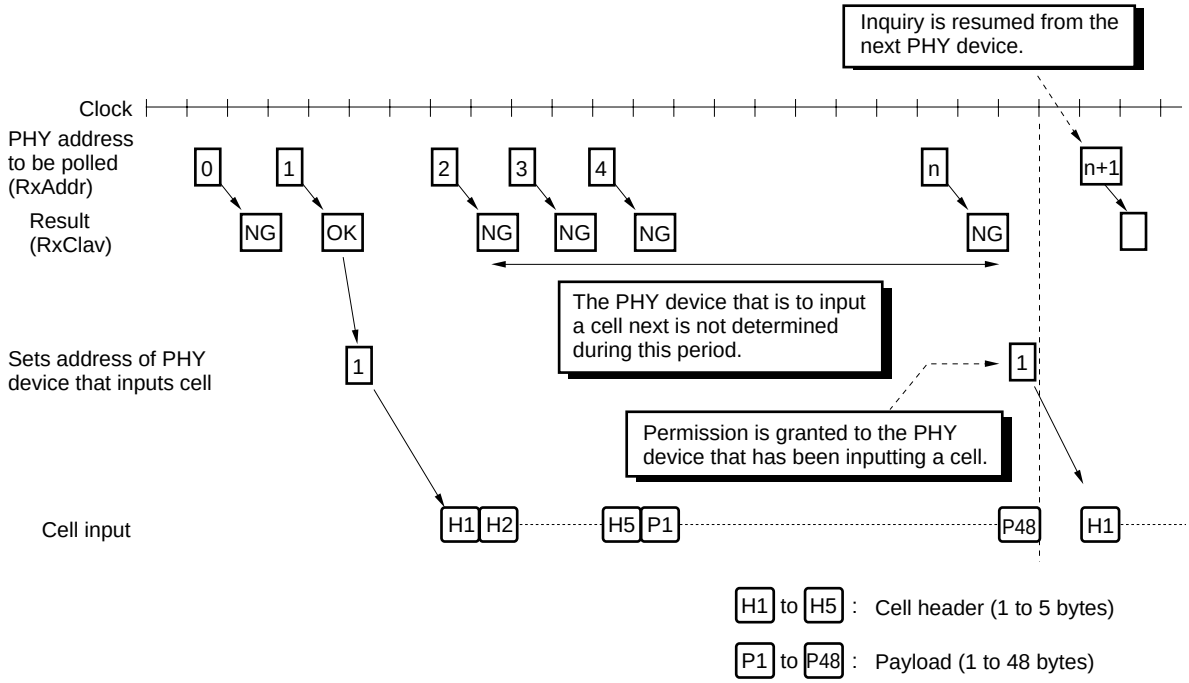
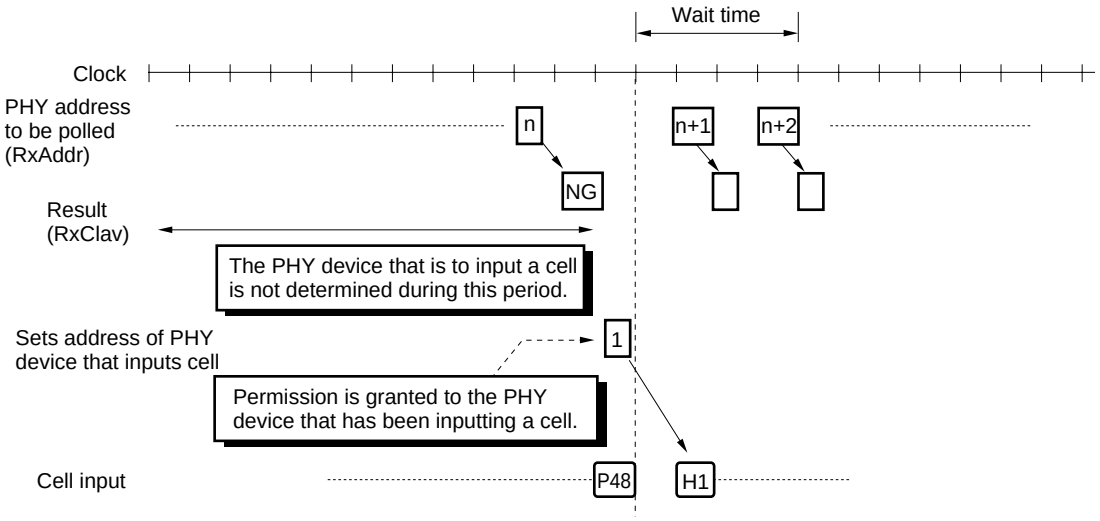


Figure 3-9. Control of Continuous Input



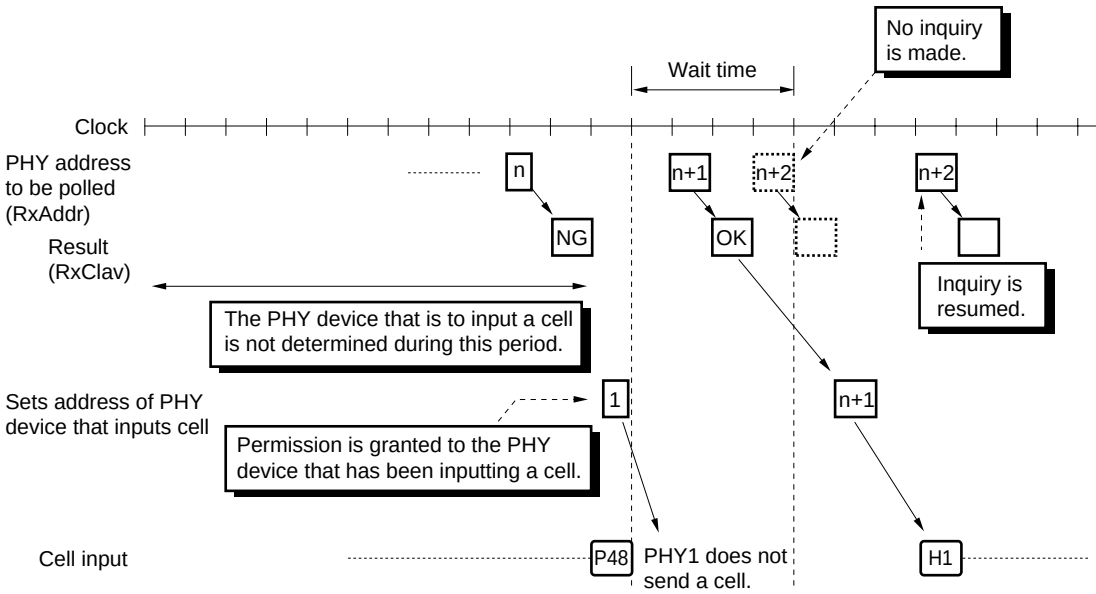
In this way, cells can be continuously input even in the case in Figure 3-9, and a drop in the transfer rate can be prevented. At this time, even if permission to input a cell is granted to the PHY device that has been inputting a cell, there is a possibility that this PHY device has no more cells. Therefore, the μPD98412 is designed to wait for a time of 4 clocks. The operations to be performed when the μPD98412 waits are illustrated below.

(a) If cell is input during wait time

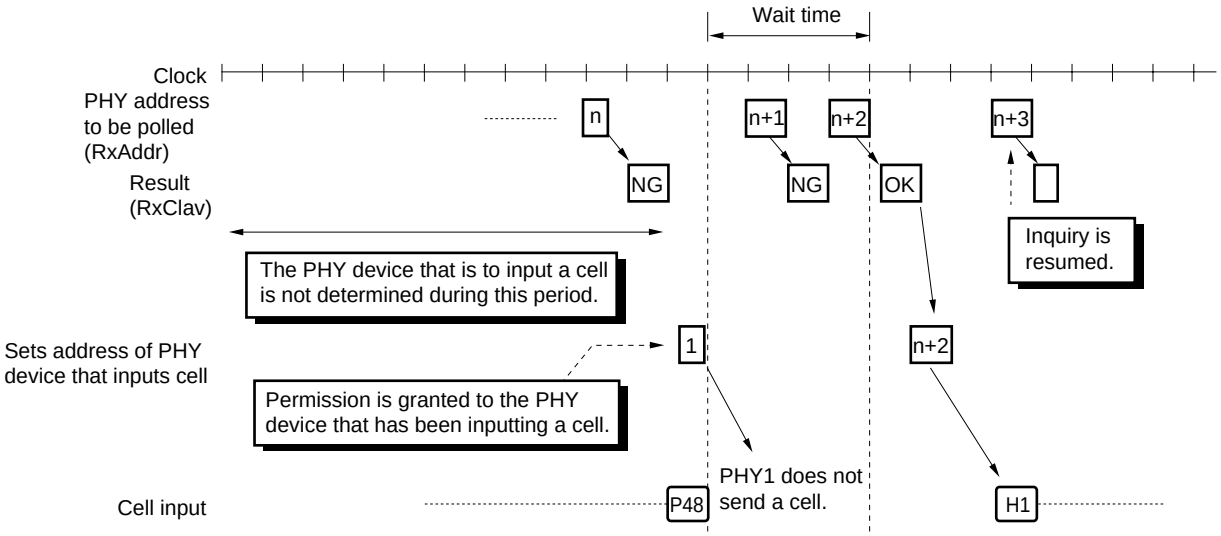


(b) If cell is not input during wait time

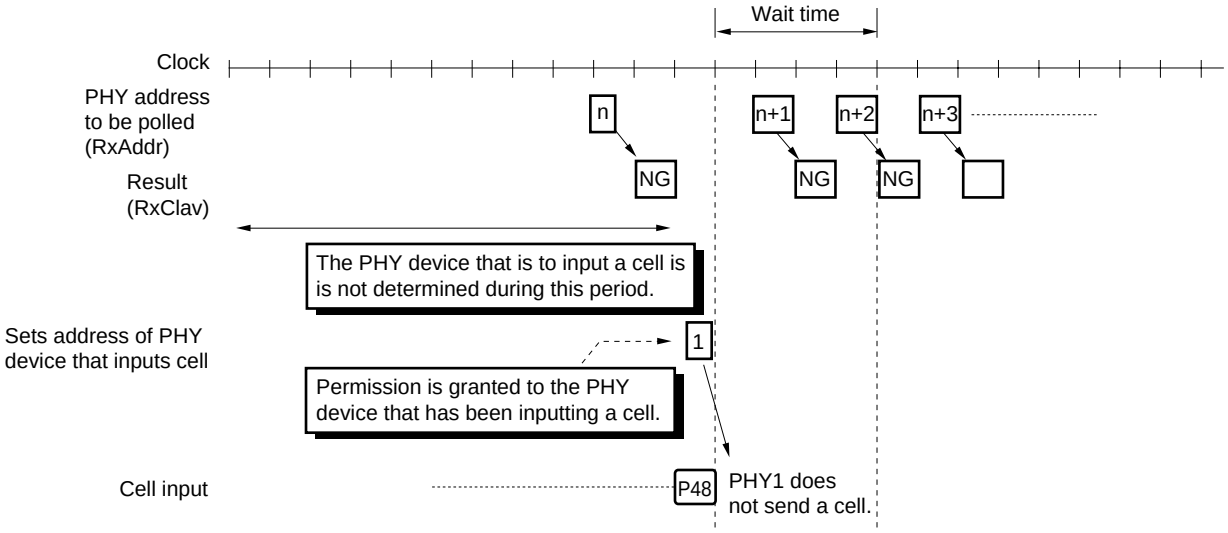
(i) If the result of polling PHY address n + 1 is OK



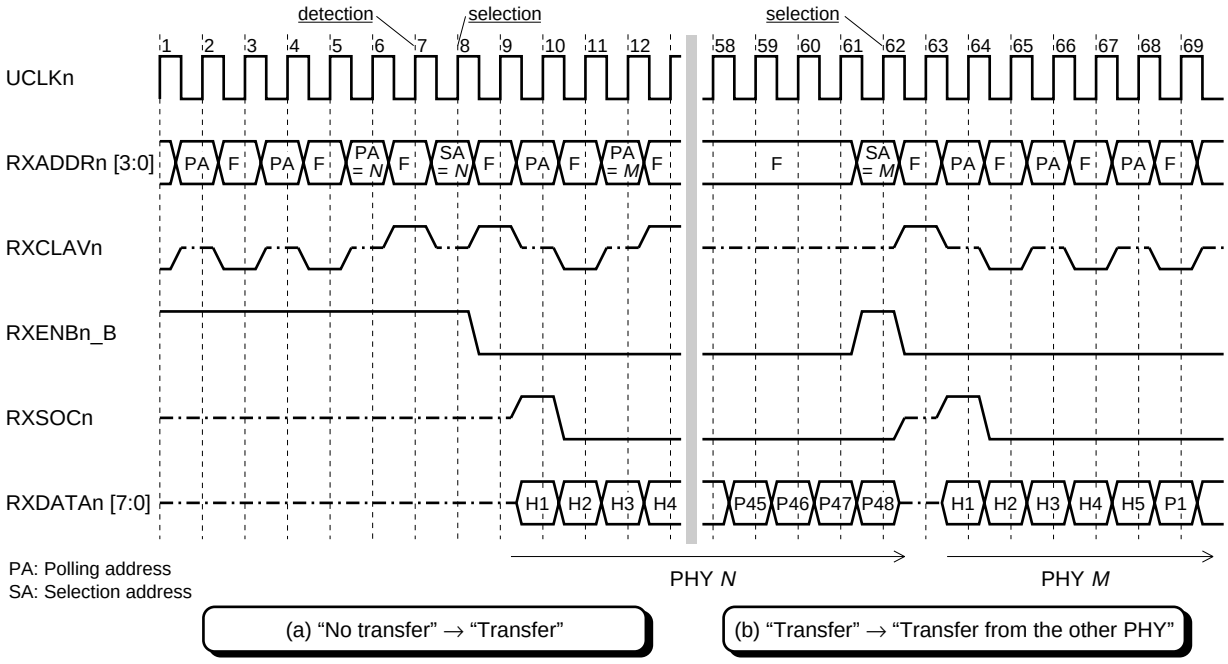
(ii) If the result of polling PHY address n + 2 is OK



(iii) If result of polling PHY addresses n + 1 and n + 2 is not OK

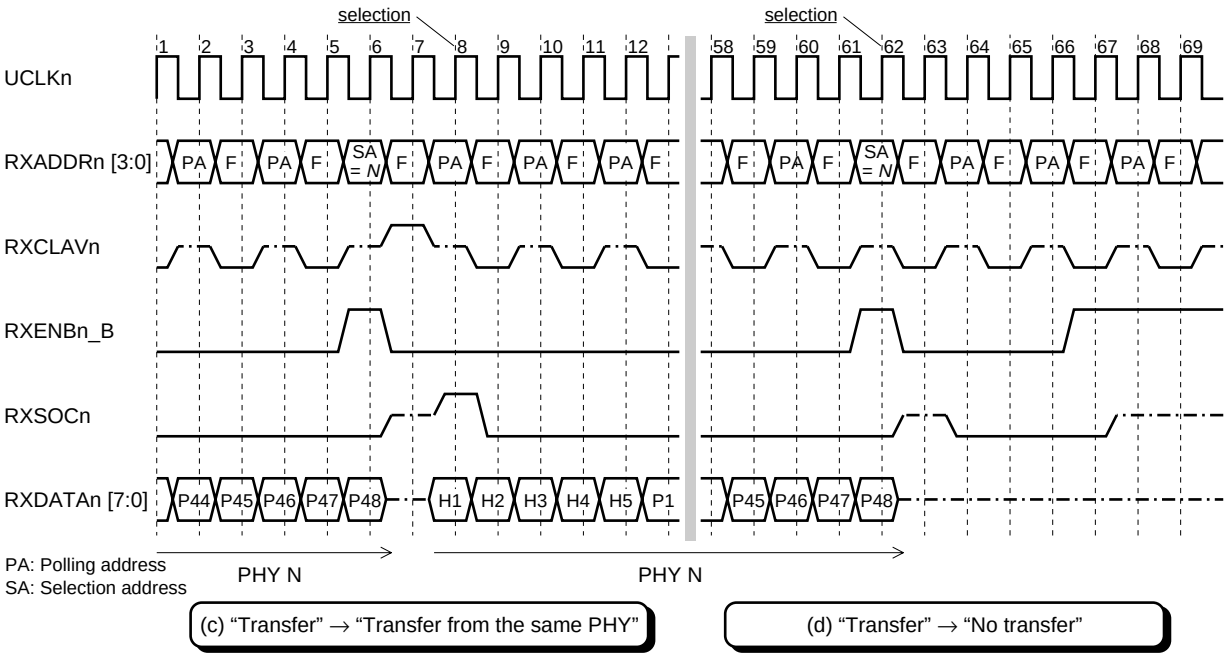


- **Timing chart**



(a) side: Once cell transfer has been started, RXENBn_B is not deasserted until cell reception is completed.

(b) side: RXENBn_B is always deasserted at the timing of P48 (payload 48). If RXADDRn [3:0] indicates "Fh" at the timing of P48, the SA timing is delayed by one clock (cell interval: 1 clock → 2 clocks).



(c) side: If cells are continuously transferred from the same PHY device, RXENBn_B is deasserted once, and selection is performed again.

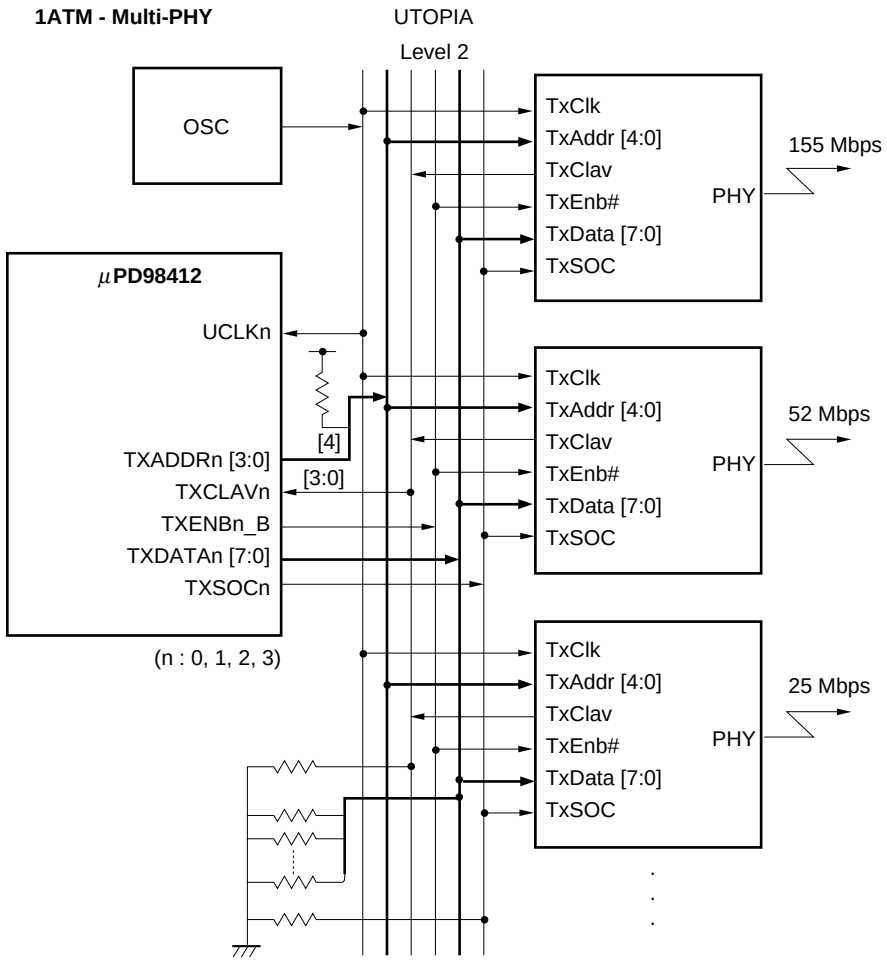
3.5.3 Output port interface

The μPD98412 can connect up to 12 output ports to the UTOPIA interfaces in 12-PHY polling mode.

An output port is mapped to a logical output port number based on the PHY address and UTOPIA interface number, in accordance with the contents of the port configuration register. The μPD98412 performs its internal processing by using this logical output port number.

Figure 3-10 shows an example of connecting multiple PHY devices to one UTOPIA interface.

Figure 3-10. Example of Connecting UTOPIA Transmit Interface



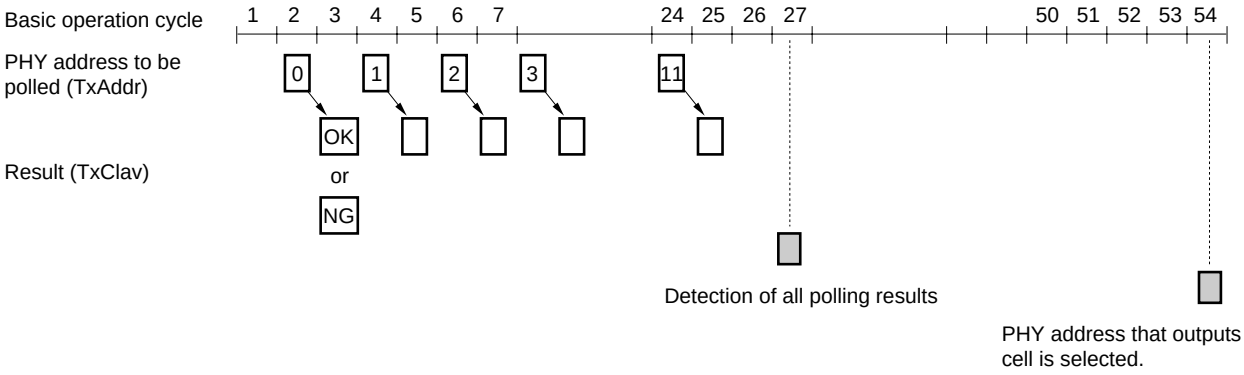
Remark Of the 5 bits of a PHY address, the low-order 4 bits are connected to the μPD98412. Pull up the highest bit. The μPD98412 outputs a PHY address of "0" through "11" for the purpose of polling.

The μPD98412 does not have a TxClk output. Supply UCLKn to the μPD98412 as a UTOPIA clock.

(1) Polling in multi-PHY mode

The relationship between polling control and the basic operation cycle is shown below.

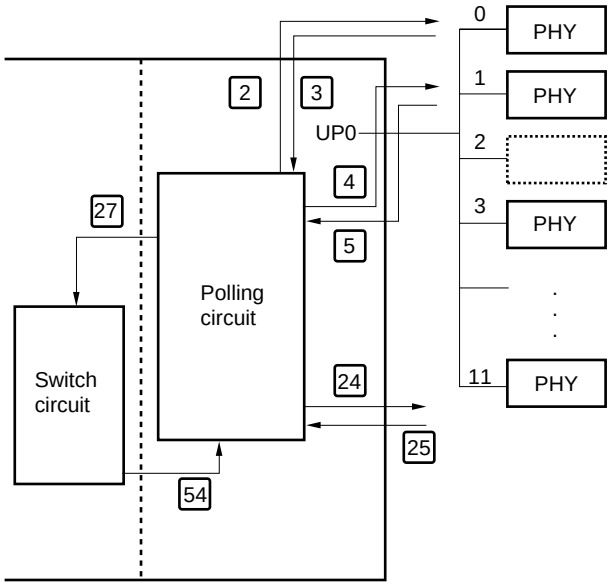
Figure 3-11. Relationship between Polling Control and Basic Operation Cycle (in Multi-PHY Mode)



<Basic operation>

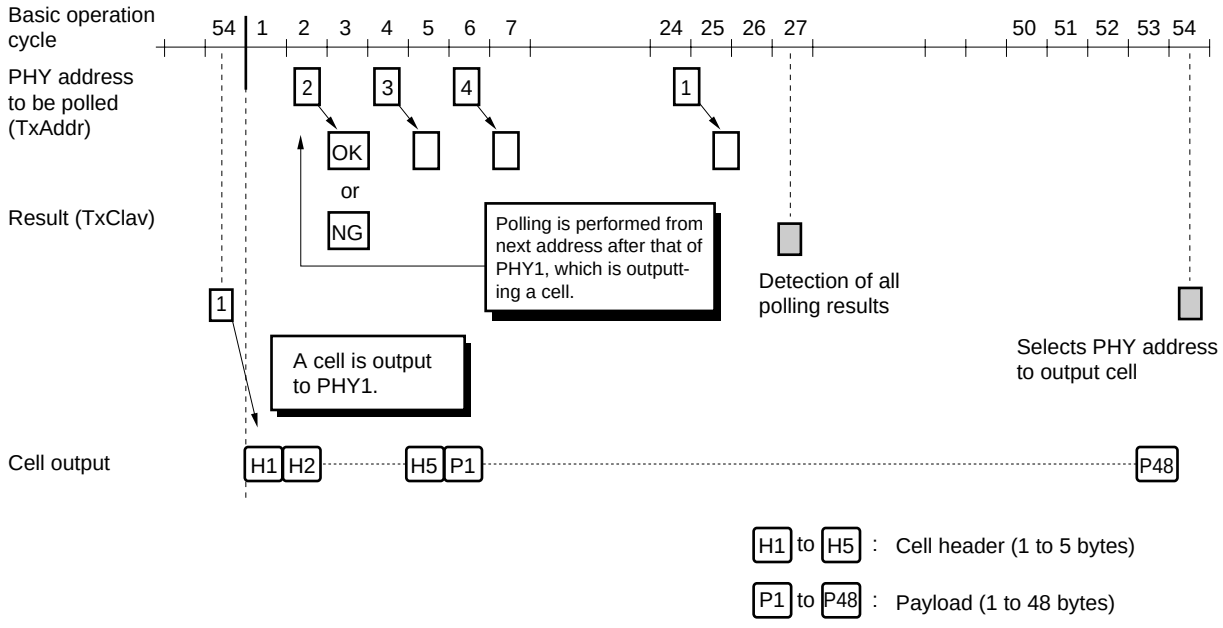
- Polling is performed starting from the second clock in the basic operation cycle.
- Inquires are made sequentially, starting from PHY address 0 (2nd, 4th, 6th, ... clock), and the result of the inquiry is returned at the next clock (3rd, 5th, 7th ... clock).
- The result of polling all the PHY devices is passed to the switch circuit at the 27th clock.
- The PHY device that outputs a cell is selected at the 54th clock (if no PHY device has a cell to output, nothing is selected).

Figure 3-12. Polling Operation during Cell Output



The μPD98412 outputs a cell to the PHY device that is selected at the 54th clock in the basic operation cycle (polling and cell output are performed in parallel). At this time, polling is started from the next PHY address after the PHY device that is currently transferring a cell.

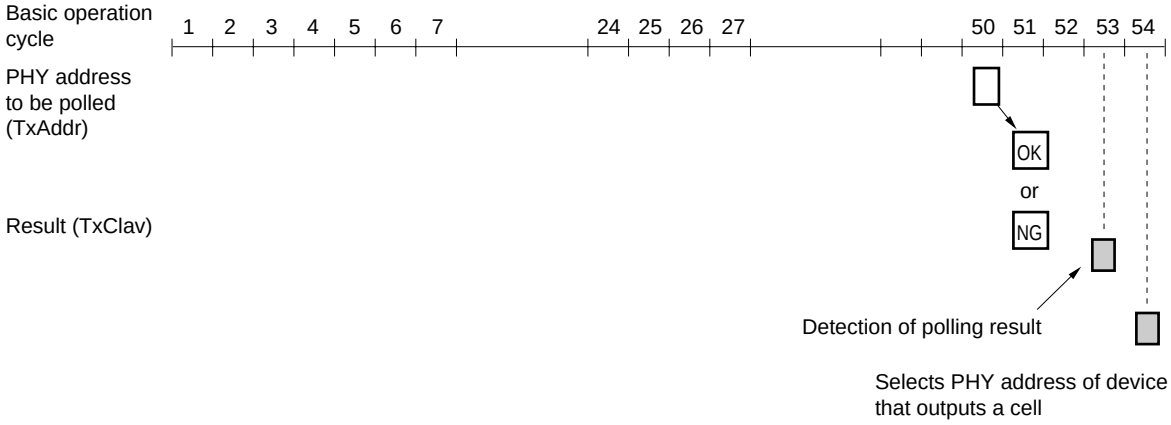
Figure 3-13. Polling Operation during Cell Output



(2) Polling in single PHY mode

The relationship between polling control and the basic operation cycle is illustrated below.

Figure 3-14. Relationship between Polling Control and Basic Operation Cycle (in Single PHY Mode)



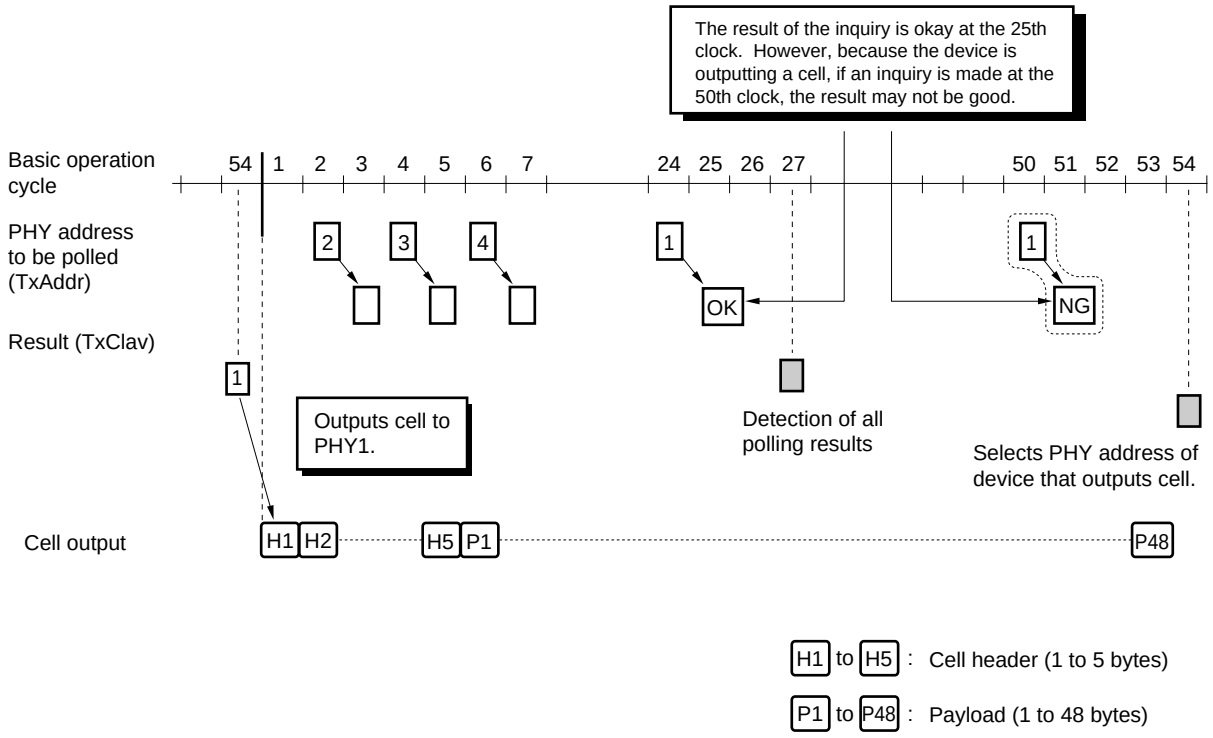
<Basic operation>

- In the single PHY mode, the PHY address connected is already known. Therefore, an inquiry is made to this PHY address at the 50th clock.
- The PHY device returns the result at the 51st clock.
- The result is passed to the switch circuit at the 53rd clock.
- If the result at the 51st clock is OK, the PHY address is selected at the 54th clock. If the result is NG, the PHY address is not selected. Even if the result at the 51st clock is OK, the PHY address is not selected if there is no cell to be output.

(3) Control of continuous output

UTOPIA Level2 stipulates that an inquiry is made at the 50th clock or onward to determine whether a cell can be output to a PHY device that is outputting a cell. However, the μPD98412 makes this inquiry between the second and the 25th clock in the multi-PHY mode, and passes the result to the internal switch circuit at the 27th clock. Consequently, the result of the inquiry may be illegal in the case shown in Figure 3-15.

Figure 3-15. Control of Continuous Output



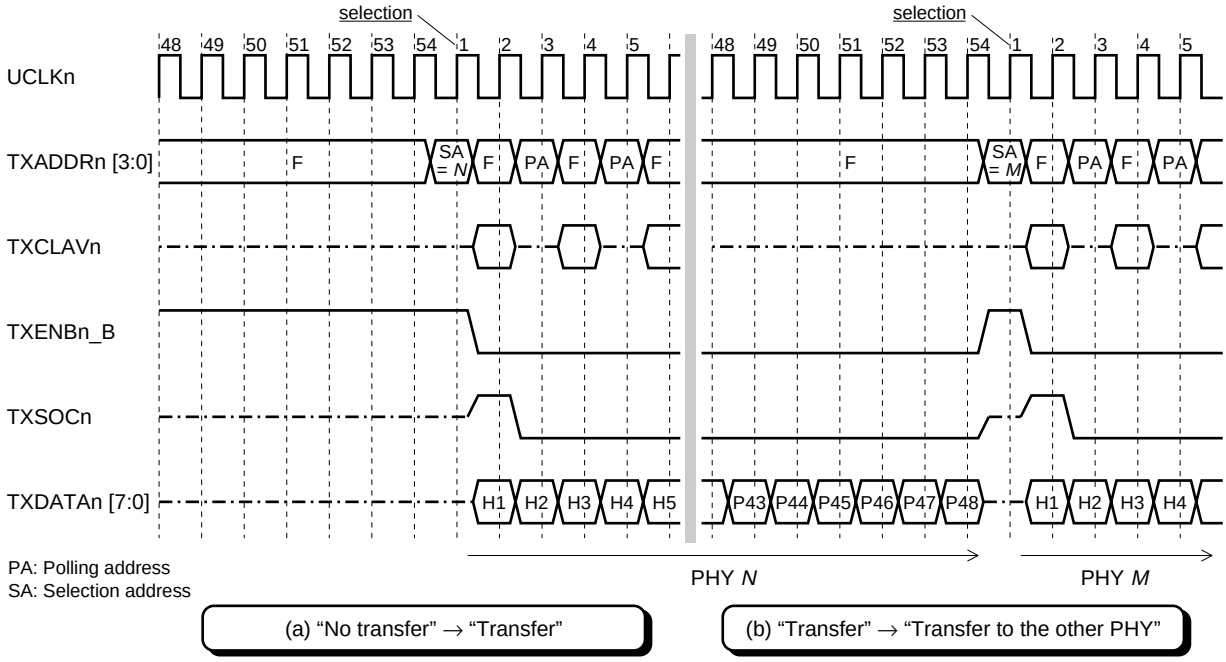
In other words, because the value detected at the 27th clock (the result of polling the PHY device that is outputting a cell) is not stipulated by UTOPIA Level2, the PHY device connected to a logical output port of the μPD98412, depending on its specifications, may return the result one cycle before and this result may be different from the real result. In this case, if cells are continuously output to PHY address 1, a problem such as lost cells, may occur.

To prevent such a problem, the μPD98412 controls successive output by using the PR bit.

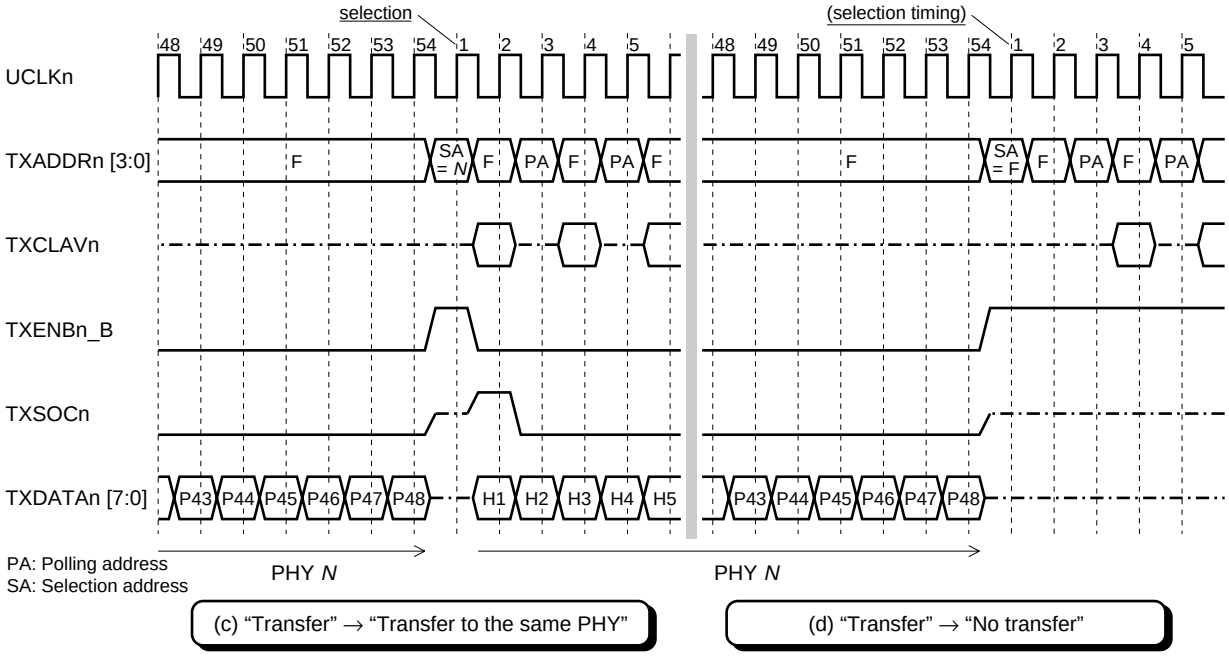
- RP = 0 → Does not permit successive output of cells to the same PHY device.
- RP = 1 → Permits successive output of cells to the same PHY device.

To output cells continuously, the validity of the result detected at the 27th clock must be guaranteed. NEC's 155M-bps PHY μPD98404 (P30) and μPD98411 (P40) satisfy this requirement and cells can be continuously output to this device.

- **Timing chart**



(a) side: Once cell transfer has been started, TXENBn_B is not deasserted until cell transmission is completed.



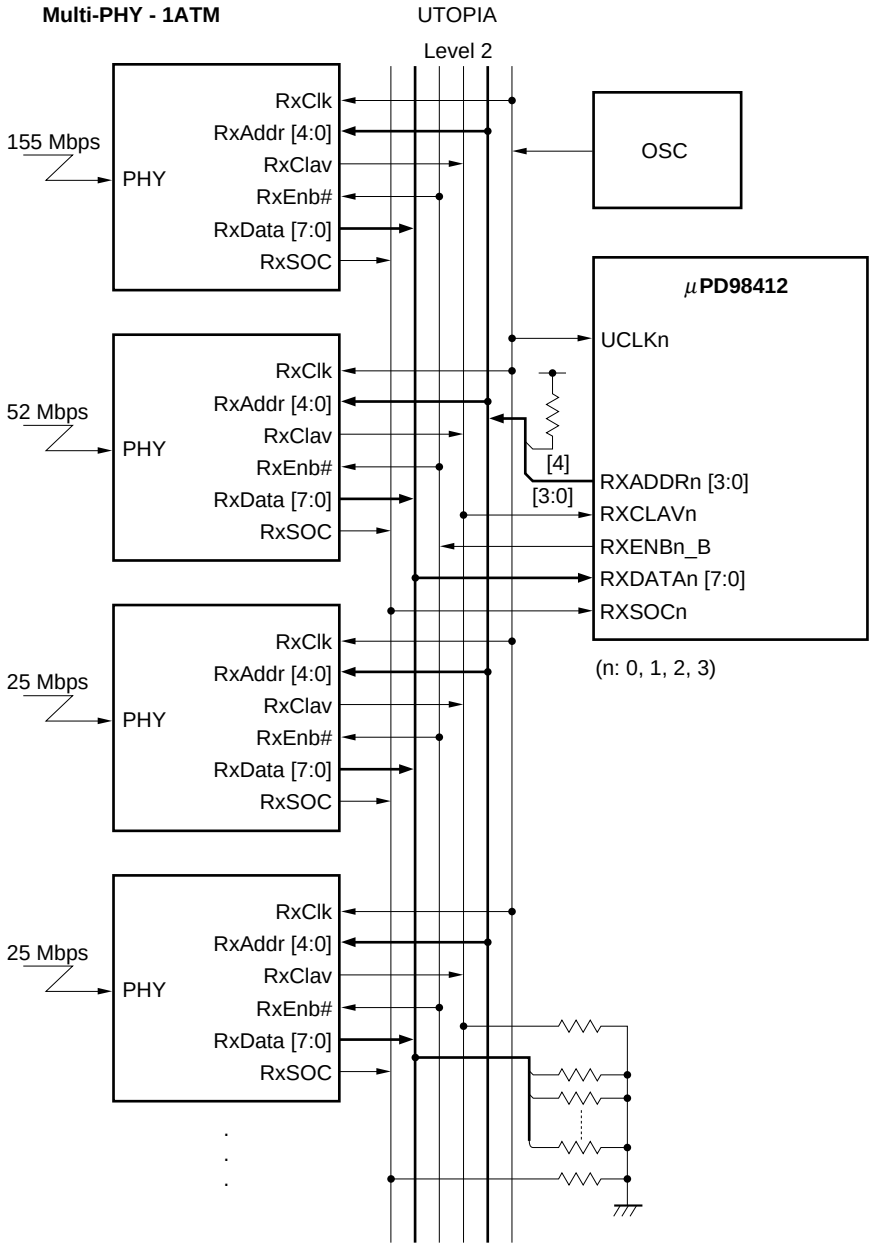
(c) side: If cells are continuously transferred from the same PHY device, TXENBn_B is deasserted once, and selection is performed again.

3.6 15-PHY Polling Mode

In the 15-PHY polling mode, up to 15 ports can be connected to the UTOPIA.

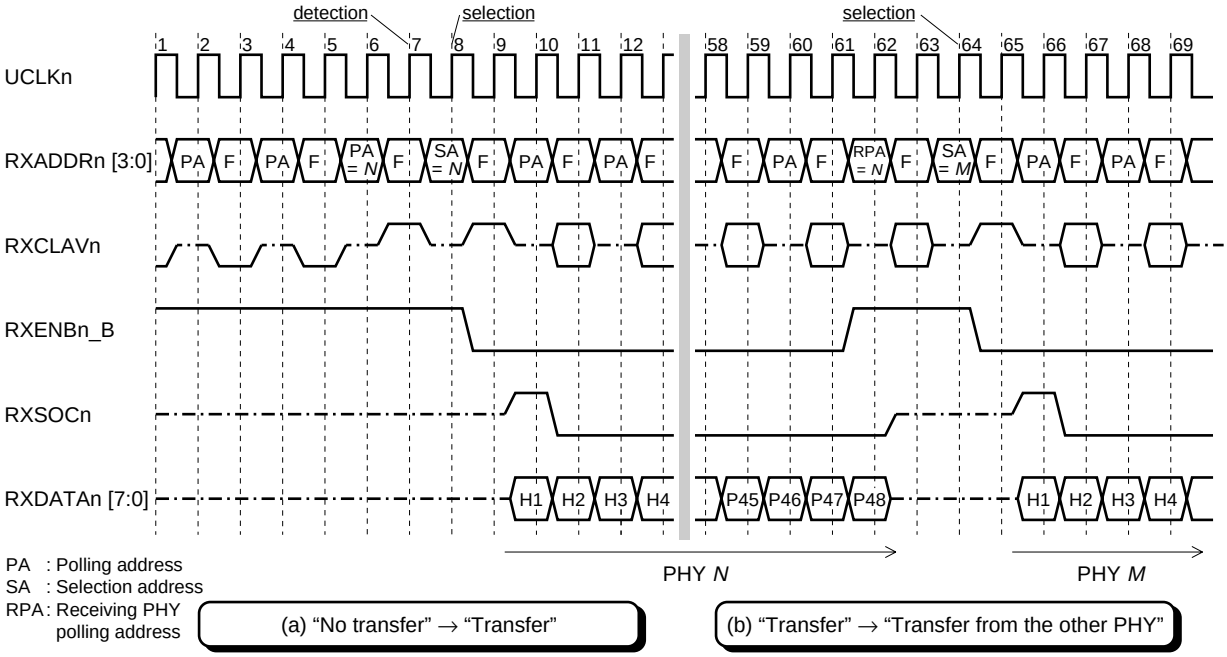
3.6.1 Input port interface

An example of connection is shown below:



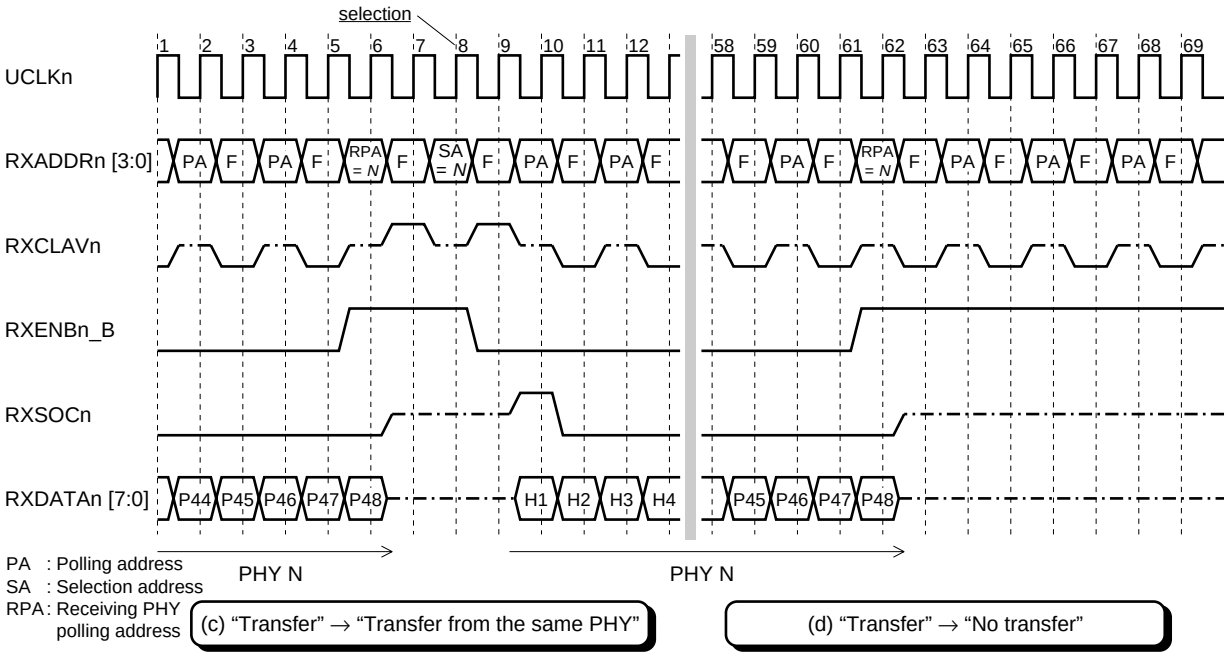
Remark A PHY address consists of 5 bits. Of these, the low-order 4-bits are connected to the μPD98412. Pull up the highest bit. The μPD98412 does not have an RxClk output. Supply UCLKn to the μPD98412 as a UTOPIA clock.

- **Timing chart (X15 handshake mode)**



(a) side: Once cell transfer has been started, RXENBn_B is not deasserted until cell reception is completed.

(b) side: RXENBn_B is always deasserted at the timing of P48 (payload 48). If RXADDRn [3:0] indicates "Fh" at the timing of P48, the RPA and SA timings are delayed by one clock (cell interval: 3 clocks → 4 clocks).



(c) side: If cells are continuously transferred from the same PHY device, RXENBn_B is deasserted once, and selection is performed again.

- **Polling**

  The polling address is output at the timing of PA (polling address) in the timing chart. As the polling address, “0h” through “Eh” are repeatedly output. However, the following two rules are applied.

  (1) A PHY address that is not assigned to any port configuration register (PT register) is not output. Instead, “Fh” is output.
  (2) While the μPD98412 receives a cell (when RXENBn_B = “L”), the address of the PHY device selected for reception is not output. Instead, “Fh” is output.

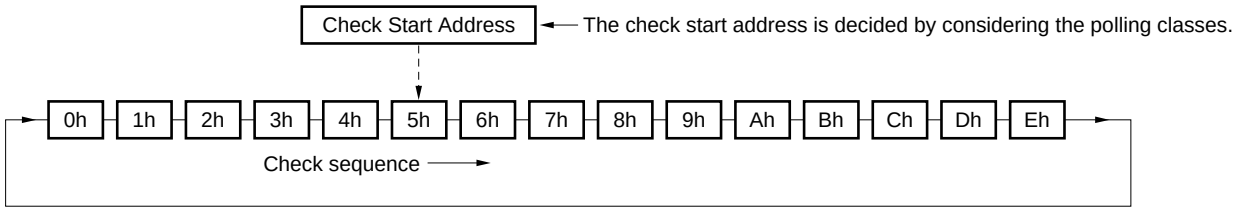
- **PHY polling during reception**

  The PHY device that is receiving a cell is polled at the timing of RPA (receiving PHY polling address) in the timing chart.

- **Selection**

  A selection address is selected by taking the obtained polling result and polling class into consideration. The selection address is output at the timing of SA (selection address) in the timing chart. RXCLAVn for the selection address is not reflected on the polling result.

  The selection address is determined by the following selection algorithm.
  In the 15-PHY polling mode, the polling result is checked starting from the check start address that has been determined by taking the polling class into consideration, in order to select the PHY device that is ready for transfer.

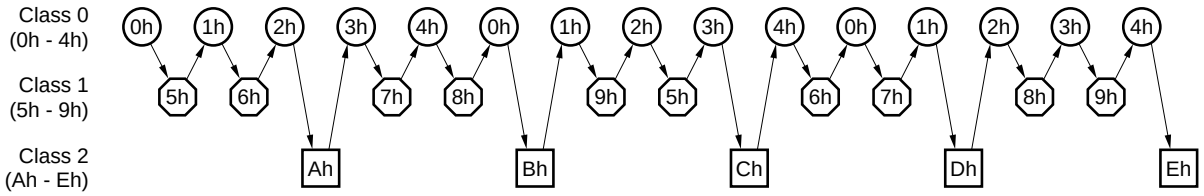


For example, if the polling result is as shown below, and if the polling result is checked starting from PHY address “5h” as shown above, the PHY device with PHY address “7h” is selected.

PHY address	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh
RxClav	L	L	L	L	L	L	L	H	H	H	L	L	L	H	H

Next, how the check start address is determined is explained.
The μPD98412 uses a polling class to determine the check start address. For details of the polling class, refer to the description of polling in the 2-group weighted polling mode. To simplify the explanation, a case where five PHY devices are allocated to each class is considered.

NPC0 = 5, NPC1 = 5, NPC2 = 5



- Setting of UTPCFG register

  NPC0 = 5, NPC1 = 5, NPC2 = 5

- PHY address

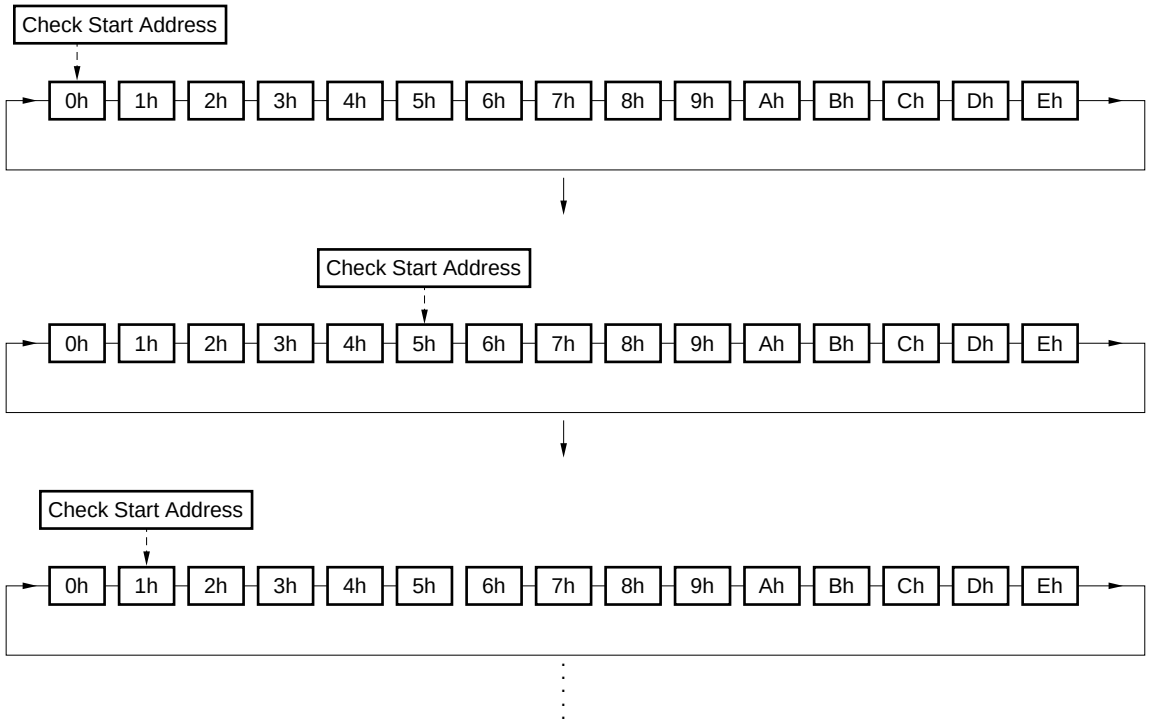
  If the UTPCFG register is set as shown above, the PHY addresses are allocated to each polling class as follows:

  Class 0: 0h through 4h

  Class 1: 5h through 9h

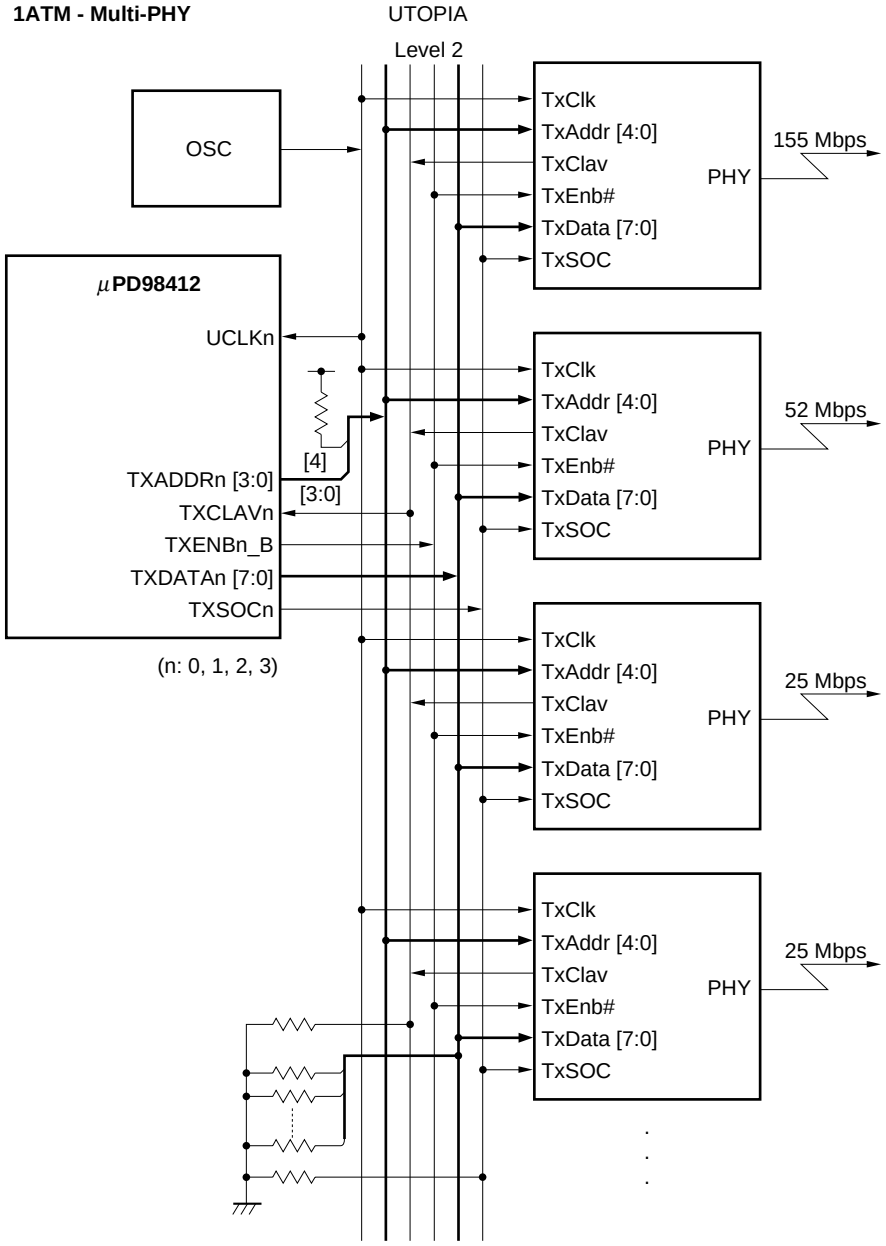
  Class 2: Ah through Eh

With the μPD98412, the check start address of the polling result changes “0h” → “5h” → “1h” → “6h”, and so on, as shown in the above figure.



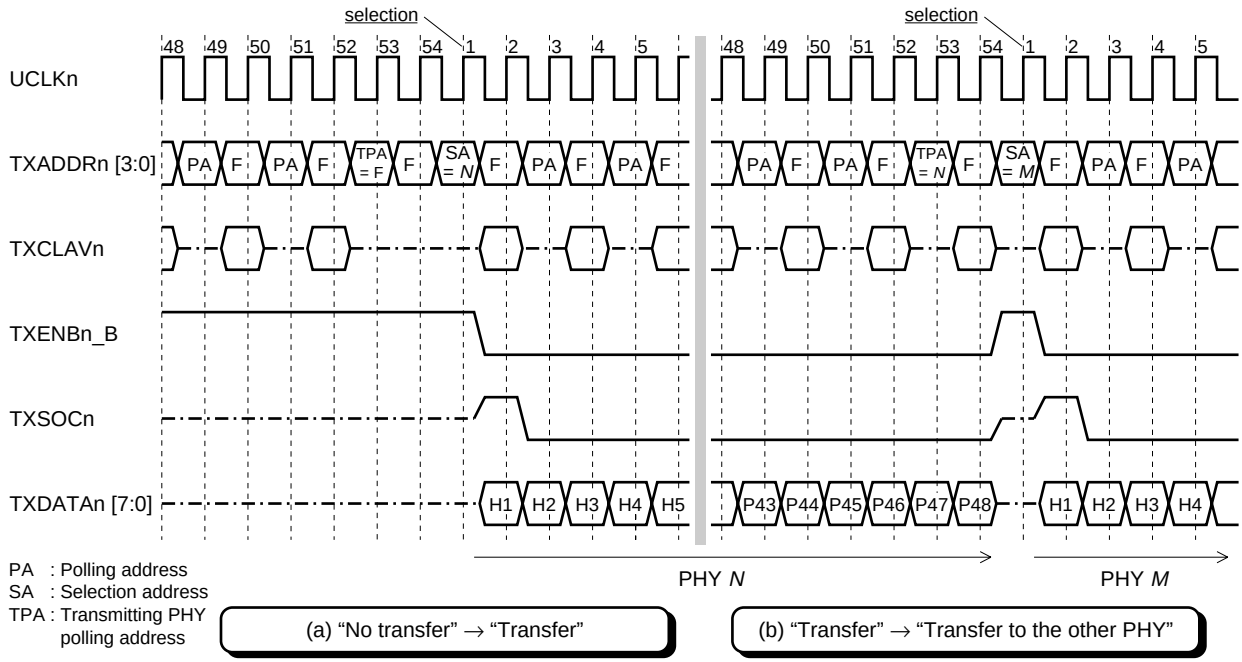
3.6.2 Output port interface

An example of connection is shown below:

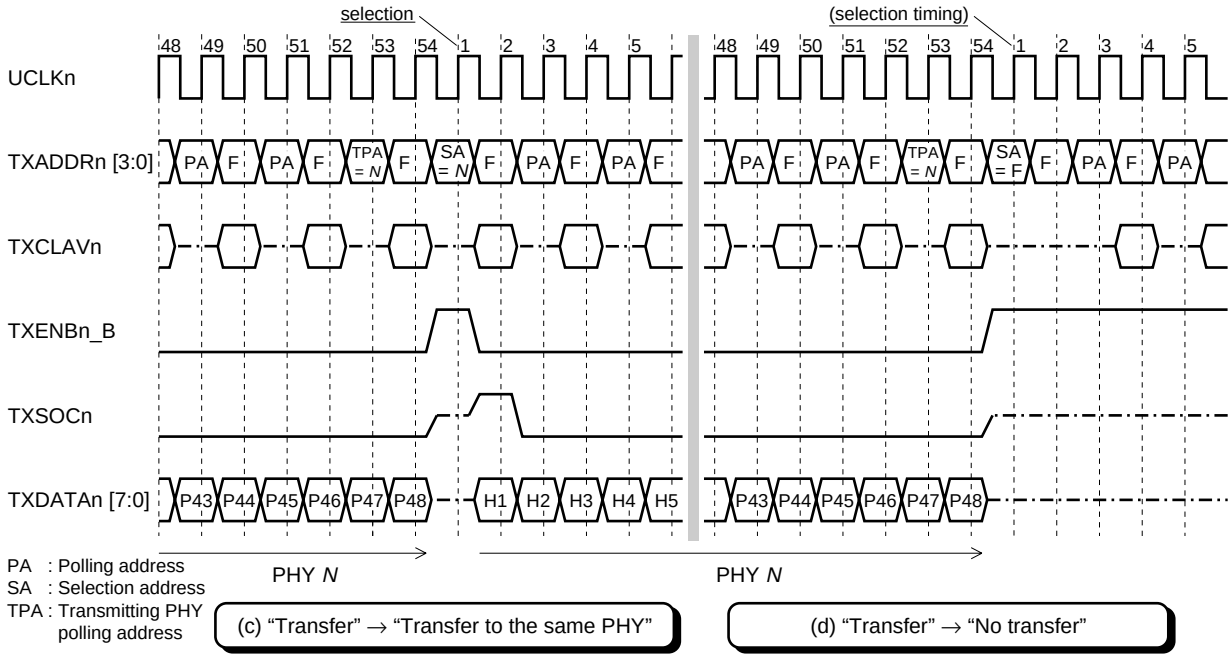


Remark A PHY address consists of 5 bits. Of these, the low-order 4-bits are connected to the μPD98412. Pull up the highest bit. The μPD98412 does not have an TxClk output. Supply UCLKn to the μPD98412 as a UTOPIA clock.

- **Timing chart**



(a) side: Once cell transfer has been started, TXENBn_B is not deasserted until cell transmission is completed.



(c) side: If cells are continuously transferred from the same PHY device, TXENBn_B is deasserted once, and selection is performed again.

- **Polling**

  The polling address is output at the timing of PA (polling address) in the timing chart. The output sequence of the polling address is the same as that of the input port interface.

- **Transferring PHY polling**

  The PHY device that is transferring a cell is polled at the timing of TPA (transferring PHY polling address) in the timing chart.

  If a cell is not transferred, “Fh” is output at the timing of TPA.

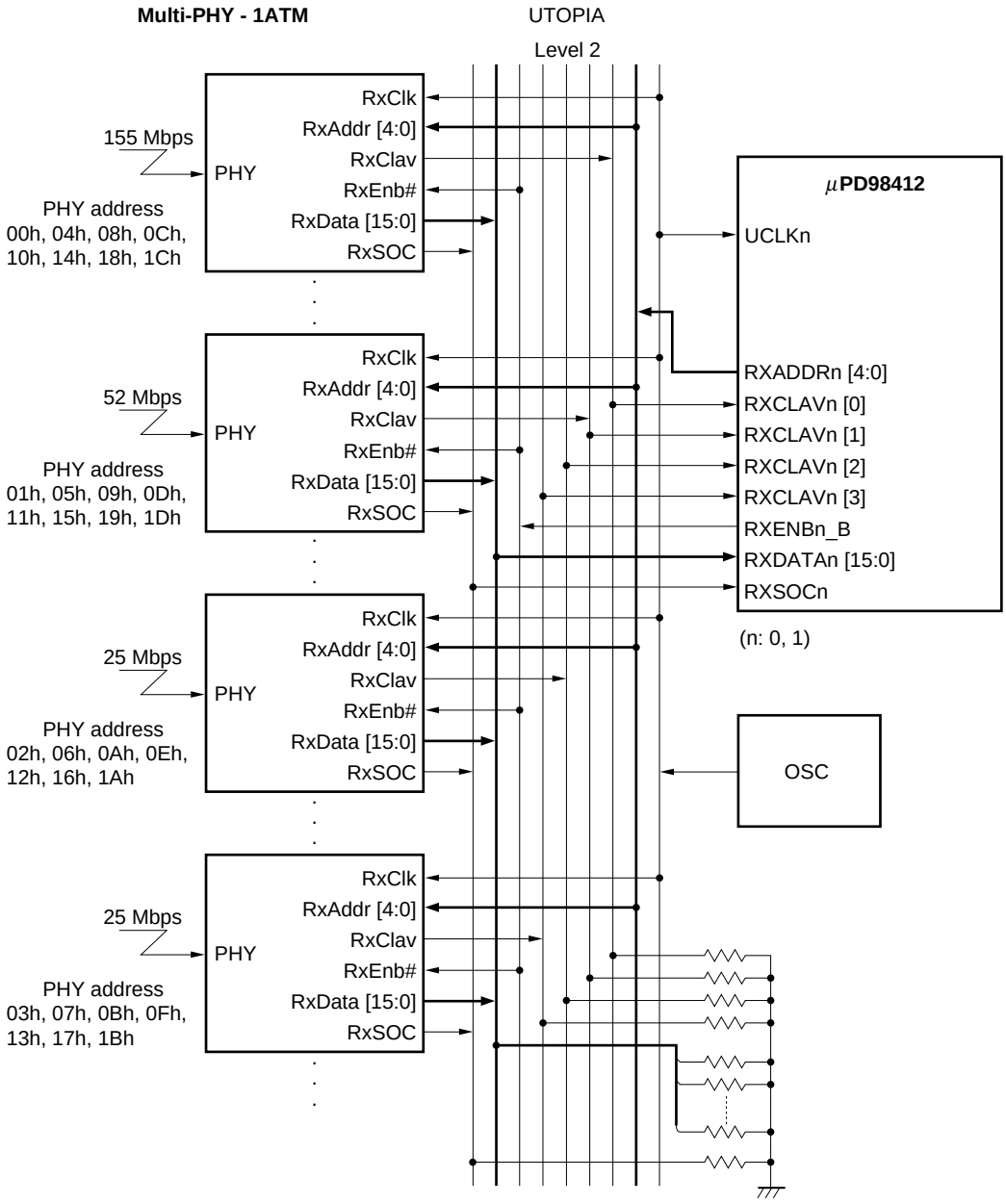
- **Selection**

  The selection address is output at the timing of SA (selection address) in the timing chart. TXCLAVn for the selection address is not reflected on the polling result.

3.7 Multiplexed Status Polling Mode

The multiplexed status polling mode supports up to 30 I/O ports with the 16-bit UTOPIA interfaces, by means of multiple PHY connection. These I/O ports can be divided into four groups by classification of PHY addresses, and each group controls the RXCALV and TXCLAV signals.

3.7.1 Input port interface

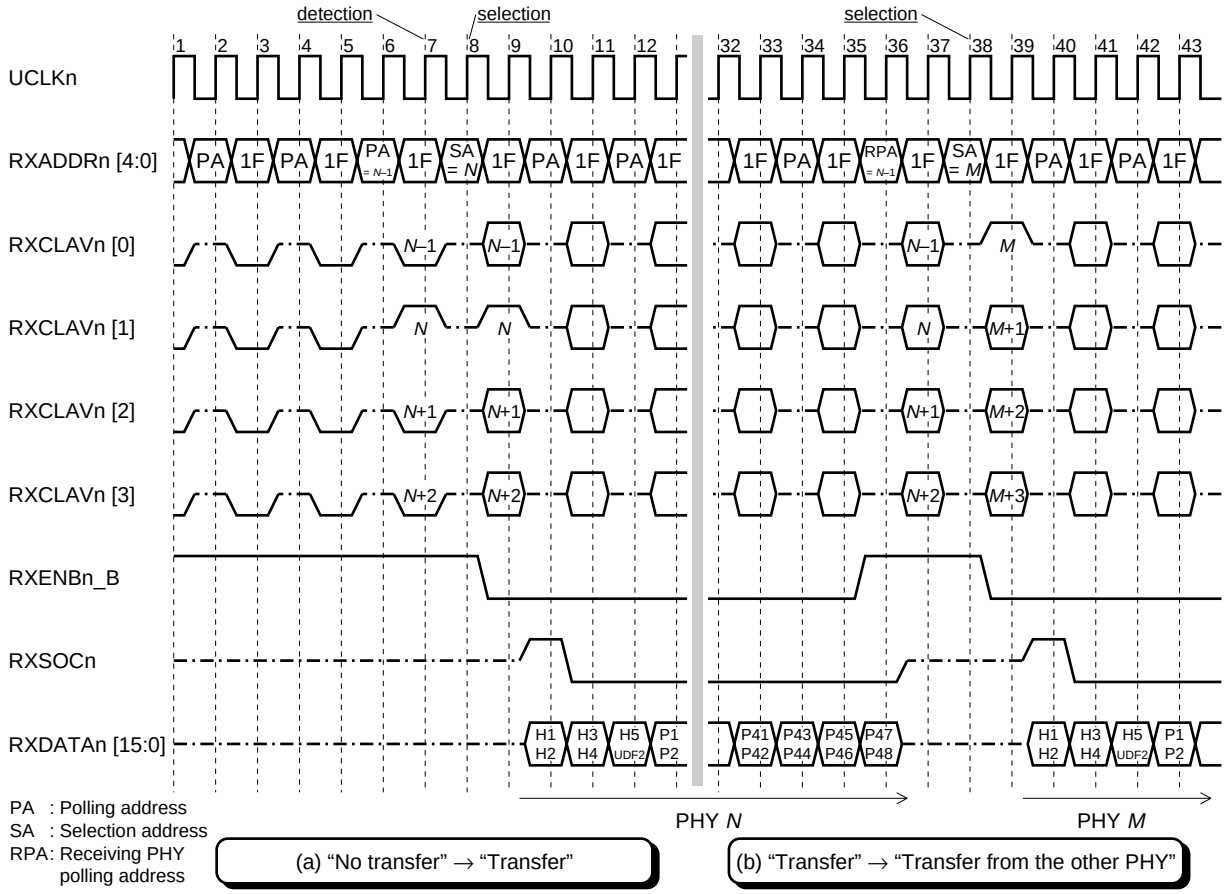


Remark Correspondence of RXCLAVn[m] connected to PHY address

PHY Address	RXCLAVn[m]
“00h”, “04h”, “08h”, “0Ch”, “10h”, “14h”, “18h”, “1Ch”,	RXCLAVn[0]
“01h”, “05h”, “09h”, “0Dh”, “11h”, “15h”, “19h”, “1Dh”,	RXCLAVn[1]
“02h”, “06h”, “0Ah”, “0Eh”, “12h”, “16h”, “1Ah”,	RXCLAVn[2]
“03h”, “07h”, “0Bh”, “0Fh”, “13h”, “17h”, “1Bh”,	RXCLAVn[3]

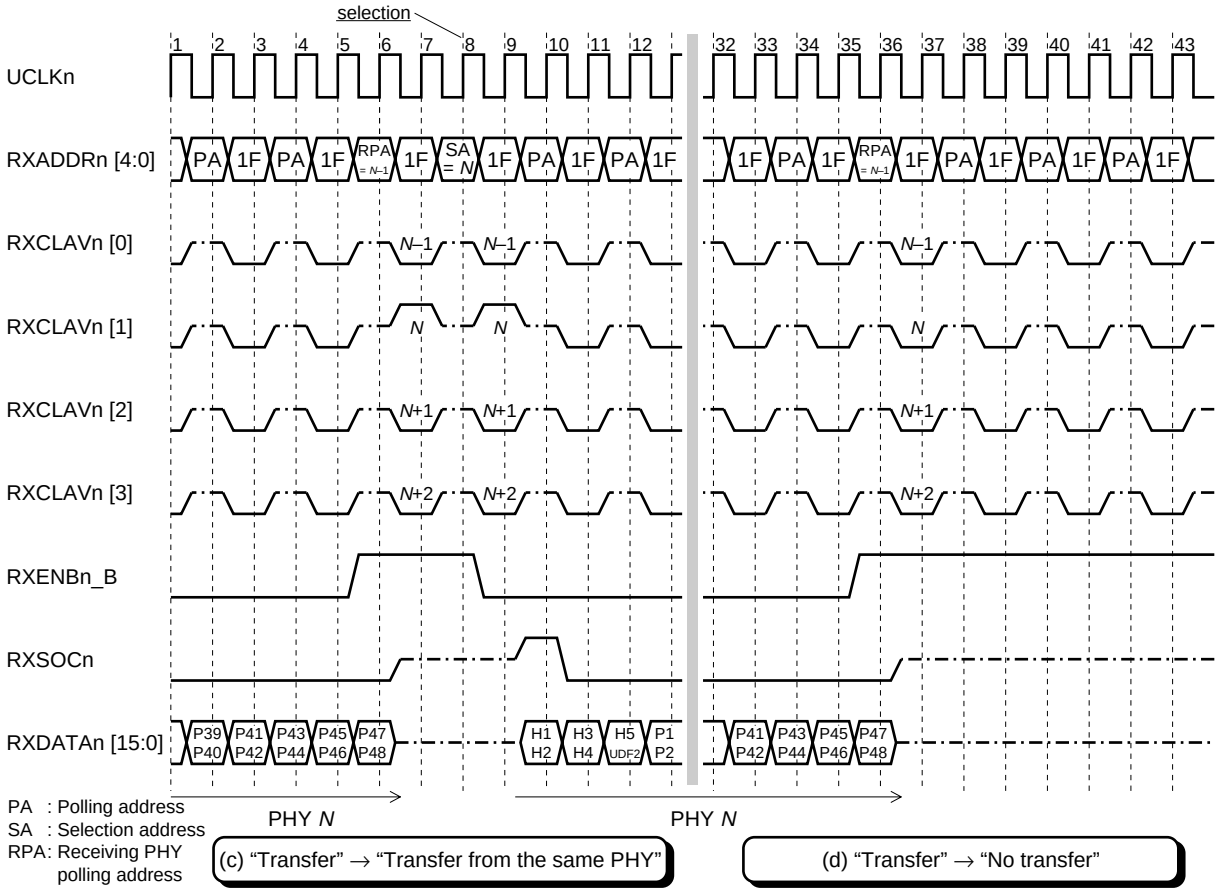
The μPD98412 does not support RxClk output. Supply UCLKn to the μPD98412 as the UTOPIA clock.

- **Timing chart (X15 handshake mode)**



(a) side: Once cell transfer has been started, RXENBn_B is not deasserted until cell reception is completed.

(b) side: RXENBn_B is always deasserted at the timing of P47/48 (payload 47/48). When RXADDRn [3:0] indicates "Fh" at the timing of P47/48, the RPA and SA timings are delayed by one clock (cell interval: 3 clocks → 4 clocks).



(c) side: If cells are continuously transferred from the same PHY device, RXENBn_B is deasserted once, and selection is performed again.

- **Polling**

  The polling address is output at the timing of PA (polling address) in the timing chart. As the polling address, "00h", "04h", "08h", "0Ch", "10h", "14h", "18h", and "1Ch" are repeatedly output.

- **PHY polling during reception**

  The PHY device that is receiving a cell is polled at the timing of RPA (receiving PHY polling address) in the timing chart.

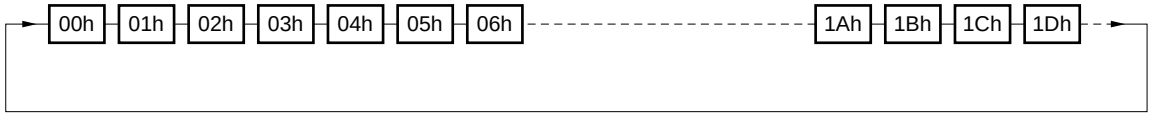
- **Selection**

  A selection address is selected by taking the obtained polling result and polling class into consideration. The selection address is output at the timing of SA (selection address) in the timing chart. RXCLAVn[0], RXCLAVn[1], RXCLAVn[2], and RXCLAVn[3] for the selection address are not reflected on the polling result.

For details of how the selection address is determined, refer to the description of the 15-PHY polling mode. This mode differs from the 15-PHY polling mode in the following way:

Check sequence)

Because the number of PHY devices that can be connected is 30, the addresses of these devices are determined from “00h” to “1Dh”, as follows:

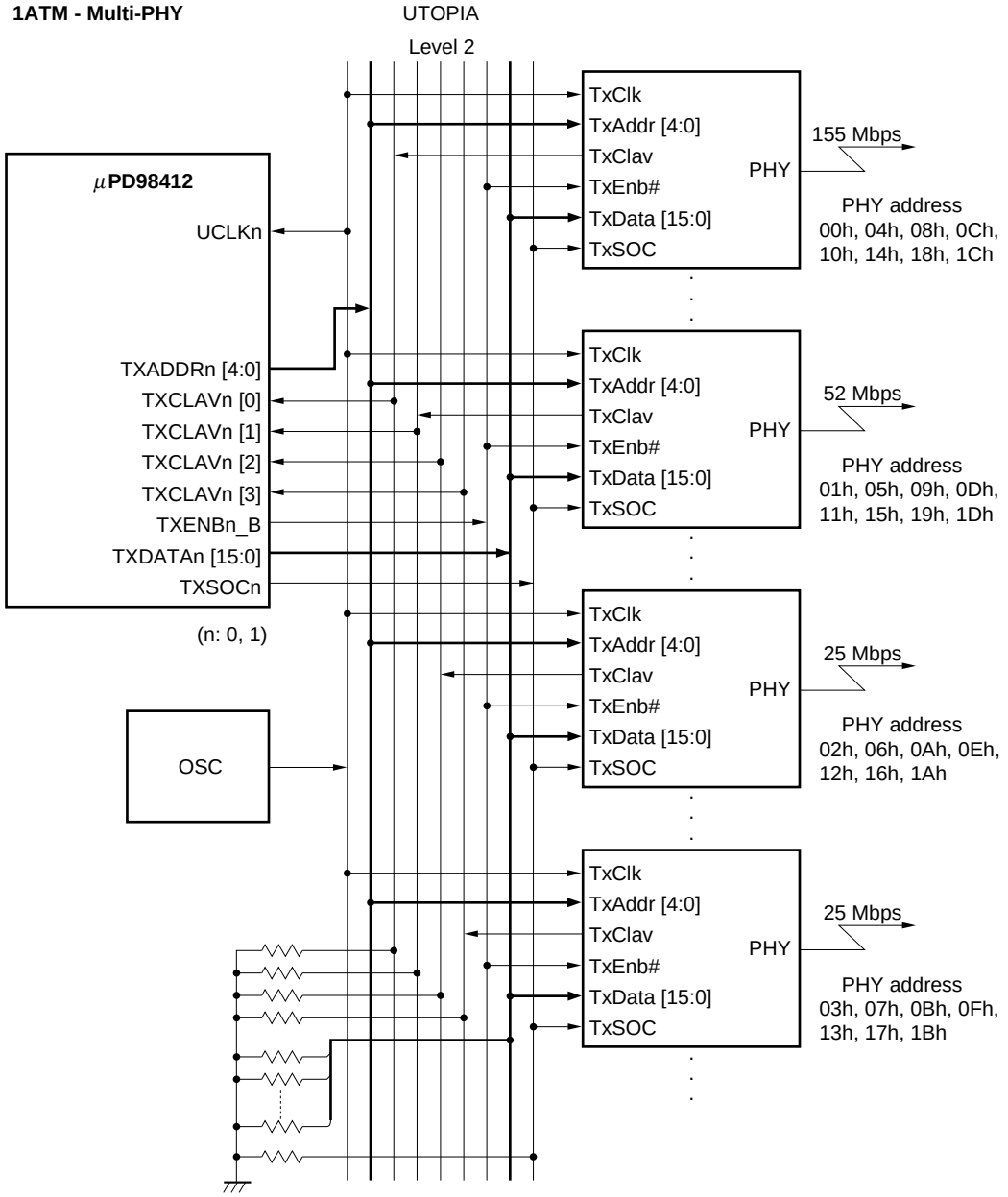


Check start address)

The check start address is determined by taking the polling class into consideration, in the same manner as in the 15-PHY polling mode. Note, however, that the number of PHY devices is 30.

3.7.2 Output port interface

An example of connection is shown below:

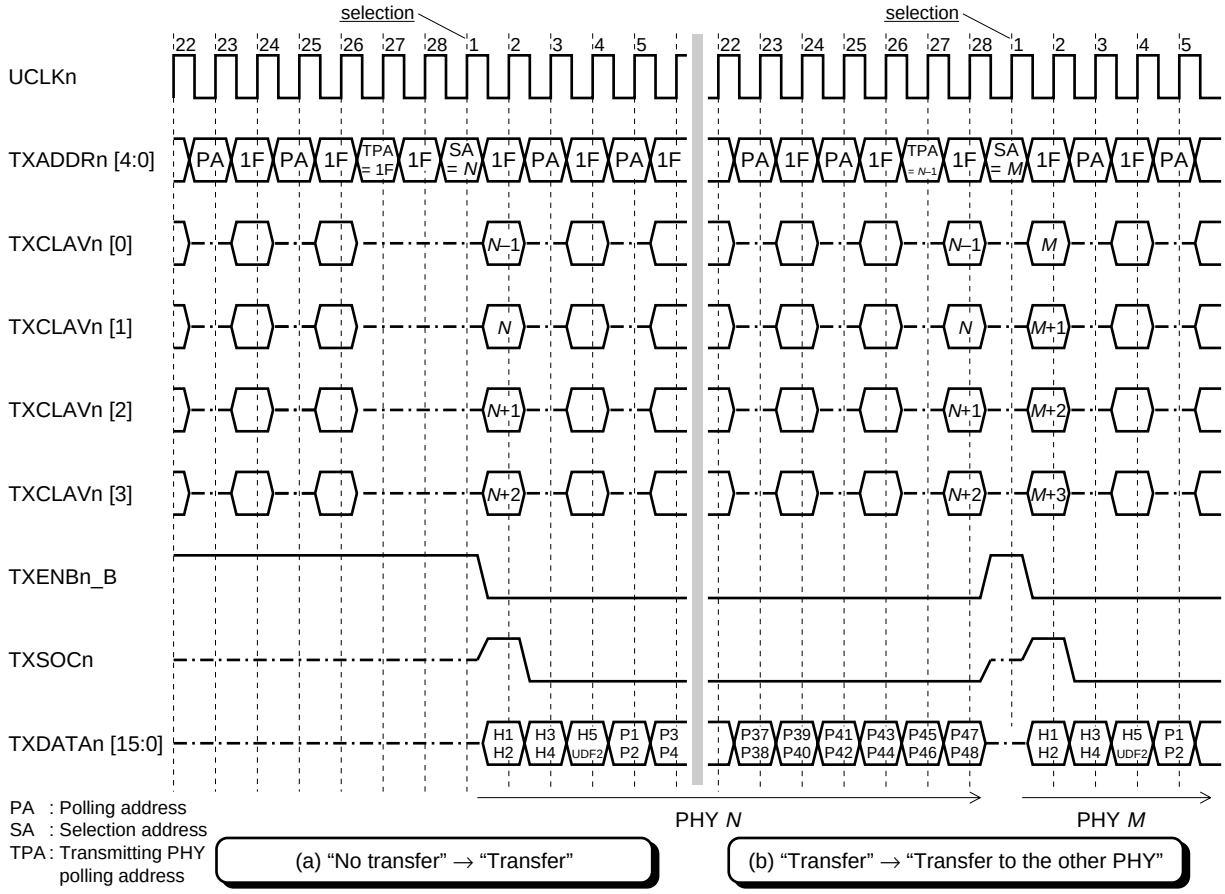


Remark Correspondence of TXCLAVn[m] connected to PHY address

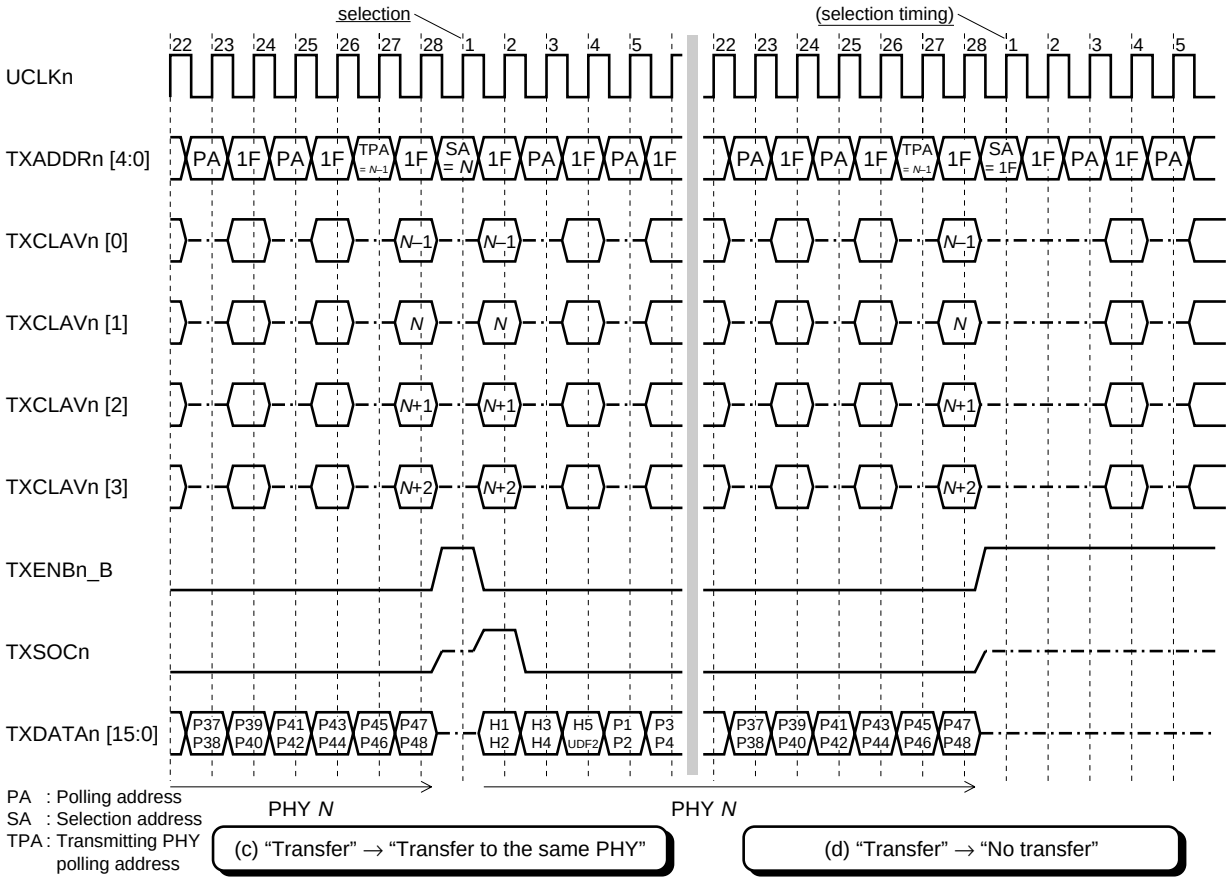
PHY Address	TXCLAVn[m]
“00h”, “04h”, “08h”, “0Ch”, “10h”, “14h”, “18h”, “1Ch”,	TXCLAVn [0]
“01h”, “05h”, “09h”, “0Dh”, “11h”, “15h”, “19h”, “1Dh”,	TXCLAVn [1]
“02h”, “06h”, “0Ah”, “0Eh”, “12h”, “16h”, “1Ah”,	TXCLAVn [2]
“03h”, “07h”, “0Bh”, “0Fh”, “13h”, “17h”, “1Bh”,	TXCLAVn [3]

The μPD98412 does not support TxClk output. Supply UCLKn to the μPD98412 as the UTOPIA clock.

- **Timing chart (Multi-PHY connection mode)**



(a) side: Once cell transfer has been started, TXENBn_B is not deasserted until cell transmission is completed.



(c) side: If cells are continuously transferred from the same PHY device, TXENBn_B is deasserted once, and selection is performed again.

- **Polling**

  The polling address is output at the timing of PA (polling address) in the timing chart. The output sequence of the polling address is the same as that of the input port interface.

- **Transferring PHY polling**

  The PHY device that is transferring a cell is polled at the timing of TPA (transferring PHY polling address) in the timing chart.

  If a cell is not transferred, "Fh" is output at the timing of TPA.

- **Selection**

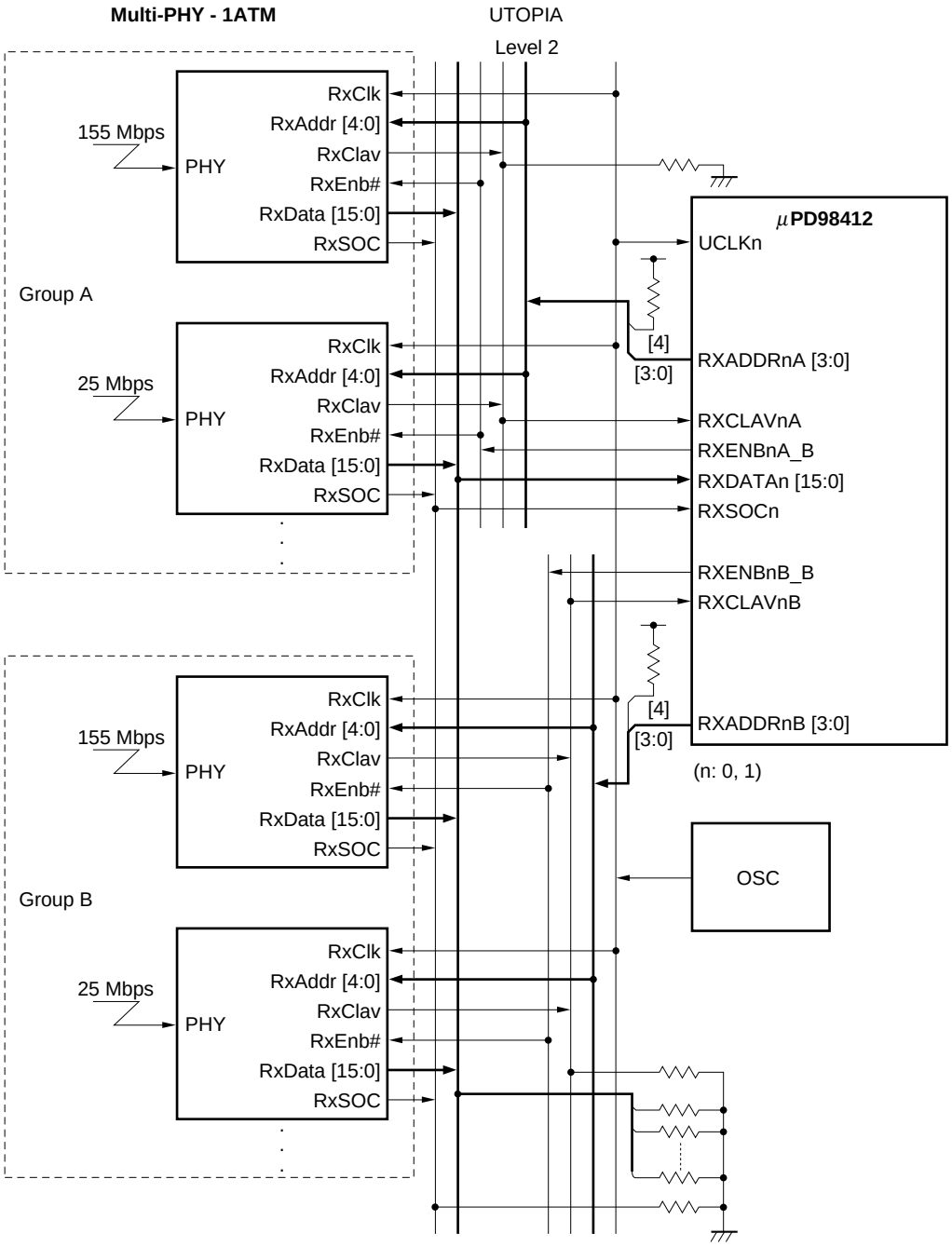
  The selection address is output at the timing of SA (selection address) in the timing chart. TXCLAVn[0], TXCLAVn[1], TXCLAVn[2], and TXCLAVn[3] for the selection address are not reflected on the polling result.

3.8 2-Group Weighted Polling Mode

The 2-group weighted polling mode supports up to 30 I/O ports with the 16-bit UTOPIA interfaces, by means of multiple PHY connection. The multiple PHY ports connected to one UTOPIA interface can be divided into two groups, and each group controls the RXCALV and TXCLAV signals.

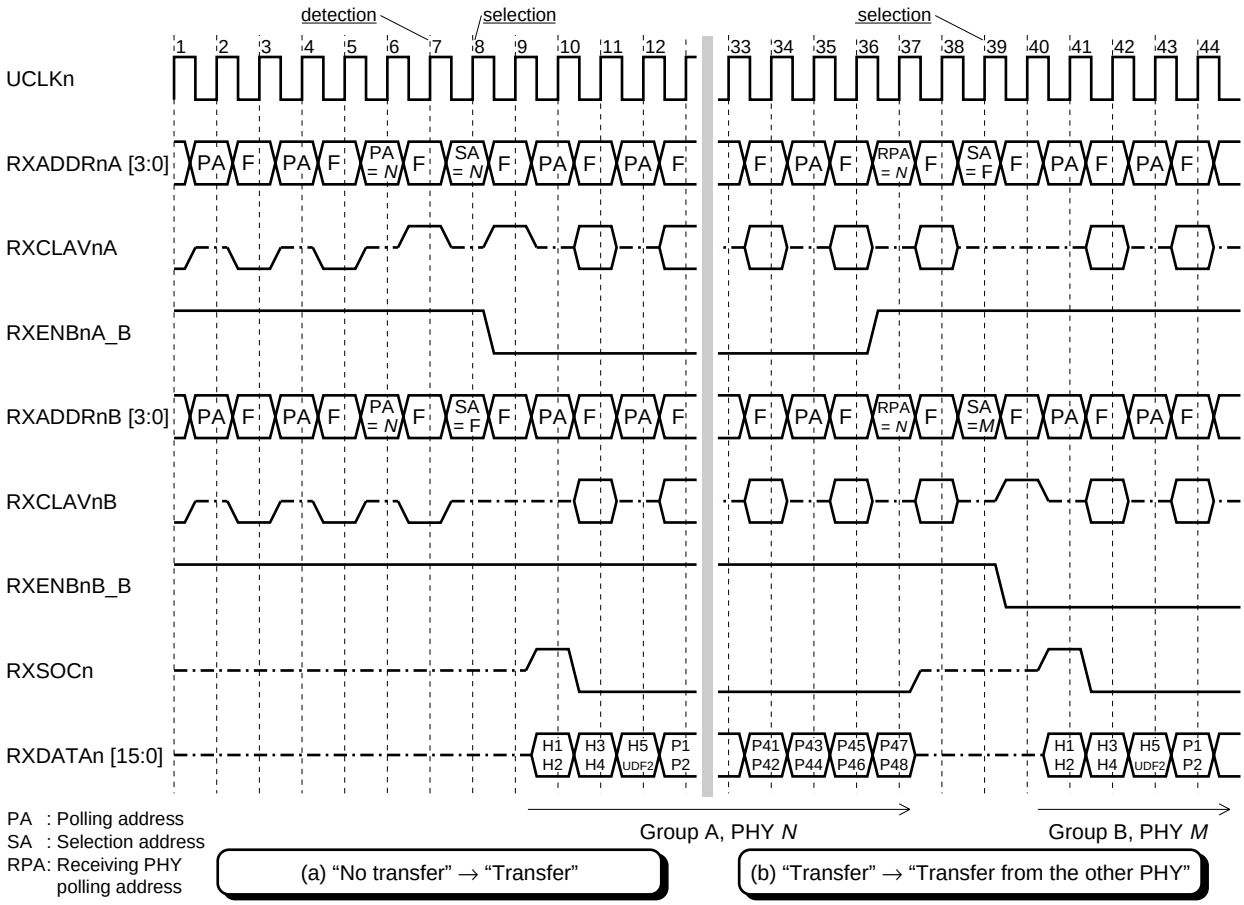
3.8.1 Input port interface

An example of connection is shown below:



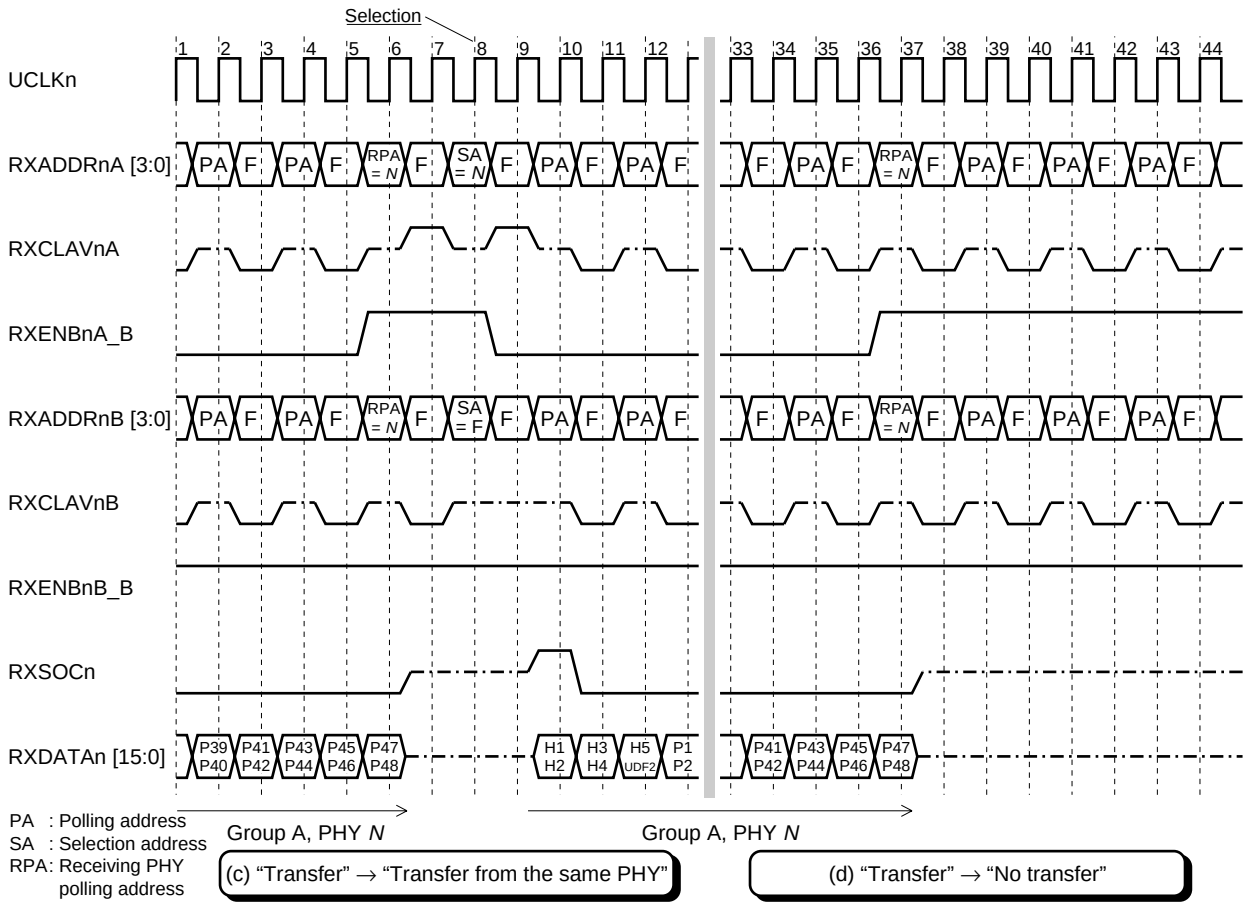
Remark A PHY address consists of 5 bits. Of these, the low-order 4-bits are connected to the μPD98412. Pull up the highest bit. The μPD98412 does not have an RxClk output. Supply UCLKn to the μPD98412 as a UTOPIA clock.

- **Timing chart (X15 handshake mode)**



(a) side: Once cell transfer has been started, RXENBn_B is not deasserted until cell reception is completed.

(b) side: RXENBn_B is always deasserted at the timing of P47/48 (payload 47/48). If RXADDRn [3:0] indicates “Fh” at the timing of P47/48, the RPA and SA timings are delayed by one clock (cell interval: 3 clocks → 4 clocks).



(c) side: If cells are continuously transferred from the same PHY device, RXENBn_B is deasserted once, and selection is performed again.

- **Polling**

The polling address is output at the timing of PA (polling address) in the timing chart. The output sequence of the polling address is determined as follows, depending on the setting of NPC0 through 2 of the UTOPIA configuration registers (UTPCFG0 through 3).

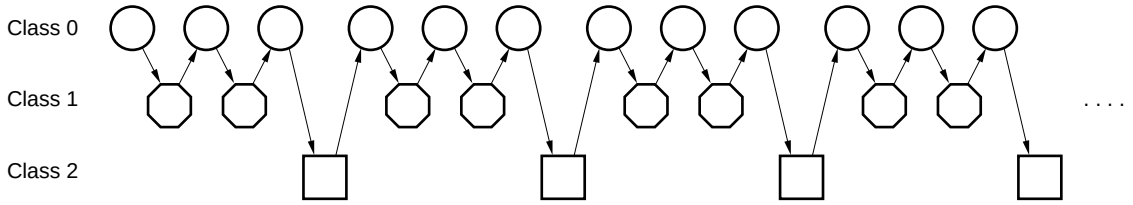
As shown in Figure 3-16, polling classes 0 through 2 have a specific “polling slot”. The polling address is determined by the number of PHY devices allocated to each polling class (NPC0 through 2 of the UTPCFG0 through 3 registers) and the frequency of the polling slot. Figure 3-17 shows a specific example of generating a polling address.

The same value is output as the address of groups A and B. However, the following two rules are applied:

(1) A PHY address that is not assigned to any port configuration register (PT register) is not output. Instead, “Fh” is output.

(2) While the μPD98412 is receiving a cell (RXENBnA_B = “L” or RXENBnB_B = “L”), the PHY address selected for reception is not output to the group that is receiving a cell. Instead, “Fh” is output.

Figure 3-16. Relation between Polling Class and "Polling Slot"

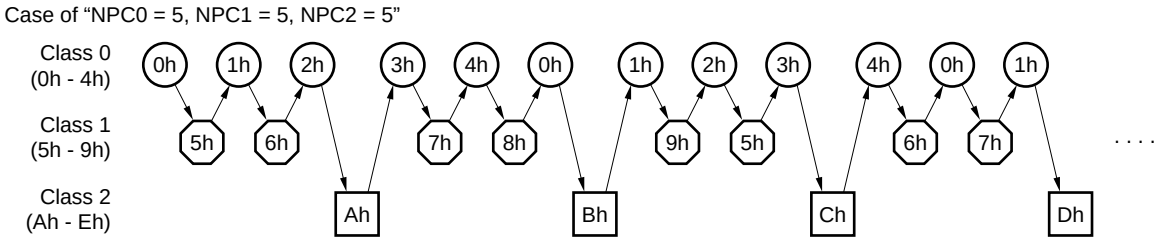


○, ◯, and □ indicate the polling slots corresponding to the respective classes. One cycle consists of six polling slots.

To poll class 0, a polling slot is allocated three times out of six times.

Similarly, to poll class 1, a polling slot is allocated two times of out of six. To poll class 2, a polling slot is allocated once out of six.

Figure 3-17. Generation of Polling Address



The number of the PHY devices allocated to each polling class is determined by using the value set to NPC0 through 2 of the UTPCFG0 through 3 registers. Figure 3-17 describes the example that NPC0, NPC1, and NPC2 are set to 5, respectively.

PHY addresses 0h through 4h are allocated to polling slot of polling class 0 (○ in the above figure). PHY addresses 5h through 9h are allocated to the polling slot of polling class 1 (◯ in the figure), and PHY addresses Ah through Eh are allocated to the polling slot of polling class 2 (□ in the figure). The polling addresses are output in the following sequence:

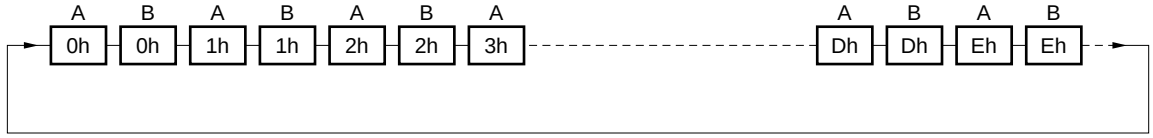
0h, 5h, 1h, 6h, 2h, Ah, 3h, 7h, 4h, ...

- **Receiving PHY polling**

  The PHY device that is receiving a cell is polled at the timing of RPA (receiving PHY polling address) in the timing chart. The same value is output to the group of the PHY devices that are not receiving a cell at the same RPA timing.

- **Selection**

  The selection address is selected by taking the obtained polling result and polling class into consideration. The selection address is output at the timing of SA (selection address) in the timing chart. "Fh" is output to the other group. The status of RXCLAVnA or RXCLAVnB for the selection address is not reflected on the polling result.
  For how the selection address is determined, refer to the description on the 15-PHY polling mode. This mode differs from the 15-PHY polling mode as follows:



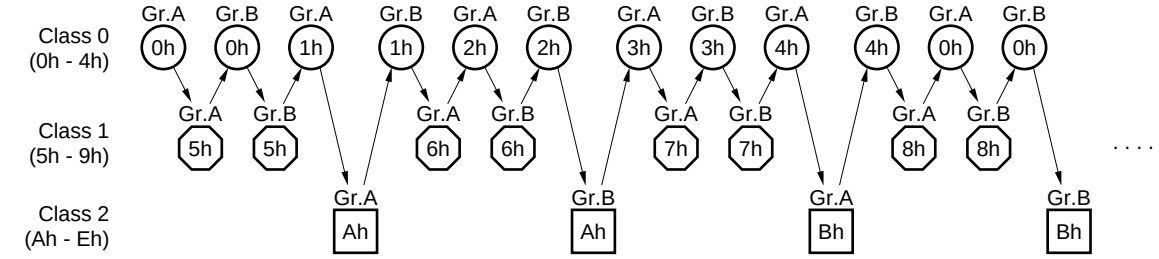
Check sequence)

The PHY devices in groups A and B are checked in the following sequence:

Check start address)

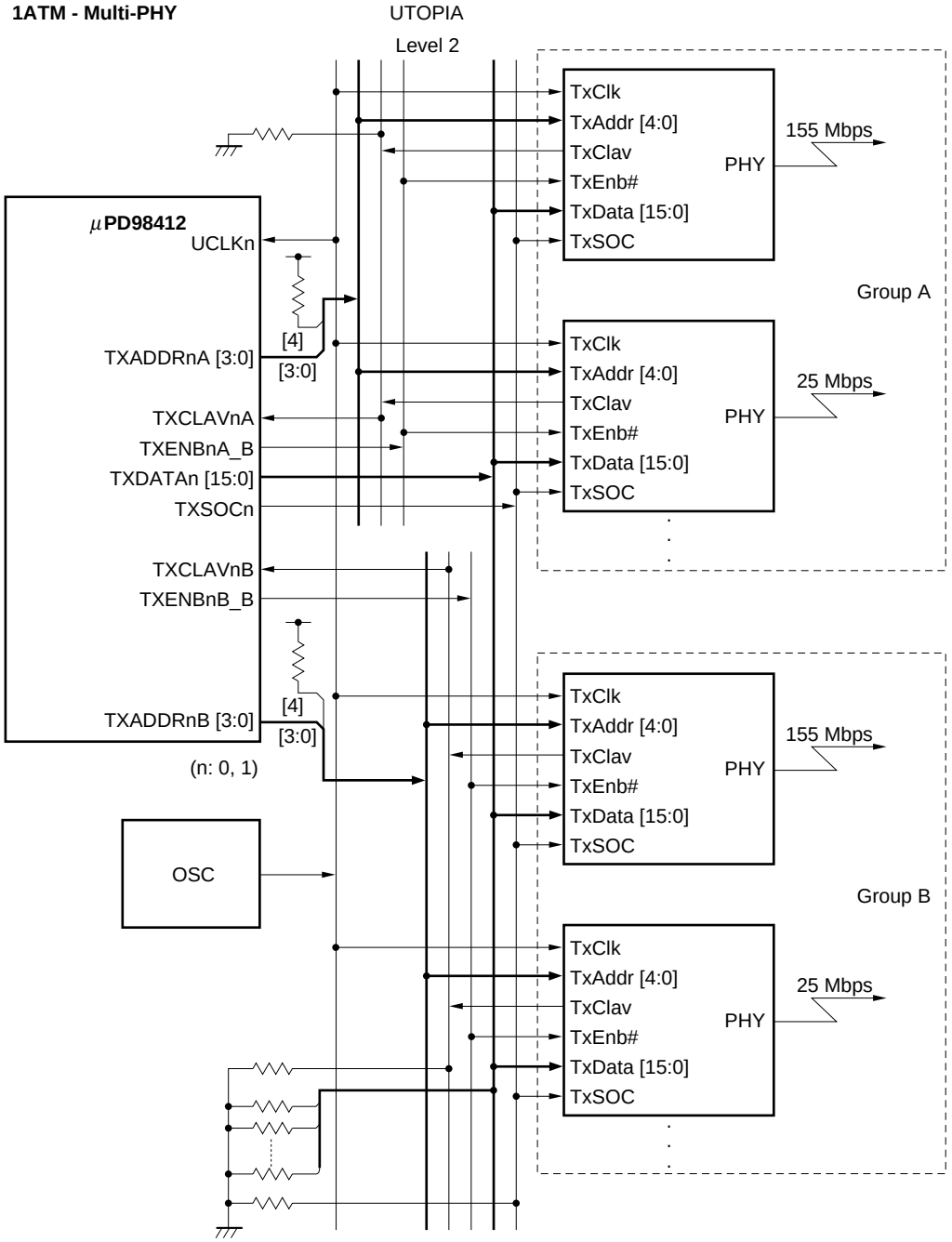
Because there are two groups (A and B), the check start address is selected between the two groups as shown below. In this figure, it is assumed that the same value as in the description of the 15-PHY polling mode is assigned to UTPCFG.

Case of "NPC0 = 5, NPC1 = 5, NPC2 = 5"



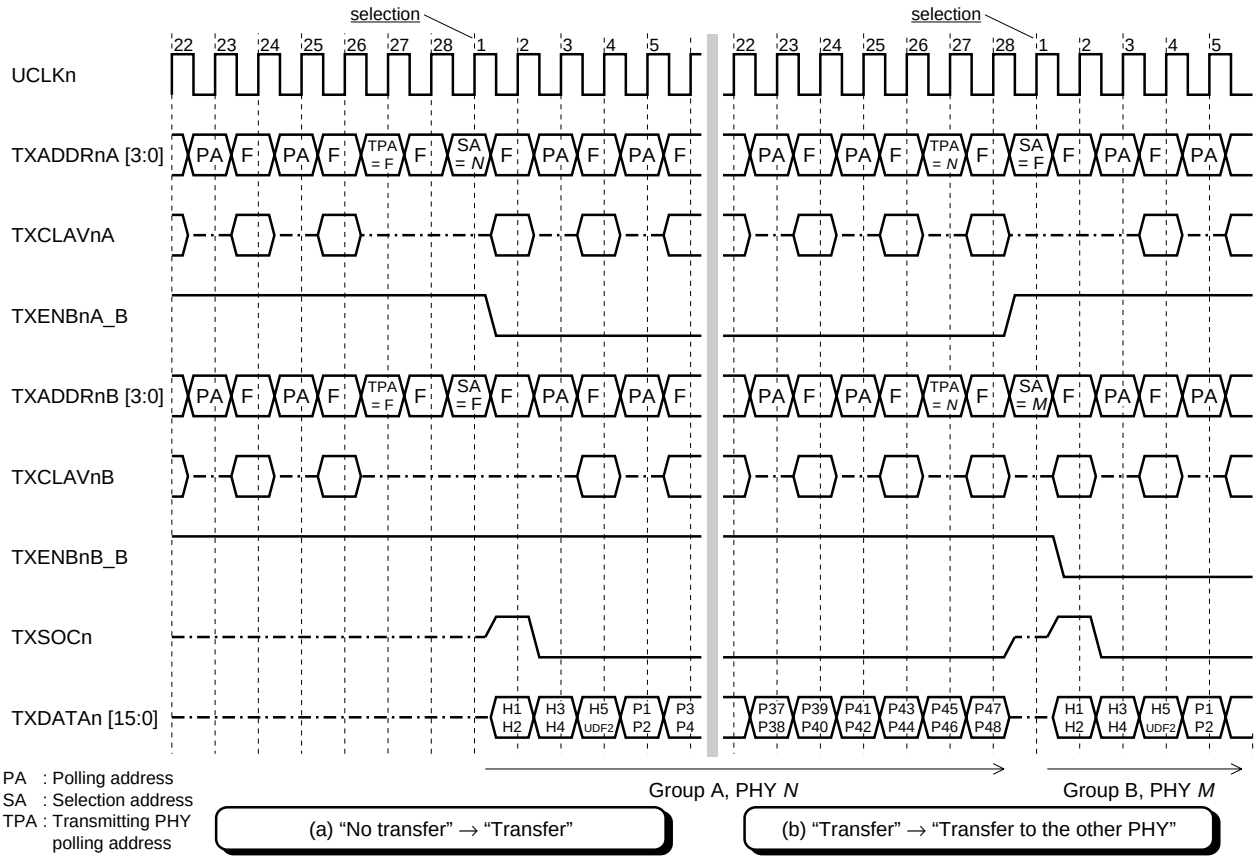
3.8.2 Output port interface

An example of connection is shown below:

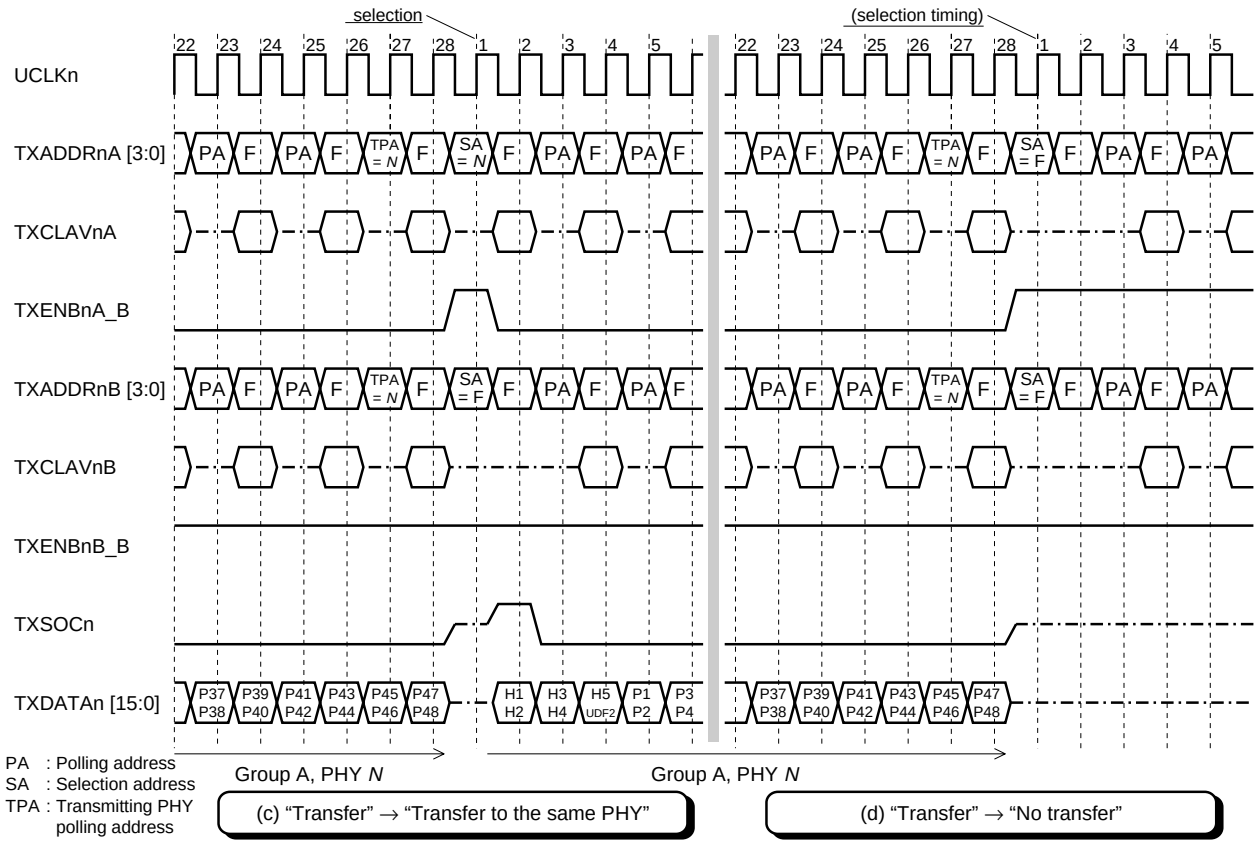


Remark A PHY address consists of 5 bits. Of these, the low-order 4-bits are connected to the μPD98412. Pull up the highest bit. The μPD98412 does not have an TxClk output. Supply UCLKn to the μPD98412 as a UTOPIA clock.

- **Timing chart (Multi-PHY connection mode)**



(a) side: Once cell transfer has been started, TXENBn_B is not deasserted until cell transmission is completed.



(c) side: If cells are continuously transferred from the same PHY device, TXENBn_B is deasserted once, and selection is performed again.

- **Polling**

  The polling address is output at the timing of PA (polling address) in the timing chart. The output sequence of the polling address is the same as that of the input port interface.

- **Transferring PHY polling**

  The PHY device that is transferring a cell is polled at the timing of TPA (transferring PHY polling address) in the timing chart. The same value is output at the same TPA timing for the other group.

  If a cell is not transferred, "Fh" is output at the timing of TPA.

- **Selection**

  The selection address is output at the timing of SA (selection address) in the timing chart. The value "Fh" is output at the same SA timing for the other group.

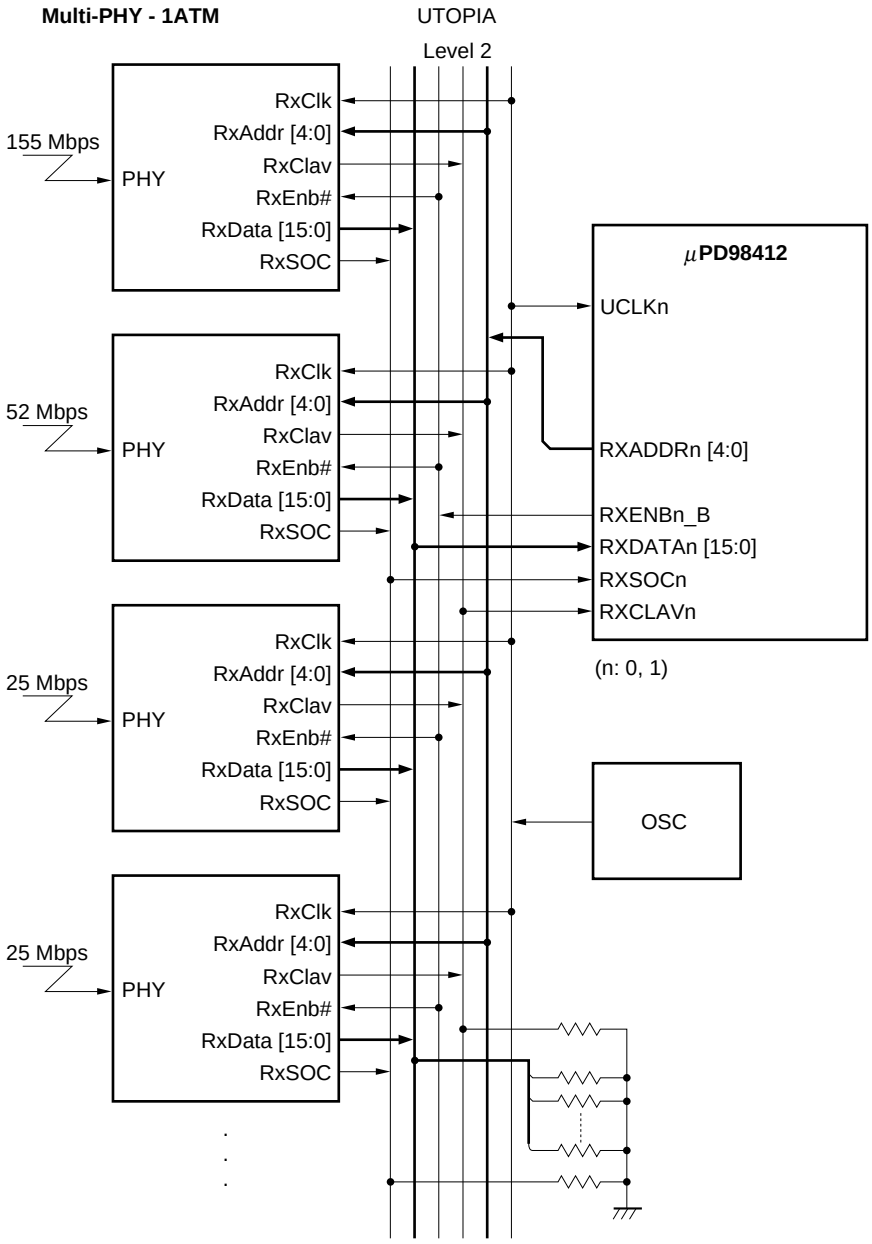
  TXCLAVnA and TXCLAVnB for the selection address are not reflected on the polling result.

3.9 1-Group Weighted Polling Mode

The 1-group weighted polling mode supports up to 30 I/O ports with the 16-bit UTOPIA interfaces, by means of multiple PHY connection. The multiple PHY ports connected to one UTOPIA interface can be integrated into one group and controlled.

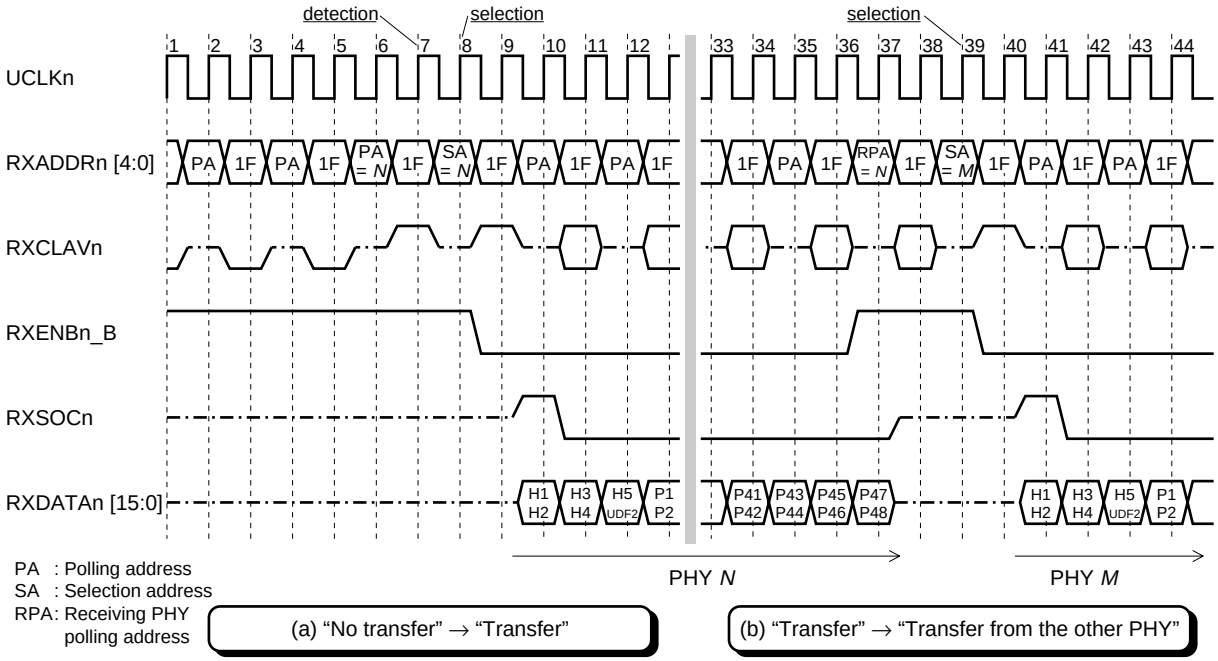
3.9.1 Input port interface

An example of connection is shown below:



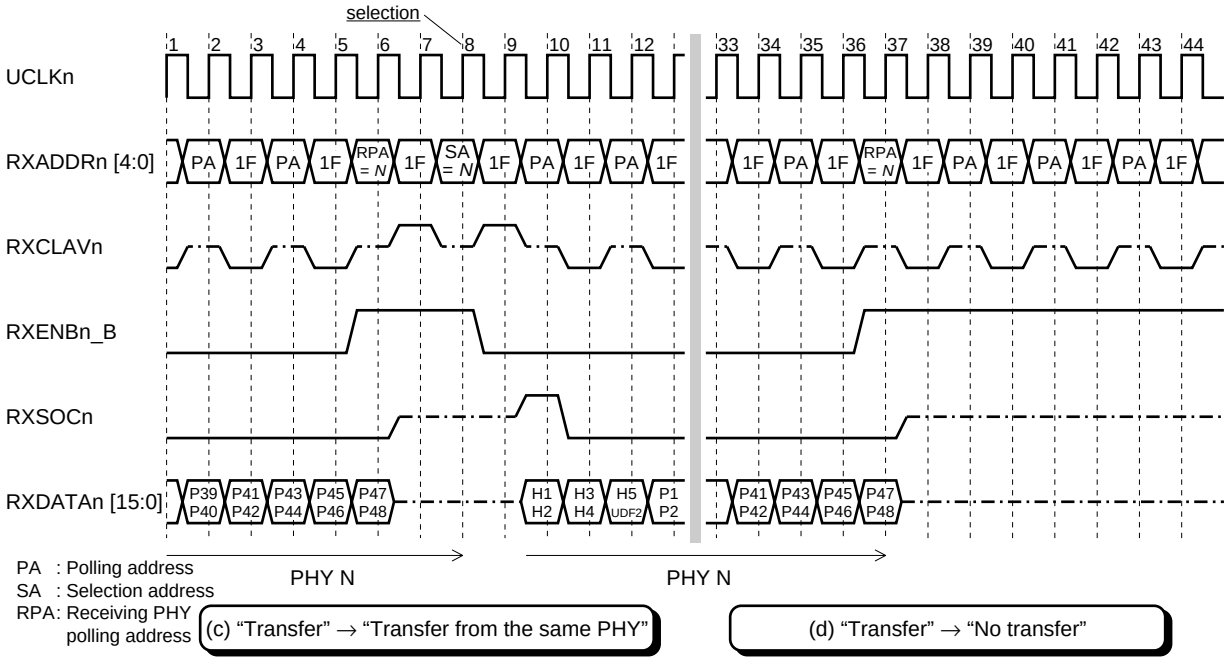
Remark The μPD98412 does not have an RxClk output. Supply UCLKn to the μPD98412 as a UTOPIA clock.

- **Timing chart (X15 handshake mode)**



(a) side: Once cell transfer has been started, RXENBn_B is not deasserted until cell reception is completed.

(b) side: RXENBn_B is always deasserted at the timing of P47/48 (payload 47/48). When RXADDRn [4:0] indicates "1Fh" at the timing of P47/48, the RPA and SA timings are delayed by one clock (cell interval: 3 clocks → 4 clocks).



(c) side: If cells are continuously transferred from the same PHY device, RXENBn_B is deasserted once, and selection is performed again.

- **Polling**

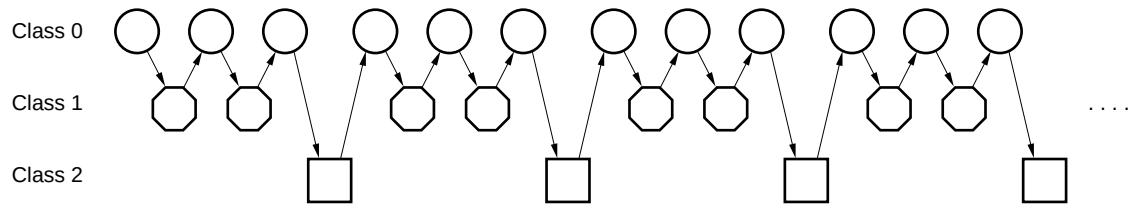
The polling address is output at the timing of PA (polling address) in the timing chart. The output sequence of the polling address is determined as follows, depending on the setting of NPC0 through 2 of the UTOPIA configuration registers.

As shown in Figure 3-18, polling classes 0 through 2 have a specific "polling slot". The polling address is determined by the number of PHY devices allocated to each polling class (NPC0 through 2 of the UTPCFG0 through 3 registers) and the frequency of the polling slot. Figure 3-19 shows a specific example of generating a polling address. However, the following two rules are applied:

(1) The PHY address that is not set to any port configuration register (PT register) is not output. Instead, "1Fh" is output.

(2) While the μPD98412 receives a cell (RXENBn_B = "L"), The PHY address selected for reception is not output to the group. Instead, "1Fh" is output.

Figure 3-18. Relation between Polling Class and "Polling Slot"

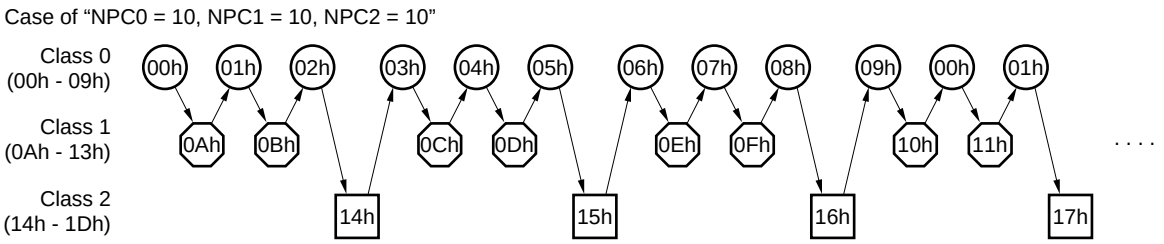


○, ◯, and □ indicate the polling slots corresponding to the respective classes. One cycle consists of six polling slots.

To poll class 0, a polling slot is allocated three times out of six times.

Similarly, to poll class 0, a polling slot is allocated two times of out of six. To poll class 2, a polling slot is allocated once out of six.

Figure 3-19. Generation of Polling Address



The number of the PHY devices allocated to each polling class is determined by using the value set to NPC0 through 2 of the UTPCFG0 through 3 registers. Figure 3-19 describes the example that NPC0, NPC1, and NPC2 are set to 10, respectively.

To polling slot of polling class 0 (○ in the above figure), PHY addresses 00h through 09h are allocated. PHY addresses 0Ah through 13h are allocated to the polling slot of polling class 1 (◯ in the figure), and PHY addresses 14h through 1Dh are allocated to the polling slot of polling class 2 (□ in the figure). The polling addresses are output in the following sequence:

00h, 0Ah, 01h, 0Bh, 02h, 14h, 03h, 0Ch, 04h, ...

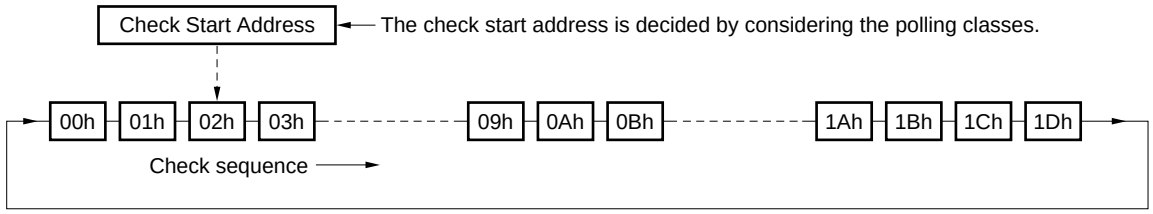
- **Receiving PHY polling**

  The PHY device that is receiving a cell is polled at the timing of RPA (receiving PHY polling address) in the timing chart.

- **Selection**

The selection address is selected by taking the obtained polling result and polling class into consideration. The selection address is output at the timing of SA (selection address) in the timing chart. The status of RXCLAVn for the selection address is not reflected on the polling result.

The selection address is determined by the following selection algorithm.
In the 1-group weighted polling mode, first the polling result is checked starting from the check start address that has been determined by taking a polling class into consideration, in order to select the PHY device that is ready for transfer.



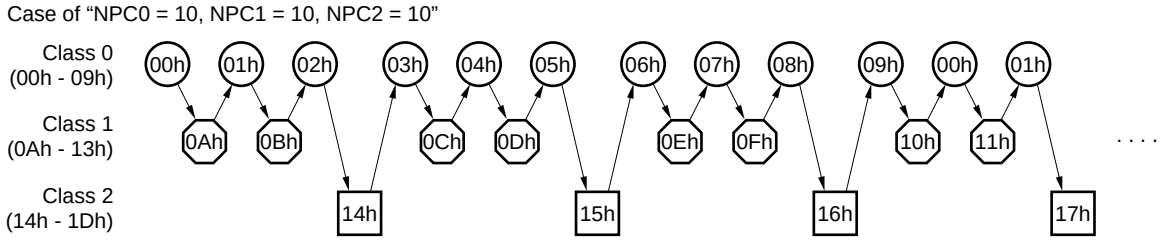
For example, if the polling result is as shown below, and if the polling result is checked starting from PHY address “02h” as shown above, the PHY device with PHY address “07h” is selected.

PHY address	00h	01h	02h	03h	04h	05h	06h	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh
RxClav	L	L	L	L	L	L	L	H	H	H	L	L	L	H	H	L

PHY address	10h	11h	12h	13h	14h	15h	16h	17h	18h	19h	1Ah	1Bh	1Ch	1Dh
RxClav	L	H	H	H	L	L	L	H	L	H	H	L	L	L

Next, how the check start address is determined is explained.

The μPD98412 uses a polling class to determine the check start address. To simplify explanation, a case where ten PHY devices are allocated to each class is considered.



- Setting of UTPCFG register

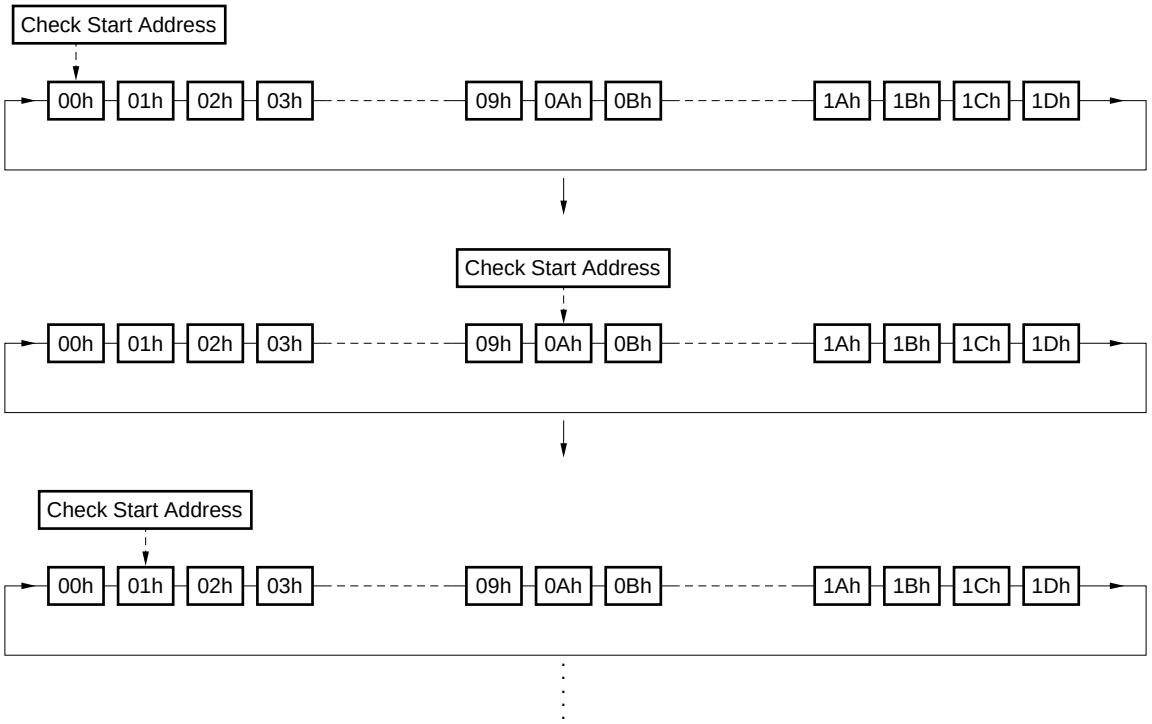
  NPC0 = 10, NPC1 = 10, NPC2 = 10

- PHY address

  If the UTPCFG register is set as shown above, the PHY addresses are allocated to each polling class as follows:

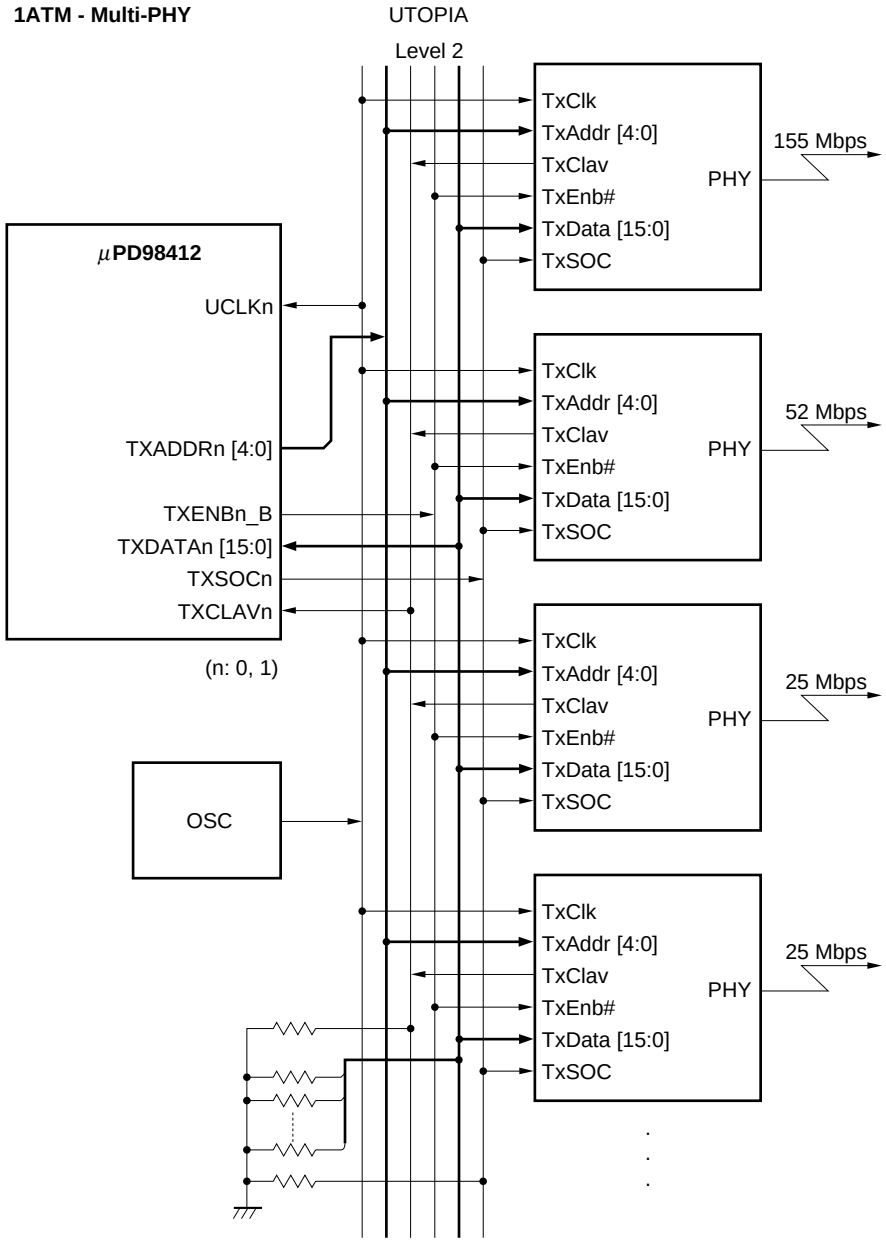
  Class 0: 00h through 09h
  Class 1: 0Ah through 13h
  Class 2: 14h through 1Dh

With the μPD98412, the check start address of the polling result changes “00h” → “0Ah” → “01h” → “0Bh”, and so on, in accordance with the above figure.



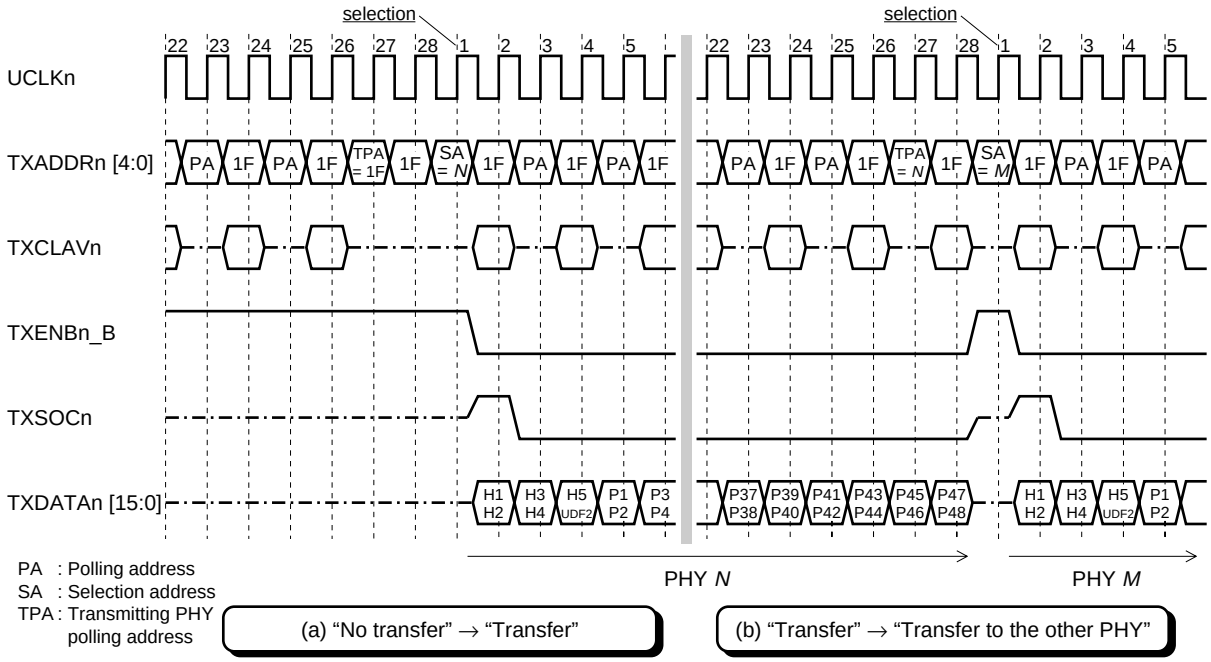
3.9.2 Output port interface

An example of connection is shown below:

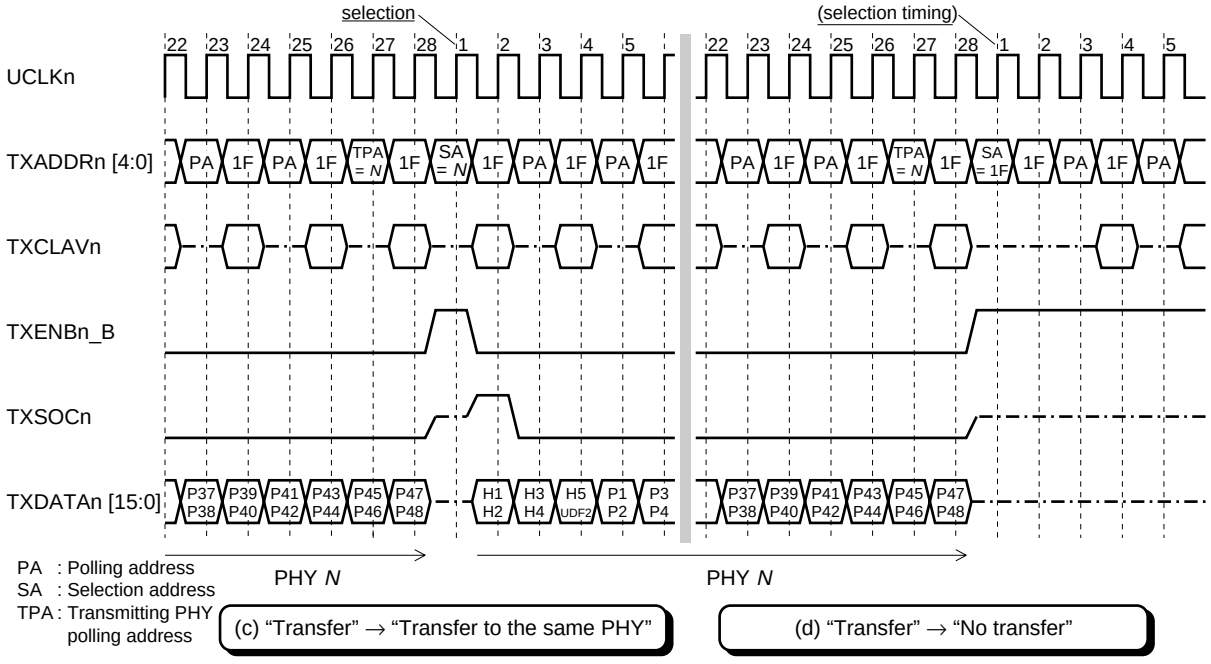


Remark The μPD98412 does not have an TxClk output. Supply UCLKn to the μPD98412 as a UTOPIA clock.

- **Timing chart (Multi-PHY connection mode)**



(a) side: Once cell transfer has been started, TXENBn_B is not deasserted until cell transmission is completed.



(c) side: If cells are continuously transferred from the same PHY device, TXENBn_B is deasserted once, and selection is performed again.

- **Polling**

  The polling address is output at the timing of PA (polling address) in the timing chart. The output sequence of the polling address is the same as that of the input port interface.

- **Transferring PHY polling**

  The PHY device that is transferring a cell is polled at the timing of TPA (transferring PHY polling address) in the timing chart.

  If a cell is not transferred, “1Fh” is output at the timing of TPA.

- **Selection**

  The selection address is output at the timing of SA (selection address) in the timing chart. TXCLAVn for the selection address is not reflected on the polling result.

3.10 Request to PHY Device (Input Port)

When two or more PHY devices are connected to one UTOPIA interface, a PHY device, even if it is ready to transfer a cell, may be kept waiting to transfer the cell to the μPD98412. This happens when the μPD98412 receives a cell from another PHY device connected to the same UTOPIA interface before the μPD98412 receives a cell from that PHY device. If the time for which the PHY device is kept waiting exceeds the limit of cell buffering of the PHY device, the cell of the PHY device is lost.

The maximum cell transfer wait time of the μPD98412 is determined as follows, by the effective throughput of the UTOPIA interface, polling mode, polling class, and the number of PHY devices connected. Therefore, connect the PHY devices that can buffer cells at least for the maximum wait time calculated by the following expression for the μPD98412.

(Expression)

15-PHY polling mode

$$T_{Wn} = \left(\frac{15}{26} + k_n \times \mathrm{NPC}n \right) \times T$$

Multiplexed status polling mode

$$T_{Wn} = \left(\frac{8}{13} + k_n \times \mathrm{NPC}n \right) \times T$$

2-group weighted polling mode

$$T_{Wn} = \left(\frac{k_n \times \mathrm{NPC}n}{13} + 2 \times k_n \times \mathrm{NPC}n \right) \times T$$

1-group weighted poling mode

$$T_{Wn} = \left(\frac{k_n \times \mathrm{NPC}n}{13} + k_n \times \mathrm{NPC}n \right) \times T$$

The meaning of each symbol is as follows:

- n : Polling class (0 to 2)
- T_{Wn} : Maximum wait time of PHY device belonging to polling class n [s]
- k_n : Coefficient of polling class n
  - $k_0 = 2$
  - $K_1 = 4$
  - $K_2 = 6$
- $NPCn$: Number of PHY devices belonging to polling class n
  (Refer to the description on the UTPCFG register.)
- T : Transfer time per cell calculated by the following expression [s]:

$$T = \left(\frac{8\ [\mathrm{bit}] \times 53\ [\mathrm{byte}]}{(\text{Effective throughput per UTOPIA interface[bps]})} \right)$$

(Example)

<<Condition>>

Two 155-Mbps PHY devices, three 52-Mbps PHY deices, and six 25-Mbps PHY devices are connected to a UTOPIA interface in the 1-group weighted polling mode under the following clock frequency condition.

UCLK = 50 MHz, SWCLK = 33 MHz

It is assumed that the 155-Mbps PHY devices, 52-Mbps PHY devices, and 25-Mbps PHY devices are allocated to polling classes 0, 1, and 2, respectively, and that NPC*n* is set as follows:

NPC0 = 2, NPC1 = 3, NPC2 = 6

<<Expression>>

First, the transfer time (*T*) per cell is calculated as follows:

$$T = \frac{8 \times 53}{\min\left(50 \times 10^6 \times 8 \times 53/28,\ 33 \times 10^6 \times 8 \times 53/22\right)}$$
$$= 0.67 \times 10^{-6} \text{ [sec]}$$

The maximum wait time of the PHY devices in polling class 0 is as follows:

$$T_{W0} = \left(\frac{k_0 \times \text{NPC0}}{13} + k_0 \times \text{NPC0} \right) \times T$$
$$= \left(\frac{2 \times 2}{13} + 2 \times 2 \right) \times 0.67 \times 10^{-6}$$
$$= 2.9 \times 10^{-6} \text{ [sec]}$$

The buffer size of the PHY devices that can buffer cells for the maximum wait time can be calculated by the following expression. This is because the 155-Mbps PHY devices receive a cell every 2.8 μs.

$$\text{(buffer size)} = \frac{2.9 \times 10^{-6}}{2.8 \times 10^{-6}} = 1.04 \approx 2$$

Similarly, the maximum wait time and PHY buffer size of the 52-Mbps PHY devices are calculated as follows (the 52-Mbps PHY devices receive a cell every 8.5 μs):

$$T_{W1} = \left(\frac{4 \times 3}{13} + 4 \times 3 \right) \times 0.67 \times 10^{-6}$$
$$= 8.7 \times 10^{-6}$$
$$\text{(buffer size)} = \frac{8.7 \times 10^{-6}}{8.5 \times 10^{-6}} = 1.02 \approx 2$$

The maximum wait time and PHY buffer size of the 25-Mbps PHY devices are calculated as follows (the 25-Mbps PHY devices receive a cell every 16.9 μs):

$$T_{W2} = \left(\frac{6 \times 6}{13} + 6 \times 6 \right) \times 0.67 \times 10^{-6}$$
$$= 26.0 \times 10^{-6}$$
$$\text{(buffer size)} = \frac{26.0 \times 10^{-6}}{16.9 \times 10^{-6}} = 1.54 \approx 2$$

(Caution)

A cell loss may occur in a PHY device depending on the traffic characteristics of the PHY device. It is therefore not absolutely guaranteed that a cell loss will not occur in a PHY device that satisfies the above requirements.

In practice, add the following buffer size as a margin to the above requirements.

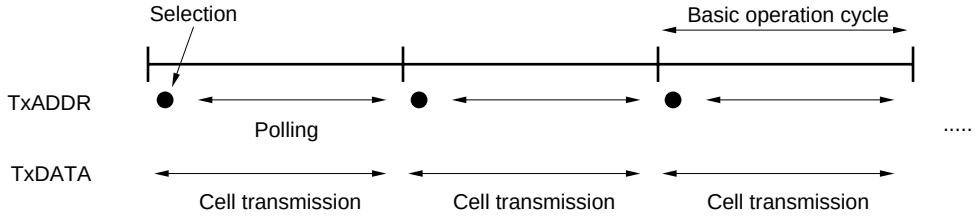
- Buffer for one cell that is kept waiting to be transferred to the μPD98412
- Buffer necessary depending on the μser system

3.11 Request to PHY Device (Output Port)

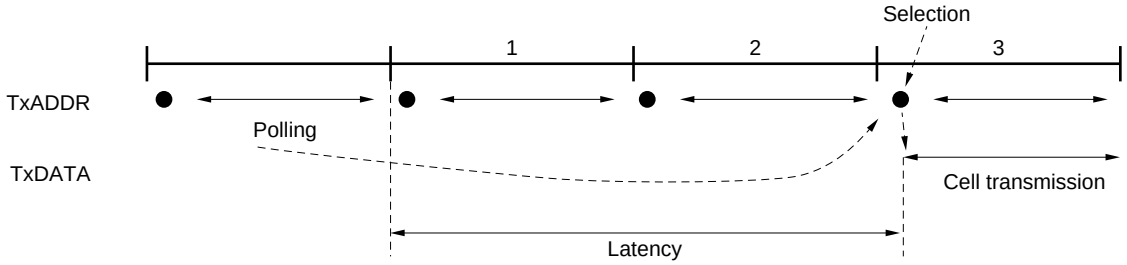
There is a delay called latency between the time at which the μPD98412 detects that the PHY device is ready to receive a cell and the time at which the μPD98412 transmits a cell. This section explains latency and the limitations due to latency.

3.11.1 Latency

A basic operation cycle of the 8-bit output UTOPIA interface of the μPD98412 consists of 54 UTOPIA clock pulses, and that of the 16-bit UTOPIA interface consists of 28 UTOPIA clock pulses. In a basic operating cycle, polling, selection (selecting a PHY device to/from which a cell is transferred), and transfer of one cell are executed.



The flow shown below illustrates the process of cell transfer (polling → selection → cell transfer). As shown in the figure, the result of polling is reflected in the selection, and a delay of several cycles is generated before the cell is actually transferred. This delay is called latency. In the figure, the latency is 3.



This latency is generated because the μPD98412 performs the following processing after it has received the result of polling and before it transmits a cell.

Processing 1:

The cell to be transmitted is determined based on the following information:

- Result of polling all the PHY devices connected to the UTOPIA interface
- Whether shaping and continuous output are enabled
- Priority of port
- WFQ

Processing 2:

The cell to be transmitted is extracted from the buffer and stored in Q-FIFO (internal output FIFO buffer of μPD98412).

The latency period differs as follows depending on the UTOPIA interface and polling mode to be used:

UTOPIA I/F	Maximum Latency
8-bit UTOPIA I/F, 12-PHY polling mode	2 basic operation cycles
8-bit UTPIA I/F, 15-PHY polling mode	3 basic operation cycles
16-bit UTOPIA I/F	4 basic operation cycles

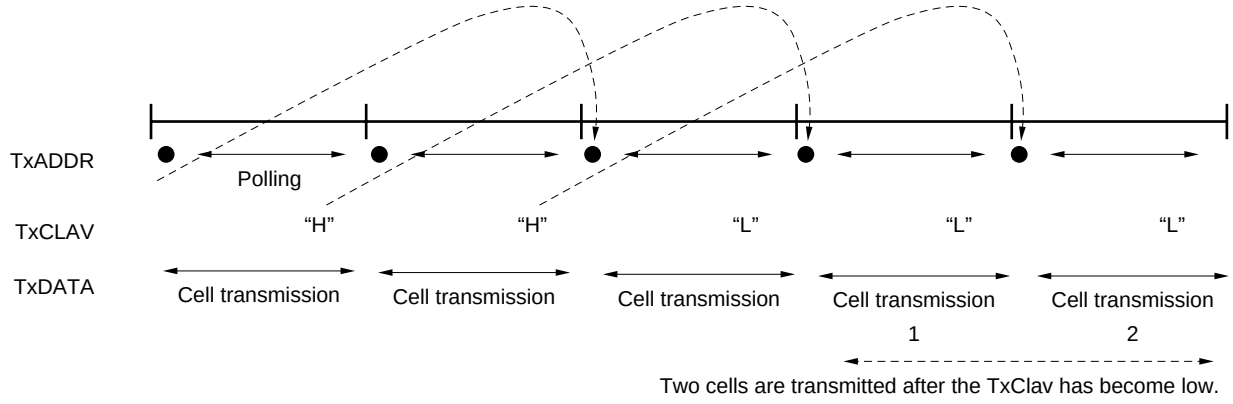
This table shows the value of the maximum latency. Because the polling circuit that performs processing 1 operates asynchronously with the switching circuit that performs processing 2, a cell may be transmitted with the shorter latency depending on the timing between these circuits.

3.11.2 Limitations related to PHY device connection

The way TxClav is controlled by the PHY devices connected to the μPD98412 must satisfy certain conditions because of the latency. This section explains these conditions. When using the 12-PHY polling mode of the 8-bit UTOPIA interface, a condition due to the timing of polling must be also satisfied, and this condition is also explained.

(1) Condition due to latency

Suppose the μPD98412 continuously transfers cells to a specific PHY device. Even if the PHY device deasserts TxClav, the μPD98412 cannot stop cell transmission immediately, and it transmits two cells to the PHY device after the PHY device has deasserted TxClav. The following figure shows an example with a latency of 3.



In this example, therefore, the PHY device must assert TxClav only when it is ready to receive three cells or more. The relation between the number of cells that can be received and the status of TxClav differs depending on the UTOPIA interface and polling mode used.

- 8-bit UTOPIA I/F, 12-PHY polling mode ... 2 cells (with limitation explained in (2) below applied)
- 8-bit UTOPIA I/F, 15-PHY polling mode ... 3 cells
- 16-bit UTOPIA I/F ... 4 cells

(2) Condition due to polling timing

In the 12-PHY polling mode of the 8-bit UTOPIA interface, the timing of polling the PHY device that is transmitting a cell differs from the other cases.

- 8-bit UTOPIA I/F, 12-PHY polling mode:
  Polling is performed immediately after transmission of P18 (18th octet of payload).
- Other modes:
  Polling is performed immediately after P44 (44th octet of payload).

The timing to poll the PHY device that is transferring a cell in the 12-PHY polling mode of the 8-bit UTOPIA interface is intended to reduce the latency. This timing is not the standard timing of UTOPIA Level2. When using this interface, therefore, PHY devices that satisfy one of the following conditions must be connected.

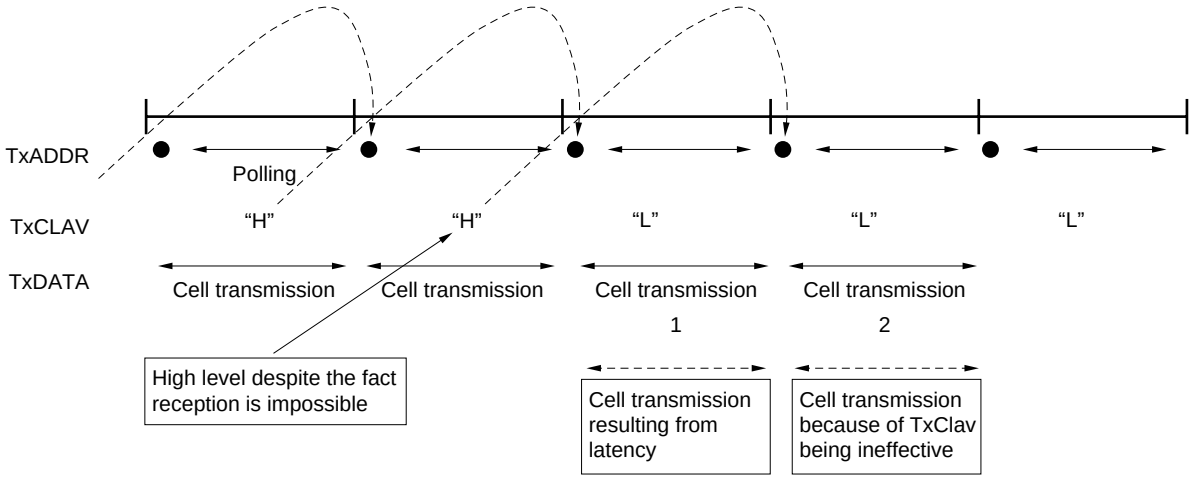
Condition 1:

The devices must be able to output a valid TxClav in response to polling immediately after transmission of P18 (“valid TxClav” means that TxClav is asserted only when the PHY device is ready to receive two or more cells as explained in (1) above, and that TxClav is deasserted if the device is ready to receive less than two cells).

Condition 2:

The PHY device must be ready to receive three cells or more (two cells explained in (1) + one cell) when TxClav is asserted.

Condition 2 applies to a PHY device that cannot output a valid TxClav in response to polling immediately after transmission of P18. Even if the device outputs “H” to TxClav in a state where it cannot receive a cell, the device can receive a cell if it is enabled to receive one more cell in addition to the given number of cells the device can receive.



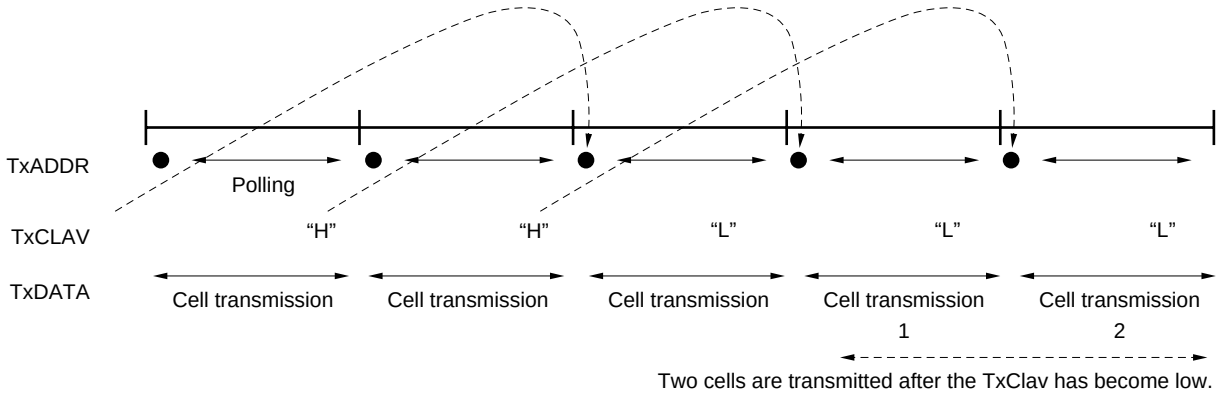
The conditions of the PHY device explained in (1) and (2) are as follows:

UTOPIA I/F, Polling Mode			Number of Cells Receivable When TxClav Is Asserted
8-bit	12-PHY polling mode	PHY device satisfying condition 1 in (2)	2 cells or more
		PHY device satisfying condition 2 in (2)	3 cells or more
	15-PHY polling mode		3 cells or more
16-bit			4 cells or more

3.11.3 Continuous output inhibit mode

To relax the conditions required of the PHY devices explained in **3.10 Request to PHY Device (Input Port)**, the μPD98412 supports a continuous output inhibit mode. In this mode, cells are not continuously transferred to the same PHY device. Therefore, the condition regarding the number of cells that can be received by a PHY device when TxClav is asserted can be relaxed. In the continuous output inhibit mode, the number of times output is suppressed can be specified. The following figure shows the conditions of the PHY device in the continuous output mode and continuous output inhibit mode (output is suppressed once or twice) with a latency of 3.

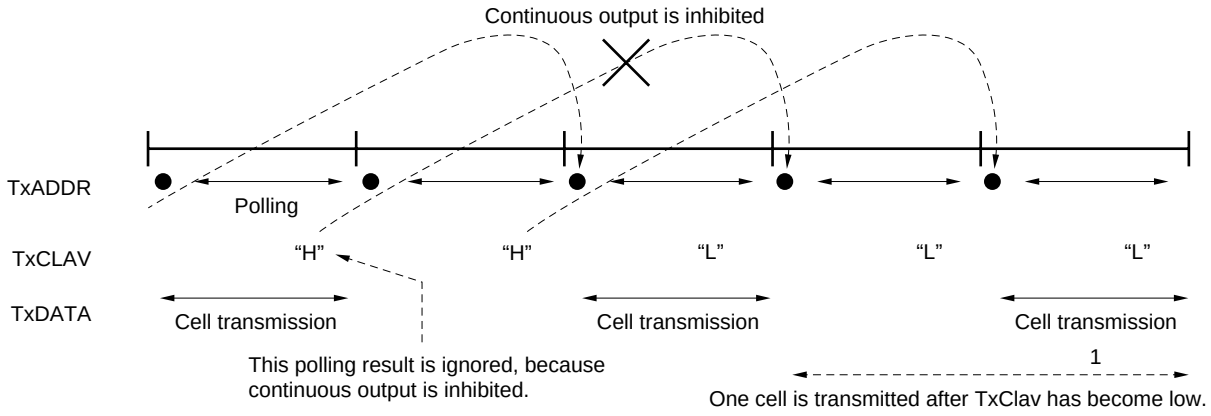
(1) Continuous output mode



The PHY device must assert TxClav when it is ready to receive three cells or more.

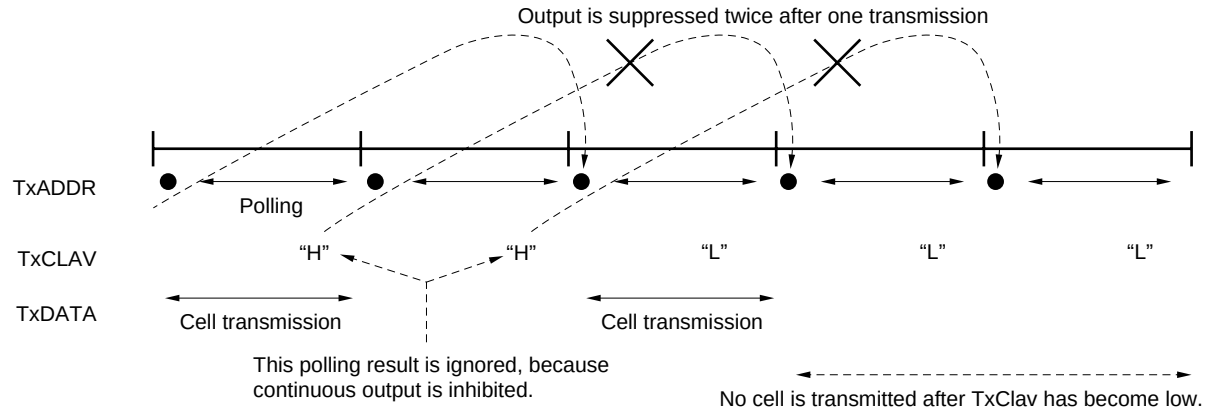
(2) Continuous output inhibit mode

(a) If output is suppressed once



The PHY device can assert TxClav if it is ready to receive two or more cells.

(b) If output is suppressed twice



The PHY device can assert TxClav if it is ready to receive at least one cell.

3.12 Header Translation

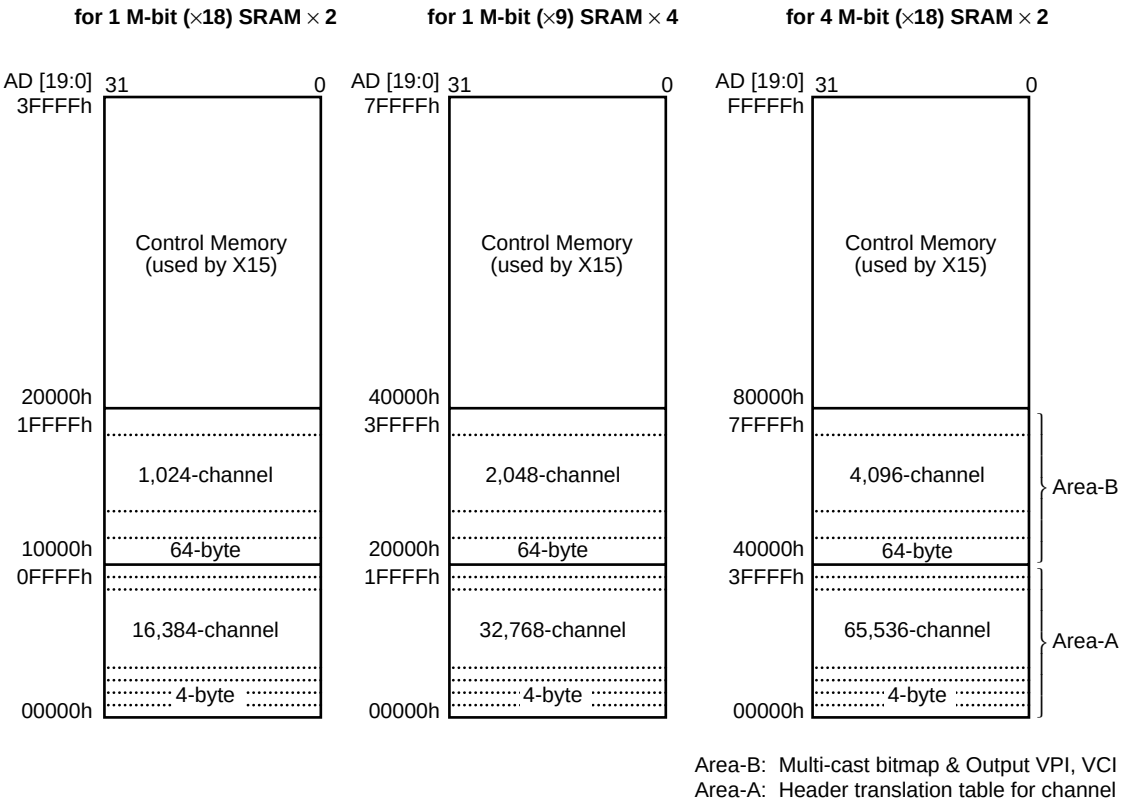
The μPD98412 translates headers in accordance with the header translation table (HTT) created in the external SRAM. Headers are translated when a cell is input in the single-cast mode, and when a cell is input or output in the multi-cast mode. The HTT is created by an external microprocessor when connection is made.

The format of the HTT and header translation procedure are explained below.

3.12.1 HTT (Header Translation Table) memory map

The HTT (Header Translation Table) is located in the HTT & control memory as Area-A and Area-B. The following three types of memories can be connected to the μPD98412 as the HTT & control memory.

Figure 3-20. HTT & Control Memory Map



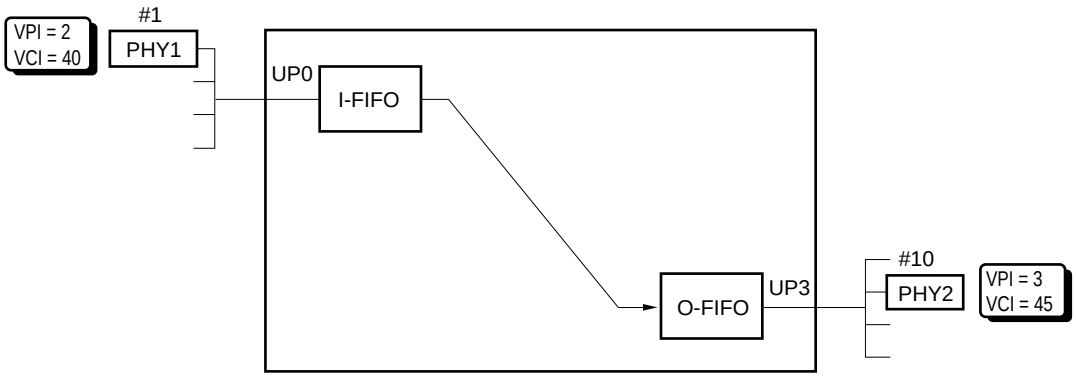
Remarks 1. The addresses shown in this figure are those accessed by the microprocessor.

2. The μPD98412 divides address AD[19:0] from the microprocessor by four and access the HTT & control memory in word units where one word consists of 4 bytes. Therefore, HTA [17:0] output an address that is divided by four.

3.12.2 General

This section outlines the processing of cell switching and header translation. First, an example where a cell input from logical input port #1 is output from logical output port #10 is given.

Figure 3-21. Example of Single Cast

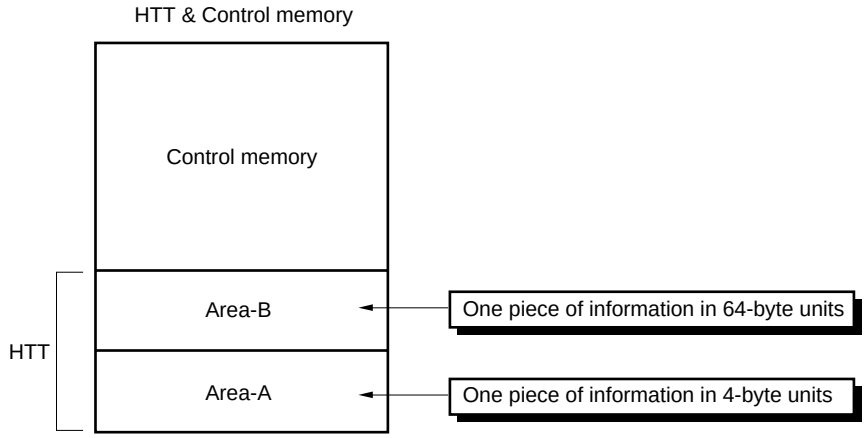


#n : Logical port number
UPn : UTOPIA port
PHYn : PHY (n indicates a PHY number.)

At this time, the μPD98412 must have the information “the cell input from logical input port #1 is output to logical output port #10”. It is the HTT (header translation table) that provides this information. The HTT is organized in the HTT & control memory, and is divided into Area-A and Area-B depending on the usage.

- Area-A ... Area used in both single cast and multi-cast modes
- Area-B ... Area used only in multi-cast mode

Figure 3-22. HTT (Header Translation Table)



Information at the output side is stored in the HTT. Information at the input side is used to calculate the addresses of the HTT area in which the information at the output side is stored. Therefore, the information at the output side is obtained based on the information at the input side.

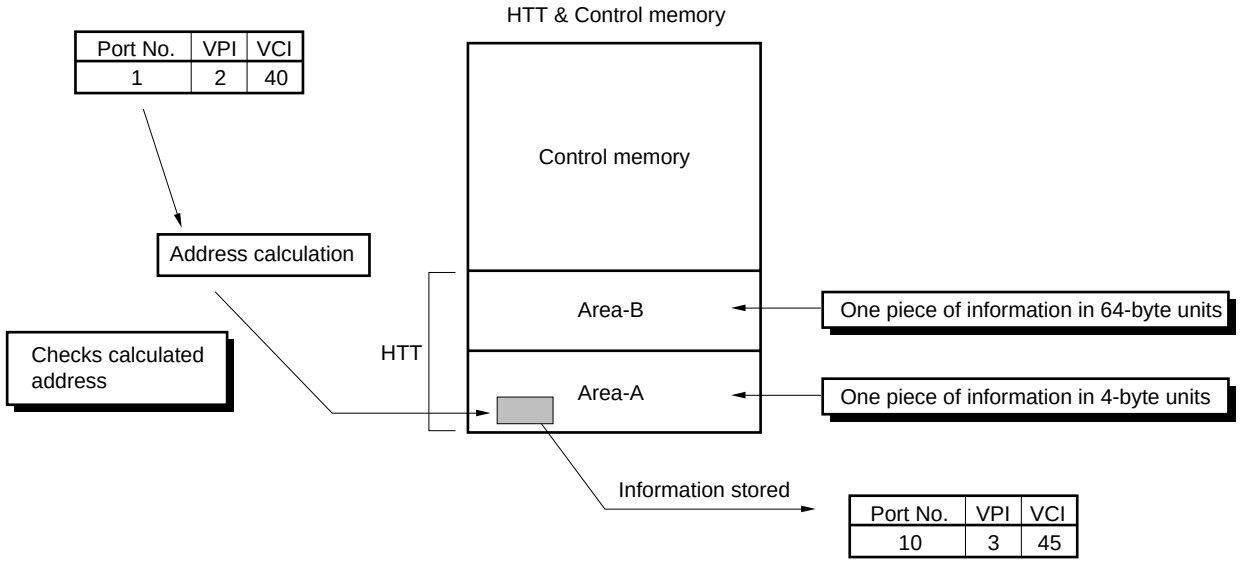
Information at output side

Port No.	VPI	VCI
10	3	45

Information at input side

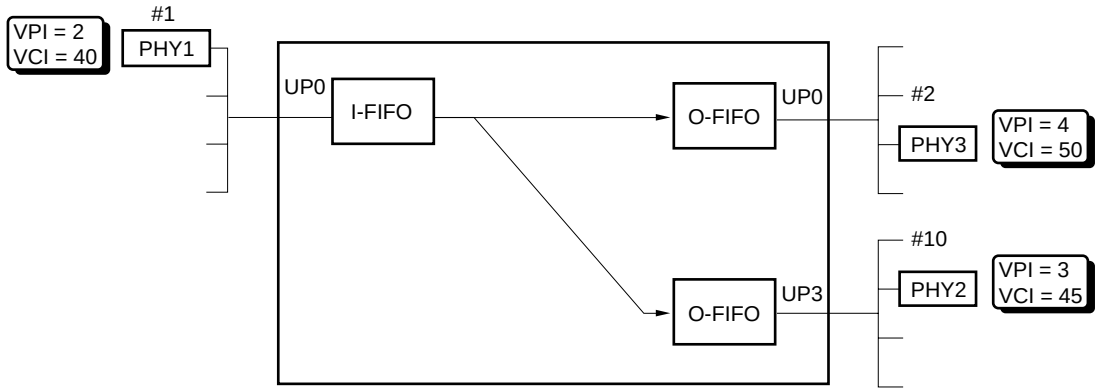
Port No.	VPI	VCI
1	2	40

Figure 3-23. Flow of Header Translation Information in Single Cast Mode



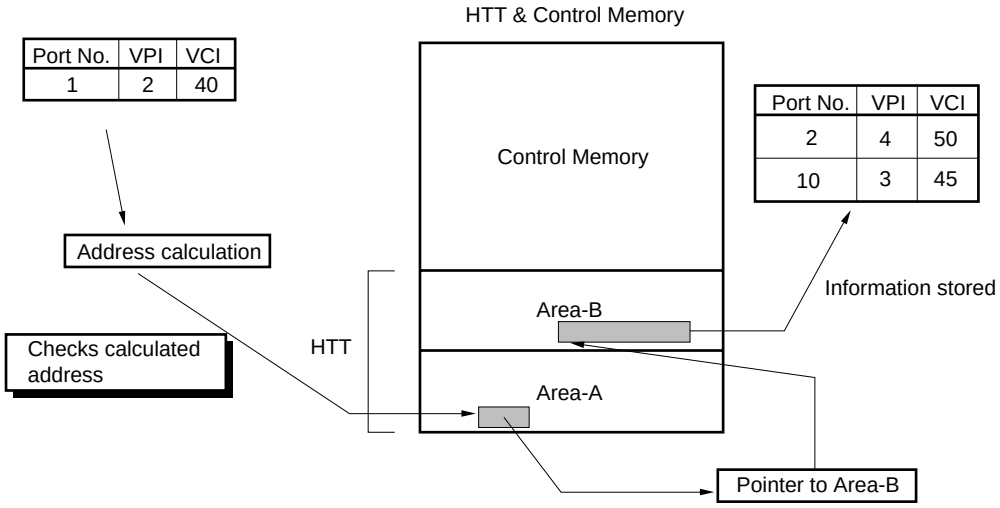
Area-B is also used in the multi-cast mode. At this time, a pointer that is used to access Area-B is stored in Area-A, and information at the output side is stored in Area-B. Figures 3-24 and 3-25 show this.

Figure 3-24. Example of Multi-Cast



#n : Logical port number
UPn : UTOPIA port
PHYn : PHY (n indicates a PHY number.)

Figure 3-25. Flow of Header Translation Information in Multi-Cast Mode



3.12.3 Format of HTT

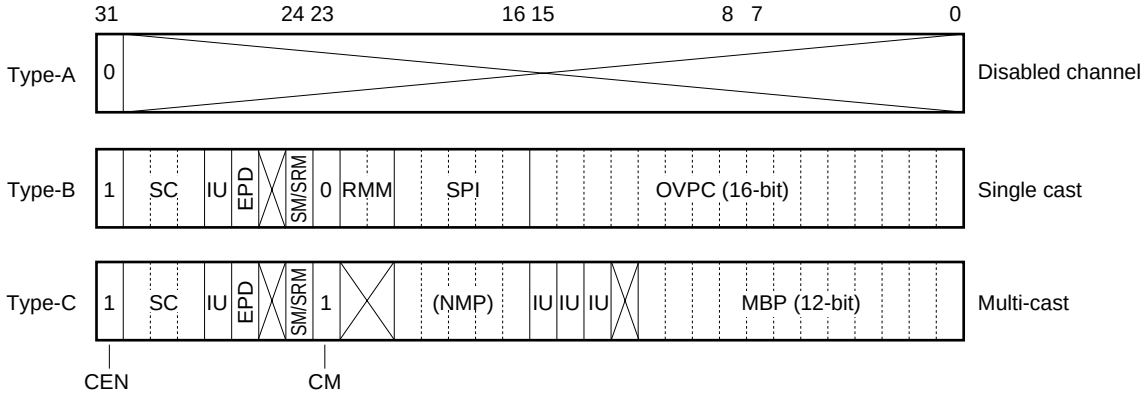
This section explains the format in which information is stored in Area-A and Area-B.

(1) Area-A format

The μPD98412 accesses Area-A by using a logical input port number, VPI, and VCI as pointers when cells are input.

Area-A stores the following information in 4-byte units.

Figure 3-26. HTT Area-A Format



- Area X is reserved. Write “0” to this area. This area is “undefined” when it is read.
- Area IU is used for the internal processing of the μPD98412. Set bit 13 of Type-C to “1”, and reset bits 14, 15, and 27 to “0”. These bits are “undefined” when read.

(1/2)

Symbol	Name	Size	Description
CEN	Channel Enable	1 bit	Makes the table valid or invalid. 0: Invalid 1: Valid
SC	Service Class	3 bits	Specifies a service class. 000: CBR 001: rtVBR 010: Reserved 011: nrtVBR 100: ABR 101: Reserved 110: UBR 111: Reserved
EPD	Early Packet Discard Enable	1 bit	Makes EPD valid or invalid. When CEN is active, the read value of this bit is not guaranteed because the μPD98412 rewrites the value. 0: EPD invalid 1: EPD valid
SM/SRM	Switching Mode/Special Routing Mode	1 bit	SM bit sets VP/VC connection. Only the SM bit in the HTT area that is accessed when VCI = 20h or VCI = the value set in the SMA field is meaningful. 0: VC connection 1: VP connection Special routing mode (SRM) is set in the HTT area that is accessed in the case of Pre-Defined Channel with an exception for the RM cell. 0: Special routing is performed. 1: Special routing is not performed. Set “0” to the HT area that is accessed if VCI = 21h or more.
CM	Cast Mode	1 bit	Selects multi-cast or single cast. 0: Single cast 1: Multi-cast
RMM	RM Cell Merge Enable	2 bits	Sets RM cell merge processing for single cast connection in the backward direction for multi-cast connection. Set these bits to “00” for any other connection. 00: No merge & transfer 01: Reserved 10: Merge & transfer 11: Merge & discard

(2/2)

Symbol	Name	Size	Description
SPI	Single Cast Port ID	5 bits	Sets a logical output port number (0 to 29) in single cast mode. 00h to 1Dh: Logical output port 0 to 29 1Eh to 1Fh: Reserved
(NMP)	Number of Multi-cast Port	5 bits	Clear this field of the μPD98412 to 00h. The operation of the μPD98412 is not affected by this field. This field is provided to maintain compatibility of the μPD98412 with the μPD98410.
OVPC	Output VPI, VCI	16 bits	Sets VPI and VCI appended to the output cell (after header translation) in single cast mode.
MBP	Multi-cast Bitmap Pointer	12 bits	Sets a pointer to access Area-B in multi-cast mode.
IU	Internal used	–	These bits are used by the μPD98412 as a work area. Set bit 13 to “1” and reset bits 14, 15, and 27 to “0”.

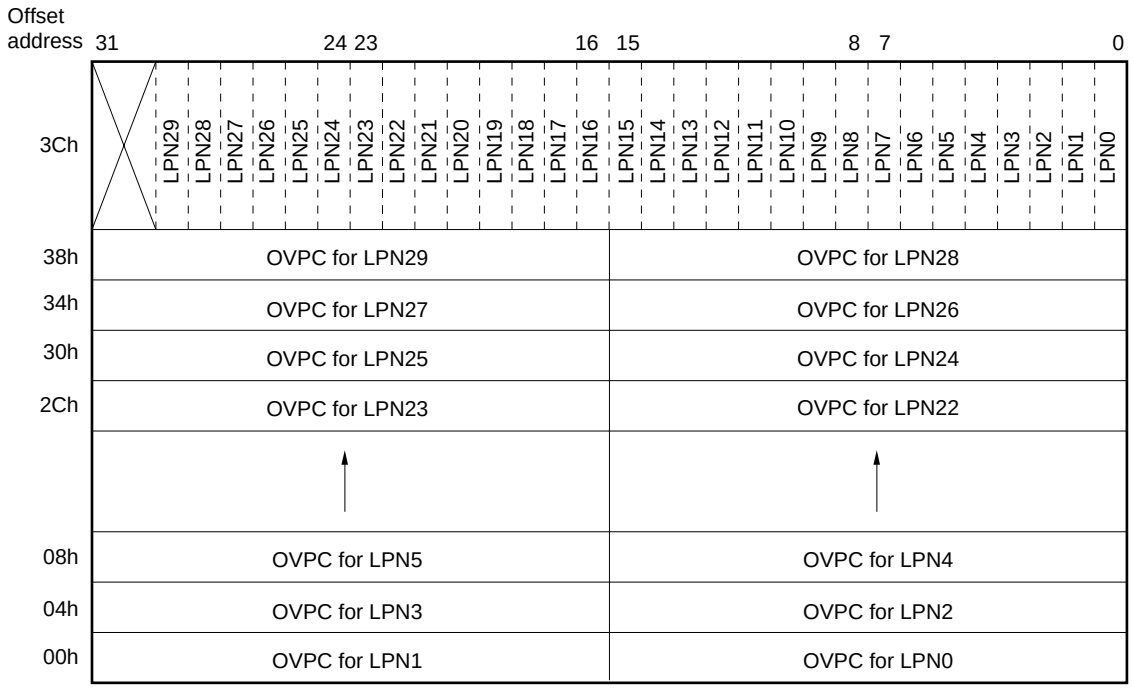
Remark Here is an example of setting the MBP bit.
If the HMS bits of the MODE1 register are 10 and the MBP bits are 001h, the HTT & control memory address of the pointer indicated by MBP is 40000h (start address of Area-B) + 40h = 40040h.

(2) Area-B format

The μPD98412 accesses Area-B by using MBP as a pointer when a multi-cast cell is input.

The following information is stored in Area-B in 64-byte units.

Figure 3-27. HTT Area-B Format



- Area X is reserved. Write “0” to this area. This area is “undefined” when it is read.

Symbol	Name	Size	Description
LPN0 - LPN30 (MB)	Logical Port Number (Multi-cast Bitmap)	30 bits	Sets the corresponding bit of the logical output port at the cast destination in multi-cast mode. 0: Does not cast to the corresponding port. 1: Casts to the corresponding port.
OVPC	Output VPI, VCI	16 bits	Sets VPI and VCI to be appended to the output cell (after header translation) in multi-cast mode.

3.12.4 Accessing HTT

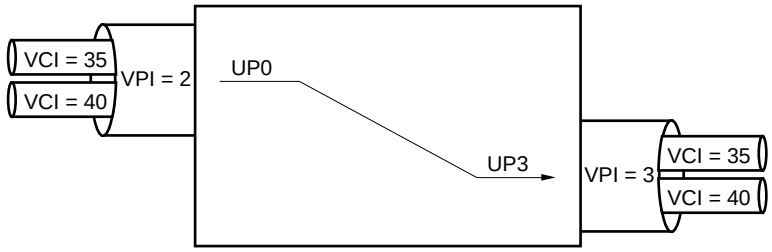
Accessing the HTT was mentioned in **3.12.2 General**. This section explains that in detail.

(1) VP connection and VC connection

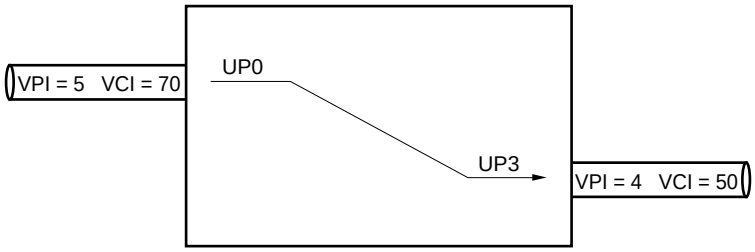
The μPD98412 performs two types of switching: VP connection and VC connection. The differences between these two modes of switching are illustrated below.

Figure 3-28. VP Connection and VC Connection

VP connection



VC connection



(VP connection)

- Replaces only VPI of a cell header.

(VC connection)

- Replaces VPI and VCI of a cell header.

(2) Access to HTT

Section **3.12.2 General** discussed how to calculate the address to access the HTT by using a logical input port number, VPI , and VCI. In practice, however, the address is calculated in the following procedure, because of the differences between VP connection and VC connection. Figure 3-29 illustrates accessing the HTT in single cast mode. The procedure for accessing Area-A is the same in multi-cast mode.

<Procedure>

<1> The HTT is accessed by using the following value. The value read identifies whether the switching mode (SM) is VPC (VP connection) or VCC (VC connection).

Port No.	VPI	VCI
Logical input port number	VPI in input cell header	20h or value set in SMA field

★ **Caution VCI changes according to the EN field setting value in the switching mode address (SMA).**

- **When the EN field is "0," VCI will equal 20h.**
- **When the EN field is "1," VCI will equal the value set in the SMA field of the SMA register.**

<2>-1 If the switching mode is a VP connection, the header translation information is assigned to the area accessed in <1>.

<2>-2 If the mode is VC connection, the HTT is accessed again by using the following value. The header translation information is assigned to this area (in a mode other than the switching mode (SM)).

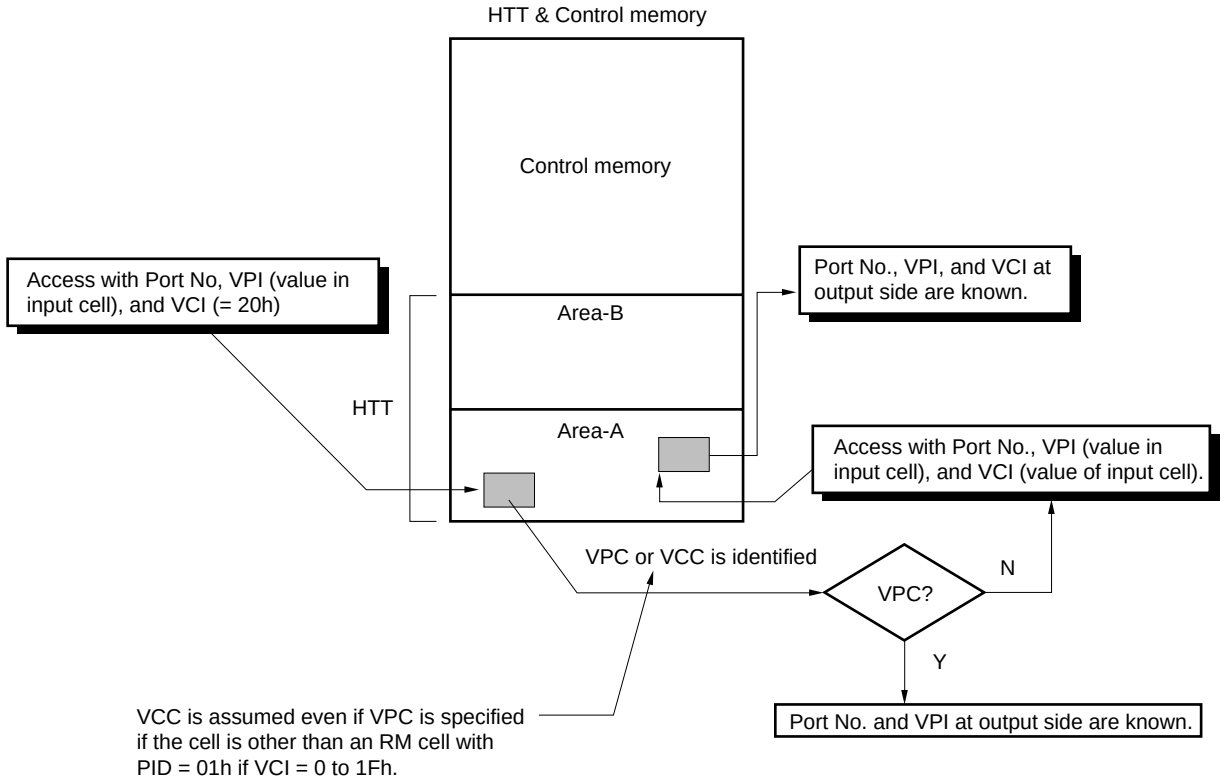
Port No.	VPI	VCI
Logical input port number	VPI in input cell header	VCI in input cell header

Cautions 1. With a Pre-Defined Channel (Input-VCI = 0 to 1Fh) of a cell other than an RM cell, the header is translated by means of normal VC connection even if VP connection is specified by the information on the switching mode (SM). For details about accessing HTT with an RM cell, refer to 3.12.8 Routing of RM cell.

★ **2. The VCI range of the input cell treated as the Pre-Defined Channel of the μPD98412 changes as shown in the table below as a result of NVCI field of the header conversion configuration register (HT) and the value set for the SMA register.**

NVCI	SMA register setting	Pre-Defined Channel
3	EN = 1, SMA = 0-7(h)	VCI = 0-7(h); excluding, however, VCI = SMA
4	EN = 1, SMA = 0-F(h)	VCI = 0-F(h); excluding, however, VCI = SMA
5	EN = 1, SMA is optional (0-1F(h))	VCI = 0-1F(h); excluding, however, VCI = SMA
6-15	Optional	VCI = 0-1F(h); excluding VCI = SMA, however, when EN = 1

Figure 3-29. Difference in Access to HTT between VPC and VCC (Single Cast)



(3) Calculating HTT address

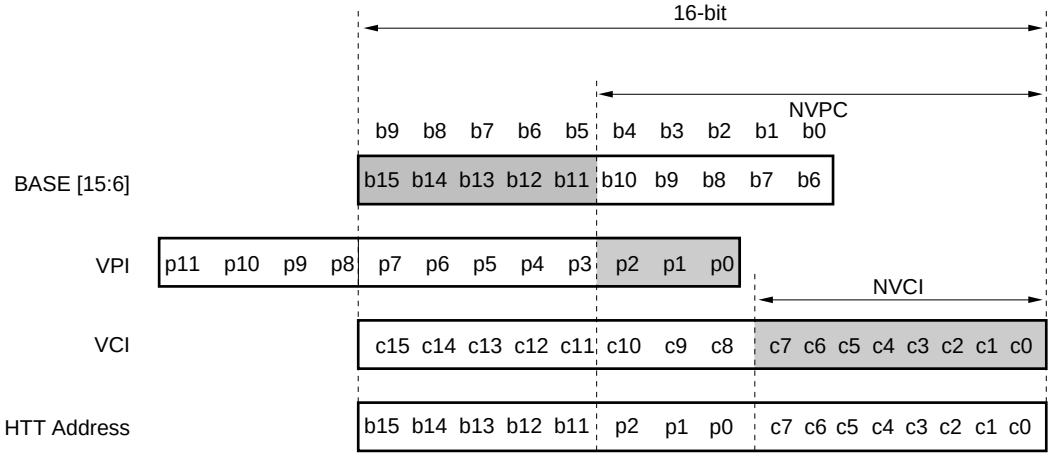
In **(2) Access to HTT**, it is explained that a logical input port number, VPI, and VCI are used to calculate an address when the Area-A of the HTT is accessed. This section explains how these parameters are used to calculate an address.

Internally, the μPD98412 has the following information for each logical input port.

NVPC	Number of valid bits of VPI + Number of valid bits of VCI
NVCI	Number of valid bits of VCI
BASE [15:6]	Base address (offset value)

An actual HTT address is calculated as shown in Figure 3-30, based on the above information. In the example below, NVPC = 11 and NVCI = 8.

Figure 3-30. Calculating HTT Address



Remark The address calculated in this figure is a value in word (4 bytes) units. If the microprocessor accesses an address, specify an address in byte units by multiplying the address value by four.

The valid range of BASE and HTT addresses is dependent upon the size of the HTT & control memory (the value of HMS bit of the mode register). The relationship between this size and the valid range of the HTT addresses is shown below (Figure 3-30 shows an example where HMS = 10).

HMS (32-bit per word)	BASE	HTT Address
00 (64K words)	[13:6]	[13:0]
01 (128K words)	[14:6]	[14:0]
10 (256K words)	[15:6]	[15:0]

(4) VPI and VCI of output cell

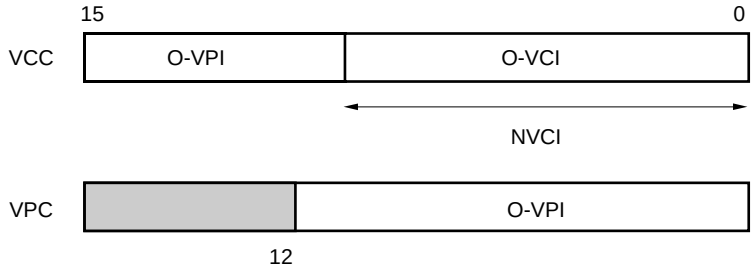
The procedure to obtain information on a port number at the output side, and VPI and VCI to be appended to an output cell has been discussed so far. Using this procedure, the information on a logical output port number can be obtained from the following:

- SPI of Area-A in single cast mode
- LPN0 through LPN23 of Area-B in multi-cast mode

Information on VPI and VCI can be obtained from the following. "OVPC" is set as shown in Figure 3-31, depending on the difference in the switching mode.

- OVPC of Area-A in single cast mode
- OVPC of Area-B in multi-cast mode

Figure 3-31. Setting Format of OVPC



NVCI is a parameter that specifies how many bits of OVPC (16 bits wide) are used as O-VCI (Output VCI). In the case of VPC, only the O-VPI (Output VPI) (12 bits) is stored. This is because the VPC replaces only the VPI and the VCI outputs the value of an input cell as is.

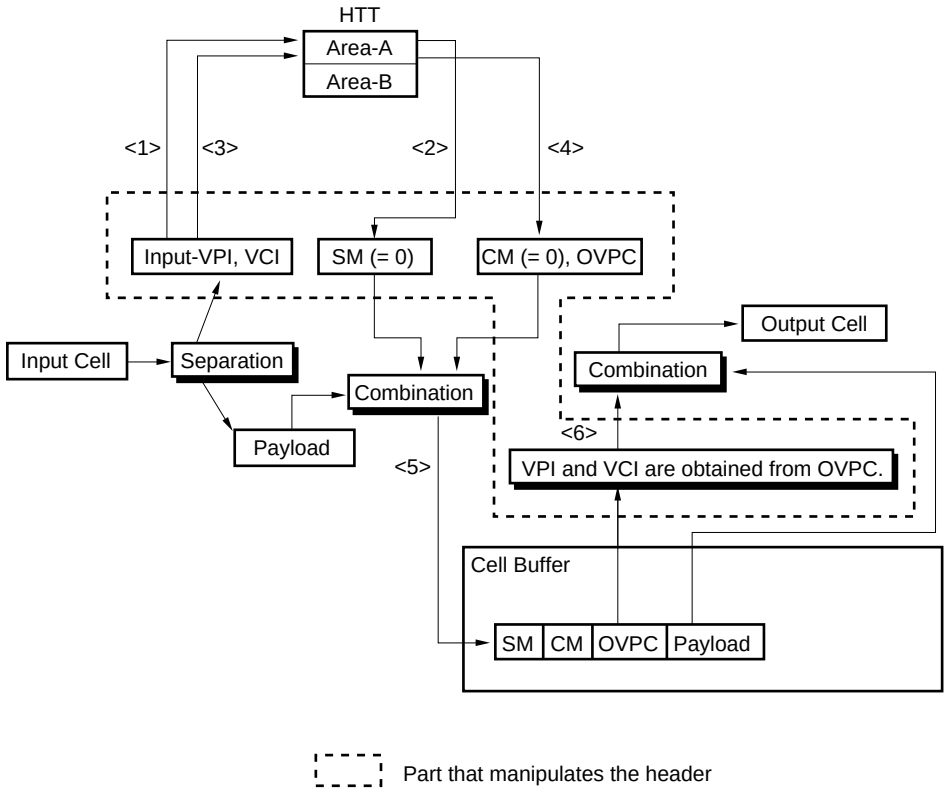
In the case of VCC, up to 16 bits can be used with VPI and VCI combined. The VPI and VCI fields in a cell header are 12 bits (NNI) and 16 bits, respectively. The 13th through 16th bits of the VPI field are fixed to "0" when a cell is output.

3.12.5 Flow of header translation

This section explains the flow of header translation depending on the differences in the switching mode and cast mode.

(1) VCC, single cast

Figure 3-32. Flow of Header Translation in VCC and Single Cast Modes



<Procedure>

<1> Area-A is accessed by using a logical input port number, Input-VPI, VCI = 20h, or VCI = the value set in the SMA field.

<2> Information about the VC connection (SM = 0) is obtained.

<3> Area-A is accessed again by using a logical input port number, Input-VPI, and Input-VCI.

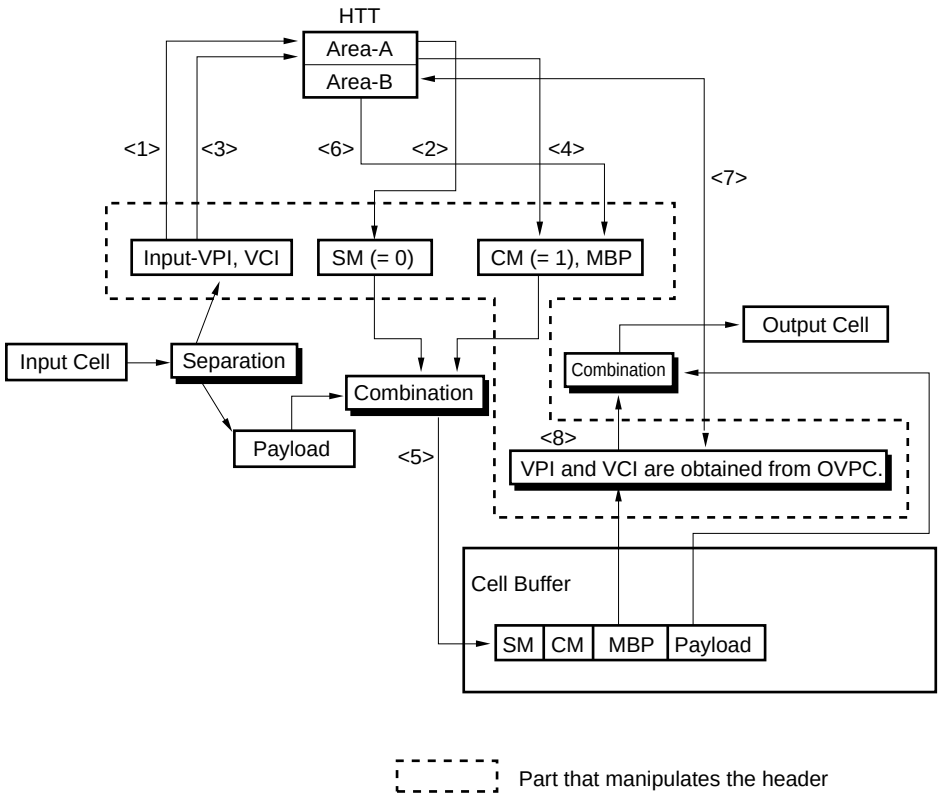
<4> OVPC is obtained in single cast mode (CM = 0). At the same time, a service class (SC) and a logical output port number (SPI) are also obtained, and the output queue that stores cell addresses is determined.

<5> SM, CM, and OVPC are stored in the cell buffer based on the payload of the input cell.

<6> VPI and VCI of the output cell header are set based on OVPC when the cell is output.

(2) VCC, multi-cast

Figure 3-33. Flow of Header Translation in VCC and Multi-Cast Modes



<Procedure>

<1> Area-A is accessed by using a logical input port number, Input-VPI, VCI = 20h, or VCI = the value set in the SMA field.

<2> Information about the VC connection (SM = 0) is obtained.

<3> Area-A is accessed again by using a logical input port number, Input-VPI, and Input-VCI.

<4> Multi-cast (CM = 1), pointer to Area-B (MBP), broadcast count (NMP), and service class (SC) are obtained.

<5> SM, CM, and MBP are stored in the cell buffer along with the payload of the input cell. The cell address is stored in the multi-cast queue.

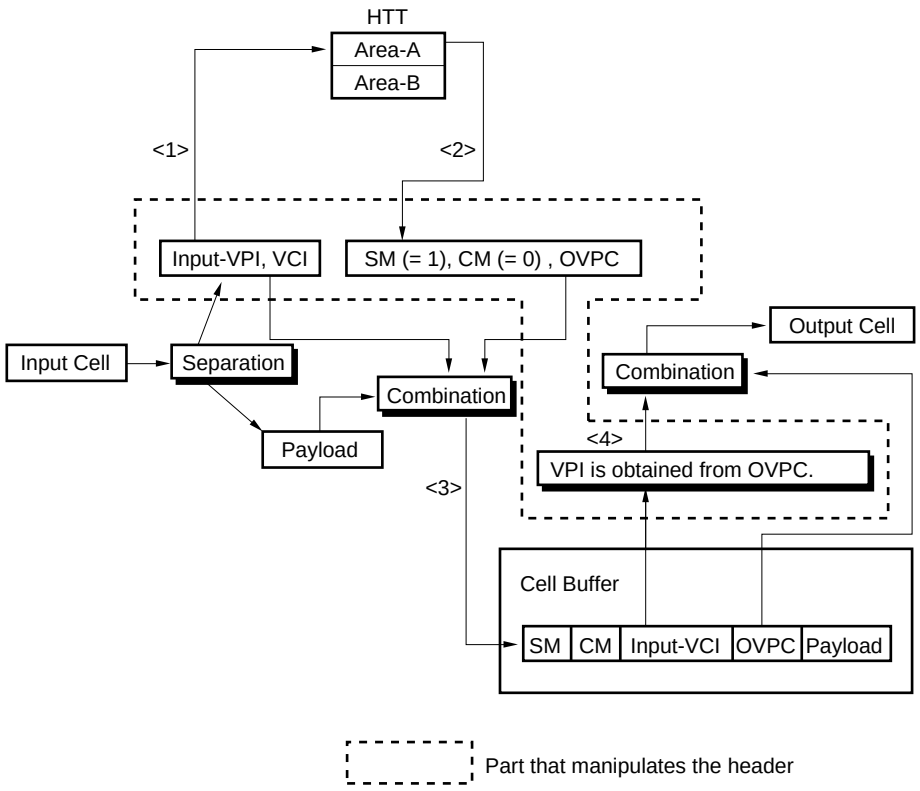
<6> Area-B is accessed by using MBP before re-queuing, and the logical output port number to be cast is obtained. At this time, the cell address is stored in the output queue.

<7> Area-B is accessed again when the cell is output, and the OVPC information on each logical output port is obtained.

<8> VPI and VCI of the output cell header are set from OVPC.

(3) VPC, single cast

Figure 3-34. Flow of Header Translation in VPC and Single Cast Modes



<Procedure>

<1> Area-A is accessed by using a logical input port number, Input-VPI, VCI = 20h, or VCI = the value set in the SMA field.

<2> Single cast (CM = 0) and OVPC (O-VPI information only in OVPC) are obtained based on information VP connection (SM = 1). Because a service class (SC) and a logical output port number (SPI) are also obtained, the output queue in which the cell address is to be stored is determined.

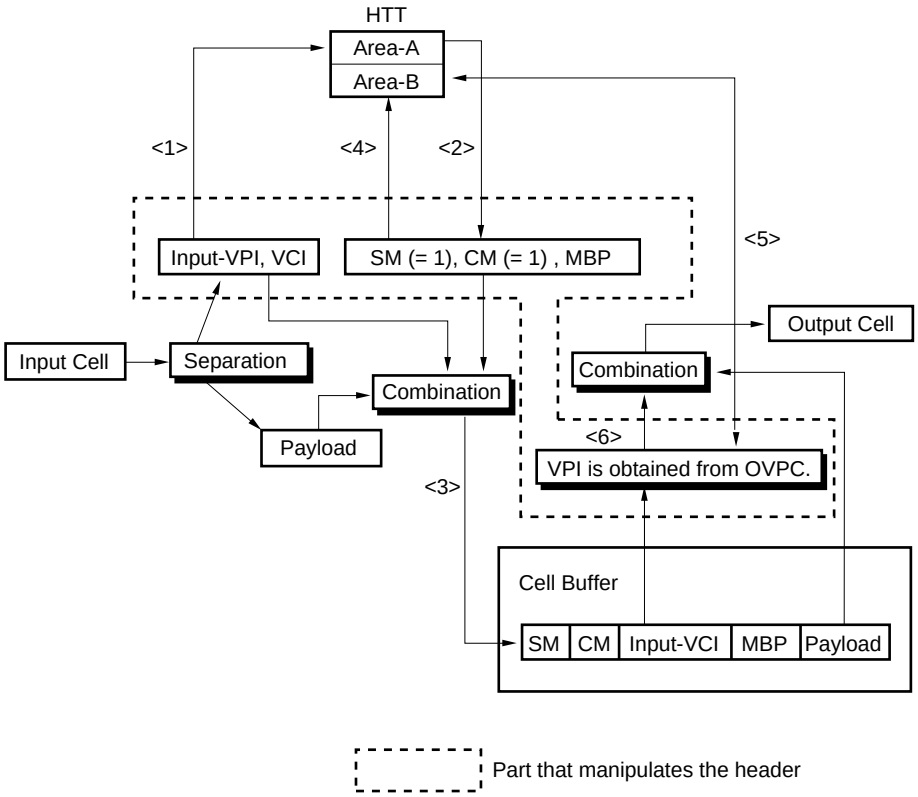
<3> SM, CM, Input-VCI, and OVPC are stored along with the payload of the input cell.

<4> VPI is obtained from OVPC when the cell is output. VCI uses Input-VCI as is.

Caution With a Pre-Defined Channel of a cell other than an RM cell, the header is translated by means of ordinary VC connection even if VP connection is specified by the information on SM obtained in <2>. In the same manner as ordinary VC connection, O-VPI and O-VCI are obtained from OVPC information. The setting of EPD is valid even if SM is specified for VP connection. For details of the RM cell, refer to 3.12.8 Routing of RM cell.

(4) VPC, multi-cast

Figure 3-35. Flow of Header Translation in VPC and Multi-Cast Modes



<Procedure>

<1> Area-A is accessed by using a logical input port number, Input-VPI, VCI = 20h, or VCI = the value set in the SMA field.

<2> Information about the VP connection (SM = 1) is obtained. At the same time, multi-cast (CM = 1), pointer to Area-B (MBP), and service class (SC) are also obtained.

<3> Input-VCI, SM, CM, and MBP are stored in the cell buffer along with the payload of the input cell. The cell address is stored in the multi-cast queue.

<4> Area-B is accessed by using MBP before re-queuing, and the logical output port number to be cast is obtained. At this time, the cell address is stored in the output queue.

<5> Area-B is accessed again when the cell is output, and the OVPC information of each logical output port is obtained.

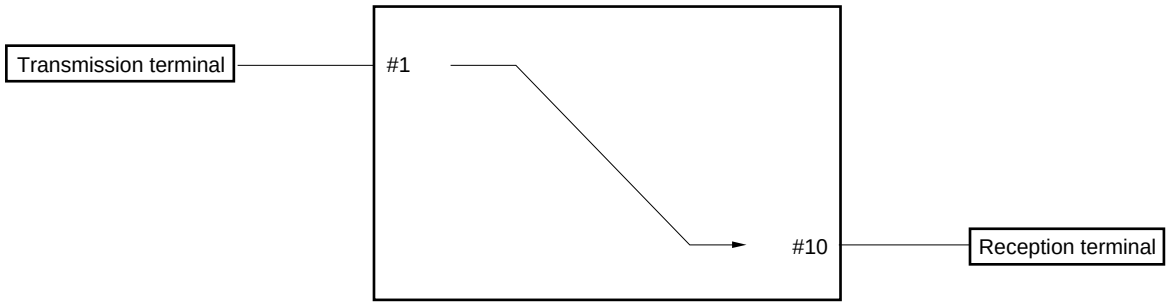
<6> VPI is obtained from OVPC. VCI uses Input-VCI as is.

Caution With a Pre-Defined Channel of a cell other than an RM cell, the header is translated by means of ordinary VC connection even if VP connection is specified by the information on SM obtained in <2>. In the same manner as ordinary VC connection, O-VPI and O-VCI are obtained from OVPC information. The setting of EPD is valid even if SM is specified for VP connection. For details of the RM cell, refer to 3.12.8 Routing of RM cell.

3.12.6 Accessing HTT with RM cell

(1) Connection in ABR class

In ABR (Available Bit Rate) class, connection of the Backward RM cell that reports congestion information in the transmission terminal direction must be set.



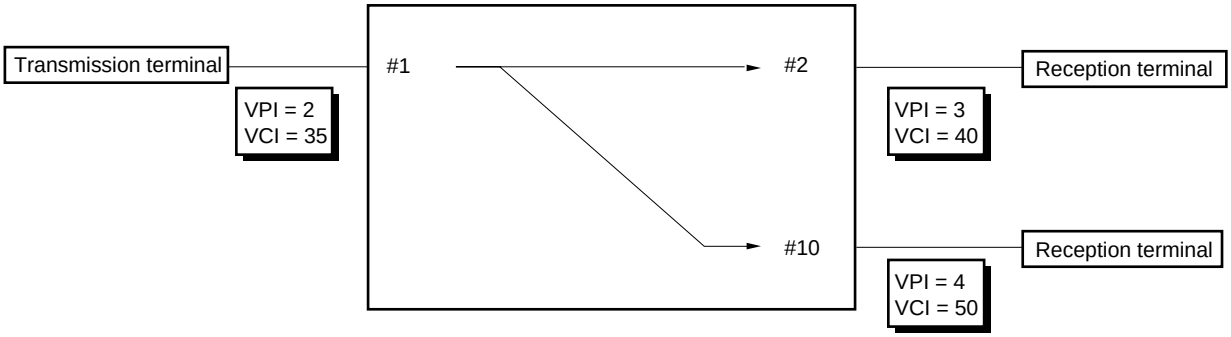
#n: Logical port number

Assuming that a cell is transmitted in the combination (A) in the table below, connection in the backward direction must be set in combination (B) to return the Backward RM cell.

	Logical Input Port Number	Logical Output Port Number
(A)	1	10
(B)	10	1

(2) Multi-cast and RM cell merge function

Next, the case of multi-cast is considered.



#n: Logical port number

In this case, multi-cast connection (a) in the table below must be set in the transmission direction of the cell, and two single cast connections such as in (b) must be set in the backward direction.

	Logical Input Port Number	Logical Output Port Number
(a)	1	2, 10
(b)	2	1
	10	1

Now, let's consider the case in which the RM cell merge function is used. This function must be used to OR the CI and NI bits of the Backward RM cell that is input from the two connections set in (b) and to AND the BN bit. At this time, the work area used for ORing and ANDing is reserved in the HTT used in (a). If the Backward RM cell is input to connection (b), therefore, the address of the HTT used in (a) (address obtained in the table below) must be determined by some means.

	Logical Input Port Number	VPI	VCI
At VPC	1	2	20h or value set in SMA field
At VCC	1	2	35

Because (b) and (a) are completely opposite to each other in terms of input/output, the following values assigned to the HTT in (b) are used to obtain the value in the above table.

	Logical Input Port Number of (a)	VPI of (a)	VCI of (a)
At VPC	Logical output port number (SPI)	OVPC	20h or value set in SMA field
At VCC	Logical output port number (SPI)	OVPC	OVPC

If the input cell is the Backward RM cell (and cells are to be merged), therefore, the HTT is accessed two times to translate the header and merge the RM cell. The RM cell merge function can be used only when RMA of the MODE1 register is set to “0x”. With this setting, however, the switching mode is identified as follows without referring to the SM bit of HTT, to reduce the number of times HTT is referenced.

- VCI in cell header = 6 → VPC
- VCI in cell header ≠ 6 → VCC

For details, refer to **3.12.8 Routing of RM cell**.

(VPC)

<1> The HTT of (b) is accessed by using:
RMA = 00 → logical input port number, VPI of the input cell, VCI = 20h, or VCI = the value set in the SMA field
RMA = 01 → logical input port number, VPI and VCI of the input cell

<2> The HTT of (a) is accessed by using a logical output port number (SPI), OVPC, VCI = 20h, or VCI = the value set in the SMA field.

(VCC)

<1> The HTT of (b) is accessed by using a logical input port number, and VPI and VCI of the input cell.

<2> The HTT of (a) is accessed by using a logical output port number (SPI), and VPI and VCI in OVPC.

3.12.7 Microprocessor connection port

The μPD98412 supports special routing, in addition to ordinary routing.

The μPD98412 can set a microprocessor connection port that can be distinguished from the other ports, for signaling processing and OAM cell processing by the microprocessor. This section explains the functions used to transmit/receive cells via the microprocessor connection port.

The microprocessor connection port can be specified by assigning a logical port number to the special routine logical port (SRLP) register.

(1) Special routing

To output cells to the microprocessor connection port, the function of ordinary routing that specifies the microprocessor connection port as the output port of HTT, and the function of special routing may be used. Special routing allows cells to be output to the microprocessor connection port whatever logical output port may be assigned to HTT. The cells supported by special routing differ between the Pre-Defined Channel and user channel.

Channel		Cell Supported by Special Routing
Pre-defined channel		Cells belonging to connection with SRM bit being 1 in HTT Area-A
User channel	VC connection	Cell with PT of its cell header matching value of specified PT filter
	VP connection	None

★ **Remarks 1.** For details of the SRM bit, refer to the format of HTT.

2. For details of the PT filter, refer to the description of the SRFLT register.

3. Cells input from the microprocessor connection port are not subject to special routing.

Special routing is used to process the cells output to the microprocessor connection port, as follows:

- VPI/VCI VPI and VCI of the input cell are not changed.
- PT EFCI marking is performed.
- CLP The value of CLP of the input cell is not changed.

(2) Information of cell header

Special information can be appended to the cell header of a cell output to the microprocessor connection port, and the special information can be obtained from the cell header of the cell that is input. The position of this information can be set as follows:

- High-order VPI bits (VPI [7:3] when UNI, VP [11:7] when NNI)
- High-order VCI bits (VCI [15:11])
- UDF1 [4:0] (UDF [4:0])
- UDF2 [4:0]

- Information appended when cell is output to microprocessor connection port
  When a cell is output to the microprocessor output port, the logical port number of the port to which the cell has been input can be appended to the cell header. The logical input port number can be appended to a cell defined by the IA bit of the SRLP register.

IA Bit	Cells
0	All cells output to microprocessor connection port (ordinary routing and special routing)
1	Cells output to microprocessor connection port by special routing (SRM = 1, or PTI = PTF)

Remark If UDF2 is specified as the information appending position even though the UTOPIA interface is of the 8-bit type, the information is not appended but this is not treated as an error.

- Information obtained when cell is input from microprocessor connection port
  A virtual logical input port number can be appended to a cell input from the microprocessor connection port. The virtual logical input port number is used to calculate the address of HTT Area-A that is accessed for header conversion. Therefore, a cell input from the microprocessor connection port can be routed in the same manner as a cell input from a port specified as a virtual logical input port. If this information is not used, the microprocessor connection port number is used. The virtual logical input port number is obtained from a cell defined by the VA bit of the SRLP register.

VA Bit	Cells
0	All cells input from microprocessor connection port
1	Cells input from microprocessor connection port and having PTI field defined by PTFLT register

★ **Remarks 1.** The following will result if UDF (or UDF1) is specified as the position of the information that can be obtained from the cell header of the input cell:

(1) HEC error check is not performed for cells with PTI fields defined by the PTFLT register for which the VA bit = 0 or 1, whether the HM bit of the MODE1 register is set or not.

(2) HEC error check can be selected for cells that do not have PTI fields defined by the PTFLT register for which the VA bit = 1 with the value to which the HM bit of the MODE1 register is set.

2. If an invalid value is specified as a virtual input port number, a header conversion error is detected, causing cells to be discarded. In this case, the IIP bit of ERHT register is set, and the value of the CTERHT register is updated.

3. If UDF2 is specified as the position of information even though the UTOPIA interface is of the 8-bit type, a header conversion error is detected, causing cells to be discarded. In this case, the IIP bit of the ERHT register is set, and the value of the CTERHT register is updated.

3.12.8 Routing of RM cell

The μPD98412 queues RM cells in the RM/nrtVBR queue, regardless of the specified service class. This section explains how the μPD98412 identifies an RM cell.

The μPD98412 identifies an RM cell differently, depending on the setting of the RMA field of the mode 1 (MODE1) register.

RMA	Identifying RM Cell
10	1. When a cell is input, the SM bit of HTT Area-A referenced when VCI = 20 or VCI = the value set in the SMA field is referenced. 2. 2. The RM cell is identified differently, as follows, depending on the value of the SM bit: SM = 0 (VC connection) If the cell configuration is as follows, this cell is regarded as a VC RM cell. PTI = 110, PID = 1 (Value of VCI is independent.) SM = 1 (VP connection) PTI = 110, PID = 1, VCI = 6 This cell is regarded as a VP RM cell. PTI = 110, PID = 1, VCI ≠ 6 This cell is not regarded as an RM cell (it is regarded as a user cell).
0x	A cell is identified by taking VCI, PTI, and PID of the cell into consideration (the SM bit of HTT Area-A is not referenced). PTI = 110, PID = 1, VCI ≠ 6 Regarded as VC RM cell. PTI = 110, PID = 1, VCI = 6 Regarded as VP RM cell.

The setting of RMA = “10” is the basic mode of the μPD98412. In this mode, however, the RM cell merge function cannot be used. The setting of RMA = “0x” is a mode in which the RM cell merge function can be used.

RMA = “10” RM cell merge function cannot be used.

RMA = “0x” RM cell merge function can be used.

If the RMA = “0x” mode is used, however, the following limitation applies because the SM bit of HTT is not referenced.

- **Limitation related to RMA = “0x” mode**

  The VC RM cell in VP connection cannot be treated in the same manner as the user cell. Therefore, the VC connection of ABR cannot be included in the VP connection (when the VC connection of ABR is set in the VP connection, the VC RM cell of the VP connection may be discarded).

Whether special routing of the VP RM cell is possible or not differs depending on RMA, because the address at which HTT Area-A is referenced differs depending on the RMA mode.

RMA	Special Routing of VP RM Cell	HTT Area-A to Be Referenced
10	Possible	SM bit of area referenced with VCI = 20h or VCI = value set in SMA field, and area referenced by VCI (= 06h) of VCI = input cell.
00	Impossible	Area referenced with VCI = 20h or VCI = value set in SMA field (μPD98410-compatible mode)
01	Possible	Area referenced by VCI (= 06h) of VCI = input cell

When using the setting of RMA = “01” or “10”, the special routing function of the VP RM cell is enabled depending on the setting of the SRM bit of HTT Area-A referenced with VCI = 06h. The setting of RMA = “00” is to keep the μPD98412 compatible with the μPD98410. When the setting of RMA = “00” is used, the special routing function cannot be used. However, the μPD98412 performs special routing of the VC RM cell regardless of the setting of RMA.

3.13 Queue Control

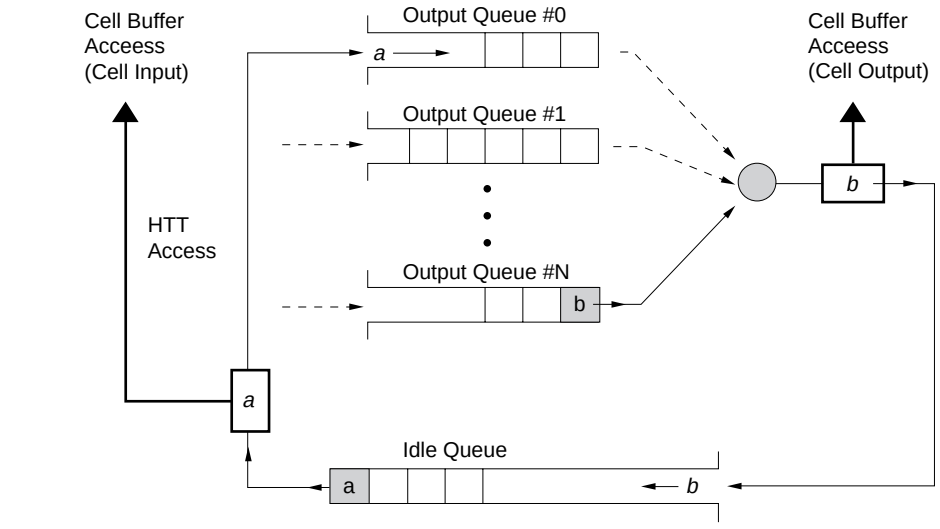
The μPD98412 organizes the following queues in the control memory for management of the cell buffer.

- The idle queue queues an address pointer that indicates the position of the cell buffer to which the cells can be stored.
- The multi-cast queue queues an address pointer that indicates the position to which the cells to be multi-cast are stored.
- The output queue which is provided for each logical output port queues an address pointer that indicates the position to which a cell for each logical output port is stored.

3.13.1 Single cast

This section explains the processing sequence of the queuing in the single cast mode.

Figure 3-36. Queuing of Cell Address (Single Cast)



a, b : Cell Address Pointer
HTT: Header Translation Table

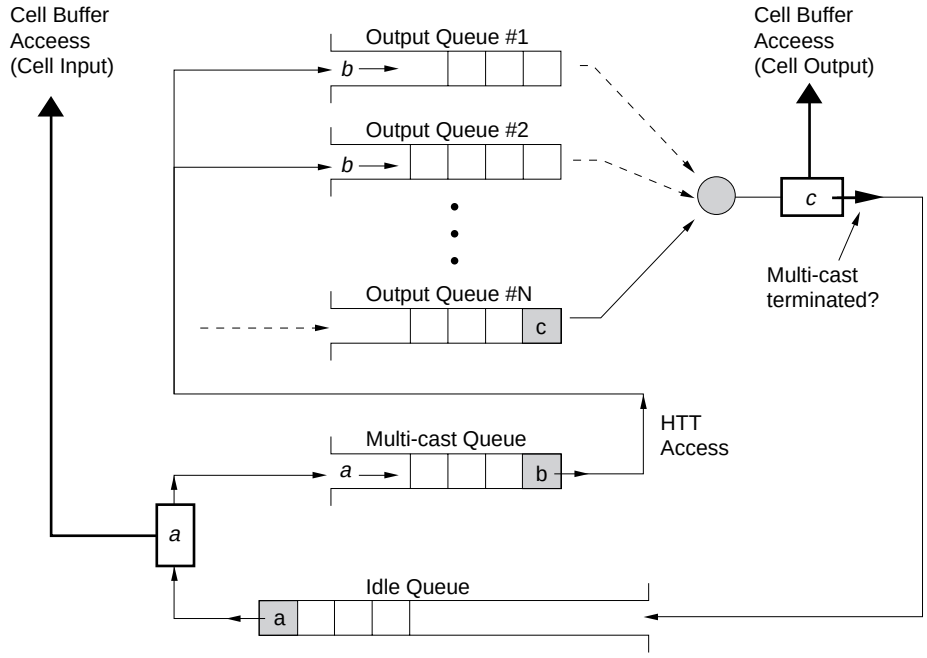
- **Cell input procedure (obtaining write address of cell buffer)**
  1. Cell address a is obtained from the idle queue.
  2. The input cell is stored in the cell buffer addressed by cell address a.
  3. A logical output port number is obtained from the header translation table (HTT).
  4. Cell address a is input to the output queue of the logical output port obtained.

- **Cell output procedure (obtaining read address of cell buffer)**
  1. Cell address b is obtained from the output queue of a logical output port.
  2. An output cell is obtained from the cell buffer indicated by cell address b.
  3. Cell address b is input to the idle queue.

3.13.2 Multi-cast

The μPD98412 realizes multi-casting by storing input cells in one location in the cell buffer and inputting cell addresses to the output queue of each logical output port. The advantage of this method is that it is not necessary to copy 53-byte cells more than once. In this way, the cell buffer can be used effectively and casting can be performed at high speed.

Figure 3-37. Queuing of Cell Address (Multi-Cast)



a, b : Cell Address Pointer
HTT: Header Translation Table

- **Cell input procedure (obtaining write address of cell buffer)**
  1. Cell address a is obtained from the idle queue.
  2. The input cell is stored in the cell buffer indicated by cell address a.
  3. Cell address a is input to the multi-cast queue.

- **Re-queuing procedure**
  1. Cell address b is obtained from the multi-cast queue.
  2. A logical output port number is obtained from the header translation table (HTT).
  3. Cell address b is input to the output queue of each logical output port.

- **Cell output procedure (obtaining read address of cell buffer)**
  1. Cell address c is obtained from the output queue of a logical output port.
  2. The output cell is obtained from the cell buffer indicated by cell address c.
  3. Cell address c is input to the idle queue after the cell has been output to all the logical output ports to be multi-cast.

3.13.3 Congestion control

ATM defines service classes based on Cell Loss/Cell Transfer Delay/Cell Delay Variation that indicate the traffic status of cells and transfer quality. The μPD98412 divides the service classes into the following four classes for management.

- CBR (Constant Bit Rate Service), rtVBR (Real time Variable Bit Rate Service)
- RM (RM cell), nrtVBR (Non real time VBR Service)
- ABR (Available Bit Rate Service)
- UBR (Unspecified Bit Rate Service)

Remark The RM cell is included in the ABR class but the μPD98412 treats the RM cell as one of the service classes. The user cannot specify a class for the RM cell.

The μPD98412 has the following queues and counters. Congestion control is performed by using the threshold values that are assigned to these queues and counters. Figure 3-38 shows the relationship between the queues, counters, and their threshold values.

- **UC: Used Cell Counter**
  This counter indicates the total number of cells retained in the cell buffer. The value assigned to the ALLmin register as the minimum queue length is also treated as the number of cells retained in the cell buffer. When performing multi-cast, only one cell is counted in, regardless of the broadcast count.

- **TC: Total Cell Counter for each class (4 classes)**
  If the number of cells retained in the output queue exceeds the minimum queue length OQminCRV/OQminRNV/OQminABR/OQminUBR of each class, this counter indicates the total sum of the number of cells of each class that exceeds the minimum length. When performing multi-cast, the number of cells is counted in accordance with broadcast count.

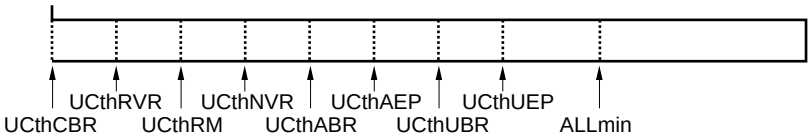
- **IQ: Idle Queue**
  This queue queues the addresses of a vacant area in the cell buffer.

- **OQ: Output Queue (30 ports × 4 classes)**
  This queue queues the addresses of the cell buffer in which the cells are stored by each logical output port and class.

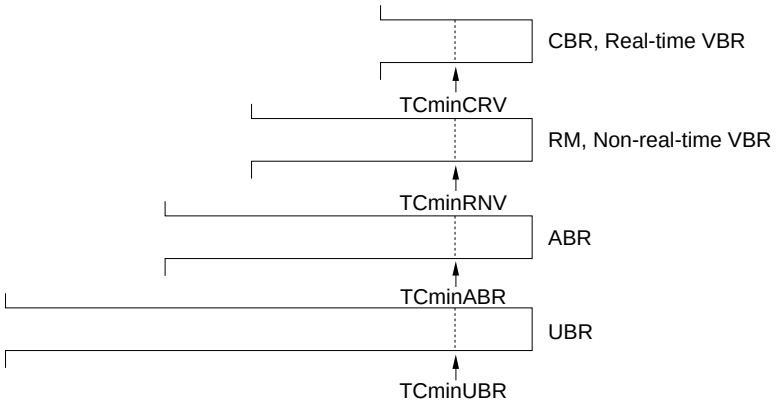
- **MQ: Multi-cast Queue (4 classes)**
  This queue queues the address of the cell buffer in which cells of each class are stored.

Figure 3-38. Queues and Counters by Service Class

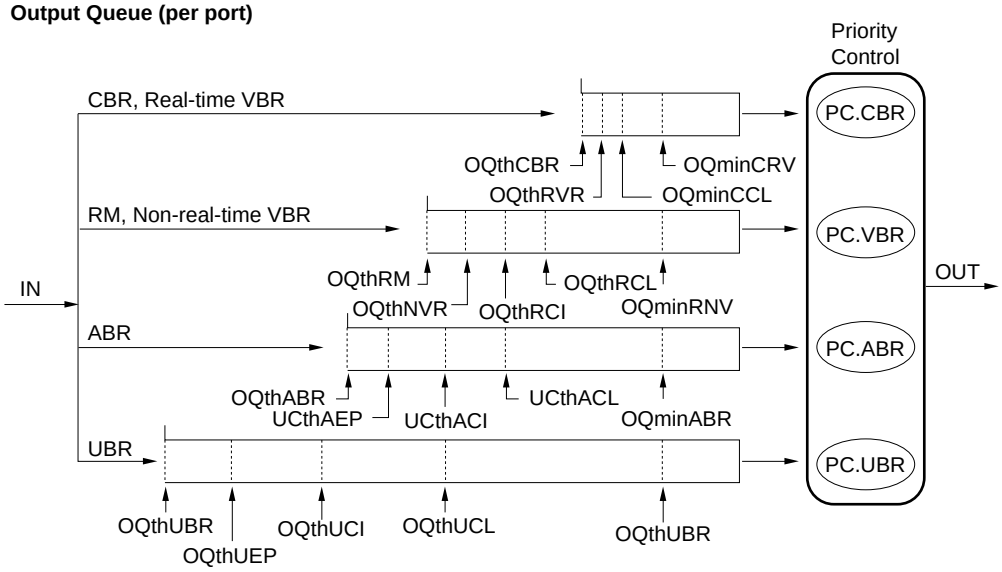
Used Cell Counter (on cell buffer)



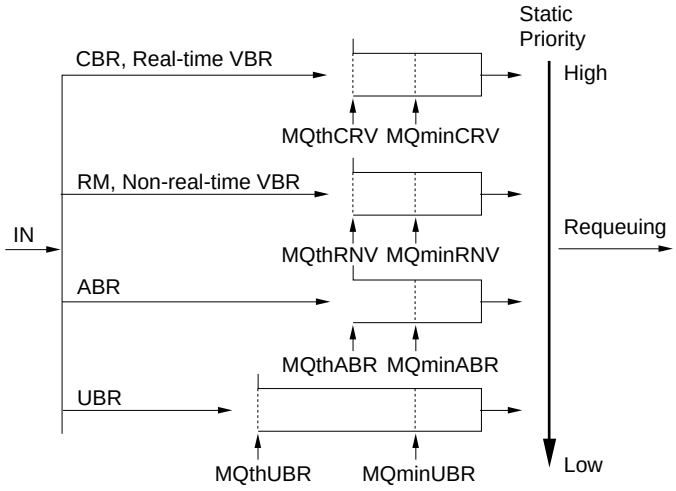
Total Cell Counter for each class (except each OQminXXX)



Output Queue (per port)



Multi-cast Queue



UC: Threshold values related to Used Cell Counter

- UCthCBR CBR cell discard threshold value
- UCthRVR rtVBR cell discard threshold value
- UCthRM RM cell discard threshold value
- UCthNVR nrtVBR cell discard threshold value
- UCthABR ABR cell discard threshold value
- UCthAEP ABR cell EPD threshold value
- UCthUBR UBR cell discard threshold value
- UCthUEP UBR cell EPD threshold value

TC: Threshold values related to Total Cell Counter for each class (none)

IQ: Threshold values related to Idle Queue (none)

OQ: Threshold values related to Output Queue

- OQthCBR CBR cell discard threshold value of output port
- OQthRVR rtVBR cell discard threshold value of output port
- OQthCCL CBR/rtVBR cell CLP discard threshold value of output port
- OQthRM RM cell discard threshold value of output port
- OQthNVR nrtVBR cell discard threshold value of output port
- OQthRCI RM/nrtVBR cell EFCI threshold value of output port
- OQthRCL RM/nrtVBR cell CLP discard threshold value of output port
- OQthABR ABR cell discard threshold value of output port
- OQthAEP ABR cell EPD threshold value of output port
- OQthACI ABR cell EFCI threshold value of output port
- OQthACL ABR cell CLP discard threshold value of output port
- OQthUBR UBR cell discard threshold value of output port
- OQthUEP UBR cell EPD threshold value of output port
- OQthUCI UBR cell EFCI threshold value of output port
- OQthUCL UBR cell CLP discard threshold value of output port

MQ: Threshold values related to Multi-cast Queue

- MQthCRV CBR/rtVBR cell discard threshold value of multi-cast queue
- MQthRNV RM/nrtVBR cell discard threshold value of multi-cast queue
- MQthABR ABR cell discard threshold value of multi-cast queue
- MQthUBR UBR cell discard threshold value of multi-cast queue

UC: Minimum queue length related to Used Cell Counter

- ALLmin Total sum of each minimum queue length

TC: Minimum queue length related to Total Cell Counter for each class

- TCminCRV Minimum queue length allocated to CBR/rtVBR class
- TCminRNV Minimum queue length allocated to RM/nrtVBR class
- TCminABR Minimum queue allocated to ABR class
- TCminUBR Minimum queue allocated to UBR class

IQ: Minimum queue length related to Idle Queue (none)

OQ: Minimum queue length related to Output Queue

- OQminCRV Minimum queue length allocated to CBR/rtVBR class of output port
- OQminRNV Minimum queue length allocated to RM/nrtVBR class of output port
- OQminABR Minimum queue length allocated to ABR class of output port
- OQminUBR Minimum queue length allocated to UBR class of output port

MQ: Threshold values related to Multi-cast Queue

- MQminCRV Minimum queue length allocated to CBR/rtVBR class of multi-cast queue
- MQminRNV Minimum queue length allocated to RM/nrtVBR class of multi-cast queue
- MQminABR Minimum queue length allocated to ABR class of multi-cast queue
- MQminUBR Minimum queue length allocated to UBR class of multi-cast queue

3.13.4 Cell discard by class

The μPD98412 forcibly discards cells that pass a congestion point if it detects congestion according to the cell discard threshold value for each class.

It controls discarding cells, giving them priorities, during the following periods:

- While the total number of cells exceeds the cell discard threshold value.
- While the output queue length of each logical output port exceeds each cell discard threshold value.

Table 3-1. Cell Discard Threshold Value Related to Total Number of Cells

Threshold Value Name	Control if Threshold Value Is Exceeded (processing during cell input)
UCthCBR	Discards CBR cell.
UCthRVR	Discards rtVBR cell.
UCthRM	Discards RM cell.
UCthNVR	Discards nrtVBR cell.
UCthABR	Discards ABR cell.
UCthUBR	Discards UBR cell.

Remark UCthAEP and UCthUEP are the cell discard threshold values for a channel that disables EPD in each class of ABR and UBR.

Table 3-2. Cell Discard Threshold Value of Output Queue Length

Threshold Value Name	Control if Threshold Value Is Exceeded (processing during cell input)
OQthCBR	Discards CBR cell of the corresponding port.
OQthRVR	Discards rtVBR cell of the corresponding port.
OQthCCL	Discards CBR/rtVBR cell of the corresponding port with CLP = 1.
OQthRM	Discards RM cell of the corresponding port.
OQthNVR	Discards nrtVBR cell of the corresponding port.
OQthRCL	Discards RM/nrtVBR cell of the corresponding port with CLP = 1.
OQthABR	Discards ABR cell of the corresponding port.
OQthACL	Discards ABR cell of the corresponding port with CLP = 1.
OQthUBR	Discards UBR cell of the corresponding port.
OQthUCL	Discards UBR cell of the corresponding port with CLP = 1.

Remarks 1. OQthAEP and OQthUEP are the cell discard threshold values for a channel that disables EPD in each class of ABR and UBR.

2. CLP is information contained in a header and indicates the priority in the same channel.

Table 3-3. Cell Discard Threshold Values Related to Multi-Cast Queue Length

Threshold Value Name	Control if Threshold Value Is Exceeded (processing during cell input)
MQthCRV	Discards CBR/rtVBR cell of multi-cast queue
MQthRNV	Discards RM/nrtVBR cell of multi-cast queue
MQthABR	Discards ABR cell of multi-cast queue
MQthUBR	Discards UBR cell of multi-cast queue

3.13.5 EPD (Early Packet Discard) control

The μPD98412 has an EPD control function. This function is to discard cells in units of the AAL-5 CS-PDU packets that are set as VC connection before congestion takes place. By discarding packets that have a high probability of being discarded after inputting packets has been started, discarding a packet that has been already input can be prevented.

Whether EPD control is performed if each queue length exceeds the EPD threshold value depends on whether control is enabled for the channel in question (by the EPD bit value of HTT). The μPD98412 operates differently, as follows, depending on whether control is enabled or disabled.

(1) If EPD control is enabled

EPD control is started as soon as the total number of cells and output queue length exceed the EPD threshold value. Once EPD control has been started, the following test is made in respect to the input cells.

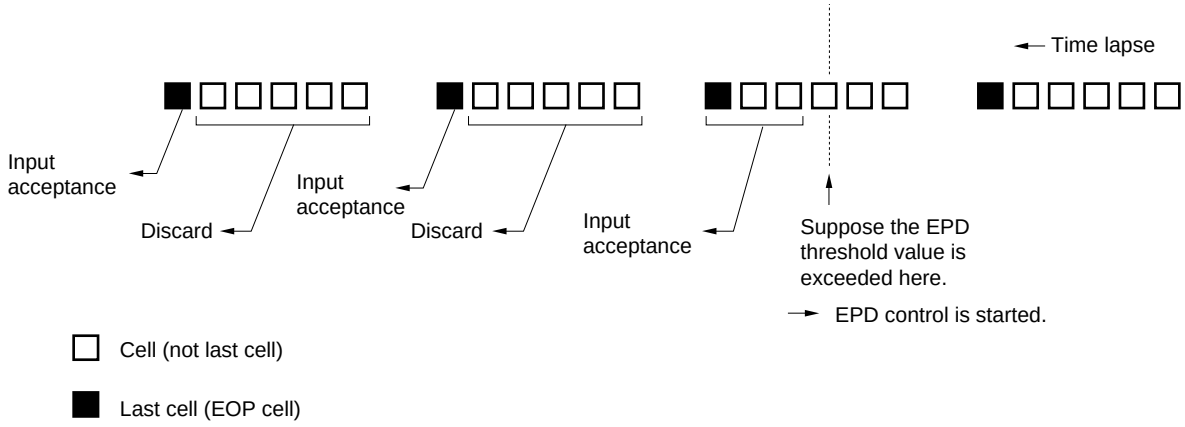
(a) If the cell is included in the packet that has been started to be input when EPD control was started

→ Input cells up to the EOP (End Of Packet) cell that indicates the end of the packet is received.

(b) If the cell is in a packet for which input started after EPD control began

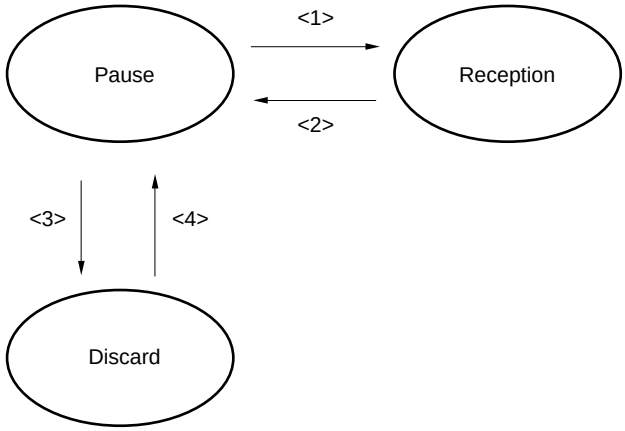
→ The cells of all the packets except the EOP cell are discarded, so that illegal packets are not processed at the reception terminal side by discarding the EOP cell.

Figure 3-39. When EPD Control Is Enabled



The figure below shows the status transition when EPD control is enabled.

Figure 3-40. Status Transition When EPD Control Is Enabled

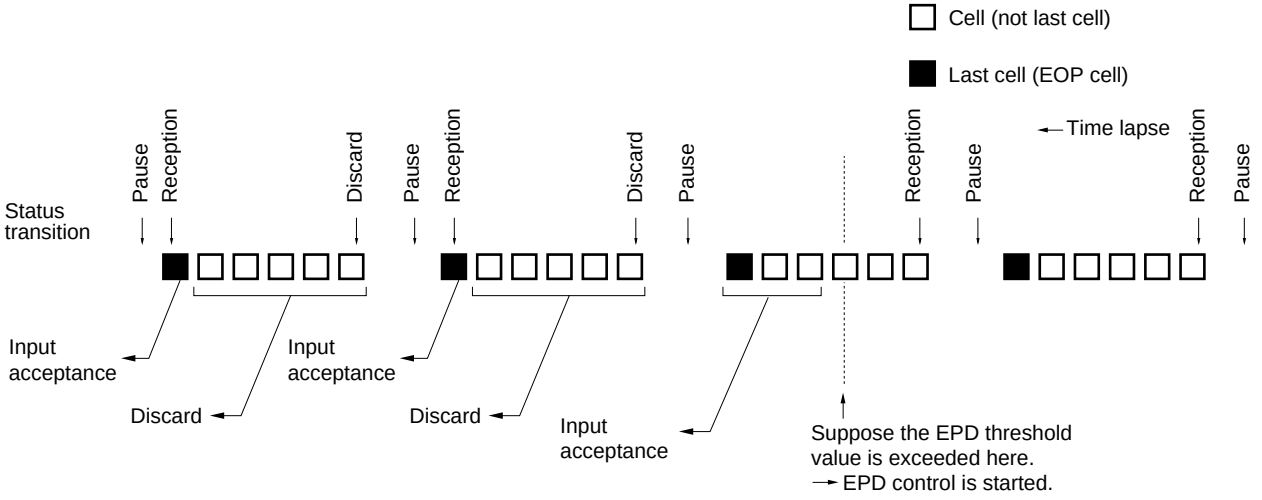


<Processing flow and status transition>

In the initial status, control is paused. If a cell is input in this status, it is checked whether the total number of current cells and output queue length exceed the EPD threshold value.

If the threshold value is not exceeded, the cell is received (<1>); if it is exceeded, the cell is discarded (<3>). When the last cell of the AAL-5 packet is input, control is paused again (<2> and <4>). If the receive status was entered when the first cell of the packet was input, therefore, all the cells are received up to the last cell. If the discard status was entered when the first cell was input, all the cells except the last cell are discarded. The last cell is always received in either status.

Figure 3-41. Status Transition of EPD Control



When receiving packets other than AAL-5, EPD control must be disabled because packets are not managed by using the last cell.

The following tables list the threshold values used for EPD control.

- **EPD threshold values related to total number of cells**

Threshold Value	Description
UCthAEP	EPD threshold value for cell of ABR class
UCthUEP	EPD threshold value for cell of UBR class

- **EPD threshold values related to output queue**

Threshold Value	Description
OQthAEP	EPD threshold value for cell of ABR class
OQthUEP	EPD threshold value for cell of UBR class

Remark A channel for which EPD control is disabled discards cells if the queue length exceeds these threshold values. For ABR and UBR classes, therefore, UCthABR, UCthUBR, OQthABR, and OQthUBR described in **3.13.4 Cell discard by class**, and the threshold values shown above play the role of cell discard threshold values.

(2) When EPD control is disabled

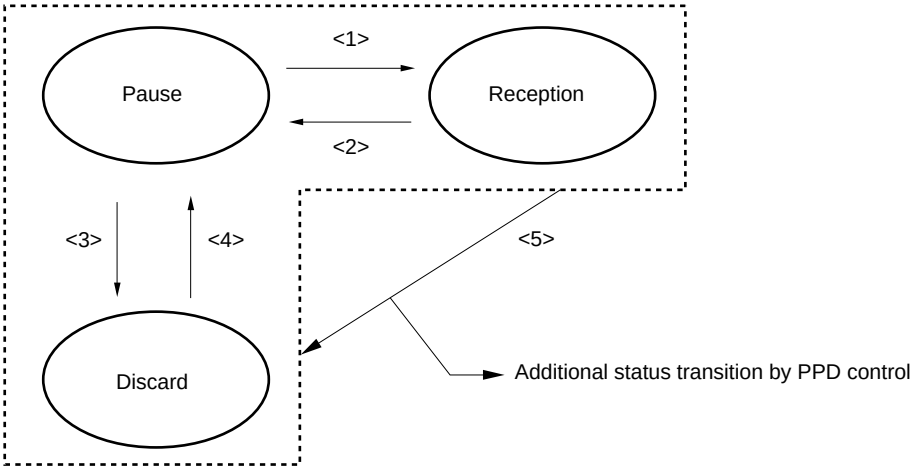
In this case, the above test is not made and the cells are discarded when all the cells in a packet exceed the EPD threshold value.

3.13.6 PPD (Partial Packet Discard) control

With PPD control, if a cell in a packet is discarded, all the subsequent cells in the packet are discarded when they are input. If the EPD threshold value is exceeded and EPD control is effected, therefore, the packet that is already being input is received up to its EOP (End of Packet) cell. If a cell is discarded because a threshold value other than the EPD threshold value is exceeded during reception controlled by the EPD control function, all the cells in the packet, except the EOP cell, are discarded.

Figure 3-42 shows the status transition when PPD control is performed. In contrast to EPD control, PPD control has additional status transition <5> shown in this figure. If a discard threshold value other than the EPD threshold value is exceeded in the reception status of EPD control, the cells are discarded.

Figure 3-42. Status Transition of PPD Control



3.13.7 Minimum queue length

With the shared buffer method, if the class of a specific logical output port is in the congestion status, the threshold values related to the total number of cells (Used Cell Counter) of that class are exceeded. As a result, the cells of the same class at the other logical output ports may be discarded.

To prevent this, the μPD98412 secures a minimum queue length that is not affected by the congestion status of other logical output ports. It also manages the queue length of each class, secures a minimum queue length that is not affected by the congestion status of the other classes, and guarantees the minimum queue length of each class for a cell that exceeds the minimum queue length of each port.

Table 3-4. Minimum Queue Length Related to Total Number of Cells (Used Cell Counter)

Threshold Value Name	Processing during Cell Input
ALLmin	Ensures the specified number of cells exist in the cell buffer to guarantee the minimum queue length. The total of all the minimum queue lengths must be specified. For details of how to calculate this value, refer to **4.2.24 Total number of cells minimum threshold value register**.

Table 3-5. Minimum Queue Length Related to Total Number of Cells of Each Class (Total Cell Counter for Each Class)

Threshold Value Name	Processing during Cell Input
TCminCRV	Guarantees the minimum queue of a class for the CBR/rtVBR cell that exceeds OQminCRV of an output port.
TCminRNV	Guarantees the minimum queue of a class for the RM/nrtVBR cell that exceeds OQminRNV of an output port.
TCminABR	Guarantees the minimum queue of a class for the ABR cell that exceeds OQminABR of an output port.
TCminUBR	Guarantees the minimum queue of a class for the UBR cell that exceeds OQminUBR of an output port.

Table 3-6. Minimum Queue Length Related to Output Queue Length

Threshold Value Name	Processing during Cell Input
OQminCRV	Guarantees minimum queue for CBR/rtVBR cell of each output port.
OQminRNV	Guarantees minimum queue for RM/nrtVBR cell of each output port.
OQminABR	Guarantees minimum queue for ABR cell of each output port.
OQminUBR	Guarantees minimum queue for UBR cell of each output port.

Table 3-7. Minimum Queue Length Related to Multi-Cast Queue

Threshold Value Name	Processing during Cell Input
MQminCRV	Guarantees minimum queue for CBR/rtVBR cell of multi-cast queue.
MQminRNV	Guarantees minimum queue for RM/nrtVBR cell of multi-cast queue.
MQminABR	Guarantees minimum queue for ABR cell of multi-cast queue.
MQminUBR	Guarantees minimum queue for UBR cell of multi-cast queue.

The priority for discarding cells when a threshold value is exceeded is as described below ((1) > (2) > (3) > (4)), and cells are discarded or queued. “Exceeding a threshold value” means the status where queue length ≥ threshold value.

(1) The cell is discarded if the discard threshold value (MAX. threshold value (*1)), the EPD threshold value (*2) of a cell not subject to EPD, or the CLP threshold value (*3) of a cell subject to CLP.
(2) The cell is queued if the minimum threshold value (MIN. threshold value of the output queue or multi-cast queue (*4) or MIN. threshold value (*5) of the total number of cells for each class (Total Cell counter for each class)) is not exceeded.
(3) The cell is discarded if the discard threshold value of the total number of cells (Used Cell Counter) (MAX. threshold value (*6) or the EPD threshold value (*7) of a cell not subject to EPD) is exceeded.
(4) The cell is queued if none of the above conditions are satisfied.

Each threshold value is classified as follows.

Table 3-8. Classification and Names of Threshold Values

Classification		OQ (Output Queue)/ MQ (Multi-cast Queue)	TC (Total Cell Counter for each class)	UC (Used Cell Counter)
Discard threshold value	MAX. threshold value	(*1) OQthCBR, OQthRVR OQthRM, OQthNVR OQthABR, OQthUBR MQthCRV, MQthRNV MQthABR, MQthUBR	—	(*6) UCthCBR, UCthRVR UCthRM, UCthNVR UCthABR, UCthUBR
	EPD threshold value	(*2) OQthAEP, OQthUEP	—	(*7) UCthAEP, UCthUEP
	CLP threshold value	(*3) OQthCCL, OQthRCL OQthACL, OQthUCL	—	—
MIN. threshold value		(*4) OQminCRV, OQminRNV OQminABR, OQminUBR MQminCRV, MQminRNV MQminABR, MQminUBR	(*5) TCminCRV, TCminRNV TCminABR, TCminUBR	—
EFCI threshold value		OQthRCI OQthACI, OQthUCI	—	—

3.13.8 Cell ejection function

The μPD98412 can eject cells congested in the output queue. This function is used to discard cells that are not output due to, for example, a network fault. Ejection is started when the CD bit of a port configuration register (PT0 through PT29) is set. Whether ejection has been completed can be checked by monitoring the queue length. Cells are ejected, one at a time, at the timing adjusted by the other active logical port. While a cell is being ejected, the port configuration register (PT0 to PT29) must not be updated because the setting of the register is referenced.

3.14 ABR Congestion Control

When the μPD98412 detects congestion status, it can report the congestion in the receiver terminal direction by using the EFCI bit of the user cell, and in the transmitter terminal direction by using the CI, NI, and BN bits of the Backward RM cell.

3.14.1 EFCI (Explicit Forward Congestion Indicator)

When the μPD98412 detects congestion status by using the EFCI threshold value, it sets the EFCI bit (PTI = 010, 011) included in the header of the user cell that passes the congestion point to report congestion in the receiver terminal direction. The EFCI bit is set for the cells belonging to the nrtVBR, ABR, and UBR classes.

EFCI control is performed while the output queue length exceeds the EFCI threshold value.

Table 3-9. EFCI Threshold Value Related to Output Queue

Threshold Value Name	Control if Threshold Value Is Exceeded (processing during cell output)
OQthRCI	Performs EFCI marking of user cell of nrtVBR class of corresponding port.
OQthACI	Performs EFCI marking of user cell of ABR class of corresponding port.
OQthUCI	Performs EFCI marking of user cell of UBR class of corresponding port.

The μPD98412 has two modes of EFCI marking. The mode bit is the EF bit of the MODE0 register.

EF Bit	Cell Subject to EFCI Marking
0	All user cells (VPC & VCC, PTI = 000, 001)
1	All user cells in VC connection (VCC, PTI = 000, 001)

3.14.2 RM cell CI/NI marking (Resource Management Cell CI/NI Congestion Indication Marking)

When the μPD98412 detects congestion status of ABR class by using the EFCI threshold value, it sets the CI bit (CI Marking) and NI bit (NI Marking) included in the payload for the Backward RM cell that passes the congestion point, in order to report the congestion in the transmitter terminal direction. The Backward RM cell that passes the congestion point is the Backward cell that is input to the logical input port having the same number as that of the logical output port in the congestion status. Figure 3-43 shows the configuration of the RM cell (Resource Management Cell).

Figure 3-43. RM Cell Configuration (ATM Forum TM Ver. 4.0)

OCTET	FIELD
1 to 5	ATM Header RM-VPC: VCI = 6 and PTI = 110 RM-VCC: PTI = 110
6	RM Protocol Identifier
7	Message Type
8, 9	ER (Explicit Cell Rate)
10, 11	CCR (Current Cell Rate)
12, 13	MCR (Minimum Cell Rate)
14 to 17	QL (Queue Length)
18 to 21	SN (Sequence Number)
22 to 51	Reserved
52, 53	Reserved (6 bits) + CRC-10

7	6	5	4	3	2	1	0
DIR	BN	CI	NI	RA	Rsv.	Rsv.	Rsv.

Message Type Field

DIR = 0 for forward RM cell
= 1 for backward RM cells
BN = 0 for Source Generated RM cells
= 1 for Switch Generated (BECN) RM cells
CI = 0 otherwise
= 1 to indicate congestion
NI = 0 otherwise
= 1 to indicate no additive increase allowed
RA - Not used for ABR (set to zero)

The threshold values to be used are the same as those in **3.14.1 EFCI (Explicit Forward Congestion Indicator)**. CI/NI marking control is performed under the following condition:

- The Backward RM cell is identified as follows while the output queue of ABR class of the logical port that has input the Backward RM cell exceeds the EFCI threshold value.

  For details of how the RM cell is identified, refer to **3.12.8 Routing of RM cell**. A Backward RM cell is a cell with DIR = 1 of the cells identified as RM cells.

Table 3-10. CI Threshold Values Related to Output Queue Length

Threshold Value Name	Control If Threshold Value Is Exceeded (processing during cell input)
OQthACI	Performs CI marking of Backward RM cell input to the corresponding port

The μPD98412 has a bit that masks the CI/NI marking function. This bit is the CI bit of the MODE1 register.

CI Bit	Processing	
0	CI/NI marking function is not masked.	(active)
1	CI/NI marking function is masked.	(inactive)

3.14.3 RM cell merge (Resource Management Cell Merge)

The μPD98412 performs RM cell merge for a backward connection in the multi-cast mode (for details, refer to **3.12.6 Accessing HTT with RM cell.**).

In the case of multi-cast, the Backward RM cells are sent from multiple channels to one channel. The μPD98412 has a mechanism that merges the multiple Backward RM cells into one RM cell.

For connection in the backward direction for multi-cast, as many header translation tables (HTTs) as the broadcast count must be set. RMM = 10 (RM cell merge and transfer) must be set for at least one of the connections, and RMM = 11 (RM cell merge and discard) for the other connections. Then the RM cell merge function can be used.

When the Backward RM cell is sent to the channel set in the multi-cast mode, the CI and NI bits that indicate the congestion status of the channel under management of the μPD98412, and the CI and NI bit of the Backward RM cell are ORed, and the cell is discarded. In the case of a channel of RMM = 10, its CI and NI bits and the CI and NI bits of the Backward RM cell are ORed and the result is transmitted from an output port.

Similarly, the BN bit that indicates what created the RM cell (switch or source) of the corresponding channel under management of the μPD98412 is ORed with the BN bit of the Backward RM cell in the case of a channel of RMM = 11, and the cell is discarded. In the case of a channel of RMM = 10, its BN bit and the BN bit of the Backward RM cell are ORed, and the result is transmitted from an output port.

3.15 WFQ (Weighted Fairness Queue)

3.15.1 General

When a cell is output from an output queue, which cell is to be output is determined by the following two conditions:

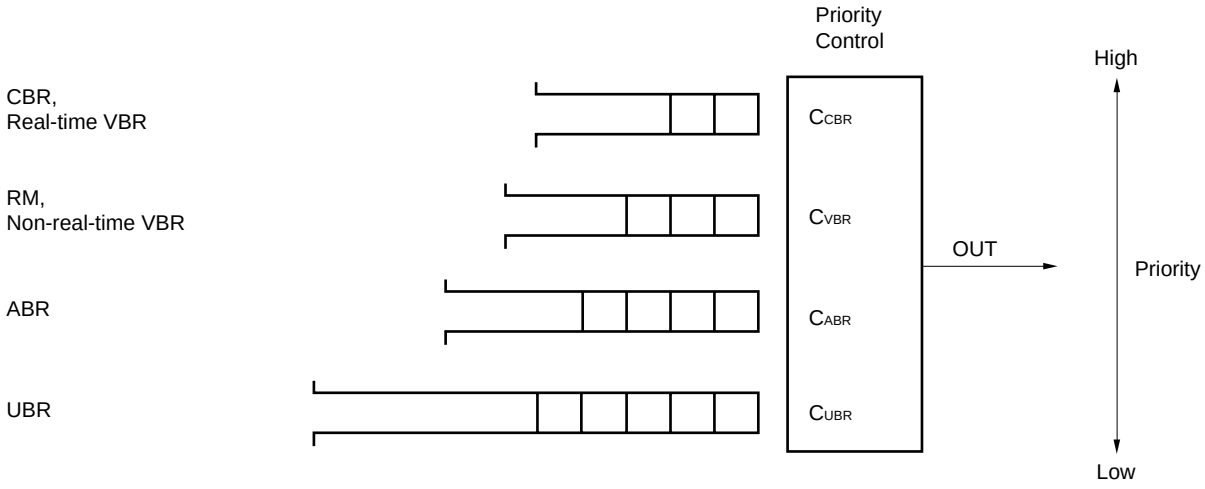
<Output cell determining conditions>

(1) The logical output port to output the cell has been determined.
(2) Of the output queues allocated to the determined logical output port, the service class of the queue from which the cell is taken out has been determined.

Of these conditions, this section explains (2), i.e., how the service class is determined. This method of determination is called the WFQ (Weighted Fairness Queue).

3.15.2 Counters and flags used

Figure 3-44. Output Queue and Counter



The queue of each logical output port of the μPD98412 has the following four queues of service classes.

- Output queue of CBR/rtVBR class
- Output queue of RM/nrtVBR class
- Output queue of ABR class
- Output queue of UBR class

As shown in Figure 3-44, these queues are assigned priorities, and the cells queued are sequentially output to these queues starting from the one with the highest priority. C_{CBR}, C_{VBR}, C_{ABR}, and C_{UBR} are the counters that control these priorities. The initial values of these counters are set as follows:

- C_{CBR}, C_{VBR} ... Number of cells permitted to be output from the corresponding queue in a specific cycle
- C_{ABR}, C_{UBR} ... Ratio of outputting cells of ABR class to cells of UBR class.
  For example, to output cells of ABR class and cells of UBR class at a ratio of 2:1, set C_{ABR} = 2 and C_{UBR} = 1.

C_{CBR}, C_{VBR}, C_{ABR}, and C_{UBR} are set by the class priority control register. In addition, as a counter that counts a specific cycle, a cycle counter is provided.

The differences in setting these counters are due to the differences in the characteristics of the classes. CBR and VBR classes reserve a band, while ABR and UBR classes do not reserve a band but transfer data at the transfer rate that is enabled at a given point. Therefore, C_{ABR} and C_{UBR} only specify a ratio and are not responsible for how many cells are actually output in a specific cycle.

These counters control the priority of each service class according to the following rules:

(1) Cycle counter (8 bits)

- The value 1 is loaded to the counter as the initial value after the counter has been reset.
- The count value of the counter is decremented at every 44 system clocks with the 8-bit UTOPIA interface. With the 16-bit UTOPIA interface, the count value is decremented at every 22 system clocks.
- When the cycle counter register is set, its set value is loaded to the counter.
- When the count value of the counter has reached “1” (time out), the set value of the cycle counter register is loaded to the counter, and the count value is decremented.

(2) C_{CBR} and C_{VBR} (7 bits)

- If the set value (including the initial value) of the class priority control register is changed, the value 127 is loaded to C_{CBR}, and the set value of the class priority control register is loaded to the C_{VBR} counter.
- If congested cells of both CBR and VBR classes exist, the cells of CBR class take precedence and are granted permission to be output. If no congested cells of CBR class exists, the output permission is granted to the cells of VBR class. When cells of CBR and VBR classes are output, the C_{CBR} and C_{VBR} counters are decremented by one.
- When the counter value reaches 0, output from the corresponding service class is prohibited.
- When the count value of the cycle counter reaches “1” (time out), the set value of the class priority control register are added and loaded to the C_{CBR} and C_{VBR} counter.
- If no congestion cells of either CBR and VBR classes exist, or if both the C_{CBR} and C_{VBR} counters reach 0 and output is prohibited, priority control by the C_{ABR} and C_{UBR} counter in (3) is started.

(3) C_{ABR}, C_{UBR} (3 bits)

- The initial value is loaded to these counters when both the counters reach 0, regardless of the cycle counter.
- If congested cells exist in the queues of both ABR and UBR classes, and if both the C_{ABR} and C_{UBR} counters are not 0 (i.e., if output is not prohibited), the two classes are alternately granted output permission. Each time a cell has been output from the corresponding queue, the C_{ABR} and C_{UBR} counters are decremented by one.
- When the value of the counter reaches 0, output from the corresponding service class is prohibited.
  Even if the ABR class has been granted the output permission because the UBR class is prohibited from outputting cells (C_{UBR} = 0), the UBR class is granted the output permission when the ABR class has no congested cells. Similarly, even if the UBR class has been granted the permission because output of the ABR class is prohibited (C_{ABR} = 0), the ABR class is permitted to output cells if the UBR class has no congested cells.
- After priority control by the C_{ABR} and C_{UBR} counters has been started, priority control by the C_{CBR} and C_{VBR} counters is started again in the following timing:

  (1) Time out of cycle counter if C_{CBR} = 0 and C_{VBR} = 0
  (2) If cells are congested in CBR and VBR classes if $C_{CBR} \neq 0$ or $C_{VBR} \neq 0$

3.16 Peak Rate Shaping Function

The μPD98412 has a simple peak rate shaping function for each logical output port. This shaping function takes effect on the transfer throughput per UTOPIA interface that is determined by SWCLK, and not on the transfer rate of the UTOPIA interface that is determined by UCLK3 through UCLK0.

The transfer throughput per UTOPIA interface and the transfer throughput after shaping are calculated as follows with one basic operation cycle consisting of 44 SWCLK for the 8-bit UTOPIA interface and of 22 SWCLK for the 16-bit UTOPIA interface:

- For 8-bit UTOPIA interface
  Transfer throughput [bps] = SWCLK frequency [Hz] ÷ 44 [SWCLK] × 53 [octet] × 8 [bits]
- For 16-bit UTOPIA interface
  Transfer throughput [bps] = SWCLK frequency [Hz] ÷ 22 [SWCLK] × 53 [octet] × 8 [bits]

Transfer throughput after shaping [bps] = Transfer throughput [bps] ÷ (SPR + 1)

For example, when the 8-bit UTOPIA interface is used where SWCLK = 33 MHz and SPR = 3, a cell is output once in four basic cycles (SPR + 1 = 4), and the transfer throughput after shaping is 79.5 Mbps.

When two or more logical output ports connected to the same UTOPIA interface simultaneously issue a cell transmission request, an output conflict occurs. As a result, the transfer throughput of the logical output port that cannot output data drops. The μPD98412 prevents this drop in transfer throughput by using a shaping error correction function to shorten the next cell transfer interval of the logical output port that could not output data by the number of basic cycles (N) kept waiting by the output conflict (SPR + 1 – N).

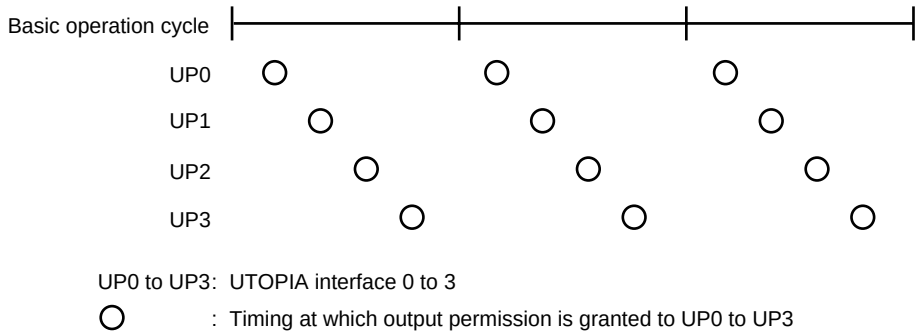
The following sections, **3.16.1** and **3.16.2**, explain an example for a 8-bit UTOPIA interface in the 12-PHY polling mode. The differences between this mode and the other modes are explained in **3.16.3**.

3.16.1 General

(1) UTOPIA interface and logical output port

The μPD98412 has four UTOPIA interfaces conforming to UTOPIA Level2. The relationship between the output enable timing of each UTOPIA interface and the internal basic cycle operation of the μPD98412 is as shown below.

Figure 3-45. Relationship between Internal Basic Cycle and Output Enable Timing of Each UTOPIA Interface



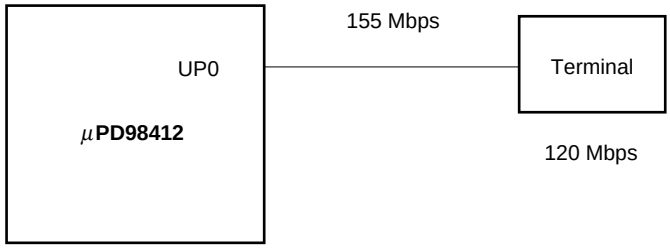
As shown in Figure 3-45, each UTOPIA interface is allocated once in one cycle. Assuming that a cell is always output when each UTOPIA interface is allocated, one UTOPIA interface has a transfer capability of 318M bps (where SWCLK Rate is 33 MHz).

Moreover, the μPD98412 can connect multiple PHY device connection allowing up to 30 logical output ports. Because the transfer rate of one UTOPIA interfere is limited by the value described in **3.1 UTOPIA Interface**, however, the total of the transfer rate of the logical output ports allocated to one UTOPIA interface must be equal to or less than this value.

(2) Peak rate shaping function

For example, suppose the μPD98412 and a terminal are connected as shown below.

Figure 3-46. Example of Connection between μPD98412 and Terminal



- Maximum transfer rate of UTOPIA interface of μPD98412: 318M bps
- Circuit rate: 155M bps
- Processing capability of receiver terminal: 120M bps
- Only one logical output port (LP0) is allocated to the UTOPIA interface (UP0).

If the μPD98412 outputs cells at 155M bps at this time, the transfer rate must be lowered to 120M bps at the μPD98412 side because the terminal cannot keep up with this transfer rate. To control the transfer rate in this way, the peak rate shaping function is used.

The peak rate shaping function controls the transfer rate by limiting allocation by the μPD98412 of the UTOPIA interface to logical output ports in each operation cycle of the μPD98412. Because the transfer rate is 318M bps when cells are output in each basic operation cycle, as described in **(1) UTOPIA interface and logical output port**, the UTOPIA interface should be allocated once in three cycles in order to lower the transfer rate to 120M bps.

The details of this control operation are described next.

3.16.2 Details

(1) Shaping rate

To control whether the UTOPIA interface is allocated to logical output ports in each cycle, the following counter and register are provided.

- Ct counter : Counter for shaping rate control
- SPR register: Shaping rate setting register ($0 \leq SPR \leq 255$)
  ... Limits transfer rate of output to 1/(SPR + 1).

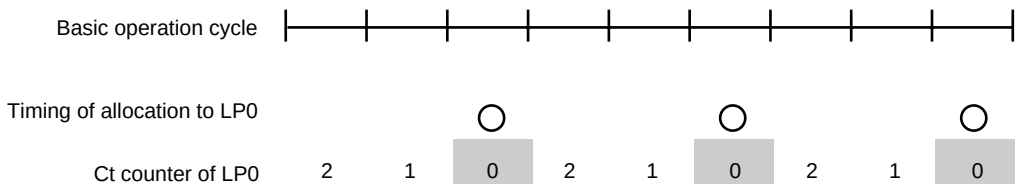
In the example in Figure 3-46, the transfer rate is limited to 1/(1 + 2) if SPR is set to 2. As a result, 318 × 1/3 = 106M bps, satisfying the limit of 120M bps. What processing is performed to allocate the UTOPIA interface to a logical output port once in three cycles is explained next.

The Ct counter is updated according to the following rules, and the interface is allocated to a logical output port when Ct = 0.

- The initial value (value of SPR) is loaded to the Ct counter as soon as the interface has been allocated to a logical output port.
- The value of the Ct counter is decremented by one if the interface is not allocated to a logical output port ($Ct \neq 0$). The output permission is allocated when Ct = 0.

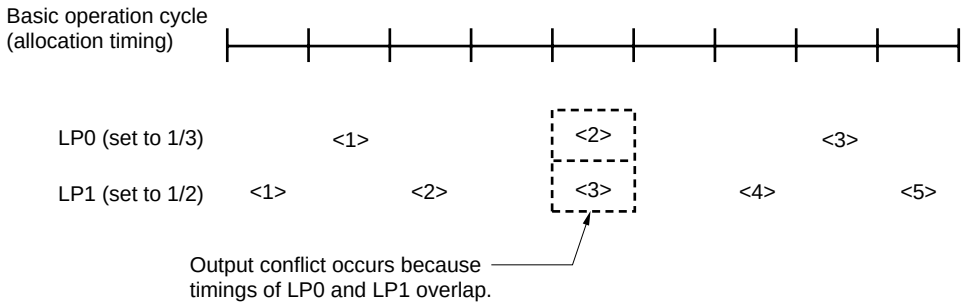
The relationship between the basic cycle, allocation of a logical output port, and the counter value is shown below.

Where SPR = 2 and the initial value of Ct = 2, the transfer rate is limited to 1/(SPR + 1) = 1/3.



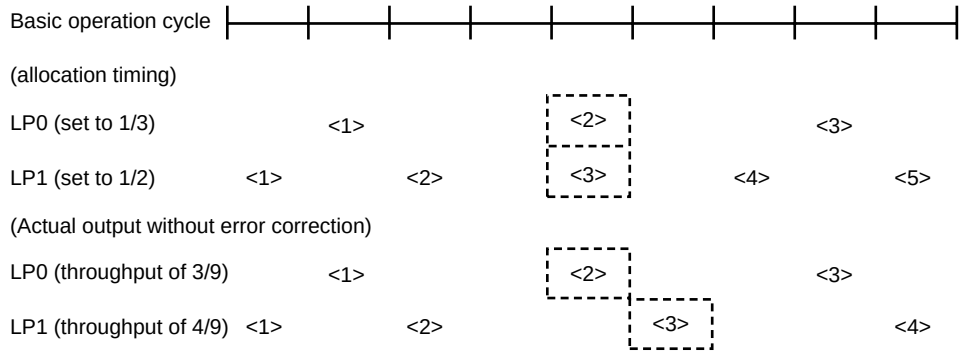
(2) Shaping error correction

If multiple logical output ports LP0 through LPn are connected to one UTOPIA interface, UP0, the timing of allocating the interface to the output ports overlap as shown below (output conflict occurs), dropping the throughput.



The μPD98412 has a shaping error correction function to prevent the throughput from being dropped by the output conflict. This function is described below.

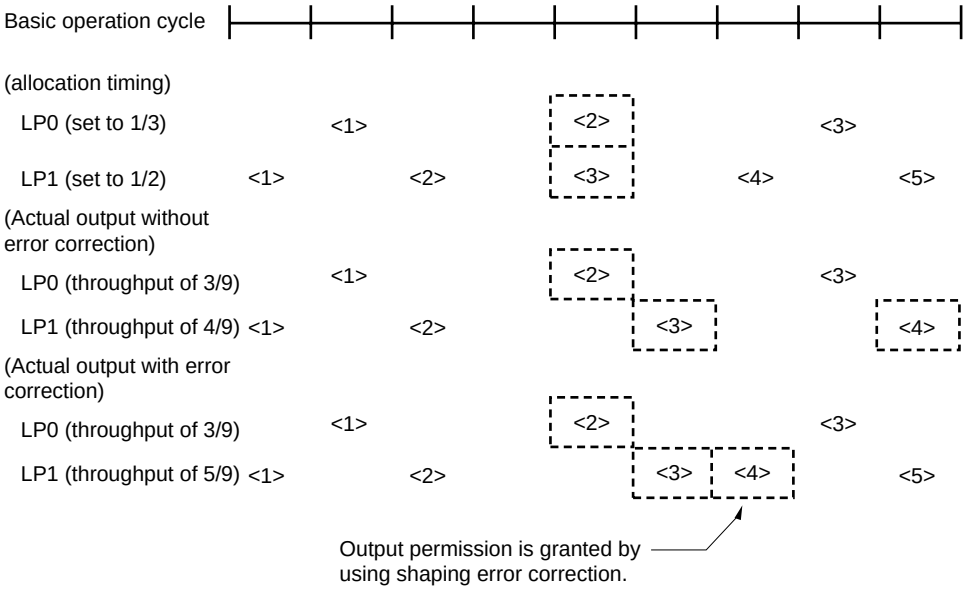
If the shaping error correction function is not used, the throughput drops as follows:



In the cycle next to the one in which cell <2> is output by LP0 in case of an output conflict, cell <3> is output by LP1 to prevent the conflict. After that, LP1 counts down the basic cycle of SPR + 1, is granted the output permission when Ct = 0, and outputs cell <4>. As a result, the actual throughput drops from the throughput set to LP1 (1/2 $\rightarrow$ 4/9).

This drop in throughput due to the output conflict can be prevented by using the shaping error correction function.

The operation is as follows:



The processing performed to carry out the above control is explained below. First, a new counter, Cs, is used to correct the shaping error.

Cs: Counter to control shaping error correction

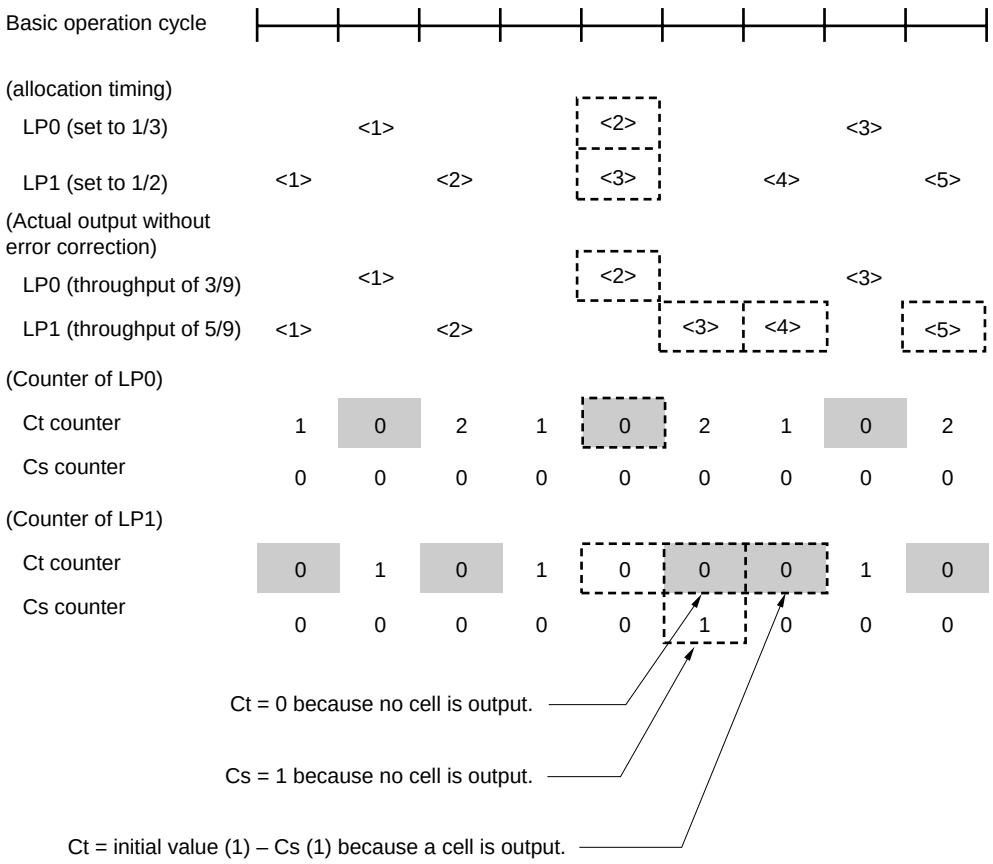
This shaping error correction counter Cs is updated according to the following rule, and the UTOPIA interface is allocated to a logical output port when Ct = 0.

- Cs = 0 if a cell can be output when the interface is allocated to a logical output port (Ct = 0).
- Cs = Cs + 1 if a cell cannot be output when the interface is allocated to a logical output port (Ct = 0), where $0 \leq Cs \leq 11$.

Counter Ct is updated as follows for shaping:

- Ct = Ct – 1 when the interface is not allocated to a logical output port ($Ct \neq 0$).
- If a cell can be output when the interface is allocated to a logical output port (Ct = 0), initial value (SPR) – Cs is loaded to the Ct counter. If no cell can be output even if the interface is allocated to a port, the Ct counter remains 0.

At this time, the counter changes as shown below.



Ct can take 12 values, 0 to 11. The reason for this explained next.

In the examples presented above, LP1 is allocated in the next output cycle. If more logical output ports are connected, however, a conflict with the other logical output ports may occur (at this time, Ct is counted up further and the next cycle is started). Because the μPD98412 allows up to 12 logical output ports to be allocated to one UTOPIA interface in 12-PHY polling mode, a logical output port can be allocated to the UTOPIA interface at least once if it waits for 12 cycles at most. For this reason, Ct can take 12 values.

3.16.3 Shaping error correction

The maximum value of shaping error correction of the μPD98412 differs as follows, depending on the polling mode:

12-PHY polling mode	11 cycles
15-PHY polling mode	14 cycles
Multiplexed status polling mode	29 cycles
2-group weighted polling mode	29 cycles
1-group weighted polling mode	29 cycles

3.17 Interrupt Request

This section explains the interrupt requests made by the μPD98412 to the microprocessor.

3.17.1 Parity error

The μPD98412 checks the HTT & control memory and cell buffer for parity error. If a parity error is detected, the μPD98412 issues an interrupt request to the microprocessor.

Even if the parity error is detected, the μPD98412 continues operation. However, the subsequent header translation and switching operation are not guaranteed. Therefore, the microprocessor must reset the μPD98412 immediately.

(a) HTT & control memory

One parity bit is generated and checked for every 8 bits of 32-bit data.

(b) Cell buffer

One parity byte is generated and checked for 54 bytes of stored cells (storage header: 6 bytes, payload: 48 bytes).

3.17.2 FIFO control error

The μPD98412 inputs cells in accordance with the UTOPIA Level2 interface. If the internal input/output FIFO of the μPD98412 overruns or underruns, the μPD98412 stores the status of the UTOPIA reception interface port in question in a monitor register (UTPSTAT register), and issues an interrupt request to the microprocessor.

If a FIFO control error is detected, cell loss occurs, but the switching operation of the other UTOPIA interfaces continue. If the relationship between the UTOPIA clock and system clock does not satisfy the condition explained in **3.1 UTOPIA Interface**, the FIFO control error occurs.

3.17.3 Queue pointer error

The μPD98412 organizes a queue that manages the cell buffer in the control memory as described in **3.13 Queue Control**, and issues an interrupt request to the microprocessor when malfunctioning of the internal queue control block of the μPD98412 is detected.

If a queue pointer error is detected, the QE bit of the status register indicates the error, and the subsequent header translation and switching operation are not guaranteed.

If no error is indicated by the CE bit of the status register, and an error is indicated only by the QE bit, the possible causes are as follows. Check the setting of the μPD98412.

- The initial value of the ALLmin register is not the value calculated by the following expression.
  (OQminCRV + OQminRNV + OQminABR + OQminUBR) × enabled ports[Note] + MQminCRV + MQminRNV + MQminABR + MQminUBR + TCminCRV + TCminRNV + TCminABR + TCminUBR

  Note "enabled ports" indicates the total number of logical ports that are scheduled to enable the EN bit of the PT register.

- The ALLmin register is re-set after the switching operation of the CMD register is enabled.
- Each minimum threshold value register is re-set after the switching operation of the CMD register is enabled.
- The test area is rewritten by an I/O register access.

3.17.4 Cast count error

The μPD98412 issues an interrupt request to the microprocessor if it detects malfunctioning of the idle queue management block or the multi-cast count management block.

If a cast count error is detected, it is indicated by the CE bit of the status register, and the subsequent header translation and switching operation cannot be guaranteed. A possible cause of this is the user's software procedure. Check the setting of the μPD98412.

If an error is indicated by the CE and QE bits of the status register, the following causes are possible. Check the setting of the μPD98412.

- The cell buffer memory is rewritten by mistake because the HC bit of the mode register is not disabled after self-diagnosis of the cell buffer memory has been completed.
- The test area is rewritten by an I/O register access.

3.17.5 Cell buffer memory shortage

With the μPD98412, the area of the cell buffer memory that stores cell data runs short if the percentage of multi-cast is too high. If the shortage occurs, cells are not stored. Therefore, cells are discarded and discarded cells are counted, and an interrupt request is issued to the microprocessor.

Even if the cell buffer memory has run short, if enough area becomes available in the cell buffer memory, normal operation is restored and the switching operation continues. If the average broadcast count of all the congested cells is greater than 2, the cell buffer memory shortage may take place.

3.17.6 Control memory shortage

As described in **3.13 Queue Control**, the μPD98412 organizes a queue for cell buffer management in the control memory. If the percentage of multi-cast is too high, the control memory may run short before the cell buffer. Should this happen, cells are not stored. Consequently, cells are discarded and discarded cells are counted, and an interrupt request is issued to the microprocessor.

Even if the cell control memory has run short, if enough area becomes available in the control memory, the normal operation is restored and the switching operation continues. If the average broadcast count of all the congested cells is greater than 2, the control memory shortage may take place.

3.17.7 HEC/CRC error

The μPD98412 performs an HEC check and CRC-10 check on input cells. If HM of the MODE1 register is set to 1, however, HEC check is not performed and HEC error cells pass. If an HEC error/CRC-10 error is detected, the corresponding cell is discarded, the corresponding logical input port number is stored in the monitor register, and an interrupt request is issued to the microprocessor. The microprocessor reads the cause register (ERHEC register) and determines the logical input port of the cell responsible for the HEC error/CRC-10 error.

Even if an HEC error/CRC-10 error is detected, the switching operation for the other cells continues.

★ In addition, the μPD98412 provides notification of HEC errors without performing auto-correction, even in the case of a 1 bit HEC error.

(a) HEC check error (header error check)

The μPD98412 performs an HEC check on input cells and HEC generation for output cells.

(b) RM cell CRC-10 error

The μPD98412 performs a CRC-10 check if it detects that the input cell is a Backword RM cell. It also performs CRC-10 generation for an output cell to rewrite the value of the payload. A “Backward RM cell” means a cell having DIR = 1 among cells identified as an RM cell by the method described in **3.12.8 Routing of RM cell**.

3.17.8 Header translation error

If the μPD98412 detects a header translation error as a result of accessing the header translation table (HTT) when a cell is input, it discards the corresponding cell, stores the logical input port number in the monitor register (ERHT) register, and issues an interrupt request to the microprocessor.

Even if a header translation error occurs, the switching operation for the other cells continue.

(a) Invalid header translation

If an attempt is made to access HTT, exceeding the HTT area allocated to the corresponding port, a header translation error occurs. This happens if it is detected that the invalid block of VPI and VCI of the input cell is not “0”. However, in the case of a channel set for connection of UNI by the HT0 through HT29 registers, the GFC field (4 bits) of the input cell is treated as “don’t care”.

(b) Invalid channel

If it is detected that the corresponding channel is set invalid (CEN = 0) as a result of an HTT access, a header translation error occurs.

(c) Invalid output port

If it is detected that the corresponding output port is set invalid (PT register EN = 0) when an attempt is made to output a cell to the logical output port obtained as a result of an HTT access, a header translation error occurs.

(d) Invalid RM cell merge

If it is detected that a channel is set invalid (CEN = 0) or single cast (CM = 0) as a result of an HTT access of the channel at the output destination when backward RM cells are merged, a header translation error occurs.

The μPD98412 has a bit that masks the IC error by using an unassigned cell. The IC error is a type of HTT error. The mask bit is the UA bit of the MODE1 register.

UA Bit	Processing
0	Does not mask IC error
1	Masks IC error

Remark The μPD98412 defines unassigned cells as follows:
GFC = 0, VPI = 0, VCI = 0, CLP = 0.

3.17.9 Exceeding buffer threshold value

If cells are congested in the cell buffer exceeding each threshold value, the μPD98412 selects and discards the corresponding input cells by means of priority cell discard control and EPD control, stores the type and class of the corresponding threshold value, and the logical output port number in the monitor register (EXTH register), and issues an interrupt request to the microprocessor.

Even when a cell is discarded, the switching operation for the other cells continues.

3.17.10 Multi-cast bitmap error

If the μPD98412 detects a multi-cast bitmap error when there are multi-cast congested cells, it holds the source of the multi-cast bitmap error in the multi-cast bitmap error indication register and issues an interrupt request to the microprocessor.

Even after the μPD98412 has detected a multi-cast bitmap error, it continues switching operation for the other cells.

(a) Invalid output port

If a logical output port is invalidated (EN of PT register = 0) when a cell is re-queued to the logical output port from an obtained multi-cast bitmap, a multi-cast bitmap error is detected. In this case, the cell in question is discarded.

(b) Invalid bitmap

If the obtained multi-cast bitmap is not re-queued to any logical output port (MB = “0”), a multi-cast bitmap error is detected. In this case, the cell in question is discarded.

(c) Invalid broadcast count

If broadcast count increases or decreases when there are multi-cast congested cells, a multi-cast bitmap error is detected. In this case, the cell in question is discarded, until there are no more cells for the connection in question.

Caution If the source of the multi-cast bitmap error is (a) Invalid output port or (b) Invalid bitmap, the μPD98412 sets the IM bit of the header conversion error indication register to maintain compatibility with the μPD98410, and generates the header conversion error interrupt.

3.18 Monitoring

3.18.1 Monitor register

The μPD98412 stores the numbers of ports responsible for errors (except for parity errors) in the monitor registers. A value valid when an error occurs is stored in each register. The values of these registers do not change until the microprocessor clears the status bits.

The following information is stored in the monitor registers.

- Type and class of threshold value that is exceeded, and logical output port number
- Number of the logical input port that input a cell in which a header translation error was detected
- Number of the logical port that input a cell in which an HEC error or CRC-10 error was detected
- Number of the port of the UTOPIA interface in which an input port overrun error was detected

3.18.2 Cell discard count due to exceeded threshold value

The μPD98412 selects and discards an input cell by means of priority cell discard control and EPD control if cells are congested in the cell buffer, exceeding each threshold value. It can monitor the number of discarded cells over any period under any conditions.

(a) Monitor condition

The following conditions can be assigned to registers.

- Specification of threshold value: MAX. threshold value/CLP threshold value/EPD threshold value
- Class specification : CBR/rtVBR/RM/nrtVBR/ABR/UBR
- Port number : Specification of logical output port number

(b) Monitor period

Counting is started when the count enable (EN) bit is set to “1”, and is stopped when EN is reset to “0”.

(c) Indication of number of discarded cells

The number of discarded cells is indicated by the number of discarded cells register when monitoring is completed. If the maximum count is reached and then a new cell is discarded, the counter is reset to 0, and continues counting. In this case, the status register indicates that the cell discard counter overflowed.

- Maximum count : FFFFFFFFh ($2^{32} – 1$)

3.18.3 Cell discard count due to header translation error

The μPD98412 discards cells when a header translation error occurs for an input cell. It can monitor the number of discarded cells over any period under any logical input port conditions.

(a) Monitor condition

The following conditions can be assigned to a register.

- Port number: Specification of logical input port number

(b) Monitor period

Counting is started when the count enable (EN) bit is set to “1”, and is stopped when EN is reset to “0”.

(c) Indication of number of discarded cells

The number of discarded cells is indicated by the number of discarded cells register when monitoring is completed. If the maximum count is reached and then a new cell is discarded, the counter is reset to 0, and continues counting. In this case, the status register indicates that the cell discard counter overflowed.

- Maximum count: FFFFFFFFh ($2^{32} – 1$)

3.18.4 Cell discard count due to HEC error or CRC error

The μPD98412 discards cells when an HEC error or CRC error occurs. It can monitor the number of discarded cells over any period under any logical input port conditions.

(a) Monitor condition

The following condition can be assigned to a register.

- Port number: Specification of logical input port number

(b) Monitor period

Counting is started when the count enable (EN) bit is set to “1”, and is stopped when EN is reset to “0”.

(c) Indication of number of discarded cells

The number of discarded cells is indicated by the number of discarded cells register when monitoring is completed. If the maximum count is reached and then a new cell is discarded, the counter is reset to 0, and continues counting. In this case, the status register indicates that the cell discard counter overflowed.

- Maximum count: FFFFFFFFh ($2^{32} – 1$)

Caution The cell discard count due to HEC errors is not counted if it is specified by the MODE1 register that cells causing an HEC error should be passed.

3.18.5 Cell discard count due to control/cell buffer memory shortage

The μPD98412 discards cells if the vacant control area of the HTT & control memory or vacant area of the cell buffer memory runs short. It can monitor the number of discarded cells over any period under any logical input port conditions.

(a) Monitor condition

The following condition can be assigned to a register.

- Cause of error: Control/cell buffer memory shortage

(b) Monitor period

Counting is started when the count enable (EN) bit is set to “1”, and is stopped when EN is reset to “0”.

(c) Indication of number of discarded cells

The number of discarded cells is indicated by the number of discarded cells register when monitoring is completed. If the maximum count is reached and then a new cell is discarded, the status register is updated, the counter is reset to 0, and continues counting. In this case, the status register indicates that the cell discard counter overflowed.

- Maximum count: FFFFFFFFh ($2^{32} – 1$)

3.18.6 Counting number of received cells

The μPD98412 can monitor the number of cells received by the UTOPIA interface port over any period.

(a) Monitor condition

The following condition can be assigned to a register.

- UTOPIA interface port number: UTOPIA0/1/2/3

(b) Monitor period

Counting is started when the count enable (EN) bit is set to “1”, and is stopped when EN is reset to “0”.

(c) Indication of number of received cells

The number of received cells is indicated by the number of input cells register when monitoring is completed. If the maximum count is reached and then a new cell is received, the counter is reset to 0, and continues counting. In this case, the status register indicates that the cell input counter overflowed.

- Maximum count: FFFFFFFFh ($2^{32} – 1$)

3.18.7 Input cell monitoring function

The μPD98412 can count the number of cells of a specific service class input from a specific logical port.

The μPD98412 also has a function for counting input cells in VP and VC units.

(a) Monitoring conditions

The following conditions can be set by using the CTENINP0 through CTENINP3 registers:

- Port number : Logical input port number
- Class : Service class
- Counted objects : HTT access addresses of input cells

(b) Monitoring period

The cell counter is started when the count enable (EN) bit of the CTENINP0 through CTENINP3 registers is set to 1.

The counter is stopped when the bit is cleared to 0.

(c) Indication of number of input cells

The number of input cells is indicated by the input cell count registers (CTINP0 through CTINP3). If a cell is input after the number of input cells has reached the maximum count value of the register, the register is reset to 0, and counting continues. In this case, the overflow of the input cell counter is indicated by the status register.

- Maximum count: FFFFFFFFh ($2^{32} - 1$)

(d) Remark

Cells discarded due to occurrence of a HEC error, CRC error, or header conversion error are not counted.

If a virtual logical input port number is obtained from a cell header when a cell is input from the microprocessor connection port (if the VLPNP field of the SRLP register is not 0), the cell is counted when a virtual logical input port number is set as a monitoring condition. If a virtual logical input port number cannot be obtained from the cell header, the cell is counted when the microprocessor connection port is set as a monitoring condition.

Cells that are discarded because the threshold value is exceeded are counted.

3.18.8 Queue length monitoring function

The μPD98412 can monitor the number of cells (queue length) of the output/multi-cast queue specified for each class.

(a) Monitoring conditions

Assign the following parameters to the MONQL register as monitoring conditions:

- Queue type
  Specify an output queue or multi-cast queue.

- Port number
  Specify the value of the logical port number 0 to 29 of the output queue. If a multi-cast queue is specify as the queue type, set this field to 0.

- Queue class
  Specify any of the following queue classes:

  CBR/rtVBR queue
  RM/nrtVBR queue
  ABR queue
  UBR queue

(b) Queue length indication

The current queue length can be read each time the MONQL register has been read.

3.18.9 Multi-cast congested cell monitoring function

In multi-cast connection, the μPD98412 can monitor the number of congested cells referencing HTT Area-B specified by the multi-cast bitmap pointer (MBP). This function is used to confirm that no congested cell is referencing HTT Area-B when HTT Area-B is to be rewritten.

(a) Monitoring condition

Set a multi-cast bitmap pointer (MBP) to the MONNMC register.

(b) Indication of number of congested cells

The current number of congested cells can be read each time the MONNMC register has been read.

3.18.10 Empty flag of cell buffer

The μPD98412 has a cell buffer empty flag that is the EC bit of the status register.

EC bit	Status
0	Cell buffer is not empty.
1	Cell buffer is empty.

When the status register is read, the EC bit indicates the current status of the cell buffer.

3.19 Microprocessor Interface

The microprocessor can access the HTT & control memory and cell buffer memory via the μPD98412, in addition to the internal I/O registers of the μPD98412.

- I/O registers : Initial setting, command issuance, status check, etc.
- HTT & control memory : Initial setting, connection setting to HTT, self-diagnosis
- Cell buffer memory : Self-diagnosis

The μPD98412 supports 32-bit multiplexed synchronous bus for connecting a microprocessor. These buses are general-purpose bus interfaces that require fewer external circuitry than ordinary I/O buses (PCI Bus, S Bus, A Bus, AP Bus, and 86 Bus).

Table 3-11. Microprocessor Interface Pin

32-bit Multiplexed Synchronous Bus
HCLK (Processor bus clock)
R/W_B (Read/Write mode)
UWE_B (Upper word enable)
AD [31:0] (Address/Data bus)
IOCS_B (I/O chip select)
MCS_B (Memory chip select)
INT (Interrupt request)
RDY_B (Bus ready)

3.19.1 I/O mapping and memory mapping

When IOCS_B is asserted active, the I/O registers are selected. When MCS_B is asserted active, the external memory is selected. Either the HTT & control memory or cell buffer memory is selected as the external memory by the HC bit of the memory mode register.

Table 3-12. Selecting Subject to Access

IOCS_B Pin	MCS_B Pin	HC Bit of Memory Mode Register	Subject to Access	Offset Address
				32-bit bus
1	1	Don't care	Setting prohibited	Setting prohibited
0	1	Don't care	I/O register	0000h - 7FFFh
1	0	1	HTT & control memory	000000h - 0FFFFFh
		0	Cell buffer memory	000000h - 3FFFFFh
0	0	Don't care	Setting prohibited	Setting prohibited

The microprocessor can access the μPD98412 in 32-bit units. However, it can write data to the cell buffer memory only in 88-bit units. The data written by the processor to the cell buffer memory is temporarily stored in the temporary internal register of the μPD98412, and written to the cell buffer in 88-bit units as soon as CB [31:0] has been written. Therefore, be sure to write data of 1 word or 88 bits to the cell buffer and write CB [31:0] last.

Table 3-13. Access Bit Width for Each Access Type

Access Type	Read Operation	Write Operation
I/O register	32 bits	32 bits
HTT & control register	32 bits	32 bits
Cell buffer memory	32 bits	88 bits (92 bits when passing through the UDF field)

To write data to address CBA [17:0] = 00000h in 32-bit units, write AD [21:0] = 000008h, 000004h, and 000000h in that order.

Write data “0” to the unused area provided for future expansion. This area should be undefined when read.

Caution Do not access the μPD98412 in 8-bit units. If data is written in 8-bit units or 24-bit units, the undefined status on the data bus lines that are not driven is written to the remaining 8 bits of a word pair, and the operation is not guaranteed.

Figure 3-47. I/O Register Mapping

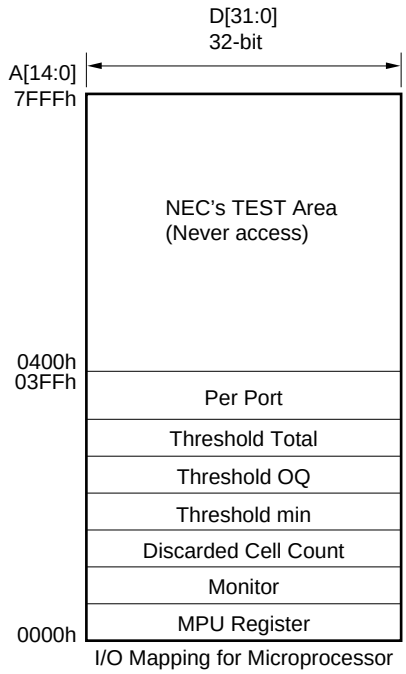
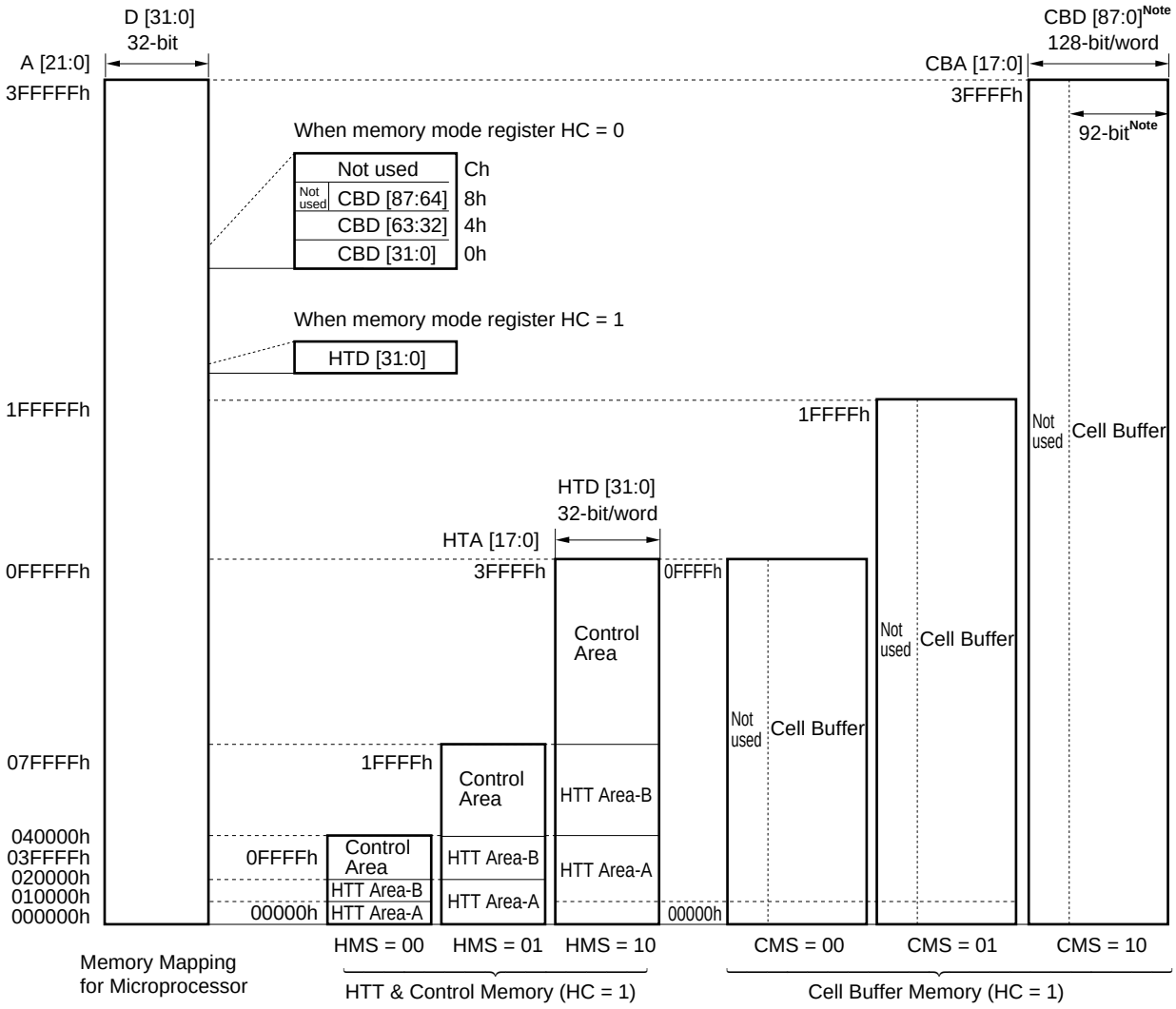


Figure 3-48. HTT & Control Memory and Cell Buffer Memory Mapping



Note Cell Buffer memory is 92 bits wide when passing through the UDF field, and 88 bits wide when not passing through the UDF field.

3.19.2 32-bit multiplexed synchronous bus

If the HSEL input pin is low at hardware reset, the 32-bit multiplexed synchronous bus is selected as the bus interface.

(1) Endian

The microprocessor bus is set to little endian as the default condition after reset. To connect a microprocessor with a big endian interface, set the BL bit of the memory read register to “1”.

The μPD98412 controls access by using AD1 (address) and UWE_B as follows. To UWE_B, a negative logic high-order word valid signal or a negative logic 4-byte valid signal can be connected.

(a) Little endian access (BL = “0”)

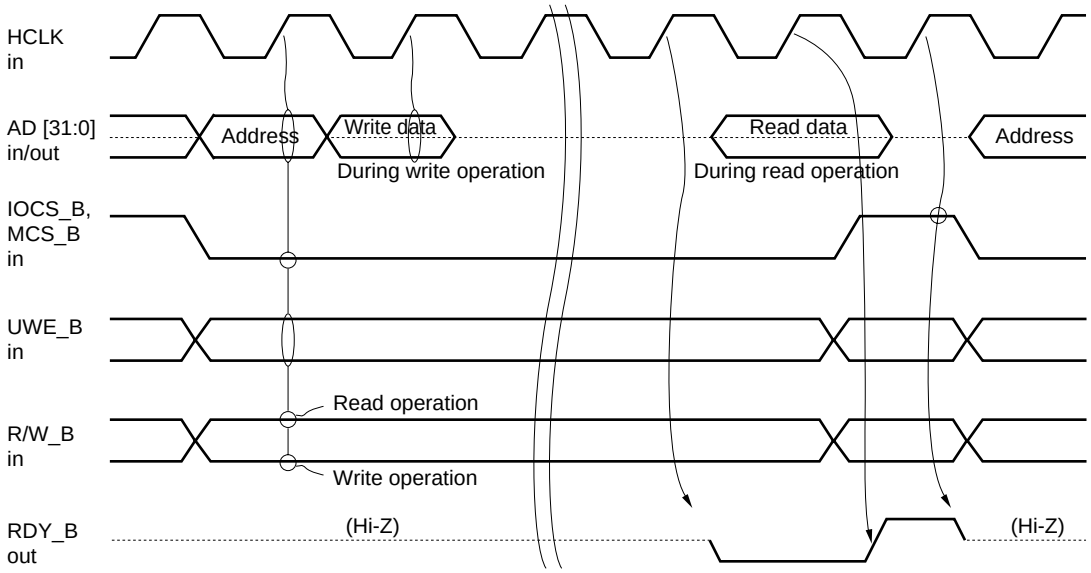
Address	UWE_B	Data	
AD1		AD [31:16]	AD [15:0]
0	0	bit [31:16]	bit [15:0]
0	1	Invalid	bit [15:0]
1	0	bit [31:16]	Invalid
1	1	bit [31:16]	Invalid

(b) Big endian access (BL = “1”)

Address	UWE_B	Data	
AD1		AD [31:16]	AD [15:0]
0	0	bit [31:16]	bit [15:0]
0	1	bit [31:16]	Invalid
1	0	Invalid	bit [15:0]
1	1	Invalid	bit [15:0]

(2) Access timing

Figure 3-49. Access Timing of 32-Bit Multiplexed Synchronous Bus



When IOCS_B or MCS_B is asserted, AD [31:0], UWE_B, and R/W_B are loaded in synchronization with the rising of HCLK, and the register or memory at the address indicated by AD [31:0] is accessed.

If R/W_B is high, a read operation is started. When data output is ready, the data is output to AD [31:0] in synchronization with the rising of HCLK, and RDY_B is asserted. When the microprocessor has received the data and negates IOCS_B and MCS_B, the μPD98412 negates RDY_B, and AD [31:0] go into a high-impedance state. At the next rising of HCLK, RDY_B goes in to a high-impedance state.

If R/W_B is low, a write operation is started. The data on AD [31:0] is loaded in synchronization with the next rising of HCLK, and RDY_B is asserted when the operation in the next bus cycle is ready. When the microprocessor negates IOCS_B and MCS_B, the μPD98412 negates RDY_B, and RDY_B goes into a high-impedance state at the next rising of HCLK.

3.20 External Memory Interface

3.20.1 HTT & control memory interface

A memory with 1 word being 36 bits wide (32 bits + 4-bit parity) and a depth of 64K words is connected as the HTT & control memory. This memory can be expanded along with the cell buffer, and 128K word and 256K word memories can be connected. This memory stores the HTT (Header Translation Table) and cell addresses (idle queue/output queue/multi-cast queue).

The μPD98412 translates headers by using the HTT. It accesses the HTT for inputting cells, multi-cast re-queuing, and outputting cells. The HTT must be created by the microprocessor in accordance with a predetermined format.

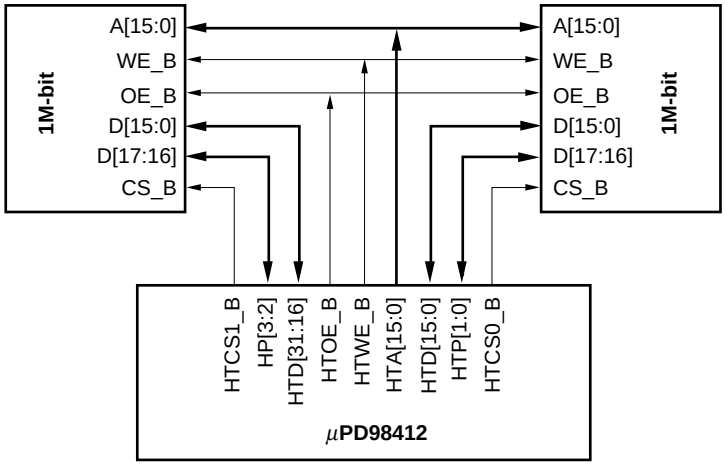
Caution The microprocessor can always access the HTT even while the μPD98412 is performing a switching operation, but a wait signal of up to 16 system clocks is inserted, until access by the microprocessor is enabled.

The μPD98412 controls cell buffers using the control memory. It stores a pointer in a cell buffer (a value 1/5 of CBA [17:0]) in 16-bit width.

Because the microprocessor runs memory diagnostics as necessary after reset, the memory can be accessed. After running the memory diagnostics, the HTT & control memory must be selected by setting the HC bit of the MODE1 register to “1”. While the switching operation is enabled, the microprocessor can access the external memory only to access the header translation table (HTT). The control memory must not be accessed.

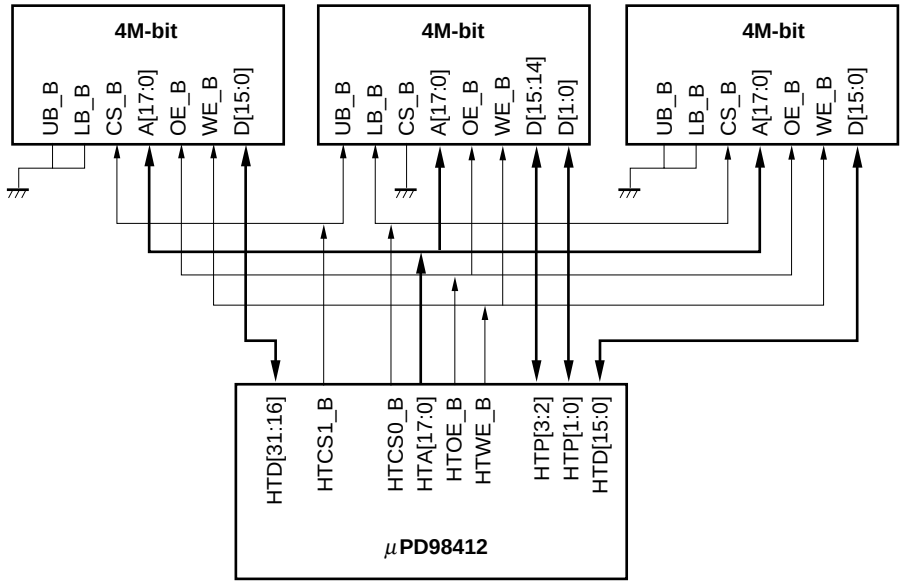
★ **Caution The μPD98412 does not automatically clear the external memory to all “0” when the power is turned on or during reset. To avoid incorrect operation, clear the external memory to all “0” from the CPU for HTT and control memory.**

Figure 3-50. Example of Connecting HTT & Control Memory (Minimum Configuration)



If the HTT & control memory is configured to its maximum size, two memories of 256K words × 18 bits, or three or four 256K word × 16 bit memories are used. If 256K word × 16 bit memories that can control byte data (e.g., μPD434016AL) are used, only three memories are required.

Figure 3-51. Example of Connecting HTT & Control Memory (Maximum Configuration)



3.20.2 Cell buffer interface

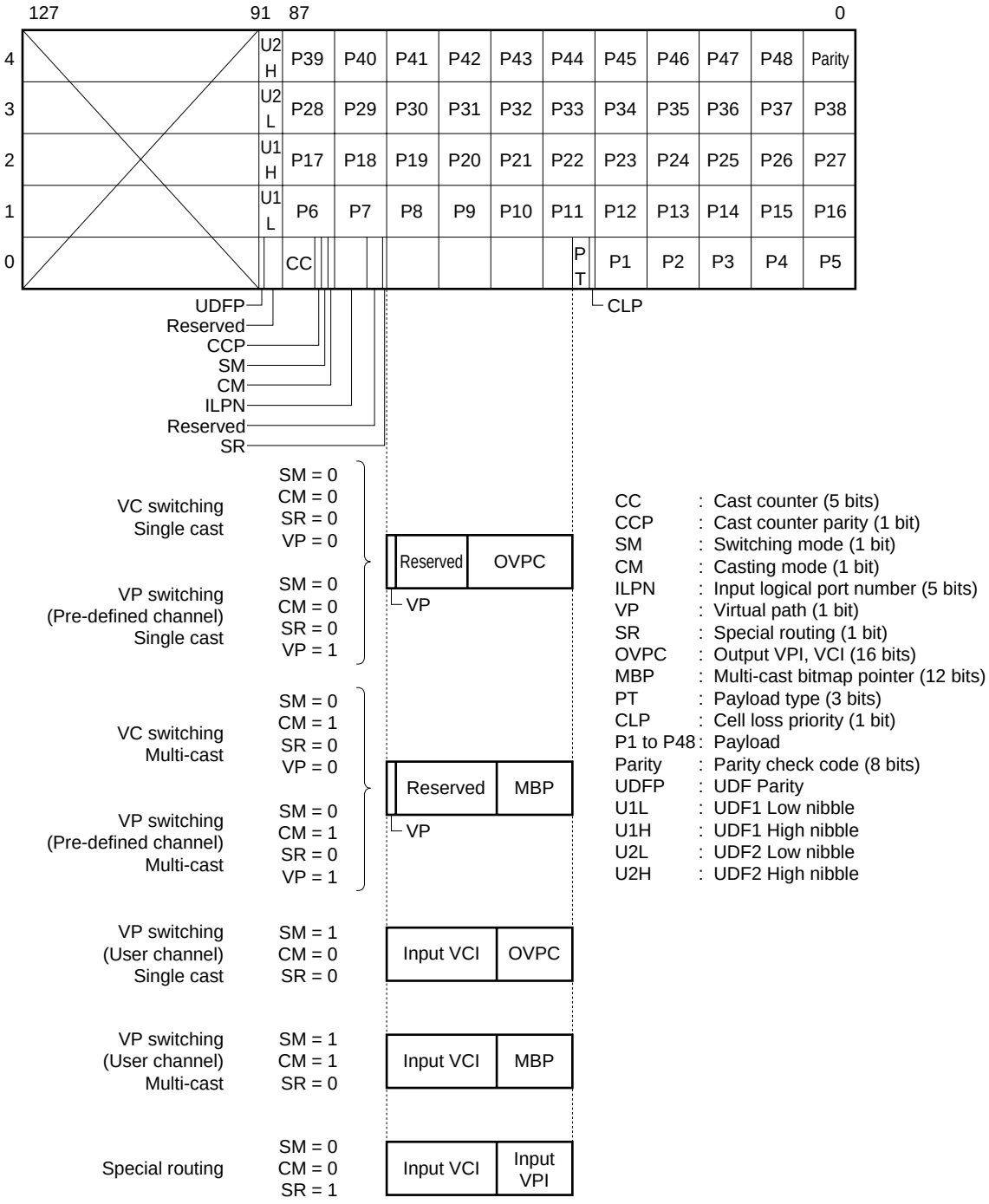
The μPD98412 uses the cell buffer memory as a shared buffer.

As the cell buffer memory, a memory with 1 word being 88 bits wide (92 bits wide when passing through the UDF field) and a depth of 64K words (128K words/256K words when expanded) is connected. For expansion, connect a memory with the same depth to the HTT & control memory. Cells are in the format shown in Figure 3-52 and have 55 bytes per cell, and are stored in the cell buffer.

When not passing through the UDF field, the μPD98412 writes the cell buffer memory in 5 cycles and reads in 6 cycles in 88-bit units. One of the read cycles is actually a write cycle in which the cast counter (CC) is decremented and written back. The CBCS1_B signal is a write enable signal that writes CC and CCP (parity) for this write cycle. If an SRAM 18 bits wide is connected as the cell buffer memory, it is recommended that CBCS1_B be connected to the memory to which CBD[87:72] is connected. Because CBD[87:70] are driven when CC is written back, CBCS1_B can be connected to CBD[87:82] to CBD[87:70] depending on the type of the SRAM to be connected.

Because the microprocessor performs memory diagnostics as necessary after reset, the memory can be accessed. After the memory diagnostics have been completed, it is necessary to set the HC bit of the MODE register to “1” and select the HTT & control memory before issuing a command to the CMD register. The microprocessor can access the external memory only to access the header translation table (HTT) while the switching operation is enabled.

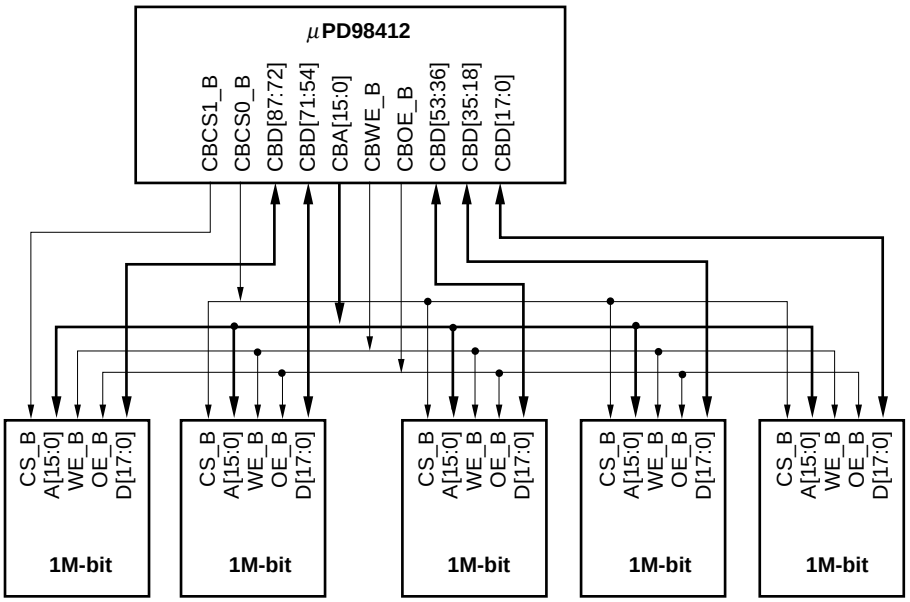
★ **Figure 3-52. Cell Buffer Storage Format**



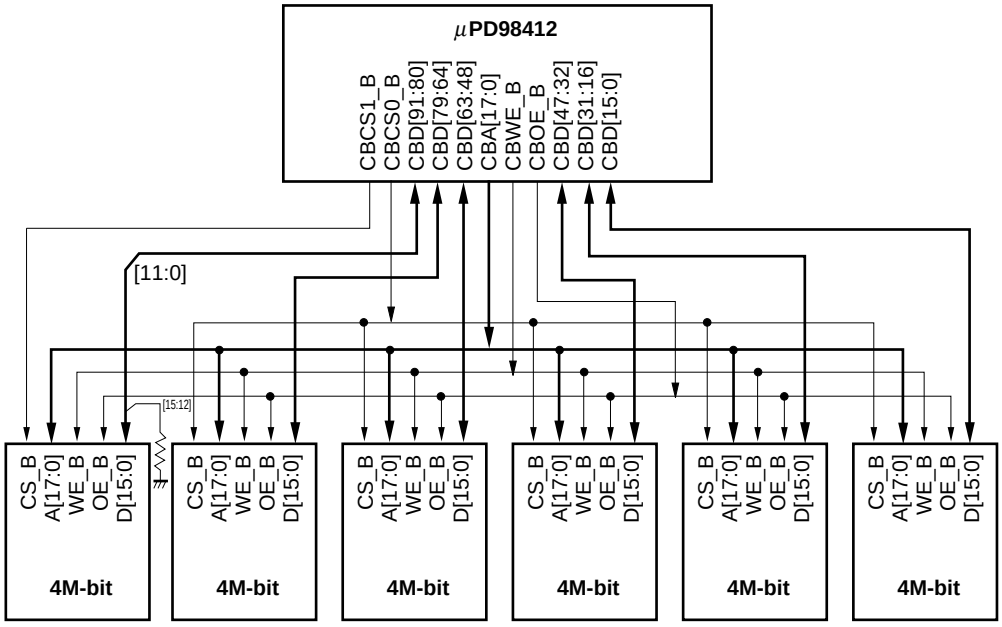
CC : Cast counter (5 bits)
CCP : Cast counter parity (1 bit)
SM : Switching mode (1 bit)
CM : Casting mode (1 bit)
ILPN : Input logical port number (5 bits)
VP : Virtual path (1 bit)
SR : Special routing (1 bit)
OVPC : Output VPI, VCI (16 bits)
MBP : Multi-cast bitmap pointer (12 bits)
PT : Payload type (3 bits)
CLP : Cell loss priority (1 bit)
P1 to P48 : Payload
Parity : Parity check code (8 bits)
UDFP : UDF Parity
U1L : UDF1 Low nibble
U1H : UDF1 High nibble
U2L : UDF2 Low nibble
U2H : UDF2 High nibble

Figure 3-53. Example of Connecting Cell Buffer Memory

(a) Minimum configuration when UDF field transmission is not performed



(b) Maximum configuration when UDF field transmission is not performed



4.1 Register List

(1/3)

Address	Register Name	Function	Bit	R/W	Section No.
0000h	CMD	Command	16	R/W	4.3.1
0004h	MODE0	Mode 0	16	R/W	4.3.2
0006h	MODE1	Mode 1	16	R/W	4.3.3
0008h	INTMASK	Interrupt mask	32	R/W	4.3.4
000Ch	STATUS	Status	32	R/W	4.3.5
0010h	EXTHMS	Threshold value exceeding discard indication mask	32	R/W	4.3.6
0014h	EXTH	Threshold value exceeding discard indication	32	R	4.3.7
0018h	ERHT	Header translation error discard indication	16	R	4.3.8
001Ah	ERHEC	HEC/CRC error discard indication	16	R	4.3.9
001Ch	UTPSTAT	UTOPIA status	16	R	4.3.10
001Eh	ERMB	Multi-cast bitmap error indication	16	R	4.3.11
0020h	CTENTH	Threshold value exceeding discard cell count enable	32	R/W	4.3.12
0024h	CTENHT	Header translation error discard cell count enable	16	R/W	4.3.13
0026h	CTENHEC	HEC/CRC error discard cell count enable	16	R/W	4.3.14
0028h	CTENMEM	Control/cell buffer memory shortage discard cell count enable	16	R/W	4.3.15
002Ah	CTENRCV	Receive cell count enable	16	R/W	4.3.16
002Ch	CTRCV	Receive cell count	32	R/W	4.3.17
0030h	CTEXTH	Threshold value exceeding discard cell count	32	R/W	4.3.18
0034h	CTERHT	Header translation error discard cell count	32	R/W	4.3.19
0038h	CTERHEC	HEC/CRC error discard cell count	32	R/W	4.3.20
003Ch	CTMEMEMP	Control/cell buffer memory shortage discard cell counter	32	R/W	4.3.21
0040h	OQminCRV	CBR + rtVBR class output queue minimum threshold value	16	R/W	4.3.22
0044h	OQminRNV	RM + nrtVBR class output queue minimum threshold value	16	R/W	
0048h	OQminABR	ABR class output queue minimum threshold value	16	R/W	
004Ch	OQminUBR	UBR class output queue minimum threshold value	16	R/W	
0050h	MQminCRV	CBR + rtVBR class multi-cast queue minimum threshold value	16	R/W	4.3.23
0054h	MQminRNV	RM + nrtVBR class multi-cast queue minimum threshold value	16	R/W	
0058h	MQminABR	ABR class multi-cast queue minimum threshold value	16	R/W	
005Ch	MQminUBR	UBR class multi-cast queue minimum threshold value	16	R/W	

(2/3)

Address	Register Name	Function	Bit	R/W	Section No.
0060h	TCminCRV	CBR + nrVBR class TC (Total Cell) counter minimum threshold value	16	R/W	4.3.24
0064h	TCminRNV	RM + nrtVBR class TC (Total Cell) counter minimum threshold value	16	R/W	
0068h	TCminABR	ABR class TC (Total Cell) counter minimum threshold value	16	R/W	
006Ch	TCminUBR	UBR class TC (Total Cell) counter minimum threshold value	16	R/W	
007Eh	ALLmin	Total number of cells minimum threshold value (total number of minimum guaranteed cells of each output queue, multi-cast queue, and TC counter)	16	R/W	4.3.25
0080h	OQthCBR	CBR class output queue maximum threshold value	16	R/W	4.3.26
0082h	OQthRVR	rtVBR class output queue maximum threshold value	16	R/W	
0086h	OQthCCL	CLP threshold value of CBR + rtVBR class output queue	16	R/W	4.3.29
0090h	OQthRM	RM class output queue maximum threshold value	16	R/W	4.3.26
0092h	OQthNVR	nrtVBR class output queue maximum threshold value	16	R/W	
0094h	OQthRCI	EFCI threshold value of RM + nrtVBR class output queue	16	R/W	4.3.28
0096h	OQthRCL	CLP threshold value of RM + nrtVBR class output queue	16	R/W	4.3.29
00A0h	OQthABR	ABR class output queue maximum threshold value	16	R/W	4.3.26
00A2h	OQthAEP	EPD threshold value of ABR class output queue	16	R/W	4.3.27
00A4h	OQthACI	EFCI threshold value of ABR class output queue	16	R/W	4.3.28
00A6h	OQthACL	CLP threshold value of ABR class output queue	16	R/W	4.3.29
00B0h	OQthUBR	UBR class output queue maximum threshold value	16	R/W	4.3.26
00B2h	OQthUEP	EPD threshold value of UBR class output queue	16	R/W	4.3.27
00B4h	OQthUCI	EFCI threshold value of UBR class output queue	16	R/W	4.3.28
00B6h	OQthUCL	CLP threshold value of UBR class output queue	16	R/W	4.3.29
00C0h	MQthCRV	CBR + rtVBR class multi-cast queue maximum threshold value	16	R/W	4.3.30
00C4h	MQthRNV	RM + nrtVBR class multi-cast queue maximum threshold value	16	R/W	
00C8h	MQthABR	ABR class multi-cast queue maximum threshold value	16	R/W	
00CCh	MQthUBR	UBR class multi-cast queue maximum threshold value	16	R/W	
00D0h	UCthCBR	CBR class UC (Used Cell) counter maximum threshold value	16	R/W	4.3.31
00D4h	UCthRVR	rtVBR class UC (Used Cell) counter maximum threshold value	16	R/W	
00D8h	UCthRM	RM class UC (Used Cell) counter maximum threshold value	16	R/W	
00DCh	UCthNVR	nrtVBR class UC (Used Cell) counter maximum threshold value	16	R/W	
00E0h	UCthABR	ABR class UC (Used Cell) counter maximum threshold value	16	R/W	
00E2h	UCthAEP	EPD threshold value of ABR class UC (Used Cell) counter	16	R/W	4.3.32
00E8h	UCthUBR	UBR class UC (Used Cell) counter maximum threshold value	16	R/W	4.3.31
00EAh	UCthUEP	EPD threshold value of UBR class UC (Used Cell) counter	16	R/W	4.3.32

(3/3)

Address	Register Name	Function	Bit	R/W	Section No.
Note 1	PT0 - PT29	Port configuration	32	R/W	4.3.33
Note 2	PC0 - PC29	Class priority control	32	R/W	4.3.34
01FCh	PERIOD	Cycle count	16	R/W	4.3.35
Note 3	HT0 - HT29	Header translation configuration	32	R/W	4.3.36
027Ch	SMA	Switching mode area setting	16	R/W	4.3.37
0280h	MONQL	Queue length monitor	32	R/W	4.3.38
0284h	MONNMC	Multi-cast congested cell monitor	32	R/W	4.3.39
0288h	SRLP	Special routing logical port	16	R/W	4.3.40
028Ah	SRFLT	Special routing filter	16	R/W	4.3.41
Note 4	UTPCFG0-3	UTOPIA configuration	32	R/W	4.3.42
Note 5	CTENINP0-3	Input cell count enable	32	R/W	4.3.43
Note 6	CTINP0-3	Input cell count	32	R/W	4.3.44

Notes 1. 0100h, 0104h, 0108h, 010Ch, 0110h, 0114h, 0118h, 011Ch, 0120h, 0124h, 0128h, 012Ch, 0130h, 0134h, 0138h, 013Ch, 0140h, 0144h, 0148h, 014Ch, 0150h, 0154h, 0158h, 015Ch, 0160h, 0164h, 0168h, 016Ch, 0170h, 0174h

2. 0180h, 0184h, 0188h, 018Ch, 0190h, 0194h, 0198h, 019Ch, 01A0h, 01A4h, 01A8h, 01ACh, 01B0h, 01B4h, 01B8h, 01BCh, 01C0h, 01C4h, 01C8h, 01CCh, 01D0h, 01D4h, 01D8h, 01DCh, 01E0h, 01E4h, 01E8h, 01ECh, 01F0h, 01F4h

3. 0200h, 0204h, 0208h, 020Ch, 0210h, 0214h, 0218h, 021Ch, 0220h, 0224h, 0228h, 022Ch, 0230h, 0234h, 0238h, 023Ch, 0240h, 0244h, 0248h, 024Ch, 0250h, 0254h, 0258h, 025Ch, 0260h, 0264h, 0268h, 026Ch, 0270h, 0274h

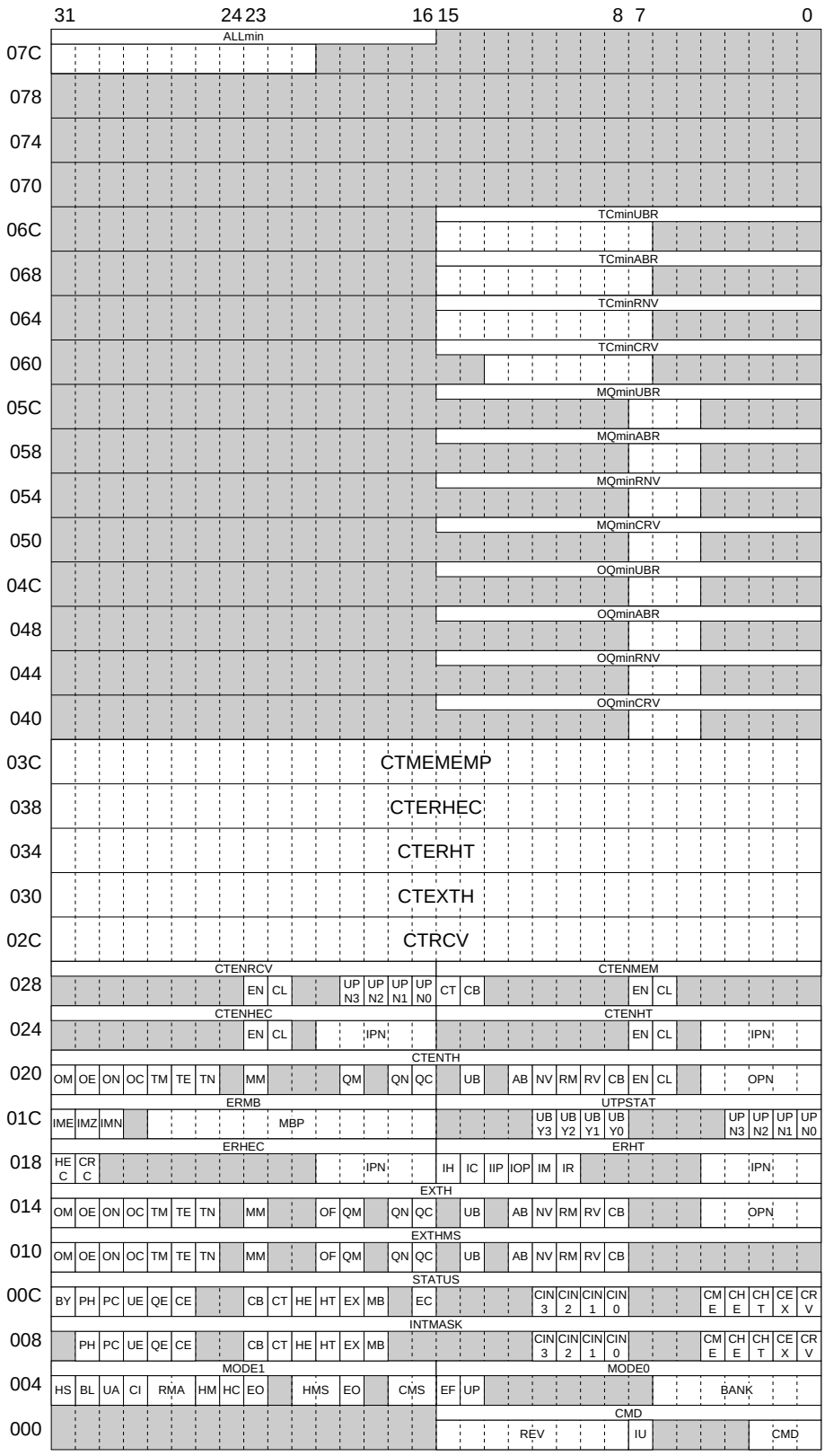
4. 0290h, 0294h, 0298h, 029Ch

5. 02A0h, 02A4h, 02A8h, 02ACh

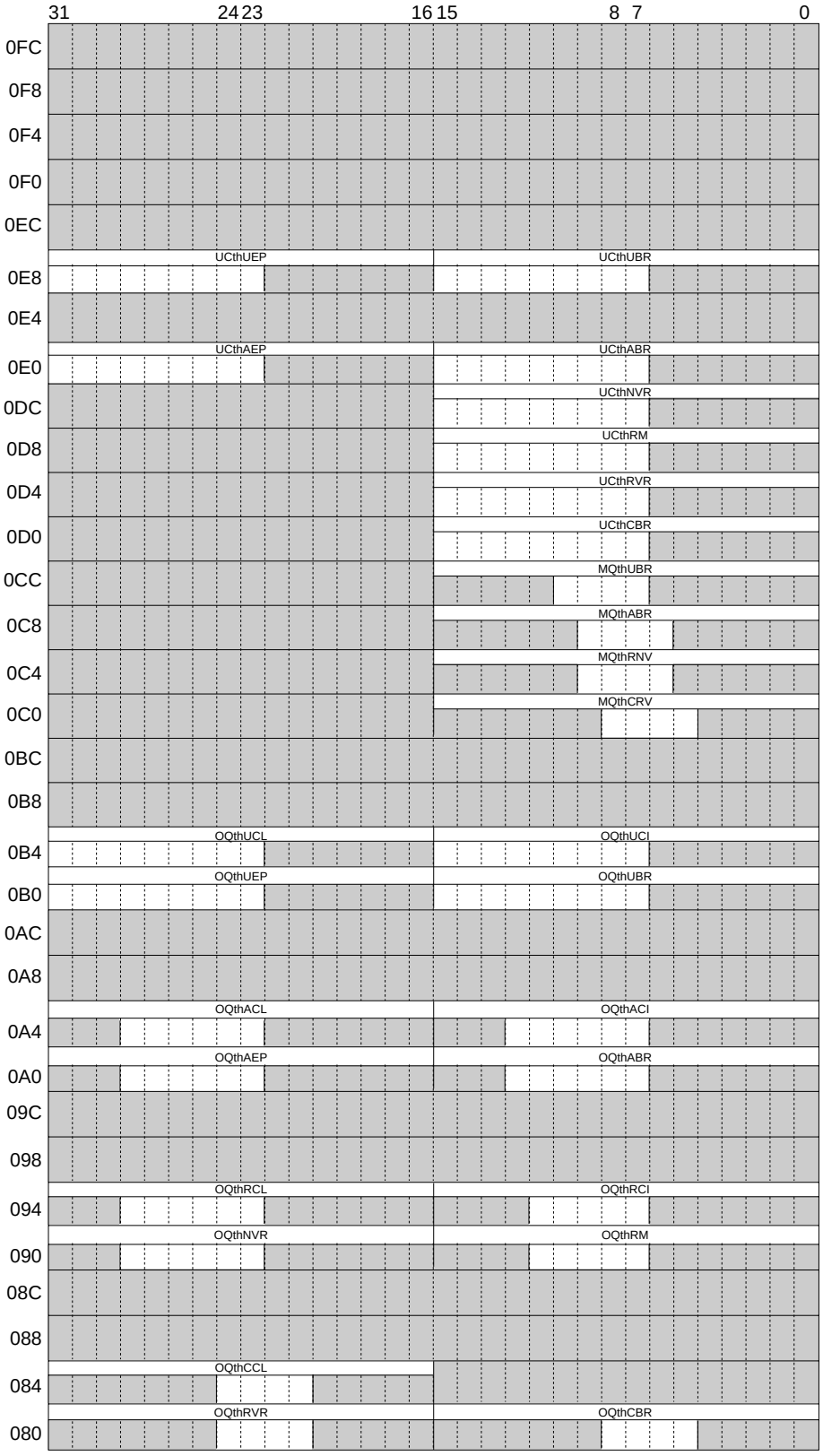
6. 02B0h, 02B4h, 02B8h, 02BCh

4.2 Register Map

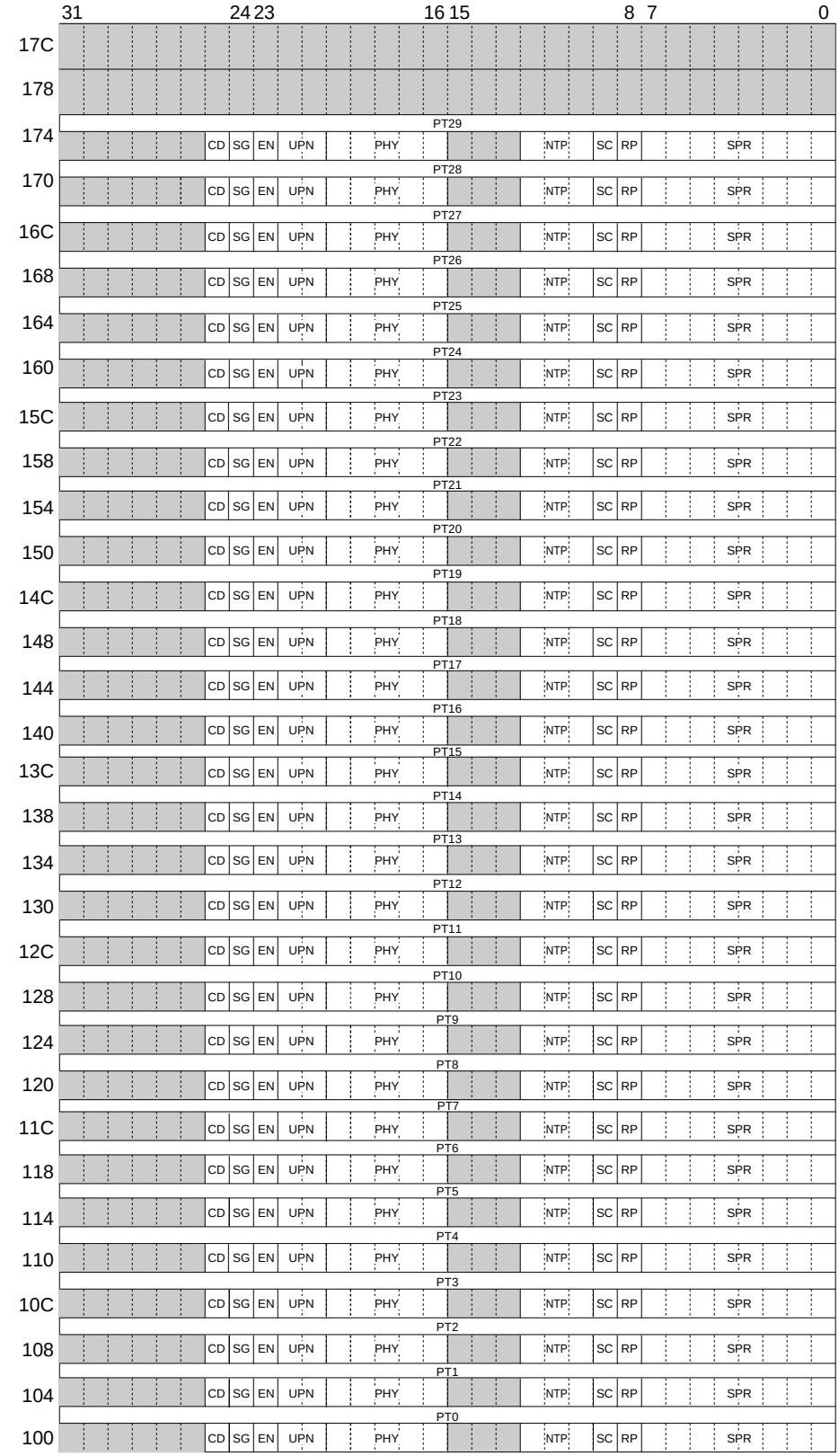
(1/6)



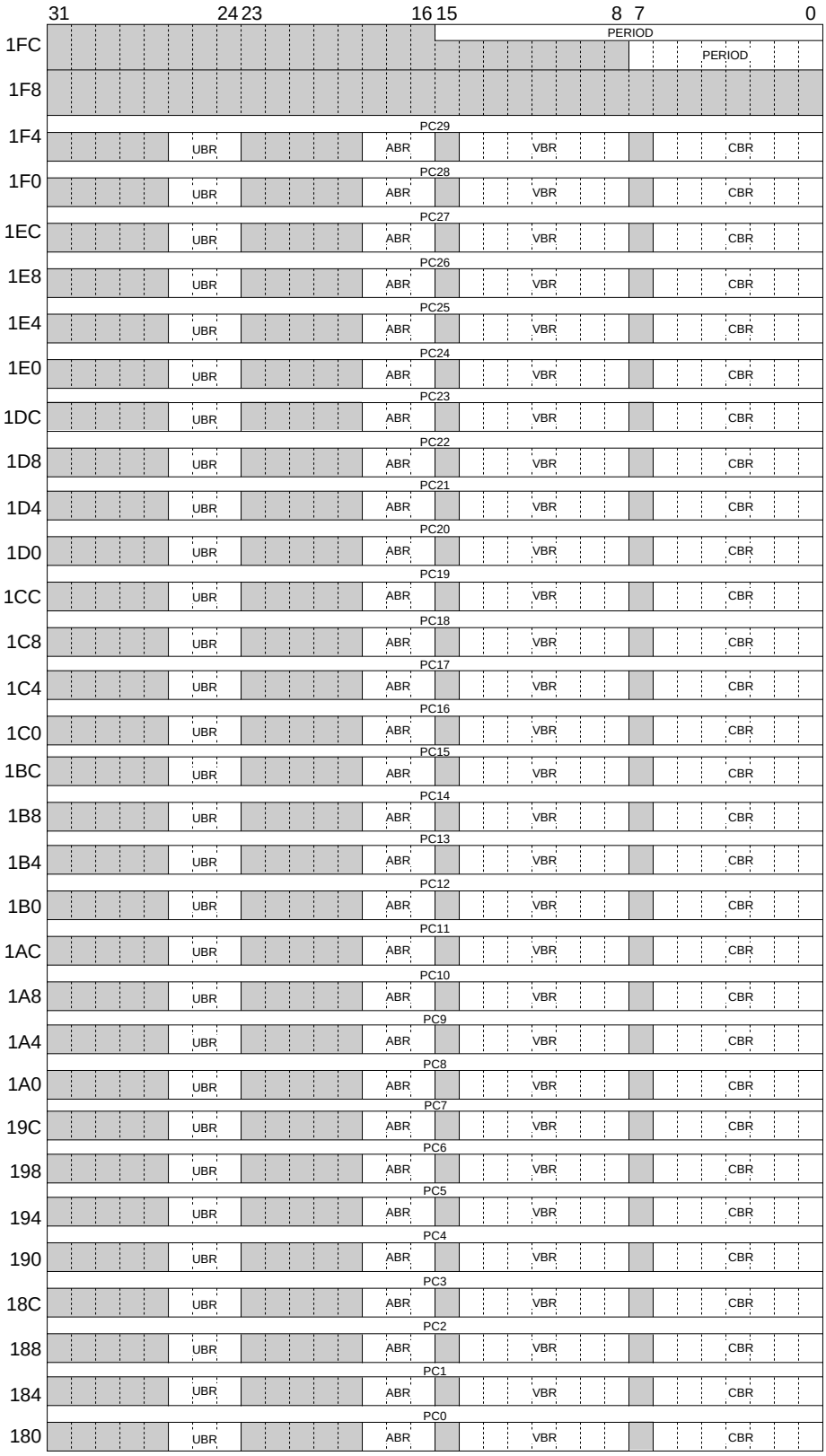
(2/6)



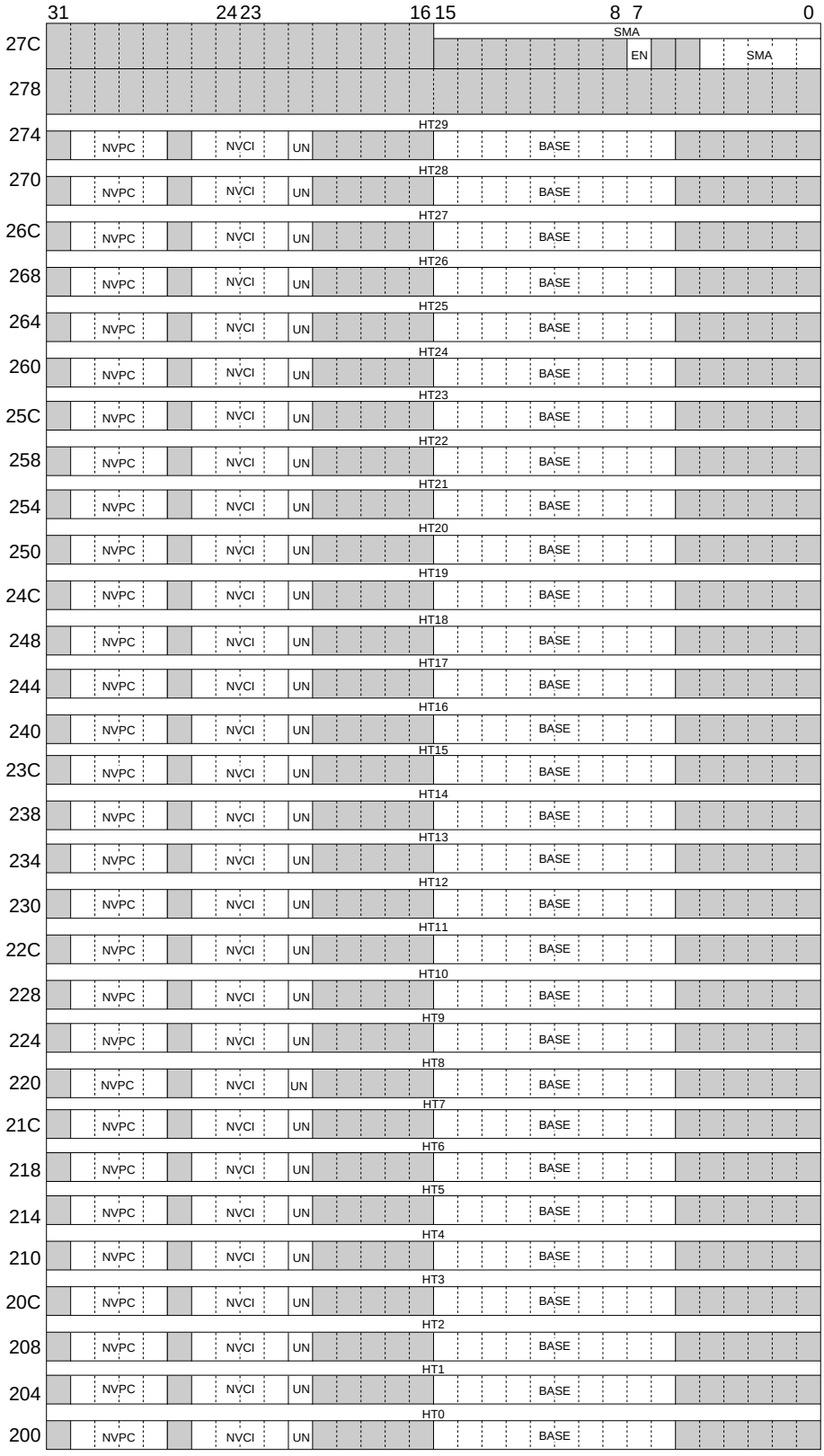
(3/6)



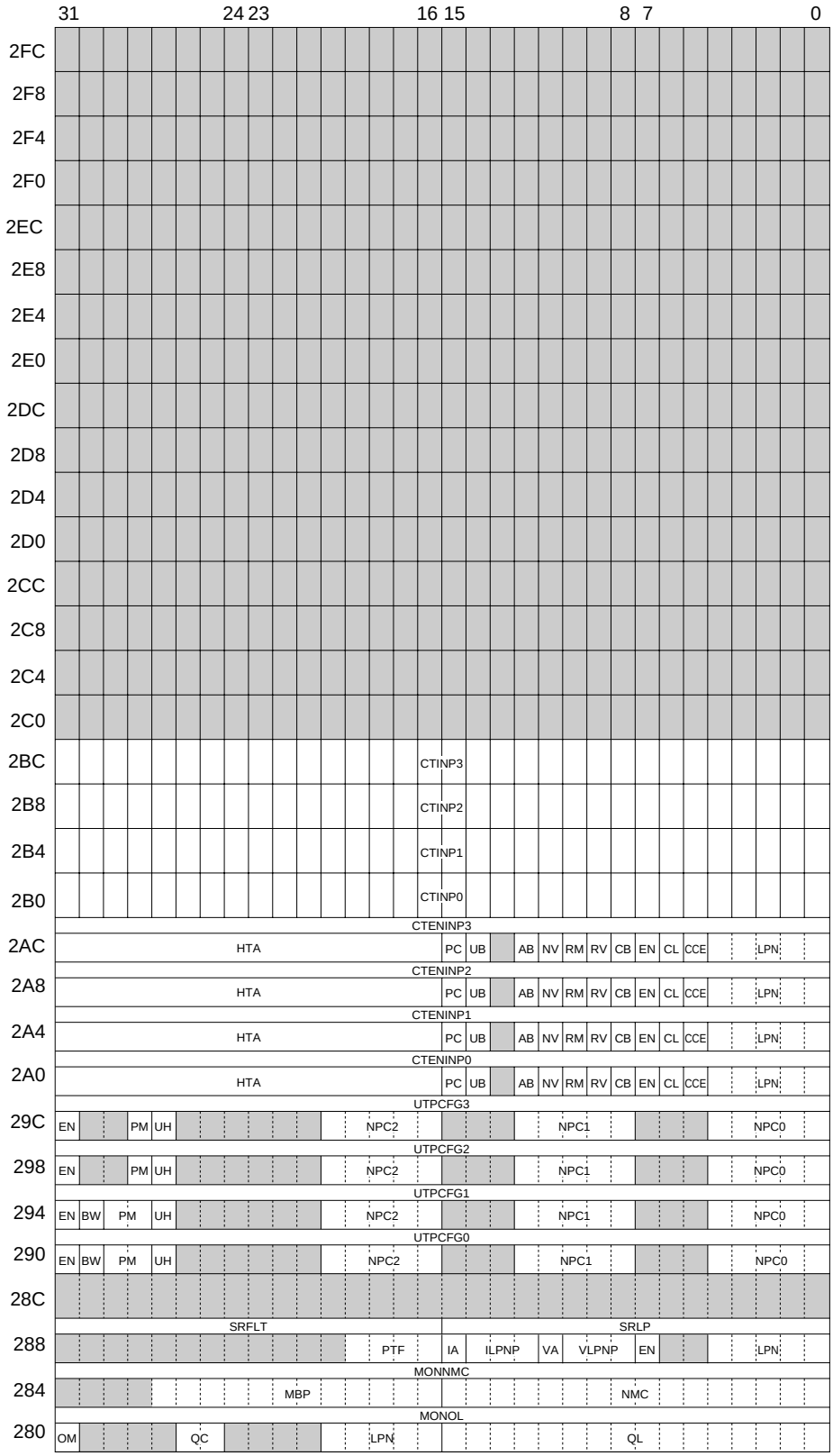
(4/6)



(5/6)



(6/6)

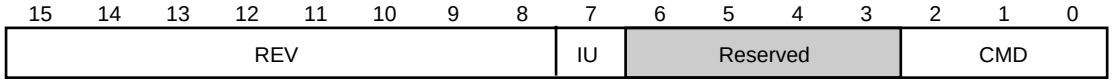


4.3 Register Functions

This section explains the registers of the μPD98412. The shaded portions in the descriptions below indicates a reserved area. Write “0” to the bits of a reserved area. These bits are “don’t care” when they are read.

4.3.1 Command register (0000h)

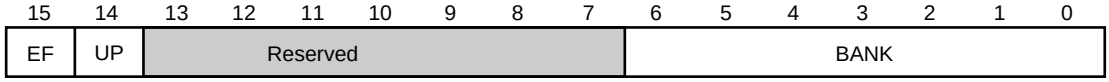
Register name	Address	Default	R/W
CMD	0000h	----_----_0xxx_x000	R/W



Field	Bit	R/W	Function	Default Value
REV	bit [15:8]	R	Indicates the version number of the μPD98412. The high-order nibble indicates the major version number, and the low-order nibble indicates the revision number. For example, “20h” means version 2.0. A value written to these bits is meaningless.	–
IU	bit [7]	R/W	This is a test mode bit for the μPD98412. Be sure to reset it to “0” when using it.	0
CMD	bit [2:0]	R/W	These bits specify a command for the μPD98412. Set CMD to enable the switching operation after the BY bit of the status register has become inactive and each register and the header translation table (HTT) have been set. If it is specified to stop the switching operation, the operation is stopped after the current processing of a cell is completed. To set CMD to enable the switching operation after the operation has been stopped, confirm that the BY bit is inactive. 000: Stops switching operation. 111: Enables switching operation.	000

★ **4.3.2 MODE0 register (0004h)**

Register name	Address	Default	R/W
MODE0	0004h	0xxx_xxxx_x000_0000	R/W



Field	Bit	R/W	Function	Default Value
EF	bit [15]	R/W	Specifies a cell subject to EFCI marking. 0: All user cells (VPC & VCC, PTI = 000, 001) 1: All user cells of VC connection (VCC, PTI = 000, 001)	0
UP	bit[14]	R/W	Enables or disables the UDF field transmission function. 0: Does not pass the UDF field (HEC check is in compliance with the setting of the HM bit of the MODE1 register). 1: Passes the UDF field (HEC check is not executed).	0
BANK	bit [6:0]	R/W	The value of this field is meaningless. This is because the μPD98412 does not support the 16-bit separation type asynchronous bus interface that is supported by the existing μPD98410. Write “0” to all the bits of this field.	00h

The UDF field that is passed to the output cell is as shown in the table below, depending on the data width of the UTOPIA I/F.

Rx	Tx	UDF1 of Output Cell	UDF2 of Output Cell
16-bit I/F	16-bit I/F	Passes UDF1 of input cell	Passes UDF2 of input cell
	8-bit I/F	Passes UDF1 of input cell	–
8-bit I/F	16-bit I/F	Passes UDF1 of input cell	FFh
	8-bit I/F	Passes UDF1 of input cell	–

If the setting of the ILPNP field of the SRLP register is 011/100, an input logic port number is appended to the low-order 5 bits of the UDF1/UDF2 field of the output cell even though the UDF field transmission function is valid. The high-order 3 bits are passed.

If a virtual logic port number is appended to the low-order 5 bits of the UDF1/UDF2 field of an input cell (SRLP register VLPNP field = 011/100), the UDF field is passed, including the appended virtual logic port number.

If the UDF field transmission function is enabled (UP bit of MODE0 register = 1), HEC check is not executed regardless of the setting of the HM bit of the MODE1.

4.3.3 MODE1 register (0006h)

Register name	Address	Default	R/W
MODE1	0006h	0000_0000_0x00_0x00	R/W

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HS	BL	UA	CI	RMA		HM	HC	EO		HMS		EO		CMS	

Caution Set this MODE1 register before issuing a command to the CMD register after reset. Do not write anything to this register until it is reset after a command has been issued to the CMD register. If the value of this register is rewritten while the operation is being carried out, the switching operation cannot be guaranteed.

Field	Bit	R/W	Function	Default Value
HS	bit [15]	R	Fixed to 0.	0
BL	bit [14]	R/W	This bit sets the byte alignment of the microprocessor to be connected. Because the default value after reset is little endian, care must be exercised if a microprocessor with a big endian interface accesses this register after reset. 0: Little endian 1: Big endian	0
UA	bit [13]	R/W	Masks or unmasks the IC error of the ERHT register due to unassigned cells. 0: Does not mask IC error. 1: Masks IC error.	0
CI	bit [12]	R/W	Masks or unmasks the CI/NI marking function of the RM cell. 0: Does not mask CI/NI marking. 1: Masks CI/NI marking.	0
RMA	bit [11:10]	R/W	Specifies how HTT is accessed when an RM cell is input and whether the RM cell merge function is used during VP switching. 00: Accesses the area referenced with VCI = 20h. The RM cell merge function is enabled (compatible with μPD98410). 01: Accesses area referenced with VCI = 06h. The RM cell merge function is enabled. 10: Accesses area referenced with VCI = 06h. The RM cell merge function is disabled. 11: Reserved	00

Field	Bit	R/W	Function	Default Value
★ HM	bit [9]	R/W	Enables or disables the cell discarding function in case of an HEC error. However, the cell discarding function is disabled when the UP bit of the MODE0 register is “1.” 0: Enables cell discarding function in case of an HEC error (discards HEC error cell). 1: Disables cell discarding function in case of an HEC error (passes HEC error cell). The HEC is generated normally for the cell output by the μPD98412 even when the discarding function is disabled by an HEC error.	0
HC	bit [8]	R/W	Selects which of the two external memories is to be selected when the memory chip select pin is active. Set this bit to “1” to select the HTT & control memory before issuing a command to the CMD register. While the switching operation is enabled, the microprocessor can access the external memory only for the header translation table (HTT), and cannot access the control memory. 0: Selects cell buffer memory. 1: Selects HTT & control memory.	0
EO	bit [7], bit [3]	R/W	Sets an even parity or odd parity for parity check of the external memory. • Bit 7: Sets HTT & control memory. • Bit 3: Sets cell buffer memory. 0: Even parity 1: Odd parity	0, 0
HMS	bit [5:4]	R/W	Sets the size of the HTT & control memory (32 bits/word). 00: 64K words 01: 128K words 10: 256K words 11: Reserved	00
CMS	bit [1:0]	R/W	Sets the size of the cell buffer memory (88 bits/word). 00: 64K words 01: 128K words 10: 256K words 11: Reserved	00

4.3.4 Interrupt mask register (0008h)

Register name	Address	Default	R/W
INTMASK	0008h	x000_00xx_0000_00xx_xxxx_0000_xxx0_0000	R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PH	PC	UE	QE	CE	Reserved		CB	CT	HE	HT	EX	MB	Reserved	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CIN3	CIN2	CIN1	CIN0	Reserved			CME	CHE	CHT	CEX	CRV

The INTMASK register masks an interrupt that occurs when the corresponding status becomes active. Indication by the status register is not masked. Each bit of this register can be set in the same manner. For the cause of an interrupt, refer to the description of the status register.

0: Masks interrupt caused by corresponding cause.
1: Requests interrupt caused by corresponding cause.

Remark No interrupt request is generated even if the BY bit of the status bit is active.

4.3.5 Status register (000Ch)

Register name	Address	Default	R/W
STATUS	000Ch	0000_00xx_0000_00x1_xxxx_0000_xxx0_0000	R/W or R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BY	PH	PC	UE	QE	CE	Reserved		CB	CT	HE	HT	EX	MB		EC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				CIN3	CIN2	CIN1	CIN0	Reserved			CME	CHE	CHT	CEX	CRV

The status register is set when the corresponding cause becomes active. An interrupt occurs for the corresponding interrupt cause, except for the BY bit and EC bit. When this register is read it indicates the current status, and when it is written the status is cleared. All bits have the same function.

When read

0: The corresponding status is inactive

1: The corresponding status is active

When written

0: Retains the corresponding status

1: Clears the corresponding status

Field	Bit	R/W	Function	Default Value
BY	bit [31]	R	Indicates that the μPD98412 is in the following operation status. No interrupt occurs even if this cause is changed. Writing this bit is meaningless. • At reset, indicates that the μPD98412 is in initializing. When the μPD98412 is reset by using the RESET_B pin, this bit becomes active. When the internal circuits of the LSI are initialized, this bit becomes inactive. • Indicates that the switching operation is enabled at times other than at reset. This bit becomes active when the operation of the μPD98412 is enabled by using the CMD register, and becomes inactive after the switching operation has stopped. **Caution Do not access the μPD98412 except to read the status register before this bit becomes inactive after reset. If any register of the μPD98412 is accessed while this bit is active, the initialization operation may not be performed correctly.**	0
PH	bit [30]	R	Indicates a parity error in the HTT & control memory.	0
PC	bit [29]	R	Indicates a parity error in the cell buffer memory.	0
UE	bit [28]	R	Indicates an overrun of the input FIFO at the reception side.	0
QE	bit [27]	R	Indicates an abnormal status in the pointer that manages the queue.	0
CE	bit [26]	R	Indicates an abnormal status in the cast counter that manages multi-cast count.	0
CB	bit [23]	R/W	Indicates that a cell has been discarded because the area for storing data has run short in the cell buffer memory.	0
CT	bit [22]	R/W	Indicates that a cell has been discarded because the area of the control memory that manages the queue of the HTT & control memory has run short. This may occur if the average broadcast count exceeds 2.	0
HE	bit [21]	R/W	Indicates an HEC error or CRC error in a received cell. If the HM bit of the MODE1 register is “1”, the HEC error is not indicated because the HEC error cell is not discarded.	0
HT	bit [20]	R/W	Indicates a header translation error.	0
EX	bit [19]	R/W	Indicates that a cell has been discarded because a threshold value, service class, or logical output port number of the EXTHMS register is exceeded.	0

Field	Bit	R/W	Function	Default Value
MB	bit [18]	R/W	Indicates that a multi-cast bitmap error has occurred.	0
EC	bit [16]	R	Indicates whether the cell buffer has a vacancy. 0: Cell buffer does not have a vacancy. 1: Cell buffer has a vacancy. An interrupt does not occur even if this source changes. Writing to this bit is meaningless.	1
CIN3, CIN2, CIN1, CIN0	bit [11:8]	R/W	Indicates that input counter CTINPn has overflown.	0
CME	bit [4]	R/W	Indicates that CTMEMEMP overflowed.	0
CHE	bit [3]	R/W	Indicates that CTERHEC overflowed.	0
CHT	bit [2]	R/W	Indicates that CTERHT overflowed.	0
CEX	bit [1]	R/W	Indicates that CTEXTH overflowed.	0
CRV	bit [0]	R/W	Indicates that CTRCV overflowed.	0

4.3.6 Threshold value exceeding discard indication mask register (0010h)

Register name	Address	Default	R/W
EXTHMS	0010h	0000_000x_0xx0_0x00_x0x0_0000_xxxx_xxxx	R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OM	OE	ON	OC	TM	TE	TN		MM	Reserved		OF	QM		QN	QC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	UB		AB	NV	RM	RV	CB	Reserved							

The EXTHMS register masks the use of the EXTH register to indicate when a threshold value is expected. Exceeding of a threshold value is reflected on the EX bit of the status register and an interrupt cause by setting the corresponding threshold value cause and condition of the corresponding class to the EXTHMS register. Regardless of the value of the EXTHMS register, cells are discarded when a threshold value is exceeded. Each bit of this register is set in the same manner. For the causes, refer to the description of the EXTH register.

0: Does not reflect corresponding cause on status.
1: Reflects corresponding cause on status.

4.3.7 Threshold value exceeding discard indication register (0014h)

Register name	Address	Default	R/W
EXTH	0014h	0000_000x_0xx0_0x00_x0x0_0000_xxx0_00 00	R

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OM	OE	ON	OC	TM	TE	TN		MM	Reserved		OF	QM		QN	QC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	UB		AB	NV	RM	RV	CB	Reserved			OPN				

The EXTH register indicates the threshold value, class, and output port that are responsible for the first discarding of a cell after the EX bit of the status register has been cleared. More than one threshold value responsible for discarding the cell may be indicated. If a cell is discarded because a threshold value is exceeded (queue length ≥ threshold value), the corresponding bit is set and, at the same time, the CTEXTH register is incremented, and the EX bit of the status register is set. While the EX bit is set, this register is not updated but retained. When the microprocessor clears the EX bit, updating this register becomes valid again. When the EX bit is cleared, the EXTH register does not indicate the correct value.

Even if a cell is discarded because of the class of threshold value masked by the EXTHMS register, it is not reflected on the EXTH register. Nor is the EX bit of the status register set.

bit [31-25, 23, 19, 17, 16] OM, OE, ON, OC, TM, TE, TN, MM, QM, QN, QC

0: The corresponding cause is not responsible for the first discarding of a cell.

1: The corresponding cause is responsible for the first discarding of a cell.

bit [14, 12-8] UB, AB, NV, RM, RV, CB

0: The corresponding class is not responsible for the first discarding of a cell.

1: The corresponding class is responsible for the first discarding of a cell.

Field	Bit	R/W	Function	Default Value
OM	bit [31]	R	Indicates that a cell has been discarded because the output queue exceeds OQthCBR, OQthRVR, OQthRM, OQthNVR, OQthABR, or OQthUBR threshold value.	0
OE	bit [30]	R	These bits simultaneously indicate that the packet of the channel set for EPD is discarded because of EPD control because the output queue exceeds OQthAEP or OQthUEP threshold value or that the UC (Used Cell) counter exceeds UCthAEP or UCthUEP threshold value. There is no functional difference between the OE and TE bits.	0
TE	bit [26]	R		0

Field	Bit	R/W	Function	Default Value
ON	bit [29]	R	Indicates that the cell of the channel not set for EPD is discarded because the output queue exceeds OQthAEP or OQthUEP threshold value.	0
OC	bit [28]	R	Indicates that the cell set for CLP is discarded because the output queue exceeds OQthCCL, OQthRCL, OQthACL, or OQthUCL threshold value.	0
TM	bit [27]	R	Indicates that a cell is discarded because the UC (Used Cell) counter exceeds UCthCBR, UCthRVR, UCthRM, UCthNVR, UCthABR, or UCthUBR threshold value.	0
TN	bit [25]	R	Indicates that the cell of the channel not set for EPD is discarded because the UC (Used Cell) counter exceeds UCthAEP or UCthUEP threshold value.	0
MM	bit [23]	R	Indicates that a multi-cast cell is discarded because the multi-cast queue exceeds MQthCRV, MQthRNV, MQthABR, or MQthUBR threshold value.	0
OF	bit [20]	R	Indicates that EFCI marking is performed because the output queue exceeds OQthRCI, OQthACI, or OQthUCI threshold value during queuing or re-queuing of multi-cast. **Remark** This bit is used for testing. Do not use it because it may be deleted in the future.	0
QM	bit [19]	R	Indicates that a cell is discarded because the output queue exceeds OQthCBR, OQthRVR, OQthRM, OQthNVR, OQthABR, or OQthUBR threshold value during re-queuing of multi-cast, or the UC (Used Cell) counter exceeds UCthCBR, UCthRVR, UCthRM, UCthNVR, UCthABR, or UCthUBR threshold value.	0
QN	bit [17]	R	Indicates that the cell of the channel not set for EPD is discarded because the output queue exceeds OQthAEP or OQthUEP threshold value during re-queuing of multi-cast, or the UC (Used Cell) counter exceeds UCthAEP or UCthUEP threshold value.	0
QC	bit [16]	R	Indicates that a cell set for CLP is discarded because the output queue exceeds OQthCCL, OQthRCL, OQthACL, or OQthUCL threshold value during re-queuing of multi-cast.	0
UB	bit [14]	R	Indicates that a cell of UBR class is discarded because a threshold value is exceeded.	0
AB	bit [12]	R	Indicates that a cell of ABR class is discarded because a threshold value is exceeded.	0

Field	Bit	R/W	Function	Default Value
NV	bit [11]	R	Indicates that a cell of nrtVBR class is discarded because a threshold value is exceeded.	0
RM	bit [10]	R	Indicates that an RM class is discarded because a threshold value is exceeded.	0
RV	bit [9]	R	Indicates that a cell of rtVBR class is discarded because a threshold value is exceeded.	0
CB	bit [8]	R	Indicates that a cell of CBR class is discarded because a threshold value is exceeded.	0
OPN	bit [4:0]	R	Indicates the number of the logical output port that discards a cell because a threshold value is exceeded. 00h to 1Dh: Indicates logical output port 0 to 29 1Fh : MM, QM, QN, or QC cause	00h

4.3.8 Header translation error discard indication register (0018h)

Register name	Address	Default	R/W
ERHT	0018h	0000_00xx_xxx1_1111	R

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IH	IC	IIP	IOP	IM	IR	Reserved					IPN				

The ERHT register indicates a header translation error and an input port that are responsible for the first cell discarding after the HT bit of the status register has been cleared. When a cell is discarded, the corresponding bit of this register is set and, at the same time, the CTERRE register is incremented, and the HT bit of the status register is set. While the HT bit is set, the ERHT register is not updated and its values are retained. When the microprocessor clears the HT bit, updating the ERHT register is enabled. When the HT bit is cleared, the ERHT register does not indicate the correct values.

bit [15:10] IH, IC, IIP, IOP, IM, IR

0: The corresponding cause is not responsible for the first discarding of a cell.

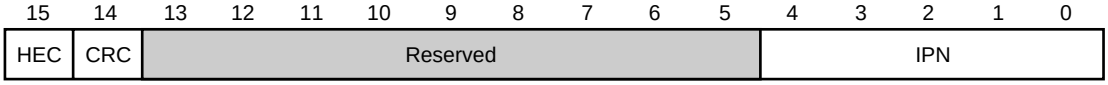
1: The corresponding cause is responsible for the first discarding of a cell.

Field	Bit	R/W	Function	Default Value
IH	bit [15]	R	Indicates that a cell has been discarded because the μPD98412 attempted to access HTT, exceeding the range set by the HT register. This happens if the VPI and VCI of the received cell are greater than the valid number of bits set to the HT register.	0
IC	bit [14]	R	Indicates that a cell has been discarded because the corresponding channel was disabled (CEN = "0") when the μPD98412 accessed HTT. This happens when a cell having VPI and VCI for which no connection is made has been received.	0
IIP	bit [13]	R	Indicates that a cell has been discarded because the logical input port specified as a virtual logical input port was disabled (PT register EN bit = 0)	0
IOP	bit [12]	R	Indicates that a cell has been discarded because the logical output port obtained as a result of μPD98412's access to HTT was disabled (PT register EN bit = "0"). This happens when a cell having VPI and VCI for which no connection is made has been received.	0

Field	Bit	R/W	Function	Default Value
IM	bit [11]	R	Indicates that a cell has been discarded because the multi-cast bitmap (MB) for the channel that was set for multi-cast (CM = “1”) was 0 and because the logical output port obtained by using MB was disabled (PT register EN bit = “0”) when the μPD98412 accessed HTT.	0
IR	bit [10]	R	Indicates that a cell has been discarded because an attempt was made to merge the RM cells of channels that were disabled (CEN = “0”) or because an attempt was made to merge the RM cells of a channel set in the single cast mode (CM = “0”) when the μPD98412 accessed HTT. This happens when a cell having VPI and VCI for which no connection is made has been received.	0
IPN	bit [4:0]	R	Indicates the number of the input port that has received the cell responsible for a header translation error. The IIP and IM causes indicates “1Fh” as a logical input port number. 00h to 1Dh: Indicates logical input port 0 to 29. 1Fh : IIP and IM causes	1Fh

4.3.9 HEC/CRC error discard indication register (001Ah)

Register name	Address	Default	R/W
ERHEC	001Ah	00xx_xxxx_xxx1_1111	R



The ERHEC register indicates an HEC error or CRC-10 error and an input port responsible for the first discarding of a cell after the HE bit of the status register has been cleared. When a cell is discarded, the corresponding bit of this register is set and, at the same time, the CTERHEC register is incremented, and the HE bit of the status register is set. While the HT bit is set, this register is not updated and its values are retained. When the microprocessor clears the HE bit, updating the ERHEC register is enabled. When the HE bit is cleared, this register does not indicate the correct values.

bit [15:14] HEC, CRC

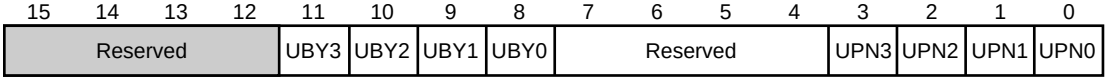
0: The corresponding cause is not responsible for the first discarding of a cell.

1: The corresponding cause is responsible for the first discarding of a cell.

Field	Bit	R/W	Function	Default Value
HEC	bit [15]	R	Indicates that a cell has been discarded because an HEC error was found as a result of checking the header area of a received cell. When the HM bit of the MODE1 register is set to “1”, the HEC error cell is not discarded; therefore, this bit indicates nothing.	0
CRC	bit [14]	R	Indicates a cell has been discarded because a CRC-10 error was found as a result of checking the payload area of a received cell that is a Backward RM cell.	0
IPN	bit [4:0]	R	Indicates the number of the logical input port that has received the cell responsible for the HEC error or CRC-10 error. 00h to 1Dh: Indicates logical input port 0 to 29.	1Fh

4.3.10 UTOPIA status register (001Ch)

Register name	Address	Default	R/W
UTPSTAT	001Ch	xxxx_0000_xxxx_0000	R



The UTPSTAT register indicates the operating status of the UTOPIA interface and if a FIFO control error has occurred. The FIFO control error indicates the occurrence of overrun or underrun inside the μPD98412.

The operating status means the status when this register is read.

A FIFO control error occurs if the relation between the UTOPIA clock and system clock is not satisfied. When a FIFO control error occurs, the corresponding bit (UPN) of this register is set and the UE bit of the status register is set. Even while the UE bit is set this register is updated. If a cell is discarded because of the above error, the number of discarded cells is not counted. Once the UPN bit is set, it cannot be cleared unless the μPD98412 is reset. If a FIFO control error occurs, the clocks must be reviewed.

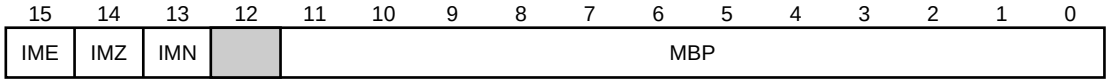
Field	Bit	R/W	Function	Default Value
UBY3-UBY0	bit [11:8]	R	Indicates the mode of the UTOPIA interface. 0: Paused. 1: Operating.	0000
UPN3-UPN0	bit [3:0]	R	Indicates the UTOPIA interface responsible for causing a FIFO control error. 0: Indicates that the corresponding UTOPIA interface did not cause a FIFO control error. 1: Indicates that the corresponding UTOPIA interface caused a FIFO control error.	0000

Remark When changing the settings of the UTOPIA interface in the ways shown below, confirm that the UBY bit is set to 0 (paused).

- When changing the contents of the UTOPIA configuration register
- When changing the PHY connection mode (SG bit of the PTn register)

4.3.11 Multi-cast bitmap error indication register (001Eh)

Register name	Address	Default	R/W
ERMB	001Eh	000x_0000_0000_0000	R



The ERMB register indicates MBP that has caused a multi-cast bitmap error for the first time after the MB bit of the status register has been cleared. It also indicates the cause of the error. If a multi-cast bitmap error occurs, not only the corresponding bit but also the MB bit of the status register are set. If the MB bit of the status register is set, the ERMB register is not updated but holds the current value. If the microprocessor clears the MB bit of the status register, updating the ERMB register is enabled. This register does not indicate the correct value when the MB bit of the status register is cleared.

Field	Bit	R/W	Function	Default Value
IME	bit [15]	R	Indicates whether the multi-cast bitmap is an error to be output to an invalid logical port. 0: No error 1: Error	0
IMZ	bit [14]	R	Indicates whether the multi-cast bitmap is an error to be output to none of the logical ports. 0: No error 1: Error	0
IMN	bit [13]	R	Indicates whether the multi-cast bitmap has been rewritten (whether broadcast count has changed) if there is a congested cell. 0: No error 1: Error	0
MBP	bit [11:0]	R	Indicates the multi-cast bitmap where an error has occurred.	000h

4.3.12 Threshold value exceeding discard cell count enable register (0020h)

Register name	Address	Default	R/W
CTENTH	0020h	0000_000x_0xxx_0x00_x0x0_0000_00x0_0000	R/W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OM	OE	ON	OC	TM	TE	TN		MM	Reserved			QM		QN	QC

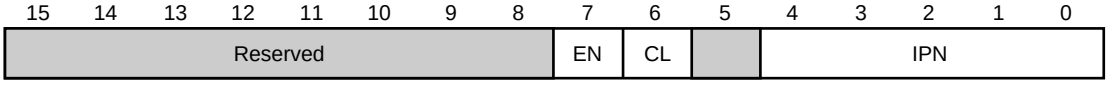
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	UB		AB	NV	RM	RV	CB	EN	CL		OPN				

The CTENTH register specifies the conditions under which cells discarded because a threshold value is exceeded are counted. The count value is indicated by the CTEXTH register. The CTENTH register gives the conditions of the corresponding threshold value, class, and output port, and enables counting the number of discarded cells by using the EN bit.

Field	Bit	R/W	Function	Default Value
OM, OE, ON, OC, TM, TE, TN, MM, QM, QN, QC	bit [31:25], bit [23], bit [19], bit [17], bit [16]	R/W	Specifies a threshold value by which the number of discarded cells is to be counted. For the correspondence between each of these bits and a threshold value, refer to the description of the EXTH register. The OE and TE bits count OE and TE causes if either of the bits is set. 0: Does not count the number of cells discarded because a threshold value is exceeded. 1: Counts the number of cells discarded because a threshold value is exceeded.	0
UB, AB, NV, RM, RV, CB	bit [14], bit [12:8]	R/W	Specifies a class in which the number of cells discarded because a threshold value is exceeded is counted. For the correspondence between each of these bits and a threshold value, refer to the description of the EXTH register. 0: Does not count the number of discarded cells in the corresponding class. 1: Counts the number of discarded cells in the corresponding class.	0
EN, CL	bit [7:6]	R/W	Enables or disables counting of the number of cells discarded because a threshold value is exceeded. 0x: Disables counting the number of cells discarded because a threshold value is exceeded. 10: Enables counting the number of cells discarded because a threshold value is exceeded. 11: Enables counting the number of cells discarded because a threshold value is exceeded, after the CTEXTH has been cleared. However, reset the EN bit to “0”, and then set EN and CL to “1”.	00
OPN	bit [4:0]	R/W	Specifies an output port that counts the number of cells discarded because a threshold value is exceeded. MM, QM, QN, and QC causes are counted only when OPN is set to “1Fh”. 00h to 1Dh: Counts discarding of cells by the corresponding output port 0 to 29. 1Eh : Reserved 1Fh : Counts discarding of cells by all the logical output ports.	00h

4.3.13 Header translation error discard cell count enable register (0024h)

Register name	Address	Default	R/W
CTENHT	0024h	xxxx_xxxx_00x0_0000	R/W

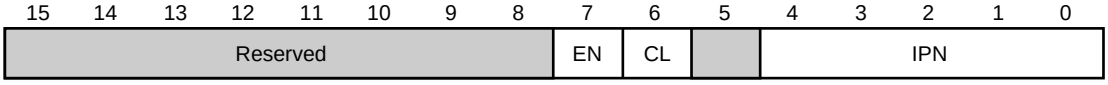


The CTENHT register specifies a logical input port that counts the number of cells discarded because a header translation error occurs. The counted value is indicated by the CTERHT register. IPN gives a condition, and the EN bit enables counting.

Field	Bit	R/W	Function	Default Value
EN, CL	bit [7:6]	R/W	Enables or disables counting of the number of cells discarded because of occurrence of a header translation error. 0x: Does not count the number of cells discarded due to occurrence of a header translation error. 10: Counts the number of cells discarded due to occurrence of a header translation error. 11: Clears CTERHT, and counts the number of cells discarded due to occurrence of a header translation error. However, reset the EN bit to “0”, and then set EN and CL to “1”.	00
IPN	bit [4:0]	R/W	Specifies a logical input port that counts the number of cells discarded because of the occurrence of a header translation error. Only discarding a cell due to the IIP cause and IM cause is counted only when IPN is set to “1Fh”. 00h to 1Dh : Counts the number of cells discarded because a header translation error has been caused by a source other than IM in the corresponding logical input port 0 to 29. 1Eh : Reserved 1Fh : Counts the number of cells discarded because of the header translation error in all the logical input ports.	00h

4.3.14 HEC/CRC error discard cell count enable register (0026h)

Register name	Address	Default	R/W
CTENHEC	0026h	xxxx_xxxx_00x0_0000	R/W

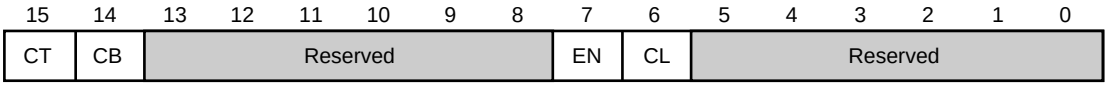


The CTENHEC register specifies a logical input port that counts the number of cells discarded because an HEC or CRC error occurs. The counted value is indicated by the CTERHEC register. IPN givens a condition, and the EN bit enables counting. While the HM bit of the MODE1 register is set to “1”, the HEC error cell is not discarded; therefore, the discarded cell is not counted.

Field	Bit	R/W	Function	Default Value
EN, CL	bit [7:6]	R/W	Enables or disables counting of the number of cells discarded due to an HEC/CRC error. 0x: Disables counting of the cells discarded due to an HEC/CRC error. 10: Enables counting of the cells discarded due to an HEC/CRC error. 11: Clears CTERHT, and enables counting of the cells discarded due to an HEC/CRC error. However, reset the EN bit to “0”, and set EN and CL to “1”.	00
IPN	bit [4:0]	R/W	Specifies a logical input port that counts the number of cells discarded due to an HEC/CRC error. 00h to 1Dh: Counts the number of cells discarded of the corresponding logical input port 0 to 29. 1Eh : Reserved. 1Fh : Counts the number of cells discarded of all the logical input port.	00h

4.3.15 Control/cell buffer memory shortage discard cell count enable register (0028h)

Register name	Address	Default	R/W
CTENMEM	0028h	00xx_xxxx_00xx_xxxx	R/W



The CTENMEM register specifies whether the number of cells discarded because the vacant control area of the HTT & control memory or the vacant area of the cell buffer memory has run short is counted. The counted value is not indicated by the CTMEMEMP register. Counting is enabled by the EN bit.

Field	Bit	R/W	Function	Default Value
CT	bit [15]	R/W	Specifies whether the number of cells discarded because the control area of the HTT & control memory has run short is counted. 0: Does not count the number of cells discarded because the vacant area of the control memory has run short. 1: Counts the number of cells discarded because the vacant area of the control memory has run short.	0
CB	bit [14]	R/W	Specifies whether the number of cells discarded because the vacant area of the cell buffer memory has run short is counted. 0: Does not count the number of cells discarded because the vacant area of the cell buffer memory has run short. 1: Counts the number of cells discarded because the vacant area of the cell buffer memory has run short.	0
EN, CL	bit [7:6]	R/W	Enables or disables counting the number of cells discarded because the vacant area of the control memory or cell buffer memory has run short. 0x: Does not count the number of cells discarded because the vacant area of the control memory or cell buffer memory has run short. 10: Counts the number of cells discarded because the vacant area of the control memory or cell buffer memory has run short. 11: Clears CTMEMEMP register and then counts the number of cells discarded because the vacant area of the control memory or cell buffer memory has run short. However, reset the EN bit to “0”, and set EN and CL to “1”.	00

4.3.16 Receive cell count enable register (002Ah)

Register name	Address	Default	R/W
CTENRCV	002Ah	xxxx_xxxx_00xx_0000	R/W

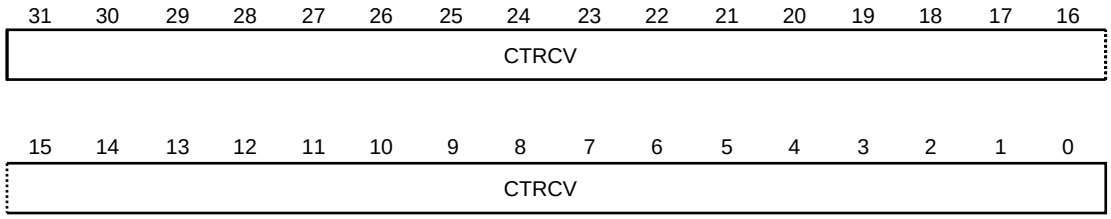
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								EN	CL	Reserved		UPN3	UPN2	UPN1	UPN0

The CTENRCV register specifies whether the number of cells received by each UTOPIA interface port is counted. The counted value is indicated by the CTRCV register. The EN bit enables counting.

Field	Bit	R/W	Function	Default Value
EN, CL	bit [7:6]	R/W	Enables or disables the number of cells received. 0x: Does not count the number of received cells. 10: Counts the number of received cells. 11: Clears CTRCV, and counts the number of received cells. However, reset the EN bit to “0”, and set EN and CL to “1”.	00
UPN3, UPN2, UPN1, UPN0	bit [3:0]	R/W	Specifies a UTOPIA interface port number that counts the number of received cells by bitmap. 0: Does not count the number of received cells of the corresponding UTOPIA interface port. 1: Counts the number of received cells of the corresponding UTOPIA interface port. **Remark** If 16-bit UTOPIA interface port 0 is subject to counting, set both the UPN0 and UPN2 bits to “1”. To count 16-bit UTOPIA interface port 1, set both the UPN1 and UPN3 bits to “1”.	0h

4.3.17 Receive cell count register (002Ch)

Register name	Address	Default	R/W
CTRCV	002Ch	0000_0000_0000_0000_0000_0000_0000_0000	R/W



The CTRCV register indicates the number of cells received under the condition specified by the CTENRCV register. The number of cells is counted while EN of the CTENRCV register is “1”. The value of this register is cleared when the reset signal is applied to the μPD98412 and when CL and EN of the CTENRCV register are set to “1”.

If a cell is received when the count value is “FFFFFFFFh”, the CRV bit of the status bit is set, an interrupt request is issued to the microprocessor, the count value is reset to “00000000h”, and counting continues. If the CRV bit of the INTMASK register is “0”, the interrupt request is not issued to the microprocessor.

Field	Bit	R/W	Function	Default Value
CTRCV	bit [31:0]	R/W	00000000h to FFFFFFFFh: Number of received cells	00000000h

Remark The CTRCV register indicates the total number of received cells of the specified UTOPIA interface port. For example, if the CTENRCV register is set to EN = 1, CL = 0, UPN0 = UPN2 = 1, and UPN1 = UPN3 = 0, the CTRCV register indicates the total number of cells received from all the PHY devices connected to UTOPIA0 and UTOPIA2.

4.3.18 Threshold value exceeding discard cell count register (0030h)

Register name	Address	Default	R/W
CTEXTH	0030h	0000_0000_0000_0000_0000_0000_0000_0000	R/W

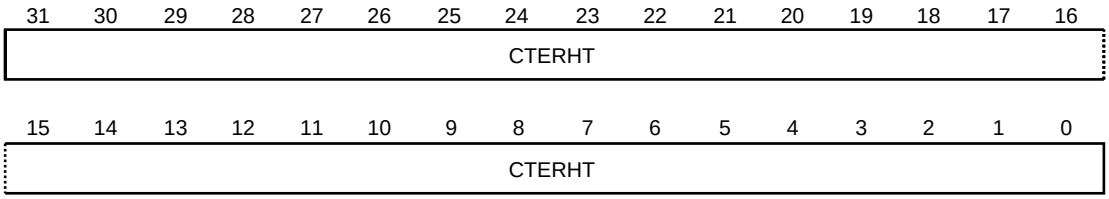
The CTEXTH register indicates the number of cells discarded under the condition specified by the CTENTH register. Counting is performed when EN of the CTENTH register is “1”, and is cleared when the reset signal is applied to the μPD98412 and when CL and EN of the CTENTH register are “1”.

If a cell is discarded when the count value is “FFFFFFFFh”, the CEX bit of the status register is set, an interrupt request is issued to the microprocessor, the count value is cleared to “00000000h”, and counting continues. If the CEX bit of the INTMASK register is “0”, no interrupt request is issued to the microprocessor.

Field	Bit	R/W	Function	Default Value
CTEXTH	bit [31:0]	R/W	00000000h to FFFFFFFFh: Number of discarded cells	00000000h

4.3.19 Header translation error discard cell count register (0034h)

Register name	Address	Default	R/W
CTERHT	0034h	0000_0000_0000_0000_0000_0000_0000_0000	R/W



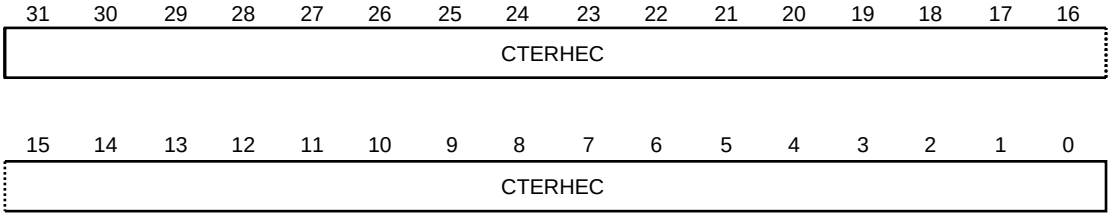
The CTERTH register indicates the number of cells discarded under the condition specified by the CTENHT register. Counting is performed when EN of the CTENHT register is “1”, and is cleared when the reset signal is applied to the μPD98412 and when CL and EN of the CTENHT register are “1”.

If a cell is discarded when the count value is “FFFFFFFFh”, the CHT bit of the status register is set, an interrupt request is issued to the microprocessor, the count value is cleared to “00000000h”, and counting continues. If the CHT bit of the INTMASK register is “0”, no interrupt request is issued to the microprocessor.

Field	Bit	R/W	Function	Default Value
CTERHT	bit [31:0]	R/W	00000000h to FFFFFFFFh: Number of discarded cells	00000000h

4.3.20 HEC/CRC error discard cell count register (0038h)

Register name	Address	Default	R/W
CTERHEC	0038h	0000_0000_0000_0000_0000_0000_0000_0000	R/W



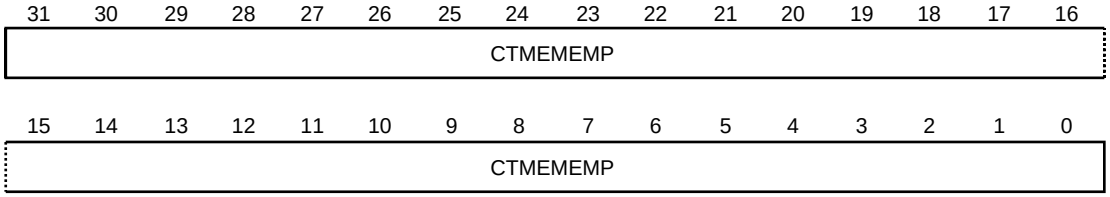
The CTERHEC register indicates the number of cells discarded under the condition specified by the CTENHEC register. Counting is performed when EN of the CTENHEC register is “1”, and is cleared when the reset signal is applied to the μPD98412 and when CL and EN of the CTENHEC register are “1”. Counting is not performed when the HM bit of the MODE1 register is set to “1” because the HEC error cell is not discarded.

If a cell is discarded when the count value is “FFFFFFFFh”, the CHE bit of the status register is set, an interrupt request is issued to the microprocessor, the count value is cleared to “00000000h”, and counting continues. If the CHE bit of the INTMASK register is “0”, no interrupt request is issued to the microprocessor.

Field	Bit	R/W	Function	Default Value
CTERHEC	bit [31:0]	R/W	00000000h to FFFFFFFFh: Number of discarded cells	00000000h

4.3.21 Control/cell buffer memory shortage discard cell count register (003Ch)

Register name	Address	Default	R/W
CTMEMEMP	003Ch	0000_0000_0000_0000_0000_0000_0000_0000	R/W



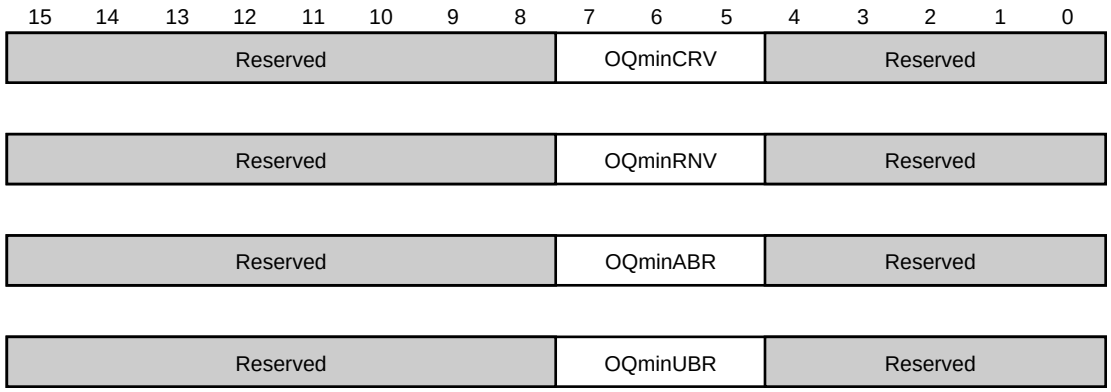
The CTMEMEMP register indicates the number of cells discarded because the vacant area in the control memory or cell buffer memory has run short. When the CT bit of the CTENMEM register is set to “1”, the number of cells discarded because the vacant area of the control memory has run short is counted; when the CB bit of the CTENMEM register is set to “1”, the number of cells discarded because the vacant area of the cell buffer memory has run short is counted. Counting is performed while EN bit of the CTENMEM register is “1”, and is cleared when the reset signal is applied to the μPD98412 and when CL and EN of the CTENMEM register are set to “1”.

If a cell is discarded when the count value is “FFFFFFFFh”, the CME bit of the status register is set to 1, an interrupt request is issued to the microprocessor, the count value is cleared to “00000000h”, and counting continues. If the CME bit of the INTMASK register is “0”, no interrupt request is issued to the microprocessor.

Field	Bit	R/W	Function	Default Value
CTMEMEMP	bit [31:0]	R/W	00000000h to FFFFFFFFh: Number of cells discarded	00000000h

4.3.22 Output queue minimum threshold value registers (0040h, 0044h, 0048h, 004Ch)

Register name	Address	Default	R/W
OQminCRV	0040h	xxxx_xxxx_000x_xxxx	R/W
OQminRNV	0044h	xxxx_xxxx_000x_xxxx	R/W
OQminABR	0048h	xxxx_xxxx_000x_xxxx	R/W
OQminUBR	004Ch	xxxx_xxxx_000x_xxxx	R/W



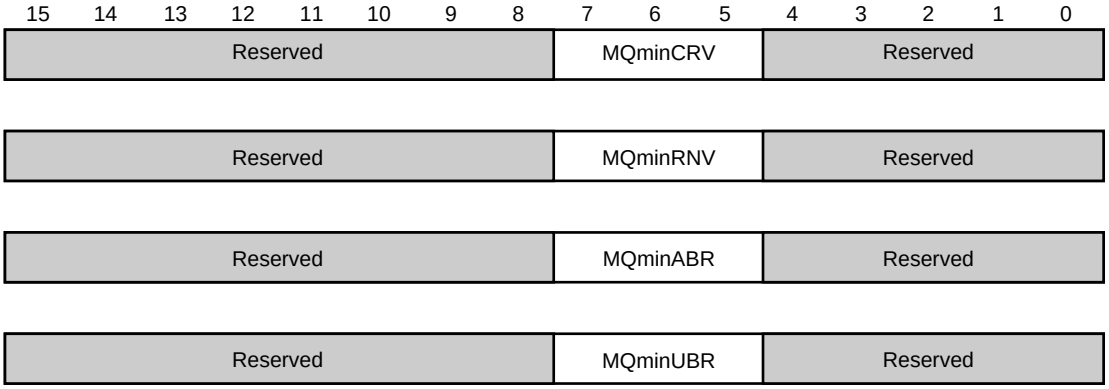
These registers specify the minimum number of guaranteed cells for each logical output port.

Be sure to set the minimum threshold value before enabling the switching operation by using the CMD register. Once the switching operation has been enabled, do not re-set the threshold value; otherwise, queue management cannot be guaranteed and the μPD98412 will malfunction.

Field	Bit	R/W	Function	Default Value
OQminCRV	bit [7:5]	R/W	000 to 111: Minimum number of guaranteed cells in CBR + rtVBR class (in 32-cell units: 0/32/64/ ... /224)	000 (0000h)
OQminRNV	bit [7:5]	R/W	000 to 111: Minimum number of guaranteed cells in RM + nrtVBR class (in 32-cell units: 0/32/64/ ... /224)	000 (0000h)
OQminABR	bit [7:5]	R/W	000 to 111: Minimum number of guaranteed cells in ABR class (in 32-cell units: 0/32/64/ ... /224)	000 (0000h)
OQminUBR	bit [7:5]	R/W	000 to 111: Minimum number of guaranteed cells in UBR class (in 32-cell units: 0/32/64/ ... /224)	000 (0000h)

4.3.23 Multi-cast queue minimum threshold value registers (0050h, 0054h, 0058h, 005Ch)

Register name	Address	Default	R/W
MQminCRV	0050h	xxxx_xxxx_000x_xxxx	R/W
MQminRNV	0054h	xxxx_xxxx_000x_xxxx	R/W
MQminABR	0058h	xxxx_xxxx_000x_xxxx	R/W
MQminUBR	005Ch	xxxx_xxxx_000x_xxxx	R/W



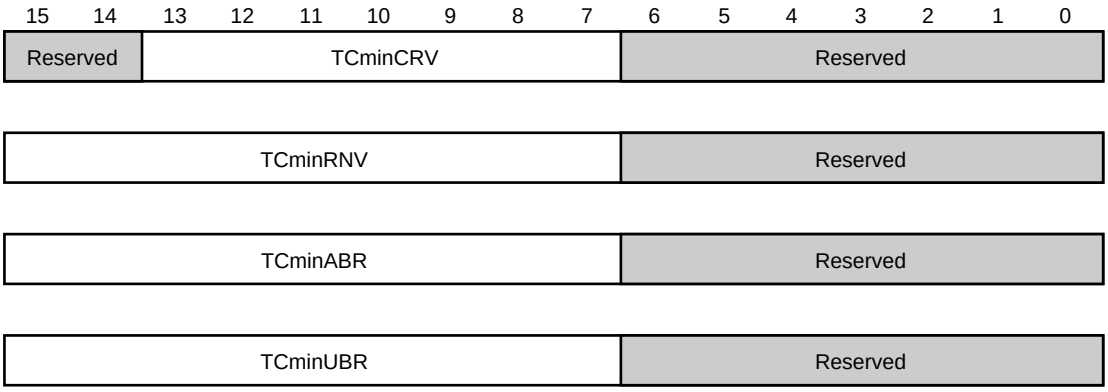
These registers specify the minimum number of guaranteed cells for the multi-cast in each class.

Be sure to set the minimum threshold value before enabling the switching operation by using the CMD register. Once the switching operation has been enabled, do not re-set the threshold value; otherwise, queue management cannot be guaranteed and the μPD98412 will malfunction.

Field	Bit	R/W	Function	Default Value
MQminCRV	bit [7:5]	R/W	000 to 111: Minimum number of guaranteed cells in CBR + rtVBR class (in 32-cell units: 0/32/64/ ... /224)	000 (0000h)
MQminRNV	bit [7:5]	R/W	000 to 111: Minimum number of guaranteed cells in RM + nrtVBR class (in 32-cell units: 0/32/64/ ... /224)	000 (0000h)
MQminABR	bit [7:5]	R/W	000 to 111: Minimum number of guaranteed cells in ABR class (in 32-cell units: 0/32/64/ ... /224)	000 (0000h)
MQminUBR	bit [7:5]	R/W	000 to 111: Minimum number of guaranteed cells in UBR class (in 32-cell units: 0/32/64/ ... /224)	000 (0000h)

4.3.24 TC (Total Cell) counter minimum threshold registers (0060h, 0064h, 0068h, 006Ch)

Register name	Address	Default	R/W
TCminCRV	0060h	xx00_0000_0xxx_xxxx	R/W
TCminRNV	0064h	0000_0000_0xxx_xxxx	R/W
TCminABR	0068h	0000_0000_0xxx_xxxx	R/W
TCminUBR	006Ch	0000_0000_0xxx_xxxx	R/W



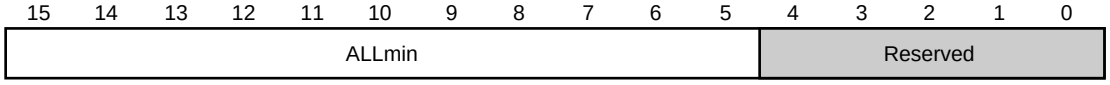
These registers specify the minimum number of guaranteed cells for each class. The minimum number of cells guaranteed for each class is counted after the number of cells has exceeded the minimum number of guaranteed cells for each logical output port.

Be sure to set the minimum threshold value before enabling the switching operation by using the CMD register. Once the switching operation has been enabled, do not re-set the threshold value; otherwise, queue management cannot be guaranteed and the μPD98412 will malfunction.

Field	Bit	R/W	Function	Default Value
TCminCRV	bit [13:7]	R/W	00_0000_0 to 11_1111_1: Minimum number of guaranteed cells in CBR + rtVBR class (in 128-cell units: 0/128/256/ ... /16256)	00_0000_0 (0000h)
TCminRNV	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: Minimum number of guaranteed cells in RM + nrtVBR class (in 128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)
TCminABR	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: Minimum number of guaranteed cells in ABR class (in 128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)
TCminUBR	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: Minimum number of guaranteed cells in UBR class (in 128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)

4.3.25 Total number of cells minimum threshold value register (007Eh)

Register name	Address	Default	R/W
ALLmin	007Eh	0000_0000_000x_xxxx	R/W



The ALLmin register specifies the total of the minimum number of guaranteed cells. Before enabling the switching operation by using the CMD register, be sure to set the value calculated by the following expression to the CMD register. Once the switching operation has been enabled, do not re-set ALLmin register; otherwise, queue management cannot be guaranteed and the μPD98412 will malfunction.

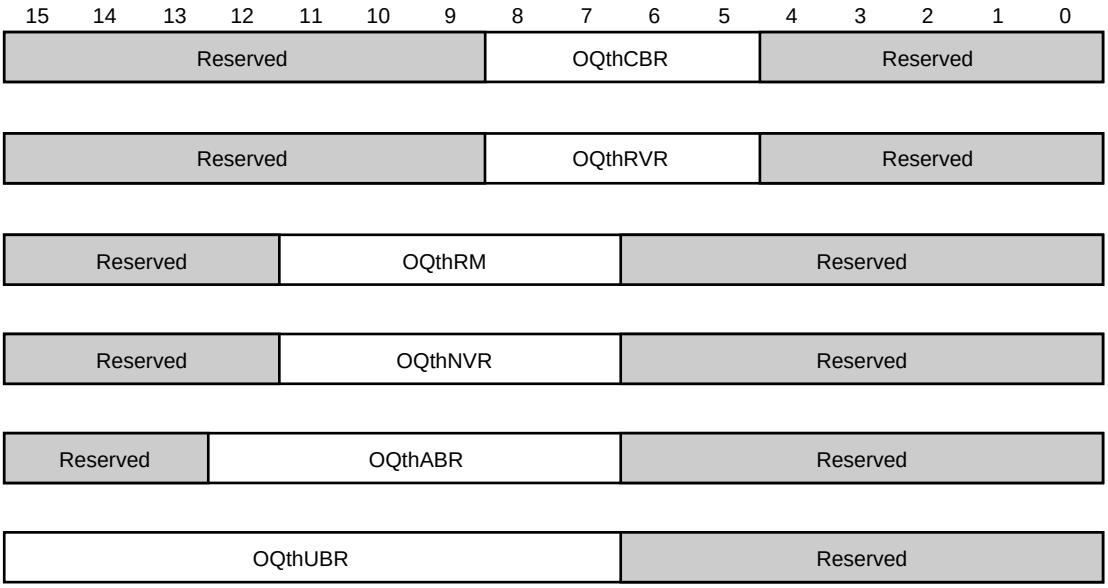
(OQminCRV + OQminRNV + OQminABR + OQminUBR) $\times$ enabled ports[Note]
+ MQminCRV + MQminRNV + MQminABR + MQminUBR
+ TCminCRV + TCminRNV + TCminABR + TCminUBR

Note "enabled ports" indicates the total number of logical ports scheduled to enable the EN bit of the PT register.

Field	Bit	R/W	Function	Default Value
ALLmin	bit [15:5]	R/W	0000_0000_000 to 1111_1111_111: Total of minimum number of guaranteed cells (in 32-cell units: 0/32/64 ... /65504)	0000_0000_000 (0000h)

4.3.26 Output queue maximum threshold value registers (0080h, 0082h, 0090h, 0092h, 00A0h, 00B0h)

Register name	Address	Default	R/W
OQthCBR	0080h	xxxx_xxx0_000x_xxxx	R/W
OQthRVR	0082h	xxxx_xxx0_000x_xxxx	R/W
OQthRM	0090h	xxxx_0000_0xxx_xxxx	R/W
OQthNVR	0092h	xxxx_0000_0xxx_xxxx	R/W
OQthABR	00A0h	xxx0_0000_0xxx_xxxx	R/W
OQthUBR	00B0h	0000_0000_0xxx_xxxx	R/W



These registers set the upper-limit threshold value of each logical output port in each class. If a cell in each class is congested in the output queue, exceeding the corresponding threshold value, the cell is discarded.

Field	Bit	R/W	Function	Default Value
OQthCBR	bit [8:5]	R/W	0_000 to 1_111: Upper-limit threshold value in CBR class (32-cell units: 0/32/64/ ... /480)	0_000 (0000h)
OQthRVR	bit [8:5]	R/W	0_000 to 1_111: Upper-limit threshold value in rtVBR class (32-cell units: 0/32/64/ ... /480)	0_000 (0000h)
OQthRM	bit [11:7]	R/W	0000_0 to 1111_1: Upper-limit threshold value in RM class (128-cell units: 0/128/256/ ... /3968)	0000_0 (0000h)
OQthNVR	bit [11:7]	R/W	0000_0 to 1111_1: Upper-limit threshold value in nrtVBR class (128-cell units: 0/128/256/ ... /3968)	0000_0 (0000h)
OQthABR	bit [12:7]	R/W	0_0000_0 to 1_1111_1: Upper-limit threshold value in ABR class (128-cell units: 0/128/256/ ... /8046)	0_0000_0 (0000h)

Field	Bit	R/W	Function	Default Value
OQthUBR	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: Upper-limit threshold value in UBR class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)

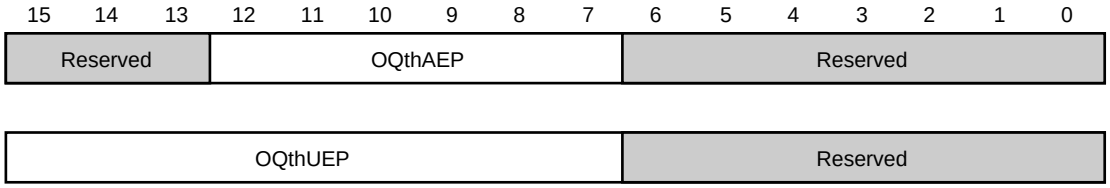
Remarks 1. OQthCBR and OQthRVR are the threshold values for the same output queue.

2. OQthRM and OQthNVR are the threshold values for the same output queue.

3. For cells in ABR and UBR classes for which EPD is disabled, OQthAEP and OQthUEP are the upper-limit threshold values.

4.3.27 Output queue EPD threshold value registers (00A2h, 00B2h)

Register name	Address	Default	R/W
OQthAEP	00A2h	xxx0_0000_0xxx_xxxx	R/W
OQthUEP	00B2h	0000_0000_0xxx_xxxx	R/W



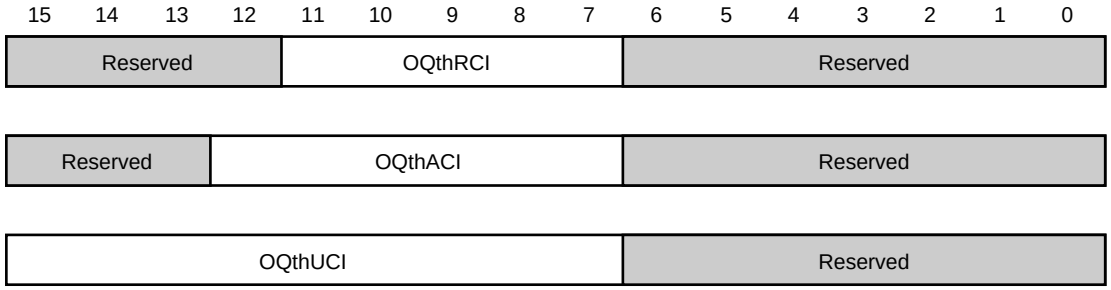
These registers set the EPD threshold value of each logical output port in each class. If a cell in each class is congested in the output queue, exceeding the corresponding threshold value, an EPD control operation is performed, and the following processing is executed:

- EPD valid cell : Cells belonging to the newly received packet are discarded. The end of packet (EOP) is received.
- EPD invalid cell : The cell is discarded.

Field	Bit	R/W	Function	Default Value
OQthAEP	bit [12:7]	R/W	0_0000_0 to 1_1111_1: EPD threshold value in ABR class (128-cell units: 0/128/256/ ... /8046)	0_0000_0 (0000h)
OQthUEP	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: EPD threshold value in UBR class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)

4.3.28 Output queue EFCI threshold value registers (0094h, 00A4h, 00B4h)

Register name	Address	Default	R/W
OQthRCI	0094h	xxxx_0000_0xxx_xxxx	R/W
OQthACI	00A4h	xxx0_0000_0xxx_xxxx	R/W
OQthUCI	00B4h	0000_0000_0xxx_xxxx	R/W

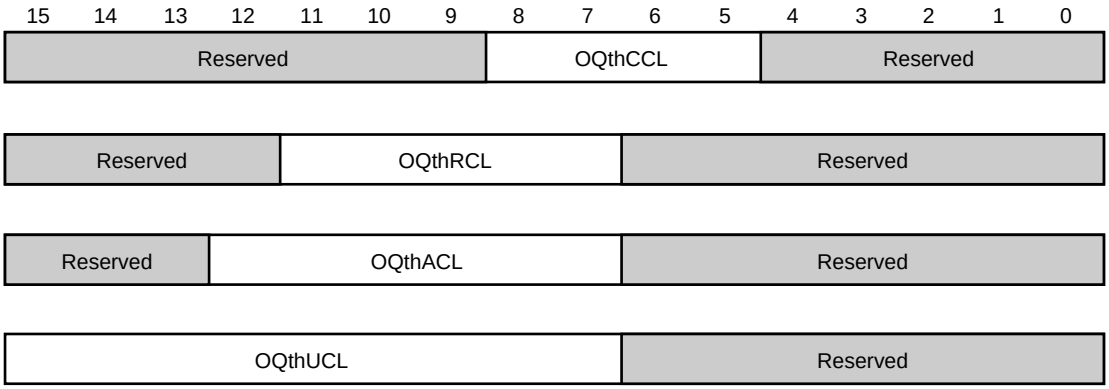


These registers set the EFCI threshold value of each logical output port in each class. If a cell in each class is congested in the output queue, exceeding the corresponding threshold value, EFCI marking is performed of the user cells and CI/NI marking is performed for the backward RM cells.

Field	Bit	R/W	Function	Default Value
OQthRCI	bit [11:7]	R/W	0000_0 to 1111_1: EFCI threshold value in RM + nrtVBR class (128-cell units: 0/128/256/ ... /3968)	0000_0 (0000h)
OQthACI	bit [12:7]	R/W	0_0000_0 to 1_1111_1: EFCI threshold value in ABR class (also used as CI threshold value) (128-cell units: 0/128/256/ ... /8064)	0_0000_0 (0000h)
OQthUCI	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: EFCI threshold value in UBR class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)

4.3.29 Output queue CLP threshold value registers (0086h, 0096h, 00A6h, 00B6h)

Register name	Address	Default	R/W
OQthCCL	0086h	xxxx_xxx0_000x_xxxx	R/W
OQthRCL	0096h	xxxx_0000_0xxx_xxxx	R/W
OQthACL	00A6h	xxx0_0000_0xxx_xxxx	R/W
OQthUCL	00B6h	0000_0000_0xxx_xxxx	R/W

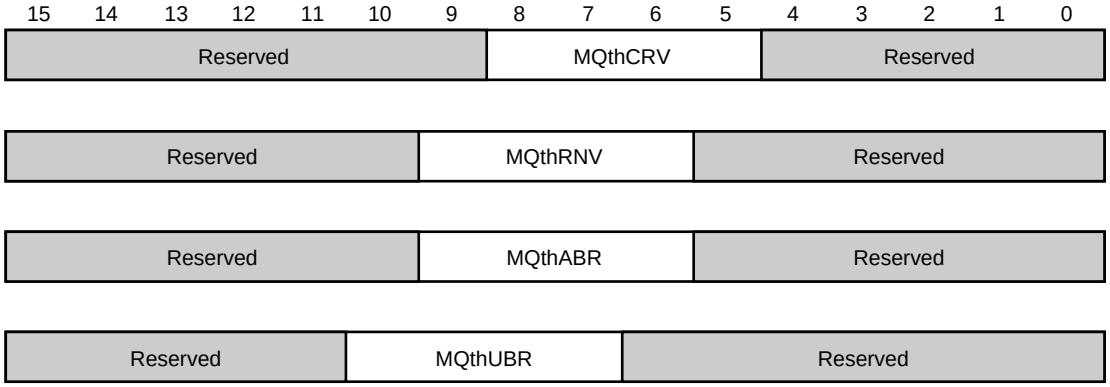


These registers set the CLP threshold value of each logical output port in each class. If a cell in each class is congested in the output queue, exceeding the corresponding threshold value, the cell for which CLP is set is discarded.

Field	Bit	R/W	Function	Default Value
OQthCCL	bit [8:5]	R/W	0_000 to 1_111: CLP threshold value in CBR + rtVBR class (32-cell units: 0/32/64/ ... / 480)	0_000 (0000h)
OQthRCL	bit [11:7]	R/W	0000_0 to 1111_1: CLP threshold value in RM + nrtVBR class (128-cell units: 0/128/256/ ... /3968)	0000_0 (0000h)
OQthACL	bit [12:7]	R/W	0_0000_0 to 1_1111_1: CLP threshold value in ABR class (128-cell units: 0/128/256/ ... /8064)	0_0000_0 (0000h)
OQthUCL	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: CLP threshold value in UBR class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)

4.3.30 Multi-cast queue maximum threshold value registers (00C0h, 00C4h, 00C8h, 00CCh)

Register name	Address	Default	R/W
MQthCRV	00C0h	xxxx_xxx0_000x_xxxx	R/W
MQthRNV	00C4h	xxxx_xx00_00xx_xxxx	R/W
MQthABR	00C8h	xxxx_xx00_00xx_xxxx	R/W
MQthUBR	00CCh	xxxx_x000_0xxx_xxxx	R/W

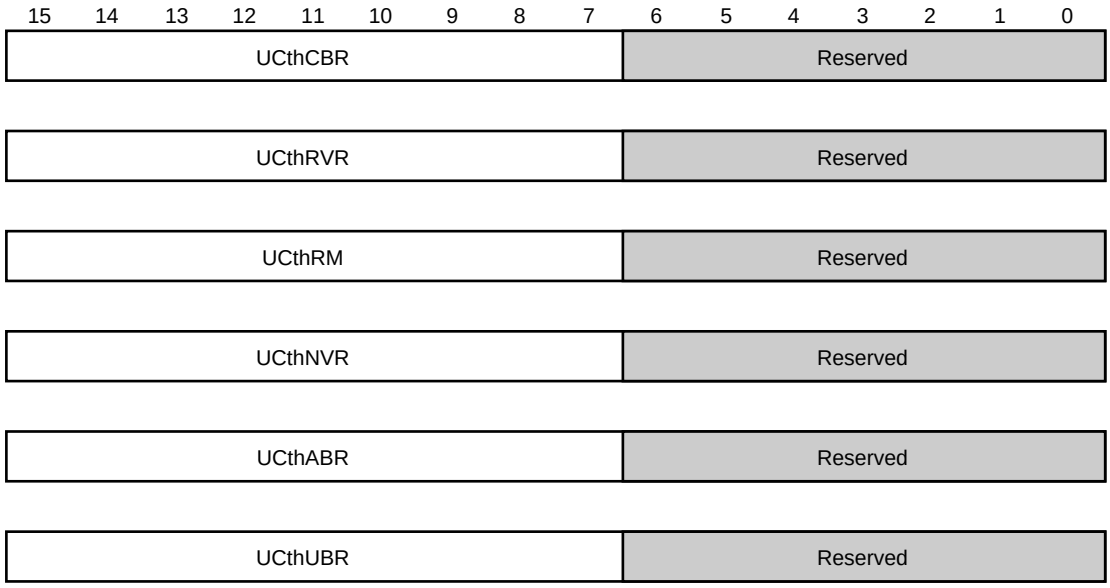


These registers set the upper-limit threshold value of the multi-cast queue in each class. If a cell in each class is congested in the multi-cast queue, exceeding the corresponding threshold value, the cell is discarded.

Field	Bit	R/W	Function	Default Value
MQthCRV	bit [8:5]	R/W	0_000 to 1_111: Upper-limit threshold value in CBR + rtVBR class (32-cell units: 0/32/64/ ... /480)	0_000 (0000h)
MQthRNV	bit [9:6]	R/W	00_00 to 11_11: Upper-limit threshold value in RM + nrtVBR class (64-cell units: 0/64/128/ ... /960)	00_00 (0000h)
MQthABR	bit [9:6]	R/W	00_00 to 11_11: Upper-limit threshold value in ABR class (64-cell units: 0/64/128/ ... /960)	00_00 (0000h)
MQthUBR	bit [10:7]	R/W	000_0 to 111_1: Upper-limit threshold value in UBR class (128-cell units: 0/128/256/ ... /1920)	000_0 (0000h)

4.3.31 UC (Used Cell) counter maximum threshold value register (00D0h, 00D4h, 00D8h, 00DCh, 00E0h, 00E8h)

Register name	Address	Default	R/W
UCthCBR	00D0h	0000_0000_0xxx_xxxx	R/W
UCthRVR	00D4h	0000_0000_0xxx_xxxx	R/W
UCthRM	00D8h	0000_0000_0xxx_xxxx	R/W
UCthNVR	00DCh	0000_0000_0xxx_xxxx	R/W
UCthABR	00E0h	0000_0000_0xxx_xxxx	R/W
UCthUBR	00E8h	0000_0000_0xxx_xxxx	R/W



These registers set the upper-limit threshold value of the Used Cell Counter in each class. If a cell in each class is congested in the cell buffer, exceeding the corresponding threshold value, the cell is discarded.

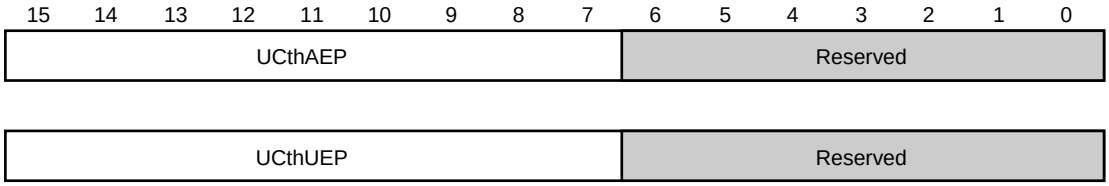
Field	Bit	R/W	Function	Default Value
UCthCBR	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: Upper-limit threshold value in CBR class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)
UCthRVR	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: Upper-limit threshold value in rtVBR class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)
UCthRM	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: Upper-limit threshold value in RM class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)

Field	Bit	R/W	Function	Default Value
UCthNVR	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: Upper-limit threshold value in nrtVBR class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)
UCthABR	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: Upper-limit threshold value in ABR class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)
UCthUBR	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: Upper-limit threshold value in UBR class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)

Remark For the cells in ABR and UBR classes for which EPD is disabled, UCthAEP and UCthUEP are the upper-limit values.

4.3.32 UC (Used Cell) Counter EPD threshold value registers (00E2h, 00EAh)

Register name	Address	Default	R/W
UCthAEP	00E2h	0000_0000_0xxx_xxxx	R/W
UCthUEP	00EAh	0000_0000_0xxx_xxxx	R/W



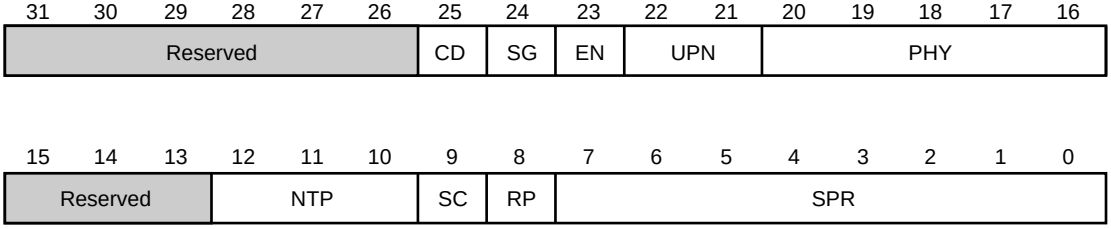
To these registers, the EPD threshold values of the UC (Used Cell) Counter in each class are set. If a cell in each class is congested in the cell buffer, exceeding the corresponding threshold value, the EPD control operation is performed and the following processing is executed:

- EPD valid cell : The cell belonging to a newly received packet is discarded. The last packet (EOP) is received, however.
- EPD invalid cell: The cell is discarded.

Field	Bit	R/W	Function	Default Value
UCthAEP	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: EPD threshold value in ABR class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)
UCthUEP	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: EPD threshold value in UBR class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)

4.3.33 Port configuration register

Register name	Address	Default	R/W
PT0-PT29	**Note**	xxxx_xx00_0001_1111_xxx0_0000_0000_0000	R/W



Note 0100h, 0104h, 0108h, 010Ch, 0110h, 0114h, 0118h, 011Ch, 0120h, 0124h, 0128h, 012Ch, 0130h, 0134h, 0138h, 013Ch, 0140h, 0144h, 0148h, 014Ch, 0150h, 0154h, 0158h, 015Ch, 0160h, 0164h, 0168h, 016Ch, 0170h, 0174h

These registers are used to map physical ports to logical ports. Do not connect an unconnected PHY device (physical port) to a logical port; otherwise, the μPD98412 polls the PHY device that does not exist and malfunctions.

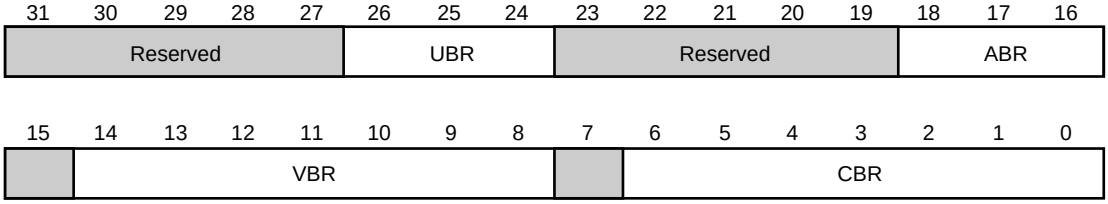
Field	Bit	R/W	Function	Default Value
CD	bit [25]	R/W	Sets the cell ejection mode. 0: Does not eject cell. 1: Ejects cell.	0
SG	bit [24]	R/W	0: Connects a physical port mapped to the corresponding logical port in the multi-PHY connection mode. 1: Connects a physical port mapped to the corresponding logical port in the single PHY connection mode. When two or more physical ports are connected in the single PHY connection mode, the lowest logical port number of each UTOPIA interface is selected.	0
EN	bit [23]	R/W	0: Invalidates the corresponding logical port. 1: Validates the corresponding logical port.	0

Field	Bit	R/W	Function	Default Value
UPN	bit [22:21]	R/W	Sets the UTOPIA interface. 8-bit UTOPIA interface 00: UTOPIA8#0 01: UTOPIA8#1 10: UTOPIA8#2 11: UTOPIA8#3 16-bit UTOPIA interface 00: UTOPIA16#0 01: UTOPIA16#1 10: Reserved 11: Reserved	00
PHY	bit [20:16]	R/W	Sets the PHY address. (1) 12-PHY polling mode (μPD98410-compatible mode) 00000-01011: PHY address 01100-11111: Reserved (2) 15-PHY polling mode 00000-01110: PHY address 01111-11111: Reserved (3) Multiplexed status polling mode and 1-group weighted polling mode 00000-11101: PHY address 11110-11111: Reserved (4) 2-group weighted polling mode PHY[4] 0: Polling Group A 1: Polling Group B PHY[3:0] 0000-1110: PHY address 11111: Reserved	11111
NTP	bit [12:10]	R/W	Specifies the number of times output is paused in the continuous output prohibit mode (RP = “0”). 0 : Output is paused once. 1 : Output is paused once. 2 : Output is paused two times. 3 : Output is paused three times. 4-7: Reserved In the 12-PHY polling mode, clear these bits to 0.	000

Field	Bit	R/W	Function	Default Value
SC	bit [9]	R/W	Corrects errors by means of shaping control. If two or more output ports connected to the same UTOPIA interface transmits cells at the same time, one of the output ports is allowed to transmit a cell and output of the other ports is delayed to prevent the throughput from dropping. 0: Does not perform shaping error correction. 1: Performs shaping error correction.	0
RP	bit [8]	R/W	Enables continuous output to the same logical output port. 0: Does not perform continuous output to the same logical output port. 1: Performs continuous output to the same logical output port. A cell may be lost if this bit is set to “1” depending on the PHY device connected. In such a case, clear this bit to “0”.	0
SPR	bit [7:0]	R/W	Sets the shaping rate of the logical output port to 1/(SPR + 1). For example, where SPR = 1, a cell is transmitted every two basic operation cycles. One basic operation cycle consists of 44 SWCLK for the 8-bit UTOPIA interface and of 22 SWCLK for the 16-bit UTOPIA interface. 00h-FFh: Sets the shaping rate in a range of 1/1 to 1/256.	00h

4.3.34 Class priority control register

Register name	Address	Default	R/W
PC0-PC29	**Note**	xxxx_x000_xxxx_x001_x111_1111_x111_1111	R/W



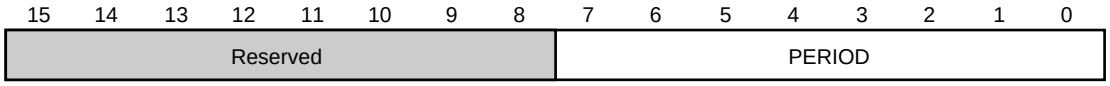
Note 0180h, 0184h, 0188h, 018Ch, 0190h, 0194h, 0198h, 019Ch, 01A0h, 01A4h, 01A8h, 01ACh, 01B0h, 01B4h, 01B8h, 01BCh, 01C0h, 01C4h, 01C8h, 01CCh, 01D0h, 01D4h, 01D8h, 01DCh, 01E0h, 01E4h, 01E8h, 01ECh, 01F0h, 01F4h

These registers specify class priority control for each logical output port. For CBR + rtVBR class and RM + nrtVBR class, the number of cells enabled to be transmitted during the period specified by the PERIOD register is specified. For ABR class and UBR class, the transmission ratio is set to ABR:UBR.

Field	Bit	R/W	Function	Default Value
CBR	bit [6:0]	R/W	00h to 7Fh: Number of CBR + rtVBR cells enabled to be transmitted during PERIOD period.	7Fh
VBR	bit [14:8]	R/W	00h to 7Fh: Number of RM + nrtVBR cells enabled to be transmitted during PERIOD period.	7Fh
ABR	bit [18:16]	R/W	0h to 7h: Cell transmission ratio of ABR class (ratio is ABR:UBR)	1h
UBR	bit [26:24]	R/W	0h to 7h: Cell transmission ratio of UBR class (ratio is UBR:ABR)	0h

4.3.35 Cycle count register (01FCh)

Register name	Address	Default	R/W
PERIOD	01FCh	xxxx_xxxx_0000_0001	R/W

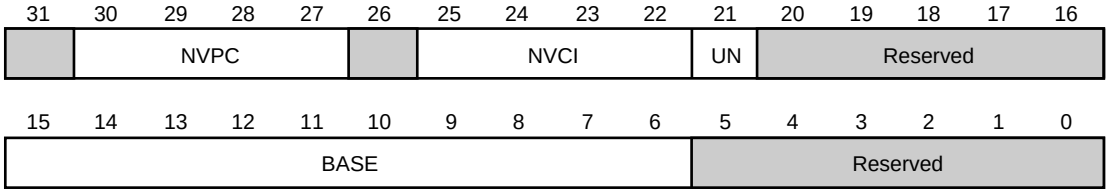


This register specifies the cycle of PC0 through PC29, CBR, and VBR. It performs class priority control of each logical output port, as well as setting of CBR and VBR for PC0 through PC29.

Field	Bit	R/W	Function	Default Value
PERIOD	bit [7:0]	R/W	00h to FFh: Cycle of class priority control	01h

4.3.36 Header translation configuration register

Register name	Address	Default	R/W
HT0-HT29	**Note**	x000_0x00_000x_xxxx_0000_0000_00xx_xxxx	R/W



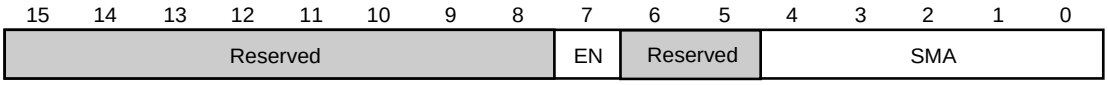
Note 0200h, 0204h, 0208h, 020Ch, 0210h, 0214h, 0218h, 021Ch, 0220h, 0224h, 0228h, 022Ch, 0230h, 0234h, 0238h, 023Ch, 0240h, 0244h, 0248h, 024Ch, 0250h, 0254h, 0258h, 025Ch, 0260h, 0264h, 0268h, 026Ch, 0270h, 0274h

This register is used to translate VPI and VCI of a received cell into the addresses of the header translation table (HTT), to translate the OVPC specified in HTT into VPC and VCI of a transmit cell, and specified NNI/UNI, for each logical output port.

Field	Bit	R/W	Function	Default Value
NVPC	bit [30:27]	R/W	6h to Fh: Valid number of VPI bits + valid number of VCI bits (6 bits to 15 bits)	0h
NVCI	bit [25:22]	R/W	3h to Fh: Valid number of VCI bits (3 bits to 15 bits)	0h
UN	bit [21]	R/W	0: Sets NNI. VPI of a received cell is treated as 12 bits, and if the invalid block of VPI is not 0 (VPI [11:(NVPC – NVCI)] ≠ 0), a header translation error occurs and the cell is discarded. The result is indicated by the HE bit of the status register and IH bit of the ERHT register. 1: Sets UNI. VPI of a received cell is treated as 8 bits, and VPI [11:8] in GFC field is treated as “don’t care”. If the invalid block of VPI is not “0” (VPI [7:(NVPC – NVCI)] ≠ 0), a header translation error occurs and the cell is discarded. The result is indicated by the HE bit of the status register and IH bit of the ERHT register.	0
BASE	bit [15:6]	R/W	0000_0000_00 to 1111_1111_11: HTT base address	000h

★ 4.3.37 Switching mode area setting register (027Ch)

Register name	Address	Default	R/W
SMA	027Ch	xxxx_xxxx_0xx0_0000	R/W



This register sets an address of the HTT that is accessed to identify the switching mode (SM).

Field	Bit	R/W	Function	Default
EN	bit[7]	R/W	0: Invalidates setting of the SMA field (VCI of input cell is replaced by 20h when calculating the HTT address to identify switching mode). 1: Validates the setting of the SMA field.	0
SMA	bit[4:0]	R/W	0-1Fh: Sets a value that replaces VCI of an input cell when calculating the HTT address to identify the switching mode.	00h

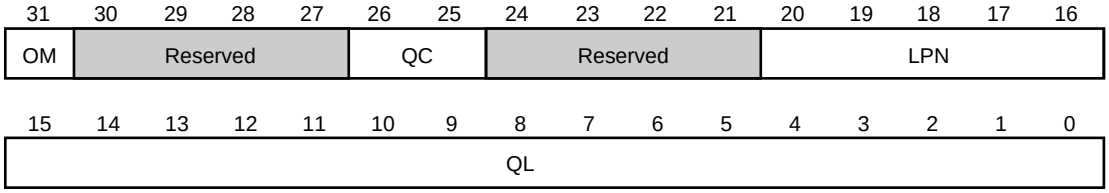
The setting range of the SMA register is limited by the set value of the NVCI field of the HTn (n = 0 to 29) register as shown in the table below. An input cell outside this range is regarded as a header conversion error and is discarded, and is indicated by the HE bit of the status register and IH bit of the ERHT register. If the set value of the NVCI field differs depending on the logic port, the SMA register must be set in accordance with the lowest value.

The range of VCI of an input cell treated by the μPD98412 as PDC (pre-defined channel) also differs as shown in the table below. All the cells that are not treated as PDC are treated as user channels.

NVCI	Setting of SMA Register	PDC
3	EN = 1, SMA = 0h to 7h	VCI = 0h to 7h, except VCI = SMA
4	EN = 1, SMA = 0h to Fh	VCI = 0h to Fh, except VCI = SMA
5	EN = 1, SMA = don't care (0h to 1Fh)	VCI = 0h to 1Fh, except VCI = SMA
6 to 15	Don't care	VCI = 0h to 1Fh, except VCI = SMA when EN = 1

4.3.38 Queue length monitor register (0280h)

Register name	Address	Default	R/W
MONQL	0280h	0xxx_x00x_xxx0_0000_0000_0000_0000_0000	R/W or R



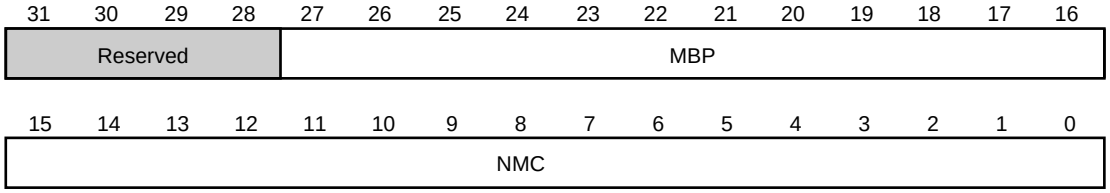
This register indicates the queue length of the queue specified by monitor conditions (output queue/multi-cast queue, queue class, and logical output port number).

A wait signal that lasts for the duration of up to 16 system clocks may be inserted until the microprocessor can access this register.

Field	Bit	R/W	Function	Default Value
OM	bit [31]	R/W	Specifies the type of the queue to be monitored. 0: Output queue 1: Multi-cast queue	0
QC	bit [26:25]	R/W	Specifies the class of the queue to be monitored. 00: CBR/rtVBR queue class 01: RM/nrtVBR queue class 10: ABR queue class 11: UBR queue class	00
LPN	bit [20:16]	R/W	Specifies the logical output port to be monitored. 00h-1Dh: Logical port number 1Eh-1Fh: Reserved	00h
QL	bit [15:0]	R	Indicates the queue length. 0000h-FFFFh: Queue length.	0000h

4.3.39 Multi-cast congested cell monitor register (0284h)

Register name	Address	Default	R/W
MONNMC	0284h	xxxx_0000_0000_0000_0000_0000_0000_0000	R/W or R



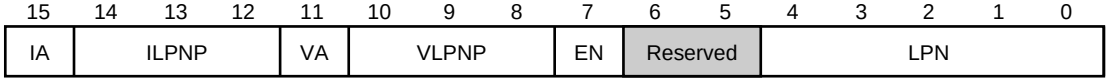
The number of congested cells that reference the HTT Area-B area specified by a multi-cast bitmap pointer (MBP) can be counted by writing the MBP set in HTT Area-A to this register.

A wait signal that lasts for the duration of up to 16 system clocks may be inserted until the MONNMC register can be accessed.

Field	Bit	R/W	Function	Default Value
MBP	bit [27:16]	R/W	Specifies the multi-cast bitmap pointer to be monitored. 000h-FFFh: Multi-cast bitmap pointer	000h
NMC	bit [15:0]	R	Indicates the number of congested cells corresponding to the specified MBP. 0000h-FFFFh: Number of congested cells	0000h

4.3.40 Special routing logical port register (0288h)

Register name	Address	Default	R/W
SRLP	0288h	0000_0000_0xx0_0000	R/W



This register is used to set the following conditions for special routing.

- Microprocessor connection port
- Position at which a virtual logical port number can be obtained
- Position at which an input logical port number is appended

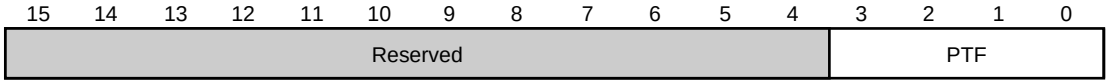
Field	Bit	R/W	Function	Default Value
IA	bit [15]	R/W	Specifies cells to which a logical input port number is to be appended. 0: All cells output to microprocessor connection port by ordinaryrouting and special routing 1: Only cells output to microprocessor connection port by special routing	0
ILPNP	bit [14:12]	R/W	Specifies the position at which a logical input port number is to be appended. 000 : Port number is not appended. 001 : High-order bits of VPI[Note] 010 : VCI [15:11] bits 011 : UDF (User Defined Field) [4:0]/UDF1 [4:0] bits 100 : UDF2 [4:0] bits 101-111: Reserved	000
VA	bit [11]	R/W	Specifies cells from which a virtual input logical port number can be obtained. 0: All cells input from microprocessor connection port 1: Cell input from microprocessor connection port and having PTI defined by SRFLT register	0
VLPNP	bit [10:8]	R/W	Specifies cells the position at which a virtual logical input port number can be obtained 000 : Port number is not used. 001 : High-order bits of VPI[Note] 010 : VCI [15:11] bits 011 : UDF [4:0]/UDF1 [4:0] bits 100 : UDF2 [4:0] bits 101-111: Reserved	000

Note The “high-order” bits are VPI [7:3] if UNI is used as the microprocessor connection port, and VPI [11:7] if NMI is used.

Field	Bit	R/W	Function	Default Value
EN	bit [7]	R/W	Specifies whether special routing is validated. 0: Invalid 1: Valid	0
LPN	bit [4:0]	R/W	Selects a microprocessor connection port for special routing. 00h-1Dh: Logical port number 0 to 29 1Eh-1Fh: Reserved	00h

4.3.41 Special routing filter register (028Ah)

Register name	Address	Default	R/W
SRFLT	028Ah	xxxx_xxxx_xxxx_0000	R/W

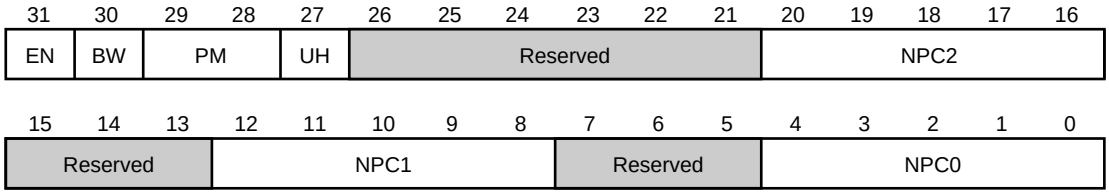


The SRFLT register is used to set the PT (payload type) field pattern of a cell supported by special routing.

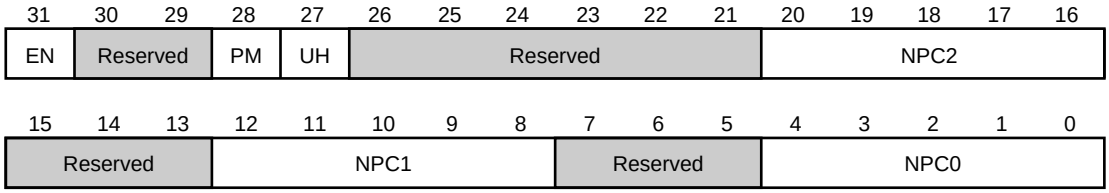
Field	Bit	R/W	Function	Default Value
PTF	bit [3:0]	R/W	Selects a PT filter for special routing. PTF [3] = Cell with PT = 111 PTF [2] = Cell with PT = 110 PTF [1] = Cell with PT = 101 PTF [0] = Cell with PT = 100 0: Special routing is not performed. 1: Special routing is performed.	0000

4.3.42 UTOPIA configuration registers (0290h, 0294h, 0298h, 029Ch)

Register name	Address	Default	R/W
UTPCFG0	0290h	1000_0xxx_xxx0_0000_xxx0_0000_xxx0_0000	R/W
UTPCDG1	0294h	1000_0xxx_xxx0_0000_xxx0_0000_xxx0_0000	R/W



Register name	Address	Default	R/W
UTPCFG2	0298h	1xx0_0xxx_xxx0_0000_xxx0_0000_xxx0_0000	R/W
UTPCFG3	029Ch	1xx0_0xxx_xxx0_0000_xxx0_0000_xxx0_0000	R/W



These registers are used to set the polling mode of the UTOPIA interfaces.

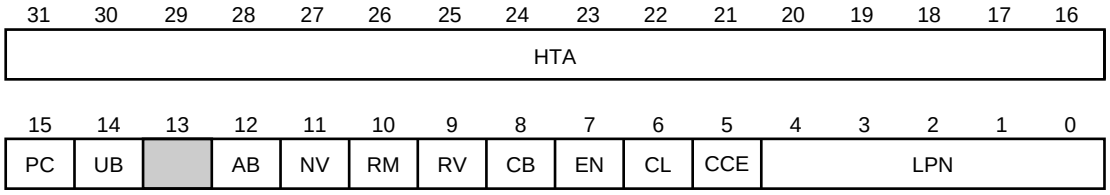
Caution If the BW bit of UTPCFG0 is set to 1, clear all the fields of UTPCFG2 to 0. If the BW bit of UTPCFG1 is set to 1, clear all the fields of UTPCFG3 to 0.

Field	Bit	R/W	Function	Default Value
EN	bit [31]	R/W	Validates or invalidates the UTOPIA interfaces. 0: UTOPIA ports are invalid. 1: UTOPIA ports are valid.	1
BW	bit [30]	R/W	Specifies the bus width of the UTOPIA interfaces. 0: 8 bits I/F 1: 16 bits I/F	0

Field	Bit	R/W	Function	Default Value
PM (UTPCFG0, UTPCFG1)	bit [29:28]	R/W	Sets a polling mode. [BW = “0” (8-bit I/F)] 00: 12-PHY polling mode (compatible with μPD98410) 01: 15-PHY polling mode 10: Reserved 11: Reserved [BW = “1” (16-bit I/F)] 00: Multiplexed status polling mode 01: 2-group weighted polling mode 10: 1-group weighted polling mode 11: Reserved	00
PM (UTPCFG2, UTPCFG3)	bit [28]	R/W	Sets a polling mode. 0: 12-PHY polling mode (compatible with μPD98410) 1: 15-PHY polling mode	0
UH	bit [27]	R/W	Sets the handshake mode of UTOPIA. 0: X10-like handshake mode 1: X15 handshake mode	0
NPC2	bit [20:16]	R/W	Sets the number of PHY devices of polling class 2. 00h-1Eh: Number of PHY devices 1Fh : Reserved	00h
NPC1	bit [12:8]	R/W	Sets the number of PHY devices of polling class 1. 00h-1Eh: Number of PHY devices 1Fh : Reserved	00h
NPC0	bit [4:0]	R/W	Sets the number of PHY devices of polling class 0. 00h-1Eh: Number of PHY devices 1Fh : Reserved	00h

★ 4.3.43 Input cell count enable register (02A0h, 02A4h, 02A8h, 02ACh)

Register name	Address	Default	R/W
CTENINP0	02A0h	0000_0000_0000_0000_00x0_0000_0000_0000	R/W
CTENINP1	02A4h	0000_0000_0000_0000_00x0_0000_0000_0000	R/W
CTENINP2	02A8h	0000_0000_0000_0000_00x0_0000_0000_0000	R/W
CTENINP3	02ACh	0000_0000_0000_0000_00x0_0000_0000_0000	R/W



These registers are used to set a condition for counting the number of input cells. The result of counting is indicated by the CTINPn register, and the EN bit is used to specify whether cells are counted.

Field	Bit	R/W	Function	Default Value
HTA	bit[31:16]	R/W	Sets the HTT access address of the input cell to be counted. In the case of counting in VP units, the low-order NVCI bit is don't care. If the HMS field of the MODE1 register is 00/01, the high-order 1/2 bits are don't care.	000h
PC	bit[15]	R/W	Sets count in VC units or count in VP units. 0: Counted in VC units 1: Counted in VP units	0
UB, AB, NV, RM, RV, CB	bit [14] bit [12:8]	R/W	Sets the service class of a cell to be counted. The abbreviations of each service class are as follows: UB: UBR class AB: ABR class NV: Non-real-time VBR class RM: RM class RV: Real-time VBR CB: CBR class 0: Not counted 1: Counted	0
EN, CL	bit [7:6]	R/W	Enables counting of cells. 0x: Not counted 10: Counted 11: Counted after counter has been cleared	00
CCE	bit[5]	R/W	Enables or disables the input cell count function in VP/VC units. 0: Disables the input cell count function in VP/VC units. 1: Enables the input cell count function in VP/VC units.	0
LPN	bit [4:0]	R/W	Sets the logical port number of a cell to be counted. 00h-1Dh: Logical port number 0 to 29 1Eh : Reserved 1Fh : All logical ports	00h

When the CCE bit of the CTENINPn (n = 0 to 3) is “0,” the target input cell is counted if the service class conditions (UB, AB, NV, RM, RV, CB) and the input logic port conditions (LPN) are met. When CCE bit is “1,” the cell is counted if the HTT access address conditions (PC, HTA) are met in addition to the service class conditions (UB, AB, NV, RM, RV, CB) and the input logic port conditions (LPN).

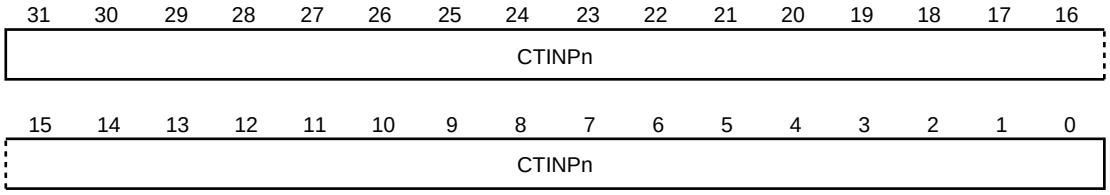
“The HTT access address of the input cell” in the explanation of the HTA field is defined as the HTT access address calculated from the input logic port BASE, input VPI, and input VCI. This differs from HTT access address calculated by replacing the input VCI with 20h (the value set in the SMA field, not 20h, when the SMA register EN bit is “1”).

The VP/VC unit input cell count function has the following restriction.

(1) VC unit input cell count cannot be performed for user channels currently executing VP switching.
(2) When the MODE1 register RMA field is set to “00,” VC unit input cell count is not performed normally for VCI = 6 or RM cell 20h (the value set in the SMA field, not 20h, when the SMA register EN bit is “1”).

4.3.44 Input cell count registers (02B0h, 02B4h, 02B8h, 02BCh)

Register name	Address	Default	R/W
CTINP0	02B0h	0000_0000_0000_0000_0000_0000_0000_0000	R/W
CTINP1	02B4h	0000_0000_0000_0000_0000_0000_0000_0000	R/W
CTINP2	02B8h	0000_0000_0000_0000_0000_0000_0000_0000	R/W
CTINP3	02BCh	0000_0000_0000_0000_0000_0000_0000_0000	R/W



The CTINPn register indicates the number of cells input under the condition set by the CTENINPn register. The input cell is counted while the EN bit of the CTENINPn register is set to 1. When the reset signal is issued to the μPD98412, the CTINPn register is cleared while the CL and EN bits of the CTENINPn register are set to 1.

When a cell is input while the current value of the counter is FFFFFFFFh, the CINn bit of the status register is set, and an interrupt request is issued to the microprocessor. At the same time, the counter is cleared to 00000000h, and continues counting. While the CINn bit of the INTMASK register is cleared to 0, the interrupt request is not issued to the microprocessor.

Field	Bit	R/W	Function	Default Value
CTINPn	bit [31:0]	R/W	Indicates the number of input cells. 00000000h-FFFFFFFFh: Number of input cells	00000000h

CHAPTER 5 JTAG BOUNDARY SCAN

The μPD98412 has a JTAG boundary scan circuit.

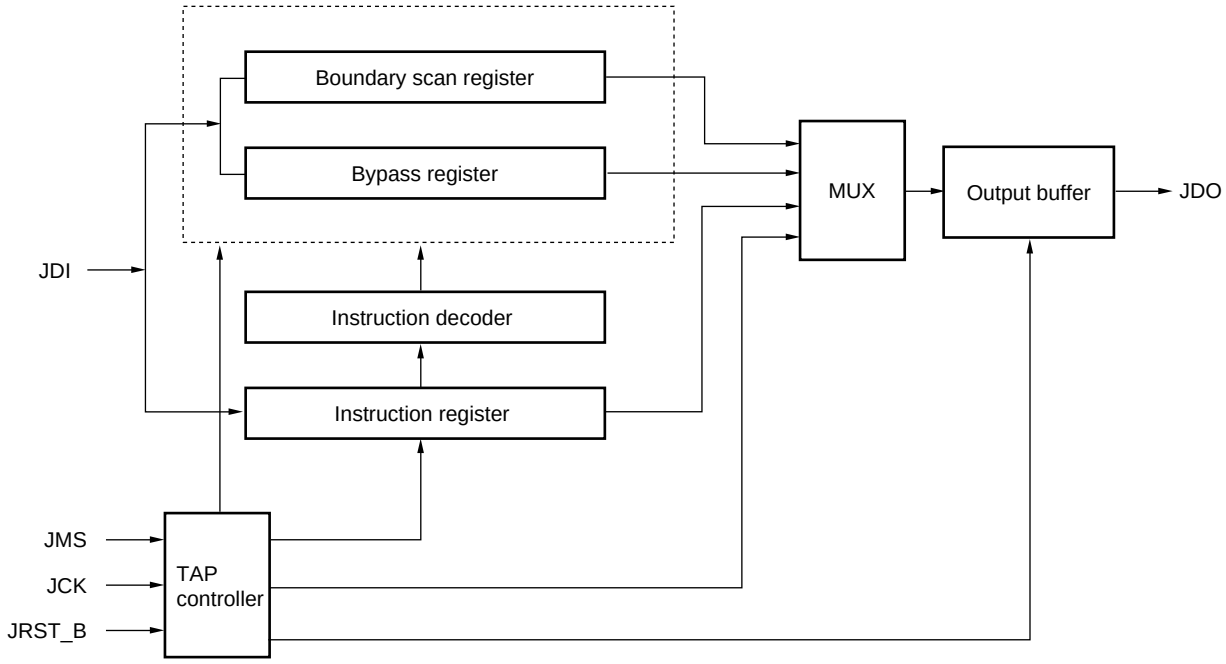
5.1 Features

- Conforms to IEEE1149.1 JTAG Boundary Scan Standard.
- Three registers dedicated to boundary scan
  - Instruction register
  - Bypass register
  - Boundary scan register
- Three instructions supported
  - BYPASS instruction
  - EXTEST instruction
  - SAMPLE/PRELOAD instruction
- Five pins dedicated to boundary scan (five pins)
  - JCK (JTAG Clock)
  - JMS (JTAG Mode Select)
  - JDI (JTAG Data Input)
  - JDO (JTAG Data Output)
  - JRST_B (JTAG Reset)

5.2 Internal Configuration of Boundary Scan Circuit

Figure 5-1 shows the block diagram of the internal JTAG boundary scan circuit of the μPD98412.

Figure 5-1. Block Diagram of Boundary Scan Circuit



5.2.1 Instruction register

The instruction register consists of a 2-bit shift register and writes instruction data from the JDI pin. The register and instruction are selected by this instruction data.

5.2.2 TAP (Test Access Port) controller

The TAP controller changes operating state by latching the signal of the JMS pin at the rising edge of the clock input to the JCK pin.

5.2.3 Bypass register

The bypass register consists of a 1-bit shift register connected between the JDI and JDO pins when the TAP controller is in Shift-DR state. If this register is selected while the TAP controller is in Shift-DR state, data is shifted to the JDO pin at the rising edge of the clock input to the JCK pin.

When this register is selected, the operation of the JTAG boundary circuit does not influence on the operation of the μPD98412.

5.2.4 Boundary scan register

The boundary scan register is located between an external pin of the μPD98412 and internal logic circuit. When this register is selected, data is latched or loaded by the instruction of the TAP controller.

If this register is selected while the TAP controller is in Shift-DR state, data is output to the JDO pin starting from the LSB at the falling edge of the clock input to the JCK pin.

5.3 Pin Function

5.3.1 JCK (JTAG Clock) pin

The JCK pin is used to supply a clock signal to the JTAG boundary scan circuit (such as the bypass register, instruction register, and TAP controller. This clock signal is isolated so as not to be supplied to the other internal circuits of the μPD98412.

5.3.2 JMS (JTAG Mode Select) pin

Input to the JMS signal is latched at the rising edge of the clock input to the JCK pin and defines the operation of the TAP controller.

5.3.3 JDI (JTAG Data Input) pin

The JDI pin is an input pin that inputs data to the JTAG boundary scan circuit register.

5.3.4 JDO (JTAG Data Output) pin

The JDO pin is an output pin that outputs data from the JTAG boundary scan circuit. This pin changes its output at the falling edge of the clock input to the JCK pin. This pin is a three-state output pin and is controlled by the TAP controller.

5.3.5 JRST_B (JTAG Reset) pin

This pin asynchronously initializes the TAP controller. This reset signal sets the μPD98412 in the normal operation mode and the boundary register in non-operation state.

5.4 Operation Description

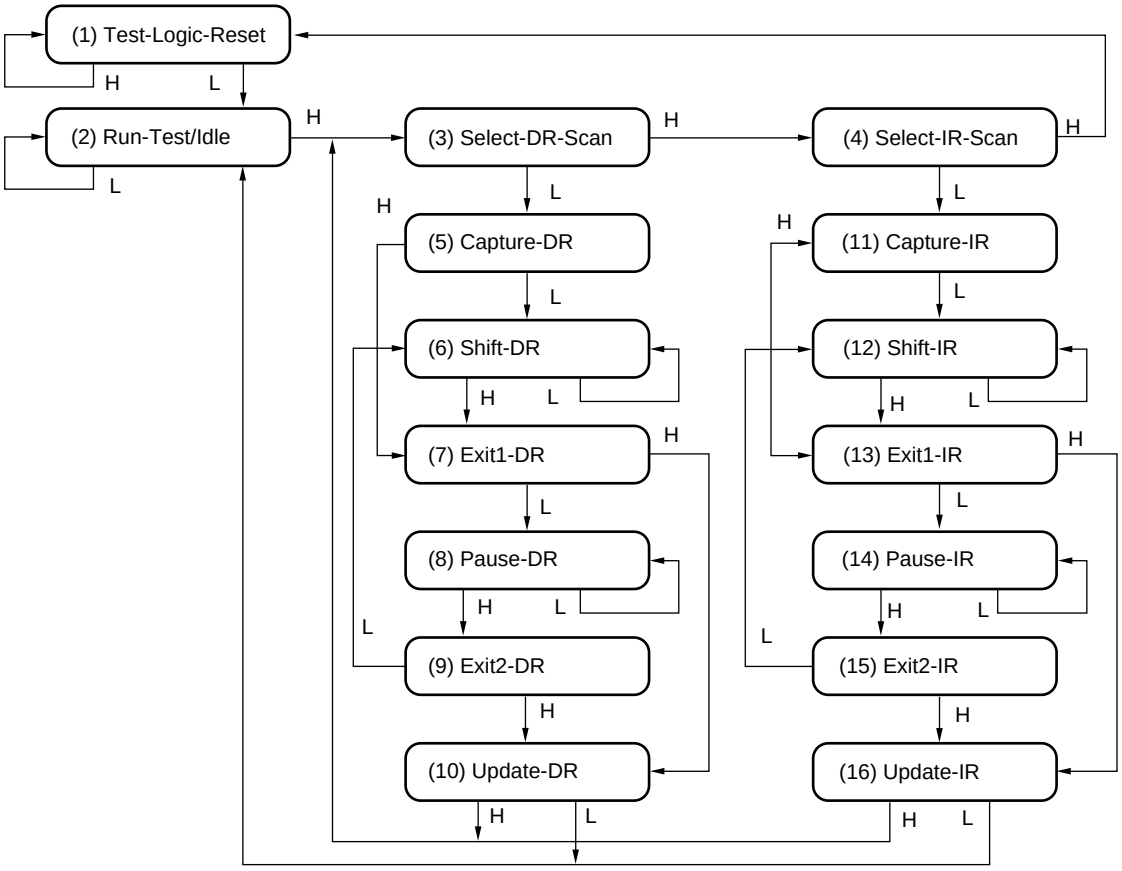
5.4.1 TAP controller

The TAP controller is a circuit having 16 states synchronized with changes of the JMS and JCK pins. Its operation is specified by IEEE Standard 1149.1.

5.4.2 TAP controller state

Figure 5-2 shows the state transition of the TAP controller. The state of the TAP controller is determined depending on the state of the JMS pin signal input at the rising edge of the clock input to the JCK pin. The operations of the instruction register, boundary scan register, and bypass register change at the rising or falling edge of the clock input to the JCK pin. (Refer to **Figure 5-3**).

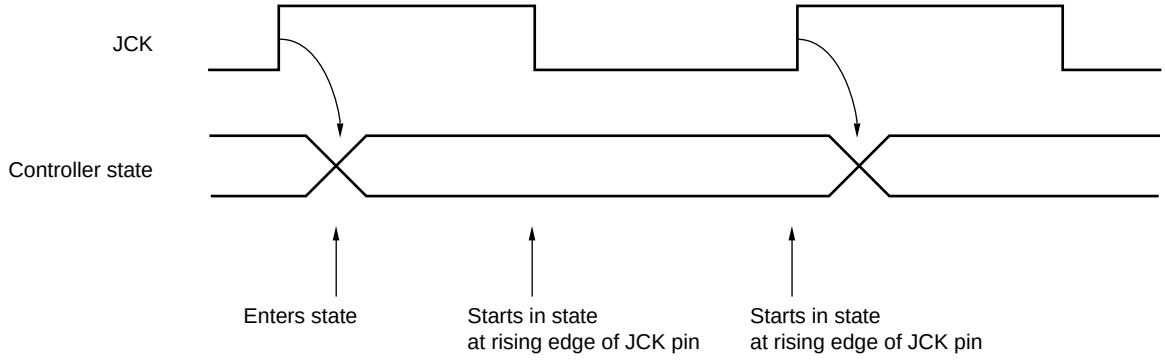
Figure 5-2. State Transition of TAP Controller



Remarks 1. "H" and "L" of the arrows indicating state transition in the above figure indicate the state of the JMS pin at the rising edge of the clock input to the JCK pin.

2. Numbers in ( ) in the above figure correspond to the explanation below.

Figure 5-3. Operation Timing in Controller State



(1) Test-Logic-Reset

The boundary scan circuit performs no operation on the μPD98412. Therefore, it does not affect the system logic of the μPD98412. This is because the bypass instruction is stored to the instruction register and executed on initialization. The TAP controller enters the Test-Logic-Reset state if the JMS pin holds the high level for the duration of at least five rising edges of the JCK pin signal, regardless of the current state of the controller. The TAP controller holds this state for the duration in which the JMS pin signal high.

If the TAP controller must be in the Test-Logic-Reset state, the controller returns to the original Test-Logic-Reset state even if a low-level signal is input once to the JMS pin by mistake (due to, for example, the influence of the external interface), if the JMS pin signal holds its high level status for the duration of three rising edges of the JCK pin signal.

The operation of the test logic does not hinder the logic operation of the μPD98412 due to the above error.

When the TAP controller exits from the Test-Logic-Reset state, the controller enters the Run-Test/Idle state. In this state, no operation is performed because the current instruction is set by the operation of the bypass register. The logic operation of the JTAG boundary scan circuit is inactive even in the Select-DR-Scan and Select-IR-Scan states.

(2) Run-Test/Idle

The TAP controller is in this state during scan operation (in Select-DR-Scan or Select-IR-Scan state). Once the controller has entered this state and if the JMS pin signal holds the low level, the controller remains in this state. The controller enters the Select-DR-Scan state if the JMS pin signal holds high level at one rising edge of the JCK pin signal.

All the test data registers (boundary register and bypass register) selected by the current instruction hold the previous status (Idle). While the TAP controller is in this state, the instruction does not change.

(3) Select-DR-Scan

This is a temporary boundary scan state. The boundary scan register and bypass register selected by the current instruction hold the previous state.

If the JMS signal is held low at the rising edge of the JCK pin signal while the TAP controller is in this state, the controller enters the Capture-DR state, and scan sequence to the selected registers is started.

If the JMS signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Select-IR-Scan state. While the controller is in this state, the instruction does not change.

(4) Select-IR-Scan

This is a temporary boundary scan state. The boundary scan register and bypass register selected by the current instruction hold the previous state.

If the JMS signal is held low at the rising edge of the JCK pin signal while the TAP controller is in this state, the controller enters the Capture-IR state, and scan sequence to the selected registers is started.

If the JMS signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Test-Logic-Reset state. While the controller is in this state, the instruction does not change.

(5) Capture-DR

In this controller state, data is loaded to the boundary scan register selected by the current instruction in parallel at the rising edge of the JCK pin signal (in this case, data is input from the input pin of each device to the corresponding boundary scan register). While the TAP controller is in this state, the instruction does not change.

If the TAP controller is in this state at the rising edge of the JCK pin signal, the controller enters the following state:

- If the JMS pin signal is held high: Exit1-DR state
- If the JMS pin signal is held low : Shift-DR state

(6) Shift-DR

In this controller state, JDI and JDO are connected (at either of the boundary scan register of bypass register) by the current instruction. The shift data is shifted one state at a time toward the serial output direction at each rising edge of the JCK pin signal.

The boundary scan register or bypass register selected by the current instruction holds the previous status without change if the controller is not on the serial bus (not in the Shift-DR state). While the controller is in this state, the instruction does not change.

If the TAP controller is in this state at the rising edge of the JCK pin signal, the controller enters the following state:

- If the JMS pin signal is held high: Exit1-DR state
- If the JMS pin signal is held low : Shift-DR state

(7) Exit1-DR

This is a temporary controller state. If the JMS pin signal is held high at the rising edge of the JCK pin signal with the TAP controller in this state, the controller enters the Update-DR state. This ends the scan process.

If the JMS pin signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Pause-DR state.

Both the bypass register and boundary scan register selected by the current instruction hold the previous status without change. While the TAP controller is in this state, the instruction does not change.

(8) Pause-DR

In this controller state, shifting between JDI and JDO connected by either the bypass register or boundary scan register is temporarily stopped. These registers selected by the current instruction hold the previous state without change.

The TAP controller remains in this state while the JMS pin signal is low. If the JMS pin signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Exit2-DR state. While the TAP controller is in this state, the instruction does not change.

(9) Exit2-DR

This is a temporary controller state. If the JMS pin signal is held high at the rising edge of the JCK pin signal with the TAP controller in this state, the controller enters the Update-DR state. This ends the scan process.

If the JMS pin signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Shift-DR state.

Both the bypass register and boundary scan register selected by the current instruction hold the previous status without change. While the TAP controller is in this state, the instruction does not change.

(10) Update-DR

The boundary scan register has a parallel output latch to prevent changes in parallel output (while shifted to the shift register path concatenated) by certain instructions (for example, EXTEST instruction).

In the Update-DR controller state, data is latched from the shift register to the parallel output latch of this register at the falling edge of the JCK pin signal.

The data retained latched to the parallel output latch changes depending on this controller state (the data does not change with the other controller states).

The previous states of all the shift register of the boundary scan register selected by the current instruction are retained.

While the TAP controller is in this state, the instruction does not change.

If the JMS pin signal is held high at the rising edge of the JCK pin signal with the TAP controller in this state, the controller enters the Select-DR-Scan state.

If the JMS signal is held low at the rising edge of the JCK signal, the TAP controller enters the Run-Test/Idle state.

(11) Capture-IR

In this controller state, the shift register loads the pattern of a fixed logic value “01B” to the instruction register at the rising edge of the JCK pin signal.

The previous states of both the bypass register and boundary scan register selected by the current instruction are retained without change.

While the TAP controller is in this state, the instruction does not change.

If the JMS pin signal is held high at the rising edge of the JCK pin signal while the controller is in this state, the controller enters the Exit1-IR state.

If the JMS pin signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Shift-IR state.

(12) Shift-IR

In this controller state, JDI and JDO are connected by the shift register in the instruction register. The shift data is shift one state toward the serial output direction at each rising edge of the JCK pin signal.

The boundary scan register or bypass register selected by the current instruction holds the previous state without change.

While the TAP controller is in this state, the instruction does not change.

If the JMS pin signal is held high at the rising edge of the JCK pin signal with the TAP controller in this state, the controller enters the Exit1-IR state. If the JMS pin signal is held low, the controller remains the Shift-IR state.

(13) Exit1-IR

This is a temporary controller state. If the JMS pin signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Update-IR state. This ends the scan process.

If the JMS pin signal is held low at the rising edge of the JCK pin, the TAP controller enters the Pause-IR state.

Both the bypass register and boundary scan register selected by the current instruction retain their states without change.

While the TAP controller is in this state, the instruction does not change.

(14) Pause-IR

In this controller state, shift of the instruction register is temporarily stopped. The bypass register and boundary scan register selected by the current instruction hold the previous state without change.

While the TAP controller is in this state, the instruction does not change. The instruction register holds the current state.

While the JMS pin signal is low, the TAP controller remains in this state. If the JMS pin signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Exit2-IR state.

(15) Exit2-IR

This is a temporary controller state. If the JMS pin signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Update-IR state. This ends the scan process.

If the JMS pin signal is held low at the rising edge of the JCK pin, the TAP controller enters the Shift-IR state.

Both the bypass register and boundary scan register selected by the current instruction retain their states without change.

While the TAP controller is in this state, or while the instruction register holds the current state, the instruction does not change.

(16) Update-IR

In this controller state, the instruction shifted to the instruction register is latched to the parallel output latch from the shift register path at the falling edge of the JCK pin signal. Once a new instruction has been latched, it is used as the current instruction.

The bypass register or boundary scan register selected by the current instruction holds the previous state.

If the JMS pin signal is held high at the rising edge of the JCK pin signal while the TAP controller is in this state, the TAP controller enters the Select-DR-Scan state.

If the JMS pin signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Run-Test/Idle state.

The Pause-DR controller state in (8) and Pause-IR controller state in (14) temporarily stop shifting of data in the bypass register, the boundary scan register, or instruction register.

5.5 TAP Controller Operation

The TAP controller operates as follows.

The state of the controller is changed by either of (1) and (2) below.

(1) Rising edge of JCK pin signal
(2) JRST_B pin input

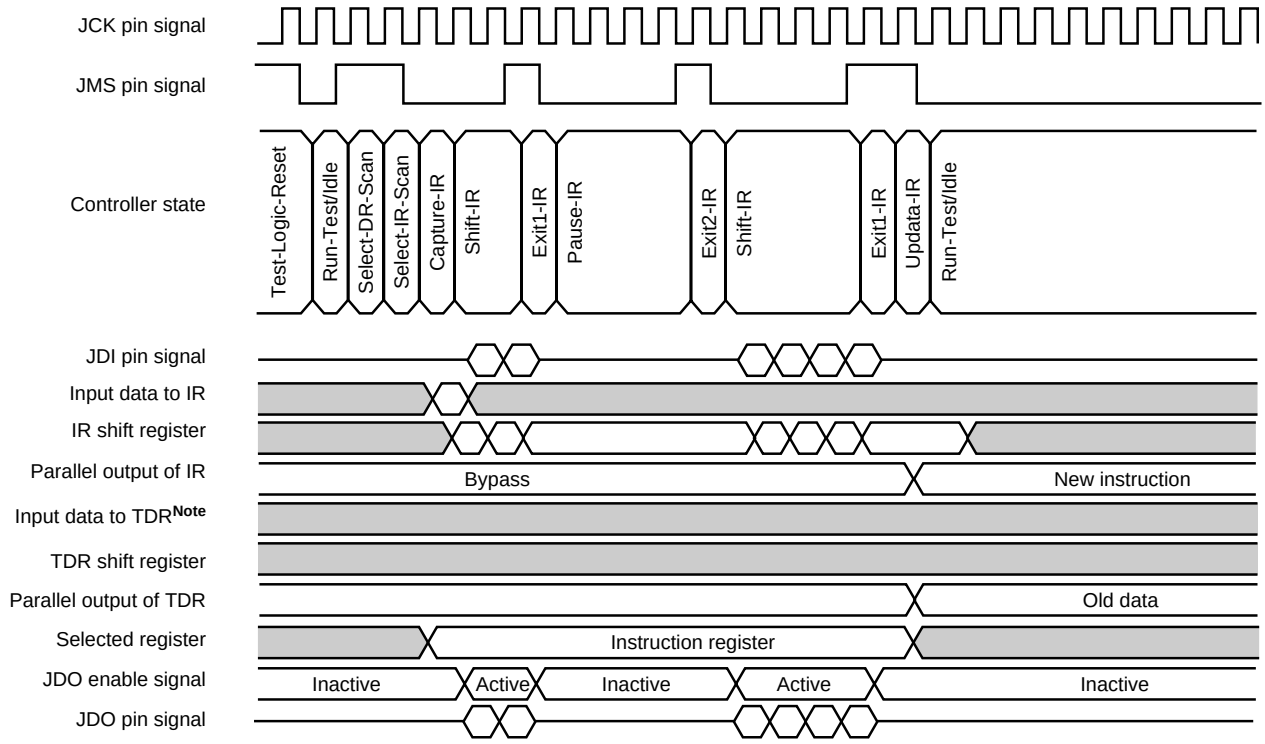
The TAP controller generates signals that control the operations of the bypass register, boundary scan register, and instruction register defined by the IEEE1149.1 JTAG Boundary Scan Standard (refer to **Figures 5-4** and **5-5**).

The JDO pin output buffer and the peripheral circuit that selects a register whose contents are to be output to the JDO pin are controlled as shown in Table 5-1. The JDO pin defined in this table changes at the falling edge of the JCK pin signal after it has entered each state.

Table 5-1. Operation in Each Controller State

Controller State	Selected Register to Be Driven to JDO Pin	JDO Pin Driver
Test-Logic-Reset	Undefined	High impedance
Run-Test/Idle		
Select-DR-Scan		
Select-IR-Scan		
Capture-IR		
Shift-IR	Instruction register	Active
Exit1-IR	Undefined	High impedance
Pause-IR		
Exit2-IR		
Update-IR		
Capture-DR		
Shift-DR	Data register (boundary scan register, bypass register)	Active
Exit1-DR	Undefined	High impedance
Pause-DR		
Exit2-DR		
Update-DR		

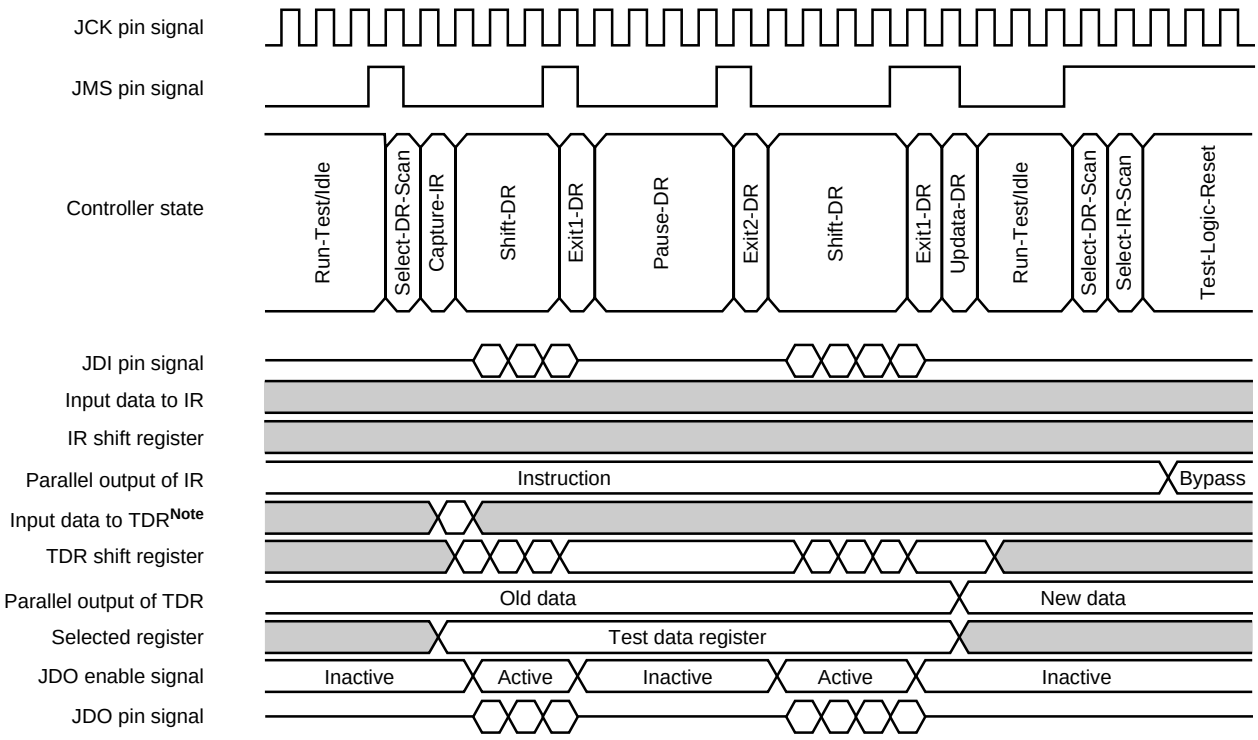
Figure 5-4. Operation of Test Logic (Instruction Scan)



Note TDR (Test Data Register): Boundary scan register and bypass register

Remark ▭: Don't care or undefined

Figure 5-5. Operation of Test Logic (Data Scan)



Note TDR (Test Data Register): Boundary scan register and bypass register

Remark ▭: Don't care or undefined

5.6 Initializing TAP Controller

The TAP controller is initialized as follows:

(1) The TAP controller is not initialized by the operation of system input such as system reset.
(2) The TAP controller enters the Test-Logic-Reset controller state at the fifth rising edge of the JCK pin signal (while the JMS pin signal is held high).
(3) The TAP controller asynchronously enters the Test-Logic-Reset state when the JRST_B signal is input.

5.7 Instruction Register

This register is defined as follows (refer to **5.2 Internal Configuration of Boundary Scan Circuit**).

(1) The instruction shifted and input to the instruction register is latched so that it changes only in the Update-IR and Test-Logic-Reset controller states.
(2) Data is not inverted since it has been serially input to the instruction register until it is serially output.
(3) A fixed binary pattern data “01” (with LSB (Least Significant Bit) being “1”) is loaded to this register cell in the Capture-IR controller state.
(4) A fixed binary pattern data “01” (with LSB being “1”) is loaded to this register cell in the Test-Logic-Reset controller state.
(5) While this register is read, data is output from the JDO pin, starting from the LSB to the MSB (Most Significant Bit), at each falling edge of the JCK pin signal.

The JTAG boundary scan circuit of the μPD98412 can support only the following three instructions depending on the data set to the instruction register.

- BYPASS instruction
- EXTEST instruction
- SAMPLE/PRELOAD instruction

x: 0 or 1

Instruction Register			Supported Instruction
D2	D1	D0	
0	0	0	EXTEST instruction
1	0	0	Unused
x	0	1	Unused
x	1	0	Unused
0	1	1	SAMPLE/PRELOAD instruction
1	1	1	BYPASS instruction

5.7.1 BYPASS instruction

This instruction is specified by instruction data “11”. This instruction is used to select only the bypass register (to access between the JDI and JDO pins serially) in the Shift-DR controller state.

While this instruction is selected, the operation of the JTAG boundary scan circuit does not affect the operation of the μPD98412.

This bypass instruction is selected while the TAP controller is in the Test-Logic-Reset state.

5.7.2 EXTEST instruction

This instruction is specified by instruction data “00”. In the Shift-DR controller state, this instruction is used to select the boundary scan register of serial access between the JDI and JDO instructions.

- While this instruction is selected:

The states of all the signals driven from the system output pins are completely defined by the data shifted to the boundary scan register. In the Update-DR controller state, the states of all the signals are changed only by the falling edge of the JCK pin signal.

The states of all the signals input from the system input pins are loaded to the boundary scan register at the rising edge of the JCK pin signal while the TAP controller is in the Capture-DR state.

5.7.3 SAMPLE/PRELOAD instruction

Input/output data can be sampled or set using the SAMPLE or PRELOAD instruction without affecting the device and external logic. Either the SAMPLE or PRELOAD function is selected depending on the status of the TAP controller. When the SAMPLE function is used during the normal operation, the status of the input/output data of each pin of the device when testing can be latched to the boundary scan register. The PRELOAD function is used to set test data to be used prior to the execution of the EXTEST instruction.

5.8 Boundary Scan Data Bit Definition

NEC will provide the BSDL (Boundary Scan Description Language) file for the μPD98412 upon request. For details, call NEC Semiconductor Technical Hot Line shown at the end of this document.

[MEMO]

CHAPTER 6 EXAMPLES OF SETTING AND OPERATION

This chapter explains specific examples of setting and operation of the μPD98412.

6.1 Example of Connection Setting Procedure

This section explains how to set a new connection, or update or delete an existing connection. Observe the procedure explained below while the μPD98412 is operating.

6.1.1 Single cast connection

<Procedure for new connection and updating>

(1) Set HTT Area-A that is referenced by VCI with VCI = input cell.
(2) Set HTT Area-A that is referenced with VCI = 20h or VCI = value set in the SMA field.

<Procedure for deletion>

- VC connection
  (1) Write 0 to the CEN field of HTT Area-A that is referenced by VCI with VCI = input cell.

- VP connection
  (1) Write 0 to the CEN field of HTT Area-A that is referenced with VCI = 20h or VCI = value set in the SMA field.

Supplement

Only HTT Area-A is set for single cast connection. The cell that is input after HTT Area-A has been updated is in compliance with the updated setting. Because HTT Area-A is referenced when a cell is input with single cast connection, the cells queued before HTT Area-A is updated are output in compliance with the setting before updating.

6.1.2 Multi-cast connection

Both HTT Area-A and HTT Area-B must be set for multicast connection. Therefore, the following procedures for new setting, updating, and deletion must be observed. This section first explains the basic procedure, and then details of the new connection, updating, and deletion procedures.

<Basic procedure>

(1) Confirm that there is no cell congestion by using the multi-cast congested cell monitoring function.
If cells are congested, it means that the corresponding HTT Area-B has been already used. In this case, either wait until there are no more congested cells, or use another HTT Area-B.

(2) Updating HTT Area-B
Assign the header information (OVPC) appended to an output cell and broadcast destination (MB) to HTT Area-B checked in step (1).

(3) Updating HTT Area-A
Set HTT Area-A in accordance with the same procedure as single cast connection, and validate multi-cast connection.

With multi-cast connection, HTT Area-B is referenced at the following timing:

- Requeuing (cell movement from multi-cast queue to output queue)
- Cell output from output queue

If HTT Area-B is re-set while cells are congested, the output destination of the congested cells is not guaranteed.

Next, each of the procedures for setting new connection, and updating and deleting existing connection is explained.

<Procedure of setting new connection>

(1) Confirm that there is no cell congestion by using the multi-cast congested cell monitoring function.
If cells are congested, the corresponding HTT Area-B is referenced by another connection. In this case, either wait until there are no more congested cells, or use another HTT Area-B.

(2) Setting of HTT Area-B
Set OVPC and MB of HTT Area-B.

(3) Setting of HTT Area-A
Set HTT Area-A and validate multi-cast connection.

The existing connection can be updated in the following two ways:

<Procedure 1> Invalidating multi-cast connection once

This procedure is a combination of deleting the existing connection and setting a new connection.

(1) Reset the CEN field of HTT Area-A to 0 to invalidate multi-cast connection.
(2) Confirm that there is no cell congestion, by using the multi-cast congested cell monitoring function.
If cells are congested, HTT Area-B cannot be updated. Wait until there are no more congested cells.
(3) Update OVPC and MB of HTT Area-B.
(4) Set the CEN field of HTT Area-A to validate multi-cast connection again.

<Procedure 2> Updating with multi-cast connection remaining valid

Use to HTT Area-B's and follow the procedure below.

(1) Find and secure an HTT Area-B not used for another connection by using the multi-cast congested cell monitoring function.
If cells are congested, it means that the corresponding HTT Area-B is being used for other connection. In this case, either wait until there are no more congested cells, or use another HTT Area-B.

(2) Setting of HTT Area-B
Write new settings to the HTT Area-B that has been confirmed that it can be used in step (1).

(3) Update the multi-cast bitmap pointer of HTT Area-A.
Update the value of MBP so that newly set HTT Area-B is updated. New cells are input in accordance with the updated setting. The cell that was queued before MBP is updated is output in accordance with the setting of HTT Area-B which has been made by the previous MBP. To use HTT Area-B before updating, therefore, step (4) must be observed.

(4) Confirm that no cell is referencing the previous setting of HTT Area-A, by using the multi-cast congested cell monitoring function.
If there are no congested cells, the previous HTT Area-B can be used again.

<Deletion procedure>

(1) Clear the CEN field of HTT Area-A to 0 to invalidate multi-cast connection.
(2) Confirm that there are no congested cells, by using the multi-cast congested cell monitoring function.

6.2 Example of Polling Sequence

[Example 1] 2-group weighted polling mode

[Setting]

Entries in Utopia Configuration 0 (UTPCFG0) Register:

EN = 1 (UTOPIA Interface enable)
BW = 1 (UTOPIA Interface 16-bit)
PM = 01 (2-group weighted polling)
UH = 1 (X15 handshake mode)
NPC0 = 0011 (3 PHYs in class 0)
NPC1 = 0100 (4 PHYs in class 1)
NPC2 = 0101 (5 PHYs in class 2)

Entries in Port Configuration (PT) Registers:

PT 0:	UPN = 00 (UTOPIA16#0)	EN = 1 (Port Enable), SG = 0 (Multi-PHY), RP = 1 (Continuous Output Enable),
	PHY [4] = 0 (Group A)	PHY [3:0] = 0000 (PHY address 0h)
PT 1:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 0 (Group A)	PHY [3:0] = 0010 (PHY address 2h)
PT 2:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 0 (Group A)	PHY [3:0] = 0100 (PHY address 4h)
PT 3:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 0 (Group A)	PHY [3:0] = 0111 (PHY address 7h)
PT 10:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 1 (Group B)	PHY [3:0] = 0010 (PHY address 2h)
PT 11:	UPN = 00	EN = 1, SG = 0, RP =1,
	PHY [4] = 1 (Group B)	PHY [3:0] = 0011 (PHY address 3h)
PT 20:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 1 (Group B)	PHY [3:0] = 0101 (PHY address 5h)
PT 21:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 1 (Group B)	PHY [3:0] = 0111 (PHY address 7h)
PT 22:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 1 (Group B)	PHY [3:0] = 1000 (PHY address 8h)

For all other PTxx Register: EN = 0 (disabled)

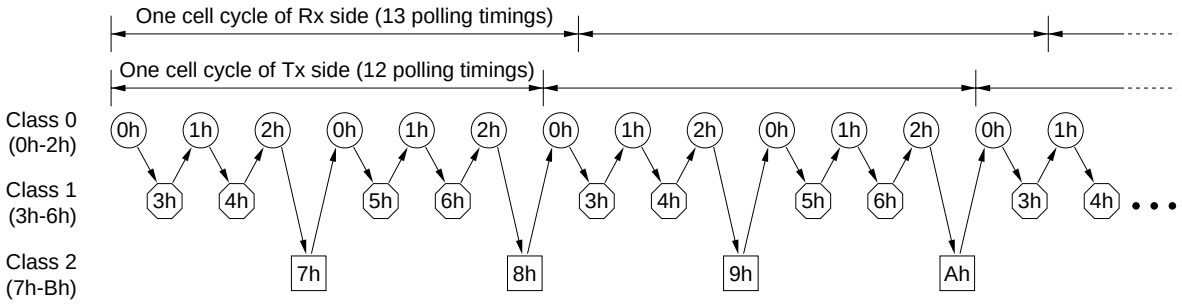
[Operation]

The PHY addresses and logical ports are allocated to polling classes as shown below.

Polling Class		PHY Address	Logical Port (PTxx)
Class 0	Group A	0h 1h 2h	0 1
	Group B	0h 1h 2h	10
Class 1	Group A	3h 4h 5h 6h	2
	Group B	3h 4h 5h 6h	11 20
Class 2	Group A	7h 8h 9h Ah Bh	3
	Group B	7h 8h 9h Ah Bh	21 22
No assign	Group A	Ch Dh Eh	none
	Group B	Ch Dh Eh	none

The order of the polling addresses is determined by the relation between polling classes and PHY addresses as shown below.

Case of “NPC0 = 3, NPC1 = 4, NPC2 = 5”



Remark PHY addresses belonging to no polling class are not shown in this order.

The polling addresses in the above figure are output to RxADDR/TxADDR at all the timings except SA (Selection Address), RPA (Receiving Polling Address)/TPA (Transmitting Polling Address). However, PHY addresses not assigned to the PT register, even if the PHY address is allocated to a polling class, are masked with Fh.

Therefore, the PHY address sequence of RxADDR/TxADDR is as follows during cell transfer:

Rx Group A	0h - Fh - Fh - 4h - 2h - 7h - 0h - Fh - Fh - Fh - 2h - Fh - 0h	-PRA - SA
Rx Group B	Fh - 3h - Fh - Fh - 2h - 7h - Fh - 5h - Fh - Fh - 2h - 8h - Fh	-PRA - SA
Tx Group A	0h - Fh - Fh - 4h - 2h - 7h - 0h - Fh - Fh - Fh - 2h - Fh - TPA	- SA
Tx Group B	Fh - 3h - Fh - Fh - 2h - 7h - Fh - 5h - Fh - Fh - 2h - 8h - TPA	- SA

[Example 2] 2-group weighted polling mode

[Setting]

Entries in Utopia Configuration 0 (UTPCFG0) Register:

EN = 1 (UTOPIA Interface enable)
BW = 1 (UTOPIA Interface 16-bit)
PM = 01 (2-group weighted polling)
UH = 1 (X15 handshake mode)
NPC0 = 0011 (3 PHYs in class 0)
NPC1 = 0101 (5 PHYs in class 1)
NPC2 = 0000 (0 PHYs in class 2)

Entries in Port Configuration (PT) Registers: (Same setting as **Example 1**)

PT 0:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 0 (Group A)	PHY [3:0] = 0000 (PHY address 0h)
PT 1:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 0 (Group A)	PHY [3:0] = 0010 (PHY address 2h)
PT 2:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 0 (Group A)	PHY [3:0] = 0100 (PHY address 4h)
PT 3:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 0 (Group A)	PHY [3:0] = 0111 (PHY address 7h)
PT 10:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 1 (Group B)	PHY [3:0] = 0010 (PHY address 2h)
PT 11:	UPN = 00	EN = 1, SG = 0, RP =1,
	PHY [4] = 1 (Group B)	PHY [3:0] = 0011 (PHY address 3h)
PT 20:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 1 (Group B)	PHY [3:0] = 0101 (PHY address 5h)
PT 21:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 1 (Group B)	PHY [3:0] = 0111 (PHY address 7h)
PT 22:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 1 (Group B)	PHY [3:0] = 1000 (PHY address 8h)

For all other PTxx Register: EN = 0 (disabled)

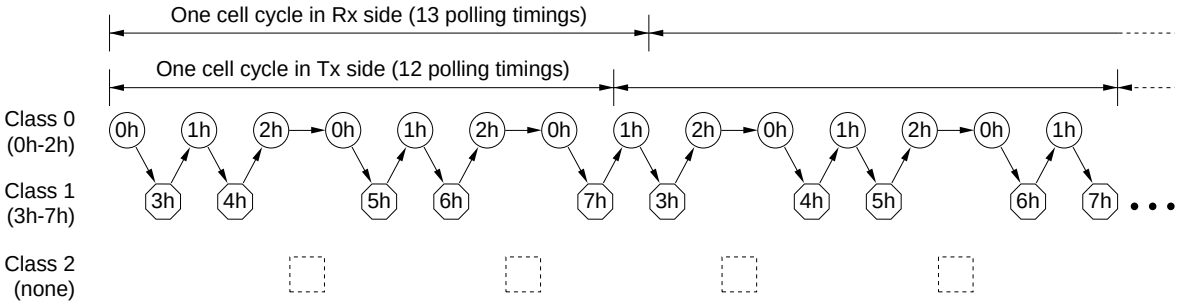
[Operation]

The PHY addresses and logical ports are allocated to polling classes as shown below.

Polling Class		PHY Address	Logical Port (PTxx)
Class 0	Group A	0h 1h 2h	0 1
	Group B	0h 1h 2h	10
Class 1	Group A	3h 4h 5h 6h 7h	2 3
	Group B	3h 4h 5h 6h 7h	11 20 21
Class 2	Group A	none	none
	Group B	none	none
No assign	Group A	8h 9h Ah Bh Ch Dh Eh	none
	Group B	8h 9h Ah Bh Ch Dh Eh	22

The order of the polling addresses is determined by the relation between polling classes and PHY addresses as shown below.

Case of “NPC0 = 3, NPC1 = 5, NPC2 = 0”



Remark PHY addresses belonging to no polling class are not shown in this order.

The PHY address sequence of RxADDR/TxADDR is as follows during cell transfer:

Rx Group A 0h - Fh - Fh - 4h - 2h - 0h - Fh - Fh - Fh - 2h - 0h - 7h - Fh -PRA - SA
Rx Group B Fh - 3h - Fh - Fh - 2h - Fh - 5h - Fh - Fh - 2h - Fh - 7h - Fh -PRA - SA

Tx Group A 0h - Fh - Fh - 4h - 2h - 0h - Fh - Fh - Fh - 2h - 0h - 7h - TPA - SA
Tx Group B Fh - 3h - Fh - Fh - 2h - Fh - 5h - Fh - Fh - 2h - Fh - 7h - TPA - SA

[Example 3] 2-group weighted polling mode

[Setting]

Entries in Utopia Configuration 0 (UTPCFG0) Register:

EN = 1 (UTOPIA Interface enable)
BW = 1 (UTOPIA Interface 16-bit)
PM = 01 (2-group weighted polling)
UH = 1 (X15 handshake mode)
NPC0 = 0100 (4 PHYs in class 0)
NPC1 = 0000 (0 PHYs in class 1)
NPC2 = 0010 (2 PHYs in class 2)

Entries in Port Configuration (PT) Registers:

PT 0:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 0 (Group A)	PHY [3:0] = 0000 (PHY address 1h)
PT 1:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 0 (Group A)	PHY [3:0] = 0010 (PHY address 2h)
PT 2:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 0 (Group A)	PHY [3:0] = 0011 (PHY address 3h)
PT 3:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 0 (Group A)	PHY [3:0] = 0100 (PHY address 4h)
PT 10:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 1 (Group B)	PHY [3:0] = 1011 (PHY address Bh)
PT 11:	UPN = 00	EN = 1, SG = 0, RP =1,
	PHY [4] = 1 (Group B)	PHY [3:0] = 1100 (PHY address Ch)
PT 20:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 0 (Group A)	PHY [3:0] = 0110 (PHY address 6h)
PT 21:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 0 (Group A)	PHY [3:0] = 0111 (PHY address 7h)
PT 22:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4] = 1 (Group B)	PHY [3:0] = 1101 (PHY address Dh)

For all other PTxx Register: EN = 0 (disabled)

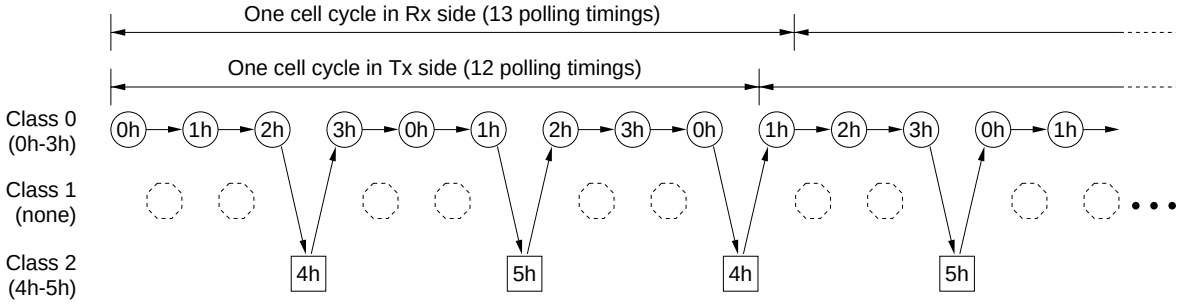
[Operation]

The PHY addresses and logical ports are allocated to polling classes as shown below.

Polling Class		PHY Address	Logical Port (PTxx)
Class 0	Group A	0h 1h 2h 3h	0 1 2
	Group B	0h 1h 2h 3h	none
Class 1	Group A	none	none
	Group B	none	none
Class 2	Group A	4h 5h	3
	Group B	4h 5h	none
No assign	Group A	6h 7h 8h 9h Ah Bh Ch Dh Eh	20 21
	Group B	6h 7h 8h 9h Ah Bh Ch Dh Eh	10 11 22

The order of the polling addresses is determined by the relation between polling classes and PHY addresses as shown below.

Case of “NPC0 = 4, NPC1 = 0, NPC2 = 2”



Remark PHY addresses belonging to no polling class are not shown in this order.

The PHY address sequence of RxADDR/TxADDR is as follows during cell transfer:

Rx Group A Fh - 1h - 2h - 4h - 3h - Fh - 1h - Fh - 2h - 3h - Fh - 4h - 1h -PRA - SA
Rx Group B Fh - Fh - Fh - Fh - Fh - Fh - Fh - Fh - Fh - Fh - Fh - Fh - Fh -PRA - SA

Tx Group A Fh - 1h - 2h - 4h - 3h - Fh - 1h - Fh - 2h - 3h - Fh - 4h - TPA - SA
Tx Group B Fh - Fh - Fh - Fh - Fh - Fh - Fh - Fh - Fh - Fh - Fh - Fh - TPA - SA

[Example 4] 1-group weighted polling mode

[Setting]

Entries in Utopia Configuration 0 (UTPCFG0) Register:

EN = 1 (UTOPIA Interface enable)
BW = 1 (UTOPIA Interface 16-bit)
PM = 01 (1-group weighted poling)
UH = 1 (X15 handshake mode)
NPC0 = 00100 (4 PHYs in class 0)
NPC1 = 01000 (8 PHYs in class 1)
NPC2 = 01100 (12 PHYs in class 2)

Entries in Port Configuration (PT) Registers:

PT 0:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4-0] = 00001 (PHY address 01h)	
PT 1:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4-0] = 00010 (PHY address 02h)	
PT 2:	UPN = 00	EN 1, SG = 0, RP = 1,
	PHY [4-0] = 00011 (PHY address 03h)	
PT 3:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4-0] = 00100 (PHY address 04h)	
PT 10:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4-0] = 01011 (PHY address 0Bh)	
PT 11:	UPN = 00	EN = 1, SG = 0, RP =1,
	PHY [4-0] = 01100 (PHY address 0Ch)	
PT 20:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4-0] = 00110 (PHY address 06h)	
PT 21:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4-0] = 00111 (PHY address 07h)	
PT 22:	UPN = 00	EN = 1, SG = 0, RP = 1,
	PHY [4-0] = 01101 (PHY address 0Dh)	

For all other PTxx: EN = 0 (disabled)

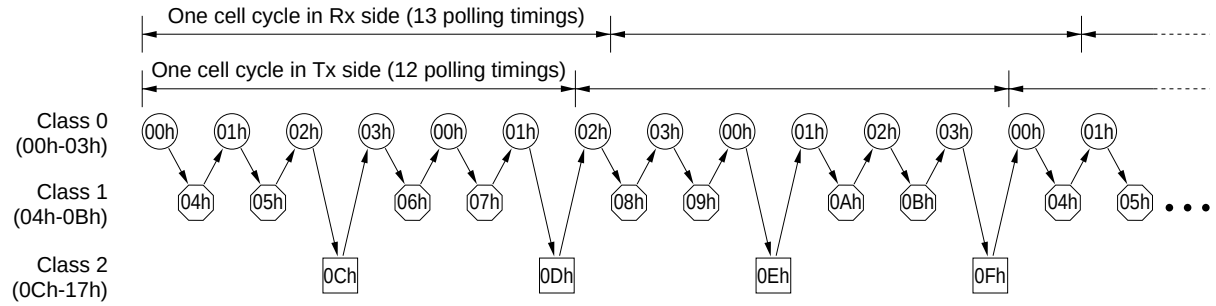
[Operation]

The PHY addresses and logical ports are allocated to polling classes as shown below.

Polling Class	PHY Address	Logical Port (PTxx)
Class 0	00h 01h 02h 03h	0 1 2
Class 1	04h 05h 06h 07h 08h 09h 0Ah 0Bh	3 10 20 21
Class 2	0Ch 0Dh 0Eh 0Fh 10h 11h 12h 13h 14h 15h 16h 17h	11 22
No assign	18h 19h 1Ah 1Bh 1Ch 1Dh	none

The order of the polling addresses is determined by the relation between polling classes and PHY addresses as shown below.

Case of “NPC0 = 4, NPC1 = 8, NPC2 = 12”



Remark The PHY addresses belonging to no polling class are not shown in this order.

The PHY address sequence of RxADDR/TxADDR is as follows during cell transfer:

Rx	1Fh - 04h - 01h - 1Fh - 02h - 0Ch - 03h - 06h - 1Fh - 07h - 01h - 0Dh - 02h - RPA - SA
Tx	1Fh - 04h - 01h - 1Fh - 02h - 0Ch - 03h - 06h - 1Fh - 07h - 01h - 0Dh - TPA - SA

6.3 Special Routing Supplement

6.3.1 Special routing function

Special routing realizes the following three functions:

(Function 1) Function to output a specific cell in the ordinary routing to the microprocessor connection port
(Function 2) Function to append a logical input port number to a cell output to the microprocessor connection port
(Function 3) Function to use a virtual logical input port number of the routing of a cell input from the microprocessor connection port

These functions are explained in detail below.

Function 1 Function to output a specific cell in the ordinary routing to the microprocessor connection port

(a) Single cast connection

If the input cell satisfies a set condition, it is output to the microprocessor connection port.

(b) Multi-cast connection

If the input cell satisfies a set condition, it is output only to the microprocessor connection port, but not to the other broadcast destinations.

[Conditions of specific cell supported by special routing]

(a) If cell is input from non-microprocessor connection port

- Pre-defined Channel
  Cell belonging to connection with SRM set to 1 in HTT Area-A

- User Channel
  Cell having PTI coinciding with the value of the PT filter (PTF field of SRFLT register)
  However, connection must be set to VC connection (SM bit of HTT Area-A is 0).
  The cell of VP connection is not supported by special routing.

(b) If cell is input from microprocessor connection port

This is not supported by special routing.

[Microprocessor connection port]

The microprocessor connection port means a logical port set by the LPN field of the SRLP register.

[PT filter]

The value of the PT filter can be set to the SRFLT register.

The PT filter can set the following values as the PTI field supported by special routing.

PTI = 111
PTI = 110
PTI = 101
PTI = 100

[VPI and VCI of output cell]

If a cell is output to the microprocessor connection port by special routing, that output cell holds the values of input VPI and VCI.

[EFCI marking]

If the queue length of the microprocessor connection port exceeds the EFCI threshold value, a special routine processes the PTI field of the cell as follows:

(a) If the EF bit of the MODE0 register is 0

Cell of VC/VP connection: Performs EFCI marking
PTI = 000 → 010
PTI = 001 → 011

(b) If the EF bit of the MODE0 register is 1

Cell of VC connection: Performs EFCI marking.
PTI = 000 → 010
PTI = 001 → 011
Cell of VP connection: Does not perform EFCI marking.

[CI/NI marking of RM cell]

If the RM cell is output to the microprocessor connection port by special routing, CI/NI marking is not performed.

[Merging RM cell]

If the RM cell is output to the microprocessor connection port by special routing, RM cell merge is not performed.

[CLP]

If the cell is output to the microprocessor connection port by special routing, CLP of the input cell is not changed.

[Threshold value for discarding cell]

If the cell is output to the microprocessor connection port, the threshold value of the microprocessor connection port is used.

Function 2 Function to append a logical input port number to a cell output to the microprocessor connection port

Cells can be also output to the microprocessor connection port by ordinary routing, not only by special routing.

(a) If the IA bit of the SRLP register is 0

A logical input port number is appended to the cell output to the microprocessor connection port by special routing and ordinary routing.

(b) If the IA bit of the SRLP register is 1

A logical input port number is appended to the cell output to the microprocessor connection port by special routing.

[Position of logical input port number]

The position at which the logical input port number is appended can be specified by using the ILPNP field of the SRLP register.

Position of logical input port	
VPI [11:7]	(NNI)
VPI [7:3]	(UNI)
VCI [15:11]	
UDF [4:0]	(8-bit UTOPIA I/F)
UDF1 [4:0]	(16-bit UTOPIA I/F)
UDF2 [4:0]	(16-bit UTOPIA I/F)

A setting that does not append a logical input port number can be also made.

Remark UDF (User Defined Field), UDF1, and UDF2 are the following fields:

- 16-bit UTOPIA interface

Bit 15 Bit 0

Header 1	Header 2
Header 3	Header 4
UDF1	UDF2
Payload 1	Payload 2
:	:
Payload 47	Payload 48

- 8-bit UTOPIA interface

Bit 8 E

Header 1
Header 2
Header 3
Header 4
UDF
Payload 1
:
Payload 48

Function 3 Function to use the virtual logical input port number of the routing of a cell input from the microprocessor connection port

When HTT is accessed, the address of HTT is calculated by using a virtual logical input port number.

(a) If the VA bit of the SRLP register is 0

The virtual logical input port number is used for all the cells input from the microprocessor connection port.

(b) If the VA bit of the SRLP register is 1

The virtual logical input port number is used only for a cell having the PTI field defined by the PTFLT register of the cells input from the microprocessor connection port.

[Position of virtual logical input port number]

The position at which the virtual logical input port number can be obtained can be specified by the VLPNP field of the SRLP register.

Position of virtual logical input port
VPI [11:7] (NNI)
VPI [7:3] (UNI)
VCI [15:11]
UDF [4:0] (8-bit UTOPIA I/F)
UDF1 [4:0] (16-bit UTOPIA I/F)
UDF2 [4:0] (16-bit UTOPIA I/F)

A setting that does not use the virtual logical input port number can be also made. In that case, HTT is accessed by using a microprocessor connection port number.

6.3.2 Examples of routing

(1) To input cells from single cast and non-microprocessor connection ports

Basic setting 1
Register
MODE0 EF = 1
MODE1 HMS = 00, CMD = 00
HT0 NVPC = 1010 (10), NVCI = 1000 (8), UN = 1 (UNI), BASE = 0000_0000_00
HT1 NVPC = 1010 (10), NVCI = 1000 (8), UN = 1 (UNI), BASE = 0000_0100_00
HT2 NVPC = 1010 (10), NVCI = 1000 (8), UN = 1 (UNI), BASE = 0000_1000_00
HT3 NVPC = 1010 (10), NVCI = 1000 (8), UN = 1 (UNI), BASE = 0000_1100_00
SRLP EN = 1, ILPNP = 010 (VCI), VLPNP = 010 (VCI), LPN = 0_0011 (3), IA = 0, VA = 0
SRFLT PTF = 0010
Queue length of logical port number 0 < OQthACI (EFCI threshold value)
Queue length of logical port number 0 < OQthACL (CLP threshold value)
Queue length of logical port number 1 < OQthACI (EFCI threshold value)
Queue length of logical port number 1 < OQthACL (CLP threshold value)
Queue length of logical port number 2 < OQthACI (EFCI threshold value)
Queue length of logical port number 2 < OQthACL (CLP threshold value)
Queue length of logical port number 3 < OQthACI (EFCI threshold value)
Queue length of logical port number 3 < OQthACL (CLP threshold value)

(Example. 1-01) ..... No function of special routing
Pre-defined channel, SRM = 0, output to non-microprocessor connection port

Basic setting 1 + following setting
HTT
//LPN#1, VPI = 1, VCI = 04h (VP OAM/F4)

01410h CEN = 1, SC = 100 (ABR), SRM = 0, CM = 0, SPI = 0_0010 (2), OVPC = 0208h

Input cell: //VP OAM (End-End)/F4 OAM
LPN#1,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0000_0100 (0004h),
PTI = 000
CLP = 0
Output cell:
LPN#2,
VPI = 0000_0000_0010 (002h),
VCI = 0000_0000_0000_1000 (0008h),
PTI = 000
CLP = 0

(Example. 1-02) ..... Special routing function 2
Pre-defined channel, SRM = 0, output to microprocessor connection port

Basic setting 1 + following setting
HTT
//LPN#1, VPI = 1, VCI = 04h (VP OAM/F4)
01410h CEN = 1, SC = 100 (ABR), SRM = 0, CM = 0, SPI = 0_0011 (3), OVPC = 0208h

Input cell: //VP OAM (End-End)/F4 OAM
LPN#1,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0000_0100 (0004h),
PTI = 000
CLP = 0
Output cell:
LPN#3,
VPI = 0000_0000_0010 (002h),
VCI = 0000_1000_0000_1000 (0808h),
PTI = 000
CLP = 0

(Example. 1-03) ..... Special routing function 1 and 2
Pre-defined channel, SRM = 1, output to non-microprocessor connection port

Basic setting 1 + following setting
HTT
//LPN#1, VPI = 1, VCI = 04h (VP OAM/F4)
01410h CEN = 1, SC = 100 (ABR), SRM = 1, CM = 0, SPI = 0_0010 (2), OVPC = 0208h

Input cell: //VP OAM (End-End)/F4 OAM
LPN#1,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0000_0100 (0004h),

PTI = 000
CLP = 0

Output cell:
LPN#3,
VPI = 0000_0000_0001 (001h),
VCI = 0000_1000_0000_0100 (0804h),
PTI = 000
CLP = 0

(Example. 1-04) ..... Special routing function 1 and 2
Pre-defined channel, SRM = 1, output to microprocessor connection port

Basic setting 1 + following setting
HTT
//LPN#1, VPI = 1, VCI = 04h (VP OAM/F4)
01410h CEN = 1, SC = 100 (ABR), SRM = 1, CM = 0, SPI = 0_0011 (3), OVPC = 0208h

Input cell: //VP OAM (End-End)/F4 OAM
LPN#1,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0000_0100 (0004h),
PTI = 000
CLP = 0

Output cell:
LPN#3,
VPI = 0000_0000_0001 (001h),
VCI = 0000_1000_0000_0100 (0804h),
PTI = 000
CLP = 0

(Example. 1-05) ..... No function of special routing
User channel, SM = 1 (VPC), CM = 0, output to non-microprocessor connection port

Basic setting 1 + following setting
HTT
//LPN#1, VPI = 1, VCI = 20h
01480h CEN = 1, SC = 100 (ABR), SM = 1, CM = 0, SPI = 0_0010 (2), OVPC = 0002h

Input cell: //VP OAM (End-End)/F5 OAM
LPN#1,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0010_0010 (0022h),
PTI = 101
CLP = 0

Output cell:
LPN#2,
VPI = 0000_0000_0010 (002h),
VCI = 0000_0000_0010_0010 (0022h),

PTI = 101
CLP = 0

(Example. 1-06) ..... Special routing function 2
User channel, SM = 1 (VPC), CM = 0, output to microprocessor connection port

Basic setting 1 + following setting
HTT
//LPN#1, VPI = 1, VCI = 20h
01480h CEN = 1, SC = 100 (ABR), SM = 1, CM = 0, SPI = 0_0011 (3), OVPC = 0002h

Input cell: //VP OAM (End-End)/F5 OAM
LPN#1,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0010_0010 (0022h),
PTI = 101
CLP = 0
Output cell:
LPN#3,
VPI = 0000_0000_0010 (002h),
VCI = 0000_1000_0010_0010 (0822h),
PTI = 101
CLP = 0

(Example. 1-07) ... No function of special routing
User channel, SM = 0 (VCC), CM = 0, output to non-microprocessor connection port, PTI ≠ PTF

Basic setting 1 + following setting
HTT
//LPN#1, VPI = 1, VCI = 20h
01480h CEN = 1, SM = 0,
//LPN#1, VPI = 1, VCI = 22h
01488h CEN = 1, SC = 100 (ABR), SM = 0, CM = 0, SPI = 0_0010 (2), OVPC = 0224h

Input cell: //VC OAM (Segment)/F5 OAM
LPN#1,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0010_0010 (0022h),
PTI = 100
CLP = 0
Output cell:
LPN#2,
VPI = 0000_0000_0010 (002h),
VCI = 0000_0000_0010_0100 (0024h),
PTI = 100
CLP = 0

(Example. 1-08) ..... Special routing function 1 and 2

User channel, SM = 0 (VCC), CM = 0, output to non-microprocessor connection port, PTI = PTF

Basic setting 1 + following setting
HTT
//LPN#1, VPI = 1, VCI = 20h
01480h CEN = 1, SM = 0
//LPN#1, VPI = 1, VCI = 22h
01488h CEN = 1, SC = 100 (ABR), SM = 0, CM = 0, SPI = 0_0010 (2), OVPC = 0224h

Input cell: //VC OAM (End-End)/F5 OAM
LPN#1,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0010_0010 (0022h),
PTI = 101
CLP = 0
Output cell:
LPN#3,
VPI = 0000_0000_0001 (001h),
VCI = 0000_1000_0010_0010 (0822h),
PTI = 101
CLP = 0

(Example. 1-09) ..... Special routing function 2
User channel, SM = 0 (VCC), CM = 0, output to microprocessor connection port, PT ≠ PTF

Basic setting 1 + following setting
HTT
//LPN#1, VPI = 1, VCI = 20h
01480h CEN = 1, SM = 0
//LPN#1, VPI = 1, VCI = 22h
01488h CEN = 1, SC = 100 (ABR), SM = 0, CM = 0, SPI = 0_0011 (3), OVPC = 0224h

Input cell: //VP OAM (Segment)/F5 OAM
LPN#1,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0010_0010 (0022h),
PTI = 100
CLP = 0
Output cell:
LPN#3,
VPI = 0000_0000_0010 (002h),
VCI = 0000_1000_0010_0100 (0824h),
PTI = 100
CLP = 0

(Example. 1-10) ..... Special routing function 1 and 2
User channel, SM = 0 (VCC), CM = 0, output to microprocessor connection port, PTI = PTF

Basic setting 1 + following setting
HTT
//LPN#1, VPI = 1, VCI = 20h
01480h CEN = 1, SM = 0
//LPN#1, VPI = 1, VCI = 22h
01488h CEN = 1, SC = 100 (ABR), SM = 0, CM = 0, SPI = 0_0011 (3), OVPC = 0224h

Input cell: //VC OAM (End-End)/F5 OAM
LPN#1,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0010_0010 (0022h),
PTI = 101
CLP = 0
Output cell:
LPN#3,
VPI = 0000_0000_0001 (001h),
VCI = 0000_1000_0010_0010 (0822h),
PTI = 101
CLP = 0

(2) To input cells from multi-cast and non-microprocessor connection ports

(Example. 2-01) ..... No function of special routing
Pre-defined channel, SRM = 0, output to non-microprocessor connection port

Basic setting 1 + following setting
HTT
//LPN#1, VPI = 1, VCI = 04h (VP OAM/F4)
01410h CEN = 1, SC = 100 (ABR), SRM = 0, CM = 1, MBP = 000h
//MBP = 0
10000h OVPC for LPN0 = 0207h
| OVPC for LPN2 = 0308h
1003Fh LPN0 = 1, LPN2 = 1, others = 0

Input cell: //VP OAM (End-End)/F4 OAM
LPN#1,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0000_0100 (0004h),
PTI = 000
CLP = 0
Output cell:
LPN#0,
VPI = 0000_0000_0010 (002h),
VCI = 0000_0000_0000_0111 (0007h),
PTI = 000
CLP = 0

LPN#2,
VPI = 0000_0000_0011 (003h),
VCI = 0000_0000_0000_1000 (0008h),
PTI = 000
CLP = 0

(Example. 2-02) ..... Special routing function 2
Pre-defined channel, SRM = 0, output to microprocessor connection port

Basic setting 1 + following setting
HTT
//LPN#1, VPI = 1, VCI = 04h (VP OAM/F4)
01410h CEN = 1, SC = 100 (ABR), SRM = 0, CM = 1, MBP = 000h
//MBP = 0
10000h OVPC for LPN2 = 0208h
| OVPC for LPN3 = 0309h
1003Fh LPN2 = 1, LPN3 = 1, others = 0

Input cell: //VP OAM (End-End)/F4 OAM
LPN#1,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0000_0100 (0004h),
PTI = 000
CLP = 0
Output cell:
LPN#2,
VPI = 0000_0000_0010 (002h),
VCI = 0000_0000_0000_1000 (0008h),
PTI = 000
CLP = 0

LPN#3,
VPI = 0000_0000_0011 (003h),
VCI = 0000_1000_0000_1001 (0809h),
PTI = 000
CLP = 0

(Example. 2-03) ..... Special routing function 1 and 2
Pre-defined channel, SRM = 1, output to microprocessor connection port

Basic setting 1 + following setting
HTT
//LPN#1, VPI = 1, VCI = 04h (VP OAM/F4)
01410h CEN = 1, SC = 100 (ABR), SRM = 1, CM = 1, MBP = 000h
//MBP = 0
10000h OVPC for LPN2 = 0208h
| OVPC for LPN2 = 0309h
1003Fh LPN2= 1, LPN3 = 1, others = 0

Input cell: //VP OAM (End-End)/F4 OAM
LPN#1,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0000_0100 (0004h),
PTI = 000
CLP = 0
Output cell:
LPN#3,
VPI = 0000_0000_0001 (001h),
VCI = 0000_1000_0000_0100 (0804h),
PTI = 000
CLP = 0

(3) When a microprocessor connection port has been changed

Basic setting 2
Register: Change the LPN field of the SRLP register. Others are the same as Basic setting 1.
SRLP EN = 1, ILPNP = 010 (VCI), VLPNP = 010 (VCI), LPN = 0_0010(2), IA = 0, VA = 0

(Example. 3-01) ..... Special routing function 2
Pre-defined channel, SRM = 0, output to microprocessor connection port

Basic setting 2 + following setting
HTT
//LPN#1, VPI = 1, VCI = 04h (VP OAM/F4)
01410h CEN = 1, SC = 100 (ABR), SRM = 0, CM = 0, SPI = 0_0010 (2), OVPC = 0208h

Input cell: //VP OAM (End-End)/F4 OAM
LPN#1,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0000_0100 (0004h),
PTI = 000
CLP = 0
Output cell:
LPN#2,
VPI = 0000_0000_0010 (002h),
VCI = 0000_1000_0000_1000 (0808h),
PTI = 000
CLP = 0

(Example. 3-02) ..... No function of special routing
Pre-defined channel, SRM = 0, output to non-microprocessor connection port

Basic setting 2 + following setting
HTT
//LPN#1, VPI = 1, VCI = 04h (VP OAM/F4)
01410h CEN = 1, SC = 100 (ABR), SRM = 0, CM = 0, SPI = 0_0011 (3), OVPC = 0208h

Input cell: //VP OAM (End-End)/F4 OAM
LPN#1,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0000_0100 (0004h),
PTI = 000
CLP = 0

Output cell:
LPN#3,
VPI = 0000_0000_0010 (002h),
VCI = 0000_0000_0000_1000 (0008h),
PTI = 000
CLP = 0

(4) When ILPNP has been changed

Basic setting 3

Register: Change the ILPNP field of the SRLP register. Others are the same as Basic setting 1.
SRLP EN = 1, ILPNP = 011 (UDF), VLPNP = 010 (VCI), LPN = 0_0011(3), IA = 0, VA = 0

(Example. 4-01) ..... Special routing function 1 and 2
User channel, SM = 0 (VCC), CM = 0, output to non-microprocessor connection port, PTI = PTF

Basic setting 3 + following setting
HTT
//LPN#1, VPI = 1, VCI = 20h
01480h CEN = 1, SM = 0
//LPN#1, VPI = 1, VCI = 22h
01488h CEN = 1, SC = 100 (ABR), SM = 0, CM = 0, SPI = 0_0010 (2), OVPC = 0224h

Input cell: //VC OAM (End-End)/F5 OAM
LPN#1,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0010_0010 (0022h),
PTI = 101
CLP = 0

Output cell:
LPN#3,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0010_0010 (0022h),
PTI = 101
CLP = 0
UDF = 0000_0001 (01h)

Basic setting 4

Register: Change the ILPNP field of the SRLP register. Others are the same as Basic setting 1.

SRLP EN = 1, ILPNP = 000 (none), VLPNP = 010 (VCI), LPN = 0_0011(3), IA = 0, VA = 0

(Example. 4-02) ..... Special routing function 1
User channel, SM = 0 (VCC), CM = 0, output to non-microprocessor connection port, PTI = PTF

Basic setting 4 + following setting
HTT
//LPN#1, VPI = 1, VCI = 20h
01480h CEN = 1, SM = 0
//LPN#1, VPI = 1, VCI = 22h
01488h CEN = 1, SC = 100 (ABR), SM = 0, CM = 0, SPI = 0_0010 (2), OVPC = 0224h

Input cell: //VP OAM (End-End)/F5 OAM
LPN#1,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0010_0010 (0022h),
PTI = 101
CLP = 0
Output cell:
LPN#3,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0010_0010 (0022h),
PTI = 101
CLP = 0

(5) When the threshold value is exceeded

Basic setting 5
Queue length of the logical port number 3 > OQthACI (EFCI threshold value)
Others are the same as Basic setting 1.

(Example. 5-01) ..... Special routing function 1 and 2
Pre-defined channel, SRM = 1, output to non-microprocessor connection port

Basic setting 5 + following setting
HTT
//LPN#1, VPI = 1, VCI = 04h (VP OAM/F4)
01410h CEN = 1, SC = 100 (ABR), SRM = 1, CM = 0, SPI = 0_0010 (2), OVPC = 0208h

Input cell: //VP OAM (End-End)/F4 OAM
LPN#1,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0000_0100 (0004h),
PTI = 000
CLP = 0
Output cell:

LPN#3,
VPI = 0000_0000_0001 (001h),
VCI = 0000_1000_0000_0100 (0804h),
PTI = 010
CLP = 0

(Example. 5-02) ..... Special routing function 1 and 2
User channel, SM = 0 (VCC), CM = 0, output to non-microprocessor connection port, PTI = PTF

Basic setting 5 + following setting
HTT
//LPN#1, VPI = 1, VCI = 20h
01480h CEN = 1, SM = 0
//LPN#1, VPI = 1, VCI = 22h
01488h CEN = 1, SC = 100 (ABR), SM = 0, CM = 0, SPI = 0_0010 (2), OVPC = 0224h

Input cell: //VC OAM (End-End)/F5 OAM
LPN#1,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0010_0010 (0022h),
PTI = 101
CLP = 0
Output cell:
LPN#3,
VPI = 0000_0000_0001 (001h),
VCI = 0000_1000_0010_0010 (0822h),
PTI = 101
CLP = 0

Basic setting 6
Queue length of the logical port number 3 > OQthACL (CLPI threshold value)
Others are the same as Basic setting 1.

(Example. 5-03) ..... No function of special routing
User channel, SM = 0 (VCC), CM = 0, output to non-microprocessor connection port, PTI = PTF

Basic setting 6 + following setting
HTT
//LPN#1, VPI = 1, VCI = 20h
01480h CEN = 1, SM = 0
//LPN#1, VPI = 1, VCI = 22h
01488h CEN = 1, SC = 100 (ABR), SM = 0, CM = 0, SPI = 0_0010 (2), OVPC = 0224h

Input cell: //VC OAM (End-End)/F5 OAM
LPN#1,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0010_0010 (0022h),

PTI = 101
CLP = 1

Output cell: When the CLP threshold value has been exceeded, the cell is discarded.

(6) To input from microprocessor connection port

(Example. 6-01) ..... Special routing function 3
Pre-defined channel, SRM = 0, output to non-microprocessor connection port

Basic setting 1 + following setting
HTT
//LPN#1, VPI = 1, VCI = 04h (VP OAM/F4)
01410h CEN = 1, SC = 100 (ABR), SRM = 0, CM = 0, SPI = 0_0010 (2), OVPC = 0208h

Input cell: //VP OAM (End-End)/F4 OAM
LPN#3,
VPI = 0000_0000_0001 (001h),
VCI = 0000_1000_0000_0100 (0804h),
PTI = 000
CLP = 0
Output cell:
LPN#2,
VPI = 0000_0000_0010 (002h),
VCI = 0000_0000_0000_1000 (0008h),
PTI = 000
CLP = 0

(Example. 6-02) ..... Special routing function 3
Pre-defined channel, SRM = 1, output to non-microprocessor connection port

Basic setting 1 + following setting
HTT
//LPN#1, VPI = 1, VCI = 04h (VP OAM/F4)
01410h CEN = 1, SC = 100 (ABR), SRM = 1, CM = 0, SPI = 0_0010 (2), OVPC = 0208h

Input cell: //VP OAM (End-End)/F4 OAM
LPN#3,
VPI = 0000_0000_0001 (001h),
VCI = 0000_1000_0000_0100 (0804h),
PTI = 000
CLP = 0
Output cell:
LPN#2,
VPI = 0000_0000_0010 (002h),
VCI = 0000_0000_0000_1000 (0008h),
PTI = 000
CLP = 0

(Example. 6-03) ..... Special routing function 3

User channel, SM = 1 (VPC), CM = 0, output to non-microprocessor connection port

Basic setting 1 + following setting

HTT

//LPN#1, VPI = 1, VCI = 20h

01480h CEN = 1, SC = 100 (ABR), SM = 1, CM = 0, SPI = 0_0010 (2), OVPC = 0002h

Input cell: //VC OAM (End-End)/F5 OAM

LPN#3,

VPI = 0000_0000_0001 (001h),

VCI = 0000_1000_0010_0010 (0822h),

PTI = 101

CLP = 0

Output cell:

LPN#2,

VPI = 0000_0000_0010 (002h),

VCI = 0000_0000_0010_0010 (0022h),

PTI = 101

CLP = 0

(Example. 6-04) ..... Special routing function 3

User channel, SM = 0 (VCC), CM = 0, output to non-microprocessor connection port, PTI = PTF

Basic setting 1 + following setting

HTT

//LPN#1, VPI = 1, VCI = 20h

01480h CEN = 1, SM = 0,

//LPN#1, VPI = 1, VCI = 22h

01488h CEN = 1, SC = 100 (ABR), SM = 0, CM = 0, SPI = 0_0010 (2), OVPC = 0224h

Input cell: //VC OAM (End-End)/F5 OAM

LPN#3,

VPI = 0000_0000_0001 (001h),

VCI = 0000_1000_0010_0010 (0822h),

PTI = 101

CLP = 0

Output cell:

LPN#2,

VPI = 0000_0000_0010 (002h),

VCI = 0000_0000_0010_0100 (0024h),

PTI = 101

CLP = 0

Basic setting 7

Register: Change the VLPNP field of the SRLP register. Others are the same as Basic setting 1.

SRLP EN = 1, ILPNP = 010 (VCI), VLPNP = 000 (none), LPN = 0_0011(3), IA = 0, VA = 0

(Example. 6-05) ..... No function of special routing
User channel, SM = 0 (VCC), CM = 0, output to non-microprocessor connection port, PTI = PTF

Basic setting 7 + following setting
HTT
//LPN#3, VPI = 1, VCI = 20h
03480h CEN = 1, SM = 0,
//LPN#3, VPI = 1, VCI = 22h
03488h CEN = 1, SC = 100 (ABR), SM = 0, CM = 0, SPI = 0_0010 (2), OVPC = 0224h

Input cell: //VP OAM (End-End)/F5 OAM
LPN#3,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0010_0010 (0022h),
PTI = 101
CLP = 0
Output cell:
LPN#2,
VPI = 0000_0000_0010 (002h),
VCI = 0000_0000_0010_0100 (0024h),
PTI = 101
CLP = 0

(Example. 6-06) ..... Special routing function 3
User channel, SM = 0 (VCC), CM = 0, output to non-microprocessor connection port, PTI = PTF

Basic setting 1 + following setting
HTT
//LPN#3, VPI = 1, VCI = 20h
03480h CEN = 1, SM = 0,
//LPN#3, VPI = 1, VCI = 22h
03488h CEN = 1, SC = 100 (ABR), SM = 0, CM = 0, SPI = 0_0010 (2), OVPC = 0224h

Input cell: //VC OAM (End-End)/F5 OAM
LPN#3,
VPI = 0000_0000_0001 (001h),
VCI = 0001_1000_0010_0010 (1822h),
PTI = 101
CLP = 0
Output cell:
LPN#2,
VPI = 0000_0000_0010 (002h),
VCI = 0000_0000_0010_0100 (0024h),
PTI = 101
CLP = 0

(7) To input from non-microprocessor connection port (EF = 0, IA = 1, VA = 1)

(Example. 7-01) ..... No function of special routing
Pre-defined channel, SRM = 0, output to microprocessor connection port

Basic setting 1 + following setting (except for EF = 0, IA = 1, VA = 1)
HTT
//LPN#1, VPI = 1, VCI = 04h (VP OAM/F4)
01410h CEN = 1, SC = 100 (ABR), SRM = 0, CM = 0, SPI = 0_0011 (3), OVPC = 0208h

Input cell: //VP OAM (End-End)/F4 OAM
LPN#1,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0000_0100 (0004h),
PTI = 000
CLP = 0
Output cell:
LPN#3,
VPI = 0000_0000_0010 (002h),
VCI = 0000_0000_0000_1000 (0008h),
PTI = 000
CLP = 0

(8) To input from microprocessor connection port (EF = 0, IA = 1, VA = 1)

(Example. 8-01) ..... Special routing function 3
Pre-defined channel, SRM = 0, output to non-microprocessor connection port

Basic setting 1 + following setting (except for EF = 0, IA = 1, VA = 1)
HTT
//LPN#3, VPI = 1, VCI = 04h (VP OAM/F4)
03410h CEN = 1, SC = 100 (ABR), SRM = 0, CM = 0, SPI = 0_0010 (2), OVPC = 0208h

Input cell: //VP OAM (End-End)/F4 OAM
LPN#3,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0000_0100 (0004h),
PTI = 000
CLP = 0
Output cell:
LPN#2,
VPI = 0000_0000_0010 (002h),
VCI = 0000_0000_0000_1000 (0008h),
PTI = 000
CLP = 0

(Example. 8-02) ..... Special routing function 3

Pre-defined channel, SRM = 1, output to non-microprocessor connection port

Basic setting 1 + following setting (except for EF = 0, IA = 1, VA = 1)
HTT
//LPN#3, VPI = 1, VCI = 04h (VP OAM/F4)
03410h CEN = 1, SC = 100 (ABR), SRM = 1, CM = 0, SPI = 0_0010 (2), OVPC = 0208h

Input cell: //VP OAM (End-End)/F4 OAM
LPN#3,
VPI = 0000_0000_0001 (001h)
VCI = 0000_0000_0000_0100 (0004h),
PTI = 000
CLP = 0
Output cell:
LPN#2,
VPI = 0000_0000_0010 (002h),
VCI = 0000_0000_0000_1000 (0008h),
PTI = 000
CLP = 0

(Example. 8-03) ..... Special routing function 3
User channel, SM = 1 (VPC), CM = 0, output to non-microprocessor connection port, PTI = PTF

Basic setting 1 + following setting (except for EF = 0, IA = 1, VA = 1)
HTT
//LPN#1, VPI = 1, VCI = 20h
01480h CEN = 1, SC = 100 (ABR), SM = 1, CM = 0, SPI = 0_0010 (2), OVPC = 0002h

Input cell: //VC OAM (End-End)/F5 OAM
LPN#3,
VPI = 0000_0000_0001 (001h),
VCI = 0000_1000_0010_0010 (0822h),
PTI = 101
CLP = 0
Output cell:
LPN#2,
VPI = 0000_0000_0010 (002h),
VCI = 0000_0000_0010_0010 (0022h),
PTI = 101
CLP = 0

(Example. 8-04) ..... Special routing function 3
User channel, SM = 0 (VCC), CM = 0, output to non-microprocessor connection port, PTI = PTF

Basic setting 1 + following setting (except for EF = 0, IA = 1, VA = 1)
HTT

//LPN#1, VPI = 1, VCI = 20h
01480h CEN = 1, SM = 0,
//LPN#1, VPI = 1, VCI = 22h
01488h CEN = 1, SC = 100 (ABR), SM = 0, CM = 0, SPI = 0_0010 (2), OVPC = 0224h

Input cell: //VC OAM (End-End)/F5 OAM
LPN#3,
VPI = 0000_0000_0001 (001h),
VCI = 0000_1000_0010_0010 (0822h),
PTI = 101
CLP = 0
Output cell:
LPN#2,
VPI = 0000_0000_0010 (002h),
VCI = 0000_0000_0010_0100 (0024h),
PTI = 101
CLP = 0

(Example. 8-05) ..... No function of special routing
User channel, SM = 0 (VCC), CM = 0, output to non-microprocessor connection port, PTI = PTF

Basic setting 7 + following setting (except for EF = 0, IA = 1, VA = 1)
HTT
//LPN#3, VPI = 1, VCI = 20h
03480h CEN = 1, SM = 0,
//LPN#3, VPI = 1, VCI = 22h
03488h CEN = 1, SC = 100 (ABR), SM = 0, CM = 0, SPI = 0_0010 (2), OVPC = 0224h

Input cell: //VC OAM (End-End)/F5 OAM
LPN#3,
VPI = 0000_0000_0001 (001h),
VCI = 0000_0000_0010_0010 (0022h),
PTI = 101
CLP = 0
Output cell:
LPN#2,
VPI = 0000_0000_0010 (002h),
VCI = 0000_0000_0010_0100 (0024h),
PTI = 101
CLP = 0

(Example. 8-06) ..... No function of special routing
User channel, SM = 0 (VCC), CM = 0, output to non-microprocessor connection port, PTI = PTF

Basic setting 1 + following setting (except for EF = 0, IA = 1, VA = 1)
HTT
//LPN#3, VPI = 1, VCI = 20h
03480h CEN = 1, SM = 0,

//LPN#3, VPI = 1, VCI = 22h
03488h CEN = 1, SC = 100 (ABR), SM = 0, CM = 0, SPI = 0_0010 (2), OVPC = 0224h

Input cell: //VP OAM (End-End)/F5 OAM
LPN#3,
VPI = 0000_0000_0001 (001h),
VCI = 0001_1000_0010_0010 (1822h),
PTI = 101
CLP = 0
Output cell:
LPN#2,
VPI = 0000_0000_0010 (002h),
VCI = 0000_0000_0010_0100 (0024h),
PTI = 101
CLP = 0

[MEMO]

★ CHAPTER 7 DIFFERENCE BY STANDARD

7.1 Added Functions

The following functions have been added from the E-standard model of the μPD98412. These functions are not provided with the initially released K-standard model of the μPD98412.

(1) UDF field transmission function
(2) Extension of VP count
(3) Input cell count function in VP/VC units

7.2 Overview of Added Functions

(1) UDF field transmission function

A UDF field transmission function passes the UDF field of an input cell to the UDF field of an output cell as is.
Use of the UDF field transmission function is enabled by the new UP bit that is provided to the MODE0 register.
The UDF field that is passed to the output cell is as shown in the table below, depending on the data width of the UTOPIA I/F.

Rx	Tx	UDF1 of Output Cell	UDF2 of Output Cell
16-bit I/F	16-bit I/F	Passes UDF1 of input cell	Passes UDF2 of input cell
	8-bit I/F	Passes UDF1 of input cell	–
8-bit I/F	16-bit I/F	Passes UDF1 of input cell	FFh
	8-bit I/F	Passes UDF1 of input cell	–

The data width of the cell buffer is extended from 88 bits to 92 bits for the sake of the UDF field transmission function. As a result, the new pins listed in the table below are provided

Pin Name	Pin No.	Function of K-Standard Model
CBD[88]	439	Internally connected signal (IC), open
CBD[89]	349	Internally connected signal (IC), open
CBD[90]	251	Internally connected signal (IC), open
CBD[91]	145	Internally connected signal (IC), open

If the UDF field transmission function is not used, open the newly provided pins. When the UDF field transmission function is not used, the K-standard model and E-standard model are pin-compatible.

(2) Extension of VP count

It is possible to extend the VP count (the maximum valid VPI bit width of an input cell is 13) that can be handled when the header is converted. As a result, the setting range of the NVCI field of the HTn (n = 0 to 29) register is extended from 6h-Fh to 3h-Fh.

As the VP count is extended, the position of HTT that is accessed to identify a switching mode (SM) (with the K-standard model HTT address is calculated by replacing VCI of an input cell with 20h) can be set by using a newly provided Switching Mode Area register.

(3) Input cell count function in VP/VC units

A function to count the input cells in VP/VC units was added to the input cell counter (CTINPn (n = 0 to 3) register). As a result, CCE bit, PC bit, and HTA field have been newly added to the Input Cell Count Enable (CTENINPn (n = 0 to 3)) register.

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