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RENESAS

User's Manual

μPD98411

(NEASCOT-P40™)

ATM Quad SONET Framer

Document No. S12736EJ4V0UM00 (4th edition)
Date Published May 2001 J CP(K)

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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M8E 00.4

Major Revision in This Edition

Page	Description
	Chapter 2, "Pin Function"
General	VDD-PE → VDD-RPE, VDD-TPE, GND-PE → GND-RPE, GND-TPE, CMOS → TTL
p.31	**2.2.8, "Handling Unused Pins"**: TDOT, TDOC, RDIT, and RDIC were added.
p.32	**2.2.9, "Initial States of Each Pin"**: ACK/RDY_B was changed.
	Chapter 3, "Functional Outline"
p.36 to p.40	**3.1, "Transmission Function"**: Descriptions and a remark were added to (2). A remark was added to (3). Descriptions in (10) were changed. A caution was added to (10).
p.47 to p.59	**3.2, "Reception Function"**: (13) was added. Descriptions and cautions were added to (3), "LOS", of Table 3-6. Descriptions were added to Table 3-9.
p.61 to p.64	**3.3.2, "Reception OAM Control"**: Descriptions and cautions 1 to 4 were added to (d) of (3). A caution and remark were added to (e). A remark was added to Table 3-12.
p.66	**3.4, "Frame Overhead Insert/Drop Function"**: (3) was added.
p.67	**3.5.1, PALM[2:0] Output Pins**: <<Examples of using the PALM pin>> was added.
p.68	**3.5.3, "SD Input Pins"**: Descriptions were added.
p.71	**3.8, "Loopback Function"**: Cautions 1 to 4 were added.
	Chapter 4, "Interfaces"
p.74 to p.79	**4.1.2, "Modes"**: A caution was added to Table 4-1. Descriptions in (c) of (2) were changed. Changes were made in Figure 4-2.
p.94	**4.1.3, "Operations"**: Descriptions in (c) of (3) were changed. Changes were made in Figure 4-19.
p.95	**4.1.4, "Supporting the UTOPIA Parity Bit"**: A caution was added to (2).
p.99 to p.101	**4.2.3, "Transmit/Receive Clocks"**: Descriptions in (1) and (2) were changed.
p.105	**4.2.4, "Examples of Connection between μPD98411 and Transceiver"**: A remark was added to Figure 4-24.
p.107	**4.3.2, "Write Operation"**: Cautions 1 and 2 were added.
p.111	**4.4.3, "Interrupt Processing"**: Descriptions were added.
	Chapter 5, "Registers"
p.119, p.120	**5.1.1, "Port Registers"**: Default values were changed.
p.123 to p.155	**5.2.1, "Port Register Function"**: A caution and remark were added to (2). Descriptions were changed in and added to the Function column of the table in (2). Bit names and contents were changed in (5), (13), (33), and (35). Default values were changed in (39) and (40). Register names were added to (62) and (72).
p.165 to p.177	**5.2.2, "Common Register"**: Bit names and contents were changed in (101). Descriptions were added to (103) to (108). Descriptions were changed in the Function column of tables in (109) and (110), and a caution was added to (109) and (110). Descriptions were added to the Function column of a table in (113). A caution was added to (114). Descriptions were changed in the Function column of a table in (116). Register names, bit names, and bit contents were changed in (119).
p.178	**Chapter 6, "JTAG Boundary Scan"**: Cautions were added.
p.190	**6.7.4, "Boundary Scan Data Bit Definition"**: Table 6-2 was deleted.
p.191, p.192	**Chapter 7, "Board Layout"**: VDD-PE → VDD-RPE, VDD-TPE, GND-PE → GND-RPE, GND-TPE in Table 7-1 and Figure 7-1.
p.195	**Chapter 8, "Restrictions"**: The whole chapter was added.

The mark ★ shows major revised points.

PREFACE

Readers This manual is intended for engineers who need to be familiar with the capabilities of the μPD98411 in order to develop application systems based on it.

Purpose The purpose of this manual is to help users understand the hardware capabilities (listed below) of the μPD98411.

Configuration This manual consists of the following chapters:

- General
- Pin function
- Functional outline
- Interfaces
- Registers
- JTAG boundary scan
- Board layout
- Restrictions

Guidance Readers of this manual should already have a general knowledge of electronics, logic circuits, and microcomputers.

To gain an overall understanding of the functions of the μPD98411:
→ Read through all the chapters, in sequence.

To check the electrical characteristics of the μPD98411:
→ Refer to the separate data sheet.

Some restrictions apply to the μPD98411. Be sure to read **Chapter 8**.

Notation This manual uses the following conventions:

Data bit significance:	High-order bits on the left side; low-order bits on the right side	
Active low:	××××_B (Pin and signal names are suffixed with _B.)	
Note:	Explanation of an indicated part of text	
Caution:	Information requiring the user's special attention	
Remark:	Supplementary information	
Numeric value:	Binary:	×××× or ××××B
	Decimal:	××××
	Hexadecimal:	××××H

Related documents Some documents may be preliminary editions, but are not indicated as such in this manual.

- μPD98411 Data Sheet: S12953E

CONTENTS

LIST OF FIGURES (1/2)

LIST OF FIGURES (2/2)

LIST OF TABLES

The μPD98411 (NEASCOT-P40) is one of ATM-LAN LSIs and provides the functions of the TC sublayer of the SONET/SDH-base physical layer of the ATM protocol specified by the ATM Forum. Its main functions include a transmission function for mapping an ATM cell passed from a high-end ATM switch device or SAR device to the payload of a 155-Mbps SONET STS-3c/SDH STM-1 frame and transmitting the cell to a transceiver at the line side, and a reception function for separating the overhead and ATM cell from the data string received from a receiver and transmitting the ATM cell to the ATM layer. The μPD98411 combines these transmission/reception functions into a port function that is realized as a single four-port LSI chip. This LSI is ideally suited for use in the ATM hubs, ATM switches, and other equipment used to configure an ATM network.

In addition, the μPD98411 also has a clock recovery function for each port to extract a synchronous clock for reception of receive data from the bit stream, and a clock synthesis function to generate a clock for transmission.

1.1 Features

- Incorporates an ATM user network interface TC sublayer function for four channels.
- Conforms to ATM FORUM UNI v3.1.
- Incorporates four clock recovery PLLs and one clock synthesizer PLL.
- ATM layer interface conforms to ATM FORUM UTOPIA Level 2 v1.0.
  - Can be selected from the multi-PHY interface (up to 800 Mbps) in several different modes.

Single 16-bit	1TCLAV/1RCLAV (Cell Available) signal mode
Single 8-bit	Direct Status Indication mode
Dual 8-bit	Multiplexed Status Polling mode

  - A CPU interface can be set to either of two modes.

RD-WR-RDY style (Intel-compatible mode)
DS-R/W-ACK style (Motorola-compatible mode)

- The line-side PMD interface accepts a P-ECL level input.
- Supports a loopback function.
- Supports a pseudo error generation frame transmission function.
- Incorporates one general input port per channel and three output ports (each able to drive an LED) per channel.
- Supports JTAG boundary scan test (IEEE 1149.1).

- Incorporates a wide range of operation, administration, and maintenance (OAM) functions.

  - Transmission

Alarm and Failure Detection	Line Quality Monitoring
APS	Insertion of B1-byte computation
Line AIS/Path AIS	Insertion of B2-byte computation
Line RDI/Path RDI	Insertion of B3-byte computation
	Automatic transmission of a Line REI
	Automatic transmission of a Path REI

  - Reception

Alarm and Failure Detection	Notification of Degraded Line Quality	Line Quality Monitor Counter (24-Bit)
External input signal change	B1 error	B1 error counter
LOS	B2 error	B2 error counter
OOF	B3 error	B3 error counter
LOF	Line REI	Line REI counter
LOP	Path REI	Path REI counter
OCD	Frequency justification	Frequency justification counter
LCD	FIFO overflow	HEC processing dropped cell counter
Line AIS/Path AIS		FIFO overflow dropped cell counter
Line RDI/Path RDI		Received idle cell counter
APS		Valid cell counter

- 0.35-μm CMOS process
- Low power consumption; +3.3 V single-voltage power supply

1.2 Ordering Information

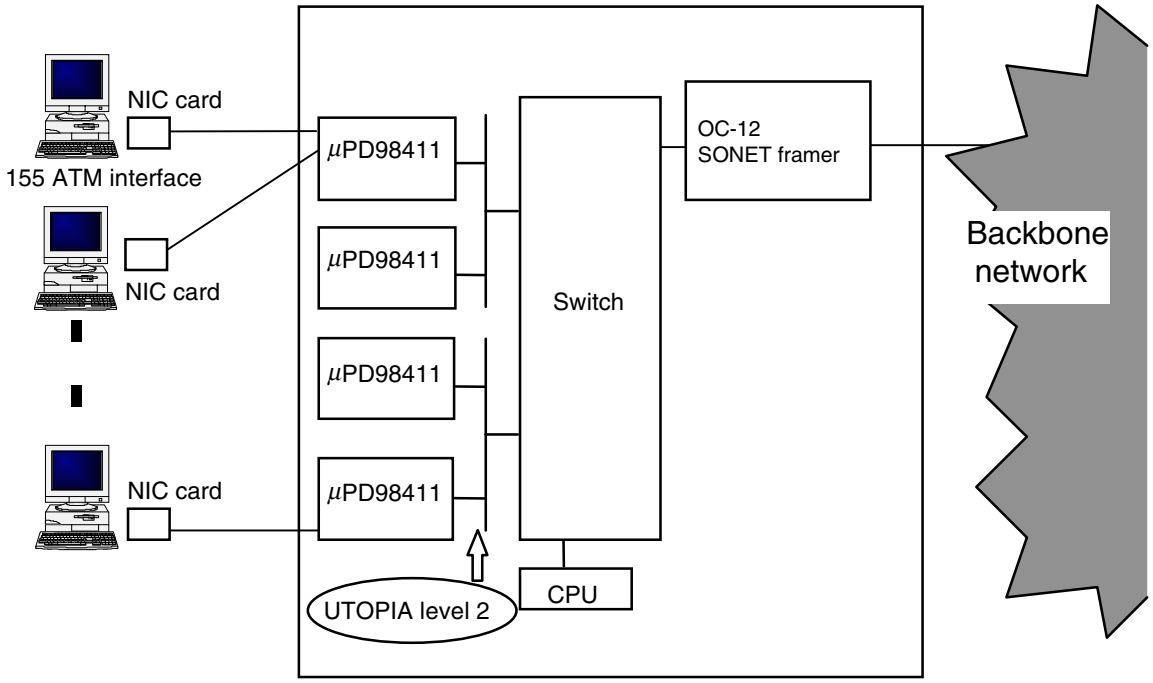
Part Number	Package
μPD98411GN-MMU	240-pin plastic QFP (fine pitch) (32 $\times$ 32 mm)

1.3 System

1.3.1 Application

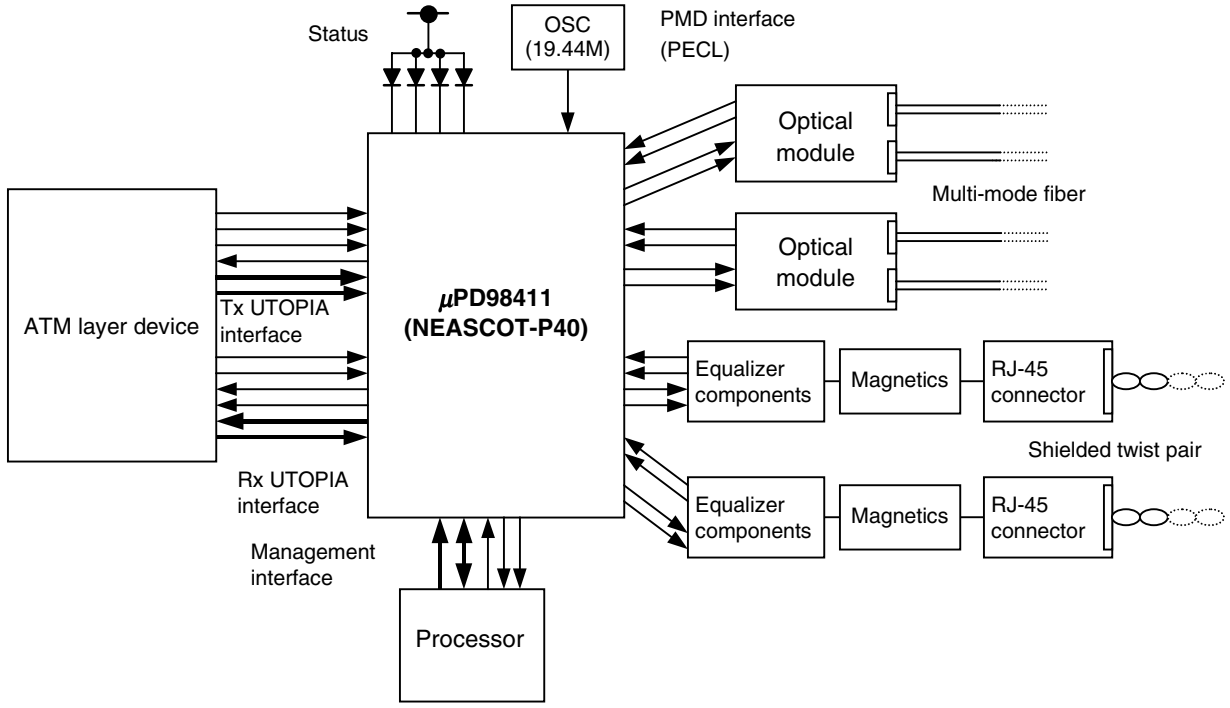
An example of a system configuration including μPD98411 chips is shown below.

Example: ATM switch



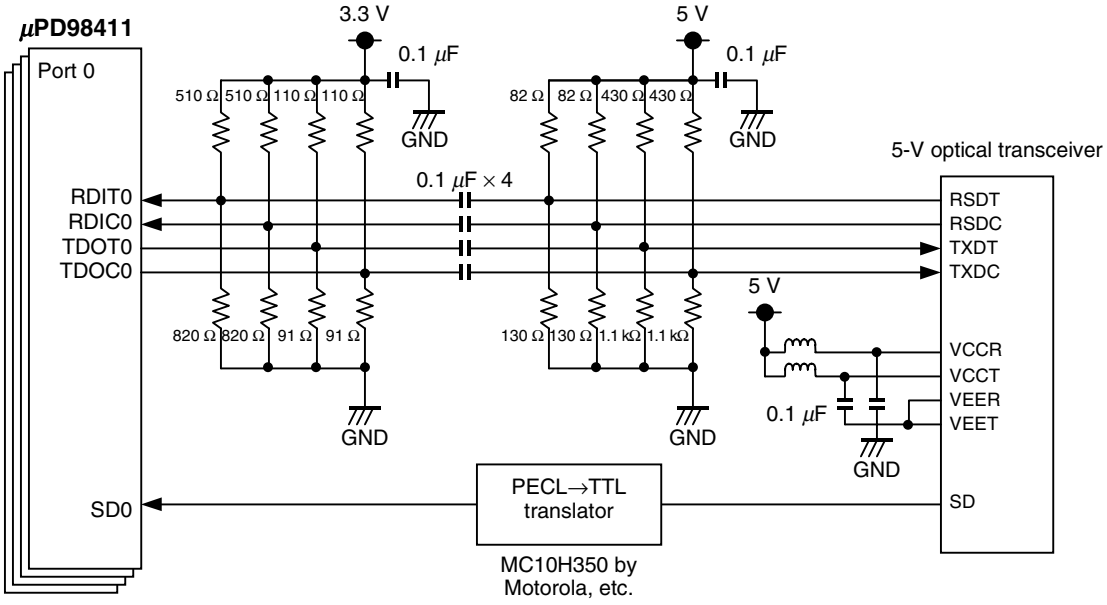
1.3.2 System Configuration

(1) μPD98411 peripherals

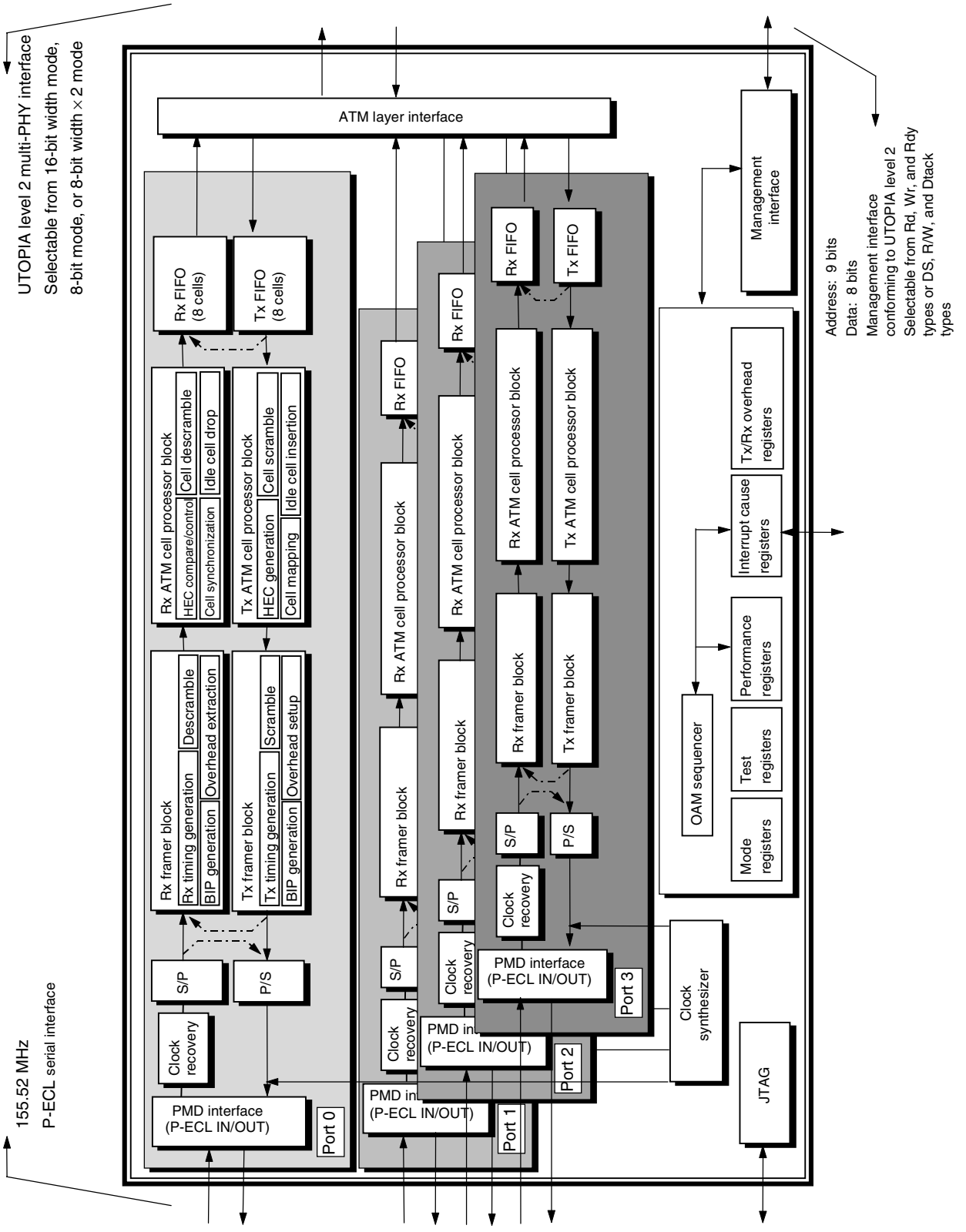


(2) Example of connection to 5-V transceiver

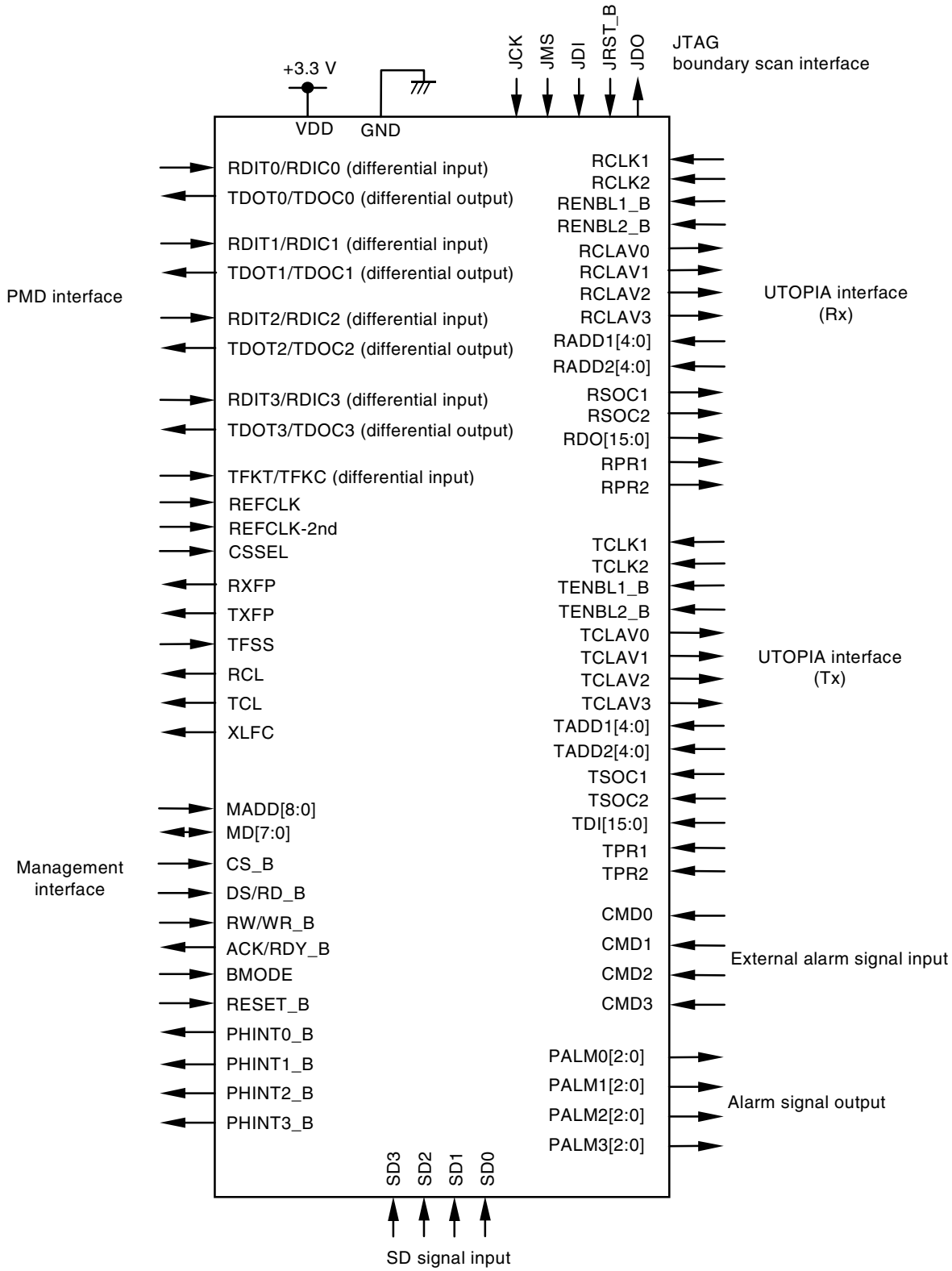
An example of connecting the μPD98411 to a 5-V optical transceiver is shown below. Because the μPD98411 operates on 3.3 V, use an AC coupling circuit to connect it to a 5-V device.



1.4 Block Diagram

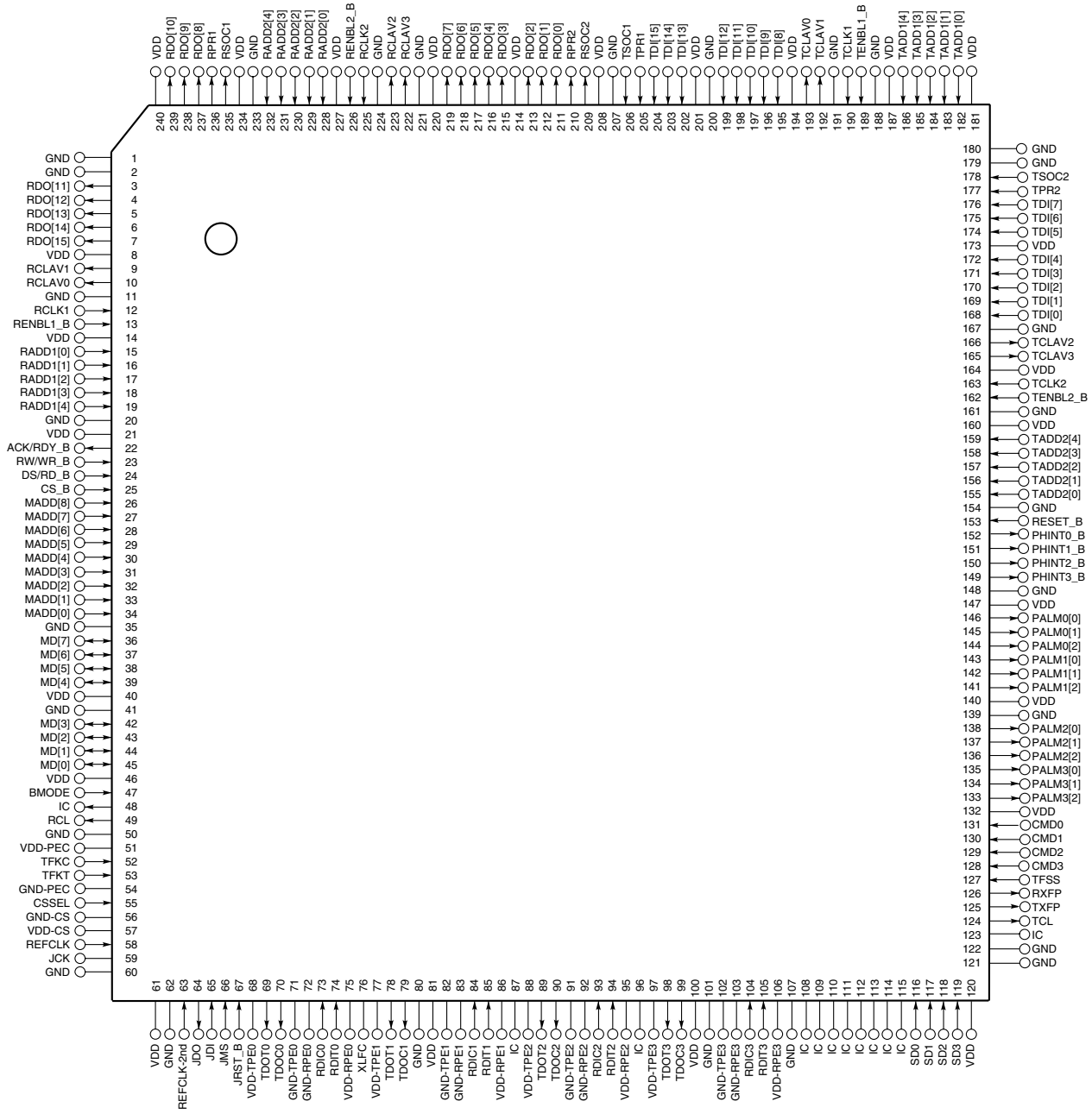


1.5 Pin Configuration



★ 2.1 Pin Configuration

- 240-pin plastic QFP (fine pitch) (32 × 32 mm)
  μPD98411GN-MMU



Remark IC: Internal connection pin. Leave the IC pins open.

Pin Arrangement Table

(1/2)

No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
1	GND	37	MD[6]	73	RDIC0	109	IC
2	GND	38	MD[5]	74	RDIT0	110	IC
3	RDO[11]	39	MD[4]	75	VDD-RPE0★	111	IC
4	RDO[12]	40	VDD	76	XLFC	112	IC
5	RDO[13]	41	GND	77	VDD-TPE1★	113	IC
6	RDO[14]	42	MD[3]	78	TDOT1	114	IC
7	RDO[15]	43	MD[2]	79	TDOC1	115	IC
8	VDD	44	MD[1]	80	GND	116	SD0
9	RCLAV1	45	MD[0]	81	VDD	117	SD1
10	RCLAV0	46	VDD	82	GND-TPE1★	118	SD2
11	GND	47	BMODE	83	GND-RPE1★	119	SD3
12	RCLK1	48	IC	84	RDIC1	120	VDD
13	RENBL1_B	49	RCL	85	RDIT1	121	GND
14	VDD	50	GND	86	VDD-RPE1★	122	GND
15	RADD1[0]	51	VDD-PEC	87	IC	123	IC
16	RADD1[1]	52	TFKC	88	VDD-TPE2★	124	TCL
17	RADD1[2]	53	TFKT	89	TDOT2	125	TXFP
18	RADD1[3]	54	GND-PEC	90	TDOC2	126	RXFP
19	RADD1[4]	55	CSSEL	91	GND-TPE2★	127	TFSS
20	GND	56	GND-CS	92	GND-RPE2★	128	CMD3
21	VDD	57	VDD-CS	93	RDIC2	129	CMD2
22	ACK/RDY_B	58	REFCLK	94	RDIT2	130	CMD1
23	RW/WR_B	59	JCK	95	VDD-RPE2★	131	CMD0
24	DS/RD_B	60	GND	96	IC	132	VDD
25	CS_B	61	VDD	97	VDD-TPE3★	133	PALM3[2]
26	MADD[8]	62	GND	98	TDOT3	134	PALM3[1]
27	MADD[7]	63	REFCLK-2nd	99	TDOC3	135	PALM3[0]
28	MADD[6]	64	JDO	100	VDD	136	PALM2[2]
29	MADD[5]	65	JDI	101	GND	137	PALM2[1]
30	MADD[4]	66	JMS	102	GND-TPE3★	138	PALM2[0]
31	MADD[3]	67	JRST_B	103	GND-RPE3★	139	GND
32	MADD[2]	68	VDD-TPE0★	104	RDIC3	140	VDD
33	MADD[1]	69	TDOT0	105	RDIT3	141	PALM1[2]
34	MADD[0]	70	TDOC0	106	VDD-RPE3★	142	PALM1[1]
35	GND	71	GND-TPE0★	107	GND	143	PALM1[0]
36	MD[7]	72	GND-RPE0★	108	IC	144	PALM0[2]

(2/2)

No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
145	PALM0[1]	170	TDI[2]	195	TDI[8]	220	VDD
146	PALM0[0]	171	TDI[3]	196	TDI[9]	221	GND
147	VDD	172	TDI[4]	197	TDI[10]	222	RCLAV3
148	GND	173	VDD	198	TDI[11]	223	RCLAV2
149	PHINT3_B	174	TDI[5]	199	TDI[12]	224	GND
150	PHINT2_B	175	TDI[6]	200	GND	225	RCLK2
151	PHINT1_B	176	TDI[7]	201	VDD	226	RENBL2_B
152	PHINT0_B	177	TPR2	202	TDI[13]	227	VDD
153	RESET_B	178	TSOC2	203	TDI[14]	228	RADD2[0]
154	GND	179	GND	204	TDI[15]	229	RADD2[1]
155	TADD2[0]	180	GND	205	TPR1	230	RADD2[2]
156	TADD2[1]	181	VDD	206	TSOC1	231	RADD2[3]
157	TADD2[2]	182	TADD1[0]	207	GND	232	RADD2[4]
158	TADD2[3]	183	TADD1[1]	208	VDD	233	GND
159	TADD2[4]	184	TADD1[2]	209	RSOC2	234	VDD
160	VDD	185	TADD1[3]	210	RPR2	235	RSOC1
161	GND	186	TADD1[4]	211	RDO[0]	236	RPR1
162	TENBL2_B	187	VDD	212	RDO[1]	237	RDO[8]
163	TCLK2	188	GND	213	RDO[2]	238	RDO[9]
164	VDD	189	TENBL1_B	214	VDD	239	RDO[10]
165	TCLAV3	190	TCLK1	215	RDO[3]	240	VDD
166	TCLAV2	191	GND	216	RDO[4]		
167	GND	192	TCLAV1	217	RDO[5]		
168	TDI[0]	193	TCLAV0	218	RDO[6]		
169	TDI[1]	194	VDD	219	RDO[7]		

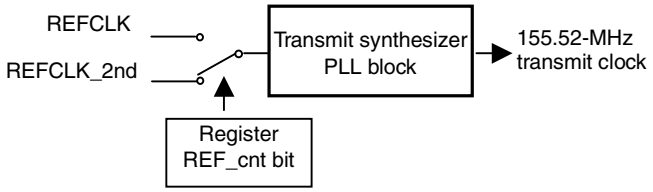
Pin Name

ACK/RDY_B : Acknowledge/Ready
BMODE : Bus Mode
CMD3-CMD0 : Command Signal
CS_B : Chip Select
CSSEL : Clock Source Select
DS/RD_B : Data Strobe/Read
GND : Ground
GND-CS : Ground for Analog PLL Block
GND-PEC : Ground for TFKT/TFKC PECL Block
GND-RPE3-GND-RPE0★ : Ground for Rx PECL Block
GND-TPE3-GND-TPE0★ : Ground for Tx PECL Block
JCK : JTAG Clock
JDI : JTAG Data Input
JDO : JTAG Data Output
JMS : JTAG Mode Select
JRST_B : JTAG Reset
MADD[8:0] : Management Interface Address Bus
MD[7:0] : Management Interface Data Bus
PALM3[2:0], PALM2[2:0], PALM1[2:0], PALM0[2:0] : Physical Alarm Output Signals
PHINT3_B-PHINT0_B : Physical Interrupt
RADD2[4:0], RADD1[4:0] : Receive Address
RCL : Internal Receive System Clock
RCLAV3-RCLAV0 : Receive Cell Available Signals
RCLK2, RCLK1 : Receive Data Transferring Clock
RDIC3-RDIC0 : Receive Data Input Complement
RDIT3-RDIT0 : Receive Data Input True
RDO[15:0] : Receive Data Output
REFCLK : System Clock
REFCLK-2nd : 2nd Reference Clock
RENBL2_B, RENBL1_B : Receive Data Enable
RESET_B : System Reset
RPR2, RPR1 : Receive Data Path Parity
RSOC2, RSOC1 : Receive Start Of Cell
RW/WR_B : Management Interface Read/Write
RXFP : Receive Frame Pulse
SD3-SD0 : Signal Detect
TADD2[4:0], TADD1[4:0] : Transmit Address
TCL : Internal Transmit System Clock
TCLAV3-TCLAV0 : Transmit Cell Available Signals
TCLK2, TCLK1 : Transmit Data transferring Clock
TDI[15:0] : Transmit Data Input from the ATM Layer
TDOC3-TDOC0 : Transmit Data Output Complement
TDOT3-TDOT0 : Transmit Data Output True
TENBL2_B, TENBL1_B : Transmit Data Enable
TFKC : Transmit Reference Clock Complement
TFKT : Transmit Reference Clock True
TFSS : Transmit Frame Set Signal
TPR2, TPR1 : Transmit Data Path Parity
TSOC2, TSOC1 : Transmit Start Of Cell
TXFP : Transmit Frame Pulse
VDD : Supply Voltage
VDD-CS : Supply Voltage for Analog PLL Block
VDD-PEC : Supply Voltage for TFKT/TFKC PECL Block
VDD-RPE3-VDD-RPE0★ : Supply Voltage for Rx PECL Block
VDD-TPE3-VDD-TPE0★ : Supply Voltage for Tx PECL Block
XLFC : Tx Loop Filter Capacity

2.2 Pin Function

2.2.1 PMD Interface

(1/2)

Pin Name	Pin No.	I/O Level	I/O	Function
RDIT3-RDIT0	105, 94, 85, 74	P-ECL True (+)	I	Receive serial data input. Refers to the differential input of the P-ECL level.
RDIC3-RDIC0	104, 93, 84, 73	P-ECL Complement (–)	I	
TDOT3-TDOT0	98, 89, 78, 69	P-ECL True (+)	O	Transmit serial data output. Refers to the differential output of the P-ECL level.
TDOC3-TDOC0	99, 90, 79, 70	P-ECL Complement (–)	O	
SD3-SD0	119-116	TTL★	I	Line signal detection signal input. Refers to the pins for inputting the SD (Signal Detect) signal of line transceivers (such as optical modules). If this signal goes low, this port detects LOS. High: Normal Low: LOS state
★ REFCLK	58	TTL★	I	System clock (19.44 MHz) input. Used as the reference clock for the internal synthesizer PLL/clock recovery PLL and the system clock for register operations.
★ REFCLK-2nd	63	TTL★	I	Second-reference clock (19.44 MHz) input. This pin is used to input the second reference clock for the internal synthesizer PLL. It is not used unless reference clock switching is needed. The CSSC register (at address 076H) specifies which of REFCLK and REFCLK-2nd clocks to use as the reference clock. The REFCLK input is selected by default. Even when REFCLK-2nd is used as the reference clock for the synthesizer PLL, REFCLK is used for register operation as well; therefore, the clock need be input. 
RXFP	126	TTL★	O	Receive frame pulse output (8 kHz). The pulse signal is output synchronously with the start of the receiving frame. The pulse signal is one cycle of the RCL clock in length. The internal FPMSK register (at address 07CH) is used to select which of the four ports will output the pulse synchronous to the receiving frame. No port is selected by default, so no pulse is output from the pin.
XLFC	76	Analog	O	Loop filter capacity connection pin. Refers to the pin connecting the loop filter of the synthesizer PLL. Leave this pin open.

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Pin Name	Pin No.	I/O Level	I/O	Function
TXFP	125	TTL★	O	Transmitting end frame pulse signal output (8 kHz). Outputs a pulse signal synchronous with the start of the transmission frame and equivalent to the one cycle of the TCL clock in length. The setting of the internal FPMSK register (at address 07CH) selects which of the four ports should output the pulse synchronous with the transmitting frame. No port is selected by default, so no pulse is output from the pin.
TFSS	127	TTL★	I	Frame transmission disable signal input. If a high level is input to this pin, the output data strings of all ports are fixed to either to 0 or 1 and frame transmission stops. If a low level is input, transmission begins at the start of the frame (1st A1 byte) in about 9 TCL clock cycles.
RCL	49	TTL★	O	Receive system clock output (19.44 MHz). Each port uses the 155.52-MHz receive clock divided by eight for internal receive processing; and this pin outputs this clock. Which port's system clock is output is selected by setting the relevant value of the RCMSK register (at address 07BH). By using the default value, the clock of port 0 is selected. During resetting or when no port is selected, Low is output. This pin can be used also to output the REFCLK_2nd clock. **Note** When the pin is used to output a clock generated by dividing the receive clock by eight, a spike may output from the pin if the receive clock changes as the condition of the receive line changes.
TCL	124	TTL★	O	Transmission system clock output (19.44 MHz). Each port uses the 155.52-MHz transmit clock divided by eight for internal transmission processing; and this pin outputs this clock. Which port's system clock is output is selected by setting the relevant value of the TCMSK register (at address 07AH). During resetting or when no port is selected, Low is output.
TFKT	53	P-ECL True (+)	I	Externally generated 155.52-MHz transmit clock input. Refers to the pin for inputting the externally generated transmit clock (155.52 MHz) when not using the internally mounted synthesizer PLL. This pin is enabled by setting the CSSEL pin to High.
TFKC	52	P-ECL Complement (–)	I	
CSSEL	55	TTL★	I	TFKT/TFKC pin enable signal input. This pin inputs the enable signal of the TFKT/TFKC pin when inputting a 155.52-MHz clock from outside the chip at the TFKT/TFKC pin. High: TFKT/TFKC pin enable Low: TFKT/TFKC pin disable

2.2.2 UTOPIA Interface

The pin used for each UTOPIA interface signal varies with the mode selected by the internal MltUT register (at address 079H). For details, see **Section 4.1**.

(1/3)

Pin Name	Pin No.	I/O Level	I/O	Function
RDO[15:11] RDO[10:8] RDO[7:3] RDO[2:0]	7-3 239-237 219-215 213-211	TTL★	O (tristate)	Receive data buses. These pins form a 16-bit data bus, used for outputting reception data to the ATM layer device. Data output is synchronized with the rising edge of the RCLK clock pulse. The pins used vary with the UTOPIA interface mode selected using the MltUT register (at address 079H). • Single 8-bit bus: RDO[7:0] • Single 16-bit bus: RDO[15:0] • Dual 8-bit bus: RDO[15:8]/RDO[7:0]
RCLK2 RCLK1	225 12	TTL★	I	Receive clock input. These pins input receive data transfer clocks. A clock pulse having a frequency of up to 50 MHz can be input. The pin used varies with the UTOPIA interface mode selected using the MltUT register (at address 079H). • Single 8-bit bus: RCLK2 • Single 16-bit bus: RCLK1 • Dual 8-bit bus: RCLK1/RCLK2
RSOC2 RSOC1	209 235	TTL★	O (tristate)	Receive cell starting location signal output. This signal indicates the first byte position of a reception cell to the ATM layer device. The pin used varies with the UTOPIA interface mode selected using the MltUT register (at address 079H). • Single 8-bit bus: RSOC2 • Single 16-bit bus: RSOC2 • Dual 8-bit bus: RSOC1/RSOC2
RENBL2_B RENBL1_B	226 13	TTL★	I	Receive enable signal input. This signal indicates that the ATM layer device is ready to receive data. The pin used varies with the UTOPIA interface mode selected using the MltUT register (at address 079H). • Single 8-bit bus: RENBL2_B • Single 16-bit bus: RENBL1_B • Dual 8-bit bus: RENBL1_B/RENBL2_B
RCLAV3 RCLAV2 RCLAV1 RCLAV0	222 223 9 10	TTL★	O (tristate)	Receive cell transferable report signal output. This signal informs the ATM layer device that 1 cell or more of data exists in the receive FIFO. In 1TCLAV&1RCLAV mode, the RCLAV signal of each port is internally multiplexed to be output as a signal. Of the four signals of RCLAV0 to RCLAV3, the signal used varies depending on the UTOPIA interface mode selected by the MltUT register (at address 079H). • Single 8-bit bus: RCLAV2 • Single 16-bit bus: RCLAV1 • Dual 8-bit bus: RCLAV1/RCLAV2 In Direct Status Indication (DSI) mode and Multiplexed Status Polling (MSP) mode, the four signals of RCLAV0 to RCLAV3 are allocated to each of the ports to identify their FIFO statuses. RCLAV0 corresponds to port 0, and RCLAV3 to port 3.

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Pin Name	Pin No.	I/O Level	I/O	Function
RADD2[4:0] RADD1[4:0]	232-228 19-15	TTL★	I	Receiving end PHY address input. The address is used to select each port. The pins used vary with the UTOPIA interface mode, selected using the MltUT register (at address 079H). • Single 8-bit bus: RADD2[4:0] • Single 16-bit bus: RADD1[4:0] • Dual 8-bit bus: RADD1[4:0]/RADD2[4:0]
RPR2 RPR1	210 236	TTL★	O	Parity bit output pins. Odd parity bits are generated and output from these pins with respect to the data output from RDO[15]-RDO[0]. The pin used varies with the UTOPIA interface mode, selected using the MltUT register (at address 079H). • Single 8-bit bus: RPR2 • Single 16-bit bus: RPR2 • Dual 8-bit bus: RPR1/RPR2
TDI[15:13] TDI[12:8] TDI[7:5] TDI[4:0]	204-202 199-195 176-174 172-168	TTL★	I	Transmit data buses. These data buses input transmit data from the ATM layer device at the rising edge of the TCLK clock. The pins used vary with the UTOPIA interface mode, selected using the MltUT register (at address 079H). • Single 8-bit bus: TDI[15:8] • Single 16-bit bus: TDI[15:0] • Dual 8-bit bus: TDI[15:8]/TDI[7:0]
TCLK2 TCLK1	163 190	TTL★	I	Transmit clock input. These pins input clocks of up to 50 MHz for transmit data transfer. The pin used varies with the UTOPIA interface mode, selected using the MltUT register (at address 079H). • Single 8-bit bus: TCLK1 • Single 16-bit bus: TCLK2 • Dual 8-bit bus: TCLK1/TCLK2
TSOC2 TSOC1	178 206	TTL★	I	Transmit cell starting location signal input. These pins input a signal which indicates the location of the first byte of the transmit cell. The pin used varies with the UTOPIA interface mode, selected using the MltUT register (at address 079H). • Single 8-bit bus: TSOC1 • Single 16-bit bus: TSOC1 • Dual 8-bit bus: TSOC1/TSOC2
TENBL2_B TENBL1_B	162 189	TTL★	I	Transmit enable signal input. This signal indicates that the ATM layer device is outputting valid transmission data to TDI[15] to TDI[0]. The pin used varies with the UTOPIA interface mode, selected using the MltUT register (at address 079H). • Single 8-bit bus: TENBL1_B • Single 16-bit bus: TENBL2_B • Dual 8-bit bus: TENBL1_B/TENBL2_B

(3/3)

Pin Name	Pin No.	I/O Level	I/O	Function
TCLAV3 TCLAV2 TCLAV1 TCLAV0	165 166 192 193	TTL★	O (tristate)	Transmit cell acceptable report signal output. The signal informs the ATM layer device that unused storage space of at least one cell is available in the transmit FIFO. In 1TCLAV&1RCLAV mode, the TCLAV signal of each port is internally multiplexed to be output as a signal. Of the four signals of TCLAV0 to TCLAV3, the signal used varies depending on the UTOPIA interface mode selected by the MltUT register (at address 079H). • Single 8-bit bus: TCLAV1 • Single 16-bit bus: TCLAV2 • Dual 8-bit bus: TCLAV1/TCLAV2 In Direct Status Indication (DSI) mode and Multiplexed Status Polling (MSP) mode, the four pins TCLAV0 to TCLAV3 are allocated to each of the ports signal by signal, and indicate the FIFO statuses of each port. TCLAV0 corresponds to port 0; and TCLAV3 to port 3.
TADD2[4:0] TADD1[4:0]	159-155 186-182	TTL★	I	Transmission PHY address input. The address is used to select a port. The pins used vary with the UTOPIA interface mode, selected using the MltUT register (at address 079H). • Single 8-bit bus: TADD1[4:0] • Single 16-bit bus: TADD2[4:0] • Dual 8-bit bus: TADD1[4:0]/TADD2[4:0]
TPR2 TPR1	177 205	TTL★	I	Parity bit input pins. These pins input the odd parity bit input from TDO[15]-TDO[0]. The pin used varies with the UTOPIA interface mode, selected using the MltUT register (at address 079H). • Single 8-bit bus: TPR1 • Single 16-bit bus: TPR1 • Dual 8-bit bus: TPR1/TPR2

2.2.3 Management Interface

Pin Name	Pin No.	I/O Level	I/O	Function
BMODE	47	TTL★	I	Mode selection input. This pin selects the mode of the management interface. BMODE = 1 : Selects <RD_B, WR_B, RDY_B> as pin function. BMODE = 0 : Selects <DS_B, R/W_B, ACK_B> as pin function.
MADD[8:0]	26-34	TTL★	I	Address input. These pins form a nine-bit address that inputs the addresses of the internal registers.
MD[7:4] MD[3:0]	36-39 42-45	TTL★	I/O (tristate)	8-bit data buses. This data bus reads or writes the data of the internal registers.
CS_B	25	TTL★	I	Chip select signal input. When this pin goes low, access to the internal registers is enabled.
DS/RD_B	24	TTL★	I	Data strobe signal input or read signal input. The function of this pin differs depending on the management interface mode selected by the signal input to the BMODE pin. BMODE = 0 : Functions as data strobe signal DS_B BMODE = 1 : Function as RD_B selecting the read access
RW/WR_B	23	TTL★	I	Read/write signal input or write signal input. The function of this pin differs depending on the management interface mode selected by the signal input to the BMODE pin. When BMODE = 0, this pin functions as read/write control signal R/W_B, as follows: R/W_B = High : Read cycle R/W_B = Low : Write cycle When BMODE = 1, this pin functions as WR_B that selects write access to the internal registers.
ACK/RDY_B	22	TTL★	O (tristate)	Data acknowledge signal output or ready signal output. This pin outputs an acknowledge or ready signal that accepts a cycle to read/write the internal registers.
PHINT3_B- PHINT0_B	149-152	TTL★	O	Interrupt signal output. These signals inform the host that an interrupt factor has occurred. Two modes are available for this purpose: one which indicates an interrupt factor for four ports using the PHINT0_B signal and the other which uses four pins PHINT0_B-PHINT3_B to indicate an individual interrupt for each port. Port 0 corresponds to the PHINT0_B pin; and port 3 to PHINT3_B.
RESET_B	153	TTL★	I	System reset signal input pin. Initializes the μPD98411. Input a low-level pulse at least 1 μs wide. Particularly on power application, this pulse width must be maintained after the level of the supply voltage has reached 90% of the rated value. When the RESET_B signal is input, the clock must be input to the REFCLK pin.

2.2.4 Alarm Signal Input/Output

Pin Name	Pin No.	I/O Level	I/O	Function
CMD3-CMD0	128-131	TTL★	I	General-purpose input signal. Refers to the general-purpose input pins which input the state signals, etc. from external peripheral devices. The signal level of these pins can also be reflected in the state bits of internal registers, and changes in these bits can be used identify interrupt factors. These bits correspond to the ports on a one-to-one basis. CMD0 corresponds to port 0, while CMD3 corresponds to port 3.
PALM3[2:0] PALM2[2:0] PALM1[2:0] PALM0[2:0]	133-135 136-138 141-143 144-146	TTL★	O	Pins for outputting PHY layer alarm detection signals. These pins output a state indicating that a port detected an alarm or failure (LOS, OOF, LOF, LOP, OCD, LCD, Line AIS, Path AIS, Line RDI, Path RDI) or that the input level of the CMD pin has changed. These pins are also used as a general-purpose output port to reflect the bit state of an internal register. The output state is selected by using the AMPR, AMPR1, and AMPR2 registers.

2.2.5 JTAG Boundary Scan

Pin Name	Pin No.	I/O Level	I/O	Function
JDI	65	TTL★	I	Boundary scan data input. Ground this pin when not used.
JDO	64	TTL★	O (tristate)	Boundary scan data output. Open this pin when not used.
JCK	59	TTL★	I	Boundary scan clock input. Ground this pin when not used.
JMS	66	TTL★	I	Boundary scan mode select signal input. Ground this pin when not used.
JRST_B	67	TTL★	I	Boundary scan reset signal input. Ground this pin when not used.

★ **Remark** About the treatment of JTAG boundary scan pins for normal operation

A pulse input to the RESET_B pin does not reset the JTAG logic.

If the JTAG logic has not been reset, the μPD98411 may not operate normally. Either of the following two methods can be used to reset the JTAG logic. If the JRST_B pin is not connected to a ground, be sure to reset the JTAG logic, using either method, after the power is switched on.

- Resetting the JTAG logic without using the JRST_B pin
  Use the JMS and JCK pins to reset the JTAG logic and keep it reset (with the JRST_B pin pulled up).
  Fix the JMS pin at 1 (pulled up), and input five or more clock cycles to the JCK pin.

- Using the JRST_B pin to reset the JTAG logic
  If a low pulse having the same width as RESET_B of the μPD98411 is input to the JRST_B pin, and the JMS and JRST_B pins are pulled up and kept at a high level, the JTAG logic is kept reset, so it does not affect normal operations. As for the JDI and JCK pins, keep the input level pulled down or up.

2.2.6 Power and Grounding Pins

Pin Name	Pin No.	I/O	Function
VDD	8, 14, 21, 40, 46, 61, 81, 100, 120, 132, 140, 147, 160, 164, 173, 181, 187, 194, 201, 208, 214, 220, 227, 234, 240	-	Low-speed section logic power supply (+3.3 V ±5%) and ground.
GND	1, 2, 11, 20, 35, 41, 50, 60, 62, 80, 101, 107, 121, 122, 139, 148, 154, 161, 167, 179, 180, 188, 191, 200, 207, 221, 224, 233	-	
VDD-PEC	51	-	TFKT/TFKC input high-speed section power supply (+3.3 V ±5%) and ground. Noise from this power supply affects the jitter characteristic. Eliminate noise through countermeasures such as filters.
GND-PEC	54	-	
VDD-CS	57	-	Transmit clock synthesizer PLL power supply (+3.3 V ±5%) and ground. Noise from this power supply affects the jitter characteristic. Eliminate noise through countermeasures such as filters.
GND-CS	56	-	
★ VDD-TPE3 VDD-TPE2 VDD-TPE1 VDD-TPE0	97 88 77 68	-	The serial-to-parallel conversion section of each port, transmit P-ECL buffer power supply (+3.3 V ±5%), and ground. Noise from this power supply affects the jitter characteristic. Eliminate noise through countermeasures such as filters.
★ GND-TPE3 GND-TPE2 GND-TPE1 GND-TPE0	102 91 82 71	-	
★ VDD-RPE3 VDD-RPE2 VDD-RPE1 VDD-RPE0	106 95 86 75	-	The receive clock recovery section of each port, receive P-ECL buffer power supply (+3.3 V ±5%), and ground. Noise from this power supply affects the jitter characteristic. Eliminate noise through countermeasures such as filters.
★ GND-RPE3 GND-RPE2 GND-RPE1 GND-RPE0	103 92 83 72	-	

2.2.7 Others

Pin Name	Pin No.	I/O Level	I/O	Function
IC	48, 87, 96, 108-115, 123	CMOS	-	Internal circuit connection test pins. These pins must be kept open.

2.2.8 Handling Unused Pins

Depending on the mode, some pins are not used. These pins must be handled as listed below.

Pin Name	Handling
RCLK2, RCLK1 RENBL2_B, RENBL1_B RADD2[4:0], RADD1[4:0] TDI[15:0] TCLK2, TCLK1 TSOC2, TSOC1 TENBL2_B, TENBL1_B TADD2[4:0], TADD1[4:0] TPR2, TPR1	Ground.
RDO[15:0] RSOC2, RSOC1 RPR2, RPR1 RCLAV3-RCLAV0 TCLAV3-TCLAV0 ★ TDOT, TDOC	Leave open.
CMD3-CMD0	Ground.
SD3-SD0	Pull up.
TFKT, TFKC ★ RDIT, RDIC	Pull up the TFKT and RDIT pins. Ground the TFKC and RDIC pins.
TFSS	Ground.
XLFC	Leave open.
REFCLK-2nd	Ground.
★ Output pins other than the above	Leave open.

2.2.9 Initial States of Each Pin

Pin Name	During a Reset	After a Reset
RDO[15:0] RSOC2, RSOC1 RCLAV3-RCLAV0 TCLAV3-TCLAV0 RPR2, RPR1	Hi-Z	Hi-Z
PHINT3_B-PHINT0_B	H	H
PALM3[2:0]-PALM0[2:0]	L	L
RXFP	L	L
TXFP	L	L
TCL	L	L
RCL	L	L
MD[7:0]	Hi-Z	Hi-Z
★ ACK/RDY_B	Hi-Z	Hi-Z
TDOT3-TDOT0	L	L
TDOC3-TDOC0	H	H

The μPD98411 is an LSI integrating, on a single chip, four framer ports that implement the function of the TC sublayer in a SONET/SDH-based physical layer of the ATM protocol. The major functions are to insert an ATM cell received from the ATM layer into a 155-Mbps SONET STS-3c/SDH STM-1 frame and output the cell to the line, or to receive the ATM cell from a receive SONET/SDH frame and output the cell to the ATM layer. The mode of the μPD98411 is set, commands are issued to the μPD98411, and its status registers are polled via the management interface.

Figure 3-1. μPD98411 and Peripheral Blocks

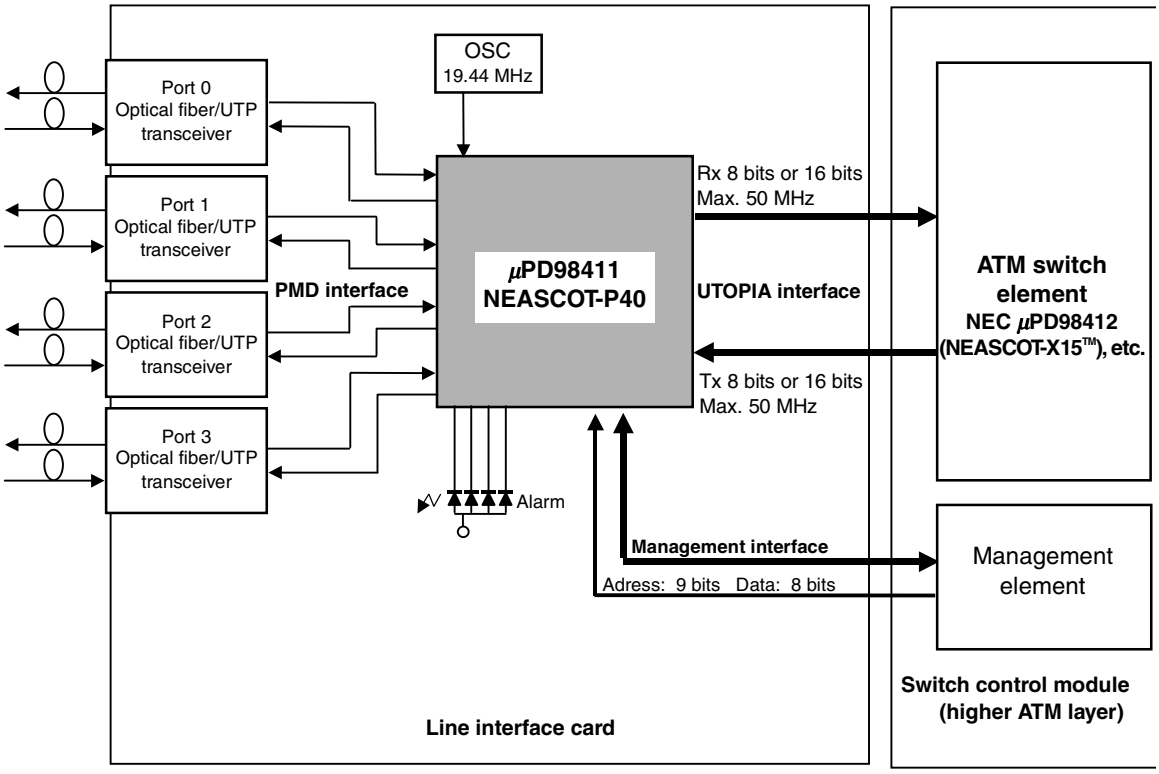
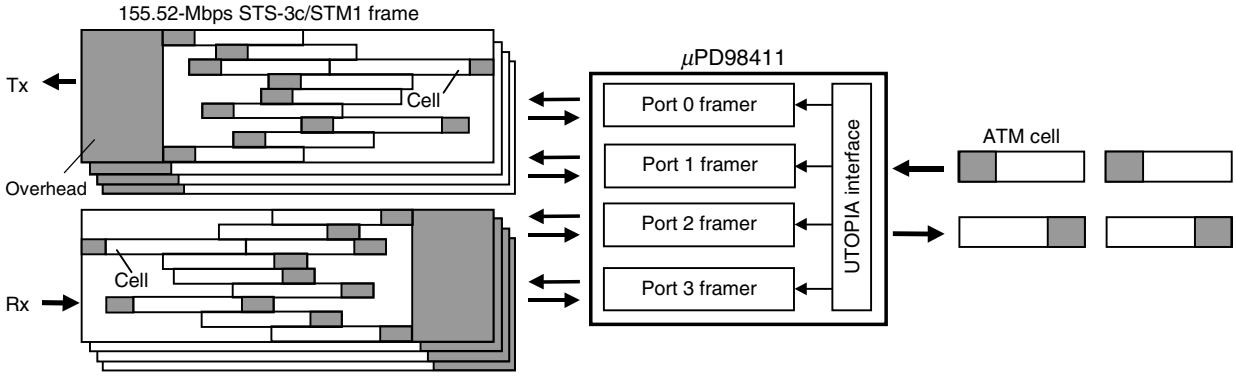
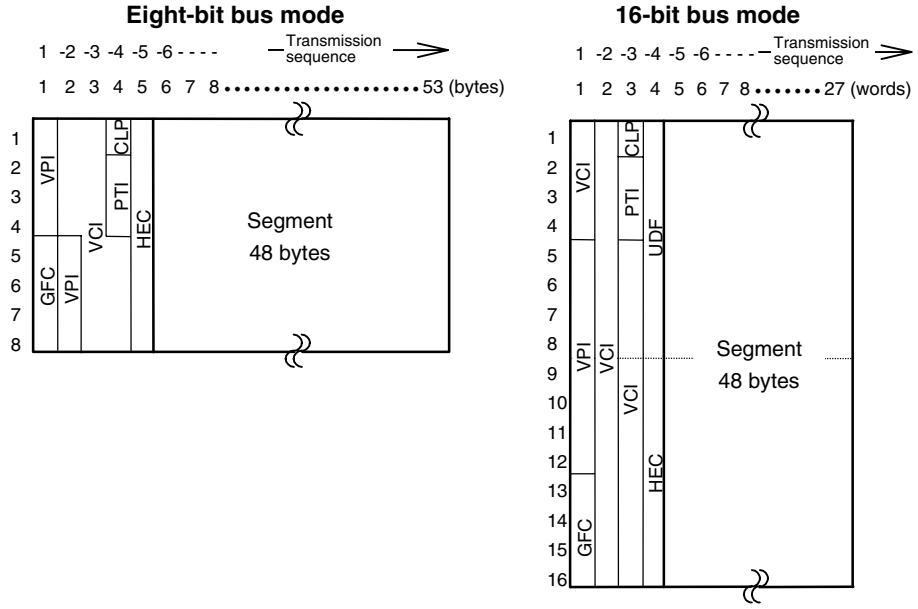


Figure 3-2. Transmit/Receive Data Flow of μPD98411



The format of the ATM cell (user network interface) is shown in Figure 3-3.

Figure 3-3. Structure of ATM Cell (for the User Network Interface (UNI))



GFC: Generic Flow Control
PTI: Payload Type Identifier
VPI: Virtual Path Identifier
CLP: Cell Loss Priority
VCI: Virtual Channel Identifier
HEC: Header Error Control
UDF: User Defined. The μPD98411 ignores this field on the transmission side (when it receives a cell from the ATM layer) or transmits it as all zeros on the reception side (when the μPD98411 transmits a cell to the ATM layer).

Figure 3-4. Format of STS-3c (1/2)

STS-3c/STM-1 frame

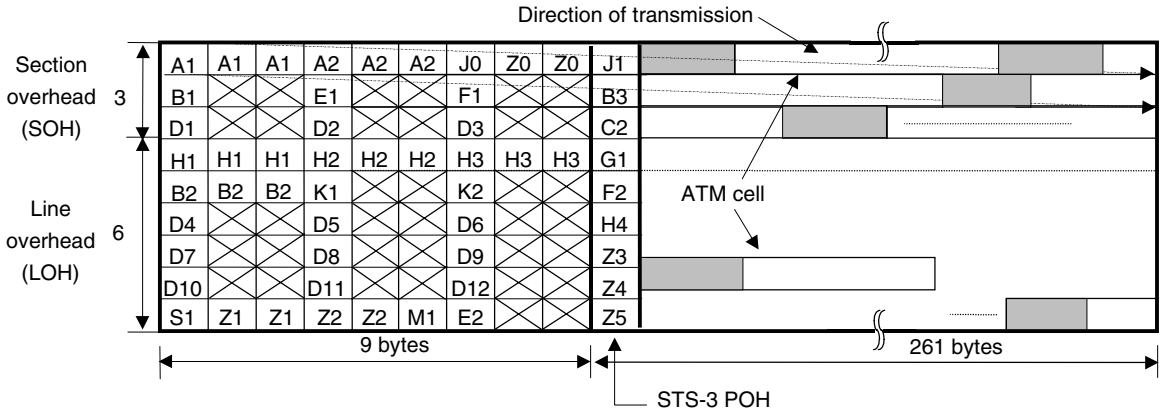
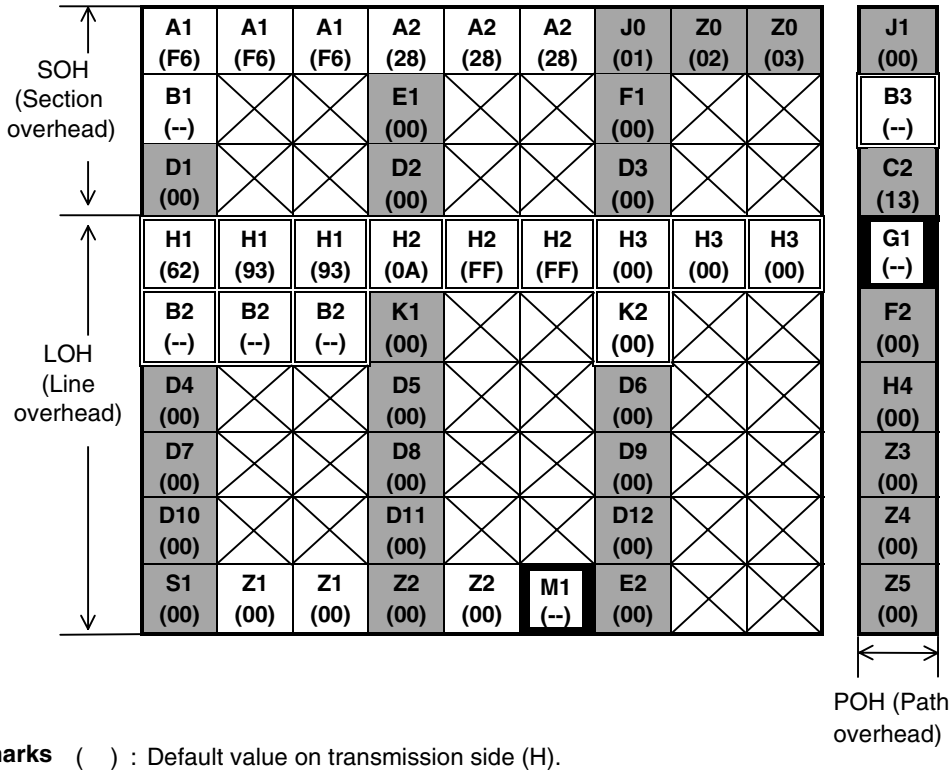


Figure 3-4. Format of STS-3c (2/2)



Remarks ( ) : Default value on transmission side (H).

: Byte area to/from which a value can be inserted or extracted by accessing a register for read or write.

: Byte area which is automatically inserted or verified by the μPD98411 and to/from which a value can be inserted/extracted by accessing a register for read or write only when a pseudo frame is transmitted.

: Byte area from which only a receive byte can be read.

: Byte area which can be automatically inserted or verified by the μPD98411 and which cannot be externally inserted or verified.

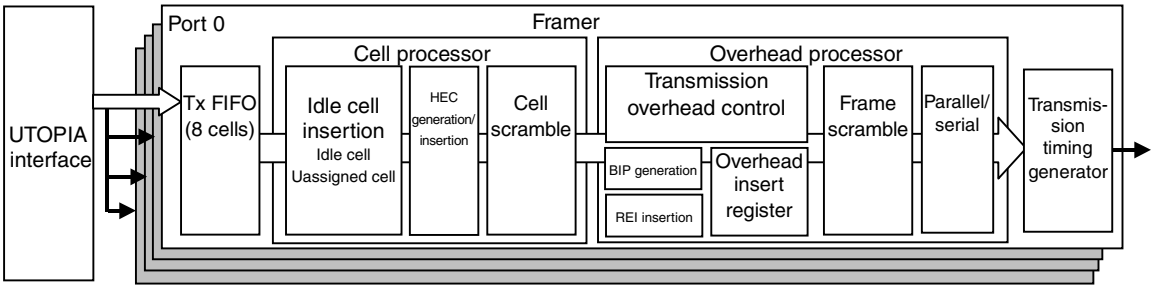
: Unused byte area. Insert 00H.

A1, A2 : Frame synchronization
J0 : Section trace
Z0 : Auxiliary
B1 : BIP-8
E1 : Order wire
F1 : User channel
D1-D3 : Data communication channel
H1, H2 : Pointer
H3 : Pointer action
B2 : BIP-24
K1 : Selection control
K2 : Section alarm indication
D4-D12 : Data communication channel
S1 : Synchronization status
Z1 : Auxiliary
Z2 : Auxiliary
M1 : Error indication
E2 : Order wire
J1 : Path trace
B3 : Path BIP-8
C2 : Signal label
G1 : Error indication, path status
F2 : Path user channel
H4 : Position indication
Z3-Z5 : Auxiliary

3.1 Transmission Function

The transmission function is used to insert a cell received from the higher ATM layer device via the multi PHY UTOPIA interface into the SONET STS-3c/SDH STM-1 frame generated by a specified port and to output the cell from the PMD interface (line side). This section explains the frame transmission function of the μPD98411 mainly based on the flow of processing.

Figure 3-5. Transmission Processing Flow



(1) Default status on transmission side

When power is applied, the framer function for all the ports is enabled and transmission is started in default mode. In this mode, the clock generated by the internal synthesizer PLL is selected as the transmission clock cause. The internal synthesizer PLL starts creating a 155.52-MHz clock from the 19.44-MHz clock input to the REFCLK pin, as soon as power is applied. However, about 10 ms must elapse before the 155.52 MHz clock supplied to each port settles in a stable state.

The UTOPIA interface is disabled until a mode is selected by accessing a register. After the interface has been initialized and before a cell is received from the higher ATM layer device, an idle cell (vacant cell) or unassigned cell is inserted into a frame and transmitted.

(2) Cell data reception from ATM layer device

A cell is received from the higher ATM layer device via the UTOPIA interface. The interface that transfers a cell between the μPD98411 and ATM layer device conforms to the multi PHY interface specified in "The ATM Forum UTOPIA Level2 v1.0 af-phy-0039.00 June 1995," as laid down by the ATM Forum. If allows you to select a bus width, handshake signal operations, and mode to support various systems. For the details of the UTOPIA interface, see **Section 4.1**.

In the default status that exists immediately after power application (after reset), the UTOPIA interface is disabled. To enable the UTOPIA interface, set the registers of the μPD98411 in the following sequence.

★ Before cell data is received, set the registers (AVLC and MltUT) related to the modes of the UTOPIA interface. Once cell data transfer has begun, do not change the contents of the registers.

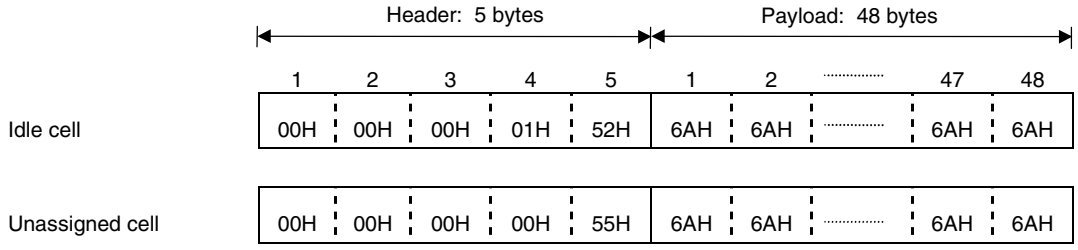
Setting (after H/W, S/W Reset)	Register
<1> Disable receive block (4 ports).	CMR2 register RDIS = 1
<2> Set PHY address and enable address (4 ports).	PHYIDR register
<3> Set the response timing of the CLAV signal (if it is necessary to change the setting).	AVLC register
<4> Set UTOPIA interface mode and enable the bus.	MltUT register
<5> Enable receive block (4 ports).	CMR2 register RDIS = 0

When cell data is received from the ATM layer device, it is stored into the transmit FIFO of a port specified by an address. Each of the four ports has a transmit FIFO with a capacity of about eight cells. This FIFO functions as a buffer to adjust the rate between the ATM layer side and PMD side.

If the transmit FIFO becomes full and cannot accept any more cells as a result of receiving the current cell, the TCLAV signal is deasserted low to inform the ATM layer. The threshold value at which the FIFO becomes full can be programmed to one to seven cells by using the **AVL1 through AVL3** bits of the **AVLC** register. This is useful for connecting an ATM layer device that cannot stop transferring cells immediately even after it has been informed by the TCALV signal that the transmit FIFO can no longer receive cells.

If no cell data is transmitted from the ATM layer and the FIFO does not have one cell of transmit data, a vacant cell (idle cell) is inserted. This idle cell can be replaced by an unassigned cell by changing the mode. To change the mode, set the **UCS** bit of the **AVLC** register (address: 78H). Figure 3-6 shows the formats of the idle cell and unassigned cell.

Figure 3-6. Format of Vacant Cell Inserted by μPD98411



★ **Remark** If cells in the idle or unassigned cell format are input to the transmit-side UTOPIA interface of the μPD98411, the μPD98411 usually treats these cells as valid data and outputs them to the line after mapping them into a frame. The μPD98411 does not drop them within it.

(3) Generation/insertion of HEC

CRC operation is performed on the high-order four bytes of the five bytes of the header of an ATM cell. The value resulting from the operation plus "55H" is inserted to the fifth byte position of the ATM header as HEC (Header Error Control).

Polynomial G (X) = $X^8 + X^2 + X + 1$

★ **Remark** The μPD98411 does not check the contents of the fifth byte (including HEC) that is counted from the start of the cell data input from the ATM layer device or use them within it. A HEC value obtained by calculation is written over this byte area. So insert a dummy byte like "00H" in the ATM layer device.

(4) Scramble of ATM cell

The data of an ATM cell is scrambled by using the following polynomial. The range of scramble is limited to the 48-byte payload of the ATM cell.

Polynomial G (X) = $X^{43} + 1$

The user can select a scramble stop mode for the purpose of testing. The scramble stop mode is set by the **CSCR** bit of **MDR3** register.

(5) Generation of SONET/SDH frame

The ATM cell stream is mapped onto the payload area of VC-4 of the virtual container of SONET/SDH, and the μPD98411 creates a SONET STS-3c/SDH STM-1 frame by combining the VC-4 path overhead (POH) and section overhead (SOH) information. The boundary of the ATM cell matches the boundary of the bytes of the VC-4 payload area. However, because its capacity (2,340 bytes) is not an integer multiple of the cell length (53 bytes), a cell may exist at the VC-4 payload boundary of two separate frames. For details of the format of the frame to be created, see **Figure 3-4**.

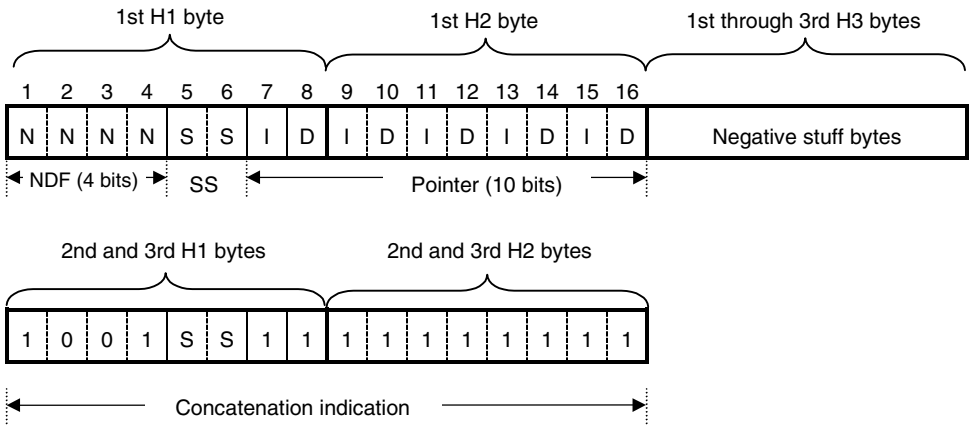
(a) AU pointer

The AU-4 pointer on the fourth line of the overhead and which consists of three types of bytes, H1, H2, and H3, is used as an address to identify the first byte (J1 byte of POH) of VC-4.

The transmit frame transmitted by the μPD98411 changes the position of neither POH (path overhead) nor the J1 byte. Therefore, the pointer value stored into the H1 and H2 bytes is always 20AH = "1000001010", and NDF is always fixed to "0110" and disabled. The SS bits that are the fifth and sixth bits of the H1 byte are "00" by default. Their values can be changed by setting the SS bit table of the MDR1 register.

Because Frequency Justification (stuff operation) is not requested at the transmission side, payload data is not set in the H3 byte that is used as a destuff byte. Instead, the H3 byte is set to all zeros and transmitted.

Figure 3-7. Format of AU Pointer (H1 through H3 Bytes)



Remark NDF: New Data Flag. Enable or disable command when the pointer value is to be changed. A disable command is issued if the μPD98411 does not change the pointer value.
NDF Enable = 1001, NDF Disable = 0010, 0110, 0100, 0111, 1110

SS bit: Indicates the type of the virtual container. The μPD98411 inserts the bit stored into the SS table of the **MDR1** register. The default value is "00".

Pointer: Indicates the position of the first byte J1 of POH and Frequency Justification (stuff operation).
I (Increment bit): Requests Positive Justification (positive stuff) operation.
D (Decrement bit): Requests Negative Justification (negative stuff) operation.

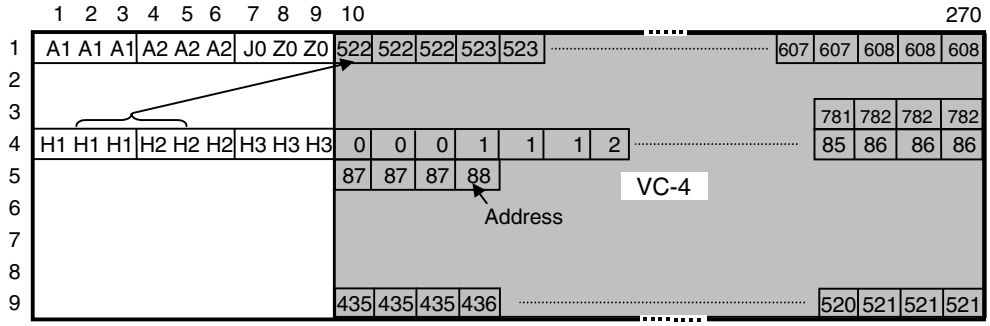
Concatenation indication: Indicates concatenation.

Contents of H1 through H3 bytes transmitted by μPD98411

	H1 Byte	H2 Byte	H3 Byte
1st	0110 SS10	0000 1010	0000 0000
2nd	1001 SS11	1111 1111	0000 0000
3rd	1001 SS11	1111 1111	0000 0000

Remark The pointer value of AU-4 is a binary number in the range of 0 to 782 and indicates the position of the first byte (J1) of VC-4. AU-4 increments the offset value of VC in three-byte units as shown in Figure 3-8. If the AU-4 pointer value is 0, for example, it indicates that VC-4 starts from the byte position immediately after the H3 byte. If the pointer value is 522 (20AH), VC-4 starts from the position immediately after the second Z0.

Figure 3-8. Offset Value of AU Pointer



(b) BIP generation

The B1, B2, and B3 bytes of the overhead are used to monitor an error of a frame. The μPD98411 performs a BIP (Bit Interleaved Parity) operation on the transmission data and inserts the result of the operation into the positions equivalent to the B1, B2, and B3 bytes of the next transmit overhead data.

(c) REI transmission

Whether a BIP error has occurred at the reception side is reported to the transmission destination device. If a B2 error is detected in a receive frame, the number of errors is stored into M1 (fourth through eighth bits) as Line REI (Remote Error Indication) for transmission. If a B3 error is detected, the number of errors is stored into G1 (first through fourth bits) as Path REI for transmission.

For an explanation of how to create BIP and transmit REI, see **(2)** in **Section 3.3.1**.

(d) Overhead area having insert register

The μPD98411 has an insert register that sets an arbitrary value in the following byte areas of the overhead for transmission. By setting this insert register via the management interface, any value can be transmitted. Until a value is set in the register, the default value of the register is transmitted. For details of the insert register, see **Section 3.4**.

- Overhead byte having insert register
  SOH: J0, 1st Z0, 2nd Z0, F1, E1, K1, K2, E2, S1, 1st Z2, D1 through D3, D4 through D12
  POH: J1, H4, F2, Z3, Z4, Z5

(6) Scramble of frame

The frame to be transmitted is scrambled by using the following polynomial expression. The entire range, except for the nine bytes, "A1, A1, A1, A2, A2, A2, J0, Z0, Z0", starting from the beginning of a frame, is scrambled.

Polynomial G (X) = $1 + X^6 + X^7$

The user can select a scramble stop mode for the purpose of testing. The scramble stop mode is selected by the **FSCR** bit of **MDR3** register.

(7) Frame output to PMD interface

The created frame data is converted into a serial data string and output to the line side from the PMD interface. The following five types of cause clocks that output data can be selected. For details of the PMD interface, see **Section 4.2**.

<1> Clock created by the internal synthesizer PLL based on the REFCLK input clock
<2> Clock created by the internal synthesizer PLL based on the REFCLK-2nd input clock
<3> Clock extracted by the internal clock recovery PLL of a port
<4> Clock extracted by the internal clock recovery PLL of another port
<5> Clock input to the TFKT/TFKC pin

Transmit data is output on the assumption that a low level is input to the TFSS pin. If a high level is input to this pin, all ports output all 1s.

(8) Transmission of alarm

By setting the **CMR1** register as necessary, alarm information APS, Line AIS, Path AIS, Line RDI, and Path RDI can be inserted into a specific overhead area of a transmit frame for transmission. Line RDI and Path RDI are automatically transmitted depending on the status of the reception side. Automatic transmission can also be masked by setting the **IACM** register. For details of transmitting an alarm, see **Section 3.3.1**.

(9) Transmitting a pseudo frame generating error

A function for generating and transmitting a pseudo error is provided for testing purposes. This function can be implemented by setting the **CMR3** register.

★ **(10) Transmission disable setting**

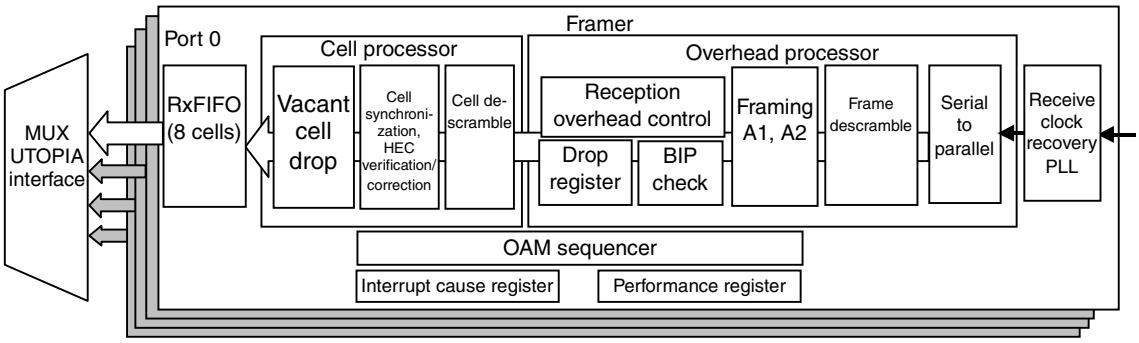
The transmission function of each port is disabled by setting the **TDIS** bit of the **CMR2** register to 1. If the **TDIS** bit is set to 1 for a port, the port stops supplying the system clock to the transmission block, and keeps outputting a bit string of all 0s to the line. Because the register keeps its contents unchanged, resetting the TDIS bit to 0 allows the previous operation to be resumed.

★ **Caution Setting the TDIS bit to 1 does not stop the UTOPIA interface block. Setting the TDIS bit to 1 for a port resets the transmit FIFO for the port. The UTOPIA interface block of the μPD98411 recognizes the transmit FIFO for the port as empty, makes the TCLAV signal high, and returns it to the ATM layer device.**
Setting the TDIS to 1 does not stop the synthesizer PLL either.

3.2 Reception Function

The reception function of the μPD98411 extracts an ATM cell from the SONET STS-3c/SDH STM-1 frame received from the PMD interface, and passes the cell to an ATM layer device by outputting it to the UTOPIA interface.

Figure 3-9. Reception Processing Flow



(1) Default status at reception side

The framer function of all the ports is enabled when power is applied, and the reception operation is started in default mode. The clock recovery PLL of each of the four ports starts extracting the clock synchronized with the bit string input to the RDIT/RDIC pin. This clock recovery is used for the sampling of receive data and the operation of the internal reception circuit. For details of the clock recovery operation, see **(2)** in **Section 4.2.3**.

The UTOPIA interface is disabled by default.

(2) Establishing frame synchronization

The bit string of the receive data is sampled and monitored by using the recovery clock. If the synchronization pattern of bytes A1 and A2 (six bytes) is detected in a bit string, the bit string at the position of bytes A1 and A2 of the next frame is checked. If the bit string has the same synchronization pattern, the frame synchronization (In frame) status is established.

Frame synchronization pattern: Six bytes (A1 A1 A1 A2 A2 A2)

A1 = 11110110 (F6H)

A2 = 00101000 (28H)

Even in the frame synchronization status, the μPD98411 always monitors the A1 and A2 byte positions (six bytes) of the receive frame. If four or more frames having a pattern different from the synchronization patterns are detected in succession, the μPD98411 enters the frame non-synchronization (Out of Frame) status.

(3) Descramble of receive frame

After frame synchronization has been established, the received frame is descrambled with the polynomial shown below. The entire range of the STS-3c/SDH STM-1 frame, except the nine bytes from the beginning, "A1, A1, A1, A2, A2, A2, J0, Z0, Z0" is descrambled.

Polynomial G (X) = $1 + X^6 + X^7$

An option mode that disables descrambling of a frame is provided for testing purposes. This mode is set by using the **FSCR** bit of the **MDR3** register.

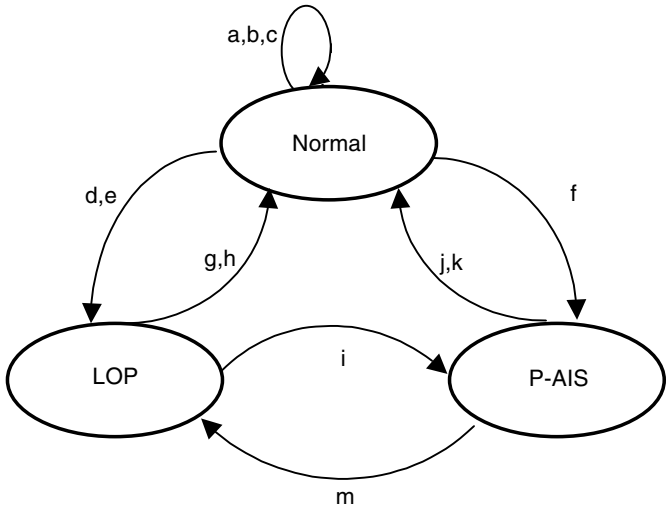
(4) Pointer processing

A pointer value that indicates the address of the first byte (J1 byte) of VC-4 is extracted from the H1 and H2 bytes of the descrambled receive frame, to establish pointer synchronization.

If an abnormal pointer is detected, the **LOP** (Loss Of Pointer) status is assumed. In addition, alarm **Path AIS** is detected from the H1 and H2 byte areas.

For the format of the pointer, see **Figure 3-7**.

Figure 3-10. Status Transition by Pointer Value



Normal status: The received pointer is normal and the pointer is received normally.

Path-AIS status: An error occurs in an upstream device or transmission path, such that the pointer cannot be received normally.

LOP status: The received pointer value is abnormal, such that the pointer is not received normally.

Table 3-1. Pointer Processing List

Transition		Condition
a	Normal → Normal	NDF Disable + same valid pointer have been received three times in a row.
b		NDF Enable + valid pointer have been received once.
c		Positive Justification/Negative Justification has been detected. See **(5)** below.
d	Normal → LOP	Invalid pointer has been received eight times in a row.
e		NDF Enable has been received eight times in a row.
f	Normal → Path-AIS	H1 and H2 bytes that are all "1" have been received three times in a row.
g	LOP → Normal	NDF Disable + same valid pointer have been received three times in a row.
h		NDF Enable + valid pointer have been received once.
i	LOP → Path-AIS	H1 and H2 bytes that are all "1" have been received three times in a row.
j	Path-AIS → Normal	NDF Disable + same valid pointer have been received three times in a row.
k		NDF Enable + valid pointer have been received once.
m	Path-AIS → LOP	H1 and H2 bytes that are not all "1" and a pointer value that does not satisfy conditions j and k, above, has been received eight times in a row.

If the OOF (Out Of Frame) status is detected, the LOP status is forcibly set.

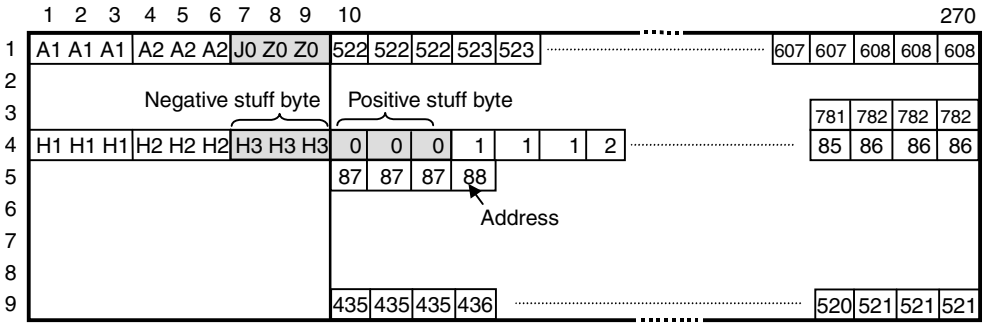
(5) Receive Frequency Justification (stuff operation)

Inversion of the I bit or D bit is identified by a majority during pointer processing at the reception side, and the Frequency Justification (stuff operation) is executed (see **Figure 3-7**).

Positive Justification (positive stuff): If it is detected that three or more I bits and up to two D bits of a new pointer are inverted with NDF = Disable, the byte at pointer address 0 is not received as payload data.

Negative Justification (negative stuff): If it is detected that up to two I bits and three or more D bits of a new pointer are inverted with NDF = Disable, the H3 byte area is received as payload data.

Figure 3-11. Stuff Byte



(6) Drop register of overhead information

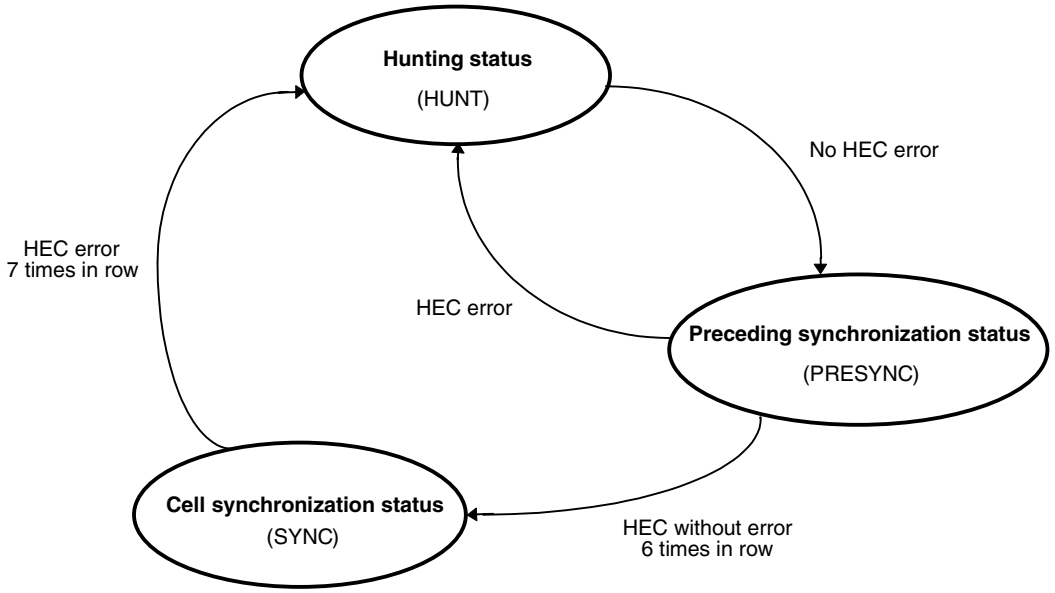
Drop registers that are used to read the contents of the following byte positions of the receive overhead are provided. By reading each drop register via the management interface, the received contents can be read. The contents of a drop register are updated each time a frame is received. However, the values of SOH and LOH are not updated if the frame is not synchronized, and the value of the POH area is not updated if the pointer is not synchronized. For details, see **Section 3.4**.

- Overhead bytes having drop register
  SOH, LOH: J0, 1st Z0, 2nd Z0, F1, E1, K1, K2, E2, S1, 1st Z2, D1 through D3, D4 through D12
  POH: J1, H4, F2, Z3, Z4, Z5

(7) Cell synchronization

Cell synchronization is used to identify a cell boundary and extract an ATM cell from the bit string accommodated in the payload area of VC-4. The cell boundary is identified by using the header error control (HEC) area for a cell header. In Figure 3-12 below, the status transition of cell synchronization by a header error control is shown. The number of protection stages is seven forward and six back.

Figure 3-12. Cell Synchronization Status Transition

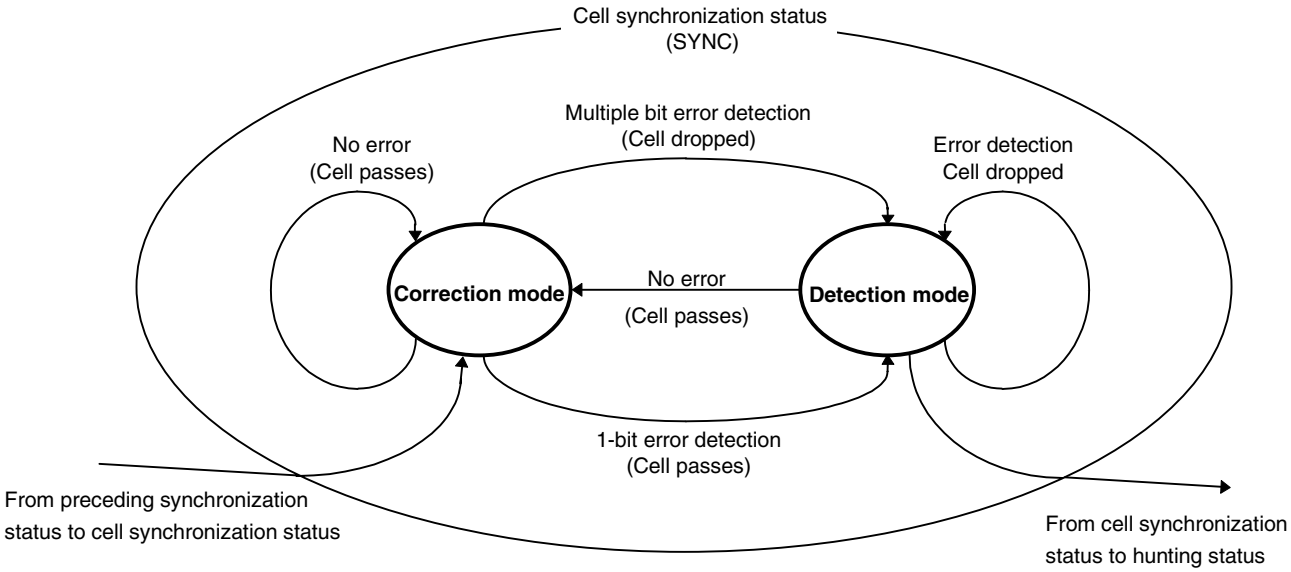


- The hunting status is that status in which synchronization is not established and a cell boundary is searched. A check of whether an HEC error has occurred is made. (CRC (Cyclic Redundancy Check) is conducted with 1 bit each shifted to check whether the remainder is 0.) If HEC coincides and an HEC with no errors is detected, the status changes to the preceding synchronization status.
- In the preceding synchronization status, reception is repeated until HEC without an error is detected six times in a row. If an HEC error is detected, the hunting status is set again. The sixth error-free cell is received and stored into the receive FIFO.
- In the cell synchronization status, it is judged that cell synchronization is no longer established if a HEC error is detected seven times in a row, and the hunting status is set again.
- Whether cell synchronization is established or not is indicated by the **OCD (Out of Cell Delineation)** bit of the ACR register. OCD indicates the hunting status or preceding synchronization status when it is 1 and the cell synchronization status when it is 0.
- If the OCD status lasts for 4 ms, the **LCD (Loss of Cell Delineation)** status occurs. LCD is cleared if the cell synchronization status lasts for 4 ms.

(8) HEC error control

While cell synchronization is established, a one-bit error of a cell header is corrected and errors of multiple bits are detected by means of header error control (HEC). As a result of the header error control processing, only the valid cell that includes error correction and which does not offer error correction in the header is stored into the receive FIFO and transferred to the ATM layer. Figure 3-13 shows the status transition of header error control.

Figure 3-13. HEC Check Status Transition in Cell Synchronization Status



- An error of only one bit is corrected in the correction mode and then the detection mode is set.
- HEC errors are continuously monitored in the detection mode. If errors are detected seven times, the status is changed from the cell synchronization status to the hunting status.
- Cell header error control differs depending on the setting of the **HECE** and **CORE** bits of **MDR3** register.

During header error control in the cell synchronization status, the mode can be changed as follows by using the **HECE** bit and **CORE** bit of the **MDR3** register.

Table 3-2. HEC Error Correction Mode

HECE	CORE	Current Mode	Event	Processing	New Mode
0	0	Correction mode	No error	-	Correction mode
			1-bit error detection	Error correction	Detection mode
			Multiple bit error detection	Cell dropped	Detection mode
		Detection mode	No error	-	Correction mode
			1-bit error detection	Cell dropped	Detection mode
			Multiple bit error detection	Cell dropped	Detection mode
	1	Correction mode	No error	-	Correction mode
			1-bit error detection	Cell dropped	Detection mode
			Multiple bit error detection	Cell dropped	Detection mode
		Detection mode	No error	-	Correction mode
			1-bit error detection	Cell dropped	Detection mode
			Multiple bit error detection	Cell dropped	Detection mode
1	x	Correction mode	No error	-	Correction mode
			1-bit error detection	-	Detection mode
			Multiple bit error detection	-	Detection mode
		Detection mode	No error	-	Correction mode
			1-bit error detection	-	Detection mode
			Multiple bit error detection	-	Detection mode

(9) Descramble of ATM cell

In the cell synchronization status, the data of the ATM cell is descrambled by the following polynomial. The range of descramble is limited to the payload of the ATM cell.

Polynomial $G(X) = X^{43} + 1$

An option mode in which the descrambling of cells can be disabled for testing purposes is supported. To set this mode, use the **CSCRM** bit of the **MDR3** register.

(10) Dropping idle and unassigned cells

If an idle cell is detected as a result of monitoring the high-order four bytes of the header of the cell stream extracted from a frame, the cell is not stored into the receive FIFO but is dropped. Patterns other than the VPI/VCI field of the header to be monitored can be changed by using the **DCHPR** and **DCHPMR** registers, so that an unassigned cell can be dropped or passed along with the idle cell. For details, see **Section 3.7**.

(11) Output of ATM cell from UTOPIA interface

Each port has a receive FIFO with a capacity of about eight cells. When cell synchronization is established, a cell that does not fit the pattern set by the **DCHPR** and **DCHPMR** registers is stored into the receive FIFO as a valid cell. The stored cell is transferred to the ATM layer device via the UTOPIA interface. If more cells are received once the receive FIFO is full, a receive FIFO overflow error occurs and those cells are dropped. The occurrence of a receive FIFO overflow error can be used as an interrupt cause.

When the power is applied, the μPD98411 starts receiving frames in default mode. However, the UTOPIA interface remains disabled until initialized by the host. If cells exceeding the capacity of the receive FIFO are received before the UTOPIA interface is enabled, the FIFO overflows and the cells are dropped. To enable the UTOPIA interface, set the registers of the μPD98411 in the following sequence:

Setting (after H/W, S/W Reset)	Register
<1> Disable receive block (4 ports).	CMR2 register RDIS = 1
<2> Set PHY address and enable address (4 ports).	PHYIDR register
<3> Set response timing of CLAV signal (if it is necessary to change setting).	AVLC register
<4> Set UTOPIA interface mode and enable the bus.	MltUT register
<5> Enable receive block (4 ports).	CMR2 register RDIS = 0

(12) Detection of line failure

A function for reporting the events that monitor and detect receive data, such as line failures, alarms, and the degradation of line quality, to the host via registers as OAM (Operation, Administration and Maintenance) information is provided.

- Detection of failure and alarm
- Detection of cause of line quality degradation
- Performance monitoring counter
- Monitoring event occurrence rate

For details, see **Section 3.3.2**.

★ **(13) Reception disable setting**

The reception function of each port is disabled by setting the **RDIS** bit of the **CMR2** register to 1. If the **RDIS** bit is set to 1 for a port, the port stops supplying the system clock to the reception block, and causes the clock recovery PLL to stop.

Cautions 1. Setting the RDIS bit to 1 for a port resets the receive FIFO for the port. If the RDIS bit is set to 1 when the port is outputting receive cell data from the UTOPIA interface, the data transfer is interrupted, and the RCLAV signal is made low.

2. Setting the RDIS bit to 1 may allow the status register to be set depending on the status of the receive line, because some register-related functions keep operating.

3.3 OAM Function

The μPD98411 has an OAM (Operation, Administration, Maintenance) function to maintain and monitor the network. This section explains the OAM functions supported by the μPD98411. Each of the four ports provides all OAM functions.

Table 3-3. OAM Functions

<table>
<tr><th rowspan="2">Action / Event</th><th colspan="2">Transmission</th><th colspan="3">Reception</th></tr>
<tr><th>Transmission of Alarm</th><th>Pseudo Error Frame Transmission</th><th>Detection of Alarm and Failure</th><th>Totalizing Counter</th><th>Monitor of Occurrence Rate</th></tr>
<tr><td>OOL</td><td rowspan="7"></td><td rowspan="2"></td><td rowspan="14">If a failure or alarm is detected, it is reported via a register.</td><td rowspan="8"></td><td rowspan="8"></td></tr>
<tr><td>LOS</td><td rowspan="13">Pseudo frame is created and transmitted by command setting. This function is intended for testing purposes.</td></tr>
<tr><td>OOF</td></tr>
<tr><td>LOF</td></tr>
<tr><td>LOP</td></tr>
<tr><td>OCD</td></tr>
<tr><td>LCD</td></tr>
<tr><td>Line RDI</td><td rowspan="2">Command or automatic return</td></tr>
<tr><td>Path RDI</td></tr>
<tr><td>Line AIS</td><td rowspan="3">Transmission by command setting</td></tr>
<tr><td>Path AIS</td></tr>
<tr><td>APS</td></tr>
<tr><td>B1 error</td><td rowspan="5">Calculated and transmitted for each frame</td><td rowspan="6">Events are counted and count value is indicated by register.</td><td rowspan="2">Whether set threshold value is exceeded while set number of frames is received is monitored. If it is exceeded, report is made.</td></tr>
<tr><td>B2 error</td></tr>
<tr><td>B3 error</td></tr>
<tr><td>Line REI</td></tr>
<tr><td>Path REI</td></tr>
<tr><td>FJ</td><td rowspan="5"></td><td rowspan="5"></td><td rowspan="5"></td><td rowspan="5"></td></tr>
<tr><td>FIFO overflow drop cell</td></tr>
<tr><td>HEC processing drop cell</td><td rowspan="3"></td></tr>
<tr><td>Receive idle cell</td></tr>
<tr><td>Valid cell</td></tr>
</table>

3.3.1 Transmission OAM Control

(1) Transmitting alarm

Alarm is written to a specific overhead area of the transmit frame and transmitted. Transmission can be started by setting a command in a register or automatically according to the line status at the reception side, depending on the type of the alarm, as shown in **Table 3-4** below.

Table 3-4. Transmitting Alarm

Alarm		Transmission Method	Related Register
(a)	APS	Transmitted/cleared by command	CMR1 register
(b)	Line AIS		
(c)	Path AIS		
(d)	Line RDI	• Transmitted/cleared by command • Automatically transmitted by occurrence of internal problem (Automatic transmission can be masked.)	CMR1 register Automatic return is masked by the IACM register.
(e)	Path RDI		

(a) Transmitting the APS (Automatic Protection Switching) code

The APS function is provided to switch a signal into an auxiliary signal in case a line fails. The switching operation is requested, confirmed, or acknowledged by using the K1 and K2 bytes in a section overhead in a line-multiplexed zone and by using the commands and protocols defined by ANSI T1.105.01 or ITU-T G.783. The APS signal is transmitted as follows:

<1> Set the APS signal to the K1T and K2T registers.

<2> Set the TAPS bit of the CMR1 register to 1. The contents of the K1T and K2T registers are stored into specific byte positions of the overhead and transmitted.

<3> To change the APS signal, update the contents of the K1T and K2T registers and then set the TAPS bit to 1 again. The new APS signal does not become valid even after the contents of the K1T and K2T registers have been updated, until the TAPS bit is set to 1.

<4> To stop the transmission of the APS signal, write 0 to the TAPS bit. When transmission is stopped, the K1 and K2 bytes of the transmit frame return either to the default value of "00H" or to the transmit condition of Line AIS and Line RDI if the condition is satisfied.

Remarks 1. If the TAPS bit of the CMR1 register is set to 1 immediately after the μPD98411 has transmitted the K1 byte of a transmit frame, a frame in which only the K2 byte is updated may be transmitted once.

2. If Line AIS, Line RDI, and APS commands are set in the CMR1 register at the same time, APS, Line AIS, and Line RDI are transmitted in that order.

3. If the APS signal is set at the same time as Path AIS, the APS signal and Path AIS are set in the same frame and transmitted.

4. While the APS signal is transmitted with TAPS set to 1, the setting of the D2 through D0 bits of the K2T register takes precedence over the sixth through eighth bits of the K2 byte. Consequently, Line RDI is not transmitted automatically.

(b) Transmitting Line AIS (Line Alarm Indication Signal)

Line AIS is a line alarm indication signal that detects a failure in the upstream and sends an alarm to the downstream during relaying. This signal is transmitted or cleared by setting a command in a register.

<1> To transmit: Set the TLAIS bit of the command set in the CMR1 register to 1.

<2> To clear: Clear the TLAIS bit of the command set in the CMR1 register to 0.

<3> Line AIS frame: Set the sixth through eighth bits of the K2 byte of the transmit frame to "111", and set all the bits in the VC-4 area (path overhead and payload) before scramble to "1" for transmission.

(c) Transmitting Path AIS (Path Alarm Indication Signal)

Path AIS is a path far-end reception failure information that is reported to the downstream when a failure is detected in the upstream and alarm is issued during relaying. This signal is transmitted or cleared by setting a command in a register.

<1> To transmit: Set the TPAIS bit of the command set in the CMR1 register to 1.

<2> To clear: Clear the TPAIS bit of the command set in the CMR1 register to 0.

<3> Path AIS frame: Set all the H1, H2, and H3 bytes in the section overhead area of the transmit frame, and all the bits of the VC-4 area (path overhead and payload) before scramble to "1" for transmission.

★ If the Path AIS and Path RDI transmission commands are set in the CMR1 register at the same time, or if the Path AIS transmission command is set in the CMR1 register while Path RDI is being automatically sent back, Path AIS and Path RDI are transmitted in the stated sequence.

(d) Transmitting Line RDI (Line Remote Detect Indication)

Line RDI is a signal that reports detection of a line receive failure (LOS, LOF, or Line AIS) to a unit in the upstream. This signal is transmitted or cleared by setting a command in a register or automatically if a failure or alarm is detected at the reception side.

<1> To transmit:
- i) Set the TLRDI bit of the CMR1 register to 1.
- ii) If the LRDIm bit of the IACM register is 0, the Line RDI signal is automatically transmitted when any of LOS, LOF, and Line AIS is detected at the reception side.
  If the LRDIm bit is 1, the automatic transmission is masked.
  It is masked by default.

<2> To clear:
- i) Clear the TLRDI bit of the CMR1 register to 0.
- ii) If the LRDIm bit of the IACM register is 0 and if all of LOS, LOF, and Line AIS are cleared at the reception side.

<3> Line RDI frame: The sixth through eighth bits of the K2 byte of the overhead are set to "110" for transmission.

(e) Transmitting Path RDI (Path Remote Detect Indication)

Path RDI is a signal that reports detection of a path receive failure (LOS, LOF, Line AIS, LOP, LCD, or Path AIS) to a unit in the upstream. This signal is transmitted or cleared by setting a command in a register or automatically transmitted if a failure or alarm is detected at the reception side.

<1> To transmit: i) Set the TPRDI bit of the CMR1 register to 1.
ii) If the PRDIm bit of the IACM register is set to 0, the Path RDI signal is automatically transmitted when any of LOS, LOF, Line AIS, LOP, LCD, and Path AIS is detected at the reception side. If the PRDIm bit is set to 1, automatic transmission is masked. It is masked by default.

<2> To clear: i) Clear the TPRDI bit of the CMR1 register to 0.
ii) If the PRDIm bit of the IACM register is 0 and if all of LOS, LOF, Line AIS, LOP, LCD, and Path AIS are cleared at the reception side.

<3> Path RDI frame: The fifth bit of the G1 byte of the overhead is set to 1 for transmission.

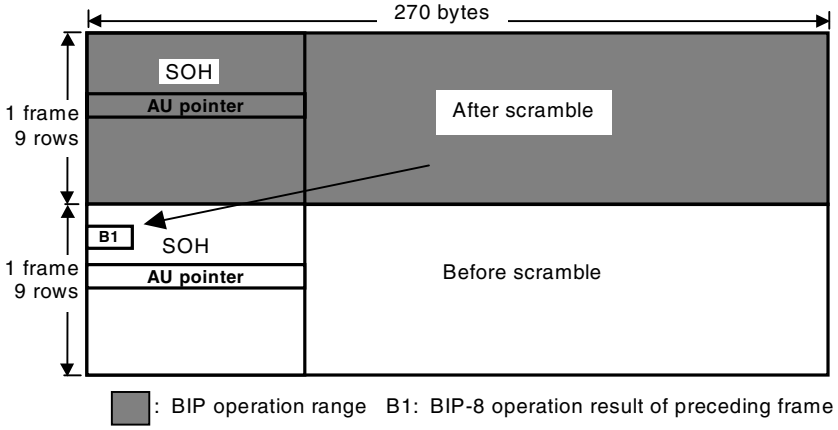
Remark If Line RDI or Path RDI is automatically transmitted because a failure or alarm that serves as a condition is detected at the reception side, and if the receive frame function of a port is disabled (RDIS bit of CMR2 register = 0), the transmission side of the port keeps transmitting the frame of Line RDI or Path RDI until the receive frame function is enabled and the failure or alarm is cleared. If this poses a problem, mask the automatic transmission function.

(2) Functions related to monitoring line quality on transmission side

(a) Bit Interleaved Parity (BIP)

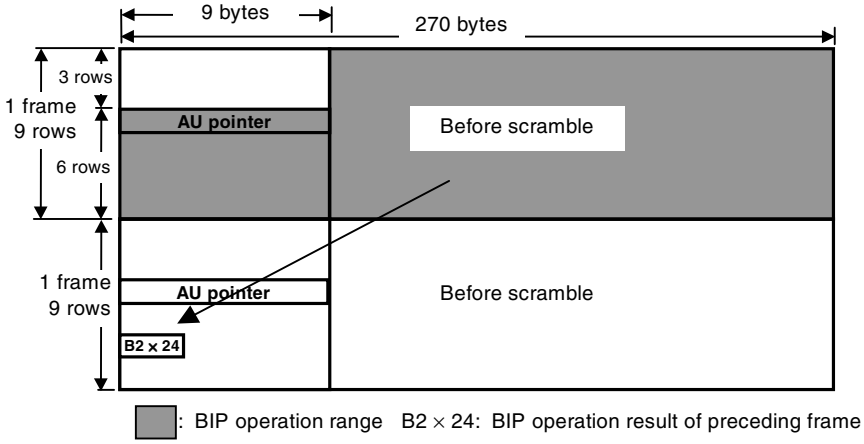
- **B1 byte (Section BIP-8)**

BIP-8 operation is performed on all the frame data (data after scramble) except the first line of SOH (section overhead) of the transmit frame, BIP-8 operation is performed on a specific area, and the result of the operation is inserted in the B1 byte of the transmit frame and transmitted.



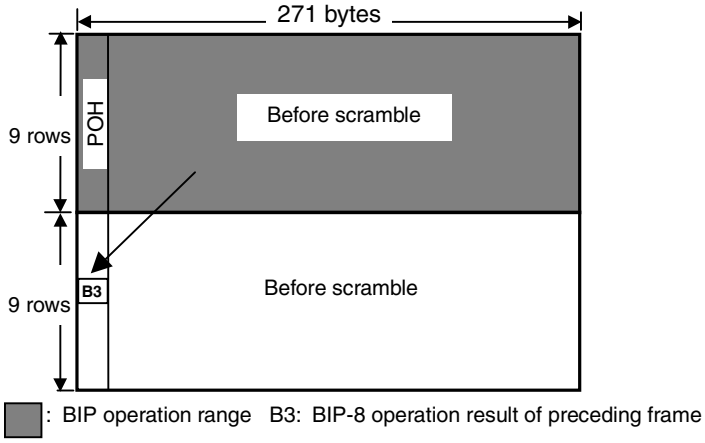
- **B2 byte (Line BIP-24)**

  BIP-24 operation is performed on all frame data (data before scramble) except the first, second, and third lines of SOH one frame before, and the result of the operation is inserted to the B2 byte of the next transmit frame and transmitted.



- **B3 byte (Path BIP-8)**

  BIP-8 operation is performed on all the payload data (data before scramble), and the result of the operation is inserted to the B3 byte of POH (path overhead) of the next transmit frame and transmitted.



(b) Transmitting Line REI (Line Remote Error Indication)

Whether Line BIP-24 error has occurred is reported to a unit in the upstream.

When the μPD98411 detects a B2 error in the receive frame, it automatically stores the number of error bytes in the M1 byte (fourth through eighth bits) of the transmit frame and transmits the byte.

(c) Transmitting Path REI (Path Remote Error Indication)

Whether Path BIP-8 error occurs is reported to a unit in the upstream.

When the μPD98411 detects a B3 error in the receive frame, it automatically stores the number of error bytes to the G1 byte (first through fourth bits) of the transmit frame and transmits the byte.

(3) Transmission function of pseudo frame for testing

A pseudo frame that can cause the errors shown in Table 3-5 can be internally generated and transmitted. This function is useful for testing a system, and can be executed by setting the **CMR3** register.

Table 3-5. Pseudo Error Frame

Target Error	Pseudo Frame Name	Description of Transmit Frame
LOS	PLOS frame	Transmit data is fixed to 00H.
OOF/LOF	POOF frame	Bytes A1 and A2 are fixed to 00H.
LOP	PLOP frame	Bytes H1, H2, and H3 are fixed to FFH, FEH, and FFH.
	PLOP II frame	Bytes H1, H2, and H3 are changed as specified by H1T, H2T, and H3T registers.
OCD, LCD	POCD frame	Cell with LSB bit in HEC field inverted is mapped.
B1 error	PB1 frame	LSB bit of B1 byte is inverted.
B2 error	PB2 frame	LSB bit of B2 byte is inverted.
	PB1 II frame	B2 byte data to be transmitted is changed to contents set in B2T register.
B3 error	PB3 frame	LSB bit of B3 byte is inverted.
	PB2 II frame	B3 byte data to be transmitted is changed to contents set in B3T register.
Line REI	PLREI frame	LSB bit of B2 byte of receive frame is inverted and passed to B2 verification block.
Path REI	PPREI frame	LSB bit of B3 byte of receive frame is inverted and passed to B3 verification block.

3.3.2 Reception OAM Control

(1) Detection of alarm and failure

Table 3-6 lists the failures and alarms monitored by the μPD98411. If any of these events has been detected, the following actions are taken.

<1> The corresponding bit of the interrupt cause register is set.
The host identifies the event that has occurred by reading the interrupt source register.

<2> An interrupt signal is asserted active to report the host.
Whether an interrupt signal corresponding to each event is asserted active can be selected.

<3> The PALM output pin is driven when an event occurs.
The occurrence of an event can be reported to an external peripheral device via the PALM[2:0] pins or by lighting an LED.

Table 3-6. Alarms and Failures (1/3)

(1) OOL (Out Of Link)
Indicates the phase relation between the receive clock recovery PLL and receive data. • Detection: If the phase of the edge of the receive data shifts through 180 degrees of more relative to the edge of the extracted clock of the clock recovery PLL • Clear: If receive data with an edge that does not shift through 180 degrees or more relative to the edge of the extracted clock of the clock recovery PLL is received for a 2,048-bit period • Indication register: PICR register (OOL bit)
(2) exCMD (External Device State)
Indicates the status of the CMD pin of the general-purpose input port. • Detection: If the CMD pin input goes high • Clear: If the CMD pin input goes back low • Indication register: PICR register (exCMD bit)
(3) LOS (Loss Of Signal)
Receive signal lost status • Detection: If a data string of all zeros is received continuously for 50 μs, or if the SD pin goes low • Clear: If patterns consisting entirely of 0s are not received for 125 μs, or if the SD pin goes high • Indication register: PICR register (LOS bit) ★ Adding a change in the input level of the SD pin as a LOS detection condition requires resetting the SDm bit of the IACM register to 0. ★ **Caution The μPD98411 is designed to allow the receive cell to be output to the UTOPIA interface even if a LOS detection status has been entered. Therefore, if cell synchronization is established, the cell is output to the receive UTOPIA interface even after a LOS detection status has been entered. If normal receive data is received from the line, making only the input to the SD pin low causes the μPD98411 reports on LOS detection; note, however, that the receive cell is output.**
(4) OOF (Out Of Frame)
Frame non-synchronization • Detection: If frame synchronization pattern (A1, A2) error is detected in four successive frames • Clear: If frame synchronization pattern is detected in two successive frames • Indication register: ACR register (OOF bit)

Table 3-6. Alarms and Failures (2/3)

(5) LOF (Loss Of Frame)
Frame lost status • Detection: If OOF status lasts for 3 ms • Clear: If non-OOF status lasts for 3 ms • Indication register: PICR register (LOF bit)
(6) LOP (Loss Of Pointer)
Pointer error detection. This occurs if a valid pointer cannot be obtained. • Detection: See **(4)** in **Section 3.2**. • Clear: See **(4)** in **Section 3.2**. • Indication register: ACR bit (LOP bit)
(7) OCD (Out of Cell Delineation)
Cell non-synchronization. This occurs when status transition from the cell synchronization status to hunting status takes place. • Detection: If cells including an error have been detected seven times continuously during HEC verification (cell synchronization status → hunting status) • Clear: If cells having valid header are detected seven times continuously (hunting status → preceding synchronization status → cell synchronization status) • Indication register: ACR register (OCD bit)
(8) LCD (Loss of Cell Delineation)
Cell synchronization loss. This occurs if the OCD status persists. • Detection: If OCD continues for more than 4 ms. • Clear: If the cell synchronization status lasts for 4 ms after OCD. • Indication register: ACR register (LCD bit)
(9) Line AIS (Line Alarm Indication Signal)
Line alarm indication signal. Detects occurrence of Line AIS in unit of transmission source (upstream). • Detection: If frames with overhead byte K2 (sixth through eighth bits) being "111" are received five times continuously • Clear: If frames with overhead byte K2 (sixth through eighth bits) not being "111" are received five times continuously • Indication register: ACR register (LAIS bit) **Remark** The number of times the detection/clear condition is to be satisfied can be changed from five times continuously to three times continuously by setting the ITUR register. The default is five times.
(10) Path AIS (Path Alarm Indication Signal)
Path alarm indication signal. Detects occurrence of Path AIS in unit of transmission source (upstream). • Detection: See **(4)** in **Section 3.2**. • Clear: See **(4)** in **Section 3.2**. • Indication register: ACR bit (PAIS bit)
(11) Line RDI (Line Remote Defect Indication)
Line remote reception failure information. Indicates detection of line reception failure (LOS, LOF, or Line AIS) in unit of transmission destination (downstream). • Detection: If frames with overhead byte K2 (sixth through eighth bits) being "110" are received five times continuously • Clear: If frames with overhead byte K2 (sixth through eighth bits) being other than "110" are received five times continuously • Indication register: ACR register (LRDI bit) **Remark** The number of times the detection/clear condition is to be satisfied can be changed from five times continuously to three times continuously by setting the ITUR register. The default is five times.

Table 3-6. Alarms and Failures (3/3)

(12) Path RDI (Path Remote Defect Indication)
Path remote reception failure information. Indicates detection of path reception failure (LOS, LOF, Line AIS, LOP, LCD, or Path AIS) in unit of transmission destination (downstream). • Detection: If frames with fifth bit of overhead byte G1 being "1" are received five times continuously • Clear: If frames with fifth bit of overhead byte G1 being "0" are received five times continuously • Indication register: ACR register (PRDI bit) **Remark** The number of times the detection/clear condition is to be satisfied can be changed from five times continuously to three times continuously by setting the ITUR register. The default is five times.
(13) APS (Automatic Protection Switching)
Detects that the APS bytes (K1 and K2 bytes) have been received for an auxiliary switching operation. • Detection: If the APS bytes are other than "00 00H" and if a frame having the same value is received three times continuously • Clear: If a frame in which the APS bytes are "00 00H" is received three times continuously, or if the RAPSCR bit of the MDR3 register is set to 1 • Indication register: PCR register (RAPS bit) If three frames having APS bytes with the same value but not "00 00H" are received three times continuously, the RAPS bit of the PCR register is set to 1. The setting of this bit can be used as an interrupt cause. When it is detected that the PCR register has been read and that the RAPS bit has been set, the K1R and K2R register are read and the APS bytes are obtained. Subsequently, the RAPSC bit of the MDR3 register is set to 1 and the μPD98411 exits from the APS detection status as a result. It also exits from the APS detection status when three frames in which the APS bytes are "00 00" are received continuously. If the interrupt mode is the mode of RCM = 0, the PCR register is read again and the RAPS bit is cleared. The RAPS bit is set next time when three or more frames containing patterns other than the preceding APS byte are received. While the same pattern as the preceding APS bytes is received, the RAPS bit is not set. **Remark** The RAPS bit is also set when the alarm indication frame of Line AIS and Line RDI, that are transmitted by using the K2 byte, is received.

(2) Detecting the degradation of line quality (performance monitor)

The events in Table 3-7 are detected when the quality of the reception line is monitored. If an event is detected, the bits of the PCR register are set, and the detection is reported to the host by using an interrupt signal. The host can identify the type of the event that has occurred by reading the PCR register. The interrupt can be masked or unmasked for each event.

Table 3-7. Causes of Degradation in Line Quality

B1 error detection
Detects section layer BIP-8 error in receive data. BIP-8 operation is performed on all frame data (data before descramble) except first line of SOH one frame before, result of this operation is verified against result of Section BIP-8 operation performed at transmission source (upstream) and stored to B1 byte of current frame, and B1 error is detected.
B2 error detection
Detects line layer BIP-24 error in receive data. BIP-24 operation is performed on all frame data (data after descramble) except first, second, and third lines of SOH one frame before, result of this operation is verified against result of Line BIP-24 operation performed at transmission source (upstream) and stored to B2 byte of current fame, and B2 error is detected.
B3 error detection
Detects path layer BIP-8 error in receive data. BIP-8 operation is performed on all payload data (data after descramble) one frame before, result of this operation is verified against result of Path BIP-8 operation performed at transmission source (upstream) and stored to B3 byte of current frame, and B3 error is checked.
Line REI detection (Line Remote Error Indication)
Line far-end block error information. Detects Line BIP-24 errors in unit at transmission destination (downstream). Detection: Line REI is detected if fourth through eighth bits of receive M1 byte are 01(H) to 18(H) Clear: Line REI is cleared if fourth through eighth bits of receive M1 byte are 00(H)
Path REI detection (Path Remote Error Indication)
Path far-end block error information. Detects Path BIP-8 errors in unit at transmission destination (downstream). Detection: Path REI is detected if first through fourth bits of receive G1 byte are 1(H) to 8(H) Clear: Path REI is cleared if first through fourth bits of receive G1 byte are 0(H)
Occurrence of Frequency Justification
Detects occurrence of Frequency Justification

Table 3-8 lists the relationships between the failure and alarm that is internally processed by the μPD98411, and event detection of performance monitoring.

Table 3-8. μPD98411 Processing upon Detection of Failure or Alarm

Alarm and Failure	Internal Processing of μPD98411			
LOS			→	(Automatic transmission of Line/Path RDI)
OOF	Loss of SOH, LOH	H1, H2, H3 byte position loss	→	LOP
		K2 byte position loss	→	Line AIS detection stopped
			→	Line RDI detection stopped
			→	APS detection stopped
		B1 byte position loss	→	B1 error detection stopped
		B2 byte position loss	→	B2 error detection stopped
			→	Transmit Line REI transmission
		M1 byte position loss	→	Receive Line REI detection stopped
	Continuation for 3 ms		→	LOF
LOF			→	(Automatic transmission of Line/Path RDI)
Path AIS	Pointer loss		→	LOP[Note]
			→	(Automatic transmission of Path RDI)
LOP	Loss of POH	G1 byte position loss	→	Path RDI detection stopped
			→	Receive Path REI detection stopped
		B3 byte position loss	→	B3 error detection stopped
			→	Transmit Path REI transmission stopped
		Cell extraction stopped	→	OCD
			→	(Automatic transmission of Path RDI)
OCD	Continuation for 4 ms		→	LCD
LCD			→	(Automatic transmission of Path RDI)
Line AIS			→	(Automatic transmission of Line/Path RDI)
Path PDI	None			
Line RDI	None			

Note The LOP bit of the ACR register is not set but the internal processing is the same as that for "pointer loss" in the LOP detection status.

(3) Performance monitoring counter

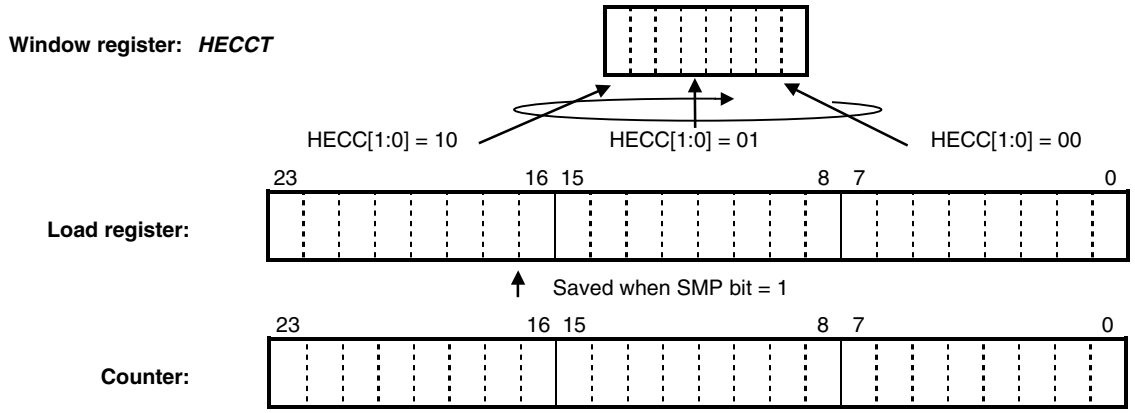
The performance monitoring counters that totalize the number of times each event for a cell reception has occurred are provided to each port as shown in Table 3-9.

★ **Table 3-9. Performance Monitoring Counters**

Classification	Counter Name	Contents	Counter Width
Line	B1 error counter	Cumulative number of detected B1 errors. Detected B1 errors (1 to 8) are counted each time a frame is received.	16 bits
	B2 error counter	Cumulative number of detected B2 errors. Detected B2 errors (1 to 24) are counted each time a frame is received.	24 bits
	B3 error counter	Cumulative number of detected B3 errors. Detected B3 errors (1 to 8) are counted each time a frame is received.	16 bits
	L-REI counter	Cumulative number of errors received at Line REI. Detected B3 errors (1 to 24) are counted each time a frame is received.	24 bits
	P-REI counter	Cumulative number of errors received at Path REI. Detected B3 errors (1 to 8) are counted each time a frame is received.	16 bits
	FJ counter	Number of Frequency Justification processings	16 bits
Cell reception	HEC counter	Total number of cells dropped by HEC processing	24 bits
	FIFO Full counter	Total number of cells dropped due to receive FIFO overflow	24 bits
	Idle Cell counter	Cumulative number of cells dropped according to the setting of the **DCHPR** and **DCHPMR** registers. The default setting of the **DCHPR/DCHPMR** register causes idle cells to be dropped.	24 bits
	Information Cell counter	Cumulative number of receive cells except those counted in the HEC and Idle Cell counters. Cells dropped because of a receive FIFO overflow are counted in both the FIFO Full and Information Cell counters.	24 bits

The counter functions and the registers which implement these functions are shown below.

Figure 3-14. Counter-Related Registers (Example: HEC Error Counter)



(a) Monitoring a counter

Two types of counters, 16-bit counters and 24-bit counters, are supported. Each counter consists of three stages: a counter, a load register, and a window register. All the counters are disabled by default.

(Monitoring a counter)

<1> Enable the counter for the event to be counted (by using the PCFR1 and PCFR2 registers).

<2> Set the SMP bit of the PCSR register to 1 (for sampling).

→ Save the values of all the counters at that point into the load registers.

→ The counters are cleared to 0.

→ The SMP bit is automatically cleared to 0.

<3> Read the window register of the counter.

→ Read a 16-bit counter two times to obtain the low-order eight bits and the high-order eight bits.
Read a 24-bit counter three times to obtain the low-order eight bits, middle-order eight bits, and high-order eight bits.

→ The PCPR1 and PCPR2 registers indicate which of the low-order, middle-order, or high-order eight bits can be read when the window register is next read. Each time the window register has been read, its value changes from 0 to 1 and from 1 to 0 in the case of a 16-bit counter, and from 00 to 01, from 01 to 10, and from 10 to 00 in the case of a 24-bit counter.

→ A value that has been saved to a load register is retained until the SMP bit is set and the value is overwritten.

(b) Initializing a counter

A counter can be initialized (cleared to 0) in the following three ways.

i) Set the PCCR bit of the CMR2 register to 1.
→ All the counters and load registers are cleared to 0.

ii) Set the bits corresponding to the PCIR1 and PCIR2 registers to 1.
→ The counter and the load register of the corresponding counter are cleared to 0.
→ The bits of the PCIR1 and PCIR2 registers that have been set return to 0 after they have been cleared.

iii) Set the SMP bit of the sample register to 1.
→ The count values of all the counters are saved to the load registers and, at the same time, are cleared to 0.

(c) Reporting detection of counter overflow

If the value of a counter has passed all F(H) after the counter started totalizing, the corresponding bits in the **PCOCR1** and **PCOCR2** registers are set to 1 to detect an overflow. The setting of these bits can be used as an interrupt cause depending on the setting of the **PCOMR1** and **PCOMR2** registers.
A counter whose value has reached all F(H) returns to 0 and continues counting.

(d) Error rate monitor

Of the ten types of counters, the six (B1 error, B2 error, B3 error, Line REI, Path REI, and Frequency Justification) which are intended to monitor the degradation of the line quality can be used to report, instead of overflow detection, that a threshold value has been reached within a specific time if a specific time (cycle) and threshold value are set.

(Error rate monitor setting procedure)

★ **<1>** Enable the counters (by using PCFR1 and PCFR2 registers).

<2> Set a threshold value in the threshold registers (such as B1THR and B2THR).

<3> Select time (cycle) from the following and set it in the **FRMN** register. The value is applied for all four ports.

Setting Bits	Cycle (Time)
00000000	Disable (infinite)
00000010	8 frames (1 ms)
00000100	80 frames (10 ms)
00001000	400 frames (50 ms)
00010000	1,000 frames (125 ms)
00100000	2,000 frames (250 ms)
01000000	4,000 frames (500 ms)
10000000	8,000 frames (1s)

<4> If the threshold value is reached within the set time, the corresponding bit of the PCOCR1 and PCOCR2 registers is set to 1. This bit can be used as an interrupt cause.
The counter is cleared to 0 and continues counting.

<5> If the set time elapses without the threshold value being reached, the counter is cleared to 0 and starts counting again.

★ (Error rate monitor clearing procedure)

<1> Load the threshold registers (such as B1THR and B2THR) with FFH.

<2> Load the FRMN register with all 0s (0000H).

★ **Caution 1. A "threshold value" set in the threshold register becomes valid only after the FRMN is write-accessed. For this reason, a value must be set in the FRMN register after the threshold register.**

★ **2. Once the FRMN register is accessed, an interval of "130 × REFCK cycle (about 7 μs)" must be allowed before the FRMN register is accessed again.**

★ **3. If the error rate monitor function is used, the host cannot load counters with values at arbitrary time. This is because setting the SMP bit of the PCSR register to 1 in order to load a counter clears all the counters to 0, thus disabling an error rate threshold value from being judged correctly.**

★ **4. When using the error rate monitor function, disable the cell-related counters. If the cell-related counters (such as the Idle Cell counter) are enabled, they count even when the error rate monitor function has been enabled. When the counters pass through all 1s (FH), therefore, they set the overflow status bit.**

(e) Relation between detection of failure and alarm and counter operation

Table 3-10 shows the operating conditions of the counter.

Table 3-10. Relation between Failure and Alarm and Counter Operation

Failure and Alarm	Counter Operation of μPD98411						
	B1	B2	Line REI	FJ	B3	Path REI	Cell-Related
LOS	×	×	×	×	×	×	×
OOF	×	×	×				
LOF	×	×	×	×	×	×	×
Line AIS		×	×	×	×	×	×
Line RDI			×				
LOP				×	×	×	×
Path AIS				×	×	×	×
Path RDI						×	
OCD							
LCD							×

×: Counting stops if an event occurs.

Blank: Counting continues even if an event occurs.

★ **Caution The specification states that all performance monitoring counters are to be kept from counting while LOS detection is under way. Therefore, the Information Cell counter does not count cells that are received while LOS detection is under way. When a loopback test is conducted by disconnecting the reception line cable and placing the μPD98411 in the TPLP loopback mode with LOS detection enabled, cells that are input to the μPD98411 pass through it and are looped back at the reception UTOPIA interface. Note that these cells are not counted by the Information Cell counter, which is intended to count receive cells.**

★ **Remark** Specification E and earlier state that the cell-related counters are to stop counting when Path RDI is detected. However, specification X and later state that the counters are not to stop counting when Path RDI is detected.

(f) Counter-related registers

Table 3-11 lists all the registers related to the counter functions.

Table 3-11. Counter-Related Registers

Type	Function
<1> Registers related to counter provided to each port	
Window registers B1ECT, B2ECT, B3ECT, LRECT, PRECT, FJCT, HECCT, FULCT, IDLCT, INFCT	Registers that read the counter value. Each time these registers have been read, their value indicates the low-order eight bits, high-order eight bits, low-order eight bits, high-order eight bits, and so on, in the case of a 16-bit counter. In the case of a 24-bit counter, the register value indicates the low-order eight bits, middle-order eight bits, then high-order eight bits.
Read pointer registers PCPR1, PCPR2	Indicate which of the low-order, middle-order, or high-order eight bits of a 16-bit or 24-bit counter can be read when the window register is next read.
Sample register PCSR	Register instructing that the value of the counter is to be saved to the load register.
Initialization registers PCIR1, PCIR2	Registers instructing that each counter is to be cleared to 0.
Freeze registers PCFR1, PCFR2	Registers that enable or disable the counter operation. All the counters are disabled by default.
Overflow report registers PCOCR1, PCOCR2	Indicate that a specific counter has reached the threshold value. Setting the bits of these registers can be used as an interrupt cause.
Mask registers PCOMR1, PCOMR2	Registers masking the reflection of setting of the overflow cause registers (PCOCR1 and PCOCR2) on the PCO bit of the interrupt cause register (PICR).
<2> Registers related to counters common to four ports	
Threshold registers B1THR, B2THR, B3THR LRETHR, PRETHR, FJTHR	These registers set the "threshold values" of all the ports. To set the threshold value of a 16-bit counter, write the low-order eight bits of the value and then the high-order eight bits into this register. For a 24-bit counter, write the low-order eight bits, middle-order eight bits, and high-order eight bits. When the host accesses this register for write, which of the low-order or high-order eight bits are written is indicated by the SYSPR register.
Write pointer register SYSPR	Indicates which of the low-order, middle-order, or high-order eight bits the host writes next to each threshold register.
Time register FRMN	Sets time (cycle) of monitoring. Counters are reset at a set cycle. The default value of this register is all zeros and cycle setting is disabled.

3.4 Frame Overhead Insert/Drop Function

The μPD98411 has an insert/drop register in the byte area of the following frame overhead and can transmit any value to the transmit frame or read a value stored into the receive frame.

Table 3-12. Insert/Drop Registers

Byte		Transmission Side			Reception Side	
		Register Name	Default	Insert Condition	Register Name	Drop Condition
SOH	J0	J0T	01(H)	Always valid	J0R	The updating of registers is stopped if OOF is detected, and the value before detection is retained.
	1st Z0	Z0#1T	02(H)		Z0#1R	
	2nd Z0	Z0#2T	03(H)		Z0#2R	
	F1	F1T	00(H)		F1R	
	E1	E1T	00(H)		E1R	
	D1-D3	DsecT	00(H)		DsecR	
LOH	SS	MDR1	00(b)	Valid except when pseudo frame PLOP or PLOP II is transmitted	None	
	H1	H1T	00(H)	Valid only when pseudo frame PLOP II is transmitted	H1R	
	H2	H2T	00(H)		H2R	
	H3	H3T	00(H)		H3R	
	B2	B2T	00(H)	Valid only when pseudo frame PB2 II is transmitted	B2R	
	K1	K1T	00(H)	Valid only when the TAPS bit of the CMR1 register is set	K1R	
	K2	K2T	00(H)		K2R	
	D4-D12	DlineT	00(H)	Always valid	DlineR	
	S1	S1T	00(H)		S1R	
	1st Z2	Z2#1T	00(H)		Z2#1R	
	M1	None	None		M1R	
	E2	E2T	00(H)	Always valid	E2R	
POH	J1	J1T	00(H)		J1R	When OOF, LOP, or Path AIS is detected, the updating of the register is stopped, and the value before detection is retained.
	C2	C2T	13(H)		C2R	
	B3	B3T	00(H)	Valid only when pseudo frame PB3 II is transmitted	B3R	
	G1	None	None		G1R	
	F2	F2T	00(H)	Always valid	F2R	
	H4	H4T	00(H)		H4R	
	Z3-Z5	Z345T	00(H)		Z345R	

★ **Remark** Setting the MGM bit of the MDR2 register to 1 switches the functions of the reception-side drop registers Z2#1R and B3R. See **(3)** in **Section 3.4**.

(1) Insert register

The value set in an insert register is stored to the specific overhead byte position and transmitted. Unless the register value is changed, the default value of the insert register is stored and transmitted.

- When the PLOS frame of the pseudo frame is transmitted, the setting of all the insert registers is ignored, and all 0 is transmitted.
- Priority of byte having multiple setting conditions

(a) H1, H2, and H3 bytes (pointer-related)

Priority	Setting	Contents of H1, H2, and H3
<1>	Pseudo error LOS frame transmission (CMR3 register)	→ All 0 transmission
<2>	Command Path AIS alarm transmission (CMR1 register)	→ All FF transmission
<3>	Pseudo error LOP II frame transmission (CMR3 register)	→ Transmission of H1T, H2T, and H3T registers' value
<4>	Pseudo error LOP frame transmission (CMR3 register)	→ FF, FF, FF, FE, FE, FE, FF, FF, FF

(b) K2 byte

Priority	Setting	Contents of K2
<1>	Pseudo error LOS frame transmission (CMR3 register)	→ All 0 transmission
<2>	APS byte transmission (CMR1 register: TAPS bit = 1)	→ Transmission of K1T and K2T byte registers' value
<3>	Command Line AIS alarm transmission (CMR1 register)	→ Sixth through eighth bits of K2 byte = 111
<4>	Command Line RDI alarm transmission (CMR1 register)	→ Sixth through eighth bits of K2 byte = 110

If the TAPS bit of the CMR1 register is set, the K2T register becomes valid, and the transmission commands of Line AIS and Line RDI are ignored.

(2) Drop register

The contents of the overhead of a receive frame are stored to the corresponding drop register and are updated for each frame. By reading the drop register, the value of the byte area stored into the receive overhead can be determined.

- In the OOF status, not all the drop registers are updated. The registers are kept updated unless the OOF status is set.
- In the LOP or Path AIS status, the drop register of POH is not updated. It is kept updated in a status other than LOP or Path AIS.

★ **(3) Number of protection stages related to the receive Z2#1 byte and the interrupt notification function**

Setting the MGM bit of the MDR2 register to 1 switches the functions related to storing of the receive 1st Z2 byte in a register.

<1> The Z2#1R register functions as the Z2_6R register.

<2> The B3R register functions as the Z2_12R register.

<3> The functions of the D7:Z2_6 and D6:Z2_12 bits of the PCOCR2 register are enabled.

<4> The functions of the D7:Z2_6m and D6:Z2_12m bits of the PCOMR2 register are enabled.

(a) Operations of the Z2_6 and Z2_6m bits of the Z2_6R register

<1> The μPD98411 monitors the dd bits (bits 6 and 7) of the receive 1st Z2 byte. If it receives the same dd bit value six times consecutively since the dd bits have changed for the first time, it stores the contents of the receive 1st Z2 byte to the Z2_6R register.

	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	bit 8	
Receive 1st Z2 byte	×	×	×	×	×	d	d	×	×: don't care

<2> When the same dd bit value has been received seven or more times, the Z2_6R register is not updated.

<3> If the same dd bit value is received six times consecutively since the dd bits have changed after the sixth occurrence of the previous same dd bit value, the Z2_6R register is updated to the new contents of the receive 1st Z2 byte.

<4> The Z2_6R register need not be updated while the received dd bits are '00' once the μPD98411 is put in the current mode. It is updated when the μPD98411 receives a value other than '00' at the dd bits six times consecutively.

<5> When the Z2_6R register is updated, the D7:Z2_6 bit of the PCOCR2 register is set to 1.

<6> If the Z2_6 bit is set to 1, it can make the interrupt signal PHINT_B active, thus enabling an interrupt to detect that the Z2_6R register has been updated.

<7> Setting the D7:Z2_6m bit of the PCOMR2 register can mask the interrupt that is based on the Z2_6 bit of the PCOCR2 register.

<8> The Z2_6 bit of the PCOCR2 register is cleared to 0 when it is read-accessed.

(b) Operations of the Z2_12 and Z2_12m bits of the Z2_12R register

<1> The μPD98411 monitors the mm bits (bits 7 and 8) of the receive 1st Z2 byte. If it receives the same mm bit value 12 times consecutively since the mm bits have changed for the first time, it stores the contents of the receive 1st Z2 byte to the Z2_12R register.

	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	bit 8	
Receive 1st Z2 byte	×	×	×	×	×	×	m	m	×: don't care

<2> When the same mm bit value has been received thirteen or more times, the Z2_12R register is not updated.

<3> If the same mm bit value is received 12 times consecutively since the mm bits have changed after the twelfth occurrence of the previous same mm bit value, the Z2_12R register is updated to the new contents of the receive 1st Z2 byte.

<4> When the Z2_12R register is updated, the D6:Z2_12 bit of the PCOCR2 register is set to 1.

<5> If the Z2_12 bit is set to 1, it can make the interrupt signal PHINT_B active, thus enabling an interrupt to detect that the Z2_12R register has been updated.

<6> Setting the D6:Z2_12m bit of the PCOMR2 register can mask the interrupt that is based on the Z2_12 bit of the PCOCR2 register.

<7> The Z2_12 bit of the PCOCR2 register is cleared to 0 when it is read-accessed.

Remark Specification X newly supports the function stated in **(3)**. Specification P or E does not support it.

3.5 Alarm Report I/O Pins (PALM, CMD)

3.5.1 PALM[2:0] Output Pins

Each port has three general-purpose output pins (PALM). The output levels of these pins can be changed in accordance with the setting of the bits in the CMR1 register.

These pins can be also set so that they are automatically driven high when the port detects a failure or alarm. One or more events to be reported are assigned to each pin. To do this, three registers, **AMPR**, **AMR1**, and **AMR2**, are used.

(Assigning event to **PALM** pin)

<1> Specify PALM0 to PALM2 pin to be set to the AMPR register.

<2> Unmask the bit corresponding to the event to be reported to the AMR1 and AMR2 registers.

<3> Repeat the above procedure for each pin.

Table 3-13 shows the events that can be selected with the AMR1 and AMR2 registers.

Table 3-13. PALM Pin Report Events

Reported Item	PALM Output Timing
CMD1, CMD2, CMD3	The PALM pin goes high when the CMD1 to CMD3 bits of the CMR1 register are set to 1. The PALM pin can also be used as general-purpose output port pin.
exCMD	The PALM pin goes high when it has been detected that the external CMD input pin has gone high.
OOL, LOS, OOF, LOF, LOP, OCD, LCD, Line AIS, Path AIS, Line RDI, Path RDI	The PALM pin goes high when an event has been detected and is kept high until the cause of the event is removed.

★ <<Example of using the **PALM** pin>>

Example 1: Specifying to output a high level from the PALM1 pin when the μPD98411 detects a LOS or LOF condition in port 0

<1> Write '01H' to the AMPR register (024H) : The PALM1 pin is selected.

<2> Write 'DEH' to the AMR1 register (025H) : The LOS and LOF masks are cleared.

<3> Write 'FFH' to the AMR2 register (026H) : The default setting is maintained (no mask is cleared).
(If it is specified to clear a mask for two or more sources, their OR result is output.)

Example 2: Specifying to output a high level from the PALM0 pin of port 2 when software sets the CMD2 bit of the CMR1 register to 1

<1> Write '00H' to the AMPR register (124H).

<2> Write 'FFH' to the AMR1 register (125H): The default setting is maintained (no mask is cleared).

<3> Write 'BFH' to the AMR2 register (126H): The CMD2 bit is unmasked.

3.5.2 CMD Input Pins

Each port has a general-purpose input pin, CMD, that inputs a status signal from a peripheral LSI. The level input to this pin is reflected on the **exCMD** bit of the **PICR** register of each port. When a high level is input to the bit, the bit is set to 1. The setting of this bit can be used as an interrupt cause.

3.5.3 SD Input Pins

The SD pin inputs the Signal Detect signal of the optical link module that is connected to the line side as a ★ transceiver. Each port has one SD pin. Using this pin requires resetting the SDm bit of the IACM register to 0. When the input to this pin goes low, the port enters a LOS detection status, and sets the LOS bit of the PICR register. Fix this pin at a high level when it is not used.

3.6 Switching Mode of Alarm Detection Conditions

As an option, a mode in which the alarm detection condition can be changed is supported. The setting of the alarm detection condition is changed by using the ITU bit of the ITUR register. Table 3-14 lists the alarms whose detection condition can be changed, together with their conditions.

Table 3-14. Alarm Whose Detection Condition Can Be Changed

Alarm	ITU Bit = 0 (Default)	ITU Bit = 1
Line RDI	**Five** consecutive receptions of a frame for which byte K2 (sixth to eighth bits) = 110	**Three** consecutive receptions of a frame for which byte K2 (sixth to eighth bits) = 110
Path RDI	**Five** consecutive receptions of a frame for which byte G1 (fifth bit) = 1	**Three** consecutive receptions of a frame for which byte G1 (fifth bit) = 1
Line AIS	**Five** consecutive receptions of a frame for which byte K2 (sixth to eighth bits) = 111	**Three** consecutive receptions of a frame for which byte K2 (sixth to eighth bits) = 111

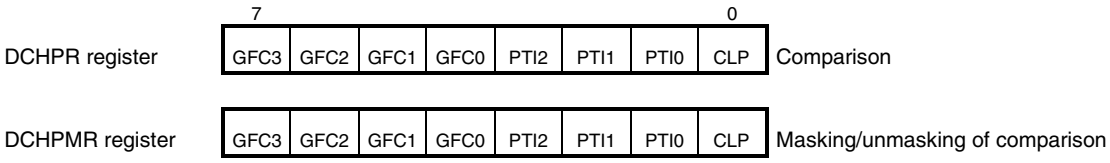
3.7 Selecting Invalid Cell

3.7.1 Selecting Drop Invalid Cell

When the VPI/VCI field detects a cell containing all zeros in the received cell stream, the cell is regarded as being an invalid cell. This cell is compared with the set values of the DCHPR and DCHPMR registers in the other header area. If the cell coincides with the register values, the cell is not stored into the receive FIFO but is dropped. If the cell does not coincide, it is not dropped but is stored into the receive FIFO and output from the UTOPIA interface.

In this way, idle cells and unassigned cells can be dropped or passed together. In default mode, only the idle cell is dropped.

Figure 3-15. DCHPR and DCHPMR Registers



<1> Set a bit pattern to be dropped in the DCHPR register.

<2> Clear the bit of the DCHPMR register whose value is to be compared with the corresponding bit of the DCHPR register.

If the VPI/VCI field detects a cell containing all zeros, the cell is compared with the bits of the DCHPR register that correspond to the bits of the DCHPMR register that are zero. If the cell coincides with the bits, it is dropped.

Table 3-15. Example of Setting the DCHPR Register

DCHPR CLP Bit	DCHPMR CLP Bit	Dropped Cells
1	0	Idle cells (default)
0	0	Unassigned cells
×	1	Both idle and unassigned cells

3.7.2 Selecting Transmission Invalid Cell

If the valid cell data in the transmit FIFO runs short of one cell, an idle cell is inserted. Depending on the setting of the register, the transmission invalid cell can be changed from an idle cell to an unassigned cell. This can be done by using the UCS bit of the AVLC register.

Table 3-16. Format of Invalid Cell Transmitted by μPD98411

Setting	Inserted Cell	Format					
		GFC	VPI	VCI	PTI	CLP	Payload
UCS = 0	Idle cell	0	0	0	0	1	All 6A(H)
UCS = 1	Unassigned cell	0	0	0	0	0	All 6A(H)

3.8 Loopback Function

The three types of loopback modes listed in Table 3-17 are supported. These modes can be selected by using the **LP[1:0]** bits of the **MDR2** register.

Table 3-17. Loopback Function (1/2)

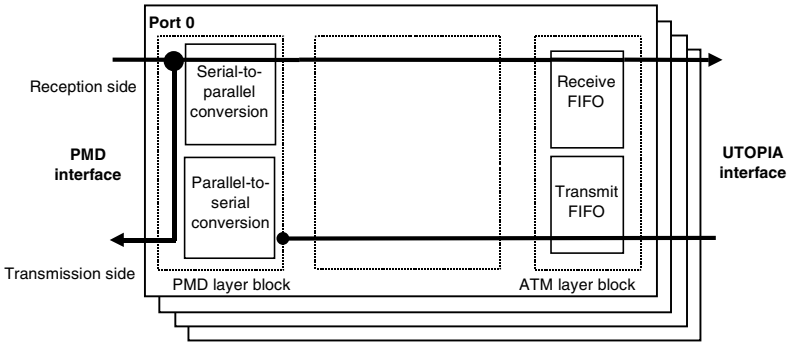
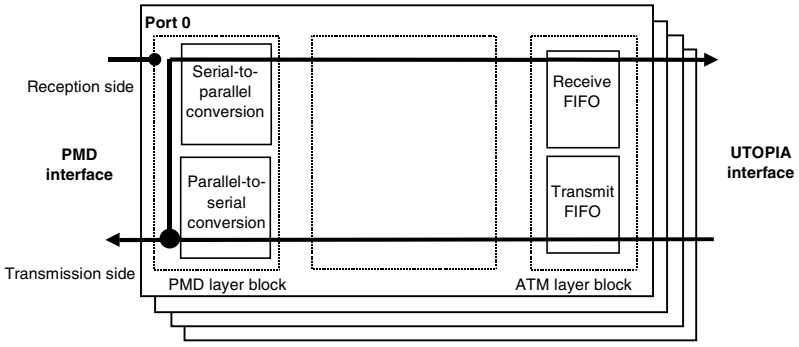
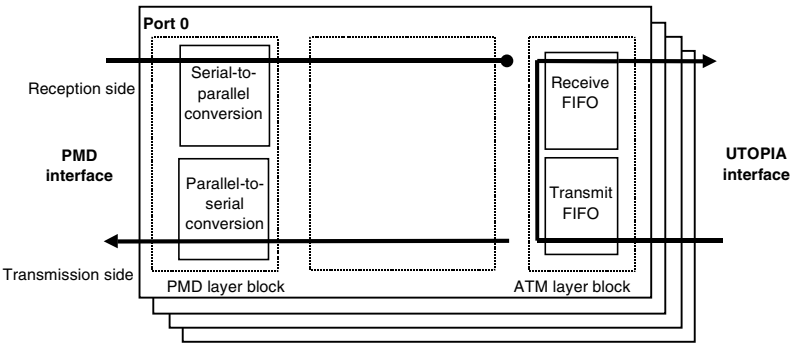
LP[1:0]	Mode
00	Normal mode
01	**RPLP mode** In this mode, the data input from the reception side of the PMD interface is returned by a serial/parallel converter block and output from the transmission side of the PMD interface. The received data is also processed normally and output from the UTOPIA interface. Because the transmission block also performs its processing normally up to the serial/parallel converter block, the transmission side of the UTOPIA interface receives the cell normally, but it is not transmitted to the line side. 
10	**TPLP mode** The transmit cell data received from the UTOPIA interface is processed up to the serial/parallel converter block, is returned there, and output from the reception side of the UTOPIA interface. The failure or alarm detection status that is reflected on the PICR register indicates the status of the transmit data that is returned. The transmit data is also output from the PMD interface normally. In this mode, the data input to the reception side of the PMD interface is ignored. 

Table 3-17. Loopback Function (2/2)

LP[1:0]	Mode
11	**ALP mode** The transmit cell received from the UTOPIA interface is output from the UTOPIA interface as a return receive cell immediately after the transmit FIFO of the ATM layer block. At this time, idle cells or unassigned cells are successively output from the PMD interface, in accordance with the setting of the **USC** bit of the **AVLC** register. The failure or alarm detection status reflected on the PICR register is the status of the receive data input to the PMD interface. 

★ **Cautions 1. When a loopback test is conducted by disconnecting the reception line cable and placing the μPD98411 in the TPLP loopback mode with LOS detection enabled, cells that are input to the μPD98411 pass through it and are looped back at the reception UTOPIA interface. Note that these cells are not counted by the Information Cell counter, which is intended to count receive cells. This is because the specification states that all performance monitoring counters are to be kept from counting while LOS detection is under way.**

★ **2. Allow at least 3.5 μs between the time when a port enters the ALP mode and the time when it exits the ALP mode.**

★ **3. Do not set the TDIS bit of the CMR2 register for a port to 1 (transmission disabled) when the port is in the ALP mode.**

★ **4. If the ALP mode is entered/exited when the receive FIFO is full (holding 8 cells), the status bit for reporting a receive FIFO overflow may be set, resulting in the FIFO Full counter being incremented even when no cell is dropped. Clear the status bit and counters if they indicate incorrect information.**

CHAPTER 4 INTERFACES

4.1 UTOPIA Interface

The UTOPIA interface transfers transmit/receive cell data to a device in the high-order ATM layer. The interface between the μPD98411 and the ATM layer conforms to "MPHY Data Path Operation" of the "UTOPIA Level 2 version 1.0 June '95" standard.

4.1.1 Signals

(1) Transmit interface

The transmit interface uses the signal lines defined below.

TCLK2, TCLK1: Each is a transmit clock signal of 8 MHz to 50 MHz, supplied by the ATM layer. All data transfer operations through the transmit interface are executed in sync with this clock signal.

TADD2[4:0]-TADD1[4:0]: Each is a 5-bit address, used to select a port from the ATM layer. Bit TADD[4] is the MSB. As the address, the value set via the management interface into the **PHYIDR** register of each port is used. The same address is used for both transmission and reception. The setting of 31 (1FH) is prohibited.

TDI[15:0]: Data signal which is used by the ATM layer to transfer transmit cell data to the μPD98411. Bit TDI[15] is the MSB, while bit TDI[0] is the LSB.

TSOC2, TSOC1: Each is a signal indicating the start of cell location for cell data flowing in TDI[15:0].

TENBL2_B, TENBL1_B: Each is a signal indicating that the ATM layer is supplying a valid data output to TDI[15:0] in the current clock cycle.

TCLAV3-TCLAV0: Active-High, tristate signals which are output by the μPD98411 to the ATM layer. The port selected by the address in the TADD[4:0] signal is driven by the next clock to the output address.

The selected port is driven high when it can accept a cell data. Otherwise, it is driven low.

TPR2, TPR1: Each is an odd parity signal of TDI[15:0], input in sync with the data. The μPD98411 verifies this parity bit. If an error is detected, the **UT** bit of the **IMST** register is set to 1.

(2) Receive interface

The receive interface uses the signal lines defined below.

RCLK2, RCLK1: Each is a receive clock signal of 8 MHz to 50 MHz, supplied by the ATM layer. All data transfer operations through the receive interface are executed in sync with this clock signal.

RADD2[4:0]-RADD1[4:0]: Each is a 5-bit address, used to select a port of the μPD98411 from the ATM layer. Bit RADD[4] is the MSB. As the address, the value set into the **PHYIDR** register of each port is used. The same address is used for both transmission and reception. The setting of 31 (1FH) is prohibited.

RDO[15:0]: Tristate data signals used by the μPD98411 to transfer receive data to the ATM layer. Bit RDO[15] is the MSB while bit RDO[0] is the LSB. RDO[15:0] is driven only while the RENBL_B signals are active.

RSOC2, RSOC1: Tristate signals indicating the start position of the cell data flowing on RDO[15:0]. These signals are output in synchronization with the first byte of the cell output by the μPD98411. They are driven only when the RENBL signal is active.

RENBL2_B, RENBL1_B: Each is an enable signal. Used by the ATM layer to enable the RDO[15:0] and RSOC signals of the μPD98411.

RCLAV3-RCLAV0: Active-high tristate signals output by the μPD98411 to the ATM layer. A port selected by an address on the RADD[4:0] signals is driven in the clock cycle next to the address. The selected port is driven high when it has one or more cells of data to be transferred to the receive FIFO; otherwise, it will be driven low.

RPR2, RPR1: Each is an odd parity signal of RDO[15:0]. This signal supports tristates and the μPD98411 drives it only while the corresponding RENBL_B signal is active.

4.1.2 Modes

In the default status that arises when the power is applied, the UTOPIA interface is disabled. To enable the interface and start transmitting cells, set a mode by using the registers related to the UTOPIA interface in the following sequence:

Setting (after H/W, S/W Reset)	Register
<1> Disable receive block (4 ports).	CMR2 register RDIS = 1
<2> Set PHY address and enable address (4 ports).	PHYIDR register
<3> Set response timing of CLAV signal (if it is necessary to change the setting).	AVLC register
<4> Set UTOPIA interface mode and enable bus.	MltUT register
<5> Enable receive block (4 ports).	CMR2 register RDIS = 0

The receive block is temporarily disabled (in **<1>**) because, if garbage data is stored in the receive FIFO as a result of receiving an unstable frame at power application, the receive FIFO should be reset, to prevent the garbage data from being output after the UTOPIA interface has been enabled.

To set a mode (in **<3>** and **<4>** above), the following parameters must be set.

Table 4-1. UTOPIA Interface Modes

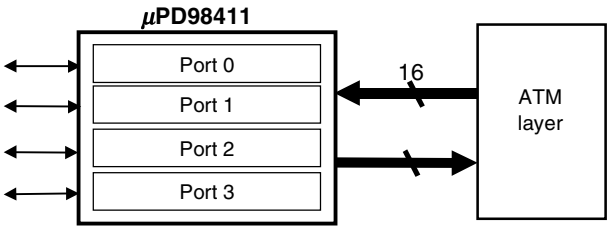
	Classification	Item	Related Register and Bit Name
1	Setting related to bus	Single 16-bit or Dual eight-bit or Single eight-bit	MltUT register MSL[1:0]
2	Setting related to cell available signal	1 × TCLAV/1RCLAV or 4 × TCLAV/1RCLAV	MltUT register MSL2
3		Timing at which transmit cell available signal becomes valid	AVLC register TCAC
4		Setting of threshold value reported by transmit cell available signal	AVLC register AVC[2:0]
5		Timing at which receive cell available signal becomes valid	AVLC register RCAC
6		PHY address decoding method	MltUT register MSL3

★ **Caution Once cell transfer has started on the UTOPIA interface, do not change or set the MltUT register.**

(1) Setting related to bus

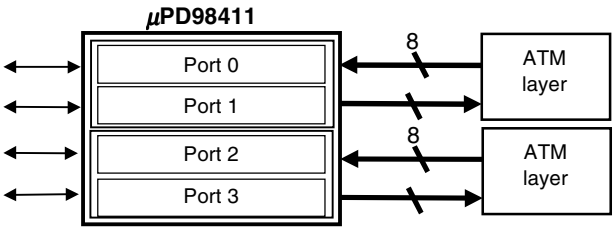
(a) Single 16-bit (MltUT register MSL = 11)

In this mode, the cell data for all the four ports is transferred via a 16-bit bus. The maximum transmission rate is 800 Mbps (16 bits × 50 MHz).



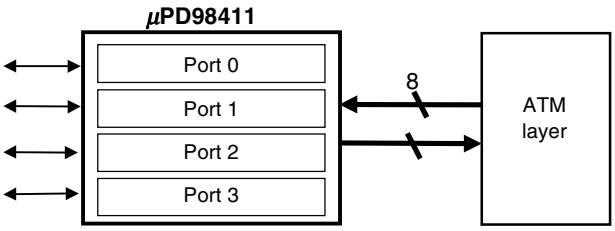
(b) Dual eight-bit (MltUT register MSL[1:0] = 01)

In this mode, an eight-bit data bus is used for two ports. Ports 0 and 1 use one eight-bit bus for transfer, and ports 2 and 3 uses another eight-bit bus. Each port operates independently.



(c) Single eight-bit (MltUT register MSL[1:0] = 10)

In this mode, the cell data for all the four ports is transferred via an eight-bit data bus. Because the maximum transmission rate is 400 Mbps (eight bits × 50 MHz), the transmit frames of all the four ports cannot be filled with cells.



The format of a cell on the eight-bit and 16-bit data buses is as shown below.

Single eight-bit/Dual eight-bit mode

7 — 0
Header1
Header2
Header3
Header4
HEC
Payload1
:
:
Payload47
Payload48

Single 16-bit mode

15	0
Header1	Header2
Header2	Header4
HEC	'XX'
Payload1	Payload2
Payload3	Payload4
Payload5	Payload6
:	:
:	:
Payload45	Payload46
Payload47	Payload48

'XX': Dummy byte "00" is inserted at the reception side. At the transmission side, the byte at this position is internally ignored and overwritten to HEC.

(2) Setting related to cell available signal

(a) Allocating cell available signal to port

(i) Using 1 × TCLAV/RCLAV [MltUT register MSL2 = 0]

The FIFO status of the four ports is multiplexed in the one cell available signal and reported. The cell available signal is used as a tristate output signal. Only the port that is addressed at polling drives the cell available signal and returns a response.

- In single 16-bit bus mode: Only the TCLAV2/RCLAV1 pair is used.
- In dual eight-bit bus mode: Ports 0 and 1 use TCALV1 and RCLAV1.
  Ports 2 and 3 use TCLAV2 and RCLAV2.
- In single eight-bit bus mode: The TCLAV1/RCLAV2 signal pair is used.

(ii) Using 4 × TCLAV/RCLAV [MItUT register MSL2 = 1]

All cell available signals TCLAV3 through TCLAV0 and RCLAV3 through RCLAV0 are enabled. A pair of TCLAV#n and RCLAV#n is assigned to each port (example: TCLAV0 and RCLAV0 → port 0, TCLAV2 and RCLAV2 → port 2). The relationship between the port numbers and signal numbers does not change.

When MSL3 = 0, two-state output is enabled during which TCLAV and RCLAV always indicate the FIFO statuses of their respective ports regardless of the address specification. The ATM layer device can directly obtain the FIFO state without the need to specify the address (**Direct Status Indication (DSI) method**).

When MSL3 = 1, the cell available signal is used as a tristate output signal and only that port whose address is specified drives the cell available signal and returns a response.

(b) Timing at which port receiving cell makes transmit cell available signal active

(i) Valid four cycles before the tail of cell [AVLC register TCAC = 0 (default)]

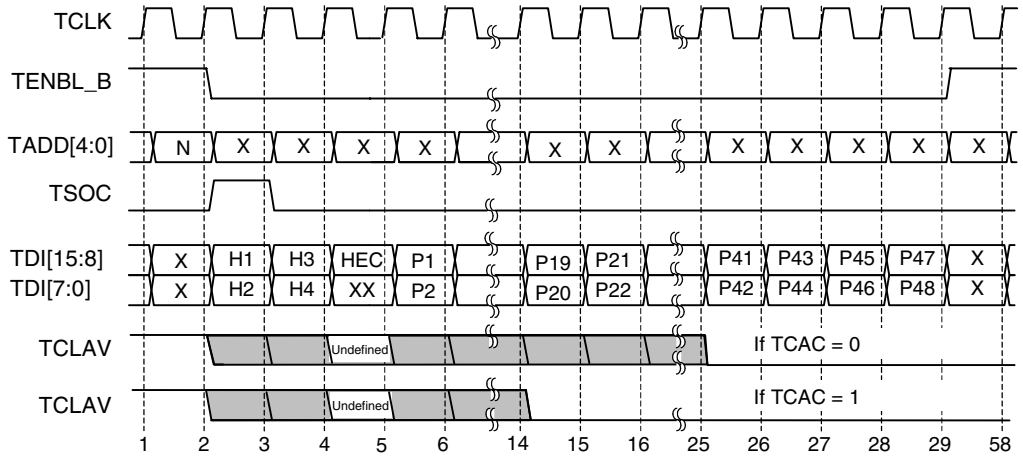
The port that is receiving a cell makes TCLAV valid four clock cycles before the tail of the cell currently being received. If the transmit FIFO has a vacancy to store one cell in addition to the currently received cell, TCLAV is held high; if the FIFO does not have a vacancy, TCLAV goes low.

(ii) Report after transmitting 20th byte [AVLC register TCAC = 1]

The port that is receiving a cell makes TCLAV valid after it has received the 20th byte of the cell currently being received. If the transmit FIFO has a vacancy to store one cell in addition to the currently received cell, TCLAV is held high; if the FIFO does not have a vacancy, TCLAV goes low.

Figure 4-1. TCLAV Change Timing

(Example in 16-bit bus direct status mode)



★ **(c) Setting conditions for changing the transmit cell available signal (AVLC register AVC[2:0])**

In the descriptions about TCLAV signal operations in (b) above, the transmit FIFO vacant area condition (underscored) under which the TCLAV signal changes can be altered.

Specify n where n is the size (in cells) of the transmit FIFO vacant area used as a criterion in making the TCLAV signal inactive.

The default setting is 000 (1 cell). This setting specifies that, when the transmit FIFO becomes full with the cells that are currently being received, that is, the size of the vacant area becomes smaller than one cell, the TCLAV signal is to become low.

If 011 (3 cells) is specified, the TCLAV signal becomes low when the sixth cell is written to the FIFO whose size is 8 cells, that is, when the size of the vacant area becomes smaller than 3 cells.

AVC2-AVC0	Number of Cells of Transmit FIFO Vacant Area
000-001	1 cell (default)
010	2 cells
011	3 cells
100	4 cells
101	5 cells
110	6 cells
111	7 cells

This setting changes the threshold value condition of the transmit FIFO that causes TCLAV to go low. If cells continue to be transferred even when TCLAV goes low, they are received by the transmit FIFO that has a capacity of eight cells, until the FIFO is full. Cells that are transferred once the FIFO is full are ignored.

(d) Timing at which a port transferring cell makes a receive cell available signal valid

(i) Keeping RCLAV high up to last byte of a cell [AVLC register: RCAC = 0]

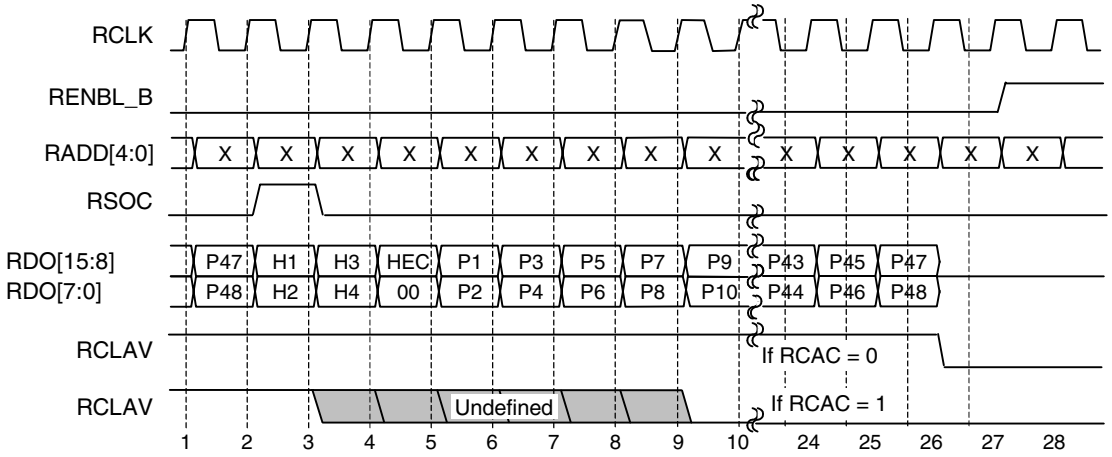
While receive cell data is being output, RCLAV is held high. If the receive FIFO has valid data consisting of one or more cells at the clock next to that at which the last byte of the transferred cell (48th byte of the payload data) has been output, RCLAV goes high; otherwise, it goes low.

(ii) Seven cycles after transfer of last cell [AVLC register: RCAC = 1]

If the data in the receive FIFO runs short by one cell as a result of transferring cells, cell transmission is started and RCLAV goes low seven clock cycles later.

★ **Figure 4-2. RCLAV Change Timing**

(Example in 16-bit bus direct status mode)



(e) PHY address decoding method

(i) Checking all five address bits [MItUT register: MSL3 = 0]

When the ATM layer polls the FIFO status of each port, the port with all five bits of the address signals coinciding drives the TCLAV/RCLAV signal. Similarly, the port with the five address bits coinciding is selected when the ATM layer selects a port that transfers cells.

(ii) Checking only high-order three bits of address [MItUT register: MSL3 = 1]

The port with its high-order three bits coinciding with ID4 through ID2 of the PHYIDR register and the low-order two bits of addresses TADD and RADD ignored drives TCLAV and RCLAV during polling **(Multiplexed Status Polling (MSP) method)**.

When the ATM layer selects a port that transfers cells, a port with all the five bits of the address coinciding is selected.

In this case, even if MSL2 = 1, TCLAV and RCLAV function as tristate output signals that are driven only by the port with its high-order three bits coinciding with its own address during polling.

By using the above modes, the UTOPIA interface can be organized in various ways as your application system requires. The operations in a selected mode are described in **Section 4.1.3**.

Table 4-2. UTOPIA Interface Modes

MSL[3:0]	Bus Mode	Method Used to Obtain State	CLAV Signal Used	CLAV Output
0001	Dual eight-bit	2TCLAV/2RCLAV	2 × TCLAV/RCLAV	Tristate
0101		Direct Status Indication	4 × TCLAV/RCLAV	Two-state
1001		Multiplexed Status Polling	1 × TCLAV/RCLAV	Tristate
1101			4 × TCLAV/RCLAV	
0010	Singe eight-bit	1TCLAV/1RCLAV	1 × TCLAV/RCLAV	Tristate
0110		Direct Status Indication	4 × TCLAV/RCLAV	Two-state
1010		Multiplexed Status Polling	1 × TCLAV/RCLAV	Tristate
1110			4 × TCLAV/RCLAV	
0011	Single 16-bit	1TCLAV/1RCLAV	1 × TCLAV/RCLAV	Tristate
0111		Direct Status Indication	4 × TCLAV/RCLAV	Two-state
1011		Multiplexed Status Polling	1 × TCLAV/RCLAV	Tristate
1111			4 × TCLAV/RCLAV	

Note that the pins to be used differ depending on the mode selected for the UTOPIA interface. Table 4-3 shows the correspondence between each mode and the pins used.

Table 4-3. Correspondence between UTOPIA Interface Modes and Pins Used (1/2)

Mode		MSL[3:0]	Pins Used (_B is omitted)		
Dual eight-bit	2TCLAV/2RCLAV	0001	Tx	Port 0/1	TCLK1, TDI[15:8], TADD1, TPR1, TENBL1_B, TCLAV1, TSOC1
				Port 2/3	TCLK2, TDI[7:0], TADD2, TPR2, TENBL2_B, TCLAV2, TSOC2
			Rx	Port 0/1	RCLK1, RDO[15:8], RADD1, RPR1, RENBL1_B, RCLAV1, RSOC1
				Port 2/3	RCLK2, RDO[7:0], RADD2, RPR2, RENBL2_B, RCLAV2, RSOC2
	Direct Status Indication Using 4TCLAV/4RCLAV signals (two-state outputs)	0101	Tx	Port 0/1	TCLK1, TDI[15:8], TADD1, TPR1, TENBL1_B, TCLAV0, TCLAV1, TSOC1
				Port 2/3	TCLK2, TDI[7:0], TADD2, TPR2, TENBL2_B, TCLAV2, TCLAV3, TSOC2
			Rx	Port 0/1	RCLK1, RDO[15:8], RADD1, RPR1, RENBL1_B, RCLAV0, RCLAV1, RSOC1
				Port 2/3	RCLK2, RDO[7:0], RADD2, RPR2, RENBL2_B, RCLAV2, RCLAV3, RSOC2
	Multiplexed Status Polling Using 1TCLAV/1RCLAV signal (tristate outputs)	1001	Tx	Port 0/1	TCLK1, TDI[15:8], TADD1, TPR1, TENBL1_B, TCLAV1, TSOC1
				Port 2/3	TCLK2, TDI[7:0], TADD2, TPR2, TENBL2_B, TCLAV2, TSOC2
			Rx	Port 0/1	RCLK1, RDO[15:8], RADD1, TPR1, RENBL1_B, RCLAV1, RSOC1
				Port 2/3	RCLK2, RDO[7:0], RADD2, TPR2, RENBL2_B, RCLAV2, RSOC2
	Multiplexed Status Polling Using 4TCLAV/4RCLAV signals (tristate outputs)	1101	Tx	Port 0/1	TCLK1, TDI[15:8], TADD1, TPR1, TENBL1_B, TCLAV0, TCLAV1, TSOC1
				Port 2/3	TCLK2, TDI[7:0], TADD2, TPR2, TENBL2_B, TCLAV2, TCLAV3, TSOC2
			Rx	Port 0/1	RCLK1, RDO[15:8], RADD1, RPR1, RENBL1_B, RCLAV0, RCLAV1, RSOC1
				Port 2/3	RCLK2, RDO[7:0], RADD2, RPR2, RENBL2_B, RCLAV2, RCLAV3, RSOC2
Single eight-bit	1TCLAV/1RCLAV	0010	Tx	TCLK1, TDI[15:8], TADD1, TPR1, TENBL1_B, TCLAV1, TSOC1	
			Rx	RCLK2, RDO[7:0], RADD2, RPR2, RENBL2_B, RCLAV2, RSOC2	
	Direct Status Indication Using 4TCLAV/4RCLAV signals (two-state outputs)	0110	Tx	TCLK1, TDI[15:8], TADD1, TPR1, TENBL1_B, TCLAV0-TCLAV3, TSOC1	
			Rx	RCLK2, RDO[7:0], RADD2, RPR2, RENBL2_B, RCLAV0-RCLAV3, RSOC2	
	Multiplexed Status Polling Using 1TCLAV/1RCLAV signal (tristate outputs)	1010	Tx	TCLK1, TDI[15:8], TADD1, TPR1, TENBL1_B, TCLAV1, TSOC1	
			Rx	RCLK2, RDO[7:0], RADD2, RPR2, RENBL2_B, RCLAV2, RSOC2	
	Multiplexed Status Polling Using 4TCLAV/4RCLAV signals (tristate outputs)	1110	Tx	TCLK1, TDI[15:8], TADD1, TPR1, TENBL1_B, TCLAV0-TCLAV3, TSOC1	
			Rx	RCLK2, RDO[7:0], RADD2, RPR2, RENBL2_B, RCLAV0-RCLAV3, RSOC2	

Table 4-3. Correspondence between UTOPIA Interface Modes and Pins Used (2/2)

Mode		MSL[3:0]	Pins Used (_B is omitted)	
Single 16-bit	1TCLAV/1RCLAV	0011	Tx	TCLK2, TDI[15:0], TADD2, **TPR1**, TENBL2_B, TCLAV2, **TSOC1**
			Rx	RCLK1, RDO[15:0], RADD1, **RPR2**, RENBL1_B, RCLAV1, **RSOC2**
	Direct Status Indication Using 4TCLAV/4RCLAV signals (two-state outputs)	0111	Tx	TCLK2, TDI[15:0], TADD2, **TPR1**, TENBL2_B, TCLAV0-TCLAV3, **TSOC1**
			Rx	RCLK1, RDO[15:0], RADD1, **RPR2**, RENBL1_B, RCLAV0-RCLAV3, **RSOC2**
	Multiplexed Status Polling Using 1TCLAV/1RCLAV signal (tristate outputs)	1011	Tx	TCLK2, TDI[15:0], TADD2, **TPR1**, TENBL2_B, TCLAV2, **TSOC1**
			Rx	RCLK1, RDO[15:0], RADD1, **RPR2**, RENBL1_B, RCLAV1, **RSOC2**
	Multiplexed Status Polling Using 4TCLAV/4RCLAV signals (tristate outputs)	1111	Tx	TCLK2, TDI[15:0], TADD2, **TPR1**, TENBL2_B, TCLAV0-TCLAV3, **TSOC1**
			Rx	RCLK1, RDO[15:0], RADD1, **RPR2**, RENBL1_B, RCLAV0-RCLAV3, **RSOC2**

4.1.3 Operations

This section explains the following three operations to be performed, depending on the mode selected for the cell available signal.

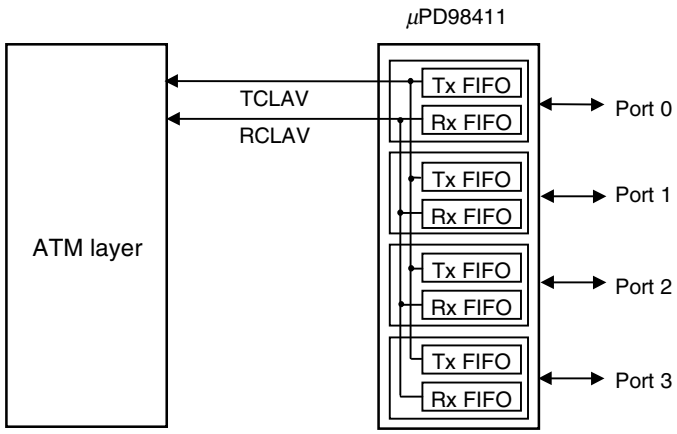
<1> 1TCLAV & 1RCLAV method
<2> Direct Status Indication method
<3> Multiplexed Status Polling method

In the following explanation, the use of single eight-bit mode is assumed.

(1) 1TCLAV & 1RCLAV method

In 1TCLAV & 1RCLAV mode, the status signal of the transmit/receive FIFO of each of the four ports is internally multiplexed with one pair of TCLAV and RCLAV signals for output. The ATM layer repeatedly performs polling by specifying the address of a port and sampling TCLAV and RCLAV to check the FIFO status of the port. Only that port whose address is specified drives the TCLAV and RCLAV signal according to the FIFO status; otherwise, the signals enter the high-impedance state.

Figure 4-3. 1TCLAV & 1RCLAV Method



(a) Transmit interface with 1TCLAV

The ATM layer outputs the address of a port onto TADD and samples the level of the TCLAV signal in the next clock cycle. Each port checks whether the address on TADD coincides with the port address. If the addresses coincide, the port drives the TCLAV signal in the clock cycle next to that in which the address has been output. If the transmit FIFO has a vacancy and can accept cell data, the TCLAV signal is driven high; if the FIFO cannot accept cell data, the signal is driven low. If the addresses do not coincide, the TCLAV signal enters the high-impedance state. The size of the vacancy in the transmit FIFO depending on which a response to the TCLAV signal is issued can be changed by using the AVC2 through AVC0 bits of the AVLC register. The ATM layer repeats this polling operation to check the FIFO status of each port.

The address of a port is the address set via a management interface into the **PHYIDR** register of the port (note that address 31 (1FH) cannot be set because it is used as an address value for none of the ports).

★ The ATM layer selects one of the ports that have returned a response indicating that they are ready to accept a cell, outputs the address of the port onto TADD, and makes TENBL_B low in the next clock cycle. Immediately before TENBL_B goes low, the port whose address coincides with the address output onto TADD in the last clock cycle in which the signal was high is selected. The selected status of the port lasts from the cycle in which the address is output onto TADD and TENBL_B goes low until TENBL_B goes low again and another port is selected.

After selecting a port, the ATM layer starts the transfer of cell data. The μPD98411 samples and inputs TDI at the rising edge of TCLK, assuming that valid data is output to TDI while TENBL_B is low. It stops inputting the data when TENBL_B goes high. The data input in the cycle in which a high level was input to TSOC is recognized as being the beginning of a cell.

While transferring cell data, the ATM layer performs polling again to select the port to which cell data is to be transferred next.

Figure 4-4 shows an example of a series of cycles in which polling is performed and cell transfer is started when two or more μPD98411s are connected, in single eight-bit mode, to one ATM layer device. In this example, the ATM layer device transfers a cell to the port of address (N). If it is found, as a result of polling, that the ports of addresses (N - 3) and (N + 3) are ready to accept cells next and therefore return a response to the ATM layer device, port (N + 3) is selected at edge 16. When cell transfer to port (N + 3) is started, the ATM layer restarts polling.

Figure 4-4. Transmission Timing in 1TCLAV & 1RCLAV Method

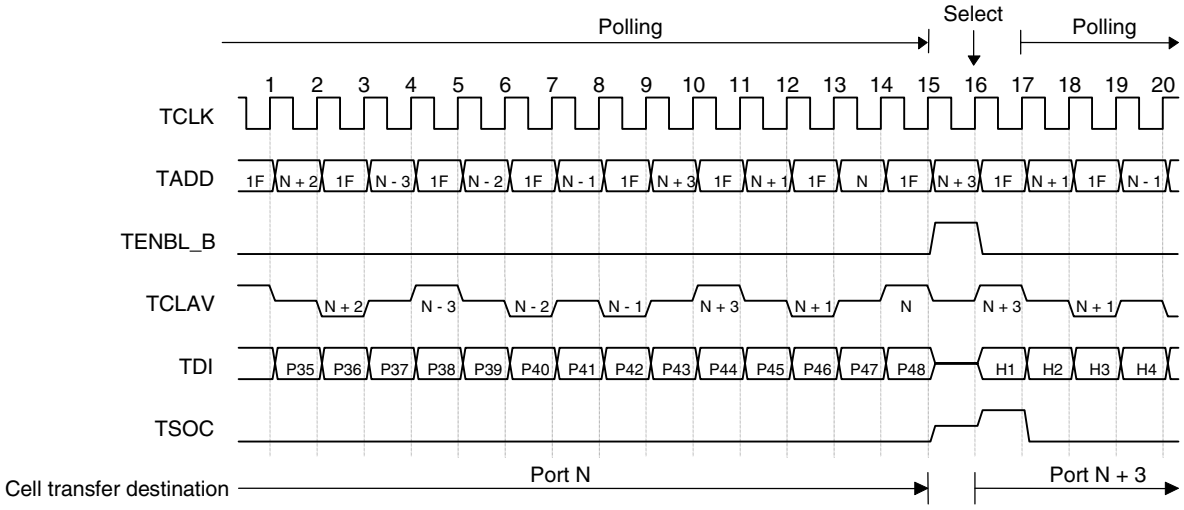
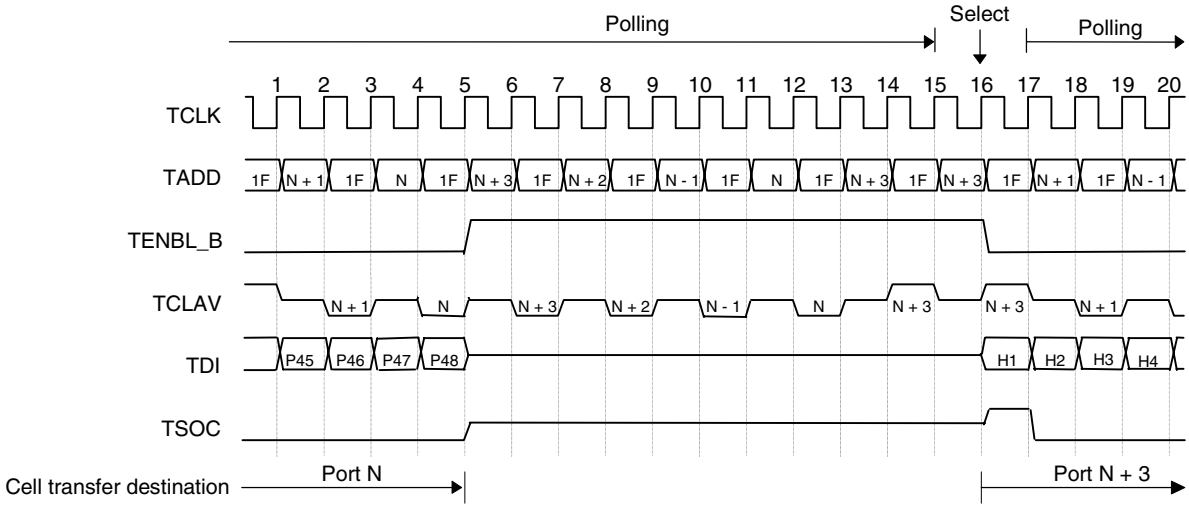


Figure 4-5 shows an example in which all the ports drive TCLAV low during polling, returning a response indicating that they are not ready to receive cells. As a result, cell transfer is stopped for a while. The ATM layer device continues polling even when it does not transfer cells.

Because port (N + 3) is ready to accept cells at edge 15, the ATM layer device outputs address (N + 3) at edge 16 to select the port, makes TENBL_B low, and then restarts cell transfer.

Figure 4-5. Interruption and Restart of Cell Transmission



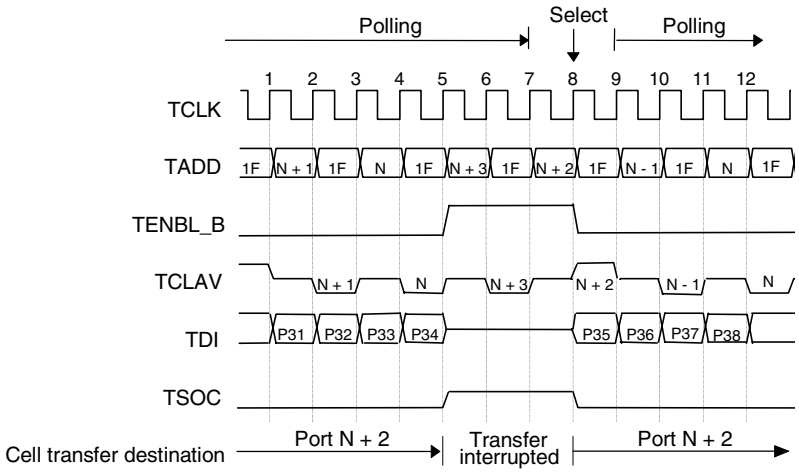
★ **Cautions 1. Figure 4-6 shows an example in which the ATM layer device makes TENBL_B high and stops data output. With the μPD98411, avoid stopping cell transfer midway as shown in this example. If cell transfer has been started once by making TENBL_B low, keep TENBL_B low until all 53 bytes of the cell have been completely transferred.**

TENBL_B control cannot be used to suspend or resume data input during the transfer of one cell.

2. If a high level is input to TSOC before the cell being transferred reaches 53 bytes after cell transfer has been started because TENBL_B went low, transfer of the cell is discontinued and the part already received is dropped by the transmit FIFO as an invalid short cell.

★ **3. Even if TENBL_B is held low after 53 bytes of a cell have been transferred, the μPD98411 regards only the first 53 bytes as being a valid cell. It ignores the data of the 54th byte and those that follow.**

Figure 4-6. Interruption of Cell Transmission (Failure)



(b) Receive interface with 1RCLAV

The ATM layer outputs the address of a port to RADD and samples RCLAV in the next clock cycle to poll the receive FIFO status of the port. Each port checks whether the address on RADD coincides with its own address. If the addresses coincide, the port drives RCLAV in the clock cycle next to that in which the address was output to RADD. If the port has valid data of one or more cells in its receive FIFO, it drives RCLAV high; otherwise, the port drives the signal low. If the addresses do not coincide, RCLAV enters the high-impedance state.

The address of a port is the address set via the management interface to the PHYIDR register of the port. The address set in the PHYIDR register is used by the port for both transmission and reception via the UTOPIA interface (note that address 31 (1FH) cannot be set because it is used as an address value of none of the ports). The ATM layer device repeats polling to check the receive FIFO status of each port.

The ATM layer selects one of the ports that have returned a response indicating that they have a valid cell, outputs the address of the port onto RADD, and makes RENBL_B low in the next clock cycle. Immediately before RENBL_B goes low, the port whose address coincides with the address output onto RADD in the last clock cycle in which the signal was high is selected. The selected status of the port lasts from the cycle in which the address is output onto RADD and RENBL_B goes low until RENBL_B goes low again and another port is selected.

When a port is selected, it starts transferring cell data to the ATM layer device. While RENBL_B is low, the port outputs data to RDO in synchronization with the RCLK clock. When RENBL_B goes high, the port stops output, and RDO enters the high-impedance state. In the cycle in which the first byte of the cell data is output, RSOC also goes high.

When the transfer of cell data has been started, the ATM layer device restarts polling to select the next port.

Figure 4-7 shows an example of a series of cycles in which polling is performed and cell transfer is started when two or more μPD98411s are connected, in single eight-bit mode, to one ATM layer device. In this example, it is reported that ports having addresses (N - 3) and (N + 3) have valid cells, as a result of polling conducted while port (N) was transferring a cell. Consequently, the ATM layer device selects port (N + 3) at edge 16. The selected port (N + 3) starts transferring a cell. In the cycle in which the first byte of the cell is output, RSOC also goes high. The ATM layer device continues polling.

Figure 4-7. Reception Timing in 1TCLAV & 1RCLAV Method (1)

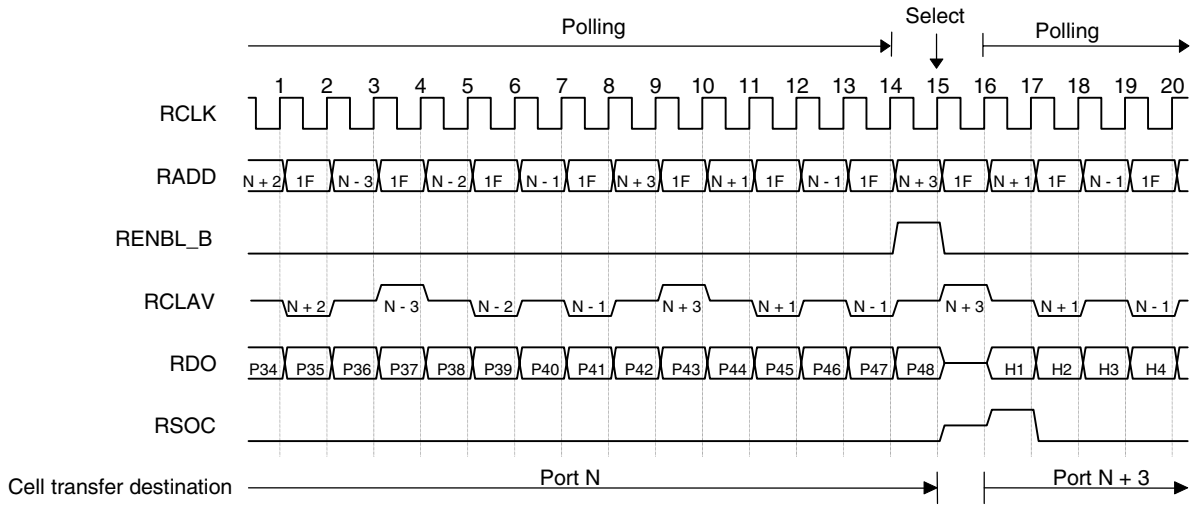


Figure 4-8 shows an example in which cell transfer from port (N) has been completed but none of the ports has valid data to be transferred. Because the ATM layer device does not have to select a port, port (N) remains selected. However, because port (N) has no more cells to be transferred, it drives RSOC low and does not output valid data to RDO. The ATM layer device assumes that the next cell is not transferred and returns RENB_B high because RSOC does not go high at edge 9.

When the μPD98411 detects the high level of RENBL_B, RSOC and RDO enter the high-impedance state in the next clock cycle.

Figure 4-8. Reception Timing in 1TCLAV & 1RCLAV Method (2)

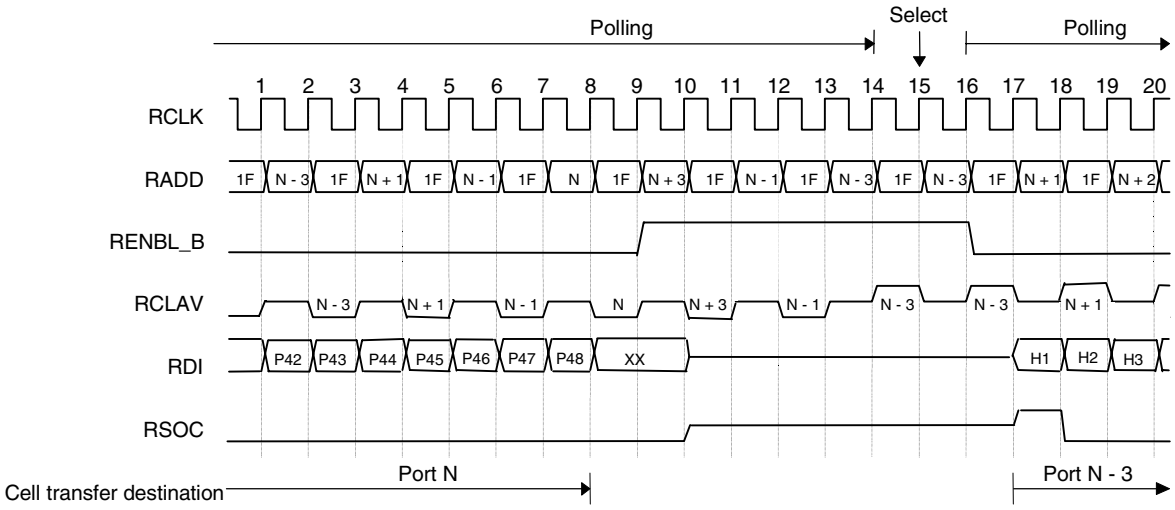


Figure 4-9 shows an example in which a valid cell to be transferred is generated again one clock cycle after port (N) has completed the transfer of the current cell. At edge 8, immediately after the port (N) has completed transferring one cell, the port does not transfer another cell because it has no more cells. At edge 9, one clock cycle after, however, the next cell is generated in the receive FIFO of port (N). The port therefore outputs the first H1 byte of the cell to RDO and drives RSOC high. The ATM layer returns RENBL_B high once, assuming that no more cells are transferred because port (N) does not drive RSOC high at edge 9. However, it detects, at edge 10, that port (N) has started data output, and therefore, selects port (N) again.

The μPD98411 (selected port) updates RDO at the rising edge of RCLK and samples RENBL. In the cycle after the low level of RENBL_B has been detected, RSOC and RDO are driven. If they are high, RSOC and RDO enter the high-impedance state. The ATM layer device inputs RSOC and RDO until the edge next to that at which RENBL_B has been driven high.

Figure 4-9. Continuous Transmission of Two Cells from the Same Port (1)

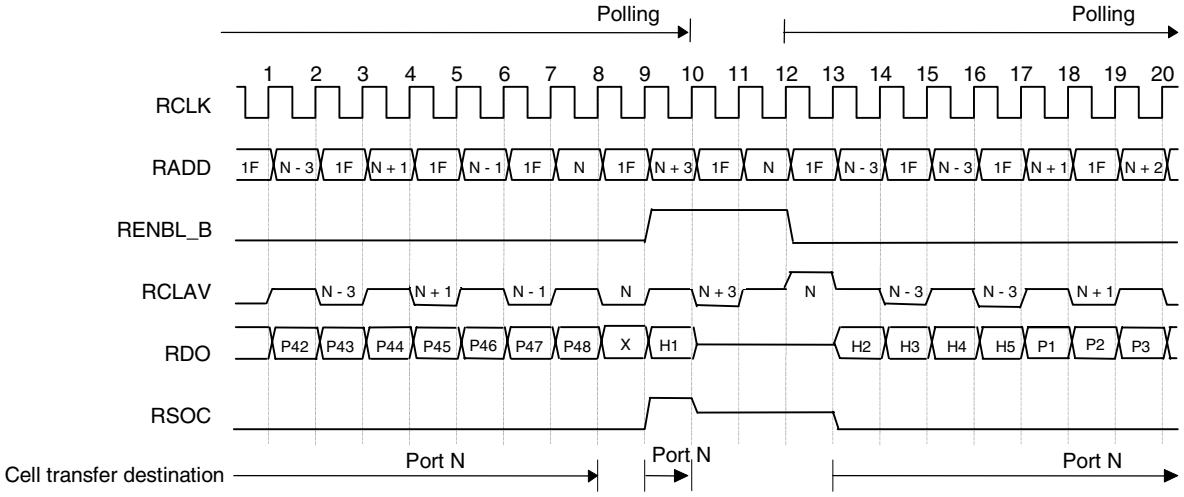


Figure 4-10 is an example in which two cells are successively transferred from the same port. When port (N) has completed the transfer of the first cell, the ATM layer device keeps selecting port (N) because the other ports do not assert RCLAV active. In the normal mode, a port transferring a cell keeps RCLAV high up to the last byte of the cell. Therefore, the ATM layer device cannot determine whether the port has more valid cells in the receive FIFO until the device reaches the last byte of the cell. In this example, port (N) actually has one more cell in the receive FIFO so successively transfers the second cell. The ATM layer device learns that the cells are successively transferred because RSOC goes high at edge 9.

The μPD98411 successively transfers cells as shown in Figure 4-10 if multiple cells are in the receive FIFO and RENBL_B remains selected at the low level. To prevent a port from successively transferring cells, RENBL_B is used for control.

The timing at which the μPD98411 drives RCLAV high or low can be changed by using the RCAC bit of the AVLC register. See **(d)** in **Section 4.1.2**.

Figure 4-10. Continuous Transmission of Two Cells from the Same Port (2)

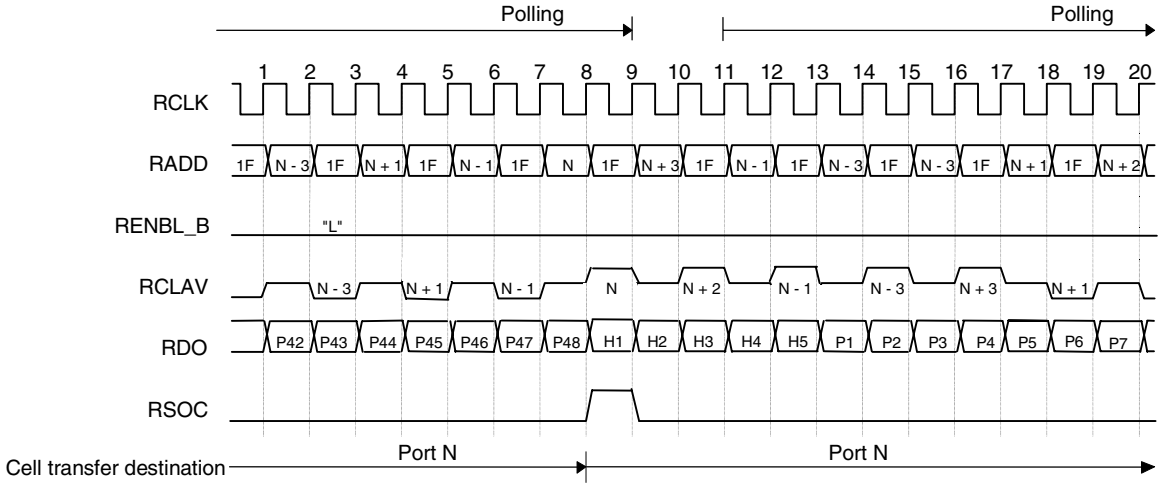
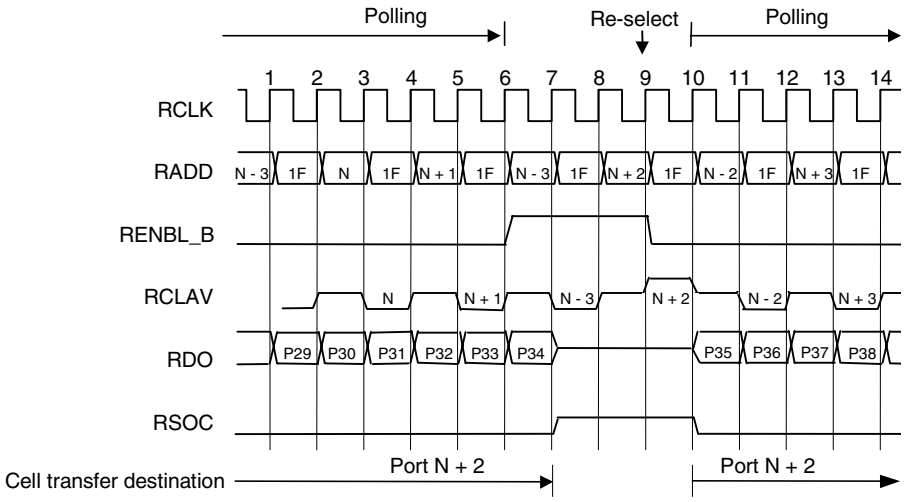


Figure 4-11 shows an example in which cell transfer from port (N + 2) is stopped for the duration of three clock cycles because the ATM layer device returns RENBL_B high. The ATM layer device must select this port by outputting the same port address before driving RENBL_B low.

The μPD98411 (selected port) stops cell transfer by making RSOC and RDO enter the high-impedance state when it has detected that RENBL_B has been driven high, even during cell transfer.

Figure 4-11. Stopping Receive Cell Transfer by ATM Layer Device

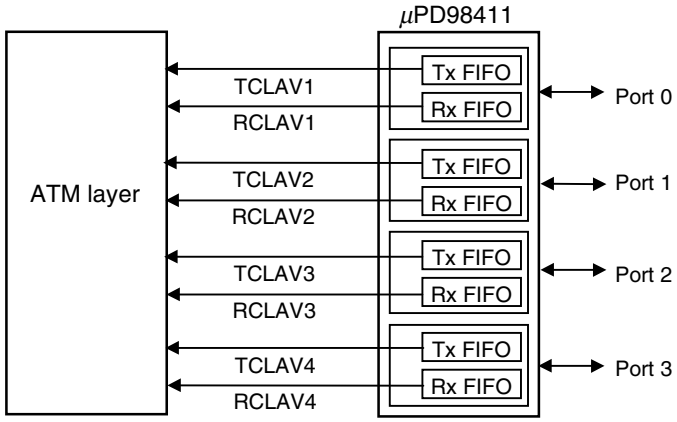


(2) Direct Status Indication (DSI) method

In the DSI method, the four ports use an independent TCLAV/RCLAV pair. The TCLAV and RCLAV signals of each port indicate the status of the transmit and receive FIFOs of the port. Because the ATM layer device can directly check the status of the FIFO by checking the signal levels of TCLAV and RCLAV of the port in question at any time, it does not have to perform polling, unlike in the 1TCLAV & 1RCLAV method described in (1) above. The address lines are used only to select a cell transfer destination or cell transfer source port.

To select a port, the address of the port is output to TADD or RADD while TENBL_B or RENBL_B is high, in the same manner as in the 1TCLAV & 1RCLAV method, and TENBL_B or RENBL_B is driven low in the next clock cycle.

Figure 4-12. Direct Status Indication Method



(a) DSI method transmit interface

Figure 4-13 shows an example of the operation of the transmit interface with the DSI method. In this example, addresses 1 to 4 are set to ports 0 to 3, respectively.

First, all the ports drive TCLAV low, indicating that a new cell cannot be accepted. Therefore, the ATM layer device does not transfer a cell. Port 0 drives TCLAV high at rising edge 2 of TCLK, thus indicating to the ATM layer device that it is ready to receive a cell. The ATM layer device detects this at edge 3, outputs address 1 to TADD, and drives TENBL_B low at the next clock cycle to select port 0. Port 0 detects its own address at TADD in the last cycle in which TENBL_B is high, and enters the select status. The ATM layer device then starts transferring a cell.

At edge 4, TCLAV of port 2 also goes high. At edge 52, port 0 drives TCLAV low, indicating that it cannot accept the next cell.

With the μPD98411, the timing at which TCLAV becomes valid can be changed by using the TCAC bit of the **AVLC** register. See **(b)** in **Section 4.1.2 (2)**.

At edge 58, port 2 is selected instead of port 0. Therefore, TENBL_B is driven high, address 3 is output to TADD, and then TENBL_B is driven low again.

To select a port, the ATM layer device outputs a port address to TADD in the last high cycle in which TENBL_B goes low from high.

Figure 4-13. Example of Transmission Timing in DSI Method (1)

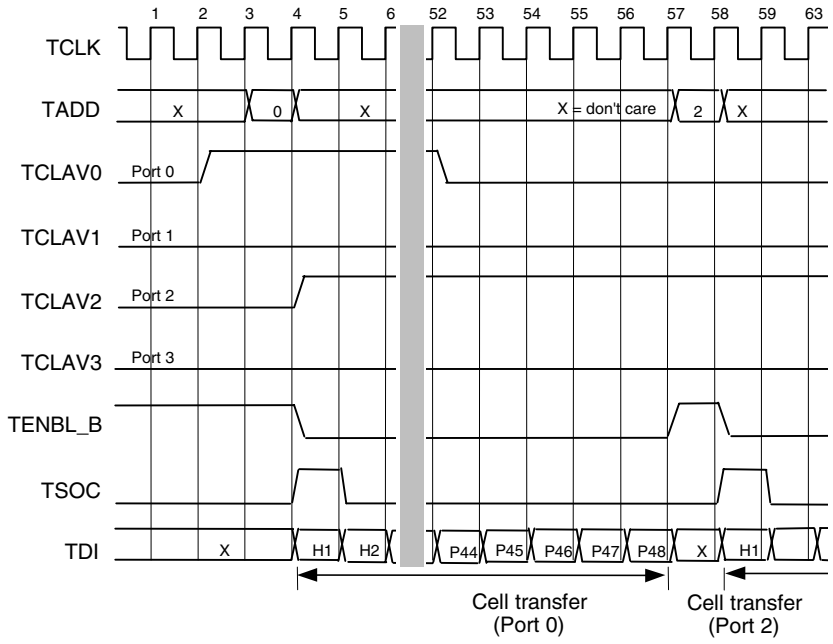
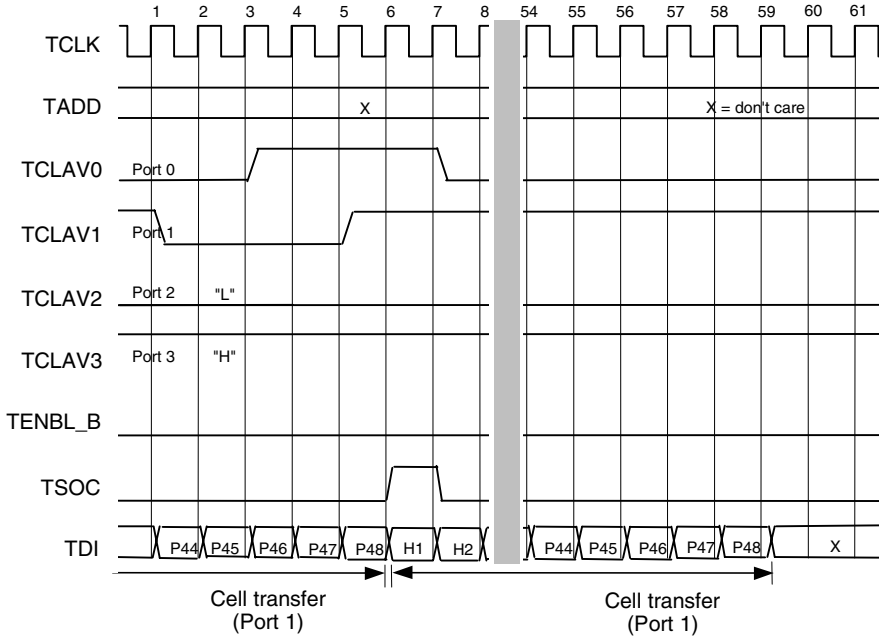


Figure 4-14 shows an example in which the ATM layer device successively transfers cells to port 1. The ATM layer device has learned, at edge 6 immediately before transfer of the first cell is completed, that port 1 can receive more cell. Therefore, it starts transferring the second cell to the port while TENBL_B remains low.

Figure 4-14. Example of Transmission Timing in DSI Method (2)



(b) DSI method receive interface

Figure 4-15 shows an example of the operation of the receive interface in the DSI method. In this example, addresses 1 to 4 are set to ports 0 to 3, respectively.

The ATM layer device monitors all four RCLAV signals and detects that RCLAV of port 0 has gone high at rising edge 3. To select port 0, the ATM layer device outputs the address of port 0 to RADD and drives RENBL_B low. Port 0 is selected and starts transmitting a cell because its address is output to RADD in the cycle before RENBL_B goes low.

At edge 5, the ATM layer device detects that RCLAV of port 2 has gone high. After it has received a cell from port 0, the ATM layer device drives RENBL_B high, outputs address 3 to RADD, and then drives RENBL_B low again to select port 2.

Even after cell transmission from port 2 has been completed, the RCLAVs of the other ports are not high. Consequently, the ATM layer device keeps selecting port 2 and holds RENBL_B low. As a result, port 2 successively transmits the second cell. Even after the second cell has been transmitted, the other ports do not drive their RCLAVs high and therefore, the selected port is not changed. However, because port 2 does not transmit a third cell, the ATM layer device drives RENBL_B high again at edge 166.

Figure 4-15. Example of Reception Timing in DSI Mode (1)

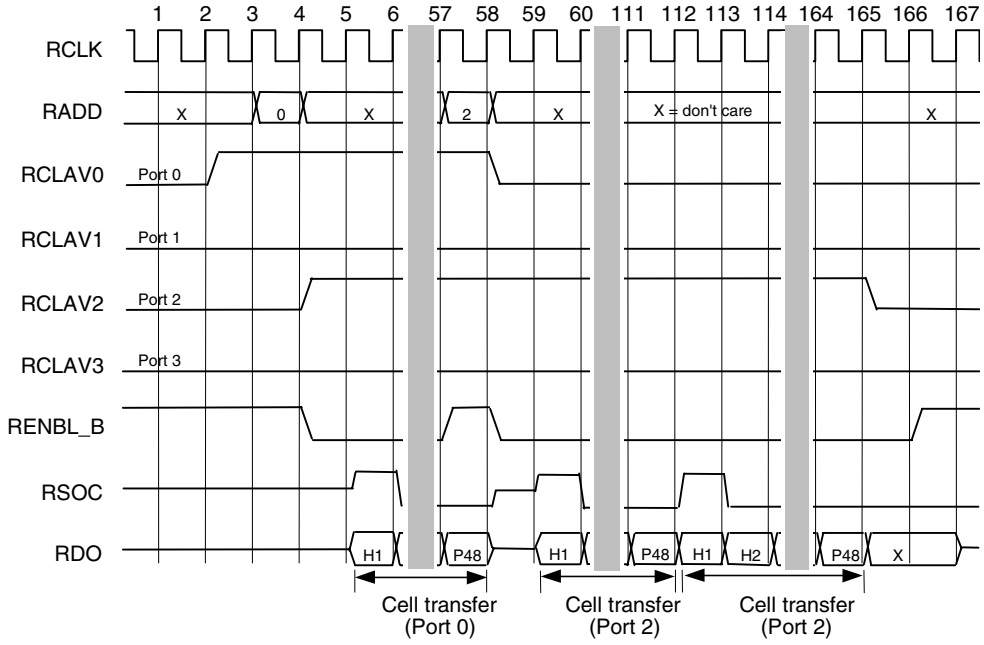
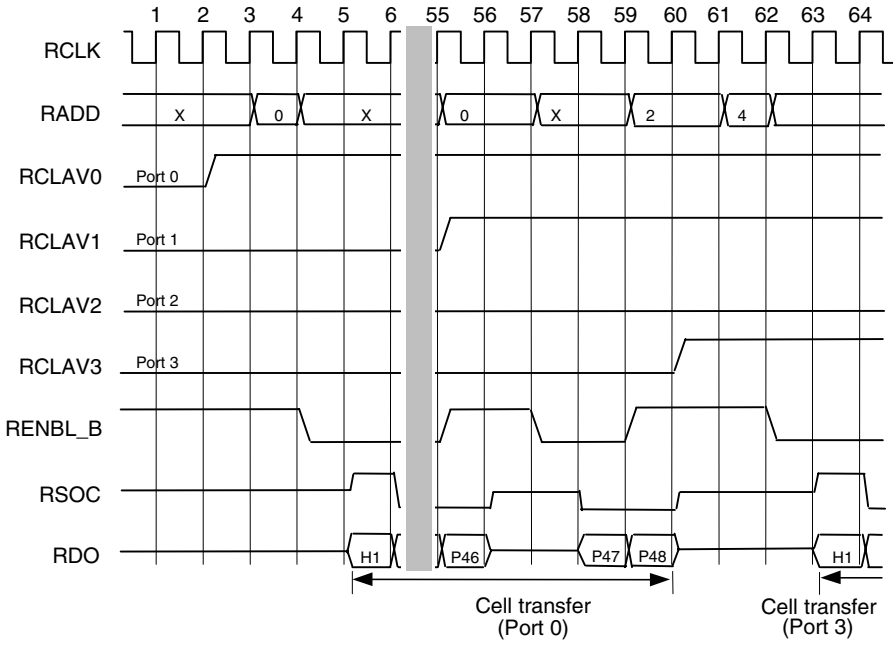


Figure 4-16 shows that the ATM layer device drives RENBL_B high to stop cell transfer while port 0 is transferring a cell. The ATM layer device can issue a request to the μPD98411 to stop cell transfer by making RENBL_B high. The μPD98411 samples RENBL_B at the rising edge of the RCLK clock. When it detects that RENBL_B has gone high, RDO enters the high-impedance state in the next cycle and cell transfer is stopped. The ATM layer device outputs the address of port 0 to RADD to select port 0 again before it drives RENBL_B low again.

In this example, the ATM layer device controls the priority of the port to be selected. Because the ATM layer device detects, at edge 56, that RCLAV of port 1 has gone high, it drives RENBL_B high and outputs address 2 to select port 1 once cell transfer from port 0 has been completed. Before the ATM layer device drives RENBL_B low, however, it detects at edge 61 that RCLAV of port 3 has gone high. Therefore, the ATM layer device changes the address on RADD to 4 and selects port 3.

Figure 4-16. Example of Reception Timing in DSI Mode (2)



(3) Multiplexed Status Polling (MSP) method

In the MSP method, the ATM layer device specifies an address and performs polling to check the transmit/receive FIFO status of each port, in the same manner as in the 1TCLAV & 1RCLAV method. In the MSP method, the ATM layer device can check the status of multiple ports by performing polling only once when the ATM layer device is connected to many ports.

★ To set the MSP mode, set the MSL3 bit of the MltUT register to 1. When this bit is set, a port whose high-order three address bits coincide with the high-order three bits on the address lines responds to polling from the ATM layer, and the low-order two bits are ignored. However, all the five bits of the address specified to transfer cell data are checked.

(a) Example of using MSP mode

An example of connecting eight μPD98411s to one ATM layer device to control a total of 31 ports is shown below. Port addresses 0H to 1EH are set for ports 0 to 30, respectively.

Tables 4-4 and 4-5 classify the 31 ports into two groups. In Table 4-4, the ports whose addresses are the same in the low-order two bits are classified as a group (grouping A). One pair of TCLAV and RCLAV is assigned to each group classified in grouping A and multiplexed. Table 4-5 classifies the ports having the same high-order three bits of the port address into one group (grouping B). Therefore, these high-order three bits are used as a group address.

The ATM layer device outputs the group address (high-order three bits of an address) onto an address to perform polling. In MSP mode, each port of the μPD98411 checks only the high-order three bits on the address lines. The port whose address coincides with the address on the address lines drives TCLAV and RCLAV in the clock cycle next to the one in which the address was put on the address lines for polling. The ATM layer identifies the responding port by recognizing the group (in grouping A) to which the driven TCLAV and RCLAV signals are assigned. The ATM layer device can obtain the statuses of four ports by performing polling once.

Table 4-4. Grouping According to Lower Two Bits of Port Addresses (Grouping A)

CLAV Signal to Be Allocated	Port Address	Lower 2 Bits
RCLAV0	0, 4, 8, 12, 16, 20, 24, 28	XXX00
RCLAV1	1, 5, 9, 13, 17, 21, 25, 29	XXX01
RCLAV2	2, 6, 10, 14, 18, 22, 26, 30	XXX10
RCLAV3	3, 7, 11, 15, 19, 23, 27	XXX11
TCLAV0	0, 4, 8, 12, 16, 20, 24, 28	XXX00
TCLAV1	1, 5, 9, 13, 17, 21, 25, 29	XXX01
TCLAV2	2, 6, 10, 14, 18, 22, 26, 30	XXX10
TCLAV3	3, 7, 11, 15, 19, 23, 27	XXX11

Table 4-5. Grouping According to Higher Three Bits of Port Addresses (Grouping B)

Port Address	Group No.	Group Address
0, 1, 2, 3	0	000XX
4, 5, 6, 7	1	001XX
8, 9, 10, 11	2	010XX
12, 13, 14, 15	3	011XX
16, 17, 18, 19	4	100XX
20, 21, 22, 23	5	101XX
24, 25, 26, 27	6	110XX
28, 29, 30	7	111XX

X = don't care

(b) Example of connection in MSP mode

Figure 4-17 shows an example of transmission direction where eight μPD98411s are connected and 31 ports are connected to one ATM layer device. Each μPD98411 sets the MSL2 and MSL3 bits of the MltUT register to 1, allocates a TCLAV/RCLAV pair to each port, and multiplexes TCLAV and RCLAV of the ports having the same low-order two bits of the address.

★ **Caution If the MSL2 bit of the MltUT register is set to 1 to assign a TCLAV/RCLAV pair to each port, port#n is assigned with TCLAV#n and RCLAV#n having the same #n (Example: A pair of TCLAV0 and RCLAV0 is assigned to port 0, and a pair of TCLAV3 and RCLAV3 is assigned to port 3). It is impossible to change the relationships between the port number and the number of the TCLAV and RCLAV signals. When using the μPD98411 in MSP mode, therefore, keep in mind that some port addresses can be assigned only to specific ports.**

The following addresses can be set up:

Port 0: #00, #04, #08, ... (the low-order two bits are 00)
Port 1: #01, #05, #09, ... (the low-order two bits are 01)
Port 2: #02, #06, #0A, ... (the low-order two bits are 10)
Port 3: #03, #07, #0B, ... (the low-order two bits are 11)

The following addresses cannot be assigned:

Port 0 = #00, #01, #08
Port 1 = #04, #02, #07
Port 2 = #08, #03, #06
Port 3 = #0C, #04, #05

Figure 4-17. Connection in MSP Mode (1) (Transmission) (μPD98411 × 8)

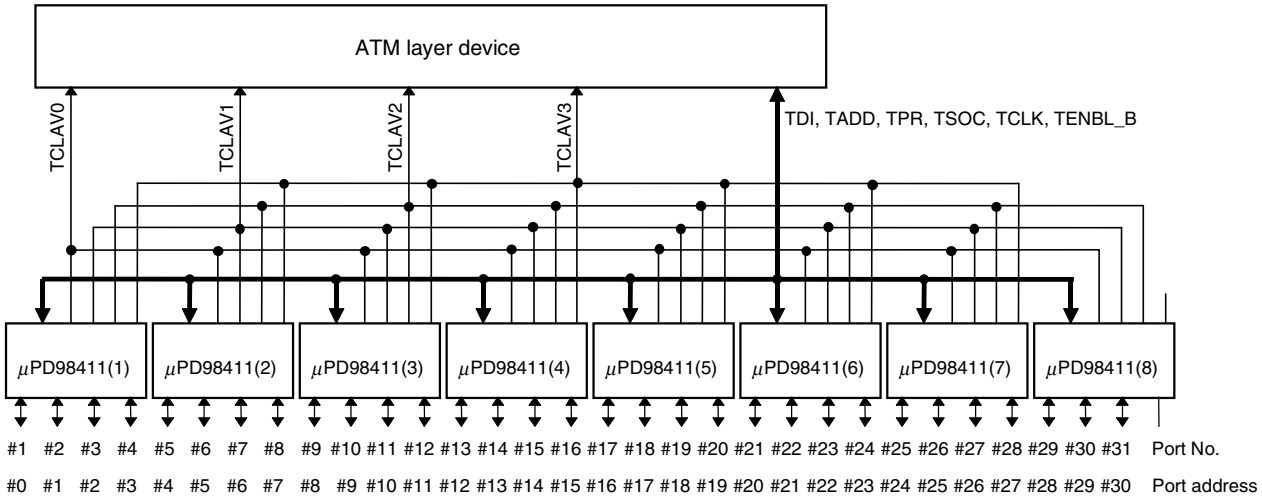
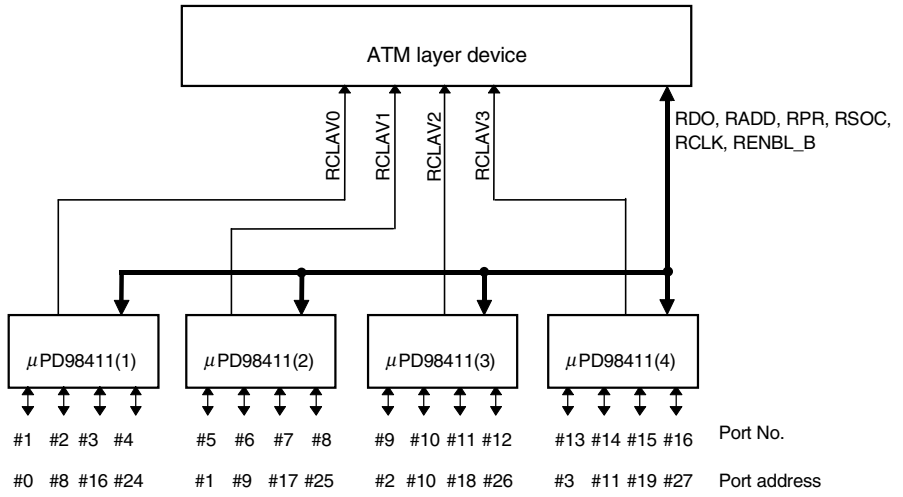


Figure 4-18 shows an example where four μPD98411s are connected to an ATM layer device. TCLAV and RCLAV that indicate the status of the transmit/receive FIFO of each port are internally multiplexed by the μPD98411. The status of the four ports is reported by one TCLAV/RCLAV pair.

Figure 4-18. Connection in MSP Mode (2) (μPD98411 × 4)

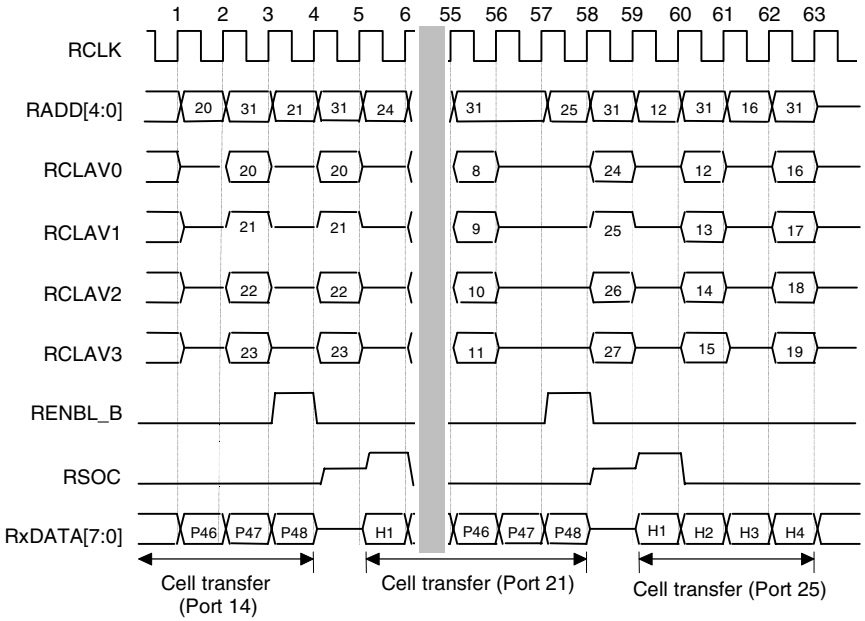


★ **(c) Example of operation in MSP mode**

Figure 4-19 shows an example of using the μPD98411 for reception in MSP mode. Also see Tables 4-4 (grouping A) and 4-5 (grouping B) and Figure 4-17. Edge 1 indicates the polling operation of the ATM layer. The ATM layer outputs an address that corresponds to group No. 5 (101XX) on RADD. The ports, 20, 21, 22, and 23, that belong to the group whose address matches the high-order three bits ("101") drive RCLAV in the next clock cycle. If the RCLAV1 signal returns a high level, for example, port 21 is supposed to have valid cells.

At edge 3, the ATM layer selects port 21. Port selection in MSP mode is carried out in the same manner as in the other modes. The target port address is output on RADD in the cycle that precedes the one in which RENBL_B goes low.

★ **Figure 4-19. Timing in MSP Mode (Reception)**



* The addresses and port Nos. above are expressed as decimal numbers.

4.1.4 Supporting the UTOPIA Parity Bit

The μPD98411 is equipped with parity bit input/output pins for the UTOPIA interface (TPR1, TPR2, RPR1, and RPR2).

(1) Receive parity

The odd parity bits are generated in the data to be output to RDO[15:0] and are output from RPR in synchronization with the data. When RENBL_B is high, RPR enters the high-impedance state in the same manner as RDO.

By setting the **UPR** bit of the **AVLC** register to 1, calculation and output of the receive parity bits can be disabled. They are enabled by default.

(2) Transmit parity

The odd parity bits input to TPR for the data on TDI[15:0] are verified when TENBL_B is low. If a parity error is detected, the **UT** bit of the **IMST** register is set to 1. The host can learn, by checking a register, whether a parity error has occurred.

If TPR is not used, it must be fixed to low. Verifying the parity can be disabled by setting the **UTC** bit of the **AVLC** register to 1.

To clear the **UT** bit of the **IMST** register that has been set, first set this **UTC** bit to 1 and then clear it to 0 again.

★ **Caution If the UTOPIA interface is used in Dual 8-bit mode, it is impossible to use the transmission-side UTOPIA parity check.**

4.2 PMD Interface

The PMD interface is used to connect a transceiver or receiver (optical link module, UTP transceiver, etc.) on the line side.

4.2.1 Signals

The PMD interface signal lines described below.

TDOT0-TDOT3/TDOC0-TDOC3: Output pins for transmitting serial data. These pins are differential output pins for the PECL level. They output signals in synchronization with the 155.52-MHz transmit clock that is selected according to the selected mode. TDOT0/TDOC0 is a pin for port 0, and TDOT3/TDOC3 is a pin for port 3.

RDIT0-RDIT3/RDIC0-RDIC3: Input pins for receiving serial data. These pins are differential input pins for the PECL level. RDIT0/RDIC0 is a pin for port 0, and RDIT3/RDIC3 is a pin for port 3.

TFKT/TFKC: This pin is used to input a transmit/receive clock generated by an external device, if any. To use this pin, input a high level to CSSEL.

CSSEL: This pin enables TFKT/TFKC input.

High: Enable, Low: Disable

SD0-SD3: This pin connects the SD (Signal Detect) signal output by the optical link module. Changes in the input level of this pin serve as a condition in which LOS is internally detected by the μPD98411. Because this pin is a TTL-level input pin, convert its level if the output of the optical link module is the PECL level.

Input levels High: Normal, Low: LOS status

TCL: This pin outputs a 19.44-MHz clock that is created by dividing the transmit clock by eight. By default, the transmit clock of port 0 is selected as the clock source. The port that is used as the clock source can be changed or clock output can be disabled depending on the setting of the **TCMSK** register. Clock output is stopped while the device is reset.

RCL: This pin outputs a 19.44-MHz clock that is created by dividing the receive clock by eight. By default, the receive clock of port 0 is selected as the clock source. The port that is used as the clock source can be changed or clock output can be disabled depending on the setting of the **RCMSK** register. Clock output is stopped while the device is reset.

TFSS: This pin controls transmit data output by the four ports. The μPD98411 samples the input signal of this pin at the rising edge of the TCL clock, and starts outputting a transmit frame from the beginning of the frame in synchronization with the rising edge, nine clock cycles after the edge at which the high level of this pin was most recently detected. When a high level is input to this pin, the transmit data output by the four ports is all 0 or all 1.

TxFP: This pin outputs an 8-kHz pulse signal whose width is equivalent to one cycle of the TCL clock, in synchronization with the first byte (A1 byte) of the frame to be transmitted. By default, this pulse signal is not output. It is output if a port that serves as a source is specified by the **FPMSK** register.

REFCLK
REFCLK-2nd:

These pins input the system clock necessary for the logic of the μPD98411 to operate and a 19.44-MHz clock that serves as a reference clock for the transmit synthesizer PLL. The reference clock for the transmit synthesizer PLL can be changed to REFCLK-2nd by using the **REF_cnt** bit of the **CSSC** register. In this case, however, the system clock must be input to REFCLK.

4.2.2 PMD Interface Blocks

Figure 4-20 is an outline block diagram of the PMD interface of the μPD98411. The transmit/receive clock paths can be changed by setting pins and registers.

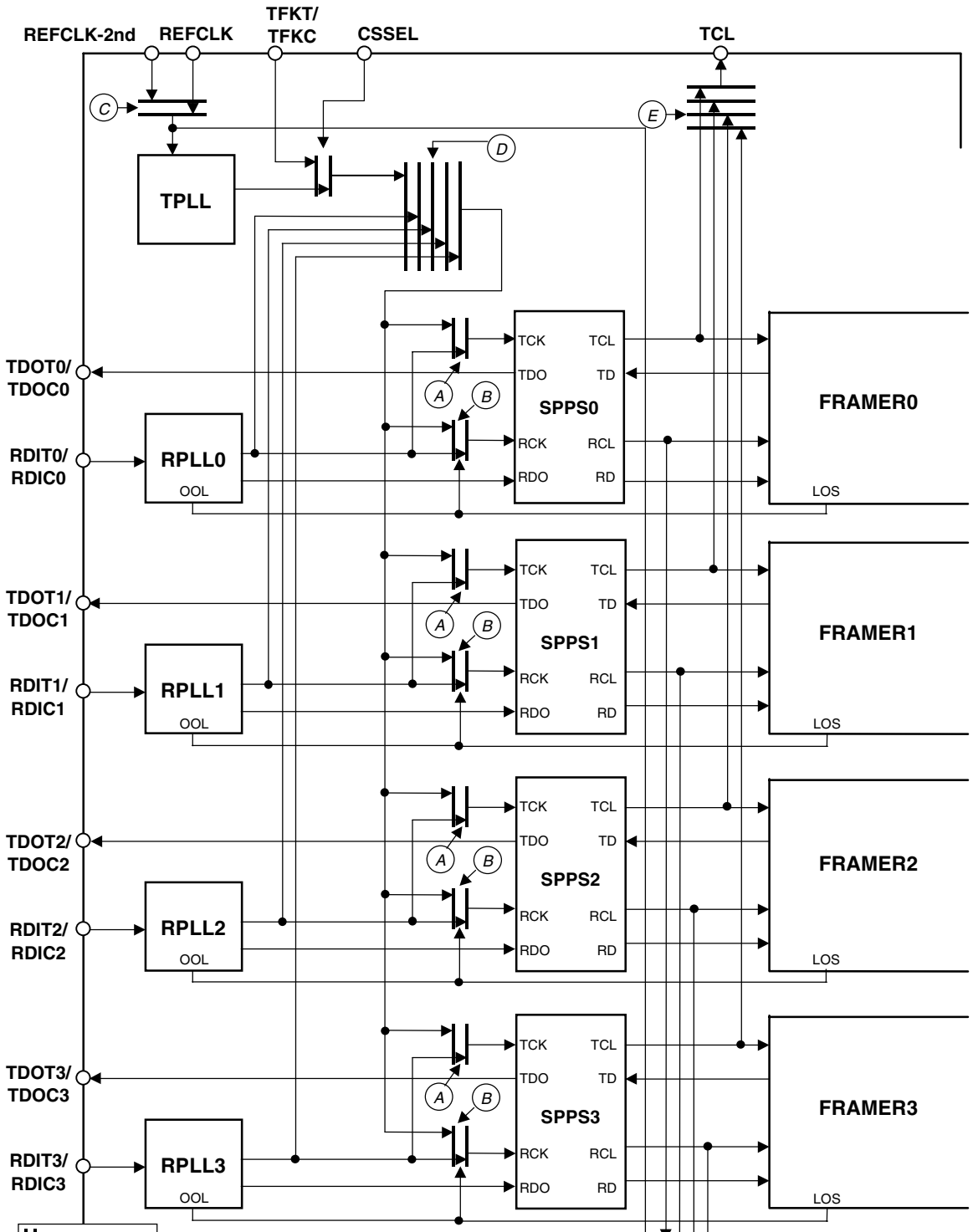
TPLL block: Synthesizer PLL which generates the transmit clock. This synthesizes the 155.52-MHz clock from the 19.44-MHz signal input to the REFCLK or REFCLK-2nd pin.

RPLL0-RPLL3 blocks: Clock recovery PLL that extracts the receive clock from the receive data string input to RDIT/RDIC.

SPPS blocks: Serial-parallel/parallel-serial converter blocks, which convert the receive serial data into 8-bit parallel data, and the transmit 8-bit serial data into serial data. Used in the processing operation of the FRAMER blocks, these also supply the 19.44-MHz clock by dividing the transmit/receive clock by eight.

FRAMER blocks: Blocks which process the frames by applying overhead processing, detecting errors, and inserting/extracting ATM cell data. Their operation is based on the 19.44-MHz clock signals supplied by the SPPS blocks.

★ **Figure 4-20. Outline Block Diagram of PMD Layer Side of μPD98411**



|| = Selectors

Symbol	Setting Registers	Bits	Address
A	TXSC	P0LP0-P3LP3	077H
B	CRSC	RCL0-RCL3	075H
C	CSSC	REF_cnt	076H
D	CSSC	P0-P3	076H
E	TCMSK	TC0-TC3	07AH
F	RCMSK	RC0-RC3	07BH
G	RCMSK	REFo	07BH

4.2.3 Transmit/Receive Clocks

The source of the transmit/receive clock can be selected in each mode in accordance with the system, by using registers and pin input.

(1) Transmit clock

The following four clocks can be selected when outputting transmit data.

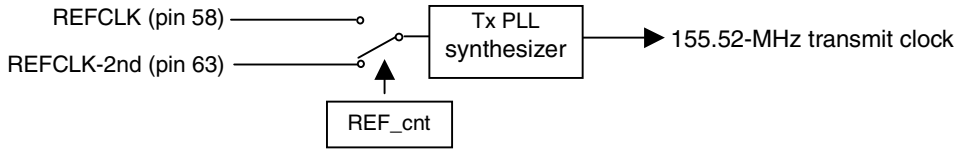
Table 4-6. Transmit Clocks

	Transmit Clock Source		Setting
a	Clock generated by internal synthesizer PLL (TPLL)		Default
b	Clock input by external device to TFKT/TFKC pin		CSSEL pin = high
c	Clock extracted from clock recovery PLL	Recovery clock of 1 port is distributed to all four ports as transmit clock	By using CSSC register
d		Receive clock of port is used as transmit clock of only that port.	By using TXSC register

Priority of setting: d > c > b > a

(a) Clock generated by internal synthesizer PLL

In the default status, in which the CSSEL pin is low and nothing is set in the CSSC and TXSC registers, ★ the 155.52-MHz clock generated by the internal synthesizer PLL in reference to REFCLK is used for transmission. To keep the output jitter for transmission to within 0.01 U.I.rms as specified by the SONET and SDH standards (Bellcore, ITU-T), input a reference clock with an accuracy of at least 40 ppm or more. Which of the clocks input to the REFCLK and REFCLK-2nd pins is to be used can be selected by using the **REF_cnt** bit of the **CSSC** register. In the default status, REFCLK input is used as the reference clock. If it is not necessary to change the reference clock, use the REFCLK input and fix the REFCLK-2nd pin to the low level. The 19.44-MHz clock must be input to REFCLK as a system clock even when the internal synthesizer PLL is not used, or when REFCLK-2nd is selected as the reference clock.



Although the synthesizer PLL starts clock output immediately after power is applied to the μPD98411, it takes about 10 ms before the clock stabilizes to 155.52 MHz. Note that the transmit frames cannot be output normally during this period. While the device is reset, the synthesizer PLL is also reset. Therefore, clock generation is stopped.

(b) Clock input from external device to TFKT/TFKC pin

When the CSSEL pin is driven high, TFKT/TFKC pin input is enabled. All the ports use the clock input to TFKT/TFKC as their transmit clock. Input the externally generated 155.52-MHz clock to the TFKT/TFKC pin.

With this setting, the clock generated by the internal synthesizer PLL is not used, but the system clock must be input to REFCLK.

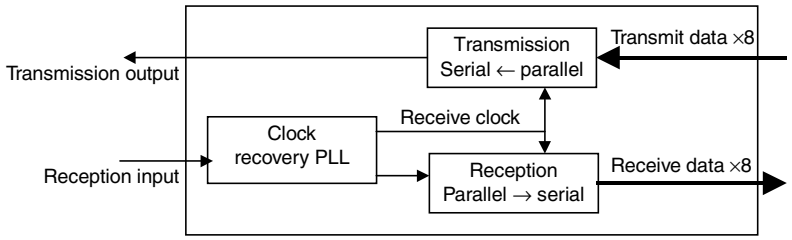
The setting of the **CSSC** and **TXSC** registers takes precedence over input to the CSSEL pin, and the transmit clock of the ports is switched.

★ **(c) Distributing a recovery clock for one port as a transmit clock for all ports**

Setting one of the **P0 to P3** bits of the **CSSC** register to 1 causes the recovery clock for the port that corresponds to the bit No. of the set bit to be used as a transmit clock for all ports. If two or more of the four bits (P0 to P3) are set to 1, the recovery clock for the port that has the highest priority determined by a priority sequence of P0 > P1 > P2 > P3 is selected. If the selected port enters the OOL or LOS status, automatic clock switching occurs to the recovery clock for the port that is set in the CSSC register and has the next highest priority. If all ports set in the CSSC register enter the OOL or LOS status, the clock generated by the synthesizer PLL is used as a transmit clock. If the port having a higher priority exits the OOL or LOS status, its recovery clock is used again.

(d) Using the receive clock of a port as the transmit clock of that port only

★ When the **P0LP through P3LP** bits of the **TXSC** register are set to 1, clock switching occurs in such a way that the recovery clock for the port that corresponds to the set bit will be used as a transmit clock. This setting is made for each port and does not affect the transmit clock setting of the other ports.



(2) Receive clock

The receive clock is extracted by the clock recovery PLL from the receive data string input by each port to RDIT/RDIC. After power is applied, the clock recovery PLL of each port starts following up with the receive data. If the correct receive data is input, a synchronization clock can be obtained about 500 μs after follow-up has been started. When the μPD98411 is reset, the clock recovery PLL is also reset. As a result, the extraction of the receive clock is stopped. The jitter tolerance of the recovery PLL of the μPD98411 conforms to the standards of SONET and SDH (Bellcore, ITU-T). The extracted clock is used for sampling receive data and for processing of the entire reception circuit.

Each port has an OOL (Out of Link) detection circuit that monitors whether the clock recovery PLL follows up with a receive data string and that the expected clock is extracted. This circuit monitors the phase difference between the clock extracted by the clock recovery PLL and the edge of the receive data. When it detects that the edge of the receive data shifts by 180 degrees or more from the edge of the extracted clock, it enters the OOL status. This status is reflected on the bits of the **PICR** register and can be used as an interrupt cause. If receive data that does not shift by 180 degrees or more from the edge of the extracted clock is received for the period equal to 2,048 bits, the OOL detection circuit exits from the OOL status. An increase in the phase difference between the extracted clock and edge of the receive data does not directly lead to the detection of a bit error, but serves as a criterion as to whether the receive clock recovery PLL can correctly extract a clock.

★ If a port enters the OOL status or a status in which the receive signal is lost (LOS status), and, consequentially, no normal recovery clock is available, automatic clock switching occurs in such a way that the transmit clock, instead of a recovery clock, will be supplied to the reception block. Alternatively, register setting can force clock switching. Either method is selected by setting up the CRSC register appropriately.

CRSC register (Address: 75H)

D7	D6	D5	D4	D3	D2	D1	D0
RAT0	RCL0	RAT1	RCL1	RAT2	RCL2	RAT3	RCL3
Port 0		Port 1		Port 2		Port 3	

★ **(a) RAT0-RAT3: Automatic selection**

These bits are used to automatically select a receive clock if a port enters the OOL or LOS status and cannot correctly extract a clock.

1: When the port enters the OOL or LOS status, automatic clock switching occurs in such a way that the clock used as the transmit clock for the port will be used as the clock for the reception block. The clock used as the transmit clock for the port is determined according to the input to the CSSEL pin and the setting of the CSSC register. It is the clock generated by the synthesizer PLL, the TFKT/TFKC input clock, or the recovery clock for one of the ports.

When the original port exits from the OOL or LOS status, supply of the clock for that port is resumed.

0: Even if the port enters the OOL or LOS status, the recovery clock is used as the reception side clock.

★ **(b) RCL0-RCL3: Forcible selection**

If any of these bits is set to 1, clock switching is forced in such a way that the port will use the transmit clock as a clock for the reception block. In addition, the clock recovery PLL for the port is reset, and the OOL bit is set.

★ **Caution While the RCL0 to RCL3 bits are set, inputting normal data to the reception line does not reset the OOL bit, because the clock recovery PLL for the port has been reset. Note that a change in the state of the OOL bit cannot be used as a condition for setting and resetting the RCL0 to RCL3 bits.**

Remark After a clock extracted by the external clock recovery PLL is input to TFKT/TFKC, setting the RCL bit enables only one port to use the extracted clock for transmission and reception.

(3) Examples of transmit and receive clocks

Figure 4-21 shows an example where two μPD98411s are used and the clock of one oscillator is used as the reference clock for the synthesizer PLLs of both μPD98411s.

Figure 4-21. Use of Internal Synthesizer PLL

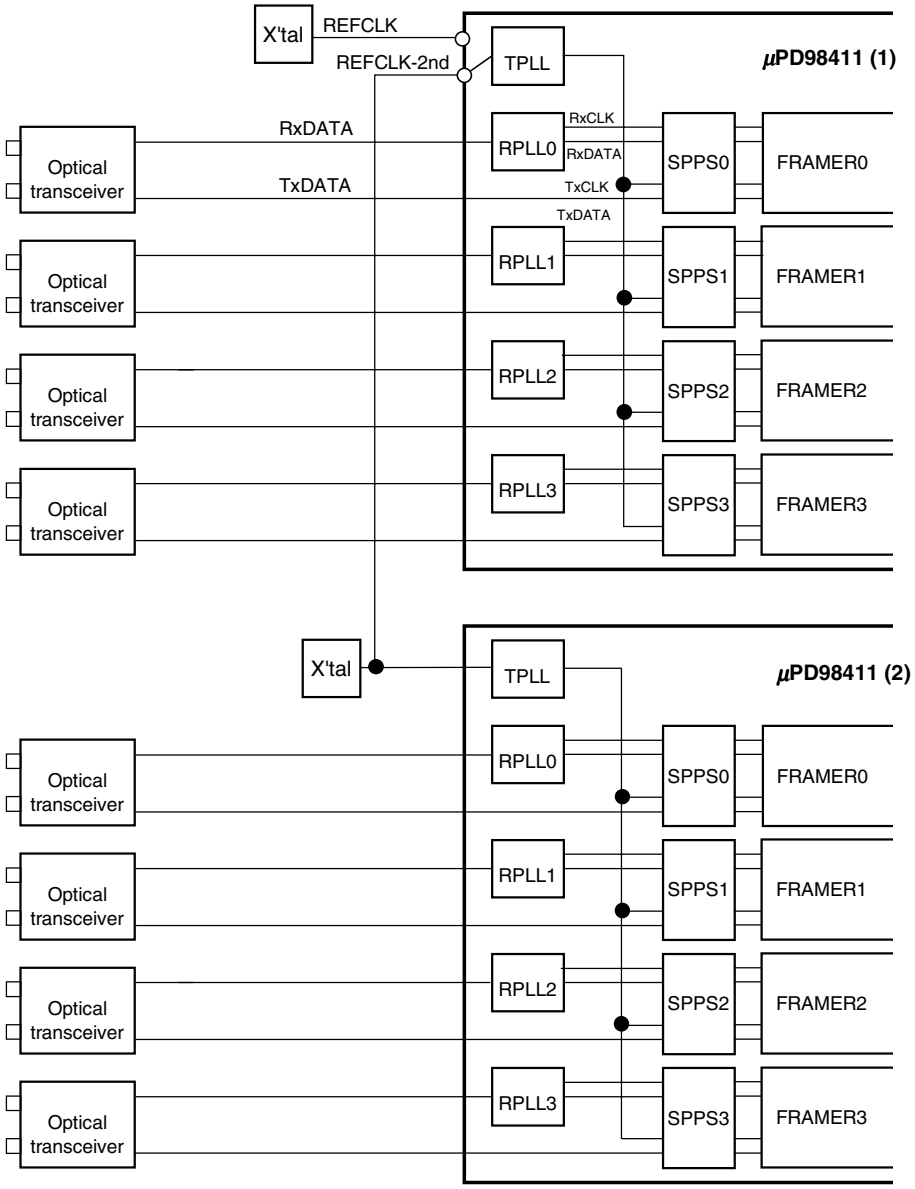
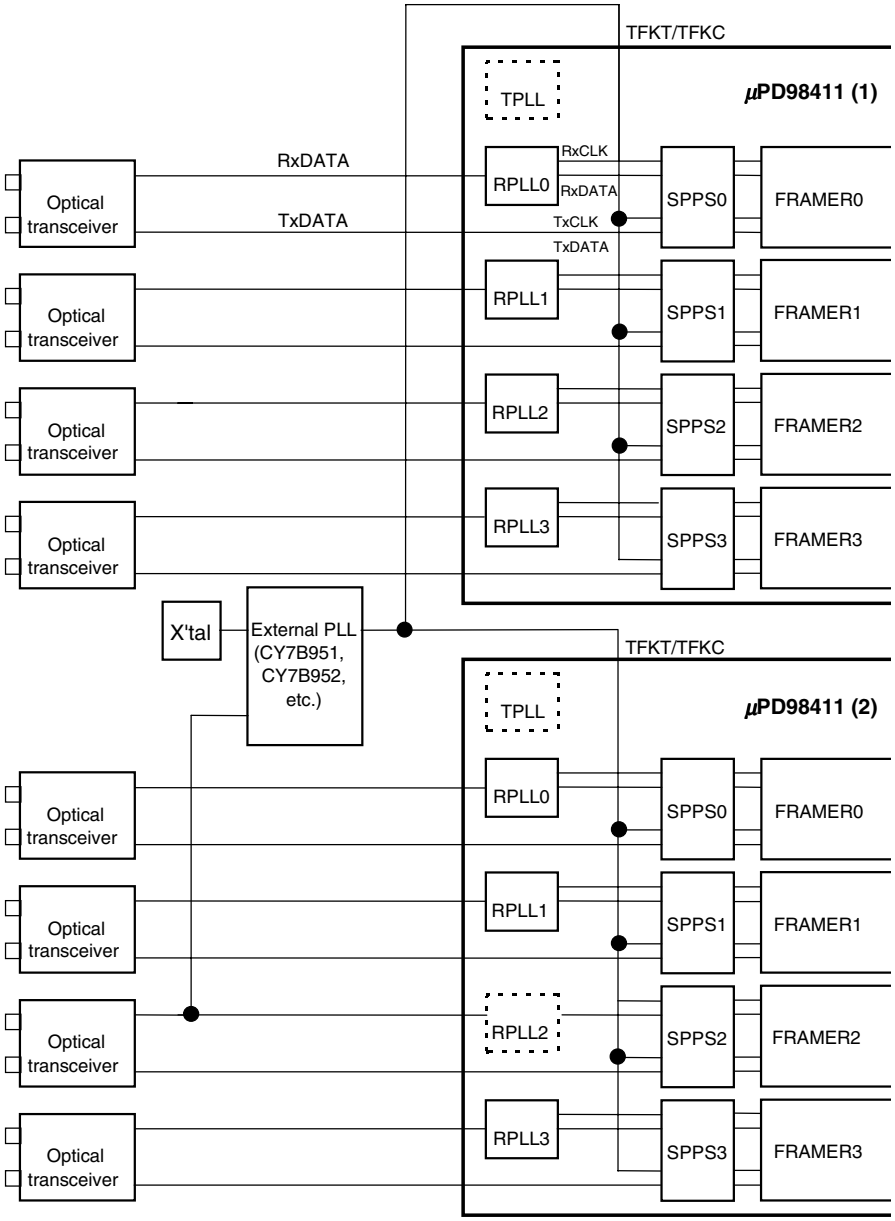


Figure 4-22 shows an example where two μPD98411s are used and the 155.52-MHz clock extracted from the data received by port 3 of one of the μPD98411s by an external clock recovery PLL is used as the transmit clock for all eight ports. The clock extracted by the external clock recovery PLL is input to the TFKT/TFKC pins of both the μPD98411s and is also used as the receive clock of port 3. This setting is made by using the CSSEL pin input and the **RCL** bit of the **CRSC** register.

Figure 4-22. Use of External PLL

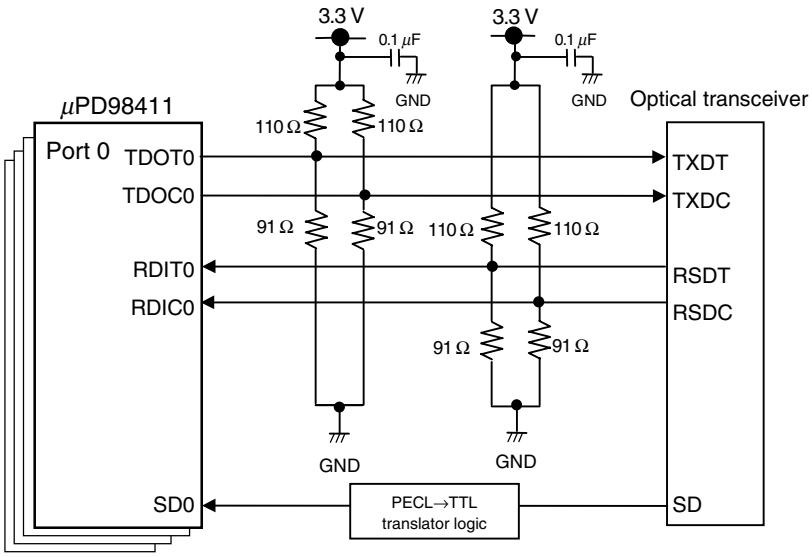


4.2.4 Examples of Connection between μPD98411 and Transceiver

(1) Connection to 3.3-V transceiver/receiver

The transmit/receive data input/output pin uses a PECL level interface. It is VDD 2 V and should have a 50-ohm termination. Since, the SD3-SD0 pins use TTL level inputs, a logic for level translation should be added in case the optical transceiver outputs PECL level signals. Figure 4-23, below, shows an example of connecting a 3.3-V optical transceiver.

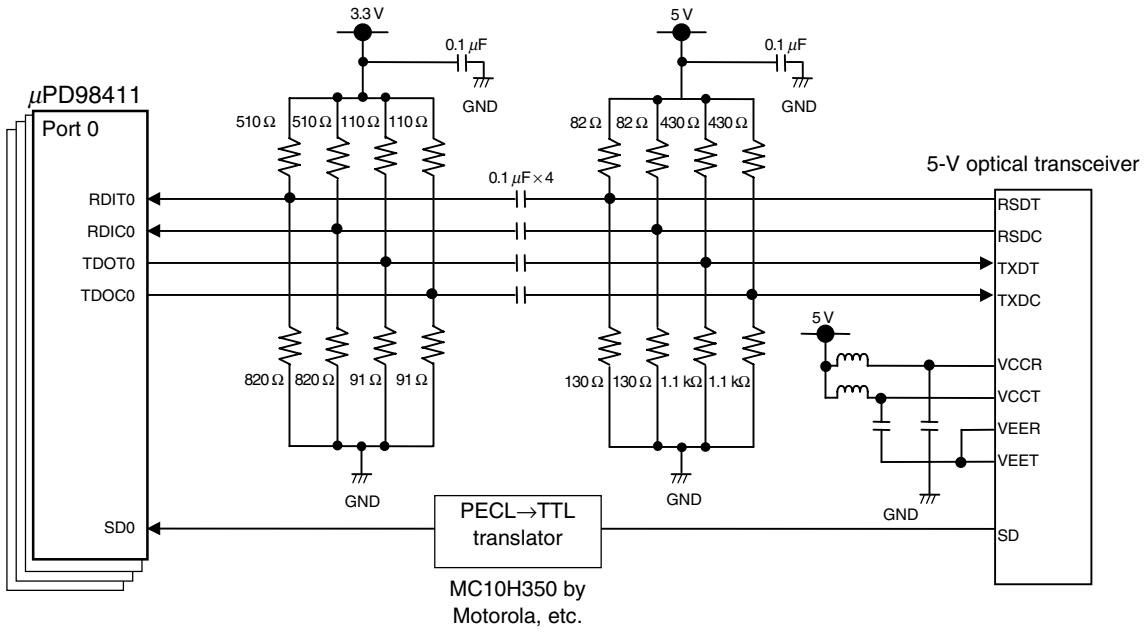
Figure 4-23. Connection to 3.3-V Optical Transceiver



(2) Connection to 5-V transceiver/receiver

Figure 4-24 shows an example of connecting the μPD98411 to a 5-V optical transceiver. Because the μPD98411 operates on 3.3 V, it is connected to a 5-V device by means of AC coupling.

Figure 4-24. Connection to 5-V Optical Transceiver



★ **Remark** When the μPD98411 is connected to an optical module by AC coupling as shown in Figure 4-24, if an optical signal is interrupted in the optical module, and data input to RDIT/RDIC becomes a string of 0s, there is no potential difference at RDIT/RDIC, and the μPD98411 may fail to recognize the receive data as a string of 0s, resulting in LOS detection disabled.

In this case, connect the optical module to the SD pin of the μPD98411 in order to enable LOS detection. Resetting the SDm bit of the IACM register causes a change in the SD pin input level to be added as a LOS detection condition.

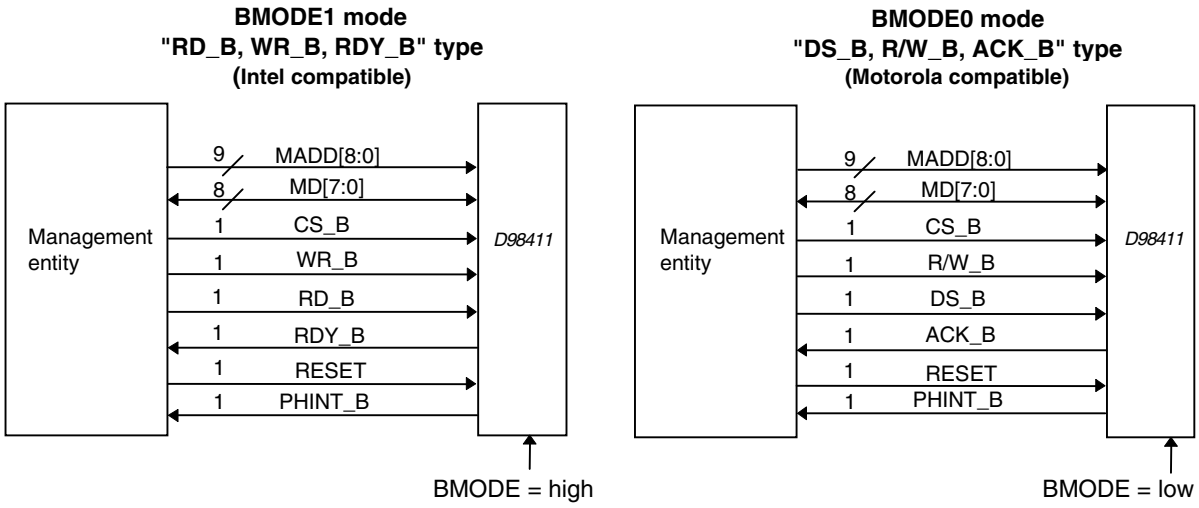
4.3 Management Interface

The management interface is used by the host processor to access the registers of the μPD98411. The μPD98411 supports two modes of this interface as shown in Table 4-7. Whether **BMODE0** or **BMODE1** mode is used is determined by the input status of the BMODE pin at hardware reset.

Table 4-7. Management Interface Mode

Mode	BMODE Input	Style
BMODE1 mode	High	RD_B, WR_B, RDY_B style (Intel compatible mode)
BMODE0 mode	Low	DS_B, R/W_B, ACK_B style (Motorola compatible mode)

Figure 4-25. Management Interface

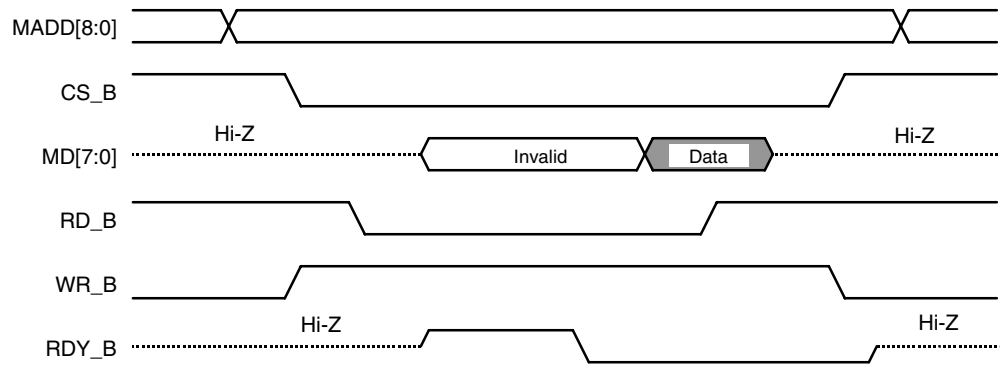


★ 4.3.1 Read Operation

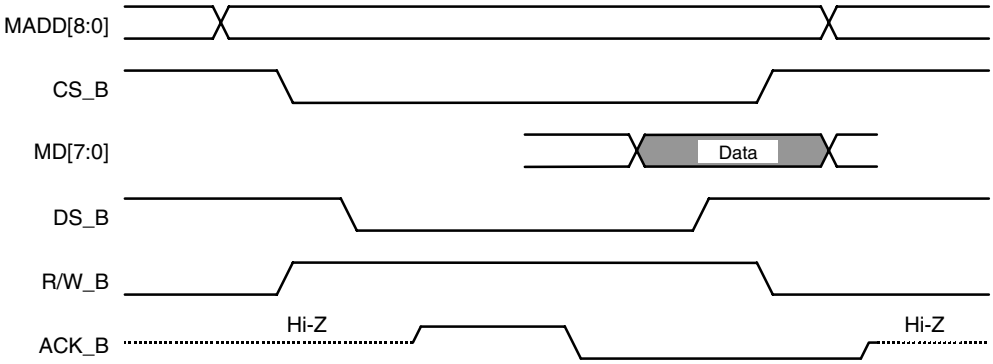
The host starts a read operation by driving an address onto MADD[8:0] and making CS_B and RD_B (DS_B) low (active). In response, the μPD98411 first drives RDY_B (ACK_B) to a high level. After it becomes ready to output requested data onto MD[7:0], it makes RDY_B (ACK_B) low. After detecting that RDY_B (ACK_B) is low, the host makes RD_B (DS_B) high and reads data from MD[7:0]. If the μPD98411 has not been selected by CS_B, it places RDY_B (ACK_B) and MD[7:0] in a high-impedance state. In BMODE1 mode, a read cycle is recognized when WR_B goes high and RD_B goes low. In BMODE0 mode, a read cycle is recognized when DS_B goes low and RW_B goes high. Figure 4-26 shows the read timing for each mode.

Figure 4-26. Read Operation

BMODE1 mode (Intel compatible)



BMODE0 mode (Motorola compatible)



★ **Cautions 1. The time that elapses since DS_B (RD_B) has gone low until the μPD98411 makes RDY_B (ACK_B) low varies with the register to be accessed. Before reading data from MD[7:0], make sure that RDY_B (ACK_B) is low.**

The maximum time that elapses since DS_B (RD_B) has gone low until the μPD98411 makes RDY_B (ACK_B) low is "4.5 × REFCLK cycle (about 235 ns)." To enable any register to be read-accessed without using RDY_B (ACK_B), make the pulse width of DS_B (RD_B) larger than or equal to "4.5 × REFCLK cycle."

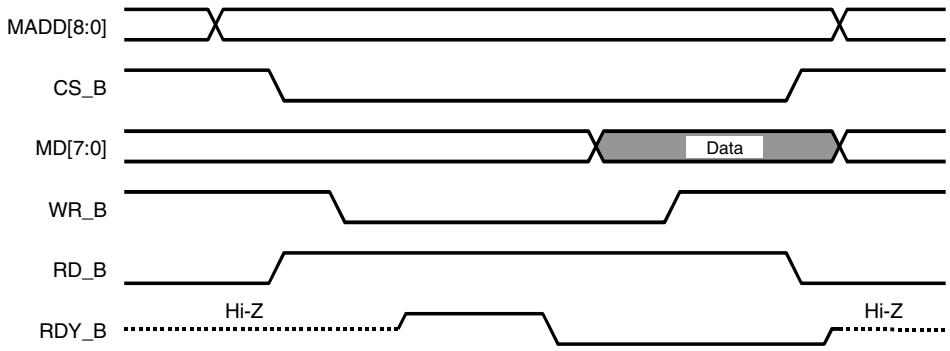
★ **2. The recovery time of DS_B (RD_B) is about 364 ns, which is 7 REFCLK clock cycles. Do not access registers at intervals smaller than 7 cycles.**

★ **4.3.2 Write Operation**

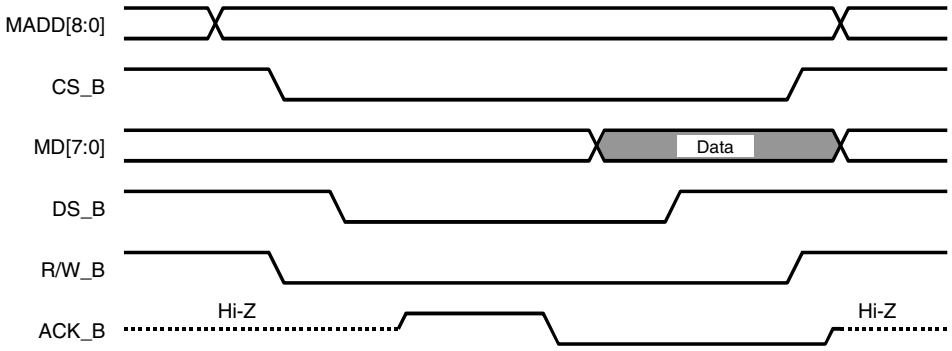
The host starts a write operation by driving an address onto MADD[8:0], outputting write data onto MD[7:0], and making CS_B and WR_B (DS_B) low. In response, the μPD98411 first drives RDY_B (ACK_B) to a high level. After it becomes ready to read, it makes RDY_B (ACK_B) low. After detecting that RDY_B (ACK_B) is low, the host makes WR_B (DS_B) high after a certain period of time. When WR_B (DS_B) goes high, the μPD98411 reads data from MD[7:0]. If the μPD98411 has not been selected by CS_B, it places RDY_B (ACK_B) in a high-impedance state. In BMODE1 mode, a write cycle is recognized when RD_B goes high and WR_B goes low. In BMODE0 mode, a write cycle is recognized when DS_B and RW_B go low. Figure 4-27 shows the write timing for each mode.

Figure 4-27. Write Operation

BMODE1 mode (Intel compatible)



BMODE0 mode (Motorola compatible)



★ **Cautions 1. The time that elapses since DS_B (WR_B) has gone low until the μPD98411 makes RDY_B (ACK_B) low varies with the register to be accessed. Before making DS_B (WR_B) high, make sure that RDY_B (ACK_B) is low.**

The maximum time that elapses since DS_B (WR_B) has gone low until the μPD98411 makes RDY_B (ACK_B) low is "4.5 × REFCLK cycle (about 235 ns)." To enable any register to be write-accessed without using RDY_B (ACK_B), make the pulse width of DS_B (WR_B) larger than or equal to "4.5 × REFCLK cycle."

★ **2. The recovery time of DS_B (WR_B) is about 364 ns, which is 7 REFCLK clock cycles. Do not access registers at intervals smaller than 7 cycles.**

4.4 Interrupt Processing

If a line error or overflow of the performance counter is detected by each port, it is reported to the host by deasserting interrupt signal PHINT_B low. When the host detects that PHINT_B is deasserted low, it reads the interrupt cause register to check the interrupt cause. It can also set an interrupt mask for each cause bit.

The method used to process an interrupt varies depending on the PHINT_B pin selection and the processing mode selection.

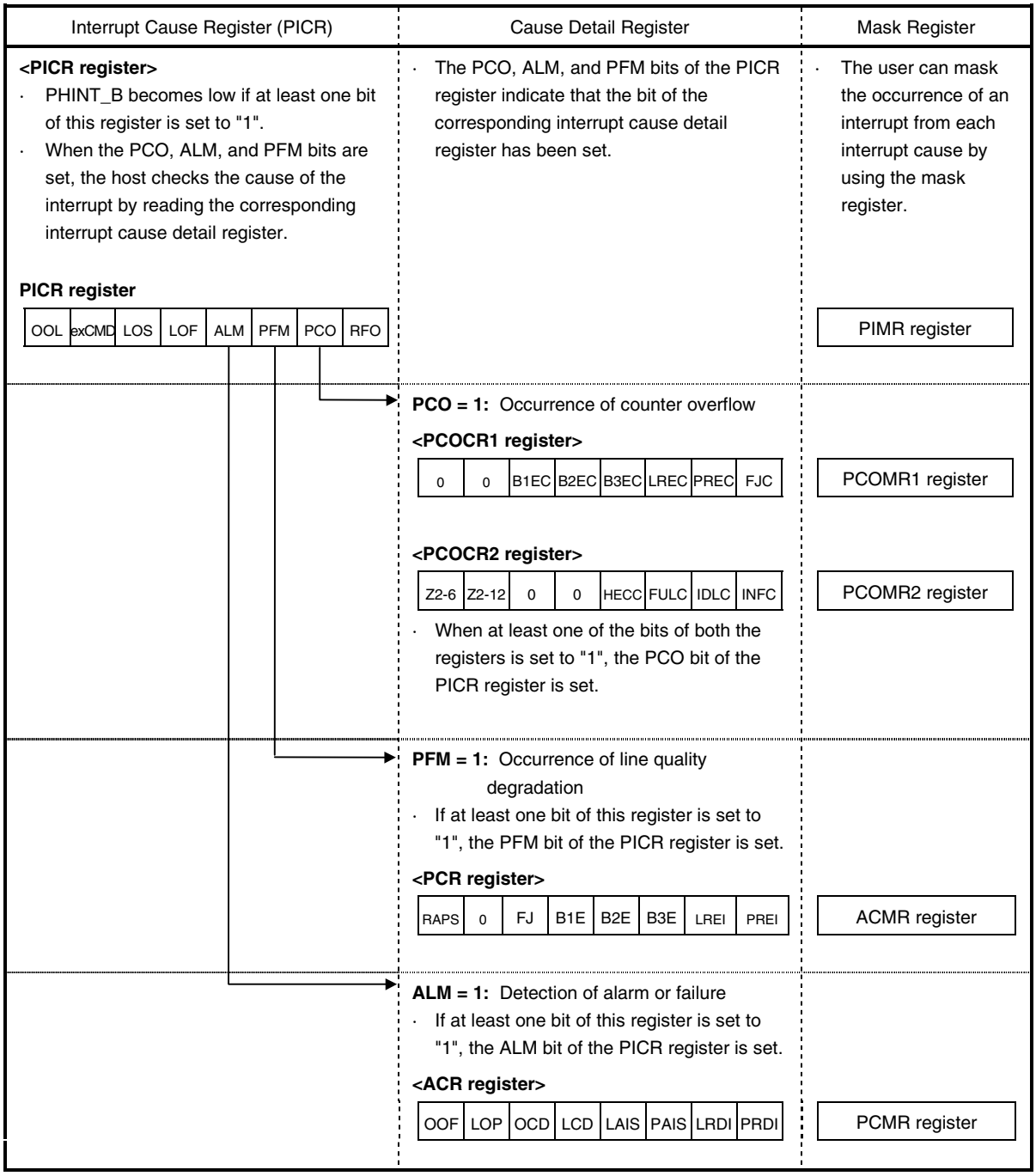
4.4.1 Interrupt Cause Register

Each port has five interrupt cause registers and an interrupt details register that are used to report the causes of interrupts to the host. For each register, a mask register that masks the interrupt cause is provided.

Interrupt signal PHINT_B goes low if even one of the bits of the cause register (PICR) is set to 1. When the host detects that PHINT_B has gone low, it reads the interrupt cause register (PICR register) to check the bits that have been set and thereby to check the interrupt cause. If the ALM, PFM, or PCO bit is set, the host also reads the interrupt cause detail registers (ACR, PCR, PCOCR1, PCOCR2) to investigate the details. Figure 4-28 shows the relationship between the interrupt-related registers.

★ **Remark** The bits of the interrupt cause registers may be set due to the reception of an undefined frame immediately after power is applied to the μPD98411 or a reset (a hardware reset or a software reset based on the ALL bit of the CMR2 register) occurs. Once the power is switched on or a reset occurs, be sure to read-clear all interrupt cause registers after initializing the mode register.

Figure 4-28. Relationship between Interrupt Cause Registers



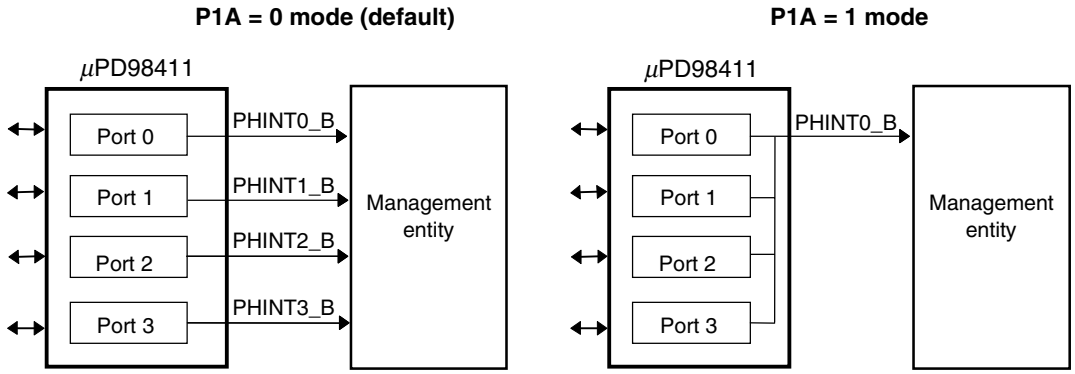
4.4.2 Interrupt Signal Report Mode

The μPD98411 has one interrupt signal pin PHINT_B per port (PHINT0_B to PHINT3_B), allowing it to indicate an interrupt independently for each port. It is also possible to establish a mode in which the interrupt signals of the four ports are multiplexed internally by the μPD98411 and output as a single signal. This mode can be switched using the **P1A** bit of the **ICNT** register. By default, a mode in which the four pins of the PHINT_B signal are used to report the occurrence of an interrupt of each port independently is selected.

In PIA=1 mode, where the interrupt signals of all the ports are indicated with a single signal, information relating to the port causing the interrupt is set in the **IMST** register. The host reads the IMST register to identify the port number before reading the PICR register of that port.

ICNT register (Address: 7EH)	
P1A = 1	The interrupt signals for all four ports are multiplexed and output as a single PHINT0_B pin. The port causing the interrupt signal to be output is indicated in the **IMST** register (address: 7FH).
P1A = 0	An independent interrupt signal is used for each port (PHINT3_B to PHINT0_B). (Default)

Figure 4-29. Interrupt Pin Modes



4.4.3 Interrupt Processing

When the host detects that the PHINT_B signal has been asserted active, it reads the interrupt cause register to check that the event that has occurred.

The events reported by the μPD98411 are classified into two types: those that report that the μPD98411 has entered or exited from a certain status, such as failure and alarm, that lasts for a specific time once it has occurred, and the events that individually occur and report history, such as the cause of the degradation of line quality and overflow of the performance counter.

Table 4-8. Types of Interrupt Sources

Type	Interrupt Cause	
	Register	Event (Bit name of register)
Events reporting status	PICR	OOL, exCMD, LOS, LOF,
	ACR	OOF, LOP, OCD, LCD, LAIS, PAIS, LRDI, PRDI
	PCR	RAPS
Events reporting history	PICR	RFO
	PCR	FJ, B1E, B2E, B3E, LREI, PREI
	PCOCR1	B1EC, B2EC, B3EC, LREC, PREC, FJC
	PCOCR2	HECC, FULC, IDLC, INFC, Z2-6, Z2-12
Other events	PICR	ALM, PFM, PCO

Two modes are available for those events that report that the μPD98411 has entered or exited from a certain status.

The interrupt processing procedure applied by the host varies depending on the selected mode. The mode is set with the **RCM** bit of the **ICNT** register.

ICNT register (Address: 7EH)	
RCM = 1	Interrupt signal PHINT_B goes low both when an event occurs and when it is cleared. The host can detect the clearing using this interrupt signal.
RCM = 0	Interrupt signal PHINT_B goes low when an event occurs, and remains low until the μPD98411 has exited from the status caused by the event. When the μPD98411 has exited from the status, it is detected by polling a register (default).

★ The specification states that the interrupt cause register bits that are set by detecting an event for reporting on a status such as LOS are to be kept set until the register is read-accessed after recovery from the event. Once the PICR register (interrupt cause register) is cleared using the ICR bit of the CMR2 register (interrupt cause register initialization), however, the bits will not be set again even if the event detection status lasts; they will be set again only when the event is detected again after recovery from it. This condition applies to all the events for reporting on the LOS, LOF, AIS, RDI, OCD, LCD, OOF, LOP, RAPS, OOL, and CMD statuses are to be reported.

There is no problem with a hardware reset and a reset caused by the ALL and ALR bits of the CMR2 register, because the interrupt cause registers are set again. There is no problem with a reset caused by a register read either, because the interrupt cause register is kept set while the detected status lasts and cleared only when the interrupt cause disappears.

(1) Interrupt processing in RCM = 0 mode

When the host detects that PHINT_B has become low, it reads the PICR register. If the ALM, PFM, or PCO bit is set, the host also reads the corresponding cause detail register (ACR, PCR, PCOCR1, PCOCR2).

The timing at which the set bit in the interrupt cause register is cleared and the PHINT_B signal is set inactive varies with the type of the cause. When one of the events reporting a status shown in Table 4-8 occurs, if a register is read after the μPD98411 has recovered from the event, the bits of the cause register and PHINT_B are cleared. While an event occurs, the bits of the cause register and PHINT_B are not cleared even if the register is read. If an event reporting history occurs, the bits and PHINT_B are cleared by reading the register.

- Change condition of PHINT_B signal
  - High → low: When even one bit of the PICR register is set
  - Low → high: When all the bits of the PICR register are cleared to 0
- Change condition of bits of interrupt cause register
  - Event reporting status: Set when an event occurs and reset when recovery from the event is made and the register is read.
  - Event reporting history: Set when an event occurs and reset when the register is read.
  - The ALM, PFM, and PCO bits of the PICR register are set when one of the bits of the ACR, PCR, and {PCOCR1, PCOCR2} registers is set to 1, and reset when all the bits of the registers are cleared to 0.

Figure 4-30 shows an example where the LOS bit of the PICR register is set and the PHINT_B signal goes low because the port has entered the LOS status. **<1>** The host receives an interrupt indication and reads the PICR register, but the bit is not cleared and the PHINT_B signal remains active because the port is still in the LOS status. **<2>** Later, the port is released from the LOS status, but the LOS bit and PHINT_B signal remain as is. **<3>** When the host reads the register again, the bit is cleared and PHINT_B is set inactive. **<4>** When the LOS status occurs again and the host reads the register, the PHINT_B signal is set inactive because the LOS status has already been released.

Figure 4-30. Example of Cause Register Bit Operation in RCM = 0 Mode

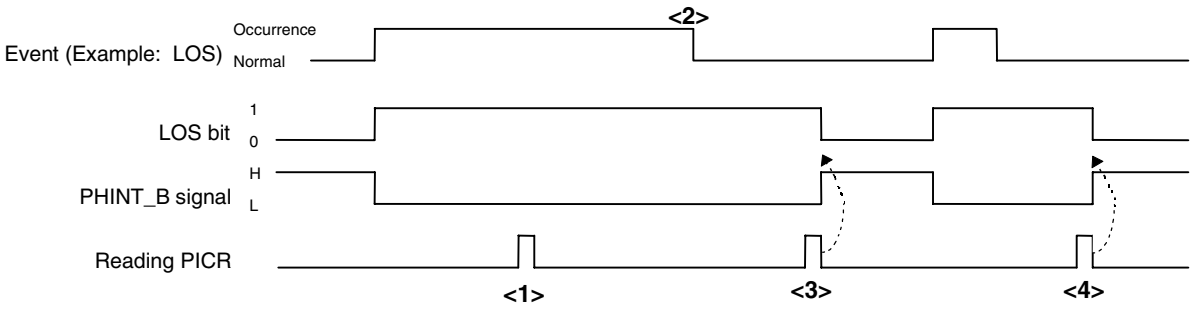
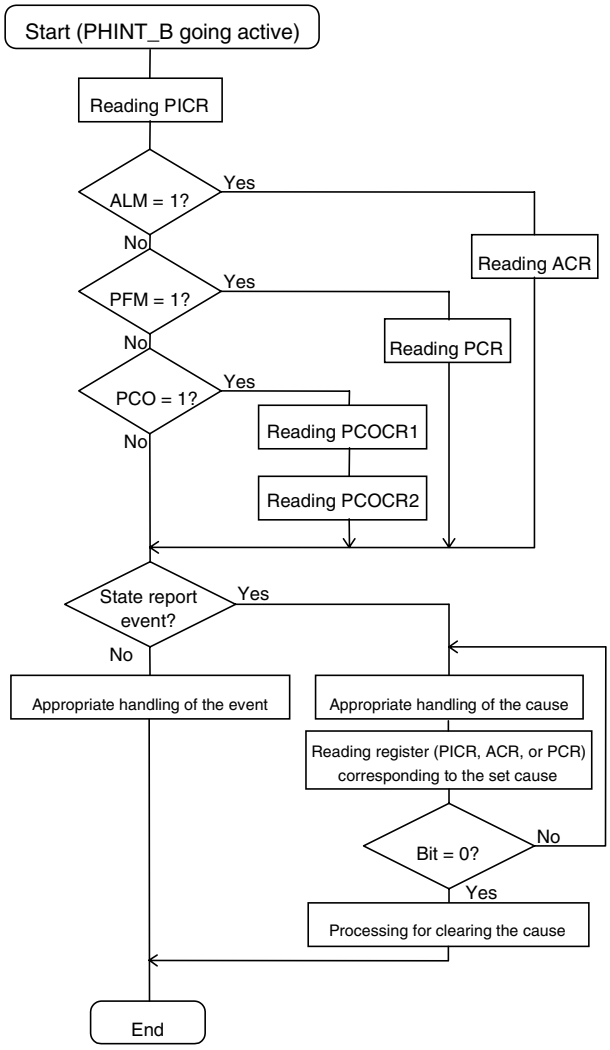
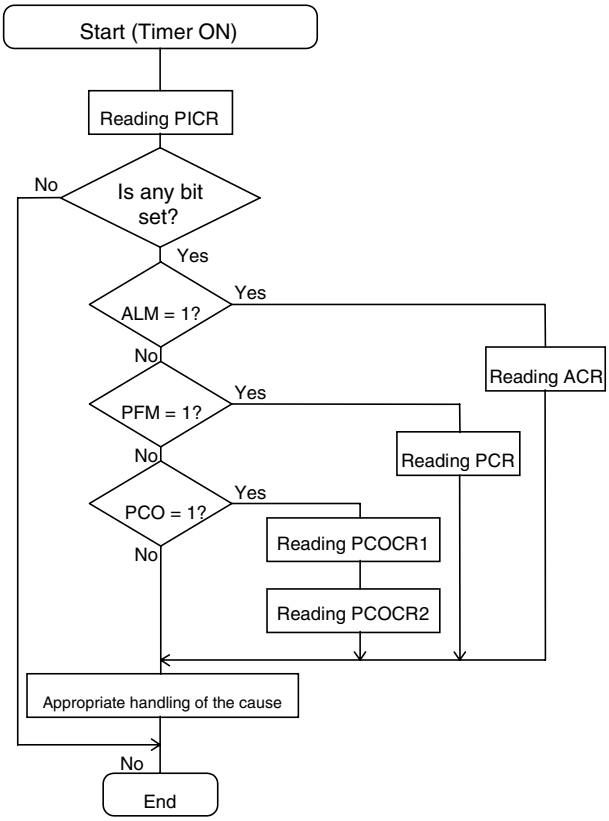


Figure 4-31. Outline of Processing Flow

<1> Processing triggered by interrupt



<2> Periodic polling of line status without relying on interrupts



(2) Interrupt processing in RCM = 1 mode

In this mode, the interrupt signal is deasserted low when the μPD98411 has entered into or exited from a status caused by one of the events reporting a status listed in Table 4-8. The host reads the PICR register when it has detected that PHINT_B has gone low. If the ALM, PFM, or PCO bit is set, the host also reads the corresponding cause detail register (ACR, PCR, PCOCR1, or PCOCR2). If an event reporting history has occurred, the bits of the cause register are cleared when the register is read, and the PHINT_B signal is deasserted inactive. If an event reporting a status has occurred, the PHINT_B signal goes high when the cause register is read. However, the bits of the cause register remain set until the μPD98411 has recovered from the event. The host saves the register value it has read to the stack. If a recovery from the event is made, the bits of the cause register are automatically reset to 0. If even one of the register bits is reset to 0, the PHINT_B signal is asserted active again. The host reads the cause register and compares its value with the value previously saved to the stack to detect the event from which the μPD98411 has recovered.

- Change condition of PHINT_B signal
  - High → low: If one of the bits of the event reporting status is set to 1
    If one of the bits of the event reporting status is reset to 0
    If one of the bits of the event reporting history is set to 1
  - Low → high: When the PICR register is read
- Change condition of bits of interrupt cause register
  - Event reporting status: Set when a cause is generated and reset when the μPD98411 has recovered from the event after reading the register, or when the register is read after the μPD98411 has recovered from the event.
  - Event reporting history: Set when an event occurs and reset when the register is read.
  - The ALM, PFM, and PCO bits of the PICR register are set to 1 if even one of the bits of the ACR, PCR, and {PCOCR1, PCOCR2} registers is set to 1, and reset if all the register bits are reset to 0.

Figure 4-32 shows an example where the port has entered the LOS status. **<1>** Upon the occurrence of an event, the LOS bit of the PICR register is set and the PHINT_B signal is set active. **<2>** The host reads the PICR register and the PHINT_B signal is set inactive. The LOS bit remains set for as long as the LOS status continues, however. **<3>** Later, the port is released from the LOS status and the PHINT_B signal is set active again to indicate this. **<4>** The host reads the PICR register and the PHINT_B signal is set inactive as a result. The host compares the register value read in **<2>** with that read in **<4>** and recognizes the release of the LOS status. **<5>** The LOS status occurs again. **<6>** The host reads the PICR register, the PHINT_B signal is set inactive, and the LOS bit of the PICR register is also reset because the LOS status has already been released. **<7>** Because the LOS bit has been reset, PHINT_B goes active to indicate the clearing of the event. **<8>** The host reads the PICR register.

Figure 4-32. Example of Cause Register Bit Operation in RCM = 1 Mode

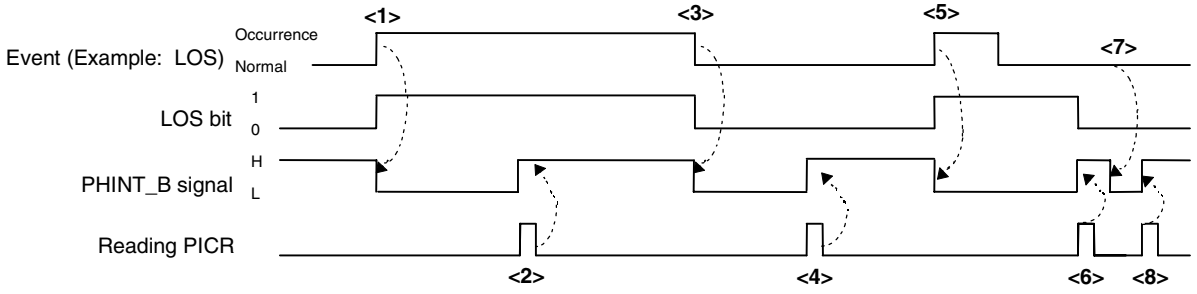


Figure 4-33. Outline of Interrupt Processing Flow in RCM = 1 Mode

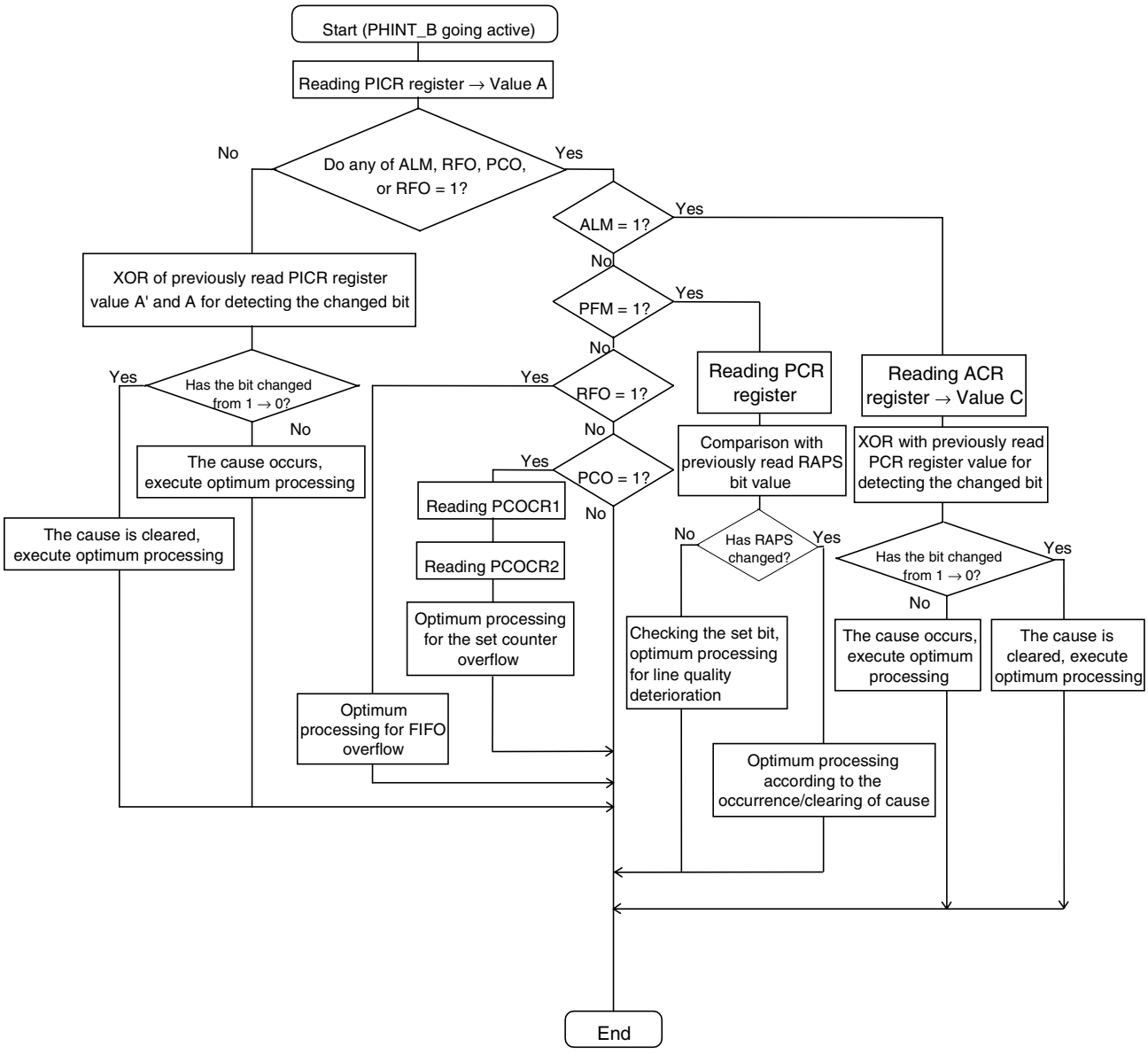


Table 4-9. Difference in Cause Register Bit Setting/Resetting Conditions According to Mode

Register	Bit	Set Condition	Reset Condition	
			RCM = 0 Mode	RCM = 1 Mode
PICR	OOL exCMD LOF LOS	When an event occurs	When this register is read after the event has been cleared	When the μPD98411 has recovered from an event after this register has been read or when this register is read after recovery from the event has been made
	ALM	When any of the ACR register bits is set	When all of the ACR register bits are reset to 0	When all of the ACR register bits are reset to 0
	PFM	When any of the PCR register bits is set	When all of the PCR register bits are reset to 0	When the PCR register is read or when this register is read
	PCO	When any of the PCOCR1 or PCOCR2 register bits is set	When all of the PCOCR1 or PCOCR2 register bits are reset to 0	When the bits of the PCOCR1 and PCOCR2 registers are read and cleared or when this register is read
	RFO	When the receive FIFO overruns	When this register is read	When this register is read
ACR	OOF LOP OCD LCD LAIS PAIS LRDI PRDI	When an event occurs	When this register is read after the event has been cleared	When the μPD98411 has recovered from an event after this register has been read or when this register is read after recovery from the event has been made
PCR	RAPS	When an event occurs	When this register is read after recovery from the event	When the μPD98411 has recovered from an event after this register has been read or when this register is read after recovery from the event has been made
	FJ B1E B2E B3E LREB PREB	When an error is detected	When this register is read	When this register is read
PCOCR1	B1EC B2EC B3EC LREC PREC FJC	When the counter value exceeds all FF	When this register is read	When this register is read
PCOCR2	Z2-6 Z2-12 HECC FULC IDLC INFC	When the counter value exceeds all FF	When this register is read	When this register is read

CHAPTER 5 REGISTERS

The μPD98411 contains registers which are used to set each operation mode and issue commands that are accessed via the management interface. The registers of the μPD98411 are classified into two groups: "port registers" that are provided for each port and which have the same register area, and "common registers" that are used by all four ports. To use a port register, select one of ports 0 to 3 with the high-order two bits of address lines MADD[8:7], and specify the register address with MADD[6:0]. The common registers are located in the second-half addresses of port 0.

Addresses	Registers
000H-065H	Port 0 set registers
06CH-07FH	Common registers
080H-0C5H	Port 1 set registers
100H-165H	Port 2 set registers
180H-1C5H	Port 3 set registers

[Caution]

The data bit string of the SONET/SDH frame the μPD98411 transmits from the PMD interface is sequentially transmitted starting from the MSB. Note that the names of the bits in the byte in the overhead of the SONET/SDH frame are described in two ways in this manual, as follows:

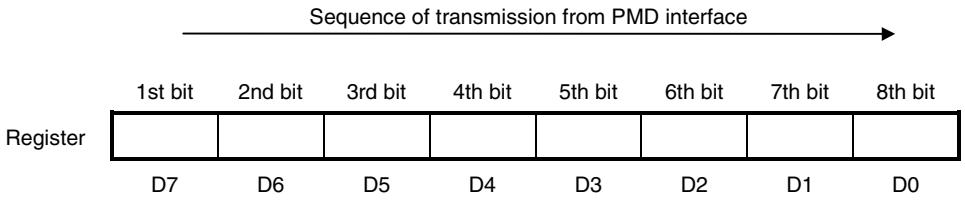
(1) First through eighth bits

These bits are mainly used to indicate the bit string of the overhead byte in the SONET/SDH frame and are in the sequence in which they are output from the PMD interface.

(2) D7 through D0 bits

These bits are mainly used to indicate the bits in the internal registers of the μPD98411 and correspond to the D7 through D0 pins of the external management interface.

- Expressing bits in internal registers



5.1 Register Map

5.1.1 Port Registers

The same port registers are provided for each port. The two high-order bits, MADD[8:7], of an address specify a port, and each address in the table indicates the MADD[6:0] bits that specify a register. The default value indicates the value set after a reset.

(1/3)

No.	Address (H)				Name	Function	R/W	Number of Bits	Default
	Port 0	Port 1	Port 2	Port 3					
(1)	000	080	100	180	CMR1	Command 1. Sets transmission of alarm frame.	R/W	5	00H
(2)	001	081	101	181	CMR2	Command 2. Sets initialization of register.	R/W	4	00H
(3)	002	082	102	182	CMR3	Command 3. Sets transmission of pseudo error frame.	R/W	5	00H
(4)	003	083	103	183	MDR1	Mode 1. Sets SS bit.	R/W	2	00H
(5)	004	084	104	184	MDR2	Mode 2. Sets loopback mode.	R/W	2	00H
(6)	005	085	105	185	MDR3	Mode 3. Sets scramble mode.	R/W	5	00H
(7)	006	086	106	186	PICR	Indicates interrupt cause.	R	8	00H
(8)	007	087	107	187	PIMR	Masks interrupt cause.	R/W	8	FFH
(9)	008	088	108	188	ACR	Indicates line failure interrupt cause detail.	R	8	00H
(10)	009	089	109	189	ACMR	Masks line failure interrupt cause.	R/W	8	FFH
(11)	00A	08A	10A	18A	PCR	Indicates performance monitoring cause detail.	R	7	00H
(12)	00B	08B	10B	18B	PCMR	Masks performance monitoring cause detail.	R/W	7	FFH
(13)	00C	08C	10C	18C	IACM	Masks automatic transmission of Path/Line RDI.	R/W	2	FFH
(14)	00D	08D	10D	18D	B1ECT	B1 error counter register	R	8	00H
(15)	00E	08E	10E	18E	B2ECT	B2 error counter register	R	8	00H
(16)	00F	08F	10F	18F	B3ECT	B3 error counter register	R	8	00H
(17)	010	090	110	190	LRECT	Line REI counter register	R	8	00H
(18)	011	091	111	191	PRECT	Path REI counter register	R	8	00H
(19)	012	092	112	192	FJCT	Frequency Justification counter register	R	8	00H
(20)	013	093	113	193	HECCT	HEC error dropped cell counter register	R	8	00H
(21)	014	094	114	194	FULCT	FIFO full dropped cell counter register	R	8	00H
(22)	015	095	115	195	IDLCT	Receive idle cell counter register	R	8	00H
(23)	016	096	116	196	INFCT	Receive valid cell counter register	R	8	00H
(24)	017-018	097-098	117-118	197-198	–	Reserved area	Prohibited	8	–
(25)	019	099	119	199	PCPR1	Indicates read byte position of counter.	R	8	00H
(26)	01A	099	11A	19A	PCPR2	Indicates read byte position of counter.	R	8	00H
(27)	01B	09A	11B	19B	PCSR	Sets sample timing of counter.	R/W	1	00H
(28)	01C	09C	11C	19C	PCIR1	Sets initialization of counters.	R/W	6	00H
(29)	01D	09D	11D	19D	PCIR2	Sets initialization of counters.	R/W	4	00H
(30)	01E	09E	11E	19E	PCFR1	Enables counters.	R/W	6	FFH
(31)	01F	09F	11F	19F	PCFR2	Enables counters.	R/W	4	FFH
(32)	020	0A0	120	1A0	PCOCR1	Indicates cause of counter overflow.	R	6	00H

(2/3)

No.	Address (H)				Name	Function	R/W	Number of Bits	Default
	Port 0	Port 1	Port 2	Port 3					
(33)	021	0A1	121	1A1	PCOCR2	Indicates cause of counter overflow.	R	4	00H
(34)	022	0A2	122	1A2	PCOMR1	Masks cause of counter overflow.	R/W	6	FFH
(35)	023	0A3	123	1A3	PCOMR2	Masks cause of counter overflow.	R/W	4	FFH
(36)	024	0A4	124	1A4	AMPR	Selects PALM pin to be set.	R/W	2	00H
(37)	025	0A5	125	1A5	AMR1	Masks alarm to be output from PALM pin.	R/W	8	FFH
(38)	026	0A6	126	1A6	AMR2	Masks alarm to be output from PALM pin.	R/W	8	FFH
(39)	027	0A7	127	1A7	DCHPR	Sets drop cell header pattern.	R/W	8	01H
(40)	028	0A8	128	1A8	DCHPMR	Masks drop cell header pattern.	R/W	8	00H
(41)	029	0A9	129	1A9	PHYIDR	Sets PHY ID address.	R/W	6	01H
(42)	02A	0AA	12A	1AA	J0R	Drop register of receive J0 byte	R	8	00H
(43)	02B	0AB	12B	1AB	Z0#1R	Drop register of receive 1st Z0 byte	R	8	00H
(44)	02C	0AC	12C	1AC	Z0#2R	Drop register of receive 2nd Z0 byte	R	8	00H
(45)	02D	0AD	12D	1AD	F1R	Drop register of receive F1 byte	R	8	00H
(46)	02E	0AE	12E	1AE	K1R	Drop register of receive K1 byte	R	8	00H
(47)	02F	0AF	12F	1AF	K2R	Drop register of receive K2 byte	R	8	00H
(48)	030	0B0	130	1B0	C2R	Drop register of receive C2 byte	R	8	00H
(49)	031	0B1	131	1B1	F2R	Drop register of receive F2 byte	R	8	00H
(50)	032	0B2	132	1B2	H4R	Drop register of receive H4 byte	R	8	00H
(51)	033	0B3	133	1B3	J0T	Insert register of transmit J0 byte	R/W	8	01H
(52)	034	0B4	134	1B4	Z0#1T	Insert register of transmit 1st Z0 byte	R/W	8	02H
(53)	035	0B5	135	1B5	Z0#2T	Insert register of transmit 2nd Z0 byte	R/W	8	03H
(54)	036	0B6	136	1B6	F1T	Insert register of transmit F1 byte	R/W	8	00H
(55)	037	0B7	137	1B7	K1T	Insert register of transmit K1 byte	R/W	8	00H
(56)	038	0B8	138	1B8	K2T	Insert register of transmit K2 byte	R/W	8	00H
(57)	039	0B9	139	1B9	C2T	Insert register of transmit C2 byte	R/W	8	13H
(58)	03A	0BA	13A	1BA	F2T	Insert register of transmit F2 byte	R/W	8	00H
(59)	03B	0BB	13B	1BB	H4T	Insert register of transmit H4 byte	R/W	8	00H
(60)	03C-03E	0BC-0BE	13C-13E	1BC-1BE	–	Reserved area	Prohib-ited	8	–
★ (61)	03F	0BF	13F	1BF	VERR	Stores version name of LSI.	R	3	××H
(62)	040	0C0	140	1C0	Z2#1R, Z2_6R	Drop register of receive 1st Z2 byte	R	8	00H
(63)	041	0C1	141	1C1	E1R	Drop register of receive E1 byte	R	8	00H
(64)	042	0C2	142	1C2	H1R	Drop register of receive 1st to 3rd H1 bytes	R	8	00H
(65)	043	0C3	143	1C3	H2R	Drop register of receive 1st to 3rd H2 bytes	R	8	00H
(66)	044	0C4	144	1C4	H3R	Drop register of receive 1st to 3rd H3 bytes	R	8	00H
(67)	045	0C5	145	1C5	B2R	Drop register of receive 1st to 3rd B2 bytes	R	8	00H
(68)	046	0C6	146	1C6	S1R	Drop register of receive S1 byte	R	8	00H
(69)	047	0C7	147	1C7	M1R	Drop register of receive M1 byte	R	8	00H

(3/3)

No.	Address (H)				Name	Function	R/W	Number of Bits	Default
	Port 0	Port 1	Port 2	Port 3					
(70)	048	0C8	148	1C8	E2R	Drop register of receive E2 byte	R	8	00H
(71)	049	0C9	149	1C9	J1R	Drop register of receive J1 byte	R	8	00H
(72)	04A	0CA	14A	1CA	B3R, Z2#_12	Drop register of receive B3 byte	R	8	00H
(73)	04B	0CB	14B	1CB	G1R	Drop register of receive G1 byte	R	8	00H
★ (74)	04C	0CC	14C	1CC	DsecR	Drop register of receive D3 to D1 bytes	R	8	00H
★ (75)	04D	0CD	14D	1CD	DlineR	Drop register of receive D12 to D4 bytes	R	8	00H
(76)	04E	0CE	14E	1CE	Z345R	Drop register of receive Z3 to Z5 bytes	R	8	00H
(77)	04F	0CF	14F	1CF	–	Reserved area	Prohib-ited	8	–
(78)	050	0D0	150	1D0	Z2#1T	Insert register of transmit 1st Z2 byte	R/W	8	00H
(79)	051	0D1	151	1D1	E1T	Insert register of transmit E1 byte	R/W	8	00H
(80)	052	0D2	152	1D2	H1T	Insert register of transmit 1st to 3rd H1 bytes	R/W	8	00H
(81)	053	0D3	153	1D3	H2T	Insert register of transmit 1st to 3rd H2 bytes	R/W	8	00H
(82)	054	0D4	154	1D4	H3T	Insert register of transmit 1st to 3rd H3 bytes	R/W	8	00H
(83)	055	0D5	155	1D5	B2T	Insert register of transmit 1st to 3rd B2 bytes	R/W	8	00H
(84)	056	0D6	156	1D6	S1T	Insert register of transmit S1 byte	R/W	8	00H
(85)	057	0D7	157	1D7	–	Reserved area	Prohib-ited	8	–
(86)	058	0D8	158	1D8	E2T	Insert register of transmit E2 byte	R/W	8	00H
(87)	059	0D9	159	1D9	J1T	Insert register of transmit J1 byte	R/W	8	00H
(88)	05A	0DA	15A	1DA	B3T	Insert register of transmit B3 byte	R/W	8	00H
(89)	05B	0DB	15B	1DB	–	Reserved area	Prohib-ited	8	–
(90)	05C	0DC	15C	1DC	DsecT	Insert register of transmit D1 to D3 bytes	R/W	8	00H
(91)	05D	0DD	15D	1DD	DlineT	Insert register of transmit D4 to D12 bytes	R/W	8	00H
(92)	05E	0DE	15E	1DE	Z345T	Insert register of transmit Z3, Z4, and Z5 bytes	R/W	8	00H
(93)	05F	0DF	15F	1DF	–	Reserved area	Prohib-ited	8	–
(94)	060	0E0	160	1E0	ROHPL	Pointer lock of receive H1, H2, and H3 drop registers	R/W	3	00H
(95)	061	0E1	161	1E1	ROHPR1	Pointer register of receive H1, H2, and H3 drop registers	R/W	8	00H
(96)	062	0E2	162	1E2	ROHPR2	Pointer register of receive DsecR, DlineR, and Z345R registers	R/W	8	00H
(97)	063	0E3	163	1E3	TOHPL	Pointer lock of transmit H1, H2, and H3 insert registers	R/W	3	00H
(98)	064	0E4	164	1E4	TOHPR1	Pointer register of transmit H1, H2, and H3 insert registers	R/W	8	00H
(99)	065	0E5	165	1E5	TOHPR2	Pointer register of transmit DsecT, DlineT, and Z345T registers	R/W	8	00H
(100)	066-06F	0E6-0EF	166-16F	1E6-1EF	–	Reserved area	Prohib-ited	8	–

5.1.2 Common Registers

No.	Address	Name	Function	R/W	Number of Bits	Default
(101)	06CH	SYSPR	Pointer register of threshold set register	R/W	6	00H
(102)	06DH	ITUR	Changes alarm detection conditions.	R/W	3	00H
(103)	06EH	B1THR	B1 error detection threshold set register	R/W	7	FFH
(104)	06FH	B2THR	B2 error detection threshold set register	R/W	8	FFH
(105)	070H	B3THR	B3 error detection threshold set register	R/W	8	FFH
(106)	071H	LRETHR	Line REI error detection threshold set register	R/W	6	FFH
(107)	072H	PRETHR	Path REI error detection threshold set register	R/W	6	FFH
(108)	073H	FJTHR	Frequency Justification detection threshold set register	R/W	3	FFH
(109)	074H	FRMN	Register which sets number of threshold monitor frames	R/W	7	00H
(110)	075H	CRSC	Receive clock recovery control register	R/W	7	00H
(111)	076H	CSSC	Clock synthesizer source set register	R/W	8	00H
(112)	077H	TXSC	Transmit clock source control register	R/W	8	00H
(113)	078H	AVLC	UTOPIA interface relating register	R/W	6	00H
(114)	079H	MltUT	Multi-PHY mode switch register	R/W	6	00H
(115)	07AH	TCMSK	Transmit operation clock output select register	R/W	3	00H
(116)	07BH	RCMSK	Recovery clock output register	R/W	6	01H
(117)	07CH	FPMSK	Frame pulse output register	R/W	6	00H
(118)	07DH	–	Reserved area	Prohib-ited	8	–
★ (119)	07EH	ICNT	Software reset/interrupt mode register	R/W	2	00H
(120)	07FH	IMST	Interrupt port indication register	R	5	00H

5.2 Register Function

5.2.1 Port Register Function

(1) Command register 1 (CMR1)

This register sets transmission of alarm signals such as Line AIS, Path AIS, Line RDI, and Path RDI. It also sets the PALM pin output level.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
CMR1	TAPS	CMD3	CMD2	CMD1	TLAIS	TPAIS	TLRDI	TPRDI	Port0:000H Port1:080H Port2:100H Port3:180H	00H	R/W

Field	Function	Default Value
D7: TAPS	When 1 is written to this bit, the values of the K1T and K2T registers are loaded into the K1 and K2 byte positions of the transmit overhead and then transferred. When the values of the K1T and K2T registers are changed, the new values are re-loaded into the transmit overhead by writing 1 to this bit again. When 0 is written to this bit, the loading of values into the K1T and K2T registers is stopped. The value of this bit is 0 when read after 1 has been written to it. The value of this bit is not retained.	0
D6-D4: CMD3-CMD1	Changes in these bits can be reflected on the output level of the PALM pin. The relationship between these bits and the PALM pin is specified by AMPR, AMR1, and AMR2. 1: Outputs high level to PALM[2:0]. 0: Outputs low level to PALM[2:0].	0
D3: TLAIS	When this bit is set to 1, alarm frame of Line AIS is transmitted. Line AIS transmission continues until this bit is cleared to 0.	0
D2: TPAIS	When this bit is set to 1, alarm frame of Path AIS is transmitted. Path AIS transmission continues until this bit is cleared to 0.	0
D1: TLRDI	When this bit is set to 1, alarm frame of Line RDI is transmitted. Line RDI transmission continues until this bit is cleared to 0.	0
D0: TPRDI	When this bit is set to 1, alarm frame of Path RDI is transmitted. Path RDI transmission continues until this bit is cleared to 0.	0

Remark If Line AIS and Line RDI are set in the same frame, Line AIS takes precedence.

(2) Command register 2 (CMR2)

This register disables the transmit/receive function and initializes the ports.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
CMR2	0	0	TDIS	RDIS	ALL	ICR	PCCR	ALR	Port0:001H Port1:081H Port2:101H Port3:181H	00H	R/W

Field	Function	Default Value
★ D7, D6	Always keep these bit areas cleared to 0.	00
D5: TDIS	Disables the transmit function. While this bit is set to 1, the transmit frame processing block stops. While the block is not operating, all 0 transmit data is output continuously. Stopping the transmission does not affect the register setting and therefore, set modes are retained. If the transmission is enabled again by clearing this bit to 0, the operation resumes in the mode set before the transmission was disabled.	0
D4: RDIS	Disables the receive function. While this bit is set to 1, the receive frame processing block and receive clock recovery PLL stop. As stopping of the receive block operations does not affect the register setting, when it is enabled again by clearing this bit to 0, the ★ operation resumes in the mode set before the reception was disabled. Even if this bit is set to 1, an attempt to detect line failure LOS and LOF continues, and therefore the interrupt cause register may be set depending on the state of the line.	0
D3: ALL	Software reset of port. When this bit is set to 1, all the logic and registers of the port are initialized. This bit is automatically cleared to 0 after a reset has been executed. ★ No common register is reset.	0
D2: ICR	Resets the interrupt cause register. When this bit is set to 1, the bits of the interrupt cause register and cause detail register are cleared. This bit is automatically cleared to 0 after a reset.	0
D1: PCCR	Resets the performance counter. When this bit is set to 1, all the registers related to the performance counter are reset. This bit is automatically cleared to 0 after a reset.	0
D0: ALR	Resets the port registers. When this bit is set to 1, all the port registers are reset. This bit is automatically cleared to 0 after a reset.	0

★ **Caution Once the interrupt cause register is cleared using the ICR bit, however, the bits will not be set again even if the event detection status lasts; they will be set again only when the event is detected again after recovery from it.**

★ **Remark** The command for resetting the entire LSI chip is in the ICNT register (07EH).

(3) Command register 3 (CMR3)

This register is used to transmit a pseudo frame that allows the targeted device to detect a failure or error during test.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
CMR3	0	0	0	CM4	CM3	CM2	CM1	CM0	Port0:002H Port1:082H Port2:102H Port3:182H	00H	R/W

Field	Function	Default Value
★ D7-D5	Always keep these bit areas cleared to 0.	000
D4-D0: CM4-CM0	Transmits the pseudo frame.	All 0

CM4-CM0	Transmit Frame
00000	Disables transmission of the pseudo frame (normal).
00001	Transmits PLOS frame.
00010	Transmits POOF frame.
00011	
00100	Transmits PLOP frame.
00101	Transmits POCD frame.
00110	
00111	Transmits PB1 frame.
01000	Transmits PB2 frame.
01001	Transmits PB3 frame.
01010	Transmits PLREI frame.
01011	Transmits PPREI frame.
10001	Transmits APS frame. (equivalent to TAPS of CMR1)
10010	Transmits PLOP II frame.
10100	Transmits PB2 II frame.
10101	Transmits PB3 II frame.
Others	Setting prohibited

For details of the contents of transmitted pseudo frames, see **(3)** in **Section 3.3.1**.

(4) Mode register 1 (MDR1)

This register sets the SS bit of the AU pointer in the transmit overhead.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
MDR1	0	SS1	SS0	0	0	0	0	0	Port0:003H Port1:083H Port2:103H Port3:183H	00H	R/W

Field	Function	Default Value
★ D7, D4-D0	Always keep these bit areas cleared to 0.	All 0
D6: SS1 D5: SS0	Sets SS bit code of 1st to 3rd H1 bytes of overhead of transmit frame.	00

	B7	B6	B5	B4	B3	B2	B1	B0
1st H1	0	1	1	0	SS1	SS0	1	0
2nd H1	1	0	0	1	SS1	SS0	1	1
3rd H1	1	0	0	1	SS1	SS0	1	1

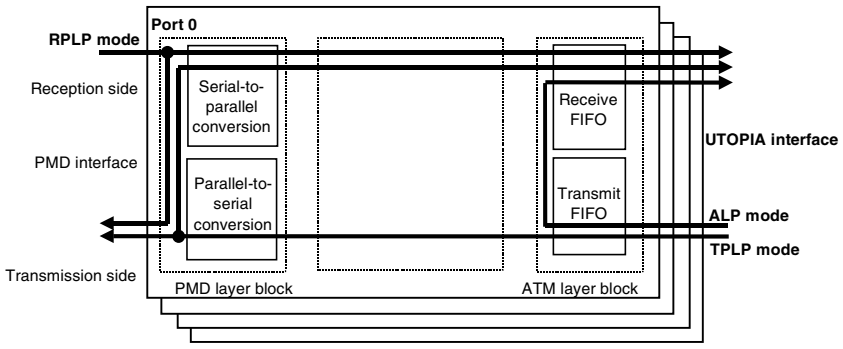
(5) Mode register 2 (MDR2)

This register sets loopback mode.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
MDR2	MGM	0	0	LP1	LP0	0	0	0	Port0:004H Port1:084H Port2:104H Port3:184H	00H	R/W

Field	Function	Default Value
★ D7: MGM	When this bit is set to 1: **<1>** The Z2#1R register is caused to function as the Z2_6R register, and the B3R register is caused to function as the Z2_12R register. **<2>** The functions of the D7:Z2_6 and D6:Z2_12 bits of the PCOCR2 register and the D7:Z2_6m and D6:Z2_12m bits of the PCOMR2 register are enabled.	0
★ D6, D5, D2-D0	Always keep these bit areas cleared to 0.	All 0
D4: LP1 D3: LP0	Sets loopback mode.	00

LP[1:0]	Mode
00	Normal mode (Normal)
01	**RPLP mode** Sets loopback from PMD side input to PMD side output via serial/parallel converter circuit.
10	**TPLP mode** Sets loopback from ATM side input to ATM side output via serial/parallel converter circuit.
11	**ALP mode** Sets loopback from ATM side input to ATM side output via receive FIFO and transmit FIFO.



(6) Mode register 3 (MDR3)

This register enables or disables frames and cell scrambling, and sets the mode of HEC processing.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
MDR3	0	FSCR	CSCR	HECE	CORE	0	0	RAPSC	Port0:005H Port1:085H Port2:105H Port3:185H	00H	R/W

Field	Function	Default Value
★ D7, D2, D1	Always keep these bit areas cleared to 0.	All 0
D6: FSCR	Disables frame scramble/descramble. When this bit is set to 1, transmit frame is not scrambled, and receive frame is not descrambled.	0
D5: CSCR	Disables cell scramble/descramble. When this bit is set to 1, transmit cell is not scrambled, and receive cell is not descrambled.	0
D4: HECE	Disables HEC error cell drop function. When this bit is set to 1, a cell in which an error of two bits or more has been detected as a result of HEC verification, is not dropped but output from the UTOPIA interface.	0
D3: CORE	Disables HEC error cell correct function. When this bit is set to 1 and a one-bit error is detected as a result of HEC verification, the error is not corrected and the cell is dropped.	0
D0: RAPSC	Clears the RAPS bit of the PCR register. When this bit is set to 1, the RAPS bit of the PCR register is cleared. This bit is automatically cleared to 0 after the RAPS bit is cleared.	0

(7) PHY interrupt cause register (PICR)

This register indicates the cause of an interrupt request (output from the PHINT_B pin).

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PICR	OOL	exCMD	LOS	LOF	ALM	PFM	PCO	RFO	Port0:006H Port1:086H Port2:106H Port3:186H	00H	R

Field	Function	Default Value
D7: OOL	Indicates the clock recovery status. When this bit is 1, it indicates that the phase difference between the clock extracted by the clock recovery PLL and receive data has shifted through 180 degrees.	0
D6: exCMD	Indicates the input level of the CMD pin. When this bit is 1, it indicates that the CMD pin input has gone high.	0
D5: LOS	Indicates the LOS occurrence status. When this bit is 1, it indicates that LOS (Loss Of Signal) has occurred.	0
D4: LOF	Indicates the LOF occurrence status. When this bit is 1, it indicates that LOF (Loss Of Frame) has occurred.	0
D3: ALM	Indicates the ACR register status. This bit indicates that one or more bits of the ACR register have been set to 1.	0
D2: PFM	Indicates status of PCR register. This bit indicates that one or more bits of the PCR register have been set to 1.	0
D1: PCO	Indicates the status of the PCOCR1 and PCOCR2 registers. When this bit is 1, it indicates that one or more bits of the PCOCR1 and PCOCR2 registers have been set to 1.	0
D0: RFO	Indicates the overflow history in the receive FIFO. When this bit is 1, it indicates that overflow has occurred in receive FIFO.	0

Remarks 1. In RCM = 0 mode, PHINT_B goes low if even one of the bits of this register (ICNT register) is set to 1. In RCM = 1 mode, PHINT_B goes low when a bit of this register changes its value (0 → 1 or 1 → 0). If, however, the bits masked by the PIMR register change their status, PHINT_B does not go low.

2. Those bits that have been set are cleared when they are read. The clear condition, however, differs depending on the setting of the RCM bit of the ICNT register. See **Section 4.4.3**.

(8) PHY interrupt mask register (PIMR)

This register masks the PICR register.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PIMR	OOL	exCMD	LOS	LOF	ALM	PFM	PCO	RFO	Port0:007H Port1:087H Port2:107H Port3:187H	FFH	R/W

Field	Function	Default Value
D7: OOL D6: exCMD D5: LOS D4: LOF D3: ALM D2: PFM D1: PCO D0: RFO	Masks the PICR register. Of these bits, the one that has been set to 1 prevents PHINT_B from going low even if the corresponding bit of the PICR register is set to 1.	All 1

(9) Alarm cause register (ACR)

This register indicates the details of a line failure that has occurred.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
ACR	OOF	LOP	OCD	LCD	LAIS	PAIS	LRDI	PRDI	Port0:008H Port1:088H Port2:108H Port3:188H	00H	R

Field	Function	Default Value
D7: OOF	Status of OOF (Out Of Frame). When this bit is 1, it indicates that the port is or has been in the OOF status.	0
D6: LOP	Status of LOP (Loss Of Pointer). When this bit is 1, it indicates that the port is or has been in the LOP status.	0
D5: OCD	Indicates OCD (Out of Cell Delineation). When this bit is 1, it indicates that the port is or has been in the OCD status.	0
D4: LCD	Status of LCD (Loss of Cell Delineation). When this bit is 1, it indicates that LCD is or has been detected.	0
D3: LAIS	Status of Line AIS reception. When this bit is 1, it indicates that Line AIS is or has been received.	0
D2: PAIS	Status of Path AIS reception. When this bit is 1, it indicates that Path AIS is or has been received.	0
D1: LRDI	Status of Line RDI reception. When this bit is 1, it indicates that Line RDI is or has been received.	0
D0: PRDI	Status of Path RDI reception. When this bit is 1, it indicates that Path RDI is or has been received.	0

Remarks 1. If even one of the bits of this register is set to "1", the ALM bit of the PICR register is set to 1. If the ALM bit is masked by the ACMR register, it is not set. When all the bits of the ACR register are cleared to 0, the ALM bit of the PICR register is also cleared to 0.

2. Those bits that have been set are cleared when they are read. The clear condition, however, differs depending on the setting of the RCM bit of the ICNT register. See **Section 4.4.3**.

(10) Alarm cause mask register (ACMR)

This bit masks reflection of the ALM bit of the PICR register for each event when a bit of the ACR register is set.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
ACMR	OOF	LOP	OCD	LCD	LAIS	PAIS	LRDI	PRDI	Port0:009H Port1:089H Port2:109H Port3:189H	FFH	R/W

Field	Function	Default Value
D7: OOF D6: LOP D5: OCD D4: LCD D3: LAIS D2: PAIS D1: LRDI D0: PRDI	Masks the ACR register. When any of these bits is set to 1, the ALM bit of the PICR register is not set, even when the corresponding bit of the ACR register changes its status.	All 1

(11) Performance cause register (PCR)

This register indicates detail causes of performance.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCR	RAPS	0	FJ	B1E	B2E	B3E	LREI	PREI	Port0:00AH Port1:08AH Port2:10AH Port3:18AH	00H	R

Field	Function	Default Value
D7: RAPS	Indicates the status of APS reception. [Condition for putting the μPD98411 in the APS reception status] The μPD98411 has an internal register for holding the current values of the K1 and K2 bytes. It compares the current K1 and K2 byte values with the newly received K1 and K2 byte values in each frame. If the μPD98411 receives the same K1 and K2 byte values that are not all 0s and different from the current values three times consecutively, it enters the APS reception status and updates the current-value register, and then sets RAPS. [Condition for exiting the RAPS status] **<1>** When K1 and K2 byte values that are not all 0s are received three times consecutively. **<2>** When the RAPSC bit of MDR3 is set. The RAPS is not read-cleared while the μPD98411 is in the APS reception status. It is cleared when it is read after the μPD98411 exits the RAPS reception status.	0
D5: FJ	Indicates history of FJ (Frequency Justification). When this bit is 1, it indicates that the FJ operation has been performed.	0
D4: B1E	Indicates history of B1 error. When this bit is 1, it indicates that a B1 error has been detected.	0
D3: B2E	Indicates history of B2 error. When this bit is 1, it indicates that a B2 error has been detected.	0
D2: B3E	Indicates history of B3 error. When this bit is 1, it indicates that a B3 error has been detected.	0
D1: LREI	Indicates history of Line REI. When this bit is 1, it indicates that Line REI has been detected.	0
D0: PREI	Indicates history of Path REI. When this bit is 1, it indicates that Path REI has been detected.	0

Remarks 1. If even one of the bits of this register is set to "1", the PFM bit of the PICR register is set to 1.

2. The RAPS bit is also set when the alarm indication frame of Line AIS and Line RDI, transmitted via the K2 byte, has been received.

(12) Performance cause mask register (PCMR)

This register masks reflection of the setting of a bit of the PCR register on the PFM bit of the PICR register for each event.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCMR	RAPS	1	FJ	B1E	B2E	B3E	LREI	PREI	Port0:00BH Port1:08BH Port2:10BH Port3:18BH	FFH	R/W

Field	Function	Default Value
★ D6	Always keep these bit areas set to 1.	1
D7: RAPS D5: FJ D4: B1E D3: B2E D2: B3E D1: LREI D0: PREI	Masks the PCR register. When any of these bits is set to 1, the PFM bit of the PICR register is not set even if the corresponding bit of the PCR register is set.	All 1

(13) Internal alarm cause mask register (IACM)

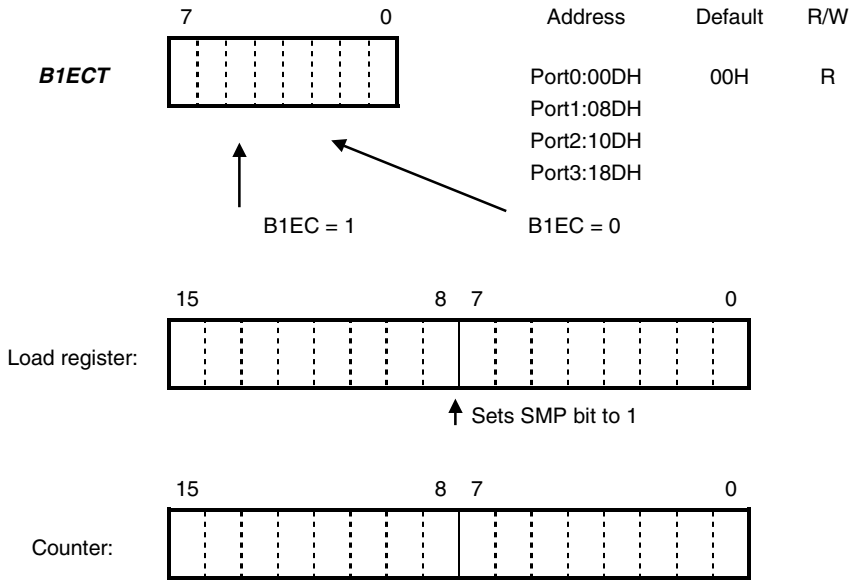
This register unmasks the functions related to automatic return transmission of Line RDI and Path RDI.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
IACM	1	1	1	1	1	SDm	LRDIm	PRDIm	Port0:00CH Port1:08CH Port2:10CH Port3:18CH	FFH	R/W

Field	Function	Default Value
★ D7-D3	Always keep these bit areas set to 1.	All 1
★ D2: SDm	Masks detection of LOS when there is an input to the SD pin. 1: The LOS bit of the PICR register is not set to 1 even when the SD pin goes low. 0: The LOS bit of the PICR register is set to 1 when the SD pin goes low.	1
D1: LRDIm	When this bit is cleared to 0, Line RDI is automatically transmitted by the transmission side if LOS, LOF, or Line AIS is detected at the reception side. When it is set to 1, the return transmission of Line RDI is masked.	1
D0: PRDIm	When this bit is cleared to 0, Path RDI is automatically transmitted by the transmission side if LOS, LOF, Line AIS, LOP, LCD, or Path AIS is detected at the reception side. When it is set to 1, the return transmission of Path RDI is masked.	1

(14) B1 error count register (B1ECT)

This register reads the total number of detected B1 errors.



This register is a register that is used to read the value of the 16-bit B1 error counter in eight-bit units. To obtain a count, first set the **SMP** bit of the **PCSR** register to 1 and save the count into the load register. At this time, the counter is cleared to 0. The value saved into the load register is retained until overwritten.

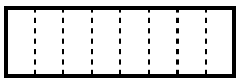
When this register read, the low-order eight bits are read first, and then the high-order eight bits are read. Whether the low-order or high-order eight bits are read when this register is read next time is indicated by the **B1EC** bit of the **PCPR1** register. Each time the B1ECT register has been read, the B1EC bit automatically changes from 0 to 1 and then back to 0 again. 0 indicates that the low-order eight bits are read and 1 indicates that the high-order eight bits are read.

When the count value passes all F, a counter overflow is assumed. As a result, the **B1EC** bit of **PCIR1** is set and the **PCO** bit of the **PICR** register is set. This setting of the PCO bit can be used as an interrupt cause. The counter whose value has reached all F continues counting up from 0.

If the error rate monitor function is enabled, whether the count value reaches the threshold value before the number of frames set to the **FRMN** register is received is checked. When the **SMP** bit of the **PCSR** register is set, all the counters are cleared to 0 and, therefore, the error rate is checked again starting from the beginning.

(15) B2 error count register (B2ECT)

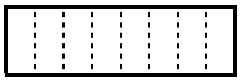
This register is a register that is used to read the value of the 24-bit B2 error counter in three parts of eight bits each. When this register read, the count value is read in the order of the low-order, middle-order, then high-order eight bits.



	Address	Default	R/W
B2ECT	Port0:00EH Port1:08EH Port2:10EH Port3:18EH	00H	R

(16) B3 error count register (B3ECT)

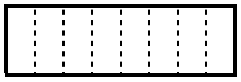
This register is a register that is used to read the value of the 16-bit B3 error counter in eight-bit units. When this register read, the low-order eight bits are read first, and then the high-order eight bits are read.



	Address	Default	R/W
B3ECT	Port0:00FH Port1:08FH Port2:10FH Port3:18FH	00H	R

(17) Line REI count register (LRECT)

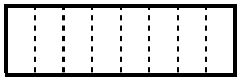
This register is a register that is used to read the value of the 24-bit Line REI counter in three parts of eight bits each. When this register read, the low-order eight bits are read first, the middle-order eight bits, and then the high-order eight bits are read.



	Address	Default	R/W
LRECT	Port0:010H Port1:090H Port2:110H Port3:190H	00H	R

(18) Path REI count register (PRECT)

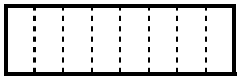
This register is a register that is used to read the value of the 16-bit Path REI counter in eight-bit units. When this register read, the low-order eight bits are read first, and then the high-order eight bits are read.



	Address	Default	R/W
PRECT	Port0:011H Port1:091H Port2:111H Port3:191H	00H	R

(19) Frequency Justification count register (FJCT)

This register is a register that is used to read the value of the 16-bit Frequency Justification operation counter in eight-bit units. When this register read, the low-order eight bits are read first, and then the high-order eight bits are read.



	Address	Default	R/W
FJCT	Port0:012H Port1:092H Port2:112H Port3:192H	00H	R

(20) HEC error count register (HECCT)

This register is a register that is used to read the value of a 24-bit counter in three blocks of eight bits each. The counter indicates the total number of cells that were dropped when HEC errors were detected. This register is read in the order of the low-order, middle-order, then high-order eight bits.

	Address	Default	R/W
HECCT	Port0:013H Port1:093H Port2:113H Port3:193H	00H	R

(21) FIFO full count register (FULCT)

This register is a register that is used to read the value of a 24-bit counter in three blocks of eight bits each. The counter indicates the total number of cells that were dropped when a receive FIFO overrun occurred. This register is read in the order of the low-order, middle-order, then high-order eight bits.

	Address	Default	R/W
FULCT	Port0:014H Port1:094H Port2:114H Port3:194H	00H	R

(22) Idle cell (vacant cell) count register (IDLCT)

This register is a register that is used to read the value of a 24-bit counter in three blocks of eight bits each. The counter indicates the total number of idle cells that were received. This register is read in the order of the low-order, middle-order, then high-order eight bits.

When the mode in which unassigned cells are to be dropped is set using the DCHPR register, the number of unassigned cells that were dropped is also added to this counter.

	7		0	Address	Default	R/W
IDLCT				Port0:015H Port1:095H Port2:115H Port3:195H	00H	R

(23) Information cell count register (INFCT)

This register is a register that is used to read the value of a 24-bit counter in three blocks of eight bits each. The counter indicates the total number of cells that were normally received and transferred via the UTOPIA interface. This register is read in the order of the low-order, middle-order, then high-order eight bits.

When the mode in which unassigned cells are not to be dropped is set using the DCHPR register, the number of unassigned cells that were received is also added to this counter.

	7		0	Address	Default	R/W
INFCT				Port0:016H Port1:096H Port2:116H Port3:196H	00H	R

(24) Reserved area

- Address: 017H and 018H, 097H to 116H, 117H and 118H, 196H and 197H
- Do not read from or write to this area.

(25) Performance counter point register 1 (PCPR1)

This register indicates the byte position of the counter to be read next when the counter register is read.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCPR1	B1EC	B2EC1	B2EC0	B3EC	LREC1	LREC0	PREC	FJC	Port0:019H Port1:099H Port2:119H Port3:199H	00H	R

Field	Function		Default Value
D7: B1EC	Indicates which bits of B1 error counter are to be read next.		0
	1	High-order eight bits are read next.	
	0	Low-order eight bits are read next.	
D6: B2EC1 D5: B2EC0	Indicates which bits of B2 error counter are to be read next.		00

B2EC[1:0]	Bits to Be Read Next
00	Low-order eight bits
01	Middle-order eight bits
10	High-order eight bits

D4: B3EC	Indicates which bits of B3 error counter are to be read next.		0
	1	High-order eight bits are read next.	
	0	Low-order eight bits are read next.	
D3: LREC1 D2: LREC0	Indicates which bits of Line REI counter are to be read next.		00

LREC[1:0]	Bits to Be Read Next
00	Low-order eight bits
01	Middle-order eight bits
10	High-order eight bits

D1: PREC	Indicates which bits of Path REI counter are to be read next.		0
	1	High-order eight bits are read next.	
	0	Low-order eight bits are read next.	
D0: FJC	Indicates which bits of FJ counter are to be read next.		0
	1	High-order eight bits are read next.	
	0	Low-order eight bits are read next.	

(26) Performance counter point register 2 (PCPR2)

This register indicates which byte of a load register corresponding to each window register is to be read next.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCPR2	HECC1	HECC0	FULC1	FULC0	IDLC1	IDLC0	INFC1	INFC0	Port0:01AH Port1:09AH Port2:11AH Port3:19AH	00H	R

Field	Function	Default Value
D7: HECC1 D6: HECC0	These bits indicate the portion of the 24-bit counter that is to be read when the HEC counter (HECCT register) is next read. 00: Low-order eight bits [23:16] 01: Middle-order eight bits [15:8] 10: High-order eight bits [7:0]	00
D5: FULC1 D4: FULC0	These bits indicate the portion of the 24-bit counter that is to be read when the FIFO full counter (FULCT register) is next read. 00: Low-order eight bits [23:16] 01: Middle-order eight bits [15:8] 10: High-order eight bits [7:0]	00
D3: IDLC1 D2: IDLC0	These bits indicate the portion of the 24-bit counter that is to be read when the idle cell counter (IDLCT register) is next read. 00: Low-order eight bits [23:16] 01: Middle-order eight bits [15:8] 10: High-order eight bits [7:0]	00
D1: INFC1 D0: INFC0	These bits indicate the portion of the 24-bit counter that is to be read when the information cell counter (INFCT register) is next read. 00: Low-order eight bits [23:16] 01: Middle-order eight bits [15:8] 10: High-order eight bits [7:0]	00

(27) Performance counter sample register (PCSR)

This register sets the performance counter sample timing. When the SMP bit of this register is set to 1, the values of all the counters are stored to the corresponding load registers, and the count values are cleared to 0.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCSR	0	0	0	0	0	0	0	SMP	Port0:01BH Port1:09BH Port2:11BH Port3:19BH	00H	R/W

Field	Function	Default Value
★ D7-D1	Always keep these bit areas cleared to 0.	All 0
D0: SMP	Stores contents of all counters to corresponding load registers when set to 1. At this time, all the counters are cleared to 0. After the contents of the counters have been loaded into the load registers, this bit is automatically cleared to 0. If this bit is set to 1 when the error rate monitor function is used, the counter is cleared to 0, making it impossible to correctly check the error rate.	0

(28) Performance counter initialization register 1 (PCIR1)

This register is used to initialize each performance counter. It clears the counter and load register to 0.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCIR1	0	0	B1EC	B2EC	B3EC	LREC	PREC	FJC	Port0:01CH Port1:09CH Port2:11CH Port3:19CH	00H	R/W

Field	Function	Default Value
★ D7, D6	Always keep these bit areas cleared to 0.	00
D5: B1EC D4: B2EC D3: B3EC D2: LREC D1: PREC D0: FJC	When any of these bits is set to 1, the corresponding counter and load register are cleared to 0. The bit that has been set is automatically cleared to 0.	All 0

(29) Performance counter initialization register 2 (PCIR2)

This register is used to initialize each performance counter. It clears the counter and load register to 0.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCIR2	0	0	0	0	HECC	FULC	IDLC	INFC	Port0:01DH Port1:09DH Port2:11DH Port3:19DH	00H	R/W

Field	Function	Default Value
★ D7-D4	Always keep these bit areas cleared to 0.	All 0
D3: HECC D2: FULC D1: IDLC D0: INFC	When any of these bits is set to 1, the corresponding counter and load register are cleared to 0. The bit that has been set is automatically cleared to 0.	All 0

(30) Performance counter stop register 1 (PCFR1)

By default, all the counters are disabled at power-on. This register is used to enable the counter to be used.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCFR1	1	1	B1EC	B2EC	B3EC	LREC	PREC	FJC	Port0:01EH Port1:09EH Port2:11EH Port3:19EH	FFH	R/W

Field	Function	Default Value
★ D7, D6	Always keep these bit areas set to 1.	All 1
D5: B1EC D4: B2EC D3: B3EC D2: LREC D1: PREC D0: FJC	These bits enable or disable the counters. 0: Counter is enabled and starts counting. 1: Counter is disabled and stops counting.	All 1

(31) Performance counter stop register 2 (PCFR2)

By default, all the counters are disabled at power-on. This register is used to enable the counter to be used.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCFR2	1	1	1	1	HECC	FULC	IDLC	INFC	Port0:01FH Port1:09FH Port2:11FH Port3:19FH	FFH	R/W

Field	Function	Default Value
★ D7-D4	Always keep these bit areas set to 1.	All 1
D3: HECC D2: FULC D1: IDLC D0: INFC	These bits enable or disable the counters. 0: Counter is enabled and starts counting. 1: Counter is disabled and stops counting.	All 1

(32) Performance counter overflow cause register 1 (PCOCR1)

This register indicates that the value of the performance counter has passed all F or that the count has reached the threshold value when the error rate monitor function is enabled. If even one of the bits of this register is set to 1, the PCO bit of the PICR register is set.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCOCR1	0	0	B1EC	B2EC	B3EC	LREC	PREC	FJC	Port0:020H Port1:0A0H Port2:120H Port3:1A0H	00H	R

Field	Function	Default Value
D5: B1EC D4: B2EC D3: B3EC D2: LREC D1: PREC D0: FJC	Setting these bits indicates that the count has passed all F. When the error rate monitor function is enabled, it indicates that the count has reached the threshold value (set by the B1THR register) within the number of frames set with the FRMN register. If any of the bits of this register is set, the PCO bit of PICR is set. If the bit is masked by the PCOMR1 register, however, the PCO bit is not set even if the bit is set. This register is cleared to 0 when read.	All 0

(33) Performance counter overflow cause register 2 (PCOCR2)

This register indicates that the value of the performance counter has passed all F. If any of the bits of this register is set, the PCO bit of the PICR register is set.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCOCR2	Z2_6	Z2_12	0	0	HECC	FULC	IDLC	INFC	Port0:021H Port1:0A1H Port2:121H Port3:1A1H	00H	R

Field	Function	Default Value
★ D7: Z2_6	Setting this bit indicates that the Z2_6 register has been updated. The bit is valid only when the MGM bit of the MDR2 register is 1.	0
★ D6: Z2_12	Setting this bit indicates that the Z2_12 register has been updated. The bit is valid only when the MGM bit of the MDR2 register is 1.	0
D3: HECC D2: FULC D1: IDLC D0: INFC	Setting these bits indicates that the value of the corresponding counter has passed all F. If any of the bits of this register is set, the PCO bit of PICR is set. If the bit is masked by the PCOMR1 register, however, the PCO bit is not set even if the bit is set. This register is cleared to 0 when it is read.	All 0

(34) Performance counter overflow mask register 1 (PCOMR1)

This register masks reflecting of the setting of a bit of the PCOCR1 register on the PCO bit of the PICR register.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCOMR1	1	1	B1EC	B2EC	B3EC	LREC	PREC	FJC	Port0:022H Port1:0A2H Port2:122H Port3:1A2H	FFH	R/W

Field	Function	Default Value
★ D7, D6	Always keep these bit areas set to 1.	All 1
D5: B1EC D4: B2EC D3: B3EC D2: LREC D1: PREC D0: FJC	When any of these bits is set to 1, the PCO bit of the PICR register is not set to 1 even if the corresponding bit of the PCOCR1 register is set.	All 1

(35) Performance counter overflow mask register 2 (PCOMR2)

This register masks reflecting of the setting of a bit of the PCOCR2 register on the PCO bit of the PICR register.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PCOMR2	Z2_6m	Z2_12m	1	1	HECC	FULC	IDLC	INFC	Port0:023H Port1:0A3H Port2:123H Port3:1A3H	FFH	R/W

	Field	Function	Default Value
★	D7: Z2_6m D6: Z2_12m	When any of these bits is set to 1, the PCO bit of the PICR register is not set to 1 even if the corresponding bit of PCOCR2 register is set. The bit is valid only when the MGM bit of the MDR2 register is 1.	All 1
★	D5, D4	Always keep these bit areas set to 1.	
★	D3: HECC D2: FULC D1: IDLC D0: INFC	When any of these bits is set to 1, the PCO bit of the PICR register is not set to 1 even if the corresponding bit of the PCOCR2 register is set.	All 1

(36) PALM pin set register (AMPR)

This register selects the PALM pin to be set to the AMR1 and AMR2 registers from the PALM[2:0] pins.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
AMPR	0	0	0	0	0	0	AMP1	AMP0	Port0:024H Port1:0A4H Port2:124H Port3:1A4H	00H	R/W

	Field	Function	Default Value
★	D7-D2	Always keep these bit areas cleared to 0.	All 0
	D1: AMP1 D0: AMP0	These bits specify one of the PALM2, PALM1, and PALM0 pins, to be set in the AMR1 and AMR2 registers.	00

AMP[1:0]	Selected PALM Pin
00	The PARM0 output pin is set.
01	The PARM1 output pin is set.
1×	The PARM2 output pin is set.

(37) Output alarm mask register 1 (AMR1)

This register selects the alarm or error to be output by the PALM pin specified by the AMPR register. If the event that is unmasked by this register is detected, the output signal of the PALM pin goes high to report the peripheral device.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
AMR1	OOL	exCMD	LOS	OOF	LOF	LOP	OCD	LCD	Port0:025H Port1:0A5H Port2:125H Port3:1A5H	FFH	R/W

Field	Function	Default Value
D7: OOL D6: exCMD D5: LOS D4: OOF D3: LOF D2: LOP D1: OCD D0: LCD	If an event corresponds to one of the bits that are cleared to 0, the PALM pin goes high while that event is detected. If two or more of these bits are cleared to 0, the events are ORed and output.	All 1

(38) Output alarm mask register 2 (AMR2)

This register selects the alarm or error to be output by the PALM pin specified by the AMPR register. If the event that is unmasked by this register is detected, the output signal of the PALM pin goes high to report the peripheral device.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
AMR2	CMD1	CMD2	CMD3	RAPS	LAIS	PAIS	LRDI	PRDI	Port0:026H Port1:0A6H Port2:126H Port3:1A6H	FFH	R/W

Field	Function	Default Value
D7: CMD1 D6: CMD2 D5: CMD3 D4: RAPS D3: LAIS D2: PAIS D1: LRDI D0: PRDI	If an event corresponds to one of the bits that are cleared to 0, the PALM pin goes high while that event is detected. If two or more of these bits are cleared to 0, the events are ORed and output.	All 1

(39) Drop cell header pattern register (DCHPR)

This register specifies the invalid cell to be dropped. Whether only idle cells, or both idle cells and unassigned cells are dropped can be selected.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
DCHPR	GFC3	GFC2	GFC1	GFC0	PTI2	PTI1	PTI0	CLP	Port0:027H Port1:0A7H Port2:127H Port3:1A7H	01H	R/W

Field	Function	Default Value
★ D7: GFC3 D6: GFC2 D5: GFC1 D4: GFC0 D3: PTI2 D2: PTI1 D1: PTI0 D0: CLP	The μPD98411 checks the pattern of the cell header before it saves the extracted receive cell to the receive FIFO. The cell in which the VPI/VCI field is all 0 compares the other header fields with the value set in this register. If a header field coincides with the value set in this register, the cell is not saved into the receive FIFO but is dropped.	01H

(40) Drop cell header pattern mask register (DCHPMR)

This register masks the DCHPR register.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
DCHPMR	GFC3	GFC2	GFC1	GFC0	PTI2	PTI1	PTI0	CLP	Port0:028H Port1:0A8H Port2:128H Port3:1A8H	FFH	R/W

Field	Function	Default Value
★ D7: GFC3 D6: GFC2 D5: GFC1 D4: GFC0 D3: PTI2 D2: PTI1 D1: PTI0 D0: CLP	When any of these bits is set to 1, the bits of the corresponding DCHPR register and the field corresponding to the bits of the receive cell while the VPI/VCI field is all 0 are not compared but ignored. Only the bit area that is cleared to 0 is compared.	All 1

Example of DCHPR Register Setting

DCHPR CLP Bit	DCHPMR CLP Bit	Dropped Cell
1	0	Idle cell (default)
0	0	Unassigned cell
×	1	Idle cell & unassigned cell

(41) PHY ID register (PHYIDR)

This register sets five port address bits that are used to select a port and to enable address decoding for the UTOPIA interface. The port address can be commonly used with both the transmit and receive UTOPIA interfaces.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PHYIDR	ENB	0	0	ID4	ID3	ID2	ID1	ID0	Port0:029H Port1:0A9H Port2:129H Port3:1A9H	01H	R/W

Field	Function	Default Value
D7: ENB	Address decode enable bit. When this bit is set to 1, the port starts verifying the signals on TADD and RADD, and ID4 to ID0.	0
★ D6, D5	Always keep these bit areas cleared to 0.	All 0
D4-D0: ID4-ID0	These bits set the 5-bit address used for the transmit/receive UTOPIA interface of the port. However, the address value cannot be set to "1FH".	00001

(42) Receive J0 drop register (J0R)

This register stores the J0 byte of the reception side SOH (Section Overhead).

The J0 byte is updated each time a frame is received, but is not updated in the OOF status.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
J0R									Port0:02AH Port1:0AAH Port2:12AH Port3:1AAH	00H	R

(43) Receive Z0 drop register (Z0#1R)

This register stores the 1st Z0 byte of the reception side SOH.

The 1st Z0 byte is updated each time a frame is received, but is not updated in the OOF status.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
Z0#1R									Port0:02BH Port1:0ABH Port2:12BH Port3:1ABH	00H	R

(44) Receive 2nd Z0 drop register (Z0#2R)

This register stores the 2nd Z0 byte of the reception side SOH.

The 2nd Z0 byte is updated each time a frame is received, but is not updated in the OOF status.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
Z0#2R									Port0:02CH Port1:0ACH Port2:12CH Port3:1ACH	00H	R

(45) Receive F1 drop register (F1R)

This register stores the F1 byte data of the reception side SOH.

The F1 byte is updated each time a frame is received, but is not updated in the OOF status.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
F1R									Port0:02DH Port1:0ADH Port2:12DH Port3:1ADH	00H	R

(46) Receive K1 drop register (K1R)

This register stores the K1 byte data of the reception side LOH (Line Overhead).

The K1 byte is updated each time a frame is received, but is not updated in the OOF status.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
K1R									Port0:02EH Port1:0AEH Port2:12EH Port3:1AEH	00H	R

(47) Receive K2 drop register (K2R)

This register stores the K2 byte data of the reception side LOH.

The K2 byte is updated each time a frame is received, but is not updated in the OOF status.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
K2R									Port0:02FH Port1:0AFH Port2:12FH Port3:1AFH	00H	R

(48) Receive C2 drop register (C2R)

This register stores the C2 byte data of the reception side POH (Path Overhead).

The C2 byte is updated each time a frame is received, but is not updated in the OOF, LOP, or Path AIS status.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
C2R									Port0:030H Port1:0B0H Port2:130H Port3:1B0H	00H	R

(49) Receive F2 drop register (F2R)

This register stores the F2 byte data of the reception side POH (Path Overhead).

The F2 byte is updated each time a frame is received, but is not updated in the OOF, LOP, or Path AIS status.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
F2R									Port0:031H Port1:0B1H Port2:131H Port3:1B1H	00H	R

(50) Receive H4 drop register (H4R)

This register stores the H4 byte data of the reception side POH (Path Overhead).

The H4 byte is updated each time a frame is received, but is not updated in the OOF, LOP, or Path AIS status.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
H4R									Port0:032H Port1:0B2H Port2:132H Port3:1B2H	00H	R

(51) Transmit J0 insert register (J0T)

This register sets the J0 byte of the transmission side SOH (Section Overhead).

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
J0T									Port0:033H Port1:0B3H Port2:133H Port3:1B3H	01H	R/W

(52) Transmit 1st Z0 insert register (Z0#1T)

This register sets the 1st Z0 byte of the transmission side SOH (Section Overhead).

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
Z0#1T									Port0:034H Port1:0B4H Port2:134H Port3:1B4H	02H	R/W

(53) Transmit 2nd Z0 insert register (Z0#2T)

This register sets the 2nd Z0 byte of the transmission side SOH (Section Overhead).

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
Z0#2T									Port0:035H Port1:0B5H Port2:135H Port3:1B5H	03H	R/W

(54) Transmit F1 insert register (F1T)

This register sets the F1 data of the transmission side SOH (Section Overhead).

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
F1T									Port0:036H Port1:0B6H Port2:136H Port3:1B6H	00H	R/W

(55) Transmit K1 insert register (K1T)

This register sets the K1 data of the transmission side LOH (Line Overhead).

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
K1T									Port0:037H Port1:0B7H Port2:137H Port3:1B7H	00H	R/W

- The register value is inserted or updated into/at the K1 byte position of the transmit overhead by writing 1 into the TAPS bit of the CMR1 register after the K1T register has been set or changed.
- By writing 0 into TAPS, inserting the register value at the byte position of the transmit overhead is stopped.

(56) Transmit K2 insert register (K2T)

This register sets the K2 data of the transmission side LOH (Line Overhead).

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
K2T									Port0:038H Port1:0B8H Port2:138H Port3:1B8H	00H	R/W

- The register value is inserted or updated at the K2 byte position of the transmit overhead by writing 1 into the TAPS bit of the CMR1 register after the K2T register has been set or changed.
- By writing 0 into TAPS, inserting the register value at the byte position of the transmit overhead is stopped.
- If the transmit command of the Line AIS and Line RDI frame and the TAPS bit are set in the CMR1 register at the same time, TAPS takes precedence and the setting of the K2T register is transmitted to the K2 byte of the transmit overhead.

(57) Transmit C2 insert register (C2T)

This register sets the C2 byte of the transmission side POH (Path Overhead).

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
C2T									Port0:039H Port1:0B9H Port2:139H Port3:1B9H	13H	R/W

(58) Transmit F2 insert register (F2T)

This register sets the F2 byte of the transmission side POH (Path Overhead).

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
F2T									Port0:03AH Port1:0BAH Port2:13AH Port3:1BAH	00H	R/W

(59) Transmit H4 insert register (H4T)

This register sets the H4 byte of the transmission side POH (Path Overhead).

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
H4T									Port0:03BH Port1:0BBH Port2:13BH Port3:1BBH	00H	R/W

(60) Reserved area

- Address: 03CH to 03EH, 0BCH to 0BEH, 13CH to 13EH, 1BCH to 1BEH
- Do not read from or write to this area.

(61) Version register (VERR)

This register stores the version name of this LSI.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
VERR	0	0	0	0	0	VER2	VER1	VER0	Port0:03FH Port1:0BFH Port2:13FH Port3:1BFH	XXH	R

Field	Function	Default Value
D2-D0: VER2-VER0	Indicates the version of this LSI.	X

★ (62) Receive 1st Z2 drop register (Z2#1R, Z2_6R)

This register stores the 1st Z2 byte of the reception side SOH (Section Overhead).

This register functions as the Z2#1R register when the D7:MGM bit of the MDR2 register is 0. It is updated to hold the newly received Z2#1 byte each time a frame is received. It is not updated when the μPD98411 is in the OOF status.

The receive 1st Z2 drop register functions as the Z2_6R register when MGM = 1. The μPD98411 monitors two bits (bits 6 and 7) of the receive 1st Z2 byte. When it receives the same receive 1st Z2 byte value six times consecutively after these bits have changed, it updates the register to hold the value.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
Z2#1R ***(Z2_6R)***									Port0:040H Port1:0C0H Port2:140H Port3:1C0H	00H	R

(63) Receive E1 drop register (E1R)

This register stores the E1 byte of the reception side SOH (Section Overhead).

The E1 byte is updated each time a frame is received, but is not updated in the OOF status.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
E1R									Port0:041H Port1:0C1H Port2:141H Port3:1C1H	00H	R

(64) Receive 1st to 3rd H1 drop register (H1R)

This is a register that stores the 1st to 3rd H1 byte of the reception side overhead.

The value of this register is updated each time a frame is received, but is not updated in the OOF status.

By repeatedly reading this register three times, the values can be obtained in the order of the 1st H1, 2nd H1, and 3rd H1. The byte to be read when this register is next read is indicated by the H1r1 and H1r0 bits of the ROHPR1 register. When the H1L bit of the ROHPL register is set to 1, the byte position to be read can be fixed.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
H1R									Port0:042H Port1:0C2H Port2:142H Port3:1C2H	00H	R

(65) Receive 1st to 3rd H2 drop register (H2R)

This is a register that stores the 1st to 3rd H2 bytes of the reception side overhead.

The value of this register is updated each time a frame is received, but is not updated in the OOF status.

By repeatedly reading this register three times, the values can be obtained in the order of the 1st H2, 2nd H2, and 3rd H2. The byte to be read when this register is next read is indicated by the H2r1 and H2r0 bits of the ROHPR1 register. When the H2L bit of the ROHPL register is set to 1, the byte position to be read can be fixed.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
H2R									Port0:043H Port1:0C3H Port2:143H Port3:1C3H	00H	R

(66) Receive 1st to 3rd H3 drop register (H3R)

This is a register that stores the 1st to 3rd H3 bytes of the reception side overhead.

The value of this register is updated each time a frame is received, but is not updated in the OOF status.

By repeatedly reading this register three times, the values can be obtained in the order of the 1st H3, 2nd H3, and 3rd H3. The byte to be read when this register is next read is indicated by the H3r1 and H3r0 bits of the ROHPR1 register. When the H3L bit of the ROHPL register is set to 1, the byte position to be read can be fixed.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
H3R									Port0:044H Port1:0C4H Port2:144H Port3:1C4H	00H	R

(67) Receive 1st to 3rd B2 drop register (B2R)

This is a register that stores the 1st to 3rd B2 bytes of the reception side LOH (Line Overhead).

The value of this register is updated each time a frame is received, but is not updated in the OOF status.

By repeatedly reading this register three times, the values can be obtained in the order of the 1st B2, 2nd B2, and 3rd B2. The byte to be read when this register is next read is indicated by the B2r1 and B2r0 bits of the ROHPR1 register.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
B2R									Port0:045H Port1:0C5H Port2:145H Port3:1C5H	00H	R

(68) Receive S1 drop register (S1R)

This register stores the S1 byte of the reception side LOH (Line Overhead).

The S1 byte is updated each time a frame is received, but is not updated in the OOF status.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
S1R									Port0:046H Port1:0C6H Port2:146H Port3:1C6H	00H	R

(69) Receive M1 drop register (M1R)

This register stores the M1 byte of the reception side LOH (Line Overhead).

The M1 byte is updated each time a frame is received, but is not updated in the OOF status.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
M1R									Port0:047H Port1:0C7H Port2:147H Port3:1C7H	00H	R

(70) Receive E2 drop register (E2R)

This is a register that stores the E2 byte of the reception side LOH (Line Overhead).

The E2 byte is updated each time a frame is received, but is not updated in the OOF status.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
E2R									Port0:048H Port1:0C8H Port2:148H Port3:1C8H	00H	R

(71) Receive J1 drop register (J1R)

This is a register that stores the J1 byte of the reception side POH (Path Overhead).

The J1 byte is updated each time a frame is received, but is not updated in the OOF, LOP, or Path AIS status.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
J1R									Port0:049H Port1:0C9H Port2:149H Port3:1C9H	00H	R

★ **(72) Receive B3 drop register (B3R, Z2#_12R)**

This register is used to hold the B3 byte of the reception side POH (Path Overhead) or the 1st Z2 byte.

It functions as the B3 register when the D7:MGM of the MDR2 register is 0. It is updated to hold the newly received B3 byte each time a frame is received. It is not updated in the OOF, LOP, or Path AIS status.

The receive B3 drop register functions as the Z2#_12R register when MGM = 1. The μPD98411 monitors two bits (bits 7 and 8) of the receive 1st Z2 byte. When it receives the same receive 1st Z2 byte value twelve times consecutively after these bits have changed, it updates the register to hold the value.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
B3R (Z2#_12R)									Port0:04AH Port1:0CAH Port2:14AH Port3:1CAH	00H	R

(73) Receive G1 drop register (G1R)

This is an eight-bit register that stores the G1 byte of the reception side POH (Path Overhead).

The data is updated each time a frame is received, but is not updated in the OOF, LOP, or Path AIS status.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
G1R									Port0:04BH Port1:0CBH Port2:14BH Port3:1CBH	00H	R

(74) Receive D1 to D3 drop register (DsecR)

This is a register that stores the D1, D2, and D3 bytes of the reception side SOH (Section Overhead).

The value of this register is updated each time a frame is received, but is not updated in the OOF status.

By repeatedly reading this register, the values can be obtained in the order of D1, D2, and D3. The byte to be read when this register is next read is indicated by the Dsr1 and Dsr0 bits of the ROHPR2 register.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
DsecR									Port0:04CH Port1:0CCH Port2:14CH Port3:1CCH	00H	R

(75) Receive D4 to D12 drop register (DlineR)

This is a register that stores the D4 through D12 bytes of the reception side LOH (Line Overhead).

The value of this register is updated each time a frame is received, but is not updated in the OOF status.

By repeatedly reading this register, the values can be obtained in the order of D4, D5, and so on, up to D11 and D12. The byte to be read when this register is next read is indicated by the DLr3 through DLr0 bits of the ROHPR2 register.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
DlineR									Port0:04DH Port1:0CDH Port2:14DH Port3:1CDH	00H	R

(76) Receive Z3, Z4, and Z5 drop register (Z345R)

This is a register that stores the Z3, Z4, and Z5 bytes of the reception side POH (Path Overhead).

By repeatedly reading this register, the values can be obtained in the order of Z3, Z4, and Z5.

The byte to be read when this register is next read is indicated by the Zr1 and Zr0 bits of the ROHPR2 register.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
Z345R									Port0:04EH Port1:0CEH Port2:14EH Port3:1CEH	00H	R

(77) Reserved area

- Address: 04FH, 0CFH, 14FH, 1CFH
- Do not read from or write to this area.

(78) Transmit 1st Z2 insert register (Z2#1T)

This is a register that sets the 1st Z2 byte of the transmission side SOH (Section Overhead).

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
Z2#1T									Port0:050H Port1:0D0H Port2:150H Port3:1D0H	00H	R/W

(79) Transmit E1 insert register (E1T)

This is an eight-bit register that sets the E1 byte of the transmission side SOH (Section Overhead).

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
E1T									Port0:051H Port1:0D1H Port2:151H Port3:1D1H	00H	R/W

(80) Transmit 1st to 3rd H1 insert register (H1T)

This is a register that sets the 1st to 3rd H1 bytes of the transmission side overhead.

This register is valid only when pseudo frame PLOP II is transmitted (CMR3 register = 10010B).

The 1st H1, 2nd H1, and 3rd H1 are written to this register in that order; therefore, this register is written three times. The byte to be set when this register is next written is indicated by the H1w1 and H1w0 bits of the TOHPR1 register. When the H1L bit of the TOHPL register is set to 1, the byte position to be set can be fixed.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
H1T									Port0:052H Port1:0D2H Port2:152H Port3:1D2H	00H	R/W

(81) Transmit 1st to 3rd H2 insert register (H2T)

This is a register that sets the 1st to 3rd H2 bytes of the transmission side overhead.

This register is valid only when pseudo frame PLOP II is transmitted (CMR3 register = 10010B).

The 1st H2, 2nd H2, and 3rd H2 are written to this register in that order; therefore, this register is written three times. The byte to be set when this register is next written is indicated by the H2w1 and H2w0 bits of the TOHPR1 register. When the H2L bit of the TOHPL register is set to 1, the byte position to be set can be fixed.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
H2T									Port0:053H Port1:0D3H Port2:153H Port3:1D3H	00H	R/W

(82) Transmit 1st to 3rd H3 insert register (H3T)

This is a register that sets the 1st to 3rd H3 bytes of the transmission side overhead.

This register is valid only when pseudo frame PLOP II is transmitted (CMR3 register = 10010B).

The 1st H3, 2nd H3, and 3rd H3 are written to this register in that order; therefore, this register is written three times. The byte to be set when this register is next written is indicated by the H3w1 and H3w0 bits of the TOHPR1 register. When the H3L bit of the TOHPL register is set to 1, the byte position to be set can be fixed.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
H3T									Port0:054H Port1:0D4H Port2:154H Port3:1D4H	00H	R/W

(83) Transmit 1st to 3rd B2 insert register (B2T)

This is a register that sets the 1st to 3rd B2 bytes of the transmission side LOH (Line Overhead).

This register is valid only when pseudo frame PB2 II is transmitted (CMR3 register = 10100B).

The 1st B2, 2nd B2, and 3rd B2 are written to this register in that order; therefore, this register is written three times. The byte to be set when this register is next written is indicated by the B2w1 and B2w0 bits of the TOHPR1 register.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
B2T									Port0:055H Port1:0D5H Port2:155H Port3:1D5H	00H	R/W

(84) Transmit S1 insert register (S1T)

This is a register that sets the S1 byte of the transmission side LOH (Line Overhead).

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
S1T									Port0:056H Port1:0D6H Port2:156H Port3:1D6H	00H	R/W

(85) Reserved area

- Address: 057, 0D7, 157, 1D7H
- Do not read from or write to this area.

(86) Transmit E2 insert register (E2T)

This is a register that sets the E2 byte of the transmission side LOH (Line Overhead).

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
E2T									Port0:058H Port1:0D8H Port2:158H Port3:1D8H	00H	R/W

(87) Transmit J1 insert register (J1T)

This is an eight-bit register that sets the J1 byte of the transmission side POH (Path Overhead).

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
J1T									Port0:059H Port1:0D9H Port2:159H Port3:1D9H	00H	R/W

(88) Transmit B3 insert register (B3T)

This is a register that sets the B3 byte of the transmission side POH (Path Overhead).

This register is valid only when pseudo frame PB3 II is transmitted (CMR3 register = 10101B).

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
B3T									Port0:05AH Port1:0DAH Port2:15AH Port3:1DAH	00H	R/W

(89) Reserved area

- Address: 05B, 0DB, 15B, 1DBH
- Do not read from or write to this area.

(90) Transmit D1 to D3 insert register (DsecT)

This is a register that sets the D1, D2, and D3 bytes of the transmission side SOH (Section Overhead).

D1, D2, and D3 are written to this register in that order; therefore, this register is written three times. The byte to be set when this register is next written is indicated by the DSw1 and DSw0 bits of the TOHPR2 register.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
DsecT									Port0:05CH Port1:0DCH Port2:15CH Port3:1DCH	00H	R/W

(91) Transmit D4 to D12 insert register (DlineT)

This is a 64-bit register that sets the D4, D5, D6, D7, D8, D9, D11, and D12 bytes of the transmission side LOH (Line Overhead).

This register is written repeatedly, in the order of the eight bits of the D4, D5, ..., D11, then D12 data. The byte to be set when this register is next written is indicated by the DLw3 through DLw0 bits of the TOHPR2 register.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
DlineT									Port0:05DH Port1:0DDH Port2:15DH Port3:1DDH	00H	R/W

(92) Transmit Z3, Z4, and Z5 insert register (Z345T)

This is a register that sets the Z3, Z4, and Z5 bytes of the transmission side POH (Path Overhead).

Z3, Z4, and Z5 are written to this register in that order; therefore, this register is repeatedly written. The byte to be set when this register is next written is indicated by the Zw1 and Zw0 bits of the TOHPR2 register.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
Z345T									Port0:05EH Port1:0DEH Port2:15EH Port3:1DEH	00H	R/W

(93) Reserved area

- Address: 05FH, 0DFH, 15FH, 1DFH
- Do not read from or write to this area.

(94) Receive overhead pointer lock register (ROHPL)

When the H1R, H2R, or H3R register is read repeatedly, the pointer to the internal register changes, and the data to be read also changes in the order of the 1st, 2nd, then 3rd byte. When a bit of this register is set to 1, the pointer of the ROHPR1 register is locked, and the byte to be read next can be fixed to any of the 1st, 2nd, and 3rd bytes.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
ROHPL	0	0	0	0	0	H3L	H2L	H1L	Port0:060H Port1:0E0H Port2:160H Port3:1E0H	00H	R/W

Field	Function	Default Value
★ D7-D3	Always keep these bit areas cleared to 0.	All 0
D2: H3L D1: H2L D0: H1L	When any of these bits is set to 1, the pointer of the ROHPR1 register is locked, and the byte to be read next can be fixed to the byte pointed to by the pointer.	All 0

(95) Receive overhead pointer register 1 (ROHPR1)

When the H1R, H2R, and H3R registers and B2 register are repeatedly read, the pointer pointing to an internal register changes, and the byte obtained is changed to 1st, 2nd, and 3rd bytes in that order. This register indicates the byte to be read when each register is next read.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
ROHPR1	H1r1	H1r0	H2r1	H2r0	H3r1	H3r0	B2r1	B2r0	Port0:061H Port1:0E1H Port2:161H Port3:1E1H	00H	R/W

Field	Function	Default Value
D7, D6: H1r1, H1r0	H1r[1:0]: Data to be read next 00: 1st H1 byte 01: 2nd H1 byte 10: 3rd H1 byte	00
D5, D4: H2r1, H2r0	H2r[1:0]: Data to be read next 00: 1st H2 byte 01: 2nd H2 byte 10: 3rd H2 byte	00
D3, D2: H3r1, H3r0	H3r[1:0]: Data to be read next 00: 1st H3 byte 01: 2nd H3 byte 10: 3rd H3 byte	00
D1, D0: B2r1, B2r0	B2r[1:0]: Data to be read next 00: 1st B2 byte 01: 2nd B2 byte 10: 3rd B2 byte	00

(96) Receive overhead pointer register 2 (ROHPR2)

When the Z345R, DsecR, and DlineR registers are repeatedly read, the pointer pointing to an internal register changes, and the byte obtained is changed. This register indicates the byte to be read when each register is next read.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
ROHPR2	Zr1	Zr0	DSr1	DSr0	DLr3	DLr2	DLr1	DLr0	Port0:062H Port1:0E2H Port2:162H Port3:1E2H	00H	R/W

Field	Function	Default Value
D7, D6: Zr1, Zr0	Zr[1:0]: Data to be read next 00: Z3 byte 01: Z4 byte 10: Z5 byte	00
D5, D4: DSr1, DSr0	DSr[1:0]: Data to be read next 00: D1 byte 01: D2 byte 10: D3 byte	00
D3-D0: DLr3-DLr0	DLr[3:0]: Next data 0000: D4 byte 0001: D5 byte 0010: D6 byte 0011: D7 byte 0100: D8 byte DLr[3:0]: Next data 0101: D9 byte 0110: D10 byte 0111: D11 byte 1000: D12 byte	0000

(97) Transmit overhead pointer lock register (TOHPL)

When the H1T, H2T, or H3T register is written repeatedly, the pointer to the internal register changes, and the data to be set also changes in the order of the 1st, 2nd, then 3rd byte. When a bit of this register is set to 1, the pointer of the TOHPR1 register is locked, and the byte to be written next can be fixed to any of the 1st, 2nd, and 3rd bytes.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
TOHPL	0	0	0	0	0	H3L	H2L	H1L	Port0:063H Port1:0E3H Port2:163H Port3:1E3H	00H	R/W

Field	Function	Default Value
★ D7-D3	Always keep these bit areas cleared to 0.	All 0
D2: H3L D1: H2L D0: H1L	When any of these bits is set to 1, the pointer of the TOHPR1 register is locked, and the byte to be written next can be fixed.	All 0

(98) Transmit overhead pointer register 1 (TOHPR1)

When the H1T, H2T, H3T, or B2T register is written repeatedly, the pointer to the internal register changes, and the data to be set also changes. This register indicates the byte to be set when each register is next written.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
TOHPR1	H1w1	H1w0	H2w1	H2w0	H3w1	H3w0	B2w1	B2w0	Port0:064H Port1:0E4H Port2:164H Port3:1E4H	00H	R/W

Field	Function	Default Value
D7, D6: H1w1, H1w0	H1w[1:0]: Data to be set next 00: 1st H1 byte 01: 2nd H1 byte 10: 3rd H1 byte	00
D5, D4: H2w1, H2w0	H2w[1:0]: Data to be set next 00: 1st H2 byte 01: 2nd H2 byte 10: 3rd H2 byte	00
D3, D2: H3w1, H3w0	H3w[1:0]: Data to be set next 00: 1st H3 byte 01: 2nd H3 byte 10: 3rd H3 byte	00
D1, D0: B2w1, B2w0	B2w[1:0]: Data to be set next 00: 1st B2 byte 01: 2nd B2 byte 10: 3rd B2 byte	00

(99) Transmit overhead pointer register 2 (TOHPR2)

When the Z345T, DsecT, or DlineT register is written repeatedly, the pointer to the internal register changes, and the data to be set also changes. This register indicates the byte to be set when each register is next written.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
TOHPR2	Zw1	Zw0	DSw1	DSw0	DLw3	DLw2	DLw1	DLw0	Port0:065H Port1:0E5H Port2:165H Port3:1E5H	00H	R/W

Field	Function	Default Value
D7, D6: Zw1, Zw0	Zw[1:0]: Data to be set next 00: Z3 byte 01: Z4 byte 10: Z5 byte	00
D5, D4: DSw1, DSw0	DSw[1:0]: Data to be set next 00: D1 byte 01: D2 byte 10: D3 byte	00
D3-D0: DLw3-DLw0	DLw[3:0]: Next data 0000: D4 byte 0001: D5 byte 0010: D6 byte 0011: D7 byte 0100: D8 byte DLw[3:0]: Next data 0101: D9 byte 0110: D10 byte 0111: D11 byte 1000: D12 byte	0000

(100) Reserved area

- Addresses: 066H to 06BH, 0E6H to 0EFH, 166H to 16FH, 1E6H to 1EFH
- Do not read from or write to this area.

5.2.2 Common Register

The common registers perform setting related to all four ports of the μPD98411.

(101) Threshold register write pointer register (SYSPR)

This register indicates a pointer that points to the high-order or low-order bytes of the threshold register (address: 06EH to 073H) to be written next. This register sets the threshold value of each counter when the error rate monitor function is used.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
★ ***SYSPR***	FJtw	PREtw	LREtw1	LREtw0	B3tw	B2tw1	B2tw0	B1tw	06CH	00H	R/W

Field	Function	Default Value
D7: FJtw D6: PREtw D5: LREtw1 D4: LREtw0 D3: B3tw D2: B2tw1 D1: B2tw0 D0: B1tw	A pointer indicated by one bit is a pointer for the threshold register of the 16-bit counter and indicates whether the high-order or low-order byte of the 16 bits is to be written next. 0: Low-order eight bits 1: High-order eight bits Two-bit pointer which indicates whether the high-order, middle-order, or low-order eight bits of the 24 bits are to be written next. 00: Low-order eight bits 01: Middle-order eight bits 10: High-order eight bits	All 0

(102) Alarm detection condition change register (ITUR)

This register detects alarms and changes the clear conditions of the alarms.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
ITUR	0	0	0	0	0	0	0	ITU	06DH	00H	R/W

Field	Function	Default Value
★ D7-D1	Always keep these bit areas cleared to 0.	All 0
D0: ITU	When the setting of this bit is changed, the alarm detection and release conditions are also changed.	0

Alarm	ITU Bit = 0	ITU Bit = 1
Line RDI	Detected when **five** contiguous frames in which the K2 byte (bits 6 through 8) is set to 110 have been received. Released when five contiguous frames containing other than 110 have been received.	Detected when **three** contiguous frames in which the K2 byte (bits 6 through 8) is set to 110 have been received. Released when three contiguous frames containing other than 110 have been received.
Path RDI	Detected when **five** contiguous frames in which the G1 byte (bit 5) is set to 1 have been received. Released when five contiguous frames containing other than 1 have been received.	Detected when **three** contiguous frames in which the G1 byte (bit 5) is set to 1 have been received. Released when three contiguous frames containing other than 1 have been received.
Line AIS	Detected when **five** contiguous frames in which the K2 byte (bits 6 through 8) is set to 111 have been received. Released when five contiguous frames containing other than the above have been received.	Detected when **three** contiguous frames in which the K2 byte (bits 6 through 8) is set to 111 have been received. Released when five contiguous frames containing other than the above have been received.

(103) B1 error threshold register (B1THR)

This register sets the threshold value for the number of times the B1 error is to be detected when the error rate monitor function is used. The 16 bits of this register are set by writing the register twice, in the order of the low-order eight bits then the high-order eight bits. When the register is next written, whether the high-order or low-order eight bits are to be written is indicated by the SYSPR register. The threshold set with this register is compared with the value of the B1 error counter for each port. When the value of the counter for a port reaches the threshold, the B1o bit of the PCOCR1 register is set to 1.

★ A threshold value set in this register becomes valid only after the FRMN register is write-accessed. Be sure to set a threshold value in the register before the FRMN register is write-accessed.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
B1THR									06EH	FFH	R/W

(104) B2 error threshold register (B2THR)

This register sets the threshold value for the number of times the B2 error is to be detected when the error rate monitor function is used. The 24 bits of this register are set in the order of the low-order eight bits, middle-order eight bits, then the high-order eight bits. When the register is next written, whether the high-order, middle-order, or low-order eight bits are to be written is indicated by the SYSPR register. When the value of the counter for a port reaches the threshold, the B2o bit of the PCOCR1 register is set to 1.

★ A threshold value set in this register becomes valid only after the FRMN register is write-accessed. Be sure to set a threshold value in the register before the FRMN register is write-accessed.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
B2THR									06FH	FFH	R/W

(105) B3 error threshold register (B3THR)

This register sets the threshold value for the number of times the B3 error is to be detected when the bit error rate monitor function is used. The 16 bits of this register are set in the order of the low-order eight bits then the high-order eight bits. When the register is next written, whether the high-order or low-order eight bits are to be written is indicated by the SYSPR register. When the value of the counter for a port reaches the threshold, the B3o bit of the PCOCR1 register is set to 1.

★ A threshold value set in this register becomes valid only after the FRMN register is write-accessed. Be sure to set a threshold value in the register before the FRMN register is write-accessed.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
B32THR									070H	FFH	R/W

(106) Line REI threshold register (LRETHR)

This is a register that sets the threshold of the Line REI detection count for the bit error rate monitoring function. The 24 bits of this register are set in the order of the low-order eight bits, middle-order eight bits, and the high-order eight bits. When the register is next written, whether the high-order, middle-order, or low-order eight bits are to be written is indicated by the SYSPR register. When the value of the counter for a port reaches the threshold, the LREo bit of the PCOCR1 register is set to 1.

★ A threshold value set in this register becomes valid only after the FRMN register is write-accessed. Be sure to set a threshold value in the register before the FRMN register is write-accessed.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
LRETHR									071H	FFH	R/W

(107) Path REI threshold register (PRETHR)

This is a register that sets the threshold of the Path REI detection count when the error rate monitoring function is used. The 16 bits of this register are set in the order of the low-order eight bits then the high-order eight bits. When the register is next written, whether the high-order or low-order eight bits are to be written is indicated by the SYSPR register. When the value of the counter for a port reaches the threshold, the PREo bit of the PCOCR1 register is set to 1.

★ A threshold value set in this register becomes valid only after the FRMN register is write-accessed. Be sure to set a threshold value in the register before the FRMN register is write-accessed.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
PRETHR									072H	FFH	R/W

(108) FJ threshold register (FJTHR)

This is a 16-bit register that sets the threshold of the Frequency Justification detection count when the error rate monitoring function is used. The 16 bits of this register are set in the order of the low-order eight bits then the high-order eight bits. When the register is next written, whether the high-order or low-order eight bits are to be written is indicated by the SYSPR register. When the value of the counter for a port reaches the threshold, the FJo bit of the PCOCR1 register is set to 1.

★ A threshold value set in this register becomes valid only after the FRMN register is write-accessed. Be sure to set a threshold value in the register before the FRMN register is write-accessed.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
FJTHR									073H	FFH	R/W

(109) Threshold monitor frame number register (FRMN)

This register is used to set the period in which the error rate is monitored.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
FRMN	FRM7	FRM6	FRM5	FRM4	FRM3	FRM2	FRM1	FRM0	074H	00H	R/W

Field	Function	Default Value
D7-D0: FRM7-FRM0	★	All 0

FRM7-FRM0	Comparison Period
00000000	No restrictions
00000010	8 frames (1 ms)
00000100	80 frames (10 ms)
00001000	400 frames (50 ms)
00010000	1,000 frames (125 ms)
00100000	2,000 frames (250 ms)
01000000	4,000 frames (500 ms)
10000000	8,000 frames (1 s)
Others	Cannot be set.

★ **Caution When using the error rate monitor function, set this register after a threshold value is set in the threshold register.**

(110) Clock recovery control register (CRSC)

If a port enters the OOL or LOS status, being unable to extract the correct clock when the clock recovery PLL is used as the transmit clock of the port (set by the TXSC register), this register is used to automatically or forcibly switch the clock to prevent the transmit clock of the port from becoming unstable.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
CRSC	RAT0	RCL0	RAT1	RCL1	RAT2	RCL2	RAT3	RCL3	075H	00H	R/W

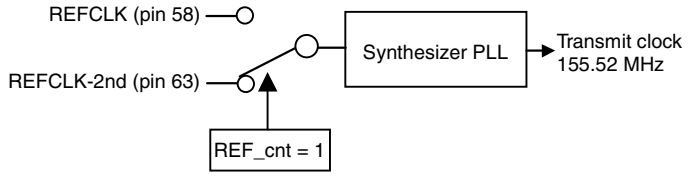
	Field	Function	Default Value
★	D7, D5, D3, D1: RAT0-RAT3	These bits are used to automatically switch the clock if the port enters the OOL or LOS status because it is unable to extract the correct clock. 1: When the port enters the OOL or LOS status, automatic clock switching occurs in such a way that the clock used as the transmit clock for the port will be used as the clock for the reception block. The clock used as the transmit clock for the port is determined according to the input to the CSSEL pin and the setting of the CSSC register. It is the clock generated by the synthesizer PLL, the TFKT/TFKC input clock, or the recovery clock for one of the ports. When the port exits the OOL or LOS status, the clock that was used before is used again. 0: Even when the port enters the OOL or LOS status, the recovery clock is kept used as the clock for the reception block.	All 0
★	D6, D4, D2, D0: RCL0-RCL3	Setting any of these bits to 1 forces clock switching in such a way that the port will use the transmit clock as a clock for the reception block. In addition, the clock recovery PLL for the port is reset, and the OOL bit is set.	All 0

★ **Caution While the RCL0 to RCL3 bits are set, inputting normal data to the reception line cannot reset the OOL bit, because the clock recovery PLL for the port has been kept reset. Note that a change in the state of the OOL bit cannot be used as a condition for judging whether to set/reset the RCL0 to RCL3 bits.**

(111) Clock source control register (CSSC)

This register selects the receive clock extracted by the clock recovery PLL of selected port as the transmit clock for all the four ports.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
CSSC	0	0	0	REF_cnt	P0	P1	P2	P3	076H	00H	R/W

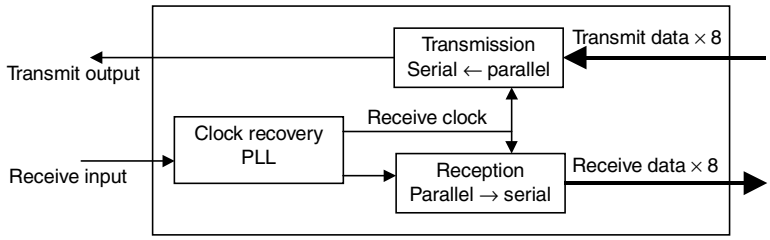
Field	Function	Default Value
★ D7-D5	Always keep these bit areas cleared to 0.	All 0
D4: REF_cnt	This bit changes the reference clock that is supplied to the synthesizer PLL that generates a transmit clock. 1: The synthesizer PLL uses the REFCLK-2nd input as the reference clock. 0: The synthesizer PLL uses the system clock input to REFCLK as the reference clock.  Even when the reference clock of the synthesizer PLL is changed to REFCLK-2nd by setting this bit, a 19.44-MHz system clock must be input to REFCLK.	0
D3-D0: P0-P3	When bit P'n' is set to 1, the recovery clock extracted by the clock recovery PLL of port 'n' is used as the transmit clock for all four ports. If two or more bits are set to 1, the clock extracted by the port with the lower 'n' takes precedence. In this case, if the port having the highest priority enters the OOL or LOS status, because it can not supply the correct clock, the recovery clock of the port having the second highest priority is selected automatically. The setting of this bit takes precedence over the setting of the external transmit clock by CSSEL pin input.	All 0

(112) Transmit clock source control register (TXSC)

This register specifies that the receive clock extracted by the clock recovery PLL of each port is to be used as the transmit clock of a port.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
TXSC	0	0	0	0	P0LP	P1LP	P2LP	P3LP	077H	00H	R/W

	Field	Function	Default Value
★	D7-D4	Always keep these bit areas cleared to 0.	All 0
	D3-D0: P0LP-P3LP	When bit P'n'LP is set to 1, port 'n' uses the clock extracted by the clock recovery PLL of that port as the transmit clock. This setting does not affect the transmit clock setting of the other ports. The setting of this register takes precedence over the setting of the CSSEL pin related to the transmit clock selection of a port and the setting of the CSSC register.	All 0



(113) UTOPIA interface relating register (AVLC)

This register sets the modes related to the UTOPIA interface.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
AVLC	UCS	RCAC	AVC2	AVC1	AVC0	UPR	UTC	TCAC	078H	00H	R/W

Field	Function	Default Value
D7: UCS	This bit changes the format of the invalid cell to be inserted into the transmit frame when the cell data in the transmit FIFO is not sufficient to constitute one cell. 1: Unassigned cell format 0: Idle cell format (default)	0
D6: RCAC	This bit changes the timing of the receive UTOPIA interface at which the port transferring a cell makes RCLAV valid. 1: RCLAV becomes valid seven clock cycles (RCLK) after cell transfer has been started when the receive FIFO is short of one cell because of the cell transfer. 0: RCLAV remains high up to the last byte (payload: 48th byte) of the cell being transferred even if the receive FIFO is short of one cell because of the cell transfer. It becomes valid after the last byte has been output (default).	0
D5-D3: AVC2-AVC0	These bits change the TCLAV signal transition conditions. They specify the number of cells in the vacant area of the transmit FIFO, at which transmit cell available signal, TCLAV, goes inactive. By default, 000 (one cell) is assumed. If the currently received cell causes the FIFO to be full, TCLAV goes low. When 011 (three cells) is specified, if the sixth cell in the FIFO is written to, TCLAV goes low because the FIFO does not have an enough vacancy of three cells. 000-001: 1 cell 010: 2 cells 011: 3 cells 101: 5 cells 100: 4 cells 110: 6 cells 111: 7 cells When cells are transferred once cell available signal, TCLAV, goes low, the μPD98411 receives these cells until the transmit FIFO becomes full. ★ Be sure to set or change this bit area before transmission cell data is input to the UTOPIA interface of the μPD98411.	000
D2: UPR	This bit disables parity output from RPR of the receive UTOPIA interface. 1: Disables 0: Enables	0
D1: UTC	This bit disables the parity check of TPR input of the transmit UTOPIA interface. At the same time, it clears the UT bit of the IMST register that reports the detection of a parity error. 1: Disables 0: Enables	0
D0: TCAC	This bit changes the timing at which the port receiving a cell makes TCLAV of the transmit UTOPIA interface valid. 1: The port transferring a cell makes TCLAV valid after the 20th byte of the cell currently being received has been output. 0: The port transferring a cell makes TCLAV valid four clocks before the last byte of the cell currently being received.	0

(114) Multi-PHY mode switch register (MltUT)

This register selects the modes related to the UTOPIA interface and, at the same time, enables the UTOPIA interface. For details, see **Section 4.1.2**.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
MltUT	0	0	0	0	MSL3	MSL2	MSL1	MSL0	079H	00H	R/W

Field	Function	Default Value
★ D7-D4	Always keep these bit areas cleared to 0.	All 0
D3: MSL3	This bit selects the bit of an address to be checked during polling to set Multi Status Polling. 1: Checks only the high-order three bits of the address during polling. The port whose high-order three bits on TADD and RADD coincide with ID4 to ID2 of the PHYIDR register drives TCLAV and RCLAV. 0: Checks all five address bits during polling. The port whose five bits on TADD and RADD coincide with ID4 to ID0 of the PHYIDR register drives TCLAV and RCLAV. When MSL2 = 1, TCLAV and RCLAV are always driven regardless of polling.	0
D2: MSL2	This bit selects the TCLAV and RCLAV signals to be allocated to a port to set Direct Status Indication. 1: Enables all the cell available signals TCLAV0 to TCLAV3 and RCLAV0 to RCLAV3, and allocates a pair of TCLAV0 and RCLAV0 to port 0, and a pair of TCLAV2 and RCLAV2 to port 2. If MSL3 = 0, each port functions as a two-state output port that drives TCLAV and RCLAV, regardless of polling. If MSL3 = 1, the port functions as a tristate output port and only the port whose address coincides during polling drives the cell available signals. 0: TCLAV and RCLAV are multiplexed and output as one signal. The port functions as a tristate output port.	0
D1, D0: MSL1, MSL0	Selects bus mode. 00: Disabled. 01: Dual eight-bit bus 10: Single eight-bit bus 11: Single 16-bit bus	00

★ **Caution Once transmission/reception cell data input/output has begun with the UTOPIA interface of the μPD98411, do not set/change the MltUT register. Be sure to set/change the register after the LSI chip is reset but before data transfer begins.**

Table 5-1. Setting of MSL Bit and UTOPIA Interface Modes

MSL[3:0]	Bus Mode	Mode to Obtain State	CLAV Signal Used	CLAV Output
0001	Dual eight-bit	2TCLAV/2RCLAV	2 × TCLAV/RCLAV	Tristate
0101		Direct Status Indication	4 × TCLAV/RCLAV	Two-state
1001		Multiplexed Status Polling	1 × TCLAV/RCLAV	Tristate
1101			4 × TCLAV/RCLAV	
0010	Singe eight-bit	1TCLAV/1RCLAV	1 × TCLAV/RCLAV	Tristate
0110		Direct Status Indication	4 × TCLAV/RCLAV	Two-state
1010		Multiplexed Status Polling	1 × TCLAV/RCLAV	Tristate
1110			4 × TCLAV/RCLAV	
0011	Single 16-bit	1TCLAV/1RCLAV	1 × TCLAV/RCLAV	Tristate
0111		Direct Status Indication	4 × TCLAV/RCLAV	Two-state
1011		Multiplexed Status Polling	1 × TCLAV/RCLAV	Tristate
1111			4 × TCLAV/RCLAV	

(115) TCL clock output enable register (TCMSK)

This register selects the clock to be output from the TCL pin.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
TCMSK	0	0	0	0	TC3o	TC2o	TC1o	TC0o	07AH	00H	R/W

Field	Function	Default Value
D7-D4	Always keep these bit areas cleared to 0.	All 0
D3-D0: TC3o-TC0o	When bit TC'n'o is set, the 155.52-MHz clock used by port 'n' for transmission is divided by eight and the resultant 19.44-MHz clock is output from the TCL pin. If two or more of these bits are set to 1, the clock of the port with the lower 'n' takes precedence. By default, the clock of none of the ports is selected and no clock is output from TCL.	All 0

(116) RCL clock output enable register (RCMSK)

This register enables the RCL pin output and selects the port for which the clock recovery is output.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
RCMSK	0	0	0	REFo	RC3o	RC2o	RC1o	RC0o	07BH	01H	R/W

	Field	Function	Default Value
★	D7-D5	Always keep these bit areas cleared to 0.	All 0
★	D4: REFo	This bit causes the reference clock of the synthesizer PLL to be output from the RCL pin. The setting of this bit takes precedence over the setting of RC3o to RC0o. 1: The reference clock of the synthesizer PLL selected by the REF_cnt bit of the CSSC register, REFCLK input, or REFCLK-2nd input is output from the RCL pin. 0: The clock generated by dividing the reception clock by eight according to the setting of RC3o to RC0o is output.	0
★	D3-D0: RC3o-RC0o	When bit RC'n'o is set, the clock used by port 'n' for reception is divided by eight is output from the RCL pin. If two or more of these bits are set to 1, the clock of the port with the lower 'n' takes precedence. By default, the clock of port 0 is selected.	0001

(117) Frame pulse output enable register (FPMSK)

This register sets the TXFP pin, from which the pulse signal synchronized with the transmit/receive frame is output, together with RXFP pin output.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
FPMSK	RFP3o	RFP2o	RFP1o	RFP0o	TFP3o	TFP2o	TFP1o	TFP0o	07CH	00H	R/W

Field	Function	Default Value
D7-D4: RFP3o-RFP0o	When the RFP'n'o bit is set to 1, a pulse (8 kHz) synchronized with the beginning of the frame received by port n is output from the RxFP pin. When two or more bits are set, that port with the lower 'n' takes precedence. By default, none of RFP3o to RFP0o is selected, and the RxFP pin output is disabled.	All 0
D3-D0: TFP3o-TFP0o	When bit TFP'n'o is set, the pulse (8 kHz) synchronized with the first byte of the frame transmitted by port 'n' is output from the TxFP pin. If two or more of these bits are set to 1, the port with the lower 'n' takes precedence. By default, none of TFP3o to TFP0o is set and the TxFP pin output is disabled.	All 0

(118) Reserved area

- Address: 07DH
- Do not read from or write to this area.

★ **(119) Software reset/interrupt control register (ICNT)**

This register is used for interrupt mode selection and an LSI reset command.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
ICNT	0	0	0	0	SYSR	0	RCM	P1A	07EH	00H	R/W

Field	Function	Default Value
★ D7-D4, D2	Always keep these bit areas cleared to 0.	All 0
★ D3: SYSR	This bit causes the entire LSI chip to be reset. Setting the bit to 1 initializes the entire LSI chip, similarly to a hardware reset. The bit automatically returns to 0 after a reset occurs.	0
D1: RCM	This bit selects a report mode by an interrupt signal when an interrupt cause event that reports a status is generated. 1: Interrupt PHINT_B signal goes low both when the cause is generated and when the cause is cleared. 0: Only when an interrupt cause occurs, the interrupt PHINT_B signal becomes active.	0
D0: P1A	This bit selects the number of interrupt signals to be used. 1: The interrupt signals of all the four ports are multiplexed and reported from PHINT0_B. When PHINT0_B goes low, the IMST register identifies the port of the interrupt cause. 0: Allocates one of PHINT0_B to PHINT3_B to each port.	0

★ **Remark** A reset command for an individual port is held in the CMR2 register.

(120) Interrupt port indication register (IMST)

This register checks the port whose PHINT_B is low when P1A of the ICNT register is 1.

Register name	D7	D6	D5	D4	D3	D2	D1	D0	Address	Default	R/W
IMST	0	0	0	UT	P3	P2	P1	P0	07FH	00H	R

Field	Function	Default Value
D4: UT	The setting of this bit indicates that a parity error has detected on the transmit UTOPIA interface. To clear this bit, set the UTC bit of the AVLC register to 1 to disable parity check. To check the parity again, clear UTC to 0.	0
D3-D0: P3-P0	This bit indicates the port for which a cause is generated if the interrupt signals of the four ports are multiplexed and output in the interrupt mode of P1A = 1 that is set by the P1A bit of the ICNT register. When bit P'n' is set, the interrupt signal is asserted active by the cause of port 'n'. These bits indicate the inverted level of PHINT_B of ports and are cleared to 0 when PHINT_B next goes high again. See **Section 4.4**.	0

CHAPTER 6 JTAG BOUNDARY SCAN

The μPD98411 has a JTAG boundary scan circuit.

★ **Cautions 1. Some pins do not support JTAG. The following table lists those pins that do not support JTAG.**

Category	Pin Name	Number of Pins
P-ECL level	RDIT3-RDIT0, RDIC3-RDIC0, TDOT3-TDOT0, TDOC3-TDOC0, TFKT, TFKC	18

★ **2. A pulse input to the RESET_B pin does not reset the JTAG logic section. After the power is switched on, besides a system reset based on RESET_B, use the method described in Section 2.2.5 to reset the JTAG logic section.**

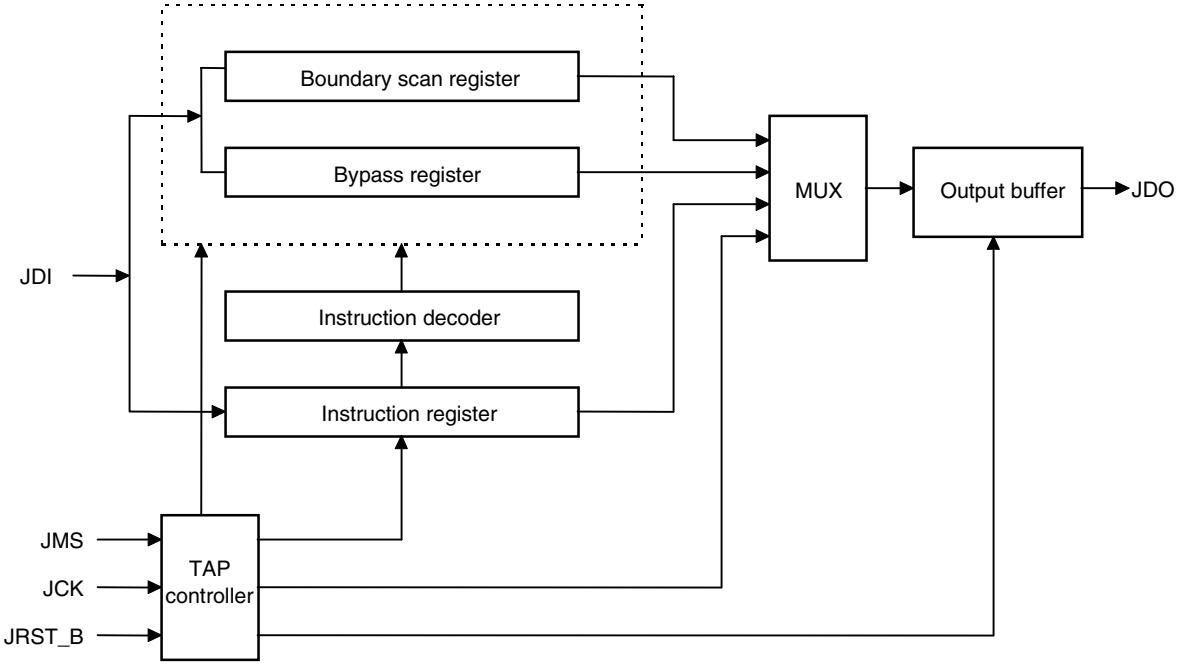
6.1 Features

- Conforms to IEEE1149.1 JTAG Boundary Scan Standard.
- Three registers dedicated to boundary scan
  - Instruction register
  - Bypass register
  - Boundary scan register
- Three instructions supported
  - BYPASS instruction
  - EXTEST instruction
  - SAMPLE/PRELOAD instruction
- Five pins dedicated to boundary scan
  - JCK (JTAG Clock)
  - JMS (JTAG Mode Select)
  - JDI (JTAG Data Input)
  - JDO (JTAG Data Output)
  - JRST_B (JTAG Reset)

6.2 Internal Configuration of Boundary Scan Circuit

Figure 6-1 shows the block diagram of the internal JTAG boundary scan circuit of the μPD98411.

Figure 6-1. Block Diagram of Boundary Scan Circuit



6.2.1 Instruction Register

The instruction register consists of a two-bit shift register and writes instruction data from the JDI pin. The register and instruction are selected by this instruction data.

6.2.2 TAP (Test Access Port) Controller

The TAP controller changes operating state by latching the signal of the JMS pin at the rising edge of the clock input to the JCK pin.

6.2.3 Bypass Register

The bypass register consists of a one-bit shift register connected between the JDI and JDO pins when the TAP controller is in Shift-DR state. If this register is selected while the TAP controller is in Shift-DR state, data is shifted to the JDO pin at the rising edge of the clock input to the JCK pin.

When this register is selected, the operation of the JTAG boundary circuit does not influence on the operation of the μPD98411.

6.2.4 Boundary Scan Register

The boundary scan register is located between an external pin of the μPD98411 and internal logic circuit. When this register is selected, data is latched or loaded by the instruction of the TAP controller.

If this register is selected while the TAP controller is in Shift-DR state, data is output to the JDO pin starting from the LSB at the falling edge of the clock input to the JCK pin.

6.3 Pin Function

6.3.1 JCK (JTAG Clock) Pin

The JCK pin is used to supply a clock signal to the JTAG boundary scan circuit (such as the bypass register, instruction register, and TAP controller. This clock signal is isolated so as not to be supplied to the other internal circuits of the μPD98411.

6.3.2 JMS (JTAG Mode Select) Pin

Input to the JMS pin is latched at the rising edge of the clock input to the JCK pin and defines the operation of the TAP controller.

6.3.3 JDI (JTAG Data Input) Pin

The JDI pin is an input pin that inputs data to the JTAG boundary scan circuit register.

6.3.4 JDO (JTAG Data Output) Pin

The JDO pin is an output pin that outputs data from the JTAG boundary scan circuit. This pin changes its output at the falling edge of the clock input to the JCK pin. This pin is a tristate output pin and is controlled by the TAP controller.

6.3.5 JRST_B (JTAG Reset) Pin

This pin asynchronously initializes the TAP controller. This reset signal sets the μPD98411 in the normal operation mode and the boundary register in non-operation state.

6.4 Operation Description

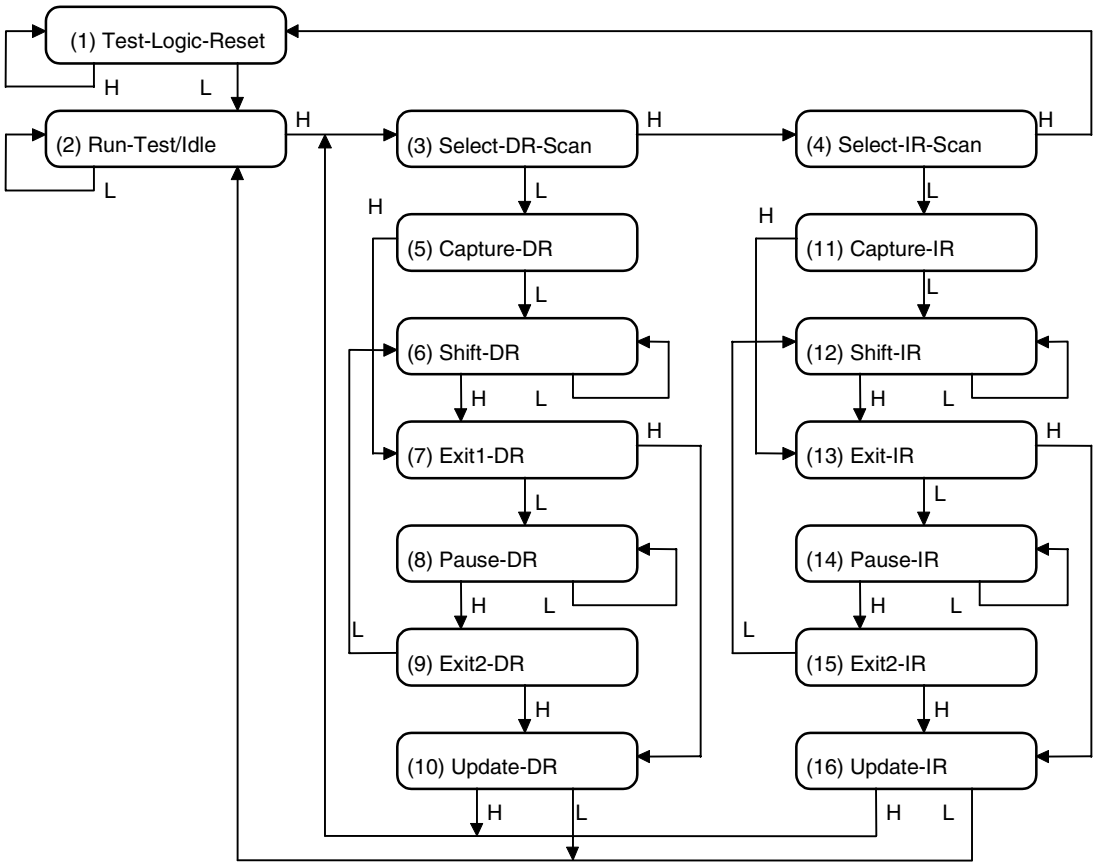
6.4.1 TAP Controller

The TAP controller is a circuit having 16 states synchronized with changes of the JMS and JCK pins. Its operation is specified by IEEE Standard 1149.1.

6.4.2 TAP Controller State

Figure 6-2 shows the state transition of the TAP controller. The state of the TAP controller is determined depending on the state of the JMS pin signal input at the rising edge of the clock input to the JCK pin. The operations of the instruction register, boundary scan register, and bypass register change at the rising or falling edge of the clock input to the JCK pin. (See **Figure 6-3**).

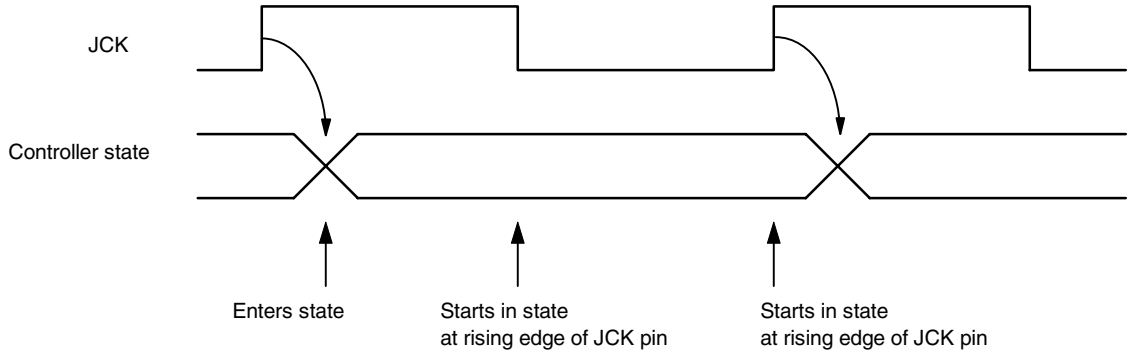
Figure 6-2. State Transition of TAP Controller



Remarks 1. "H" and "L" of the arrows indicating state transition in the above figure indicate the state of the JMS pin at the rising edge of the clock input to the JCK pin.

2. Numbers in ( ) in the above figure correspond to the explanation below.

Figure 6-3. Operation Timing in Controller State



(1) Test-Logic-Reset

The JTAG boundary scan circuit performs no operation on the μPD98411. Therefore, it does not affect the system logic of the μPD98411. This is because the bypass instruction is stored to the instruction register and executed on initialization. The TAP controller enters the Test-Logic-Reset state if the JMS pin signal holds the high level for the duration of at least five rising edges of the JCK pin signal, regardless of the current state of the controller. The TAP controller holds this state for the duration in which the JMS pin signal high.

If the TAP controller must be in the Test-Logic-Reset state, the controller returns to the original Test-Logic-Reset state even if a low-level signal is input once to the JMS pin by mistake (due to, for example, the influence of the external interface), if the JMS pin signal holds its high level status for the duration of three rising edges of the JCK pin signal.

The operation of the test logic does not hinder the logic operation of the μPD98411 due to the above error.

When the TAP controller exits from the Test-Logic-Reset state, the controller enters the Run-Test/Idle state. In this state, no operation is performed because the current instruction is set by the operation of the bypass register. The logic operation of the JTAG boundary scan circuit is inactive even in the Select-DR-Scan and Select-IR-Scan states.

(2) Run-Test/Idle

The TAP controller is in this state during scan operation (in Select-DR-Scan or Select-IR-Scan state). Once the controller has entered this state and if the JMS pin signal holds the low level, the controller remains in this state. The controller enters the Select-DR-Scan state if the JMS pin signal holds high level at one rising edge of the JCK pin signal.

All the test data registers (boundary register and bypass register) selected by the current instruction hold the previous status (Idle). While the TAP controller is in this state, the instruction does not change.

(3) Select-DR-Scan

This is a temporary boundary scan state. The boundary scan register and bypass register selected by the current instruction hold the previous state.

If the JMS signal is held low at the rising edge of the JCK pin signal while the TAP controller is in this state, the controller enters the Capture-DR state, and scan sequence to the selected registers is started.

If the JMS signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Select-IR-Scan state. While the controller is in this state, the instruction does not change.

(4) Select-IR-Scan

This is a temporary boundary scan state. The boundary scan register and bypass register selected by the current instruction hold the previous state.

If the JMS signal is held low at the rising edge of the JCK pin signal while the TAP controller is in this state, the controller enters the Capture-IR state, and scan sequence to the selected registers is started.

If the JMS signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Test-Logic-Reset state. While the controller is in this state, the instruction does not change.

(5) Capture-DR

In this controller state, data is loaded to the boundary scan register selected by the current instruction in parallel at the rising edge of the JCK pin signal (in this case, data is input from the input pin of each device to the corresponding boundary scan register). While the TAP controller is in this state, the instruction does not change.

If the TAP controller is in this state at the rising edge of the JCK pin signal, the controller enters the following state:

- If the JMS pin signal is held high: Exit1-DR state
- If the JMS pin signal is held low: Shift-DR state

(6) Shift-DR

In this controller state, JDI and JDO are connected (at either of the boundary scan register of bypass register) by the current instruction. The shift data is shifted one state at a time toward the serial output direction at each rising edge of the JCK pin signal.

The boundary scan register or bypass register selected by the current instruction holds the previous status without change if the controller is not on the serial bus (not in the Shift-DR state). While the TAP controller is in this state, the instruction does not change.

If the TAP controller is in this state at the rising edge of the JCK pin signal, the controller enters the following state:

- If the JMS pin signal is held high: Exit1-DR state
- If the JMS pin signal is held low: Shift-DR state

(7) Exit1-DR

This is a temporary controller state. If the JMS pin signal is held high at the rising edge of the JCK pin signal with the TAP controller in this state, the controller enters the Update-DR state. This ends the scan process.

If the JMS pin signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Pause-DR state.

Both the bypass register and boundary scan register selected by the current instruction hold the previous status without change. While the TAP controller is in this state, the instruction does not change.

(8) Pause-DR

In this controller state, shifting between JDI and JDO connected by either the bypass register or boundary scan register is temporarily stopped. These registers selected by the current instruction hold the previous state without change.

The TAP controller remains in this state while the JMS pin signal is low. If the JMS pin signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Exit2-DR state. While the TAP controller is in this state, the instruction does not change.

(9) Exit2-DR

This is a temporary controller state. If the JMS pin signal is held high at the rising edge of the JCK pin signal with the TAP controller in this state, the controller enters the Update-DR state. This ends the scan process.

If the JMS pin signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Shift-DR state.

Both the bypass register and boundary scan register selected by the current instruction hold the previous status without change. While the TAP controller is in this state, the instruction does not change.

(10) Update-DR

The boundary scan register has a parallel output latch to prevent changes in parallel output (while shifted to the shift register path concatenated) by certain instructions (for example, EXTEST instruction).

In the Update-DR controller state, data is latched from the shift register to the parallel output latch of this register at the falling edge of the JCK pin signal.

The data retained latched to the parallel output latch changes depending on this controller state (the data does not change with the other controller states).

The previous states of all the shift register of the boundary scan register selected by the current instruction are retained.

While the TAP controller is in this state, the instruction does not change.

If the JMS pin signal is held high at the rising edge of the JCK pin signal with the TAP controller in this state, the controller enters the Select-DR-Scan state.

If the JMS signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Run-Test/Idle state.

(11) Capture-IR

In this controller state, the shift register loads the pattern of a fixed logic value [01 (binary)] to the instruction register at the rising edge of the JCK pin signal.

The previous states of both the bypass register and boundary scan register selected by the current instruction are retained without change.

While the TAP controller is in this state, the instruction does not change.

If the JMS pin signal is held high at the rising edge of the JCK pin signal while the TAP controller is in this state, the controller enters the Exit1-IR state.

If the JMS pin signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Shift-IR state.

(12) Shift-IR

In this controller state, JDI and JDO are connected by the shift register in the instruction register. The shift data is shift one state toward the serial output direction at each rising edge of the JCK pin signal.

The boundary scan register or bypass register selected by the current instruction holds the previous state without change.

While the TAP controller is in this state, the instruction does not change.

If the JMS pin signal is held high at the rising edge of the JCK pin signal with the TAP controller in this state, the controller enters the Exit1-IR state. If the JMS pin signal is held low, the controller remains the Shift-IR state.

(13) Exit1-IR

This is a temporary controller state. If the JMS pin signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Update-IR state. This ends the scan process.

If the JMS pin signal is held low at the rising edge of the JCK pin, the TAP controller enters the Pause-IR state.

Both the bypass register and boundary scan register selected by the current instruction retain their states without change.

While the TAP controller is in this state, the instruction does not change.

(14) Pause-IR

In this controller state, shift of the instruction register is temporarily stopped. The bypass register and boundary scan register selected by the current instruction hold the previous state without change.

While the TAP controller is in this state, the instruction does not change. The instruction register holds the current state.

While the JMS pin signal is low, the TAP controller remains in this state. If the JMS pin signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Exit2-IR state.

(15) Exit2-IR

This is a temporary controller state. If the JMS pin signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Update-IR state. This ends the scan process.

If the JMS pin signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Shift-IR state.

Both the bypass register and boundary scan register selected by the current instruction retain their states without change.

While the TAP controller is in this state, or while the instruction register holds the current state, the instruction does not change.

(16) Update-IR

In this controller state, the instruction shifted to the instruction register is latched to the parallel output latch from the shift register path at the falling edge of the JCK pin signal. Once a new instruction has been latched, it is used as the current instruction.

The bypass register and boundary scan register selected by the current instruction hold the previous state.

If the JMS pin signal is held high at the rising edge of the JCK pin signal while the TAP controller is in this state, the TAP controller enters the Select-DR-Scan state.

If the JMS pin signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Run-Test/Idle state.

The Pause-DR controller state in (8) and Pause-IR controller state in (14) temporarily stop shifting of data in the bypass register, boundary scan register, or instruction register.

6.5 TAP Controller Operation

The TAP controller operates as follows.

The state of the controller is changed by either of (1) and (2) below.

(1) Rising edge of JCK pin signal
(2) JRST_B pin input

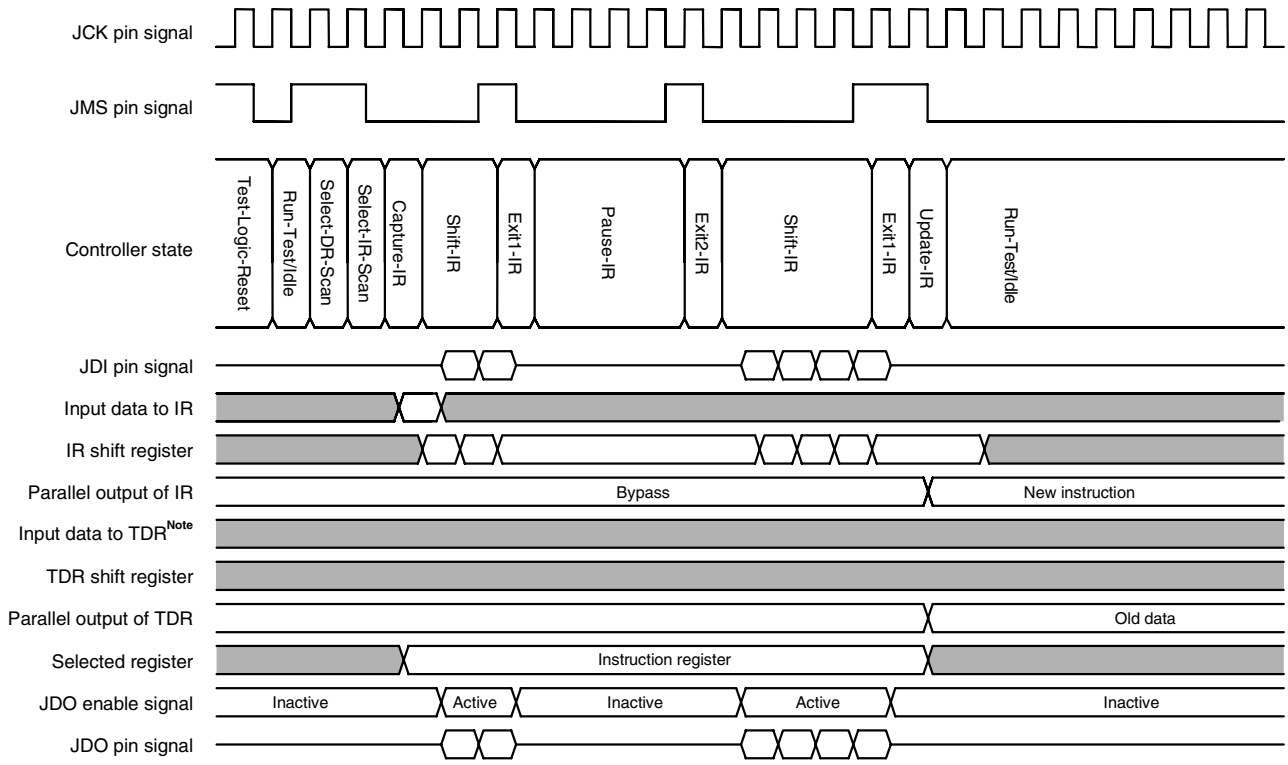
The TAP controller generates signals that control the operations of the bypass register, boundary scan register, and instruction register defined by the IEEE1149.1 JTAG Boundary Scan Standard (see **Figures 6-4** and **6-5**).

The JDO pin output buffer and the peripheral circuit that selects a register whose contents are to be output to the JDO pin are controlled as shown in Table 6-1. The JDO pin defined in this table changes at the falling edge of the JCK pin signal after it has entered each state.

Table 6-1. Operation in Each Controller State

Controller State	Selected Register to Be Driven to JDO Pin	JDO Pin Driver
Test-Logic-Reset	Undefined	High impedance
Run-Test/Idle		
Select-DR-Scan		
Select-IR-Scan		
Capture-IR		
Shift-IR	Instruction register	Active
Exit1-IR	Undefined	High impedance
Pause-IR		
Exit2-IR		
Update-IR		
Capture-DR		
Shift-DR	Data register (boundary scan register, bypass register)	Active
Exit1-DR	Undefined	High impedance
Pause-DR		
Exit2-DR		
Update-DR		

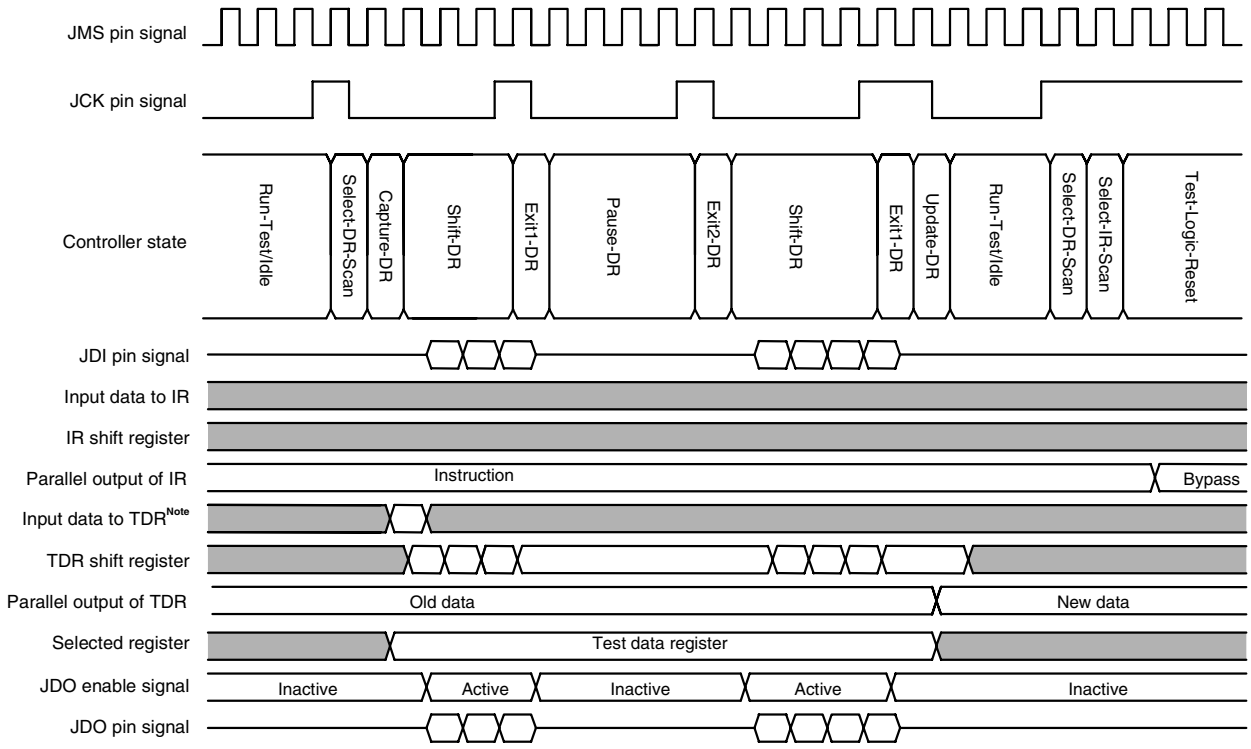
Figure 6-4. Operation of Test Logic (Instruction Scan)



Note TDR (Test Data Register): Boundary scan register and bypass register

Remark : Don't care or undefined

Figure 6-5. Operation of Test Logic (Data Scan)



Note TDR (Test Data Register): Boundary scan register and bypass register

Remark : Don't care or undefined

6.6 Initializing TAP Controller

The TAP controller is initialized as follows:

(1) The TAP controller is not initialized by the operation of system input such as system reset.
(2) The TAP controller enters the Test-Logic-Reset controller state at the fifth rising edge of the JCK pin signal (while the JMS pin signal is held high).
(3) The TAP controller asynchronously enters the Test-Logic-Reset state when the JRST_B signal is input.

6.7 Instruction Register

This register is defined as follows (see **Section 6.2**).

(1) The instruction shifted and input to the instruction register is latched so that it changes only in the Update-IR and Test-Logic-Reset controller states.
(2) Data is not inverted since it has been serially input to the instruction register until it is serially output.
(3) A fixed binary pattern data "01" (with LSB (Least Significant Bit) being "1") is loaded to this register cell in the Capture-IR controller state.
(4) A fixed binary pattern data "01" (with LSB (Least Significant Bit) being "1") is loaded to this register cell in the Test-Logic-Reset controller state.
(5) While this register is read, data is output from the JDO pin, starting from the LSB to the MSB, at each falling edge of the JCK pin signal.

The JTAG boundary scan circuit of the μPD98411 can support only the following three instructions depending on the data set to the instruction register.

- BYPASS instruction
- EXTEST instruction
- SAMPLE/PRELOAD instruction

Instruction Register		Supported Instruction
D1	D0	
0	0	EXTEST instruction
0	1	SAMPLE/PRELOAD instruction
1	0	Unused (BYPASS instruction)
1	1	BYPASS instruction

6.7.1 BYPASS Instruction

This instruction is specified by instruction data "11" or "10". This instruction is used to select only the bypass register (to access between the JDI and JDO pins serially) in the Shift-DR controller state.

While this instruction is selected, the operation of the JTAG boundary scan circuit does not affect the operation of the μPD98411.

This bypass instruction is selected while the TAP controller is in the Test-Logic-Reset state.

6.7.2 EXTEST Instruction

This instruction is specified by instruction data "00". In the Shift-DR controller state, this instruction is used to select the boundary scan register of serial access between the JDI and JDO instructions.

- While this instruction is selected:
  The states of all the signals driven from the system output pins are completely defined by the data shifted to the boundary scan register. In the Update-DR controller state, the states of all the signals are changed only by the falling edge of the JCK pin signal.
  The states of all the signals input from the system input pins are loaded to the boundary scan register at the rising edge of the JCK pin signal while the TAP controller is in the Capture-DR state.

6.7.3 SAMPLE/PRELOAD Instruction

This instruction is specified by instruction data "01". This instruction can execute two functions, SAMPLE and PRELOAD, with a single instruction.

6.7.4 Boundary Scan Data Bit Definition

NEC can supply the BSDL (Boundary Scan Description Language) file for the μPD98411 upon request.

CHAPTER 7 BOARD LAYOUT

Because the μPD98411 has a PLL circuit whose operation is likely to be affected by noise, and because the interface at the line side is high-speed, this must be considered when determining the layout of the board.

The power and ground pins of the μPD98411 are classified according to the supply destination block, into the three types listed in Table 7-1.

Table 7-1. Classification of Power and Ground Pins

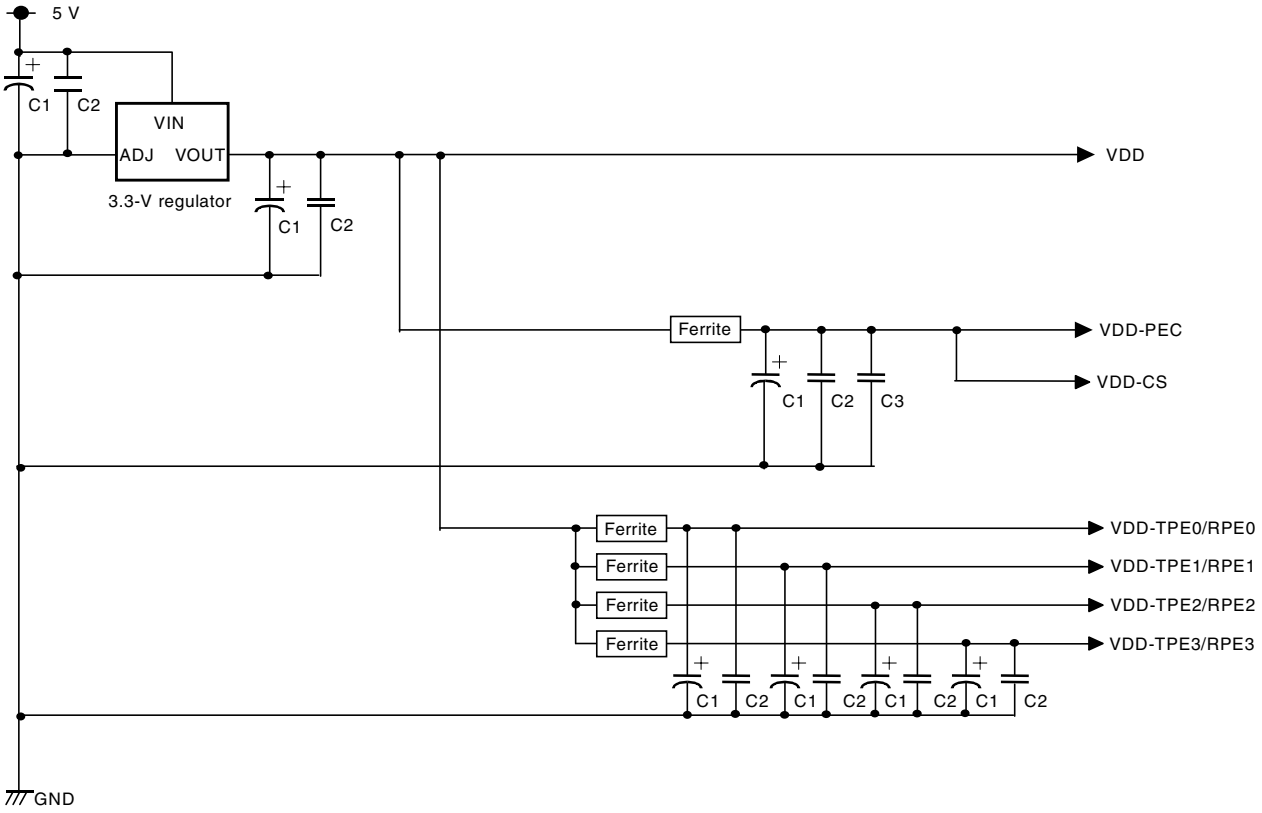
Supply Block		Pin Name	Pin No.	Noise Immunity
<1> Logic block power and ground		VDD	8, 14, 21, 40, 46, 61, 81, 100, 120, 132, 140, 147, 160, 164, 173, 181, 187, 194, 201, 208, 214, 220, 227, 234, 240	
		GND	1, 2, 11, 20, 35, 41, 50, 60, 62, 80, 101, 107, 121, 122, 139, 148, 154, 161, 167, 179, 180, 188, 191, 200, 207, 221, 224, 233	
<2> Power and ground for transmit clock synthesizer PLL		VDD-PEC	51	Low
		GND-PEC	54	
		VDD-CS	57	
		GND-CS	56	
★ **<3>** High-speed interface block section	Serial-to-parallel conversion section and power supply ground for transmission P-ECL section	VDD-TPE0 VDD-TPE1 VDD-TPE2 VDD-TPE3	68 77 88 97	Low
		GND-TPE0 GND-TPE1 GND-TPE2 BND-TPE3	71 82 91 102	
	Clock recovery PLL block section and power supply ground for reception P-ECL section	VDD-RPE0 VDD-RPE1 VDD-RPE2 VDD-RPE3	75 86 95 106	Low
		GND-RPE0 GND-RPE1 GND-RPE2 GND-RPE3	72 83 92 103	

Pins **<2>** and **<3>**, except those in the logic block **<1>**, supply power to the internal synthesizer/clock recovery PLL and high-speed interface block of the μPD98411. The noise superimposed on these power and ground lines affects the characteristics of the μPD98411, such as the jitter output of the transmit data and the jitter tolerance of the receive data. Therefore, make sure that no noise leaks from other circuits to these lines.

(1) Insertion of capacitor

Insert a capacitor into each power pin. Insert a pair consisting of a laminated tantalum capacitor (10 to 47 μF) and a 0.1-μF ceramic capacitor into power pins **<2>** and **<3>**. Position the 0.1-μF capacitor as close to the pin as possible.

★ **Figure 7-1. μPD98411 and Peripheral Block**



C1 = 10 to 47-μF laminated capacitor, C2 = 0.1 μF, C3 = 330-pF ceramic capacitor

Ferrite : (Ferrite beads) A filter that is inserted depending on the frequency of the noise. This filter is not essential.

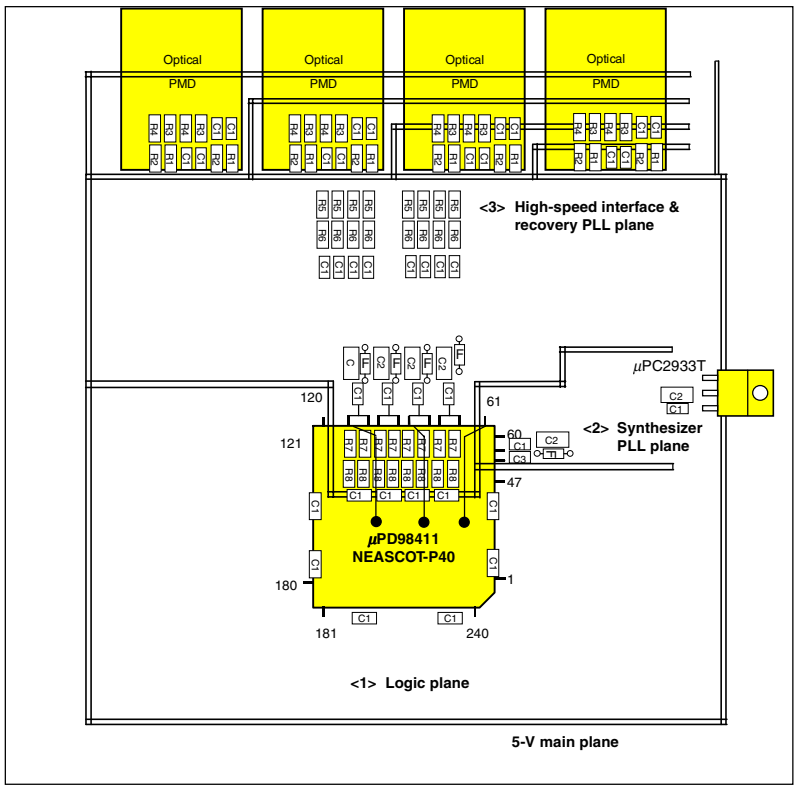
3.3-V regulator : The μPD98411 draws a maximum of 800 mA. Select a regulator with a sufficient margin.

(2) Division of power plane

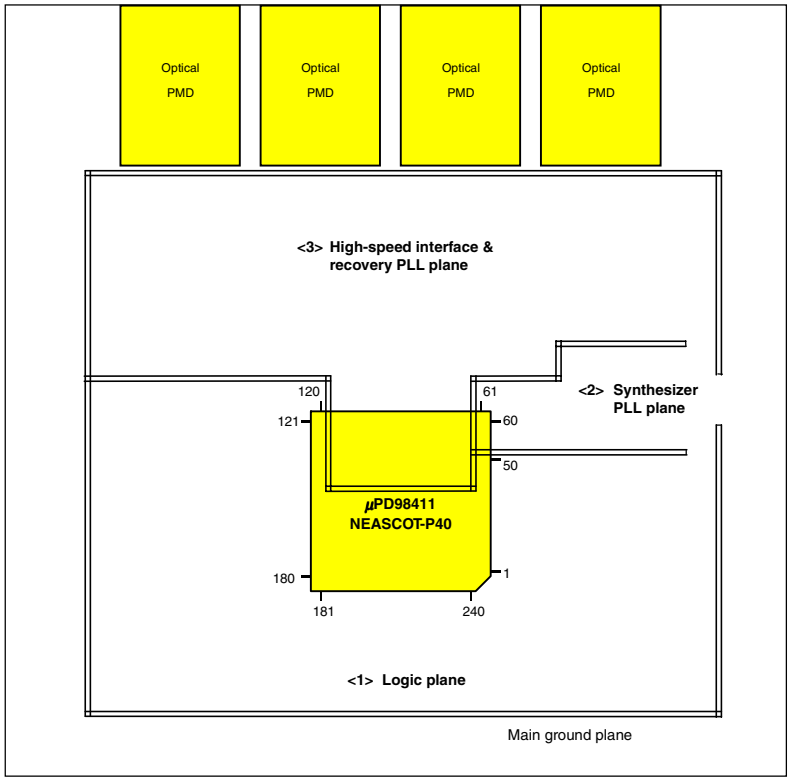
Figure 7-2 shows an example in which separate power and ground planes are used on a four-layer printed circuit board. **<1>**, **<2>**, and **<3>** in the figure corresponds to the classification numbers in Table 7-1. Position the 3.3-V regulator equidistant from the three planes. Make sure that noise is not superimposed on the synthesizer PLL plane **<2>** and the high-speed interface plane **<3>** from the logic plane **<1>**. Each power plane should have as wide an area as possible so that the impedance of each plane does not rise as a result of using separate planes. Especially, the high-speed interface plane **<3>** must be relatively large in area because it consumes a large amount of power. If a sufficient area cannot be provided, the use of a separate ground plane is not recommended. Use a united plane.

Figure 7-2. Power and Ground Planes

Power layer



Ground layer

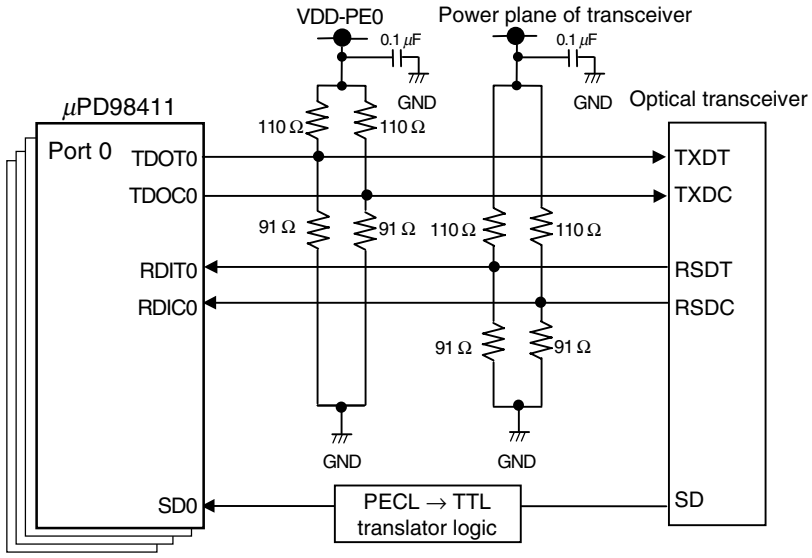


(3) Pull-up power supply of PECL interface

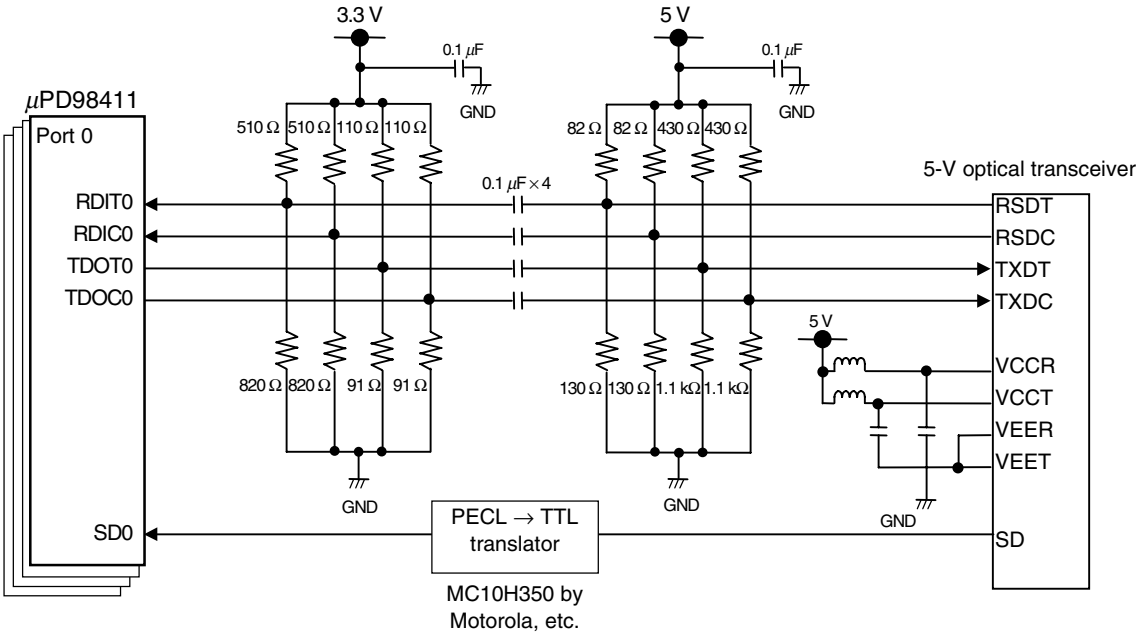
The interface at the line side of the μPD98411 is a PECL-level interface that must be terminated with 50 ohms at VDD-2V. NEC recommends that power be supplied to the pull-up resistor of the interface from the high-speed interface plane **<3>** containing VDD-PE0 to VDD-PE3. In addition, insert a 0.1-μF capacitor into each pull-up resistor.

Figure 7-3. PECL Interface

Example of connecting 3.3-V transceiver



Example of connecting 5-V transceiver



8.1 Restrictions

Table 8-1 lists the restrictions that apply to the μPD98411. Before using the μPD98411, please study them sufficiently.

Table 8-1. Restrictions

	Item
1	Performance counters are stopped when SD = L is detected.
2	Disappearance of cause for alarm detection at a software reset based on the ICR bit
3	Cell transfer in the LOS detection status based on SD = L
4	Restriction related to register access interval
5	Restrictions related to the error rate monitor setting procedure
6	Restriction related to the setting/resetting of transmission of a pseudo-error frame
7	Restriction related to changes to the transmission OH byte insert register
8	Restriction related to changes to receive cell processing mode
9	Restriction related to the setting/resetting of ATM loopback mode
10	Restriction related to ATM loopback mode switching when FIFO is full
11	Restriction related to the UTOPIA parity function in Dual 8-bit mode
12	Restriction related to reading of the interrupt cause register

8.2 Descriptions of Restrictions

8.2.1 Performance Counters Are Stopped When SD = L Is Detected

The specification states that all performance monitoring counters (Information Cell, Idle Cell, FIFO Full, HEC, B1, B2, B3, L-REI, P-REI, and FJ) are to be forced to stop when LOS detection is under way (0s are received consecutively for 50 μs or the SD pin input is low).

The Information Cell counter does not count cells that are received while LOS detection is under way. When a loopback test is conducted by disconnecting the reception line cable and placing the μPD98411 in TPLP loopback mode with LOS detection enabled, cells that are input to the μPD98411 pass through it and are looped back at the reception UTOPIA interface. Note, however, that these cells are not counted by the Information Cell counter, which is intended to count receive cells.

8.2.2 Disappearance of Cause for Alarm Detection at a Software Reset Based on the ICR Bit

The specification states that the interrupt cause register bits that are set by detecting an event for reporting on a status such as LOS are to be kept set until the register is read-accessed after recovery from the event. Once the PICR register (interrupt cause register) is cleared using the ICR bit of the CMR2 register (interrupt cause register initialization), however, the bits will not be set again even if the event detection status lasts; they will be set again only when the event is detected again after recovery from it. This condition applies to the events for reporting on the LOS, LOF, AIS, RDI, OCD, LCD, OOF, LOP, RAPS, OOL, and CMD statuses.

There is no problem with a hardware reset and a reset caused by the ALL bit of the CMR2 register, because the interrupt cause register is set again. There is no problem with a reset caused by a register read either, because the interrupt cause register is kept set while the detected status lasts, and cleared only when the interrupt cause disappears.

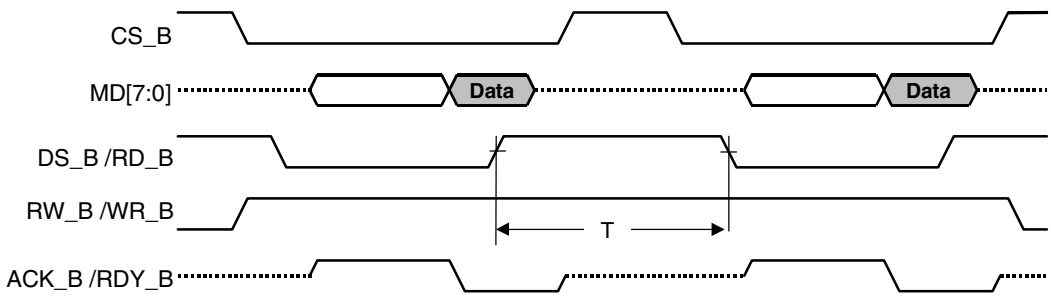
8.2.3 Cell Transfer in the LOS Detection Status Based on SD = L

The μPD98411 enters the LOS detection status when data consisting of all 0s is received consecutively for 50 µs or the SD pin input goes low. The μPD98411 is designed to allow the receive cell to be output to the UTOPIA interface even when the LOS detection status is entered. Therefore, if cell synchronization is established, the cell is stored to the receive FIFO and output to the reception UTOPIA interface even after the LOS detection status is entered. When normal receive data is received from the line, making only the input to the SD pin low causes the μPD98411 to report on LOS detection; note, however, that the receive cell is output.

8.2.4 Restriction Related to Register Access Interval

If the host CPU attempts to read-/write-access the registers in the μPD98411 at intervals shorter than "7 $\times$ REFCLK cycles (about 364 ns)", a read/write may not be performed normally. Be sure to keep the register access interval (T in Figure 8-1) longer than at least "7 $\times$ REFCLK cycle".

Figure 8-1. Register Access Interval (Example of Read → Read)



8.2.5 Restrictions Related to the Error Rate Monitor Setting Procedure

When the error rate monitor function is used, it is necessary to set a "threshold value" in the threshold registers (such as B1THR and B2THR) and the "monitor time" in the time register (FRMN register). The following restrictions apply when these values are set.

<1> A "threshold value" set in the threshold register becomes valid only after the FRMN is write-accessed. For this reason, a value must be set in the FRMN register after the threshold register.

<2> Once the FRMN register is accessed, an interval of "130 × REFCLK cycle (about 7 μs)" must be allowed before the FRMN register is accessed again. This does not apply unless the FRMN register has been accessed before the threshold register is set.

8.2.6 Restriction Related to the Setting/Resetting of Transmission of a Pseudo-Error Frame

If the timing of transmission of transmission OH bytes coincides with the timing of the setting and resetting of transmission of a pseudo-error frame related to the bytes, the OH byte data being transferred may be disrupted. Transmission of OH bytes with disrupted data can occur only in one frame immediately after the timing coincidence.

8.2.7 Restriction Related to Changes to the Transmission OH Byte Insert Register

If the timing of transmission of transmission OH bytes coincides with the changing to the relevant OH insert register, the OH byte data being transmitted may be disrupted. Transmission of OH bytes with disrupted data can occur only in one frame immediately after the timing coincidence. It does not occur when the same value is written to the insert register.

8.2.8 Restriction Related to Changes to Receive Cell Processing Mode

If the timing of changing the receive cell processing mode coincides with the timing of reception of the relevant cell, the wrong processing may be performed. Before receiving valid cells, set or change the mode.

Table 8-2. Mode Changes and Incorrect Operations

Mode Change and Receive Cell	Operation
If the setting/changing of the DCHPR and DCHPMR registers coincide with the reception of cells having a header VPI/VCI = 0/0	Cells may be dropped by mistake even when they do not match the drop cell header patterns in the DCHPR and DCHPMR registers. Cells that are dropped are only those cells that have the header VPI/VCI = 0/0.
If the changing to the CORE bit of the MDR3 register coincides with the reception of a cell having a 1-bit error in the overhead	The received cell may be output without correcting the 1-bit error. Only one cell is output by mistake.

8.2.9 Restriction Related to the Setting/Resetting of ATM Loopback Mode

If switching occurs from ALP mode to ordinary transmission/reception mode under either of the following conditions, the first cell data to be output to the transmission line side and reception UTOPIA interfaces immediately after the mode switching may be disrupted.

<1> ALP mode is set and reset at intervals of about 3.5 μs or shorter.

<2> The transmission function is disabled in ALP mode (TDIS bit of the CMR2 register = 1).

Once ALP mode is set, allow 3.5 μs or more before ALP mode is reset. Do not disable the transmission function after ALP mode has been set.

8.2.10 Restriction Related to ATM Loopback Mode Switching when FIFO Is Full

If ATM layer loopback mode (ALP mode) is set or reset when the receive FIFO is full (8 cells have been stored), the status bit for indicating a receive FIFO overflow may be set and the FIFO Full counter may be incremented even when no cell has been dropped.

After the ATM loopback is set/reset, clear the status bit that indicates an FIFO overflow by mistake, and the counter value.

8.2.11 Restriction Related to the UTOPIA Parity Function in Dual 8-Bit Mode

When the UTOPIA interface is used in Dual 8-bit mode, the μPD98411 cannot make a transmission-side UTOPIA parity check correctly. In this mode, ignore the result of the parity check.

8.2.12 Restriction Related to Reading of the Interrupt Cause Register

If the timing when an event within the LSI chip occurs for the interrupt cause register (for reporting the detection of a line failure, counter overflow, and other events) coincides with the timing when the host reads the register, the μPD98411 may fail to set the relevant register bits, resulting in the host failing to detect the occurrence of the event.

In interrupt (RCM = 0) mode, the interrupt signal may fail to become active if the timing of event occurrence coincides with the timing of a register read. In RCM = 1 mode, the interrupt signal may fail to become active if the timing of setting the interrupt cause register because of event occurrence coincides with the timing of a register read.

Table 8-3 lists the interrupt cause registers and their bits that may experience the symptoms described above.

Table 8-3. Interrupt Cause Registers and Their Bits

Register	Bit		Indicated Information	Remark
PICR	0	RFO	Occurrence of receive FIFO overflow	This bit is set when cells are dropped because of a receive FIFO overflow. It is set for an individual cell. If cells are dropped consecutively, the bit is set again if the second cell is dropped even when the first cell cannot be detected. This symptom does not occur to the other bits of the PICR register.
PCR	5	FJ	Occurrence of FJ	These bits are set if an event is detected in a receive frame. They are set for an individual receive frame. This symptom does not occur to the other bits of the PCR register.
	4	B1E	Occurrence of B1 bit error	
	3	B2E	Occurrence of B2 bit error	
	2	B3E	Occurrence of B3 bit error	
	1	LREI	Detection of LREI	
	0	PREI	Detection of PREI	
PCOCR1	5	B1EC	Occurrence of B1 counter overflow	These bits are set if the PM counter passes through all 1s (FH).
	4	B2EC	Occurrence of B2 counter overflow	
	3	B3EC	Occurrence of B3 counter overflow	
	2	LREC	Occurrence of LREI counter overflow	
	1	PREC	Occurrence of PREI counter overflow	
	0	FJC	Occurrence of FJ counter overflow	
PCOCR2	7	Z2_6	Six occurrences of receive Z2#1 byte matching	These bits are used only when the MGM bit of the MDR2 register is set to 1. They are set if the same receive Z2#1 byte is received 6 or 12 times consecutively.
	6	Z2_12	Twelve occurrences of receive Z2#1 byte matching	
	3	HECC	Occurrence of overflow from the HEC dropped cell counter	These bits are set if the PM counter passes through all 1s (FH).
	2	FULC	Occurrence of overflow from the FIFO Overflow dropped cell counter	
	1	IDLC	Occurrence of idle cell counter overflow	
	0	INFC	Occurrence of receive cell counter overflow	

Table 8-4. Countermeasures

Register/bit	Countermeasure
PICR (RFO) PCR	Besides the history report function of these registers, a counter is available which counts the number of detected events. Poll these counters as an alternative method for history confirmation.
PCOCR1 and PCOCR2 (excluding Z2_6 and Z2_12)	These counters are cleared to 0 each time the CPU read-accesses them. Reading a counter before it overflows can prevent its overflow. The counters B1, B3, and P-REI can overflow within the shortest time, that is, 1.024 seconds. Keeping these counters polled at intervals of one second or below can suppress their overflow.

[MEMO]

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