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RENESAS

User's Manual

μPD98410

(NEASCOT-X10™)

1.2G ATM SWITCH LSI

Document No. S12523EJ2V0UMJ1 (2nd edition)
Date Published October 2000 N CP(K)

Phase-out/Discontinued

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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M8E 00. 4

PREFACE

Readers

This manual is intended for user engineers who wish to understand the functions of the μPD98410 and design application systems using it.

Purpose

This manual explains the hardware functions of the μPD98410 in the following organization.

Organization

This manual consists of the following chapters.

- General
- Pin functions
- Functional outline
- Internal registers
- JTAG boundary scan
- Limitations
- FAQ (Frequency Asked Questions)

How to Read This Manual

It is assumed that the readers of this manual have a general knowledge of electricity, logic circuits, and microcomputers.

To understand the overall functions of the μPD98410
→ Read this manual in the order of Table of Contents.

If you have any questions about the operation of the μPD98410
→ Read **CHAPTER 7 FAQ (Frequently Asked Questions).**

Conventions

Data significance	:	Left: high-order digit, right: low-order digit
Active low	:	××××_B (_B following pin or signal name)
Memory map address	:	Top: high-order, bottom: low-order
Note	:	Explanation of part of text marked **Note**
Caution	:	Important information
Remark	:	Supplementary information
Numeric notation	:	Binary ... ×××× or ××××B Decimal ... ×××× Hexadecimal ... ××××H

Related documentation

Some of the related documents are preliminary editions but are not so specified below.

- Pamphlet : S12131E
- Data sheet : S12624E
- Application Note : S13107E

Phase-out/Discontinued

[MEMO]

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LIST OF FIGURES (2/2)

LIST OF TABLES

Phase-out/Discontinued

[MEMO]

CHAPTER 1 GENERAL

The μPD98410 (NEASCOT-X10) is an LSI integrating ATM switch functions on a single chip. It has four UTOPIA Level2 interfaces and can switch 24 × 24 circuits by connecting multiple PHY devices. This LSI employs a shared buffer non-blocking type switch and realizes a switch capacity of 1.2G bps by using an externally connected SRAM for buffering cells.

1.1 Features

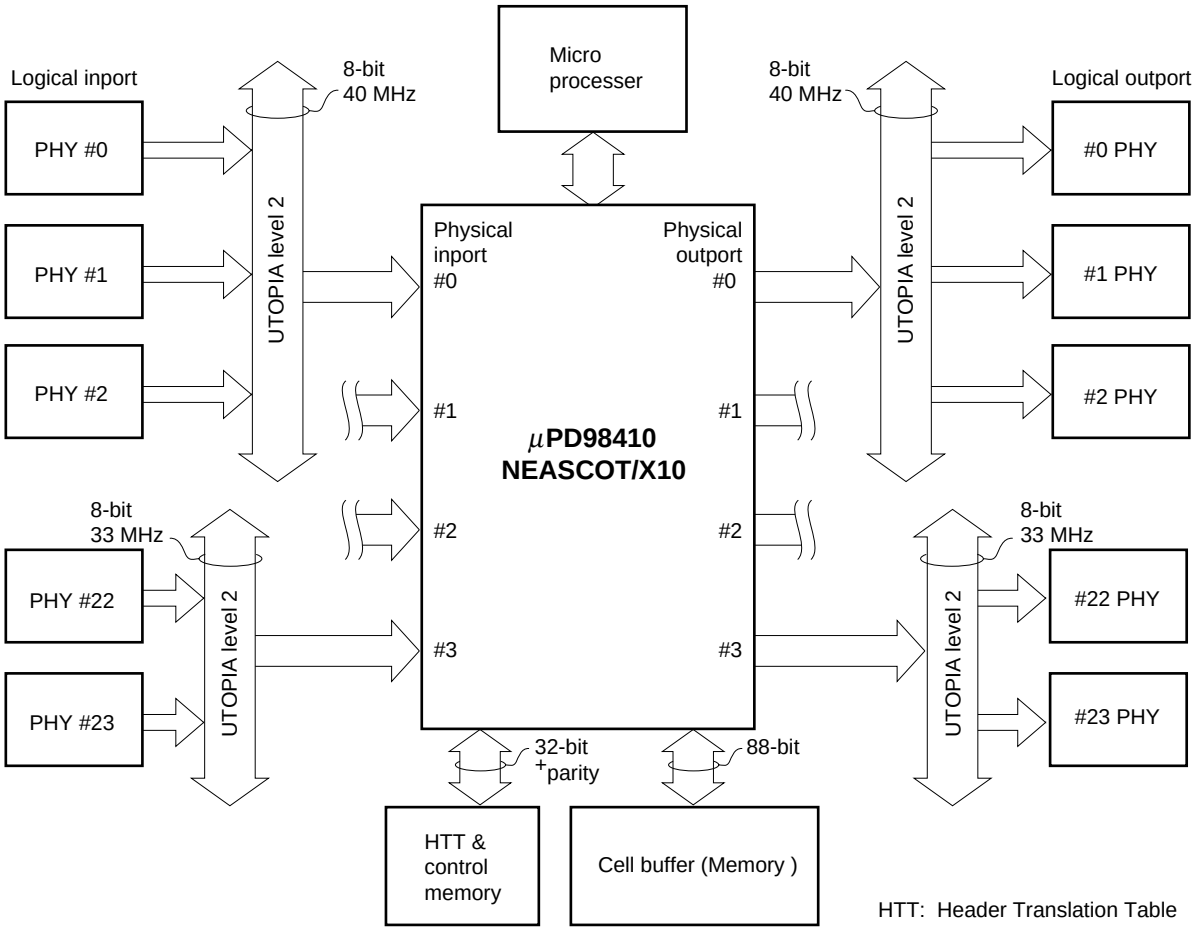
- Conforms to ATM FORUM UNI Version 3.1 & 4.0
- Realizes all switch functions with a single chip
- Non-blocking type with switch capacity of 1.2G bps
- Can switch 24 logical ports via four UTOPIA Level2 (8 bits/40 MHz) interfaces
- Multi-speed (155M bps, 52M bps, 25M bps, etc.)
- Supports 16K/32K/64K VP/VC and 1K/2K/4K multi-cast VP/VC
- Shared buffer architecture using standard SRAM
- Cell buffer capacity: 12.8K/25.6K/51.2K cells
- Supports four QOS classes (CBR, VBR, ABR, UBR)
- ABR traffic control (binary mode)
- Supports EPD (Early Packet Discard) and PPD (Partial Packet Discard)
- +3.3-V single power source (directly connectable with +5-V TTL level signals)
- Test function: Supports JTAG (IEEE 1149.1)

1.2 Ordering Information

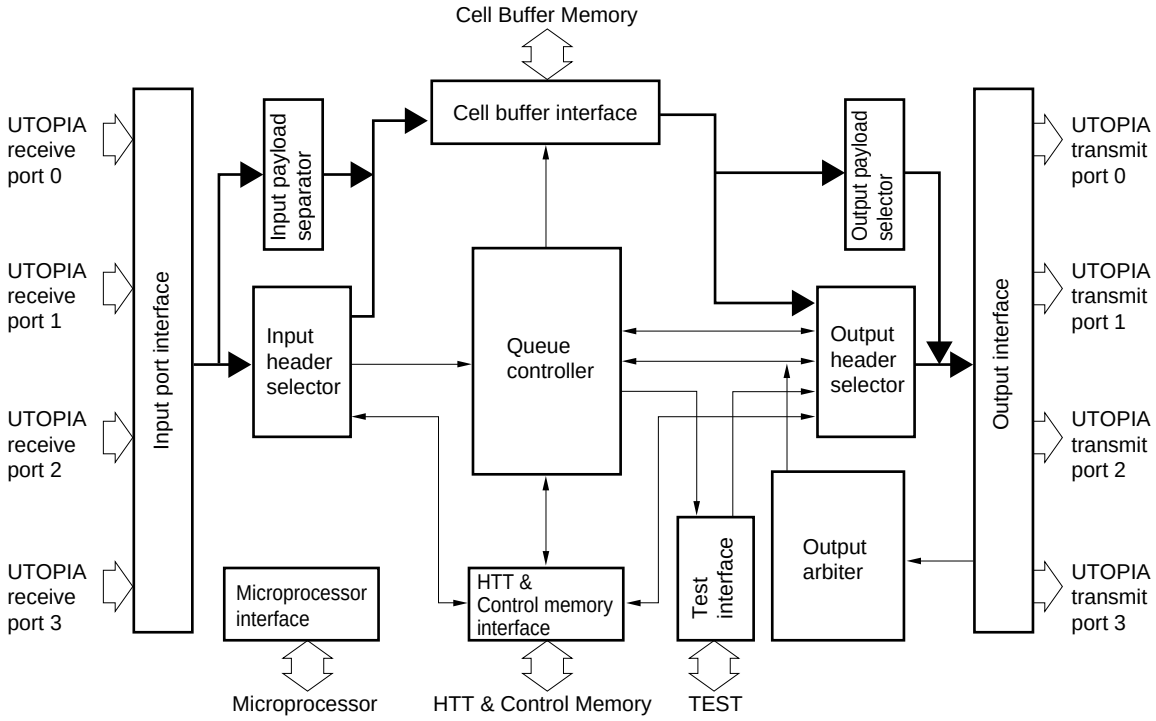
Part Number	Package
μPD98410S2-K6	580-pin plastic BGA (45 × 45 mm)

1.3 Example of System Configuration (Application)

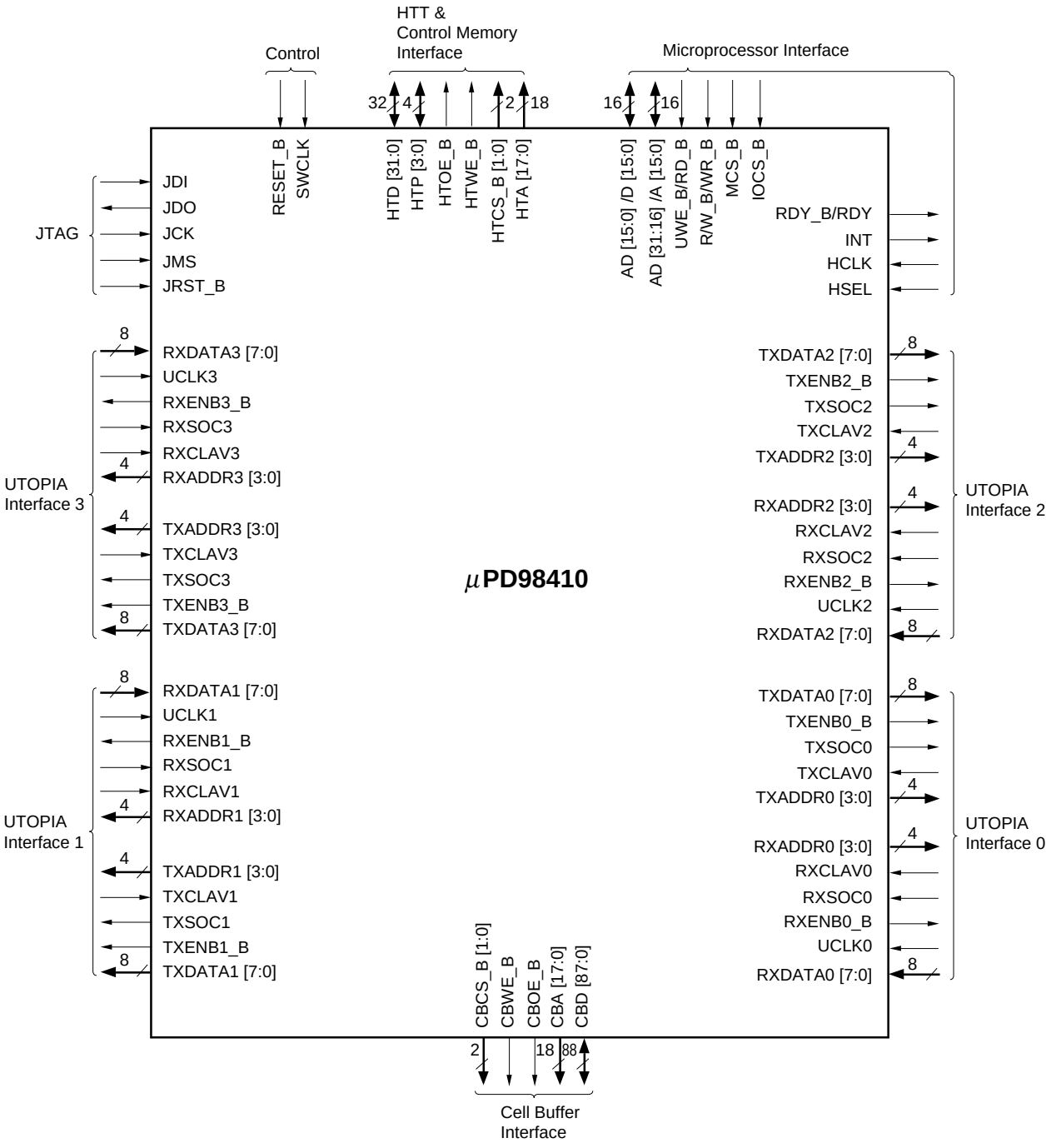
The μPD98410 can be used to realize an ATM layer cell switching function by connecting it to a microprocessor, SRAM for use as a cell buffer, and a header translation table (HTT)/SRAM for storing control information as shown below.



1.4 Block Diagram

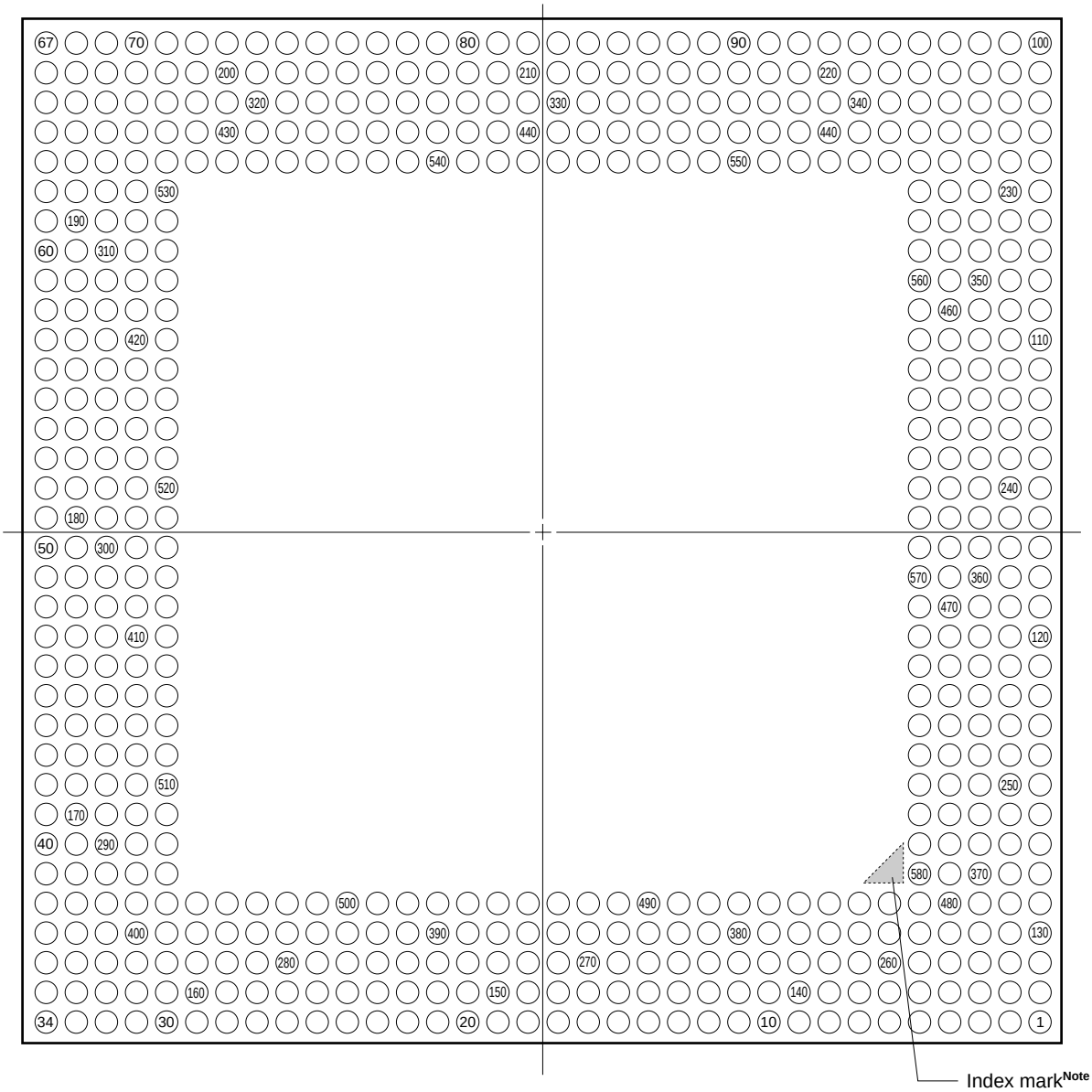


1.5 Pin Configuration



2.1 Pin Configuration (Bottom View)

580-pin BGA package



Note The index mark is shown in Top View.

Pin name

(1) Power

V_{DD} : Supply Voltage
GND : Ground

(2) UTOPIA

RXADDR*3 - RXADDR*0 : Receive Address
RXDATA*7 - RXDATA*0 : Receive Data Bus
RXSOC3 - RXSOC0 : Receive Start of Cell
RXENB3_B - RXENB0_B : Receive Enable Data Transfers
RXCLAV3 - RXCLAV0 : Receive Cell Buffer Available
UCLK3 - UCLK0 : UTOPIA Clock
TXADDR*3 - TXADDR*0 : Transmit Address
TXDATA*7 - TXDATA*0 : Transmit Data Bus
TXSOC3 - TXSOC0 : Transmit Start of Cell
TXENB3_B - TXENB0_B : Transmit Enable Data
TXCLAV3 - TXCLAV0 : Transmit Cell Buffer Available

(3) Memory Interface

HTA17 - HTA0 : HTT Memory Address
HTD31 - HTD0 : HTT Memory Data Bus
HTP3 - HTP0 : HTT Memory Data Bus Parity
HTCS1_B, HTCS0_B : HTT Memory Chip Select
HTWE_B : HTT Memory Write Enable
HTOE_B : HTT Memory Output Enable
CBA17 - CBA0 : Cell Buffer Memory Address
CBD87 - CBD0 : Cell Buffer Memory Data Bus
CBCS1_B, CBCS0_B : Cell Buffer Memory Chip Select
CBWE_B : Cell Buffer Memory Write Enable
CBOE_B : Cell Buffer Memory Output Enable

* = 0 to 3

(4) CPU Interface

HSEL : Host Bus Mode Select
IOCS_B : I/O Chip Select
MCS_B : Memory Chip Select
RDY_B, RDY : I/O Ready, Memory Ready
INT : Interrupt Request
HCLK : Host Clock
AD31 - AD0 : Address and Data
R/W_B : Read/Write
UWE_B : Upper Word Enable
A15 - A0 : Address
D15 - D0 : Data
WR_B : Write Strobe
RD_B : Read Strobe

(5) JTAG

JDI : JTAG Data Input
JDO : JTAG Data Output
JCK : JTAG Data Clock
JMS : JTAG Mode Select
JRST_B : JTAG Reset

(6) Other

SWCLK : System Clock
RESET_B : Hardware Reset
IC : Internal Connected
CG : Connect Ground
PU : Pull-up

2.2 Pin Layout

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Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O
1	GND		37	CBD72	I/O	73	RXDATA05	I
2	GND		38	CBD69	I/O	74	V_{DD}	
3	IC	O	39	CBD66	I/O	75	GND	
4	IC	O	40	CBD63	I/O	76	RXCLAV0	I
5	CG	I	41	IC	O	77	V_{DD}	
6	IC	O	42	CBD58	I/O	78	TXADDR01	O
7	JRST_B	I	43	CBD56	I/O	79	TXENB0_B	O
8	RXDATA36	I	44	CBD51	I/O	80	TXDATA04	O
9	RXDATA32	I	45	CBD49	I/O	81	TXDATA00	O
10	IC	O	46	CBD46	I/O	82	RXDATA26	I
11	RXSOC3	I	47	CBWE_B	O	83	V_{DD}	
12	RXADDR31	O	48	CBA17	O	84	RXDATA25	I
13	TXADDR31	O	49	GND		85	GND	
14	TXENB3_B	O	50	CBA13	O	86	GND	
15	V_{DD}		51	IC	O	87	RXCLAV2	I
16	TXDATA32	O	52	CBA9	O	88	RXADDR21	O
17	TXDATA30	O	53	CBA7	O	89	TXADDR21	O
18	TXDATA31	O	54	CBA4	O	90	TXCLAV2	I
19	RXDATA17	I	55	CBA0	O	91	GND	
20	RXDATA13	I	56	CBD41	I/O	92	TXDATA23	O
21	RXDATA10	I	57	CBD37	I/O	93	TXDATA20	O
22	RXENB1_B	O	58	CBD35	I/O	94	IOCS_B	I
23	V_{DD}		59	CBD30	I/O	95	RDY_B/RDY	O
24	RXADDR10	O	60	V_{DD}		96	CG	I
25	GND		61	CBD24	I/O	97	CG	I
26	V_{DD}		62	CBD20	I/O	98	IC	O
27	TXDATA15	O	63	CBD17	I/O	99	GND	
28	TXDATA11	O	64	CBD15	I/O	100	GND	
29	CBD86	I/O	65	GND		101	GND	
30	CBD84	I/O	66	GND		102	IC	O
31	CBD80	I/O	67	GND		103	V_{DD}	
32	V_{DD}		68	GND		104	AD18/A2	I/O
33	GND		69	CBD10	I/O	105	AD14/D14	I/O
34	GND		70	CBD7	I/O	106	AD10/D10	I/O
35	GND		71	CBD4	I/O	107	AD6/D6	I/O
36	CBD74	I/O	72	CBD2	I/O	108	AD3/D3	I/O

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Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O
109	AD1/D1	I/O	146	TXDATA36	O	183	CBA2	O
110	HTA14	O	147	TXDATA33	O	184	CBD42	I/O
111	V_{DD}		148	TXDATA34	O	185	CBD38	I/O
112	HTA9	O	149	GND		186	V_{DD}	
113	V_{DD}		150	RXDATA15	I	187	CBD33	I/O
114	GND		151	RXDATA12	I	188	CBD28	I/O
115	HTCS1_B	O	152	V_{DD}		189	CBD26	I/O
116	GND		153	RXCLAV1	I	190	CBD23	I/O
117	HTCS0_B	O	154	RXADDR11	O	191	GND	
118	V_{DD}		155	TXADDR12	O	192	V_{DD}	
119	HTD29	I/O	156	TXCLAV1	I	193	CBD13	I/O
120	HTD26	I/O	157	TXDATA17	O	194	CBD12	I/O
121	HTD23	I/O	158	TXDATA13	O	195	GND	
122	HTD20	I/O	159	TXDATA10	O	196	CBD9	I/O
123	HTD16	I/O	160	V_{DD}		197	CBD8	I/O
124	HTD15	I/O	161	CBD82	I/O	198	IC	O
125	HTD10	I/O	162	CBD78	I/O	199	V_{DD}	
126	V_{DD}		163	CBD77	I/O	200	RXDATA06	I
127	HTD5	I/O	164	GND		201	RXDATA03	I
128	HTD2	I/O	165	CBD76	I/O	202	RXDATA01	I
129	SWCLK	I	166	CBD73	I/O	203	RXSOC0	I
130	V_{DD}		167	V_{DD}		204	RXADDR02	O
131	GND		168	CBD67	I/O	205	TXADDR03	O
132	GND		169	IC	O	206	TXCLAV0	I
133	GND		170	CBD62	I/O	207	TXDATA06	O
134	CG	I	171	CBD59	I/O	208	TXDATA02	O
135	CG	I	172	CBD57	I/O	209	V_{DD}	
136	IC	O	173	CBD53	I/O	210	RXDATA27	I
137	V_{DD}		174	V_{DD}		211	RXDATA23	I
138	GND		175	GND		212	RXDATA21	I
139	V_{DD}		176	CBCS1_B	O	213	RXENB2_B	O
140	RXDATA34	I	177	V_{DD}		214	RXADDR23	O
141	RXDATA30	I	178	CBA15	O	215	TXADDR23	O
142	V_{DD}		179	CBOE_B	O	216	TXADDR20	O
143	RXADDR33	O	180	CBA11	O	217	TXENB2_B	O
144	TXADDR33	O	181	V_{DD}		218	TXDATA25	O
145	TXCLAV3	I	182	CBA6	O	219	TXDATA22	O

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Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O
220	HCLK	I	256	IC	I/O	293	V_{DD}	
221	MCS_B	I	257	IC	I/O	294	CBD54	I/O
222	R/W_B/	I	258	GND		295	CBD52	I/O
	WR_B		259	GND		296	CBD48	I/O
223	AD31/A15	I/O	260	JDI	I	297	CBD47	I/O
224	AD28/A12	I/O	261	JCK	I	298	CBD45	I/O
225	AD27/A11	I/O	262	RXDATA37	I	299	CBCS0_B	O
226	GND		263	RXDATA33	I	300	CBA16	O
227	AD25/A9	I/O	264	RXDATA31	I	301	CBA12	O
228	AD22/A6	I/O	265	RXENB3_B	O	302	CBA10	O
229	AD20/A4	I/O	266	RXADDR32	O	303	CBA5	O
230	AD16/A0	I/O	267	RXADDR30	O	304	GND	
231	AD12/D12	I/O	268	TXADDR32	O	305	CBA1	O
232	AD8/D8	I/O	269	TXSOC3	O	306	GND	
233	V_{DD}		270	TXDATA37	O	307	CBD39	I/O
234	AD2/D2	I/O	271	V_{DD}		308	CBD34	I/O
235	GND		272	RXDATA14	I	309	GND	
236	HTA12	O	273	GND		310	CBD29	I/O
237	GND		274	RXDATA11	I	311	CBD25	I/O
238	HTA6	O	275	IC	O	312	CBD21	I/O
239	HTA4	O	276	RXSOC1	I	313	CBD18	I/O
240	HTA1	O	277	RXADDR13	O	314	CBD14	I/O
241	HTA3	O	278	TXADDR13	O	315	CBD11	I/O
242	HTOE_B	O	279	TXADDR10	O	316	GND	
243	HTD31	I/O	280	TXENB1_B	O	317	CBD5	I/O
244	HTD28	I/O	281	TXDATA14	O	318	CBD1	I/O
245	HTD24	I/O	282	TXDATA12	O	319	RXDATA07	I
246	GND		283	CBD85	I/O	320	RXDATA04	I
247	HTD17	I/O	284	GND		321	RXDATA00	I
248	V_{DD}		285	CBD79	I/O	322	RXENB0_B	O
249	NTD13	I/O	286	GND		323	RXADDR01	O
250	HTD8	I/O	287	V_{DD}		324	TXADDR02	O
251	HTD7	I/O	288	CBD70	I/O	325	TXADDR00	O
252	HTD4	I/O	289	CBD68	I/O	326	TXSOC0	O
253	HTD0	I/O	290	CBD65	I/O	327	TXDATA05	O
254	RESET_B	I	291	GND		328	TXDATA03	O
255	IC	I/O	292	GND		329	RXDATA24	I

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Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O
330	RXDATA20	I	368	HTD9	I/O	406	CBD60	I/O
331	UCLK2	I	369	HTD6	I/O	407	CBD55	I/O
332	RXSOC2	I	370	GND		408	GND	
333	RXADDR22	O	371	V_{DD}		409	CBD50	I/O
334	GND		372	IC	I/O	410	V_{DD}	
335	TXADDR22	O	373	IC	O	411	CBD44	I/O
336	TXSOC2	O	374	V_{DD}		412	V_{DD}	
337	TXDATA26	O	375	CG	I	413	CBA14	O
338	V_{DD}		376	JDO	O	414	V_{DD}	
339	V_{DD}		377	JMS	I	415	CBA8	O
340	HSEL	I	378	RXDATA35	I	416	V_{DD}	
341	V_{DD}		379	GND		417	CBA3	O
342	AD30/A14	I/O	380	UCLK3	I	418	CBD43	I/O
343	AD29/A13	I/O	381	RXCLAV3	I	419	CBD40	I/O
344	AD26/A10	I/O	382	GND		420	CBD36	I/O
345	AD23/A7	I/O	383	TXADDR30	O	421	CBD32	I/O
346	AD19/A3	I/O	384	V_{DD}		422	CBD31	I/O
347	GND		385	TXDATA35	O	423	CBD27	I/O
348	AD13/D13	I/O	386	V_{DD}		424	CBD22	I/O
349	AD09/D09	I/O	387	RXDATA16	I	425	CBD19	I/O
350	AD7/D7	I/O	388	V_{DD}		426	CBD16	I/O
351	AD4/D4	I/O	389	UCLK1	I	427	IC	O
352	HTA17	O	390	V_{DD}		428	CBD6	I/O
353	HTA15	O	391	GND		429	CBD3	I/O
354	HTA11	O	392	RXADDR12	O	430	CBD0	I/O
355	HTA10	O	393	TXADDR11	O	431	GND	
356	HTA8	O	394	TXSOC1	O	432	RXDATA02	I
357	HTA5	O	395	TXDATA16	O	433	UCLK0	I
358	HTA2	O	396	GND		434	RXADDR03	O
359	HTWE_B	O	397	CBD87	I/O	435	RXADDR00	O
360	HTP3	I/O	398	CBD83	I/O	436	GND	
361	HTD27	I/O	399	CBD81	I/O	437	TXDATA07	O
362	GND		400	CBD75	I/O	438	V_{DD}	
363	HTP2	I/O	401	CBD71	I/O	439	TXDATA01	O
364	HTD21	I/O	402	GND		440	V_{DD}	
365	HTD18	I/O	403	IC	O	441	RXDATA22	I
366	HTD14	I/O	404	CBD64	I/O	442	V_{DD}	
367	HTD11	I/O	405	CBD61	I/O	443	V_{DD}	

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Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O
444	V_{DD}		481	V_{DD}		518	GND	
445	RXADDR20	O	482	GND		519	V_{DD}	
446	V_{DD}		483	V_{DD}		520	GND	
447	TXDATA27	O	484	GND		521	V_{DD}	
448	TXDATA24	O	485	V_{DD}		522	GND	
449	TXDATA21	O	486	GND		523	V_{DD}	
450	GND		487	V_{DD}		524	GND	
451	INT	O	488	GND		525	V_{DD}	
452	UWE_B/RD_B	I	489	V_{DD}		526	GND	
453	GND		490	GND		527	V_{DD}	
454	AD24/A8	I/O	491	V_{DD}		528	GND	
455	AD21/A5	I/O	492	GND		529	V_{DD}	
456	AD17/A1	I/O	493	V_{DD}		530	GND	
457	AD15/D15	I/O	494	GND		531	V_{DD}	
458	AD11/D11	I/O	495	V_{DD}		532	GND	
459	GND		496	GND		533	V_{DD}	
460	AD5/D5	I/O	497	V_{DD}		534	GND	
461	AD0/D0	I/O	498	GND		535	V_{DD}	
462	HTA16	O	499	V_{DD}		536	GND	
463	HTA13	O	500	GND		537	V_{DD}	
464	V_{DD}		501	V_{DD}		538	GND	
465	HTA7	O	502	GND		539	V_{DD}	
466	V_{DD}		503	V_{DD}		540	GND	
467	HTA0	O	504	GND		541	V_{DD}	
468	V_{DD}		505	V_{DD}		542	GND	
469	HTD30	I/O	506	GND		543	V_{DD}	
470	V_{DD}		507	V_{DD}		544	GND	
471	HTD25	I/O	508	GND		545	V_{DD}	
472	HTD22	I/O	509	V_{DD}		546	GND	
473	HTD19	I/O	510	GND		547	V_{DD}	
474	HTP1	I/O	511	V_{DD}		548	GND	
475	HTD12	I/O	512	GND		549	V_{DD}	
476	GND		513	V_{DD}		550	GND	
477	HTP0	I/O	514	GND		551	V_{DD}	
478	HTD3	I/O	515	V_{DD}		552	GND	
479	HTD1	I/O	516	GND		553	V_{DD}	
480	PU	I	517	V_{DD}		554	GND	

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Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O
555	V_{DD}		564	GND		573	V_{DD}	
556	GND		565	V_{DD}		574	GND	
557	V_{DD}		566	GND		575	V_{DD}	
558	GND		567	V_{DD}		576	GND	
559	V_{DD}		568	GND		577	V_{DD}	
560	GND		569	V_{DD}		578	GND	
561	V_{DD}		570	GND		579	V_{DD}	
562	GND		571	V_{DD}		580	GND	
563	V_{DD}		572	GND				

2.3 Pin Functions

Although the μPD98410 is a device operating at 3.3 V, it can be directly connected to a PHY device, CPU, and memory with a 5-V TTL interface.

2.3.1 Power supply

Pin Name	Pin No.	I/O	Function
V_{DD}	15, 23, 26, 32, 60, 74, 77, 83, 103, 111, 113, 118, 126, 130, 137, 139, 142, 152, 160, 167, 174, 177, 181, 186, 192, 199, 209, 233, 248, 271, 287, 293, 338, 339, 341, 371, 374, 384, 386, 388, 390, 410, 412, 414, 416, 438, 440, 442, 443, 444, 446, 464, 466, 468, 470, 481, 483, 485, 487, 489, 491, 493, 495, 497, 499, 501, 503, 505, 507, 509, 511, 513, 515, 517, 519, 521, 523, 525, 527, 529, 531, 533, 535, 537, 539, 541, 543, 545, 547, 549, 551, 553, 555, 557, 559, 561, 563, 565, 567, 569, 571, 573, 575, 577, 579	—	These pins supply a power of +3.3 V ± 5%.
GND	1, 2, 25, 33, 34, 35, 49, 65, 66, 67, 68, 75, 85, 86, 91, 99, 100, 101, 114, 116, 131, 132, 133, 138, 149, 164, 175, 191, 195, 226, 235, 237, 246, 258, 259, 273, 284, 286, 291, 292, 304, 306, 309, 316, 334, 347, 362, 370, 379, 382, 391, 396, 402, 408, 431, 436, 450, 453, 459, 476, 482, 484, 486, 488, 490, 492, 494, 496, 498, 500, 502, 504, 506, 508, 510, 512, 514, 516, 518, 520, 522, 524, 526, 528, 530, 532, 534, 536, 538, 540, 542, 544, 546, 548, 550, 552, 554, 556, 558, 560, 562, 564, 566, 568, 570, 572, 574, 576, 578, 580	—	These are ground pins.

2.3.2 UTOPIA interface

The μPD98410 employs a UTOPIA Level2 (cell level transfer) interface between PHY layer and ATM layer. Tables 2-1 and 2-2 lists the interface signals.

Table 2-1. Receive Interface Signals (1/2)

Symbol	Pin No.	I/O	Function
RXADDR03 - RXADDR00	434, 204, 323, 435	O	Multi-PHY select address of receive interface 0. RXADDR03 is the MSB.
RXDATA07 - RXDATA00	319, 200, 73, 320, 201, 432, 202, 321	I	Cell data input of receive interface 0. Cell data is input from a PHY layer device in byte units. The μPD98410 reads the data at the rising edge of UCLK0. RXDATA07 is the MSB.
RXSOC0	203	I	Cell transfer start signal of receive interface 0. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB0_B	322	O	Transfer enable signal of receive interface 0. This signal informs a PHY layer device that the μPD98410 is ready for reception in the next clock cycle.
RXCLAV0	76	I	Cell transfer enable signal of receive interface 0. This pin inputs a signal that indicates that no more cells will be supplied to the μPD98410 after the current cell has been transferred.
UCLK0	433	I	UTOPIA clock input of receive interface 0. Data is transferred/received in synchronization with the rising edge of this clock.
RXADDR13 - RXADDR10	277, 392, 154, 24	O	Multi-PHY select address of receive interface 1. RXADDR13 is the MSB.
RXDATA17 - RXDATA10	19, 387, 150, 272, 20, 151, 274, 21	I	Cell data input of receive interface 1. Cell data is input from a PHY layer device in byte units. The μPD98410 reads the data at the rising edge of UCLK1. RXDATA17 is the MSB.
RXSOC1	276	I	Cell transfer start signal of receive interface 1. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB1_B	22	O	Transfer enable signal of receive interface 1. This signal informs a PHY layer device that the μPD98410 is ready for reception in the next clock cycle.
RXCLAV1	153	I	Cell transfer enable signal of receive interface 1. This pin inputs a signal that indicates that no more cells will be supplied to the μPD98410 after the current cell has been transferred.
UCLK1	389	I	UTOPIA clock input of receive interface 1. Data is transferred/received in synchronization with the rising edge of this clock.

Table 2-1. Receive Interface Signals (2/2)

Symbol	Pin No.	I/O	Function
RXADDR23 - RXADDR20	214, 333, 88, 445	O	Multi-PHY select address of receive interface 2. RXADDR23 is the MSB.
RXDATA27 - RXDATA20	210, 82, 84, 329, 211, 441, 212, 330	I	Cell data input of receive interface 2. Cell data is input from a PHY layer device in byte units. The μPD98410 reads the data at the rising edge of UCLK2. RXDATA27 is the MSB.
RXSOC2	332	I	Cell transfer start signal of receive interface 2. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB2_B	213	O	Transfer enable signal of receive interface 2. This signal informs a PHY layer device that the μPD98410 is ready for reception in the next clock cycle.
RXCLAV2	87	I	Cell transfer enable signal of receive interface 2. This pin inputs a signal that indicates that no more cells will be supplied to the μPD98410 after the current cell has been transferred.
UCLK2	331	I	UTOPIA clock input of receive interface 2. Data is transferred/received in synchronization with the rising edge of this clock.
RXADDR33 - RXADDR30	143, 266, 12, 267	O	Multi-PHY select address of receive interface 3. RXADDR33 is the MSB.
RXDATA37 - RXDATA30	262, 8, 378, 140, 263, 9, 264, 141	I	Cell data input of receive interface 3. Cell data is input from a PHY layer device in byte units. The μPD98410 reads the data at the rising edge of UCLK3. RXDATA37 is the MSB.
RXSOC3	11	I	Cell transfer start signal of receive interface 3. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB3_B	265	O	Transfer enable signal of receive interface 3. This signal informs a PHY layer device that the μPD98410 is ready for reception in the next clock cycle.
RXCLAV3	381	I	Cell transfer enable signal of receive interface 3. This pin inputs a signal that indicates that no more cells will be supplied to the μPD98410 after the current cell has been transferred.
UCLK3	380	I	UTOPIA clock input of receive interface 3. Data is transferred/received in synchronization with the rising edge of this clock.

Table 2-2. Transmit Interface Signal (1/2)

Symbol	Pin No.	I/O	Function
TXADDR03 - TXADDR00	205, 324, 78, 325	O	Multi-PHY select address of transmit interface 0. TXADDR03 is the MSB.
TXDATA07 - TXDATA00	437, 207, 327, 80, 328, 208, 439, 81	O	Cell data output of transmit interface 0. Cell data is output to a PHY layer device in byte units. The μPD98410 outputs the data at the rising edge of UCLK0. TXDATA07 is the MSB. (3-state buffer)
TXSOC0	326	O	Cell transfer start signal of transmit interface 0. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)
TXENB0_B	79	O	Transfer enable signal of transmit interface 0. This signal informs a PHY layer device that the μPD98410 outputs data in the current clock cycle.
TXCLAV0	206	I	Cell transfer enable signal of transmit interface 0. This pin inputs a signal that indicates that the μPD98410 is ready to receive the next cell after transfer of the current cell is completed.
TXADDR13 - TXADDR10	278, 155, 393, 279	O	Multi-PHY select address of transmit interface 1. TXADDR13 is the MSB.
TXDATA17 - TXDATA10	157, 395, 27, 281, 158, 282, 28, 159	O	Cell data output of transmit interface 1. Cell data is output to a PHY layer device in byte units. The μPD98410 outputs the data at the rising edge of UCLK1. TXDATA17 is the MSB. (3-state buffer)
TXSOC1	394	O	Cell transfer start signal of transmit interface 1. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)
TXENB1_B	280	O	Transfer enable signal of transmit interface 1. This signal informs a PHY layer device that the μPD98410 outputs data in the current clock cycle.
TXCLAV1	156	I	Cell transfer enable signal of transmit interface 1. This pin inputs a signal that indicates that the μPD98410 is ready to receive the next cell after transfer of the current cell is completed.

Table 2-2. Transmit Interface Signal (2/2)

Symbol	Pin No.	I/O	Function
TXADDR23 - TXADDR20	215, 335, 89, 216	O	Multi-PHY select address of transmit interface 2. TXADDR23 is the MSB.
TXDATA27 - TXDATA20	447, 337, 218, 448, 92, 219, 449, 93	O	Cell data output of transmit interface 2. Cell data is output to a PHY layer device in byte units. The μPD98410 outputs the data at the rising edge of UCLK2. TXDATA27 is the MSB. (3-state buffer)
TXSOC2	336	O	Cell transfer start signal of transmit interface 2. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)
TXENB2_B	217	O	Transfer enable signal of transmit interface 2. This signal informs a PHY layer device that the μPD98410 outputs data in the current clock cycle.
TXCLAV2	90	I	Cell transfer enable signal of transmit interface 2. This pin inputs a signal that indicates that the μPD98410 is ready to receive the next cell after transfer of the current cell is completed.
TXADDR33 - TXADDR30	144, 268, 13, 383	O	Multi-PHY select address of transmit interface 3. TXADDR33 is the MSB.
TXDATA37 - TXDATA30	270, 146, 385, 148, 147, 16, 18, 17	O	Cell data output of transmit interface 3. Cell data is output to a PHY layer device in byte units. The μPD98410 outputs the data at the rising edge of UCLK3. TXDATA37 is the MSB. (3-state buffer)
TXSOC3	269	O	Cell transfer start signal of transmit interface 3. This signal is output to a PHY layer device in synchronization with the first byte of cell data. (3-state buffer)
TXENB3_B	14	O	Transfer enable signal of transmit interface 3. This signal informs a PHY layer device that the μPD98410 outputs data in the current clock cycle.
TXCLAV3	145	I	Cell transfer enable signal of transmit interface 3. This pin inputs a signal that indicates that the μPD98410 is ready to receive the next cell after transfer of the current cell is completed.

2.4 Memory Interface Signals

The μPD98410 has two types of memory interfaces. One of them is used to store a cell header translation table and an address pointer to the cell buffer to the HTT & control memory, and the other is used to store cell data to the cell buffer memory. Table 2-3 shows the interface signals of the HTT & control memory. Table 2-4 shows the interface signals of the cell buffer memory.

Table 2-3. HTT & Control Memory Interface Signals

Symbol	Pin No.	I/O	Function
HTA17 - HTA0	352, 462, 353, 110, 463, 236, 354, 355, 112, 356, 465, 238, 357, 239, 241, 358, 240, 467	O	Address output
HTD31 - HTD0	243, 469, 119, 244, 361, 120, 471, 245, 121, 472, 364, 122, 473, 365, 247, 123, 124, 366, 249, 475, 367, 125, 368, 250, 251, 369, 127, 252, 478, 128, 479, 253	I/O	Data I/O bus (32-bit/word units) (w/pull-down resistor)
HTP3 - HTP0	360, 363, 474, 477	I/O	Parity I/O (w/pull-down resistor)
HTCS1_B, HTCS0_B	115 117	O	Chip select signal
HTWE_B	359	O	Write enable signal
HTOE_B	242	O	Output enable signal

Table 2-4. Cell Buffer Memory Interface Signals

Symbol	Pin No.	I/O	Function
CBA17 - CBA0	48, 300, 178, 413, 50, 301, 180, 302, 52, 415, 53, 182, 303, 54, 417, 183, 305, 55	O	Address output
CBD87 - CBD0	397, 29, 283, 30, 398, 161, 399, 31, 285, 162, 163, 165, 400, 36, 166, 37, 401, 288, 38, 289, 168, 39, 290, 404, 40, 170, 405, 406, 171, 42, 172, 43, 407, 294, 173, 295, 44, 409, 45, 296, 297, 46, 298, 411, 418, 184, 56, 419, 307, 185, 57, 420, 58, 308, 187, 421, 422, 59, 310, 188, 423, 189, 311, 61, 190, 424, 312, 62, 425, 313, 63, 426, 64, 314, 193, 194, 315, 69, 196, 197, 70, 428, 317, 71, 429, 72, 318, 430	I/O	Data bus (88-bit/word units) (w/pull-down resistor)
CBCS1_B CBCS0_B	176 299	O	Chip select signal
CBWE_B	47	O	Write enable signal
CBOE_B	179	O	Output enable signal

2.4.1 Microprocessor interface signals

The μPD98410 supports the following two types of microprocessor interfaces:

(1) 32-bit address/data multiplexed synchronous bus

(2) 16-bit address/data separated asynchronous bus

The functions of some pins differ depending on the mode used.

Table 2-5. Microprocessor Interface

Symbol	Pin No.	I/O	Function
HSEL	340	I	Microprocessor interface select signal. The 32-bit multiplexed synchronous bus is selected if HSEL is low at hardware reset, and the 16-bit separated asynchronous bus is selected if HSEL is high.
IOCS_B	94	I	I/O chip select signal
MCS_B	221	I	Memory chip select signal
INT	451	O	Interrupt request signal

Table 2-6. 32-Bit Multiplexed Synchronous Interface

Symbol	Pin No.	I/O	Function
HCLK	220	I	Microprocessor bus clock (8 M to 33 MHz)
AD31 - AD0	223, 342, 343, 224, 225, 344, 227, 454, 345, 228, 455, 229, 346, 104, 456, 230, 457, 105, 348, 231, 458, 106, 349, 232, 350, 107, 460, 351, 108, 234, 109, 461	I/O	Address/data bus
R/W_B	222	I	Read/write select signal
UWE_B	452	I	High-order word enable signal
RDY_B	95	O	Ready signal (3-state buffer)

Table 2-7. 16-Bit Separated Asynchronous Interface

Symbol	Pin No.	I/O	Function
HCLK	220	I	Connect this pin to GND or pull it up to V_{DD}.
A15	223	I	Connect this pin to GND or pull it up to V_{DD}.
A14 - A0	342, 343, 224, 225, 344, 227, 454, 345, 228, 455, 229, 346, 104, 456, 230	I	Address input
D15 - D0	457, 105, 348, 231, 458, 106, 349, 232, 350, 107, 460, 351, 108, 234, 109, 461	I/O	Data bus
WR_B	222	I	Write strobe signal
RD_B	452	I	Read strobe signal
RDY_B, RDY	95	O	Ready signal (3-state buffer)

2.4.2 JTAG

Table 2-8. JTAG Interface Signals

Symbol	Pin No.	I/O	Function
JDI	260	I	JTAG serial data input
JDO	376	O	JTAG serial data output (normally open) (3-state buffer)
JCK	261	I	JTAG serial clock input
JMS	377	I	JTAG mode select signal
JRST_B	7	I	JTAG reset signal

2.4.3 Others

Table 2-9. Other Interface Signals

Symbol	Pin No.	I/O	Function
SWCLK	129	I	System clock input (8 M to 33 MHz)
RESET_B	254	I	Hardware reset signal (Schmitt input buffer)
CG	5, 96, 97, 134, 135, 375	I	Always connected to GND.
PU	480	I	Always pulled up to V_{DD}.
IC	3, 4, 6, 10, 41, 98, 102, 136, 169, 198, 255, 256, 257, 275, 372, 373, 403, 427	O	Internally connected (always open).

2.5 Recommended Connections of Unused Pins

Table 2-10. Recommended Connections of Unused Pins

Pin Name	I/O	Recommended Connections
RXDATA07 - RXDATA00 RXDATA17 - RXDATA10 RXDATA27 - RXDATA20 RXDATA37 - RXDATA30	I	Connect to GND.
RXSOC3 - RXSOC0	I	Connect to GND.
RXCLAV3 - RXCLAV0	I	Connect to GND.
UCLK3 - UCLK0	I	Connect to GND.
TXCLAV3 - TXCLAV0	I	Connect to GND.
HTD31 - HTD0	I/O (w/pull-down resistor)	Open
HTP3 - HTP0	I/O (w/pull-down resistor)	Open
CBD87 - CBD0	I/O (w/pull-down resistor)	Open
HSEL	I	Connected to GND when 32-bit multiplexed synchronous bus is used. Pulled up to V_{DD} when 16-bit separated asynchronous bus is used.
HCLK	I	Pulled up to V_{DD} or connected to GND
IOCS_B	I	Pulled up to V_{DD}
MCS_B	I	Pulled up to V_{DD}
AD31 - AD0	I/O	Pulled up to V_{DD}
A15 - A0	I	Connect to GND.
D15 - D0	I/O	Pulled up to V_{DD}
R/W_B, WR_B	I	Pulled up to V_{DD}
UWE_B, RD_B	I	Pulled up to V_{DD}
JDI	I	Connect to GND.
JCK	I	Connect to GND.
JMS	I	Connect to GND.
JRST_B	I	Connect to GND.
All output pins	O	Open

2.6 Pin Status at Reset

Table 2-11. Pin Status at Reset

Pin Name	I/O	Pin Status at Reset
RXADDR03 - RXADDR00 RXADDR13 - RXADDR10 RXADDR23 - RXADDR20 RXADDR33 - RXADDR30	O	High level
RXENB3_B - RXENB0_B	O	High level
TXADDR03 - TXADDR00 TXADDR13 - TXADDR10 TXADDR23 - TXADDR20 TXADDR33 - TXADDR30	O	High level
TXDATA07 - TXDATA00 TXDATA17 - TXDATA10 TXDATA27 - TXDATA20 TXDATA37 - TXDATA30	O (3-state buffer)	Hi-Z
TXSOC3 - TXSOC0	O (3-state buffer)	Hi-Z
TXENB3_B - TXENB0_B	O	High level
HTA17 - HTA0	O	Low level
HTCS1_B, HTCS0_B	O	High level
HTWE_B	O	High level
HTOE_B	O	High level
HTP3 - HTP0	I/O (w/pull-down resistor)	Low level
HTD31 - HTD0	I/O (w/pull-down resistor)	Low level
CBD87 - CBD0	I/O (w/pull-down resistor)	Low level
CBA17 - CBA0	O	Low level
CBOE_B	O	High level
CBWE_B	O	High level
CBCS1_B, CBCS0_B	O	High level
INT	O	Low level
RDY	O (3-state buffer)	Hi-Z
AD31 - AD0	I/O	Hi-Z
D15 - D0	I/O	Hi-Z
JDO	O (3-state buffer)	Hi-Z

CHAPTER 3 FUNCTIONAL OUTLINE

The μPD98410 is a shared-buffer non-blocking ATM switch which has a header translation function. Its circuit interfaces conform to UTOPIA Level2 and can connect up to 24 circuits of different rates by connecting multiple PHY devices. A header translation table is stored in external SRAM. By referencing this table, the μPD98410 can simultaneously translate headers of up to 64K connections (at the full memory capacity) during switching. The external SRAM is also used as a shared buffer to which up to 51.2K cells (at full memory capacity) can be stored.

The μPD98410 also controls transfer quality by using EPD (Early Packet Discard), PPD (Partial Packet Discard), priority cell discard control, and ABR (Available Bit Rate) traffic control features.

3.1 UTOPIA Interfaces

The μPD98410 has four UTOPIA interfaces conforming to UTOPIA Level2. These interfaces support single ATM-multi-PHY, 8-bit data width, and cell level handshaking. Octet level handshaking is not supported.

The μPD98410 supports multiple PHY device connection, and can connect up to 24 PHY devices. One UTOPIA interface can connect up to 12 PHY devices, but the total transfer rate of the PHY devices must be kept to within 314M bps (at UTOPIA clock rate = 40 MHz).

The PHY devices connected to the UTOPIA interface are mapped to logical port numbers by the UTOPIA interface number and PHY address, in accordance with the contents of the port configuration register. The μPD98410 performs its internal processing by using these logical port numbers.

The relationship between the maximum transfer rate of one UTOPIA interface and UTOPIA clock rate is shown below. The μPD98410 realizes a total throughput of 1.2G bps at a UTOPIA clock rate of 40 MHz.

Table 3-1. Maximum Transfer Rate and UTOPIA Clock Rate

UTOPIA Level 2 (8-bit)	UTOPIA Clock Rate (Hz)	UTOPIA Throughput MAX. (bps)	Total Throughput MAX. (bps)
Enhanced	40 M	314 M	1.256 G
Standard	33 M	259 M	1.036 G
	20 M	157 M	628 G

The maximum transfer rate of one UTOPIA interface can be calculated with the following expression. One cell (53 octets) is processed in the basic timing (54 UTOPIA clocks) of the UTOPIA interface.

UTOPIA throughput [Mbps] = UTOPIA clock rate [MHz] × 8 [bits] × 53/54

Caution Make sure that the following relationship between the UTOPIA clock frequency and system clock frequency is satisfied.

System clock frequency ≥ 33/40 × UTOPIA clock frequency

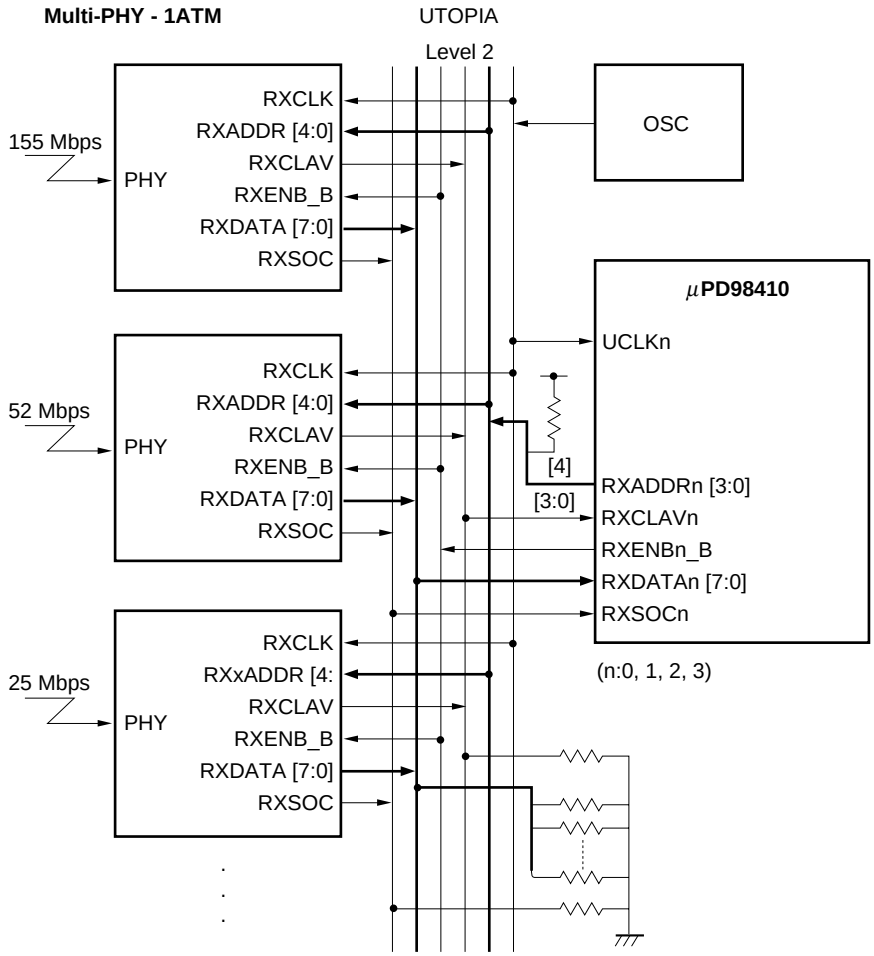
3.1.1 Input port interface

The μPD98410 has four UTOPIA interfaces and supports multiple PHY device connection allowing up to 24 input ports. Up to 12 ports can be connected to each UTOPIA interface.

An input port is mapped to a logical input port number based on the PHY address and UTOPIA interface number, in accordance with the contents of the port configuration register. The μPD98410 performs its internal processing by using this logical input port number.

Figure 3-1 shows an example of connecting multiple PHY devices to one UTOPIA interface.

Figure 3-1. Example of Connecting UTOPIA Receive Interface



Remark Of the 5 bits of a PHY address, the low-order 4 bits are connected to the μPD98410. Pull up the highest bit. The μPD98410 outputs a PHY address of "0" through "11" for the purpose of polling.
The μPD98410 does not have an RXCLK output. Supply UCLKn to the μPD98410 as a UTOPIA clock.

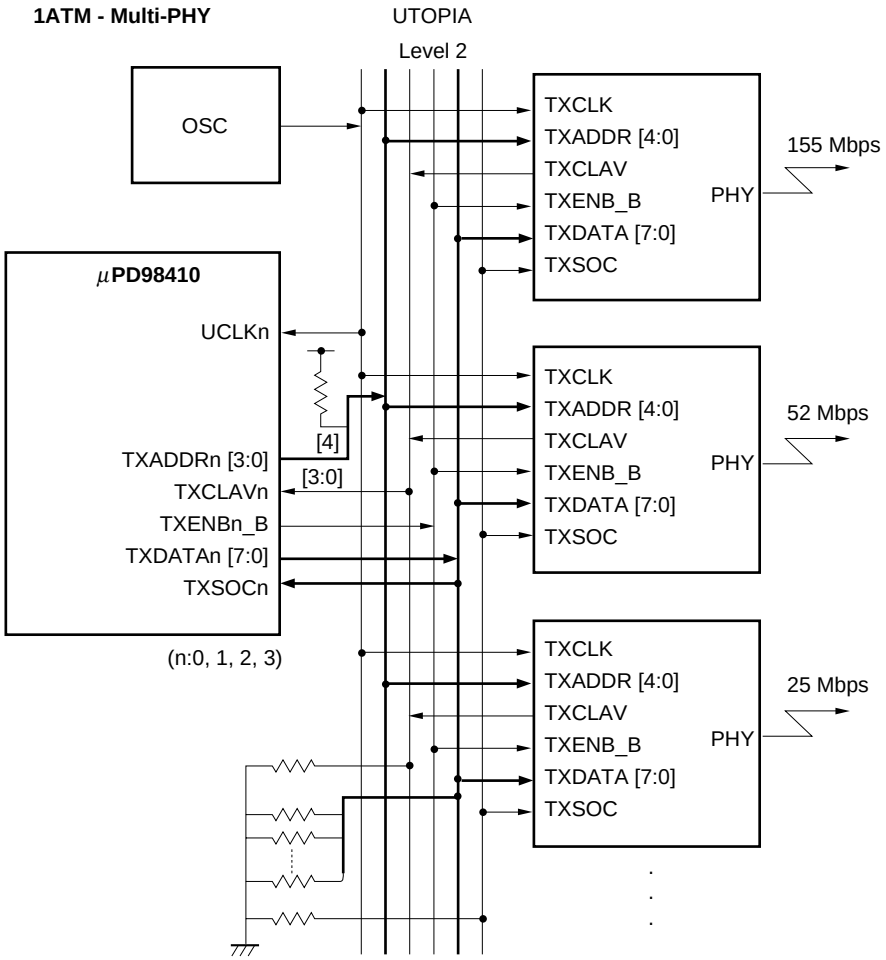
3.1.2 Output port interface

The μPD98410 has four UTOPIA interfaces and supports multiple PHY device connection allowing up to 24 output ports. Up to 12 output ports can be connected to each UTOPIA interface.

An output port is mapped to a logical output port number based on the PHY address and UTOPIA interface number, in accordance with the contents of the port configuration register. The μPD98410 performs its internal processing by using this logical output port number.

Figure 3-2 shows an example of connecting multiple PHY devices to one UTOPIA interface.

Figure 3-2. Example of Connecting UTOPIA Transmit Interface



Remark Of the 5 bits of a PHY address, the low-order 4 bits are connected to the μPD98410. Pull up the highest bit. The μPD98410 outputs a PHY address of "0" through "11" for the purpose of polling.
The μPD98410 does not have a TXCLK output. Supply UCLKn to the μPD98410 as a UTOPIA clock.

3.2 Polling

Cells are input to the μPD98410 in the following sequence:

<1> The μPD98410 inquires whether a PHY device has a cell (polling).
<2> If the device has a cell, the μPD98410 inputs the cell. If not, the μPD98410 makes an inquiry to the next PHY device of those that are mapped to the logical port by the port configuration register.

Cells are output from the output queue in the following sequence:

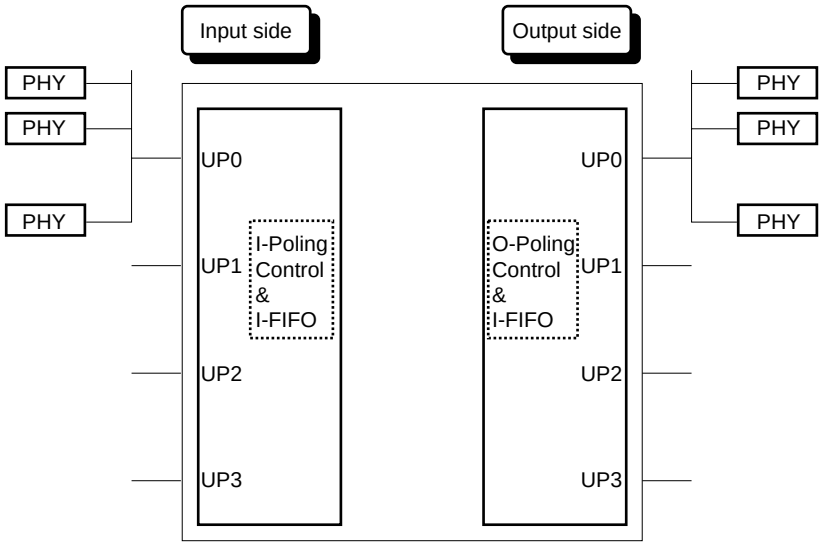
<1> The μPD98410 inquires whether each PHY device is ready to receive a cell (polling).
<2> Based on output rate control (shaping), cell stop information, and the result of polling in <1>, the μPD98410 determines from which output port to output a cell.
<3> Of the output queues corresponding to the logical output port determined, the μPD98410 determines the service class of the queue used to output the cell (WFQ (Weighted Fairness Queue)).

The way in which polling is used to input or output cells is explained below.

3.2.1 Outline of polling

Figure 3-3 shows the related functional blocks of the μPD98410.

Figure 3-3. Functional Blocks of μPD98410



- UP0-UP3 : UTOPIA interface ports
- I/O-Polling Control : Polling control block for input and output sides
- I/O-FIFO : Input or output FIFO. A FIFO exists for each UTOPIA port and corresponds to UP0 to UP3.

Basically, cells are input or output as follows:

(Input)

- The polling control block inquires whether each PHY device is ready to transmit a cell, and determines the logical input port that inputs the cell.
- The cell is input to the I-FIFO.

(Output)

- The polling control block inquires whether each PHY device is ready to receive a cell.
- The output cell is determined based on the result of polling, shaping, and WFQ, and is stored to the O-FIFO.
- The cell is transmitted to the corresponding logical output port.

Up to 12 PHY devices (PHY addresses 0 through 11) can be connected to one UTOPIA port.

Only the PHY address mapped to a logical port by PHY, UPN, and EN of the port configuration register are polled for input.

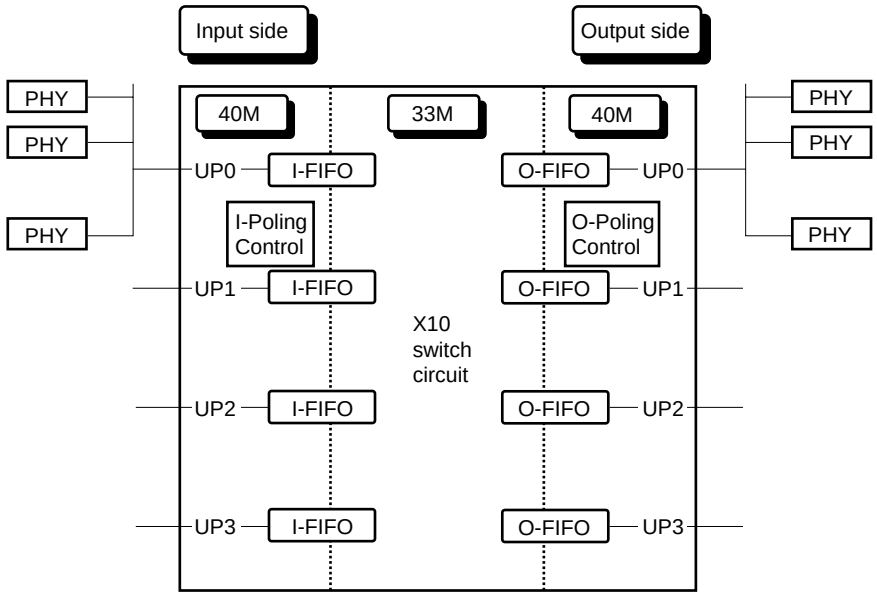
All the mapped PHY addresses (0 through 11) are polled for output.

The UTOPIA clock of UTOPIA ports UP0 through UP3 that conform to UTOPIA Level2 can be set to any rate, as long as the condition to be described later is satisfied (the UTOPIA clock rate is assumed to be 40 MHz here). Similarly, the system clock of the internal switch circuit of the μPD98410 can be also set to any rate as long as the condition to be described later is satisfied (the system clock is assumed to be 33 MHz here). The internal switch circuit uses 44 system clocks for one basic processing cycle, while a PHY device operates with 54 UTOPIA clocks. Therefore, the following difference in real time takes place between the internal switch circuit and polling control block.

	Clock Rate (Hz)	Basic Operation Cycle	Real Time of Cycle (ns)
Internal circuit	33 M	44 clocks	1320
PHY	40 M	54 clocks	1350

To make up this difference, the μPD98410 has I/O FIFOs.

Figure 3-4. Clock Relation



Caution The following relationship between the UTOPIA clock frequency and system clock frequency must be satisfied.

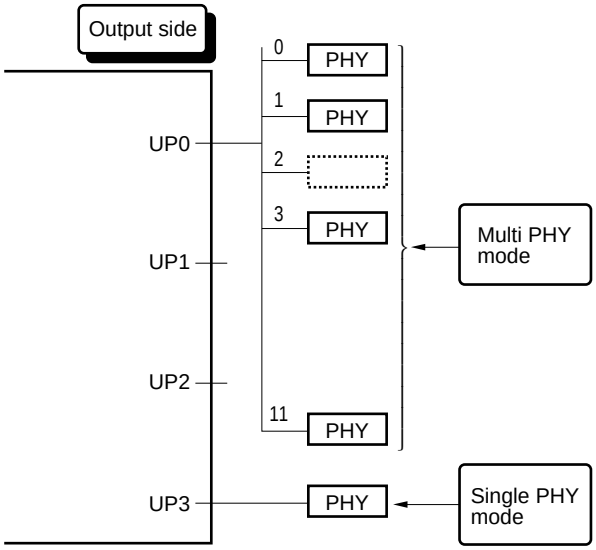
System clock frequency ≥ 33/40 × UTOPIA clock frequency

Unless this relationship is satisfied, the internal receive FIFO of the μPD98410 overruns. As a result, some cells are lost (cell loss occurs).

3.2.2 Polling during cell output

Depending on how the PHY device(s) is connected, the multi-PHY mode or single PHY mode is used.

Figure 3-5. Single PHY Mode and Multi-PHY Mode



Each mode is explained below.

<1> Multi-PHY mode

In this mode, two or more PHY devices can be connected to one UTOPIA output port. It is also possible to connect only one PHY device in this mode. Even if only one PHY device is connected, the operation in this mode is different from that in the single PHY mode.

<2> Single PHY mode

In this mode, one PHY device is connected to one UTOPIA output port.

Either multi-PHY mode or single PHY mode can be specified for each logical output port by using the SG bit of the port configuration register. In the single PHY mode, one PHY device is connected to one UTOPIA port. If two or more PHY devices are connected, the lowest logical output port number is selected.

If one UTOPIA output port is set in both the multi-PHY mode and single PHY mode, the single PHY mode takes precedence.

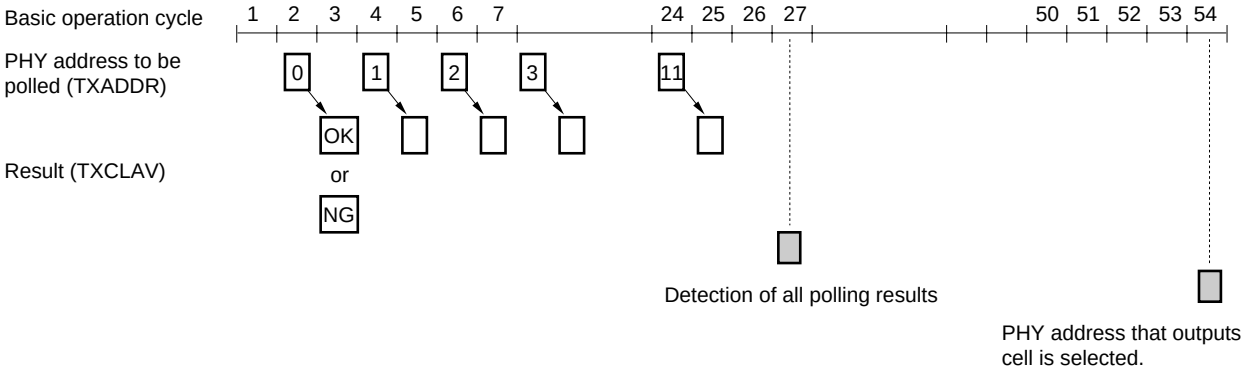
Cautions 1. If the setting of the SG bit of the port configuration register is changed while the μPD98410 is operating, two cells may be output to an illegal PHY device, or cell loss may occur because the result of polling does not match immediately before and after the mode is changed between single PHY and multi-PHY mode. After that, however, transmission is performed normally.

2. If mapping to the logical output port is changed by changing the setting of PHY, UPN, and EN of the port configuration register while the μPD98410 is operating, two cells may be output to an illegal PHY device, or cell loss may occur because the result of polling does not match immediately before and after the mode is changed between single PHY and multi-PHY mode. After that, however, transmission is performed normally.

(1) Polling in multi-PHY mode

The relationship between polling control and the basic operation cycle is shown below.

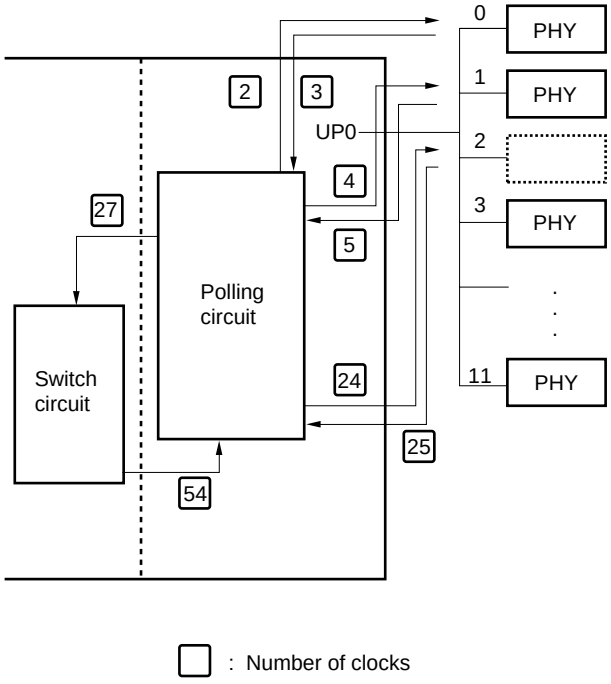
Figure 3-6. Relationship between Polling Control and Basic Operation Cycle (in multi-PHY mode)



<Basic operation>

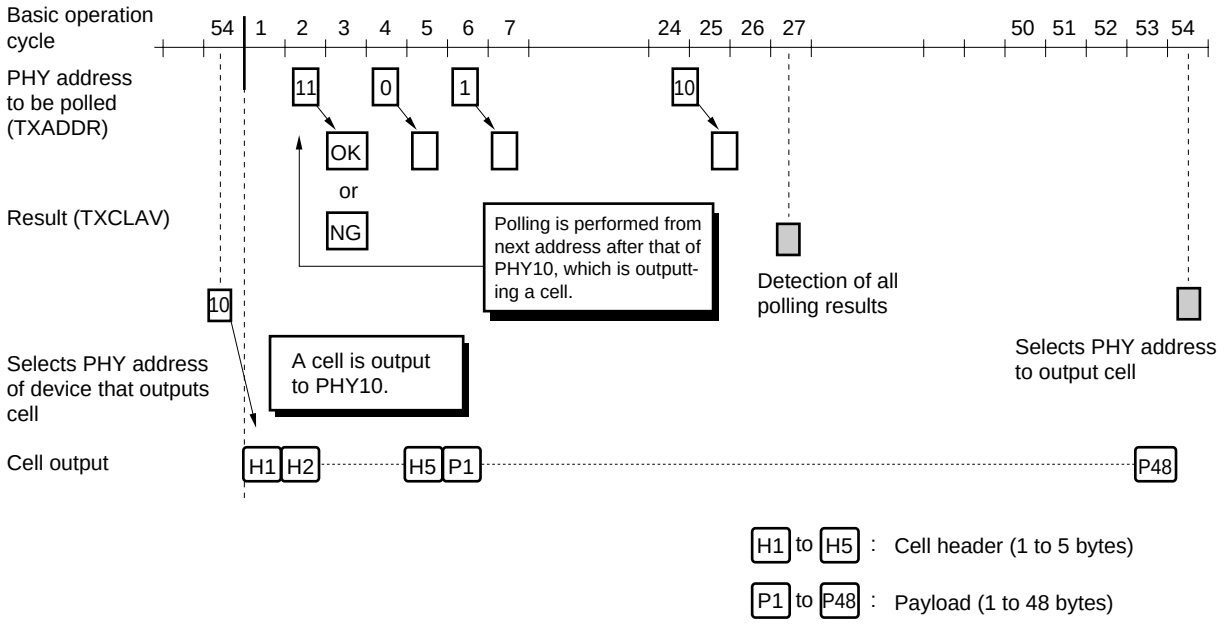
- Polling is performed starting from the second clock in the basic operation cycle.
- Inquires are made sequentially, starting from PHY address 0 (2nd, 4th, 6th, ... clock), and the result of the inquiry is returned at the next clock (3rd, 5th, 7th ... clock).
- The result of polling all the PHY devices is passed to the switch circuit at the 27th clock.
- The PHY device that outputs a cell is selected at the 54th clock (if no PHY device has a cell to output, nothing is selected).

Figure 3-7. Polling Operation during Cell Output



The μPD98410 outputs a cell to the PHY device that is selected at the 54th clock in the basic operation cycle (polling and cell output are performed in parallel). At this time, polling is started from the next PHY address after the PHY device that is currently transferring a cell.

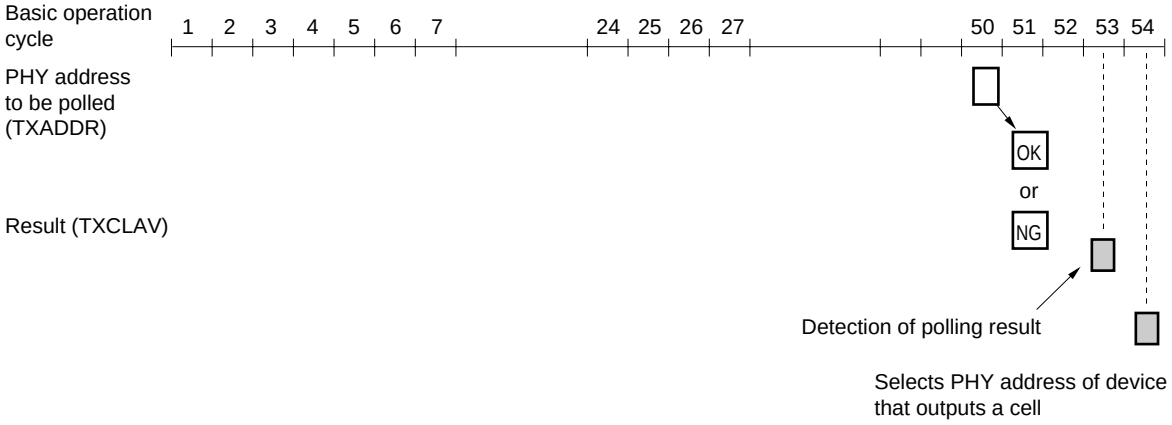
Figure 3-8. Polling Operation during Cell Output



(2) Polling in single PHY mode

The relationship between polling control and the basic operation cycle is illustrated below.

Figure 3-9. Relationship between Polling Control and Basic Operation Cycle (single PHY mode)



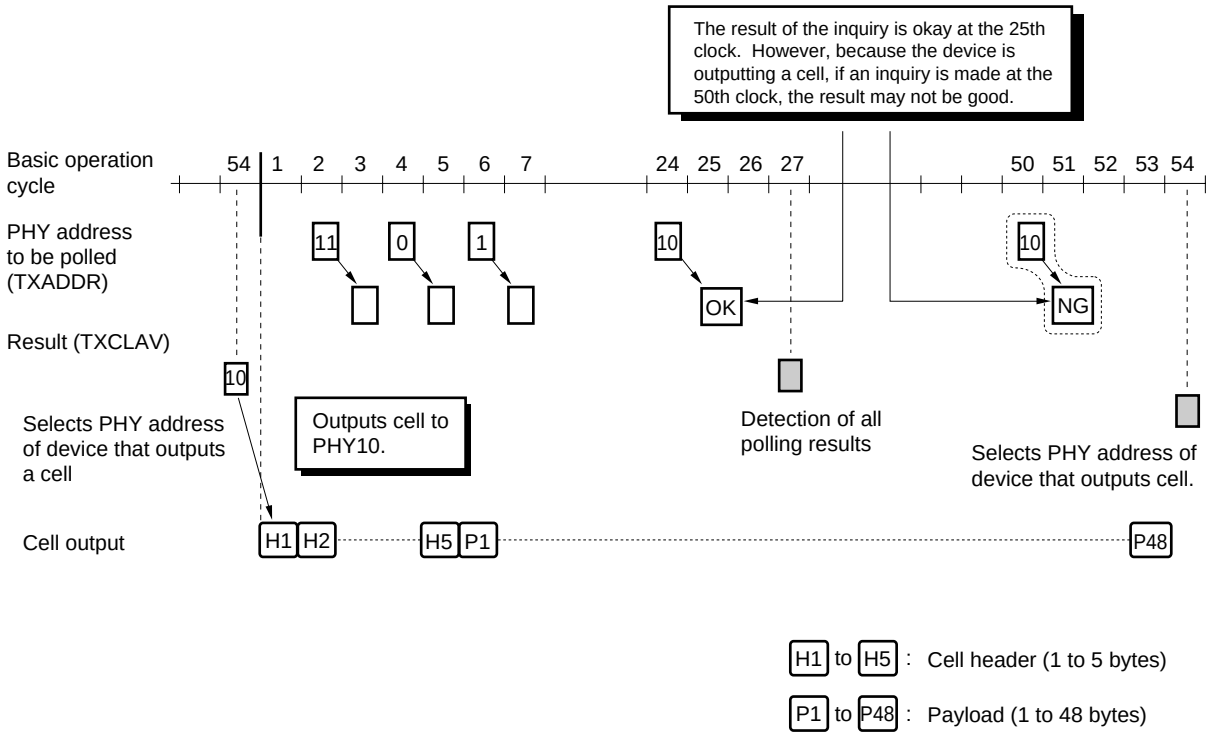
<Basic operation>

- In the single PHY mode, the PHY address connected is already known. Therefore, an inquiry is made to this PHY address at the 50th clock.
- The PHY device returns the result at the 51st clock.
- The result is passed to the switch circuit at the 53rd clock.
- If the result at the 51st clock is OK, the PHY address is selected at the 54th clock. If the result is NG, the PHY address is not selected. Even if the result at the 51st clock is OK, the PHY address is not selected if there is no cell to be output.

(3) Control of successive output

UTOPIA Level2 stipulates that an inquiry is made at the 50th clock or onward to determine whether a cell can be output to a PHY device that is outputting a cell. However, the μPD98410 makes this inquiry between the second and the 25th clock in the multi-PHY mode, and passes the result to the internal switch circuit at the 27th clock. Consequently, the result of the inquiry may be illegal in the case shown in Figure 3-10.

Figure 3-10. Control of Successive Output



In other words, because the value detected at the 27th clock (the result of polling the PHY device that is outputting a cell) is not stipulated by UTOPIA Level2, the PHY device connected to a logical output port of the μPD98410, depending on its specifications, may return the result one cycle before and this result may be different from the real result. In this case, if cells are successively output to PHY10, a problem such as lost cells, may occur.

To prevent such a problem, the μPD98410 controls successive output by using the PR bit.

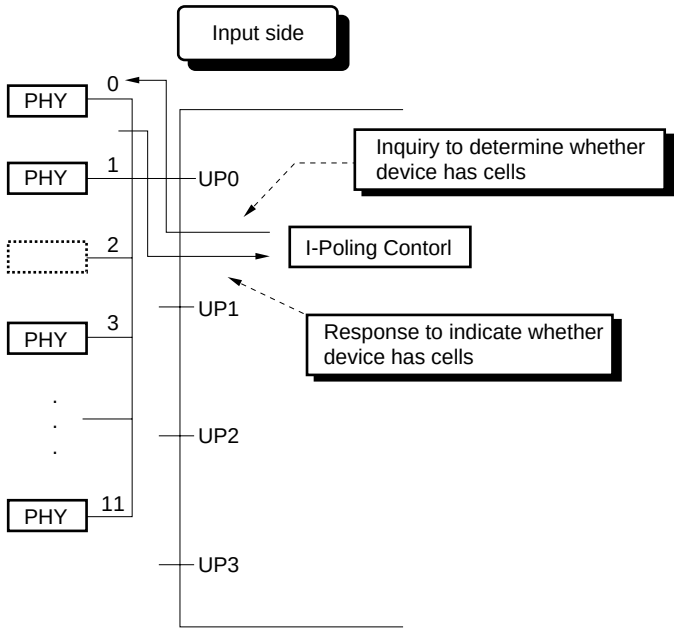
- RP = 0 → Does not permit successive output of cells to the same PHY device.
- RP = 1 → Permits successive output of cells to the same PHY device.

To output cells successively, the validity of the result detected at the 27th clock must be guaranteed. NEC's 155M-bps PHY μPD98404 (P30) satisfies this requirement and cells can be successively output to this device. To connect a PHY device from another maker, reset PR to 0 (not to permit successive output).

3.2.3 Polling during cell input

(1) Basic operation

Figure 3-11. Basic Operation of Polling during Cell Input

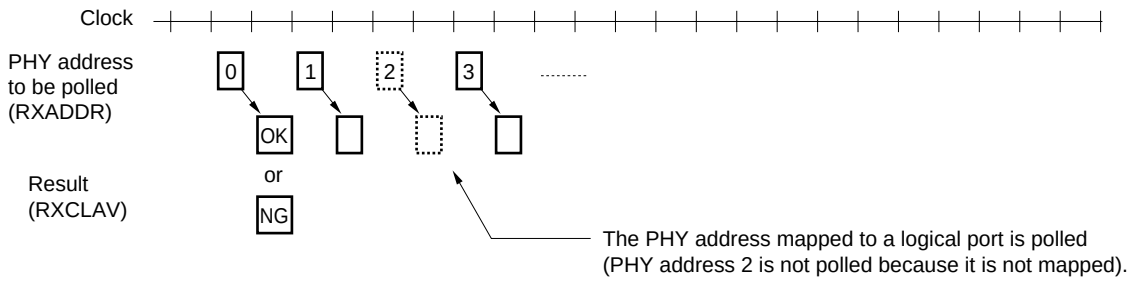


Cells are input to the μPD98410 in the following sequence:

<1> The μPD98410 inquires whether a PHY device has cells.
<2> The PHY device returns a response to indicate whether the device has cells.

This sequence is performed for a PHY device mapped to a logical port by PHY, UPN, and EN of the port configuration register. Figure 3-12 shows the relationship between the clock and polling control at this time. Polling control at the input side has no relationship with the basic operation cycle (= 54 UTOPIA clocks) units.

Figure 3-12. Relationship between Polling Control and Basic Operation Cycle (during cell input)

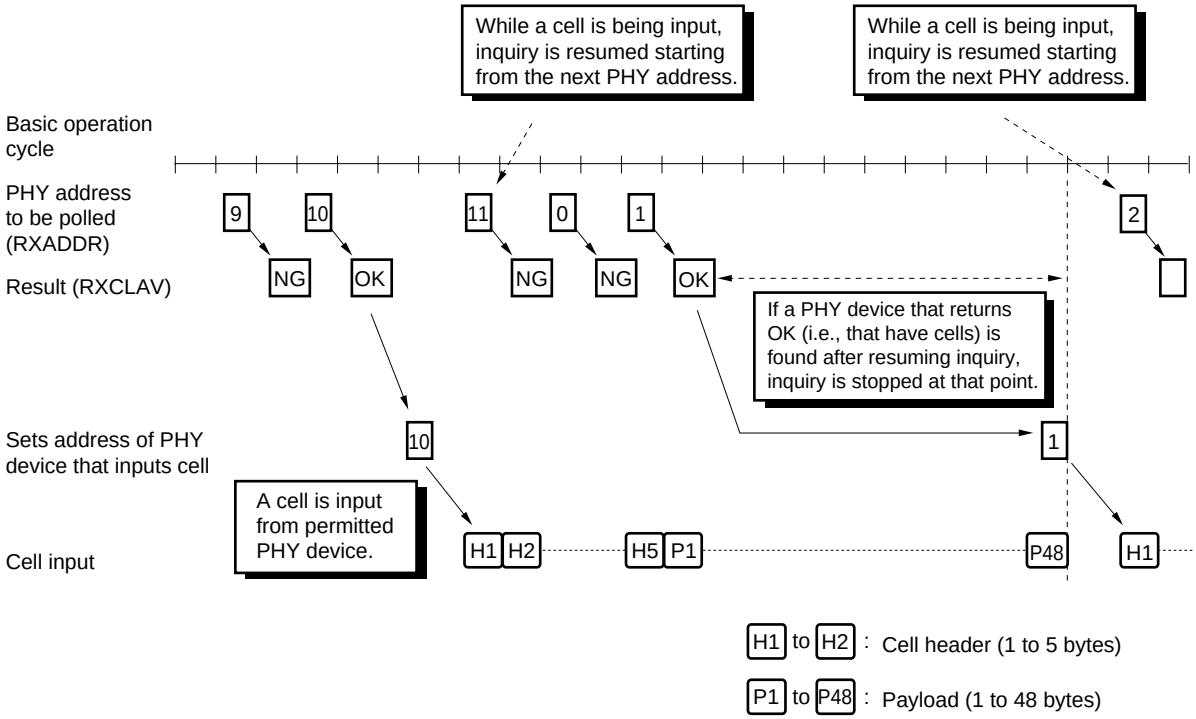


Caution Never map a PHY device that is not connected to a logical port. Otherwise, the input side polls a PHY device that does not exist, resulting in a hang up of the corresponding UTOPIA receive interface port.

(2) Cell input timing

If the result of polling is okay (i.e., if the device has cells), the cells are input as follows:

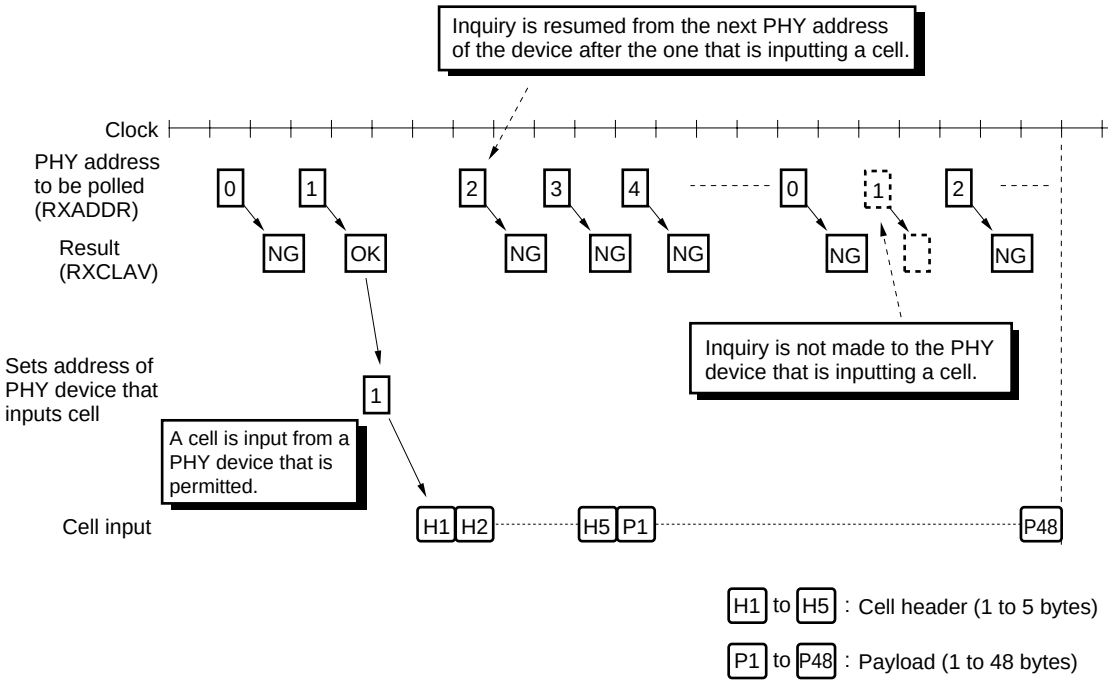
Figure 3-13. Basic Cell Input Timing 1



<Operation>

- If a PHY device returns OK in response to the inquiry, that PHY device is selected at the next clock.
- A cell is input from the selected PHY device at the clock after next.
- Inquiry is resumed at the input timing of H1. At this time, the PHY address is that of the next PHY device after the one that is inputting a cell.
- An inquiry is not made to a PHY device that is not mapped to a logical port. Nor is one made to a PHY device that is inputting a cell.
- If another PHY device that returns OK in response to the inquiry is found while one PHY device is inputting a cell, the inquiry is stopped at that point.
- The PHY device that is to input a cell next is selected at the input timing of P48.
- Inquiry is resumed from the input timing of H1. The PHY address at this time is that of the next PHY device after the one that is inputting a cell.

Figure 3-14. Basic Cell Input Timing 2



(3) Control of successive input

If the same PHY device successively input cells to the μPD98410, the μPD98410 does not make an inquiry to the PHY device that is inputting the cells. As a result, the interval between inputting a cell and inputting the next cell is widened as shown in Figure 3-15, reducing the transfer rate. For this reason, the μPD98410 permits the PHY device that has been inputting cells to continue inputting if the PHY device that is to input a cell next is not determined until the clock of P48 is input.

Figure 3-15. Drop in Transfer Rate during Successive Input

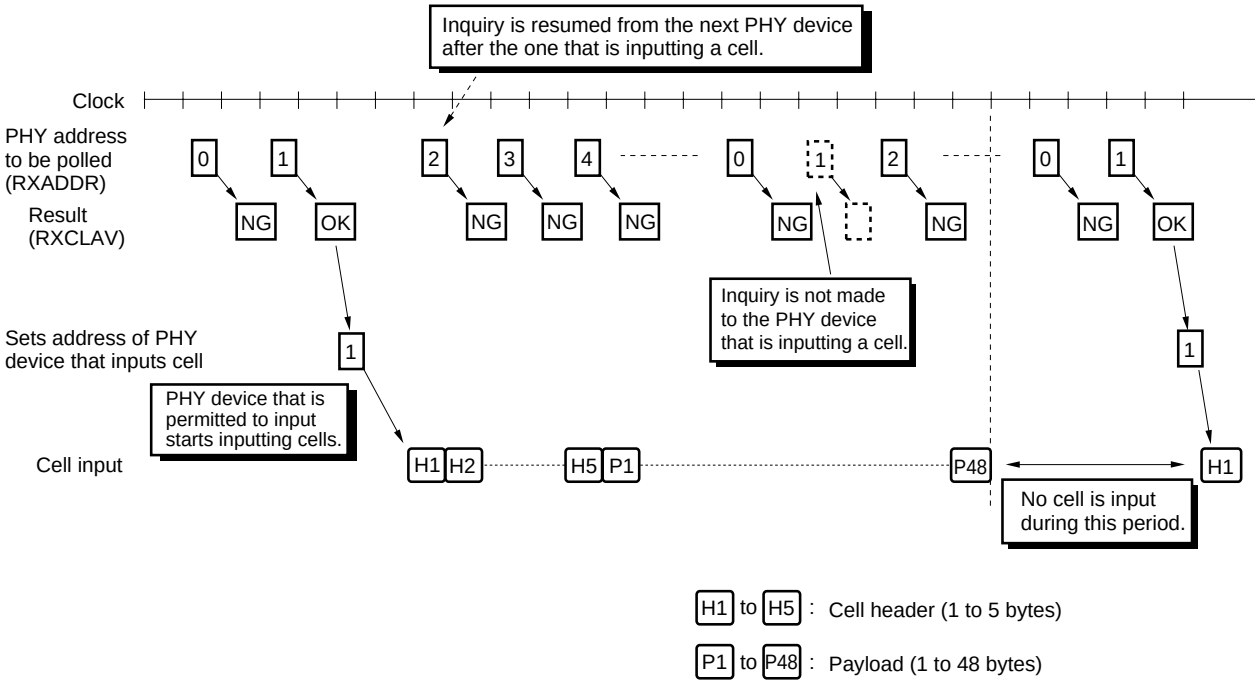
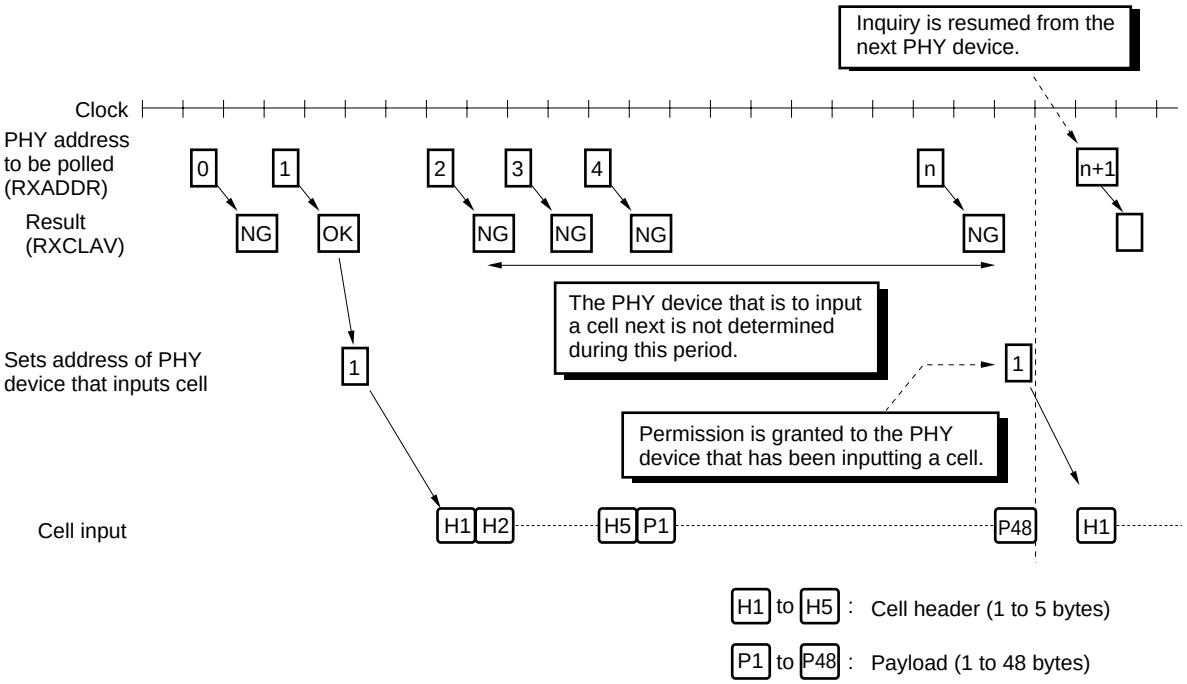
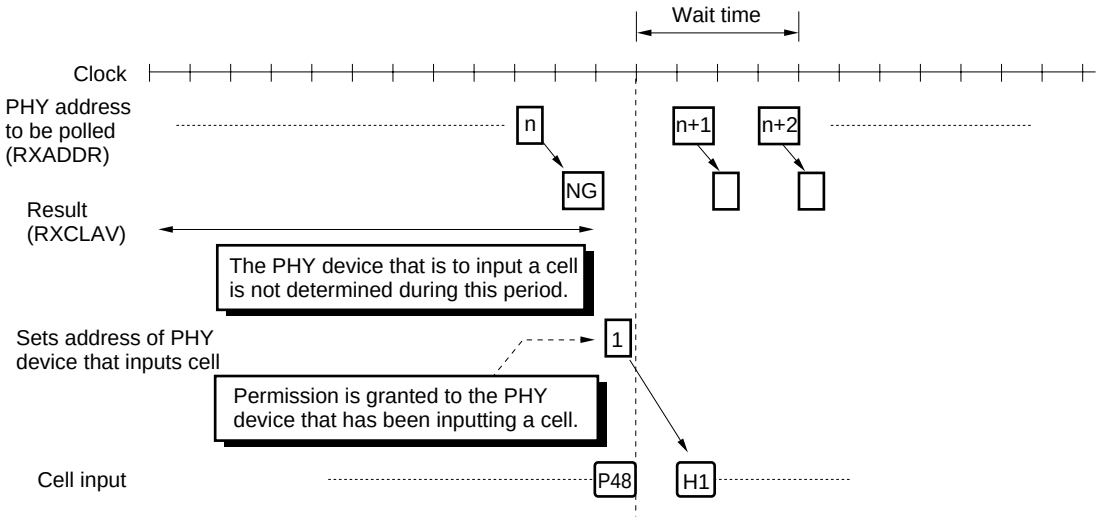


Figure 3-16. Control of Successive Input



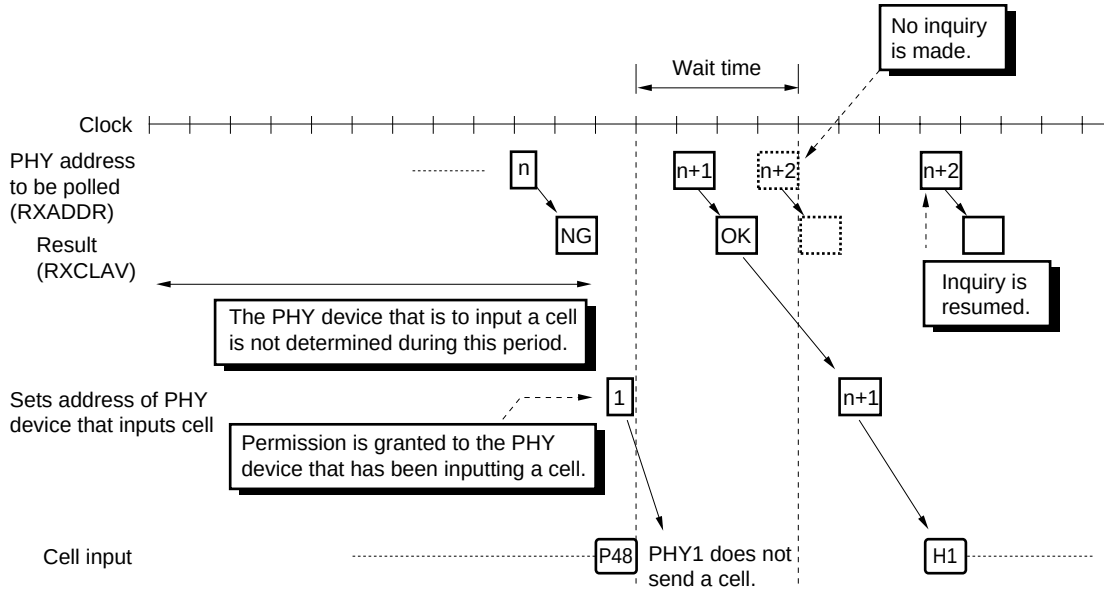
In this way, cells can be successively input even in the case in Figure 3-16, and a drop in the transfer rate can be prevented. At this time, even if permission to input a cell is granted to the PHY device that has been inputting a cell, there is a possibility that this PHY device has no more cells. Therefore, the μPD98410 is designed to wait for a time of 4 clocks. The operations to be performed when the μPD98410 waits are illustrated below.

(a) If cell is input during wait time

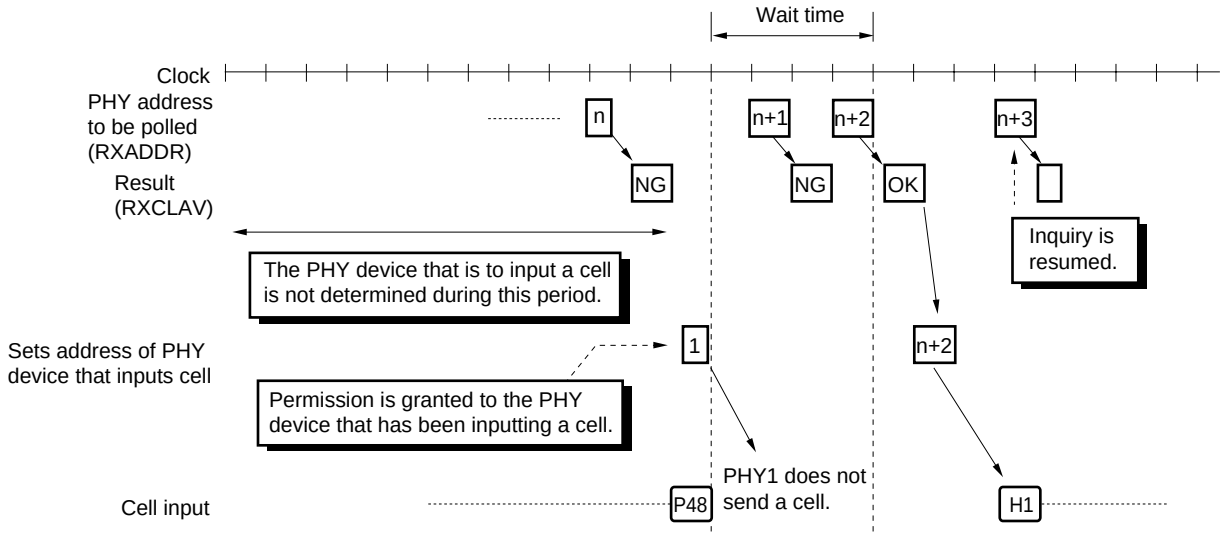


(b) If cell is not input during wait time

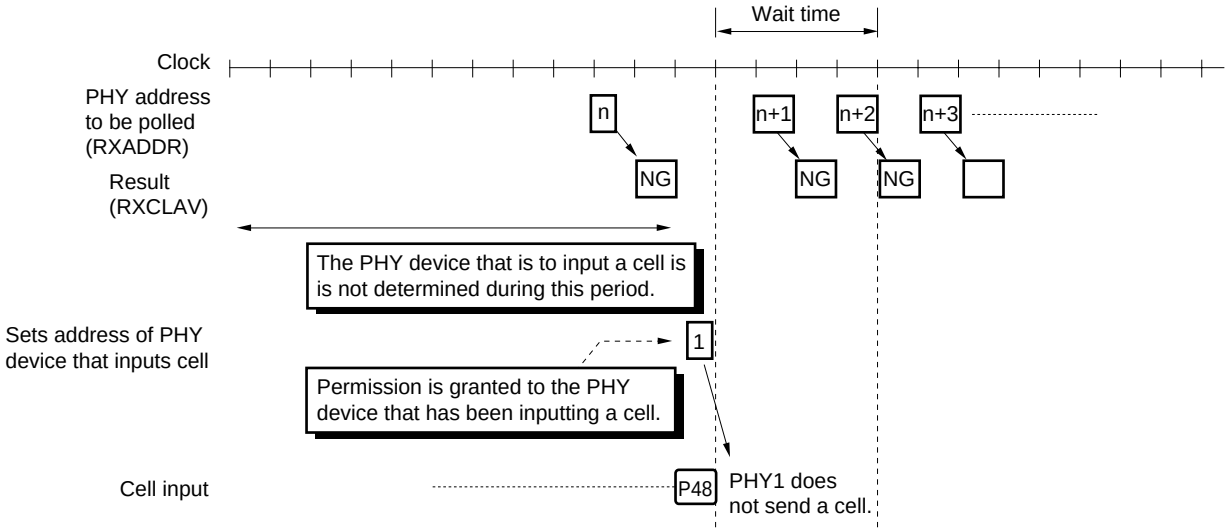
(i) If the result of polling PHY address n + 1 is OK



(ii) If the result of polling PHY address n + 2 is OK



(iii) If result of polling PHY addresses n + 1 and n + 2 is not OK



3.3 Header Translation

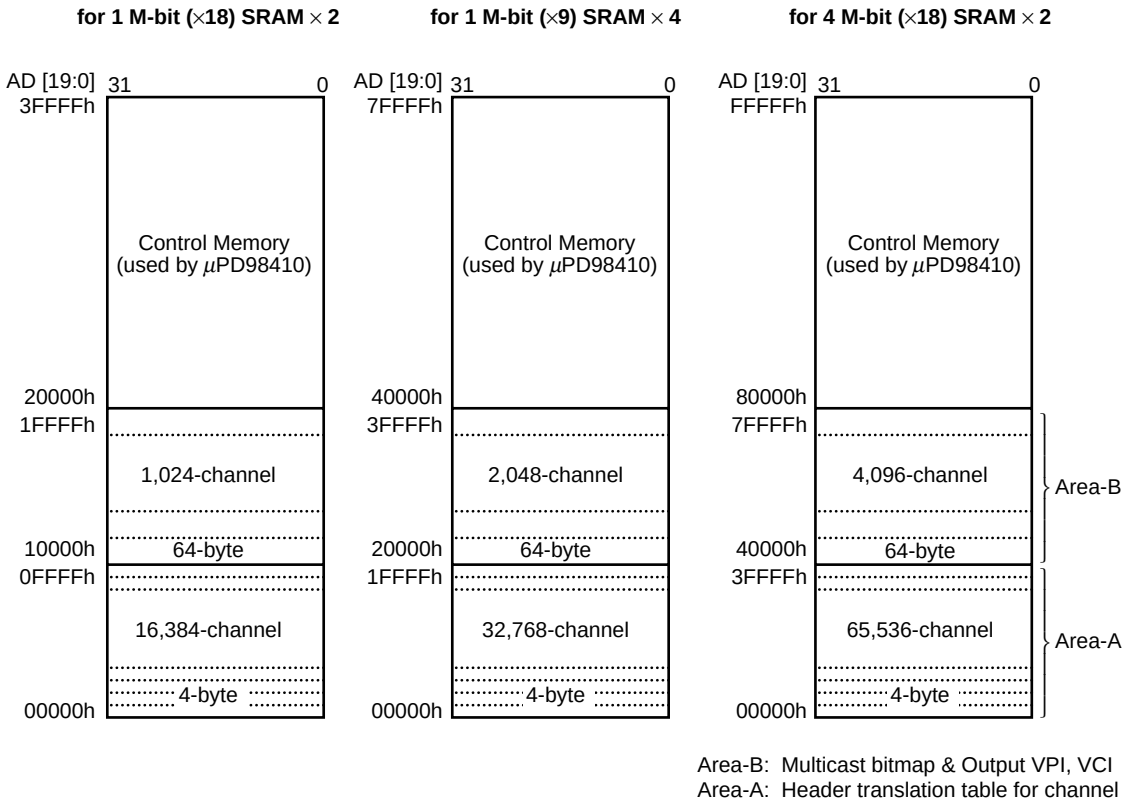
The μPD98410 translates headers in accordance with the header translation table (HTT) created in the external SRAM. Headers are translated when a cell is input in the single-cast mode, and when a cell is input or output in the multi-cast mode. The HTT is created by an external microprocessor when connection is made.

The format of the HTT and header translation procedure are explained below.

3.3.1 HTT (Header Translation Table) memory map

The HTT (Header Translation Table) is located in the HTT & control memory as Area-A and Area-B. The following three types of memories can be connected to the μPD98410 as the HTT & control memory.

Figure 3-17. HTT & Control Memory Map



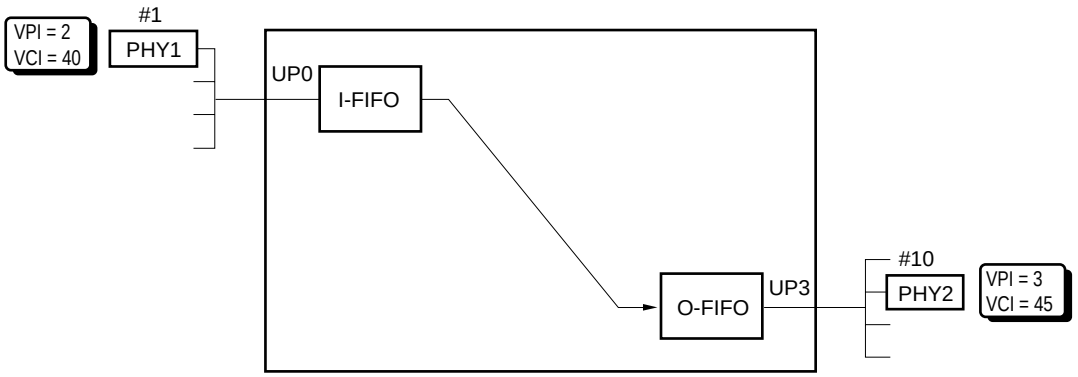
Remarks 1. The addresses shown in this figure are those accessed by the microprocessor.

2. The μPD98410 divides address AD[19:0] from the microprocessor by four and access the HTT & control memory in word units where one word consists of 4 bytes. Therefore, HTA[17:0] output an address that is divided by four.

3.3.2 General

This section outlines the processing of cell switching and header translation. First, an example where a cell input from logical input port #1 is output from logical output port #10 is given.

Figure 3-18. Example of Single Cast

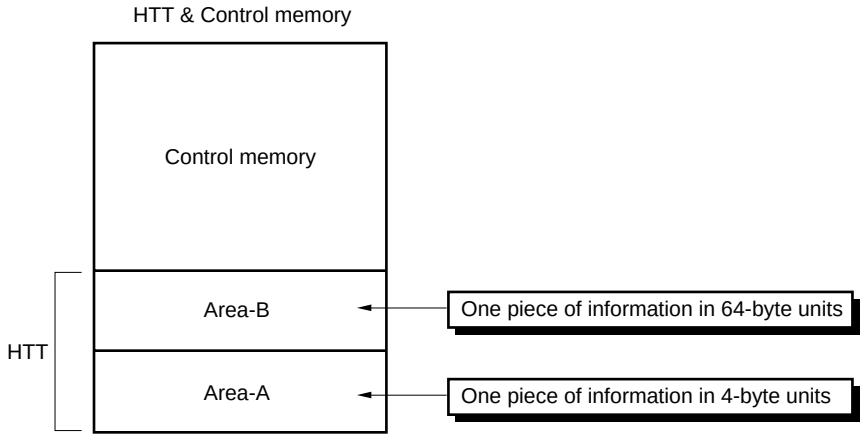


#n : Logical port number
UPn : UTOPIA port
PHYn : PHY (n indicates a PHY number.)

At this time, the μPD98410 must have the information “the cell input from logical input port #1 is output to logical output port #10”. It is the HTT (header translation table) that provides this information. The HTT is organized in the HTT & control memory, and is divided into Area-A and Area-B depending on the usage.

- Area-A ... Area used in both single cast and multi-cast modes
- Area-B ... Area used only in multi-cast mode

Figure 3-19. HTT (Header Translation Table)



Information at the output side is stored in the HTT. Information at the input side is used to calculate the addresses of the HTT area in which the information at the output side is stored. Therefore, the information at the output side is obtained based on the information at the input side.

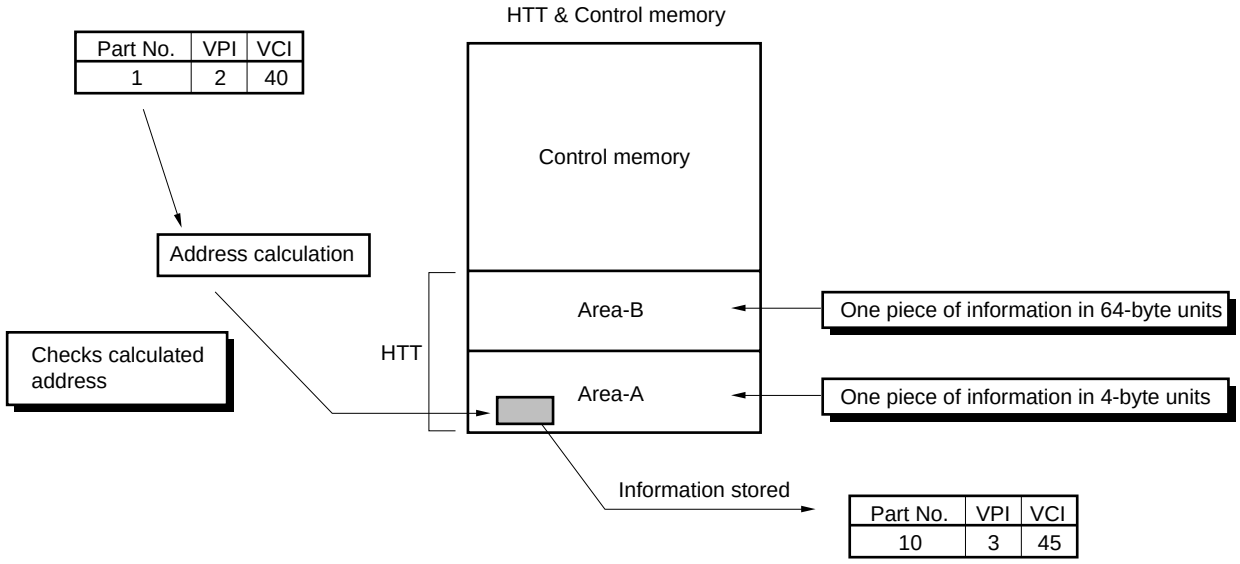
Information at output side

Port No.	VPI	VCI
10	3	45

Information at input side

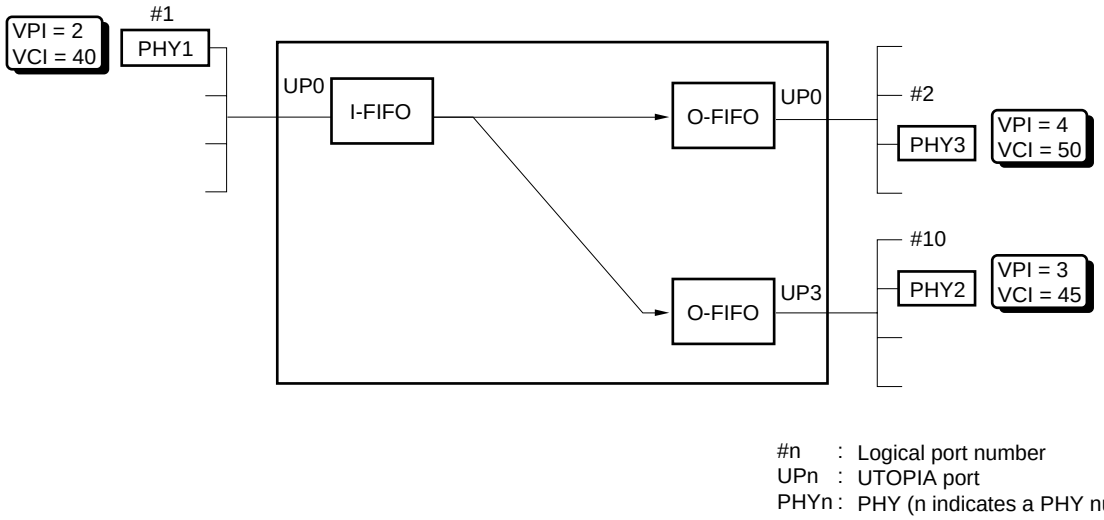
Port No.	VPI	VCI
1	2	40

Figure 3-20. Flow of Header Translation Information in Single-Cast Mode



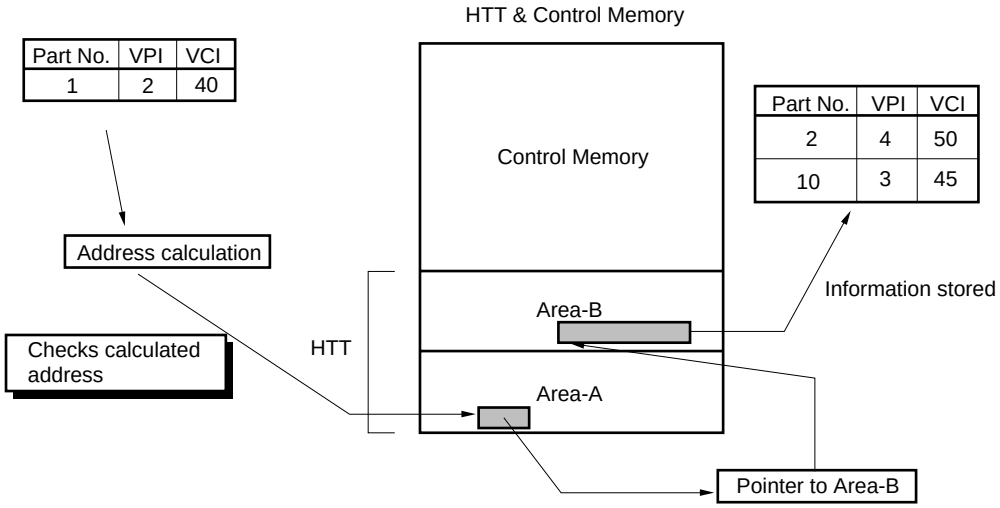
Area-B is also used in the multi-cast mode. At this time, a pointer that is used to access Area-B is stored in Area-A, and information at the output side is stored in Area-B. Figures 3-21 and 3-22 show this.

Figure 3-21. Example of Multi-Cast



#n : Logical port number
UPn : UTOPIA port
PHYn : PHY (n indicates a PHY number.)

Figure 3-22. Flow of Header Translation Information in Multi-Cast Mode



3.3.3 Format of HTT

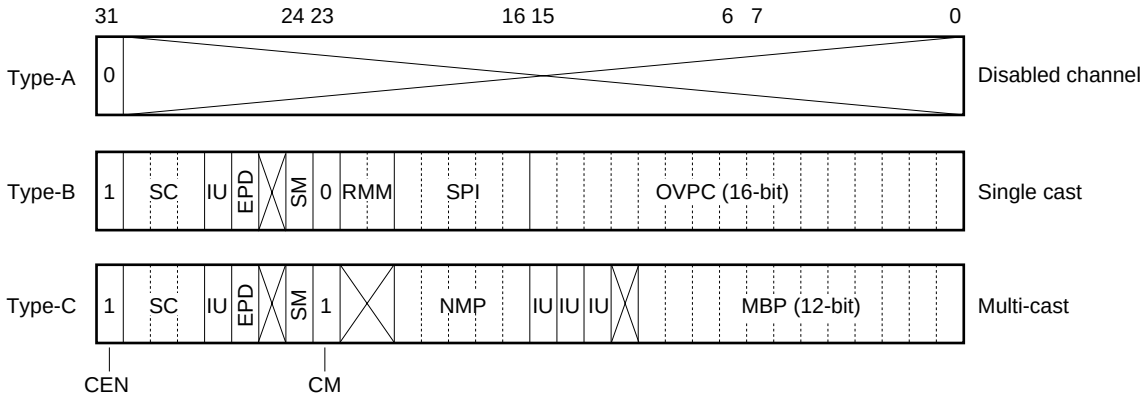
This section explains the format in which information is stored in Area-A and Area-B.

(a) Area-A format

The μPD98410 accesses Area-A by using a logical input port number, VPI, and VCI as pointers when cells are input.

Area-A stores the following information in 4-byte units.

Figure 3-23. HTT Area-A Format



- Area X is reserved. Write “0” to this area. This area is “undefined” when it is read.
- Area IU is used for the internal processing of the μPD98410. Set bit 13 of Type-C to “1”, and reset bits 14, 15, and 27 to “0”. These bits are “undefined” when read.

Symbol	Name	Size	Description
CEN	Channel Enable	1 bit	Makes the table valid or invalid. 0: Invalid 1: Valid
SC	Service Class	3 bits	Specifies a service class. 000: CBR 001: rtVBR 010: Reserved 011: nrtVBR 100: ABR 101: Reserved 110: UBR 111: Reserved

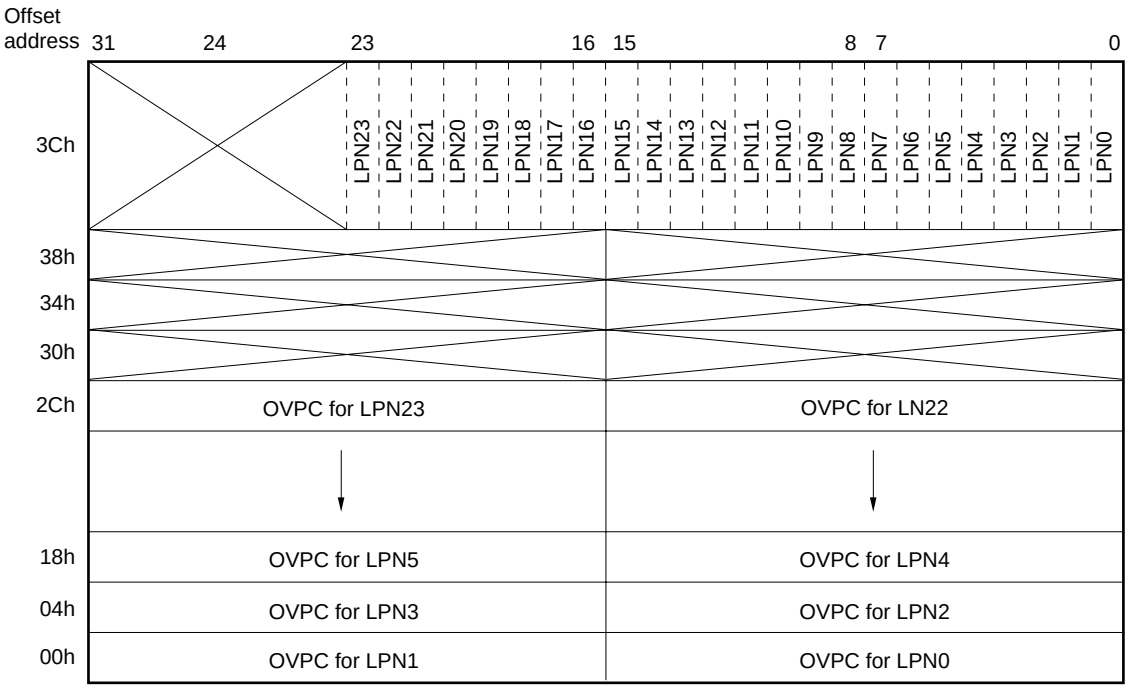
Symbol	Name	Size	Description
EPD	Early Packet Discard Enable	1 bit	Makes EPD valid or invalid. When CEN is active, the read value of this bit is not guaranteed because the μPD98410 rewrites the value. 0: EPD invalid 1: EPD valid
SM	Switching Mode	1 bit	Sets VP/VC connection. Only the SM bit in the HTT area that is accessed when VCI = 20h is meaningful. Reset the SM bits in the other areas to 0. However, the SM bit in the HTT area that is accessed when VCI = 20h is meaningless in Pre-Defined Channel (input VCI is 0 to 1Fh) of an RM cell having PID = 01H, and VC connection is set. 0: VC connection 1: VP connection
CM	Cast Mode	1 bit	Selects multi-cast or single cast. 0: Single cast 1: Multi-cast
RMM	RM Cell Merge Enable	2 bits	Sets RM cell merge processing for single cast connection in the backward direction for multi-cast connection. Set these bits to “00” for any other connection. 00: No merge & transfer 01: Reserved 10: Merge & transfer 11: Merge & discard
SPI	Single Cast Port ID	5 bits	Sets a logical output port number (0 to 23) in single cast mode. 00h to 17h: Logical output port 0 to 23
NMP	Number of Multi-Cast Port	5 bits	Sets a broadcasting count in multi-cast mode. 02h to 18h: Broadcast count 2 to 24
OVPC	Output VPI, VCI	16 bits	Sets VPI and VCI appended to the output cell (after header translation) in single cast mode.
MBP	Multicast Bitmap Pointer	12 bits	Sets a pointer to access Area-B in multi-cast mode.
IU	Internal used	–	These bits are used by the μPD98410 as a work area. Set bit 13 to “1” and reset bits 14, 15, and 27 to “0”.

(b) Area-B format

The μPD98410 accesses Area-B by using MBP as a pointer when a multi-cast cell is input.

The following information is stored in Area-B in 64-byte units.

Figure 3-24. HTT Area-B Format



- Area X is reserved. Write “0” to this area. This area is “undefined” when it is read.

Symbol	Name	Size	Description
LPN0 - LPN23 (MB)	Logical Port Number (Multicast Bitmap)	1 bit × 24	Sets the corresponding bit of the logical output port at the cast destination in multi-cast mode. 0: Does not cast to the corresponding port. 1: Casts to the corresponding port.
OVPC	Output VPI, VCI	16 bits × 24 ports	Sets VPI and VCI to be appended to the output cell (after header translation) in multi-cast mode.

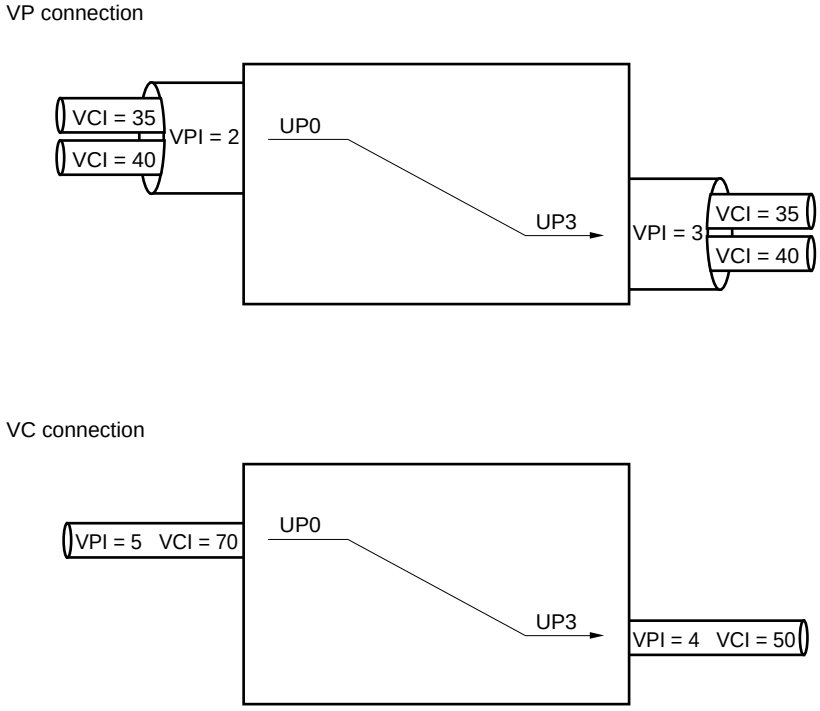
3.3.4 Accessing HTT

Accessing the HTT was mentioned in **3.3.2 General**. This section explains that in detail.

(1) VP connection and VC connection

The μPD98410 performs two types of switching: VP connection and VC connection. The differences between these two modes of switching are illustrated below.

Figure 3-25. VP Connection and VC Connection



(VP connection)

- Replaces only VPI of a cell header.

(VC connection)

- Replaces VPI and VCI of a cell header.

(2) Access to HTT

Section **3.3.2 General** discussed how to calculate the address to access the HTT by using a logical input port number, VPI , and VCI. In practice, however, the address is calculated in the following procedure, because of the differences between VP connection and VC connection. Figure 3-26 illustrates accessing the HTT in single cast mode. The procedure for accessing Area-A is the same in multi-cast mode.

<Procedure>

<1> The HTT is accessed by using the following value. The value read identifies whether the switching mode (SM) is VPC (VP connection) or VCC (VC connection).

Port No.	VPI	VCI
Logical input port number	VPI in input cell header	20h

<2>-1 If the switching mode is a VP connection, the header translation information is assigned to the area accessed in <1>.

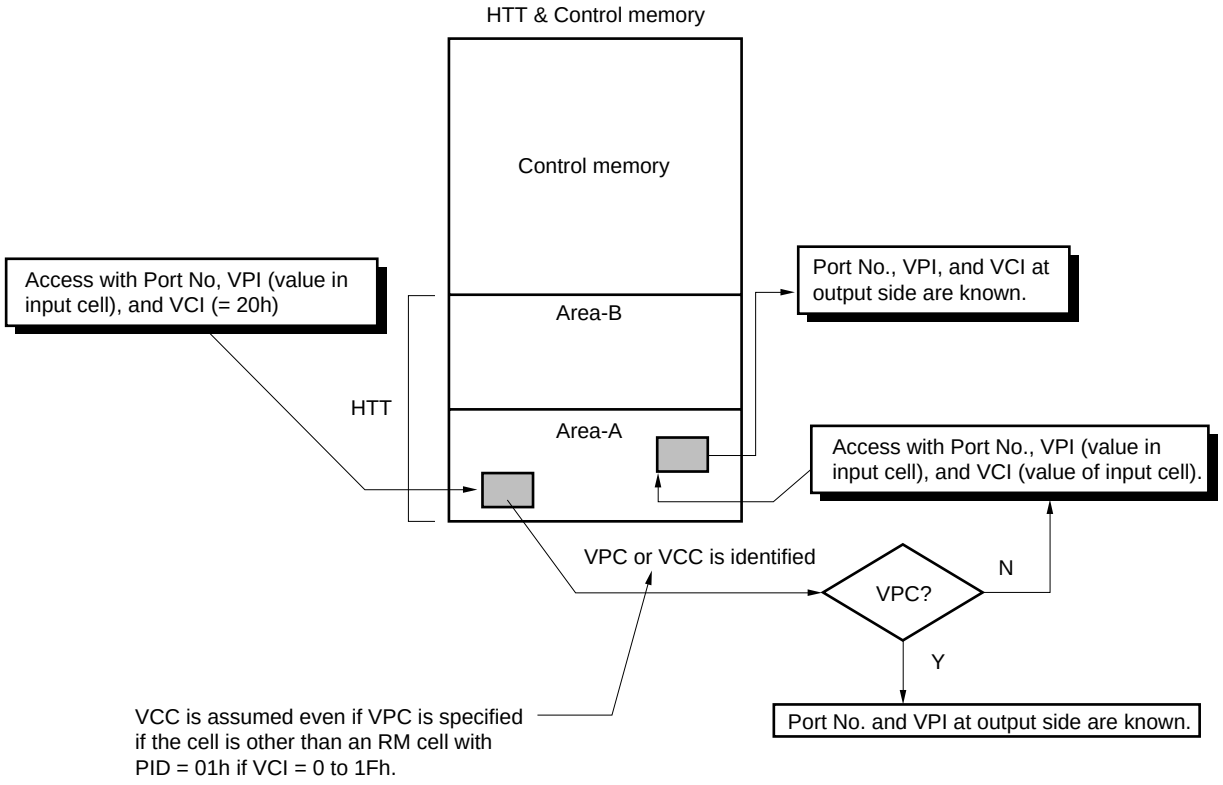
<2>-2 If the mode is VC connection, the HTT is accessed again by using the following value. The header translation information is assigned to this area (in a mode other than the switching mode (SM)).

Port No.	VPI	VCI
Logical input port number	VPI in input cell header	VCI in input cell header

Cautions 1. With a Pre-Defined Channel (Input-VCI = 0 to 1Fh) of a cell other than an RM cell with PID = 01h, the header is translated by means of normal VC connection even if VP connection is specified by the information on the switching mode (SM).

2. For an RM cell with PID = 01h, refer to 3.3.6 Accessing HTT with RM cell.

Figure 3-26. Difference in Access to HTT between VPC and VCC (single cast)



(3) Calculating HTT address

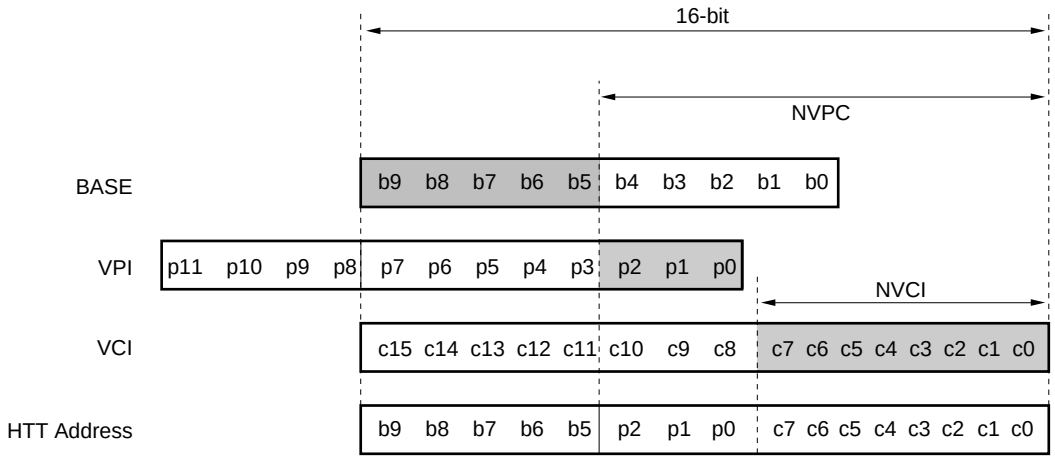
In **3.3.4 (2)**, it is explained that a logical input port number, VPI, and VCI are used to calculate an address when the Area-A of the HTT is accessed. This section explains how these parameters are used to calculate an address.

Internally, the μPD98410 has the following information for each logical input port.

NVPC	Number of valid bits of VPI + Number of valid bits of VCI
NVCI	Number of valid bits of VCI
BASE	Base address (offset value)

An actual HTT address is calculated as shown in Figure 3-27, based on the above information. In the example below, NVPC = 11 and NVCI = 8.

Figure 3-27. Calculating HTT Address



The valid range of BASE and HTT addresses is dependent upon the size of the HTT & control memory (the value of HMS bit of the mode register). The relationship between this size and the valid range of the HTT addresses is shown below (Figure 3-27 shows an example where HMS = 10).

HMS (32-bit per word)	BASE	HTT Address
00 (64K words)	[7:0]	[13:0]
01 (128K words)	[8:0]	[14:0]
10 (256K words)	[9:0]	[15:0]

(4) VPI and VCI of output cell

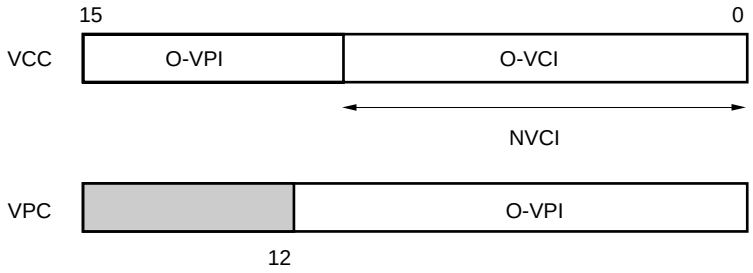
The procedure to obtain information on a port number at the output side, and VPI and VCI to be appended to an output cell has been discussed so far. Using this procedure, the information on a logical output port number can be obtained from the following:

- SPI of Area-A in single cast mode
- LPN0 through LPN23 of Area-B in multi-cast mode

Information on VPI and VCI can be obtained from the following. "OVPC" is set as shown in Figure 3-28, depending on the difference in the switching mode.

- OVPC of Area-A in single cast mode
- OVPC of Area-B in multi-cast mode

Figure 3-28. Setting Format of OVPC



NVCI is a parameter that specifies how many bits of OVPC (16 bits wide) are used as O-VCI (Output VCI). In the case of VPC, only the O-VPI (Output VPI) (12 bits) is stored. This is because the VPC replaces only the VPI and the VCI outputs the value of an input cell as is.

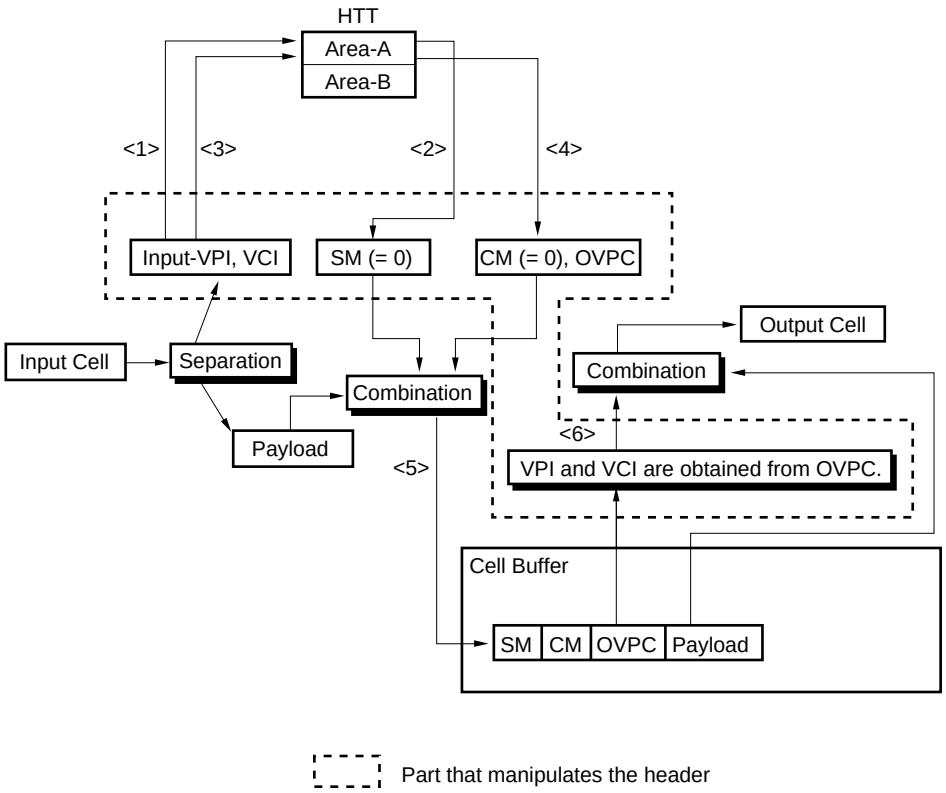
In the case of VCC, up to 16 bits can be used with VPI and VCI combined. The VPI and VCI fields in a cell header are 12 bits (NNI) and 16 bits, respectively. The 13th through 16th bits of the VPI field are fixed to "0" when a cell is output.

3.3.5 Flow of header translation

This section explains the flow of header translation depending on the differences in the switching mode and cast mode.

(1) VCC, single cast

Figure 3-29. Flow of Header Translation in VCC and Single Cast Modes



<Procedure>

<1> Area-A is accessed by using a logical input port number, Input-VPI, and VCI = 20h.

<2> Information about the VC connection (SM = 0) is obtained.

<3> Area-A is accessed again by using a logical input port number, Input-VPI, and Input-VCI.

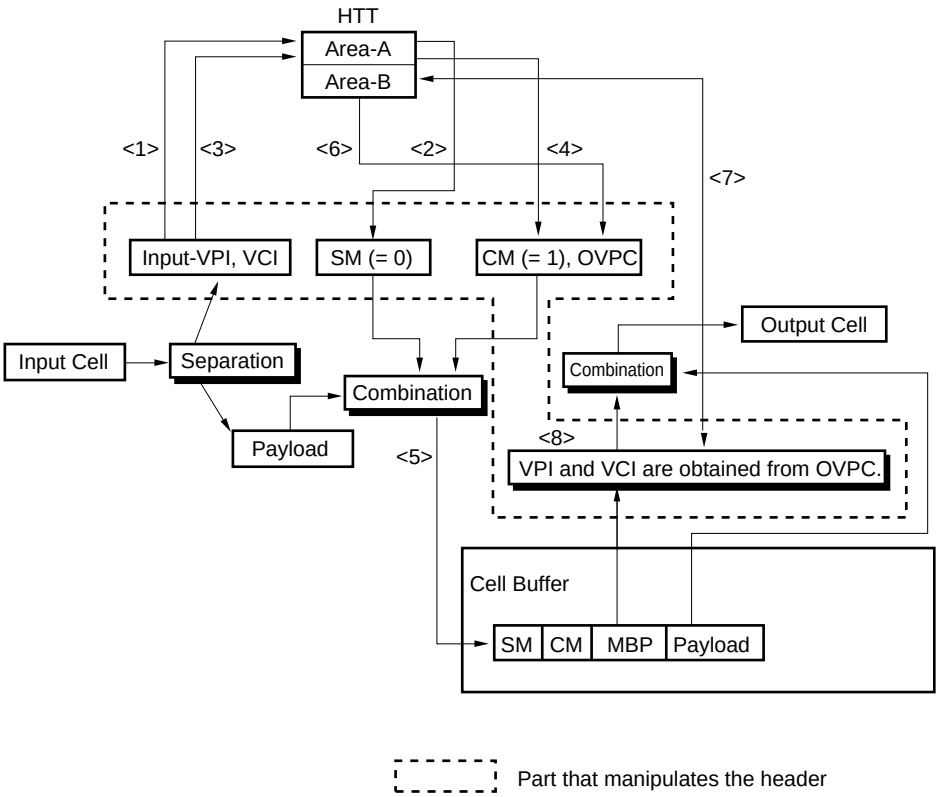
<4> OVPC is obtained in single cast mode (CM = 0). At the same time, a service class (SC) and a logical output port number (SPI) are also obtained, and the output queue that stores cell addresses is determined.

<5> SM, CM, and OVPC are stored in the cell buffer based on the payload of the input cell.

<6> VPI and VCI of the output cell header are set based on OVPC when the cell is output.

(2) VCC, multi-cast

Figure 3-30. Flow of Header Translation in VCC and Multi-Cast Modes



<Procedure>

<1> Area-A is accessed by using a logical input port number, Input-VPI, and VCI = 20h.

<2> Information about the VC connection (SM = 0) is obtained.

<3> Area-A is accessed again by using a logical input port number, Input-VPI, and Input-VCI.

<4> Multi-cast (CM = 1), pointer to Area-B (MBP), broadcast count (NMP), and service class (SC) are obtained.

<5> SM, CM, and MBP are stored in the cell buffer along with the payload of the input cell. The cell address is stored in the multi-cast queue.

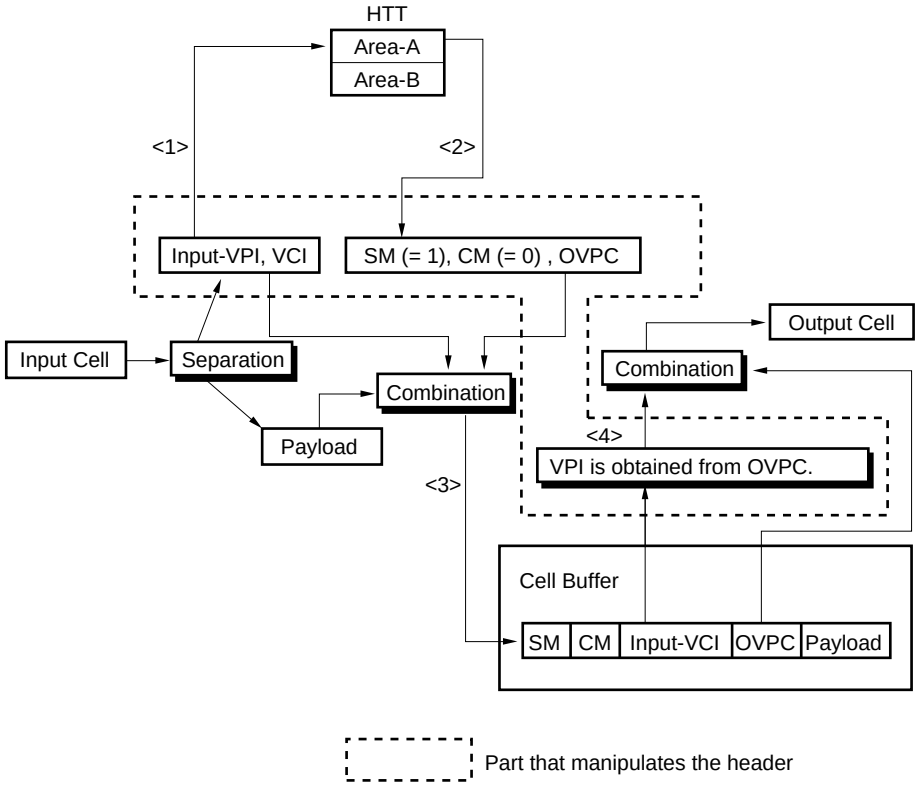
<6> Area-B is accessed by using MBP before re-queuing, and the logical output port number to be cast is obtained. At this time, the cell address is stored in the output queue.

<7> Area-B is accessed again when the cell is output, and the OVPC information on each logical output port is obtained.

<8> VPI and VCI of the output cell header are set from OVPC.

(3) VPC, single cast

Figure 3-31. Flow of Header Translation in VPC and Single Cast Modes



<Procedure>

<1> Area-A is accessed by using a logical input port number, Input-VPI, and VCI = 20h.

<2> Single cast (CM = 0) and OVPC (O-VPI information only in OVPC) are obtained based on information VP connection (SM = 1). Because a service class (SC) and a logical output port number (SPI) are also obtained, the output queue in which the cell address is to be stored is determined.

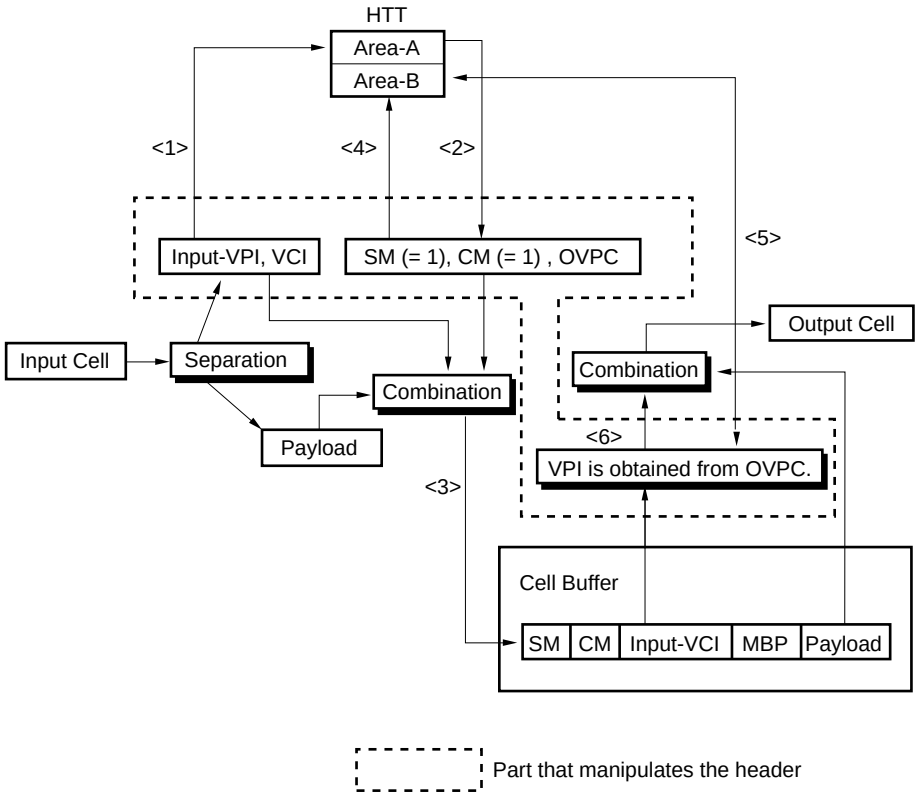
<3> SM, CM, Input-VCI, and OVPC are stored along with the payload of the input cell.

<4> VPI is obtained from OVPC when the cell is output. VCI uses Input-VCI as is.

Caution With a Pre-Defined Channel (Input-VCI = 0 to 1Fh) of a cell other than an RM cell with PID = 01h, the header is translated by means of ordinary VC connection even if VP connection is specified by the information on SM obtained in <2>. In the same manner as ordinary VC connection, O-VPI and O-VCI are obtained from OVPC information. The setting of EPD is valid even if SM is specified for VP connection.

(4) VPC, multi-cast

Figure 3-32. Flow of Header Translation in VPC and Multi-Cast Modes



<Procedure>

<1> Area-A is accessed by using a logical input port number, Input-VPI, and VCI = 20h.

<2> Information about the VP connection (SM = 1) is obtained. At the same time, multi-cast (CM = 1), pointer to Area-B (MBP), broadcast count (NMP), and service class (SC) are also obtained.

<3> Input-VCI, SM, CM, and MBP are stored in the cell buffer along with the payload of the input cell. The cell address is stored in the multi-cast queue.

<4> Area-B is accessed by using MBP before re-queuing, and the logical output port number to be cast is obtained. At this time, the cell address is stored in the output queue.

<5> Area-B is accessed again when the cell is output, and the OVPC information of each logical output port is obtained.

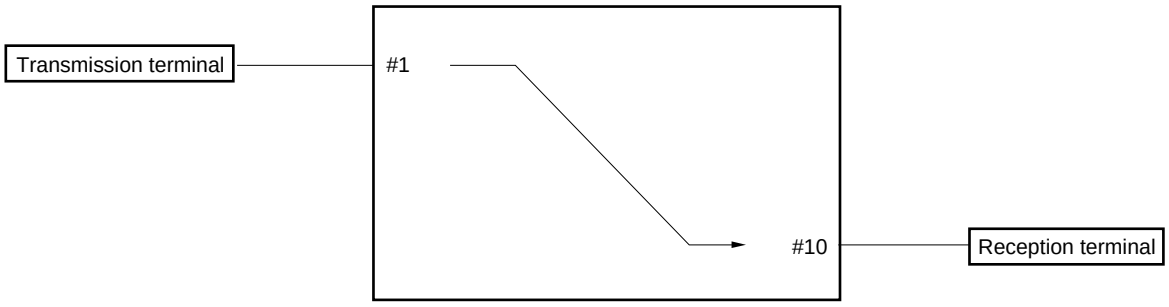
<6> VPI is obtained from OVPC. VCI uses Input-VCI as is.

Caution With a Pre-Defined Channel (Input-VCI = 0 to 1Fh) of a cell other than an RM cell with PID = 01h, the header is translated by means of ordinary VC connection even if VP connection is specified by the information on SM obtained in <2>. In the same manner as ordinary VC connection, O-VPI and O-VCI are obtained from OVPC information. The setting of EPD is valid even if SM is specified for VP connection.

3.3.6 Accessing HTT with RM cell

(1) Connection in ABR class

In ABR (Available Bit Rate) class, connection of the Backward RM cell that reports congestion information in the transmission terminal direction must be set.



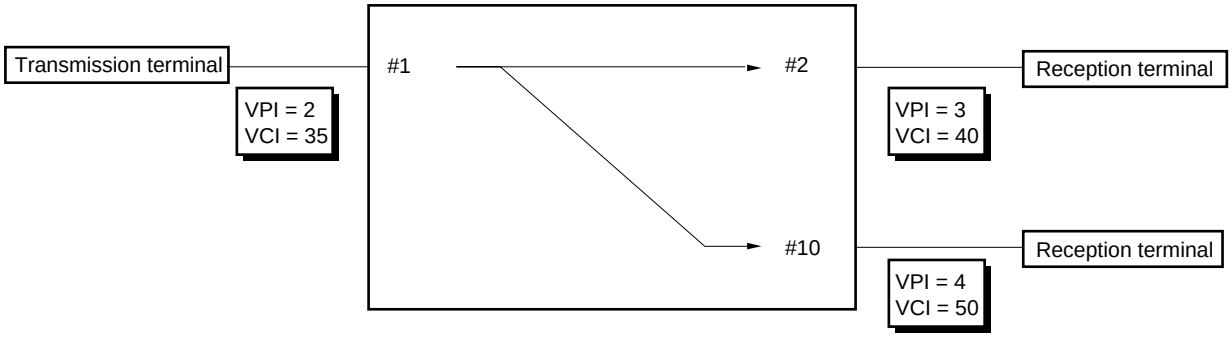
#n: Logical port number

Assuming that a cell is transmitted in the combination (A) in the table below, connection in the backward direction must be set in combination (B) to return the Backward RM cell.

	Logical Input Port Number	Logical Output Port Number
(A)	1	10
(B)	10	1

(2) Multi-cast and RM cell merge function

Next, the case of multi-cast is considered.



#n: Logical port number

In this case, multi-cast connection (a) in the table below must be set in the transmission direction of the cell, and two single cast connections such as in (b) must be set in the backward direction.

	Logical Input Port Number	Logical Output Port Number
(a)	1	2, 10
(b)	2	1
	10	1

Now, let's consider the case in which the RM cell merge function is used. This function must be used to OR the CI and NI bits of the Backward RM cell that is input from the two connections set in (b) and to AND the BN bit. At this time, the work area used for ORing and ANDing is reserved in the HTT used in (a). If the Backward RM cell is input to connection (b), therefore, the address of the HTT used in (a) (address obtained in the table below) must be determined by some means.

	Logical Input Port Number	VPI	VCI
At VPC	1	2	20h
At VCC	1	2	35

Because (b) and (a) are completely opposite to each other in terms of input/output, the following values assigned to the HTT in (b) are used to obtain the value in the above table.

	Logical Input Port Number of (a)	VPI of (a)	VCI of (a)
At VPC	Logical output port number (SPI)	OVPC	20h
At VCC	Logical output port number (SPI)	OVPC	OVPC

If the input cell is the Backward RM cell (and cells are to be merged), therefore, the HTT is accessed two times to translate the header and merge the RM cell. In **3.3.5 Flow of header translation**, the switching mode is identified by the value of SM when the HTT is accessed with VCI = 20h. With an RM cell having PID = 01h, VPC is identified if VCI in the cell header is 6, and VCC is identified if it is other than 6. Consequently, care must be exercised because the μPD98410 performs its processing assuming that both a VPC RM cell and a VC RM cell flowing in that VP are RM cells.

(VPC)

<1> The HTT of (b) is accessed by using a logical input port number, VPI of the input cell, and VCI = 20h.

<2> The HTT of (a) is accessed by using a logical output port number (SPI), OVPC, and VCI = 20h.

(VCC)

<1> The HTT of (b) is accessed by using a logical input port number, and VPI and VCI of the input cell.

<2> The HTT of (a) is accessed by using a logical output port number (SPI), and VPI and VCI in OVPC.

3.4 Queue Control

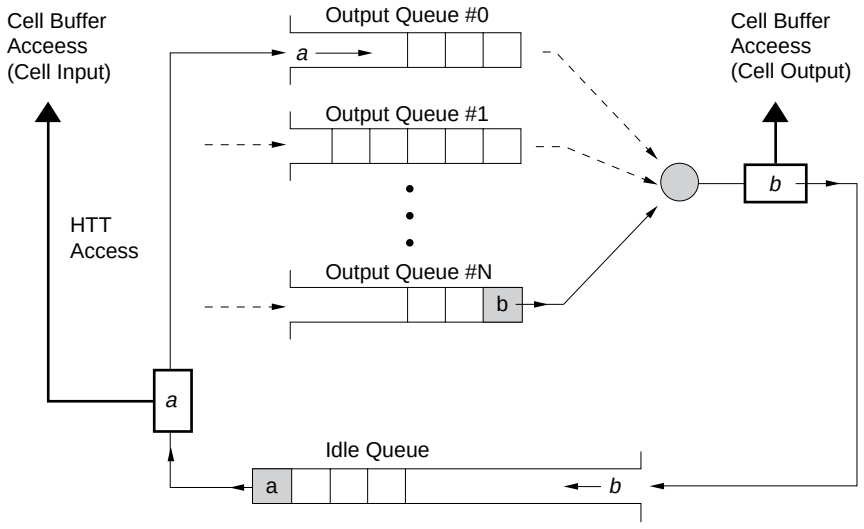
The μPD98410 organizes the following queues in the control memory for management of the cell buffer.

- The idle queue queues an address pointer that indicates the position of the cell buffer to which the cells can be stored.
- The multi-cast queue queues an address pointer that indicates the position to which the cells to be multi-cast are stored.
- The output queue which is provided for each logical output port queues an address pointer that indicates the position to which a cell for each logical output port is stored.

3.4.1 Single cast

This section explains the processing sequence of the output queue in the single cast mode.

Figure 3-33. Queuing of Cell Address (Single Cast)



a, b : Cell Address Pointer
HTT: Header Translation Table

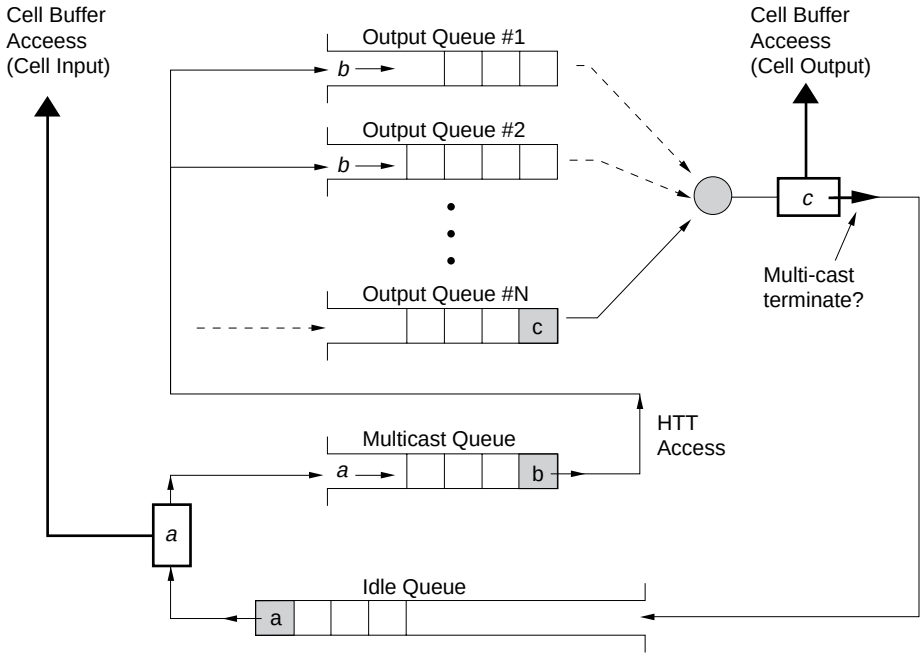
- **Cell input procedure (obtaining write address of cell buffer)**
  1. Cell address a is obtained from the idle queue.
  2. The input cell is stored in the cell buffer indicated by cell address a.
  3. A logical output port number is obtained from the header translation table (HTT).
  4. Cell address a is input to the output queue of the logical output port obtained.

- **Cell output procedure (obtaining read address of cell buffer)**
  1. Cell address b is obtained from the output queue of a logical output port.
  2. An output cell is obtained from the cell buffer indicated by cell address b.
  3. Cell address b is input to the idle queue.

3.4.2 Multi-cast

The μPD98410 realizes multi-casting by storing input cells in one location in the cell buffer and inputting cell addresses to the output queue of each logical output port. The advantage of this method is that it is not necessary to copy 53-byte cells more than once. In this way, the cell buffer can be used effectively and casting can be performed at high speed.

Figure 3-34. Queuing of Cell Address (Multi-Cast)



a, b : Cell Address Pointer
HTT: Header Translation Table

- **Cell input procedure (obtaining write address of cell buffer)**
  1. Cell address a is obtained from the idle queue.
  2. The input cell is stored in the cell buffer indicated by cell address a.
  3. Cell address a is input to the multi-cast queue.

- **Re-queuing procedure**
  1. Cell address b is obtained from the multi-cast queue.
  2. A logical output port number is obtained from the header translation table (HTT).
  3. Cell address b is input to the output queue of each logical output port.

- **Cell output procedure (obtaining read address of cell buffer)**
  1. Cell address c is obtained from the output queue of a logical output port.
  2. The output cell is obtained from the cell buffer indicated by cell address c.
  3. Cell address c is input to the idle queue after the cell has been output to all the logical output ports to be multi-cast.

3.4.3 Congestion control

ATM defines service classes based on Cell Loss Ratio/Cell Transfer Delay/Cell Delay Variation that indicate the traffic status of cells and transfer quality. The μPD98410 divides the service classes into the following four classes for management.

- CBR (Constant Bit Rate Service), rtVBR (Real time Variable Bit Rate Service)
- RM (RM cell), nrtVBR (Non real time VBR Service)
- ABR (Available Bit Rate Service)
- UBR (Unspecified Bit Rate Service)

Remark The RM cell is included in the ABR class but the μPD98410 treats the RM cell as one of the service classes. The user cannot specify a class for the RM cell.

The μPD98410 has the following queues and counters. Congestion control is performed by using the threshold values that are assigned to these queues and counters. Figure 3-35 shows the relationship between the queues, counters, and their threshold values.

- **UC: Used Cell Counter**
  This counter indicates the total number of cells retained in the cell buffer. The value assigned to the ALLmin register as the minimum queue length is also treated as the number of cells retained in the cell buffer. When performing multi-cast, only one cell is counted in, regardless of the broadcast count.

- **TC: Total Cell Counter for each class (4 classes)**
  If the number of cells retained in the output queue exceeds the minimum queue length OQminCRV/OQminRNV/OQminABR/OQminUBR of each class, this counter indicates the total sum of the number of cells of each class that exceeds the minimum length. When performing multi-cast, the number of cells is counted in accordance with broadcast count.

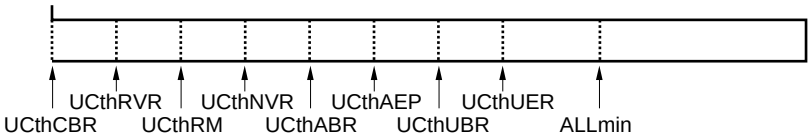
- **IQ: Idle Queue**
  This queue queues the addresses of a vacant area in the cell buffer.

- **OQ: Output Queue (24 ports × 4 classes)**
  This queue queues the addresses of the cell buffer in which the cells are stored by each logical output port and class.

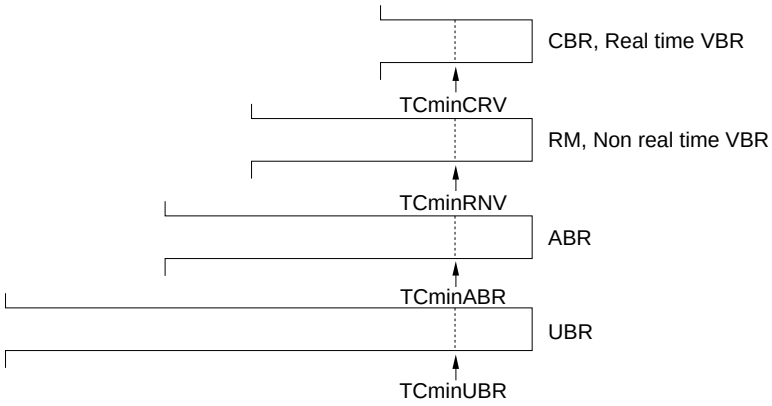
- **MQ: Multicast Queue (4 classes)**
  This queue queues the address of the cell buffer in which cells of each class are stored.

Figure 3-35. Queues and Counters by Service Class

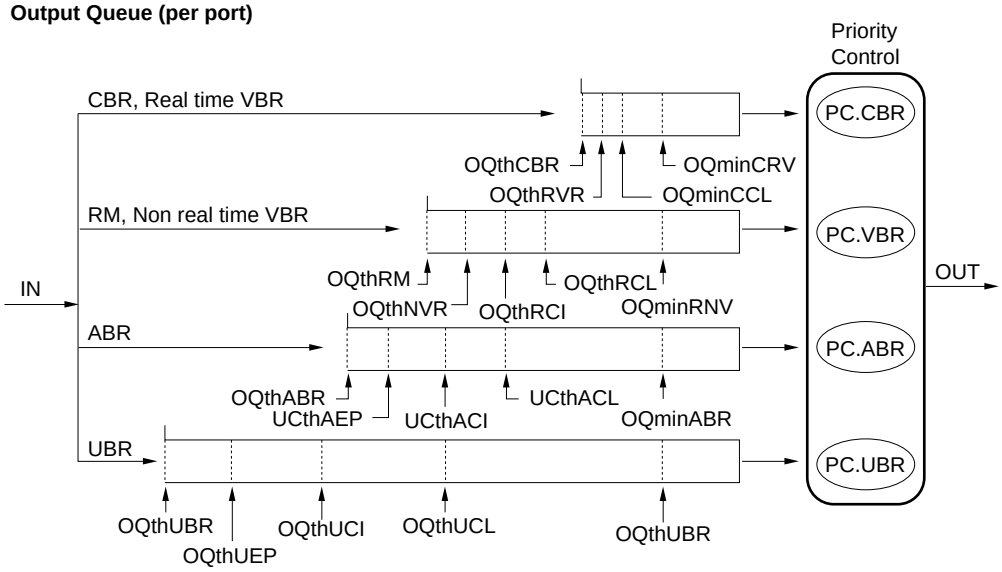
Used Cell Counter (on cell buffer)



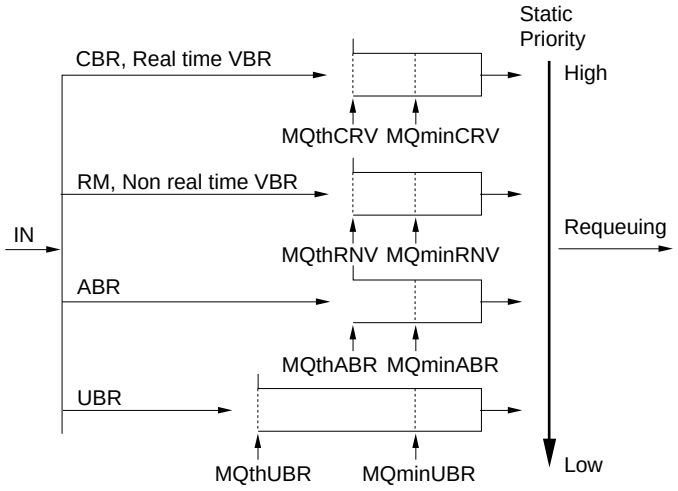
Total Cell Counter for each class (except each OQminXXX)



Output Queue (per port)



Multicast Queue



UC: Threshold values related to Used Cell Counter

- UCthCBR CBR cell discard threshold value
- UCthRVR rtVBR cell discard threshold value
- UCthRM RM cell discard threshold value
- UCthNVR nrtVBR cell discard threshold value
- UCthABR ABR cell discard threshold value
- UCthAEP ABR cell EPD threshold value
- UCthUBR UBR cell discard threshold value
- UCthUEP UBR cell EPD threshold value

TC: Threshold values related to Total Cell Counter for each class (none)

IQ: Threshold values related to Idle Queue (none)

OQ: Threshold values related to Output Queue

- OQthCBR CBR cell discard threshold value of output port
- OQthRVR rtVBR cell discard threshold value of output port
- OQthCCL CBR/rtVBR cell CLP discard threshold value of output port
- OQthRM RM cell discard threshold value of output port
- OQthNVR nrtVBR cell discard threshold value of output port
- OQthRCI RM/nrtVBR cell EFCI threshold value of output port
- OQthRCL RM/nrtVBR cell CLP discard threshold value of output port
- OQthABR ABR cell discard threshold value of output port
- OQthAEP ABR cell EPD threshold value of output port
- OQthACI ABR cell EFCI threshold value of output port
- OQthACL ABR cell CLP discard threshold value of output port
- OQthUBR UBR cell discard threshold value of output port
- OQthUEP UBR cell EPD threshold value of output port
- OQthUCI UBR cell EFCI threshold value of output port
- OQthUCL UBR cell CLP discard threshold value of output port

MQ: Threshold values related to Multicast Queue

- MQthCRV CBR/rtVBR cell discard threshold value of multi-cast queue
- MQthRNV RM/nrtVBR cell discard threshold value of multi-cast queue
- MQthABR ABR cell discard threshold value of multi-cast queue
- MQthUBR UBR cell discard threshold value of multi-cast queue

UC: Minimum queue length related to Used Cell Counter

- ALLmin Total sum of each minimum queue length

TC: Minimum queue length related to Total Cell Counter for each class

- TCminCRV Minimum queue length allocated to CBR/rtVBR class
- TCminRNV Minimum queue length allocated to RM/nrtVBR class
- TCminABR Minimum queue allocated to ABR class
- TCminUBR Minimum queue allocated to UBR class

IQ: Minimum queue length related to Idle Queue (none)

OQ: Minimum queue length related to Output Queue

- OQminCRV Minimum queue length allocated to CBR/rtVBR class of output port
- OQminRNV Minimum queue length allocated to RM/nrtVBR class of output port
- OQminABR Minimum queue length allocated to ABR class of output port
- OQminUBR Minimum queue length allocated to UBR class of output port

MQ: Threshold values related to Multicast Queue

- MQminCRV Minimum queue length allocated to CBR/rtVBR class of multi-cast queue
- MQminRNV Minimum queue length allocated to RM/nrtVBR class of multi-cast queue
- MQminABR Minimum queue length allocated to ABR class of multi-cast queue
- MQminUBR Minimum queue length allocated to UBR class of multi-cast queue

3.4.4 Cell discard by class

The μPD98410 forcibly discards cells that pass a congestion point if it detects congestion according to the cell discard threshold value for each class.

It controls discarding cells, giving them priorities, during the following periods:

- While the total number of cells exceeds the cell discard threshold value.
- While the output queue length of each logical output port exceeds each cell discard threshold value.

Table 3-2. Cell Discard Threshold Value Related to Total Number of Cells

Threshold Value Name	Control if Threshold Value Is Exceeded (processing during cell input)
UCthCBR	Discards CBR cell.
UCthRVR	Discards rtVBR cell.
UCthRM	Discards RM cell.
UCthNVR	Discards nrtVBR cell.
UCthABR	Discards ABR cell.
UCthUBR	Discards UBR cell.

Remark UCthAEP and UCthUEP are the cell discard threshold values for a channel that disables EPD in each class of ABR and UBR.

Table 3-3. Cell Discard Threshold Value of Output Queue Length

Threshold Value Name	Control if Threshold Value Is Exceeded (processing during cell input)
OQthCBR	Discards CBR cell of the corresponding port.
OQthRVR	Discards rtVBR cell of the corresponding port.
OQthCCL	Discards CBR/rtVBR cell of the corresponding port with CLP = 1.
OQthRM	Discards RM cell of the corresponding port.
OQthNVR	Discards nrtVBR cell of the corresponding port.
OQthRCL	Discards RM/nrtVBR cell of the corresponding port with CLP = 1.
OQthABR	Discards ABR cell of the corresponding port.
OQthACL	Discards ABR cell of the corresponding port with CLP = 1.
OQthUBR	Discards UBR cell of the corresponding port.
OQthUCL	Discards UBR cell of the corresponding port with CLP = 1.

Remarks 1. OQthAEP and OQthUEP are the cell discard threshold values for a channel that disables EPD in each class of ABR and UBR.

2. CLP is information contained in a header and indicates the priority in the same channel.

Table 3-4. Cell Discard Threshold Values Related to Multi-Cast Queue Length

Threshold Value Name	Control if Threshold Value Is Exceeded (processing during cell input)
MQthCRV	Discards CBR/rtVBR cell of multi-cast queue
MQthRNV	Discards RM/nrtVBR cell of multi-cast queue
MQthABR	Discards ABR cell of multi-cast queue
MQthUBR	Discards UBR cell of multi-cast queue

3.4.5 EPD (Early Packet Discard) control

The μPD98410 has an EPD control function. This function is to discard cells in units of the AAL-5 CS-PDU packets that are set as VC connection before congestion takes place. By discarding packets that have a high probability of being discarded after inputting packets has been started, discarding a packet that has been already input can be prevented.

Whether EPD control is performed if each queue length exceeds the EPD threshold value depends on whether control is enabled for the channel in question (by the EPD bit value of HTT). The μPD98410 operates differently, as follows, depending on whether control is enabled or disabled.

(1) If EPD control is enabled

EPD control is started as soon as the total number of cells and output queue length exceed the EPD threshold value. Once EPD control has been started, the following test is made in respect to the input cells.

(a) If the cell is included in the packet that has been started to be input when EPD control was started

→ Input cells up to the EOP (End Of Packet) cell that indicates the end of the packet is received.

(b) If the cell is in a packet for which input started after EPD control began

→ The cells of all the packets except the EOP cell are discarded, so that illegal packets are not processed at the reception terminal side by discarding the EOP cell.

Figure 3-36. When EPD Control Is Enabled

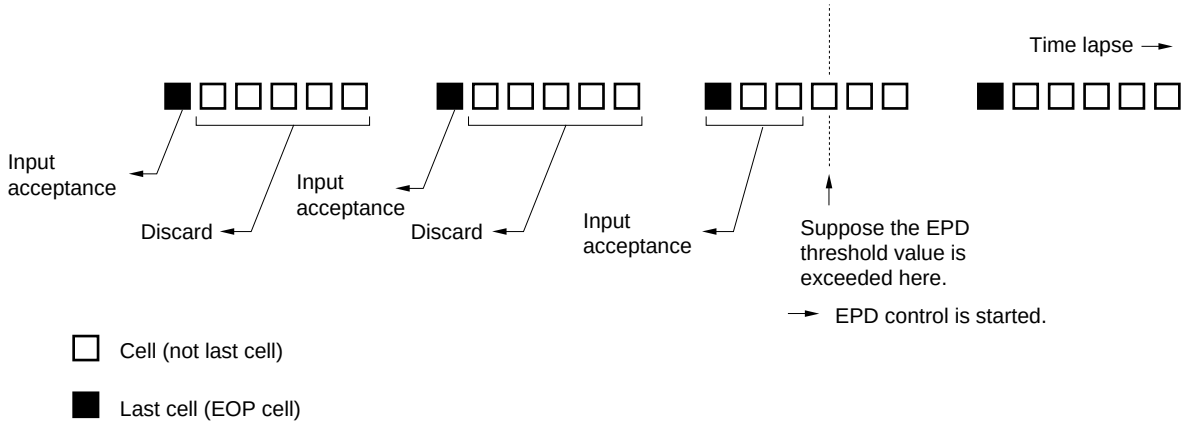
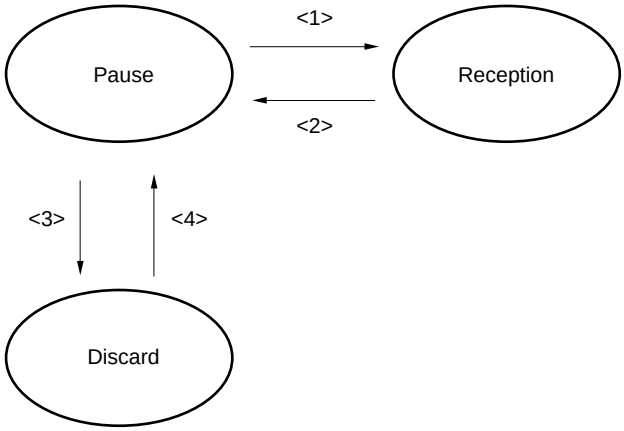


Figure 3-37 shows the status transition when EOP control is enabled.

Figure 3-37. Status Transition When EOP Control Is Enabled

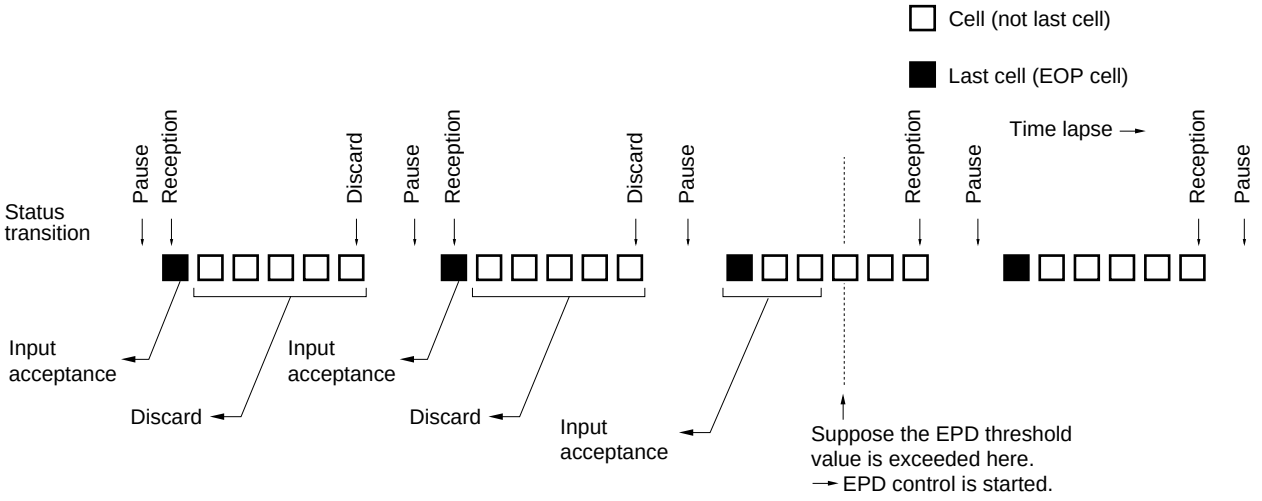


<Processing flow and status transition>

In the initial status, control is paused. If a cell is input in this status, it is checked whether the total number of current cells and output queue length exceed the EPD threshold value.

If the threshold value is not exceeded, the cell is received (<1>); if it is exceeded, the cell is discarded (<3>). When the last cell of the AAL-5 packet is input, control is paused again (<2> and <4>). If the receive status was entered when the first cell of the packet was input, therefore, all the cells are received up to the last cell. If the discard status was entered when the first cell was input, all the cells except the last cell are discarded. The last cell is always received in either status.

Figure 3-38. Status Transition of EPD Control



When receiving packets other than AAL-5, EPD control must be disabled because packets are not managed by using the last cell.

The following tables list the threshold values used for EPD control.

- **EPD threshold values related to total number of cells**

Threshold Value	Description
UCthAEP	EPD threshold value for cell of ABR class
UCthUEP	EPD threshold value for cell of UBR class

- **EPD threshold values related to output queue**

Threshold Value	Description
OQthAEP	EPD threshold value for cell of ABR class
OQthUEP	EPD threshold value for cell of UBR class

Remark A channel for which EPD control is disabled discards cells if the queue length exceeds these threshold values. For ABR and UBR classes, therefore, UCthABR, UCthUBR, OQthABR, and OQthUBR described in **3.4.4 Cell discard by class**, and the threshold values shown above play the role of cell discard threshold values.

(2) When EPD control is disabled

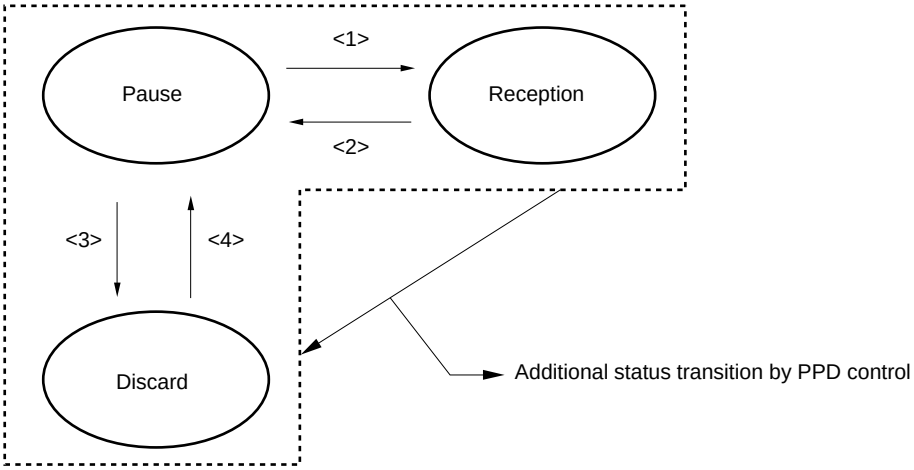
In this case, the above test is not made and the cells are discarded when all the cells in a packet exceed the EPD threshold value.

3.4.6 PPD (Partial Packet Discard) control

With PPD control, if a cell in a packet is discarded, all the subsequent cells in the packet are discarded when they are input. If the EPD threshold value is exceeded and EPD control is effected, therefore, the packet that is already being input is received up to its EOP (End of Packet) cell. If a cell is discarded because a threshold value other than the EPD threshold value is exceeded during reception controlled by the EPD control function, all the cells in the packet, except the EOP cell, are discarded.

Figure 3-39 shows the status transition when PPD control is performed. In contrast to EPD control, PPD control has additional status transition <5> shown in this figure. If a discard threshold value other than the EPD threshold value is exceeded in the reception status of EPD control, the cells are discarded.

Figure 3-39. Status Transition of PPD Control



3.4.7 Minimum queue length

With the shared buffer method, if the class of a specific logical output port is in the congestion status, the threshold values related to the total number of cells (Used Cell Counter) of that class are exceeded. As a result, the cells of the same class at the other logical output ports may be discarded.

To prevent this, the μPD98410 secures a minimum queue length that is not affected by the congestion status of other logical output ports. It also manages the queue length of each class, secures a minimum queue length that is not affected by the congestion status of the other classes, and guarantees the minimum queue length of each class for a cell that exceeds the minimum queue length of each port.

Table 3-5. Minimum Queue Length Related to Total Number of Cells (Used Cell Counter)

Threshold Value Name	Processing during Cell Input
ALLmin	Ensures the specified number of cells exist in the cell buffer to guarantee the minimum queue length. The total of all the minimum queue lengths must be specified. For details of how to calculate this value, refer to **4.2.24 Total number of cells minimum threshold value register**.

Table 3-6. Minimum Queue Length Related to Total Number of Cells of Each Class (Total Cell Counter for each class)

Threshold Value Name	Processing during Cell Input
TCminCRV	Guarantees the minimum queue of a class for the CBR/rtVBR cell that exceeds OQminCRV of an output port.
TCminRNV	Guarantees the minimum queue of a class for the RM/nrtVBR cell that exceeds OQminRNV of an output port.
TCminABR	Guarantees the minimum queue of a class for the ABR cell that exceeds OQminABR of an output port.
TCminUBR	Guarantees the minimum queue of a class for the UBR cell that exceeds OQminUBR of an output port.

Table 3-7. Minimum Queue Length Related to Output Queue Length

Threshold Value Name	Processing during Cell Input
OQminCRV	Guarantees minimum queue for CBR/rtVBR cell of each output port.
OQminRNV	Guarantees minimum queue for RM/nrtVBR cell of each output port.
OQminABR	Guarantees minimum queue for ABR cell of each output port.
OQminUBR	Guarantees minimum queue for UBR cell of each output port.

Table 3-8. Minimum Queue Length Related to Multi-Cast Queue

Threshold Value Name	Processing during Cell Input
MQminCRV	Guarantees minimum queue for CBR/rtVBR cell of multi-cast queue.
MQminRNV	Guarantees minimum queue for RM/nrtVBR cell of multi-cast queue.
MQminABR	Guarantees minimum queue for ABR cell of multi-cast queue.
MQminUBR	Guarantees minimum queue for UBR cell of multi-cast queue.

The priority for discarding cells when a threshold value is exceeded is as described below ((1) > (2) > (3) > (4)), and cells are discarded or queued. “Exceeding a threshold value” means the status where queue length ≥ threshold value.

(1) The cell is discarded if the discard threshold value (MAX. threshold value (*1)) of an output queue or multi-cast queue is exceeded, if the EPD threshold value (*2) is exceeded by a cell not subject to EPD, or if the CLP threshold value (*3) is exceeded by a cell subject to CLP.
(2) The cell is queued if the minimum threshold value (MIN. threshold value of the output queue or multi-cast queue (*4) or MIN. threshold value (*5) of the total number of cells for each class (Total Cell counter for each class)) is not exceeded.
(3) The cell is discarded if the discard threshold value of the total number of cells (Used Cell Counter (MAX. threshold value (*6) or if the EPD threshold value (*7) is exceeded by a cell not subject to EPD.
(4) The cell is queued if none of the above conditions are satisfied.

Each threshold value is classified as shown in Table 3-9.

Table 3-9. Classification and Names of Threshold Values

Classification		OQ (Output Queue)/ MQ (Multicast Queue)	TC (Total Cell Counter for each class)	UC (Used Cell Counter)
Discard threshold value	MAX. threshold value	(*1) OQthCBR, OQthRVR OQthRM, OQthNVR OQthABR, OQthUBR MQthCRV, MQthRNV MQthABR, MQthUBR	—	(*6) UCthCBR, UCthRVR UCthRM, UCthNVR UCthABR, UCthUBR
	EPD threshold value	(*2) OQthAEP, OQthUEP	—	(*7) UCthAEP, UCthUEP
	CLP threshold value	(*3) OQthCCL, OQthRCL OQthACL, OQthUCL	—	—
MIN. threshold value		(*4) OQminCRV, OQminRNV OQminABR, OQminUBR MQminCRV, MQminRNV MQminABR, MQminUBR	(*5) TCminCRV, TCminRNV TCminABR, TCminUBR	—
EFCI threshold value		OQthRCI OQthACI, OQthUCI	—	—

3.5 ABR Congestion Control

When the μPD98410 detects congestion status, it can report the congestion in the receiver terminal direction by using the EFCI bit of the user cell, and in the transmitter terminal direction by using the CI, NI, and BN bits of the Backward RM cell.

3.5.1 EFCI (Explicit Forward Congestion Indicator)

When the μPD98410 detects congestion status by using the EFCI threshold value, it sets the EFCI bit (PTI = 010, 011) included in the header of the user cell that passes the congestion point to report congestion in the receiver terminal direction. The EFCI bit is set for the cells belonging to the nrtVBR, ABR, and UBR classes.

EFCI control is performed while the output queue length exceeds the EFCI threshold value.

Table 3-10. EFCI Threshold Value Related to Output Queue

Threshold Value Name	Control if Threshold Value Is Exceeded (processing during cell output)
OQthRCI	Performs EFCI marking of user cell of nrtVBR class of corresponding port.
OQthACI	Performs EFCI marking of user cell of ABR class of corresponding port.
OQthUCI	Performs EFCI marking of user cell of UBR class of corresponding port.

3.5.2 RM cell CI/NI marking (Resource Management Cell CI/NI Congestion Indication Marking)

When the μPD98410 detects congestion status of ABR class by using the EFCI threshold value, it sets the CI bit (CI Marking) and NI bit (NI Marking) included in the payload for the Backward RM cell of protocol ID = 1 that passes the congestion point, in order to report the congestion in the transmitter terminal direction. The Backward RM cell that passes the congestion point is the Backward cell that is input to the logical input port having the same number as that of the logical output port in the congestion status. Figure 3-40 shows the configuration of the RM cell (Resource Management Cell).

Figure 3-40. RM Cell Configuration (ATM Forum TM Ver. 4.0)

OCTET	FIELD
1 to 5	ATM Header RM-VPC: VCI = 6 and PTI = 110 RM-VCC: PTI = 110
6	RM Protocol Identifier
7	Message Type
8 to 9	ER (Explicit Cell Rate)
10 to 11	CCR (Current Cell Rate)
12 to 13	MCR (Minimum Cell Rate)
14 to 17	QL (Queue Length)
18 to 21	SN (Sequence Number)
22 to 51	Reserved
52 to 53	Reserved (6 bits) + CRC-10

7	6	5	4	3	2	1	0
DIR	BN	CI	NI	RA	Rsv.	Rsv.	Rsv.

Message Type Field

DIR = 0 for forward RM cell
= 1 for backward RM cells
BN = 0 for Source Generated RM cells
= 1 for Switch Generated (BECN) RM cells
CI = 0 otherwise
= 1 to indicate congestion
NI = 0 otherwise
= 1 to indicate no additive increase allowed
RA - Not used for ABR (set to zero)

The threshold values to be used are the same as those in **3.5.1 EFCI**. CI/NI marking control is performed under the following condition:

- The Backward RM cell is identified as follows while the output queue of ABR class of the logical port that has input the Backward RM cell exceeds the EFCI threshold value.

  - PTI = 110 & DIR = 1 (VC switching)
  - VCI = 6 & PTI = 110 & DIR = 1 (VP switching)

Table 3-11. CI Threshold Values Related to Output Queue Length

Threshold Value Name	Control If Threshold Value Is Exceeded (processing during cell input)
OQthACI	Performs CI marking of Backward RM cell input to the corresponding port

3.5.3 RM cell merge (Resource Management Cell Merge)

The μPD98410 performs RM cell merge for a channel set in the multi-cast mode.

In the case of multi-cast, the Backward RM cells are sent from multiple channels to one channel. The μPD98410 has a mechanism that merges the multiple Backward RM cells into one RM cell.

For connection in the backward direction for multi-cast, as many header translation tables (HTTs) as the broadcast count must be set. RMM = 10 (RM cell merge and transfer) must be set for at least one of the connections, and RMM = 11 (RM cell merge and discard) for the other connections. Then the RM cell merge function can be used.

When the Backward RM cell is sent to the channel set in the multi-cast mode, the CI and NI bits that indicate the congestion status of the channel under management of the μPD98410, and the CI and NI bit of the Backward RM cell are ORed, and the cell is discarded. In the case of a channel of RMM = 10, its CI and NI bits and the CI and NI bits of the Backward RM cell are ORed and the result is transmitted from an output port.

Similarly, the BN bit that indicates what created the RM cell (switch or source) of the corresponding channel under management of the μPD98410 is ORed with the BN bit of the Backward RM cell in the case of a channel of RMM = 11, and the cell is discarded. In the case of a channel of RMM = 10, its BN bit and the BN bit of the Backward RM cell are ORed, and the result is transmitted from an output port.

3.6 WFQ (Weighted Fairness Queue)

3.6.1 General

When a cell is output from an output queue, which cell is to be output is determined by the following two conditions:

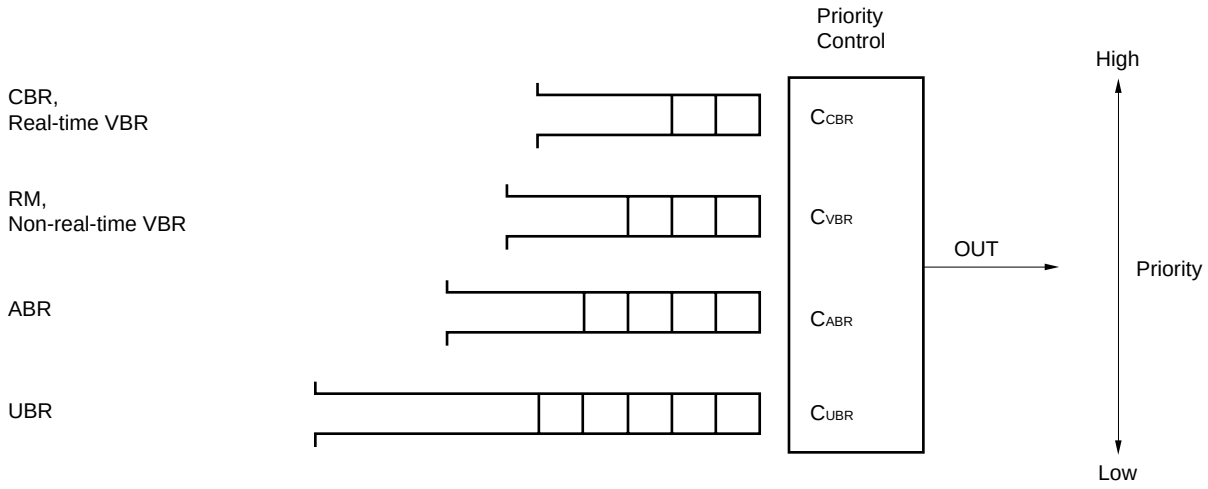
<Output cell determining conditions>

(1) The logical output port to output the cell has been determined.
(2) Of the output queues allocated to the determined logical output port, the service class of the queue from which the cell is taken out has been determined.

Of these conditions, this section explains (2), i.e., how the service class is determined. This method of determination is called the WFQ (Weighted Fairness Queue).

3.6.2 Counters and flags used

Figure 3-41. Output Queue and Counter



The queue of each logical output port of the μPD98410 has the following four queues of service classes.

- Output queue of CBR/rtVBR class
- Output queue of RM/nrtVBR class
- Output queue of ABR class
- Output queue of UBR class

As shown in Figure 3-41, these queues are assigned priorities, and the cells queued are sequentially output to these queues starting from the one with the highest priority. C_{CBR}, C_{VBR}, C_{ABR}, and C_{UBR} are the counters that control these priorities. The initial values of these counters are set as follows:

- C_{CBR}, C_{VBR} ... Number of cells permitted to be output from the corresponding queue in a specific cycle
- C_{ABR}, C_{UBR} ... Ratio of outputting cells of ABR class to cells of UBR class.
  For example, to output cells of ABR class and cells of UBR class at a ratio of 2:1, set C_{ABR} = 2 and C_{UBR} = 1.

C_{CBR}, C_{VBR}, C_{ABR}, and C_{UBR} are set by the class priority control register. In addition, as a counter that counts a specific cycle, a cycle counter is provided.

The differences in setting these counters are due to the differences in the characteristics of the classes. CBR and VBR classes reserve a band, while ABR and UBR classes do not reserve a band but transfer data at the transfer rate that is enabled at a given point. Therefore, C_{ABR} and C_{UBR} only specify a ratio and are not responsible for how many cells are actually output in a specific cycle.

These counters control the priority of each service class according to the following rules:

(1) Cycle counter (8 bits)

- The value 1 is loaded to the counter as the initial value after the counter has been reset.
- The count value of the counter is decremented at every 44 system clocks.
- When the cycle counter register is set, its set value is loaded to the counter.
- When the count value of the counter has reached “1” (time out), the set value of the cycle counter register is loaded to the counter, and the count value is decremented.

(2) C_{CBR} and C_{VBR} (7 bits)

- If the set value (including the initial value) of the class priority control register is changed, the value 127 is loaded to C_{CBR}, and the set value of the class priority control register is loaded to the C_{VBR} counter.
- If congested cells of both CBR and VBR classes exist, the cells of CBR class take precedence and are granted permission to be output. If no congested cells of CBR class exists, the output permission is granted to the cells of VBR class. When cells of CBR and VBR classes are output, the C_{CBR} and C_{VBR} counters are decremented by one.
- When the counter value reaches 0, output from the corresponding service class is prohibited.
- When the count value of the cycle counter reaches “1” (time out), the set value of the class priority control register are added and loaded to the C_{CBR} and C_{VBR} counter.
- If no congestion cells of either CBR and VBR classes exist, or if both the C_{CBR} and C_{VBR} counters reach 0 and output is prohibited, priority control by the C_{ABR} and C_{UBR} counter in (3) is started.

(3) C_{ABR}, C_{UBR} (3 bits)

- The initial value is loaded to these counters when both the counters reach 0, regardless of the cycle counter.
- If congested cells exist in the queues of both ABR and UBR classes, and if both the C_{ABR} and C_{UBR} counters are not 0 (i.e., if output is not prohibited), the two classes are alternately granted output permission. Each time a cell has been output from the corresponding queue, the C_{ABR} and C_{UBR} counters are decremented by one.
- When the value of the counter reaches 0, output from the corresponding service class is prohibited.
  Even if the ABR class has been granted the output permission because the UBR class is prohibited from outputting cells (C_{UBR} = 0), the UBR class is granted the output permission when the ABR class has no congested cells. Similarly, even if the UBR class has been granted the permission because output of the ABR class is prohibited (C_{ABR} = 0), the ABR class is permitted to output cells if the UBR class has no congested cells.
- If both ABR and UBR classes have no congested cells, and if the CBR class has congested cells, the output permission is granted to the CBR class. If the CBR class has no congested cells, and if the VBR class has congested cells, the VBR class is permitted to output the cells.
  After priority control by the C_{ABR} and C_{UBR} counters has been started, priority control by the C_{CBR} and C_{VBR} counters is started again in the following timing:

  (1) Time out of cycle counter if C_{CBR} = 0 and C_{VBR} = 0
  (2) If cells are congested in CBR and VBR classes if $C_{CBR} \neq 0$ or $C_{VBR} \neq 0$

3.7 Peak Rate Shaping Function

The μPD98410 has a simple peak rate shaping function for each logical output port. This shaping function takes effect on the transfer throughput per UTOPIA interface that is determined by SWCLK, and not on the transfer rate of the UTOPIA interface that is determined by UCLK3 through UCLK0.

The transfer throughput per UTOPIA interface and transfer throughput after shaping can be calculated from the value set to SPR of the PT register as follows, with 44 SWCLK as one basic cycle:

- Transfer throughput [bps] = SWCLK frequency [Hz] ÷ 44 [SWCLK] × 53 [octet] × 8 [bits]
- Transfer throughput after shaping [bps] = Transfer throughput [bps] ÷ (SPR + 1)

For example, where SWCLK = 33 MHz and SPR = 3, output is suppressed to once in every 4 basic cycles (SPR + 1 = 4), and the transfer throughput after shaping is 79.5M bps.

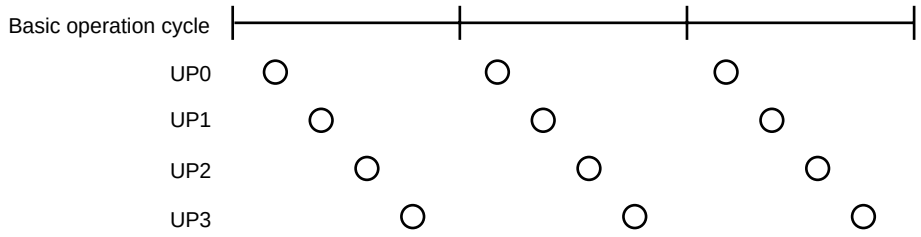
When two or more logical output ports connected to the same UTOPIA interface simultaneously issue a cell transmission request, an output conflict occurs. As a result, the transfer throughput of the logical output port that cannot output data drops. The μPD98410 prevents this drop in transfer throughput by using a shaping error correction function to shorten the next cell transfer interval of the logical output port that could not output data up to 11 basic cycles by the number of basic cycles (N) kept waiting by the output conflict (SPR + 1 – N).

3.7.1 General

(1) UTOPIA interface and logical output port

The μPD98410 has four UTOPIA interfaces conforming to UTOPIA Level2. The relationship between the output enable timing of each UTOPIA interface and the internal basic cycle operation of the μPD98410 is as shown below.

Figure 3-42. Relationship between Internal Basic Cycle and Output Enable Timing of Each UTOPIA Interface



UP0 to UP3: UTOPIA interface 0 to 3

○ : Timing at which output permission is granted to UP0 to UP3

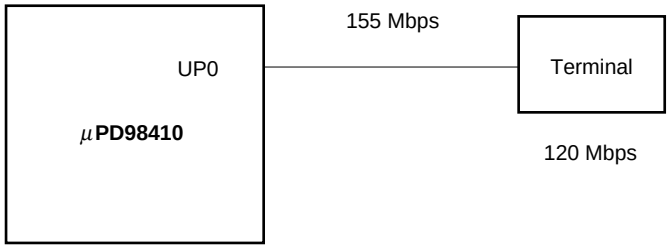
As shown in Figure 3-42, each UTOPIA interface is allocated once in one cycle. Assuming that a cell is always output when each UTOPIA interface is allocated, one UTOPIA interface has a transfer capability of 318M bps (where SWCLK Rate is 33 MHz).

Moreover, the μPD98410 can connect multiple PHY device connection allowing up to 24 logical output ports, and can allocate up to 12 logical output ports to one UTOPIA interface. Because the transfer rate of one UTOPIA interfere is limited by the value described in **3.1 UTOPIA Interface**, however, the total of the transfer rate of the logical output ports allocated to one UTOPIA interface must be equal to or less than this value.

(2) Peak rate shaping function

For example, suppose the μPD98410 and a terminal are connected as shown below.

Figure 3-43. Example of Connection between μPD98410 and Terminal



- Maximum transfer rate of UTOPIA interface of μPD98410: 318M bps
- Circuit rate: 155M bps
- Processing capability of receiver terminal: 120M bps
- Only one logical output port (LP0) is allocated to the UTOPIA interface (UP0).

If the μPD98410 outputs cells at 155M bps at this time, the transfer rate must be lowered to 120M bps at the μPD98410 side because the terminal cannot keep up with this transfer rate. To control the transfer rate in this way, the peak rate shaping function is used.

The peak rate shaping function controls the transfer rate by limiting allocation by the μPD98410 of the UTOPIA interface to logical output ports in each operation cycle of the μPD98410. Because the transfer rate is 318M bps when cells are output in each basic operation cycle, as described in **3.7.1 (1) UTOPIA interface and logical output port**, the UTOPIA interface should be allocated once in three cycles in order to lower the transfer rate to 120M bps.

The details of this control operation are described next.

3.7.2 Details

(1) Shaping rate

To control whether the UTOPIA interface is allocated to logical output ports in each cycle, the following counter and register are provided.

- Ct counter : Counter for shaping rate control
- SPR register: Shaping rate setting register ($0 \leq SPR \leq 255$) ... Limits transfer rate of output to 1/(SPR + 1).

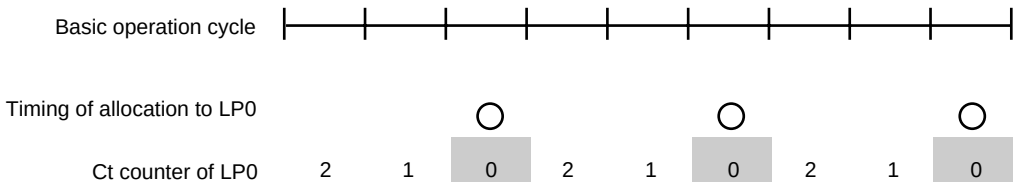
In the example in Figure 3-43, the transfer rate is limited to 1/(1 + 2) if SPR is set to 2. As a result, $318 \times 1/3 = 106$M bps, satisfying the limit of 120M bps. What processing is performed to allocate the UTOPIA interface to a logical output port once in three cycles is explained next.

The Ct counter is μPDated according to the following rules, and the interface is allocated to a logical output port when Ct = 0.

- The initial value (value of SPR) is loaded to the Ct counter as soon as the interface has been allocated to a logical output port.
- The value of the Ct counter is decremented by one if the interface is not allocated to a logical output port ($Ct \neq 0$). The output permission is allocated when Ct = 0.

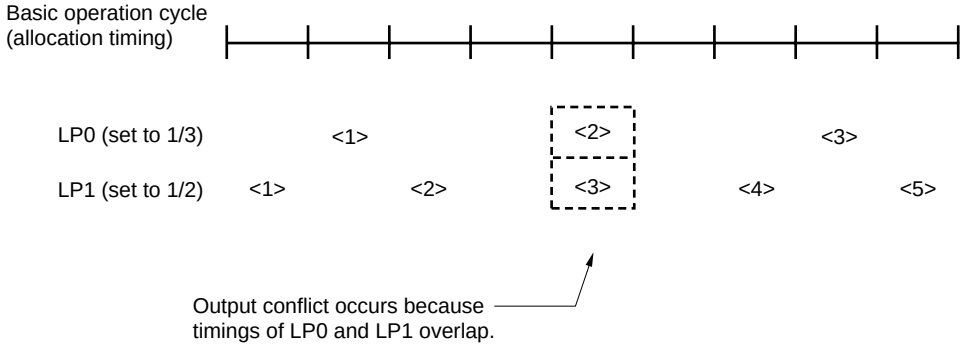
The relationship between the basic cycle, allocation of a logical output port, and the counter value is shown below.

Where SPR = 2 and the initial value of Ct = 2, the transfer rate is limited to 1/(SPR + 1) = 1/3.



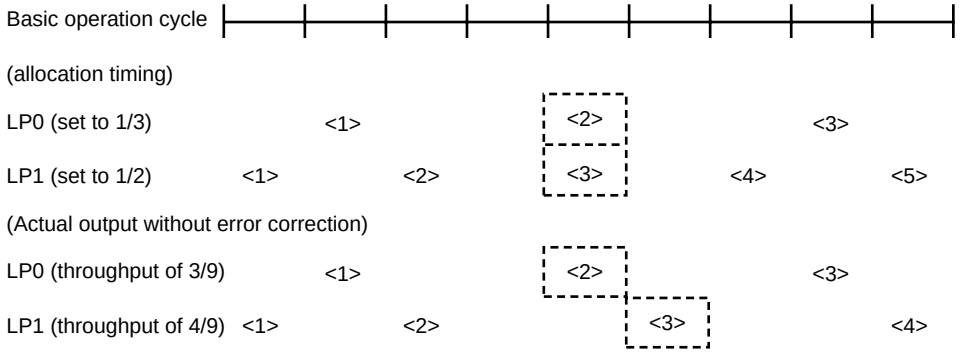
(2) Shaping error correction

If multiple logical output ports LP0 through LPn are connected to one UTOPIA interface, UP0, the timing of allocating the interface to the output ports overlap as shown below (output conflict occurs), dropping the throughput.



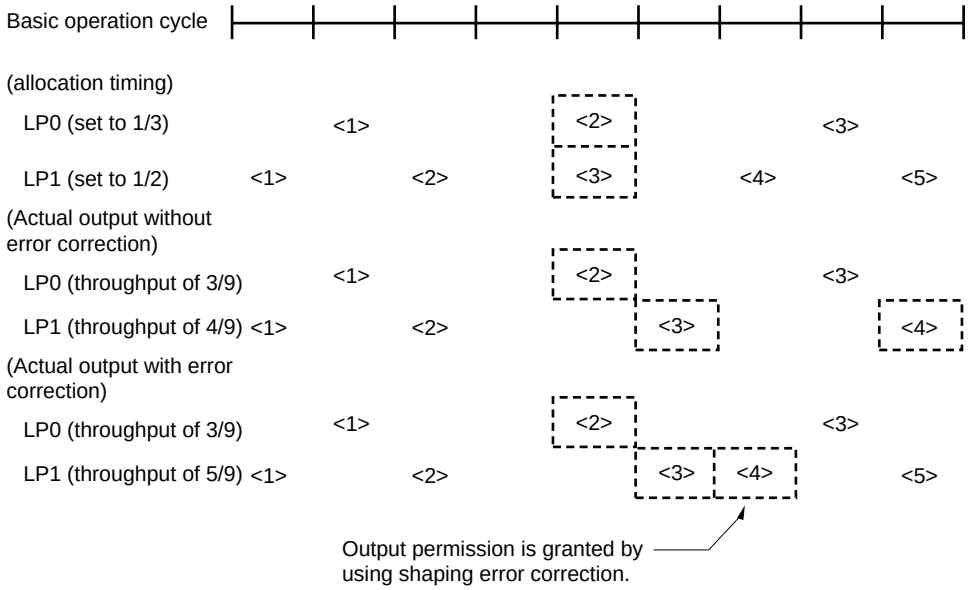
The μPD98410 has a shaping error correction function to prevent the throughput from being dropped by the output conflict. This function is described below.

If the shaping error correction function is not used, the throughput drops as follows:



In the cycle next to the one in which cell <2> is output by LP0 in case of an output conflict, cell <3> is output by LP1 to prevent the conflict. After that, LP1 counts down the basic cycle of SPR + 1, is granted the output permission when Ct = 0, and outputs cell <4>. As a result, the actual throughput drops from the throughput set to LP1 (1/2 $\rightarrow$ 4/9).

This drop in throughput due to the output conflict can be prevented by using the shaping error correction function.
The operation is as follows:



The processing performed to carry out the above control is explained below. First, a new counter, Cs, is used to correct the shaping error.

Cs: Counter to control shaping error correction

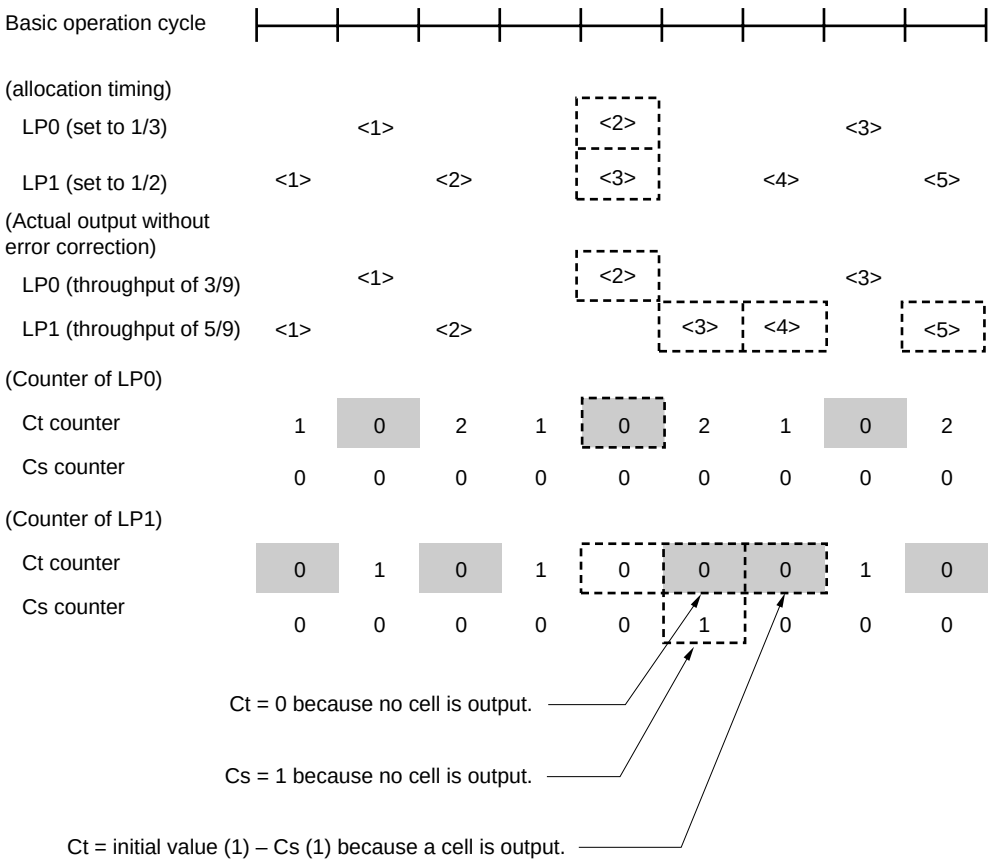
This shaping error correction counter Cs is updated according to the following rule, and the UTOPIA interface is allocated to a logical output port when Ct = 0.

- Cs = 0 if a cell can be output when the interface is allocated to a logical output port (Ct = 0).
- Cs = Cs + 1 if a cell cannot be output when the interface is allocated to a logical output port (Ct = 0), where $0 \leq Cs \leq 11$.

Counter Ct is updated as follows for shaping:

- Ct = Ct – 1 when the interface is not allocated to a logical output port ($Ct \neq 0$).
- If a cell can be output when the interface is allocated to a logical output port (Ct = 0), initial value (SPR) – Cs is loaded to the Ct counter. If no cell can be output even if the interface is allocated to a port, the Ct counter remains 0.

At this time, the counter changes as shown below.



Ct can take 12 values, 0 to 11. The reason for this explained next.

In the examples presented above, LP1 is allocated in the next output cycle. If more logical output ports are connected, however, a conflict with the other logical output ports may occur (at this time, Ct is counted up further and the next cycle is started). Because the μPD98410 allows up to 12 logical output ports to be allocated to one UTOPIA interface, a logical output port can be allocated to the UTOPIA interface at least once if it waits for 12 cycles at most. For this reason, Ct can take 12 values.

3.8 Successive Transmission

Although the UTOPIA Level2 interface can connect multiple PHY devices, a mode must be set for the μPD98410 in accordance with the PHY device to be connected. The following modes are used depending on the PHY device to be connected:

(a) NEC's 155M bps PHY "μPD98404 (P30)" → Successive output mode & multi-PHY mode
(b) PHY of more than 1/3 of UTOPIA transfer rate → Single PHY mode
(c) PHY of less than 1/3 of UTOPIA transfer rate → Non-successive output mode & multi-PHY mode

If the μPD98410 is set in the non-successive output mode and multi-PHY mode, successive cells are not output to the same PHY device. Consequently, the maximum transfer rate that can be guaranteed per PHY device is 1/3 of the UTOPIA interface's transfer rate.

To connect a circuit with a transfer rate more than 1/3 of the UTOPIA interface, either connect the "μPD98404" that can successively output cells from the μPD98410, or connect only one PHY device to one UTOPIA interface.

Table 3-12. PHY Device Connected and Mode Setting of μPD98410

Polling Mode Setting		Connectable PHY Device	Transfer Rate per PHY Device	Cell Output to Same PHY Device
Transfer PHY polling	Single/multi-polling[Note 1]			
Possible	Single/multi	NEC's "μPD98404 (P30)"	Upper limit of PHY device	Can be output successively
Impossible	Single	Different vendor's PHY devices (including NEC's "μPD98402A (P15)")	Upper limit of PHY device	Can be output successively
Impossible	Multi[Note 2]		Upper limit of PHY device but less than 1/3 of UTOPIA transfer rate	Cannot be output successively

Notes 1. In the multi-PHY mode, connection of multiple PHY devices is supported, including connection of one PHY device.

2. The multi-PHY mode is set after reset.

Cells are not output to the same PHY device because polling is performed again after it has been performed once and before a cell is output, and two cells must be stored in the output FIFO. If the PHY device is ready to receive one cell, it returns a Cell Available signal. However, the second cell may not be correctly received and cell loss may occur.

The μPD98410 therefore does not successively output cells to such a PHY device.

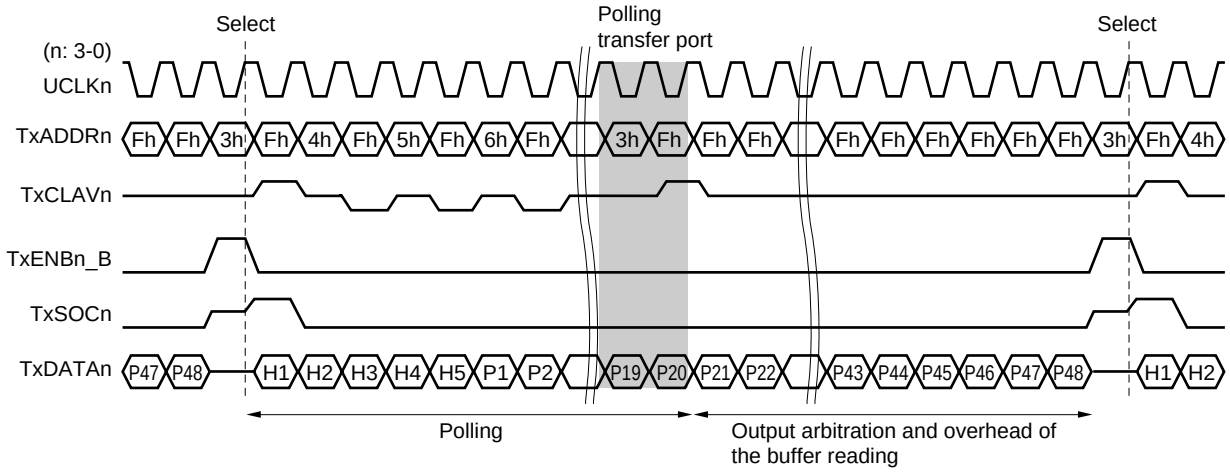
(a) Successive output mode & multi-PHY mode (NEC's 155M bps "μPD98404")

In this mode, the maximum transfer rate per PHY device is equivalent to the transfer rate of the UTOPIA interface. However, because polling is performed at a timing different from that of the UTOPIA Level2 interface, only a PHY device with the timing matching this timing can be connected. The successive output mode is valid even if a PHY device in the non-successive output mode (a PHY device of the other maker) exists on the same UTOPIA interface.

If the successive mode (PT register RP = "1") and multi-PHY mode are set, the μPD98410 polls the PHY device that is transferring a cell to determine whether the device can receive the next cell when P19 (payload 19) is transferred. Because NEC's 155M bps PHY "μPD98404" has a mode in which the correct result is returned in response to this polling, it can successively output cells to the μPD98410.

Do not set the PHY devices of the other manufacturers in the successive output mode because cell loss may occur on the UTOPIA interface. Setting the successive output mode is different from setting of peak rate shaping.

Figure 3-44. Polling Timing (a)



When setting the successive output mode, it is all right to set the multi-PHY mode even when only one PHY device is connected. If the single PHY mode is set, polling is performed in the single PHY mode.

If two or more PHY devices are connected to the same UTOPIA interface, the μPD98410 cannot reflect the result of polling that is carried out when P45 (payload 45) is transferred to the PHY device that is transferring a cell on the next cell transfer. By performing polling when P19 is transferred, however, output is arbitrated based on the result of the polling, the overhead to read the cell buffer is absorbed, and successive output is carried out.

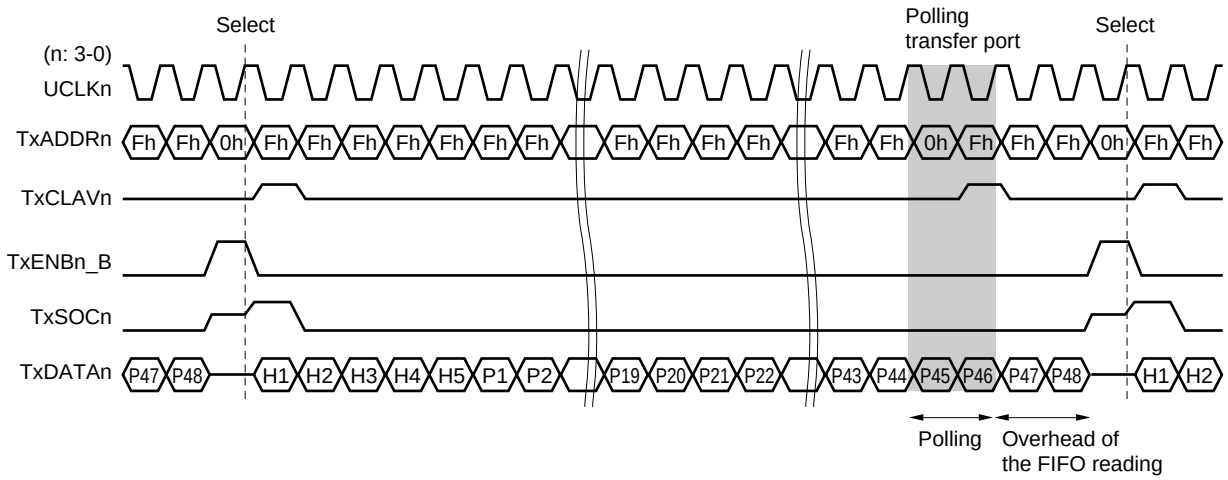
(b) Single PHY mode (PHY device of more than 1/3 of UTOPIA transfer rate)

In this mode, the maximum transfer rate per PHY device is equivalent to the transfer rate of the UTOPIA interface. This mode is used when a PHY device with a transfer rate of more than 1/3 of the UTOPIA interface is connected. However, only one PHY device can be connected to one UTOPIA interface.

When the single PHY mode (PT register SG = "1") is set, the μPD98410 polls the PHY device that is transferring a cell whether the device can receive the next cell when P45 (payload 45) is transferred. The μPD98410 does not poll the other PHY devices.

If only one PHY device is connected to the UTOPIA interface, no head of line blocking occurs. Therefore, cells can be successively transferred between the PHY device and μPD98410 in this mode.

Figure 3-45. Polling Timing (b)



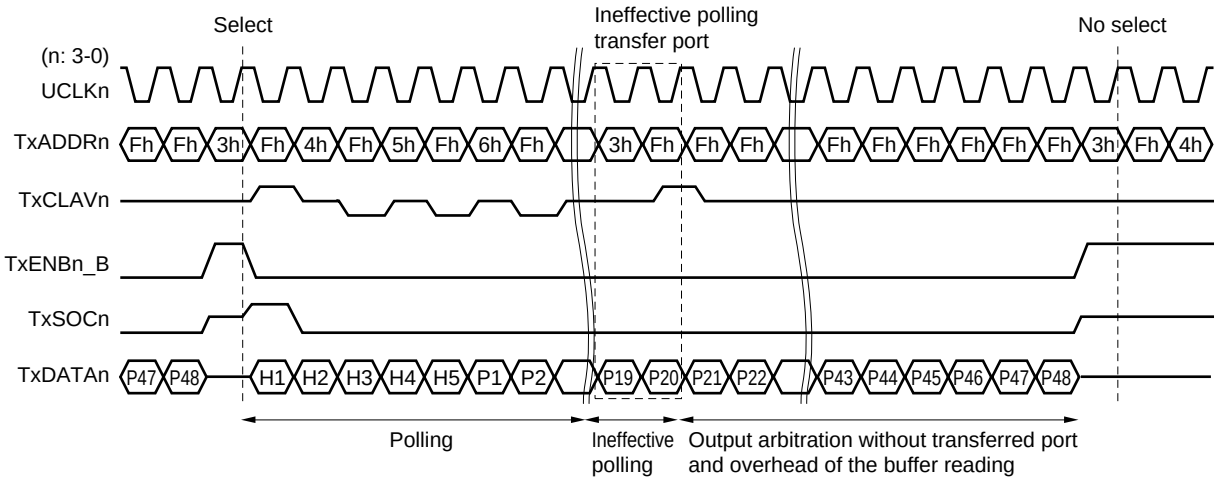
The PHY device that is transferring a cell is polled when P45 (payload 45) is transferred, and transfer of the next cell that is stored in the output FIFO is controlled, and the cell is read from the cell buffer and stored in the output FIFO.

(c) Non-successive output mode & multi-PHY mode (PHY device of less than 1/3 of UTOPIA transfer rate)

In this mode, the maximum transfer rate that can be guaranteed per PHY device is 1/3 of the UTOPIA interface's transfer rate. This mode is used to connect a PHY device with a transfer rate of 1/3 of the UTOPIA interface. The non-successive output mode is valid even when a PHY device in the successive output mode (such as NEC's PHY device) exists on the same UTOPIA interface.

If the non-successive output mode (PT register RP = "0") and multi-PHY mode are set, the μPD98410 does not reflect the result of polling made when P19 (payload 19) is transferred to the PHY device that is transferring a cell on the output arbitration. Consequently, the maximum transfer rate per PHY device is limited. However, the transfer rate of the PHY device can be satisfied on the condition that a PHY device with a transfer rate 1/3 of the UTOPIA interface is connected.

Figure 3-46. Polling Timing (c)



3.9 Interrupt Request

This section explains the interrupt requests made by the μPD98410 to the microprocessor.

3.9.1 Parity error

The μPD98410 checks the HTT & control memory and cell buffer for parity error. If a parity error is detected, the μPD98410 issues an interrupt request to the microprocessor.

Even if the parity error is detected, the μPD98410 continues operation. However, the subsequent header translation and switching operation are not guaranteed. Therefore, the microprocessor must reset the μPD98410 immediately.

(a) HTT & control memory

One parity bit is generated and checked for every 8 bits of 32-bit data.

(b) Cell buffer

One parity byte is generated and checked for 54 bytes of stored cells (storage header: 6 bytes, payload: 48 bytes).

3.9.2 Input port overrun

The μPD98410 inputs cells in accordance with the UTOPIA Level2 interface. If the internal input FIFO of the μPD98410 overruns, the μPD98410 stores the status of the UTOPIA reception interface port in question in a monitor register (ERINOV register), and issues an interrupt request to the microprocessor.

If an input port overrun is detected, cell loss occurs, but the switching operation of the other UTOPIA reception interfaces continue. If the relationship between the UTOPIA clock and system clock does not satisfy the condition explained in **3.1 UTOPIA Interface**, the input FIFO overruns.

3.9.3 Queue pointer error

The μPD98410 organizes a queue that manages the cell buffer in the control memory as described in **3.4 Queue Control**, and issues an interrupt request to the microprocessor when malfunctioning of the internal queue control block of the μPD98410 is detected.

If a queue pointer error is detected, the QE bit of the status register indicates the error, and the subsequent header translation and switching operation are not guaranteed.

If no error is indicated by the CE bit of the status register, and an error is indicated only by the QE bit, the possible causes are as follows. Check the setting of the μPD98410.

- The initial value of the ALLmin register is not the value calculated by the following expression.
  (OQminCRV + OQminRNV + OQminABR + OQminUBR) × enabled ports[Note] + MQminCRV + MQminRNV + MQminABR + MQminUBR + TCminCRV + TCminRNV + TCminABR + TCminUBR
- The ALLmin register is re-set after the switching operation of the CMD register is enabled.
- Each minimum threshold value register is re-set after the switching operation of the CMD register is enabled.
- The test area is rewritten by an I/O register access.

Note “enabled ports” indicates the total number of logical ports that are scheduled to enable the EN bit of the PT register.

3.9.4 Cast count error

The μPD98410 issues an interrupt request to the microprocessor if it detects malfunctioning of the idle queue management block or the multi-cast count management block.

If a cast count error is detected, it is indicated by the CE bit of the status register, and the subsequent header translation and switching operation cannot be guaranteed. A possible cause of this is the user's software procedure. Check the setting of the μPD98410.

If an error is indicated by the CE and QE bits of the status register, the following causes are possible. Check the setting of the μPD98410.

- The broadcast count of the HTT area A does not match the broadcast count set by the bit map of HTT area B.
- The cell buffer memory is rewritten by mistake because the HC bit of the mode register is not disabled after self-diagnosis of the cell buffer memory has been completed.
- The test area is rewritten by an I/O register access.

3.9.5 Cell buffer memory shortage

With the μPD98410, the area of the cell buffer memory that stores cell data runs short if the percentage of multi-cast is too high. If the shortage occurs, cells are not stored. Therefore, cells are discarded and discarded cells are counted, and an interrupt request is issued to the microprocessor.

Even if the cell buffer memory has run short, if enough area becomes available in the cell buffer memory, normal operation is restored and the switching operation continues. If the average broadcast count of all the congested cells is greater than 2, the cell buffer memory shortage may take place.

3.9.6 Control memory shortage

As described in **3.4 Queue Control**, the μPD98410 organizes a queue for cell buffer management in the control memory. If the percentage of multi-cast is too high, the control memory may run short before the cell buffer. Should this happen, cells are not stored. Consequently, cells are discarded and discarded cells are counted, and an interrupt request is issued to the microprocessor.

Even if the cell control memory has run short, if enough area becomes available in the control memory, the normal operation is restored and the switching operation continues. If the average broadcast count of all the congested cells is greater than 2, the control memory shortage may take place.

3.9.7 HEC/CRC error

The μPD98410 performs an HEC check and CRC-10 check on input cells. If HM of the MODE register is set to 1, however, HEC check is not performed and HEC error cells pass. If an HEC error/CRC-10 error is detected, the corresponding cell is discarded, the corresponding logical input port number is stored in the monitor register, and an interrupt request is issued to the microprocessor. The microprocessor reads the cause register (ERHEC register) and determines the logical input port of the cell responsible for the HEC error/CRC-10 error.

Even if an HEC error/CRC-10 error is detected, the switching operation for the other cells continues.

(a) HEC check error (header error check)

The μPD98410 performs an HEC check on input cells and HEC generation for output cells.

(b) RM cell CRC-10 error

The μPD98410 performs a CRC-10 check if it detects that the input cell is an RM cell having PID = 01h. It also performs CRC-10 generation for an output cell to rewrite the value of the payload if the cell is a Backward RM cell having PID = 01h.

3.9.8 Header translation error

If the μPD98410 detects a header translation error as a result of accessing the header translation table (HTT) by an input cell, it discards the corresponding cell, stores the logical input port number in the monitor register (ERHT) register, and issues an interrupt request to the microprocessor.

Even if a header translation error occurs, the switching operation for the other cells continue.

(a) Invalid header translation

If an attempt is made to access HTT, exceeding the HTT area allocated to the corresponding port, a header translation error occurs. This happens if it is detected that the invalid block of VPI and VCI of the input cell is not "0". However, in the case of a channel set for connection of UNI by the HT0 through HT23 registers, the GFC field (4 bits) of the input cell is treated as "don't care".

(b) Invalid channel

If it is detected that the corresponding channel is set invalid (CEN = 0) as a result of an HTT access, a header translation error occurs.

(c) Invalid output port

If it is detected that the corresponding output port is set invalid (PT register EN = 0) when an attempt is made to output a cell to the logical output port obtained as a result of an HTT access, a header translation error occurs.

(d) Invalid multi-cast

If it is detected that broadcast count (NMP) = 0 or Multicast Bitmap = 0 as a result of an HTT access, despite the fact that multi-cast (CM = 1) is set, a header translation error occurs.

(e) Invalid RM cell merge

If it is detected that a channel is set invalid (CEN = 0) or single cast (CM = 0) as a result of an HTT access of the channel at the output destination when backward RM cells are merged, a header translation error occurs.

3.9.9 Exceeding buffer threshold value

If cells are congested in the cell buffer exceeding each threshold value, the μPD98410 selects and discards the corresponding input cells by means of priority cell discard control and EPD control, stores the type and class of the corresponding threshold value, and the logical output port number in the monitor register (EXTH register), and issues an interrupt request to the microprocessor.

Even when a cell is discarded, the switching operation for the other cells continues.

3.9.10 Count over detection

The μPD98410 issues an interrupt request to the microprocessor when it detects an overflow ("count over") in the following counters. If a count over is detected, the counters are reset to 0 and continue counting.

- Control/cell buffer memory shortage discard cell counter
- HEC/CRC error discard cell counter
- Header translation error discard cell counter
- Threshold value excess discard cell counter
- Reception cell counter

3.10 Monitoring

3.10.1 Monitor register

The μPD98410 stores the numbers of ports responsible for errors (except for parity errors) in the monitor registers. A value valid when an error occurs is stored in each register. The values of these registers do not change until the microprocessor clears the status bits.

The following information is stored in the monitor registers.

- Type and class of threshold value that is exceeded, and logical output port number
- Number of the logical input port that input a cell in which a header translation error was detected
- Number of the logical port that input a cell in which an HEC error or CRC-10 error was detected
- Number of the port of the UTOPIA interface in which an input port overrun error was detected

3.10.2 Cell discard count due to exceeded threshold value

The μPD98410 selects and discards an input cell by means of priority cell discard control and EPD control if cells are congested in the cell buffer, exceeding each threshold value. It can monitor the number of discarded cells over any period under any conditions.

(a) Monitor condition

The following conditions can be assigned to registers.

- Specification of threshold value : MAX. threshold value/CLP threshold value/EPD threshold value
- Class specification : CBR/rtVBR/RM/nrtVBR/ABR/UBR
- Port number : Specification of logical output port number

(b) Monitor period

Counting is started when the count enable (EN) bit is set to “1”, and is stopped when EN is reset to “0”.

(c) Indication of number of discarded cells

The number of discarded cells is indicated by the number of discarded cells register when monitoring is completed. If the maximum count is reached and then a new cell is discarded, the counter is reset to 0, and continues counting. In this case, the status register indicates that the cell discard counter overflowed.

- Maximum count : FFFFFFFFh ($2^{32} – 1$)

3.10.3 Cell discard count due to header translation error

The μPD98410 discards cells when a header translation error occurs for an input cell. It can monitor the number of discarded cells over any period under any logical input port conditions.

(a) Monitor condition

The following conditions can be assigned to a register.

- Port number: Specification of logical input port number

(b) Monitor period

Counting is started when the count enable (EN) bit is set to “1”, and is stopped when EN is reset to “0”.

(c) Indication of number of discarded cells

The number of discarded cells is indicated by the number of discarded cells register when monitoring is completed. If the maximum count is reached and then a new cell is discarded, the counter is reset to 0, and continues counting. In this case, the status register indicates that the cell discard counter overflowed.

- Maximum count: FFFFFFFFh ($2^{32} – 1$)

3.10.4 Cell discard count due to HEC error or CRC error

The μPD98410 discards cells when an HEC error or CRC error occurs. It can monitor the number of discarded cells over any period under any logical input port conditions.

(a) Monitor condition

The following condition can be assigned to a register.

- Port number: Specification of logical input port number

(b) Monitor period

Counting is started when the count enable (EN) bit is set to “1”, and is stopped when EN is reset to “0”.

(c) Indication of number of discarded cells

The number of discarded cells is indicated by the number of discarded cells register when monitoring is completed. If the maximum count is reached and then a new cell is discarded, the counter is reset to 0, and continues counting. In this case, the status register indicates that the cell discard counter overflowed.

- Maximum count: FFFFFFFFh ($2^{32} – 1$)

Caution The cell discard count due to HEC errors is not counted if it is specified by the MODE register that cells causing an HEC error should be passed.

3.10.5 Cell discard count due to control/cell buffer memory shortage

The μPD98410 discards cells if the vacant control area of the HTT & control memory or vacant area of the cell buffer memory runs short. It can monitor the number of discarded cells over any period under any logical input port conditions.

(a) Monitor condition

The following condition can be assigned to a register.

- Cause of error: Control/cell buffer memory shortage

(b) Monitor period

Counting is started when the count enable (EN) bit is set to “1”, and is stopped when EN is reset to “0”.

(c) Indication of number of discarded cells

The number of discarded cells is indicated by the number of discarded cells register when monitoring is completed. If the maximum count is reached and then a new cell is discarded, the status register is updated, the counter is reset to 0, and continues counting. In this case, the status register indicates that the cell discard counter overflowed.

- Maximum count: FFFFFFFFh ($2^{32} – 1$)

3.10.6 Counting number of received cells

The μPD98410 can monitor the number of cells received by the UTOPIA interface port over any period.

(a) Monitor condition

The following condition can be assigned to a register.

- UTOPIA interface port number: UTOPIA0/1/2/3

(b) Monitor period

Counting is started when the count enable (EN) bit is set to “1”, and is stopped when EN is reset to “0”.

(c) Indication of number of received cells

The number of received cells is indicated by the number of input cells register when monitoring is completed. If the maximum count is reached and then a new cell is received, the counter is reset to 0, and continues counting. In this case, the status register indicates that the cell input counter overflowed.

- Maximum count: FFFFFFFFh ($2^{32} – 1$)

3.11 Microprocessor Interface

The microprocessor can access the HTT & control memory and cell buffer memory via the μPD98410, in addition to the internal I/O registers of the μPD98410.

- I/O registers : Initial setting, command issuance, status check, etc.
- HTT & control memory : Initial setting, connection setting to HTT, self-diagnosis
- Cell buffer memory : Self-diagnosis

The μPD98410 supports two interfaces for connecting a microprocessor: 32-bit multiplexed synchronous bus and 16-bit separated asynchronous bus. These buses are general-purpose bus interfaces that require fewer external circuitry than ordinary I/O buses (PCI Bus, S Bus, A Bus, AP Bus, and 86 Bus).

The interface with the microprocessor is determined as follows, depending on the status of the HSEL input pin at hardware reset.

Table 3-13. Microprocessor Interface Pin

HSEL = Low 32-bit Multiplexed Synchronous Bus	HSEL = High 16-bit Separated Asynchronous Bus
HCLK (Processor bus clock)	Pull up or pull down
R/W_B (Read/Write mode)	WR_B (Write strobe)
UWE_B (Upper word enable)	RD_B (Read strobe)
AD [31:16] (Address/Data bus)	A[15] (Pull up or pull down) A[14:0] (Address bus)
AD [15:0] (Address/Data bus)	D[15:0] (Data bus)
IOCS_B (I/O chip select)	
MCS_B (Memory chip select)	
INT (Interrupt request)	
RDY_B (Bus ready)	RDY (Bus ready)

3.11.1 I/O mapping and memory mapping

When IOCS_B is asserted active, the I/O registers are selected. When MCS_B is asserted active, the external memory is selected. Either the HTT & control memory or cell buffer memory is selected as the external memory by the HC bit of the memory mode register.

Table 3-14. Selecting Subject to Access

IOCS_B Pin	MCS_B Pin	HC Bit of Memory Mode Register	Subject to Access	Offset Address	
				32-bit bus	16-bit bus
1	1	Don't care	None	—	—
0	1	Don't care	I/O register	0000h - 7FFFh	0000h - 7FFFh
1	0	1	HTT & control memory	000000h - 0FFFFFh	0000h - 7FFFh[Note]
		0	Cell buffer memory	000000h - 3FFFFFh	0000h - 7FFFh[Note]
0	0	Don't care	None	—	—

Note With the 16-bit separated asynchronous bus, the external memory space is mapped via memory bank register.

The microprocessor can access the μPD98410 in 16-bit or 32-bit units. However, it can write data to the cell buffer memory only in 88-bit units. The data written by the processor to the cell buffer memory is temporarily stored in the temporary internal register of the μPD98410, and written to the cell buffer in 88-bit units as soon as CB[15:0] or CB[31:0] has been written. Therefore, be sure to write data of 1 word or 88 bits to the cell buffer and write CB[15:0] or CB[31:0] last.

Table 3-15. Access Bit Width for Each Access Type

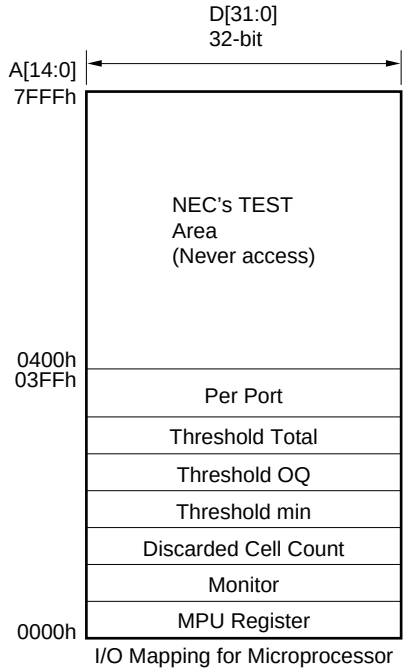
Access Type	Read Operation	Write Operation
I/O register	16/32 bits	16/32 bits
HTT & control register	16/32 bits	16/32 bits
Cell buffer memory	16/32 bits	88 bits

To write data to address CBA[17:0] = 00000h in 32-bit units, write AD[21:0] = 000008h, 000004h, and 000000h in that order. If big endian is specified, write address 000002h last in 16-bit units.

Write data "0" to the unused area provided for future expansion. This area should be undefined when read.

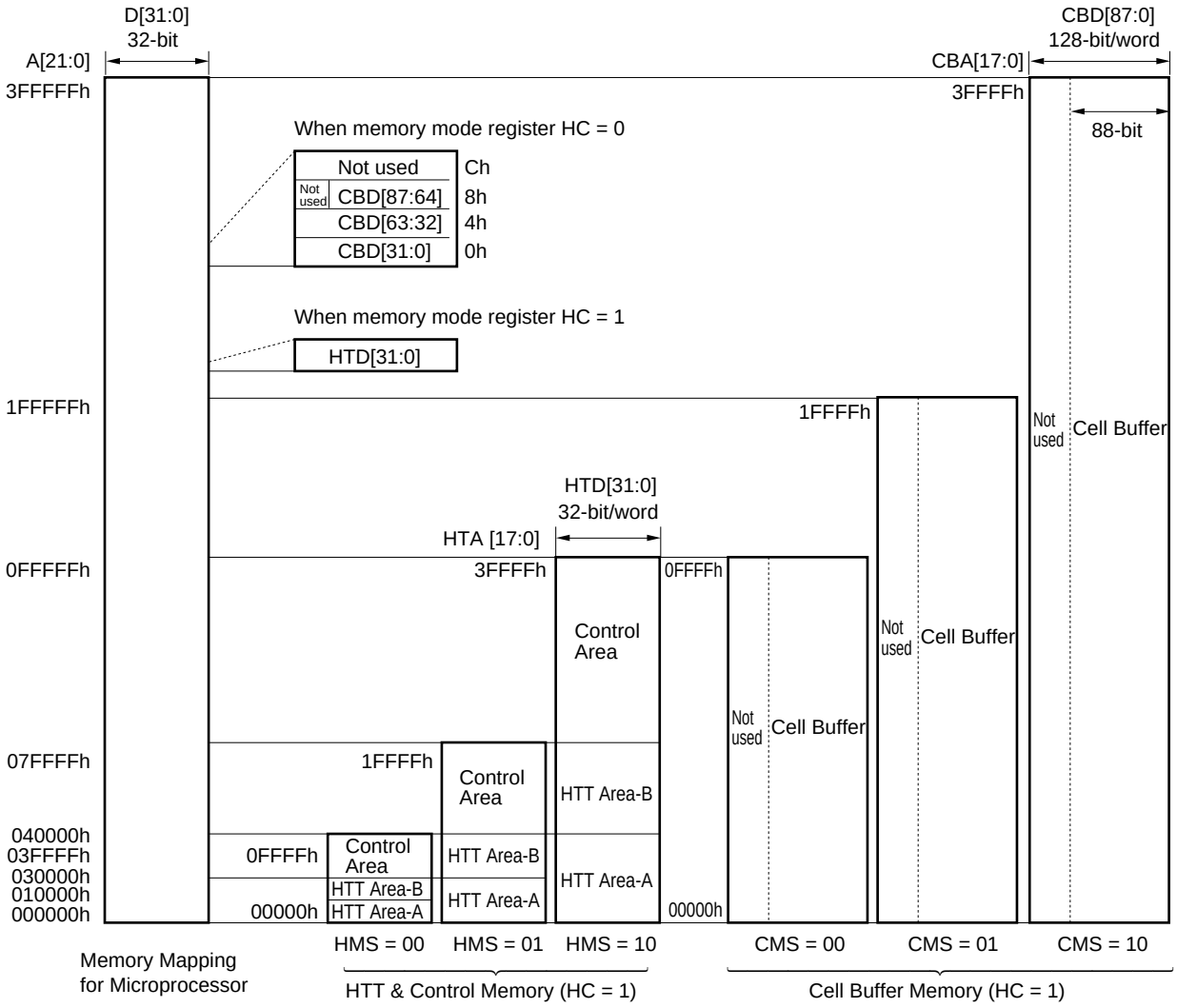
Caution Do not access the μPD98410 in 8-bit units. If data is written in 8-bit units or 24-bit units, the undefined status on the data bus lines that are not driven is written to the remaining 8 bits of a word pair, and the operation is not guaranteed.

Figure 3-47. I/O Register Mapping



I/O Mapping for Microprocessor

Figure 3-48. HTT & Control Memory and Cell Buffer Memory Mapping



3.11.2 32-bit multiplexed synchronous bus (HSEL = Low)

If the HSEL input pin is low at hardware reset, the 32-bit multiplexed synchronous bus is selected as the bus interface.

(1) Endian

The microprocessor bus is set to little endian as the default condition after reset. To connect a microprocessor with a big endian interface, set the BL bit of the memory read register to "1".

The μPD98410 controls access by using AD1 (address) and UWE_B as follows. To UWE_B, a negative logic high-order word valid signal or a negative logic 4-byte valid signal can be connected.

(a) Little endian access (BL = "0")

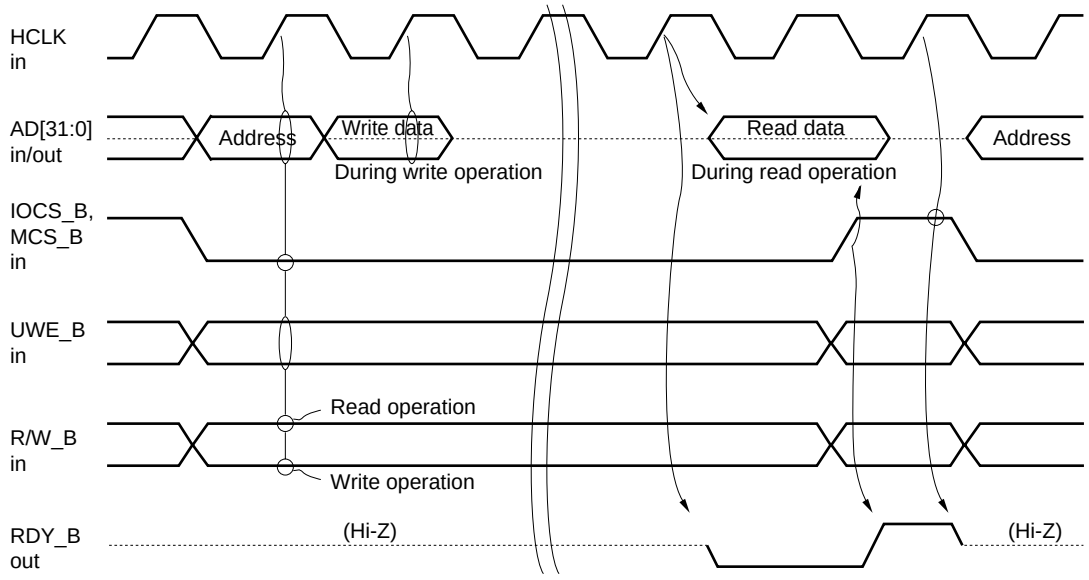
Address	UWE_B	Data	
AD1		AD [31:16]	AD [15:0]
0	0	bit [31:16]	bit [15:0]
0	1	Invalid	bit [15:0]
1	0	bit [31:16]	Invalid
1	1	bit [31:16]	Invalid

(b) Big endian access (BL = "1")

Address	UWE_B	Data	
AD1		AD [31:16]	AD [15:0]
0	0	bit [31:16]	bit [15:0]
0	1	bit [31:16]	Invalid
1	0	Invalid	bit [15:0]
1	1	Invalid	bit [15:0]

(2) Access timing

Figure 3-49. Access Timing of 32-Bit Multiplexed Synchronous Bus



When IOCS_B or MCS_B is asserted, AD[31:0], UWE_B, and R/W_B are loaded in synchronization with the rising of HCLK, and the register or memory at the address indicated by AD[31:0] is accessed.

If R/W_B is high, a read operation is started. When data output is ready, the data is output to AD[31:0] in synchronization with the rising of HCLK, and RDY_B is asserted. When the microprocessor has received the data and negates IOCS_B and MCS_B, the μPD98410 immediately negates RDY_B, and AD[31:0] go into a high-impedance state. At the next rising of HCLK, RDY_B goes in to a high-impedance state.

If R/W_B is low, a write operation is started. The data on AD[31:0] is loaded in synchronization with the next rising of HCLK, and RDY_B is asserted when the operation in the next bus cycle is ready. When the microprocessor negates IOCS_B and MCS_B, the μPD98410 immediately negates RDY_B, and RDY_B goes into a high-impedance state at the next rising of HCLK.

3.11.3 16-bit separated asynchronous bus (HSEL = High)

If the HSEL input pin is high at hardware reset, the 16-bit separated asynchronous bus is selected as the bus interface.

(1) Endian

The microprocessor bus is set to little endian as the default condition after reset. To connect a microprocessor with a big endian interface, set the BL bit of the mode register to “1” to access in 32-bit units and with big endian interface, though the default condition can be used as is.

The μPD98410 controls access by using A1 (address).

(a) Little endian access (BL = “0”)

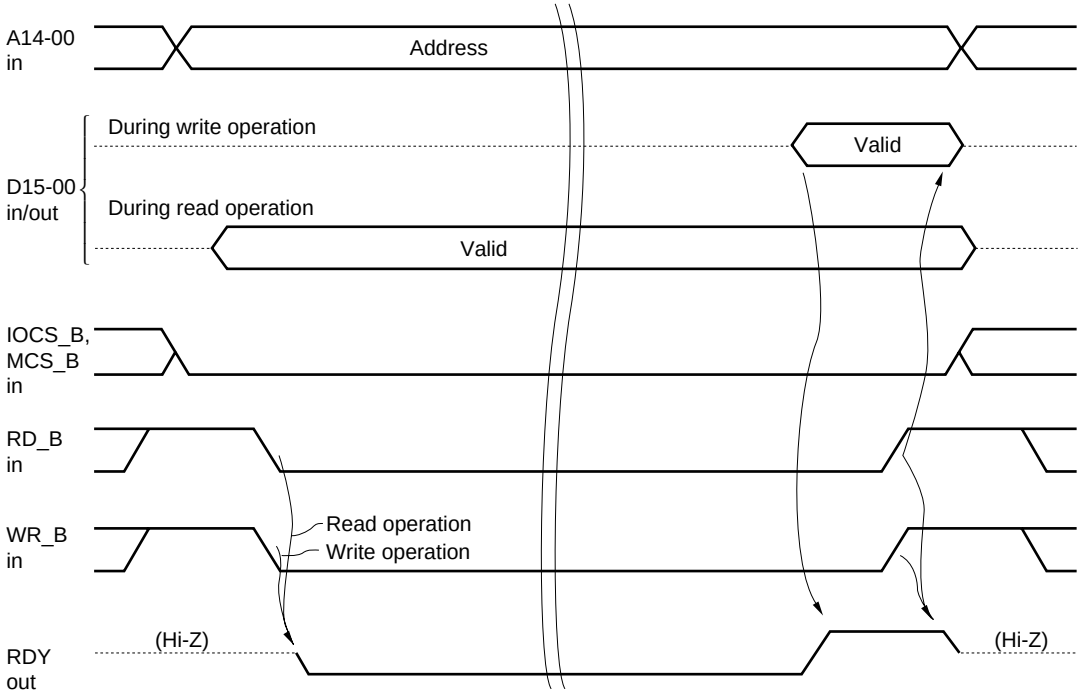
Address	Data
A1	D [15:0]
0	bit [15:0]
1	bit [31:16]

(b) Big endian access (BL = “1”)

Address	Data
A1	D [15:0]
0	bit [31:16]
1	bit [15:0]

(2) Access timing

Figure 3-50. Access Timing of 16-Bit Separated Asynchronous Bus



If RD_B or WR_B is asserted when IOCS_B or MCS_B is asserted, RDY is immediately negated and the register or memory at the address indicated by A[14:0] is accessed.

If RD_B is asserted, a read operation is started. When data output is ready, the data is output to D[15:0], and RDY is asserted. When the microprocessor receives the data and negates IOCS_B and MCS_B, the μPD98410 immediately makes RDY and D[15:0] go into a high-impedance state.

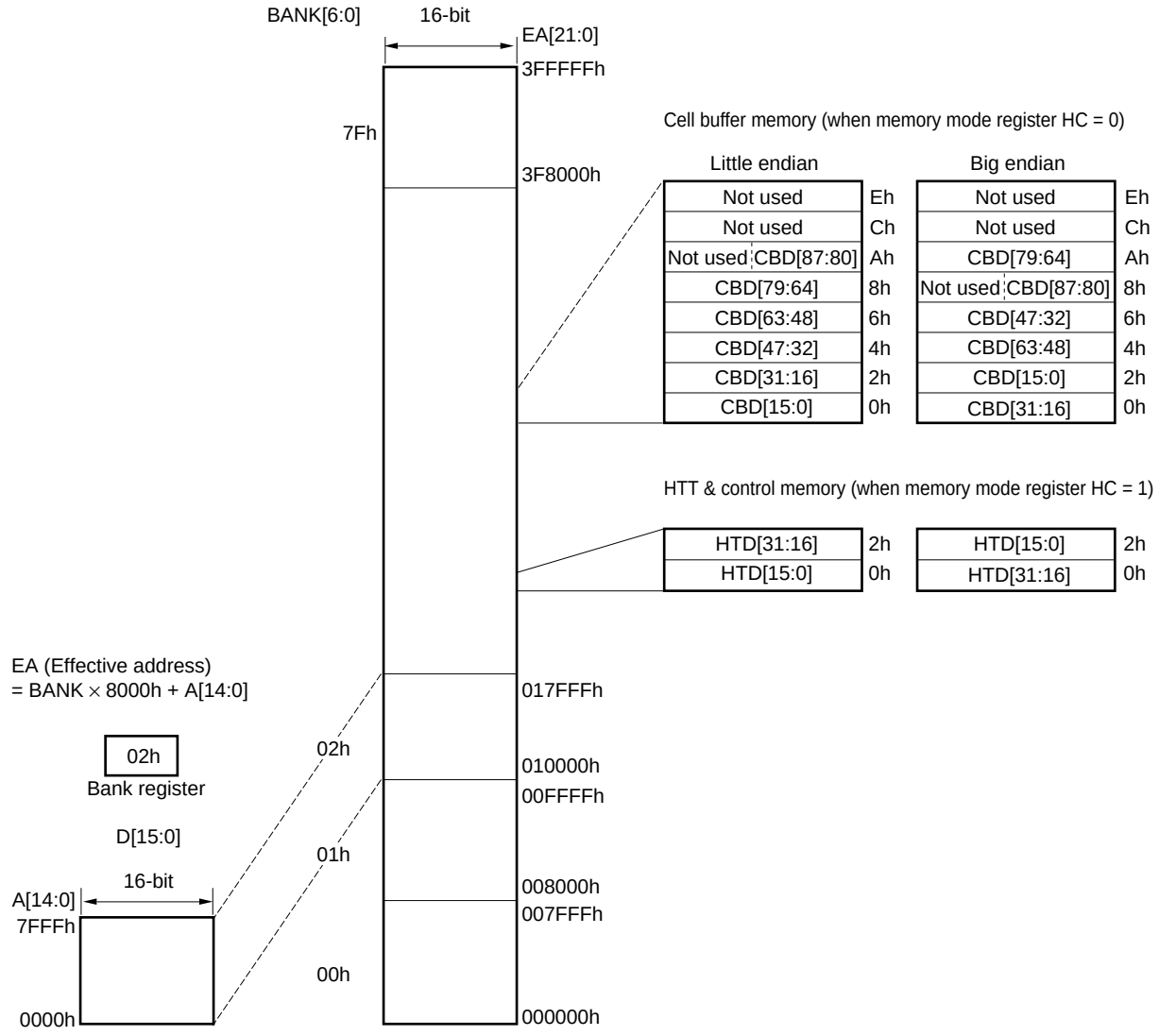
If WR_B is asserted, a write operation is started. When the data on D[31:0] is loaded and the operation in the next bus cycle is enabled, RDY is asserted. When the microprocessor negates IOCS_B and MCS_B, the μPD98410 immediately makes RDY go into a high-impedance state.

Caution Do not assert RD_B and WR_B at the same time.

(3) Bank register

The 16-bit separated asynchronous bus access an area of the external memory by using the BANK register.

Figure 3-51. Memory Map of 16-Bit Separated Asynchronous Bus



Memory Mapping for Microprocessor

3.12 External Memory Interface

3.12.1 HTT & control memory interface

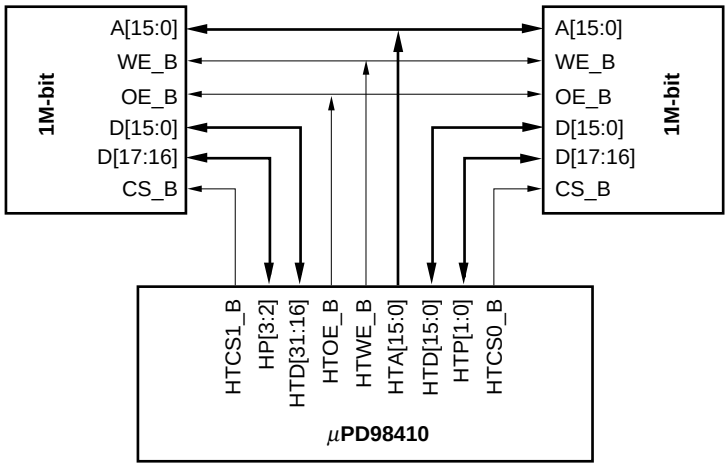
A memory with 1 word being 36 bits wide (32 bits + 4-bit parity) and a depth of 64K words is connected as the HTT & control memory. This memory can be expanded along with the cell buffer, and 128K word and 256K word memories can be connected. This memory stores the HTT (Header Translation Table) and cell addresses (idle queue/output queue/multi-cast queue).

The μPD98410 translates headers by using the HTT. It accesses the HTT for inputting cells, multi-cast re-queuing, and outputting cells. The HTT must be created by the microprocessor in accordance with a predetermined format.

Caution The microprocessor can always access the HTT even while the μPD98410 is performing a switching operation, but a wait signal of up to 16 system clocks is inserted, until access by the microprocessor is enabled.

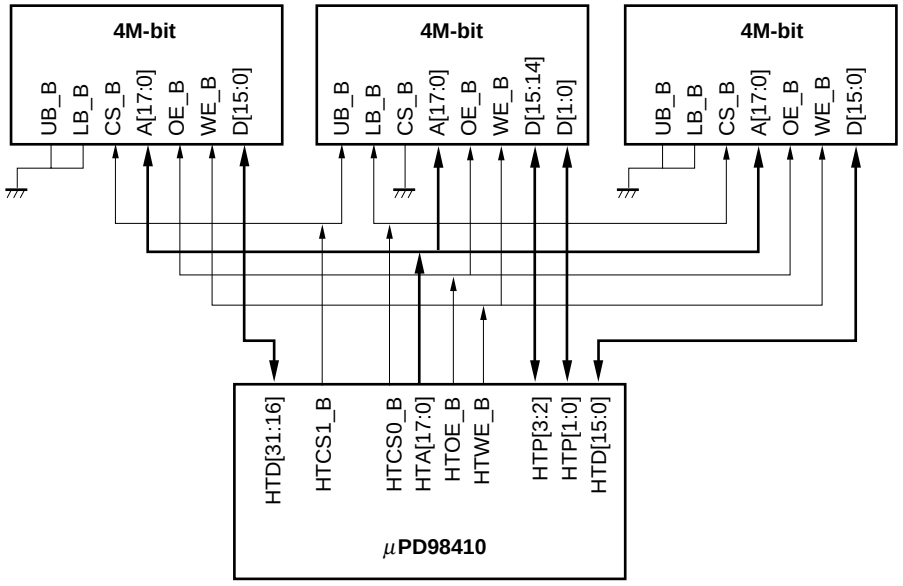
Because the microprocessor runs memory diagnostics as necessary after reset, the memory can be accessed. After running the memory diagnostics, the HTT & control memory must be selected by setting the HC bit of the MODE register to “1”. While the switching operation is enabled, the microprocessor can access the external memory only to access the header translation table (HTT). The control memory must not be accessed.

Figure 3-52. Example of Connecting HTT & Control Memory (minimum configuration)



If the HTT & control memory is configured to its maximum size, two memories of 256K words × 18 bits, or three or four 256K word × 16 bit memories are used. If 256K word × 16 bit memories that can control byte data (e.g., μPD434016AL) are used, only three memories are required.

Figure 3-53. Example of Connecting HTT & Control Memory (maximum configuration)



3.12.2 Cell buffer interface

The μPD98410 uses the cell buffer memory as a shared buffer.

As the cell buffer memory, a memory with 1 word being 88 bits wide and a depth of 64K words (128K words/256K words when expanded) is connected. For expansion, connect a memory with the same depth to the HTT & control memory. Cells are in the format shown in Figure 3-54 and have 55 bytes per cell, and are stored in the cell buffer.

The μPD98410 writes the cell buffer memory in 5 cycles and reads in 6 cycles in 88-bit units. One of the read cycles is actually a write cycle in which the cast counter (CC) is decremented and written back. The CBCS1_B signal is a write enable signal that writes CC and CCP (parity) for this write cycle. If an SRAM 18 bits wide is connected as the cell buffer memory, it is recommended that CBCS1_B be connected to the memory to which CBD[87:72] is connected. Because CBD[87:70] are driven when CC is written back, CBCS1_B can be connected to CBD[87:82] to CBD[87:70] depending on the type of the SRAM to be connected.

Because the microprocessor performs memory diagnostics as necessary after reset, the memory can be accessed. After the memory diagnostics have been completed, it is necessary to set the HC bit of the MODE register to “1” and select the HTT & control memory before issuing a command to the CMD register. The microprocessor can access the external memory only to access the header translation table (HTT) while the switching operation is enabled.

Figure 3-54. Cell Buffer Storage Format

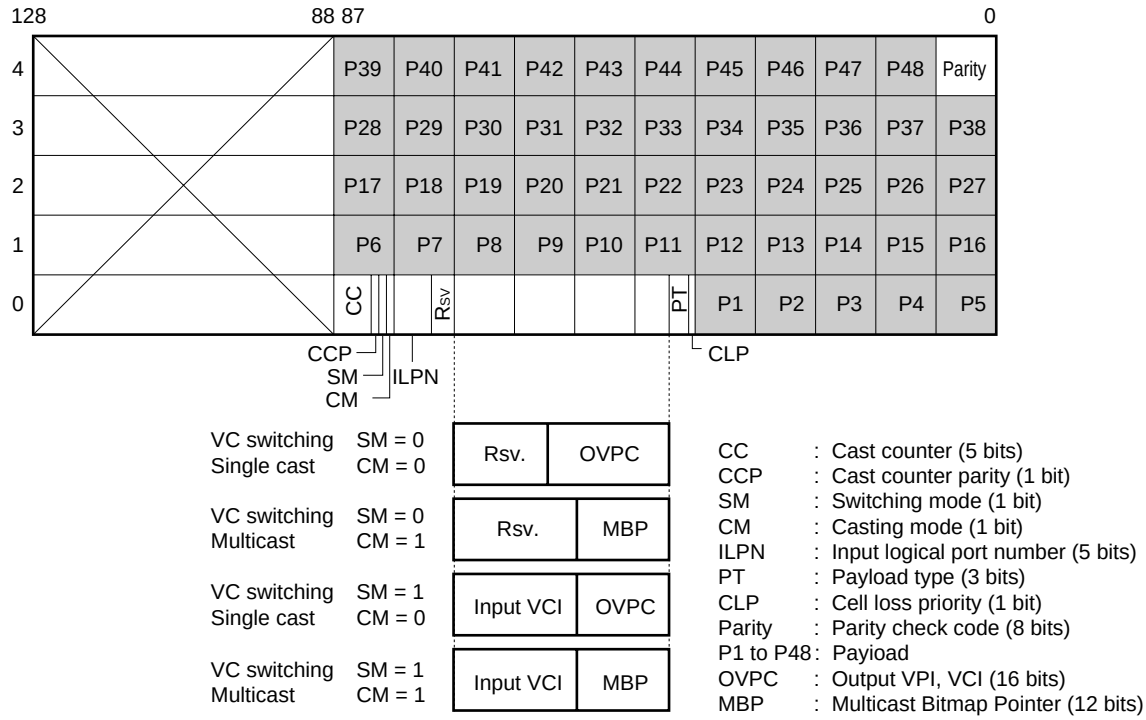
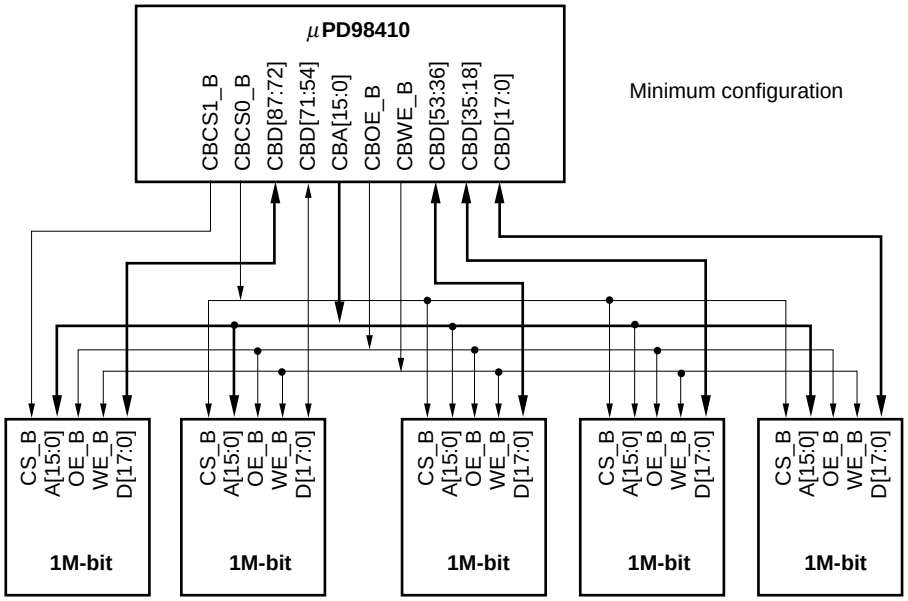
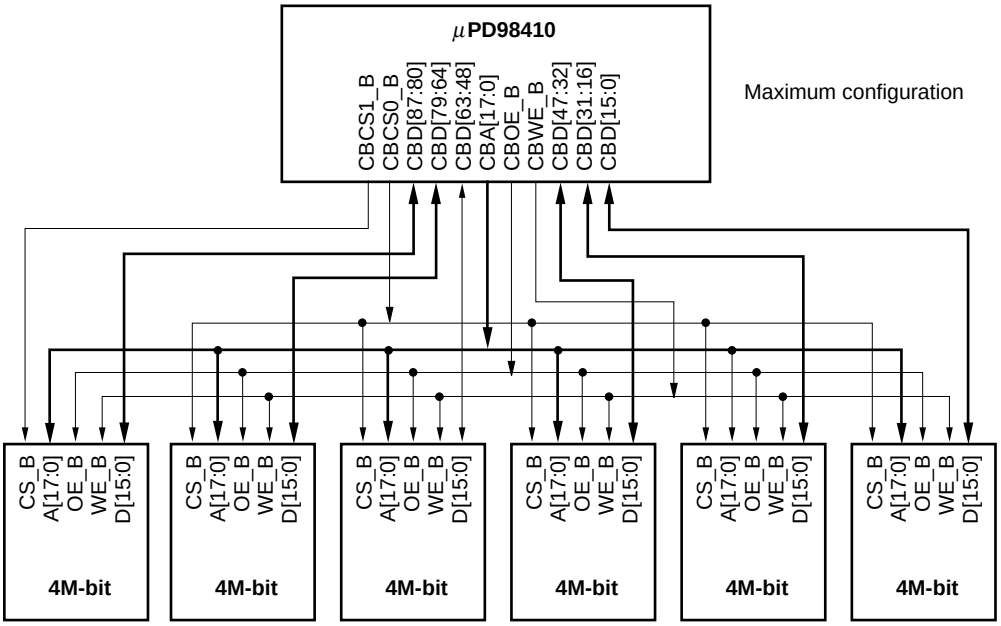


Figure 3-55. Example of Connecting Cell Buffer Memory





[MEMO]

4.1 Register List

(1/2)

Address	Register Name	Function	Bit	R/W	Section No.
0000h	CMD	Command	16	R/W	4.2.1
0004h	BANK	Memory bank	16	R/W	4.2.2
0006h	MODE	Memory mode	16	R/W	4.2.3
0008h	INTMASK	Interrupt mask	32	R/W	4.2.4
000Ch	STATUS	Status	32	R/W	4.2.5
0010h	EXTHMS	Threshold value exceeding discard indication mask	32	R/W	4.2.6
0014h	EXTH	Threshold value exceeding discard indication	32	R	4.2.7
0018h	ERHT	Header translation error discard indication	16	R	4.2.8
001Ah	ERHEC	HEC/CRC error discard indication	16	R	4.2.9
001Ch	ERINOV	Input port overrun error discard indication	16	R	4.2.10
0020h	CTENTH	Threshold value exceeding discard cell count enable	32	R/W	4.2.11
0024h	CTENHT	Header translation error discard cell count enable	16	R/W	4.2.12
0026h	CTENHEC	HEC/CRC error discard cell count enable	16	R/W	4.2.13
0028h	CTENMEM	Control/cell buffer memory shortage discard cell count enable	16	R/W	4.2.14
002Ah	CTENRCV	Receive cell count enable	16	R/W	4.2.15
002Ch	CTRCV	Receive cell count	32	R/W	4.2.16
0030h	CTEXTH	Threshold value exceeding discard cell count	32	R/W	4.2.17
0034h	CTERHT	Header translation error discard cell count	32	R/W	4.2.18
0038h	CTERHEC	HEC/CRC error discard cell count	32	R/W	4.2.19
003Ch	CTMEMEMP	Control/cell buffer memory shortage discard cell counter	32	R/W	4.2.20
0040h	OQminCRV	CBR + rtVBR class output queue minimum threshold value	16	R/W	4.2.21
0044h	OQminRNV	RM + nrtVBR class output queue minimum threshold value	16	R/W	
0048h	OQminABR	ABR class output queue minimum threshold value	16	R/W	
004Ch	OQminUBR	UBR class output queue minimum threshold value	16	R/W	
0050h	MQminCRV	CBR + rtVBR class multi-cast queue minimum threshold value	16	R/W	4.2.22
0054h	MQminRNV	RM + nrtVBR class multi-cast queue minimum threshold value	16	R/W	
0058h	MQminABR	ABR class multi-cast queue minimum threshold value	16	R/W	
005Ch	MQminUBR	UBR class multi-cast queue minimum threshold value	16	R/W	
0060h	TCminCRV	CBR + nrVBR class TC (Total Cell) counter minimum threshold value	16	R/W	4.2.23
0064h	TCminRNV	RM + nrtVBR class TC (Total Cell) counter minimum threshold value	16	R/W	
0068h	TCminABR	ABR class TC (Total Cell) counter minimum threshold value	16	R/W	
006Ch	TCminUBR	UBR class TC (Total Cell) counter minimum threshold value	16	R/W	
007Eh	ALLmin	Total number of cells minimum threshold value (total number of minimum guaranteed cells of each output queue, multi-cast queue, and TC counter)	16	R/W	4.2.24

(2/2)

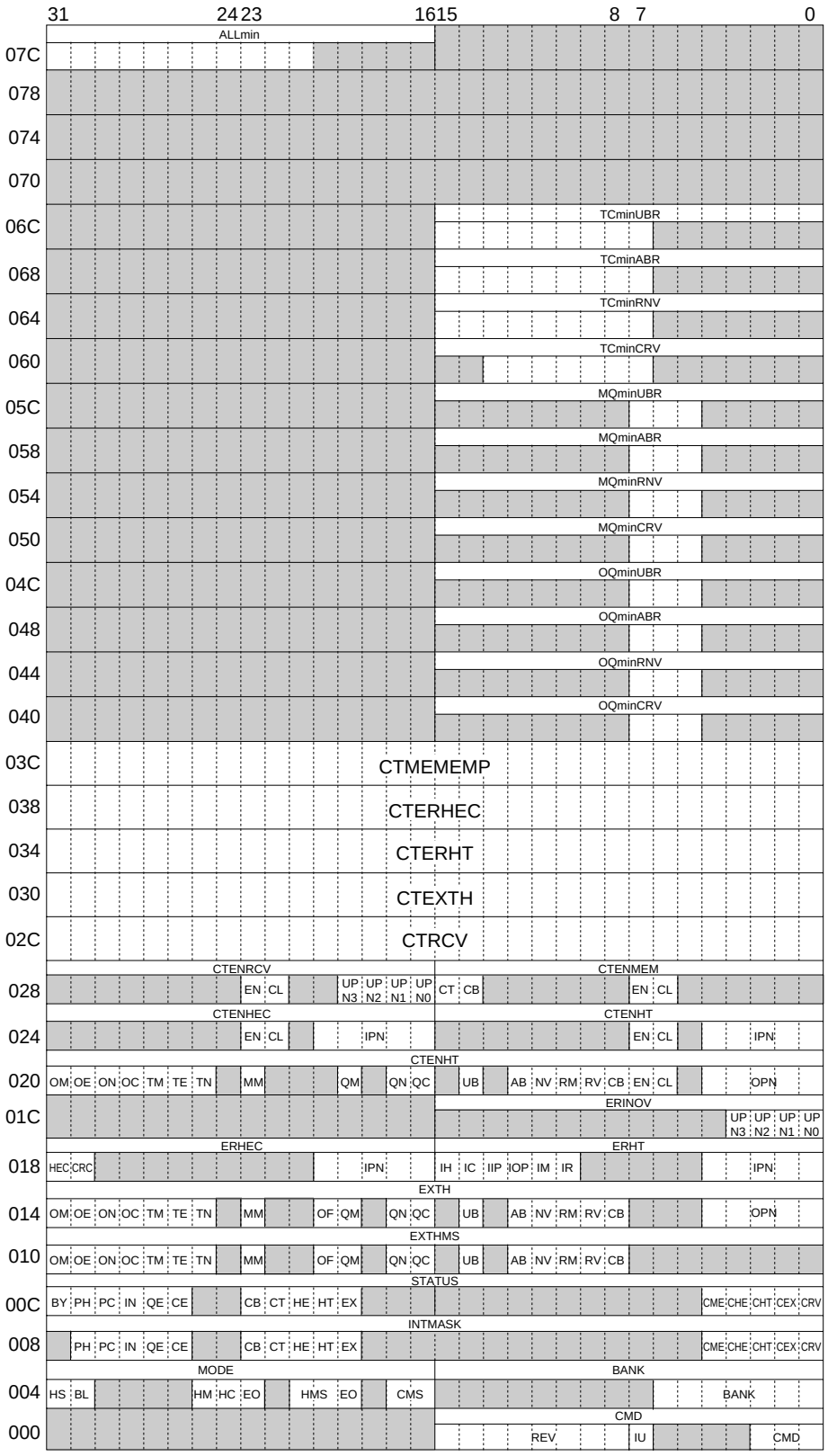
Address	Register Name	Function	Bit	R/W	Section No.
0080h	OQthCBR	CBR class output queue maximum threshold value	16	R/W	4.2.25
0082h	OQthRVR	rtVBR class output queue maximum threshold value	16	R/W	4.2.25
0086h	OQthCCL	CLP threshold value of CBR + rtVBR class output queue	16	R/W	4.2.28
0090h	OQthRM	RM class output queue maximum threshold value	16	R/W	4.2.25
0092h	OQthNVR	nrtVBR class output queue maximum threshold value	16	R/W	4.2.25
0094h	OQthRCI	EFCI threshold value of RM + nrtVBR class output queue	16	R/W	4.2.27
0096h	OQthRCL	CLP threshold value of RM + nrtVBR class output queue	16	R/W	4.2.28
00A0h	OQthABR	ABR class output queue maximum threshold value	16	R/W	4.2.25
00A2h	OQthAEP	EPD threshold value of ABR class output queue	16	R/W	4.2.26
00A4h	OQthACI	EFCI/CI threshold value of ABR class output queue	16	R/W	4.2.27
00A6h	OQthACL	CLP threshold value of ABR class output queue	16	R/W	4.2.28
00B0h	OQthUBR	UBR class output queue maximum threshold value	16	R/W	4.2.25
00B2h	OQthUEP	EPD threshold value of UBR class output queue	16	R/W	4.2.26
00B4h	OQthUCI	EFCI threshold value of UBR class output queue	16	R/W	4.2.27
00B6h	OQthUCL	CLP threshold value of UBR class output queue	16	R/W	4.2.28
00C0h	MQthCRV	CBR + rtVBR class multi-cast queue maximum threshold value	16	R/W	4.2.29
00C4h	MQthRNV	RM + nrtVBR class multi-cast queue maximum threshold value	16	R/W	4.2.29
00C8h	MQthABR	ABR class multi-cast queue maximum threshold value	16	R/W	4.2.29
00CCh	MQthUBR	UBR class multi-cast queue maximum threshold value	16	R/W	4.2.29
00D0h	UCthCBR	CBR class UC (Used Cell) counter maximum threshold value	16	R/W	4.2.30
00D4h	UCthRVR	rtVBR class UC (Used Cell) counter maximum threshold value	16	R/W	
00D8h	UCthRM	RM class UC (Used Cell) counter maximum threshold value	16	R/W	
00DCh	UCthNVR	nrtVBR class UC (Used Cell) counter maximum threshold value	16	R/W	
00E0h	UCthABR	ABR class UC (Used Cell) counter maximum threshold value	16	R/W	
00E2h	UCthAEP	EPD threshold value of ABR class UC (Used Cell) counter	16	R/W	4.2.31
00E8h	UCthUBR	UBR class UC (Used Cell) counter maximum threshold value	16	R/W	4.2.30
00EAh	UCthUEP	EPD threshold value of UBR class UC (Used Cell) counter	16	R/W	4.2.31
Note 1	PT0 - PT23	Port configuration	32	R/W	4.2.32
Note 2	PC0 - PC23	Class priority control	32	R/W	4.2.33
01FCh	PERIOD	Cycle count	16	R/W	4.2.34
Note 3	HT0 - HT23	Header translation configuration	32	R/W	4.2.35

Notes 1. 100h, 0104h, 0108h, 010Ch, 0110h, 0114h, 0118h, 011Ch, 0120h, 0124h, 0128h, 012Ch, 0130h, 0134h, 0138h, 013C, 0140h, 0144h, 0148h, 014Ch, 0150h, 0154h, 0158h, 015Ch

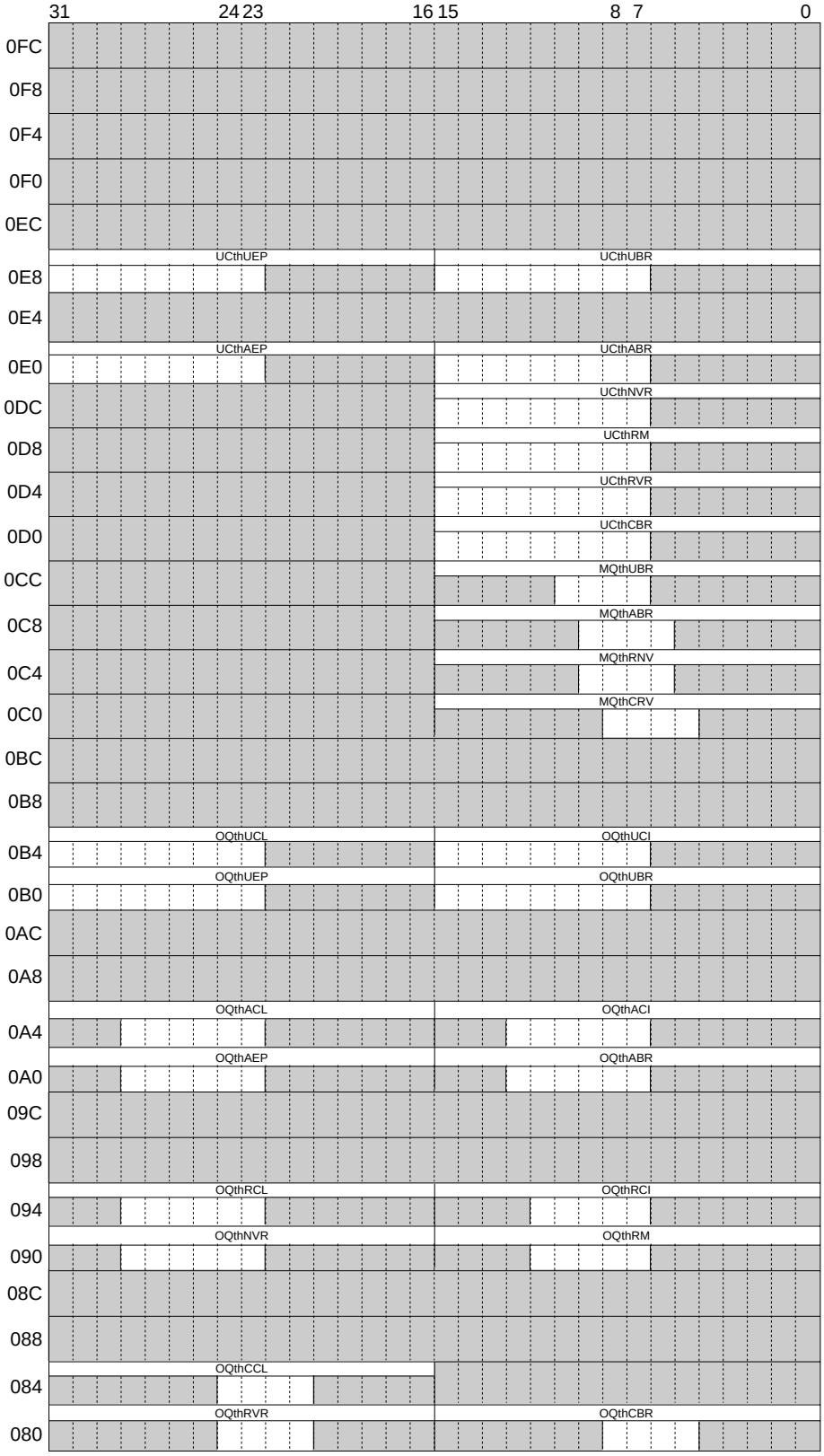
2. 0180h, 0184h, 0188h, 018Ch, 0190h, 0194h, 0198h, 019Ch, 01A0h, 01A4h, 01A8h, 01ACh, 01B0h, 01B4h, 01B8h, 01BCh, 01C0h, 01C4h, 01C8h, 01CCh, 01D0h, 01D4h, 01D8h, 01DCh

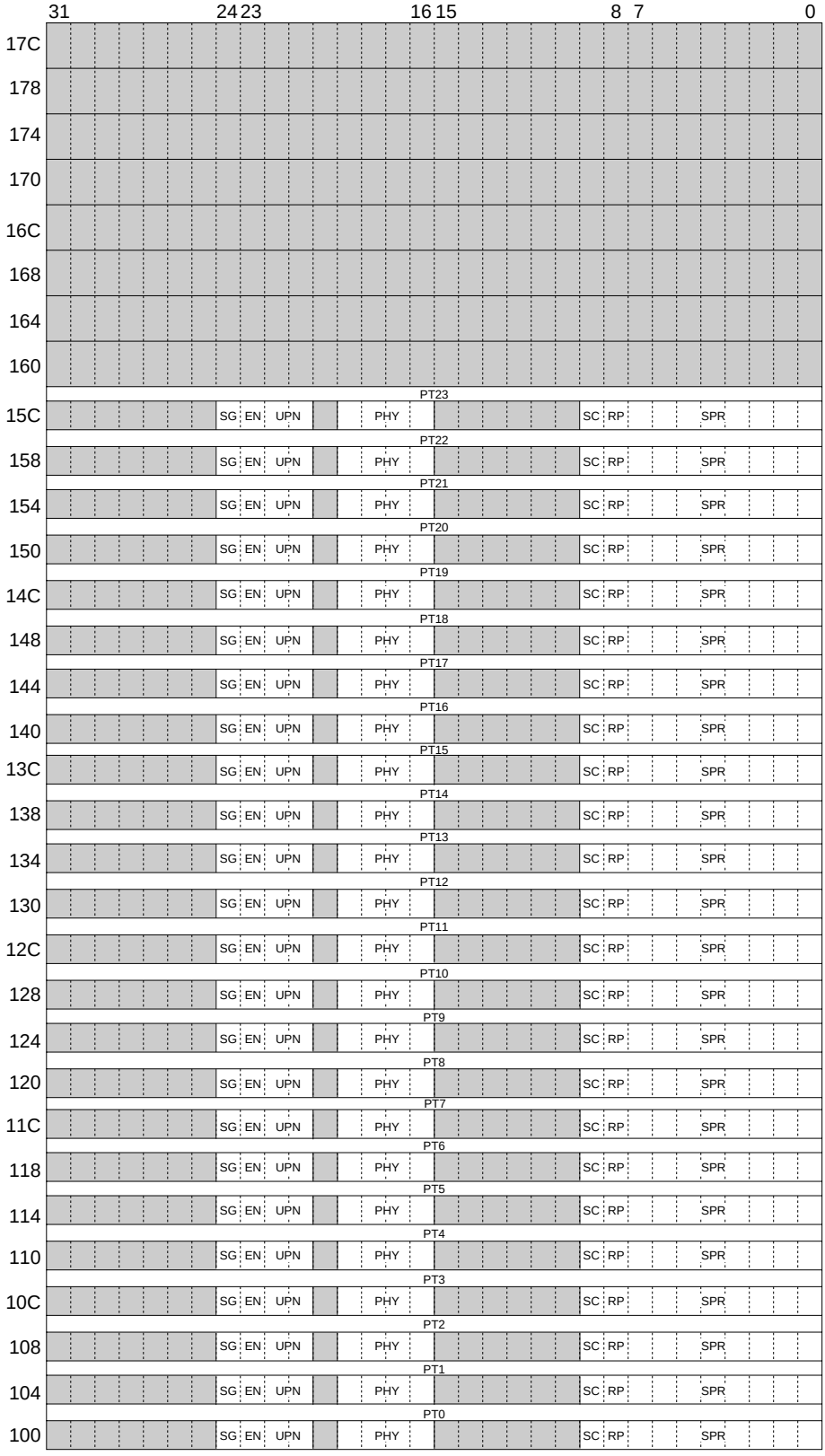
3. 0200h, 0204h, 0208h, 020Ch, 0210h, 0214h, 0218h, 021Ch, 0220h, 0224h, 0228h, 022Ch, 0230h, 0234h, 0238h, 023Ch, 0240h, 0244h, 0248h, 024Ch, 0250h, 0254h, 0258h, 025Ch

4.2 Register Map

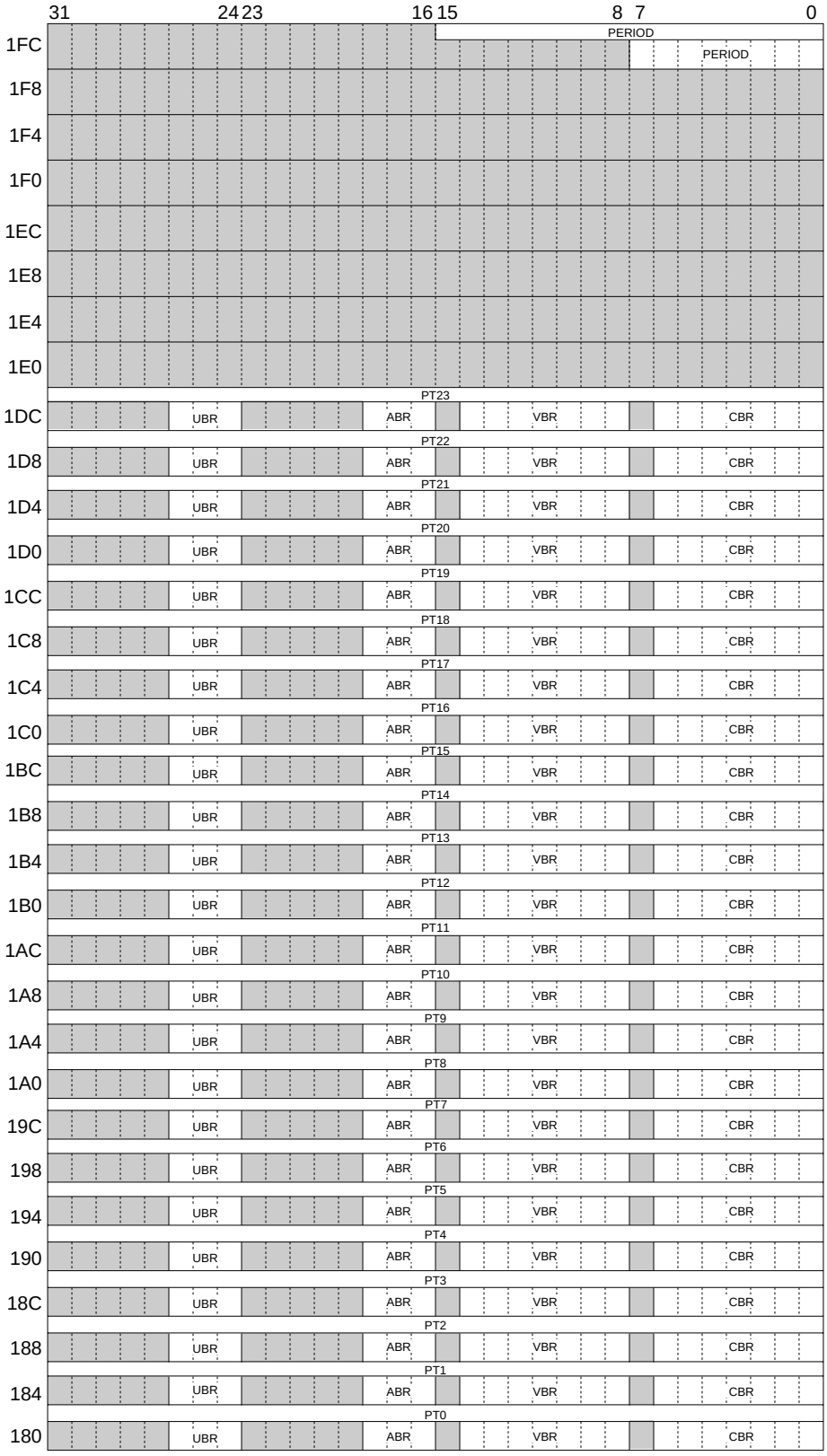


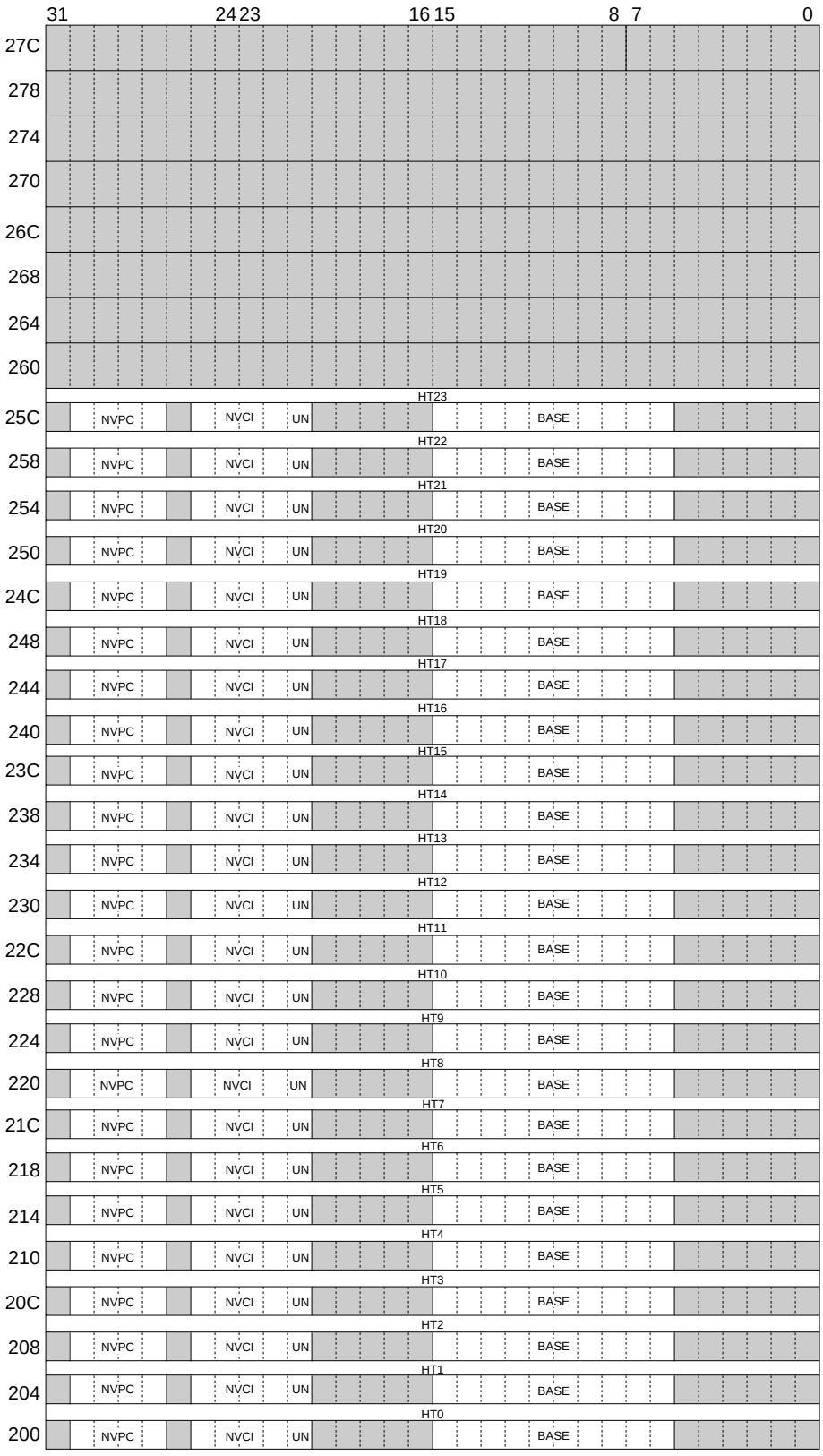
Phase-out/Discontinued



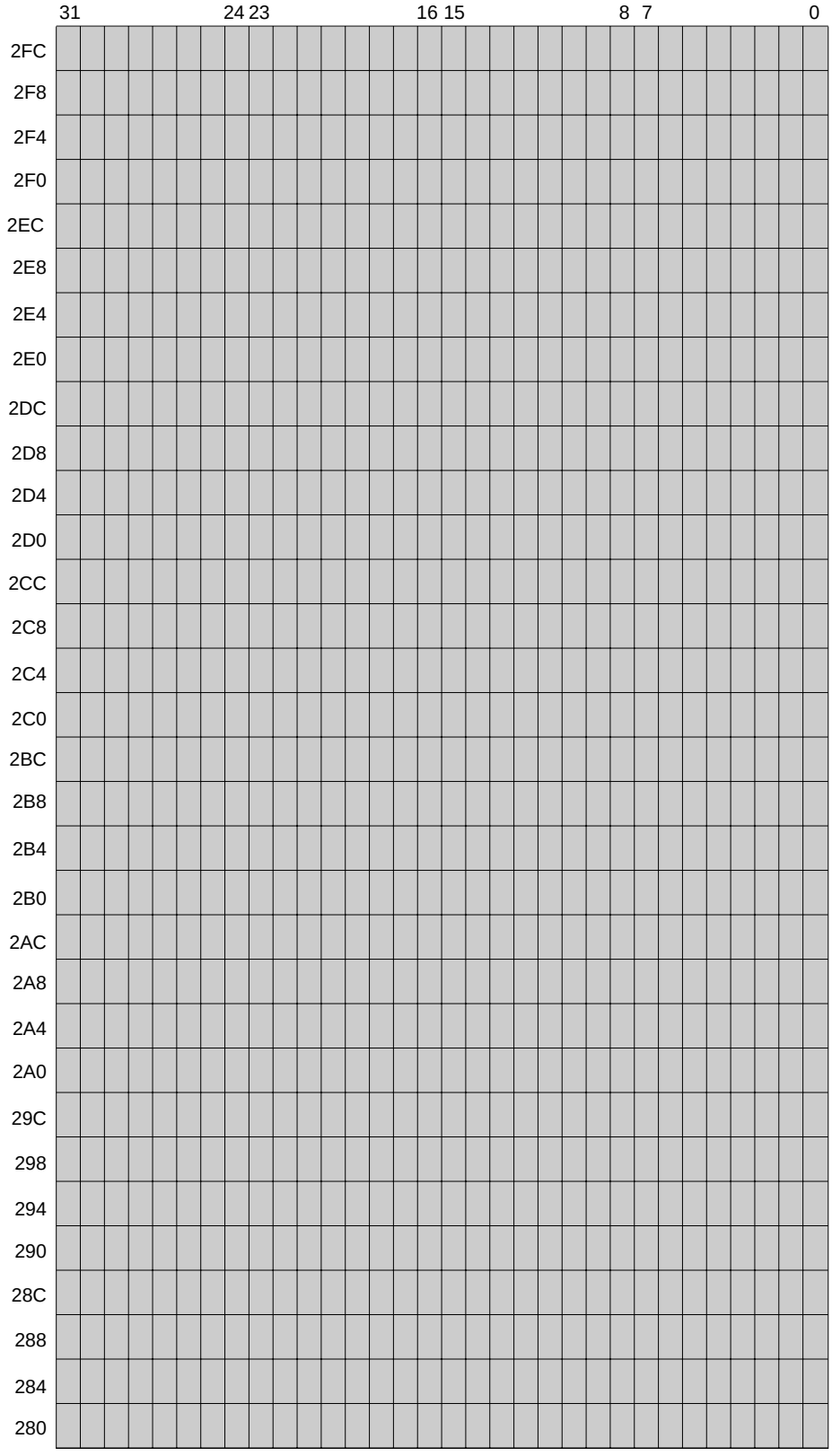


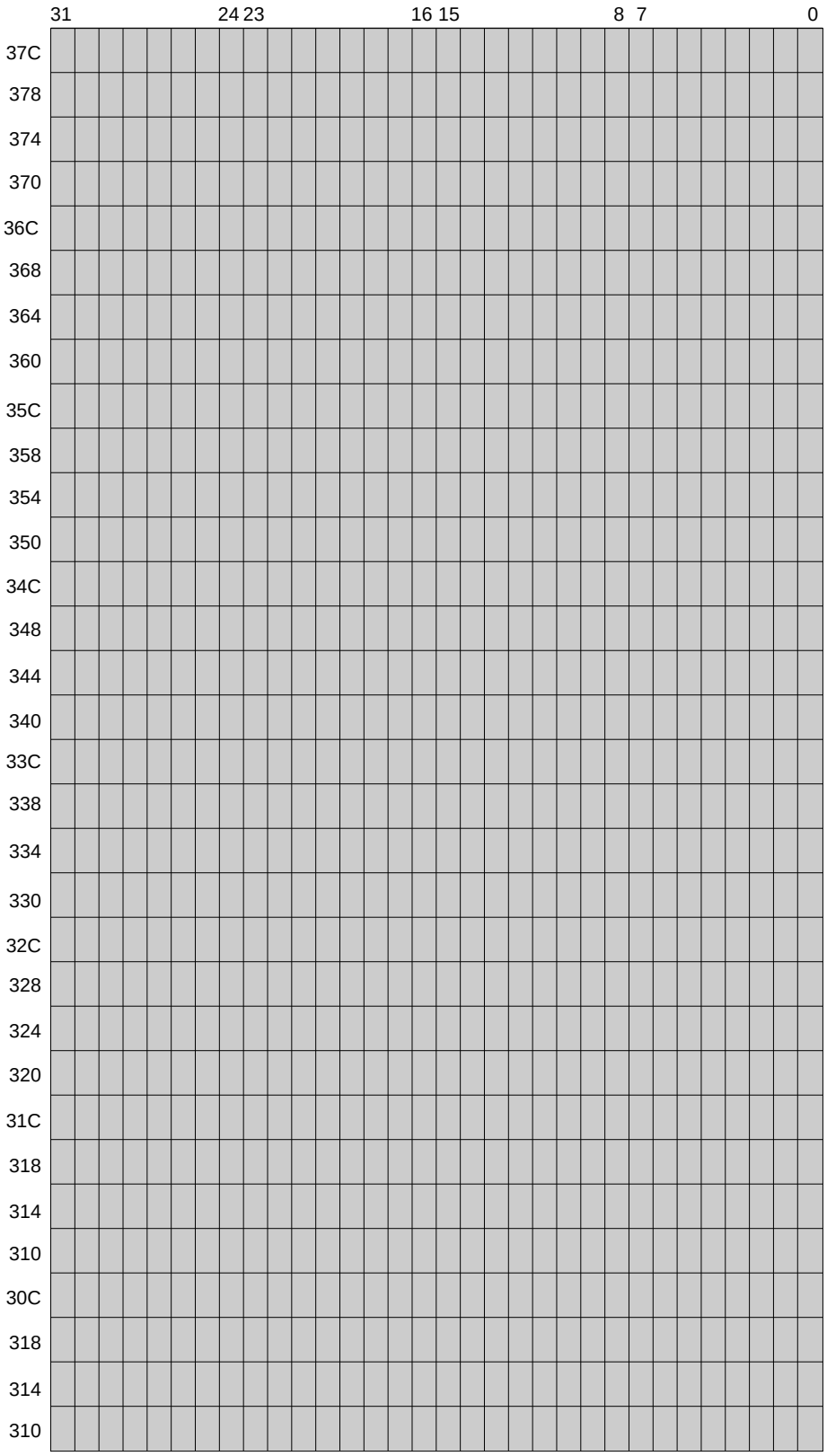
Phase-out/Discontinued



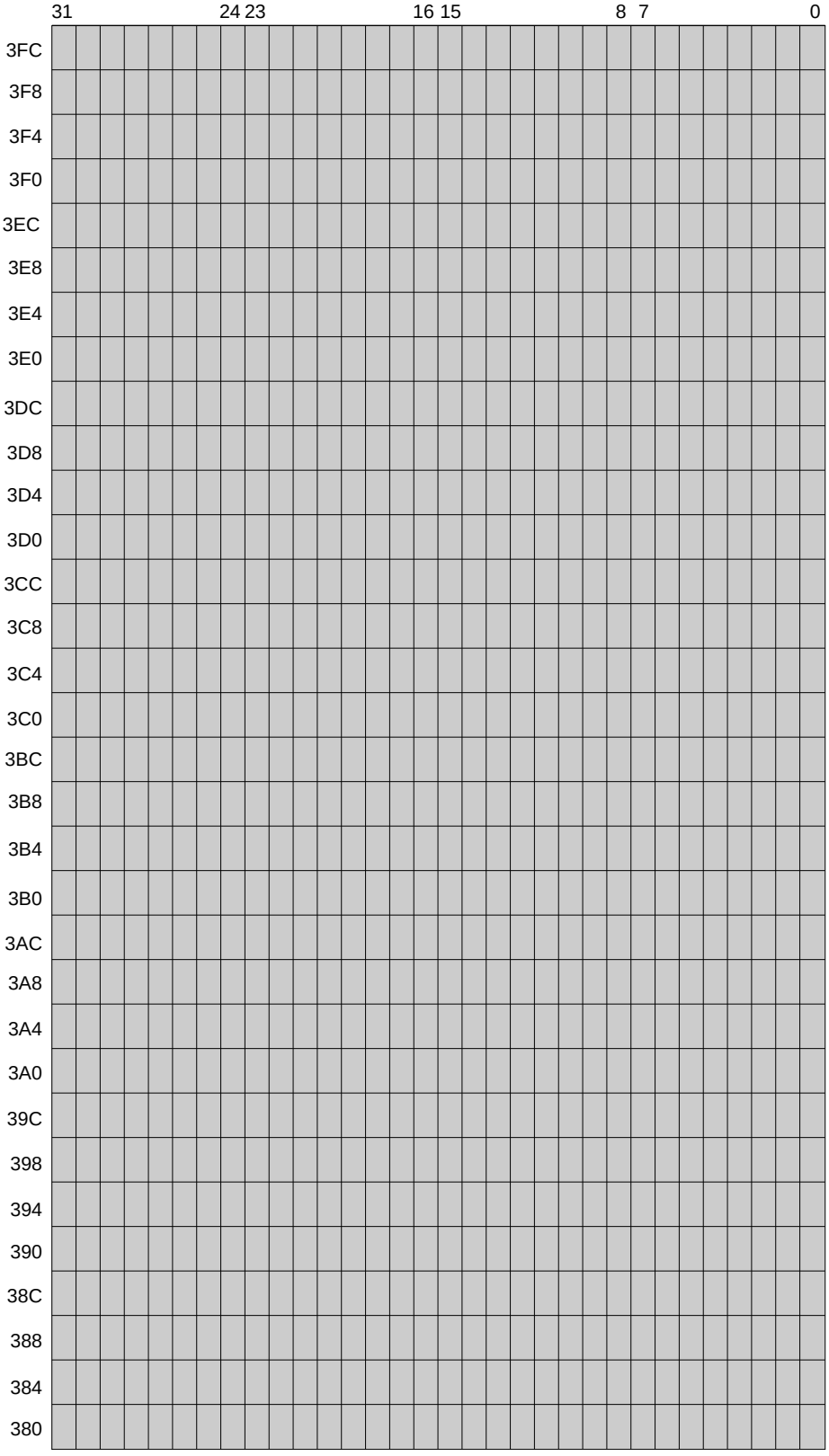


Phase-out/Discontinued





Phase-out/Discontinued

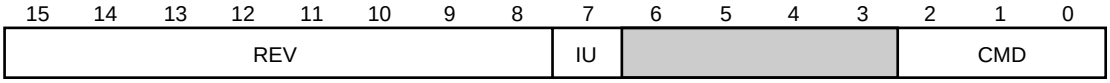


4.3 Register Functions

This section explains the registers of the μPD98410. The shaded portions in the descriptions below indicates a reserved area. Write "0" to the bits of a reserved area. These bits are "don't care" when they are read.

4.3.1 Command register (0000h)

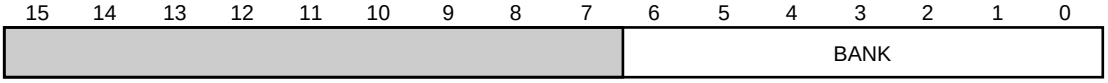
Register name	Address	Default	R/W
CMD	0000h	0001_0000_0xxx_x000	R/W or R



Field	Bit	R/W	Function	Default Value
REV	bit [15:8]	R	Indicates the version number of the μPD98410. The high-order nibble indicates the major version number, and the low-order nibble indicates the revision number. For example, "10h" means version 1.0. A value written to these bits is meaningless.	Fixed to 10h
IU	bit [7]	R/W	This is a test mode bit for the μPD98410. Be sure to reset it to "0" when using it.	0
CMD	bit [2:0]	R/W	These bits specify a command for the μPD98410. Set CMD to enable the switching operation after the BY bit of the status register has become inactive and each register and the header translation table (HTT) have been set. If it is specified to stop the switching operation, the operation is stopped after the current processing of a cell is completed. To set CMD to enable the switching operation after the operation has been stopped, confirm that the BY bit is inactive. 000: Stops switching operation. 111: Enables switching operation.	000

4.3.2 Memory bank register (0004h)

Register name	Address	Default	R/W
BANK	0004h	xxxx_xxxx_x000_0000	R/W

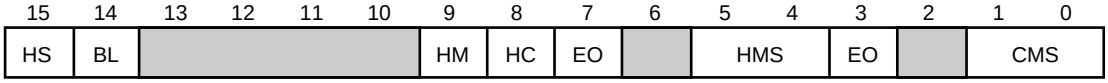


Field	Bit	R/W	Function	Default Value
BANK	bit [6:0]	R/W	These bits specify a bank used to access the external memory when the 16-bit separated asynchronous bus interface is used. For details, refer to **3.11 Microprocessor Interface**. "00h" to "7Fh": BANK number for accessing external memory	00h

Remark The value of this register is meaningless when the 32-bit multiplexed synchronous bus interface is used.

4.3.3 Memory mode register (0006h)

Register name	Address	Default	R/W
MODE	0006h	!0xx_xx00_0x00_0x00	R/W or R



Caution Set this MODE register before issuing a command to the CMD register after reset. Do not write anything to this register until it is reset after a command has been issued to the CMD register. If the value of this register is rewritten while the operation is being carried out, the switching operation cannot be guaranteed.

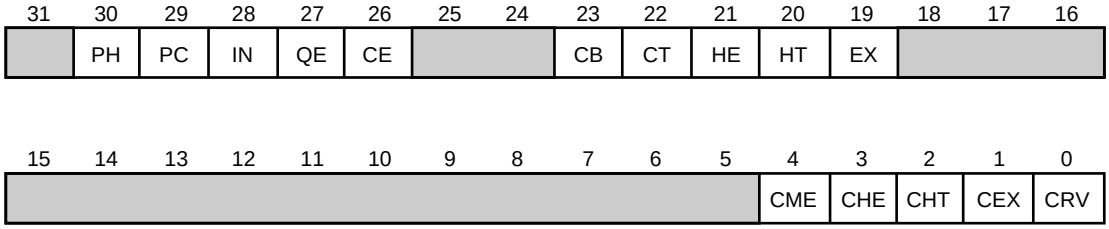
Remark The value indicated by ! under the heading Default Value is reset to 0 when a low level is input to the HSEL pin and is set to 1 when a high level is input to the HSEL pin.

Field	Bit	R/W	Function	Default Value
HS	bit [15]	R	Indicates the level of the HSEL pin, i.e., the mode of interfacing with the microprocessor. A value written to this bit is meaningless. 0: 32-bit multiplexed synchronous bus interface 1: 16-bit separated asynchronous bus interface	Fixed to 0 or 1

Field	Bit	R/W	Function	Default Value
BL	bit [14]	R/W	This bit sets the byte alignment of the microprocessor to be connected. Because the default value after reset is little endian, care must be exercised if a microprocessor with a big endian interface accesses this register after reset. 0: Little endian 1: Big endian	0
HM	bit [9]	R/W	Enables or disables the cell discarding function in case of an HEC error. 0: Enables cell discarding function in case of an HEC error (discards HEC error cell). 1: Disables cell discarding function in case of an HEC error (passes HEC error cell).	0
HC	bit [8]	R/W	Selects which of the two external memories is to be selected when the memory chip select pin is active. Set this bit to “1” to select the HTT & control memory before issuing a command to the CMD register. While the switching operation is enabled, the microprocessor can access the external memory only for the header translation table (HTT), and cannot access the control memory. 0: Selects cell buffer memory. 1: Selects HTT & control memory.	0
EO	bit [7], [3]	R/W	Sets an even parity or odd parity for parity check of the external memory. • Bit 7: Sets HTT & control memory. • Bit 3: Sets cell buffer memory. 0: Odd parity 1: Even parity	0
HMS	bit [5:4]	R/W	Sets the size of the HTT & control memory (32 bits/word). 00: 64K words 01: 128K words 10: 256K words 11: Reserved	00
CMS	bit [1:0]	R/W	Sets the size of the cell buffer memory (88 bits/word). 00: 64K words 01: 128K words 10: 256K words 11: Reserved	00

4.3.4 Interrupt mask register (0008h)

Register name	Address	Default	R/W
INTMASK	0008h	x000_00xx_0000_0xxx_xxxx_xxxx_xxx0_0000	R/W



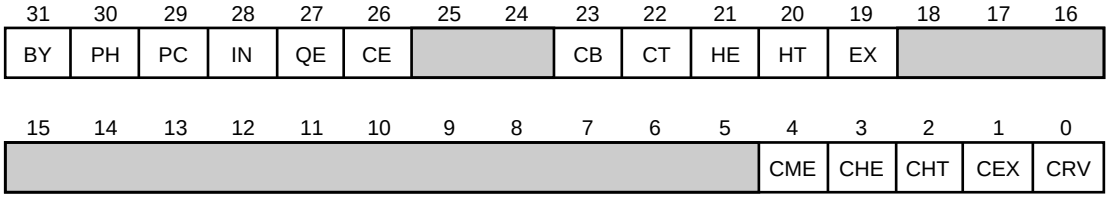
The INTMASK register masks an interrupt that occurs when the corresponding status becomes active. Indication by the status register is not masked. Each bit of this register can be set in the same manner. For the cause of an interrupt, refer to the description of the status register.

0: Masks interrupt caused by corresponding cause.
1: Requests interrupt caused by corresponding cause.

Remark No interrupt request is generated even if the BY bit of the status bit is active.

4.3.5 Status register (000Ch)

Register name	Address	Default	R/W
STATUS	000Ch	0000_00xx_0000_0xxx_xxxx_xxxx_xxx0_0000	R/W or R



The status register is set when the corresponding cause becomes active. An interrupt occurs for the corresponding interrupt cause, except for the BY bit. When this register is read it indicates the current status, and when it is written the status is cleared. All bits have the same function.

When read

0: Indicates that the corresponding status is inactive

1: Indicates that the corresponding status is active

When written

0: Retains the corresponding status

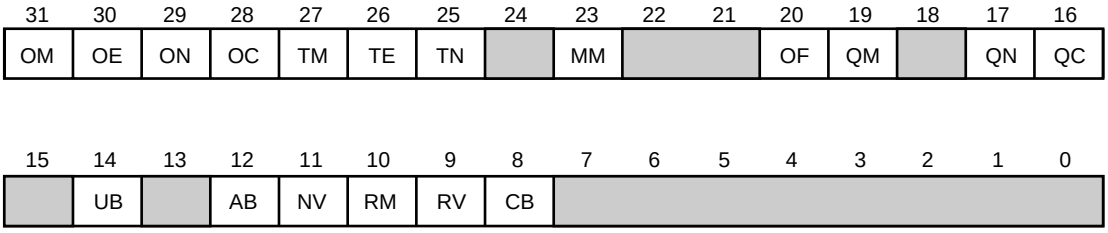
1: Clears the corresponding status

Field	Bit	R/W	Function	Default Value
BY	bit [31]	R	Indicates that the μPD98410 is in the following operation status. No interrupt occurs even if this cause is changed. Writing this bit is meaningless. • At reset, indicates that the μPD98410 is in initializing. When the μPD98410 is reset by using the RESET_B pin, this bit becomes active. When the internal circuits of the LSI are initialized, this bit becomes inactive. • Indicates that the switching operation is enabled at times other than at reset. This bit becomes active when the operation of the μPD98410 is enabled by using the CMD register, and becomes inactive after the switching operation has stopped. **Caution Do not access the μPD98410 except to read the status register before this bit becomes inactive after reset. If any register of the μPD98410 is accessed while this bit is active, the initialization operation may not be performed correctly.**	0

Field	Bit	R/W	Function	Default Value
PH	bit [30]	R	Indicates a parity error in the HTT & control memory.	0
PC	bit [29]	R	Indicates a parity error in the cell buffer memory.	0
IN	bit [28]	R	Indicates an overrun of the input FIFO at the reception side.	0
QE	bit [27]	R	Indicates an abnormal status in the pointer that manages the queue.	0
CE	bit [26]	R	Indicates an abnormal status in the cast counter that manages multi-cast count.	0
CB	bit [23]	R/W	Indicates that a cell has been discarded because the area for storing data has run short in the cell buffer memory.	0
CT	bit [22]	R/W	Indicates that a cell has been discarded because the area of the control memory that manages the queue of the HTT & control memory has run short. This may occur if the average broadcast count exceeds 2.	0
HE	bit [21]	R/W	Indicates an HEC error or CRC error in a received cell. If the HM bit of the MODE register is “1”, the HEC error is not indicated because the HEC error cell is not discarded.	0
HT	bit [20]	R/W	Indicates a header translation error.	0
EX	bit [19]	R/W	Indicates that a cell has been discarded because a threshold value, service class, or logical output port number of the EXTHMS register is exceeded.	0
CME	bit [4]	R/W	Indicates that CTMEMEMP overflowed.	0
CHE	bit [3]	R/W	Indicates that CTERHEC overflowed.	0
CHT	bit [2]	R/W	Indicates that CTERHT overflowed.	0
CEX	bit [1]	R/W	Indicates that CTEXTH overflowed.	0
CRV	bit [0]	R/W	Indicates that CTRCV overflowed.	0

4.3.6 Threshold value exceeding discard indication mask register (0010h)

Register name	Address	Default	R/W
EXTHMS	0010h	0000_000x_0xx0_0x00_x0x0_0000_xxxx_xxxx	R/W

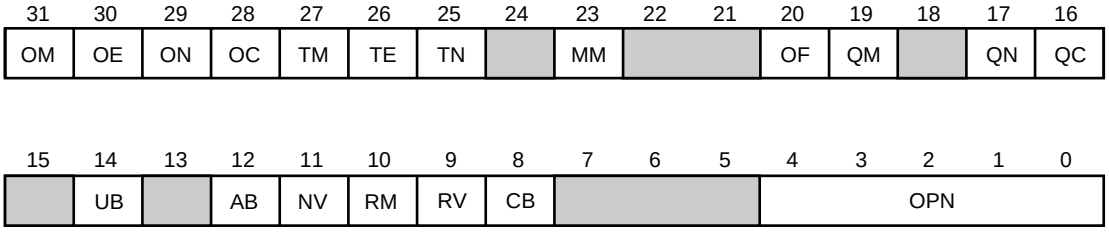


The EXTHMS register masks the use of the EXTH register to indicate when a threshold value is expected. Exceeding of a threshold value is reflected on the EX bit of the status register and an interrupt cause by setting the corresponding threshold value cause and condition of the corresponding class to the EXTHMS register. Regardless of the value of the EXTHMS register, cells are discarded when a threshold value is exceeded. Each bit of this register is set in the same manner. For the causes, refer to the description of the EXTH register.

0: Does not reflect corresponding cause on status.
1: Reflects corresponding cause on status.

4.3.7 Threshold value exceeding discard indication register (0014h)

Register name	Address	Default	R/W
EXTH	0014h	0000_000x_0xx0_0x00_x0x0_0000_xxx0_00	R
		00	



The EXTH register indicates the threshold value, class, and output port that are responsible for the first discarding of a cell after the EX bit of the status register has been cleared. More than one threshold value responsible for discarding the cell may be indicated. If a cell is discarded because a threshold value is exceeded (queue length ≥ threshold value), the corresponding bit is set and, at the same time, the EX bit of the status register is set. If the cell discarding cause satisfies the condition of the CTENTH register, the CTEXTH register is incremented. While the EX bit is set, this register is not updated but retained. When the microprocessor clears the EX bit, updating this register becomes valid again. When the EX bit is cleared, the EXTH register does not indicate the correct value.

Even if a cell is discarded because of the class of threshold value masked by the EXTHMS register, it is not reflected on the EXTH register. Nor is the EX bit of the status register set.

bit [31 through 25, 23, 19, 17, 16] OM, OE, ON, OC, TM, TE, TN, MM, QM, QN, QC

0: Indicates that the corresponding class did not bring about discarding a cell first.

1: Indicates that the corresponding class did bring about discarding a cell first.

bit [14, 12 through 8] UB, AB, NV, RM, RV, CB

0: Indicates that the corresponding class did not bring about discarding a cell first.

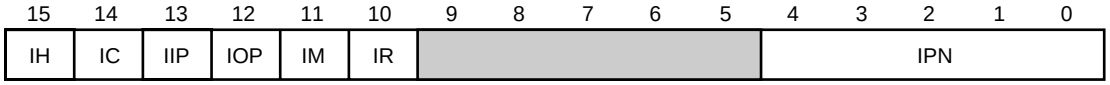
1: Indicates that the corresponding class did bring about discarding a cell first.

Field	Bit	R/W	Function	Default Value
OM	bit [31]	R	Indicates that a cell has been discarded because the output queue exceeds OQthCBR, OQthRVR, OQthRM, OQthNVR, OQthABR, or OQthUBR threshold value.	0
OE	bit [30]	R	These bits simultaneously indicate that the packet of the channel set for EPD is discarded because of EPD control because the output queue exceeds OQthAEP or OQthUEP threshold value or that the UC (Used Cell) counter exceeds UCthAEP or UCthUEP threshold value. There is no functional difference between the OE and TE bits.	0
TE	bit [26]	R		0
ON	bit [29]	R	Indicates that the cell of the channel not set for EPD is discarded because the output queue exceeds OQthAEP or OQthUEP threshold value.	0
OC	bit [28]	R	Indicates that the cell set for CLP is discarded because the output queue exceeds OQthCCL, OQthRCL, OQthACL, or OQthUCL threshold value.	0
TM	bit [27]	R	Indicates that a cell is discarded because the UC (Used Cell) counter exceeds UCthCBR, UCthRVR, UCthRM, UCthNVR, UCthABR, or UCthUBR threshold value.	0
TN	bit [25]	R	Indicates that the cell of the channel not set for EPD is discarded because the UC (Used Cell) counter exceeds UCthAEP or UCthUEP threshold value.	0
MM	bit [23]	R	Indicates that a multi-cast cell is discarded because the multi-cast queue exceeds MQthCRV, MQthRNV, MQthABR, or MQthUBR threshold value.	0
OF	bit [20]	R	Indicates that EFCI marking is performed because the output queue exceeds OQthRCI, OQthACI, or OQthUCI threshold value during queuing or re-queuing of multi-cast. **Remark** This bit is used for testing. Do not use it because it may be deleted in the future.	0
QM	bit [19]	R	Indicates that a cell is discarded because the output queue exceeds OQthCBR, OQthRVR, OQthRM, OQthNVR, OQthABR, or OQthUBR threshold value during re-queuing of multi-cast, or the UC (Used Cell) counter exceeds UCthCBR, UCthRVR, UCthRM, UCthNVR, UCthABR, or UCthUBR threshold value.	0

Field	Bit	R/W	Function	Default Value
QN	bit [17]	R	Indicates that the cell of the channel not set for EPD is discarded because the output queue exceeds OQthAEP or OQthUEP threshold value during re-queuing of multi-cast, or the UC (Used Cell) counter exceeds UCthAEP or UCthUEP threshold value.	0
QC	bit [16]	R	Indicates that a cell set for CLP is discarded because the output queue exceeds OQthCCL, OQthRCL, OQthACL, or OQthUCL threshold value during re-queuing of multi-cast.	0
UB	bit [14]	R	Indicates that a cell of UBR class is discarded because a threshold value is exceeded.	0
AB	bit [12]	R	Indicates that a cell of ABR class is discarded because a threshold value is exceeded.	0
NV	bit [11]	R	Indicates that a cell of nrtVBR class is discarded because a threshold value is exceeded.	0
RM	bit [10]	R	Indicates that an RM class is discarded because a threshold value is exceeded.	0
RV	bit [9]	R	Indicates that a cell of rtVBR class is discarded because a threshold value is exceeded.	0
CB	bit [8]	R	Indicates that a cell of CBR class is discarded because a threshold value is exceeded.	0
OPN	bit [4:0]	R	Indicates the number of the logical output port that discards a cell because a threshold value is exceeded. 00h to 17h : Indicates logical output port 0 to 23 1Fh : MM, QM, QN, or QC cause	00h

4.3.8 Header translation error discard indication register (0018h)

Register name	Address	Default	R/W
ERHT	0018h	0000_00xx_xxx1_1111	R



The ERHT register indicates a header translation error and an input port that are responsible for the first cell discarding after the HT bit of the status register has been cleared. When a cell is discarded, the corresponding bit of this register is set and, at the same time, the HT bit of the status register is set. If the condition of the CTENHT register is satisfied, the CTERHT register is incremented. While the HT bit is set, the ERHT register is not updated and its values are retained. When the microprocessor clears the HT bit, updating the ERHT register is enabled. When the HT bit is cleared, the ERHT register does not indicate the correct values.

bit [15, 14, 12, 11, 10] IH, IC, IOP, IM, IR

0: Indicates that the corresponding cause is not responsible for the first discarding of a cell.

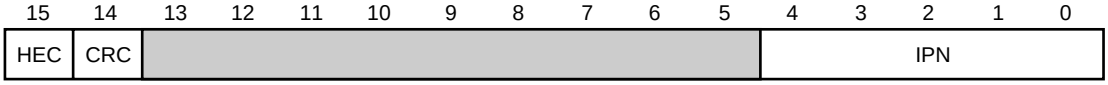
1: Indicates that the corresponding cause is responsible for the first discarding of a cell.

Field	Bit	R/W	Function	Default Value
IH	bit [15]	R	Indicates that a cell has been discarded because the μPD98410 attempted to access HTT, exceeding the range set by the HT register. This happens if the VPI and VCI of the received cell are greater than the valid number of bits set to the HT register.	0
IC	bit [14]	R	Indicates that a cell has been discarded because the corresponding channel was disabled (CEN = “0”) when the μPD98410 accessed HTT. This happens when a cell having VPI and VCI for which no connection is made has been received.	0
IIP	bit [13]	R	This bit is used for testing the μPD98410 and must not be used.	0
IOP	bit [12]	R	Indicates that a cell has been discarded because the logical output port obtained as a result of μPD98410’s access to HTT was disabled (PT register EN bit = “0”). This happens when a cell having VPI and VCI for which no connection is made has been received.	0
IM	bit [11]	R	Indicates that a cell has been discarded because the multi-cast bit map (MB) for the channel that was set for multi-cast (CM = “1”) was 0 and because the logical output port obtained by using MB was disabled (PT register EN bit = “0”) when the μPD98410 accessed HTT. This happens when a cell having VPI and VCI for which no connection is made has been received.	0

Field	Bit	R/W	Function	Default Value
IR	bit [10]	R	Indicates that a cell has been discarded because an attempt was made to merge the RM cells of channels that were disabled (CEN = “0”) or because an attempt was made to merge the RM cells of a channel set in the single cast mode (CM = “0”) when the μPD98410 accessed HTT. This happens when a cell having VPI and VCI for which no connection is made has been received.	0
IPN	bit [4:0]	R	Indicates the number of the input port that has received the cell responsible for a header translation error. The IM cause indicates “1Fh” as a logical input port number. 00h to 17h: Indicates logical input port 0 to 23. 1Fh : IM cause	1Fh

4.3.9 HEC/CRC error discard indication register (001Ah)

Register name	Address	Default	R/W
ERHEC	001Ah	00xx_xxxx_xxx1_1111	R



The ERHEC register indicates an HEC error or CRC-10 error and an input port responsible for the first discarding of a cell after the HE bit of the status register has been cleared. When a cell is discarded, the corresponding bit of this register is set and, at the same time, the HE bit of the status register is set.

If the condition of the CTENHEC register is satisfied, the CTERHEC register is incremented. While the HT bit is set, this register is not updated and its values are retained. When the microprocessor clears the HE bit, updating the ERHEC register is enabled. When the HE bit is cleared, this register does not indicate the correct values.

bit [15, 14] HEC, CRC

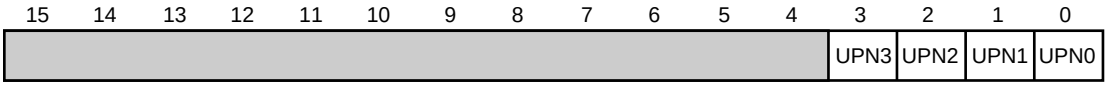
0: Indicates that the corresponding cause is not responsible for the first discarding of a cell.

1: Indicates that the corresponding cause is responsible for the first discarding of a cell.

Field	Bit	R/W	Function	Default Value
HEC	bit [15]	R	Indicates that a cell has been discarded because an HEC error was found as a result of checking the header area of a received cell. When the HM bit of the MODE register is set to “1”, the HEC error cell is not discarded; therefore, this bit indicates nothing.	0
CRC	bit [14]	R	Indicates a cell has been discarded because a CRC-10 error was found as a result of checking the payload area of a received cell that is an RM cell of PTI = “110” & PID = “01h”.	0
IPN	bit [4:0]	R	Indicates the number of the logical input port that has received the cell responsible for the HEC error or CRC-10 error. 00h to 17h: Indicates logical input port 0 to 23.	1Fh

4.3.10 Input port overrun error discard indication register (001Ch)

Register name	Address	Default	R/W
ERINOV	001Ch	xxxx_xxxx_xxxx_0000	R



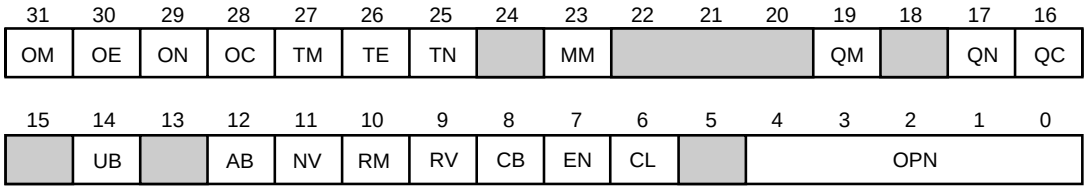
The ERINOV register indicates a port number of the UTOPIA receive interface that has caused a cell to be discarded. A cell is discarded because the internal receive FIFO of the μPD98410 overruns if the relation between the UTOPIA clock and system clock (SWCLK) described in **3.1 UTOPIA Interface** is not satisfied. When a cell is discarded, the corresponding bit of this register is set and, at the same time, the IN bit of the status register is set. Even while the IN bit is set, this register is updated.

If a cell is discarded because of the above cause, it does not count the number of discarded cells. If a cell has been discarded because the relation between the UTOPIA clock and system clock is not satisfied, the clocks must be reviewed.

Field	Bit	R/W	Function	Default Value
UPN3 - UPN0	bit [3:0]	R	Indicates the port number of the UTOPIA interface responsible for discarding a cell by bit map. 0: Indicates that the corresponding UTOPIA interface did not cause a cell to be discarded. 1: Indicates that the corresponding UTOPIA interface caused a cell to be discarded.	0h

4.3.11 Threshold value exceeding discard cell count enable register (0020h)

Register name	Address	Default	R/W
CTENTH	0020h	0000_000x_0xxx_0x00_x0x0_0000_00x0_0000	R/W

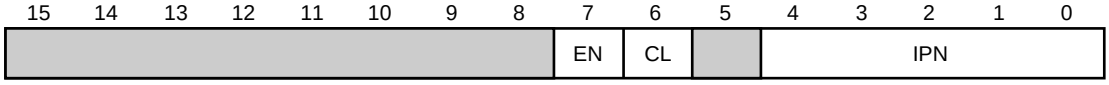


The CTENTH register specifies the conditions under which cells discarded because a threshold value is exceeded are counted. The count value is indicated by the CTEXTH register. The CTENTH register gives the conditions of the corresponding threshold value, class, and output port, and enables counting the number of discarded cells by using the EN bit.

Field	Bit	R/W	Function	Default Value
OM, OE, ON, OC, TM, TE, TN, MM, QM, QN, QC	bit [31:25, 23, 19, 17, 16]	R/W	Specifies a threshold value by which the number of discarded cells is to be counted. For the correspondence between each of these bits and a threshold value, refer to the description of the EXTH register. The OE and TE bits count OE and TE causes if either of the bits is set. 0: Does not count the number of cells discarded because a threshold value is exceeded. 1: Counts the number of cells discarded because a threshold value is exceeded.	0
UB, AB, NV, RM, RV, CB	bit [14, 12:8]	R/W	Specifies a class in which the number of cells discarded because a threshold value is exceeded is counted. For the correspondence between each of these bits and a threshold value, refer to the description of the EXTH register. 0: Does not count the number of discarded cells in the corresponding class. 1: Counts the number of discarded cells in the corresponding class.	0
EN, CL	bit [7:6]	R/W	Enables or disables counting of the number of cells discarded because a threshold value is exceeded. 0x: Disables counting the number of cells discarded because a threshold value is exceeded. 10: Enables counting the number of cells discarded because a threshold value is exceeded. 11: Enables counting the number of cells discarded because a threshold value is exceeded, after the CTEXTH has been cleared. However, reset the EN bit to “0”, and then set EN and CL to “1”.	00
OPN	bit [4:0]	R/W	Specifies an output port that counts the number of cells discarded because a threshold value is exceeded. MM, QM, QN, and QC causes are counted only when OPN is set to “1Fh”. 00h to 17h : Counts discarding of cells by the corresponding output port 0 to 23. 1Fh : Counts discarding of cells by all the logical output ports.	00h

4.3.12 Header translation error discard cell count enable register (0024h)

Register name	Address	Default	R/W
CTENHT	0024h	xxxx_xxxx_00x0_0000	R/W

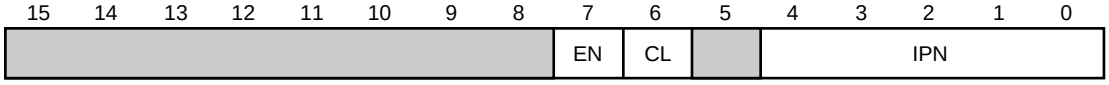


The CTENHT register specifies a logical input port that counts the number of cells discarded because a header translation error occurs. The counted value is indicated by the CTERHT register. IPN gives a condition, and the EN bit enables counting.

Field	Bit	R/W	Function	Default Value
EN, CL	bit [7:6]	R/W	Enables or disables counting of the number of cells discarded because of occurrence of a header translation error. 0x: Does not count the number of cells discarded due to occurrence of a header translation error. 10: Counts the number of cells discarded due to occurrence of a header translation error. 11: Clears CTERHT, and counts the number of cells discarded due to occurrence of a header translation error. However, reset the EN bit to “0”, and then set EN and CL to “1”.	00
IPN	bit [4:0]	R/W	Specifies a logical input port that counts the number of cells discarded because of the occurrence of a header translation error. Only discarding a cell due to the IM cause (discarding a cell due to multi-cast bit map (MB)) is counted only when IPN is set to “1Fh”. 00h to 17h: Counts the number of cells discarded because a header translation error has been caused by a source other than IM in the corresponding logical input port 0 to 23. 1Fh : Counts the number of cells discarded because of the header translation error in all the logical input ports.	00h

4.3.13 HEC/CRC error discard cell count enable register (0026h)

Register name	Address	Default	R/W
CTENHEC	0026h	xxxx_xxxx_00x0_0000	R/W

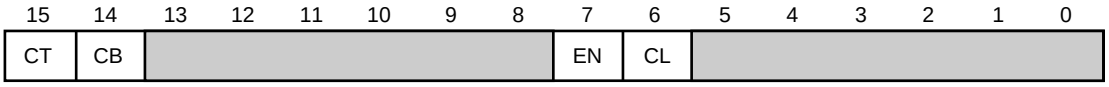


The CTENHEC register specifies a logical input port that counts the number of cells discarded because an HEC or CRC error occurs. The counted value is indicated by the CTERHEC register. IPN givens a condition, and the EN bit enables counting. While the HM bit of the MODE register is set to “1”, the HEC error cell is not discarded; therefore, the discarded cell is not counted.

Field	Bit	R/W	Function	Default Value
EN, CL	bit [7:6]	R/W	Enables or disables counting of the number of cells discarded due to an HEC/CRC error. 0x: Disables counting of the cells discarded due to an HEC/CRC error. 10: Enables counting of the cells discarded due to an HEC/CRC error. 11: Clears CTERHT, and enables counting of the cells discarded due to an HEC/CRC error. However, reset the EN bit to “0”, and set EN and CL to “1”.	00
IPN	bit [4:0]	R/W	Specifies a logical input port that counts the number of cells discarded due to an HEC/CRC error. 00h to 17h : Counts the number of cells discarded of the corresponding logical input port 0 to 23. 1Fh : Counts the number of cells discarded of all the logical input port.	00h

4.3.14 Control/cell buffer memory shortage discard cell count enable register (0028h)

Register name	Address	Default	R/W
CTENMEM	0028h	00xx_xxxx_00xx_xxxx	R/W

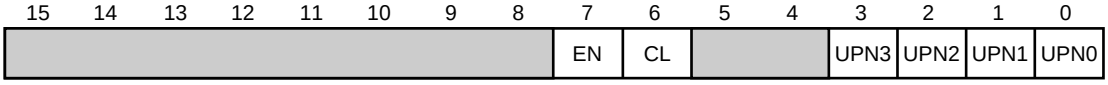


The CTENMEM register specifies whether the number of cells discarded because the vacant control area of the HTT & control memory or the vacant area of the cell buffer memory has run short is counted. The counted value is not indicated by the CTMEMEMP register. Counting is enabled by the EN bit.

Field	Bit	R/W	Function	Default Value
CT	bit [15]	R/W	Specifies whether the number of cells discarded because the control area of the HTT & control memory has run short is counted. 0: Does not count the number of cells discarded because the vacant area of the control memory has run short. 1: Counts the number of cells discarded because the vacant area of the control memory has run short.	0
CB	bit [14]	R/W	Specifies whether the number of cells discarded because the vacant area of the cell buffer memory has run short is counted. 0: Does not count the number of cells discarded because the vacant area of the cell buffer memory has run short. 1: Counts the number of cells discarded because the vacant area of the cell buffer memory has run short.	0
EN, CL	bit [7:6]	R/W	Enables or disables counting the number of cells discarded because the vacant area of the control memory or cell buffer memory has run short. 0x: Does not count the number of cells discarded because the vacant area of the control memory or cell buffer memory has run short. 10: Counts the number of cells discarded because the vacant area of the control memory or cell buffer memory has run short. 11: Clears CTMEMEMP and then counts the number of cells discarded because the vacant area of the control memory or cell buffer memory has run short. However, reset the EN bit to “0”, and set EN and CL to “1”.	00

4.3.15 Receive cell count enable register (002Ah)

Register name	Address	Default	R/W
CTENRCV	002Ah	xxxx_xxxx_00xx_0000	R/W

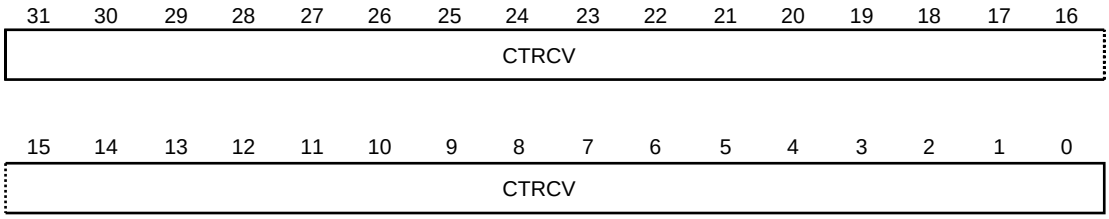


The CTENRCV register specifies whether the number of cells received by each UTOPIA interface port is counted. The counted value is indicated by the CTRCV register. The EN bit enables counting.

Field	Bit	R/W	Function	Default Value
EN, CL	bit [7:6]	R/W	Enables or disables the number of cells received. 0x: Does not count the number of received cells. 10: Counts the number of received cells. 11: Clears CTRCV, and counts the number of received cells. However, reset the EN bit to “0”, and set EN and CL to “1”.	00
UPN3 - UPN0	bit [3:0]	R/W	Specifies a UTOPIA interface port number that counts the number of received cells by bit map. 0: Does not count the number of received cells of the corresponding UTOPIA interface port. 1: Counts the number of received cells of the corresponding UTOPIA interface port.	0h

4.3.16 Receive cell count register (002Ch)

Register name	Address	Default	R/W
CTRCV	002Ch	0000_0000_0000_0000_0000_0000_0000_0000	R/W



The CTRCV register indicates the number of cells received under the condition specified by the CTENRCV register. The number of cells is counted while EN of the CTENRCV register is “1”. The value of this register is cleared when the reset signal is applied to the μPD98410 and when CL and EN of the CTENRCV register are set to “1”.

If a cell is received when the count value is “FFFFFFFFh”, the CRV bit of the status bit is set, an interrupt request is issued to the microprocessor, the count value is reset to “00000000h”, and counting continues. If the CRV bit of the INTMASK register is “0”, the interrupt request is not issued to the microprocessor.

Field	Bit	R/W	Function	Default Value
CTRCV	bit [31:0]	R/W	00000000h to FFFFFFFFh: Indicates the number of received cells.	0000_0000h

Remark The CTRCV register indicates the total number of received cells of the specified UTOPIA interface port. For example, if the CTENRCV register is set to EN = 1, CL = 0, UPN0 = UPN2 = 1, and UPN1 = UPN3 = 0, the CTRCV register indicates the total number of cells received from all the PHY devices connected to UTOPIA0 and UTOPIA2.

4.3.17 Threshold value exceeding discard cell count register (0030h)

Register name	Address	Default	R/W
CTEXTH	0030h	0000_0000_0000_0000_0000_0000_0000_0000	R/W

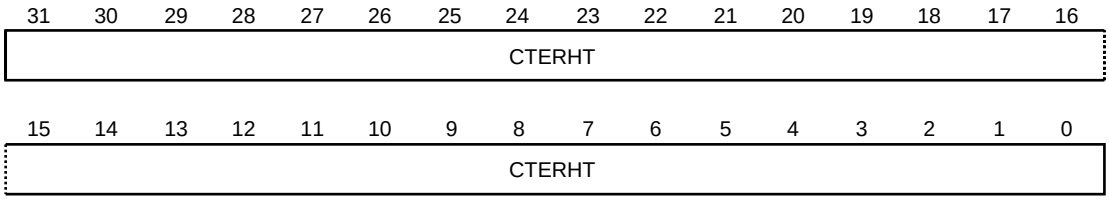
The CTEXTH register indicates the number of cells discarded under the condition specified by the CTENTH register. Counting is performed when EN of the CTENTH register is “1”, and is cleared when the reset signal is applied to the μPD98410 and when CL and EN of the CTENTH register are “1”.

If a cell is discarded when the count value is “FFFFFFFFh”, the CEX bit of the status register is set, an interrupt request is issued to the microprocessor, the count value is cleared to “00000000h”, and counting continues. If the CEX bit of the INTMASK register is “0”, no interrupt request is issued to the microprocessor.

Field	Bit	R/W	Function	Default Value
CTEXTH	bit [31:0]	R/W	00000000h to FFFFFFFFh: Indicates the number of discarded cells.	0000_0000h

4.3.18 Header translation error discard cell count register (0034h)

Register name	Address	Default	R/W
CTERHT	0034h	0000_0000_0000_0000_0000_0000_0000_0000	R/W



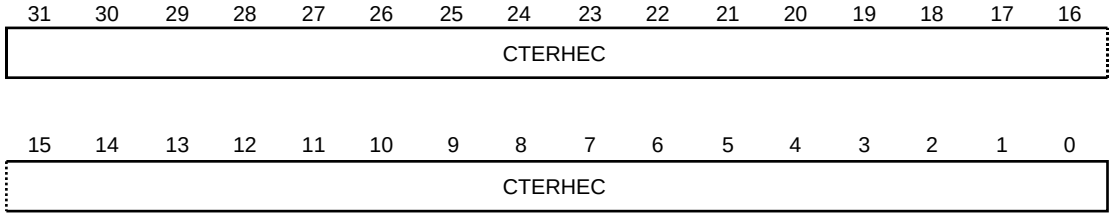
The CTERTH register indicates the number of cells discarded under the condition specified by the CTENHT register. Counting is performed when EN of the CTENHT register is “1”, and is cleared when the reset signal is applied to the μPD98410 and when CL and EN of the CTENHT register are “1”.

If a cell is discarded when the count value is “FFFFFFFFh”, the CHT bit of the status register is set, an interrupt request is issued to the microprocessor, the count value is cleared to “00000000h”, and counting continues. If the CHT bit of the INTMASK register is “0”, no interrupt request is issued to the microprocessor.

Field	Bit	R/W	Function	Default Value
CTERHT	bit [31:0]	R/W	00000000h to FFFFFFFFh: Indicates the number of discarded cells.	0000_0000

4.3.19 HEC/CRC error discard cell count register (0038h)

Register name	Address	Default	R/W
CTERHEC	0038h	0000_0000_0000_0000_0000_0000_0000_0000	R/W



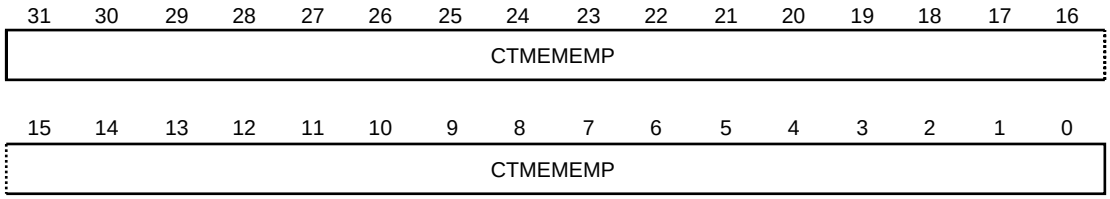
The CTERHEC register indicates the number of cells discarded under the condition specified by the CTENHEC register. Counting is performed when EN of the CTENHEC register is “1”, and is cleared when the reset signal is applied to the μPD98410 and when CL and EN of the CTENHEC register are “1”. Counting is not performed when the HM bit of the MODE register is set to “1” because the HEC error cell is not discarded.

If a cell is discarded when the count value is “FFFFFFFFh”, the CHE bit of the status register is set, an interrupt request is issued to the microprocessor, the count value is cleared to “00000000h”, and counting continues. If the CHE bit of the INTMASK register is “0”, no interrupt request is issued to the microprocessor.

Field	Bit	R/W	Function	Default Value
CTERHEC	bit [31:0]	R/W	00000000h to FFFFFFFFh: Indicates the number of discarded cells.	0000_0000h

4.3.20 Control/cell buffer memory shortage discard cell count register (003Ch)

Register name	Address	Default	R/W
CTMEMEMP	003Ch	0000_0000_0000_0000_0000_0000_0000_0000	R/W



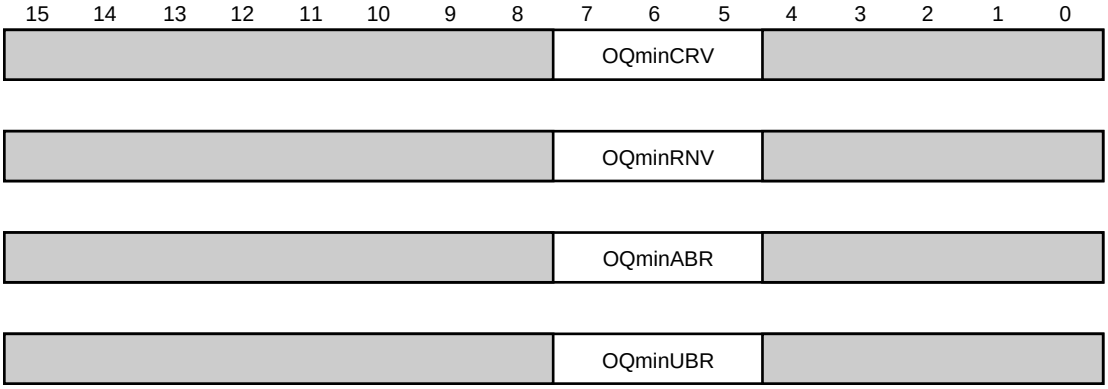
The CTMEMEMP register indicates the number of cells discarded because the vacant area in the control memory or cell buffer memory has run short. When the CT bit of the CTENMEM register is set to “1”, the number of cells discarded because the vacant area of the control memory has run short is counted; when the CB bit of the CTENMEM register is set to “1”, the number of cells discarded because the vacant area of the cell buffer memory has run short is counted. Counting is performed while EN of the CTENMEM register is “1”, and is cleared when the reset signal is applied to the μPD98410 and when CL and EN of the CTENMEM register are set to “1”.

If a cell is discarded when the count value is “FFFFFFFFh”, the CME bit of the status register is set to 1, an interrupt request is issued to the microprocessor, the count value is cleared to “00000000h”, and counting continues. If the CME bit of the INTMASK register is “0”, no interrupt request is issued to the microprocessor.

Field	Bit	R/W	Function	Default Value
CTMEMEMP	bit [31:0]	R/W	00000000h to FFFFFFFFh: Indicates the number of cells discarded.	0000_0000h

4.3.21 Output queue minimum threshold value registers (0040h, 0044h, 0048h, 004Ch)

Register name	Address	Default	R/W
OQminCRV	0040h	xxxx_xxxx_000x_xxxx	R/W
OQminRNV	0044h	xxxx_xxxx_000x_xxxx	R/W
OQminABR	0048h	xxxx_xxxx_000x_xxxx	R/W
OQminUBR	004Ch	xxxx_xxxx_000x_xxxx	R/W



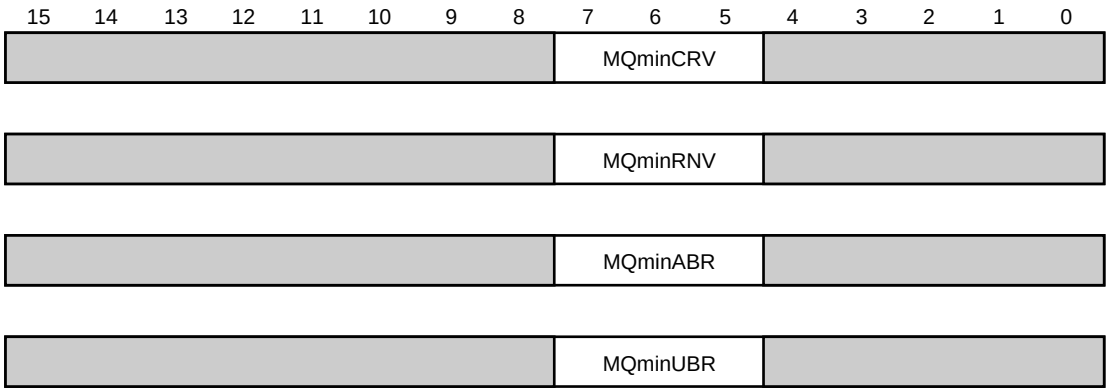
These registers specify the minimum number of guaranteed cells for each logical output port.

Be sure to set the minimum threshold value before enabling the switching operation by using the CMD register. Once the switching operation has been enabled, do not re-set the threshold value; otherwise, queue management cannot be guaranteed and the μPD98410 will malfunction.

Field	Bit	R/W	Function	Default Value
OQminCRV	bit [7:5]	R/W	000 to 111: Minimum number of guaranteed cells in CBR + rtVBR class (in 32-cell units: 0/32/64/ ... /224)	000 (0000h)
OQminRNV	bit [7:5]	R/W	000 to 111: Minimum number of guaranteed cells in RM + nrtVBR class (in 32-cell units: 0/32/64/ ... /224)	000 (0000h)
OQminABR	bit [7:5]	R/W	000 to 111: Minimum number of guaranteed cells in ABR class (in 32-cell units: 0/32/64/ ... /224)	000 (0000h)
OQminUBR	bit [7:5]	R/W	000 to 111: Minimum number of guaranteed cells in UBR class (in 32-cell units: 0/32/64/ ... /224)	000 (0000h)

4.3.22 Multi-cast queue minimum threshold value registers (0050h, 0054h, 0058h, 005Ch)

Register name	Address	Default	R/W
MQminCRV	0050h	xxxx_xxxx_000x_xxxx	R/W
MQminRNV	0054h	xxxx_xxxx_000x_xxxx	R/W
MQminABR	0058h	xxxx_xxxx_000x_xxxx	R/W
MQminUBR	005Ch	xxxx_xxxx_000x_xxxx	R/W



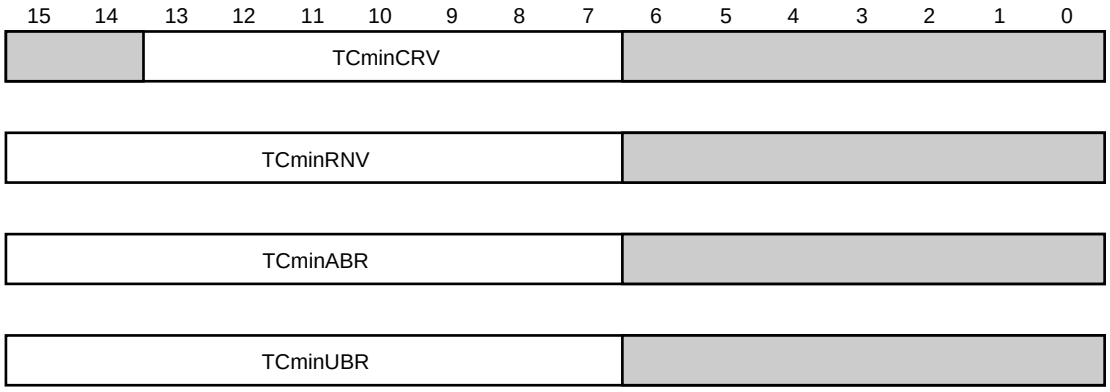
These registers specify the minimum number of guaranteed cells for the multi-cast in each class.

Be sure to set the minimum threshold value before enabling the switching operation by using the CMD register. Once the switching operation has been enabled, do not re-set the threshold value; otherwise, queue management cannot be guaranteed and the μPD98410 will malfunction.

Field	Bit	R/W	Function	Default Value
MQminCRV	bit [7:5]	R/W	000 to 111: Minimum number of guaranteed cells in CBR + rtVBR class (in 32-cell units: 0/32/64/ ... /224)	000 (0000h)
MQminRNV	bit [7:5]	R/W	000 to 111: Minimum number of guaranteed cells in RM + nrtVBR class (in 32-cell units: 0/32/64/ ... /224)	000 (0000h)
MQminABR	bit [7:5]	R/W	000 to 111: Minimum number of guaranteed cells in ABR class (in 32-cell units: 0/32/64/ ... /224)	000 (0000h)
MQminUBR	bit [7:5]	R/W	000 to 111: Minimum number of guaranteed cells in UBR class (in 32-cell units: 0/32/64/ ... /224)	000 (0000h)

4.3.23 TC (Total Cell) counter minimum threshold registers (0060h, 0064h, 0068h, 006Ch)

Register name	Address	Default	R/W
TCminCRV	0060h	xx00_0000_0xxx_xxxx	R/W
TCminRNV	0064h	0000_0000_0xxx_xxxx	R/W
TCminABR	0068h	0000_0000_0xxx_xxxx	R/W
TCminUBR	006Ch	0000_0000_0xxx_xxxx	R/W



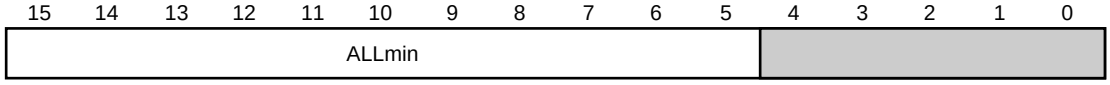
These registers specify the minimum number of guaranteed cells for each class. The minimum number of cells guaranteed for each class is counted after the number of cells has exceeded the minimum number of guaranteed cells for each logical output port.

Be sure to set the minimum threshold value before enabling the switching operation by using the CMD register. Once the switching operation has been enabled, do not re-set the threshold value; otherwise, queue management cannot be guaranteed and the μPD98410 will malfunction.

Field	Bit	R/W	Function	Default Value
TCminCRV	bit [13:7]	R/W	00_0000_0 to 11_1111_1: Minimum number of guaranteed cells in CBR + rtVBR class (in 128-cell units: 0/128/256/ ... /16256)	00_0000_0 (0000h)
TCminRNV	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: Minimum number of guaranteed cells in RM + nrtVBR class (in 128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)
TCminABR	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: Minimum number of guaranteed cells in ABR class (in 128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)
TCminUBR	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: Minimum number of guaranteed cells in UBR class (in 128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)

4.3.24 Total number of cells minimum threshold value register (007Eh)

Register name	Address	Default	R/W
ALLmin	007Eh	0000_0000_000x_xxxx	R/W



The ALLmin register specifies the total of the minimum number of guaranteed cells. Before enabling the switching operation by using the CMD register, be sure to set the value calculated by the following expression to the CMD register. Once the switching operation has been enabled, do not re-set ALLmin register; otherwise, queue management cannot be guaranteed and the μPD98410 will malfunction.

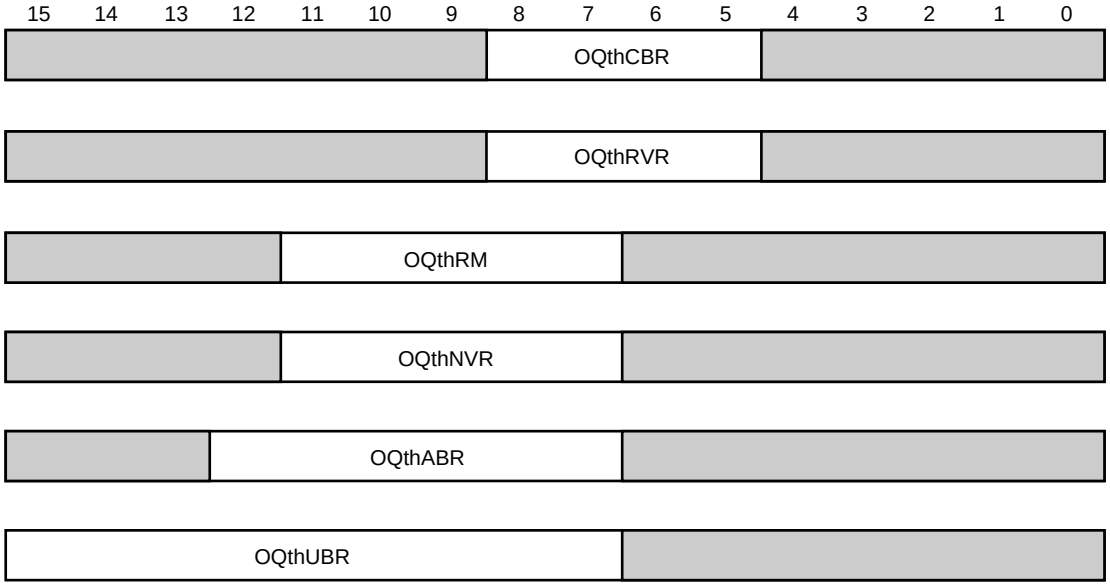
(OQminCRV + OQminRNV + OQminABR + OQminUBR) $\times$ enabled ports[Note]
+ MQminCRV + MQminRNV + MQminABR + MQminUBR
+ TCminCRV + TCminRNV + TCminABR + TCminUBR

Note "enabled ports" indicates the total number of logical ports scheduled to enable the EN bit of the PT register.

Field	Bit	R/W	Function	Default Value
ALLmin	bit [15:5]	R/W	0000_0000_000 to 1111_1111_111: Total of minimum number of guaranteed cells (in 32-cell units: 0/32/64 ... /65504)	0000_0000_000 (0000h)

4.3.25 Output queue maximum threshold value registers (0080h, 0082h, 0090h, 0092h, 00A0h, 00B0h)

Register name	Address	Default	R/W
OQthCBR	0080h	xxxx_xxx0_000x_xxxx	R/W
OQthRVR	0082h	xxxx_xxx0_000x_xxxx	R/W
OQthRM	0090h	xxxx_0000_0xxx_xxxx	R/W
OQthNVR	0092h	xxxx_0000_0xxx_xxxx	R/W
OQthABR	00A0h	xxx0_0000_0xxx_xxxx	R/W
OQthUBR	00B0h	0000_0000_0xxx_xxxx	R/W



These registers set the upper-limit threshold value of each logical output port in each class. If a cell in each class is congested in the output queue, exceeding the corresponding threshold value, the cell is discarded.

Field	Bit	R/W	Function	Default Value
OQthCBR	bit [8:5]	R/W	0_000 to 1_111: Upper-limit threshold value in CBR class (32-cell units: 0/32/64/ ... /480)	0_000 (0000h)
OQthRVR	bit [8:5]	R/W	0_000 to 1_111: Upper-limit threshold value in rtVBR class (32-cell units: 0/32/64/ ... /480)	0_000 (0000h)
OQthRM	bit [11:7]	R/W	0000_0 to 1111_1: Upper-limit threshold value in RM class (128-cell units: 0/128/256/ ... /3968)	0000_0 (0000h)
OQthNVR	bit [11:7]	R/W	0000_0 to 1111_1: Upper-limit threshold value in nrtVBR class (128-cell units: 0/128/256/ ... /3968)	0000_0 (0000h)
OQthABR	bit [12:7]	R/W	0_0000_0 to 1_1111_1: Upper-limit threshold value in ABR class (128-cell units: 0/128/256/ ... /8046)	0_0000_0 (0000h)
OQthUBR	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: Upper-limit threshold value in UBR class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)

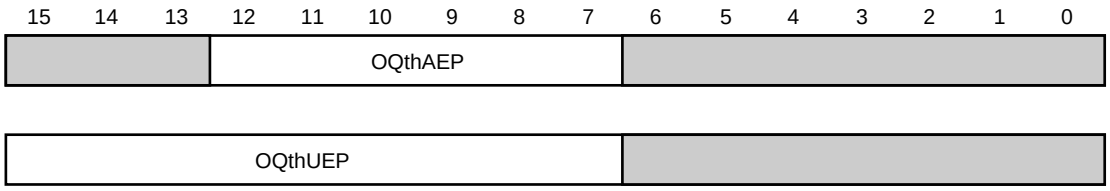
Remarks 1. OQthCBR and OQthRVR are the threshold values for the same output queue.

2. OQthRM and OQthNVR are the threshold values for the same output queue.

3. For cells in ABR and UBR classes for which EPD is disabled, OQthAEP and OQthUEP are the upper-limit threshold values.

4.3.26 Output queue EPD threshold value registers (00A2h, 00B2h)

Register name	Address	Default	R/W
OQthAEP	00A2h	xxx0_0000_0xxx_xxxx	R/W
OQthUEP	00B2h	0000_0000_0xxx_xxxx	R/W



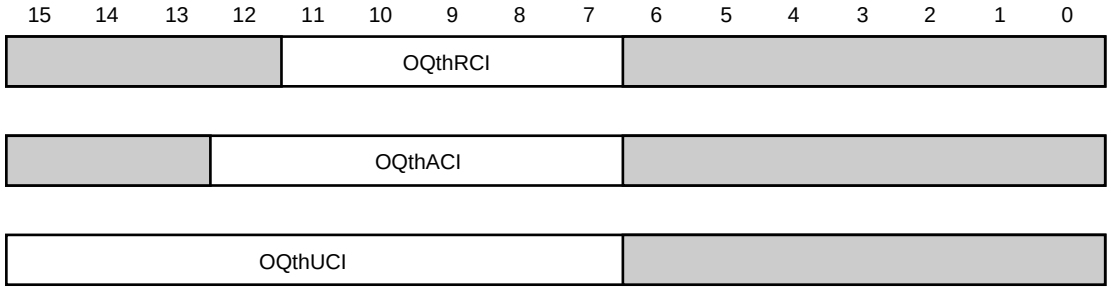
These registers set the EPD threshold value of each logical output port in each class. If a cell in each class is congested in the output queue, exceeding the corresponding threshold value, an EPD control operation is performed, and the following processing is executed:

- EPD valid cell : Cells belonging to the newly received packet are discarded. The last cell (EOP) of the packet is received, however.
- EPD invalid cell : The cell is discarded.

Field	Bit	R/W	Function	Default Value
OQthAEP	bit [12:7]	R/W	0_0000_0 to 1_1111_1: EPD threshold value in ABR class (128-cell units: 0/128/256/ ... /8046)	0_0000_0 (0000h)
OQthUEP	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: EPD threshold value in UBR class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)

4.3.27 Output queue EFCI threshold value registers (0094h, 00A4h, 00B4h)

Register name	Address	Default	R/W
OQthRCI	0094h	xxxx_0000_0xxx_xxxx	R/W
OQthACI	00A4h	xxx0_0000_0xxx_xxxx	R/W
OQthUCI	00B4h	0000_0000_0xxx_xxxx	R/W

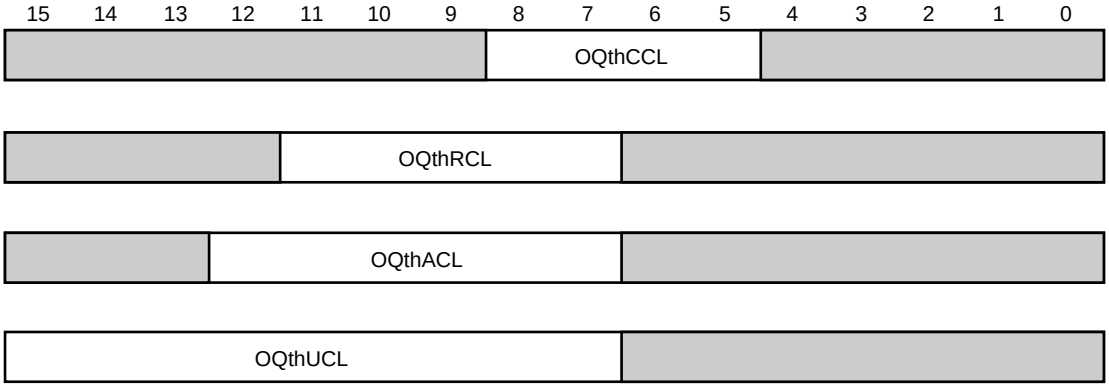


These registers set the EFCI threshold value of each logical output port in each class. If a cell in each class is congested in the output queue, exceeding the corresponding threshold value, EFCI marking is performed of the user cells and CI/NI marking is performed for the backward RM cells.

Field	Bit	R/W	Function	Default Value
OQthRCI	bit [11:7]	R/W	0000_0 to 1111_1: EFCI threshold value in RM + nrtVBR class (128-cell units: 0/128/256/ ... /3968)	0000_0 (0000h)
OQthACI	bit [12:7]	R/W	0_0000_0 to 1_1111_1: EFCI threshold value in ABR class (also used as CI threshold value) (128-cell units: 0/128/256/ ... /8064)	0_0000_0 (0000h)
OQthUCI	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: EFCI threshold value in UBR class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)

4.3.28 Output queue CLP threshold value registers (0086h, 0096h, 00A6h, 00B6h)

Register name	Address	Default	R/W
OQthCCL	0086h	xxxx_xxx0_000x_xxxx	R/W
OQthRCL	0096h	xxxx_0000_0xxx_xxxx	R/W
OQthACL	00A6h	xxx0_0000_0xxx_xxxx	R/W
OQthUCL	00B6h	0000_0000_0xxx_xxxx	R/W

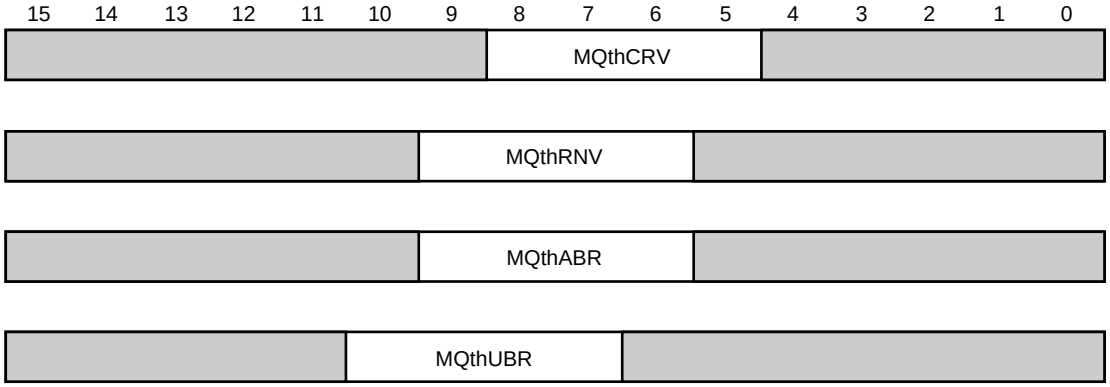


These registers set the CLP threshold value of each logical output port in each class. If a cell in each class is congested in the output queue, exceeding the corresponding threshold value, the cell for which CLP is set is discarded.

Field	Bit	R/W	Function	Default Value
OQthCCL	bit [8:5]	R/W	0_000 to 1_111: CLP threshold value in CBR + rtVBR class (32-cell units: 0/32/64/ ... / 480)	0_000 (0000h)
OQthRCL	bit [11:7]	R/W	0000_0 to 1111_1: CLP threshold value in RM + nrtVBR class (128-cell units: 0/128/256/ ... /3968)	0000_0 (0000h)
OQthACL	bit [12:7]	R/W	0_0000_0 to 1_1111_1: CLP threshold value in ABR class (128-cell units: 0/128/256/ ... /8064)	0_0000_0 (0000h)
OQthUCL	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: CLP threshold value in UBR class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)

4.3.29 Multi-cast queue maximum threshold value registers (00C0h, 00C4h, 00C8h, 00CCh)

Register name	Address	Default	R/W
MQthCRV	00C0h	xxxx_xxx0_000x_xxxx	R/W
MQthRNV	00C4h	xxxx_xx00_00xx_xxxx	R/W
MQthABR	00C8h	xxxx_xx00_00xx_xxxx	R/W
MQthUBR	00CCh	xxxx_x000_0xxx_xxxx	R/W

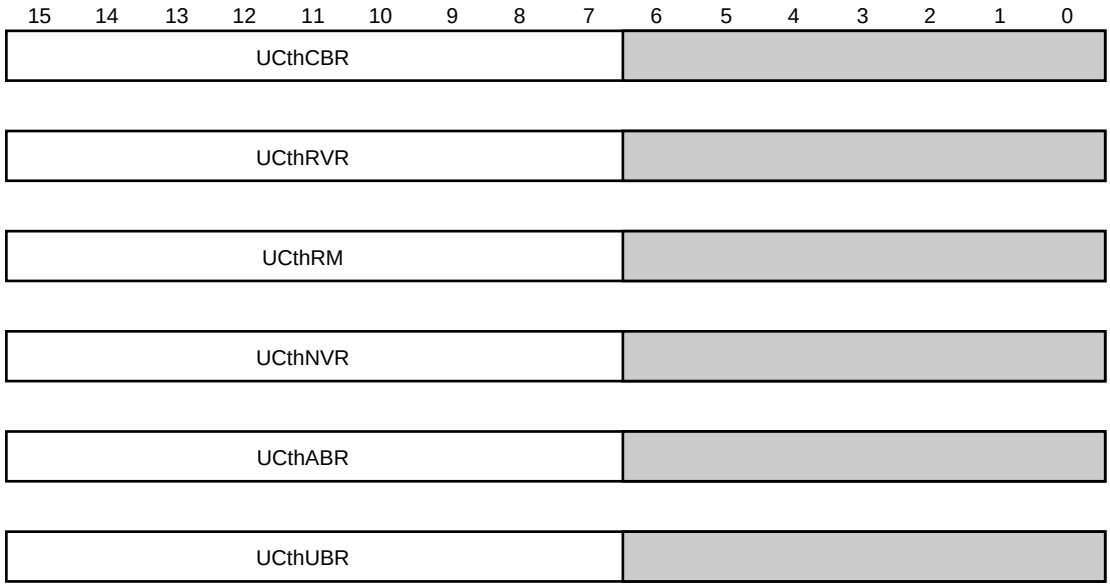


These registers set the upper-limit threshold value of the multi-cast queue in each class. If a cell in each class is congested in the multi-cast queue, exceeding the corresponding threshold value, the cell is discarded.

Field	Bit	R/W	Function	Default Value
MQthCRV	bit [8:5]	R/W	0_000 to 1_111: Upper-limit threshold value in CBR + rtVBR class (32-cell units: 0/32/64/ ... /480)	0_000 (0000h)
MQthRNV	bit [9:6]	R/W	00_00 to 11_11: Upper-limit threshold value in RM + nrtVBR class (64-cell units: 0/64/128/ ... /960)	00_00 (0000h)
MQthABR	bit [9:6]	R/W	00_00 to 11_11: Upper-limit threshold value in ABR class (64-cell units: 0/64/128/ ... /960)	00_00 (0000h)
MQthUBR	bit [10:7]	R/W	000_0 to 111_1: Upper-limit threshold value in UBR class (128-cell units: 0/128/256/ ... /1920)	000_0 (0000h)

4.3.30 UC (Used Cell) counter maximum threshold value register (00D0h, 00D4h, 00D8h, 00DCh, 00E0h, 00E8h)

Register name	Address	Default	R/W
UCthCBR	00D0h	0000_0000_0xxx_xxxx	R/W
UCthRVR	00D4h	0000_0000_0xxx_xxxx	R/W
UCthRM	00D8h	0000_0000_0xxx_xxxx	R/W
UCthNVR	00DCh	0000_0000_0xxx_xxxx	R/W
UCthABR	00E0h	0000_0000_0xxx_xxxx	R/W
UCthUBR	00E8h	0000_0000_0xxx_xxxx	R/W



These registers set the upper-limit threshold value of the Used Cell Counter in each class. If a cell in each class is congested in the cell buffer, exceeding the corresponding threshold value, the cell is discarded.

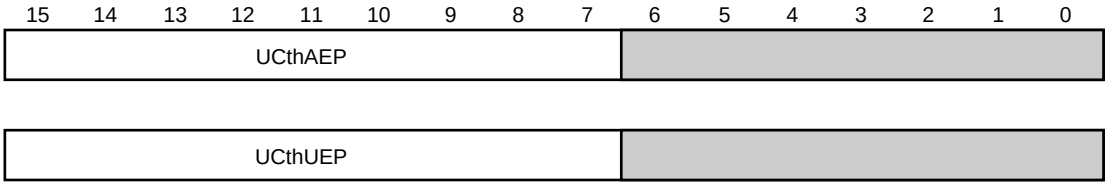
Field	Bit	R/W	Function	Default Value
UCthCBR	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: Upper-limit threshold value in CBR class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)
UCthRVR	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: Upper-limit threshold value in rtVBR class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)
UCthRM	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: Upper-limit threshold value in RM class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)
UCthNVR	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: Upper-limit threshold value in nrtVBR class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)

Field	Bit	R/W	Function	Default Value
UCthABR	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: Upper-limit threshold value in ABR class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)
UCthUBR	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: Upper-limit threshold value in UBR class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)

Remark For the cells in ABR and UBR classes for which EPD is disabled, UCthAEP and UCthUEP are the upper-limit values.

4.3.31 UC (Used Cell) Counter EPD threshold value registers (00E2h, 00EAh)

Register name	Address	Default	R/W
UCthAEP	00E2h	0000_0000_0xxx_xxxx	R/W
UCthUEP	00EAh	0000_0000_0xxx_xxxx	R/W



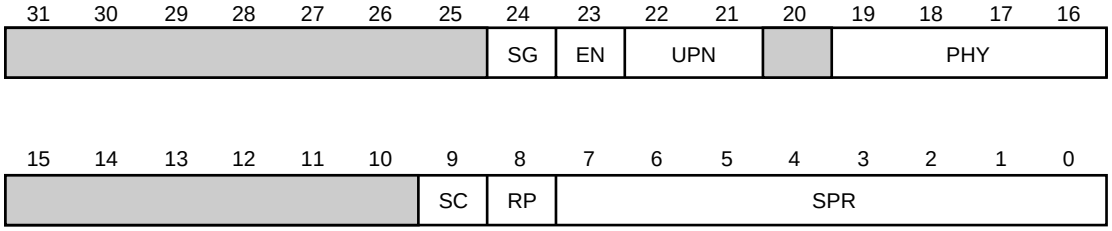
To these registers, the EPD threshold values of the Used Cell Counter in each class are set. If a cell in each class is congested in the cell buffer, exceeding the corresponding threshold value, the EPD control operation is performed and the following processing is executed:

- EPD valid cell: The cell belonging to a newly received packet is discarded. The last packet (EOP) is received, however.
- EPD invalid cell: The cell is discarded.

Field	Bit	R/W	Function	Default Value
UCthAEP	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: EPD threshold value in ABR class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)
UCthUEP	bit [15:7]	R/W	0000_0000_0 to 1111_1111_1: EPD threshold value in UBR class (128-cell units: 0/128/256/ ... /65408)	0000_0000_0 (0000h)

4.3.32 Port configuration register

Register name	Address	Default	R/W
PT0-PT23	**Note**	xxxx_xxx0_000x_1111_xxxx_xx00_0000_0000	R/W



Note 0100h, 0104h, 0108h, 010Ch, 0110h, 0114h, 0118h, 011Ch, 0120h, 0124h, 0128h, 012Ch, 0130h, 0134h, 0138h, 013Ch, 0140h, 0144h, 0148h, 014Ch, 0150h, 0154h, 0158h, 015Ch

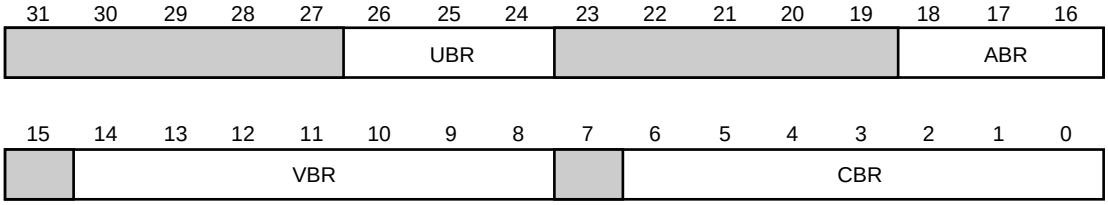
These registers are used to map physical ports to logical ports. Do not connect an unconnected PHY device (physical port) to a logical port; otherwise, the μPD98410 polls the PHY device that does not exist and malfunctions.

Field	Bit	R/W	Function	Default Value
SG	bit [24]	R/W	0: Connects a physical port mapped to the corresponding logical port in the multi-PHY connection mode. 1: Connects a physical port mapped to the corresponding logical port in the single PHY connection mode. When two or more physical ports are connected in the single PHY connection mode, the lowest logical port number of each UTOPIA interface is selected.	0
EN	bit [23]	R/W	0: Invalidates the corresponding logical port. 1: Validates the corresponding logical port.	0
UPN	bit [22:21]	R/W	00 to 11: Allocates UTOPIA interface 0 to 3.	00
PHY	bit [19:16]	R/W	0000 to 1011: Allocates PHY address 0 to 11.	1111
SC	bit [9]	R/W	Corrects errors by means of shaping control. If two or more output ports connected to the same UTOPIA interface transmits cells at the same time, one of the output ports is allowed to transmit a cell and output of the other ports is delayed to prevent the throughput from dropping. 0: Does not perform shaping error correction. 1: Performs shaping error correction.	0

Field	Bit	R/W	Function	Default Value
RP	bit [8]	R/W	Enables successive output to the same logical output port. 0: Does not performs successive output to the same logical output port. 1: Performs successive output to the same logical output port. Refer to **3.6 Successive Transmission**.	0
SPR	bit [7:0]	R/W	Specifies a shaping rate for a logical output port. Output is shaped to 1/(SPR + 1). If SPR = "1", for example, transmission is performed once in two basic cycles. The basic cycle is 1 cell processing cycle = 44 – SWCLK. 0000_0000 to 1111_1111: Sets shaping rate to 1/1 to 1/256.	0000_0000

4.3.33 Class priority control register

Register name	Address	Default	R/W
PC0-PC23	**Note**	xxxx_x000_xxxx_x001_x000_0001_x000_0001	R/W



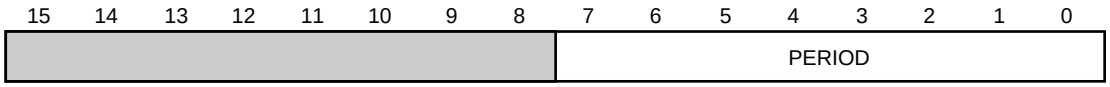
Note 0180h, 0184h, 0188h, 018Ch, 0190h, 0194h, 0198h, 019Ch, 01A0h, 01A4h, 01A8h, 01ACh, 01B0h, 01B4h, 01B8h, 01BC0h, 01C0h, 01C4h, 01C8h, 01CCh, 01D0h, 01D4h, 01D8h, 01DCh

These registers specify class priority control for each logical output port. For CBR + rtVBR class and RM + nrtVBR class, the number of cells enabled to be transmitted during the period specified by the PERIOD register is specified. For ABR class and UBR class, the transmission ratio is set to ABR:UBR.

Field	Bit	R/W	Function	Default Value
CBR	bit [6:0]	R/W	00h to 7Fh: Number of CBR + rtVBR cells enabled to be transmitted during PERIOD period.	01h
VBR	bit [14:8]	R/W	00h to 7Fh: Number of RM + nrtVBR cells enabled to be transmitted during PERIOD period.	01h
ABR	bit [18:16]	R/W	0h to 7h: Cell transmission ratio of ABR class (ratio is ABR:UBR)	1h
UBR	bit [26:24]	R/W	0h to 7h: Cell transmission ratio of UBR class (ratio is UBR:ABR)	0h

4.3.34 Cycle count register (01FCh)

Register name	Address	Default	R/W
PERIOD	01FCh	xxxx_xxxx_0000_0001	R/W

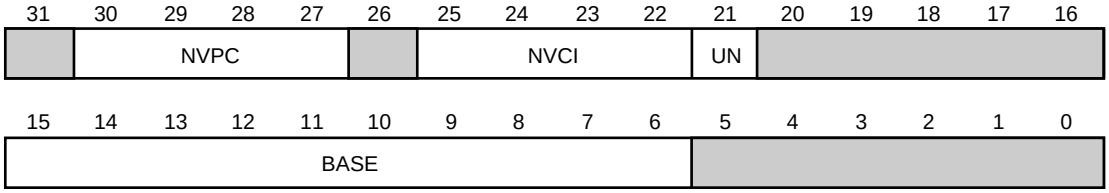


This register specifies the cycle of PC0 through PC23, CBR, and VBR. It performs class priority control of each logical output port, as well as setting of CBR and VBR for PC0 through PC23.

Field	Bit	R/W	Function	Default Value
PERIOD	bit [7:0]	R/W	00h to FFh: Cycle of class priority control	01h

4.3.35 Header translation configuration register

Register name	Address	Default	R/W
HT0-HT23	**Note**	x000_0x00_000x_xxxx_0000_0000_00xx_xxxx	R/W



Note 0200h, 0204h, 0208h, 020Ch, 0210h, 0214h, 0218h, 021Ch, 0220h, 0224h, 0228h, 022Ch, 0230h, 0234h, 0238h, 023Ch, 0240h, 0244h, 0248h, 024Ch, 0250h, 0254h, 0258h, 025Ch

This register is used to translate VPI and VCI of a received cell into the addresses of the header translation table (HTT), to translate the OVPC specified in HTT into VPC and VCI of a transmit cell, and specified NNI/UNI, for each logical output port.

Field	Bit	R/W	Function	Default Value
NVPC	bit [30:27]	R/W	6h to Fh: Valid number of VPI bits + valid number of VCI bits (6 bits to 15 bits)	0h
NVCI	bit [25:22]	R/W	6h to Fh: Valid number of VCI bits (6 bits to 15 bits)	0h
UN	bit [21]	R/W	0: Sets UNI. VPI of a received cell is treated as 8 bits, and VPI [11:8] in GFC field is treated as “don’t care”. If the invalid block of VPI is not “0” (VPI [7:(NVPC – NVCI – 1] ≠ 0), a header translation error occurs and the cell is discarded. The result is indicated by the HE bit of the status register and IH bit of the ERHT register. 1: Sets NNI. VPI of a received cell is treated as 12 bits, and if the invalid block of VPI is not 0 (VPI [11:(NVPC – NVCI – 1: ≠ 0), a header translation error occurs and the cell is discarded. The result is indicated by the HE bit of the status register and IH bit of the ERHT register.	0
BASE	bit [15:6]	R/W	0000_0000_00 to 1111_1111_11: HTT base address	000h

[MEMO]

CHAPTER 5 JTAG BOUNDARY SCAN

The μPD98410 has a JTAG boundary scan circuit.

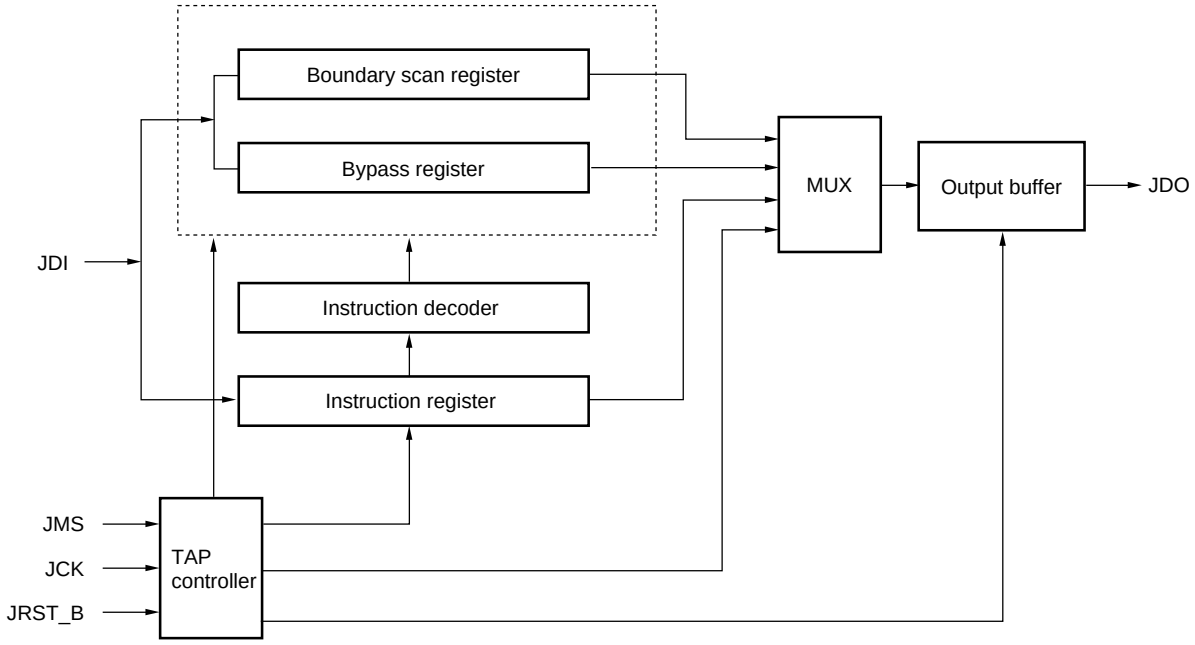
5.1 Features

- Conforms to IEEE1149.1 JTAG Boundary Scan Standard.
- Three registers dedicated to boundary scan
  - Instruction register
  - Bypass register
  - Boundary scan register
- Two instructions supported
  - BYPASS instruction
  - EXTEST instruction
- Five pins dedicated to boundary scan (five pins)
  - JCK (JTAG Clock)
  - JMS (JTAG Mode Select)
  - JDI (JTAG Data Input)
  - JDO (JTAG Data Output)
  - JRST_B (JTAG Reset)

5.2 Internal Configuration of Boundary Scan Circuit

Figure 5-1 shows the block diagram of the internal JTAG boundary scan circuit of the μPD98410.

Figure 5-1. Block Diagram of Boundary Scan Circuit



5.2.1 Instruction register

The instruction register consists of a 2-bit shift register and writes instruction data from the JDI pin. The register and instruction are selected by this instruction data.

5.2.2 TAP (Test Access Port) controller

The TAP controller changes operating state by latching the signal of the JMS pin at the rising edge of the clock input to the JCK pin.

5.2.3 Bypass register

The bypass register consists of a 1-bit shift register connected between the JDI and JDO pins when the TAP controller is in Shift-DR state. If this register is selected while the TAP controller is in Shift-DR state, data is shifted to the JDO pin at the rising edge of the clock input to the JCK pin.

When this register is selected, the operation of the JTAG boundary circuit does not influence on the operation of the μPD98410.

5.2.4 Boundary scan register

The boundary scan register is located between an external pin of the μPD98410 and internal logic circuit. When this register is selected, data is latched or loaded by the instruction of the TAP controller.

If this register is selected while the TAP controller is in Shift-DR state, data is output to the JDO pin starting from the LSB at the falling edge of the clock input to the JCK pin.

5.3 Pin Function

5.3.1 JCK (JTAG Clock) pin

The JCK pin is used to supply a clock signal to the JTAG boundary scan circuit (such as the bypass register, instruction register, and TAP controller. This clock signal is isolated so as not to be supplied to the other internal circuits of the μPD98410.

5.3.2 JMS (JTAG Mode Select) pin

Input to the JMS signal is latched at the rising edge of the clock input to the JCK pin and defines the operation of the TAP controller.

5.3.3 JDI (JTAG Data Input) pin

The JDI pin is an input pin that inputs data to the JTAG boundary scan circuit register.

5.3.4 JDO (JTAG Data Output) pin

The JDO pin is an output pin that outputs data from the JTAG boundary scan circuit. This pin changes its output at the falling edge of the clock input to the JCK pin. This pin is a three-state output pin and is controlled by the TAP controller.

5.3.5 JRST_B (JTAG Reset) pin

This pin asynchronously initializes the TAP controller. This reset signal sets the μPD98410 in the normal operation mode and the boundary register in non-operation state.

5.4 Operation Description

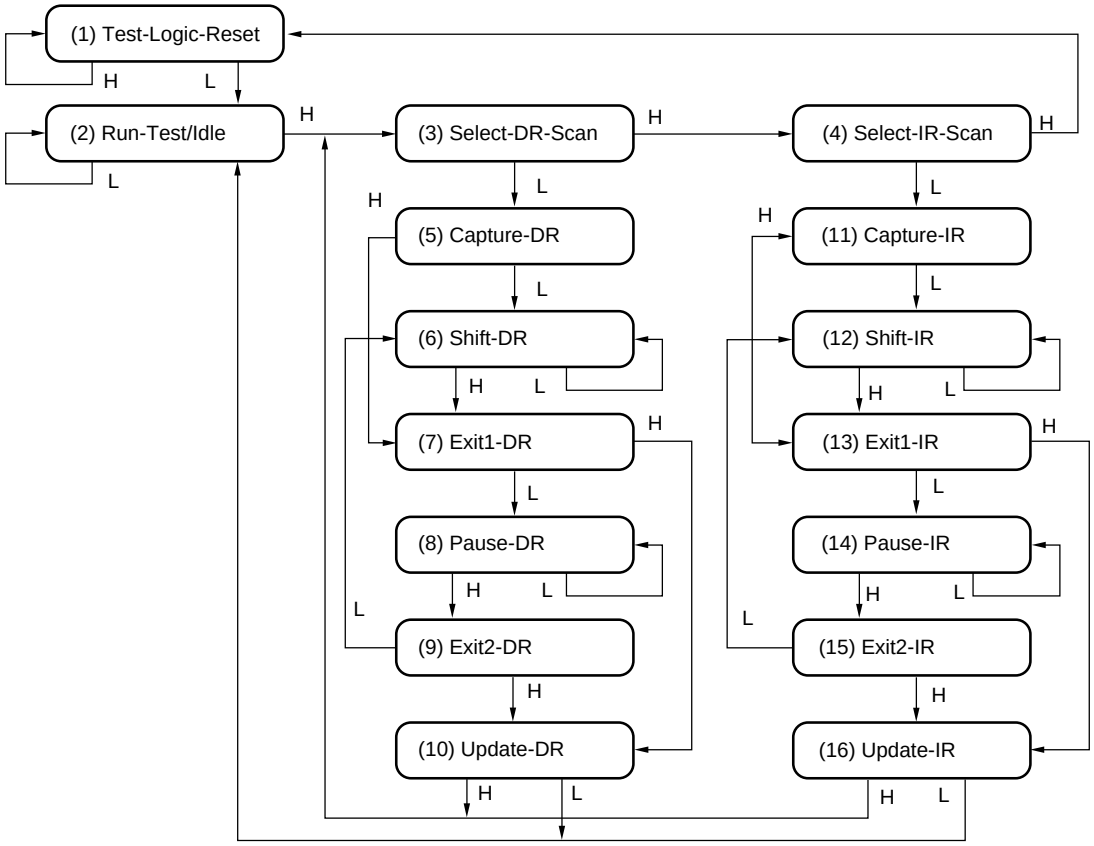
5.4.1 TAP controller

The TAP controller is a circuit having 16 states synchronized with changes of the JMS and JCK pins. Its operation is specified by IEEE Standard 1149.1.

5.4.2 TAP controller state

Figure 5-2 shows the state transition of the TAP controller. The state of the TAP controller is determined depending on the state of the JMS pin signal input at the rising edge of the clock input to the JCK pin. The operations of the instruction register, boundary scan register, and bypass register change at the rising or falling edge of the clock input to the JCK pin. (Refer to **Figure 5-3**).

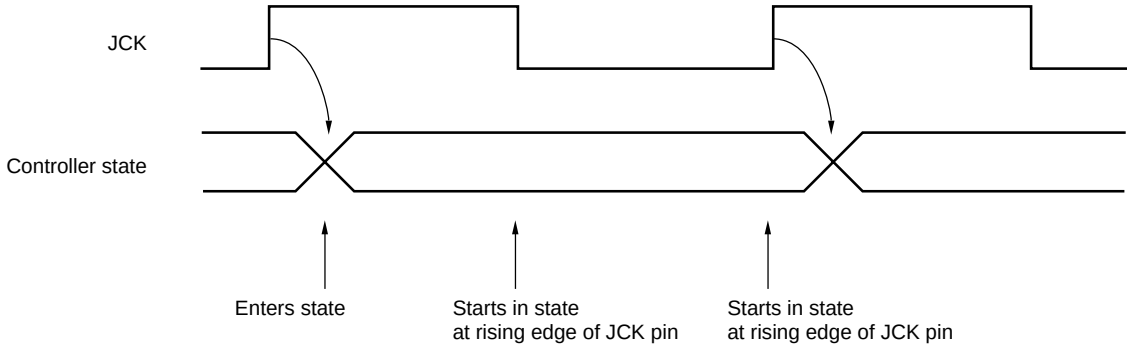
Figure 5-2. State Transition of TAP Controller



Remarks 1. "H" and "L" of the arrows indicating state transition in the above figure indicate the state of the JMS pin at the rising edge of the clock input to the JCK pin.

2. Numbers in ( ) in the above figure correspond to the explanation below.

Figure 5-3. Operation Timing in Controller State



(1) Test-Logic-Reset

The boundary scan circuit performs no operation on the μPD98410. Therefore, it does not affect the system logic of the μPD98410. This is because the bypass instruction is stored to the instruction register and executed on initialization. The TAP controller enters the Test-Logic-Reset state if the JMS pin holds the high level for the duration of at least five rising edges of the JCK pin signal, regardless of the current state of the controller. The TAP controller holds this state for the duration in which the JMS pin signal high.

If the TAP controller must be in the Test-Logic-Reset state, the controller returns to the original Test-Logic-Reset state even if a low-level signal is input once to the JMS pin by mistake (due to, for example, the influence of the external interface), if the JMS pin signal holds its high level status for the duration of three rising edges of the JCK pin signal.

The operation of the test logic does not hinder the logic operation of the μPD98410 due to the above error.

When the TAP controller exits from the Test-Logic-Reset state, the controller enters the Run-Test/Idle state. In this state, no operation is performed because the current instruction is set by the operation of the bypass register. The logic operation of the JTAG boundary scan circuit is inactive even in the Select-DR-Scan and Select-IR-Scan states.

(2) Run-Test/Idle

The TAP controller is in this state during scan operation (in Select-DR-Scan or Select-IR-Scan state). Once the controller has entered this state and if the JMS pin signal holds the low level, the controller remains in this state. The controller enters the Select-DR-Scan state if the JMS pin signal holds high level at one rising edge of the JCK pin signal.

All the test data registers (boundary register and bypass register) selected by the current instruction hold the previous status (Idle). While the TAP controller is in this state, the instruction does not change.

(3) Select-DR-Scan

This is a temporary boundary scan state. The boundary scan register and bypass register selected by the current instruction hold the previous state.

If the JMS signal is held low at the rising edge of the JCK pin signal while the TAP controller is in this state, the controller enters the Capture-DR state, and scan sequence to the selected registers is started.

If the JMS signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Select-IR-Scan state. While the controller is in this state, the instruction does not change.

(4) Select-IR-Scan

This is a temporary boundary scan state. The boundary scan register and bypass register selected by the current instruction hold the previous state.

If the JMS signal is held low at the rising edge of the JCK pin signal while the TAP controller is in this state, the controller enters the Capture-IR state, and scan sequence to the selected registers is started.

If the JMS signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Test-Logic-Reset state. While the controller is in this state, the instruction does not change.

(5) Capture-DR

In this controller state, data is loaded to the boundary scan register selected by the current instruction in parallel at the rising edge of the JCK pin signal (in this case, data is input from the input pin of each device to the corresponding boundary scan register). While the TAP controller is in this state, the instruction does not change.

If the TAP controller is in this state at the rising edge of the JCK pin signal, the controller enters the following state:

- If the JMS pin signal is held high: Exit1-DR state
- If the JMS pin signal is held low : Shift-DR state

(6) Shift-DR

In this controller state, JDI and JDO are connected (at either of the boundary scan register of bypass register) by the current instruction. The shift data is shifted one state at a time toward the serial output direction at each rising edge of the JCK pin signal.

The boundary scan register or bypass register selected by the current instruction holds the previous status without change if the controller is not on the serial bus (not in the Shift-DR state). While the controller is in this state, the instruction does not change.

If the TAP controller is in this state at the rising edge of the JCK pin signal, the controller enters the following state:

- If the JMS pin signal is held high: Exit1-DR state
- If the JMS pin signal is held low : Shift-DR state

(7) Exit1-DR

This is a temporary controller state. If the JMS pin signal is held high at the rising edge of the JCK pin signal with the TAP controller in this state, the controller enters the Update-DR state. This ends the scan process.

If the JMS pin signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Pause-DR state.

Both the bypass register and boundary scan register selected by the current instruction hold the previous status without change. While the TAP controller is in this state, the instruction does not change.

(8) Pause-DR

In this controller state, shifting between JDI and JDO connected by either the bypass register or boundary scan register is temporarily stopped. These registers selected by the current instruction hold the previous state without change.

The TAP controller remains in this state while the JMS pin signal is low. If the JMS pin signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Exit2-DR state. While the TAP controller is in this state, the instruction does not change.

(9) Exit2-DR

This is a temporary controller state. If the JMS pin signal is held high at the rising edge of the JCK pin signal with the TAP controller in this state, the controller enters the Update-DR state. This ends the scan process.

If the JMS pin signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Shift-DR state.

Both the bypass register and boundary scan register selected by the current instruction hold the previous status without change. While the TAP controller is in this state, the instruction does not change.

(10) Update-DR

The boundary scan register has a parallel output latch to prevent changes in parallel output (while shifted to the shift register path concatenated) by certain instructions (for example, EXTEST instruction).

In the Update-DR controller state, data is latched from the shift register to the parallel output latch of this register at the falling edge of the JCK pin signal.

The data retained latched to the parallel output latch changes depending on this controller state (the data does not change with the other controller states).

The previous states of all the shift register of the boundary scan register selected by the current instruction are retained.

While the TAP controller is in this state, the instruction does not change.

If the JMS pin signal is held high at the rising edge of the JCK pin signal with the TAP controller in this state, the controller enters the Select-DR-Scan state.

If the JMS signal is held low at the rising edge of the JCK signal, the TAP controller enters the Run-Test/Idle state.

(11) Capture-IR

In this controller state, the shift register loads the pattern of a fixed logic value “01H” to the instruction register at the rising edge of the JCK pin signal.

The previous states of both the bypass register and boundary scan register selected by the current instruction are retained without change.

While the TAP controller is in this state, the instruction does not change.

If the JMS pin signal is held high at the rising edge of the JCK pin signal while the controller is in this state, the controller enters the Exit1-IR state.

If the JMS pin signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Shift-IR state.

(12) Shift-IR

In this controller state, JDI and JDO are connected by the shift register in the instruction register. The shift data is shift one state toward the serial output direction at each rising edge of the JCK pin signal.

The boundary scan register or bypass register selected by the current instruction holds the previous state without change.

While the TAP controller is in this state, the instruction does not change.

If the JMS pin signal is held high at the rising edge of the JCK pin signal with the TAP controller in this state, the controller enters the Exit1-IR state. If the JMS pin signal is held low, the controller remains the Shift-IR state.

(13) Exit1-IR

This is a temporary controller state. If the JMS pin signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Update-IR state. This ends the scan process.

If the JMS pin signal is held low at the rising edge of the JCK pin, the TAP controller enters the Pause-IR state.

Both the bypass register and boundary scan register selected by the current instruction retain their states without change.

While the TAP controller is in this state, the instruction does not change.

(14) Pause-IR

In this controller state, shift of the instruction register is temporarily stopped. The bypass register and boundary scan register selected by the current instruction hold the previous state without change.

While the TAP controller is in this state, the instruction does not change. The instruction register holds the current state.

While the JMS pin signal is low, the TAP controller remains in this state. If the JMS pin signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Exit2-IR state.

(15) Exit2-IR

This is a temporary controller state. If the JMS pin signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Update-IR state. This ends the scan process.

If the JMS pin signal is held low at the rising edge of the JCK pin, the TAP controller enters the Shift-IR state.

Both the bypass register and boundary scan register selected by the current instruction retain their states without change.

While the TAP controller is in this state, or while the instruction register holds the current state, the instruction does not change.

(16) Update-IR

In this controller state, the instruction shifted to the instruction register is latched to the parallel output latch from the shift register path at the falling edge of the JCK pin signal. Once a new instruction has been latched, it is used as the current instruction.

The bypass register or boundary scan register selected by the current instruction holds the previous state.

If the JMS pin signal is held high at the rising edge of the JCK pin signal while the TAP controller is in this state, the TAP controller enters the Select-DR-Scan state.

If the JMS pin signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Run-Test/Idle state.

The Pause-DR controller state in (8) and Pause-IR controller state in (14) temporarily stop shifting of data in the bypass register, the boundary scan register, or instruction register.

5.5 TAP Controller Operation

The TAP controller operates as follows.

The state of the controller is changed by either of (1) and (2) below.

(1) Rising edge of JCK pin signal
(2) JRST_B pin input

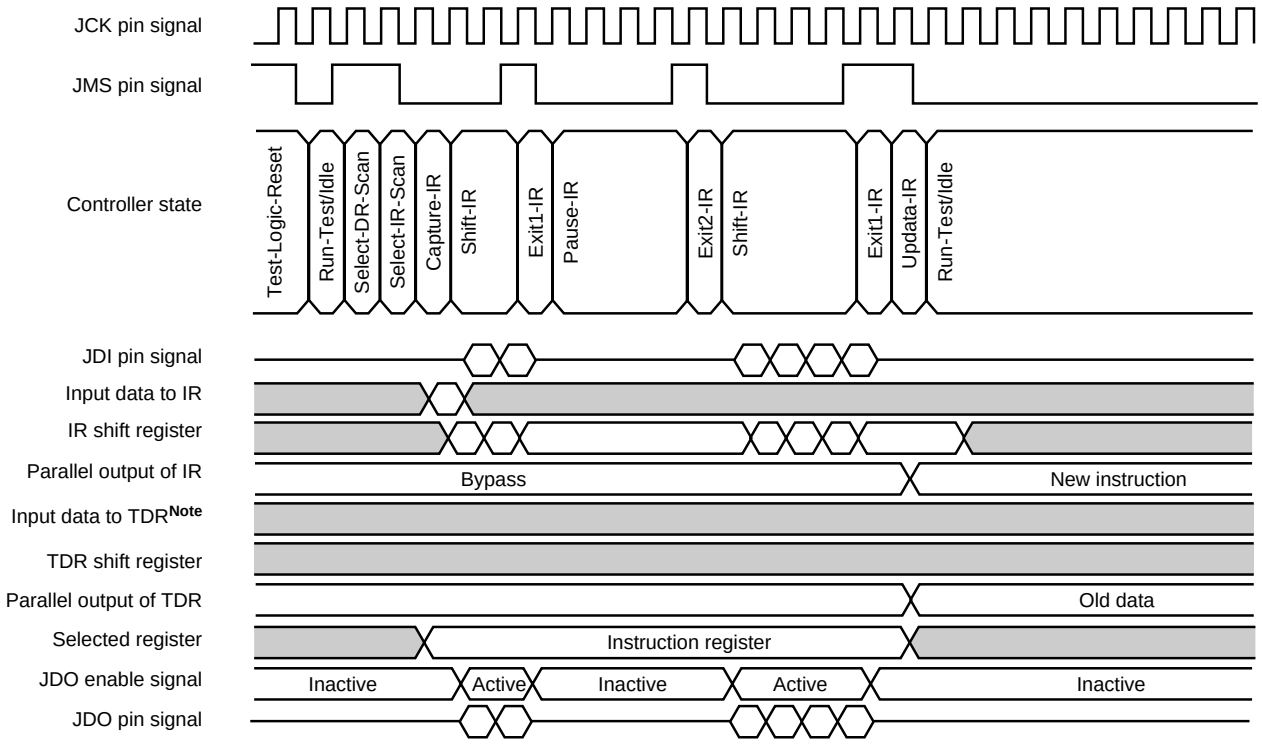
The TAP controller generates signals that control the operations of the bypass register, boundary scan register, and instruction register defined by the IEEE1149.1 JTAG Boundary Scan Standard (refer to **Figures 5-4** and **5-5**).

The JDO pin output buffer and the peripheral circuit that selects a register whose contents are to be output to the JDO pin are controlled as shown in Table 5-1. The JDO pin defined in this table changes at the falling edge of the JCK pin signal after it has entered each state.

Table 5-1. Operation in Each Controller State

Controller State	Selected Register to Be Driven to JDO Pin	JDO Pin Driver
Test-Logic-Reset	Undefined	High impedance
Run-Test/Idle		
Select-DR-Scan		
Select-IR-Scan		
Capture-IR		
Shift-IR	Instruction register	Active
Exit1-IR	Undefined	High impedance
Pause-IR		
Exit2-IR		
Update-IR		
Capture-DR		
Shift-DR	Data register (boundary scan register, bypass register)	Active
Exit1-DR	Undefined	High impedance
Pause-DR		
Exit2-DR		
Update-DR		

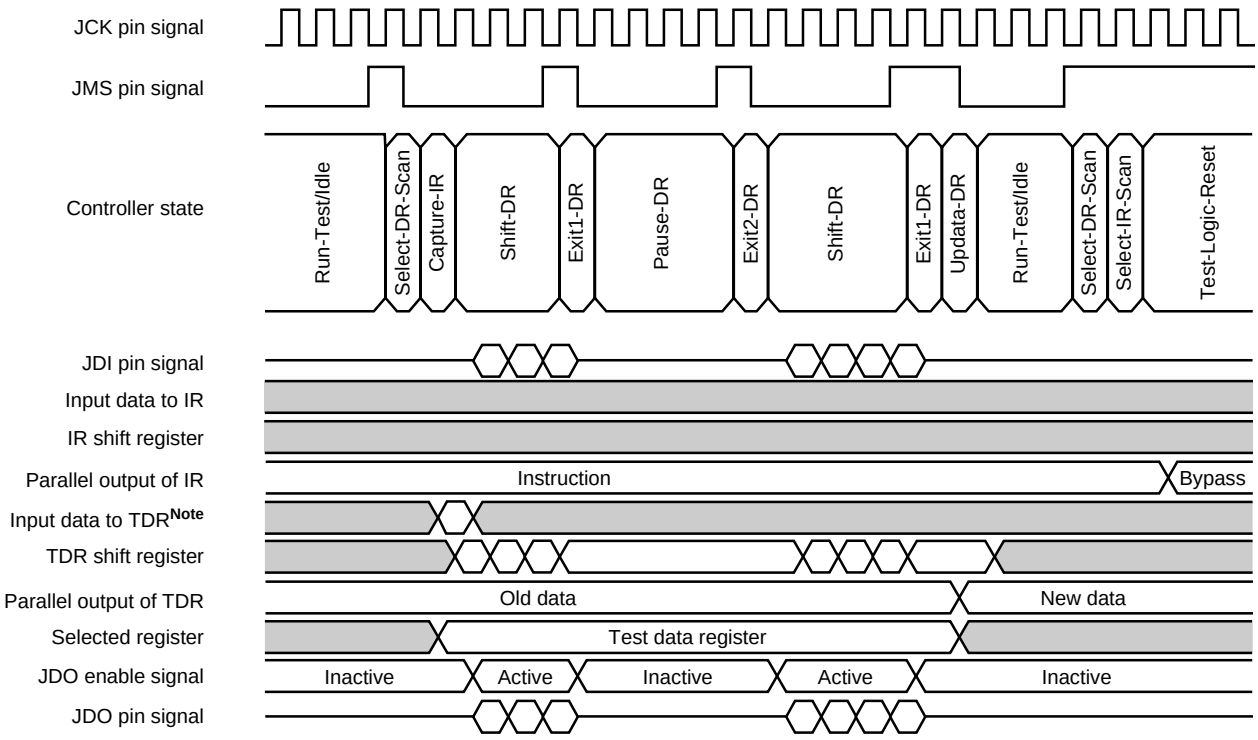
Figure 5-4. Operation of Test Logic (instruction scan)



Note TDR (Test Data Register): Boundary scan register and bypass register

Remark ▭ : Don't care or undefined

Figure 5-5. Operation of Test Logic (data scan)



Note TDR (Test Data Register): Boundary scan register and bypass register

Remark ▭ : Don't care or undefined

5.6 Initializing TAP Controller

The TAP controller is initialized as follows:

(1) The TAP controller is not initialized by the operation of system input such as system reset.
(2) The TAP controller enters the Test-Logic-Reset controller state at the fifth rising edge of the JCK pin signal (while the JMS pin signal is held high).
(3) The TAP controller asynchronously enters the Test-Logic-Reset state when the JRST_B signal is input.

5.7 Instruction Register

This register is defined as follows (refer to **5.2 Internal Configuration of Boundary Scan Circuit**).

(1) The instruction shifted and input to the instruction register is latched so that it changes only in the Update-IR and Test-Logic-Reset controller states.
(2) Data is not inverted since it has been serially input to the instruction register until it is serially output.
(3) A fixed binary pattern data “01” (with LSB (Least Significant Bit) being “1”) is loaded to this register cell in the Capture-IR controller state.
(4) A fixed binary pattern data “01” (with LSB being “1”) is loaded to this register cell in the Test-Logic-Reset controller state.
(5) While this register is read, data is output from the JDO pin, starting from the LSB to the MSB (Most Significant Bit), at each falling edge of the JCK pin signal.

The JTAG boundary scan circuit of the μPD98410 can support only the following two instructions depending on the data set to the instruction register.

- BYPASS instruction
- EXTEST instruction

Instruction Register		Supported Instruction
D1	D0	
0	0	EXTEST instruction
0	1	Unused
1	0	Unused
1	1	BYPASS instruction

5.7.1 BYPASS instruction

This instruction is specified by instruction data “11”. This instruction is used to select only the bypass register (to access between the JDI and JDO pins serially) in the Shift-DR controller state.

While this instruction is selected, the operation of the JTAG boundary scan circuit does not affect the operation of the μPD98410.

This bypass instruction is selected while the TAP controller is in the Test-Logic-Reset state.

5.7.2 EXTEST instruction

This instruction is specified by instruction data “00”. In the Shift-DR controller state, this instruction is used to select the boundary scan register of serial access between the JDI and JDO instructions.

- While this instruction is selected:

  The states of all the signals driven from the system output pins are completely defined by the data shifted to the boundary scan register. In the Update-DR controller state, the states of all the signals are changed only by the falling edge of the JCK pin signal.

  The states of all the signals input from the system input pins are loaded to the boundary scan register at the rising edge of the JCK pin signal while the TAP controller is in the Capture-DR state.

5.8 Boundary Scan Data Bit Definition

NEC will provide the BSDL (Boundary Scan Description Language) file for the μPD98410 upon request. For details, call NEC Semiconductor Technical Hot Line shown at the end of this document.

[MEMO]

CHAPTER 6 LIMITATIONS

The K model of the μPD98410 has the following 11 limitations.

6.1 Limitations

(1) Error in 52-byte short cell reception
(2) Error in cell transmission when multi-PHY mode is changed
(3) Limitation of logical port mapping (output of congested cell)
(4) Limitation when operation command is issued
(5) Limitation of logical port mapping (output of illegal cell)
(6) Limitation of logical port mapping (mapping of unconnected PHY)
(7) Indication error of QE and CE bits of status register
(8) Shortage of driving capability of UTOPIA output pins
(9) Error in queue management
(10) Queue management malfunctioning due to unmatched broadcast count and problem of timing of reusing Area-B
(11) Limitation in accessing cell buffer memory MPU

6.2 Description of Limitations

(1) Error in 52-byte short cell reception

<Phenomenon>

If the following two conditions are satisfied at the same time, the cell following a short cell of 52 bytes is lost.

(a) When RXSOC (input of a high level to the RXSOC pin) is received at the P48 (payload 48) timing of a received cell

(b) When a PHY device that can be transferred next is received before reception of RXSOC in (a)
The μPD98410 receives a cell from a PHY device detected as a result of polling after one cell has been lost, and continues the normal operation.

<Remedy>

This symptom does not occur because a 52-byte short cell is not transmitted as long as the PHY device transmits cells normally.

(2) Error in cell transmission when multi-PHY mode is changed

<Phenomenon>

Two cells may be lost when the SG bit of the port configuration register (PT) goes 0 from 1 (i.e., when mode of an active logical port (EN bit = 1) is changed from the single PHY mode to multi-PHY mode). After that, the μPD98410 continues normal operation.

<Remedy>

Unless a new circuit card is inserted onto the UTOPIA interface that is operating, the mode cannot be changed from the single PHY mode to multi-PHY mode. Therefore, this phenomenon does not occur unless a circuit card is inserted.

(3) Limitation of logical port mapping (output of congested cell)

<Phenomenon>

If the mapping of a logical port is changed, illegal cells are output until the queue of that port becomes empty. Specifically, the cells that should be output to the old PHY device are output to the new PHY device.

<Remedy>

The mapping of a logical port is not necessary unless a circuit card is inserted or removed during operation. Therefore, this phenomenon does not occur unless a circuit card is removed or inserted.

(4) Limitation when operation command is issued

<Phenomenon>

If the CMD bit of the command register is set to 111 (an operation command is issued) without confirming that the BY bit of the status register (STATUS) is 0 after the CMD bit has been cleared to 000 (a stop command is issued), a cell may transmitted to an illegal cell, or up to two cells may be lost. After that, the μPD98410 continues normal operation.

<Remedy>

Be sure to confirm that the BY bit is 0 before issuing an operation command.

(5) Limitation of logical port mapping (output of illegal cell)

<Phenomenon>

If the mapping of a logical port is changed while it is active (EN bit = 1), one cell may be output to the new PHY address on UTOPIA immediately before the change.

Example The mapping of a logical port is changed when EN = "1".

Before change		After change
UPN = "00"	→	UPN = "10"
PHY = "0011"	→	PHY = "0101"

One cell may be output to UPN = "00", PHY = "0101" immediately after the change.

<Remedy>

Change the mapping after waiting for 44-SWCLK after making the logical port inactive (EN = 0).

(6) Limitation of logical port mapping (mapping of unconnected PHY)

<Phenomenon>

The Rx side is polled even if a PHY device for which the EN bit of the port configuration register (PT) is set to 1 is not connected. Therefore, the μPD98410 may receive RXCLAV in the floating status and malfunction. Consequently, the corresponding UTOPIA may hang up.

<Remedy>

Be sure to clear the EN bit for a PHY device not connected to 0.

(7) Indication error of QE and CE bits of status register

<Phenomenon>

The QE and CE bits of the status register may indicate illegal information if a multi-cast cell is discarded because of any of the following settings:

(a) If LPNn (n = 0 to 23) in Area-B in the header translation table (HTT) are all "0".
(b) If the EN bit of the port configuration (PT) register of the logical output port to be used is "0".
(c) If any of the output queue maximum threshold registers (OQthCBR, OQthRVR, OQthRM, OQthNVR, OQthABR, and OQthUBR) is "0".
(e) If any of the output queue minimum threshold registers (OQminCRV, OQminRNV, OQminABR, and OQminUBR) is "0", if any of the TC counter minimum threshold value registers (TCminCRV, TCminRNV, TCminABR, and TCminUBR) is "0", and if any of the UC counter maximum threshold registers (UCthCBR, UCthRVR, UCthRM, UCthNVR, UCthABR, and UCthUBR) is "0"
(f) If any of the output queue EPD threshold value registers (OQthAEP and OQthUEP) is "0", and if the input cell is not subject to EPD
(g) If any of the output queue minimum threshold registers (OQminCRV, OQminRNV, OQminABR, and OQminUBR) is "0", if any of the TC counter minimum threshold value registers (TCminCRV, TCminRNV, TCminABR, and TCminUBR) is "0", if any of the UC counter EPD threshold value registers (UCthAEP and UCthUEP) is "0", and if the input cell is not subject to EPD
(h) If any of the output queue CLP threshold registers (OQthCCL, OQthRCL, OQthACL, and OQthUCL) is "0", and if the input cell is subject to CLP

<Remedy>

Do not perform any of the above settings (a) through (h).

(8) Shortage of driving capability of UTOPIA output pins

<Phenomenon>

Although the ATM Forum Recommendation specifies the high-level output current (I_{OH}) to be MIN. –8 mA, the μPD98410 has a high-level output current of TYP. –8 mA. The low-level output current (I_{OL}) of the μPD98410 is 8 mA or more, which poses no problem.

<Remedy>

Do not connect too many devices.

There is no problem when connecting two NEC's 155M-PHY (μPD98404s) to one UTOPIA port, or when connecting two 6-port 25M-PHY (μPD98408s) to one UTOPIA port.

(9) Error in queue management

<Phenomenon>

If too many multi-cast cells are congested, the TC counter may overflow. As a result, queue management malfunctions.

<Remedy>

This phenomenon does not occur if any of the following conditions is satisfied.

(a) Minimize the external memory configuration.

(b) Set the OQmax and OQmin threshold values, and MQmax and MQmin threshold values, so that the following condition is satisfied.

(OQmax threshold value – OQmin threshold value) × n +
(MQmax threshold value – MQmin threshold value) < (65535 – n)

where n indicates the number of ports used

(10) Queue management malfunctioning due to unmatched broadcast count and problem of timing of reusing Area-B

<Phenomena>

If multi-cast connection is added, changed, or deleted while the μPD98410 operates, the following two phenomena may occur.

[Problem 1] Queue management malfunctioning due to mismatching broadcast count

If the broadcast count is changed for multi-cast connection, and if the cells of the corresponding connection are congested, queue management malfunctions.

The malfunctioning occurs if HTT (header translation table) broadcast destination output ports LPN0 through 23 of memory Area-B: Logical Port (MB: Multicast Bitmap)) are changed for a connection for which cells are congested.

Even if broadcast count is changed for multi-cast connection, if no cells are congested, queue management is performed normally. Even if the output destination for single cast connection is changed, queue management is performed normally.

The mechanism of this phenomenon is as follows:

The μPD98410 stores the broadcast count (NMP: Number of Multicast Port) set in Area-A of the HTT memory in the cell buffer as broadcast count (CC: Cast Counter) along with the received cell when a cell is received. When transmitting a cell, the μPD98410 references the broadcast destination output port (MB) in Area-B of the HTT memory and broadcast count of the cell buffer (CC), to identify the broadcast destination port and completion of broadcast. If the broadcast destination output port (MB) in Area-B of the HTT memory is changed before a cell is output, the broadcast count (CC) before change and broadcast destination output port (MB) after change are referenced, resulting in mismatching. Consequently, cells remain in the cell buffer, or cells that have not completed broadcast is released, and the μPD98410 cannot correctly manage the queue.

[Problem 2] Problem of timing of re-using Area-B

As described in Problem 1 above, the setting of Area-B of the HTT memory must be maintained until all the cells of the corresponding connection are output, regarding multi-cast connection. However, the timing to change connection cannot be judged because it cannot be judged whether all the cells have been output. Area-A of the HTT memory can be changed at any time, without posing a problem concerning queue management. In this case, received and congested cells are switched by information either before or after change.

<Remedy>

To prevent Problem 1, “queue management malfunctioning due to unmatched broadcast count”, divide Area-B of the HTT memory by broadcast count.

To prevent Problem 2, “problem of timing of re-using Area-B”, prepare a queue dedicated to each broadcast at the microprocessor side.

Next, an example of setting the HTT memory from the microprocessor is shown below.

[Initial setting]

- Divide the Area-B of the HTT memory by each broadcast count and use the same area for connection of the same broadcast count. Even if Area-B is changed during re-queuing, broadcast count is not unmatched because it is the same before and after the change, and queue management does not malfunction (in the example below, 2048 channels are used as the area of Area-B, and a dedicated area is prepared for each broadcast count where broadcast count is 2 to 24).

Example Area-B

0ch-88ch	For 2 broadcasts
89ch-177ch	For 3 broadcasts
178ch-266ch	For 4 broadcasts
267ch-355ch	For 5 broadcasts
:	
:	
:	
1958ch-2046ch	For 24 broadcasts

- To make sure that a sufficient time elapses until Area-B of the HTT memory is used again, the microprocessor prepares a dedicated broadcast queue for each broadcast count, and manages the usable channels (free channels).

Example A queue of 0ch, 1ch, ... 87ch, 88ch is created as a 2-broadcast queue.

[To register new multi-cast connection]

- A free channel is obtained from the dedicated broadcast queue prepared by the microprocessor.
- Connection information is set in the Area-B of the obtained channel.
- Connection information is set in Area-A[Note].

Note When the 16-bit separated asynchronous bus mode is used, the procedure is “setting of HTT[15:0] → setting of HTT[31:16]”.

[To delete existing multi-cast connection]

- Clear Area-A (clear bit 31 of Type-C (CEN: Channel Enable) to “0”).
- Release the channel used of Area-B as a free channel and writes it back to the dedicated broadcast queue.
- The contents of Area-B used are not changed.

[To update existing multi-cast connection]

- Obtain a free channel from the dedicated broadcast queue prepared at the microprocessor side.
- Set the connection information to be updated in the Area-B of the obtained channel.
- Set the connection information to be updated in Area-A[Note].
- Release the channel of Area-B used as a free channel, and writes it back to the dedicated broadcast queue.
- The contents of Area-B used are not changed.

Note When the 16-bit separated asynchronous bus mode is used, the procedure is “clearing bit 31 of Type-C (CEN) to “0” → updating HTT [15:0] → updating HTT [31:16]” (CEN = “1”).

<Effect of remedy>

Problem 1 can be prevented by taking the above remedial action. It is considered that Problem 2 can be almost completely prevented in actual operating conditions, however, there is no perfect remedy.

This is because whether all the cells congested in the queue of each channel have been output cannot be known. As a result, mismatching of a broadcast port and output VPI/VCI occurs when Area-B is changed, and an illegal cell may be output.

Even after connection has been deleted or updated, the cell of the connection before deletion/updating may remain in the multi-cast queue. In particular, cells with the lower priority are likely to remain in the queue for a long time. If the connection information of Area-B before deletion/updating is used again in this case, mismatching of broadcast count and broadcast destination information occurs during re-queuing.

Information on broadcast count is especially important for the μPD98410, and Area-B is divided by broadcast count to prevent Problem 1, "queue management malfunctioning due to unmatched broadcast count". If Area-B is divided by broadcast count, mismatching of broadcast count does not occur even if Area-B is used during re-queuing, and therefore, queue management malfunctioning does not occur.

To prevent Problem 2, "problem of timing of re-using Area-B", a dedicated broadcast queue is prepared for each broadcast count at the microprocessor side. By providing this dedicated broadcast queue, it can be ensured that enough time elapses before Area-B is used.

(11) Limitation in accessing cell buffer memory MPU

The microprocessor writes data to the cell buffer memory to confirm the initial operation of the cell buffer memory after reset. When reading the cell buffer memory, the following limitation applies.

<Limitation>

Be sure to write data of 1 word or 88 bits to the cell buffer memory. Write CBD (Cell Buffer Data) [31:0] or CBD [15:0] at last.

Writing of one word is completed by writing 88 bits of data followed by CBD [31:0] or CBD [15:0].

If the switching operation is enabled by using the CMD register (CMD = 111) when writing of one word is not completed, i.e., when CBD [31:0] or CBD [15:0] has not been written yet, the μPD98410 does not write the received cell data to the cell buffer memory. As a result, the subsequent switching operation is not performed correctly.

[MEMO]

CHAPTER 7 FAQ (Frequently Asked Questions)

Here are the questions frequently asked concerning the μPD98410 (X10) and answers to them.

Q.1

What are the recommended soldering conditions?

A.1

Refer to Condition IR20-202-3 in NEC's **Semiconductor Device Mounting Technology Manual (C10535E)**.

Q.2

How should X10 be set to output an input cell of VCI = 0 to a specific output port, regardless of the VPI value?

A.2

It is necessary to set parameters for all the VPI values on the HTT (Header Translation Table) memory before starting a switching operation.

Q.3

How are the OAM cells of F4 and F5 are treated?

A.3

The OAM cell of F4 can be handled. The OAM cell of input F4 can be recognized by X10 and output to a specific port.

The OAM cell of F5 cannot be handled by X10 alone. For example, a control function to output the OAM cell of input F5 to the port of an SAR device (OAM filtering function) is not provided. The OAM cell of F5 must be processed.

Q.4

How fast should the access speed of the SRAM that is connected as the cell buffer memory or HTT & control memory be?

A.4

SRAM of 15 ns is recommended, though the access speed differs depending on the number of SRAMs to be connected and wiring length.

Q.5

Is the address to access Area-A generated from offset + VPI/VCI synthesis address?

A.5

Yes. Refer to **3.3.4 Accessing HTT**.

Q.6

How may queues does X10 have?

A.6

X10 has the following queues. Of these, the total queue is not actually a queue but a counter.

Idle queue	: 1
Output queue	: 96 (= 4 classes × 24 ports)
Multi-cast queue	: 4 (= 4 classes)
Total queue of each class	: Counter
Total queue	: Counter

Q.7

Is the set value of OQminXXX (output minimum queue length) the same for each logical port?

A.7

Yes, it is the same for each logical port.

Q.8

(1) In what sequence are cells output to an actual port from the output queue of each logical output port? Are they output in a simple round-robin mode? If a cell exists in a specific queue such as the CBR queue, does that cell take precedence, or not?
(2) CBR and rt-VBR are in the same output queue. How are the cells of CBR class output at constant intervals?

A.8

Cells are output from an output queue in the following sequence:

(a) Each PHY device is polled if it is ready for transmission.
(b) A logical output port is determined based on output rate control (shaping), cell congestion information, and the result of polling.
(c) A service class is determined in the determined logical output port.

The service class is determined by WFQ (Weighted Fairness Queuing) method in the order of CBR + rtVBR, RM + VBR, ABR, and UBR. The output generation interval is shaping concerning ports, and WFQ concerning classes. Output of only CBR cannot be adjusted concerning the queue of CBR and rt-VBR. Because real-time feature is important for rt-VBR class as well as for CBR class, the same queue of a high priority is used.

Q.9

If a cell other than valid cells, such as an idle cell or unassigned cell, is input to the input port, what is output to the output port?

A.9

Because both the idle cell and unassigned cell are VPI = 0 and VCI = 0, they are output to the output port in accordance with the setting of the HTT memory. If a cell not set to the HTT memory is input, a header translation error occurs, and the input cell is discarded.

Q.10

There are four multi-cast queues corresponding to each class, and the priority of a multi-cast queue is fixed during re-queuing. Does this mean that the cell of the low-order multi-cast queue is output when no cell is congested in the high-order multi-cast queue (for example, is the cell of UBR class output when no cell is congested at CBR, VBR, or ABR class)?

A.10

That's right.

Q.11

This is a question related to the WFQ operation. When a time out of the cycle counter occurs, are the present values of C_{CBR} and C_{VBR} counters and the set value of the class priority control register loaded to C_{CBR} and C_{VBR} counters?

A.11

Yes.

Q.12

Even if priority control by the C_{ABR} and C_{UBR} counters is started, the output permission is granted to the CBR and VBR classes if there are no congested cells at ABR and UBR classes, and if there are congested cells at CBR and VBR class. In this case, is the count value decremented by the number of cells output if the C_{CBR} and C_{VBR} counters are not zero?

A.12

Priority control by C_{ABR} and C_{UBR} is performed in the following case:

"If $C_{CBR} = 0$, or no cells are congested in the CBR queue", and
"if $C_{VBR} = 0$, or no cells are congested in the VBR queue"

In the case in the question, therefore, the output permission is granted to the CBR and VBR class only when cells are congested but the counter is 0. In this case, the counter remains 0 even if the cell has been output.

Q.13

How much is the output (re-queuing) throughput of the multi-cast queue?

A.13

The HTT & control memory is accessed in the following three ways during re-queuing of the multi-cast cell (= cell storage address copy):

- The cell storage address is read.
- HTT Area-B is read.
- The cell storage address for each output queue is written.

In the case of multi-cast of 1:7, for example, two read operations and seven write operations are necessary for processing one multi-cast cell. Because the μPD98410 requires an idle period once between a read operation and a write operation, ten accesses must be made to process one multi-cast cell.

Incidentally, the μPD98410 operates using 44SWCLK as a basic cycle, and allocates at least 8 memory accesses per basic cycle to multi-cast processing.

To process eight multi-cast cells, therefore, 56 cells (= 8 ports $\times$ 7 directions) are re-queued by using 80 access timings (= 10 times $\times$ 8 cells). In this case, the re-queuing throughput is about 1.7 [Gbps] where SWCLK = 33 [MHz].

This exceeds the switching capability of 1.256 [Gbps]. As a result, cells are congested in the output queue.

$$\frac{56\ (\text{cells}) \times 53\ (\text{octets/cells}) \times 8\ (\text{bits/octets})}{\frac{80\ (\text{times})}{8\ (\text{times})} \times \frac{1}{33 \times 10^6}\ (\text{sec/SWCLK}) \times 44\ (\text{SWCLK})} = 1.7808 \times 10^9\ (\text{bps})$$

Next, cell congestion in the multi-cast queue is explained.

As described above, multi-cast of 1:7 requires 10 access timings for processing one multi-cast cell. This means that a cell is read once from the multi-cast queue each time processing has been performed 10 times. Therefore, the read speed of the multi-cast queue is equivalent to 254.4 [Mbps].

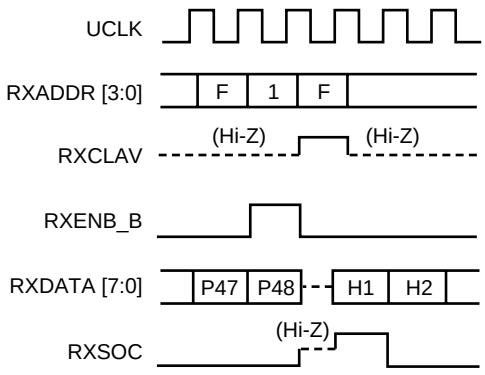
$$\frac{1\ (\text{cell}) \times 53\ (\text{octets/cells}) \times 8\ (\text{bits/octets})}{\frac{10\ (\text{times})}{8\ (\text{times})} \times \frac{1}{33 \times 10^6}\ (\text{sec/SWCLK}) \times 44\ (\text{SWCLK})} = 254.4 \times 10^6\ (\text{bps})$$

If the total speed of multi-cast connection (total throughput of input cells) exceeds 254.4 [Mbps], cells are increasingly congested in the multi-cast queue. If the speed does not exceed 254.4 [Mbps], up to eight cells are congested in the multi-cast queue.

The value of 254.4 [Mbps] sounds as if the capability were low. If there are eight multi-cast connections of 1:7, however, cells are congested in the output queue rather than in the multi-cast queue. Therefore, this value is considered sufficient.

Q.14

While X10 receives a cell from a certain PHY (e.g., PHY#1), it selects PHY#1 again after it has received the cell if the result of polling the other PHY devices is no good. At this time, does RXENB_B go high again as shown below?



A.14

X10 returns RXENB_B to the high level again.

Q.15

Give me an example of initializing the device.

A.15

Power application

→ Input a low level to the RESET_B pin.

→ Read the status register (STATUS). If BY = 1, proceed to the next step. If BY = 0, read the STATUS register again.

→ Write the memory mode register (MODE). Set each field.

→ Initialize the HTT memory to 0.

→ Write the interrupt mask register (INTMASK). Set each field.

→ Write the port configuration registers (PT0 through PT23). Set each field.

→ Write the header translation configuration registers (HT0 through HT23). Set each field.

→ Write each count enable register (CTENTH, CTENHT, CTENHEC, CTENMEM, and CTENRCV). Set each field.

→ Write each threshold value register (such as OQminCRV). Set each field.

→ Write the class priority control registers (PC0 through PC23) and cycle count register (PERIOD). Set each field.

→ Write the HTT (Header Translation Table) memory. Set each field.

→ Write the command register (CMD). Set CMD to 111.

→ Start a switching operation.

Q.16

Give me an example of interrupt processing.

A.16

The microprocessor detects the low level of the INT_B pin.

→ Read the status register (STATUS) and recognize the interrupt cause.

The processing branches depending on the interrupt cause.

(1) Parity error (PH, PC = 1)
The microprocessor resets X10.

(2) Input port overrun (IN = 1)
The microprocessor recognizes a UTOPIA number responsible for discarding a cell by reading the input port overrun error discard indication register (ERINOV).

(3) Queue pointer or cast counter error (QE, CE = 1)
The microprocessor resets X10.

(4) Cell buffer or control memory shortage (CB, CT = 1)
Cells are temporarily discarded. If sufficient area becomes available on the memory, X10 automatically returns to the normal operation, and continues the switching operation.

(5) HEC/CRC error (HE = 1)
The microprocessor recognizes a logical input port responsible for discarding a cell by reading the HEC/CRC error discard indication register (ERHEC).

(6) Header translation error (HT = 1)
The microprocessor recognizes a logical input port responsible for discarding a cell by reading the header translation error discard indication register (ERHT).

(7) Buffer threshold exceeding (EX = 1)
The microprocessor recognizes a logical output port responsible for discarding a cell by reading the threshold exceeding discard indication register (EXTH).

(8) Count over (CME, CHE, CHT, CEX, CRV = 1)
X10 returns the counter value of the counter that has overflown to 0 and the counter continues counting.

Q.17

Give me an example of changing the setting of the HTT memory.

A.17

(1) Single cast

[To register new single cast connection]

Set connection information in Area-A.

Remark When the 16-bit separated asynchronous bus mode is used, the procedure is “setting of HTT [15:0] → setting of HTT [31:16]”.

[To delete existing single cast connection]

Clear Area-A (clear bit 31 of Type-B (CEN: Channel Enable) to “0”).

[To update existing single cast connection]

Set connection information to be updated in Area-A.

Remark When the 16-bit separated asynchronous bus mode is used, the procedure is “clearing bit 31 of Type-B (CEN) to “0” → updating HTT [15:0] → updating HTT [31:6] (CEN = 1)”.

(2) Multi-cast

Refer to **(10)** in **CHAPTER 6 LIMITATIONS**.

Q.18

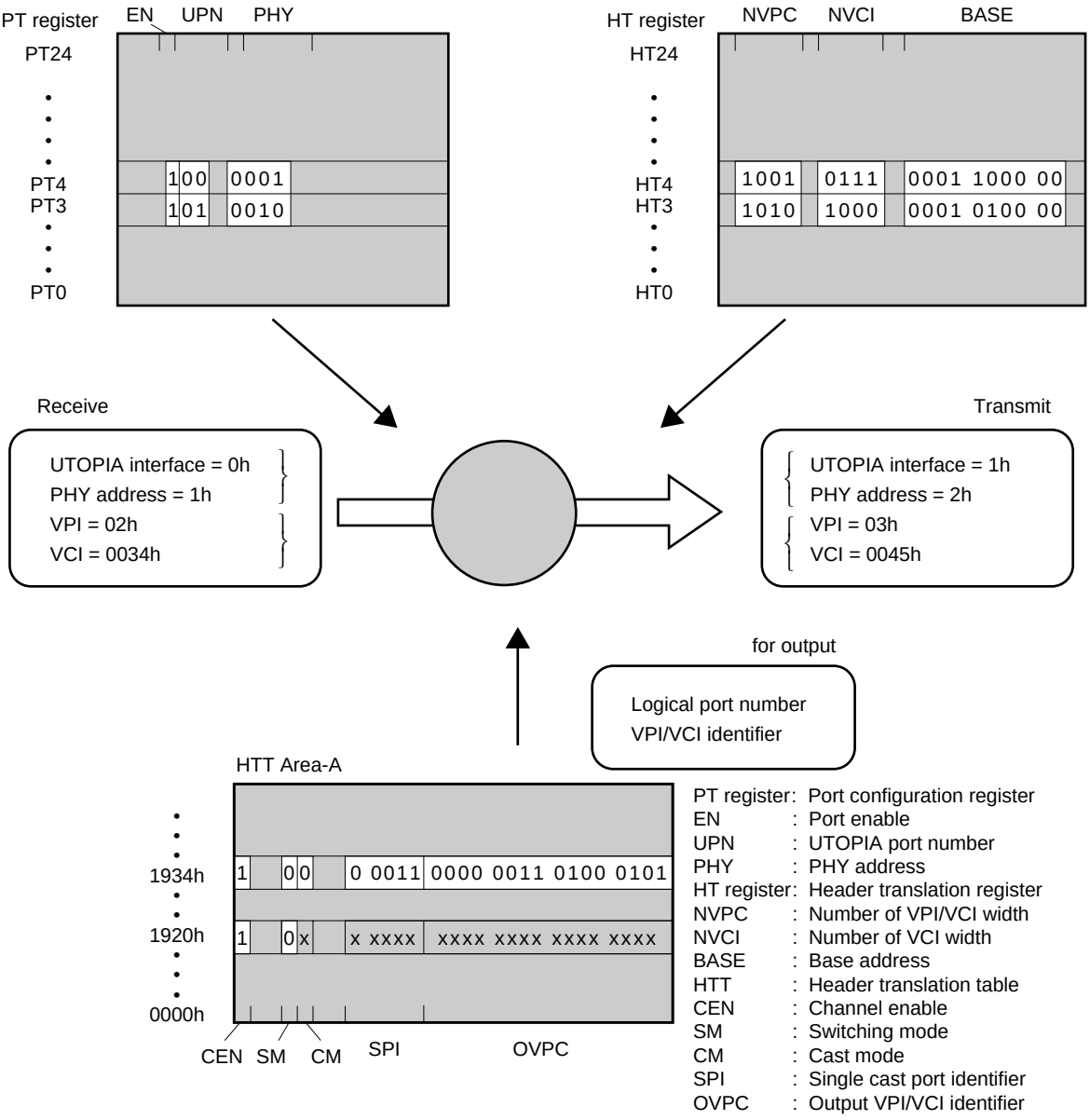
How the header translation operation is performed in the case of V_{CC} switching and single cast?

A.18

Let's assume the case where an input cell of UTOPIA interface = 0h, PHY address = 1h, VPI = 02h, and VCI = 0034h is output to UTOPIA interface = 1h, PHY address = 2h, VPI = 03h, VCI = 0045h.

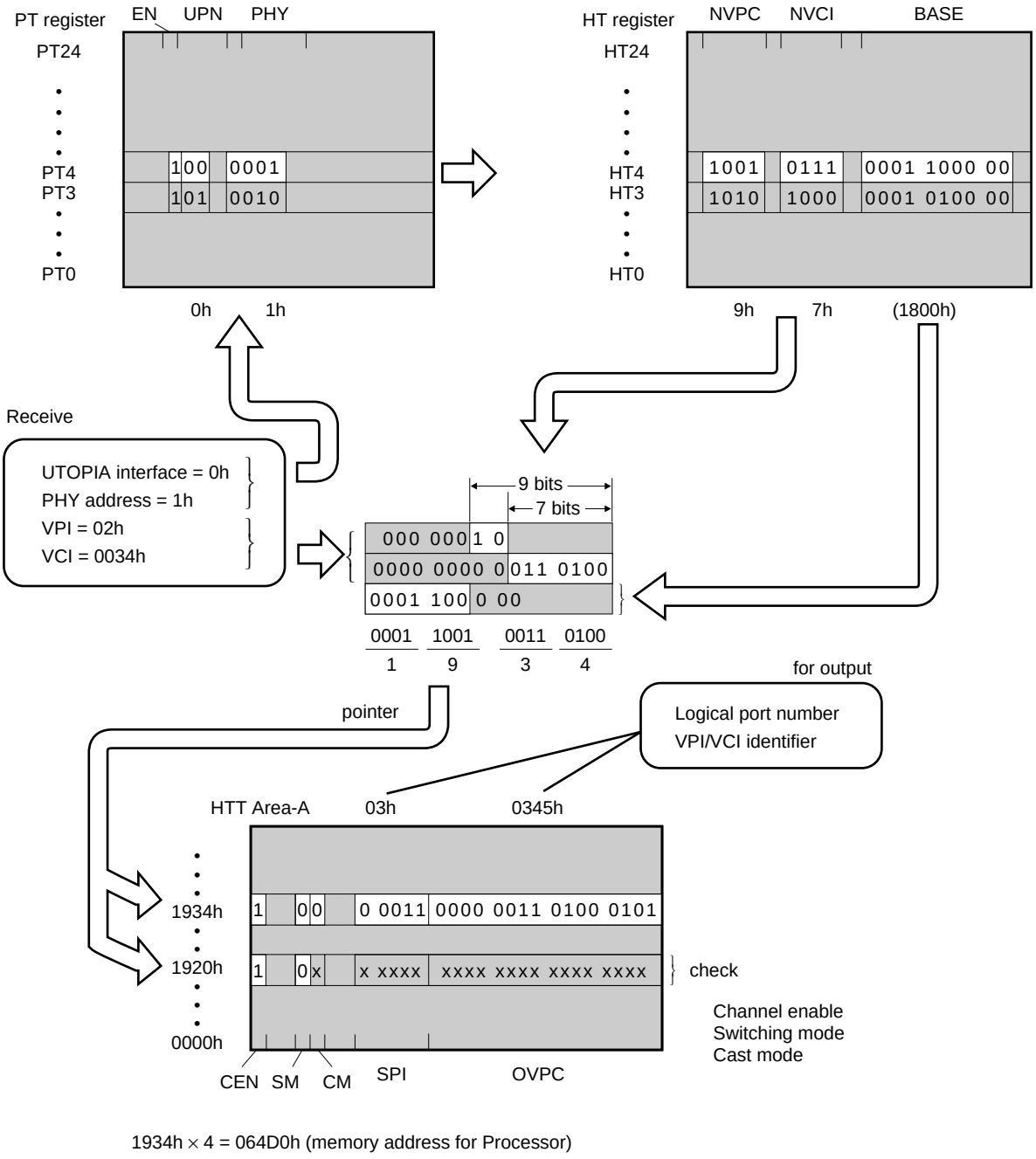
The X10's header translation operation in this case is shown in Figures 7-1 through 7-3.

Figure 7-1. Header Translation Flow (overall)



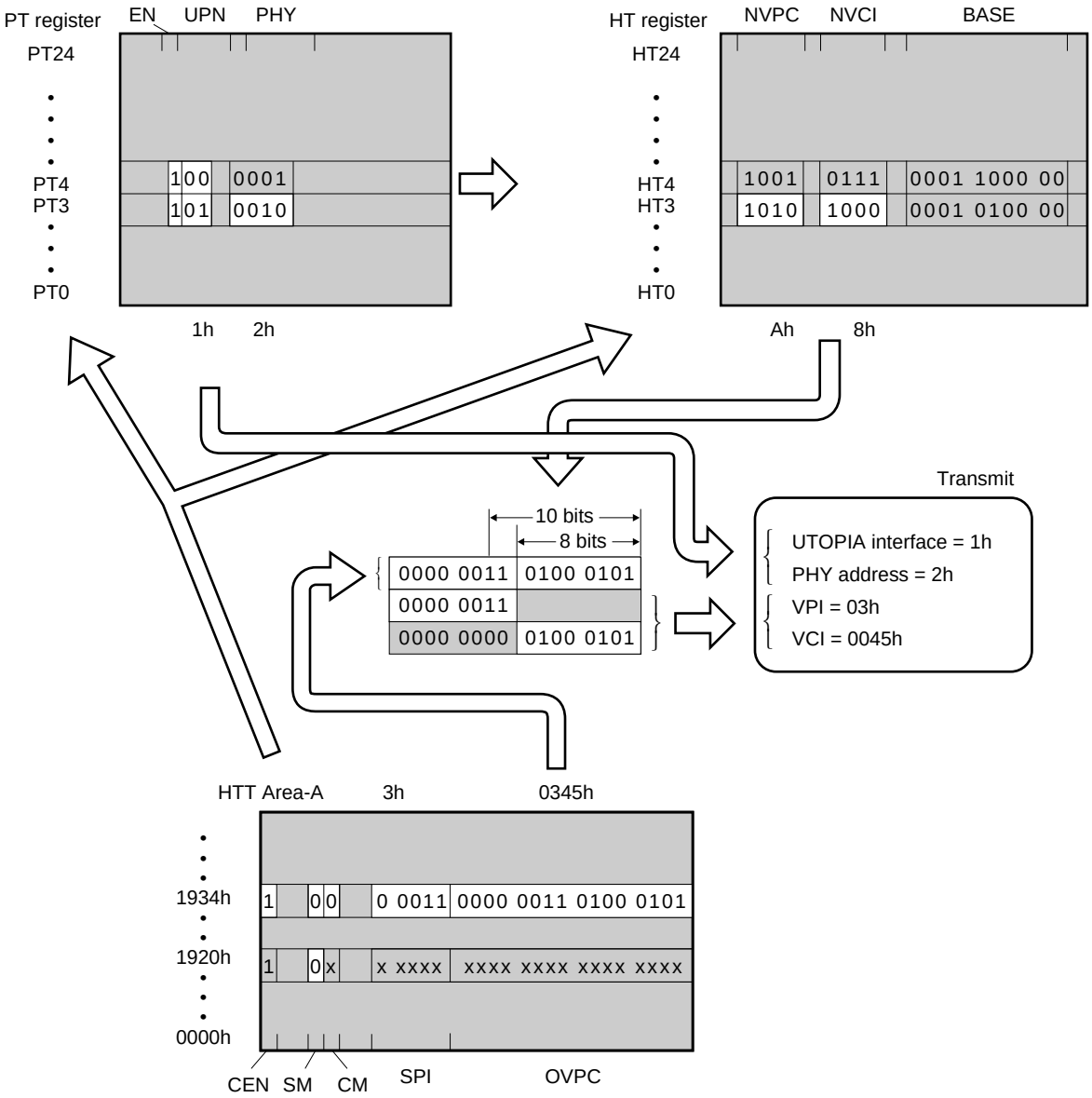
1934h × 4 = 064D0h (memory address for Processor)

Figure 7-2. Header Translation Flow (reception side)



1934h × 4 = 064D0h (memory address for Processor)

Figure 7-3. Header Translation Flow (transmission side)



Q.19

Give me a specific mapping example of the HTT memory.

A.19

For example, if the HT23 through HT0 registers are set as shown in Figure 7-4, the mapping of the HTT memory is as shown in Figure 7-5.

Figure 7-4. Example of Setting HT Registers

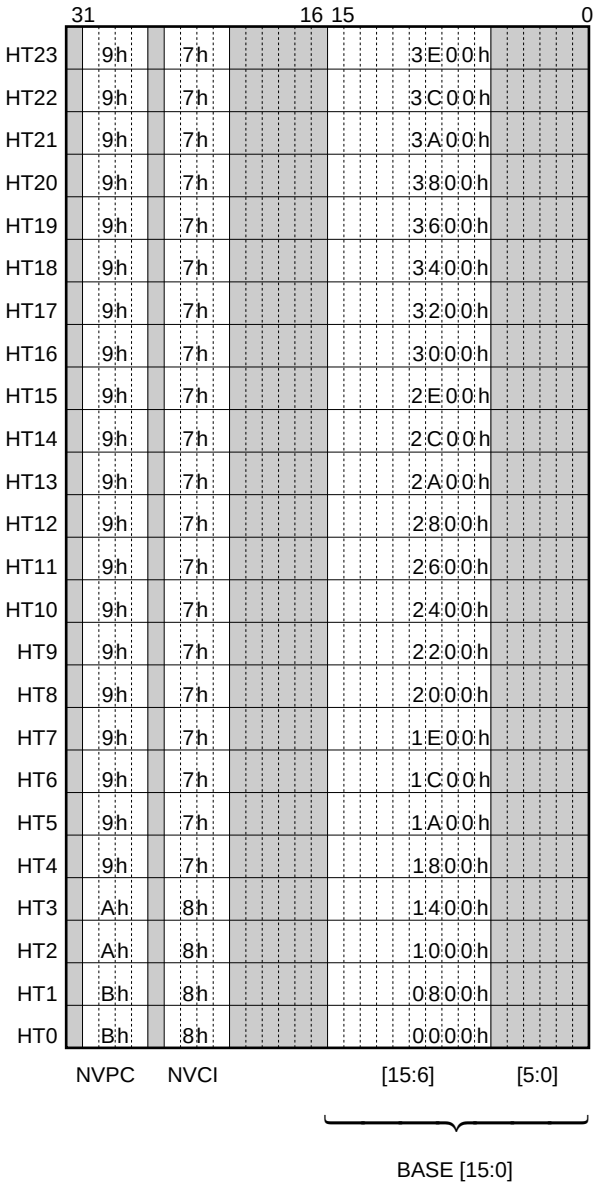
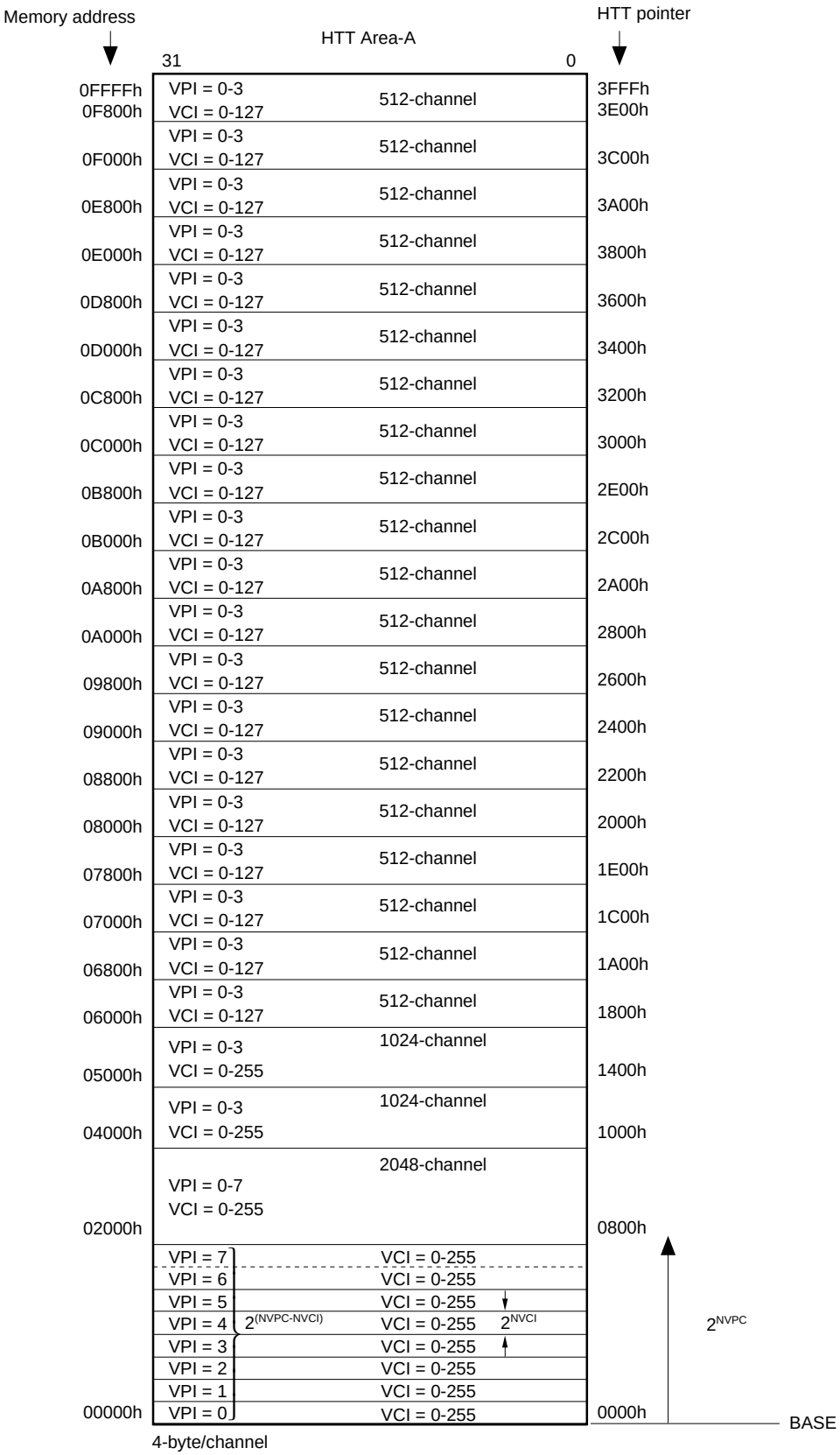


Figure 7-5. Example of HTT Memory Mapping

Example 1M-bits (×18) SRAM × 7



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