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RENESAS

# User's Manual


# μPD98404

## (NEASCOT-P30™)

## ADVANCED ATM SONET FRAMER

Document No. S11821EJ5V0UM00 (5th edition)
Date Published January 2003 NS CP(K)

**[MEMO]**

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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M8E 02. 11-1

## MAJOR REVISIONS IN THIS EDITION

| Page | Contents |
|---|---|
| | **CHAPTER 1 GENERAL** |
| | **1.3 System Configuration Example** |
| p.15 | Change of device used in the figure. |
| | **CHAPTER 2 PIN FUNCTION** |
| | **2.2.1 PMD interface** |
| p.22 | Addition of description to PMDALM pin. |
| | **2.2.6 Power supply and ground** |
| p.27 | Change of description to pins. |
| | **CHAPTER 3 FUNCTIONAL OUTLINE** |
| p.52 | Addition of description to **Table 3-10**. |
| p.55 | Addition of **Caution 2** to **Table 3-13**. |
| | **CHAPTER 4 INTERFACES** |
| p.63 | Change of description in **Table 4-2**. |
| p.73 | Addition of description to **4.2.1 (1)**. |
| p.74 | Change of **Figure 4-18**. |
| | **CHAPTER 7 BOARD LAYOUT** |
| p.150 | Change of description in **Table 7-1**. |
| | **CHAPTER 8 CONSTRAINTS** |
| p.156 | Addition of **8.2.3 Abnormal operation in ALP mode**. |
| p.157 | Addition of **8.2.4 Fixed receiver circuit status in RPLP mode**. |

**The mark ★ shows major revised points.**

# PREFACE

**Readers of this manual**

This manual is intended for user engineers who wish to design and develop an application system using the μPD98404.

**Purpose**

This manual introduces the hardware functions of the μPD98404 in the following organization.

**Organization**

This manual consists of the following chapters.

- General
- Pin function
- Functional outline
- Interfaces
- Registers
- JTAG boundary scan
- Board layout
- Constraints

**How to Read This Manual**

It is assumed that the readers of this manual have a general knowledge of electricity, logic circuits, and microcomputers.

For the overall functions of the μPD98404
→ Read this manual in the order of Table of Contents.

For the electrical characteristics of the μPD98404
→ Refer to the Data Sheet separately available.

The data bit string of SONET/SDH is transmitted by the μPD98404 via the PMD interface, starting from the MSB. In this manual, the bits in the overhead of the SONET/SDH framer are referred to using the following two types of bit names:

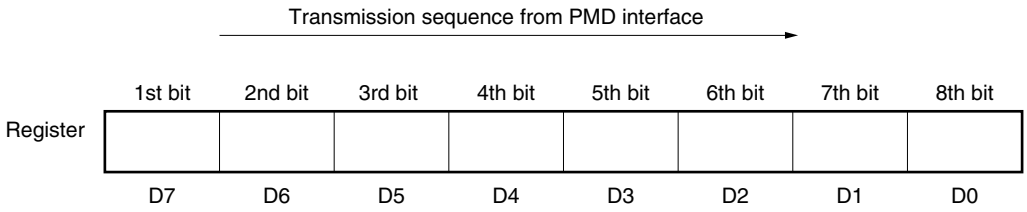
**(1) First bit through eighth bit**

These bit names are mainly used to indicate a bit string in the overhead byte in the SONET/SDH frame and indicate in the order in which the bits are output from the PMD interface.

**(2) D7 bit through D0 bit**

These bit names are mainly used to indicate the bits of an internal register of the μPD98404 and are equivalent to the D7 through D0 pins of the external management interface.

- Indication of bits in internal register




**Conventions**

| | | |
|---|---|---|
| Data significance | : | Left: high-order digit, Right: low-order digit |
| Active low | : | ××××_B (_B after pin or signal name) |
| Address of memory map | : | Top: High-order, bottom: low-order |
| **Note** | : | Explanation of items marked with **Note** in the text |
| **Caution** | : | Important information |
| **Remark** | : | Supplement |
| Numeric notation | : | Binary … ×××× or ××××B |
| | | Decimal number ... ×××× |
| | | Hexadecimal number ... ××××H |

**Related documents**

Some of the related documents listed below are preliminary versions but are not so specified here.

- Brochure : S11631E
- Data sheet : S11822E

TABLE OF CONTENTS

## LIST OF FIGURES (1/2)

## LIST OF FIGURES (2/2)

## LIST OF TABLES

# CHAPTER 1 GENERAL

The μPD98404 NEASCOT-P30™ is one of ATM-LAN LSIs and is intended for use in ATM adapter boards, ATM hubs, and ATM switches to connect an personal computer or an workstation to an ATM network. This LSI provides the functions of the TC sublayer of the SONET/SDH-base physical layer of the ATM protocol specified by ATM Forum UNI3.1 Recommendation.

Its main functions include a transmission function to map an ATM cell passed from an ATM layer to the payload of 155 Mbps SONET STS-3c/SDH STM-1 frame and transmit the circuit side to the PMD (Physical Media Dependent) sublayer of the physical layer, and a reception function to separate the overhead and ATM cell from the data string received from the circuit side and transmit the ATM cell to the ATM layer device. In addition, the μPD98404 also has a clock recovery function to extract sync clock for reception of receive data from the bit stream, and a clock synthesis function to generate a clock for transmission.

## 1.1 Features

- Clock recovery function/clock synthesis function
- Supplies function of TC sublayer of ATM protocol physical layer
- Supports 155 Mbps SONET STS-3c frame/SDH STM-1 frame formats
- Conforms to ATM Forum UTOPIA interface Level2 V1.0 (June 1995), and supports three modes for the interface with the ATM layer device.
  - Single PHY octet level handshake
  - Single PHY cell level handshake
  - Multi-PHY mode
- Selectable drop/pass length for unassigned cells
- Supports internal PMD layer return and ATM layer return loopback functions
- Supports two types of PMD interfaces: serial and parallel
  - 155.52 Mbps serial interface
  - 19.44 MHz parallel interface
- Overhead information writing/reading registers
  SOH (Section Overhead): J0 byte, Z0 (first and second) byte, F1 byte
  LOH (Line Overhead) : K1 byte, K2 byte
  POH (Pass Overhead) : F2 byte, C2 byte, H4 byte
- Supports pseudo transmission test function for each errors
- Supports JTAG boundary scan test (IEEE 1149.1)
- CMOS technology
- +3.3 V single power source
- Many OAM (Operation And Maintenance) functions

**Transmission side**

- Transmission of various types of alarm signals
  - Automatic return transmission on occurrence
    Line RDI, Path RDI
    Line REI, Path REI
  - Transmission on command
    Line AIS, Path AIS
- Pseudo error generation frame transmission function
  LOS generation frame
  OOF, LOF generation frame
  LOP generation frame
  OCD, LCD generation frame
  B1 error generation frame
  B2 error generation frame
  B3 error generation frame

**Reception side**

- Detection of alarm and error signals
  LOS (Loss Of Signal)
  OOF (Out Of Frame)
  LOF (Loss Of Frame)
  LOP (Loss Of Pointer)
  OCD (Out of Cell Delineation)
  LOC (Loss Of Cell delineation)
  Line RDI, Path RDI
  Line AIS, Path AIS
- Detection and indication of cause of quality degradation
  B1 error, B2 error, B3 error, Line REI, Path REI
- Counters counting number of times of error generation
  B1 byte error counter (16-bit width)
  B2 byte error counter (20-bit width)
  B3 byte error counter (16-bit width)
  Line REI error counter (20-bit width)
  Path REI error counter (16-bit width)
  Reception side Frequency Justification processing counter (12-bit width)
  HEC error dropped cell counter (20-bit width)
  FIFO overflow dropped cell counter (20-bit width)
  Valid cell counter (20-bit width)

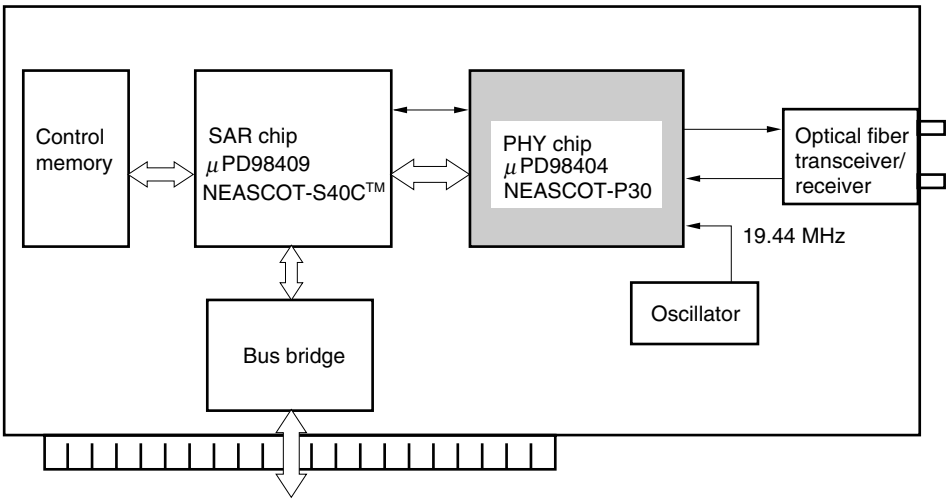
## 1.2 Ordering Information

| Part Number | Package |
|---|---|
| $\mu$PD98404GJ-KEU | 144-pin plastic QFP (fine pitch) (20 $\times$ 20) |

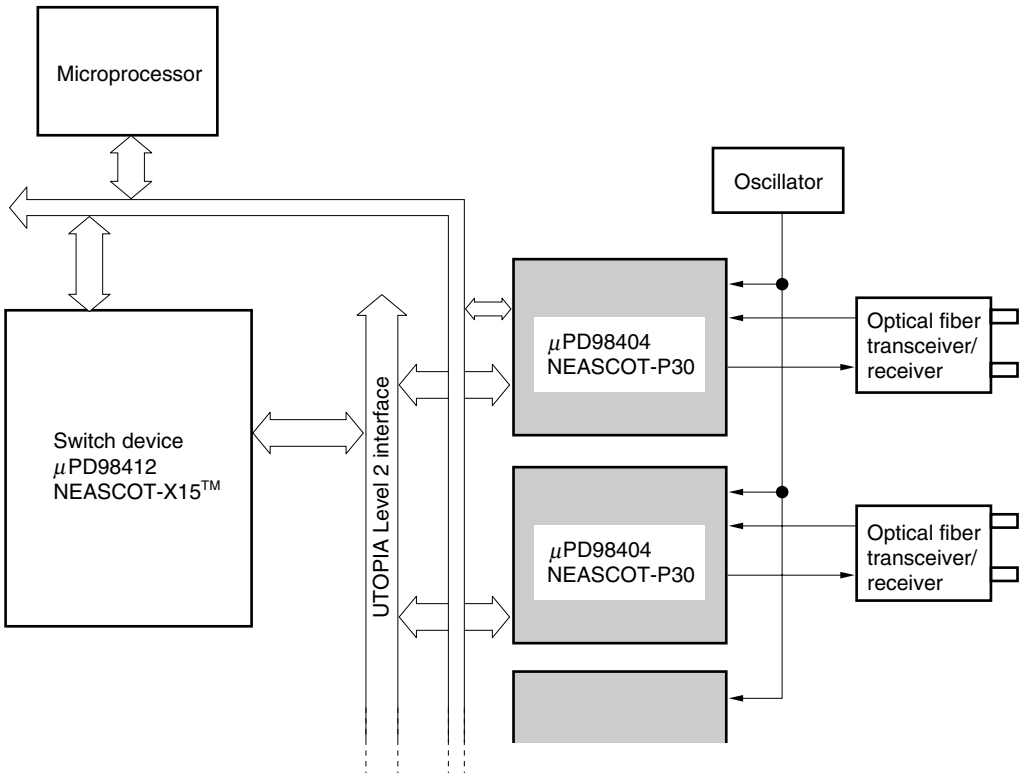
## 1.3 System Configuration Example

An example of a system using the μPD98404 is shown below.

★ **ATM adapter card application**

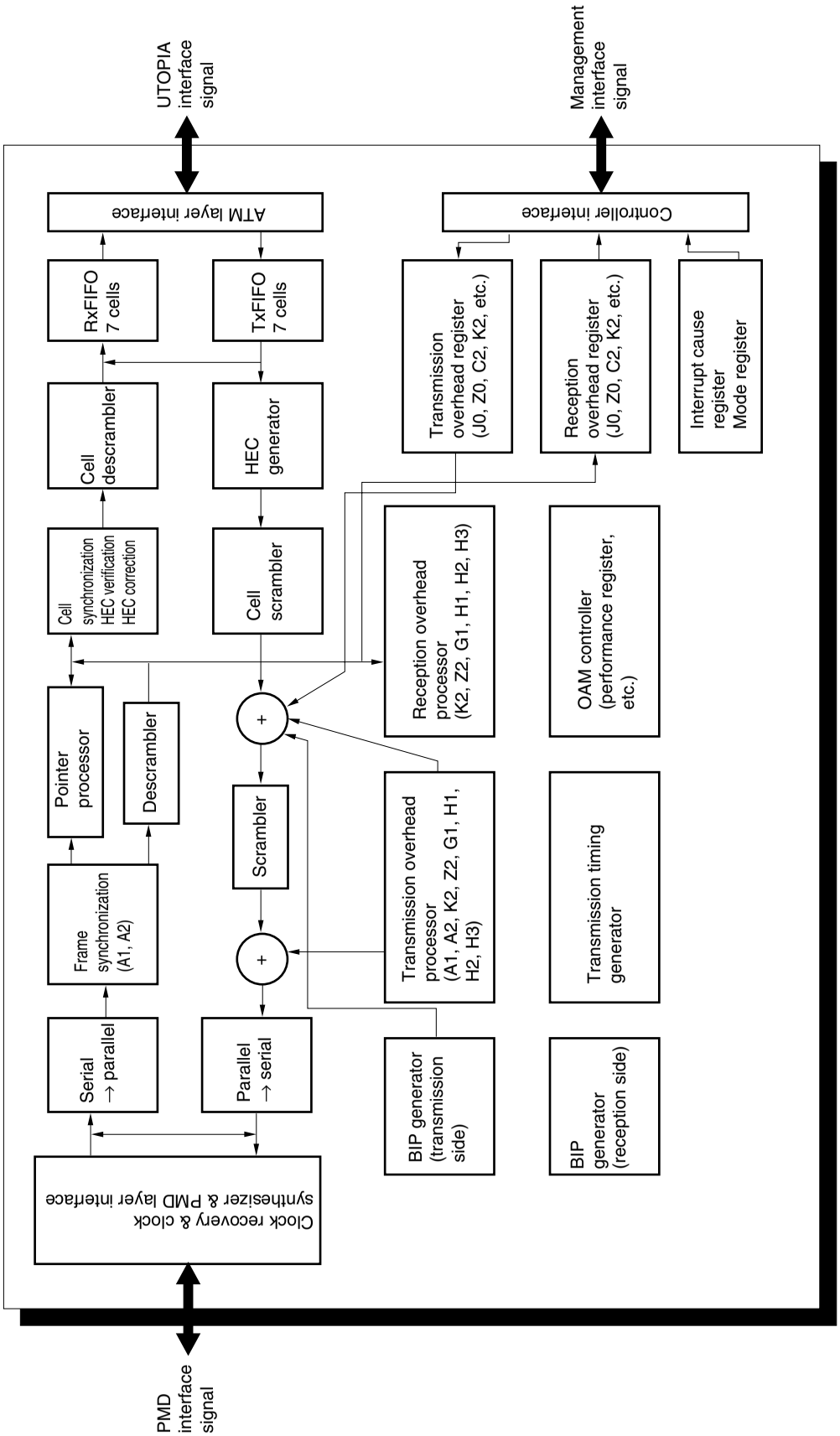



**Hub (terminal side) application**

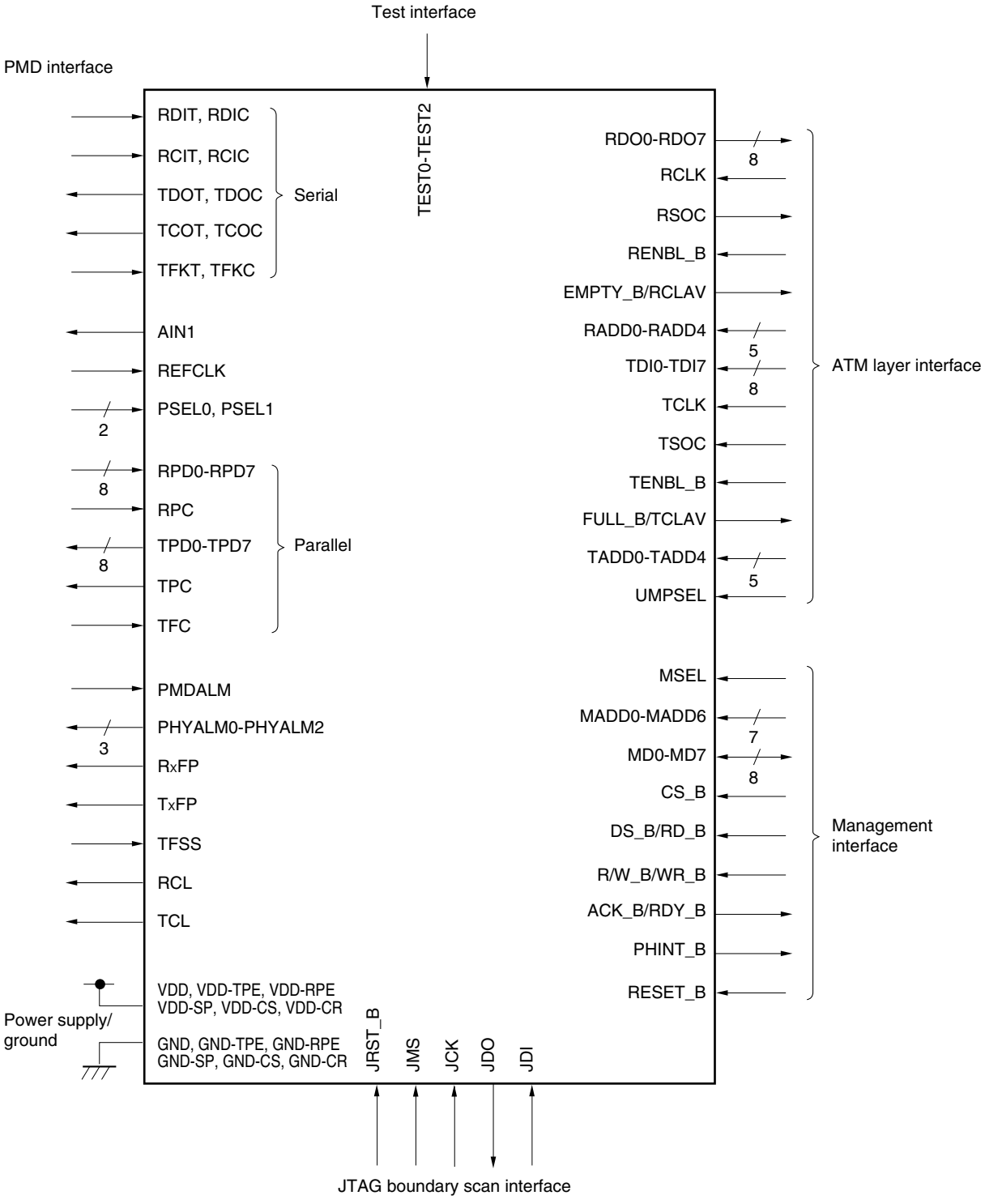


Phase-out/Discontinued

## 1.4 Block Diagram

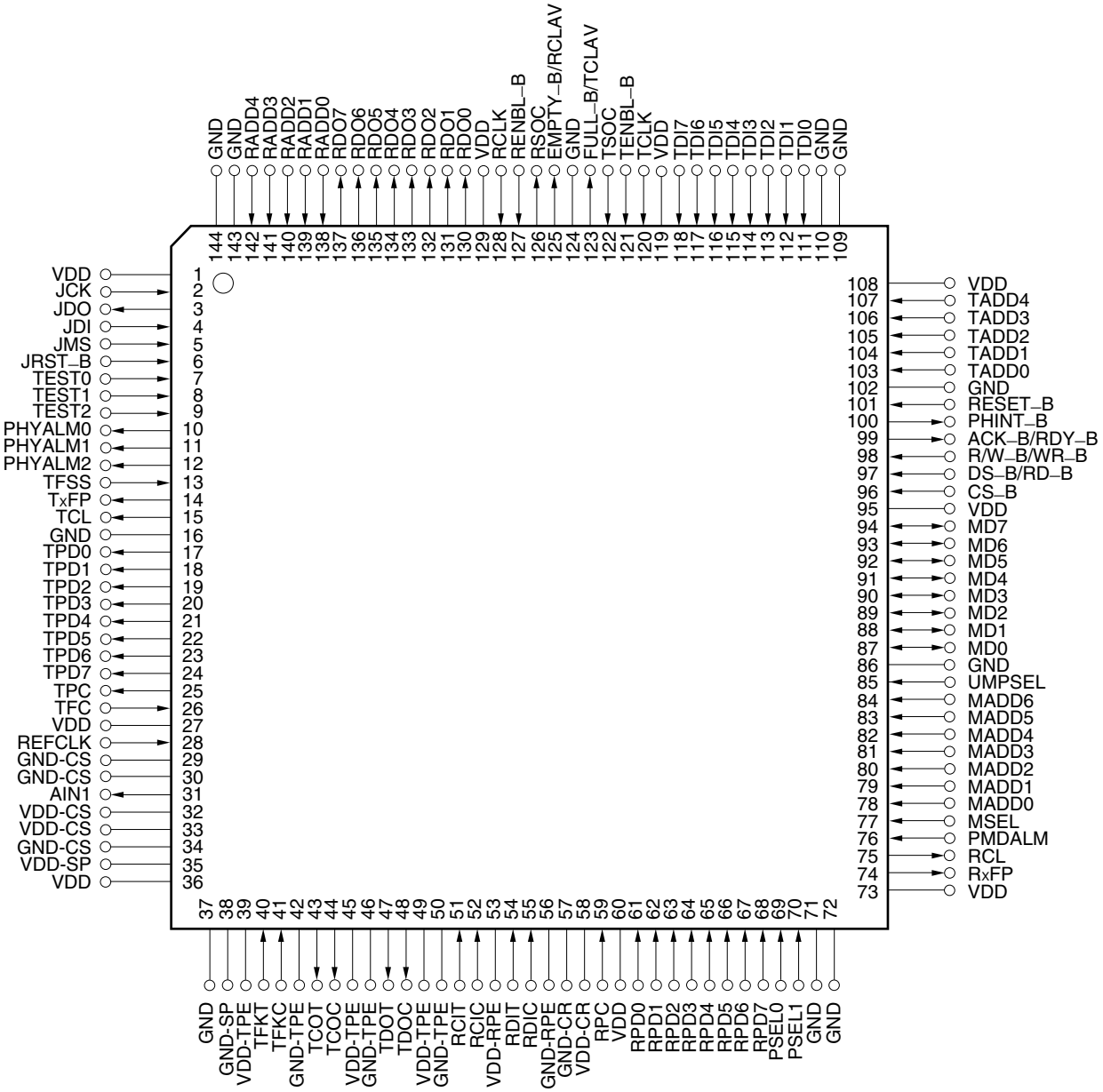


## 1.5 Pin Configuration



## 2.1 Pin Configuration

- **144-pin plastic QFP (fine pitch) (20 × 20) (Top View)**



**Pin Assignment**

| Number | Pin Name | Number | Pin Name | Number | Pin Name | Number | Pin Name |
|---|---|---|---|---|---|---|---|
| 1 | VDD | 37 | GND | 73 | VDD | 109 | GND |
| 2 | JCK | 38 | GND-SP | 74 | RxFP | 110 | GND |
| 3 | JDO | 39 | VDD-TPE | 75 | RCL | 111 | TDI0 |
| 4 | JDI | 40 | TFKT | 76 | PMDALM | 112 | TDI1 |
| 5 | JMS | 41 | TFKC | 77 | MSEL | 113 | TDI2 |
| 6 | JRST_B | 42 | GND-TPE | 78 | MADD0 | 114 | TDI3 |
| 7 | TEST0 | 43 | TCOT | 79 | MADD1 | 115 | TDI4 |
| 8 | TEST1 | 44 | TCOC | 80 | MADD2 | 116 | TDI5 |
| 9 | TEST2 | 45 | VDD-TPE | 81 | MADD3 | 117 | TDI6 |
| 10 | PHYALM0 | 46 | GND-TPE | 82 | MADD4 | 118 | TDI7 |
| 11 | PHYALM1 | 47 | TDOT | 83 | MADD5 | 119 | VDD |
| 12 | PHYALM2 | 48 | TDOC | 84 | MADD6 | 120 | TCLK |
| 13 | TFSS | 49 | VDD-TPE | 85 | UMPSEL | 121 | TENBL_B |
| 14 | TxFP | 50 | GND-RPE | 86 | GND | 122 | TSOC |
| 15 | TCL | 51 | RCIT | 87 | MD0 | 123 | FULL_B/TCLAV |
| 16 | GND | 52 | RCIC | 88 | MD1 | 124 | GND |
| 17 | TPD0 | 53 | VDD-RPE | 89 | MD2 | 125 | EMPTY_B/RCLAV |
| 18 | TPD1 | 54 | RDIT | 90 | MD3 | 126 | RSOC |
| 19 | TPD2 | 55 | RDIC | 91 | MD4 | 127 | RENBL_B |
| 20 | TPD3 | 56 | GND-RPE | 92 | MD5 | 128 | RCLK |
| 21 | TPD4 | 57 | GND-CR | 93 | MD6 | 129 | VDD |
| 22 | TPD5 | 58 | VDD-CR | 94 | MD7 | 130 | RDO0 |
| 23 | TPD6 | 59 | RPC | 95 | VDD | 131 | RDO1 |
| 24 | TPD7 | 60 | VDD | 96 | CS_B | 132 | RDO2 |
| 25 | TPC | 61 | RPD0 | 97 | DS_B/RD_B | 133 | RDO3 |
| 26 | TFC | 62 | RPD1 | 98 | R/W_B/WR_B | 134 | RDO4 |
| 27 | VDD | 63 | RPD2 | 99 | ACK_B/RDY_B | 135 | RDO5 |
| 28 | REFCLK | 64 | RPD3 | 100 | PHINT_B | 136 | RDO6 |
| 29 | GND-CS | 65 | RPD4 | 101 | RESET_B | 137 | RDO7 |
| 30 | GND-CS | 66 | RPD5 | 102 | GND | 138 | RADD0 |
| 31 | AIN1 | 67 | RPD6 | 103 | TADD0 | 139 | RADD1 |
| 32 | VDD-CS | 68 | RPD7 | 104 | TADD1 | 140 | RADD2 |
| 33 | VDD-CS | 69 | PSEL0 | 105 | TADD2 | 141 | RADD3 |
| 34 | GND-CS | 70 | PSEL1 | 106 | TADD3 | 142 | RADD4 |
| 35 | VDD-SP | 71 | GND | 107 | TADD4 | 143 | GND |
| 36 | VDD | 72 | GND | 108 | VDD | 144 | GND |

| | | |
|---|---|---|
| ACK_B | : | Read/write Cycle Receive Acknowledge |
| AIN1 | : | External Filter Connection |
| CS | : | Chip Select |
| DS_B | : | Data Strobe |
| EMPTY_B | : | Output Buffer Empty |
| FULL_B | : | Buffer Full |
| GND | : | Ground |
| GND-RPE | : | Ground for Receive PECL buffer |
| GND-CR | : | Ground for Clock Recovery Circuit |
| GND-CS | : | Ground for Clock Synthesis |
| GND-SP | : | Ground for Serial/Parallel Circuit |
| GND-TPE | : | Ground for Transmit PECL buffer |
| JCK | : | JTAG Clock |
| JDI | : | JTAG Data Input |
| JDO | : | JTAG Data Output |
| JMS | : | JTAG Mode Select |
| JRST_B | : | JTAG Reset |
| MADD0-MADD6 | : | Management Interface Address Bus |
| MD0-MD7 | : | Management Interface Data Bus |
| MSEL | : | Management Interface Mode Select |
| PHINT_B | : | Physical Interrupt |
| PHYALM0-PHYALM2 | : | PHY Alarm Detection |
| PMDALM | : | PMD Device Alarm |
| PSEL0, PSEL1 | : | PMD Mode Select |
| RADD0-RADD4 | : | Receive PHY Device Address |
| RCIC | : | Receive Clock Input Complement |
| RCIT | : | Receive Clock Input True |
| RCL | : | Internal Receive System Clock |
| RCLAV | : | Receive Cell Available |
| RCLK | : | Receive Data Transferring Clock |
| RD_B | : | Read Select |
| RDIC | : | Receive Data Input Complement |
| RDIT | : | Receive Data Input True |
| RDO0-RDO7 | : | Receive Data Output |
| RDY_B | : | Ready Signal |
| REFCLK | : | System Clock |
| RENBL_B | : | Receive Data Enable |
| RESET_B | : | System Reset |
| RPC | : | Receive Parallel Data Clock |
| RPD0-RPD7 | : | Receive Parallel Data |
| RSOC | : | Receive Start Address of ATM Cell |
| RxFP | : | Receive Frame Pulse |
| R/W_B | : | Read/write Control |
| TADD0-TADD4 | : | Transmit PHY Device Address |
| TCL | : | Internal Transmit System Clock |
| TCLAV | : | Transmit Cell Available |
| TCLK | : | Transmit Data Transferring Clock |
| TCOC | : | Transmit Clock Output Complement |
| TCOT | : | Transmit Clock Output True |
| TDI0-TDI7 | : | Transmit Data Input from the ATM Layer |
| TDOC | : | Transmit Data Output Complement |
| TDOT | : | Transmit Data Output True |
| TENBL_B | : | Transmit Data Enable |
| TEST0-TEST2 | : | Test Mode Pin |
| TFC | : | Transmit Reference Clock |
| TFKC | : | Transmit Reference Clock Complement |
| TFKT | : | Transmit Reference Clock True |
| TFSS | : | Transmit Frame Set Signal |
| TPC | : | Transmit Parallel Data Clock |
| TPD0-TPD7 | : | Transmit Parallel Data |
| TSOC | : | Transmit Start Address of ATM Cell |
| TxFP | : | Transmit Frame Pulse |
| UMPSEL | : | UTOPIA Multi-PHY Mode Select |
| VDD | : | Supply Voltage for Logic Circuit |
| VDD_RPE | : | Voltage Supply for Receive PECL buffer |
| VDD-CR | : | Voltage Supply for Clock Recovery Circuit |
| VDD-CS | : | Voltage Supply for Clock Synthesis |
| VDD-SP | : | Voltage Supply for Serial/Parallel Circuit |
| VDD_TPE | : | Voltage Supply for Transmit PECL buffer |
| WR_B | : | Write Select |

## 2.2 Pin Function

### 2.2.1 PMD interface (1/3)

| Pin Name | Pin No. | I/O Level | I/O | Function |
|---|---|---|---|---|
| RDIT | 54 | P-ECL True (+) | I | Receive serial data input pins. The input data is sampled with the recovered clock from the internal clock recovery PLL when PSEL[1:0] = “00”. When PSEL[1:0] = “01”, the data is sampled with the clock input to RCIT/RCIC. |
| RDIC | 55 | P-ECL Complement (–) | I | |
| RCIT | 51 | P-ECL True (+) | I | Receive serial clock input pins (155.52 MHz). When PSEL[1:0] = “01”, these pins are used as the receive clock. |
| RCIC | 52 | P-ECL Complement (–) | I | |
| TDOT | 47 | P-ECL True (+) | O | Transmit serial data output pins. Data is output from these pins in synchronization with the rising of serial clock TCOT. |
| TDOC | 48 | P-ECL Complement (–) | O | |
| TCOT | 43 | P-ECL True (+) | O | Transmit serial clock output pins (155.52 MHz). The clock generated by the internal synthesizer PLL is output as the transmit clock when PSEL[1:0] = “00”. When PSEL[1:0] = “01”, the clock input to TFKT/TFKC is output. Depending on the mode selected, the transmit data may be latched by the receive clock for output. Even in such a case, this pin outputs the clock of the internal synthesizer or the clock input to the TFKT/TFKC pin in accordance with the setting of the PSEL[1:0] pins. It does not output the receive recovery clock. |
| TCOC | 44 | P-ECL Complement (–) | O | |
| TFKT | 40 | P-ECL True (+) | I | Transmit serial clock input pins (155.52 MHz). When PSEL[1:0] = “01”, these pins are used as the transmit clock. |
| TFKC | 41 | P-ECL Complement (–) | I | |
| RPD0-RPD7 | 61-68 | TTL | I | Receive parallel data input pins. These pins input receive data when PSEL[1:0] = “1X”. The data input to these pins is sampled in synchronization with the rising of receive parallel clock RPC. |
| RPC | 59 | TTL | I | Receive parallel clock input pin (19.44 MHz). In the parallel mode when PSEL[1:0] = “1X”, this pin is used to input a clock (19.44 MHz) synchronized with a receive data. |
| TPD0-TPD7 | 17-24 | TTL | O | Transmit parallel data output pins. In the parallel mode when PSEL[1:0] = “1X”, transmit data is output from these pins in synchronization with the rising of PC. |
| TPC | 25 | TTL | O | Transmit parallel clock output pin. When PSEL[1:0] = “1X”, the clock (19.44 MHz) input to TFC is output. |
| TFC | 26 | TTL | I | Transmit parallel clock input pin. In the parallel mode when PSEL[1:0] = “1X”, this pin is used to input the transmit clock (19.44 MHz). If the TxCL bits [1:0] of the MDR1 register are set to 10 in the serial mode with PSEL[1:0] = “00”, input the 19.44 MHz source clock of the internal clock synthesizer PLL. |

### 2.2.1 PMD interface (2/3)

| Pin Name | Pin No. | I/O Level | I/O | Function |
|---|---|---|---|---|
| REFCLK | 28 | TTL | I | Reference clock input.<br>Inputs the system clock (19.44 MHz) to the internal clock recovery/synthesizer. Always input this clock. |
| PSEL0,<br>PSEL1 | 69, 70 | TTL | I | PMD interface mode select input.<br>Selects the mode of the PMD layer interface.<br>PSEL[1:0] =<br>00: Serial mode. The clock generated by the internal clock recovery & synthesizer PLL is used for transmission/reception.<br>01: Serial mode. An external clock is input to RCIT/RCIC TFKT/TFKC for transmission/reception.<br>1x: Parallel mode. The clock input to RPC & TFC is used. |
| AIN1 | 31 | Analog | I/O | Pin for connecting a loop filter for internal synthesizer PLL.<br>Leave open. |
| PMDALM | 76 | TTL | I | PMD layer alarm signal input.<br>The signal level of this pin is reflected in a state bit in an internal register, and a change in that bit can be used as an interrupt source.<br>Input the state signal of a peripheral device to this pin.<br>Input to this pin can be added as a condition of detecting the LOS error according to the setting of the PMD bit of the IACM register. For details, refer to **3.5 Alarm Report Pins (PHYALM[2:0], PMDALM)**. |
| PHYALM0-<br>PHYALM2 | 10-12 | TTL | O | PHY layer alarm detection signal output.<br>These signals report the detection of the internally monitored errors (PMDALM, CMDARM, LOS, OOF, LOF, LOP, OCD, LCD, Line AIS, Path AIS, Line RDI, Path RDI). One error or two or more errors ORed can be output to one of these pins. The errors to be reported can be selected by using the internal AMPR, AMR1, and AMR2 registers.<br>For details on use, refer to **3.5 Alarm Report Pins (PHYALM[2:0], PMDALM)** in **μPD98404 User's Manual (S11821E)**. |
| RxFP | 74 | TTL | O | Reception-side frame pulse output pin (8 kHz).<br>Outputs a pulse signal with a width of one clock cycle in synchronization with the RCL clock. |
| TxFP | 14 | TTL | O | Transmission-side frame pulse output pin (8 kHz).<br>Outputs a pulse signal with a width of one clock cycle in synchronization with the TCL clock. |
| TFSS | 13 | TTL | I | Transmit frame output disable signal input.<br>When this signal goes high, output of the transmit frame is stopped; when it goes low, transmission is started from the beginning of the frame. The μPD98404 samples this signal at the rising of the TCL clock. Transmission frame output is resumed after the TCL clock has risen for the 9th time after the rising edge at which the high level of this signal was last detected. |
| RCL | 75 | TTL | O | Reception side internal system clock output (19.44 MHz).<br>This pin outputs the receive clock divided by eight. The source receive clock differs depending on the mode selected (clock generated by the internal clock recovery or clock supplied from the RCIT/RCIC or RFC pin). Clock output from this pin is stopped while the device is being reset. |

### 2.2.1 PMD interface (3/3)

| Pin Name | Pin No. | I/O Level | I/O | Function |
|---|---|---|---|---|
| TCL | 15 | TTL | O | Transmission side internal system clock output (19.44 MHz).<br>This pin outputs the transmit clock divided by eight. The source transmit clock differs depending on the mode selected (clock generated by the internal synthesizer or clock supplied from the TCIT/TCIC or TFC pin). Clock output from this pin is stopped while the device is being reset. |

### 2.2.2 ATM layer interface (1/2)

| Pin Name | Pin No. | I/O Level | I/O | Function |
|---|---|---|---|---|
| RDO0-RDO7 | 130-137 | TTL | O (2-/3-state) | Receive data output pins.<br>These pins form an 8-bit data bus to output receive data to an ATM layer device. Data is output in synchronization with the rising of the RCLK clock. These pins operate in 2-state or 3-state mode in accordance with the UTOPIA interface mode. |
| RCLK | 128 | TTL | I | Receive clock input pin.<br>Inputs a clock for receive data transfer. A clock of up to 40 MHz is input. |
| RSOC | 126 | TTL | O (2-/3-state) | Receive cell start position signal output pin.<br>Outputs a signal that indicates the position of the first byte of a receive cell. This pin operates in 2-state or 3-state mode in accordance with the UTOPIA interface mode. |
| RENBL_B | 127 | TTL | I | Receive enable signal input pin.<br>Inputs a signal that indicates that the ATM layer is ready to accept receive data. |
| EMPTY_B/ RCLAV | 125 | TTL | O (2-/3-state) | Receive FIFO data transfer disable signal output or receive FIFO cell data transfer enable output pin.<br>This pin operates in two ways depending on the selected mode of the UTOPIA interface.<br>EMPTY_B indicates that no byte of receive data to be transferred to the ATM layer exists in the receive FIFO. RCLAV indicates that 1 or more bytes to be transferred to the ATM layer exist in the receive FIFO. |
| RADD0-RADD4 | 138-142 | TTL | I | Reception-side PHY address input pins.<br>These pins input an address to select a PHY layer device in the multi-PHY mode. |
| TDI0-TDI7 | 111-118 | TTL | I | Transmit data input pins.<br>These pins form an 8-bit data bus that inputs the transmit data. Data is input in synchronization with the rising of the TCLK clock. |
| TCLK | 120 | TTL | I | Transmit clock input pin.<br>Inputs a clock for transmit data transfer. A clock of 20 to 40 MHz is input.<br>**Caution The μPD98404 also uses this clock as the system clock of the management interface block. Therefore, always input a clock of 20 MHz or higher.** |
| TSOC | 122 | TTL | I | Transmit cell start position output pin.<br>This pin inputs a signal that indicates the position of the first byte of a transmit cell input to the μPD98404. |
| TENBL_B | 121 | TTL | I | Transmit enable input pin.<br>Inputs a signal that indicates that an ATM layer device outputs valid transmit data to TDI0 through TDI7. |

### 2.2.2 ATM layer interface (2/2)

| Pin Name | Pin No. | I/O Level | I/O | Function |
|---|---|---|---|---|
| FULL_B/ TCLAV | 123 | TTL | O (2-/3-state) | Transmit FIFO data transfer disable signal output or transmit FIFO cell data transfer enable output pin.<br>This pin operates in two modes depending on the mode of the UTOPIA interface.<br>FULL_B indicates that there is no vacant area available in the transmit FIFO that receives data transferred from the ATM layer. TCLAV indicates that one cell or more of vacant area is available in the transmit FIFO to store the data transferred. |
| TADD0- TADD4 | 103-107 | TTL | I | Transmission-side PHY address input pin.<br>Inputs an address to select a PHY layer device in the multi-PHY mode. |
| UMPSEL | 85 | TTL | I | Multi-PHY mode select signal input.<br>High : Multi-PHY mode.<br>When a high level is input to this pin, the multi-PHY mode is selected.<br>Low : Single PHY mode. |

### 2.2.3 Management interface (1/2)

| Pin Name | Pin No. | I/O Level | I/O | Function |
|---|---|---|---|---|
| MSEL | 77 | TTL | I | Management interface mode select signal input pin.<br>The mode of the management interface changes depending on the input level to this pin.<br>MSEL=:<br>1 : Selects <RD_B, WR_B, RDY_B> as pin function.<br>0 : Selects <DS_B, R/W_B, ACK_B> as pin function. |
| MADD0- MADD6 | 78-84 | TTL | I | Address input pins.<br>These pins form an address bus that inputs the addresses of the internal registers of the μPD98404. |
| MD0-MD7 | 87-94 | TTL | I/O (3-state) | 8-bit data bus.<br>This data bus reads or writes the data of the internal registers of the μPD98404. |
| CS_B | 96 | TTL | I | Chip select signal input pin.<br>When this pin goes low, access to the internal registers is enabled. |
| DS_B/ RD_B | 97 | TTL | I | Data strobe signal input or read signal input pin.<br>This pin has two functions: DS_B and RD_B. The function to be used depends on the mode selected by the MSEL pin.<br>MSEL = 0: Data strobe signal DS_B<br>MSEL = 1: RD_B that selects a read access. |

### 2.2.3 Management interface (2/2)

| Pin Name | Pin No. | I/O Level | I/O | Function |
|---|---|---|---|---|
| R/W_B/ WR_B | 98 | TTL | I | Read/write signal input or write signal input pin.<br>This pin has two functions: R/W_B and WR_B. The function to be used depends on the mode selected by the MSEL pin.<br>MSEL = 0: Read/write control signal R/W_B, as follows:<br>R/W_B=:<br>High level: Read cycle<br>Low level : Write cycle<br>MSEL = 1: WR_B that selects write access to the internal registers. |
| ACK_B/ RDY_B | 99 | TTL | O (3-state) | Data acknowledge signal output or ready signal output.<br>This pin has two functions: ACK_B and RDY_B. The function to be used depends on the mode selected by the MSEL pin.<br>MSEL = 0: Data strobe signal ACK_B<br>MSEL = 1: Read access select signal RDY_B |
| PHINT_B | 100 | TTL | O | Interface interrupt signal output pin.<br>This reports to the host that an interrupt has been generated by making it low active. |
| RESET_B | 101 | TTL | I | System reset signal input pin.<br>Initializes the $\mu$PD98404. Input a low-level pulse at least 1 $\mu$s wide. Particularly on power application, this pulse width must be maintained after the level of the supply voltage has reached 90% of the rated value.<br>When the RESET_B signal is input, the following clock must be input in accordance with the mode of the PMD interface.<br>In serial mode : TCLK/RCLK clock<br>In parallel mode : All TCLK/RCLK and TFC/RPC clocks |

### 2.2.4 JTAG boundary scan

| Pin Name | Pin No. | I/O Level | I/O | Function |
|---|---|---|---|---|
| JDI | 4 | TTL | I | Boundary scan data input.<br>Ground this pin when not used. |
| JDO | 3 | TTL | O (3-state) | Boundary scan data output.<br>Open this pin when not used. |
| JCK | 2 | TTL | I | Boundary scan clock input.<br>Ground this pin when not used. |
| JMS | 5 | TTL | I | Boundary scan mode select signal input.<br>Ground this pin when not used. |
| JRST_B | 6 | TTL | I | Boundary scan reset signal input.<br>Ground this pin when not used. |

**Remark** Processing of JTAG boundary scan pins not used (during normal operation)

The reason that the JRST_B pin is grounded when it is not used (during normal operation) is to better prevent malfunctioning of the JTAG logic. The JTAG pin may be also processed in either of the following ways:

- Reset the JTAG logic without using the JRST_B pin
  Reset the JTAG logic by using the JMS and JCK pins and keep it in the reset status (the JRST_B pin is pulled up).
  Fix the JMS pin to 1 (pull up) and input 5 clock cycles or more to the JCK pin.

- Reset the JTAG logic by using the JRST_B pin
  Input a low pulse of the same width as RESET_B of the μPD98404 to the JRST_B pin. If both the JMS and JRST_B pins are pulled up and kept high, the JTAG logic is not released from the reset status. Therefore, the normal operation is not affected. Fix the input level of the JDI and JCK pins by pulling them down or up.

### 2.2.5 Internal test pin

| Pin Name | Pin No. | I/O Level | I/O | Function |
|---|---|---|---|---|
| TEST0-<br>TEST2 | 7-9 | TTL | I | These pins are used to test the μPD98404.<br>Usually, ground all these pins.<br>TEST[2:0] = "000" : Normal operation<br>TEST[2:0] = Other than "000": Test mode |

★ **2.2.6 Power supply and ground**

| Pin Name | Pin No. | I/O | Function |
|---|---|---|---|
| VDD | 1, 27, 36, 60, 73, 95, 108, 119, 129 | — | General-purpose logic power supply (+3.3 V ± 0.15 V) and ground. |
| GND | 16, 37, 71, 72, 86, 102, 109, 110, 124, 143, 144 | — | |
| VDD-TPE | 39, 45, 49 | — | Output PECL I/O power supply (+3.3 V ± 0.15 V) and ground.<br>Noise on this power supply pin affects the jitter characteristics. Prevent noise by using a filter. |
| GND-TPE | 42, 46 | — | |
| VDD-RPE | 53 | — | Input PECL I/O power supply (+3.3 V± 0.15 V) and ground.<br>Noise on this power supply pin affects the jitter characteristics. Prevent noise by using a filter. |
| GND-RPE | 50, 56 | — | |
| VDD-SP | 35 | — | Serial/parallel block power supply (+3.3 V ± 0.15 V) and ground.<br>Noise on this power supply pin affects the jitter characteristics. Prevent noise by using a filter. |
| GND-SP | 38 | — | |
| VDD-CS | 32, 33 | — | Clock synthesizer PLL block power supply (+3.3 V ± 0.15 V) and ground.<br>Noise on this power supply pin affects the jitter characteristics. Prevent noise by using a filter. |
| GND-CS | 29, 30, 34 | — | |
| VDD-CR | 58 | — | Clock recovery PLL block power supply (+3.3 V ± 0.15 V) and ground.<br>Noise on this power supply pin affects the jitter characteristics. Prevent noise by using a filter. |
| GND-CR | 57 | — | |

## 2.3 Processing of Unused Pins

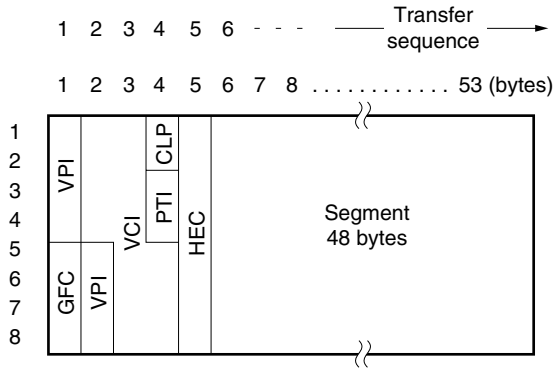
| Pin | Processing of Unused Pins |
|---|---|
| Each input pin at level other than P-ECL | Connect to ground (parallel input pin in serial mode)<br>RPD0 through RPD7, RPC, TFC<br>(Multi-PHY pins in single PHY mode)<br>TADD0 to TADD4, RADD0 through RADD4<br>(others)<br>TFSS (essential) |
| Each input pin at P-ECL level | Pull up True(+) pins (TFKT, RCIT, RDIT) to 3.3 V.<br>Connect Complement(–) pins (TFKC, RCIC, RDIC) to ground. |
| Output pin | Leave open.<br>(Parallel input pins in serial mode)<br>TPD0 to TPD7<br>TPC<br>(others)<br>TxFP, RxFP, TCL, RCL |
| Output pin at P-ECL level | Leave open.<br>TDOT, TDOC, TCOT, TCOC |
| AIN1 | Leave Open.<br>Because noise on this pin affects the characteristics of the internal PLL, do not wire a clock line in the vicinity. |

# CHAPTER 3 FUNCTIONAL OUTLINE

The major functions of the μPD98404 are to insert an ATM cell received from the ATM layer into a 155 Mbps SONET STS-3c/SDH STM-1 frame and output the cell to the circuit, or to receive the ATM cell from a receive SONET/SDH frame and output the cell to the ATM layer.

Figure 3-1 outlines the formats of an ATM cell (user-network interface) and a STS-3c frame.

**Figure 3-1. Structure of ATM Cell (user-network interface (UNI))**




GFC: Generic Flow Control, PTI: Payload Type Identifier

VPI: Virtual Path Identifier, CLP: Cell Priority

VCI: Virtual Channel Identifier, HEC: Header Error Control

**Figure 3-2. Outline of Frame Format (1/2)**

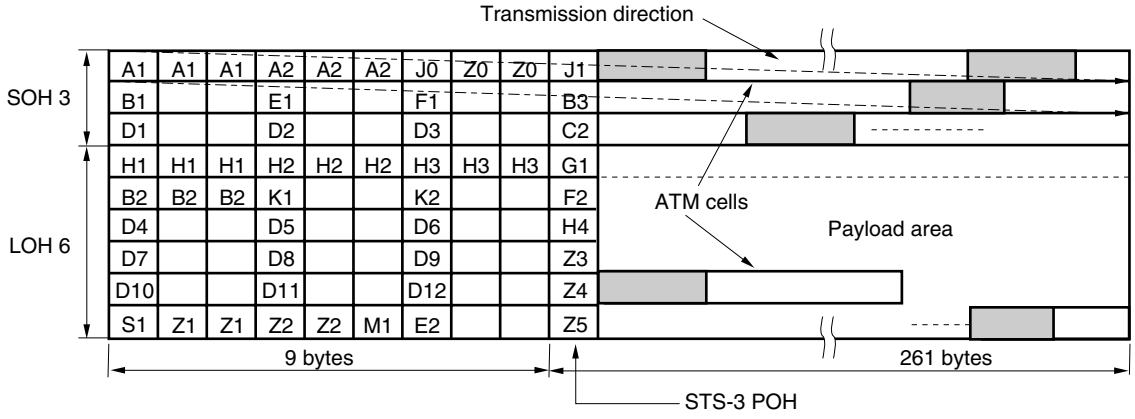
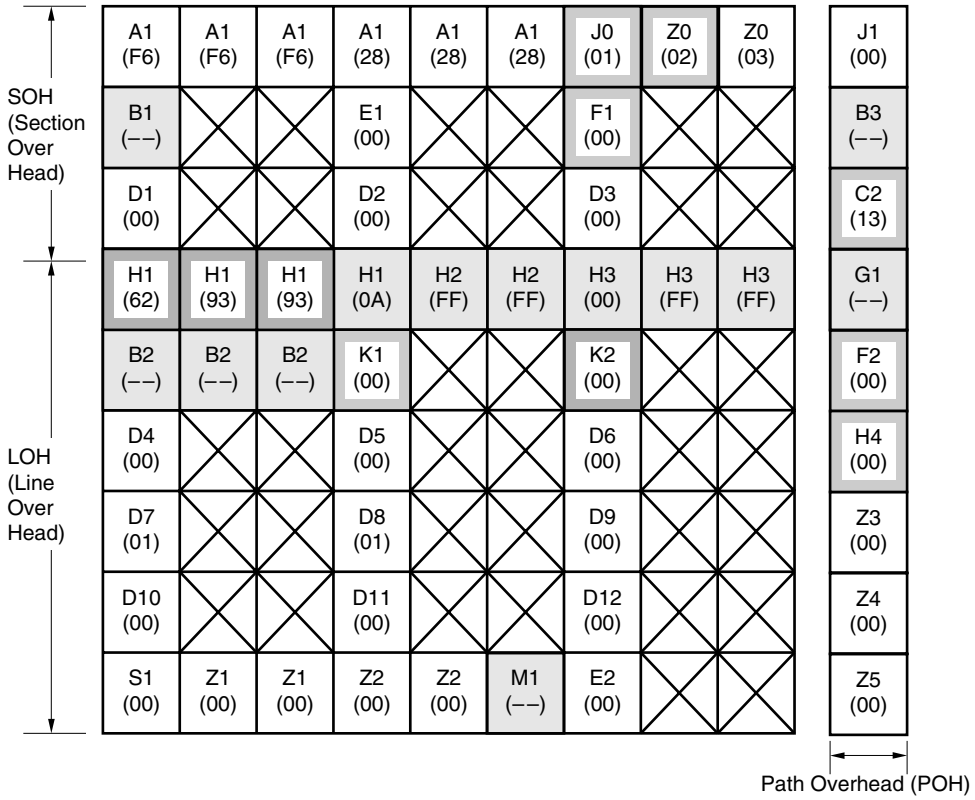


**Figure 3-2. Outline of Frame Format (2/2)**




( ) : Transmitter side default value (H)

: Byte area automatically inserted/verified by μPD98404

: Byte area that can be read or written by register access

: Byte area some bits of which can be changed by register write.

(Only SS bit of H1 byte can be rewritten.)

(Bits 1 through 5 of K2 byte can be rewritten.)

: Byte area that cannot be read or written

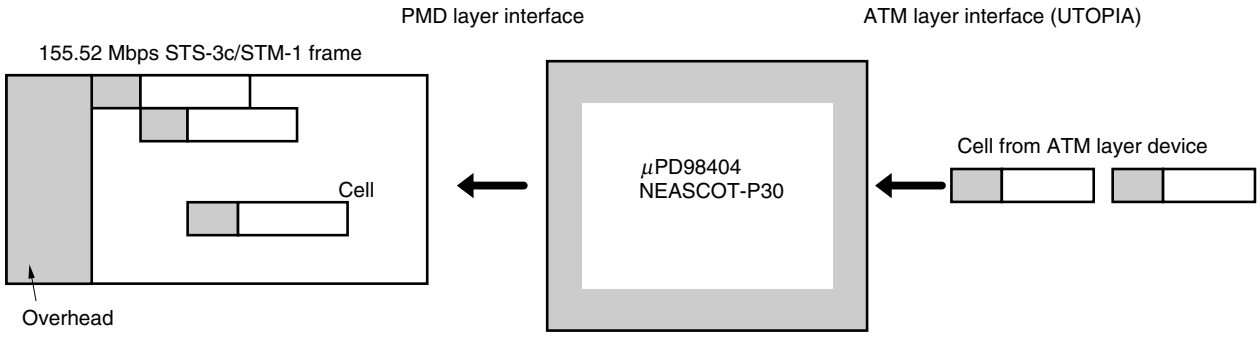
: Unused byte area. Insert 00H to this area.

A1, A2 : Framing
J0 : Section trace
Z0 : Spare
B1 : BIP-8
E1 : Order wire
F1 : User channel
D1-D3 : Data communication channel
H1, H2 : Pointer
H3 : Pointer action
B2 : BIP-24
K1 : Protection switching channel
K2 : Section alarm indication
D4-D12 : Data communication channel
S1 : Synchronization status
Z1 : Spare
Z2 : Spare
M1 : Error indication
E2 : Order wire
J1 : Path trace
B3 : Path BIP-8
C2 : Signal label
G1 : Error indication, path status
F2 : Path user channel
H4 : Position indicator
Z3-Z5 : Spare

## 3.1 Transmission Function

The transmission function of the μPD98404 inserts an ATM cell received from an ATM layer device into a SONET STS-3c/SDH STM-1 frame, and outputs the cell to the PMD interface. This section explains the frame transmission function of the μPD98404 mainly based on the flow of processing.

**Figure 3-3. Outline of μPD98404's Frame Transmission Function**




On power application, the μPD98404 starts operation in the mode determined by the default value of each mode register, and transmits STS-3c frames until the setting of the mode register is changed. At this time, the μPD98404 inserts idle cells (vacant cells) in the frames until it receives an ATM cell from an ATM layer device.

The μPD98404 processes transmit data in the following sequence:

**(1) Cell data reception from ATM layer device**

The μPD98404 receives 53 byte length cell data from an ATM layer device via the ATM layer interface and stores the data in the transmit FIFO. The transmit FIFO has a capacity of about 7 cells (384 bytes) and has a buffer function to adjust the rate between the ATM layer and PMD.

If there is a period during which no cell data is sent from the ATM layer and if the transmit data in the FIFO is 1 cell or less, vacant cell is inserted in the frame. The vacant cell to be inserted is in the idle cell format in the default mode. However, its format can be changed to the unassigned cell format by setting the idlenb bit of the mode register 2 (MDR2). Figure 3-3 shows these formats. For the details of the ATM layer interface, refer to **4.1 ATM Layer Interface**.

**Figure 3-4. Vacant Cell Format Inserted by μPD98404**

| | Header: 5 bytes | | | | | Payload: 48 bytes | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 1 | 2 | ··· | 47 | 48 |
| Idle cell | 00H | 00H | 00H | 01H | 52H | 6AH | 6AH | ··· | 6AH | 6AH |
| Unassigned cell | 00H | 00H | 00H | 00H | 55H | 00H | 00H | ··· | 00H | 00H |

**Remark** If cells in the idle cell or unassigned cell format are input to the ATM layer interface at the transmitter side of the μPD98404, the μPD98404 handles them in the same manner as normal valid data, maps them to a frame and outputs the frame to the circuit side. It does not internally discard the cells.

**(2) Generation of HEC**

CRC operation is performed on the high-order 4 bytes of the 5 bytes of the header of an ATM cell. The value resulting from the operation plus “55H” is overwritten to the fifth byte position of the ATM header to carry out HEC (Header Error Check).

Polynomial G (X) = $X^8 + X^2 + X + 1$

**Remark** The $\mu$PD98404 does not check the content of the fifth byte (position of HEC) from the beginning of the cell data input from the ATM layer device, or does not internally use the content. Because the value of the calculated HEC is overwritten to this byte area, the ATM layer device must insert a dummy byte such as "“00H” into this area.

**(3) Scramble of ATM cell**

The data of an ATM is scrambled by using the following polynomial. The range of scramble is limited to the payload of the ATM cell.

Polynomial G (X) = $X^{43} + 1$

The user can select a scramble stop mode for the purpose of testing. The scramble stop mode is set by the CSCRM bit of mode register 3 (MDR3).

**(4) Generation of frame**

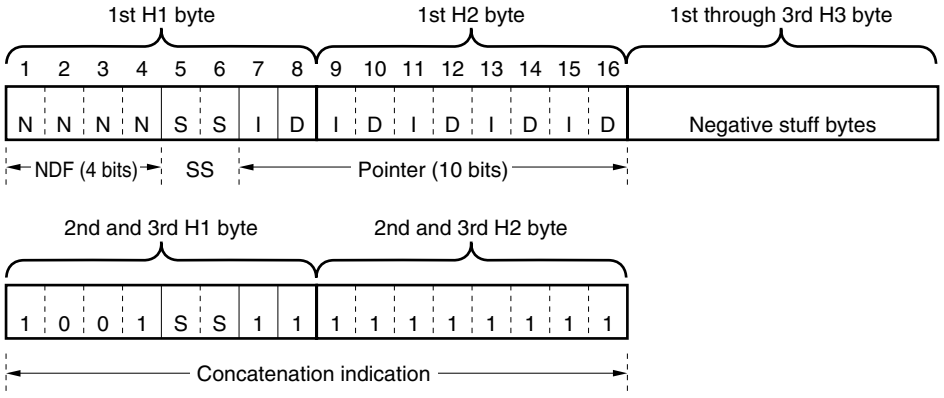
SONET frame format is generated by multiplexing the overhead information on successive ATM cells. The $\mu$PD98404 generates H1, H2, H3, K2, Z2, G1, A1, and A2 bytes as frame overhead information, links these bytes with the payload. For the format of the frame, refer to **Figure 3-2. Outline of Frame Format**.

(a) AU pointer and generation of byte information

The transmit frame sent out by the $\mu$PD98404 does not change the position of POH (Path Overhead). Nor is the position of the J1 byte changed. Therefore, the pointer value to be assigned to the H1 and H2 bytes is always 20AH = “1000001010”, and NDF is fixed to “0110” (disable). The SS bits, which are the fifth and sixth bits of the H1 byte, are “00” as default assumption. These bits can be changed by setting the SS bit table of the MDR1 register.

Because the transmitter side does not request Frequency Justification (stuff operation), no data is stored in the H3 bytes that are used as de-stuff bytes.

**Figure 3-5. Format of AU Pointer (H1 through H3 bytes)**



**Remark** NDF : New Data Flag. Enable or disable command when the pointer value is changed. The μPD98404 does not change the pointer value (disable).

SS bit : Indicates the type of the virtual container. Insert the bit stored in the SS table of MDR1. The default value is "00".

Pointer : Indicates the position of the first byte J1 of POH and indicates Frequency Justification (stuff operation).

I (Increment bit) : Positive Justification (positive stuff) operation request

D (Decrement bit) : Negative Justification (negative stuff) operation request

Concatenation indication : Indicates concatenation.

**H1 through H3 Bytes of Transmit Frame**

| | H1 Byte | H2 Byte | H3 Byte |
|---|---|---|---|
| 1st | 0110 SS10 | 0000 1010 | 0000 0000 |
| 2nd | 1001 SS11 | 1111 1111 | 1111 1111 |
| 3rd | 1001 SS11 | 1111 1111 | 1111 1111 |

Insert registers are available for bytes J0, Z0, F1, K1, K2, F2, C2, and H4 of the byte information of the overhead. Any value can be stored and transmitted by setting the insert register. The μPD98404 transmits the default value unless changed.

(b) Transmit BIP generation

The μPD98404 performs a BIP (Bit Interleaved Parity) operation on the transmit data, and inserts the result of the operation to the positions equivalent to the B1, B2, and B3 bytes of the next transmit overhead data.

For details, refer to **3.3.1 (2) Functions related to monitoring circuit quality on transmission side**.

**(5) Scramble of frame**

The frame to be transmitted is scrambled with the polynomial below. The entire range of the STS-3c/SDH STM-1 frame, except the 9 bytes from the beginning "A1 (1), A1 (2), A1 (3), A2 (1), A2 (2), A2 (3), C1 (1), C1 (2), C1 (3)", is scrambled.

Polynomial $G(X) = 1 + X^6 + X^7$

The user can select a scramble stop mode for the purpose of testing. The scramble stop mode is selected by the FSCRM bit of mode register 3 (MDR3).

**(6) Output from PMD interface**

The PMD interface converts data into an 8-bit parallel string or serial data string for output.

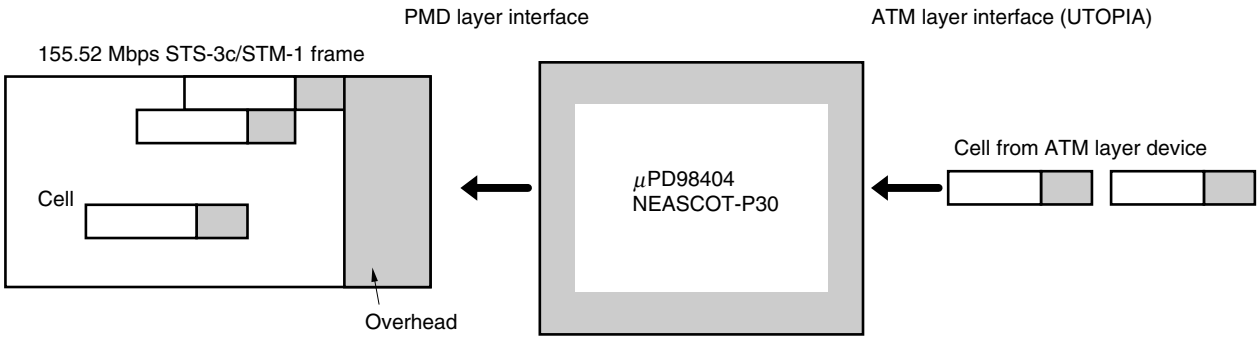
The user can select the serial or parallel interface mode and the use of the transmit clock synthesizer PLL by using the PSEL[1:0] pins.

For the details of the PMD interface, refer to **4.2 PMD Interface**.

## 3.2 Reception Function

The reception function of the μPD98404 extracts an ATM cell from the frame received from the PMD interface, and outputs cell to an ATM layer device by outputting it to the ATM interface.

**Figure 3-6. Outline of μPD98404's Frame Reception Function**




After power application, the μPD98404 immediately starts receiving a frame in the default operation mode.

This section explains the reception function of the μPD98404 mainly based on the flow of processing.

The μPD98404 processes receive data in the following sequence:

**(1) Frame reception**

The μPD98404 receives the data stream of the frame from the PMD interface. In the serial interface mode, the μPD98404 samples the data signal input to the RDIC/RDIT pin with the receive clock generated by the internal clock recovery or the clock synchronized with the data input to the RCIC/RCIT pin.

In the parallel interface mode, the μPD98404 samples the data signals input to the RPD0 through RPD7 pins with the synchronization clock input to the RPC pin. The serial or parallel interface mode and the use of the receive clock recovery PLL is selected by using the PSEL[1:0] pins.

For the details of the PMD interface, refer to **4.2 PMD Interface**.

**(2) Synchronization of receive frame**

The μPD98404 monitors the bit string of the receive data if frame synchronization is not established. If the synchronization pattern of bytes A1 and A2 (6 bytes) is detected in a bit string, the bit string at the position of bytes A1 and A2 of the next frame is checked. If the bit string in bytes A1 and A2 has the same synchronization pattern, the frame synchronization (In frame) status is established.

**Table 3-1. Synchronization Pattern**

| Frame Synchronization Byte | |
|---|---|
| A1 | 11110110 (F6H) |
| A2 | 00101000 (28H) |

Even in the frame synchronization status, the μPD98404 always monitors the A1 and A2 byte positions (6 bytes) of the receive frame. If four or more frames having a pattern different from the patterns of the A1 and A2 bytes are received at the positions of the A1 and A2 bytes in succession, the μPD98404 enters the frame non-synchronization (Out of Frame) status.

If the OOF status continues for 3 ms, the LOF (Loss Of Frame) status takes place. LOF is cleared if frame synchronization status continues for 3 ms.

**(3) Descramble of receive frame**

After synchronization has been established, the received frame is descrambled with the polynomial shown below. The entire range of the frame, except the 9 bytes from the beginning, “A1 (1), A1 (2), A1 (3), A2 (1), A2 (2), A2 (3), C1 (1), C1 (2), C1 (3)” is descrambled.

Polynomial $G(X) = 1 + X^6 + X^7$

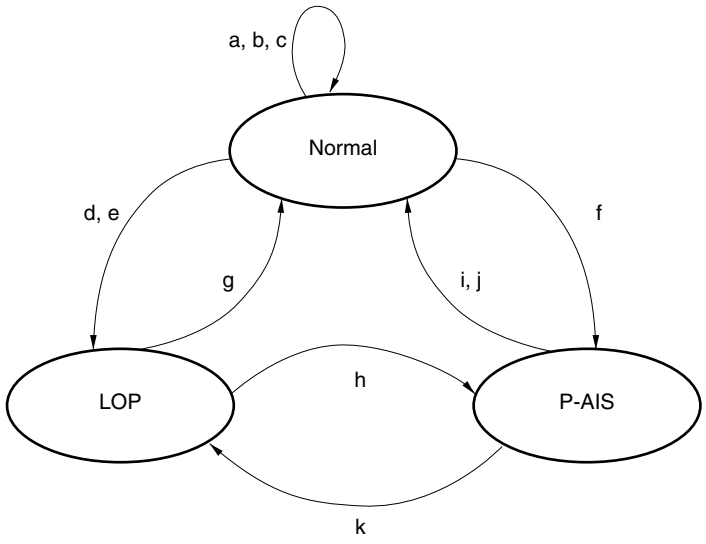
The user can select a descramble stop mode for the purpose of testing. The descramble stop mode is selected by the FSCRM bit of mode register 3 (MDR3).

**(4) Pointer processing**

Frame descramble detects the pointer that indicates the first J1 byte address in the received data string to extract the payload area, and updates the pointer each time a frame has been received.

If the pointer cannot be updated, the LOP (Loss Of Pointer) status occurs. Path AIS is also detected from the H1 and H2 bytes of SOH.

**Figure 3-7. Pointer Status Transition**




Normal status : The received pointer is normal and reception is performed normally.

Path-AIS status : An error occurred in an upstream unit or transmission path, and reception is not performed normally.

LOP status : The received pointer value is abnormal and reception is not performed normally.

| Transition | | Condition |
|---|---|---|
| a | Normal → Normal | NDF Disable + Same valid pointer three times in a row |
| b | | NDF Enable + Valid pointer |
| c | | Positive justification/negative justification |
| d | Normal → LOP | Eight pointers other than valid pointer in a row |
| e | | Eight NDF Enables in a row |
| f | Normal → Path-AIS | H1 and H2 bytes are all “1” three times in a row. |
| g | LOP → Normal | NDF Disable + Same valid pointer three times in a row |
| h | LOP → Path-AIS | H1 and H2 bytes are all “1” three times in a row. |
| i | Path-AIS → Normal | NDF Disable + Same valid pointer three times in a row |
| j | | NDF Enable + Valid pointer |
| k | Path-AIS → LOP | H1 and H2 bytes are not all “1” and eight pointer values in a row that do not satisfy the above conditions i and j. |

**(5) Reception Frequency Justification (stuff operation)**

Frequency Justification (stuff operation) is detected and the following operation is performed if three or more bits of the I/D bits (5 bits) are inverted during pointer processing (refer to **Figure 3-5 Format of AU Pointer** (**H1 through H3 bytes**).

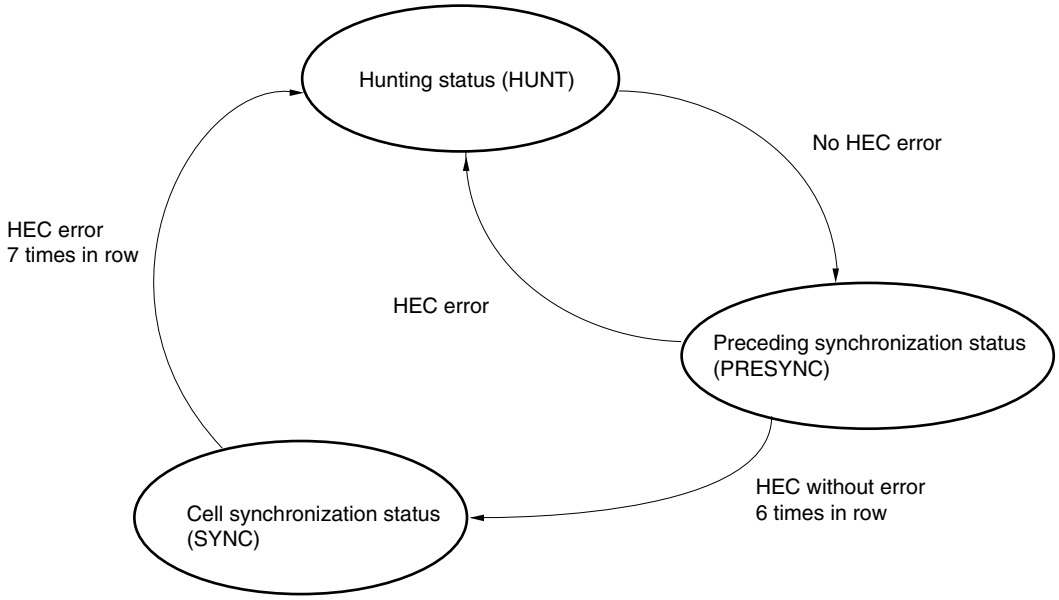
Positive Justification (positive stuff) : The byte at pointer address 0 is not received as payload data if it is detected that three or more bits of I bits are inverted.

Negative Justification (negative stuff) : The H3 byte area is received as payload data if it is detected that three bits or more of the D bits are inverted.

**(6) Cell synchronization**

The boundary of cells is detected to extract an ATM cell from the area excluding the overhead in the frame. The status in which the boundary is correctly detected and the cell can be extracted is called cell synchronization status. The cell boundary is detected by HEC (header error check) processing included in the header of a cell as shown in the status transition in Figure 3-8. The number of protection stages is 7 forward and 6 backward.

**Figure 3-8. Cell Synchronization Status Transition**




- In the hunting status, whether an HEC error has occurred is checked. Once HEC has been satisfied and HEC without an error has been detected, the preceding synchronization status is established.
- In the preceding synchronization status, reception is repeated until HEC without an error is detected six times in a row. If an HEC error is detected, the hunting status is set again.
- In the cell synchronization status, it is judged that cell synchronization is no longer established if a HEC error is detected seven times in a row, and the hunting status is set again.
- Whether cell synchronization is established or not is indicated by the OCD (Out of Cell Delineation) bit of the ACR register.

**Table 3-2. OCD Bit**

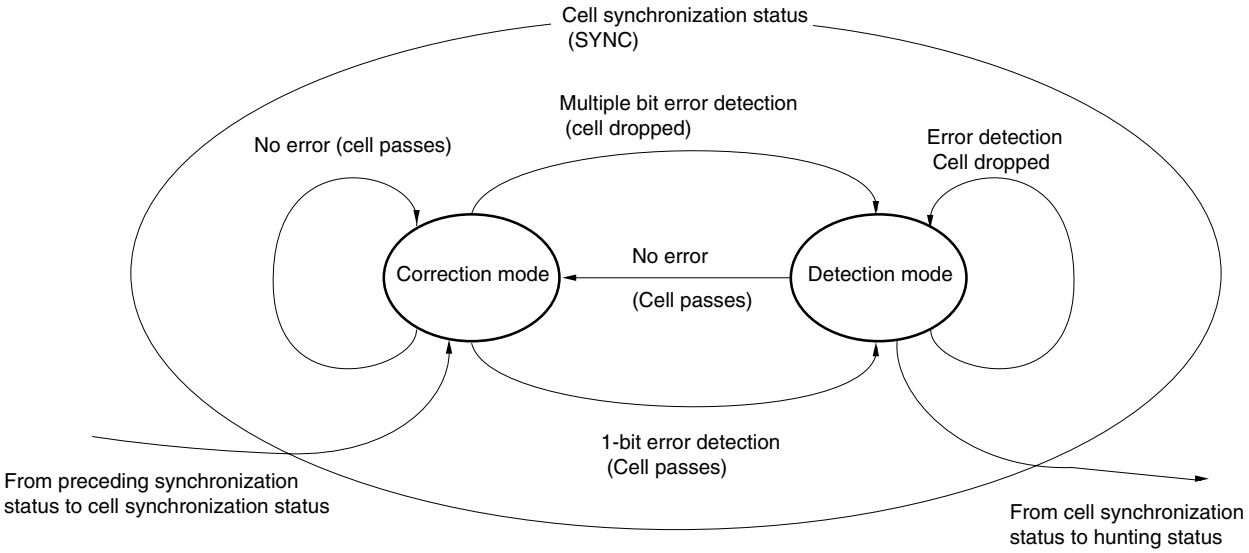
| Status | OCD Bit |
|---|---|
| HUNT/PRESYNC status | 1 |
| SYNC status | 0 |

- If the OCD status lasts for 4 ms, the LCD (Loss of Cell Delineation) status occurs. LCD is cleared if the cell synchronization status lasts for 4 ms.

**(7) HEC error detection/correction**

HEC errors are detected and corrected while cell synchronization is established.

**Figure 3-9. HEC Check Status Transition in Cell Synchronization Status**




- An error of only 1 bit is corrected in the correction mode and then the detection mode is set.
- HEC errors are continuously monitored in the correction mode. If errors are detected seven times, the status is changed from the cell synchronization status to the hunting status.
- Cell header error control differs depending on the setting of the HECENB and CORENB bits of mode register 3 (MDR3).

With the $\mu$PD98404, the HEC check processing in the cell synchronization status can be changed as follows by using the HECENB and CORENB bits of the MDR3 register.

**Table 3-3. HEC Error Correction Mode**

| HECENB | CORENB | Current Mode | Event | Processing | New Mode |
|---|---|---|---|---|---|
| 0 | 0 | Correction mode | No error | — | Correction mode |
| | | | 1-bit error detection | Error correction | Detection mode |
| | | | Multiple bit error detection | Cell dropped | Detection mode |
| | | Detection mode | No error | — | Correction mode |
| | | | 1-bit error detection | Cell dropped | Detection mode |
| | | | Multiple bit error detection | Cell dropped | Detection mode |
| | 1 | Correction mode | No error | — | Correction mode |
| | | | 1-bit error detection | Cell dropped | Detection mode |
| | | | Multiple bit error detection | Cell dropped | Detection mode |
| | | Detection mode | No error | — | Correction mode |
| | | | 1-bit error detection | Cell dropped | Detection mode |
| | | | Multiple bit error detection | Cell dropped | Detection mode |
| 1 | x | Correction mode | No error | — | Correction mode |
| | | | 1-bit error detection | — | Detection mode |
| | | | Multiple bit error detection | — | Detection mode |
| | | Detection mode | No error | — | Correction mode |
| | | | 1-bit error detection | — | Detection mode |
| | | | Multiple bit error detection | — | Detection mode |

**(8) Descramble of ATM cell**

In the cell synchronization status, the data of the ATM cell is descrambled by the following polynomial. The range of descramble is limited to the payload of the ATM cell.

Polynomial G (X) = $X^{43} + 1$

The user can select a descramble stop mode for the purpose of testing. The descramble stop mode is selected by the CSCRM bit of mode register 3 (MDR3).

**(9) Dropping idle cell (vacant cell)**

The $\mu$PD98404 drops an ATM cell whose high-order 4 bytes are “00 00 00 01H” as an idle cell.

**(10) Unassigned cell dropping mode**

After power application, the μPD98404 passes an unassigned cell, as default operation, with the high-order 4 bytes of its ATM header being "00 00 00 00H" to the ATM layer as a valid cell when it has received such a cell. The μPD98404 also has a mode in which this unassigned cell is dropped if received. To use the μPD98404 in the unassigned cell dropping mode, set the CLP bit of both DCHPR and DCHPMR registers.

(a) Functions of DCHPR and DCHPMR registers

The CLP field of a receive cell with VPI/VCI fields all at 0 is compared with the contents of the DCHPR register. If this field coincides with the register contents, the cell is dropped. DCHPMR is a register that masks a bit to be compared. If the CLP bit of this register is set to "1", the field of the receive cell is not compared with the CLP bit of DCHPR.

★ **Table 3-4. Example When CLP Bit Is Used**

| DCHPR | DCHPMR | Cells Dropped |
|---|---|---|
| 01 | 00 | Drops idle cells (default mode) |
| 00 | 00 | Drops unassigned cells |
| 00 | 01 | Drops idle cells and unassigned cells |

**(11) Output of ATM cell from ATM layer interface**

★ The ATM cell is stored to a receive FIFO with a capacity of about 4 cells (256 bytes) to adjust the rate with the ATM layer interface. The ATM cell is always output to an ATM layer device via the ATM layer interface. For the details of the ATM layer interface, refer to **4.1 ATM Layer Interface**.

## 3.3 OAM Information Control Function

The μPD98404 has an OAM (Operation And Maintenance) function to maintain and monitor the network. This section explains the OAM functions supported by the μPD98404.

### 3.3.1 Transmission OAM control

**(1) Transmitting alarm**

Alarm is written to a specific overhead area of the transmit frame and transmitted.

**Table 3-5. Transmitting Alarm**

| Alarm | Transmission Method |
|---|---|
| Line AIS/Path AIS | Transmitted/cleared by command |
| Line RDI<br>Path RDI | · Transmitted/cleared by command<br>· Automatically transmitted by occurrence of internal problem (automatic transmission can be masked) |
| Line REI/Path REI | Automatically generated and transmitted internally |

**(a) Transmitting Line AIS (Line Alarm Indication Signal)**

Line AIS is a line alarm indication signal that detects a failure in the upstream and sends an alarm to the downstream during relaying.

The μPD98404 changes the sixth through eighth bits of the K2 byte of the transmit frame to “111” and sets the bits in all the areas of POH and payload (before scramble) to “1” for transmission if the LAIS bit of command register 1 (CMR1) is set to 1. Whether Line AIS is transmitted or cleared is determined by the user.

Transmission overhead : K2 byte (6th through 8th bits) = 111 and areas of POH and payload = 1
Transmission/clearing condition: Transmission or clearing is controlled by the host by setting the LAIS bit of the command register 1 (CMR1).

**(b) Transmitting Path AIS (Path Alarm Indication Signal)**

Path AIS is a path far-end reception failure information that is reported to the downstream when a failure is detected in the upstream and alarm is issued during relaying.

The μPD98404 changes all the bits of the overhead H1, H2, and H3 bytes of the transmit frame to “1” and all the bits in the SPE area (before scramble) to “1” for transmission if the PAIS bit of command register 1 (CMR1) is set to 1.

Transmission overhead : H1 through H3 bytes = all “1” & SPE bit area = all “1”
Transmission/clearing condition: Transmission/clearing is controlled by the host by setting the PAIS bit of command register 1 (CMR1).

**(c) Transmitting Line RDI (Line Remote Detect Indication)**

Line RDI is a signal that reports detection of a line receive failure (LOS, LOF, or Line AIS) to a unit in the upstream. The μPD98404 sets the sixth through eight bits of overhead K2 byte of the transmit frame to "110" for transmission if the LRDI bit of command register 1 (CMR1) is set to 1. It also automatically transmits these bits when an internal problem (occurrence of LOS, LOF, or Line AIS) is detected. This automatic transmission due to occurrence of an internal problem can be masked by the IACM register.

Transmission overhead : K2 byte (6th through 8th bits) = 110

Transmission/clearing condition:
- Setting by command register
- Automatic transmission/clearing by occurrence of the following internal actions (can be masked by command register)
  - Detection/clearing of LOF
  - Detection/clearing of LOS
  - Detection/clearing of Line AIS

**Caution If the μPD98404 is used in the mode in which the PSEL[1:0] pins = 01 (serial mode in which the externally supplied RCIT/RCIC and TFKT/TFKC clocks are used as transmit/receive clocks), the μPD98404 does not automatically transmit Line-RDI even if LOS, LOF, or Line-AIS is detected at the receiver circuit side, unless the receive clock is input to the RCIT/RCIC pin. This is because the automatic transmitter circuit of Line-RDI needs part of the receive clock. Therefore, be sure to input the receive clock when using the Line-RDI automatic detection function in the mode in which the PSEL[1:0] pins = 01.**

**(d) Transmitting Path RDI (Path Remote Detect Indication)**

Path RDI is a signal that reports detection of a path receive failure (LOS, LOF, Line AIS, LOP, LCD, or Path AIS) to a unit in the upstream. The μPD98404 sets the fifth bit of the overhead G1 byte of the transmit frame to "1" for transmission if the PRDI bit of the command register 1 (CMR1) is set to 1. It also automatically transmits this bit if an internal problem (occurrence of LOS, LOF, Line AIS, LOP, LCD, or Path AIS) is detected. This automatic transmission due to occurrence of an internal problem can be masked by the IACM register.

Transmission overhead : G1 byte (5th bit) = 1

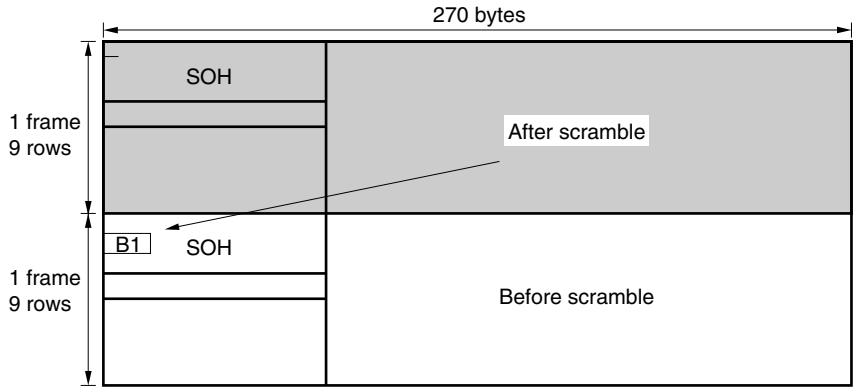
Transmission/clearing condition:
- Setting by command register
- Automatic transmission/clearing by occurrence of the following internal actions (can be masked)
  - Detection/clearing of LOF
  - Detection/clearing of LOS
  - Detection/clearing of LOP
  - Detection/clearing of LCD
  - Detection/clearing of Line AIS
  - Detection/clearing of Path AIS

**(2) Functions related to monitoring circuit quality on transmission side**

**(a) Bit Interleaved Parity (BIP)**

B1 byte (Section BIP-8):

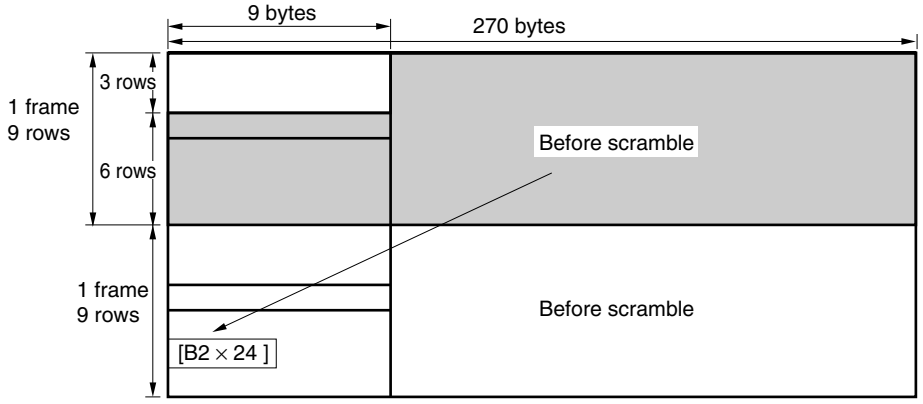
BIP-8 operation is performed on all the frame data (data after scramble) except the first line of SOH (Section Overhead) of the transmit frame, BIP-8 operation is performed on a specific area, and the result of the operation is inserted in the B1 byte of the transmit frame and transmitted.




: BIP operation range B1: BIP-8 operation result of preceding frame

B2 byte (Line BIP-24):

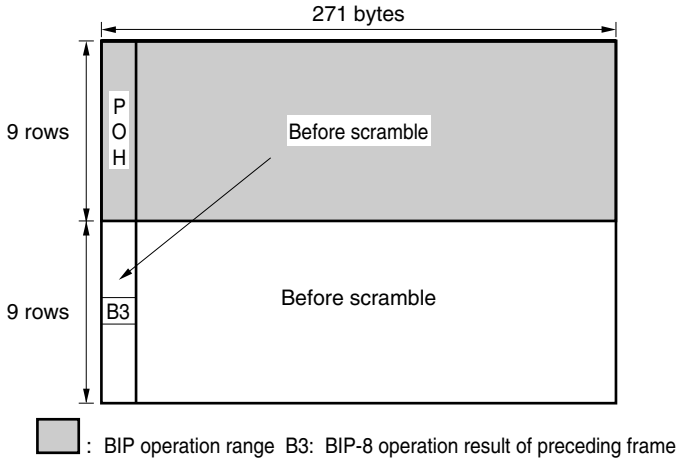
BIP-24 operation is performed on all frame data (data before scramble) except the first, second, and third lines of SOH one frame before, and the result of the operation is inserted to the B2 byte of the next transmit frame and transmitted.




: BIP operation range B2 × 24: BIP operation result of preceding frame

B3 byte (Path BIP-8):

BIP-8 operation is performed on all the payload data (data before scramble), and the result of the operation is inserted to the B3 byte of POH (Path Overhead) of the next transmit frame and transmitted.




**(b) Detecting Line REI (Line Remote Error Indication)**

Whether Line BIP-24 error has occurred is reported to a unit in the upstream.

When the $\mu$PD98404 detects a B2 error in the receive frame, it automatically stores the number of errors in the M1 byte (fourth through eighth bits) of the transmit frame and transmits the byte.

**(c) Transmitting Path REI (Path Remote Error Indication)**

Whether Path BIP-8 error occurs is reported to a unit in the upstream.

When the $\mu$PD98404 detects a B3 error in the receive frame, it automatically stores the number of errors to the G1 byte (first through fourth bits) of the transmit frame and transmits the byte.

### 3.3.2 Reception OAM Control

**(1) Detection of alarm and failure**

The μPD98404 sets the corresponding bit of the internal interrupt cause register if any of the following alarms or failures is detected, to report the occurrence of the alarm or failure to cause the host via an interrupt signal. The host can identify the alarm or failure that has occurred by reading the corresponding interrupt cause register. Each interrupt cause can be masked or unmasked. Detection of an alarm or failure can be reported cause using three PHYALM (2 through 0) output pins. Which alarm or failure is output to each PHYALM pin is specified by the AMPR, AMP1, and AMR2 registers.

**Table 3-6. Alarm and Failure List (1/2)**

| |
|---|
| PMD (PMD Layer Device) Alarm |
| Indicates that PMDALM pin goes high.<br>Detection : Detects high level of the PMDALM pin<br>Clear : Detects that PMDALM pin goes back low |
| LOS (Loss Of Signal) |
| Receive signal lost status<br>Detection : If a pattern of all 0s or all 1s is received for about 80 μs continuously or if the PMDALM pin goes high when the PMD bit of the IACM register = 0<br>Clear : If LOS condition is not detected for 125 μs or if the PMDALM pin goes low when the PMD bit of the IACM register = 0 |
| OOF (Out Of Frame) |
| Frame non-synchronization<br>Detection : If frame synchronization pattern (A1, A2) error of receive data is detected in four successive frames<br>Clear : If frame synchronization pattern is detected in two successive frames |
| LOF (Loss Of Frame) |
| Loss of Frame<br>Detection : If OOF status lasts for 3 ms<br>Clear : If not OOF status lasts for 3 ms |
| LOP (Loss Of Pointer) |
| Pointer error detection<br>Detection : Refer to **3.2 (4) Pointer processing**.<br>Clear : Refer to **3.2 (4) Pointer processing**.<br>If OOF is detected, LOP status is forcibly set. |
| OCD (Out of Cell Delineation) |
| Cell non-synchronization<br>Detection : If cells having header in which error is detected as result of HEC check are received seven times continuously. OCD status is forcibly set if OOF, LOP, or PATH-AIS is detected.<br>Clear : If cells having valid header are detected seven times continuously |
| LCD (Loss of Cell Delineation) |
| Cell non-synchronization detection<br>Detection : If OCD status lasts for 4 ms<br>Clear : If cell synchronization status lasts for 4 ms |
| Line AIS (Line Alarm Indication Signal) |
| Line alarm indication signal. Detects occurrence of Line AIS in unit of transmission source (upstream).<br>Detection : If frames with overhead K2 byte (6th through 8th bits) being “111” are received five times continuously<br>Clear : If frames with overhead K2 byte (6th through 8th bits) not being “111” are received five times continuously |

**Table 3-6. Alarm and Failure List (2/2)**

| |
|---|
| Path AIS (Path Alarm Indication Signal) |
| Path alarm indication signal. Detects occurrence of Path AIS in unit of transmission source (upstream).<br>Detection : Refer to **3.2 (4) Pointer processing**.<br>Clear : Refer to **3.2 (4) Pointer processing**. |
| Line RDI (Line Remote Defect Indication) |
| Line remote reception failure information. Indicates detection of line reception failure (LOS, LOF, or Line AIS) in unit of transmission destination (downstream).<br>Detection : If frames with overhead K2 byte (6th through 8th bits) being “110” are received five times continuously<br>Clear : If frames with overhead K2 byte (6th through 8th bits) being other than “110” are received five times continuously |
| Path RDI (Path Remote Defect Indication) |
| Path remote reception failure information. Indicates detection of path reception failure (LOS, LOF, Line AIS, LOP, LCD, or Path AIS) in unit of transmission destination (downstream).<br>Detection : If frames with 5th bit of overhead G1 byte being “1” are received five times continuously<br>Clear : If frames with 5th bit of overhead G1 byte being “0” are received five times continuously |
| OOL (Out Of Link) |
| Indicates whether the receive clock recovery PLL has correctly locked on to the receive data stream, and whether it is the expected clock signal.<br>Detection : When the difference between the clock signal input to the REFCLK pin and the clock signal generated by the recovery PLL divided by eight is greater than 244 ppm.<br>Clear : When the difference between the clock signal input to the REFCLK pin and the clock signal generated by the recovery PLL divided by eight is within 244 ppm. |

**(2) Reporting degradation of reception side circuit quality (performance monitor)**

The μPD98404 sets the corresponding bit of the internal interrupt cause register and reports to the host using an interrupt signal if it detects degradation of the circuit quality. The host can identify the cause of degradation of the circuit quality by reading the interrupt cause register. Each interrupts cause can be masked or unmasked.

**Table 3-7. Performance Cause Register (PCR register)**

| |
|---|
| B1 error detection |
| Detects section layer BIP-8 error in receive data. BIP-8 operation is performed on all frame data (data after scramble) except first line of SOH one frame before, result of this operation is verified against result of Section BIP-8 operation performed at transmission source (upstream) and stored to B1 byte of current frame, and B1 error is checked. |
| B2 error detection |
| Detects line layer BIP-24 error in receive data. BIP-24 operation is performed on all frame data (data before scramble) except first, second, and third lines of SOH one frame before, result of this operation is verified against result of Line BIP-24 operation performed at transmission source (upstream) and stored to B2 byte of current fame, and B2 error is checked. |
| B3 error detection |
| Detects path layer BIP-8 error in receive data. BIP-8 operation is performed on all payload data (data before scramble) one frame before, result of this operation is verified against result of Path BIP-8 operation performed at transmission source (upstream) and stored to B3 byte of current frame, and B3 error is checked. |
| Line REI detection (Line Remote Error Indication) |
| Line far end block error information. Detects Line BIP-24 errors in unit at transmission destination (downstream).<br>Detection : Line REI is detected if 4th through 8th bits of receive M1 byte are 01 to 18 (H)<br>Clear : Line REI is cleared if 4th through 8th bits of receive M1 byte are 00 (H) |
| Path REI detection (Path Remote Error Indication) |
| Path far end block error information. Detects Path BIP-8 errors in unit at transmission destination (downstream).<br>Detection : Path REI is detected if 1st through 4th bits of receive G1 byte are 1 to 8 (H)<br>Clear : Path REI is cleared if 1st through 4th bits of receive G1 byte are 0 (H) |
| Occurrence of Frequency Justification |
| Detects occurrence of Frequency Justification |

**(3) Monitoring circuit quality using count register**

The μPD98404 counts the number of faults that degrade the circuit quality, the number of times receive Frequency Justification has occurred, and the number of cells dropped due to occurrence of an HEC error with counters, in order to monitor the circuit quality. The host can obtain the value of these counters by reading the registers.

**Table 3-8. Counters**

| Counter Name | Count Contents | Number of Counter Bits |
|---|---|---|
| B1 error counter | Number of times B1 error has been detected | 16 |
| B2 error counter | Number of times B2 error has been detected | 20 |
| B3 error counter | Number of times B3 error has been detected | 16 |
| Line-REI counter | Total number of errors received by Line REI | 20 |
| Path-REI counter | Total number of errors received by Path REI | 16 |
| FJ counter | Number of Frequency Justification operations | 12 |
| HEC counter | Total number of cells dropped by HEC processing | 20 |
| FIFO full counter | Total number of cells dropped due to FIFO overflow | 20 |
| Idle cell counter | Total number of received idle cells (cells dropped by setting of DCHPR and DCHPMR registers) | 20 |
| Information cell counter | Total number of valid cells transferred to ATM layer device (including cell with HEC error corrected) | 20 |

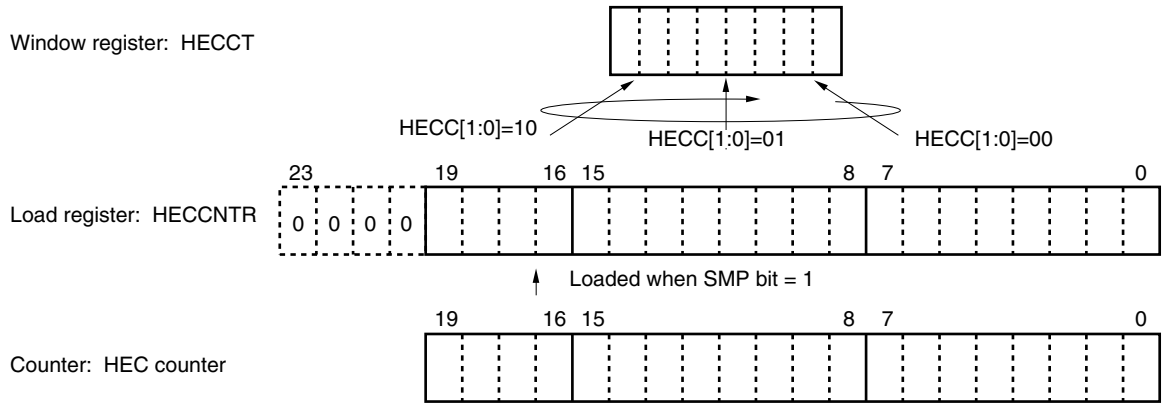
The counter functions are implemented by the following registers. These registers are provided to each of the above counters.

Counter : Counter that counts the internal events. When the count value reaches “F(H)”, the corresponding bits of the PCOCR1 and PCOCR2 registers are set, and detection of an overflow is reported. The count value of the counter returns to 0 and the counter continues counting up.

Load registers : If the SMP bit of the PCSR register is set to “1” by the host, the current count values of all the counters are stored to the corresponding load registers. The contents of this register are retained until the SMP bit is set to 1 next time.

Window register: This is an 8-bit register used by the host to read the contents of the load registers. To obtain a load register value 12 or 16 bits wide, the value of the load register is output in 8-bit units, in the order of the low-order 8 bits, high-order 8-bits, the low-order 8-bits, high-order 8-bits, and so on, each time the host reads the window register. Therefore, the host reads the window register two times. Which of the low-order or high-order 8 bits are output when the host reads the wind register next time is indicated by the corresponding bits of the PCPR1 and PCPR2 registers. To read a load register 20 bits wide, the host reads the window register three times to read the low-order, middle-order, and high-order bits in that order.

**Figure 3-10. Counter-Related Registers (Example: HEC error counter)**




The following counter-related functions are also available.

**<1> Clearing all counters [PCR bit of CMR2 register (01H) = 1]**

All the counters can be cleared to 0 by setting the PCR bit of the command register 2 (CMR2) to "1". The PCR bit is automatically returned to 0 after the counters have been cleared.

**<2> Clearing in counter units [PCIR1 register (1CH), PCIR2 register (1DH)]**

Only a counter that has been set can be cleared to 0 by setting the corresponding bit in the PICR1 and PICR2 registers to "1". The set bit is automatically returned to 0 after the counter has been cleared to 0.

**<3> Loading all counters [PCSR register (1BH)]**

All the counter values are stored in the corresponding load register by setting the SMP bit of the PCSR register to "1". The SMP bit is automatically returned to 0 after the operation has been completed. At this time, the values in all counters are cleared.

**<4> Stopping unused counters [PCFR1 register (1EH), PCFR2 register (1FH)]**

To reduce the power consumption, the counters not in use are stopped. When the bit of the PCFR1 and PCFR2 registers corresponding to the unused counter is set to 1, the counter is stopped. When the corresponding bit of the RCFR1 or RCFR2 register is set to 1, the counter stops functioning. All the counters are stopped by default. Once a counter has been started and then stopped, the counter holds the current value.

**<5> Reporting occurrence of overflow in each counter [PCOCR1 register (20H), PCOCR2 register (21H)]**

When all the count values have passed "F", the $\mu$PD98404 reports detection of an overflow by setting the corresponding bit of the PCOCR1 and PCOCR2 registers and asserting interrupt signal PHINT_B active. The interrupt can be masked for each bit.

**<<Counter stopping conditions>>**

| Counter | Stopping Condition |
|---|---|
| B1, B2, B3, Line REI, Path REI, and FJ counters | Counting up of these counters is forcibly stopped while the LOS, LOF, LOP, Line AIS, or Path AIS error is detected. |
| HEC, FIFO full, idle cell, and information cell counters | Counting up of these counters is forcibly stopped while the LOS, LOF, LOP, Line AIS, Path AIS, or LCD error is detected. |

**Caution The counter functions are constrained. For details, refer to CHAPTER 8 CONSTRAINTS.**

## 3.4 Frame Overhead Insert/Drop Function

The μPD98404 has an insert/drop register in the byte area of the following frame overhead and can transmit any value to the transmit frame or read a value stored to the receive frame.

**Figure 3-11. Overhead Byte with Insert/Drop Register**

| | | Transmission Default value |
|---|---|---|
| SOH Section Overhead | J0 byte | 01 (H) |
| | 1st Z0 byte | 02 (H) |
| | 2nd Z0 byte | 03 (H) |
| | F1 byte | 00 (H) |
| LOH Line Overhead | K1 byte | 00 (H) |
| | K2 byte | 00 (H) |
| POH Path Overhead | F2 byte | 00 (H) |
| | C2 byte | 13 (H) |
| | H4 byte | 00 (H) |

- **Insert register**

  The host stores and transmits the value it has written to the insert register in the corresponding overhead byte area of the transmit frame for transmission. Unless the host change the value, the default value of the insert register is transmitted.

  Because bits 6 through 8 of the K2 byte are used to transfer Line-RDI, the value of the insert register is ignored.

- **Drop register**

  The contents of the overhead of a receive frame are stored in the corresponding drop register, and are updated each time a frame has been received. The host can learn the value of the overhead byte of the receive frame by reading each drop register.

  In the LOP or P-AIS status, the register of POH is not updated. If frame non-synchronization (OOF) takes place, all the registers are not updated.

## 3.5 Alarm Report Pins (PHYALM[2:0], PMDALM)

The μPD98404 has output pins PHYALM [2:0] that output signals reporting that the host has detected an alarm or error to the peripheral device. The user can select one or more alarms or errors to be output to one PHYALM pin from those listed in Table 3-9. This selection is done by using three registers: AMPR, AMR1, and AMR2.

First, specify which of the PHYALM0 through PHYALM2 pins is to be set, using the AMPR register. Next, specify masking or unmasking of the bit corresponding to each type of alarm and error using the AMR1 and AMR2 registers. Repeat these operations three times to set the three pins: PHYALM0 through PHYALM2.

**Table 3-9. PHYALM Pin Report Contents**

| Reported Item | PHYALM Output Timing |
|---|---|
| Bit setting of the register is reflected. | PHYALM pin goes high when the host writes 1 to the ARM bit of the command register 1 (CMR1). |
| Input level of the PMDALM pin is reflected as is. | The PHYALM pin goes high when it has been detected that the external PMDALM input pin has gone high. |
| Detection of alarms or errors is reported. (LOS, OOF, LOF, LOP, OCD, LCD, Line AIS, Path AIS, Line RDI, Path RDI) | The PHYALM pin goes high when an alarm or error has been detected and is kept high until the cause of the alarm or error is removed. |

**<<Example of using PHYALM pins>>**

**Example 1**: To output a high level from the PHYALM1 pin when the μPD98404 has detected LOS or LOF

<1> Write '01H' to the AMPR register (24H): Selects the PHYALM1 pin.
<2> Write 'DEH' to the AMR1 register (25H): Unmasks LOS and LOF.
<3> Write 'FFH' to the AMR2 register (26H): Default (no unmasking)

If two or more sources are unmasked, they are ORed for output.

**Example 2**: To output a high level from the PHYALM0 pin when the software has set the ARM bit of the CMR1 register to 1.

<1> Write '00H' to the AMPR register (24H): Selects the PHYALM0 pin.
<2> Write '7FH' to the AMR1 register (25H): Unmasks the CMD bit.
<3> Write 'FFH' to the AMR2 register (26H): Default (no unmasking)

The μPD98404 also has external input port PMDALM pin. The function of this pin differs depending on the setting of the PMD bit of the IACM register. Table 3-10 shows the functions of the PMD bit and PMDALM pin.

**Table 3-10. PMDALM Pin Function**

| PMD Bit: IACM Register | Function of PMDALM Pin |
|---|---|
| 1<br>(Default) | The input level of this pin is reflected by the PMD bit of the PICR register and is used as a general-purpose input port. It is not included in the LOS detection condition. |
| 0 | The input level of this pin is reflected by the PMD bit of the PICR register and can be also used as an interrupt cause.<br>A change in this input level is also included in the LOS detection condition. When the input level is high, LOS is detected. A LOS output by an optical module is connected to this input.<br>★ Low: normal<br>High: LOS is detected |

## 3.6 Pseudo Error Frame Transmission Function

The μPD98404 has a function to generate internally and transmit a pseudo error frame as shown in Table 3-11. This function is effective for testing the system and can be executed by setting command register 3 (CMR3).

**Table 3-11. Pseudo Error Frame**

| Error | Generation of Pseudo Error |
|---|---|
| LOS frame generation | Fixes transmit data to 00H |
| OOF/LOF frame generation | Fixes A1 and A2 bytes to 00H |
| LOP frame generation | Fixes H1, H2, and H3 bytes to FFH, FEH, and FFH |
| OCD, LCD frame generation | Inverts LSB bit of HEC field |
| Generation of B1 error | Inverts and transmits LSB bit of B1 byte |
| Generation of B2 error | Inverts and transmits LSB bit of B2 byte |
| Generation of B3 error | Inverts and transmits LSB bit of B3 byte |
| Generation of Line REI | Inverts and transmits LSB bit of M1 byte (4th through 8th bits) |
| Generation of Path REI | Inverts and transmits LSB bit of G1 byte (1st through 4th bits) |

## 3.7 Register Function

The μPD98404 has many registers that can be accessed by the host via management interface. The host sets the operation mode of the μPD98404, transmits alarm signals, and services interrupts by accessing these registers. The registers of the μPD98404 can be broadly divided as follows by classification of function.

**Table 3-12. Registers of μPD98404**

| Classification | Functional Outline | Register Name |
|---|---|---|
| Command-related | Set commands such as those transmitting error frame | CMR1, CMR2, CMR3 |
| Mode setting-related | Select mode | MDR1, MDR2, MDR3 |
| Interrupt-related | Status registers indicating interrupt causes and mask registers masking each interrupt | PICR, PIMR, ACR, ACMR, PCR, PCMR, IACMR |
| Counter-related | Store values of performance counters | B1ECT, B2ECT, B3ECT, LRECT, PRECT, FJCT, HECCT, FULCT, IDLCT, INFCT, PCPR1, PCPR2, PCSR, PCIR1, PCIR2, PCFR1, PCFR2, PCOCR1, PCOCR2, PCOMR1, PCOMR2 |
| PHYALM pin output signal setting | Select information to be output to PHYALM pins | AMPR, AMR1, AMR2 |
| Drop cell | Determine cells other than idle cell to be dropped | DCHPR, DCHPMR |
| PHY ID | Used in multi-PHY mode. Sets address of this LSI | PHYIDR |
| Insert/drop | Insert registers that insert value to overhead of transmit frame and drop registers that store value from overhead of transmit frame | J0R, Z01R, Z02R, F1R, K1R, K2R, C2R, F2R, H4R, J0T, Z01T, Z02T, F1T, K1T, K2T, F2T, C2T, F2T, H4T |

For the details of each register, refer to **CHAPTER 5 REGISTERS**.

## 3.8 Loopback Function

The μPD98404 has loopback modes in which transmit/receive data is internally returned for the purpose of testing. The following three loopback modes are available. These modes are set by the LP (1, 0) bits of mode register 2 (MDR2).

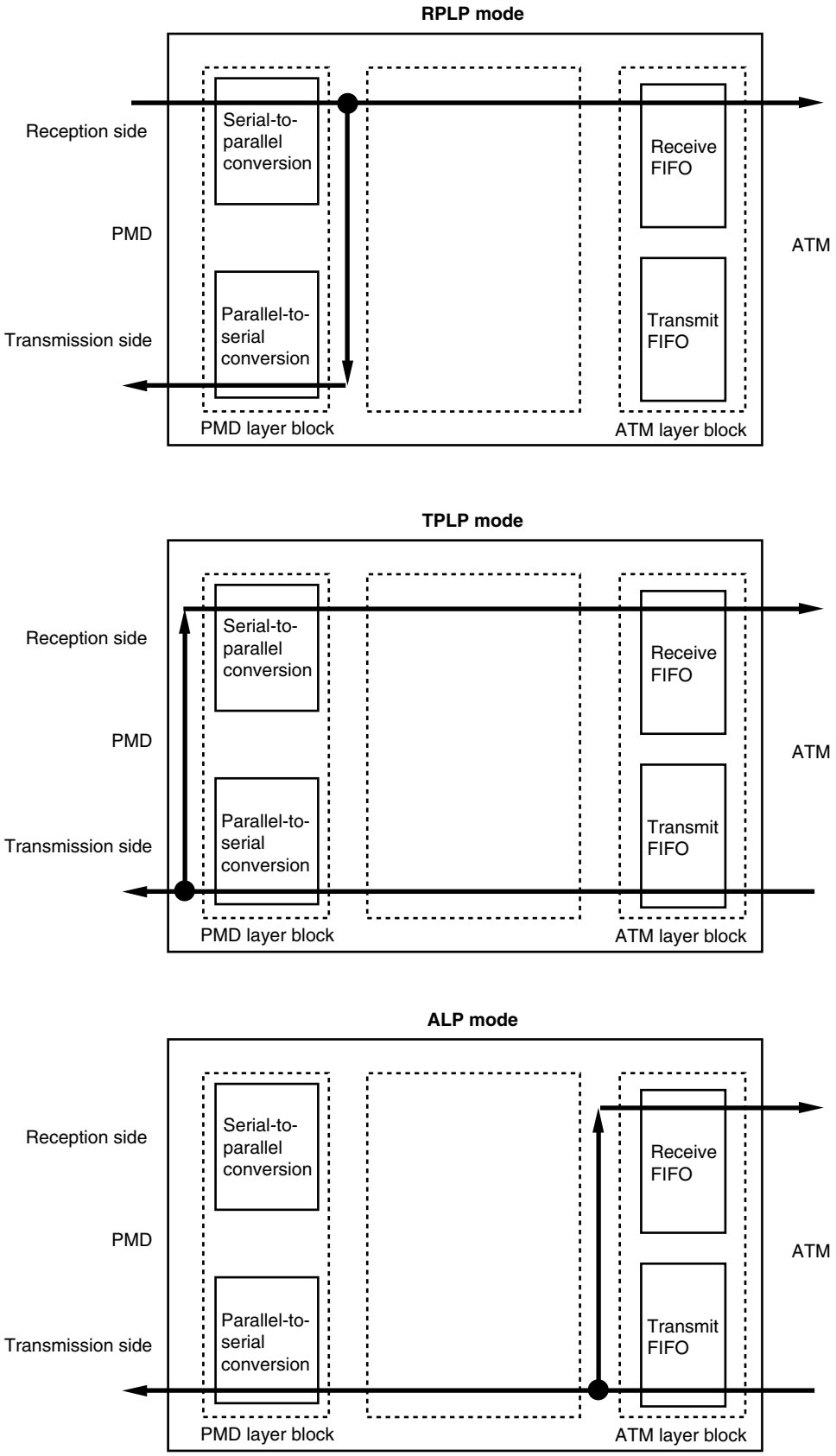
**Table 3-13. Loopback Function**

| LP[1:0] | Mode |
|---|---|
| 00 | Normal mode |
| 01 | PMD layer loopback <1> : RPLP mode<br>Returns data input from reception side of PMD layer interface with serial/parallel converter and outputs data from transmission side of PMD layer interface. At this time, however, the clock is not returned. The clock output from TCOT/TCOC pin is the transmit PLL generation clock or the transmit clock input from TFKT/TFKC pin. Received data is also output from ATM layer interface. In the RPLP mode, the register that indicates the circuit status, such as the PICR register, indicates the input status of the receiver circuit. |
| 10 | PMD layer loopback <2> : TPLP mode<br>Proceeds internal processing on transmit cell data received from ATM layer interface up to PMD side, returns data at PMD layer side and outputs it from reception side of ATM layer. At this time, received cell is also output from transmission side of PMD layer interface. In the TPLP mode, the register that indicates the circuit status, such as the PICR register, indicates the status of the transmit data that has been looped back. |
| 11 | ATM layer loopback : ALP mode<br>Returns transmit ATM cell received from ATM layer interface as return receive ATM cell by using internal FIFO of μPD98404. At this time, received data is also output from PMD layer interface as transmit data. In the ALP mode, the register that indicates the circuit status, such as the PICR register, becomes undefined and does not indicate the status of the receiver circuit. |

**Cautions 1. In the RPLP loop back mode (LP[1:0] = 01), the data output from the TDOT/TDOC pin is latched and output at the clock of the receive clock recovery PLL. In the meantime, the TCOT/TCOC pin outputs the clock of the internal synthesizer or the clock input to the TFKT/TFKC pin, regardless of the above mode, in accordance with the setting of the PSEL[1:0] pins. Note that the TCOT/TCOC pin does not loop back and output the receive clock and that the data output by TDOT/TDOC and the clock output by TCOT/TCOC are not in synchronization.**

★ **2. Loopback cannot be executed even if the TPLP mode or ALP mode is set if a mode that uses the external clock (PSEL[1:0] = 01) is selected and if the transmit clock is not input to the TFKT/TFKC pin.**

**Figure 3-12. Loopback Function**



# CHAPTER 4 INTERFACES

## 4.1 ATM Layer Interface

The ATM layer interface transfers transmit/receive data to a device of the high-order ATM layer. The interface between the μPD98404 and ATM layer conforms to UTOPIA Level2 version 1.0 June '95 Standard.

### 4.1.1 Signals

**(1) Transmission interface**

TCLK : A clock of 20 to 40 MHz supplied from the ATM layer. All the operations of the transmission interface related to data transfer are executed in synchronization with this clock.

TADD[4:0] : 5-bit address signal used by the ATM layer to select one μPD98404 in multi-PHY configuration where two or more μPD98404s are connected to one ATM layer device.

TDI[7:0] : Data signals used by the ATM layer to drive transmit cell data to the μPD98404. TDI7 is the MSB and TDI0 is the LSB.

TSOC : Signal indicating the start position of cell data. This signal is output by the ATM layer in synchronization with the first byte of a cell.

TENBL_B : Signal indicating that the ATM layer is outputting valid data onto TDI[7:0] in the current clock cycle.

FULL_B/TCLAV : Signal used by the μPD98404 to report the status of the transmit FIFO to the ATM layer. Which of FULL_B and TCLAV is used depends on the mode. FULL_B is used for octet level handshake of a single PHY, and becomes active (low level) if a vacant area of 4 bytes or more is not available in the transmit FIFO. This signal functions as TCLAV in the case of cell handshake and becomes active (high level) if a cell has a vacant area of one cell or more. The size of the vacant cell area to be reported can be selected from 1 cell or 2 cells.

In the multi-PHY configuration, this signal is used as TCLAV and operates in the same manner as in the case of cell handshake. However, only the μPD98404 with the address set to the PHYID register coinciding with the address given by the ATM layer onto TADD[4:0] drives TCLAV at the clock next to the output address.

**(2) Reception interface**

The signal lines used for the reception interface are defined below.

RCLK : A clock of up to 40 MHz supplied from the ATM layer. All the operations of the reception interface related to data transfer are executed in synchronization with this clock.

RADD[4:0] : These signals are not used in the single PHY configuration. In the multi-PHY configuration, these signals are used as a 5-bit address signal used by the ATM layer to select one μPD98404. The address is set to the PHYID register of the μPD98404. The same address is used for transmission and reception. The address must not be set to 31 (1FH).

RDO[7:0] : These are data signals used by the μPD98404 to transfer receive data to the ATM layer. RDO7 is the MSB, and RDO0 is the LSB. Two-state or three-state operation is selectable.

RSOC : This signal indicates the start position of cell data, and is output by the μPD98404 in synchronization with the first byte of a cell. A two-state or three-state operation is selected depending on the mode.

RENBL_B : This signal is used by the ATM layer to enable data output by the μPD98404.

EMPTY_B/RCLAV : This signal is used by the μPD98404 to report the status of the receive FIFO to the ATM layer. In the octet level handshake mode of single PHY configuration, this signal functions as EMPTY_B and becomes active (low level) if no valid data exists in the receive FIFO. In the cell level handshake mode, this signal functions as RCLAV, and becomes active (high level) if one cell or more of valid data exists in the receive FIFO. The timing to change RCLAV can be changed to report whether valid cell to be transferred next exists during cell transfer.

In the multi-PHY configuration, this signal functions as RCLAV in the same manner as in the cell level handshake mode. However, only the μPD98404 selected by the address on the RADD[4:0] signals is driven by the clock next to the output address.

### 4.1.2 Mode

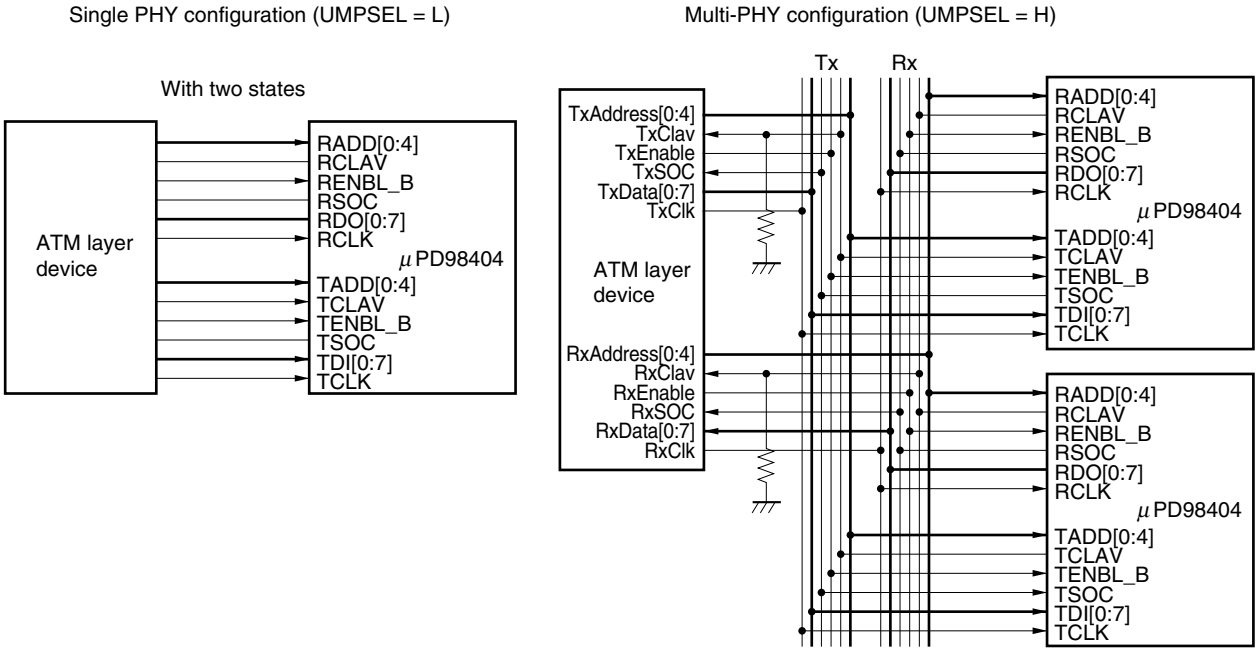
The μPD98404 supports the modes listed in Table 4-1.

**Table 4-1. Mode of ATM Layer Interface**

| Mode | Mode Name | Operation at Reception Side | MDR1 Register | | UMPSEL Pin Input |
|---|---|---|---|---|---|
| | | | CSEL | HSEL | |
| 1 | Single PHY octet level handshake | RDO[7:0]&RSOC 2-state operation | 0 | 0 | L |
| 2 | | RDO[7:0]&RSOC 3-state operation | 0 | 1 | |
| 3 | Single PHY cell level handshake | RDO[7:0]&RSOC 2-state operation | 1 | 0 | |
| 4 | | RDO[7:0]&RSOC 3-state operation | 1 | 1 | |
| 5 | Multi-PHY | RDO[7:0]&RSOC&RCLAV 3-state | x | x | H |

"Single PHY" is a mode in which an ATM layer device and a μPD98404 are connected on a one-to-one basis. "Multi-PHY" is a mode in which two or more μPD98404s are connected to one ATM layer device and one of the μPD98404s is selected by using a 5-bit address line. The single PHY or multi-PHY mode is selected by using the UMPSEL pin. When a high level is input to this pin, the multi-PHY mode is selected regardless of the setting of the MDR1 register.

**Figure 4-1. Single PHY and Multi-PHY Modes**



### 4.1.3 Single PHY octet level handshake mode

Octet level handshake is a mode in which the transfer of transmit/receive cell data with the ATM layer device is controlled in 1-byte units. The FULL_B/TCLAV and EMPTY_B/RCLAV signals that report the status of the transmit/receive FIFO function as FULL_B and EMPTY_B, respectively, and report the status of the FIFO to the ATM layer device in 1-byte units.

**(1) Transmit interface**

The μPD98404 has a transmit FIFO in the ATM layer interface block at the transmitter side. This FIFO can store 384 bytes (about 7 cells). Write cell data on TDI[7:0] to this FIFO in the following procedure:

In the clock cycle in which TENBL_B is active (low level), the μPD98404 recognizes the data on TDI[7:0] as valid. If TENBL_B has gone low after reset, the μPD98404 first checks TSOC. If it has detected that TSOC is high, the μPD98404 writes the TDI[7:0] data in that clock cycle to the transmit FIFO as the first byte of a cell. Starting from this byte, the μPD98404 writes the data of up to 53rd byte as one cell of data. After it has written the 53 bytes, the μPD98404 checks TSOC again and waits for the first byte of a cell. After the μPD98404 has written 53 bytes, it ignores the data of the 54th byte and those that follow and writes nothing to the transmit FIFO until TSOC goes high the next time, even if a low level is kept input to TEBL_B to indicate that the data on TDI[7:0] is valid.

If a high level is input to TSOC after writing data has been started from the first byte and before the 53rd byte is written, the data so far written to the transmit FIFO is discarded as a short cell that runs short of 53 bytes and is not output to the circuit side. In this case, counting data is started again starting from the cycle in which TSOC is high.

If the vacant area of the transmit FIFO is 4 bytes or less, the μPD98404 asserts the FULL_B signal active (low level). The ATM layer device must stop transmitting valid data by deasserting TENBL_B inactive (high level) within 4 clock cycles after the device has detected that FULL_B went low. If FULL_B has been asserted active, it is deasserted inactive when the transmit FIFO has a vacancy of 8 bytes or more.

The high-end ATM layer device can stop outputting data while it is transferring cell data, by deasserting TENBL_B (high level). In the cycle in which TENBL_B is high, the μPD98404 ignores the data on TDI[7:0] as invalid, and does not count these data into 53 bytes. The μPD98404 resumes counting after TENBL_B has gone low.

**Figure 4-2. Transmission Timing of Octet Level Handshake (1)**

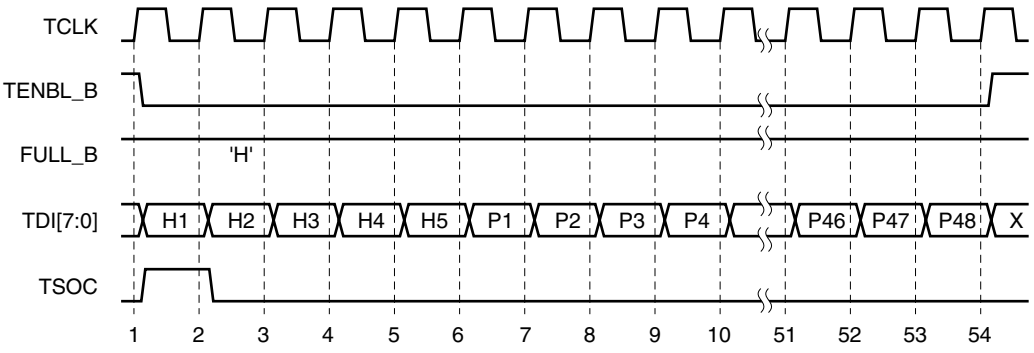
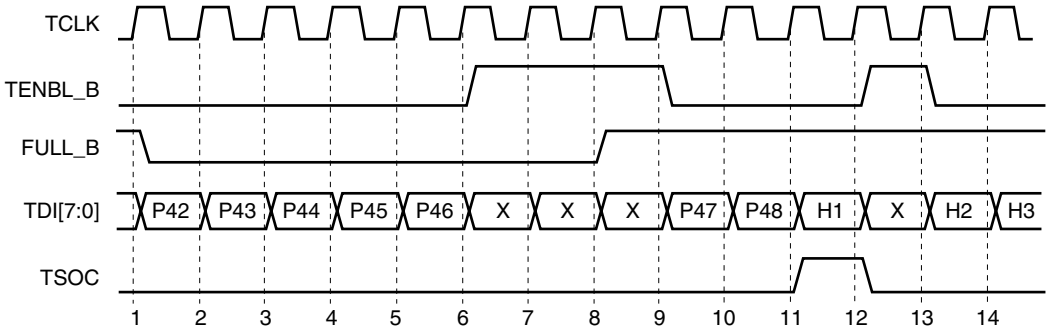


**Figure 4-3. Transmission Timing of Octet Level Handshake (2)**




**(2) Reception interface**

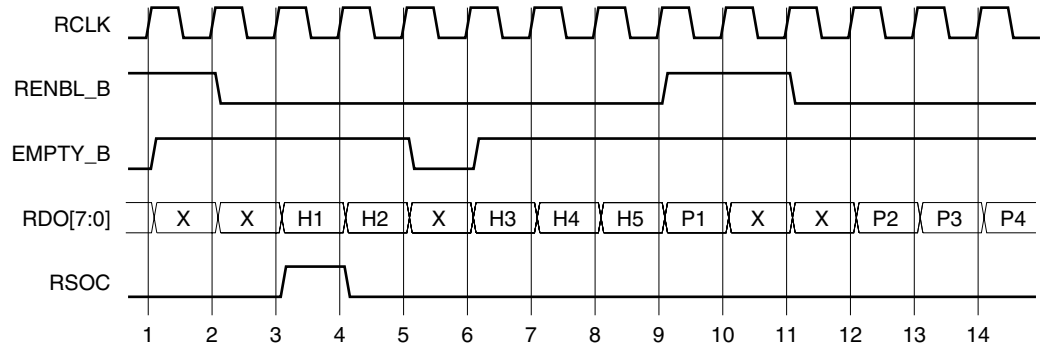
The reception interface in the single PHY octet level handshake mode changes the operation of the RDO[7:0] and RSOC signals between the two-state and three-state operation, depending on whether mode 1 or 2 is selected by the HSEL bit of the MDR1 register.

**(a) Two-state reception interface in single PHY octet level mode**

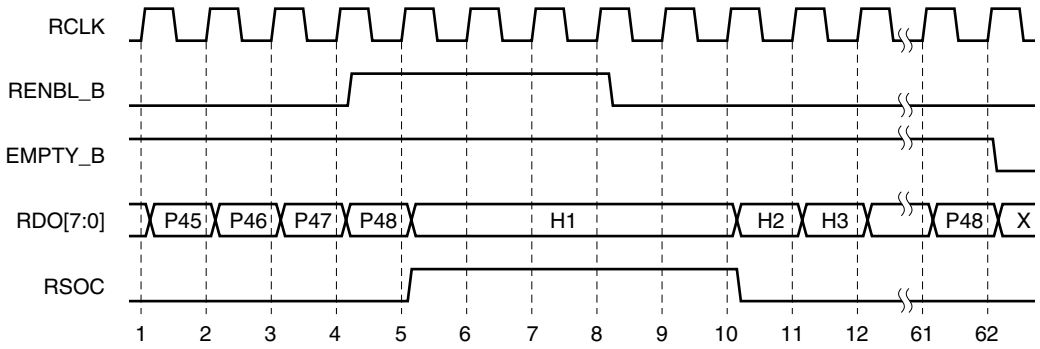
★ The $\mu$PD98404 stores the cell data it receives from a circuit in a receive FIFO having a capacity of 256 bytes (about 4 cells), and transfers this data to the ATM layer device in synchronization with the RCLK clock.

If valid data exists in the receive FIFO, it is reported to the ATM layer device by deasserting the EMPTY_B signal inactive (high level) (Edge 1 in the figure below). If the ATM layer device is ready to receive the data, it asserts RENBL_B active (low level) (Edge 2). The $\mu$PD98404 outputs data onto RDO[7:0] at the rising edge of the clock after the rising edge of RCLK at which RENBL_B has been asserted active (Edge 3). When the receive FIFO no longer has valid data, the RDO[7:0] output is undefined (Edge 5) by asserting EMPTY_B active. While the first byte of the cell header is output to RDO[7:0], RSOC is active (high level). When it is detected that the RENBL_B signal is deasserted inactive, data output is undefined (Edge 10).

**Figure 4-4. Octet Level Handshake Reception Timing (two-state operation)**



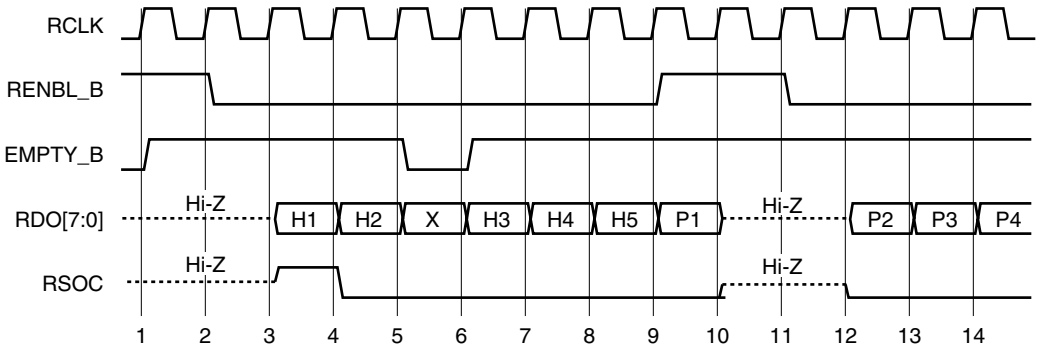

**Remark** If the $\mu$PD98404 deasserts RENBL_B inactive (high level) at the clock at which the 48th bytes of the payload is output, and if the first byte of the next cell is already in the receive FIFO, the $\mu$PD98404 asserts the RSOC signal active (high level) for the next cell, even if RENBL_B is inactive. This happens regardless of the 2-state or 3-state operation.




**(b) Three-state reception interface in single PHY octet level mode**

When it is detected that RENBL_B is deasserted inactive, receive data RDO[7:0] and cell header RSOC signal go into a high-impedance state (Edges 10 and 11 in the figure below). While RENBL_B is active (low level), the $\mu$PD98404 releases RDO[7:0] and RSOC from the high-impedance state and drives them even if it does not have cell data to output. Other than that, the operation is the same as that in mode 1.

**Figure 4-5. Octet Level Handshake Reception Timing (three-state operation)**



### 4.1.4 Single PHY cell level handshake mode

The cell level handshake mode is used to control transfer of transmit/receive cell data with the ATM layer device in cell units. The FULL_B/TCLAV and EMPTY_B/RCLAV signals that report the status of the transmit/receive FIFO respectively function as TCLAV and RCLAV signals, and report the status of the FIFO to the ATM layer device in cell units.

**(1) Transmission interface**

The μPD98404 asserts TCLAV active (high level) to inform the ATM layer device that it is ready to receive cells if there is a vacancy of one cell or more in the transmit FIFO (Edge 1 in Figure 4-6). When the ATM layer device detects that TCLAV has gone high, it asserts TENBL_B active (low level) and outputs data to TDI[7:0] (Edge 2). The μPD98404 writes the data on TDI[7:0] to the transmit FIFO in the clock cycles (edges 3 through 55) in which TENBL_B is low. In the cycles in which TEBL_B is inactive (high level), it does not write the data to the transmit FIFO (edges 56 through 58). In the cycles in which TSOC is high, the data on TDI is recognized as the first byte of a cell. While a cell is transferred, TCLAV goes high (active) if the next cell can be received; it goes low (inactive) if the next cell cannot be received.

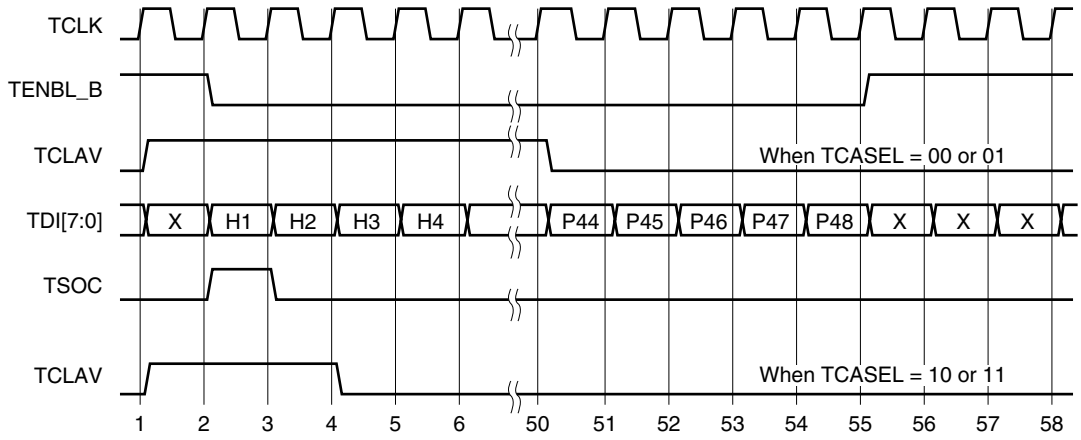
The timing of changing TCLAV can be selected from the modes listed in Table 4-2, depending on the setting of the TCASEL[1:0] bits of the mode register 3 (MDR3).

**Table 4-2. Selecting Timing Mode of Changing TCLAV Signal**

| TCASEL [1:0] | TCLAV Signal Changing Timing |
|---|---|
| ★ 00 (default) | After the byte five clocks before the tail of a cell (44th byte of the payload data) is transmitted while a cell is being transferred (Edge 50 in **Figure 4-5**), TCLAV is kept active if the transmit FIFO has a vacancy to store one cell in addition to the cell currently being received; TCLAV is deasserted inactive if the transmit FIFO has no vacancy. TCLAV is always active immediately before the data of the 44th byte of the payload data is transmitted. After TCLAV is deasserted inactive, the next cell cannot be transferred. |
| 01 | An operation same as the above is performed if the transmit FIFO has a vacancy of "two cells" instead of "one cell". After TCLAV is deasserted inactive, one more cell can be received. |
| 10 | TCLAV is asserted active if the transmit FIFO has a vacancy of one cell or more in addition to the storage area of the transmit cell currently received when the third byte (H3) of the cell data is transmitted (Edge 5 in **Figure 4-5**) while a cell is being transferred; TCLAV is deasserted inactive if the FIFO does not have a vacancy of one cell or more. |
| 11 | An operation same as the above is performed if the transmit FIFO has a vacancy of "two cells" instead of "one cell". After TCLAV is deasserted inactive, one more cell can be received. |

**Caution Select a mode by using TCASEL[1:0] only in the cell level handshake mode (CSEL bit = 1). In the octet level handshake mode (CSEL bit = 0), make sure that TCASEL[1:0] = 00 (default).**

**Figure 4-6. Cell Level Handshake Transmission Timing**



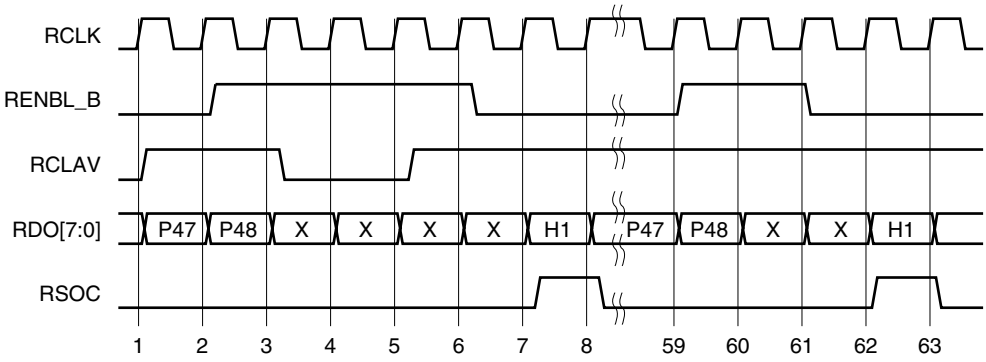

**(2) Reception interface**

In the single PHY cell level handshake mode, the two-state or three-state operation of RDO[7:0] and RSOC signal is selected by setting the HESEL bit of the MDR1 register and thereby changing the mode between 3 and 4.

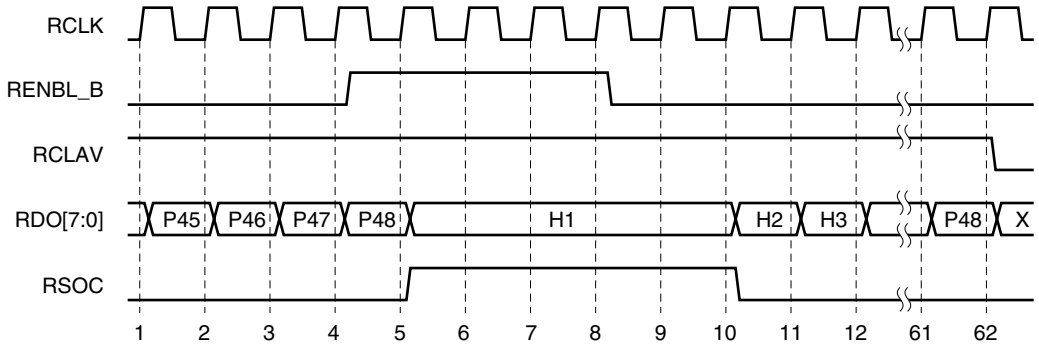
**(a) Two-state reception interface of single PHY cell level**

If the receive FIFO has one cell or more of valid data, the $\mu$PD98404 asserts RCLAV active (high level) to inform the ATM layer device (Edge 5 in **Figure 4-7**). When the ATM layer device detects the high level of RCLAV, it asserts RENBL_B active (low level) if it can receive the cell (Edge 6). The $\mu$PD98404 outputs the data to RDO[7:0] at the rising edge of the clock after the rising edge of RCLK at which RENBL_B becomes active. While the first byte of the cell is output, RSOC is also asserted active (high level) (Edge 7). If it is detected that RENBL_B has been deasserted inactive (high level) while the cell is being transferred, data output is undefined (Edge 60).

**Figure 4-7. Cell Level Handshake Reception Timing (two-state operation)**



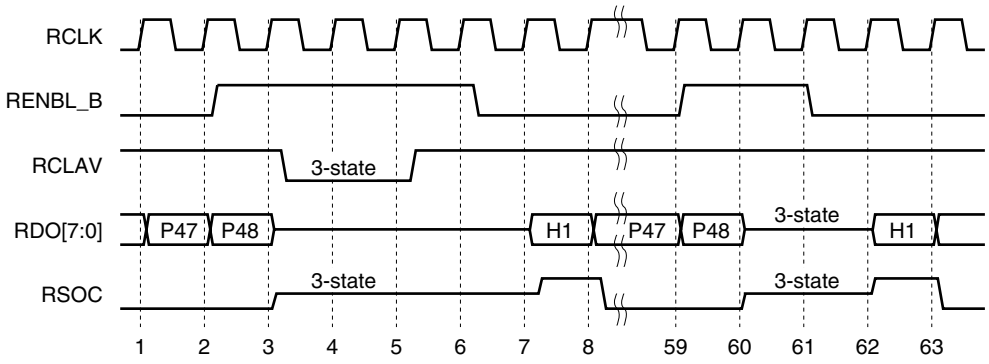
**Remark** If the μPD98404 deasserts RENBL_B inactive (high level) at the clock at which the 48th byte of the payload is output, and if the first byte of the next cell is already in the receive FIFO, the μPD98404 asserts the RSOC signal active (high level) for the next cell, even if RENBL_B is inactive. This happens regardless of the 2-state or 3-state operation.




**(b) Three-state reception interface of single PHY cell level**

When it is detected that RENBL_B has been deasserted inactive, receive data RDO[7:0] and RSOC go into a high-impedance state. Other than that, the operation is performed in the same manner as in mode 3.

**Figure 4-8. Cell Level Handshake Reception Timing (three-state operation)**




During the default operation of cell level handshake in modes 3 and 4, RCLAV remains active, once it has been asserted active, up to the cycle in which the 48th byte of the payload data is output. The level of RCLAV is changed, depending on the status of the receive FIFO, in the clock cycle next to the one in which the 48th byte of the payload data is output. The timing to change RCLAV can be selected from the modes shown in Table 4-3 by setting the RCASEL bit of the mode register 3 (MDR3).

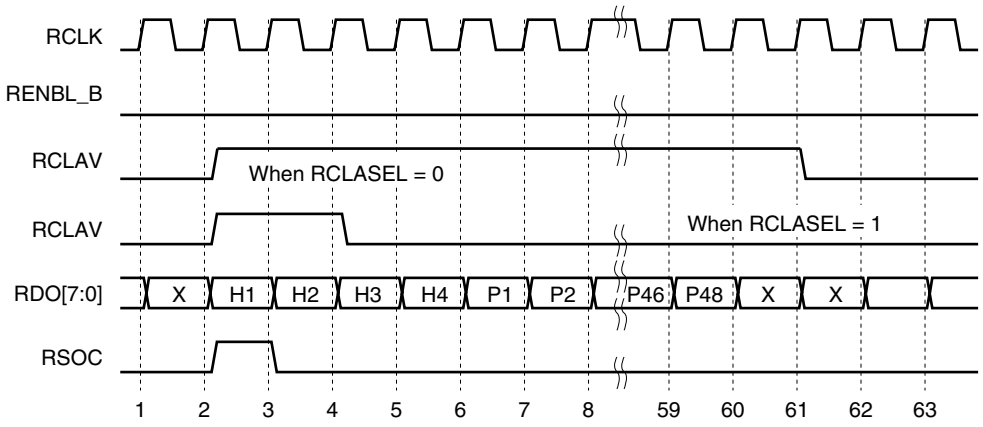
**Table 4-3. Selecting Changing Timing Mode of RCLAV Signal**

| RCASEL | Changing Timing of Signal RCLAV |
|---|---|
| 0<br>(default) | RCLAV is asserted active (high level) if the receive FIFO has one cell or more of valid data at the clock after the one at which the last byte of the cell (48th byte of the payload data) is output; it is deasserted inactive (low level) if the FIFO has no data. While the receive cell data is being output, RCLAV is always active. |
| 1 | RCLAV is asserted active if the receive FIFO has one cell or more of data in addition to the receive data currently output after the clock at which the second byte (H2) of the header of the receive cell data is being output; it is deasserted active if the FIFO has no data. |

**Cautions 1. There are limitations on the RCASEL = 1 mode. For details, refer to CHAPTER 8 CONSTRAINTS.**

**2. Select a mode by using the RCASEL bit only in the case of cell level handshake (CSEL bit = 1). In the case of octet level handshake, make sure that RCASEL = 0 (default).**

**Figure 4-9. RCLAV Changing Timing**



### 4.1.5 Multi-PHY mode (TCLV/RCLV 3-state)

**(1) Transmission interface**

In the multi-PHY mode, the ATM layer device gives in advance specific addresses to the μPD98404s to be connected. Each of these addresses is stored in the PHYID register (address: 29H) of the corresponding μPD98404 via the management interface, and at the same time, the enable bit (EN bit of MSB) is set to 1. In this way, the μPD98404 checks the signal on TADD[4:0].

The ATM layer device sequentially outputs the addresses of the μPD98404s connected to TADD[4:0], and checks TCLAV and polls the status of each transmit FIFO. Each μPD98404 checks whether its address (value set in the PHYID register) coincides with the signal on TADD[4:0]. If they coincide, the μPD98404 drives the TCLAV signal in the clock cycle after the one in which the address was output. The TCALV signal goes high if the ATM layer is ready to receive a cell; it goes low if it is not. The signal goes into a high-impedance state if the addresses do not coincide.

The ATM layer device selects one of the μPD98404s ready to receive a cell, outputs the address of the selected μPD98404 to TADD while TENBL_B is inactive (high level), and then asserts TENBL_B active (low level). The μPD98404 whose address coincides with the address output to TADD[4:0] in the cycle preceding that in which TENBL_B is asserted active is selected. This selected status starts from the cycle following the cycle in which the address of the μPD98404 was output to TADD[4:0] and TENBL_B went low (active), and is cleared in the cycle in which TENBL_B is asserted active again. The ATM layer device starts transferring cell data after it has selected the μPD98404, and performs polling again.

Figure 4-10 is an example showing the cycles required for the ATM layer device to start polling and to complete cell transfer. In this example, four μPD98404s with addresses (N), (N + 1), (N + 2), and (N + 3), respectively, are connected. The ATM layer device performs polling by repeatedly outputting these four addresses. One cycle of 1F(H) is inserted in between the valid addresses on TADD[4:0]. Address 1F(H) is used as an address value that is not equivalent to any of the addresses of the μPD98404s. A μPD98404 drives TCLAV in the cycle next to the one in which 1F(H) is output next after the valid address has been output. In the example, μPD98404 of (N + 3) and μPD98404 of (N) that is transferring a cell are ready to receive the next cell. While a cell is being transferred, TCLAV becomes valid at the 44th byte or later in the default mode (MDR3 register TCASEL = 00). Before that, TCLAV remains high. Therefore, TCLAV = H at Edge 7 in the figure below means that TCLAV simply remains high, but TCALV = H at Edge 15 indicates that the μPD98404 of address (N) is ready to receive the next cell.

In this example, (N + 3) is selected. This address is output to TADD[4:0] while TENBL_B is inactive (high) at Edges 15 and 16, and the μPD98404 assigned this address is selected when TENBL_B is asserted active again. After that, cell transfer is started, and the ATM layer device immediately starts polling.

**Figure 4-10. Transmission Timing of Multi-PHY**

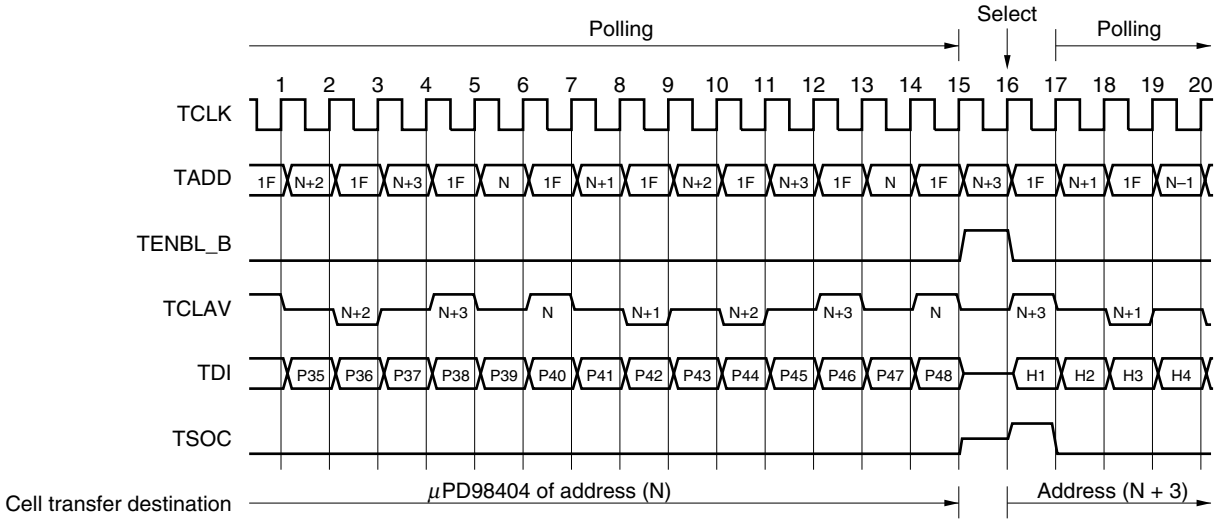



Figure 4-11 shows an example where cell transfer is stopped because none of the μPD98404s can receive a new cell. Polling goes on during the period of several clocks in which cell transfer is stopped. During this period, TDI[7:0] and TSOC go into a high-impedance state, and the TENBL signal remains inactive (high level). In this example, the μPD98404 of (N + 3) is ready to receive a cell. The ATM layer device learns that this μPD98404 is ready to receive a cell by means of polling, outputs address (N + 3) again to select this μPD98404 before asserting TENBL_B active (low level) (Edge 16 in the figure).

**Figure 4-11. End and Cell Transmission and Re-transmission**

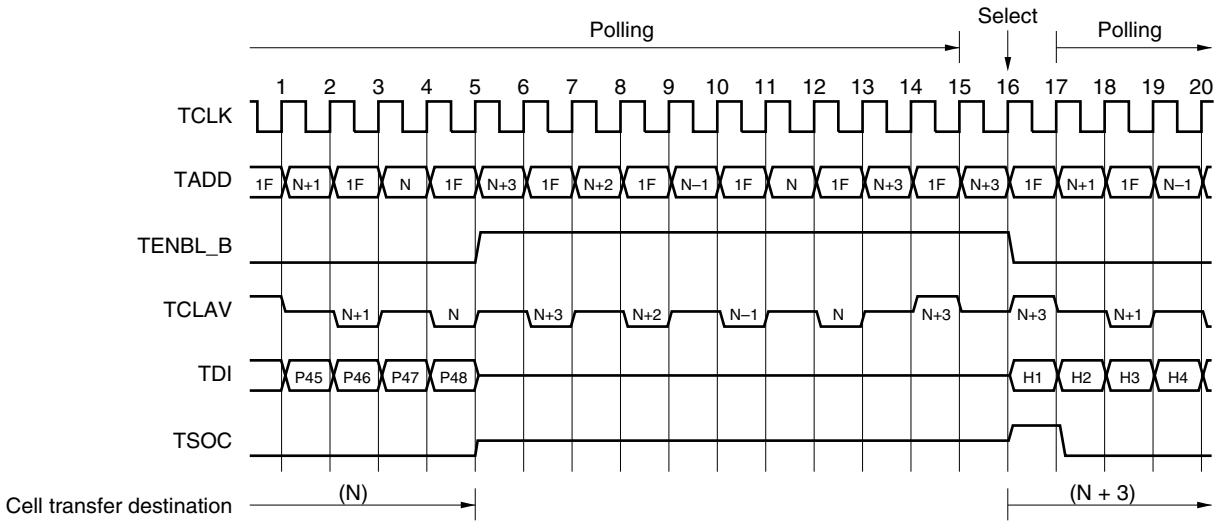
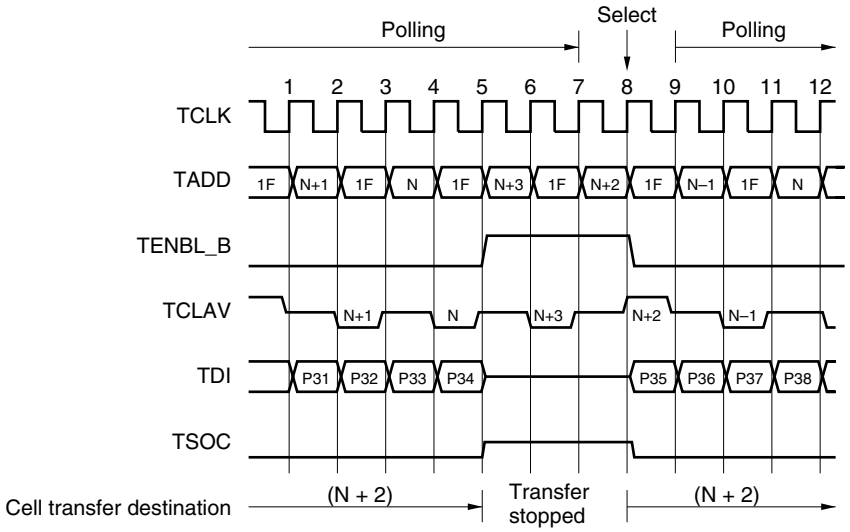


Figure 4-12 shows an example in which data transfer is stopped while the ATM layer device is transferring a cell because data was not prepared in time. In this example, transfer is stopped during the period of three clock cycles. During this period, TENBL_B is deasserted inactive, and TDI and TSOC go into a high-impedance state. Even during this period, polling can go on. To resume data transfer, the address of the μPD98404 previously selected is output to TADD[4:0] to select the μPD98404 again.

**Figure 4-12. Stopping Cell Transmission**




**(2) Reception interface**

The ATM layer device sequentially outputs the addresses of the connected μPD98404s to RADD[4:0], checks RCLAV, and polls the status of the receive FIFO of each μPD98404. The address used at the reception side is the value in the PHYID register, i.e., the same address as the transmission side. The address in the PHYID register is used in the same manner at both the transmission and reception sides. The μPD98404 whose address coincides with the signal on RADD[4:0] drives RCLAV in the clock cycle after the one in which the address was output. If the ATM layer device has a cell to output, RCLAV is asserted active (high level); if not, it is deasserted inactive (low level). If the address does not coincide, RCLAV goes into a high-impedance state.

The ATM layer device selects one of the μPD98404s that have returned the high level of RCLAV, outputs the address of the selected μPD98404 to RADD[4:0] while RENBL_B is inactive (high level), and then deasserts RENBL_B active (low level). The μPD98404 whose address coincides with the signal on RADD[4:0] in the cycle preceding the one in which RENBL_B is asserted active is selected.

The selected μPD98404 starts transferring cell data to the ATM layer device. When transfer of the cell is started, the ATM layer device starts polling again. The selected status of the μPD98404 is cleared in the cycle in which RENBL_B is deasserted inactive (high level).

Figure 4-13 shows an example of cycles in which a μPD98404 is polled and cell transfer is completed. In this example, four μPD98404s with addresses (N), (N + 1), (N + 2), and (N + 3), respectively, are connected. Polling performed while the cell of the μPD98404 of address (N) is being transferred indicates that the μPD98404 of address (N + 3) has a cell to be transferred, and that (N + 3) is selected. This μPD98404 is selected at the rising edge (Edge 16) of RCLK. Immediately after transferring a cell to (N + 3) is started, the ATM layer devices resumes polling.

During polling, the μPD98404 having address (N) returns the high level of RCLAV. This is because RCLAV is always kept high while receive data is output if the timing of making RCLAV valid is set in the default mode (RCASEL bit of MDR3 register = 0), and does not mean that the μPD98404 has more valid cells.

**Figure 4-13. Example of Reception Timing in Multi-PHY Mode (1)**

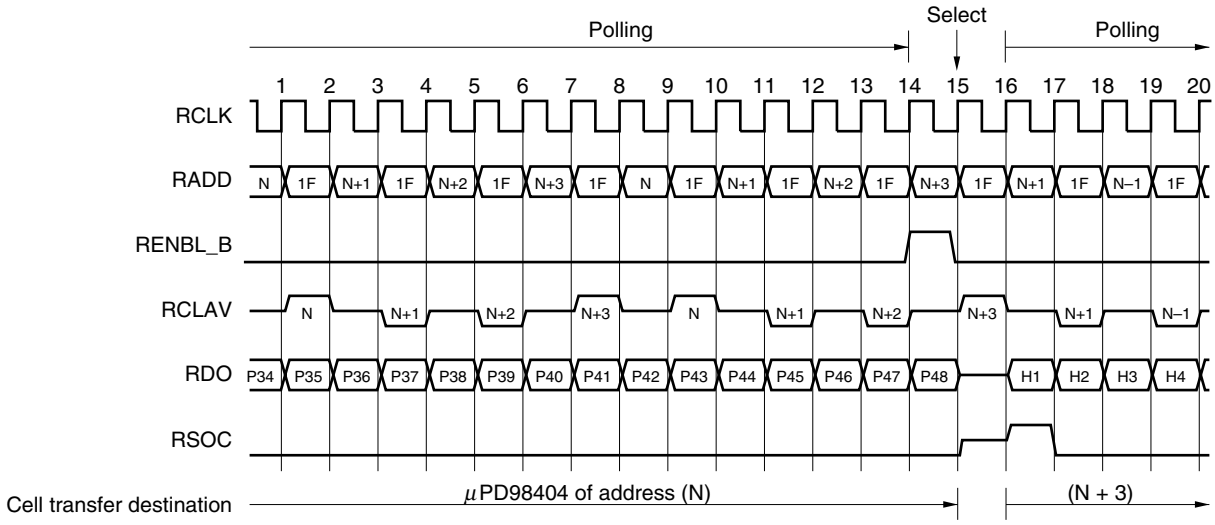


Figure 4-14 shows a case where no other μPD98404s have valid data to be transferred when transfer of one cell from a μPD98404 has been completed. Because no μPD98404 can be selected, the ATM layer device keeps RENBL_B active (low level). Although the μPD98404 of (N) remains selected, the ATM layer device deasserts RENBL_B inactive (high level) because no cell is output. The ATM layer device continues polling. As a result, it detects that the μPD98404 of (N + 3) has a cell to be transferred and therefore, outputs address (N + 3) to select the μPD98404 again.

**Figure 4-14. Example of Reception Timing in Multi-PHY Mode (2)**

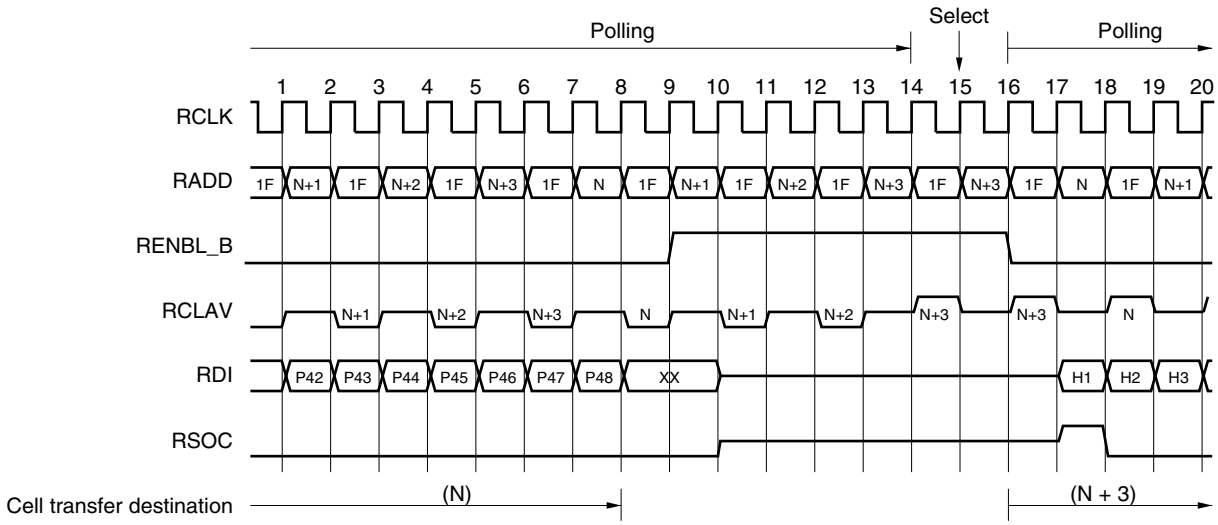



Figure 4-15 shows a case in which a valid cell to be transferred is found after an interval of one clock cycle, although the selected μPD98404 of address (N) has completed transferring a cell. Because RENBL_B is active at Edge 9, the μPD98404 of address (N) asserts the RSOC signal active (high level) and starts outputting cell data. The ATM layer device has deasserted RENBL_B inactive, but selects the μPD98404 of address (N) again for reception.

**Figure 4-15. Example of Transmitting Two Cells in Succession from the Same μPD98404 (1)**

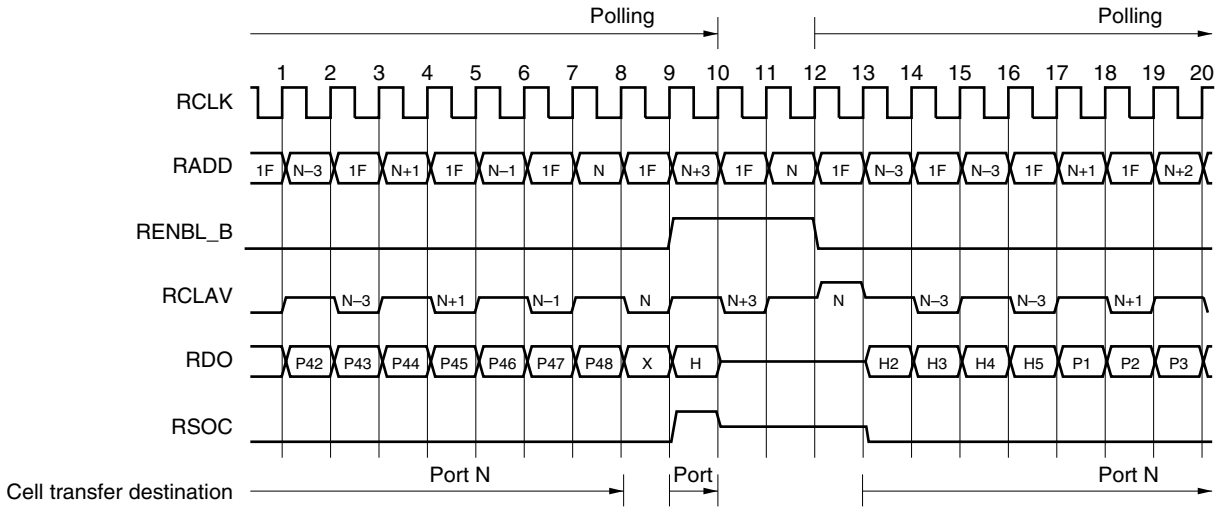


Figure 4-16 shows an example where the same μPD98404 successively transmits two cells. Because the other μPD98404s do not return an active level (high level) of RCLAV when the μPD98404 of address (N) completes cell transmission, the ATM layer device continues selecting the μPD98404 of address (N) and keeps RENBL_B active (low level). In this example, two cells are transmitted in succession because the μPD98404 of address (N) has another valid cell. The ATM layer device recognizes that another cell is transmitted when RSOC goes high.

**Figure 4-16. Example of Transmitting Two Cells in Succession from the Same μPD98404 (2)**

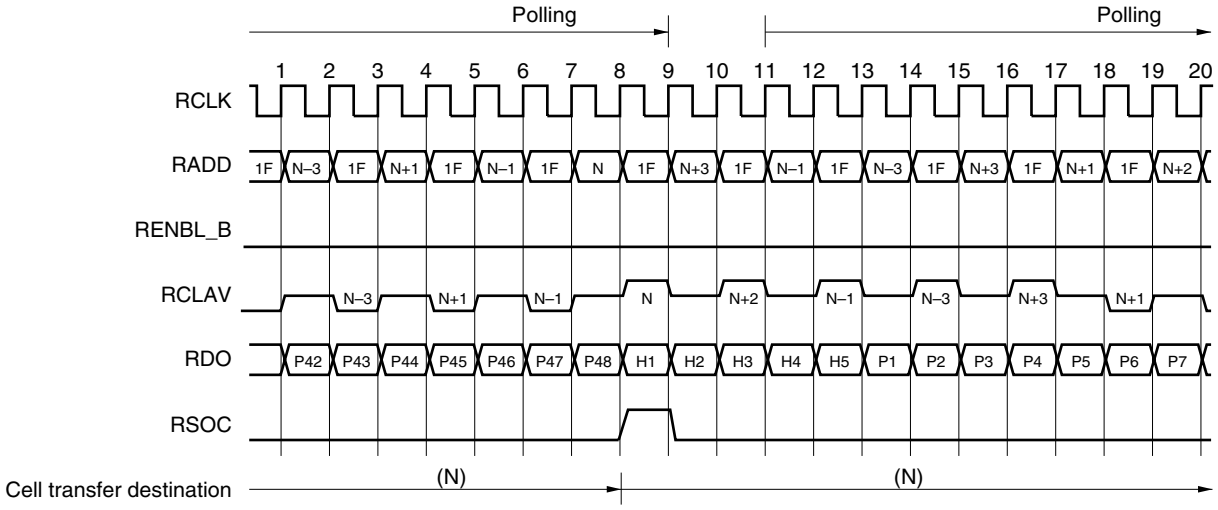
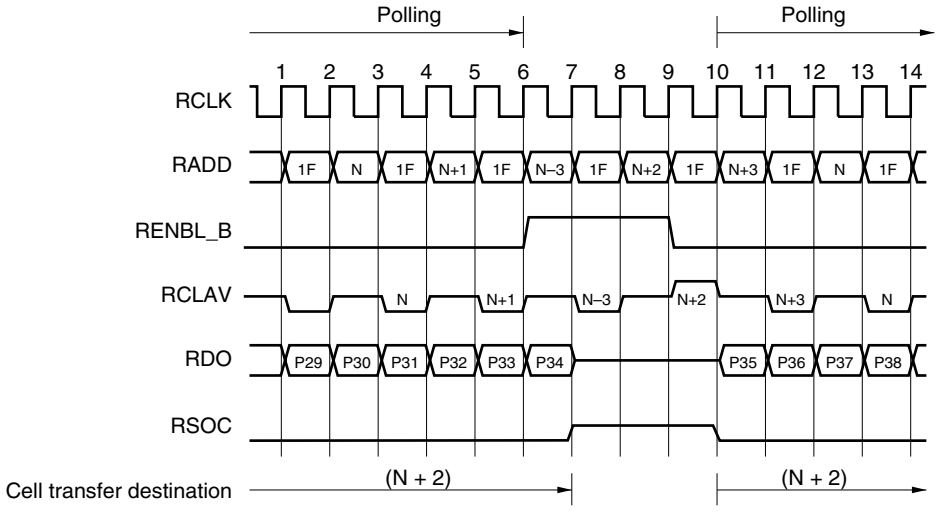



Figure 4-17 shows an example where the ATM layer devices stops cell transfer from the μPD98404 of address (N + 2) for the duration of three clock cycles. Before asserting RENBL_B active again, the ATM layer device outputs the address of the μPD98404 whose data transfer has been stopped, to select that μPD98404 again.

**Figure 4-17. Example of ATM Layer Device Stopping Transfer**



## 4.2 PMD Interface

The PMD interface is used to connect transceiver/receivers on circuit side. The PMD interface of the μPD98404 supports three modes as shown in Table 4-4. These modes are selected by using the PSEL[1:0] input pins.

**Table 4-4. PMD Interface Mode**

| PSEL [1:0] | Mode |
|---|---|
| 00 | Serial mode using internal clock recovery/synthesizer (default) |
| 01 | Serial mode using RCIT/RCIC, TFKT/TFKC clocks supplied from external devices |
| 1X | Parallel interface using RPC/TFC pin input clock |

### 4.2.1 Serial interface mode

The serial interface mode is used in two ways: by using the clock generated by the internal clock recovery/synthesizer as the transmit/receive clock and by using the clock supplied to the RCIT/RCIC or TFKT/TFKC pin from an external source.

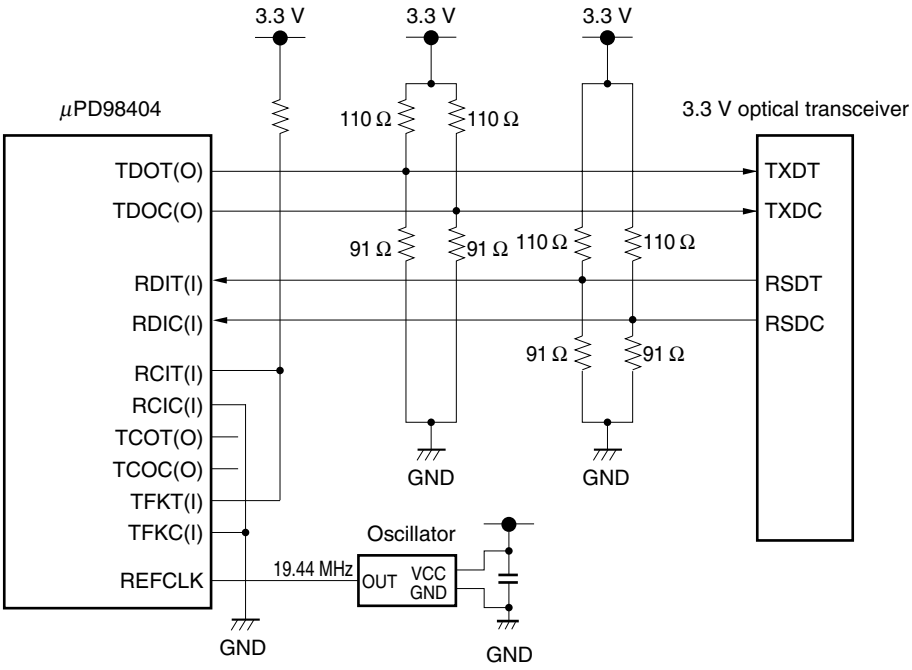
**(1) Mode using internal clock recovery/synthesizer function (PSEL[1:0] = 00)**

The internal clock recovery and synthesizer functions are enabled when the PSEL[1:0] pin is “00”. At this time, the RCIT/RCIC and TFKT/TFKC pins for transmits/receive clock input are not used. Transmit/receive data are input/output via PECL level interface. Terminate TDOT/TDOC at the transmitter side at VDD-2V and 50 Ω. Figure 4-18 shows an example of connecting an optical module as a transceiver/receiver, by using the internal clock recovery/synthesizer function.

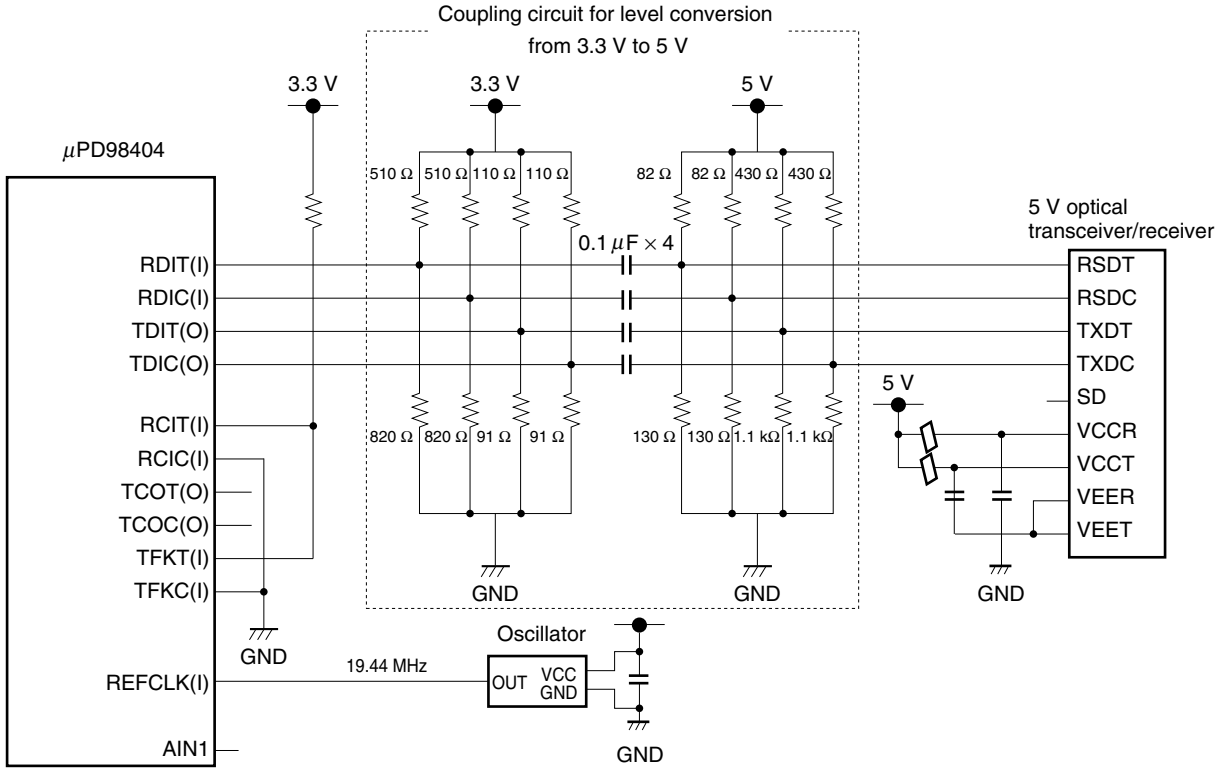
★ When the μPD98404 and an optical module are AC-coupled as shown in Figure 4-18 (bottom), and if optical input is not supplied to the optical module and successive 0s are input to RDIT/RDIC as data, the potential levels of RDIT and RDIC have no difference. Consequently, the μPD98404 cannot recognize the receive data as successive 0s, and cannot detect LOS. In this case, connect the optical input cut signal output pin of the optical module to the PMDALM pin of the μPD98404 to detect LOS. By clearing the PMD bit of the IACM register, the μPD98404 adds a change of the input level of the PMDALM pin as a condition of detecting LOS (PMDALM pin Low: Normal, High: LOS detection).

★ **Figure 4-18. Example of Connection in Serial Interface Mode (with internal PLL used)**

**Connecting 3.3 V Optical Transceiver**




**Connecting 5 V Optical Transceiver**



- **Receive clock recovery PLL function**

  The internal clock recovery PLL unit extracts a receive clock from the receive data string input to the RDIT/RDIC pin.

  The μPD98404 has an OOL (Out of Link) detection circuit that checks to see if the receive clock recovery PLL is correctly locked onto the receive data string and extracts the clock as expected. This circuit compares the clock generated by PLL and divided by eight with the frequency of the clock input to the REFCLK pin. If the difference between the two clock frequencies exceeds 244 ppm, the OOL detection circuit judges that the receive clock recovery PLL is not locked as expected (OOL status). If the difference is within 244 ppm, the OOL status is cleared. The OOL status is reflected on the bits by the PICR register and can be used as an interrupt cause.

  To prevent the receiver circuit from operating with an unstable clock in the OOL status, the receive clock that is used by the receiver circuit as a source clock can be automatically changed to the clock generated by the transmit synthesizer. When the OOL status is cleared, the recovery clock is used as the receive clock again. This function is enabled by default. It can be disabled by setting the oolenb bit of the mode register 2 (MDR2) to 1.

  Immediately after power application, the receive clock recovery PLL starts extracting the clock, but it enters the OOL status because data synchronization cannot be established immediately. When a correct data string is input to RDIT/RDIC, it takes the OOL detection circuit about 0.6 s to judge whether the frequency difference between the recovered clock and REFCLK clock is within 244 ppm. The OOL status is cleared, therefore, after 0.6 s, and the recovery clock is supplied to the receiver circuit.

  If the oolenb bit is disabled, however, and if receive data is correctly input in the OOL status, the receive clock recovery PLL is synchronized within 1 ms.

**Caution If a circuit signal loss (LOS) error occurs, the receive PLL enters the free-run status. Consequently, the frequency shifts from that of REFCLK, resulting in the OOL status. If the oolenb bit of the mode register 2 (MDR2) is 0 at this time, the clock generated by the transmit synthesizer PLL is automatically switched to the receive clock. If this happens, the OOL detection circuit compares the clock of the transmit synthesizer PLL with REFCLK. As a result, the OOL status is cleared and the recovery clock is switched to the receive clock again.**

**While LOS is detected, the OOL status takes place and is cleared repeatedly. If interrupt servicing mode 2 is selected, note that the OOL bit of the interrupt cause register (PICR) is repeatedly set and reset in accordance with this operation. Disable automatic selection by setting oolenb to 1.**

The receive clock can be forcibly switched to the clock generated by the transmit synthesizer PLL by using the RxCL bit of the mode register 2 (MDR2), as follows:

| Setting of RxCL Bit | Receive Clock |
|---|---|
| 1 | Clock generated by transmit synthesizer PLL |
| 0 | Clock extracted by receive clock recovery PLL |

- **Transmit PLL function**

  The internal synthesizer generates a clock of 155.52 MHz based on the 19.44 MHz clock input to the REFCLK pin. The clock to be input to the synthesizer can be selected as follows by using TxCL[1:0] of the mode register 1 (MDR1).

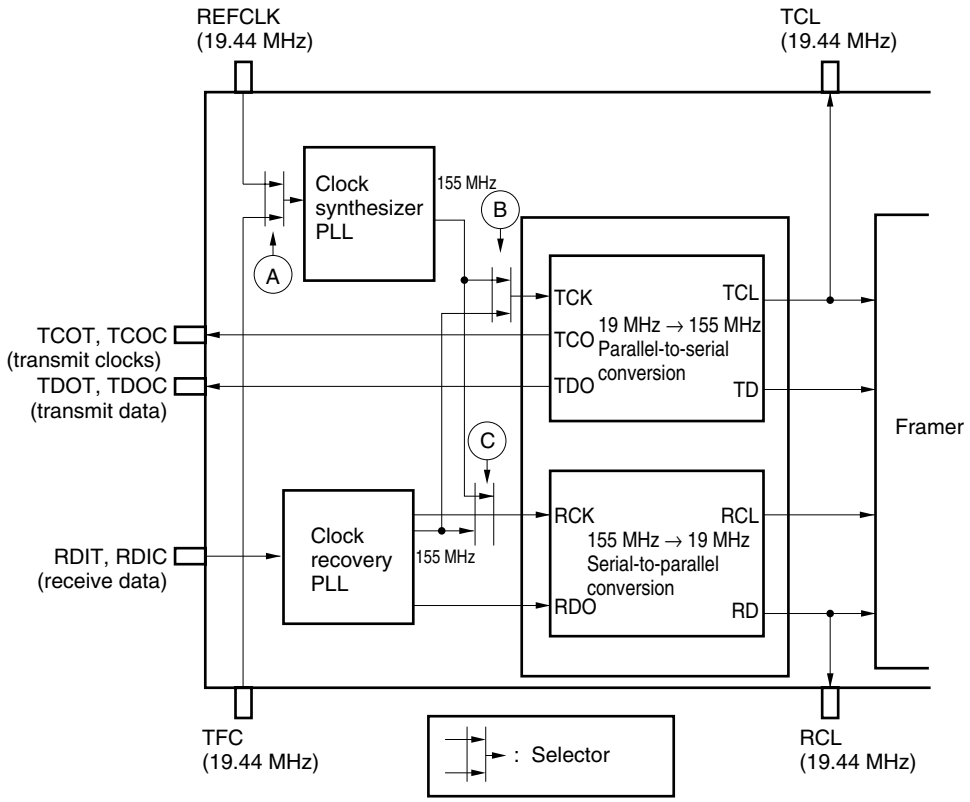
| Mode | TxCL[1:0] | Synthesizer Reference Clock |
|---|---|---|
| 1 | 00 | Clock input to REFCLK pin (default) |
| 2 | 10 | Clock input to TFC pin |
| 3 | X1 | Clock of receive clock recovery PLL is used as clock at transmission side as is. |

**Cautions 1. When the clock extracted by the receive clock recovery PLL is used as the transmit clock in mode 3, be sure to set the oolenb bit of the mode register 2 to 1 so that the clock extracted by the clock recovery PLL is always supplied as the receive clock.**

**2. The data output from the TDOT/TDOC pin when the TxCL[1:0] bits of the MDR1 register = X1 is latched at the clock of the receive clock recovery PLL. In the meantime, the TCOT/TCOC pin outputs the clock of the internal synthesizer or clock input to the TFKT/TFKC pin in accordance with the setting of the PSEL[1:0] pins. If the clock of the receiver side is used as the source clock of transmit data, the data output by TDOT/TDOC and the clock output by TCOT/TCOC are not in synchronization.**

**3. The TFC inputs the transmit clock for the parallel interface in the parallel mode (PSEL[1:0] pins = 1X). However, it inputs the source clock for the internal clock synthesizer if the TxCL[1:0] bits of the MDR1 register = 10 in the serial mode in which the internal clock synthesizer is used (PSEL[1:0] pins = 00).**

**Figure 4-19. Outline of PMD Layer Block**



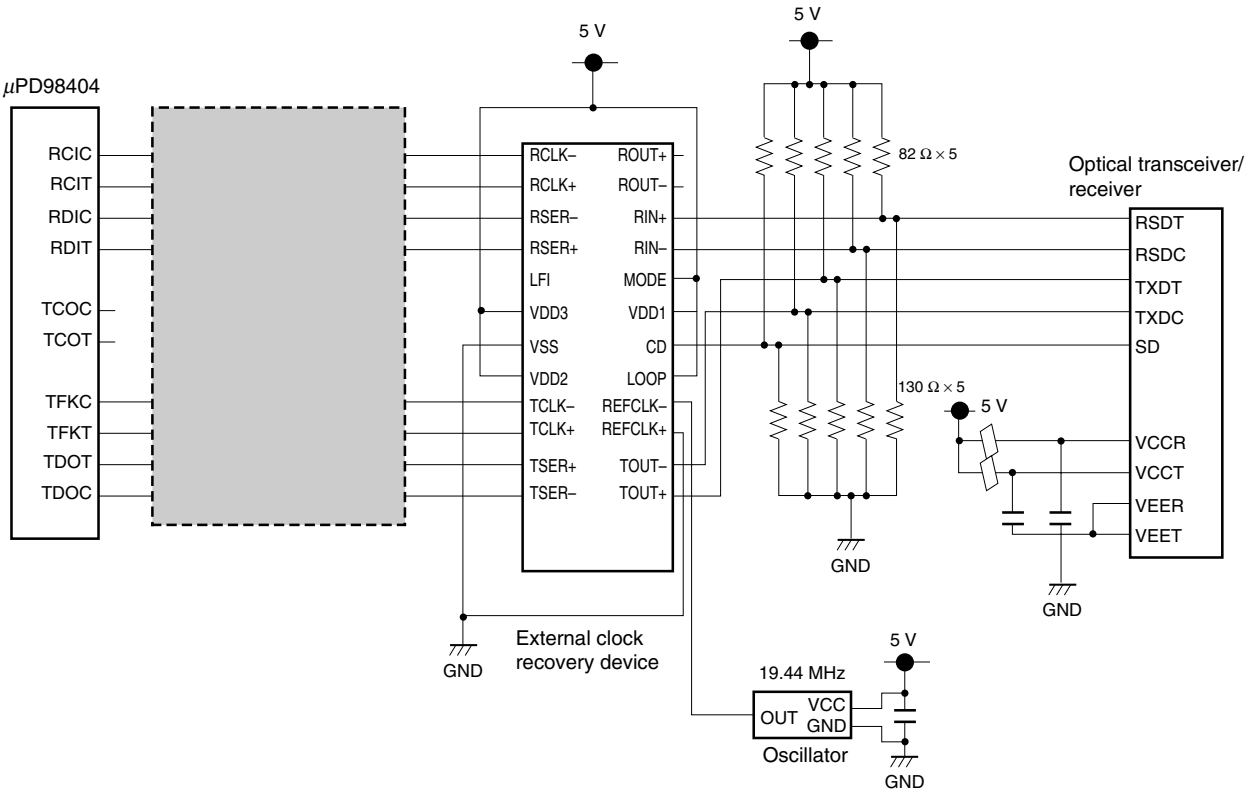

Selector A: MDR1 Register TxCL[bit 1]
Selector B: MDR1 Register TxCL[bit 0]
Selector C: MDR2 Register RxCL

**(2) To use RCIT/RCIC, TFKT/TFKC clock input**

When the PSEL[1:0] pins are “01”, the internal clock recovery/synthesizer function is disabled, and the 155.52 MHz clock input to the RCIT/RCIC or TFKT/TFKC pin is used as the transmit/receive clock. The μPD98404 outputs the transmit data from the TDOT/TDOC pin in synchronization with the clock input to the TFKT/TFKC pin. The receive data input to the RDIT/RDIC pin is sampled with the clock input by an external clock recovery device to the RDIT/RDIC pin.

Moreover, the clock input to the RCIT/RCIC pin can be selected as the transmit clock by setting the TxCL[1:0] bits of the mode register to “11”. At this time, the TFKT/TFKC pin is not used.

**Figure 4-20. Example of Connection in Serial Interface Mode (with external PLL used)**




: 3.3 V-to-5 V conversion. Refer to the portion enclosed by the dotted line in Figure 4-18.

### 4.2.2 Parallel interface mode

The 8-bit parallel interface mode is set when the PSEL[1:0] pins are “1X”.

The μPD98404 outputs parallel transmit data from the TPD0 through TPD7 pins in synchronization with the 19.44 MHz clock input to the TFC pin, and loads the receive data input to the RPD0 through RPD7 pins in synchronization with the clock input to RPC pin. A 19.44 MHz clock in synchronization with the receive data extracted by a clock recovery LSI is input to the RPC pin.

The TPC pin usually outputs the transmit clock input to the TFC pin. In the PMD layer loopback mode 2, however, the clock input to the RPC pin is output.

## 4.3 Management Interface

The management interface is an interface with the bus of the host processor to control the μPD98404. The μPD98404 supports three modes of this interface as shown in Table 4-5. Whether MSEL0 or MSEL1 mode is used is determined by the input status of the MSEL pin at hardware reset.

When the MSEL pin is low, two modes can be selected: the normal MSEL0 mode and S15 mode in which NEC's SAR chip μPD98401A (NEASCOT-S15) is connected. These two modes are automatically selected when the μPD98404 checks the timing of the CS_B and DSB signals during the first read or write operation on power application. The conditions under which the MSEL or S15 mode is set are shown in Table 4-6.

**Table 4-5. Management Interface Mode**

| | |
|---|---|
| MSEL0 mode | RD_B, WR_B, ACK_B style (Motorola compatible mode) |
| MSEL1 mode | DS_B, R/W_B, RDY_B style (Intel compatible mode) |
| S15 mode | Mode to connect NEC SAR LSI μPD98401A (NEASCOT-S15) .<br>CS_B, DS_B, R/W_B are used. |

**Table 4-6. Mode Select Condition When MSEL Pin Is Low**

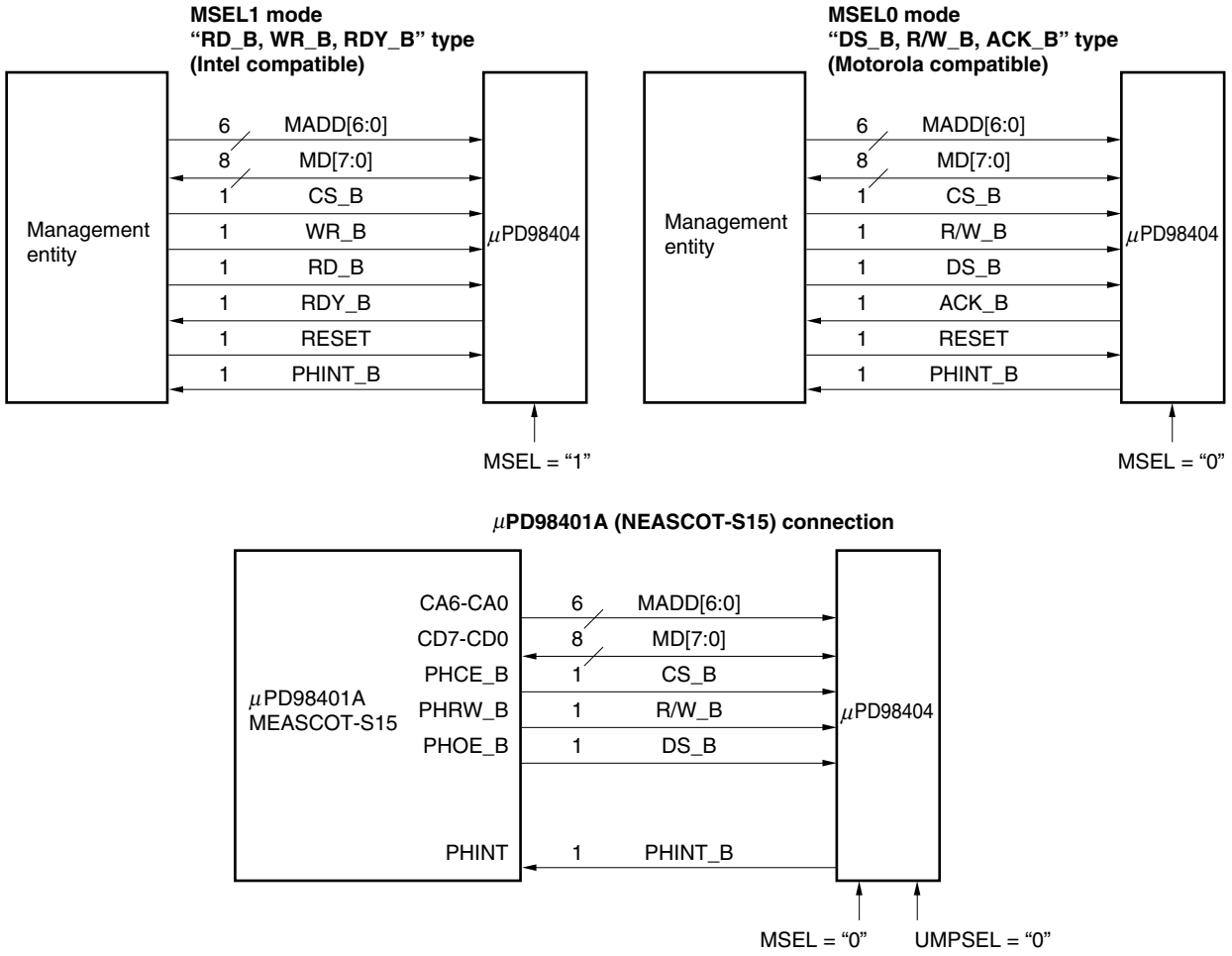
| Initial Operation | MSEL Mode Setting Condition | S15 Mode Setting Condition |
|---|---|---|
| Read | MSEL mode is identified if low pulse is input to DS_B until 9 clock cycles elapse after CS_B has gone low. | S15 mode is identified if low pulse is input to DS_B after 11 clock cycles have elapsed after CS_B fell. |
| Write | MSEL mode is identified if low pulse is input to DS_B while CS_B is low. | S15 mode is identified if DS_B retains high while CS_B is low. |

**Cautions 1. If the first operation is a read operation and if it is detected that DSB has gone low at the 10th clock cycle after CS_B fell, it is unclear whether the μPD98404 is subsequently set in the MSEL or S15 mode.**

**2. Allow a recovery time of "4 x TCLK" clock cycle or longer (from DS_B↑ to DS↓) between one register access and the next access.**

**3. If the device is reset in software by setting the CMR2 register, do not read or write all the registers for at least the duration of "20 x TCLK clock cycle" from the write cycle in which the device has been reset. This is because the registers may not be correctly read or written.**

**Figure 4-21. Management Interface**



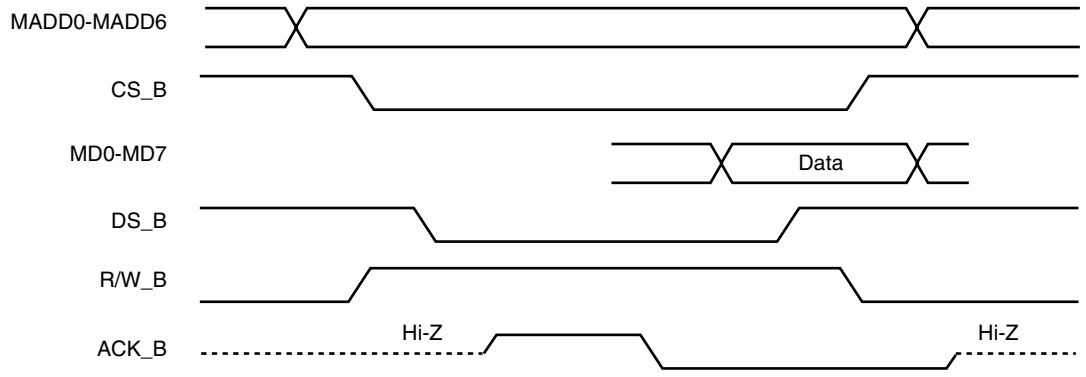

### 4.3.1 Read operation

The host starts a read operation by driving an address onto MADD[6:0] and asserting CS_B and RD_B or DS_B active (low level). In response, the μPD98404 drives RDY_B (ACK_B) low and outputs the requested data to MD[7:0] within a specific time. The host acknowledges that RDY_B (ACK_B) has gone low, deasserts RD_B (DS_B) high, and reads the data on MD[7:0]. If the μPD98404 is not selected by CS_B, it makes RDY_B (ACK_B) and MD[7:0] go into a high-impedance state. In the MSEL1 mode, a read cycle is recognized when RD_B is asserted low while WR_B is high. In the MSEL0 mode, a read cycle is recognized when RW_B is deasserted high while DS_B is low. Figure 4-22 shows the read timing in each mode.

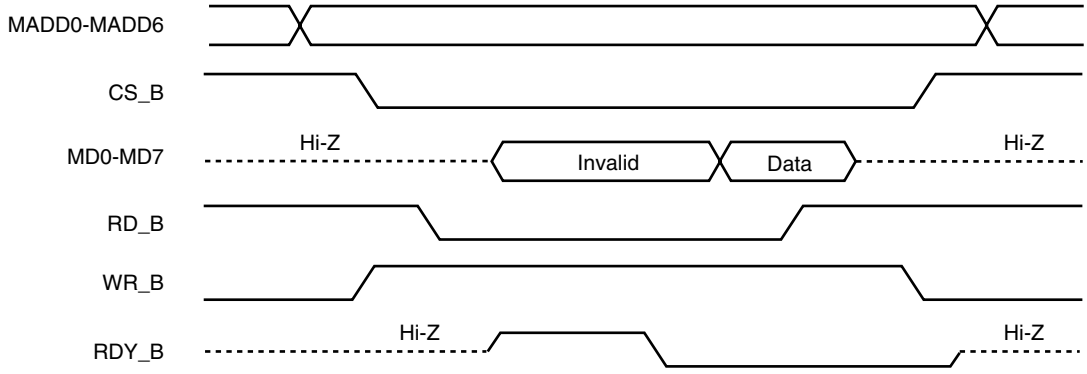
**Remark** The time from when DS_B (RD_B) has gone low until the μPD98404 asserts ACK_B (RDY_B) low differs depending on the register to be accessed, but it is “4 x TCLK clock cycle” at maximum. To read any register without using ACK_B (RDY_B), make sure that the pulse width of RS_B (RD_B) is at least “4 x TCLK clock cycle”.

**Figure 4-22. Read Operation**

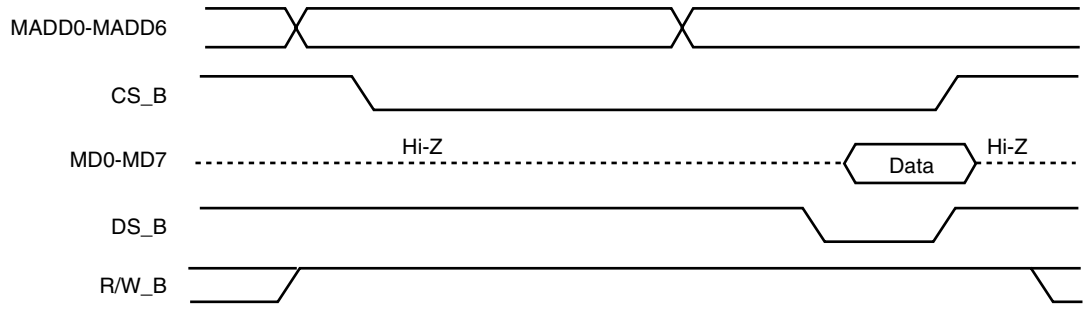
- **MSEL0 mode (Motorola compatible)**




- **MSEL1 mode (Intel compatible)**




- **S15 mode (MSEL pin = 0)**



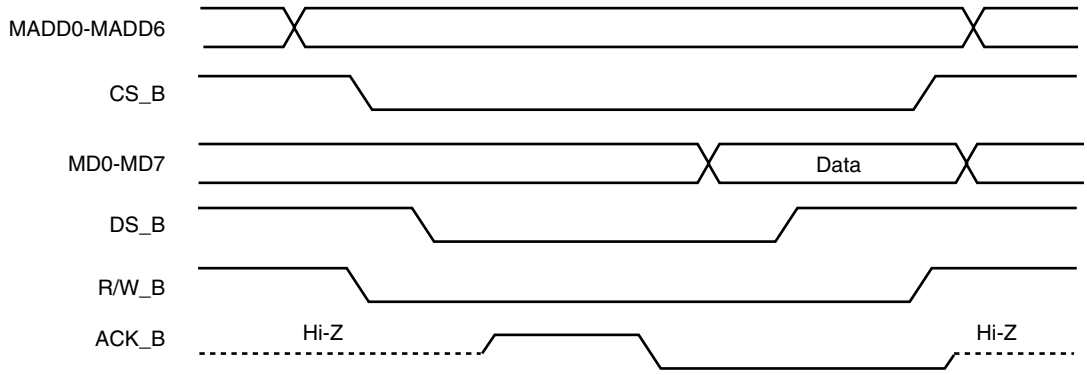
### 4.3.2 Write operation

The host starts a write cycle by driving an address onto MADD[6:0], outputting the data to MD[7:0], and asserting CS_B and WR_B or DS_B low. In response, the μPD98404 informs the host that it is ready for reading data, by asserting RDY_B (ACK_B) low. The host acknowledges that RDY_B (ACK_B) is low and deasserts WR_B (DS_B) high. The μPD98404 reads the data on MD[7:0] at the rising edge of WR_B(DS_B). If it is not selected by CS_B, RDY_B (ACK_B) goes into a high-impedance state. In the MSEL1 mode, the μPD98404 recognizes a write cycle when WR_B is asserted low while RD_B is high. In the MSEL0 mode, it recognizes a write cycle when RW_B is asserted low while DS_B is high. Figure 4-23 shows the write timing.

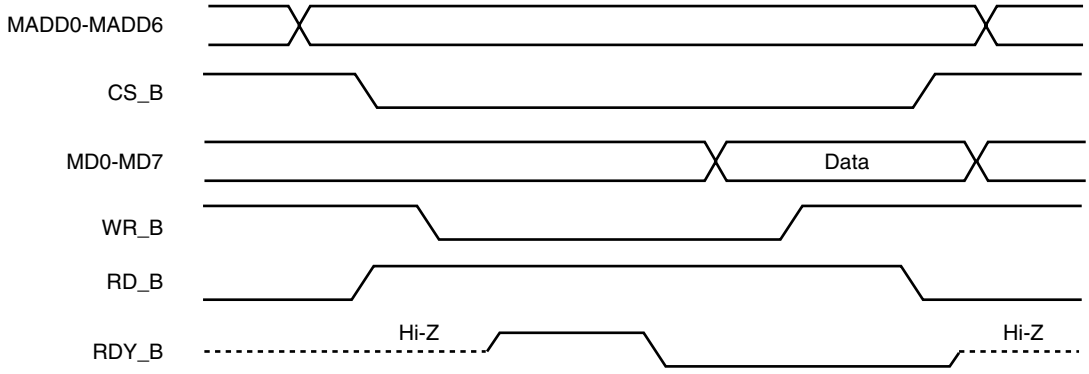
**Remark** The time from when DS_B (WR_B) has gone low until the μPD98404 asserts ACK_B (RDY_B) low differs depending on the register to be accessed, but it is “4 x TCLK clock cycle” at maximum. To write any register without using ACK_B (RDY_B), make sure that the pulse width of RS_B (WR_B) is at least “4 x TCLK clock cycle”.

**Figure 4-23. Write Operation**

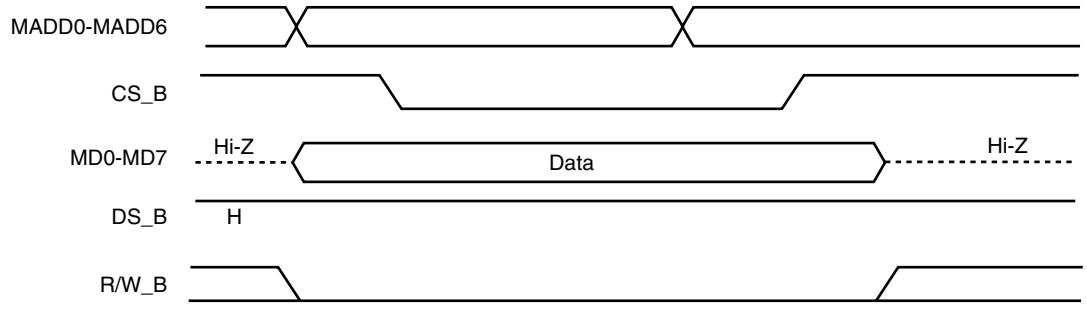
- **MSEL0 mode (Motorola compatible)**




- **MSEL1 mode (Intel compatible)**




- **S15 mode (MSEL pin = 0)**



### 4.3.3 Interrupt processing

The μPD98404 has an interrupt output pin PHINT_B. By using this pin, the μPD98404 reports detection of an error and occurrence of a counter overflow to the host.

The PHINT_B becomes active if one of the bits of the PHY interrupt cause register (PICR) is set to "1". When the host detects that PHINT_B has become active, it first reads the PICR register and identifies the interrupt cause. If the cause is PCO, ALM, or PFM, the host also reads the corresponding PCOCR, ACR, and PCR registers to check the cause of the interrupt.

Figure 4-25 shows the relationship of the registers to the interrupt cause. The user can mask each interrupt cause. Resetting the bit status of the interrupt cause register and the operation of the PHINT_B are performed in three modes when the host reads the PHY interrupt cause register. These modes are selected by using the RCM [1:0] bits of the mode register 2 (MDR2).

**(1) Selecting interrupt servicing mode (MDR2: RCM[1:0])**

- **Interrupt servicing mode 1 (MDR2: RCM[1:0] = "00")**
  If an interrupt is generated and one of the bits of the PICR register is set, PHINT_B becomes active. Even if the cause of the event no longer exists, the bit status of the register is maintained until the host reads the register, and the PHINT_B remains active. If the host reads the register when the cause of the interrupt no longer exists, the bit of the interrupt cause register is reset to 0 and the PHINT_B becomes inactive.
  In the example in Figure 4-24, the LOS bit of the PICR register is set and the PHINT_B becomes active because LOS is detected. The host reads the PICR register once. However, the LOS status still persists at this time, the LOS bit of the PICR register is not cleared, and the PHINT_B does not become inactive, either. Although a recovery is later made from the LOS status and the cause of the interrupt no longer exists, the current statuses of the LOS bit and PHINT_B are maintained because the host read the register under reset condition. When the host reads the register the second time, the LOS status no longer exists. Consequently, the register bit is reset and the PHINT_B becomes inactive at the same time.

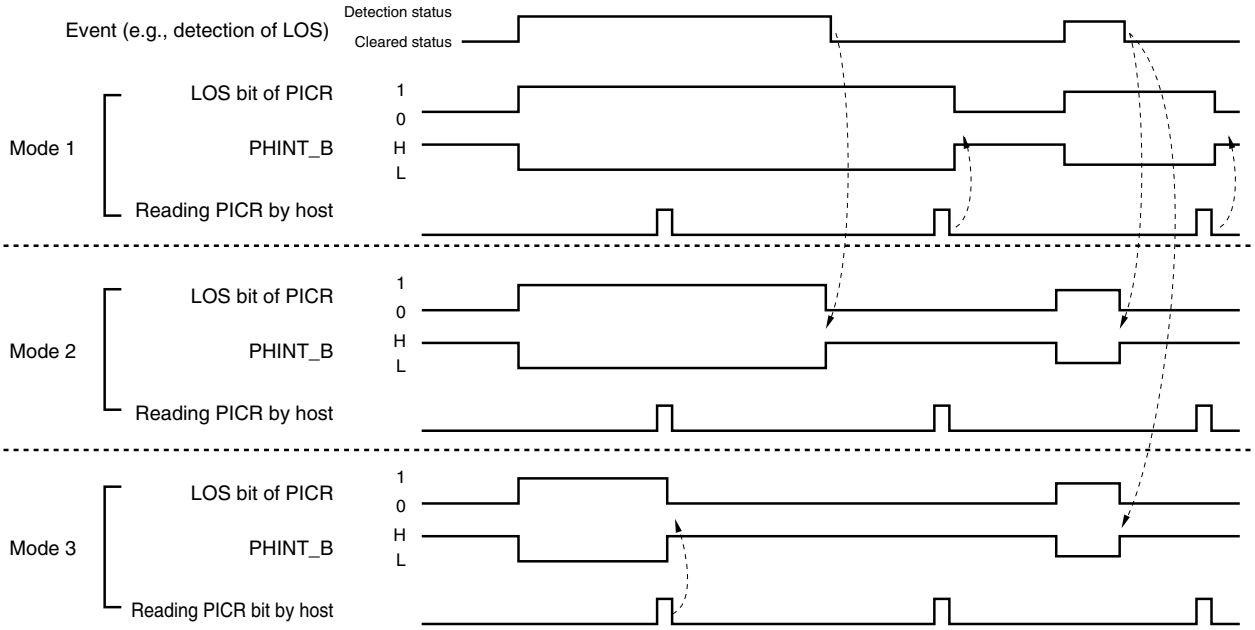
- **Interrupt servicing mode 2 (MDR2: RCM[1:0] = "01")**
  The bit of the interrupt cause register is reset and the PHINT_B becomes inactive only when an event that causes an interrupt is detected or recovered. Even if the host reads the PHY interrupt cause register, the bit of the register is not reset as long as the event continues, and the PHINT_B does not become inactive, either.

- **Interrupt servicing mode 3 (MDR2: RCM[1:0] = "1X")**
  The bit of the interrupt cause register is reset and the PHINT_B becomes inactive only if the event that causes an interrupt no longer exists or if the host reads the cause register. Even if the event continues, the bit of the register is reset and the PHINT_B becomes inactive if the host reads the register.

**Cautions 1. The bits of the register are cleared if the event of the source disappears in interrupt modes 2 and 3, so the bits may have been already cleared when the host reads the register.**

**2. Each cause bit may be set due to reception of an undefined frame immediately after power application to the μPD98404. After power application, therefore, clear all the interrupt cause registers to 0 by using the ICR bit of the command register 2 (CMR2).**

**Figure 4-24. Differences in Operation of Interrupt Cause Register Bit and PHINT_B due to Interrupt Mode**




Reset condition

Mode 1 : Register read by the host when interrupt cause no longer exists

Mode 2 : Interrupt cause no longer exists

Mode 3 : Interrupt cause no longer exists or register read by host

**Figure 4-25. Relationship between Interrupt Cause Registers**

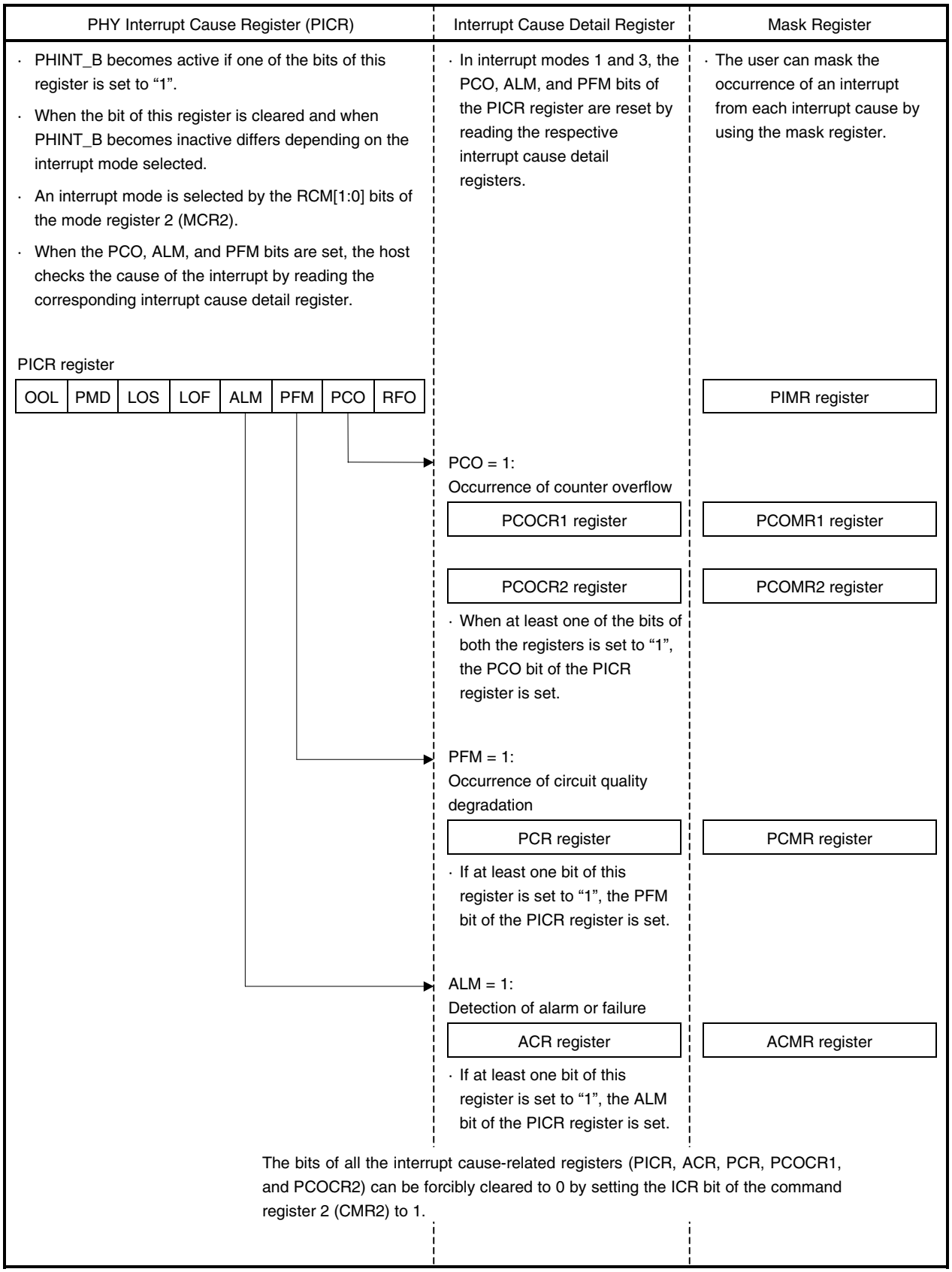


**Table 4-7. Setting/Resetting Condition of Each Bit of Interrupt Cause Registers**

| Register Name | Bit Name | Setting Condition | Resetting Condition | | |
|---|---|---|---|---|---|
| | | | RCM[1:0] bit = 00 | RCM[1:0] bit = 01 | RCM[1:0] bit = 1x |
| PICR | OOL<br>PMD<br>LOF<br>LOS | Occurrence of each interrupt | Reading of this register (on assumption that cause no longer exists) | Interrupt no longer exists | Reading of this register |
| | ALM | When one of bits of ACR register is set | All bits of ACR register are cleared to 0. | | |
| | PCO | When one of bits of PCOCR1 and PCOCR2 registers is set | All the bits of PCOCR1 and PCOCR2 registers are cleared to 0. | | |
| | PFM | When one of bits of PCR register is set | All bits of PCR register are cleared to 0. | | |
| | RFO | When receive buffer overrun occurs | Reading of this register only | | |
| PCOCR1 | B1EC<br>B2EC<br>B3EC<br>LREC | When count value passes all “FF” | Cleared to 0 by reading of this register | | |
| PCOCR2 | HECC<br>FULC<br>IDLC<br>INFC | When count value passes all “FF” | Cleared to 0 by reading of this register | | |
| ACR | OOF<br>LOP<br>OCD<br>LCD<br>LAIS<br>PAIS<br>LRDI<br>PRDI | Occurrence of each interrupt | Reading of this register (on assumption that interrupt no longer exists) | Interrupt no longer exists. | Reading of this register |
| PCR | FJ<br>B1E<br>B2E<br>B3E<br>LREI<br>PREI | Occurrence of each interrupt | Reading of this register (on assumption that interrupt no longer exists) | Interrupt no longer exists. | Reading of this register |

**Remark** Even if the ICR bit of the CMR register is set to 1, the bits of all the interrupt cause registers are reset.

# CHAPTER 5 REGISTERS

This chapter explains in detail the register map of the internal registers and the function of each register. The default value of each register is the value set after reset.

## 5.1 Register Map

| No. | Address | Name | Function | R/W | Number of Bits | Default Value |
|---|---|---|---|---|---|---|
| (1) | 00H | CMR1 | Command register 1. Sets transmission of alarm frame. | R/W | 5 | 00H |
| (2) | 01H | CMR2 | Command register 2. Sets initialization of register. | R/W | 4 | 00H |
| (3) | 02H | CMR3 | Command register 3. Sets transmission of pseudo error frame. | R/W | 4 | 00H |
| (4) | 03H | MDR1 | Mode register 1. Sets interface mode. | R/W | 8 | 00H |
| (5) | 04H | MDR2 | Mode register 2. Sets interrupt loopback mode. | R/W | 6 | 00H |
| (6) | 05H | MDR3 | Mode register 3. Sets scramble mode and TCLAV mode. | R/W | 7 | 00H |
| (7) | 06H | PICR | Indicates interrupt cause. | R | 7 | 00H |
| (8) | 07H | PIMR | Masks interrupt cause. | R/W | 7 | FFH |
| (9) | 08H | ACR | Indicates circuit failure interrupt cause detail. | R | 8 | 00H |
| (10) | 09H | ACMR | Masks circuit failure interrupt cause. | R/W | 8 | FFH |
| (11) | 0AH | PCR | Indicates performance monitoring interrupt cause detail. | R | 6 | 00H |
| (12) | 0BH | PCMR | Masks performance monitoring interrupt cause detail. | R/W | 6 | FFH |
| (13) | 0CH | IACM | Masks automatic transmission of Path/Line RDI. | R/W | 3 | FFH |
| (14) | 0DH | B1ECT | B1 error counter | R | 8 | 00H |
| (15) | 0EH | B2ECT | B2 error counter | R | 8 | 00H |
| (16) | 0FH | B3ECT | B3 error counter | R | 8 | 00H |
| (17) | 10H | LRECT | Line-REI counter | R | 8 | 00H |
| (18) | 11H | PRECT | Path-REI counter | R | 8 | 00H |
| (19) | 12H | FJCT | Frequency Justification counter | R | 8 | 00H |
| (20) | 13H | HECCT | Dropped cell counter in case of HEC error | R | 8 | 00H |
| (21) | 14H | FULCT | Dropped cell counter in case of FIFO full | R | 8 | 00H |
| (22) | 15H | IDLCT | Receive idle cell counter | R | 8 | 00H |
| (23) | 16H | INFCT | Reads receive valid cell counter | R | 8 | 00H |
| (24) | 19H | PCPR1 | Indicates read byte position of counter. | R/W | 8 | 00H |
| (25) | 1AH | PCPR2 | Indicates read byte position of counter. | R/W | 8 | 00H |
| (26) | 1BH | PCSR | Sets sample timing of counter to load register. | R/W | 1 | 00H |
| (27) | 1CH | PCIR1 | Sets initialization of counters (B1EC, B2EC, B3EC, LREC, PREC, FJC) | R/W | 6 | 00H |
| (28) | 1DH | PCIR2 | Sets initialization of counters (HECC, FULC, IDLC, INFC) | R/W | 4 | 00H |
| (29) | 1EH | PCFR1 | Disables counters (B1EC, B2EC, B3EC, LREC, PREC, FJC). | R/W | 6 | FFH |
| (30) | 1FH | PCFR2 | Disables counters (HECC, FULC, IDLC, INFC). | R/W | 4 | FFH |

| No. | Address | Name | Function | R/W | Number of Bits | Default Value |
|---|---|---|---|---|---|---|
| (31) | 20H | PCOCR1 | Indicates cause of counter overflow. | R | 6 | 00H |
| (32) | 21H | PCOCR2 | Indicates cause of counter overflow. | R | 4 | 00H |
| (33) | 22H | PCOMR1 | Masks interrupt due to counter overflow. | R/W | 6 | FFH |
| (34) | 23H | PCOMR2 | Masks interrupt due to counter overflow. | R/W | 4 | FFH |
| (35) | 24H | AMPR | Selects PHYALM pin to be set. | R/W | 2 | 00H |
| (36) | 25H | AMR1 | Masks alarm to be output from PHYARM pin. | R/W | 8 | FFH |
| (37) | 26H | AMR2 | Masks alarm to be output from PHYARM pin. | R/W | 4 | FFH |
| (38) | 27H | DCHPR | Sets drop cell header pattern. | R/W | 1 | 01H |
| (39) | 28H | DCHPMR | Masks drop cell header pattern. | R/W | 1 | 00H |
| (40) | 29H | PHYIDR | Sets PHY ID address when multi-PHY mode is used. | R/W | 5 | 01H |
| (41) | 2AH | J0R | Stores J0 byte of receive frame. | R | 8 | 00H |
| (42) | 2BH | Z01 | Stores 1st Z0 byte of receive frame. | R | 8 | 00H |
| (43) | 2CH | Z02 | Stores 2nd Z0 byte of receive frame. | R | 8 | 00H |
| (44) | 2DH | F1R | Stores F1 byte of receive frame. | R | 8 | 00H |
| (45) | 2EH | K1R | Stores K1 byte of receive frame. | R | 8 | 00H |
| (46) | 2FH | K2R | Stores K2 byte of receive frame. | R | 8 | 00H |
| (47) | 30H | C2R | Stores C2 byte of receive frame. | R | 8 | 00H |
| (48) | 31H | F2R | Stores F2 byte of receive frame. | R | 8 | 00H |
| (49) | 32H | H4R | Stores H4 byte of receive frame. | R | 8 | 00H |
| (50) | 33H | J0T | Sets J0 byte of transmit frame. | R/W | 8 | 01H |
| (51) | 34H | Z01T | Sets 1st Z0 byte of transmit frame. | R/W | 8 | 02H |
| (52) | 35H | Z02T | Sets 2nd Z0 byte of transmit frame. | R/W | 8 | 03H |
| (53) | 36H | F1T | Sets F1 byte of transmit frame. | R/W | 8 | 00H |
| (54) | 37H | K1T | Sets K1 byte of transmit frame. | R/W | 8 | 00H |
| (55) | 38H | K2T | Sets K2 byte of transmit frame. | R/W | 5 | 00H |
| (56) | 39H | C2T | Sets C2 byte of transmit frame. | R/W | 8 | 13H |
| (57) | 3AH | F2T | Sets F2 byte of transmit frame. | R/W | 8 | 00H |
| (58) | 3BH | H4T | Sets H4 byte of transmit frame. | R/W | 8 | 00H |
| (59) | 3CH-3EH | Reserved area (read/write prohibited) | | | | |
| (60) | 3FH | VERR | Stores version name of LSI. | R | 8 | 00H |
| (61) | 40H-7FH | Reserved area (read/write prohibited) | | | | |

**[Caution]**

The data bit string of the SONET/SDH frame the μPD98404 transmits from the PMD interface is sequentially transmitted starting from the MSB. Note that the names of the bits in the byte in the overhead of the SONET/SDH frame are described in two ways in this manual, as follows:

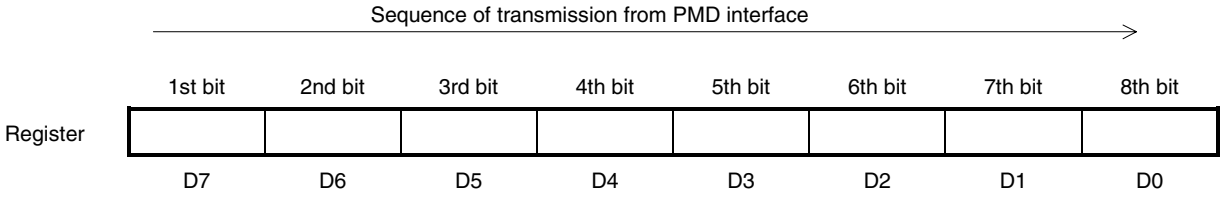
**(1) First through eighth bits**

These bits are mainly used to indicate the bit string of the overhead byte in the SONET/SDH frame and are in the sequence in which they are output from the PMD interface.

**(2) D7 through D0 bits**

These bits are mainly used to indicate the bits in the internal registers of the μPD98404 and correspond to the D7 through D0 pins of the external management interface.

- Expressing bits in internal registers



## 5.2 Register Function

### (1) Command register (CMR1)

This register sets transmission of alarm signals such as Line AIS, Path AIS, Line RDI, and Path RDI. It also sets the PHYALM pin output.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CMR1 | 0 | 0 | 0 | ARM | LAIS | PAIS | LRDI | PRDI | 00H | 00H | R/W |

| Field | Function | | Default Value |
|---|---|---|---|
| D4: ARM | Sets the output level of the PHYALM[2:0] pins not masked by the AMR1/2 registers. | | 0 |
| | 1 | Outputs high level to PHYALM[2:0] pins. | |
| | 0 | Does not set PHYALM output. | |
| D3: LAIS | Sets Line AIS transmission. | | 0 |
| | 1 | Transmits Line AIS transmission. Sets K2 (bits 6 through 8) of transmit frame to “111” and changes all bits of transmit frame to 1 before scrambling POH and payload block. | |
| | 0 | Does not set Line AIS. | |
| D2: PAIS | Sets Path AIS transmission. | | 0 |
| | 1 | Transmits Path AIS transmission. Sets all bits of H1 through H3 of transmit frame to “1” and changes all bits in payload area of transmit frame to 1. | |
| | 0 | Does not set Path AIS. | |
| D1: LRDI | Sets Line RDI transmission. | | 0 |
| | 1 | Transmits Line RDI transmission. Changes K2 byte (bits 6 through 8) of transmit frame to “110”. | |
| | 0 | Does not set Line RDI. | |
| D0: PRDI | Sets Path RDI transmission. | | 0 |
| | 1 | Transmits Path RDI transmission. Changes bit 5 of G1 byte of transmit frame to “1”. | |
| | 0 | Does not set Path RDI. | |

**Remarks 1.** If Line AIS and Line RDI are set in the same frame, Line AIS takes precedence.

**2.** When this register is read, the high-order 3 bits are always “0”. Nothing can be written to these bits.

**(2) Command register 2 (CMR2)**

This register initializes the registers of the μPD98404.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CMR2 | 0 | 0 | 0 | 0 | ALL | ICR | PCR | ALR | 01H | 00H | R/W |

| Field | Function | | Default Value |
|---|---|---|---|
| D3: ALL | Software reset of LSI | | 0 |
| | 1 | Executes software reset. Initializes all internal states of this LSI. | |
| | 0 | Does not execute software reset. | |
| D2: ICR | Initializes all interrupt cause registers. | | 0 |
| | 1 | Initializes all interrupt cause registers (PICR, ACR, PCR, and PCOCR) and the mask register (PIMR, ACMR, PCMP, PCOMR). | |
| | 0 | Does not initialize interrupt cause registers. | |
| D1: PCR | Initializes all performance counters. | | 0 |
| | 1 | Initializes all performance counters and registers related to performance counters. | |
| | 0 | Does not initialize performance counters and registers related to performance counters. | |
| D0: ALR | Initializes all registers. | | 0 |
| | 1 | Initializes all registers of LSI to default values. | |
| | 0 | Does not initialize registers. | |

**Caution If the device is reset via software by setting this register, do not read or write all the registers for the duration of at least "20 x TCLK clock cycle ($t_{CYTK}$)" from that write cycle. Otherwise, the registers may not be read or written correctly.**

**Remarks 1.** All bits are automatically cleared to "0" after they have been initialized.

**2.** When this register is read, the high-order 4 bits are always "0". Nothing can be written to these bits.

**(3) Command register 3 (CMR3)**

This register transmits a frame including an alarm signal or error report. This function allows the user to forcibly transmit a pseudo frame including an error report. This register is useful for testing.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CMR3 | 0 | 0 | 0 | 0 | CM3 | CM2 | CM1 | CM0 | 02H | 00H | R/W |

| Field | Function | Default Value |
|---|---|---|
| D3-D0: CM3-CM0 | Transmits pseudo error frame including alarm or error | All 0 |

| CM3-CM0 | Transmit frame |
|---|---|
| 0000 | Transmits normal frame. |
| 0001 | Transmits LOS frame. |
| 0010 | Transmits OOF frame. |
| 0011 | Transmits LOF frame. |
| 0100 | Transmits LOP frame. |
| 0101 | Transmits OCD frame. |
| 0110 | Transmits LCD frame. |
| 0111 | Transmits B1 error frame. |
| 1000 | Transmits B2 error frame. |
| 1001 | Transmits B3 error frame. |
| 1010 | Transmits Line REI frame. |
| 1011 | Transmits Path REI frame. |
| Others | Transmits normal frame. |

**Remark** When this register is read, the high-order 4 bits are always “0”. Nothing can be written to these bits.

### (4) Mode register 1 (MDR1)

This register sets the mode of the line interface or UTOPIA interface.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MDR1 | 0 | SS1 | SS0 | TxCL1 | TxCL0 | 0 | CSEL | HSEL | 03H | 00H | R/W |

| Field | Function | Default Value |
|---|---|---|
| D6, D5: SS1, SS0 | Sets SS bit code of 1st to 3rd H1 bytes of overhead of transmit frame. | 00 |

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| 1st H1 | 0 | 1 | 1 | 0 | SS1 | SS0 | 1 | 0 |
| 2nd H1 | 1 | 0 | 0 | 1 | SS1 | SS0 | 1 | 1 |
| 3rd H1 | 1 | 0 | 0 | 1 | SS1 | SS0 | 1 | 1 |

| Field | Function | Default Value |
|---|---|---|
| D4, D3: TxCL1, TxCL0 | Selects reference clock used by transmit synthesizer as source clock. | 00 |

| TxCL[1:0] | Mode |
|---|---|
| 00 | Uses REFCLK pin input as reference clock of transmit synthesizer PLL. |
| 10 | Uses TFC pin input as reference clock of transmit synthesizer PLL. |
| X1 | Uses recovery clock of receive clock recovery PLL as transmit clock as is. |

| Field | | | Default Value |
|---|---|---|---|
| D1: CSEL | Selects mode of ATM layer interface when UMPSEL pin = L (single PHY). | | 0 |
| | 1 | Selects cell level handshake mode. | |
| | 0 | Selects octet level handshake mode. | |
| D0: HSEL | Uses recovery clock of receive clock recovery PLL as transmit clock as is. | | 0 |
| | 1 | Selects 3-state mode for RDO & RSOC output. | |
| | 0 | Selects 2-state mode for RDO & RSOC output. | |

**Remark** When this register is read, bits D7 and D2 are always “0”. Nothing can be written to these bits.

**Table 5-1. ATM Layer Interface Modes Selected by Combination of CSEL and HSEL Bits and UMPSEL Pin**

| D1, D0 | UMPSEL Pin | Mode |
|---|---|---|
| 00 | 0 | Single PHY; octet level handshake; RDI [7:0] & RSOC 2-state (default) |
| 01 | | Single PHY; octet level handshake; RDI [7:0] & RSOC 3-state |
| 10 | | Single PHY; cell level handshake; RDO [7:0] & RSOC 2-state |
| 11 | | Single PHY; cell level handshake; RDO [7:0] & RSOC 3-state |
| XX | 1 | Multi-PHY; RDO [7:0], RSOC, RCLAV & TCLAV 3-state |

### (5) Mode register 2 (MDR2)

This register selects the mode of the μPD98404.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MDR2 | 0 | oolenb | idlenb | LP1 | LP0 | RxCL | RCM1 | RCM0 | 04H | 00H | R/W |

| Field | Function | | Default Value |
|---|---|---|---|
| D6: oolenb | Disable receive clock automatic selection in OOL status. | | 0 |
| | 1 | Transmit clock is not automatically switched to receive clock even in OOL status. | |
| | 0 | Transmit clock is automatically switched to receive clock if receive clock recovery PLL is unlocked (OOL status). | |
| D5: idenb | Selects format of vacant cell. | | 0 |
| | 1 | Inserts unassigned cell as vacant cell. | |
| | 0 | Inserts idle cell as vacant cell. | |
| D4: LP1<br>D3: LP0 | Sets loopback mode | | 00 |

| LP[1:0] | Mode |
|---|---|
| 00 | Sets normal mode |
| 01 | RPLP mode<br>Sets loopback from PMD side input to PMD side output via serial/parallel converter circuit |
| 10 | TPLP mode<br>Sets loopback from ATM side input to ATM side output via serial/parallel converter circuit |
| 11 | ATMLP mode<br>Sets loopback from ATM side input to ATM side output via receive FIFO and transmit FIFO |

| | | | |
|---|---|---|---|
| D2: RxCL | Selects source clock of receive clock recovery PLL circuit | | 0 |
| | 1 | Selects source of receive clock. Uses clock generated by transmit synthesizer PLL as receive clock. | |
| | 0 | Uses clock extracted by receive clock recovery PLL as receive clock. | |

**Caution The oolenb bit disables the function automatically to select the source of the receive clock. Set this bit to 1 (refer to Caution in • Receive clock recovery PLL function in 4.2.1 (1)).**

<table>
<tr><th>Field</th><th>Function</th><th>Default Value</th></tr>
<tr><td>D1: RCM1<br>D0: RCM0</td><td>Selects interrupt mode<br><br><table><tr><th>RCM [1:0]</th><th>Mode</th></tr><tr><td>00</td><td>Selects interrupt mode 1.<br>Bits of interrupt cause register and PHINT_B signal are retained until they are read by host. Even if cause condition disappears, status bit is retained.</td></tr><tr><td>01</td><td>Selects interrupt mode 2.<br>Even if host reads PHY interrupt cause register, bit is not reset and PHINT_B signal does not become inactive. Status is retained until cause disappears.</td></tr><tr><td>1X</td><td>Selects interrupt mode 3.<br>When host reads interrupt cause register, register bits are reset even if cause condition is still valid, and PHINT_B signal becomes inactive.</td></tr></table></td><td>00</td></tr>
</table>

**Remark** When this register is read, the most significant bit is always “0”. Nothing can be written to this bit.

### (6) Mode register 3 (MDR3)

This register is used to select the mode of the μPD98404.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MDR3 | INTENB | FSCRM | CSCRM | HECENB | CORENB | RCASEL | TCASEL1 | TCASEL0 | 05H | 00H | R/W |

| Field | Function | | Default Value |
|---|---|---|---|
| D7: INTENB | Selects cell synchronization status transition. | | 0 |
| | 1 | Cell does not enter hunting status if circuit fault (OOF, LOP, P-AIS) becomes active. | |
| | 0 | Cell is forcibly set in hunting status and then OCD status if circuit fault (OOF, LOP, P-AIS) becomes active. | |
| D6: FSCRM | Selects frame scramble/descramble mode. | | 0 |
| | 1 | Does not execute frame scramble/descramble. | |
| | 0 | Executes frame scramble/descramble. | |
| D5: CSCRM | Selects cell scramble/descramble mode. | | 0 |
| | 1 | Does not execute cell scramble/descramble. | |
| | 0 | Executes cell scramble/descramble. | |
| D4: HECENB | Selects HEC error cell drop mode. | | 0 |
| | 1 | Does not drop cell in which HEC error is detected. | |
| | 0 | Drops cell in which HEC error is detected. | |
| D3: CORENB | Selects HEC error correction mode. | | 0 |
| | 1 | Does not correct 1-bit HEC error. Cell in which 1-bit HEC error is detected is dropped. | |
| | 0 | Corrects 1-bit HEC error. | |
| D2: RCASEL | Selects operation mode of RCLAV signal of UTOPIA interface. | | 0 |
| | 1 | Indicates whether there is 1 cell of valid data at the next clock after the one that outputs second byte (header second byte) of receive cell data. | |
| | 0 | Indicates whether there is 1 cell of valid data at the next clock after the one that outputs last byte of receive cell data (48th byte of payload). | |

**Caution There are limitations on the RCASEL = 1 mode. For details, refer to CHAPTER 8 CONSTRAINTS.**

<table>
<tr><th>Field</th><th>Function</th><th>Default Value</th></tr>
<tr><td>D1: TCASEL1<br>D0: TCASEL0</td><td>Selects operation mode of TCLAV signal of UTOPIA interface.<br><br><table><tr><th>TCASEL[1:0]</th><th>TCLAV asserting/deasserting timing</th></tr><tr><td>00</td><td>Reports whether one more cell of data can be received by asserting TCLAV active four cycles before transfer of cell data currently being received is completed.</td></tr><tr><td>01</td><td>Indicates whether two more cell data can be accepted 4 cycles before transfer of currently accepted cell is completed.</td></tr><tr><td>10</td><td>Reports whether one more cell of data can be received by asserting TCLAV active after H3 byte of the cell data currently being received.</td></tr><tr><td>11</td><td>Indicates whether two more cell data can be accepted 1 cycle before transfer of currently accepted cell is completed.</td></tr></table><br>Caution Select a mode by using TCASEL[1:0] only in the cell level handshake mode (CSEL bit = 1). In the octet level handshake mode (CSEL bit = 0), make sure that TCASEL[1:0] = 00 (default).</td><td>00</td></tr>
</table>

### (7) PHY interrupt cause register (PICR)

This register indicates the cause of an interrupt request (output from the PHINT_B pin).

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PICR | OOL | PMD | LOS | LOF | ALM | PFM | PCO | RFO | 06H | 00H | R |

| Field | Function | | Default Value |
|---|---|---|---|
| D7: OOL | Indicates status of receive clock recovery PLL. | | 0 |
| | 1 | Indicates that recovery PLL is not correctly extracting the clock. | |
| | 0 | Indicates that recovery PLL is correctly extracting the clock. | |
| D6: PMD | Status of PMDALM pin input. | | 0 |
| | 1 | Indicates that PMDALM pin input is high. | |
| | 0 | Indicates that PMDALM pin input is low. | |
| D5: LOS | Indicates LOS (Loss Of Signal) status. | | 0 |
| | 1 | Indicates that LOS has occurred. | |
| | 0 | Indicates that LOS does not occur. | |
| D4: LOF | Indicates LOF (Loss Of Frame) status. | | 0 |
| | 1 | Indicates that LOF has occurred. | |
| | 0 | Indicates that LOF does not occur. | |
| D3: ALM | Indicates ACR register status. | | 0 |
| | 1 | Indicates that circuit failure (OOF, LOP, OCD, LCD, Line AIS, Path AIS, Line RDI, Path RDI) of ACR register has occurred. | |
| | 0 | Indicates that circuit failure of ACR register has not occurred. | |
| D2: PFM | Indicates status of PCR register. | | 0 |
| | 1 | Indicates that detailed performance interrupt (Frequency justification, B1E, B2E, B3E, Line REI, Path REI) indicated by PCR has been detected. | |
| | 0 | Indicates that detailed performance interrupt indicated by PCR has not been detected | |
| D1: PCO | Status of performance counters. | | 0 |
| | 1 | Indicates that overflow has occurred in performance counters. | |
| | 0 | Indicates that overflow has not occurred in performance counters. | |
| D0: RFO | Indicates overflow of receive FIFO. | | 0 |
| | 1 | Indicates that overflow has occurred in receive FIFO. | |
| | 0 | Indicates that overflow has not occurred in receive FIFO. | |

**Remarks 1.** If even one of the bits of this register not masked by the PIMR register is set to "1", PHINT_B is asserted active.

**2.** The operations of the OOL, PMD, LOF, and LOS bits of this register differ depending on the setting of the mode register 2 (MDR2) (RCM1 and RCM0 bits).

### (8) PHY interrupt mask register (PIMR)

This register masks each interrupt cause of PICR (06H).

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PIMR | OOL | PMD | LOS | LOF | ALM | PFM | PCO | RFO | 07H | FFH | R/W |

| Field | Function | | Default Value |
|---|---|---|---|
| D7: OOL | Masks or unmasks interrupt request on occurrence of OOL. | | 1 |
| | 1 | Masks interrupt on occurrence of OOL. | |
| | 0 | Does not mask interrupt on occurrence of OOL. | |
| D6: PMD | Masks/unmasks interrupt request due to occurrence of PMD alarm. | | 1 |
| | 1 | Masks interrupt request due to change in PMDALM pin input. | |
| | 0 | Does not mask interrupt request due to change in PMDALM pin input. | |
| D5: LOS | Masks/unmasks interrupt request due to occurrence of LOS. | | 1 |
| | 1 | Masks interrupt request due to occurrence of LOS. | |
| | 0 | Does not mask interrupt request due to occurrence of LOS. | |
| D4: LOF | Masks/unmasks interrupt request due to occurrence of LOF. | | 1 |
| | 1 | Masks interrupt request due to occurrence of LOF. | |
| | 0 | Does not mask interrupt request due to occurrence of LOF. | |
| D3: ALM | Masks/unmasks interrupt request due to occurrence of circuit failure. | | 1 |
| | 1 | Masks interrupt request due to circuit failure (OOF, LOP, OCD, LCD, Line AIS, Path AIS, Line RDI, Path RDI) indicated by ACR register (Address: 08H). | |
| | 0 | Masks interrupt request due to circuit failure indicated by ACR (Alarm Cause Register, Address: 08H). | |
| D2: PFM | Masks/unmasks interrupt request due to occurrence of detailed performance interrupt. | | 1 |
| | 1 | Masks interrupt request due to detailed performance interrupt (B1EC, B2EC, B3EC, LREC, PREC, FJC, HECC, FULC, IDLC, INFC) indicted by PCR register (Address: 0AH). | |
| | 0 | Does not mask interrupt request due to detailed performance interrupt indicated by PCR. | |
| D1: PCO | Masks/unmasks interrupt request due to occurrence of overflow in performance counter. | | 1 |
| | 1 | Masks interrupt request due to occurrence of overflow in performance counter. | |
| | 0 | Does not mask interrupt request due to occurrence of overflow in performance counter. | |
| D0: RFO | Masks/unmasks interrupt request due to occurrence of overflow in receive FIFO. | | 1 |
| | 1 | Masks interrupt request due to occurrence of overflow in receive FIFO. | |
| | 0 | Does not mask interrupt request due to occurrence of overflow in receive FIFO. | |

### (9) Alarm cause register (ACR)

This register indicates a circuit failure.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ACR | OOF | LOP | OCD | LCD | LAIS | PAIS | LRDI | PRDI | 08H | 00H | R |

| Field | Function | | Default Value |
|---|---|---|---|
| D7: OOF | Status of OOF (Out Of Frame). | | 0 |
| | 1 | Indicates that OOF has occurred. | |
| | 0 | Indicates that OOF has not occurred. | |
| D6: LOP | Status of LOP (Loss Of Pointer). | | 0 |
| | 1 | Indicates that LOP has occurred. | |
| | 0 | Indicates that LOP has not occurred. | |
| D5: OCD | Indicates OCD (Out of Cell Delineation). | | 0 |
| | 1 | Indicates that OCD has occurred. | |
| | 0 | Indicates that OCD has not occurred. | |
| D4: LCD | Status of LCD (Loss of Cell Delineation). | | 0 |
| | 1 | Indicates that LCD has occurred. | |
| | 0 | Indicates that LCD has not occurred. | |
| D3: LAIS | Status of Line AIS. | | 0 |
| | 1 | Indicates that Line AIS has occurred. | |
| | 0 | Indicates that Line AIS has not occurred. | |
| D2: PAIS | Status of Path AIS. | | 0 |
| | 1 | Indicates that Path AIS has occurred. | |
| | 0 | Indicates that Path AIS has not occurred. | |
| D1: LRDI | Status of Line RDI. | | 0 |
| | 1 | Indicates that Line RDI has occurred. | |
| | 0 | Indicates that Line RDI has not occurred. | |
| D0: PRDI | Status of Path RDI. | | 0 |
| | 1 | Indicates that Path RDI has occurred. | |
| | 0 | Indicates that Path RDI has not occurred. | |

**Caution The LOP bit is not cleared when the status of the pointer changes from LOP to AIS. To identify LOP in software, include clearing of the P-AIS bit to 0 into the condition (refer to Figure 3-7 Pointer Status Transition).**

**Remarks 1.** If even one of the bits of this register not masked by the ACMR register is set to "1", PICR (address: 06H) ALM bit is set to 1. Even if a bit masked by the ACMR register is set, the ALM bit is not set to 1.

**2.** The operation of this register is controlled by mode register 2 (MDR2) (bits RCM1 and RCM0).

**(10) Alarm cause mask register (ACMR)**

This register can mask the circuit failure causes of ACR (Address: 08H). When they are masked, the ALM bit of PICR (Address: 06H) is not set.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ACMR | OOF | LOP | OCD | LCD | LAIS | PAIS | LRDI | PRDI | 09H | FFH | R/W |

| Field | Function | | Default Value |
|---|---|---|---|
| D7: OOF | Masks report on detection of OOF (Out Of Frame). | | 1 |
| | 1 | Masks report on occurrence of OOF. | |
| | 0 | Does not mask report on occurrence of OOF. | |
| D6: LOP | Masks report on detection of LOP (Loss Of Pointer). | | 1 |
| | 1 | Masks report on occurrence of LOP. | |
| | 0 | Does not mask report on occurrence of LOP. | |
| D5: OCD | Masks report on detection of OCD (Out of Cell Delineation). | | 1 |
| | 1 | Masks report on occurrence of OCD. | |
| | 0 | Does not mask report on occurrence of OCD. | |
| D4: LCD | Masks report on detection of LCD (Loss of Cell Delineation). | | 1 |
| | 1 | Masks report on occurrence of LCD. | |
| | 0 | Does not mask report on occurrence of LCD. | |
| D3: LAIS | Masks report on detection of Line AIS. | | 1 |
| | 1 | Masks report on occurrence of Line AIS. | |
| | 0 | Does not mask report on occurrence of Line AIS. | |
| D2: PAIS | Masks report on detection of Path AIS. | | 1 |
| | 1 | Masks report on occurrence of Path AIS. | |
| | 0 | Does not mask report on occurrence of Path AIS. | |
| D1: LRDI | Masks report on detection of Line RDI. | | 1 |
| | 1 | Masks report on occurrence of Line RDI. | |
| | 0 | Does not mask report on occurrence of Line RDI. | |
| D0: PRDI | Masks report on detection of Path RDI. | | 1 |
| | 1 | Masks report on occurrence of Path RDI. | |
| | 0 | Does not mask report on occurrence of Path RDI. | |

### (11) Performance cause register (PCR)

This register indicates causes of performance interrupt.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCR | 0 | 0 | FJ | B1E | B2E | B3E | LREI | RREI | 0AH | 00H | R |

| Field | Function | | Default Value |
|---|---|---|---|
| D5: FJ | Status of JF (Frequency Justification). | | 0 |
| | 1 | Indicates that FJ has occurred. | |
| | 0 | Indicates that FJ has not occurred. | |
| D4: B1E | Status of B1 error. | | 0 |
| | 1 | Indicates that B1 error has occurred. | |
| | 0 | Indicates that B1 error has not occurred. | |
| D3: B2E | Status of B2 error. | | 0 |
| | 1 | Indicates that B2 error has occurred. | |
| | 0 | Indicates that B2 error has not occurred. | |
| D2: B3E | Status of B3 error. | | 0 |
| | 1 | Indicates that B3 error has occurred. | |
| | 0 | Indicates that B3 error has not occurred. | |
| D1: LREI | Status of Line REI. | | 0 |
| | 1 | Indicates that Line REI has occurred. | |
| | 0 | Indicates that Line REI has not occurred. | |
| D0: PREI | Status of Path REI. | | 0 |
| | 1 | Indicates that Path REI has occurred. | |
| | 0 | Indicates that Path REI has not occurred. | |

**Remarks 1.** When this register is read, the high-order 2 bits are always “0”. Nothing can be written to these bits.

**2.** Even if one of the bits of this register not masked by the PCMR register is set to “1”, PICR (address: 06H) PFM bit is set to 1. Even if a bit masked by the PCMR register is set to 1, the PFM bit is not set to 1.

**3.** The operation of this register is controlled by mode register 2 (MDR2) (bits RCM1 and RCM0).

**(12) Performance cause mask register (PCMR)**

This register can mask the causes of performance interrupt of PCR (Address: 0A). When they are masked, the PFM bit of PICR (Address: 06H) is not set.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCMR | 1 | 1 | FJ | B1E | B2E | B3E | LREI | PREI | 0BH | FFH | R/W |

| Field | Function | | Default Value |
|---|---|---|---|
| D5: FJ | Masks report on occurrence of FJ (Frequency Justification). | | 1 |
| | 1 | Masks report on occurrence of FJ. | |
| | 0 | Does not mask report on occurrence of FJ. | |
| D4: B1E | Masks report on occurrence of B1 error. | | 1 |
| | 1 | Masks report on occurrence of B1 error. | |
| | 0 | Does not mask report on occurrence of B1 error. | |
| D3: B2E | Masks report on occurrence of B2 error. | | 1 |
| | 1 | Masks report on occurrence of B2 error. | |
| | 0 | Does not mask report on occurrence of B2 error. | |
| D2: B3E | Masks report on occurrence of B3 error. | | 1 |
| | 1 | Masks report on occurrence of B3 error. | |
| | 0 | Does not mask report on occurrence of B3 error. | |
| D1: LREI | Masks report on occurrence of Line REI. | | 1 |
| | 1 | Masks report on occurrence of Line REI. | |
| | 0 | Does not mask report on occurrence of Line REI. | |
| D0: PREI | Masks report on occurrence of Path REI. | | 1 |
| | 1 | Masks report on occurrence of Path REI. | |
| | 0 | Does not mask report on occurrence of Path REI. | |

**Remark** When this register is read, the high-order 2 bits are always “1”. Nothing can be written to these bits.

### (13) Internal alarm cause mask register (IACM)

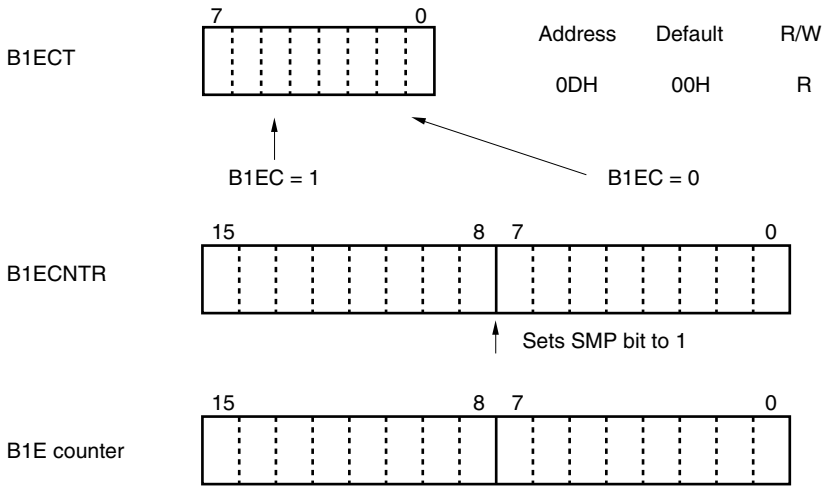
This register can mask transmission of an alarm frame that is automatically generated internally.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| IACM | 1 | 1 | 1 | 1 | 1 | PMD | LRDI | PRDI | 0CH | FFH | R/W |

| Field | Function | | Default Value |
|---|---|---|---|
| D2: PMD | Masks “PMDALM”. | | 1 |
| | 1 | Only the input level of the PMDALM pin is reflected on the PMD bit of the PICR register. This is not included in the condition for detecting LOS. | |
| | 0 | The input level of this pin is included in the condition for detecting LOS. The input level of this pin is reflected on the PMD bit of the PICR register. If it is high, LOS is detected. This field is set when the optical input cutoff signal output by an optical module is input. | |
| D1: LRDI | Masks automatic transmission of Line RDI. | | 1 |
| | 1 | Masks transmission of Line RDI automatically generated internally. | |
| | 0 | Does not mask transmission of Line RDI automatically generated internally. | |
| D0: PRDI | Masks automatic transmission of Path RDI. | | 1 |
| | 1 | Masks transmission of Path RDI automatically generated internally. | |
| | 0 | Does not mask transmission of Path RDI automatically generated internally. | |

**Remark** When this register is read, the high-order 5 bits are always “1”. Nothing can be written to these bits.

### (14) B1 error count register (B1ECT)



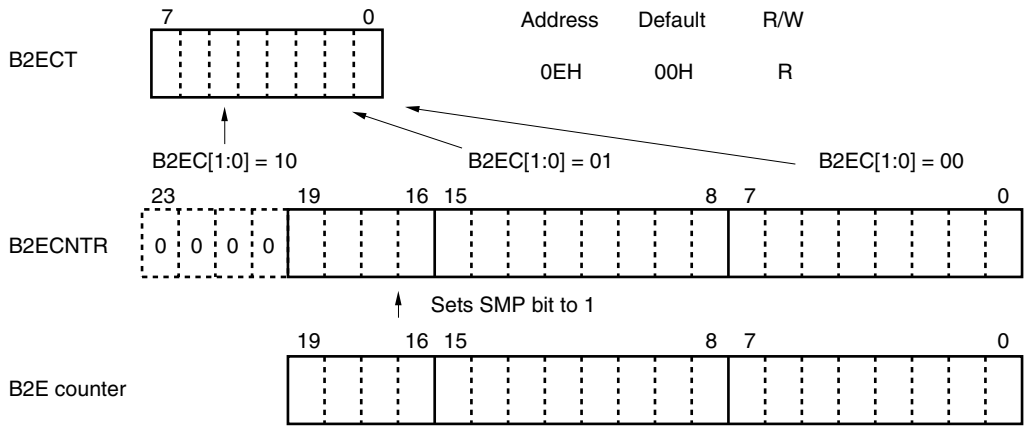

This register is a window register that is used to read the value of the 16-bit B1ECNTR register in 8-bit units. When this register read, the low-order 8 bits of B1ECNTR [7:0] are read first, and then the high-order 8 bits of B1ECNTR [15:8] are read. Whether the low-order or high-order 8 bits of B1ECNTR are read when this register is read next time is indicated by the B1EC bit of the PCPR1 register (address: 19H). The default value of the B1EC bit of the PCPR1 register is 0. Each time the B1ECT register has been read, the B1EC bit automatically changes from 0 to 1 and then back to 0 again.

The B1ECNTR register is a load register that samples (stores) the value of the B1 error counter. When the SMP bit of the PCSR register (1BH) is set to 1, the value of the B1E counter is stored to the B1ECNTR register This value indicates the total of the number of B1 errors that have occurred after the contents of the B1E counter have been previously sampled. The value stored to the B1ECNTR register is retained until the B1E counter is sampled again.

The contents of the B1E counter are cleared to 0 each time the counter has been sampled. The counter is also cleared when 1 is written to the B1EC bit of the PCIR1 (1CH) register.

When the value of the counter reaches all “F”, an overflow is detected and the B1EC bit of PCOCR1 (20H) is set to 1. In addition, the PCO bit of the PICR (06H) register is set to 1, causing an interrupt. Even after an overflow occurs, the B1E counter continues counting up.

### (15) B2 error count register (B2ECT)



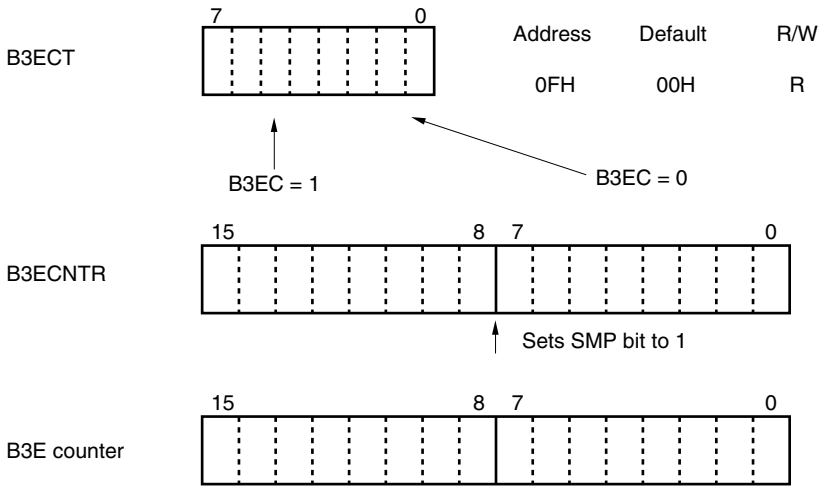

This register is a window register that is used to read the value of the 20-bit B2ECNTR register in three parts of 8 bits each. When this register read, the low-order 8 bits of B2ECNTR [7:0] are read first, the middle-order 8 bits of B2ECNTR [15:8], and then the high-order 4 bits of B2ECNTR [19:15] are read. Whether the low-order or middle-order 8 bits or high-order 4 bits of B2ECNTR are read when this register is read next time is indicated by the B2EC1 and B2EC0 bits of the PCPR1 register (address: 19H). The default values of these bits are 00. Each time the B2ECT register has been read, these bits automatically change from 00 to 01, from 01 to 10, from 10 to 00, and so on.

The B2ECNTR register is a load register that samples (stores) the value of the B2 error counter. When the SMP bit of the PCSR register (1BH) is set to 1, the value of the B2E counter is stored to the B2ECNTR register. This value indicates the total of the number of B2 errors that have occurred after the contents of the B2E counter have been previously sampled. The value stored to the B2ECNTR register is retained until the B2E counter is sampled again.

The contents of the B2E counter are cleared to 0 each time the counter has been sampled. The counter is also cleared when 1 is written to the B2EC bit of the PCIR1 (1CH) register.

When the value of the counter reaches all “F”, an overflow is detected and the B2EC bit of PCOCR1 (20H) is set to 1. In addition, the PCO bit of the PICR (06H) register is set to 1, causing an interrupt. Even after an overflow occurs, the B2E counter continues counting up.

### (16) B3 error count register (B3ECT)



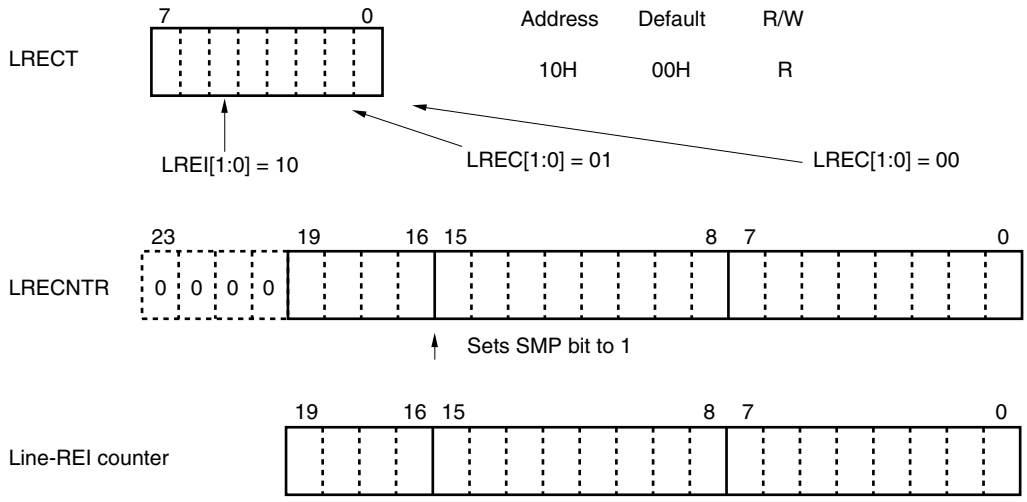

This register is a window register that is used to read the value of the 16-bit B3ECNTR register in 8-bit units. When this register read, the low-order 8 bits of B3ECNTR [7:0] are read first, and then the high-order 8 bits of B3ECNTR [15:8] are read. Whether the low-order or high-order 8 bits of B3ECNTR are read when this register is read next time is indicated by the B3EC bit of the PCPR1 register (address: 19H). The default value of the B3EC bit of the PCPR1 register is 0. Each time the B3ECT register has been read, the B3EC bit automatically changes from 0 to 1 and then back to 0 again.

The B3ECNTR register is a load register that samples (stores) the value of the B3 error counter. When the SMP bit of the PCSR register (1BH) is set to 1, the value of the B3E counter is stored to the B3ECNTR register This value indicates the total of the number of B3 errors that have occurred after the contents of the B3E counter have been previously sampled. The value stored to the B3ECNTR register is retained until the B3E counter is sampled again.

The contents of the B3E counter are cleared to 0 each time the counter has been sampled. The counter is also cleared when 1 is written to the B3EC bit of the PCIR1 (1CH) register.

When the value of the counter reaches all “F”, an overflow is detected and the B3EC bit of PCOCR1 (20H) is set to 1. In addition, the PCO bit of the PICR (06H) register is set to 1, causing an interrupt. Even after an overflow occurs, the B3E counter continues counting up.

### (17) Line REI error count register (LRECT)



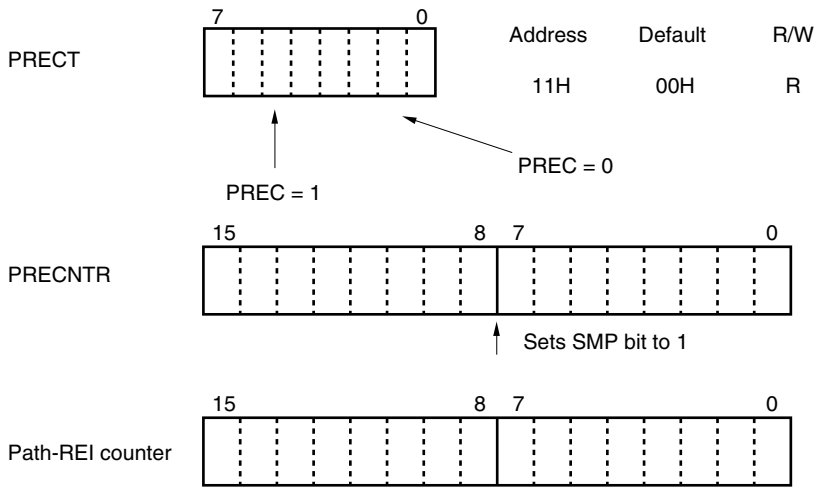

This register is a window register that is used to read the value of the 20-bit LRECNTR register in three parts of 8 bits each. When this register read, the low-order 8 bits of LRECNTR [7:0] are read first, the middle-order 8 bits of LRECNTR [15:8], and then the high-order 4 bits of LRECNTR [19:15] are read. Whether the low-order or middle-order 8 bits or high-order 4 bits of LRECNTR are read when this register is read next time is indicated by the LREC1 and LREC0 bits of the PCPR1 register (address: 19H). The default value of these bits are 0. Each time the LRECT register has been read, this bit automatically change from 00 to 01, from 01 to 10, from 10 to 00, and so on.

The LRECNTR register is a load register that samples (stores) the value of the Line-REI counter. When the SMP bit of the PCSR register (1BH) is set to 1, the value of the Line-REI counter is stored to the LRECNTR register. This value indicates the total of the number of Line-REIs that have occurred after the contents of the Line-REI counter have been previously sampled. The value stored to the RECNTR register is retained until the Line-REI counter is sampled again.

The contents of the Line-REI counter are cleared to 0 each time the counter has been sampled. The counter is also cleared when 1 is written to the LREC bit of the PCIR1 (1CH) register.

When the value of the counter reaches all “F”, an overflow is detected and the LREC bit of PCOCR1 (20H) is set to 1. In addition, the PCO bit of the PICR (06H) register is set to 1, causing an interrupt. Even after an overflow occurs, the Line-REI counter continues counting up.

**(18) Path REI error count register (PRECT)**



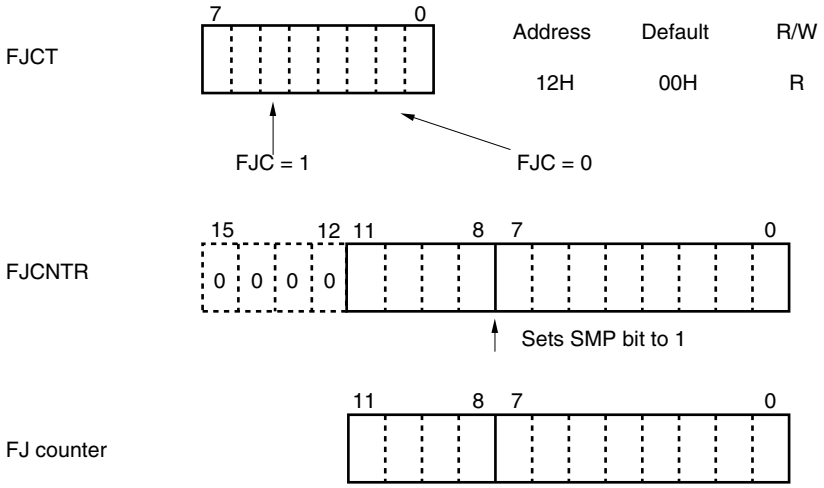

This register is a window register that is used to read the value of the 16-bit PRECNTR register in 8-bit units. When this register read, the low-order 8 bits of PRECNTR [7:0] are read first, and then the high-order 4 bits of PRECNTR [15:8] are read. Whether the low-order 8 bits or high-order 4 bits of PRECNTR are read when this register is read next time is indicated by the PREC bit of the PCPR1 register (address: 19H). The default value of this bit is 0. Each time the PRECT register has been read, these bits automatically change from 0 to 1 and then back to 0 again.

The PRECNTR register is a load register that samples (stores) the value of the Path-REI counter. When the SMP bit of the PCSR register (1BH) is set to 1, the value of the Path-REI counter is stored to the PRECNTR register This value indicates the total of the number of Path-REIs that have occurred after the contents of the Path-REI counter have been previously sampled. The value stored to the PRECNTR register is retained until the Path-REI counter is sampled again.

The contents of the Path-REI counter are cleared to 0 each time the counter has been sampled. The counter is also cleared when 1 is written to the PFBC bit of the PCIR1 (1CH) register.

When the value of the counter reaches all “F”, an overflow is detected and the PREC bit of PCOCR1 (20H) is set to 1. In addition, the PCO bit of the PICR (06H) register is set to 1, causing an interrupt. Even after an overflow occurs, the Path-REI counter continues counting up.

**(19) Frequency Justification count register (FJCT)**



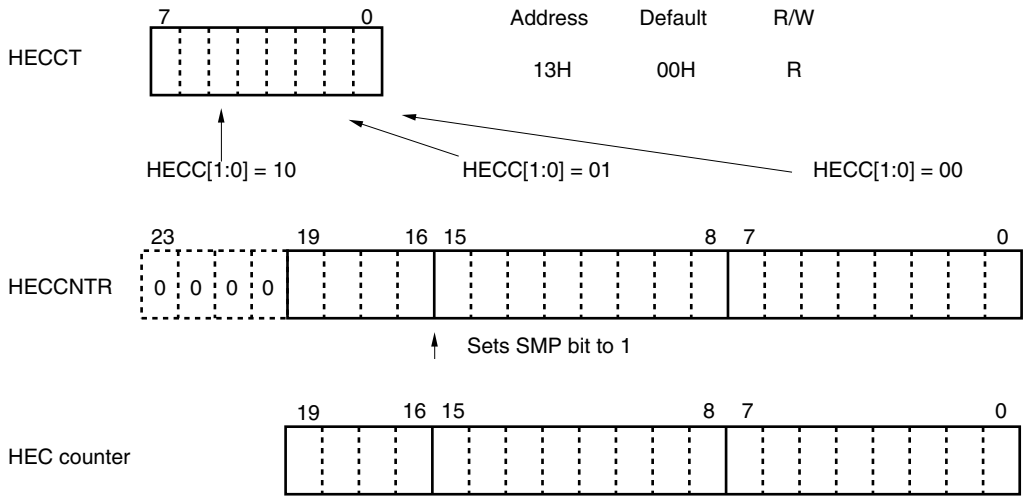

This register is a window register that is used to read the value of the 12-bit FJCNTR register in two parts of 8 bits and 4 bits. When this register read, the low-order 8 bits of FJCNTR [7:0] are read first, and then the high-order 4 bits of FJCNTR [11:8] are read. Whether the low-order 8 bits or high-order 4 bits of FJCNTR are read when this register is read next time is indicated by the FJC bit of the PCPR1 register (address: 19H). The default value of this bit is 0. Each time the FJCT register has been read, these bits automatically change from 0 to 1 and then back to 0 again.

The FJCNTR register is a load register that samples (stores) the value of the FJ counter. When the SMP bit of the PCSR register (1BH) is set to 1, the value of the FJ counter is stored to the FJCNTR register. This value indicates the total of the number of Frequency Justification operations that have occurred after the contents of the FJ counter have been previously sampled. The value stored to the FJCNTR register is retained until the FJ counter is sampled again.

The contents of the FJ counter are cleared to 0 each time the counter has been sampled. The counter is also cleared when 1 is written to the FJC bit of the PCIR1 (1CH) register.

When the value of the counter reaches all “F”, an overflow is detected and the FJC bit of PCOCR1 (20H) is set to 1. In addition, the PCO bit of the PICR (06H) register is set to 1, causing an interrupt. Even after an overflow occurs, the FJ counter continues counting up.

**(20) HEC error count register (HECCT)**



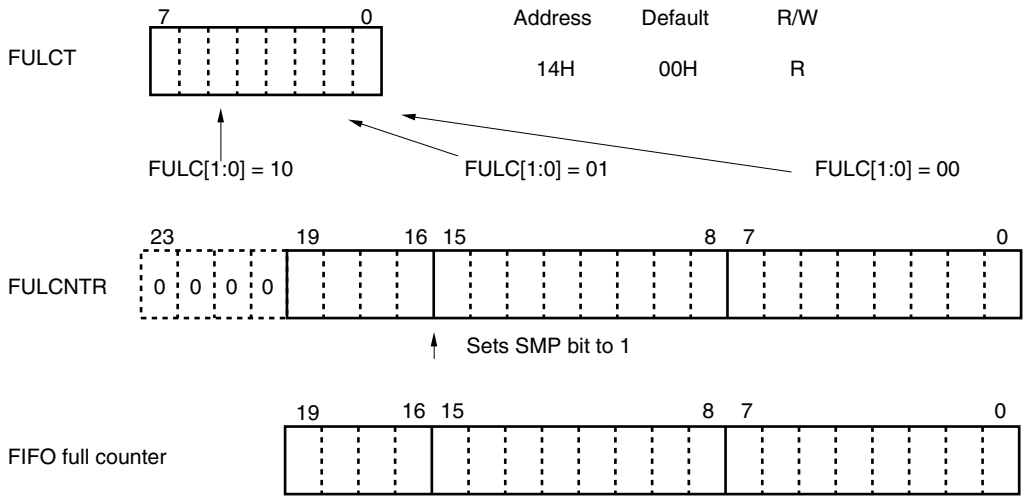

This register is a window register that is used to read the value of the 20-bit HECCNTR register in three parts of 8 bits each. When this register read, the low-order 8 bits of HECCNTR [7:0] are read first, the middle-order 8 bits of HECCNTR [15:8], and then the high-order 4 bits of HECCNTR [19:15] are read. Whether the low-order or middle-order 8 bits or high-order 4 bits of HECCNTR are read when this register is read next time is indicated by the HECC1 and HECC0 bits of the PCPR2 register (address: 1AH). The default values of these bits are 00. Each time the HECCT register has been read, these bits automatically change from 00 to 01, from 01 to 10, from 10 to 00, and so on.

The HECCNTR register is a load register that samples (stores) the value of the HEC counter. When the SMP bit of the PCSR register (1BH) is set to 1, the value of the HEC counter is stored to the HECCNTR register. This value indicates the total of the number of cells that have been dropped due to occurrence of a HEC error after the contents of the HEC counter have been previously sampled. The value stored to the HECCNTR register is retained until the HEC counter is sampled again.

The contents of the HEC counter are cleared to 0 each time the counter has been sampled. The counter is also cleared when 1 is written to the HECC bit of the PCIR2 (1DH) register.

When the value of the counter reaches all “F”, an overflow is detected and the HECC bit of PCOCR2 (21H) is set to 1. In addition, the PCO bit of the PICR (06H) register is set to 1, causing an interrupt. Even after an overflow occurs, the HEC counter continues counting up.

**(21) FIFO full count register (FULCT)**



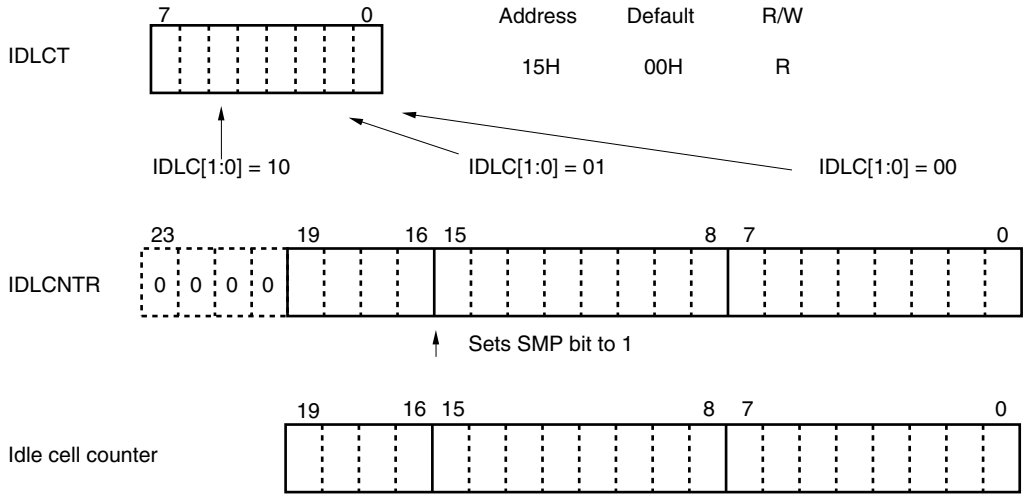

This register is a window register that is used to read the value of the 20-bit FULCNTR register in three parts of 8 bits each. When this register read, the low-order 8 bits of FULCNTR [7:0] are read first, the middle-order 8 bits of FULCNTR [15:8], and then the high-order 4 bits of FULCNTR [19:15] are read. Whether the low-order or middle-order 8 bits or high-order 4 bits of FULCNTR are read when this register is read next time is indicated by the FULC1 and FULC0 bits of the PCPR2 register (address: 1AH). The default values of these bits are 00. Each time the FULCT register has been read, these bits automatically change from 00 to 01, from 01 to 10, from 10 to 00, and so on.

The FULCNTR register is a load register that samples (stores) the value of the FIFO full counter. When the SMP bit of the PCSR register (1BH) is set to 1, the value of the FIFO full counter is stored to the FULCNTR register. This value indicates the total of the number of cells that have been dropped because the FIFO is full after the contents of the FIFO full counter have been previously sampled. The value stored to the FULCNTR register is retained until the FIFO full counter is sampled again.

The contents of the FIFO full counter are cleared to 0 each time the counter has been sampled. The counter is also cleared when 1 is written to the FULC bit of the PCIR2 (1DH) register.

When the value of the counter reaches all “F”, an overflow is detected and the FULC bit of PCOCR2 (21H) is set to 1. In addition, the PCO bit of the PICR (06H) register is set to 1, causing an interrupt. Even after an overflow occurs, the FIFO full counter continues counting up.

**(22) Idle cell (vacant cell) count register (IDLCT)**




This register is a window register that is used to read the value of the 20-bit IDLCNTR register in three parts of 8 bits each. When this register read, the low-order 8 bits of IDLCNTR [7:0] are read first, the middle-order 8 bits of IDLCNTR [15:8], and then the high-order 4 bits of IDLCNTR [19:15] are read. Whether the low-order or middle-order 8 bits or high-order 4 bits of HECCNTR are read when this register is read next time is indicated by the IDLC1 and IDLC0 bits of the PCPR2 register (address: 1AH). The default values of these bits are 00. Each time the IDLCT register has been read, these bits automatically change from 00 to 01, from 01 to 10, from 10 to 00, and so on.

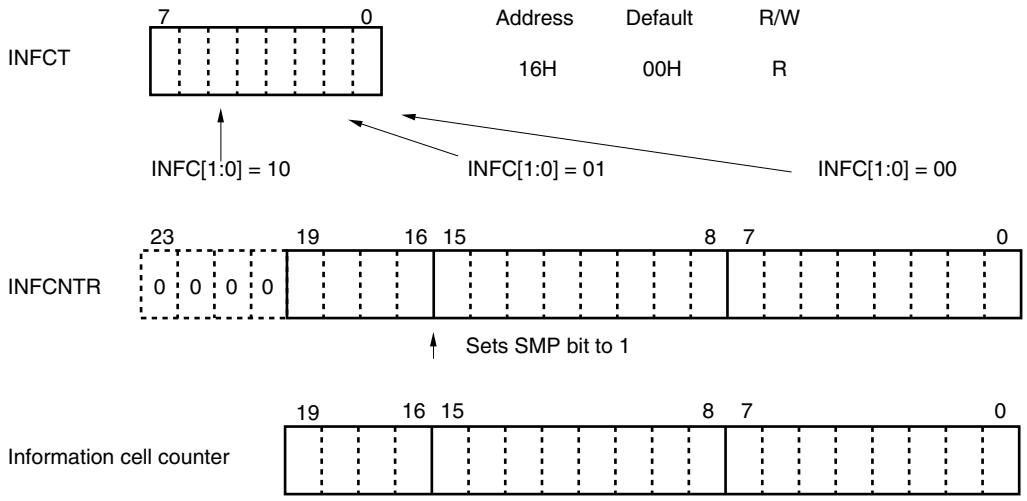
The IDLCNTR register is a load register that samples (stores) the value of the idle cell counter.

When the SMP bit of the PCSR register (1BH) is set to 1, the value of the idle cell counter is stored to the IDLCNTR register. This value indicates the total of the number of idle cells that have been received after the contents of the idle cell counter have been previously sampled. The value stored to the IDLCNTR register is retained until the idle cell counter is sampled again.

The contents of the idle cell counter are cleared to 0 each time the counter has been sampled. The counter is also cleared when 1 is written to the IDLC bit of the PCIR2 (1DH) register.

When the value of the counter reaches all “F”, an overflow is detected and the IDLC bit of PCOCR2 (21H) is set to 1. In addition, the PCO bit of the PICR (06H) register is set to 1, causing an interrupt. Even after an overflow occurs, the idle cell counter continues counting up.

**(23) Information cell count register (INFCT)**




This register is a window register that is used to read the value of the 20-bit INFCNTR register in three parts of 8 bits each. When this register read, the low-order 8 bits of INFCNTR [7:0] are read first, the middle-order 8 bits of INFCNTR [15:8], and then the high-order 4 bits of INFCNTR [19:15] are read. Whether the low-order or middle-order 8 bits or high-order 4 bits of INFCNTR are read when this register is read next time is indicated by the INFC1 and INFC0 bits of the PCPR2 register (address: 1AH). The default values of these bits are 00. Each time the INFCT register has been read, these bits automatically change from 00 to 01, from 01 to 10, from 10 to 00, and so on.

The INFCNTR register is a load register that samples (stores) the value of the information cell counter. When the SMP bit of the PCSR register (1BH) is set to 1, the value of the information cell counter is stored to the INFCNTR register. This value indicates the total of the number of valid cells (cells transferred to the ATM layer device) that have been received after the contents of the information cell counter have been previously sampled. The value stored to the INFCNTR register is retained until the information cell counter is sampled again.

The contents of the information cell counter are cleared to 0 each time the counter has been sampled. The counter is also cleared when 1 is written to the INFC bit of the PCIR2 (1DH) register.

When the value of the counter reaches all “F”, an overflow is detected and the INFC bit of PCOCR2 (21H) is set to 1. In addition, the PCO bit of the PICR (06H) register is set to 1, causing an interrupt. Even after an overflow occurs, the information cell counter continues counting up.

### (24) Performance counter point register 1 (PCPR1)

This register indicates which byte of a load register corresponding to each wind register is to be read next.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCPR1 | B1EC | B2EC1 | B2EC0 | B3EC | LREC1 | LREC0 | PREC | FJC | 19H | 00H | R/W |

| Field | Function | | Default Value |
|---|---|---|---|
| D7: B1EC | Indicates which bits of B1 error counter are to be read next. | | 0 |
| | 1 | High-order 8 bits [15:8] of 16-bit counter are read next. | |
| | 0 | Low-order 8 bits [7:0] of 16-bit counter are read next. | |
| D6: B2EC1<br>D5: B2EC0 | Indicates which bits of B2 error counter are to be read next. | | 00 |
| | B2EC [1:0] | Bits to be read next | |
| | 00 | Low-order 8 bits [7:0] | |
| | 01 | Middle-order 8 bits [15:8] | |
| | 10 | High-order 4 bits [19:16] | |
| D4: B3EC | Indicates which bits of B3 error counter are to be read next. | | 0 |
| | 1 | High-order 8 bits [15:8] of 16-bit counter are read next. | |
| | 0 | Low-order 8 bits [7:0] of 16-bit counter are read next. | |
| D3: LREC1<br>D2: LREC0 | Indicates which bits of Line-REI counter are to be read next. | | 00 |
| | LREC [1:0] | Bits to be read next | |
| | 00 | Low-order 8 bits [7:0] | |
| | 01 | Middle-order 8 bits [15:8] | |
| | 10 | High-order 4 bits [19:16] | |
| D1: PREC | Indicates which bits of Path-REI counter are to be read next. | | 0 |
| | 1 | High-order 8 bits [15:8] of 16-bit counter are read next. | |
| | 0 | Low-order 8 bits [7:0] of 16-bit counter are read next. | |
| D0: FJC | Indicates which bits of FJ counter are to be read next. | | 0 |
| | 1 | High-order 4 bits [11:8] of 12-bit counter are read next. | |
| | 0 | Low-order 8 bits [7:0] of 12-bit counter are read next. | |

### (25) Performance counter point register 2 (PCPR2)

This register indicates which byte of a load register corresponding to each window register is to be read next.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCPR2 | HECC1 | HECC0 | FULC1 | FULC0 | IDLC1 | IDLC0 | INFC1 | INFC0 | 1AH | 00H | R/W |

| Field | Function | Default Value |
|---|---|---|
| D7: HECC1<br>D6: HECC0 | Indicates which bits of HEC error counter are to be read next. | 00 |

| HECC [1:0] | Bits to be read next |
|---|---|
| 00 | Low-order 8 bits [7:0] |
| 01 | Middle-order 8 bits [15:8] |
| 10 | High-order 4 bits [19:16] |

| Field | Function | Default Value |
|---|---|---|
| D5: FULC1<br>D4: FULC0 | Indicates which bits of FIFO full counter are to be read next. | 00 |

| FULC [1:0] | Bits to be read next |
|---|---|
| 00 | Low-order 8 bits [7:0] |
| 01 | Middle-order 8 bits [15:8] |
| 10 | High-order 4 bits [19:16] |

| Field | Function | Default Value |
|---|---|---|
| D3: IDLC1<br>D2: IDLC0 | Indicates which bits of idle cell counter are to be read next. | 00 |

| IDLC [1:0] | Bits to be read next |
|---|---|
| 00 | Low-order 8 bits [7:0] |
| 01 | Middle-order 8 bits [15:8] |
| 10 | High-order 4 bits [19:16] |

| Field | Function | Default Value |
|---|---|---|
| D1: INFC1<br>D0: INFC0 | Indicates which bits of information cell counter are to be read next. | 00 |

| INFC [1:0] | Bits to be read next |
|---|---|
| 00 | Low-order 8 bits [7:0] |
| 01 | Middle-order 8 bits [15:8] |
| 10 | High-order 4 bits [19:16] |

**(26) Performance counter sample register (PCSR)**

This register sets the performance counter sample timing. When the SMP bit of this register is set to 1, the current values of all the counters are stored to the corresponding load registers, and the count values are cleared to 0.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCSR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SMP | 1BH | 00H | R/W |

| Field | Function | | Default Value |
|---|---|---|---|
| D0: SMP | Samples count value. | | 0 |
| | 1 | Stores contents of all counters to corresponding load registers. At this time, all counters are initialized. | |
| | 0 | Does not store counters to the load register. | |

**Remarks 1.** When the SMP bit is set to 1, it is automatically cleared to 0 after the sampling operation has been completed.

**2.** When this register is read, the high-order 7 bits are always “0”. Nothing can be written to these bits.

**(27) Performance counter initialization register 1 (PCIR1)**

This register initializes each performance counter. Although the value of the counter is cleared to 0, the value stored to the corresponding load register is not cleared.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCIR1 | 0 | 0 | B1EC | B2EC | B3EC | LREC | PREC | FJC | 1CH | 00H | R/W |

| Field | Function | | Default Value |
|---|---|---|---|
| D5: B1EC | Initializes B1 error counter. | | 0 |
| | 1 | Value of B1 error counter is cleared to 0. | |
| | 0 | Counter value is not cleared. | |
| D4: B2EC | Initializes B2 error counter. | | 0 |
| | 1 | Value of B2 error counter is cleared to 0. | |
| | 0 | Counter value is not cleared. | |
| D3: B3EC | Initializes B3 error counter. | | 0 |
| | 1 | Value of B3 error counter is cleared to 0. | |
| | 0 | Counter value is not cleared. | |
| D2: LREC | Initializes Line-REI counter. | | 0 |
| | 1 | Value of Line-REI counter is cleared to 0. | |
| | 0 | Counter value is not cleared. | |
| D1: PREC | Initializes Path-REI counter. | | 0 |
| | 1 | Value of Path-REI counter is cleared to 0. | |
| | 0 | Counter value is not cleared. | |
| D0: FJC | Initializes FJ counter. | | 0 |
| | 1 | Value of FJ counter is cleared to 0. | |
| | 0 | Counter value is not cleared. | |

**Remarks 1.** Each bit of this register is automatically cleared to “0” after initialization.

**2.** When this register is read, the high-order 2 bits are always 0. Nothing can be written to these bits.

**(28) Performance counter initialization register 2 (PCIR2)**

This register initializes each performance counter. Although the value of the counter is cleared to 0, the value stored to the corresponding load register is not cleared.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCIR2 | 0 | 0 | 0 | 0 | HECC | FULC | IDLC | INFC | 1DH | 00H | R/W |

| Field | Function | | Default Value |
|---|---|---|---|
| D3: HECC | Initializes HEC counter value. | | 0 |
| | 1 | Value of HEC counter is cleared to 0. | |
| | 0 | Counter value is not cleared. | |
| D2: FULC | Initializes FIFO full counter value. | | 0 |
| | 1 | Value of FIFO full counter is cleared to 0. | |
| | 0 | Counter value is not cleared. | |
| D1: IDLC | Initializes idle cell counter value. | | 0 |
| | 1 | Value of idle cell counter is cleared to 0. | |
| | 0 | Counter value is not cleared. | |
| D0: INFC | Initializes information cell counter value. | | 0 |
| | 1 | Value of information cell counter is cleared to 0. | |
| | 0 | Counter value is not cleared. | |

**Remarks 1.** Each bit of this register is automatically cleared to “0” after initialization.

**2.** When this register is read, the high-order 4 bits are always 0. Nothing can be written to these bits.

**(29) Performance counter stop register 1 (PCFR1)**

This register stops the count operation of counters which are not in use. All the counters are stopped at initial status after power application.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCFR1 | 1 | 1 | B1EC | B2EC | B3EC | LREC | PREC | FJC | 1EH | FFH | R/W |

| Field | | Function | Default Value |
|---|---|---|---|
| D5: B1EC | Stops B1 error counter. | | 1 |
| | 1 | B1 error counter does not operate. | |
| | 0 | B1 error counter operates. | |
| D4: B2EC | Stops B2 error counter. | | 1 |
| | 1 | B2 error counter does not operate. | |
| | 0 | B2 error counter operates. | |
| D3: B3EC | Stops B3 error counter. | | 1 |
| | 1 | B3 error counter does not operate. | |
| | 0 | B3 error counter operates. | |
| D2: LREC | Stops Line-REI counter. | | 1 |
| | 1 | Line-REI counter does not operate. | |
| | 0 | Line-REI counter operates. | |
| D1: PREC | Stops Path-REI counter. | | 1 |
| | 1 | Path-REI counter does not operate. | |
| | 0 | Path-REI counter operates. | |
| D0: FJC | Stops FJ counter. | | 1 |
| | 1 | FJ counter does not operate. | |
| | 0 | FJ counter operates. | |

**Remark** When this register is read, the high-order 2 bits are always “1”. Nothing can be written to these bits.

**(30) Performance counter stop register 2 (PCFR2)**

This register stops the count operation of counters which are not in use. All the counters are sopped at initial status after power application.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCFR2 | 1 | 1 | 1 | 1 | HECC | FULC | IDLC | INFC | 1FH | FFH | R/W |

| Field | Function | | Default Value |
|---|---|---|---|
| D3: HECC | Stops HEC counter. | | 1 |
| | 1 | HEC counter does not operate. | |
| | 0 | HEC counter operates. | |
| D2: FULC | Stops FJ counter. | | 1 |
| | 1 | FIFO full counter does not operate. | |
| | 0 | FIFO full counter operates. | |
| D1: IDLC | Stops idle cell counter. | | 1 |
| | 1 | Idle cell counter does not operate. | |
| | 0 | Idle cell counter operates. | |
| D0: INFC | Stops information cell counter. | | 1 |
| | 1 | Information cell counter does not operate. | |
| | 0 | Information cell counter operates. | |

**Remark** When this register is read, the high-order 4 bits are always “1”. Nothing can be written to these bits.

### (31) Performance counter overflow cause register 1 (PCOCR1)

This register indicates the cause of an overflow in a performance counter.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCOCR1 | 0 | 0 | B1EC | B2EC | B3EC | LREC | PREC | FJC | 20H | 00H | R |

| Field | Function | | Default Value |
|---|---|---|---|
| D5: B1EC | Indicates occurrence of overflow in B1 error counter. | | 0 |
| | 1 | Indicates that overflow has occurred in B1 error counter. | |
| | 0 | Indicates that overflow has not occurred in B1 error counter. | |
| D4: B2EC | Indicates occurrence of overflow in B2 error counter. | | 0 |
| | 1 | Indicates that overflow has occurred in B2 error counter. | |
| | 0 | Indicates that overflow has not occurred in B2 error counter. | |
| D3: B3EC | Indicates occurrence of overflow in B3 error counter. | | 0 |
| | 1 | Indicates that overflow has occurred in B3 error counter. | |
| | 0 | Indicates that overflow has not occurred in B3 error counter. | |
| D2: LREC | Indicates occurrence of overflow in Line-REI counter. | | 0 |
| | 1 | Indicates that overflow has occurred in Line-REI counter. | |
| | 0 | Indicates that overflow has not occurred in Line REI counter. | |
| D1: PREC | Indicates occurrence of overflow in Path-REI counter. | | 0 |
| | 1 | Indicates that overflow has occurred in Path-REI counter. | |
| | 0 | Indicates that overflow has not occurred in Path-REI counter. | |
| D0: FJC | Indicates occurrence of overflow in FJ counter. | | 0 |
| | 1 | Indicates that overflow has occurred in FJ counter. | |
| | 0 | Indicates that overflow has not occurred in FJ counter. | |

**Remarks 1.** When this register is read, the high-order 2 bits are always “0”. Nothing can be written to these bits.

**2.** If even one of the bits of this register not masked by the PCOMR1 register is set to 1, the PCO bit of PICR (address: 06H) is set to “1”.

**3.** This register is cleared when it is read.

**(32) Performance counter overflow cause register 2 (PCOCR2)**

This register indicates the cause of an overflow in a performance counter.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCOCR2 | 0 | 0 | 0 | 0 | HECC | FULC | IDLC | INFC | 21H | 00H | R |

| Field | Function | | Default Value |
|---|---|---|---|
| D3: HECC | Indicates occurrence of overflow in HEC counter. | | 0 |
| | 1 | Indicates that overflow has occurred in HEC counter. | |
| | 0 | Indicates that overflow has not occurred in HEC counter. | |
| D2: FULC | Indicates occurrence of overflow in FIFO full counter. | | 0 |
| | 1 | Indicates that overflow has occurred in FIFO full counter. | |
| | 0 | Indicates that overflow has not occurred in FIFO full counter. | |
| D1: IDLC | Indicates occurrence of overflow in idle cell counter. | | 0 |
| | 1 | Indicates that overflow has occurred in idle cell counter. | |
| | 0 | Indicates that overflow has not occurred in idle cell counter. | |
| D0: INFC | Indicates occurrence of overflow in information cell counter. | | 0 |
| | 1 | Indicates that overflow has occurred in information cell counter. | |
| | 0 | Indicates that overflow has not occurred in information cell counter. | |

**Remarks 1.** When this register is read, the high-order 4 bits are always “0”. Nothing can be written to these bits.

**2.** If even one of the bits of this register not masked by the PCOMR2 register is set to 1, the PCO bit of PICR (address: 06H) is set to “1”.

**3.** This register is cleared when it is read.

**(33) Performance counter overflow mask register 1 (PCOMR1)**

This register masks the overflow cause of PCOCR1 (address: 20H). If an overflow cause is masked, the PCO bit of PICR (address: 06H) is not set.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCOMR1 | 1 | 1 | B1EC | B2EC | B3EC | LREC | PREC | FJC | 22H | FFH | R/W |

| Field | Function | | Default Value |
|---|---|---|---|
| D5: B1EC | Masks occurrence of B1 error counter overflow. | | 1 |
| | 1 | Masks occurrence of overflow in B1 error counter. | |
| | 0 | Does not mask occurrence of overflow in B1 error counter. | |
| D4: B2EC | Masks occurrence of B2 error counter overflow. | | 1 |
| | 1 | Masks occurrence of overflow in B2 error counter. | |
| | 0 | Does not mask occurrence of overflow in B2 error counter. | |
| D3: B3EC | Masks occurrence of B3 error counter overflow. | | 1 |
| | 1 | Masks occurrence of overflow in B3 error counter. | |
| | 0 | Does not mask occurrence of overflow in B3 error counter. | |
| D2: LREC | Masks occurrence of Line-REI counter overflow. | | 1 |
| | 1 | Masks occurrence of overflow in Line-REI counter. | |
| | 0 | Does not mask occurrence of overflow in Line-REI counter. | |
| D1: PREC | Masks occurrence of Path-REI counter overflow. | | 1 |
| | 1 | Masks occurrence of overflow in Path-REI counter. | |
| | 0 | Does not mask occurrence of overflow in Path-REI counter. | |
| D0: FJC | Masks occurrence of FJ counter overflow. | | 1 |
| | 1 | Masks occurrence of overflow in FJ counter. | |
| | 0 | Does not mask occurrence of overflow in FJ counter. | |

**Remark** When this register is read, the high-order 2 bits are always 1. Nothing can be written to these bits.

**(34) Performance counter overflow mask register 2 (PCOMR2)**

This register masks the overflow cause of PCOCR1 (address: 20H). If an overflow cause is masked, the PCO bit of PICR (address: 06H) is not set.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCOMR2 | 1 | 1 | 1 | 1 | HECC | FULC | IDLC | INFC | 23H | FFH | R/W |

| Field | Function | | Default Value |
|---|---|---|---|
| D3: HECC | Masks occurrence of HEC counter overflow. | | 1 |
| | 1 | Masks occurrence of overflow in HEC counter. | |
| | 0 | Does not mask occurrence of overflow in HEC counter. | |
| D2: FULC | Masks occurrence of FIFO full counter overflow. | | 1 |
| | 1 | Masks occurrence of overflow in FIFO full counter. | |
| | 0 | Does not mask occurrence of overflow in FIFO full counter. | |
| D1: IDLC | Masks occurrence of idle cell counter overflow. | | 1 |
| | 1 | Masks occurrence of overflow in idle cell counter. | |
| | 0 | Does not mask occurrence of overflow in idle cell counter. | |
| D0: INFC | Masks occurrence of information cell counter overflow. | | 1 |
| | 1 | Masks occurrence of overflow in information cell counter. | |
| | 0 | Does not mask occurrence of overflow in information cell counter. | |

**Remark** When this register is read, the high-order 4 bits are always 1. Nothing can be written to these bits.

**(35) Alarm output pin setting register (AMPR)**

This register selects which of the three PHYALM[2:0] pins is to be set when setting AMR1 and AMR0 registers to select which of the alarm signal is to be output from the PHYALM pin.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| AMPR | 0 | 0 | 0 | 0 | 0 | 0 | AMP1 | AMP0 | 24H | 00H | R/W |

| Field | Function | Default Value |
|---|---|---|
| D1: AMP1<br>D0: AMP0 | Specifies which of PHYALM[2:0] pins is to be set by setting AMR1 and AMR0 registers. | 00 |

| AMP [1:0] | Selected PHYALM pin |
|---|---|
| 00 | PHYALM0 output pin mode is set. |
| 01 | PHYALM1 output pin mode is set. |
| 1X | PHYALM2 output pin mode is set. |

**Remark** When this register is read, the high-order 6 bits are always “0”. Nothing can be written to these bits.

**(36) Output alarm mask register 1 (AMR1)**

This register selects an alarm or error signal (CMR, PMD, LOS, OOF, LOF, LOP, OCD, or LCD) to be output from the PHYALM pin specified by the AMPR register. When the alarm or error set to "1" by this register is detected, the output signal of the PHYALM pin is made high until the condition disappears.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| AMR1 | CMD | PMD | LOS | OOF | LOF | LOP | OCD | LCD | 25H | FFH | R/W |

| Field | Function | | Default Value |
|---|---|---|---|
| D7: CMD | Specifies whether ARM bit of command register is set is reported from PHYALM output pin specified by AMPR register. | | 1 |
| | 1 | Does not report that ARM bit is set. | |
| | 0 | Reports by making PHY output high when ARM bit is set. | |
| D6: PMD | Specifies whether to report that PMDALM pin input goes high from PHYALM pin specified by AMPR register. | | 1 |
| | 1 | Does not report that PMDALM pin input goes high. | |
| | 0 | Reports by making PHYAML pin high when PMDALM pin goes high. | |
| D5: LOS | Specifies whether to report that LOS is detected from PHYALM pin specified by AMPR register. | | 1 |
| | 1 | Does not report even if LOS is detected. | |
| | 0 | Makes PHYALM pin output high when LOS is detected. | |
| D4: OOF | Specifies whether to report that OOF is detected from PHYALM pin specified by AMPR register. | | 1 |
| | 1 | Does not report even if OOF is detected. | |
| | 0 | Makes PHYALM pin output high when OOF is detected. | |
| D3: LOF | Specifies whether to report that LOF is detected from PHYALM pin specified by AMPR register. | | 1 |
| | 1 | Does not report even if LOF is detected. | |
| | 0 | Makes PHYALM pin output high when LOF is detected. | |
| D2: LOP | Specifies whether to report that LOP is detected from PHYALM pin specified by AMPR register. | | 1 |
| | 1 | Does not report even if LOP is detected. | |
| | 0 | Makes PHYALM pin output high when LOP is detected. | |
| D1: OCD | Specifies whether to report that OCD is detected from PHYALM pin specified by AMPR register. | | 1 |
| | 1 | Does not report even if OCD is detected. | |
| | 0 | Makes PHYALM pin output high when OCD is detected. | |
| D0: LCD | Specifies whether to report that LCD is detected from PHYALM pin specified by AMPR register. | | 1 |
| | 1 | Does not report even if LCD is detected. | |
| | 0 | Makes PHYALM pin output high when LCD is detected. | |

**(37) Output alarm mask register 2 (AMR2)**

This register selects an alarm or error signal (Line AIS, Path AIS, Line RDI, or Path RDI) to be output from the PHYALM pin specified by the AMPR register. When the alarm or error set to "1" by this register is detected, the output signal of the PHYALM pin is made high until the condition disappears.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| AMR2 | 1 | 1 | 1 | 1 | LAIS | PAIS | LRDI | PRDI | 26H | FFH | R/W |

| Field | Function | | Default Value |
|---|---|---|---|
| D3: LAIS | Specifies whether to report that Line AIS is detected from PHYALM pin specified by AMPR register. | | 1 |
| | 1 | Does not report even if Line AIS is detected. | |
| | 0 | Makes PHYALM pin output high when Line AIS is detected. | |
| D2: PAIS | Specifies whether to report that Path AIS is detected from PHYALM pin specified by AMPR register. | | 1 |
| | 1 | Does not report even if Path AIS is detected. | |
| | 0 | Makes PHYALM pin output high when Path AIS is detected. | |
| D1: LRDI | Specifies whether to report that Line RDI is detected from PHYALM pin specified by AMPR register. | | 1 |
| | 1 | Does not report even if Line RDI is detected. | |
| | 0 | Makes PHYALM pin output high when Line RDI is detected. | |
| D0: PRDI | Specifies whether to report that Path RDI is detected from PHYALM pin specified by AMPR register. | | 1 |
| | 1 | Does not report even if Path RDI is detected. | |
| | 0 | Makes PHYALM pin output high when Path RDI is detected. | |

**Remark** When this register is read, the high-order 4 bits are always "1". Nothing can be written to these bits.

**(38) Drop cell header pattern register (DCHPR)**

This register specifies the cell to be dropped. Whether only idle cells, or both idle cells and unassigned cells are dropped can be selected.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DCHPR | GFC3 | GFC2 | GFC1 | GFC0 | PTI2 | PTI1 | PTI0 | CLP | 27H | 01H | R/W |

| Field | Function | Default Value |
|---|---|---|
| D7:GFC3<br>D6:GFC2<br>D5:GFC1<br>D4:GFC0<br>D3:PTI2<br>D2:PTI1<br>D1:PTI0<br>D0:CLP | The μPD98404 checks the pattern of the cell header before it stores the extracted receive cell in the receive FIFO. In the case of a cell with VPI/VCI field being all 0, the other header fields are compared with the set value of this register. If a header field coincides with the setting of this register, the cell is not stored in the receive FIFO but is discarded.<br>However, the bits masked by the DCHPMR register are not compared. | 01 |

### (39) Drop cell header pattern mask register (DCHPMR)

This register specifies whether the CLP field of the receive cell header is compared with the CLP bit of the DCHPR register or ignored (masked) when the cell to be dropped is determined.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DCHPMR | GFC3 | GFC2 | GFC1 | GFC0 | PTI2 | PTI1 | PTI0 | CLP | 28H | 00H | R/W |

| Field | Function | Default Value |
|---|---|---|
| D7:GFC3<br>D6:GFC2<br>D5:GFC1<br>D4:GFC0<br>D3:PTI2<br>D2:PTI1<br>D1:PTI0<br>D0:CLP | If a bit of this register is set, the corresponding bit of the DCHPR register, and the field corresponding to each bit of the receive cell with the VPI/VCI field being all 0 are not compared. Only the bits to which 0 is written is compared. | 0 |

★ **Example of Setting DCHPR/DCHPMR Register**

| DCHPR | DCHPMR | Discarded Cell |
|---|---|---|
| 01 | 00 | Idle cell (default) |
| 00 | 00 | Unassigned cell |
| 00 | 01 | Idle cell and unassigned cell |

### (40) PHY ID register (PHYIDR)

This register selects the PHY ID address to be given to the μPD98404 in the multi-PHY mode, and enables or disables giving the address to the μPD98404.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PHYIDR | EN | 0 | 0 | PHA4 | PHA3 | PHA2 | PHA1 | PHA0 | 29H | 01H | R/W |

| Field | Function | | Default Value |
|---|---|---|---|
| D7: EN | Enables address check on TADD[4:0] and RADD[4:0] on the ATM layer interface in the multi-PHY mode (UMPSEL pin = high). | | 0 |
| | 1 | Enables address check. | |
| | 0 | Disables address check. | |
| D4-D0:<br>PHA4-PHA0 | Sets address to be given to μPD98404. If address set by this field is output to TADD[4:0] and RADD[4:0], μPD98404 is selected. | | 01 |

**Remark** When this register is read, the high-order 3 bits are “0”. Nothing can be written to these bits.

**(41) J0R data register (J0R)**

This is an 8-bit register that stores the J0 byte of the reception side SOH (Section Overhead).

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| J0R | | | | | | | | | 2AH | 00H | R |

**(42) Z01R data register (Z01R)**

This is an 8-bit register that stores the first Z0 byte of the reception side SOH.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Z01R | | | | | | | | | 2BH | 00H | R |

**(43) Z02R data register (Z02R)**

This is an 8-bit register that stores the second Z0 byte of the reception side SOH.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Z02R | | | | | | | | | 2CH | 00H | R |

**(44) F1R data register (F1R)**

This is an 8-bit register that stores the F1 byte data of the reception side SOH.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| F1R | | | | | | | | | 2DH | 00H | R |

**(45) K1R data register (K1R)**

This is an 8-bit register that stores the K1 byte data of the reception side LOH (Line Overhead).

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| K1R | | | | | | | | | 2EH | 00H | R |

**(46) K2R data register (K2R)**

This is an 8-bit register that stores the K2 byte data of the reception side LOH.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| K2R | | | | | | | | | 2FH | 00H | R |

**(47) C2R data register (C2R)**

This is an 8-bit register that stores the C2 byte data of the reception side POH (Path Overhead).

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| C2R | | | | | | | | | 30H | 00H | R |

**(48) F2R data register (F2R)**

This is an 8-bit register that stores the F2 byte data of the reception side POH.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| F2R | | | | | | | | | 31H | 00H | R |

**(49) H4R data register (H4R)**

This is an 8-bit register that stores the H4 byte data of the reception side POH.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| H4R | | | | | | | | | 32H | 00H | R |

**(50) J0T data register (J0T)**

This is an 8-bit register that stores the J0 byte of the transmission side SOH.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| J0T | | | | | | | | | 33H | 01H | R/W |

**(51) Z01T data register (Z01T)**

This is an 8-bit register that stores the first Z0 byte of the transmission side SOH.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Z01T | | | | | | | | | 34H | 02H | R/W |

**(52) Z02T data register (Z02T)**

This is an 8-bit register that stores the second Z0 byte of the transmission side SOH.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Z02T | | | | | | | | | 35H | 03H | R/W |

**(53) F1T data register (F1T)**

This is an 8-bit register that stores the F1 data of the transmission side SOH.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| F1T | | | | | | | | | 36H | 00H | R/W |

**(54) K1T data register (K1T)**

This is an 8-bit register that stores the K1 data of the transmission side LOH.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| K1T | | | | | | | | | 37H | 00H | R/W |

**(55) K2T data register (K2T)**

This 5-bit register sets the high-order 5 bits of the KA2 byte of the transmission side LOH.

Because the low-order 3 bits of the K2 byte are used to transmit Line AIS and Line RDI, the low-order 3 bits set in this register are ignored.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| K2T | | | | | | X | X | X | 38H | 00H | R/W |

**(56) C2T data register (C2T)**

This is an 8-bit register that stores the C2 byte of the transmission side POH.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| C2T | | | | | | | | | 39H | 00H | R/W |

**(57) F2T data register (F2T)**

This is an 8-bit register that stores the F2 byte of the transmission side POH.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| F2T | | | | | | | | | 3AH | 00H | R/W |

**(58) H4T data register (H4T)**

This is an 8-bit register that stores the H4 byte of the transmission side POH.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| H4T | | | | | | | | | 3BH | 00H | R/W |

**(59) Reserved area**

- Address: 3CH through 3EH
- Do not read or write this area.

**(60) Version register (VERR)**

This register stores the version name of this LSI.

| Register name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address | Default | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VERR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3FH | 00H | R |

**(61) Reserved area**

- Address: 40H through 7FH
- Do not read or write this area.

# CHAPTER 6 JTAG BOUNDARY SCAN

The $\mu$PD98404 has a JTAG boundary scan circuit.

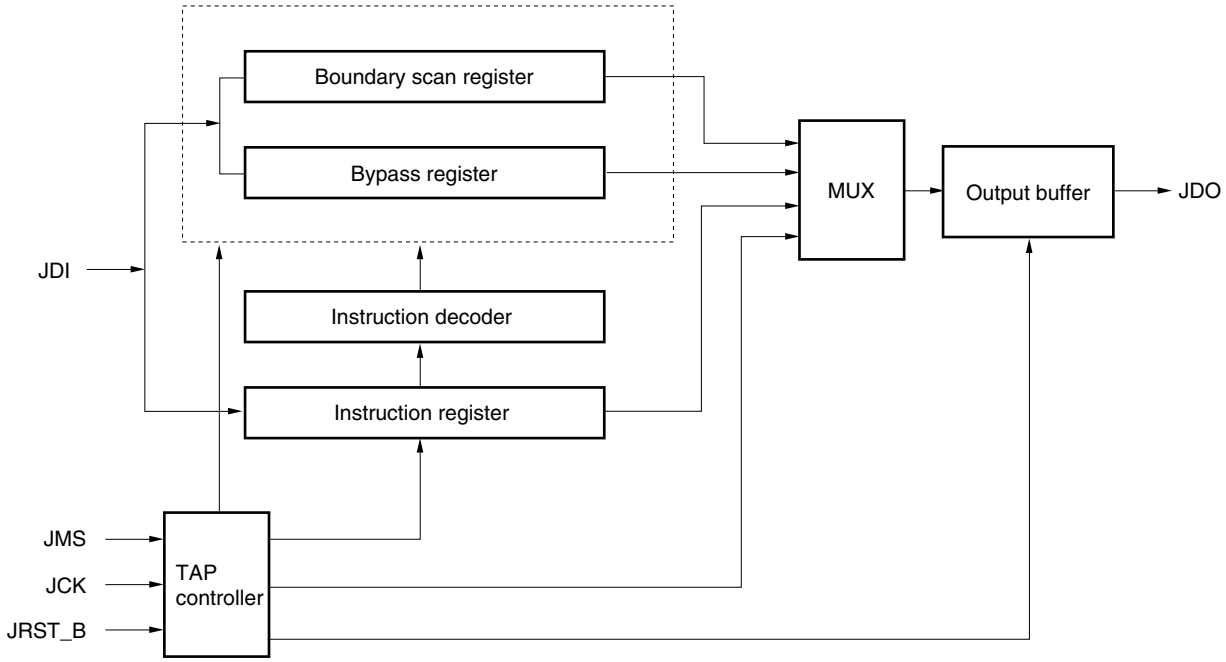
## 6.1 Features

- Conforms to IEEE1149.1 JTAG Boundary Scan Standard.
- Three registers dedicated to boundary scan
  - Instruction register
  - Bypass register
  - Boundary scan register
- Three instructions supported
  - BYPASS instruction
  - EXTEST instruction
  - SAMPLE/PRELOAD instruction
- Five pins dedicated to boundary scan
  - JCK (JTAG Clock)
  - JMS (JTAG Mode Select)
  - JDI (JTAG Data Input)
  - JDO (JTAG Data Output)
  - JRST_B (JTAG Reset)

## 6.2 Internal Configuration of Boundary Scan Circuit

Figure 6-1 shows the block diagram of the internal JTAG boundary scan circuit of the μPD98404.

**Figure 6-1. Block Diagram of Boundary Scan Circuit**




### 6.2.1 Instruction register

The instruction register consists of a 2-bit shift register and writes instruction data from the JDI pin. The register and instruction are selected by this instruction data.

### 6.2.2 TAP (Test Access Port) controller

The TAP controller changes operating state by latching the signal of the JMS pin at the rising edge of the clock input to the JCK pin.

### 6.2.3 Bypass register

The bypass register consists of a 1-bit shift register connected between the JDI and JDO pins when the TAP controller is in Shift-DR state. If this register is selected while the TAP controller is in Shift-DR state, data is shifted to the JDO pin at the rising edge of the clock input to the JCK pin.

When this register is selected, the operation of the JTAG boundary circuit does not influence on the operation of the μPD98404.

### 6.2.4 Boundary scan register

The boundary scan register is located between an external pin of the μPD98404 and internal logic circuit. When this register is selected, data is latched or loaded by the instruction of the TAP controller.

If this register is selected while the TAP controller is in Shift-DR state, data is output to the JDO pin starting from the LSB at the falling edge of the clock input to the JCK pin.

## 6.3 Pin Function

### 6.3.1 JCK (JTAG Clock) pin

The JCK pin is used to supply a clock signal to the JTAG boundary scan circuit (such as the bypass register, instruction register, and TAP controller. This clock signal is isolated so as not to be supplied to the other internal circuits of the μPD98404.

### 6.3.2 JMS (JTAG Mode Select) pin

Input to the JMS signal is latched at the rising edge of the clock input to the JCK pin and defines the operation of the TAP controller.

### 6.3.3 JDI (JTAG Data Input) pin

The JDI pin is an input pin that inputs data to the JTAG boundary scan circuit register.

### 6.3.4 JDO (JTAG Data Output) pin

The JDO pin is an output pin that outputs data from the JTAG boundary scan circuit. This pin changes its output at the falling edge of the clock input to the JCK pin. This pin is a three-state output pin and is controlled by the TAP controller.

### 6.3.5 JRST_B (JTAG Reset) pin

This pin asynchronously initializes the TAP controller. This reset signal sets the μPD98404 in the normal operation mode and the boundary register in non-operation state.

## 6.4 Operation Description

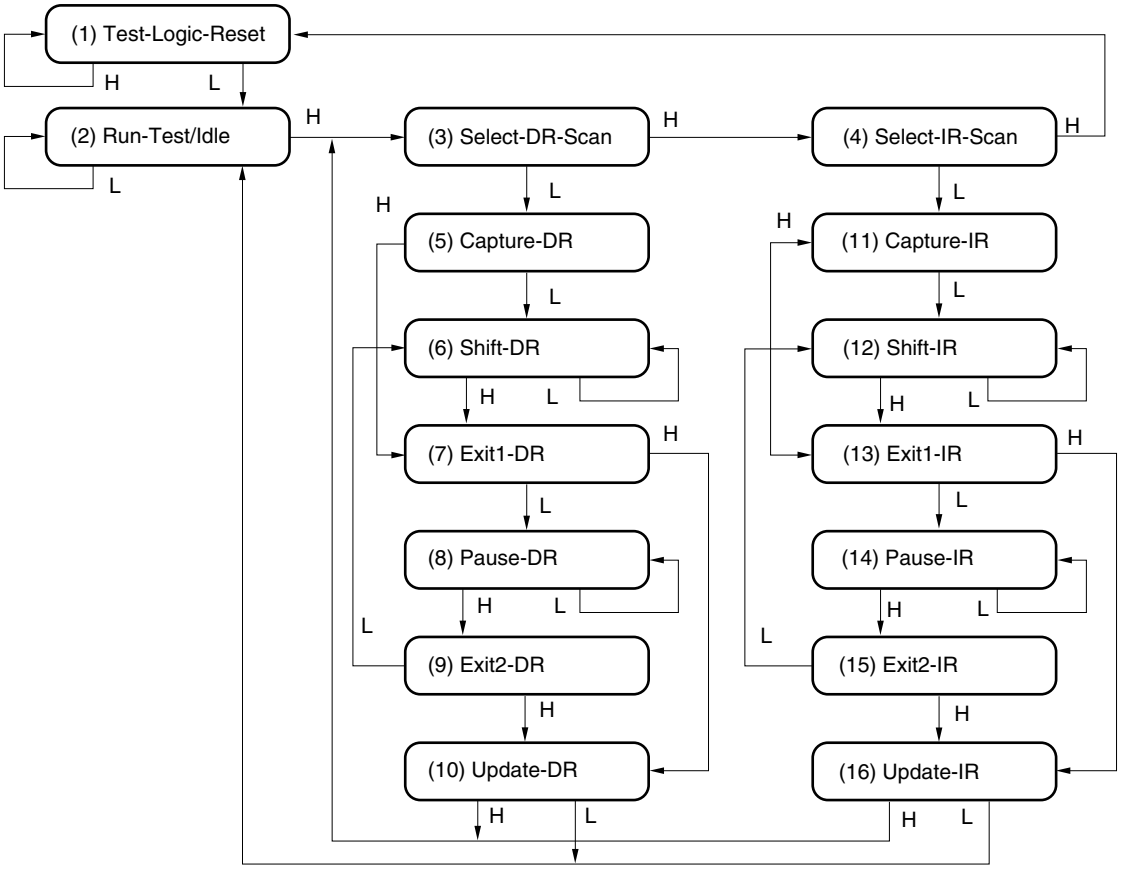
### 6.4.1 TAP controller

The TAP controller is a circuit having 16 states synchronized with changes of the JMS and JCK pins. Its operation is specified by IEEE Standard 1149.1.

### 6.4.2 TAP controller state

Figure 6-2 shows the state transition of the TAP controller. The state of the TAP controller is determined depending on the state of the JMS pin signal input at the rising edge of the clock input to the JCK pin. The operations of the instruction register, boundary scan register, and bypass register change at the rising or falling edge of the clock input to the JCK pin. (Refer to **Figure 6-3**).

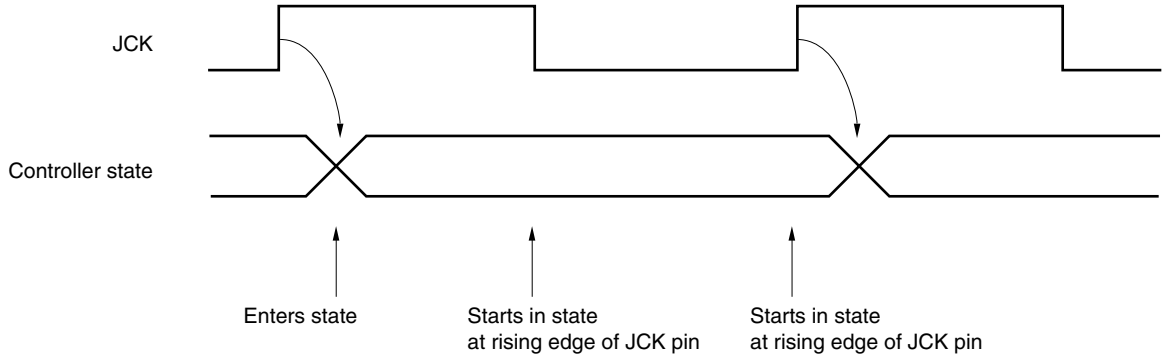
**Figure 6-2. State Transition of TAP Controller**




**Remarks 1.** "H" and "L" of the arrows indicating state transition in the above figure indicate the state of the JMS pin at the rising edge of the clock input to the JCK pin.

**2.** Numbers in ( ) in the above figure correspond to the explanation below.

**Figure 6-3. Operation Timing in Controller State**




**(1) Test-Logic-Reset**

The boundary scan circuit performs no operation on the μPD98404. Therefore, it does not affect the system logic of the μPD98404. This is because the bypass instruction is stored to the instruction register and executed on initialization. The TAP controller enters the Test-Logic-Reset state if the JMS pin holds the high level for the duration of at least five rising edges of the JCK pin signal, regardless of the current state of the controller. The TAP controller holds this state for the duration in which the JMS pin signal high.

If the TAP controller must be in the Test-Logic-Reset state, the controller returns to the original Test-Logic-Reset state even if a low-level signal is input once to the JMS pin by mistake (due to, for example, the influence of the external interface), if the JMS pin signal holds its high level status for the duration of three rising edges of the JCK pin signal.

The operation of the test logic does not hinder the logic operation of the μPD98404 due to the above error.

When the TAP controller exits from the Test-Logic-Reset state, the controller enters the Run-Test/Idle state. In this state, no operation is performed because the current instruction is set by the operation of the bypass register. The logic operation of the JTAG boundary scan circuit is inactive even in the Select-DR-Scan and Select-IR-Scan states.

**(2) Run-Test/Idle**

The TAP controller is in this state during scan operation (in Select-DR-Scan or Select-IR-Scan state). Once the controller has entered this state and if the JMS pin signal holds the low level, the controller remains in this state. The controller enters the Select-DR-Scan state if the JMS pin signal holds high level at one rising edge of the JCK pin signal.

All the test data registers (boundary register and bypass register) selected by the current instruction hold the previous status (Idle). While the TAP controller is in this state, the instruction does not change.

**(3) Select-DR-Scan**

This is a temporary boundary scan state. The boundary scan register and bypass register selected by the current instruction hold the previous state.

If the JMS signal is held low at the rising edge of the JCK pin signal while the TAP controller is in this state, the controller enters the Capture-DR state, and scan sequence to the selected registers is started.

If the JMS signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Select-IR-Scan state. While the controller is in this state, the instruction does not change.

**(4) Select-IR-Scan**

This is a temporary boundary scan state. The boundary scan register and bypass register selected by the current instruction hold the previous state.

If the JMS signal is held low at the rising edge of the JCK pin signal while the TAP controller is in this state, the controller enters the Capture-IR state, and scan sequence to the selected registers is started.

If the JMS signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Test-Logic-Reset state. While the controller is in this state, the instruction does not change.

**(5) Capture-DR**

In this controller state, data is loaded to the boundary scan register selected by the current instruction in parallel at the rising edge of the JCK pin signal (in this case, data is input from the input pin of each device to the corresponding boundary scan register). While the TAP controller is in this state, the instruction does not change.

If the TAP controller is in this state at the rising edge of the JCK pin signal, the controller enters the following state:

- If the JMS pin signal is held high: Exit1-DR state
- If the JMS pin signal is held low : Shift-DR state

**(6) Shift-DR**

In this controller state, JDI and JDO are connected (at either of the boundary scan register of bypass register) by the current instruction. The shift data is shifted one state at a time toward the serial output direction at each rising edge of the JCK pin signal.

The boundary scan register or bypass register selected by the current instruction holds the previous status without change if the controller is not on the serial bus (not in the Shift-DR state). While the controller is in this state, the instruction does not change.

If the TAP controller is in this state at the rising edge of the JCK pin signal, the controller enters the following state:

- If the JMS pin signal is held high: Exit1-DR state
- If the JMS pin signal is held low : Shift-DR state

**(7) Exit1-DR**

This is a temporary controller state. If the JMS pin signal is held high at the rising edge of the JCK pin signal with the TAP controller in this state, the controller enters the Update-DR state. This ends the scan process.

If the JMS pin signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Pause-DR state.

Both the bypass register and boundary scan register selected by the current instruction hold the previous status without change. While the TAP controller is in this state, the instruction does not change.

**(8) Pause-DR**

In this controller state, shifting between JDI and JDO connected by either the bypass register or boundary scan register is temporarily stopped. These registers selected by the current instruction hold the previous state without change.

The TAP controller remains in this state while the JMS pin signal is low. If the JMS pin signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Exit2-DR state. While the TAP controller is in this state, the instruction does not change.

**(9) Exit2-DR**

This is a temporary controller state. If the JMS pin signal is held high at the rising edge of the JCK pin signal with the TAP controller in this state, the controller enters the Update-DR state. This ends the scan process.

If the JMS pin signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Shift-DR state.

Both the bypass register and boundary scan register selected by the current instruction hold the previous status without change. While the TAP controller is in this state, the instruction does not change.

**(10) Update-DR**

The boundary scan register has a parallel output latch to prevent changes in parallel output (while shifted to the shift register path concatenated) by certain instructions (for example, EXTEST instruction).

In the Update-DR controller state, data is latched from the shift register to the parallel output latch of this register at the falling edge of the JCK pin signal.

The data retained latched to the parallel output latch changes depending on this controller state (the data does not change with the other controller states).

The previous states of all the shift register of the boundary scan register selected by the current instruction are retained.

While the TAP controller is in this state, the instruction does not change.

If the JMS pin signal is held high at the rising edge of the JCK pin signal with the TAP controller in this state, the controller enters the Select-DR-Scan state.

If the JMS signal is held low at the rising edge of the JCK signal, the TAP controller enters the Run-Test/Idle state.

**(11) Capture-IR**

In this controller state, the shift register loads the pattern of a fixed logic value [01 (binary)] to the instruction register at the rising edge of the JCK pin signal.

The previous states of both the bypass register and boundary scan register selected by the current instruction are retained without change.

While the TAP controller is in this state, the instruction does not change.

If the JMS pin signal is held high at the rising edge of the JCK pin signal while the controller is in this state, the controller enters the Exit1-IR state.

If the JMS pin signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Shift-IR state.

**(12) Shift-IR**

In this controller state, JDI and JDO are connected by the shift register in the instruction register. The shift data is shift one state toward the serial output direction at each rising edge of the JCK pin signal.

The boundary scan register or bypass register selected by the current instruction holds the previous state without change.

While the TAP controller is in this state, the instruction does not change.

If the JMS pin signal is held high at the rising edge of the JCK pin signal with the TAP controller in this state, the controller enters the Exit1-IR state. If the JMS pin signal is held low, the controller remains the Shift-IR state.

**(13) Exit1-IR**

This is a temporary controller state. If the JMS pin signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Update-IR state. This ends the scan process.

If the JMS pin signal is held low at the rising edge of the JCK pin, the TAP controller enters the Pause-IR state.

Both the bypass register and boundary scan register selected by the current instruction retain their states without change.

While the TAP controller is in this state, the instruction does not change.

**(14) Pause-IR**

In this controller state, shift of the instruction register is temporarily stopped. The bypass register and boundary scan register selected by the current instruction hold the previous state without change.

While the TAP controller is in this state, the instruction does not change. The instruction register holds the current state.

While the JMS pin signal is low, the TAP controller remains in this state. If the JMS pin signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Exit2-IR state.

**(15) Exit2-IR**

This is a temporary controller state. If the JMS pin signal is held high at the rising edge of the JCK pin signal, the TAP controller enters the Update-IR state. This ends the scan process.

If the JMS pin signal is held low at the rising edge of the JCK pin, the TAP controller enters the Shift-IR state.

Both the bypass register and boundary scan register selected by the current instruction retain their states without change.

While the TAP controller is in this state, or while the instruction register holds the current state, the instruction does not change.

**(16) Update-IR**

In this controller state, the instruction shifted to the instruction register is latched to the parallel output latch from the shift register path at the falling edge of the JCK pin signal. Once a new instruction has been latched, it is used as the current instruction.

The bypass register or boundary scan register selected by the current instruction holds the previous state.

If the JMS pin signal is held high at the rising edge of the JCK pin signal while the TAP controller is in this state, the TAP controller enters the Select-DR-Scan state.

If the JMS pin signal is held low at the rising edge of the JCK pin signal, the TAP controller enters the Run-Test/Idle state.

The Pause-DR controller state in (8) and Pause-IR controller state in (14) temporarily stop shifting of data in the boundary scan register or instruction register.

## 6.5 TAP Controller Operation

The TAP controller operates as follows.

The state of the controller is changed by either of (1) and (2) below.

(1) Rising edge of JCK pin signal
(2) JRST_B pin input

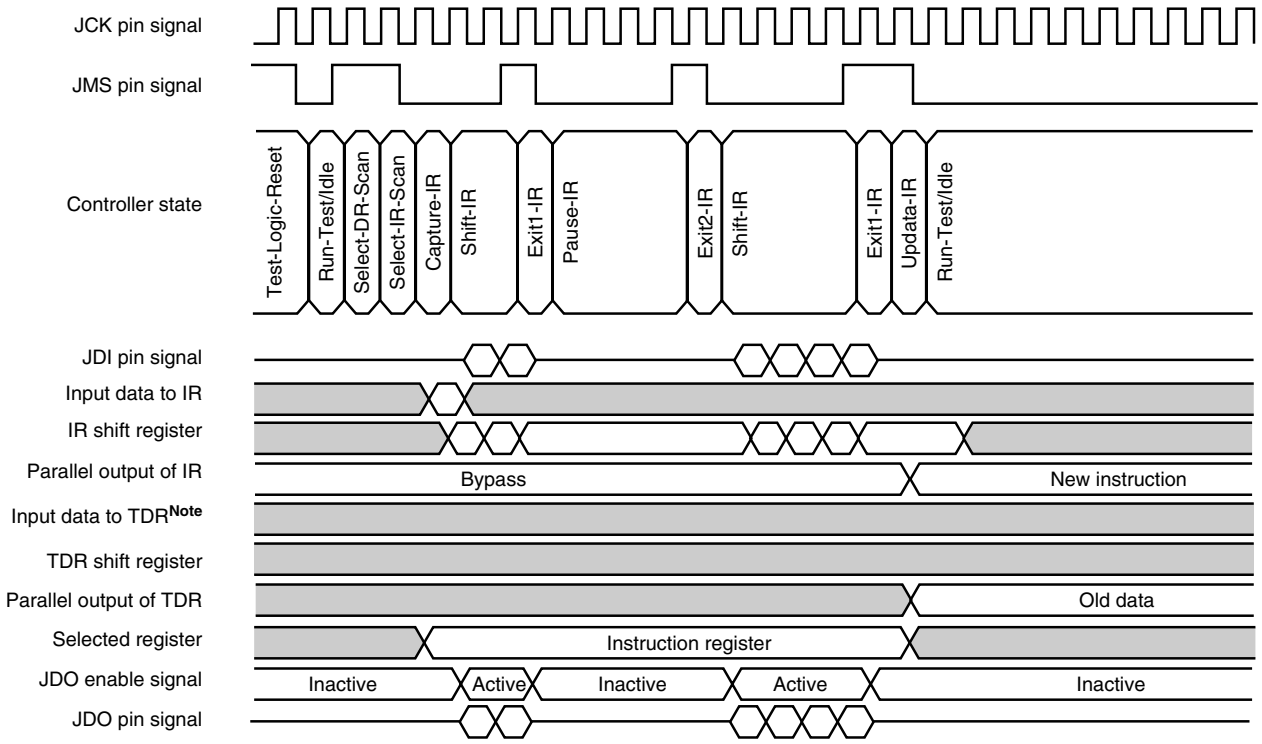
The TAP controller generates signals that control the operations of the bypass register, boundary scan register, and instruction register defined by the IEEE1149.1 JTAG Boundary Scan Standard (refer to **Figures 6-4** and **6-5**).

The JDO pin output buffer and the peripheral circuit that selects a register whose contents are to be output to the JDO pin are controlled as shown in Table 6-1. The JDO pin defined in this table changes at the falling edge of the JCK pin signal after it has entered each state.

**Table 6-1. Operation in Each Controller State**

| Controller State | Selected Register to Be Driven to JDO Pin | JDO Pin Driver |
|---|---|---|
| Test-Logic-Reset | Undefined | High impedance |
| Run-Test/Idle | | |
| Select-DR-Scan | | |
| Select-IR-Scan | | |
| Capture-IR | | |
| Shift-IR | Instruction register | Active |
| Exit1-IR | Undefined | High impedance |
| Pause-IR | | |
| Exit2-IR | | |
| Update-IR | | |
| Capture-DR | | |
| Shift-DR | Data register (boundary scan register, bypass register) | Active |
| Exit1-DR | Undefined | High impedance |
| Pause-DR | | |
| Exit2-DR | | |
| Update-DR | | |

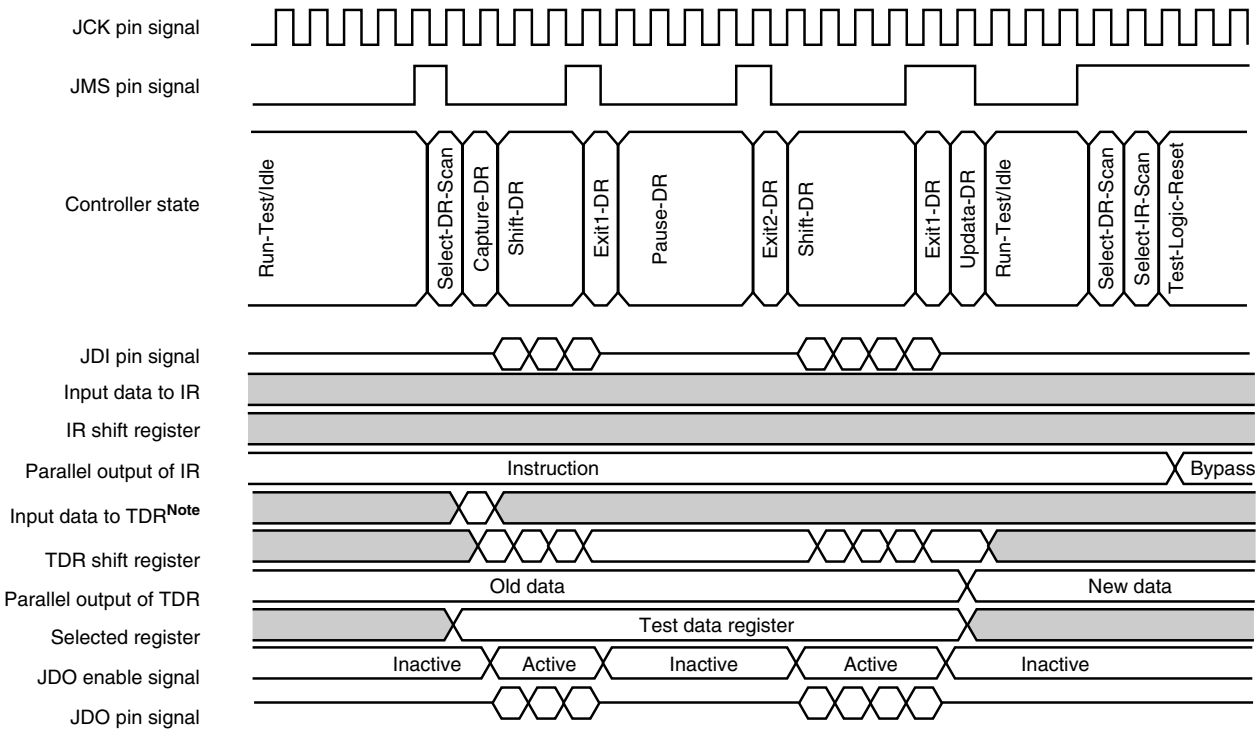
**Figure 6-4. Operation of Test Logic (instruction scan)**




**Note** TDR (Test Data Register): Boundary scan register and bypass register

**Remark** : Don't care or undefined

**Figure 6-5. Operation of Test Logic (data scan)**




**Note** TDR (Test Data Register): Boundary scan register and bypass register

**Remark** ▭: Don't care or undefined

## 6.6 Initializing TAP Controller

The TAP controller is initialized as follows:

(1) The TAP controller is not initialized by the operation of system input such as system reset.
(2) The TAP controller enters the Test-Logic-Reset controller state at the fifth rising edge of the JCK pin signal (while the JMS pin signal is held high).
(3) The TAP controller asynchronously enters the Test-Logic-Reset state when the JRST_B signal is input.

## 6.7 Instruction Register

This register is defined as follows (refer to **6.2 Internal Configuration of Boundary Scan Circuit**).

(1) The instruction shifted and input to the instruction register is latched so that it changes only in the Update-IR and Test-Logic-Reset controller states.
(2) Data is not inverted since it has been serially input to the instruction register until it is serially output.
(3) A fixed binary pattern data “01” (with LSB (Least Significant Bit) being “1”) is loaded to this register cell in the Capture-IR controller state.
(4) A fixed binary pattern data “01” (with LSB (Least Significant Bit) being “1”) is loaded to this register cell in the Test-Logic-Reset controller state.
(5) While this register is read, data is output from the JDO pin, starting from the LSB to the MSB, at each falling edge of the JCK pin signal.

The JTAG boundary scan circuit of the μPD98404 can support only the following two instructions depending on the data set to the instruction register.

- BYPASS instruction
- EXTEST instruction
- SAMPLE/PRELOAD instruction

| Instruction Register | | Supported Instruction |
|---|---|---|
| D1 | D0 | |
| 0 | 0 | EXTEST instruction |
| 0 | 1 | SAMPLE/PRELOAD instruction |
| 1 | 0 | Unused (BYPASS instruction) |
| 1 | 1 | BYPASS instruction |

### 6.7.1 BYPASS instruction

This instruction is specified by instruction data “11”. This instruction is used to select only the bypass register (to access between the JDI and JDO pins serially) in the Shift-DR controller state.

While this instruction is selected, the operation of the JTAG boundary scan circuit does not affect the operation of the μPD98404.

This bypass instruction is selected while the TAP controller is in the Test-Logic-Reset state.

### 6.7.2 EXTEST instruction

This instruction is specified by instruction data “00”. In the Shift-DR controller state, this instruction is used to select the boundary scan register of serial access between the JDI and JDO instructions.

- While this instruction is selected:

  The states of all the signals driven from the system output pins are completely defined by the data shifted to the boundary scan register. In the Update-DR controller state, the states of all the signals are changed only by the falling edge of the JCK pin signal.

  The states of all the signals input from the system input pins are loaded to the boundary scan register at the rising edge of the JCK pin signal while the TAP controller is in the Capture-DR state.

### 6.7.3 SAMPLE/PRELOAD Instruction

This instruction is specified by setting "01" as the instruction data. This instruction executes the SAMPLE function and PRELOAD function in one instruction.

### 6.7.4 Boundary scan data bit definition

In response to customer requests, NEC Electronics has made available the BSDL (Boundary Scan Description Language) reference file for the μPD98404. To obtain this file, contact an NEC Electronics sales representative.

# CHAPTER 7 BOARD LAYOUT

Because the μPD98404 has an internal PLL circuit that is susceptible to noise, consideration must be given when designing the layout of the power supply and ground on the board so that the PLL circuit is not affected by noise as for as possible.

The power supply and ground pins of the μPD98404 can be classified into the six types shown in Table 7-1 by the block to which the power is supplied. The power on <2> through <6>, and not logic supply <1>, is supplied to the internal PLL block and high-speed operation circuit block, and the noise superimposed on this power supply affects the jitter output and immunity of the PLL. It is necessary to take measures against the noise from signal lines.

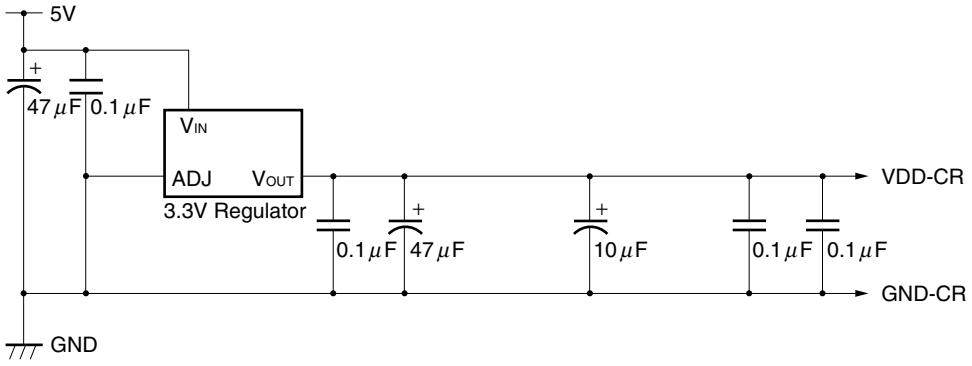
★ **Table 7-1. Power and Ground Pins of μPD98404**

| | Pin Name | Pin No. | I/O | Function |
|---|---|---|---|---|
| <1> | VDD | 1, 27, 36, 60, 73, 95, 108, 119, 129 | – | General logic power supply (+3.3 V±0.15 V) and ground |
| | GND | 16, 37, 71, 72, 86, 102, 109, 110, 124, 143, 144 | – | |
| <2> | VDD-TPE | 39, 45, 49 | – | Power supply (+3.3 V±0.15 V) and ground for output PECL I/O |
| | GND-TPE | 42, 46 | – | |
| <3> | VDD-RPE | 53 | – | Power supply (+3.3 V±0.15 V) and ground for input PECL I/O |
| | GND-RPE | 50, 56 | – | |
| <4> | VDD-SP | 35 | – | Power supply (+3.3 V±0.15 V) and ground for serial/ parallel block |
| | GND-SP | 38 | – | |
| <5> | VDD-CS | 32, 33 | – | Power supply (+3.3 V±0.15 V) and ground for clock synthesizer PLL block |
| | GND-CS | 29, 30, 34 | – | |
| <6> | VDD-CR | 58 | – | Power supply (+3.3 V±0.15 V) and ground for clock recovery PLL block |
| | GND-CR | 57 | – | |

**(1) Inserting capacitor**

Connect a pass capacitor to each power supply pin. In particular, connect a 10 μF capacitor and a 0.1 μF capacitor pair to the power supply pins <2> through <6>. Locate the 0.1 μF capacitors as close to the pins as possible. Closely connecting two or more capacitors in parallel to the pins is an effective countermeasure against noise.

**Figure 7-1. Example of Capacitor Insertion**

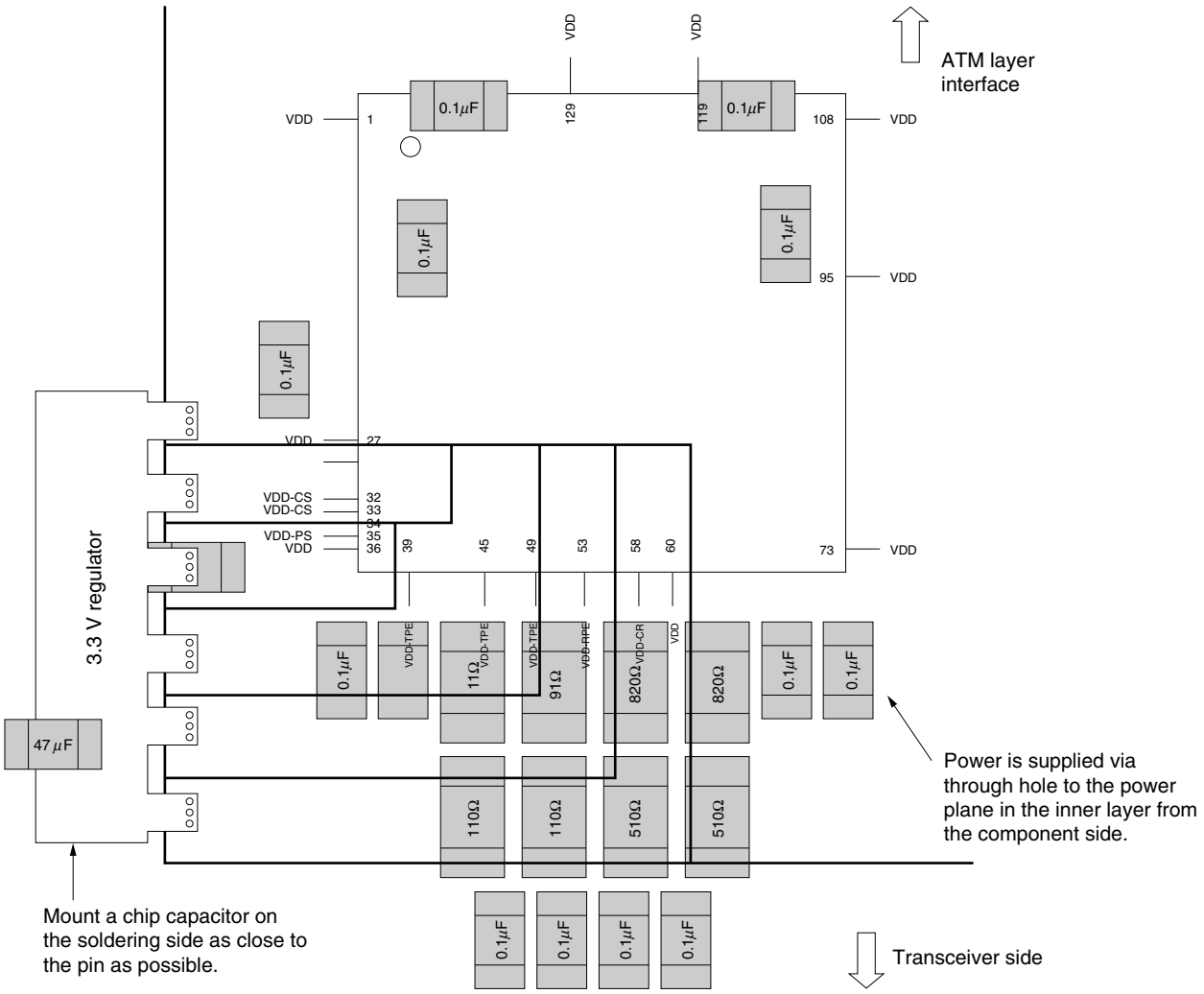


**(2) Separating power planes**

Separate the planes from the power supply to the power supply pins of the μPD98404 by using a splitter to prevent noise from the power supply affecting the power supply pins. However, make sure that the area of each power plane is as large as possible to prevent the impedance of each plane from increasing as a result of dividing the plane into small groups.

In particular, because the power consumption of the PECL I/O block to which the VDD-TPE pin <2> supplies power is high, the area of the plane including this block must be accordingly large.

**Figure 7-2. Board Layout Image**




**(3) Interface at circuit side**

Locate the μPD98404 and transceiver as closely as possible and keep the transmit/receive data lines of TDOT/TDOC and RDIT/RDIC as short as possible.

# CHAPTER 8 CONSTRAINTS

Two constraints apply to the μPD98404. Make sure you thoroughly understand these constraints when using the μPD98404.

## 8.1 Constraints

(1) Abnormal clearing of performance counter
(2) Abnormal output of RCLAV signal in RCASEL = 1 mode
(3) Abnormal operation in ALP mode
(4) Fixed receiver circuit status in RPLP mode

## 8.2 Description

### 8.2.1 Clearing error of performance counter

**(1) Description**

If the counter is sampled by setting the SMP bit of the PCSR register to 1 or cleared by the PCIR1 or PCIR2 register when the counter is stopped (under condition 2 to be described below), the counter may not be correctly cleared to 0. The counter value sampled by the software should be the total value of time from the previous sampling to the current sampling. If sampling is executed while the counter is stopped such as because LOS has been detected, the sampled counter value is valid. However, the counter value sampled next is invalid because the counter continues totaling without being cleared.

This problem occurs in all the 10 counters of the μPD98404 (B1 error, B2 error, B3 error, Line-REI, Path-REI, FJ, HEC, FIFO full, idle cell, and information cell counters).

**(a) Stopping condition of counter**

<1> Stop command by using PCFR1 and PCFR2 registers
<2> Stopping counter due to occurrence of LOS, LOF, LOP, LAIS, PAIS, or LCD status

**(b) Clearing condition of counter**

<1> SMP bit of PCSR register = 1 (sampling of all counters) : Prohibited
<2> Clear command by using PCIR1 and PCIR2 registers (clearing each counter) : Prohibited
<3> PCR bit of CMR2 register = 1 (resetting all counters) : OK

**(2) Countermeasures**

Of the above three methods of clearing the counter, B-3 (resetting all counters by setting the PCR bit of the CMR2 register to 1) can be executed without problem even while the counter is stopped. When a counter is sampled or cleared, the counter must be cleared to 0 by using this command. Resetting all the counters by setting the PCR bit of the CMR2 register resets all the registers related to the counters. If this is executed, the PCFR1 and PCFR2 registers are set to the default value, all the counters are stopped, and the contents of the load register are also cleared. After execution of reset, it takes the circuit 20 cycles of TCLK clock to recover from the reset status. During this time, do not access the registers related to the counter.

**(a) Example of countermeasures against counter sampling**

<1> Release the stop on the counter by using the PCFR1 and PCFR2 registers (starting counting).

<2> Sample the counter by setting the SMP bit of the PCSR register to 1.

<3> Read the counter value from the load register.

<4> Issue a set command by setting the PCR bit of the CMR2 register to 1.

- All the counters stop because the value of the PCFR1 and PCFR2 registers are returned to the default value.

<5> Wait for the duration of TCLK clock cycle x 20.

<6> Release the stop on the counter by using the PCFR1 and PCFR2 registers (resuming counting).

### 8.2.2 Output error of RCLAV signal in RCASEL = 1 mode

**(1) Description**

The RCLAV signal does not operate as specified when the RCASEL bit of the MDR3 register is 1. The RCLAV signal should go high when one cell of data has been stored in the receive FIFO. In the mode in which the RCASEL bit = 1, however, the RCLAV signal does not go high unless data of two cells have been stored in the receive FIFO. When the receive FIFO no longer has data to transfer, the RCLAV signal does not go low as soon as the second byte of the cell being transferred has been output. Instead, the RCLAV signal goes low when one cell remains in the receive FIFO.

Because of this problem, the high-end ATM layer device cannot enable output of one cell data in the receive FIFO of the $\mu$PD98404 by using the RENBL_B signal. Consequently, one cell always remains in the receive FIFO of the $\mu$PD98404,

This problem occurs only in the cell handshake mode of RCASEL = 1, and does not occur in the mode of RCASEL = 0 (default mode).

**Figure 8-1. Timing of Change in RCLAV**

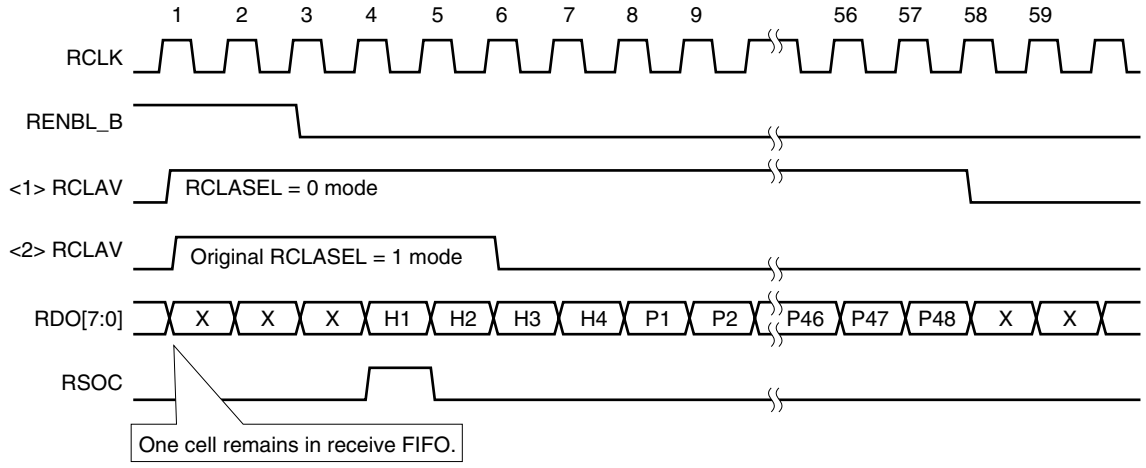



**Figure 8-2. Problem of RCLAV (1) (if the number of cells in receive FIFO increases from 0 to 2)**

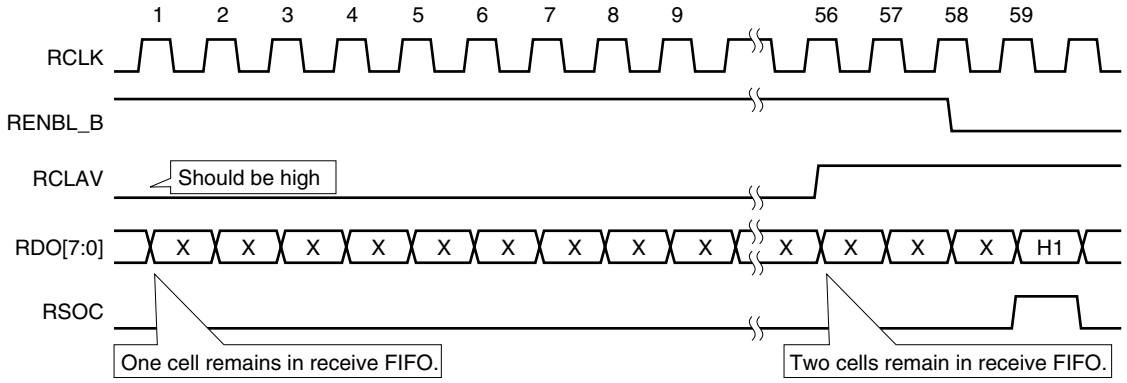
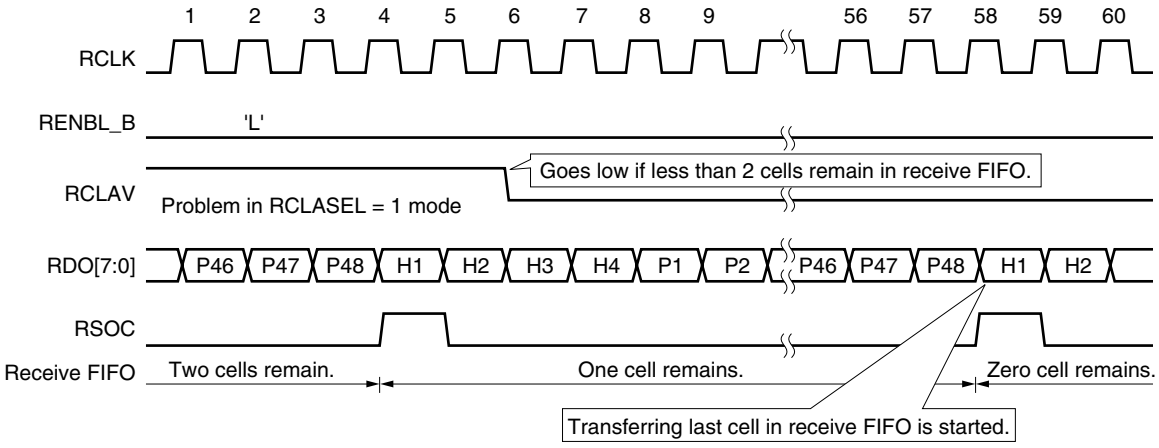



**Figure 8-3. Problem of RCLAV (2) (if the number of cells in receive FIFO increases from 3 to 0)**



**(2) Countermeasures**

(a) Do not use the mode in which the RCASEL bit of the MDR3 register is 1.

(b) To avoid the state where only one cell remains in the receive FIFO, input received idle cells and unassigned cells to the receive FIFO.

The idle cells and unassigned cells pass the receive FIFO and can be output to the UTOPIA interface side by setting the DCHPR and DCHPMR registers as follows:

DCHPR register (address 27H) : FFH
DCHPMR register (address 28H) : 00H

Because the idle cells and unassigned cells that are supposed to be discarded by the μPD98404 are output to the UTOPIA interface, the ATM layer device must discard these cells. In addition, because the μPD98404 always outputs cells at the full rate of 149.76 Mbps, the number of connectable μPD98404s is limited if two or more μPD98404s are connected to one UTOPIA interface.

**<<Supplement>>**

By using the EMPTY_B/RCLAV signal of the UTOPIA interface, the μPD98404 notifies the status of the receive FIFO to the high-end ATM layer device. In the octet level handshake mode (UMPSEL pin = low level, CSEL bit of MDR1 register = 0), this signal functions as EMPTY_B signal and goes high if one byte or more of valid data exists in the receive FIFO. In the cell level handshake mode (UMPSEL pin = low or high, CSEL bit of MDR1 register = 1), the EMPTY_B/RCLAV signal functions as RCLAV and goes high if one cell or more of valid data exists in the receive FIFO. In the cell handshake mode, the RCLAV signal changes in the following two modes. These modes can be selected by using the RCASEL bit of the MDR3 register. Note that the problem mentioned above occurs when RCASEL = 1.

RCASEL = 0: The RCLAV signal is kept high up to the end of the cell being transferred, and RCLAV signal is changed to indicate whether a cell to be transferred next exists, in the clock cycle following the end of the first cell.

RCASEL = 1: The RCLAV signal is changed to indicate whether data to be transferred next exists in a cycle following the second byte of the cell being transferred.

### ★ 8.2.3 Abnormal operation in ALP mode

**(1) Description**

When the μPD98404 is set in the ALP mode, the cell data output to the ALM layer side may be damaged (the data output to the PMD layer side is not damaged).

The ALP mode is used to loopback cell data from the transmit FIFO to the receive FIFO. When data is looped back in this mode, the data synchronized with the transmitter circuit clock (TCL) is re-synchronized with the receiver circuit clock (RCL). The data may be damaged due to a defect in the circuit that changes the synchronization clock.

This abnormal operation occurs if the timing relationship between the clock and data violates the setup/hold time when the phase delay of the data changes due to the operating temperature, voltage, or production variation.

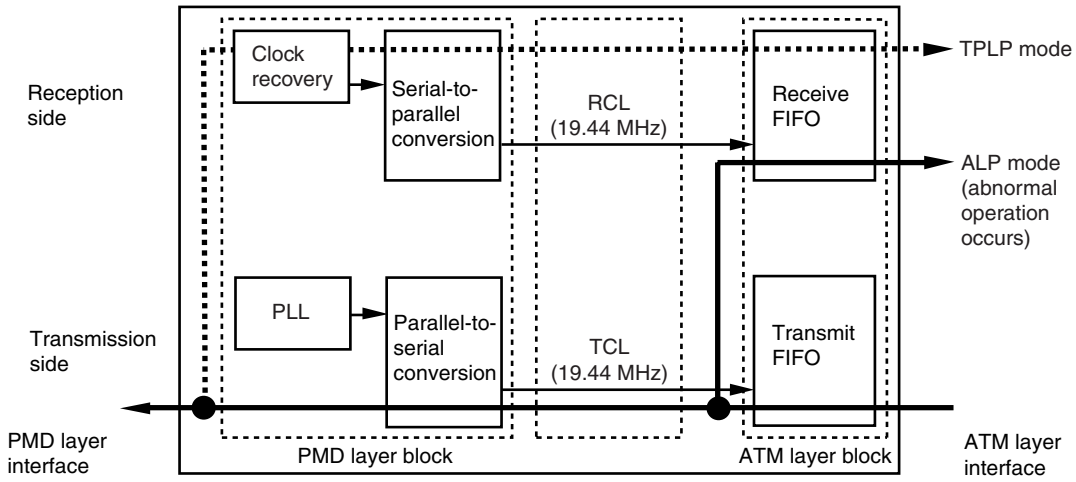
The probability that an abnormal operation occurs in the ALP mode is theoretically 1/8 because the TCL and RCL clocks (19.44 MHz) and both the source clocks (155.52 MHz) are in a 1-to-8 relationship.

Once this abnormal operation has occurred, the damaged data continues to be output until the ALP mode is cleared or the LSI is reset.

**(2) Countermeasures**

Do not use the ALP mode. Use the TPLP mode. The TPLP mode returns the cell data input from the ATM layer interface at the block on the serial side, and outputs the data to the ATM layer side as a receive cell.

**Figure 8-4. ALP Mode and TPLP Mode**



### ★ 8.2.4 Fixed receiver circuit status in RPLP mode

**(1) Description**

When the μPD98404 operates in the RPLP mode, the status bit that should be set, or read and cleared in accordance with changes in the status of the receiver circuit is fixed to the status in which the RPLP mode was set.

The RPLP mode is used to loopback serial data received from the circuit side to the serial output at the transmission side before the serial-to-parallel converter.

The fixed-status abnormality occurs in the LOS (Loss Of Signal) and LOF (Loss Of Frame) bits of the PICR register, and the LCD (Loss of Cell Delineation) bit of the ACR register. The status bits other than the LOS, LOF, and LCD bits indicate the input status of the receiver circuit. The actual data that is looped back has no problem.

**<Example of phenomenon>**

- If an error frame is input during normal operation, the μPD98404 sets the LOF bit to 1.
- After setting the μPD98404 in the RPLP mode, input of normal frame is switched.
- If the PICR register is read after the time in which the clearing condition of LOF is satisfied has elapsed, the LOF bit should be cleared to 0. In the RPLP mode, however, it remains set to 1 no matter how many times it is read. The data to be looped back is the normal frame input to the reception side.

This phenomenon occurs only in the RPLP mode. In the normal mode, the LOS, LOF, and LCD bits are updated according to the status of the receiver circuit.

**(2) Countermeasures**

This phenomenon occurs because clock distribution to the circuit that controls detection/clearing of the LOS, LOF, and LCD statuses stops when the path of data and clock is switched inside the LSI to output receive data to the transmission side. To update indication of the LOS, LOF, and LCD statuses in the RPLP mode, the clock mode must be changed as follows when the RPLP mode is set.

MDR1 register [D3] (TxCL0) = 1
MDR2 register [D6] (oolenb) = 1

Set these bits to 1 when setting the RPLP mode and clear them to 0 when clearing the mode. This mode switching is not necessary in principle, but should be evaluated as a countermeasure.

If the oolenb bit is set to 1 as the initial setting, it does not have to be set and cleared (refer to **5.2 (5) Mode register 2 (MDR2)**, **4.2.1 (1) • Receive clock recovery PLL function)**.

**Figure 8-5. RPLP Mode**