User's Manual

8

# μPD78F807x Microcontroller with LIN Transceiver & Half-Bridge Drivers

## User's Manual: Hardware

## RENESAS MCU
## μPD78F807x Microcontroller

μPD78F8071(A)
μPD78F8072(A)
μPD78F8073(A)
μPD78F8074(A)
μPD78F8075(A)
μPD78F8077D



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NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

# How to Use This Manual

**Readers** This manual is intended for user engineers who wish to understand the functions of the μPD78F807x, and to design and develop application systems and programs for this device.

**Purpose** This manual is intended to give users an understanding of the functions described in the **Organization** below.

**Organization** There are four manuals for the μPD78F807x microcontroller: this manual, 78K0/Kx2 User's Manual, 78K0/Kx2 ROM Expansion Products User's Manual, and the Instructions edition (common to the 78K0 Series).

| μPD78F807x Microcontroller **User's Manual** | 78K0/Kx2 **User's Manual** | 78K0/Kx2 ROM Expansion Products **User's Manual** |
|---|---|---|
| • Pin functions<br>• Internal block functions<br>• On-chip peripheral functions<br>• Electrical specifications | • Pin functions<br>• Internal block functions<br>• Interrupts<br>• Other on-chip peripheral functions<br>• Electrical specifications | • CPU architecture<br>• Memory bank switching function<br>• Multiplier/divider<br>• Flash memory |

| 78K/0 Series User's Manual Instructions |
|---|
| • CPU functions<br>• Instruction set<br>• Explanation of each instruction |

**How to Read This Manual** It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

- To gain a general understanding of functions:
  → Read this manual in the order of the **CONTENTS**. The mark "<R>" shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

- The notation of the product name

  → Description of (A) is omitted in this manual. "(A)" product names should be read as follows.

  - μPD78F8071 → μPD78F8071(A)
  - μPD78F8072 → μPD78F8072(A)
  - μPD78F8073 → μPD78F8073(A)
  - μPD78F8074 → μPD78F8074(A)
  - μPD78F8075 → μPD78F8075(A)

- To know details of the microcontroller block:

  → Refer to the separate documents: **78K0/Kx2 User's Manual (R01UH0008) and** 78K0/Kx2 ROM Expansion Products User's Manual (U19719E).

| 78K0/KC2 Microcontroller Products | Product Name corresponding to 78K0/KC2 Microcontroller Products |
|---|---|
| μPD78F0511A | μPD78F8071 |
| μPD78F0512A | μPD78F8072 |
| μPD78F0513A | μPD78F8073 |
| μPD78F0514A | μPD78F8074 |
| μPD78F0515A | μPD78F8075 |
| μPD78F0517DA | μPD78F8077D |

- To know details of the 78K0 microcontroller instructions:

  → Refer to the separate document: **78K/0 Series Instructions User's Manual (U12326E)**.

| | | |
|---|---|---|
| **Conventions** | Data significance: | Higher digits on the left and lower digits on the right |
| | Active low representations: | $\overline{\times\times\times}$ (overscore over pin and signal name) |
| | **Note**: | Footnote for item marked with **Note** in the text |
| | **Caution**: | Information requiring particular attention |
| | **Remark**: | Supplementary information |
| | Numerical representations: | Binary ···××××  or ××××B |
| | | Decimal ···×××× |
| | | Hexadecimal ···××××H |

**Related Documents** The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

| Document Name | Document No. |
|---|---|
| μPD78F807x Microcontroller with LIN Transceiver & Half-Bridge Drivers User's Manual: Hardware | This Manual |
| 78K0/Kx2 User's Manual | R01UH0008 |
| 78K0/Kx2 ROM Expansion Products User's Manual | U19719E |
| 78K/0 Microcontroller Instructions User's Manual | U12326E |
| 78K0/Kx2 Flash Memory Programming (Programmer) Application Note | U17739E |
| 78K0 Microcontrollers Self Programming Library Type01 User's Manual | U18274E |
| 78K0 Microcontrollers EEPROM™ Emulation Library Type01 User's Manual | U18275E |

Documents Related to Flash Memory Programming

| Document Name | Document No. |
|---|---|
| PG-FP5 Flash Memory Programmer User's Manual | R20UT0008 |

Other Documents

| Document Name | Document No. |
|---|---|
| RENESAS MICROCOMPUTER GENERAL CATALOG | R01CS0001E |
| Semiconductor Package Mount Manual | **Note** |
| Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD) | C11892E |
| Review of Quality and Reliability Handbook Information | C12769E |

**Note** See the "Semiconductor Package Mount Manual" website (http://www.renesas.com/products/package/manual/index.jsp)

**Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.**

Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, inc.

**CONTENTS**

# 1. Outline

μPD78F807x is an MCP (Multi-Chip Package) which includes 2 chips in 1 package: an analog chip (incorporating the LIN transceiver, power supply, six-channel half-bridge drivers) and an 8-bit microcontroller chip. The 78K0/KC2 is used in the 8-bit microcontroller block of μPD78F807x.

## 1.1 Features

- ROM, RAM capacities

| ROM Note | High-Speed RAM Note | Expansion RAM Note | Product (64 Pins) |
|---|---|---|---|
| 16 KB | 768 B | - | μPD78F8071 |
| 24 KB | 1 KB | - | μPD78F8072 |
| 32 KB | 1 KB | - | μPD78F8073 |
| 48 KB | 1 KB | 1 KB | μPD78F8074 |
| 60 KB | 1 KB | 2 KB | μPD78F8075 |
| 128 KB | 1 KB | 6 KB | μPD78F8077D |

Note The internal flash memory, internal high-speed RAM capacities, and internal expansion RAM capacities can be changed using the internal memory size switching register (IMS) and the internal expansion RAM size switching register (IXS).

- On-chip single-power-supply flash memory
- Self-programming (with boot swap function)
- On-chip debug function (μPD78F8077D only) Note 1
- On-chip power-on-clear (POC) circuit and low-voltage detector (LVI)
- On-chip watchdog timer (operable with the internal low speed oscillation clock)
- On-chip multiplier/divider Note 2
- On-chip key interrupt function
- I/O ports: μPD78F807x: 26 (N-ch open drain: 2)

Notes 1. The μPD78F8077D has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. Only supported by the product with 48-Kbyte or more flash memory.

- Timer: 7 channels
  - 16-bit timer/event counter: 1 channel
  - 8-bit timer/event counter: 2 channels
  - 8-bit timer: 2 channels
  - Watch timer: 1 channel
  - Watch dog timer: 1 channel
- Serial interface: 3 channels
  - UART (LIN (Local Interconnect Network)-bus supported): 1 channel
  - CSI/UART [Note] : 1 channel
  - IIC: 1 channel

<R> • 10-bit resolution A/D converter: 5 channels
On-chip power supply circuit
Output voltage: 5 V ± 3%
On-chip power supply output function for external sensors
On-chip external dropper auxiliary function
On-chip over current limiter

- LIN transceiver

<R> The LIN transceiver complies with LIN Specifications Rev.2.0, 2.1
Low power consumption achieved with on-chip sleep function
On-chip pull-up resistors for slave applications
On-chip over current limiter

- Driver

Half-bridge driver: 6 channels
On-chip over current limiter

- Overheat protection circuit
- SPI & PWM controller:1 channel

<R>
- Package: 64-pin plastic WQFN (fine-pitch) (9x9)
- Operation ambient temperature: (A) grade products: $T_A$ = -40 to +85 °C

Note Select either of these functions since they share the same pins.

## 1.2 Applications

- Automotive equipment
  System control for body electronic control units
  — Mirror control
  — Flap control, etc.

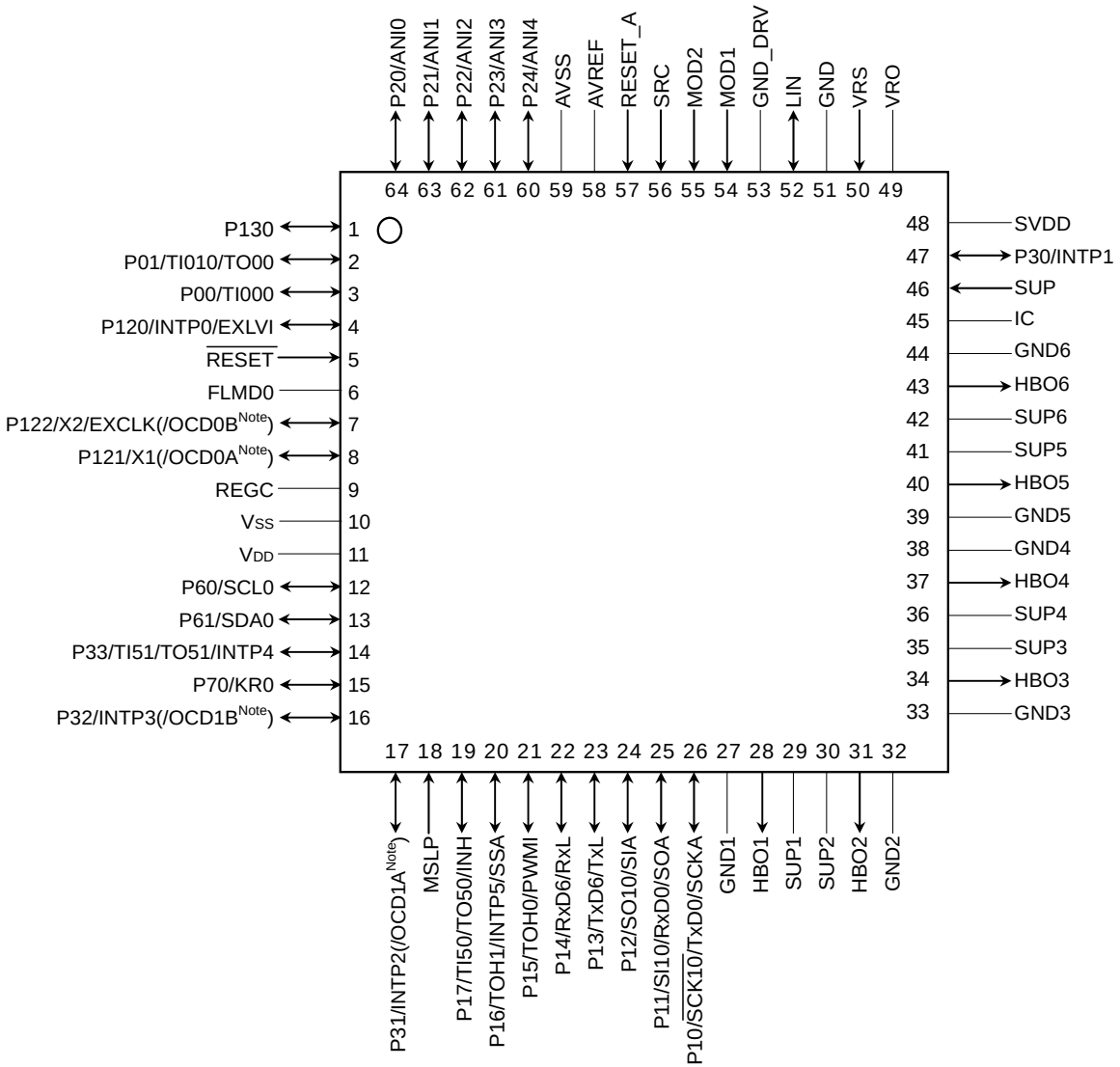
## 1.3 Ordering Information

| Part Number | Package | Quality Grade |
|---|---|---|
| μPD78F8071K8A-6B4-G Note | 64-pin plastic WQFN (fine pitch) (9×9) | Special (for high-reliability electronics equipment) |
| μPD78F8072K8A-6B4-G Note | 64-pin plastic WQFN (fine pitch) (9×9) | Special (for high-reliability electronics equipment) |
| μPD78F8073K8A-6B4-G Note | 64-pin plastic WQFN (fine pitch) (9×9) | Special (for high-reliability electronics equipment) |
| μPD78F8074K8A-6B4-G Note | 64-pin plastic WQFN (fine pitch) (9×9) | Special (for high-reliability electronics equipment) |
| μPD78F8075K8A-6B4-G Note | 64-pin plastic WQFN (fine pitch) (9×9) | Special (for high-reliability electronics equipment) |
| μPD78F8077DK8-6B4-G | 64-pin plastic WQFN (fine pitch) (9×9) | Standard (for general electronics equipment) |

Note (A) grade product

## 1.4 Pin Configuration (Top View)

<R> **64-pin plastic WQFN (fine-pitch) (9×9)**




Note µPD78F8077D (with on-chip debug function) only

Cautions 1. Make GND, GND1 to GND6, and GND_DRV the same potential as VSS and AVSS.

2. Connect the REGC pin to VSS via a capacitor (0.47 µF to 1 µF).

<R> 3. ANI0/P20 to ANI4/P24 are in the analog input mode after reset release.

4. Make SUP the same potential as SUP1 to SUP6.

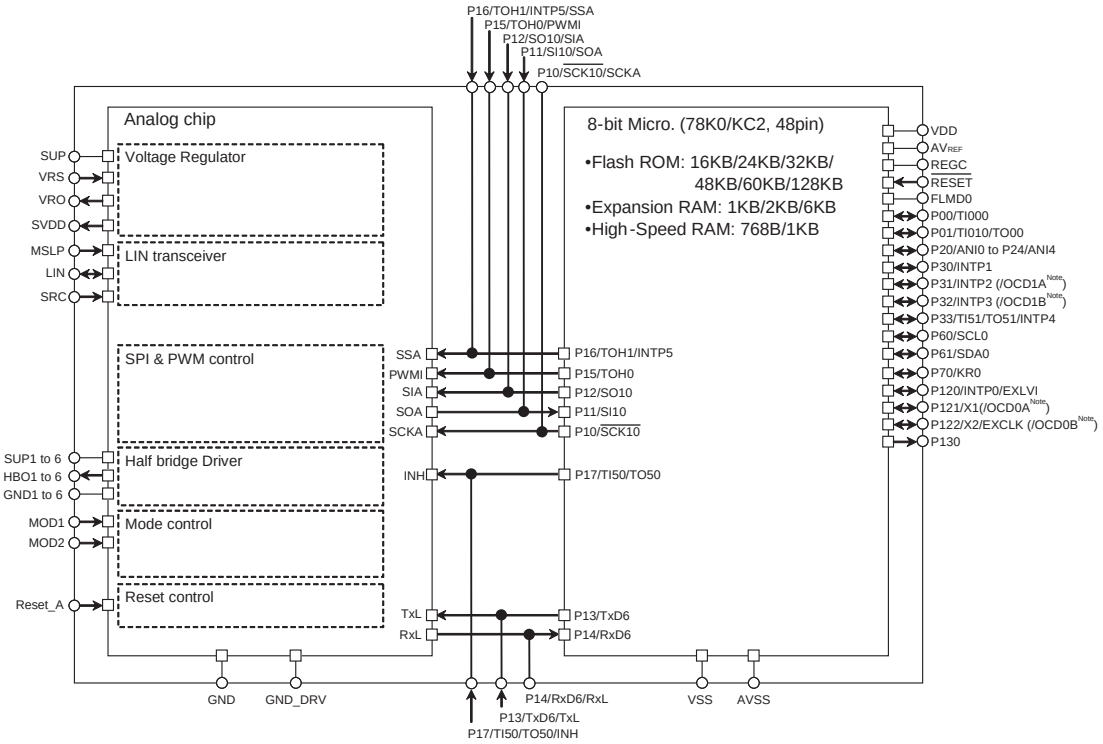
<R> 5. Make VDD the same potential as VRS or VRO when the on-chip P-ch MOS is used for the 5-V output dropper.

<R> 6. Make VDD the same potential as VRS when the external dropper is used for the 5-V output dropper.

## <R> Pin Identification

| | |
|---|---|
| ANI0 to ANI4 | : Analog Input |
| $AV_{REF}$ | : Analog Reference Voltage |
| $AV_{SS}$ | : Analog Ground |
| EXCLK | : External Clock Input (Main System Clock) |
| EXLVI | : External potential Input for Low-voltage detector |
| FLMD0 | : Flash Programming Mode |
| GND | |
| GND1 to GND6 | |
| GND_DRV | : Ground |
| HBO1 to HBO6 | : Half-bridge Driver Output |
| IC | : Internal Connection |
| INTP0 to INTP5 | : External Interrupt Input |
| KR0 | : Key Return |
| LIN | : LIN Bus |
| MOD1, MOD2 | : Pin Mode Control Input |
| MSLP | : Sleep Mode Control Input |
| OCD0A, OCD0B, OCD1A, OCD1B | : On-Chip Debug Input/Output |
| P00, P01 | : Port 0 |
| P10 to P17 | : Port 1 |
| P20 to P24 | : Port 2 |
| P30 to P33 | : Port 3 |
| P60, P61 | : Port 6 |
| P70 | : Port 7 |
| P120 to P122 | : Port 12 |
| P130 | : Port 130 |
| REGC | : Regulator Capacitance |
| $\overline{\text{RESET}}$ | : Reset |
| RxD0, RxD6 | : Receive Data |
| $\overline{\text{SCK10}}$, SCL0 | : Serial Clock Input/Output |
| SDA0 | : Serial Data Input/Output |
| SI10 | : Serial Data Input |
| SO10 | : Serial Data Output |
| SRC | : Slew Rate Control Input |
| SUP | |
| SUP1 to SUP6 | : Battery Power Supply |
| SCKA | : Serial Clock Input |
| SIA | : Serial Data Input |
| SOA | : Serial Data Output |
| SSA | : Slave Select Input |
| PWMI | : PWM Input |
| TI000 TI010, TI50, TI51 | : Timer Input |
| TO00, TO01, TO50, TO51, TOH0, TOH1 | : Timer Output |
| TxD0, TxD6 | : Transmit Data |
| INH | : Inhibit Input for Half-bridge Driver Enable |
| $V_{DD}$ | : Power Supply |
| VRO | : Voltage Regulator Output |
| VRS | : Voltage Regulator Input |
| SVDD | : Voltage Regulator Output for External Sensor device |
| RESET_A | : Analog chip Reset |
| $V_{SS}$ | : Ground |
| X1, X2 | : Crystal Oscillator (Main System Clock) |

## <R> 1.5 Block Diagram

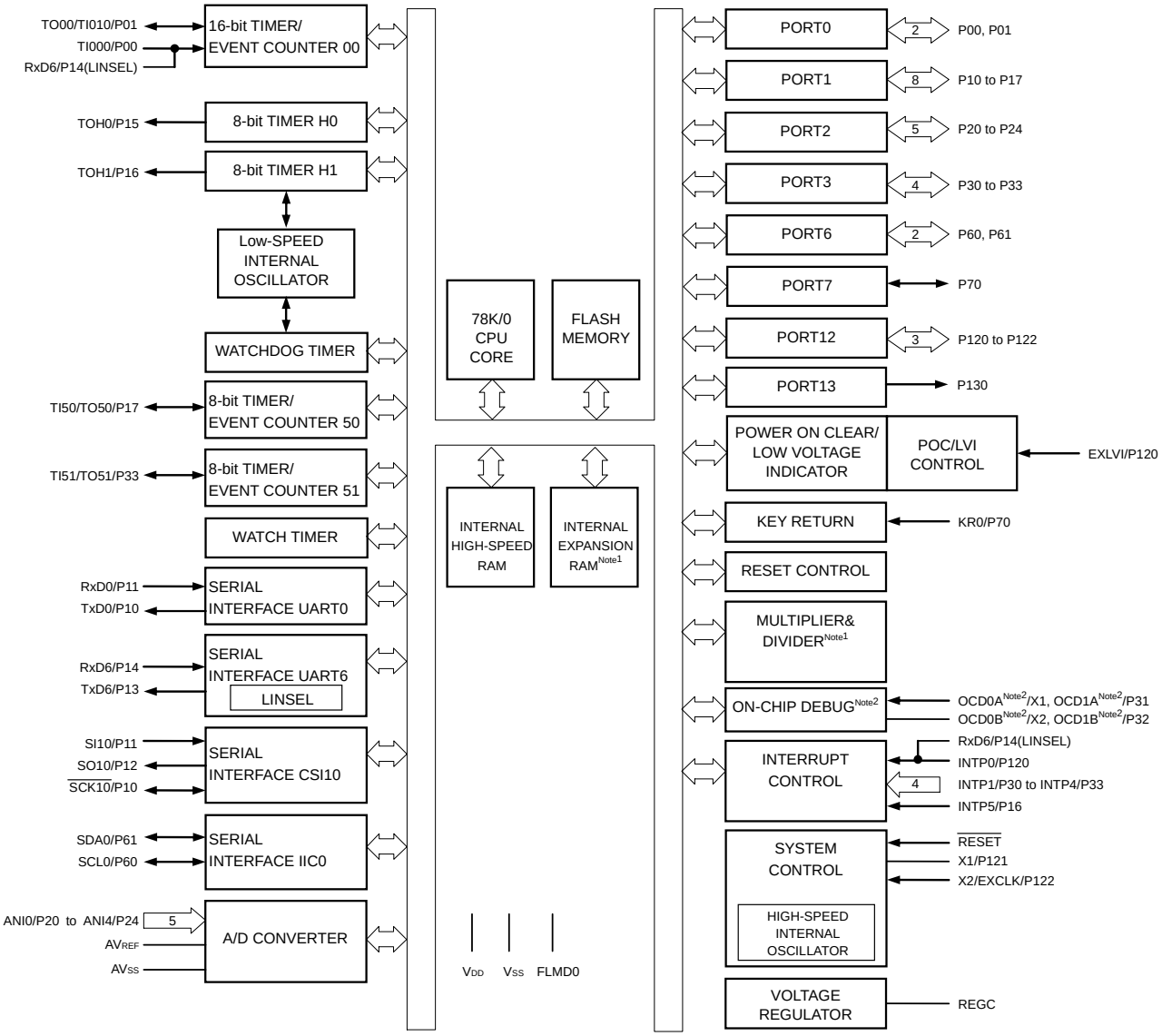



Note µPD78F8077D (with on-chip debug function) only

Cautions 1. µPD78F807x is developed as an MCP (Multi-Chip Package) which includes two chips in the package, a microcontroller chip and an analog chip (power supply circuit, LIN transceiver, and half-bridge circuit).

2. The P10/SCK10/SCKA, P11/SI10/SOA, P12/SO10/SIA, P13/TxD6/TxL, P14/RxD6/RxL, P15/TOH0/PWMI, P16/TOH1/INTP5/SSA, and P17/TI50/TO50/INH pins are connected inside the package.

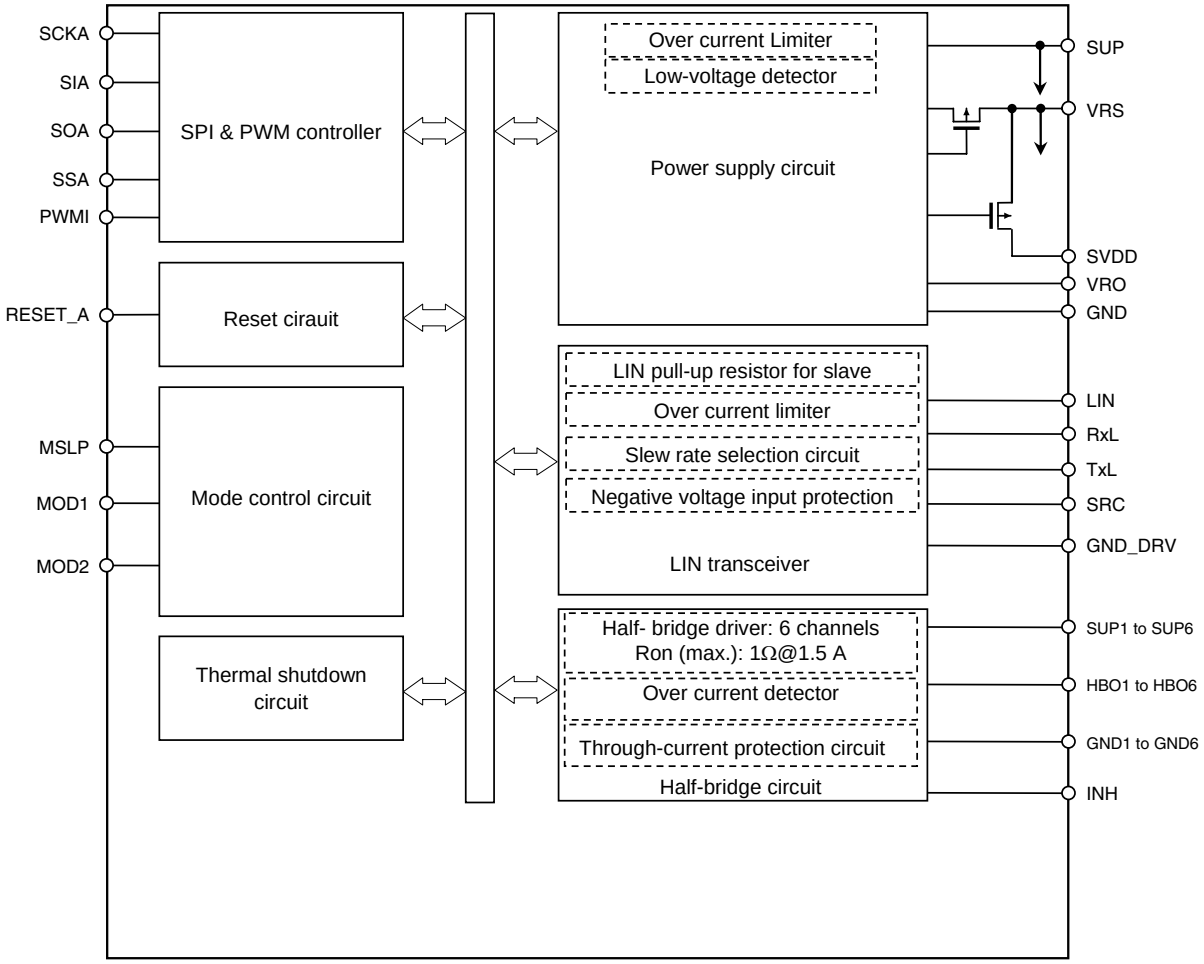
### <R> 1.5.1 Microcontroller Block Diagram




Notes 1. Only supported by the products with 48-Kbyte or more flash memory.

2. µPD78F8077D (with on-chip debug function) only.

### <R> 1.5.2 Analog Block Diagram



## 1.6 Outline of Functions

(1/2)

| Item | | | µPD78F8071 | µPD78F8072 | µPD78F8073 | µPD78F8074 | µPD78F8075 | µPD78F8077D |
|---|---|---|---|---|---|---|---|---|
| Flash memory (KB) | | | 16 | 24 | 32 | 48 | 60 | 128 |
| High-Speed RAM | | | 768 bytes | 1 Kbyte | | | | |
| Expansion RAM (KB) | | | - | | | 1 | 2 | 6 |
| Bank (flash memory) | | | - | | | | | 6 |
| Power supply voltage | | | $V_{DD}$ = 1.8 to 5.5 V | | | | | |
| Regulator | | | Included | | | | | |
| Minimum instruction execution time | | | 0.1 µs (20 MHz: $V_{DD}$ = 2.7 to 5.5 V/0.4 µs (5 MHz: $V_{DD}$ = 1.8 to 5.5 V) | | | | | |
| Clock | Main | High-speed system | 20 MHz: $V_{DD}$ = 2.7 to 5.5 V/5 MHz: $V_{DD}$ = 1.8 to 5.5 V | | | | | |
| | | Internal high-speed oscillation | 8 MHz (TYP.): $V_{DD}$ = 1.8 to 5.5 V | | | | | |
| | Internal low-speed oscillation | | 240 kHz (TYP.): $V_{DD}$ = 1.8 to 5.5 V | | | | | |
| Port | Total | | 26 ch | | | | | |
| | N-ch O.D. (6 V tolerance) | | 2 ch | | | | | |
| Timer | 16 bits (TM0) | | 1 ch | | | | | |
| | 8 bits (TM5) | | 2 ch | | | | | |
| | 8 bits (TMH) | | 2 ch | | | | | |
| | Watch | | 1 ch | | | | | |
| | WDT | | 1 ch | | | | | |
| Serial interface | UART/3-wire CSI Note | | 1 ch | | | | | |
| | UART supporting LIN-bus | | 1 ch | | | | | |
| | $I^2C$ bus | | 1 ch | | | | | |
| <R> 10-bit A/D | | | 5 ch | | | | | |
| Interrupt | External | | 7 | | | | | |
| | Internal | | 16 | | | | | |
| Key interrupt | | | - | | | | | |
| Reset | $\overline{\text{RESET}}$ pin | | Provided | | | | | |
| | POC | | 1.59 V±0.15 V | | | | | |
| | LVI | | The detection level of the supply voltage is selectable. | | | | | |
| | WDT | | Provided | | | | | |
| Multiplier/divider | | | Not provided | | | Provided | | |
| On-chip debug function | | | Not provided | | | | | Provided |
| Operation ambient temperature | | | $T_A$ = -40 to +85 °C | | | | | |

Note Select either of these functions since they share the same pins.

(2/2)

<R>

| Item | μPD78F8071 | μPD78F8072 | μPD78F8073 | μPD78F8074 | μPD78F8075 | μPD78F8077D |
|---|---|---|---|---|---|---|
| Power Supply | • Includes P-ch MOS for dropper<br>- Output voltage: 5 V ± 3% (operating voltage range: 6 to 19 V, output current: 50 mA or less)<br>• On-chip external-dropper (NPN transistor) auxiliary function<br>- Output voltage: 5 V ± 3% (operating voltage range: 7 to 19 V, output current: 150 mA or less)<br>• On-chip power supply output function for external sensors<br>• On-chip over current protection circuit<br>• Low-voltage detector | | | | | |
| LIN transceiver | • Complies with LIN Specifications Rev.2.0, 2.1<br>• Sleep function supported<br>• On-chip slew rate select function<br>• On-chip pull-up resistors for slave applications<br>• On-chip LIN driver current protection circuit | | | | | |
| Driver | • Half-bridge driver: 6 channels<br>• On-chip over current limiter<br>• On-chip through-current protection circuit | | | | | |
| SPI & PWM controller | 1 ch | | | | | |
| Overheat protection circuit | 1 ch | | | | | |

An outline of the timer is shown below.

| | | 16-Bit Timer/ Event Counter 00 | 8-Bit Timer/ Event Counters 50 and 51 | | 8-Bit Timers H0 and H1 | | Watch Timer | Watchdog Timer |
|---|---|---|---|---|---|---|---|---|
| | | TM00 | TM50 | TM51 | TMH0 | TMH1 | | |
| Function | Interval timer | 1 channel | 1 channel | 1 channel | 1 channel | 1 channel | - | - |
| | External event counter | 1 channel | 1 channel | 1 channel | - | - | - | - |
| | PPG output | 1 output | - | - | - | - | - | - |
| | PWM output | - | 1 output | 1 output | 1 output | 1 output | - | - |
| | Pulse width measurement | 2 input | - | - | - | - | - | - |
| | Square-wave output | 1 output | 1 output | 1 output | 1 output | 1 output | - | - |
| | Carrier generator | - | - | - | - | 1 output[Note] | - | - |
| | Watch Timer | - | - | - | - | - | - | - |
| | Watchdog timer | - | - | - | - | - | - | 1 channel |
| Interrupt source | | 2 | 1 | 1 | 1 | 1 | - | - |

Note TM51 and TMH1 can be used in combination as a carrier generator mode.

# 2. Pin Functions

The differences in microcontroller pin functions between the µPD78F807x and 78K0/KC2 are as follows.

<R> **(1) Port and alternate function pins**

| µPD78F807x | | 78K0/KC2 µPD78F0511A, 78F0512A, 78F0513A, 78F0514A, 78F0515A, 78F0517DA | |
|---|---|---|---|
| **Pin name** | **Alternate function** | **Pin name** | **Alternate function** |
| P10 | $\overline{\text{SCK10}}$/TxD0/SCKA | P10 | $\overline{\text{SCK10}}$/TxD0 |
| P11 | SI10/RxD0/SOA | P11 | SI10/RxD0 |
| P12 | SO10/SIA | P12 | SO10 |
| P13 | TxD6/TxL | P13 | TxD6 |
| P14 | RxD6/RxL | P14 | RxD6 |
| P15 | TOH0/PWMI | P15 | TOH0 |
| P16 | TOH1/INTP5/SSA | P16 | TOH1/INTP5 |
| P17 | TI50/TO50/INH | P17 | TI50/TO50 |
| P20 to P24 | ANI0 to ANI4 | P20 to P27 | ANI0 to ANI7 |
| - | - | P40 to P41 | - |
| - | - | P62 | EXSCL0 |
| - | - | P63 | - |
| P70 | KR0 | P70 to P73 | KR0 to KR3 |
| - | - | P74, P75 | - |
| - | - | P123 | XT1 |
| - | - | P124 | XT2/EXCLKS |
| - | - | P140 | PCL/INTP6 |

## 2.1 Microcontroller Block Pin Functions

There are two types of pin I/O buffer power supplies: $AV_{REF}$, and $V_{DD}$. The relationship between these power supplies and the pins are shown below.

<R> **Table 2-1. Pin I/O Buffer Power Supplies**

| Power Supply | Corresponding Pins |
|---|---|
| $AV_{REF}$ | P20 to P24 |
| $V_{DD}$ | Pins other than P20 to P24 |

**(1) Port pins (1/2)**

| Function Name | I/O | Function | After Reset | Alternate Function |
|---|---|---|---|---|
| P00 | I/O | Port 0.<br>2-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by software setting. | Input port | TI000 |
| P01 | | | | TI010/TO00 |
| P10 | I/O | Port 1.<br>8-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by software setting. | Input port | $\overline{SCK10}$/TxD0/SCKA Note1 |
| P11 | | | | SI10/RxD0/SOA Note1 |
| P12 | | | | SO10/SIA Note1 |
| P13 | | | | TxD6/TxL Note1 |
| P14 | | | | RxD6/RxL Note1 |
| P15 | | | | TOH0/PWMI Note1 |
| P16 | | | | TOH1/INTP5/SSA Note1 |
| P17 | | | | TI50/TO50/INH Note1 |
| <R> P20 to P24 | I/O | Port 2.<br>5-bit I/O port.<br>Input/output can be specified in 1-bit units. | Analog input | ANI0 to ANI4 |
| <R> P30 | I/O | Port 3.<br>4-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by software setting. | Input port | INTP1 |
| P31 | | | | INTP2/OCD1A Note2 |
| P32 | | | | INTP3/OCD1B Note2 |
| P33 | | | | INTP4/TI51/TO51 |

Notes 1. Analog pin functions. This pin is connected to a function pin of the analog part inside the package.
2. μPD78F8077D only.

**(1) Port pins (2/2)**

| Function Name | I/O | Function | After Reset | Alternate Function |
|---|---|---|---|---|
| P60 | I/O | Port 6.<br>2-bit I/O port (N-ch open-drain).<br>Input/output can be specified in 1-bit units. | Input port | SCL0 |
| P61 | | | | SDA0 |
| P70 | I/O | Port 7.<br>1-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by software setting. | Input port | KR0 |
| P120 | I/O | Port 12.<br>3-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Only for P120, use of an on-chip pull-up resistor can be specified by software setting. | Input port | INTP0/EXLVI |
| P121 | | | | X1/OCD0A Note |
| P122 | | | | X2/EXCLK/OCD0B Note |
| <R> P130 | Output | Port 13.<br>1-bit output only port. | Output port | - |

Note μPD78F8077D only.

### (2) Non-port functions (1/2)

| Function Name | I/O | Function | After Reset | Alternate Function |
|---|---|---|---|---|
| <R> ANI0 to ANI4 | Input | A/D converter analog input | Analog input | P20 to P24 |
| EXLVI | Input | Potential input for external low-voltage detection | Input port | P120/INTP0 |
| FLMD0 | - | Flash memory programming mode setting | - | - |
| INTP0 | Input | External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified | Input port | P120/EXLVI |
| <R> INTP1 | | | | P30 |
| INTP2 | | | | P31/OCD1A Note2 |
| INTP3 | | | | P32/OCD1B Note2 |
| INTP4 | | | | P33/TI51/TO51 |
| INTP5 | | | | P16/TOH1/SSA Note1 |
| KR0 | Input | Key interrupt input | Input port | P70 |
| REGC | - | Connecting regulator output (2.5 V) stabilization capacitance for internal operation.<br>Connect to $V_{SS}$ via a capacitor (0.47 to 1 μF). | - | - |
| $\overline{\text{RESET}}$ | Input | System reset input | - | - |
| RxD0 | Input | Serial data input to UART0 | Input port | P11/SI10/SOA Note1 |
| RxD6 | Input | Serial data input to UART6 | Input port | P14/RxL Note1 |
| $\overline{\text{SCK10}}$ | I/O | Clock input/output for CSI10 | Input port | P10/TxD0/SCKA Note1 |
| <R> SI10 | Input | Serial data input from CSI10 | Input port | P11/RxD0/SOA Note1 |
| SO10 | Output | Serial data output from CSI10 | Input port | P12 |
| SCL0 | I/O | Clock input/output for IIC | Input port | P60 |
| SDA0 | I/O | Serial data I/O for IIC | Input port | P61 |
| TI000 | Input | External count clock input to 16-bit timer/event counter 00<br>Capture trigger input to capture registers (CR000, CR010) of 16-bit timer/event counter 00 | Input port | P00 |
| TI010 | | Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00 | | P01/TO00 |
| TI50 | Input | External count clock input to 8-bit timer/event counter 50 | Input port | P17/TO50/INH Note1 |
| TI51 | | External count clock input to 8-bit timer/event counter 51 | | P33/TO51/INTP4 |
| TO00 | Output | 16-bit timer/event counter 00 output | Input port | P01/TI010 |
| TO50 | Output | 8-bit timer/event counter 50 output | Input port | P17/TI50/INH Note1 |
| TO51 | | 8-bit timer/event counter 51 output | | P33/TI51/INTP4 |
| TOH0 | | 8-bit timer H0 output | | P15/PWMI Note1 |
| TOH1 | | 8-bit timer H1 output | | P16/INTP5/SSA Note1 |
| TxD0 | Output | Serial data output from UART0 | Input port | P10/$\overline{\text{SCK10}}$/SCKA Note1 |
| TxD6 | Output | Serial data output from UART6 | Input port | P13/TxL Note1 |

Notes 1. Analog pin functions. This pin is connected to a function pin of the analog part inside the package.
2. μPD78F8077D only.

**(2) Non-port functions (2/2)**

| Function Name | I/O | Function | After Reset | Alternate Function |
|---|---|---|---|---|
| X1 | - | Main system clock resonator connection | Input port | P121/OCD0A Note |
| X2 | - | | | P122/EXCLK/ OCD0B Note |
| EXCLK | Input | External clock input for main system clock | Input port | P122/X2 |
| $V_{DD}$ | - | Positive power supply for pins other than P20 to P24 | - | - |
| $AV_{REF}$ | - | A/D converter reference voltage input and positive power supply for P20 to P24 and A/D converter | - | - |
| $V_{SS}$ | - | Ground potential for pins other than P20 to P24 | - | - |
| $AV_{SS}$ | - | A/D converter ground potential. Make the same potential as $V_{SS}$. | - | - |

Note: μPD78F8077D only.

## 2.2 Analog Part Pins

(1/2)

| Function Name | I/O | Function |
|---|---|---|
| SSA Note | Input | Slave select input |
| PWMI Note | Input | External PWM input |
| RxL Note | Output | Serial data output |
| TxL Note | Input | Serial data input |
| SIA Note | Input | Serial data input |
| SOA Note | Output | Serial data output |
| SCKA Note | Input | Clock input |
| GND1 | - | Ground potential for half-bridge channel 1 |
| HBO1 | Output | Output for half-bridge channel 1 |
| SUP1 | - | Power supply for half-bridge channel 1 |
| GND2 | - | Ground potential for half-bridge channel 2 |
| HBO2 | Output | Output for half-bridge channel 2 |
| SUP2 | - | Power supply for half-bridge channel 2 |
| GND3 | - | Ground potential for half-bridge channel 3 |
| HBO3 | Output | Output for half-bridge channel 3 |
| SUP3 | - | Power supply for half-bridge channel 3 |
| GND4 | - | Ground potential for half-bridge channel 4 |
| HBO4 | Output | Output for half-bridge channel 4 |
| SUP4 | - | Power supply for half-bridge channel 4 |
| GND5 | - | Ground potential for half-bridge channel 5 |
| HBO5 | Output | Output for half-bridge channel 5 |
| SUP5 | - | Power supply for half-bridge channel 5 |
| GND6 | - | Ground potential for half-bridge channel 6 |
| HBO6 | Output | Output for half-bridge channel 6 |
| SUP6 | - | Power supply for half-bridge channel 6 |

Note This pin is connected to the microcontroller pin functions inside the package.

Cautions 1. Make GND, GND1 to GND6, and GND_DRV the same potential as Vss and AVss.
2. Make SUP1 to SUP6 the same potential as SUP.

(2/2)

| Function Name | I/O | Function |
|---|---|---|
| <R> SUP | - | Power supply connection |
| SVDD | Output | Power supply output for external sensors |
| VRO | Output | Power supply output or base control output for using external NPN transistor |
| VRS | Input | Power supply and power-supply voltage monitor |
| GND | - | Power supply circuit GND potential |
| LIN | I/O | LIN Bus connection pin |
| GND_DRV | - | LIN transceiver circuit GND |
| MOD1, MOD2 | Input | Pin mode control input |
| MSLP | Input | Sleep mode selection |
| SRC | Input | Slew rate control input |
| RESET_A | Input | Reset input to the analog chip side |
| INH[Note] | Input | Half-bridge output-disable input |

Note This pin is connected to the microcontroller pin functions inside the package

Cautions 1. Make GND, GND1 to GND6, and GND_DRV the same potential as VSS and AVSS.

2. Make SUP1 to SUP6 the same potential as SUP.

<R> 3. Make VDD the same potential as VRS or VRO when the on-chip P-ch MOS is used for the 5-V output dropper.

<R> 4. Make VDD the same potential as VRS when the external dropper is used for the 5-V output dropper.

## 2.3 Description of Pin Functions

### 2.3.1 P00, P01 (Port 0)

P00 and P01 are a 2-bit I/O port. These pins also function as timer I/O.

The following operation modes can be specified in 1-bit units.

**(1) Port mode**

P00 and P01 function as a 2-bit I/O port. These pins can be set to input or output port in 1-bit units using port mode register 0 (PM0). An on-chip pull-up resistor can be used by setting the pull-up resistor option register 0 (PU0).

**(2) Control mode**

P00 and P01 function as timer I/O pins.

**(a) TI000**

Functions as the external count clock input pin to 16-bit timer/event counter 00 and capture trigger signal input pin to the capture registers (CR000, CR010) of 16-bit timer/event counter 00.

**(b) TI010**

Functions as the capture trigger signal input pin to the capture register (CR000) of 16-bit timer/event counters 00 and 01.

**(c) TO00**

Functions as the timer output pin for 16-bit timer/event counter 00.

### 2.3.2 P10 to P17 (Port 1)

P10 to P17 are an 8-bit I/O port. These pins also function as external interrupt request input, serial interface data I/O, clock I/O, and timer I/O pins.

The following operation modes can be specified in 1-bit units.

**(1) Port mode**

P10 to P17 function as an 8-bit I/O port. These pins can be set to input or output port in 1-bit units using port mode register 1 (PM1). An on-chip pull-up resistor can be used by setting the pull-up resistor option register 1 (PU1).

**(2) Control mode**

P10 to P17 function as the external interrupt request input, serial interface data I/O, clock I/O, and timer I/O pins.

**(a) SI10**

Functions as the serial data input pin for the serial interface CSI10.

**(b) SO10**

Functions as the serial data output pin for the serial interface CSI10.

**(c) $\overline{\text{SCK10}}$**

Functions as the serial clock I/O pin for the serial interface CSI10.

**(d) RxD0**

Functions as the serial data input pin for the serial interface UART0.

**(e) RxD6**

Functions as the serial data input pin for the serial interface UART6.

**(f) TxD0**

Functions as the serial data output pin for the serial interface UART0.

**(g) TxD6**

Functions as the serial data output pin for the serial interface UART6.

**(h) TI50**

Functions as the external count clock input pin for the 8-bit timer/event counter 50.

**(i) TO50**

Functions as the timer output pin for the 8-bit timer/event counter 50.

**(j) TOH0, TOH1**

Function as the timer output pins for the 8-bit timers H0 and H1.

**(k) INTP5**

Functions as the external interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

### <R> 2.3.3 P20 to P24 (Port 2)

P20 to P24 are an 5-bit I/O port. These pins also function as A/D converter analog input pins.

The following operation modes can be specified in 1-bit units.

**(1) Port mode**

P20 to P24 function as an 5-bit I/O port. These pins can be set to input or output port in 1-bit units using port mode register 2 (PM2).

**(2) Control mode**

P20 to P24 function as the A/D converter analog input pins (ANI0 to ANI4). When using these pins as analog input pins, see 13.6 Cautions for A/D Converter in 78K0/Kx2 User's Manual (R01UH0008E).

**(a) ANI0 to ANI4**

Functions as the A/D converter analog input pins.

Caution ANI0/P20 to ANI4/P24 are set to analog input mode after a reset is released.

### 2.3.4 P30 to P33 (port 3)

P30 to P33 are a 4-bit I/O port. These pins also function as external interrupt request input and timer I/O pins.

The following operation modes can be specified in 1-bit units.

**(1) Port mode**

P30 to P33 function as a 4-bit I/O port. These pins can be set to input or output port in 1-bit units using port mode register 3 (PM3). An on-chip pull-up resistor can be used by setting the pull-up resistor option register 3 (PU3).

**(2) Control mode**

P30 to P33 function as the external interrupt request input and timer I/O pins.

**(a) INTP1 to INTP4**

Function as the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

**(b) TI51**

Functions as the external count clock input pin to 8-bit timer/event counter 51.

**(c) TO51**

Functions as the timer output pin from 8-bit timer/event counter 51.

Cautions 1. In μPD78F8077D (a product with the on-chip debug function), be sure to pull down the P31/INTP2/OCD1A pin before reset release to prevent malfunction.

2. When the flash memory programmer or on-chip debug emulator is connected but the P31/INTP2/OCD1 pin in a product with the on-chip debug function (μPD78F8077D) is not used, this pin should be handled as follows:

| | | P31/INTP2/OCD1A |
|---|---|---|
| Flash memory programmer connected | | Connect to $V_{SS}$ via a resistor. |
| On-chip debug emulator connected (when P31/INTP2/OCD1A is not used as on-chip debug mode setting pin) | During reset | |
| | When a reset is released | Input: Connect to $V_{DD}$ or $V_{SS}$ via a resistor.<br>Output: Leave open. |

Remarks In μPD78F8077D (a product with the on-chip debug function), P31 and P32 can be used as on-chip debug mode setting pins (OCD1A, OCD1B) when the on-chip debug function is used. For the connection to the in-circuit emulator supporting on-chip debugging (QB-78K0MINI), see CHAPTER 28 ON-CHIP DEBUG FUNCTION in 78K0/Kx2 User's Manual (R01UH0008E).

### 2.3.5 P60 to P61 (port 6)

P60 and P61 are a 2-bit I/O port. These pins also function as serial interface data I/O and clock I/O pins.

The following operation modes can be specified in 1-bit units.

**(1) Port mode**

P60 and P61 function as a 2-bit I/O port. These pins can be set to input or output port in 1-bit units using port mode register 6 (PM6).

Output of P60 and P61 is N-ch open-drain output (6 V tolerance).

**(2) Control mode**

P60 and P61 function as serial interface data I/O and clock I/O pins.

**(a) SDA0**

Functions as the serial data I/O pin for the serial interface IIC0.

**(b) SCL0**

Functions as the serial clock I/O pin for the serial interface IIC0.

### 2.3.6 P70 (port 7)

P70 is a 1-bit I/O port. This pin also functions as a key interrupt input pin.

The following operation modes can be specified.

**(1) Port mode**

P70 functions as a 1-bit I/O port. This pin can be set to input or output port using port mode register 7 (PM7). An on-chip pull-up resistor can be used by setting the pull-up resistor option register 7 (PU7).

**(2) Control mode**

P70 functions as the key interrupt input pin.

**(a) KR0**

Functions as the key interrupt input pin.

### 2.3.7 P120 to P122 (port 12)

P120 to P122 are a 3-bit I/O port. These pins also function as external interrupt request input, external low-voltage detection potential input, main system clock resonator connection, and main system clock external clock input pins. The following operation modes can be specified in 1-bit units.

**(1) Port mode**

P120 to P122 function as a 3-bit I/O port. These pins can be set to input or output port using port mode register 12 (PM12). Only for P120, an on-chip pull-up resistor can be used by setting the pull-up resistor option register 12 (PU12).

**(2) Control mode**

P120 to P122 function as pins for the external interrupt request input, potential input for external low-voltage detection, connecting resonator for main system clock, and external clock input for main system clock.

**(a) INTP0**

Functions as the external interrupt request input pin (INTP0) for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

**(b) EXLVI**

Functions as the potential input pin for external low-voltage detection.

**(c) X1, X2**

Function as the resonator connection pins for the main system clock.

**(d) EXCLK**

Functions as the external clock input pin for the main system clock.

Caution When the flash memory programmer or on-chip debug emulator is connected but the P121/X1/OCD0A pin in a product with the on-chip debug function (μPD78F8077D) is not used, this pin should be handled as follows:

| | | P121/X1/OCD0A |
|---|---|---|
| Flash memory programmer connected | | Connect to $V_{SS}$ via a resistor. |
| On-chip debug emulator connected (when P121/X1/OCD0A is not used as on-chip debug mode setting pin) | During reset | |
| | When a reset is released | Input: Connect to $V_{DD}$ or $V_{SS}$ via a resistor.<br>Output: Leave open. |

Remarks In μPD78F8077D (a product with the on-chip debug function), P121 and P122 can be used as on-chip debug mode setting pins (OCD0A, OCD0B) when the on-chip debug function is used. For the connection to the in-circuit emulator supporting on-chip debugging (QB-78K0MINI), see CHAPTER 28 ON-CHIP DEBUG FUNCTION in 78K0/Kx2 User's Manual (R01UH0008E).

<R> ### 2.3.8 P130 (port 13)

P130 functions as an output-only port.

Remark When the device is reset, P130 outputs a low level. Therefore, to output a high level from P130 before the device is reset, the output signal of P130 can be used as a pseudo reset signal of the CPU (see the figure for Remark in 5.2.10 Port 13 in 78K0/Kx2 User's Manual (R01UH0008E)).

### 2.3.9 $AV_{REF}$, $AV_{SS}$, $V_{DD}$, $V_{SS}$

#### (a) $AV_{REF}$

<R> $AV_{REF}$ is the A/D converter reference voltage input pin and the positive power supply pin for P20 to P24 and A/D converter.

When the A/D converter is not used, connect this pin directly to $V_{DD}$[Note].

Note Make the $AV_{REF}$ pin the same potential as the $V_{DD}$ pin when port 2 is used as a digital port.

#### (b) $AV_{SS}$

$AV_{SS}$ is the A/D converter ground potential pin. Even when the A/D converter is not used, always use this pin with the same potential as the $V_{SS}$ pin.

#### (c) $V_{DD}$

<R> $V_{DD}$ is the positive power supply pin for the pins other than P20 to P24.

#### (d) $V_{SS}$

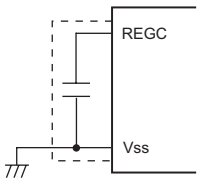
<R> $V_{SS}$ is the ground potential pin for the ports other than P20 to P24.

### 2.3.10 $\overline{\text{RESET}}$

RESET is the active-low system reset input pin.

### 2.3.11 REGC

REGC is the pin for connecting regulator output (2.5 V) stabilization capacitance for internal operation. Connect this pin to Vss via a capacitor (0.47 to 1 μF).




Caution Keep the wiring length as short as possible for the broken-line part in the above figure.

### 2.3.12 FLMD0

FLMD0 is the flash memory programming mode setting pin.
Connect FLMD0 to Vss during the normal operation mode.
In the flash memory programming mode, connect this pin to the flash programmer.

### 2.3.13 HBO1 to HBO 6

HBO1 to HBO6 are the half-bridge driver output pins.
Half-bridge driver output is controlled by the SPI & PWM controller.
For details, see chapter 7 Half-Bridge Circuit.

### 2.3.14 SUP1 to SUP6

SUP1 to SUP6 are the half-bridge driver power supply pins.
Make SUP1 to SUP6 the same potential as the SUP pin potential.

### 2.3.15 GND, GND1 to GND6, GND_DRV

GND is the ground potential pin for the power supply circuit.
GND1 to GND6 are the half-bridge circuit ground potential pins.
GND_DRV is the LIN transceiver ground potential pin.
GND, GND1 to GND6, and GND_DRV potentials should be the same.

### 2.3.16 RESET_A

RESET_A is the active-low reset input pin for the analog chip.

### 2.3.17 LIN

LIN is the LIN Bus connection pin.

### 2.3.18 MSLP

MSLP is the mode transition acceptance pin.

In the normal mode the analog chip function block goes into the sleep mode when MSLP is set to low, and in the sleep mode the analog chip function block goes into the normal mode when MSLP is set to high.

MSLP is internally pulled down.

For detail, see chapter 6.2 Operating Modes.

### 2.3.19 SUP

SUP is the power supply pin.

<R>

### 2.3.20 MOD1, MOD2

MOD1 and MOD2 are the port mode select pins.

For details, see chapter 6.1 LIN Transceiver Function.

### 2.3.21 VRO

VRO functions as the power supply circuit output pin when the internal P-ch MOS is used as the 5-V output dropper, and functions as the base control output pin when the external NPN transistor is used as the 5-V output dropper.

### 2.3.22 VRS

VRS is the power supply circuit input and output voltage monitor pin.

### 2.3.23 SVDD

SVDD is the power supply circuit output pin for external sensors.

For details, see chapter 5 Power Supply Circuit.

### 2.3.24 SRC

SRC is the LIN communication slew rate select pin.

For details, see chapter 6.1 LIN Transceiver Functions.

### 2.3.25 SCKA

SCKA is the SPI & PWM controller clock input pin.

### 2.3.26 SOA

SOA is the SPI & PWM controller serial data output pin.

### 2.3.27 SIA

SIA is the SPI & PWM controller serial data input pin.

### 2.3.28 SSA

SSA is the SPI & PWM controller slave select input pin.

### 2.3.29 PWMI

PWMI is the SPI & PWM controller external PWM input pin.

### 2.3.30 INH

INH is the half-bridge circuit output-disable control input pin.

For details, see chapter 7 Half-Bridge Circuit.

<R> **2.3.31 IC**

IC is the internal connection pin.

## 2.4 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-3 shows the types of pin I/O circuits and the recommended connections of unused pins.

Refer to Figure 2-1 for the I/O circuit configuration of each type.

**Table 2-3. Pin I/O Circuit Types (1/3)**

| Pin Name | I/O Circuit Type | I/O | Recommended Connection of Unused Pin |
|---|---|---|---|
| P00/TI000 | 5-AQ | I/O | Input: Connect independently to $V_{DD}$ or $V_{SS}$ via a resistor.<br>Output: Leave open. |
| P01/TI010/TO00 | | | |
| P10/$\overline{SCK10}$/TxD0/ SCKA Note2 | | | |
| P11/SI10/RxD0/SOA Note2 | | | |
| P12/SO10/SIA Note2 | 5-AG | | |
| P13/TxD6/TxL Note1 | | | |
| P14/RxD6/RxL Note1 | 5-AQ | | |
| P15/TOH0/PWMI Note2 | 5-AG | | |
| P16/TOH1/INTP5/ SSA Note2 | 5-AQ | | |
| P17/TI50/TO50/INH Note2 | 5-AQ | | Input/output: Connect independently to $V_{SS}$ via a resistor. |
| <R> P20/ANI0 to P24/ANI4 Note3 | 11-G | | <Digital input setting or analog input setting><br>Connect independently to $AV_{REF}$ or $AV_{SS}$ via a resistor.<br><Digital output setting><br>Leave open. |
| <R> P30/INTP1 | 5-AQ | | Input: Connect independently to $V_{DD}$ or $V_{SS}$ via a resistor.<br>Output: Leave open. |
| P31/INTP2 | 5-AQ | | |
| P32/INTP3 | | | |
| P33/TI51/TO51/INTP4 | | | |

Notes 1. This pin also has the LIN transceiver function. When this pin is used as the LIN transceiver function pin, leave it open.

2. Analog part pin functions. This pin is connected to an analog part pin function inside the package.

<R> 3. P20/ANI0 to P24/ANI4 enter the analog input mode after a reset is released.

<R> **Table 2-3. Pin I/O Circuit Types (2/3)**

| Pin Name | I/O Circuit Type | I/O | Recommended Connection of Unused Pin |
|---|---|---|---|
| P60/SCL0 | 13-AI | I/O | Input: Connect to $V_{SS}$.<br>Output: Leave this pin open at low-level output after clearing the output latch of the port to 0. |
| P61/SDA0 | | | |
| P70/KR0 | 5-AQ | | Input: Connect independently to $V_{DD}$ or $V_{SS}$ via a resistor.<br>Output: Leave open. |
| P120/INTP0/EXLVI | | | |
| P121/X1 Note1 | 37 | I/O | Input: Connect independently to $V_{DD}$ or $V_{SS}$ via a resistor.<br>Output: Leave open. |
| P122/X2/EXCLK Note1 | | | |
| P130 | 3-C | Output | Leave open. |
| $\overline{\text{RESET}}$ | 2 | Input | Connect to $V_{DD}$ directly or via a resistor. |
| FLMD0 Note4 | 38-A | - | Connect to $V_{SS}$. |
| $AV_{REF}$ | - | - | Connect directly to $V_{DD}$ Note3. |
| $AV_{SS}$ | | | Connect directly to $V_{SS}$. |
| MOD1 | LIN-1 | Input | Connect directly to $V_{SS}$ or VRS. |
| MOD2 | | | |
| SRC | | Input | Connect directly to $V_{SS}$ or VRS. |
| SCKA Note3 | LIN-1-C | Input | Leave open. |
| SOA Note3 | LIN-2 | Output | Leave open. |
| SIA Note3 | LIN-1-C | Input | Leave open. |
| SSA Note3 | LIN-1-D | Input | Leave open. |
| PWMI Note3 | LIN-1-C | Input | Leave open. |
| INH Note3 | LIN-1-D | Input | Leave open. |
| LIN | LIN-3 | I/O | Leave open. |
| MSLP | LIN-1-A | Input | Leave open. |

Notes 1. Set the I/O port mode with the clock operating mode select register (OSCCTL) and use the recommended connection method described above when these pins are not used.

2. Make this pin the same potential as the $V_{DD}$ pin when port 2 is used as a digital port.

3. These pins are connected to the microcontroller pin functions inside the package.

<R> 4. FLMD0 is a pin that is used to write data to the flash memory. To rewrite the data of the flash memory on-board, connect this pin to $V_{SS}$ via a resistor (10 kΩ: recommended). The same applies when executing on-chip debugging with a product with an on-chip debug function (μPD78F8077D).

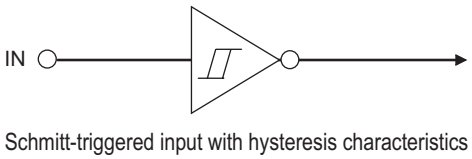
**Table 2-3. Pin I/O Circuit Types (3/3)**

| Pin Name | I/O Circuit Type | I/O | Recommended Connection of Unused Pin |
|---|---|---|---|
| HBO1 | LIN-4 | Output | Leave open. |
| HBO2 | | | |
| HBO3 | | | |
| HBO4 | | | |
| HBO5 | | | |
| HBO6 | | | |
| <R> VRO | LIN-5 | Output | Connect directly to $V_{DD}$. |
| VRS | | Input | Connect directly to VRO. |
| RxL | LIN-2 | Output | -Note |
| TxL | LIN-6 | Input | -Note |
| SVDD | LIN-5 | Output | Leave open. |
| RESET_A | LIN-1-B | Input | Connect directly to VRS. |

Note These pins are connected to the microcontroller pin functions inside the package.

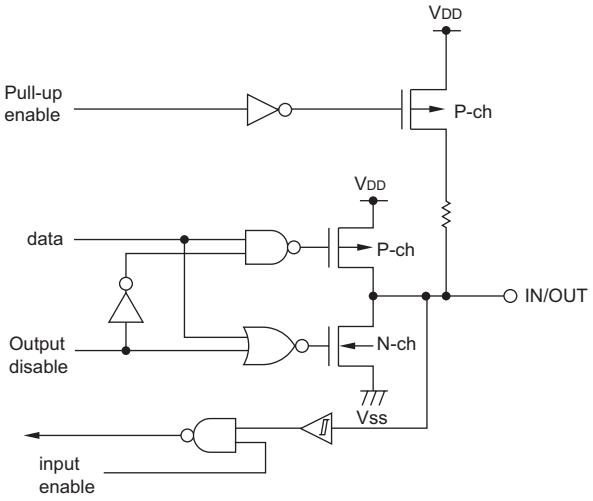
**Figure 2-1. Pin I/O Circuit List (1/4)**

**Type 2**



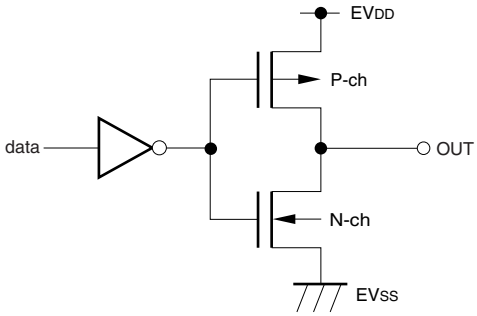

Schmitt-triggered input with hysteresis characteristics

**Type 5-AQ**

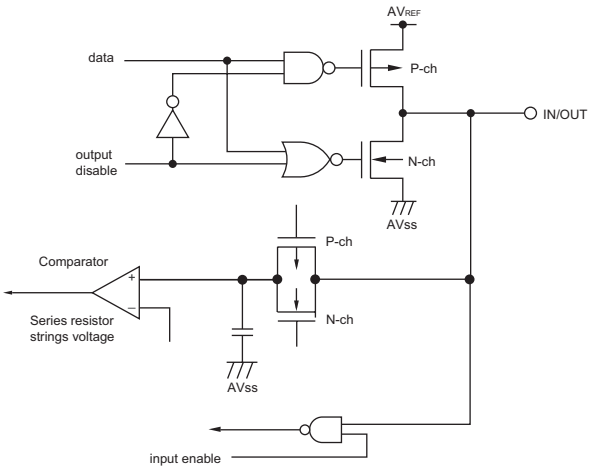



<R>

**Type 3-C**




**Type 11-G**




**Type 5-AG**

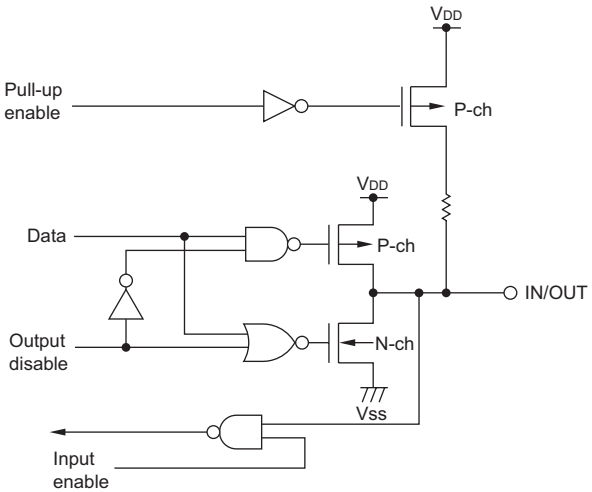
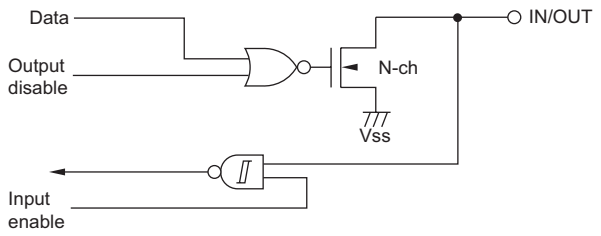
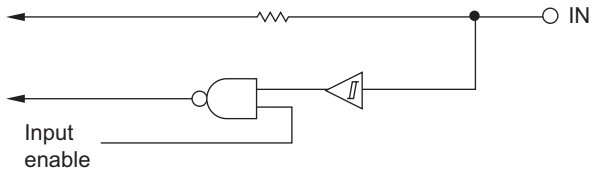


**Figure 2-1. Pin I/O Circuit List (2/4)**

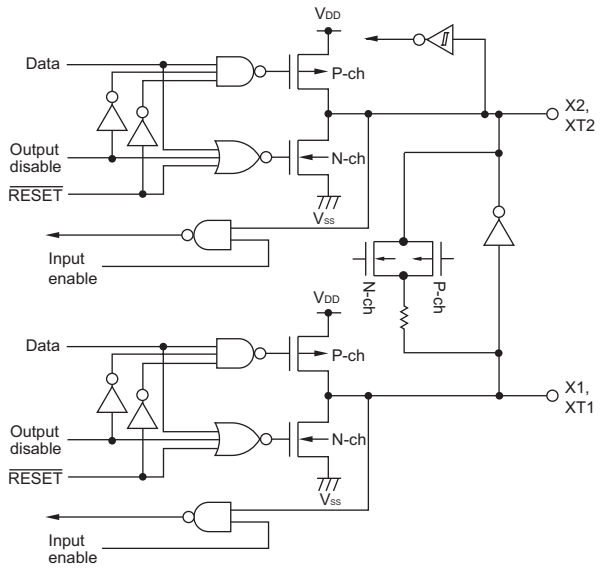
**Type 13-AI**




**Type 38-A**



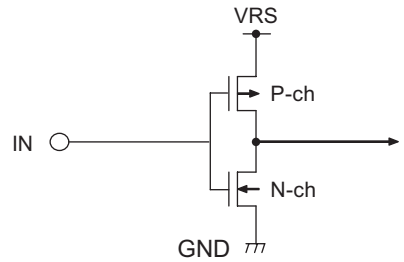

**Type 37**



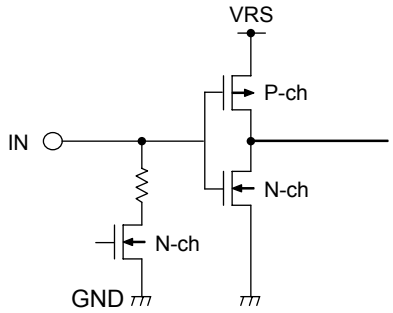
<R>

**Figure 2-1. Pin I/O Circuit List (3/4)**

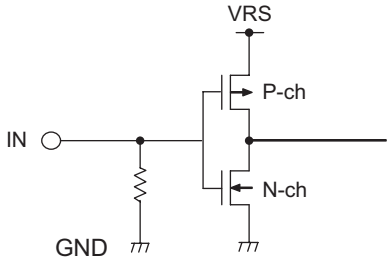
**LIN-1**



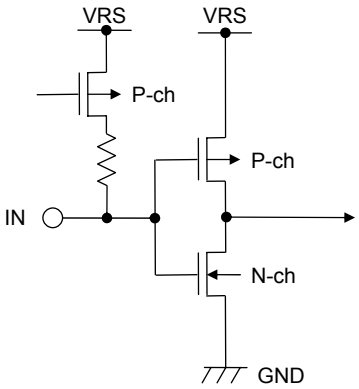

**LIN-1-C**



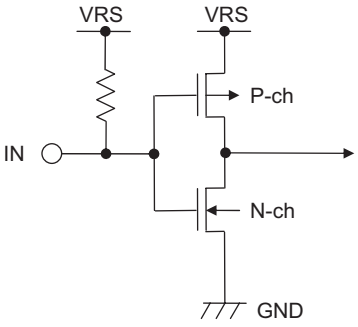

**LIN-1-A**



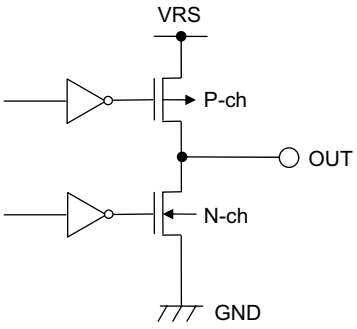

**LIN-1-D**




**LIN-1-B**

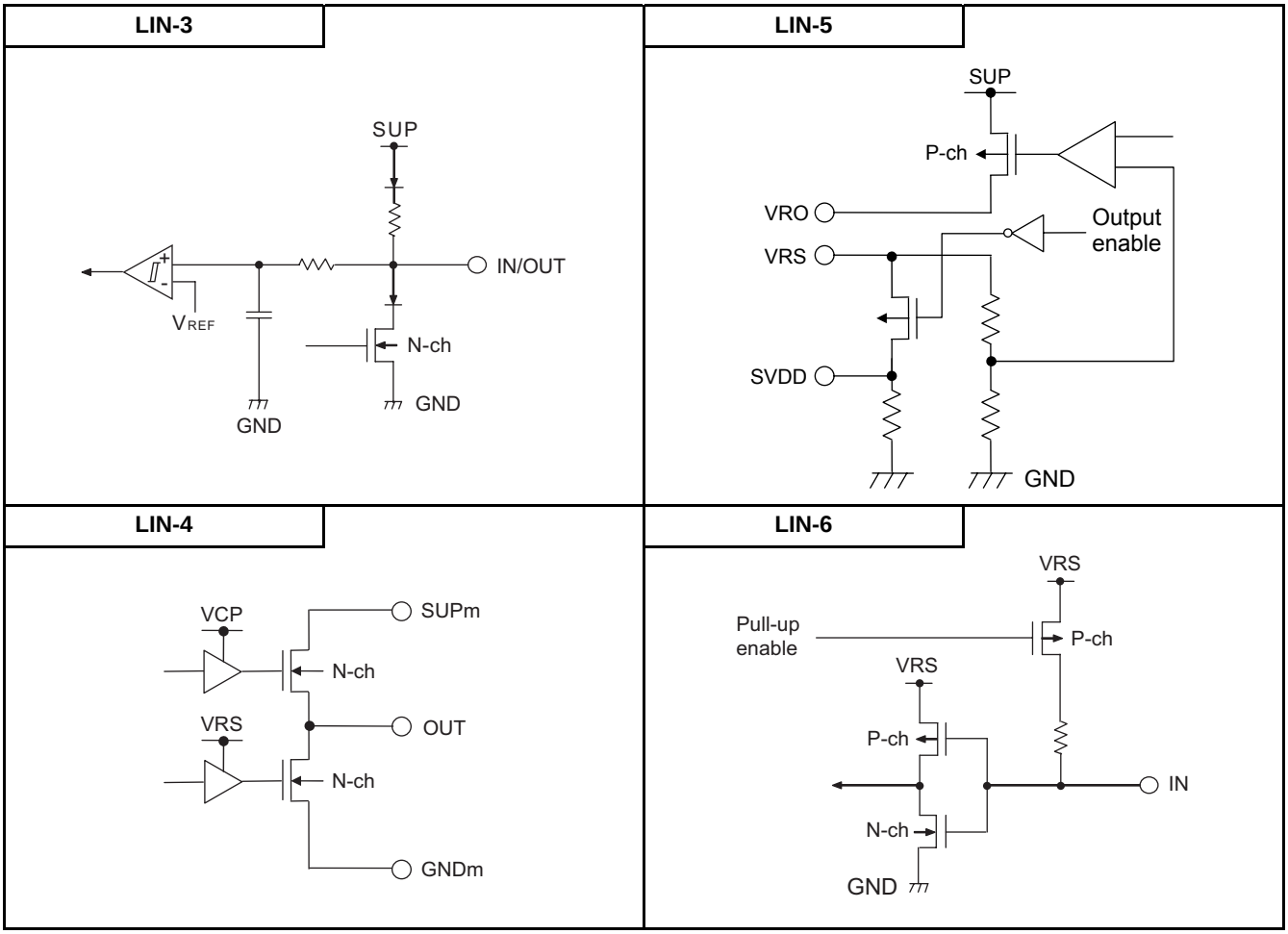



**LIN-2**



<R>

**Figure 2-1. Pin I/O Circuit List (4/4)**




Remark m = 1 to 6

# 3. Microcontroller Functions

The 78K0/KC2 is used for the 8-bit microcontroller block. The supported functions of the μPD78F807x are different from those of the 78K0/KC2 because some of the 78K0/KC2 function pins are not available externally.

This manual describes the differences in functions and registers between the μPD78F807x and 78K0/KC2.

For a description of each function of the microcontroller block, see the 78K0/Kx2 User's Manual (R01UH0008E).

## 3.1 Differences in Functions between μPD78F807x and 78K0/KC2

The functional differences between the μPD78F807x and 78K0/KC2 (48 pins) are as follows.

| | Item | | μPD78F807x | 78K0/KC2 (48 pins)<br>μPD78F0511A, 78F0512A, 78F0513A<br>78F0514A, 78F0515A, 78F0517DA |
|---|---|---|---|---|
| | Subsystem clock (oscillation frequency) | | - | XT1 (crystal) oscillation<br>External subsystem clock input (EXCLKS)<br>32.768 kHz (TYP.) : $V_{DD}$ = 1.8 to 5.5 V |
| | I/O ports | | Total: 26<br>CMOS I/O: 24<br>N-ch open-drain I/O (6-V tolerance): 2 | Total: 41<br>CMOS I/O: 37<br>N-ch open-drain I/O (6-V tolerance): 4 |
| | Clock output | | - | • 156.25 kHz, 312.5 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (peripheral hardware clock: $f_{PRS}$ = 20 MHz operation)<br>• 32.768 kHz (subsystem clock: $f_{SUB}$ = 32.768 kHz operation) |
| <R> | A/D converter | | 10-bit resolution x 5 channels ($AV_{REF}$ = 2.3 to 5.5 V) | 10-bit resolution x 8 channels ($AV_{REF}$ = 2.3 to 5.5 V) |
| | Vectored interrupt sources | Internal | 16 | 16 |
| | | External | 7 | 8 |
| | Key interrupt | | Key interrupt (INTKR) occurs when the falling edge of the key input pin (KR0) is detected. | Key interrupt (INTKR) occurs when the falling edge of the key input pin (KR0 to KR3) is detected. |

## 3.2 Differences in Special Function Registers between μPD78F807x and 78K0/KC2

The differences in special function registers between the μPD78F807x and 78K0/KC2 (48 pins) are as follows.

(1/2)

| | Address | μPD78F807x | | 78K0/KC2 μPD78F0511A, 78F0512A, 78F0513A 78F0514A, 78F0515A, 78F0517DA | |
|---|---|---|---|---|---|
| | | Special Function Register (SFR) Name | Symbol | Special Function Register (SFR) Name | Symbol |
| | FF02H | Port register 2 Note 1 | P2 | Port register 2 | P2 |
| | FF04H | - Note 2 | - | Port register 4 | P4 |
| | FF06H | Port register 6 Note 1 | P6 | Port register 6 | P6 |
| | FF07H | Port register 7 Note 1 | P7 | Port register 7 | P7 |
| <R> | FF0CH | Port register 12 Note 1 | P12 | Port register 12 | P12 |
| | FF0EH | - Note 2 | - | Port register 14 | P14 |
| | FF22H | Port mode register 2 Note 1 | PM2 | Port mode register 2 | PM2 |
| | FF24H | Port mode register 4 Note 1 | PM4 | Port mode register 4 | PM4 |
| | FF26H | Port mode register 6 Note 1 | PM6 | Port mode register 6 | PM6 |
| | FF27H | Port mode register 7 Note 1 | PM7 | Port mode register 7 | PM7 |
| | FF29H | Analog input channel specification register Note 1 | ADS | Analog input channel specification register | ADS |
| | FF2CH | Port mode register 12 Note 1 | PM12 | Port mode register 12 | PM12 |
| | FF2EH | Port mode register 14 Note 1 | PM14 | Port mode register 14 | PM14 |
| | FF2FH | A/D port configuration register Note 1 | ADPC | A/D port configuration register | ADPC |
| <R> | FF34H | Pull up resistor option register 4 Note 1 | PU4 | Pull up resistor option register 4 | PU4 |
| | FF37H | Pull-up resistor option register 7 Note 1 | PU7 | Pull up resistor option register 7 | PU7 |
| <R> | FF3EH | Pull up resistor option register 14 Note 1 | PU14 | Pull up resistor option register 14 | PU14 |
| | FF40H | - Note 2 | - | Clock output selection register | CKS |
| | FF48H | External interrupt rising edge enable register Note 1 | EGP | External interrupt rising edge enable register | EGP |
| | FF49H | External interrupt falling edge enable register Note 1 | EGN | External interrupt falling edge enable register | EGN |
| | FF6EH | Key return mode register Note 1 | KRM | Key return mode register | KRM |
| | FF6FH | Watch timer operation mode register Note 1 | WTM | Watch timer operation mode register | WTM |
| | FF9FH | Clock operation mode selection register Note 1 | OSCCTL | Clock operation mode selection register | OSCCTL |
| | FFA8H | IIC clock selection register 0 Note 1 | IICCL0 | IIC clock selection register 0 | IICCL0 |

Notes 1. There are differences in bit setting.
2. Be sure not to write to this register.

(2/2)

| Address | μPD78F807x | | | 78K0/KC2 μPD78F0511A, 78F0512A, 78F0513A 78F0514A, 78F0515A, 78F0517DA | | |
|---|---|---|---|---|---|---|
| | Special Function Register (SFR) Name | Symbol | | Special Function Register (SFR) Name | Symbol | |
| FFE2H | Interrupt request flag register 1L Note | IF1 | IF1L | Interrupt request flag register 1L | IF1 | IF1L |
| FFE6H | Interrupt mask register 1L Note | MK1 | MK1L | Interrupt mask register 1L | MK1 | MK1L |
| FFEAH | Priority specification flag register 1L Note | PR1 | PR1L | Priority specification flag register 1L | PR1 | PR1L |
| FFFBH | Processor clock control register Note | PCC | | Processor clock control register | PCC | |

Note There are differences in bit setting.

## 3.3 Differences in Register Bit Settings between μPD78F807x and 78K0/KC2

### 3.3.1 Port mode register

**μPD78F807x**

| | Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| <R> | PM2 | 1 | 1 | 1 | PM24 | PM23 | PM22 | PM21 | PM20 | FF22H | FFH | R/W |
| | PM4 | 1 | 1 | 1 | 1 | 1 | 1 | PM41 | PM40 | FF24H | FFH | R/W |
| | PM6 | 1 | 1 | 1 | 1 | PM63 | PM62 | PM61 | PM60 | FF26H | FFH | R/W |
| | PM7 | 1 | 1 | PM75 | PM74 | PM73 | PM72 | PM71 | PM70 | FF27H | FFH | R/W |
| | PM12 | 1 | 1 | 1 | PM124 | PM123 | PM122 | PM121 | PM120 | FF2CH | FFH | R/W |
| | PM14 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | PM140 | FF2EH | FFH | R/W |

<R> Cautions
1. Bits 5 to 7 in PM2 should always be 1.
2. Bits 2 to 7 in PM4 should always be 1. Bits 0 and 1 in PM4 should always be 0.
3. Bits 4 to 7 in PM6 should always be 1. Bits 2 and 3 in PM6 should always be 0.
4. Bits 6 and 7 in PM7 should always be 1. Bits 1 to 5 in PM7 should always be 0.
5. Bits 5 to 7 in PM12 should always be 1. Bits 3 and 4 in PM12 should always be 0.
6. Bits 1 to 7 in PM14 should always be 1. Bit 0 in PM14 should always be 0.

**78K0/KC2**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PM2 | PM27 | PM26 | PM25 | PM24 | PM23 | PM22 | PM21 | PM20 | FF22H | FFH | R/W |
| PM4 | 1 | 1 | 1 | 1 | 1 | 1 | PM41 | PM40 | FF24H | FFH | R/W |
| PM6 | 1 | 1 | 1 | 1 | PM63 | PM62 | PM61 | PM60 | FF26H | FFH | R/W |
| PM7 | 1 | 1 | PM75 | PM74 | PM73 | PM72 | PM71 | PM70 | FF27H | FFH | R/W |
| PM12 | 1 | 1 | 1 | PM124 | PM123 | PM122 | PM121 | PM120 | FF2CH | FFH | R/W |
| PM14 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | PM140 | FF2EH | FFH | R/W |

### 3.3.2 Port register

**μPD78F807x**

| | Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| <R> | P2 | 0 | 0 | 0 | P24 | P23 | P22 | P21 | P20 | FF02H | 00H (output latch) | R/W |
| | P6 | 0 | 0 | 0 | 0 | 0 | 0 | P61 | P60 | FF06H | 00H (output latch) | R/W |
| | P7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | P70 | FF07H | 00H (output latch) | R/W |
| | P12 | 0 | 0 | 0 | 0 | 0 | P122 | P121 | P120 | FF0CH | 00H (output latch) | R/W |

Cautions 1. Bits 6 and 7 in P2 should always be 0.
2. Bits 2 to 7 in P6 should always be 0.
3. Bits 1 to 7 in P7 should always be 0.
4. Bits 3 to 7 in P12 should always be 0.

**78K0/KC2**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| P2 | P27 | P26 | P25 | P24 | P23 | P22 | P21 | P20 | FF02H | 00H (output latch) | R/W |
| P6 | 0 | 0 | 0 | 0 | P63 | P62 | P61 | P60 | FF06H | 00H (output latch) | R/W |
| P7 | 0 | 0 | P75 | P74 | P73 | P72 | P71 | P70 | FF07H | 00H (output latch) | R/W |
| P12 | 0 | 0 | 0 | P124 | P123 | P122 | P121 | P120 | FF0CH | 00H (output latch) | R/W |

### 3.3.3 Pull-up resistor option register

**μPD78F807x**

| | Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| <R> | PU4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FF34H | 00H | R/W |
| | PU7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PU70 | FF37H | 00H | R/W |
| <R> | PU14 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FF3EH | 00H | R/W |

<R> Cautions 1. Bits 0 to 7 in PU4 should always be 0.
2. Bits 1 to 7 in PU7 should always be 0.
<R> 3. Bits 0 to 7 in PU14 should always be 0.

**78K0/KC2**

| | Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| <R> | PU4 | 0 | 0 | 0 | 0 | 0 | 0 | PU41 | PU40 | FF34H | 00H | R/W |
| | PU7 | 0 | 0 | PU75 | PU74 | PU73 | PU72 | PU71 | PU70 | FF37H | 00H | R/W |
| <R> | PU14 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PU140 | FF3EH | 00H | R/W |

### 3.3.4 Analog input channel specification register

**µPD78F807x**

**Address: FF29H After reset: 00H R/W**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|
| ADS | 0 | 0 | 0 | 0 | ADS2 | ADS1 | ADS0 |

<R>

| ADS2 | ADS1 | ADS0 | Analog input channel specification |
|---|---|---|---|
| 0 | 0 | 0 | ANI0 |
| 0 | 0 | 1 | ANI1 |
| 0 | 1 | 0 | ANI2 |
| 0 | 1 | 1 | ANI3 |
| 1 | 0 | 0 | ANI4 |
| 1 | 0 | 1 | Setting prohibited |
| 1 | 1 | 0 | Setting prohibited |
| 1 | 1 | 1 | Setting prohibited |

Caution Bits 3 to 7 should always be 0.

**78K0/KC2**

**Address: FF29H After reset: 00H R/W**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|
| ADS | 0 | 0 | 0 | 0 | ADS2 | ADS1 | ADS0 |

| ADS2 | ADS1 | ADS0 | Analog input channel specification |
|---|---|---|---|
| 0 | 0 | 0 | ANI0 |
| 0 | 0 | 1 | ANI1 |
| 0 | 1 | 0 | ANI2 |
| 0 | 1 | 1 | ANI3 |
| 1 | 0 | 0 | ANI4 |
| 1 | 0 | 1 | ANI5 |
| 1 | 1 | 0 | ANI6 |
| 1 | 1 | 1 | ANI7 |

Caution Bits 3 to 7 should always be 0.

### 3.3.5 A/D port configuration register

**µPD78F807x**

**Address: FF2FH After reset: 00H R/W**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ADPC | 0 | 0 | 0 | 0 | 0 | ADPC2 | ADPC1 | ADPC0 |

<R>

| ADPC2 | ADPC1 | ADPC0 | Analog input(A) / Digital I/O (D) Switching | | | | |
|---|---|---|---|---|---|---|---|
| | | | ANI4/P24 | ANI3/P23 | ANI2/P22 | ANI1/P21 | ANI0/P20 |
| 0 | 0 | 0 | A | A | A | A | A |
| 0 | 0 | 1 | A | A | A | A | D |
| 0 | 1 | 0 | A | A | A | D | D |
| 0 | 1 | 1 | A | A | D | D | D |
| 1 | 0 | 0 | A | D | D | D | D |
| 1 | 0 | 1 | D | D | D | D | D |
| Other than above | | | Setting prohibited | | | | |

Caution Bits 3 to 7 should always be 0.

**78K0/KC2**

**Address: FF2FH After reset: 00H R/W**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ADPC | 0 | 0 | 0 | 0 | ADPC3 | ADPC2 | ADPC1 | ADPC0 |

| ADPC3 | ADPC2 | ADPC1 | ADPC0 | Analog input(A) / Digital I/O (D) Switching | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | ANI5 /P27 | ANI4 /P26 | ANI5 /P25 | ANI4 /P24 | ANI3 /P23 | ANI2 /P22 | ANI1 /P21 | ANI0 /P20 |
| 0 | 0 | 0 | 0 | A | A | A | A | A | A | A | A |
| 0 | 0 | 0 | 1 | A | A | A | A | A | A | A | D |
| 0 | 0 | 1 | 0 | A | A | A | A | A | A | D | D |
| 0 | 0 | 1 | 1 | A | A | A | A | A | D | D | D |
| 0 | 1 | 0 | 0 | A | A | A | A | D | D | D | D |
| 0 | 1 | 0 | 1 | A | A | A | D | D | D | D | D |
| 0 | 1 | 1 | 0 | A | A | D | D | D | D | D | D |
| 0 | 1 | 1 | 1 | A | D | D | D | D | D | D | D |
| 1 | 0 | 0 | 0 | D | D | D | D | D | D | D | D |
| Other than above | | | | Setting prohibited | | | | | | | |

### 3.3.6 External interrupt rising/falling edge enable register

**µPD78F807x**

**Address: FF48H After reset: 00H R/W**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| EGP | 0 | 0 | EGP5 | EGP4 | EGP3 | EGP2 | EGP1 | EGP0 |

Caution Bits 6 and 7 should always be 0.

**Address: FF49H After reset: 00H R/W**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| EGN | 0 | 0 | EGN5 | EGN4 | EGN3 | EGN2 | EGN1 | EGN0 |

Caution Bits 6 and 7 should always be 0.

**78K0/KC2**

**Address: FF48H After reset: 00H R/W**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| EGP | 0 | EGP6 | EGP5 | EGP4 | EGP3 | EGP2 | EGP1 | EGP0 |

**Address: FF49H After reset: 00H R/W**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| EGN | 0 | EGN6 | EGN5 | EGN4 | EGN3 | EGN2 | EGN1 | EGN0 |

### 3.3.7 Key return mode register

**µPD78F807x**

**Address: FF6EH After reset: 00H R/W**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| KRM | 0 | 0 | 0 | 0 | 0 | 0 | 0 | KRM0 |

Caution Bits 1 to 7 should always be 0.

**78K0/KC2**

**Address: FF6EH After reset: 00H R/W**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| KRM | 0 | 0 | 0 | 0 | KRM3 | KRM2 | KRM1 | KRM0 |

### 3.3.8 Watch timer operation mode register

**µPD78F807x**

**Address: FF6FH After reset: 00H R/W**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | <1> | <0> |
|---|---|---|---|---|---|---|---|---|
| WTM | 0 | WTM6 | WTM5 | WTM4 | WTM3 | WTM2 | WTM1 | WTM0 |

Caution Bit 7 is a read-only bit and should be fixed to 0.

**78K0/KC2**

**Address: FF6FH After reset: 00H R/W**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | <1> | <0> |
|---|---|---|---|---|---|---|---|---|
| WTM | WTM7 | WTM6 | WTM5 | WTM4 | WTM3 | WTM2 | WTM1 | WTM0 |

| WTM7 | Watch timer count clock selection (fW) | | | | | |
|---|---|---|---|---|---|---|
| | | $f_{SUB}$= 32.768 kHz | $f_{PRS}$ = 2 MHz | $f_{PRS}$ = 5 MHz | $f_{PRS}$ = 10 MHz | $f_{PRS}$ = 20 MHz |
| 0 | $f_{PRS}/2^7$ | - | 15.625 kHz | 39.062 kHz | 78.125 kHz | 156.25 kHz |
| 1 | $f_{SUB}$ | 32.768 k HZ | - | | | |

Remarks 1. $f_W$: Watch timer clock frequency ($f_{PRS}/2^7$ or $f_{SUB}$)
2. $f_{PRS}$: Peripheral hardware clock frequency
3. $f_{SUB}$: Subsystem clock frequency

### 3.3.9 Clock operation mode select register

**µPD78F807x**

**Address: FF9FH After reset: 00H R/W**

| Symbol | <7> | <6> | 5 | 4 | 3 | 2 | 1 | <0> |
|---|---|---|---|---|---|---|---|---|
| OSCCTL | EXCLK | OSCSEL | 0 | 0 | 0 | 0 | 0 | AMPH |

Caution Bits 4 and 5 should always be 0.

**78K0/KC2**

**Address: FF9FH After reset: 00H R/W**

| Symbol | <7> | <6> | <5> | <4> | 3 | 2 | 1 | <0> |
|---|---|---|---|---|---|---|---|---|
| OSCCTL | EXCLK | OSCSEL | EXCLKS | OSCSELS | 0 | 0 | 0 | AMPH |

### 3.3.10 Processor clock control register

**µPD78F807x**

**Address: FFFBH After reset: 01H R/W**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PCC | 0 | 0 | 0 | 0 | 0 | PCC2 | PCC1 | PCC0 |

Cautions 1. Bit 5 is a read-only bit.
2. Bits 4 and 6 should always be 0.

**78K0/KC2**

**Address: FFFBH After reset: 01H R/W**

| Symbol | 7 | 6 | <5> | <4> | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PCC | 0 | XTSTART | CLS | CSS | 0 | PCC2 | PCC1 | PCC0 |

Caution 1. Bit 5 is a read-only bit.

### 3.3.11 IIC clock selection register 0

**µPD78F807x**

**Address: FFA8H After reset: 00H R/W**

| Symbol | 7 | 6 | <5> | <4> | <3> | <2> | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| IICCL0 | 0 | 0 | CLD0 | DAD0 | SMC0 | DFC0 | CL01 | CL00 |

**Selection Clock Setting**

| IICX0 | IICCL0 | | | Selection Clock (fw) | Transfer Clock (fw/m) | Settable Selection Clock (fw) Range | Operation Mode |
|---|---|---|---|---|---|---|---|
| Bit 0 | Bit 3 | Bit 1 | Bit 0 | | | | |
| CLX0 | SMC0 | CL01 | CL00 | | | | |
| 0 | 0 | 0 | 0 | $f_{PRS}/2$ | fw/44 | 2.00 to 4.19 MHz | Normal mode (SMC0 bit = 0) |
| 0 | 0 | 0 | 1 | $f_{PRS}/2$ | fw/86 | 4.19 to 8.38 MHz | |
| 0 | 0 | 1 | 0 | $f_{PRS}/4$ | fw/86 | | |
| 0 | 0 | 1 | 1 | Setting prohibited | | | |
| 0 | 1 | 0 | x | $f_{PRS}/2$ | fw/24 | 4.00 to 8.38 MHz | High-speed mode (SMC0 bit = 1) |
| 0 | 1 | 1 | 0 | $f_{PRS}/4$ | fw/24 | | |
| 0 | 1 | 1 | 1 | Setting prohibited | | | |
| 1 | 0 | x | x | Setting prohibited | | | |
| 1 | 1 | 0 | x | $f_{PRS}/2$ | fw/12 | 4.00 to 4.19 MHz | High-speed mode (SMC0 bit = 1) |
| 1 | 1 | 1 | 0 | $f_{PRS}/4$ | fw/12 | | |
| 1 | 1 | 1 | 1 | Setting prohibited | | | |

**78K0/KC2**

**Address: FFA8H After reset: 00H R/W**

| Symbol | 7 | 6 | <5> | <4> | <3> | <2> | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| IICCL0 | 0 | 0 | CLD0 | DAD0 | SMC0 | DFC0 | CL01 | CL00 |

**Selection Clock Setting**

| IICX0 | IICX0 | | | Selection Clock (fw) | Transfer Clock (fw/m) | Settable Selection Clock (fw) Range | Operation Mode |
|---|---|---|---|---|---|---|---|
| Bit 0 | Bit 3 | Bit 1 | Bit 0 | | | | |
| CLX0 | SMC0 | CL01 | CL00 | | | | |
| 0 | 0 | 0 | 0 | $f_{PRS}$/2 | fw/44 | 2.00 to 4.19 MHz | Normal mode (SMC0 bit = 0) |
| 0 | 0 | 0 | 1 | $f_{PRS}$/2 | fw/86 | 4.19 to 8.38 MHz | |
| 0 | 0 | 1 | 0 | $f_{PRS}$/4 | fw/86 | | |
| 0 | 0 | 1 | 1 | $f_{EXSCL0}$ | fw/66 | 6.4 MHz | |
| 0 | 1 | 0 | x | $f_{PRS}$/2 | fw/24 | 4.00 to 8.38 MHz | High-speed mode (SMC0 bit = 1) |
| 0 | 1 | 1 | 0 | $f_{PRS}$/4 | fw/24 | | |
| 0 | 1 | 1 | 1 | $f_{EXSCL0}$ | fw/18 | 6.4 MHz | |
| 1 | 0 | x | x | Setting prohibited | | | |
| 1 | 1 | 0 | x | $f_{PRS}$/2 | fw/12 | 4.00 to 4.19 MHz | High-speed mode (SMC0 bit = 1) |
| 1 | 1 | 1 | 0 | $f_{PRS}$/4 | fw/12 | | |
| 1 | 1 | 1 | 1 | Setting prohibited | | | |

Remarks 1. x: Don't care
2. $f_{PRS}$: Peripheral hardware clock frequency
3. $f_{EXSCL0}$: External clock frequency from EXSCL0 pin

### 3.3.12 Interrupt request flag register (IF1L)

**µPD78F807x**

**Address: FFE2H After reset: 00H R/W**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| IF1L | 0 | 0 | WTIF | KRIF | TMIF51 | WTIIF | SRIF0 | ADIF |

Caution 1. Bits 6 and 7 should always be 0.

**78K0/KC2**

**Address: FFE2H After reset: 00H R/W**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| IF1L | 0 | PIF6 | WTIF | KRIF | TMIF51 | WTIIF | SRIF0 | ADIF |

### 3.3.13 Interrupt mask flag register (MK1L)

**µPD78F807x**

**Address: FFE6H After reset: 01H R/W**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| MK1L | 1 | 1 | WTMK | KRMK | TMMK51 | WTIMK | SRMK0 | ADMK |

Caution 1. Bits 6 and 7 should always be 1.

**78K0/KC2**

**Address: FFE6H After reset: 01H R/W**

| Symbol | 7 | 6 | <5> | <4> | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| MK1L | 1 | PMK6 | WTMK | KRMK | TMMK51 | WTIMK | SRMK0 | ADMK |

### 3.3.14 Priority specification flag register (PR1L)

**µPD78F807x**

**Address: FFEAH After reset: 00H R/W**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PR1L | 1 | 1 | WTPR | KRPR | TMPR51 | WTIPR | SRPR0 | ADPR |

Caution 1. Bits 6 and 7 should always be 1.

**78K0/KC2**

**Address: FFEAH After reset: 00H R/W**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PR1L | 1 | PPR6 | WTPR | KRPR | TMPR51 | WTIPR | SRPR0 | ADPR |

# 4. Writing with Flash Programmer

Data can be written to the flash memory on-board or off-board, by using a dedicated flash programmer.

**(1) On-board programming**

The contents of the flash memory can be rewritten after the device has been mounted on the target system. The connectors that connect the dedicated flash programmer must be mounted on the target system.

**(2) Off-board programming**

Data can be written to the flash memory with a dedicated program adapter (FA series) before the device is mounted on the target system.

Remark The FA series is a product of Naito Densei Machida Mfg. Co., Ltd.

**Table 4-1. Wiring Dedicated Flash Programmer**

| Pin Configuration of Dedicated Flash Programmer | | | With CSI10 | | With UART6 | |
|---|---|---|---|---|---|---|
| Signal Name | I/O | Pin Function | Pin Name | Pin No. 64 Pins | Pin Name | Pin No. 64 Pins |
| SI/RxD | Input | Receive signal | SO10/P12 | 24 | TxD6/P13 | 23 |
| SO/TxD | Output | Transmit signal | SI10/RxD0/P11 | 25 | RxD6/P14 | 22 |
| SCK | Output | Transfer clock | $\overline{SCK10}$/TxD0/P10 | 26 | - | - |
| CLK | Output | Clock to Micro | -Note 1 | - | Note2 | Note2 |
| $\overline{RESET}$ | Output | Reset signal | $\overline{RESET}$ | 5 | $\overline{RESET}$ | 5 |
| FLMD0 | Output | Mode signal | FLMD0 | 6 | FLMD0 | 6 |
| $V_{DD}$ | I/O | $V_{DD}$ voltage generation/ power monitoring | $V_{DD}$ | 11 | $V_{DD}$ | 11 |
| | | | $AV_{REF}$ | 58 | $AV_{REF}$ | 58 |
| | | | VRO | 49 | VRO | 49 |
| | | | VRS | 50 | VRS | 50 |
| <R> | | | SUP | 46 | SUP | 46 |
| | | | SUP1 to SUP6 | 29, 30, 35, 36, 41, 42 | SUP1 to SUP6 | 29, 30, 35, 36, 41, 42 |
| | | | MOD1 | 54 | MOD1 | 54 |
| $V_{SS}$ | - | GND | $V_{SS}$ | 10 | $V_{SS}$ | 10 |
| | | | $AV_{SS}$ | 59 | $AV_{SS}$ | 59 |
| | | | GND | 51 | GND | 51 |
| | | | GND1 to GND6 | 27, 32, 33, 38, 39, 44 | GND1 to GND6 | 27, 32, 33, 38, 39, 44 |
| | | | GND_DRV | 53 | GND_DRV | 53 |
| | | | MOD2 | 55 | MOD2 | 55 |
| | | | MSLP | 18 | MSLP | 18 |
| | | | SRC | 56 | SRC | 56 |
| <R> | | | RESET_A | 57 | RESET_A | 57 |

Notes 1. Only the internal high-speed oscillation clock ($f_{RH}$) can be used when CSI10 is used.

2. Only the X1 clock ($f_X$) or external main system clock ($f_{EXCLK}$) can be used when UART6 is used. When using the clock out of the flash programmer, connect CLK and EXCLK of the programmer.

PG-FP5, FL-PR5: Please connect the programmer's CLK to EXCLK/X2/P122.

# 5. Power Supply Circuit

## 5.1 Power Supply Function

The power supply circuit is a series regulator that generates 5 V (typ.) output voltage from 12 V battery supply voltage.

- Regulator output function
- External sensor power supply output function
- Over current protection function
- Low-voltage detection function
- External dropper auxiliary function

## 5.2 Regulator Output Function

The regulator output function generates 5 V (typ.) from 12-V battery supply voltage.

## 5.3 External Sensor Power Supply Output Function

The external sensor power supply output function generates the external sensor voltage from the 5-V (typ.) regulator output voltage.

The output can be controlled using the SVDDON bit in the system control register (SC).

## 5.4 Over Current Protection Function

The over current protection function limits the current to protect the device if the over current flows in the regulator output due to load short-circuiting.

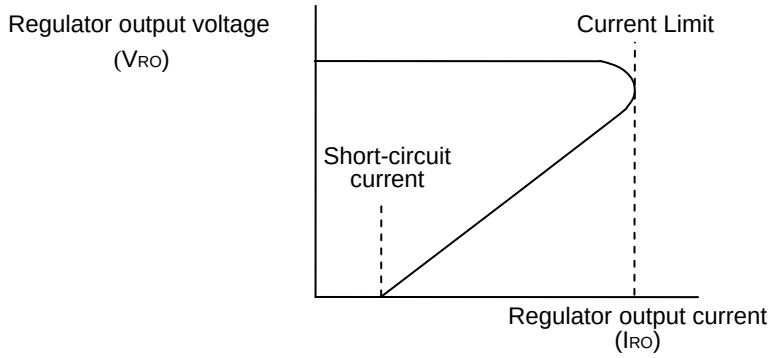
The normal state automatically recovers when the over current disappears. If the over current flows in the external sensor power supply output, the SVDD bit in the system control register (SC) is cleared, turning off the output forcibly. The over current in the external sensor power supply output can be checked using the SVDDOC bit in the system status register (SS).

<R> Regulator output current limit: 51 mA (min., 7 V ≤ VSUP ≤ 19 V), 26 mA (min., 6 V ≤ VSUP < 7 V)

SVDD output shutdown current: 21 mA (min.)

Caution When the external dropper auxiliary function is used, the over current protection function is not available for the regulator output.

**Figure 5-1. Regulator Output Current Limit Characteristics**




## 5.5 Low-Voltage Detection Function

The low-voltage detection function detects a drop in a regulator output voltage caused by load short-circuiting. The regulator output voltage can be checked using the LVI bit in the system status register.

Low-voltage detection value: 4.2 V (typ.)

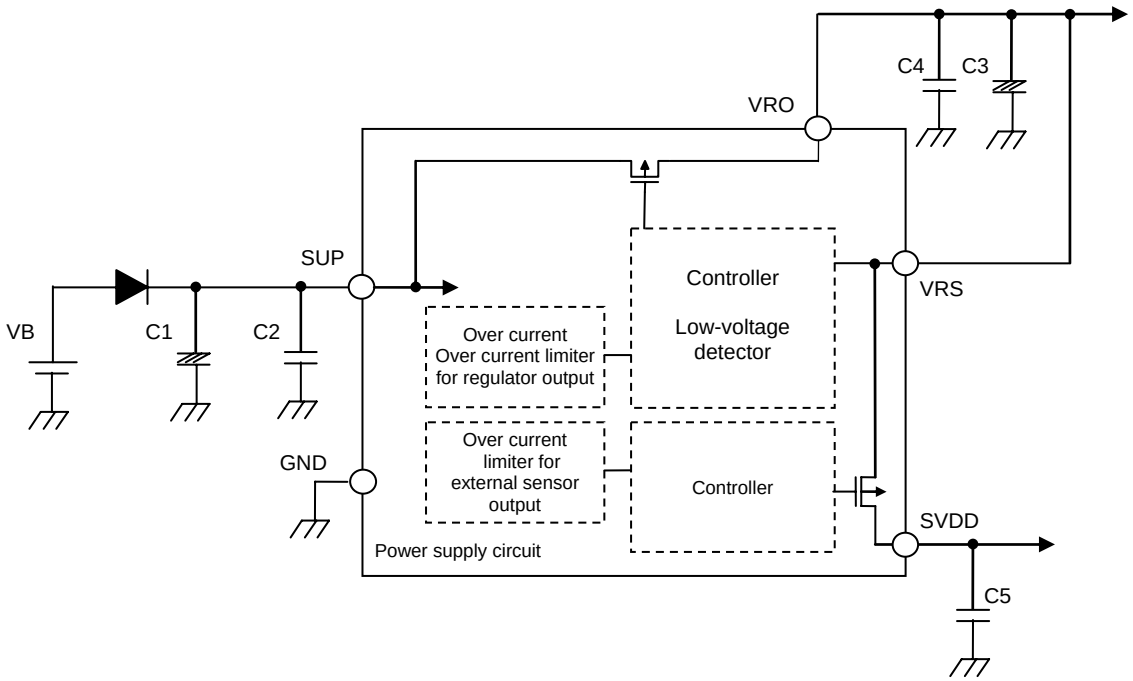
## 5.6 External Dropper Auxiliary Function

The external dropper auxiliary function allows enhancing the output current capability by adding an external dropper (NPN transistor) to the 5-V output dropper according to the output current.

Output current: When 2SD1584 is used, 150 mA (min.)

<R> Caution When the external dropper auxiliary function is used, the over current protection function is not available for the regulator output.

<R> **Figure 5-2. Power Supply Circuit Application Example Using On-Chip P-ch MOS**

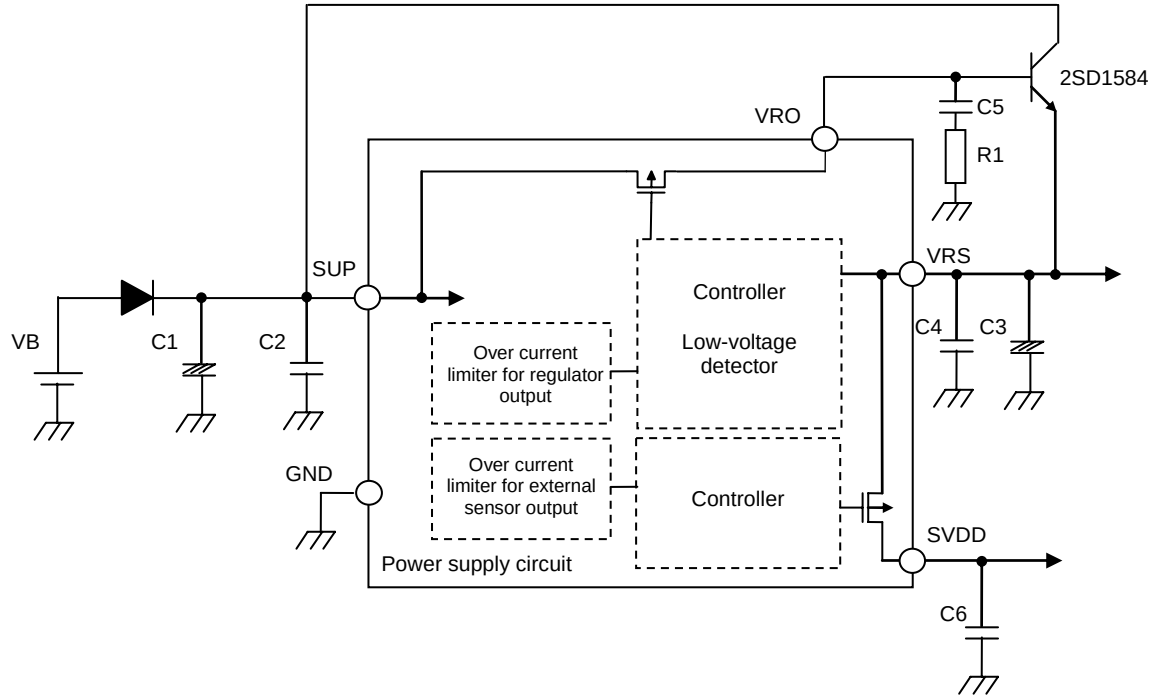



Recommended values for external capacitors

C1 ≥ 33 μF
C2 ≥ 0.01 μF
4.7 μF ≤ C3 ≤ 100 μF
C4 ≥ 0.01 μF
<R> C5 ≤ 0.01 μF

Caution Place the ceramic capacitors (C2 and C4) between the SUP and GND pins and between the VRO and GND pins, close to the SUP and VRO pins and use the shortest possible wiring.

<R> **Figure 5-3. Power Supply Circuit Application Example Using External NPN Transistor**




Recommended values for external capacitors and resistors

C1 ≥ 33 μF
C2 ≥ 0.01 μF
4.7 μF ≤ C3 ≤ 100 μF
C4 ≥ 0.01 μF
C5: TBD
R1: TBD
<R> C6 ≤ 0.01 μF

Cautions1. Place the ceramic capacitors (C2 and C4) between the SUP and GND pins and between the VRS and GND pins, close to the SUP and VRS pins and use the shortest possible wiring.

2. Place the external NPN transistor close to the VRO, VRS, and SUP pins and use the shortest possible wiring for the base, emitter, and collector.

3. Place the ceramic capacitor (C5) and resistor (R1) between the VRO and GND pins, close to the VRO pin and use the shortest possible wiring.

# 6. LIN Transceiver

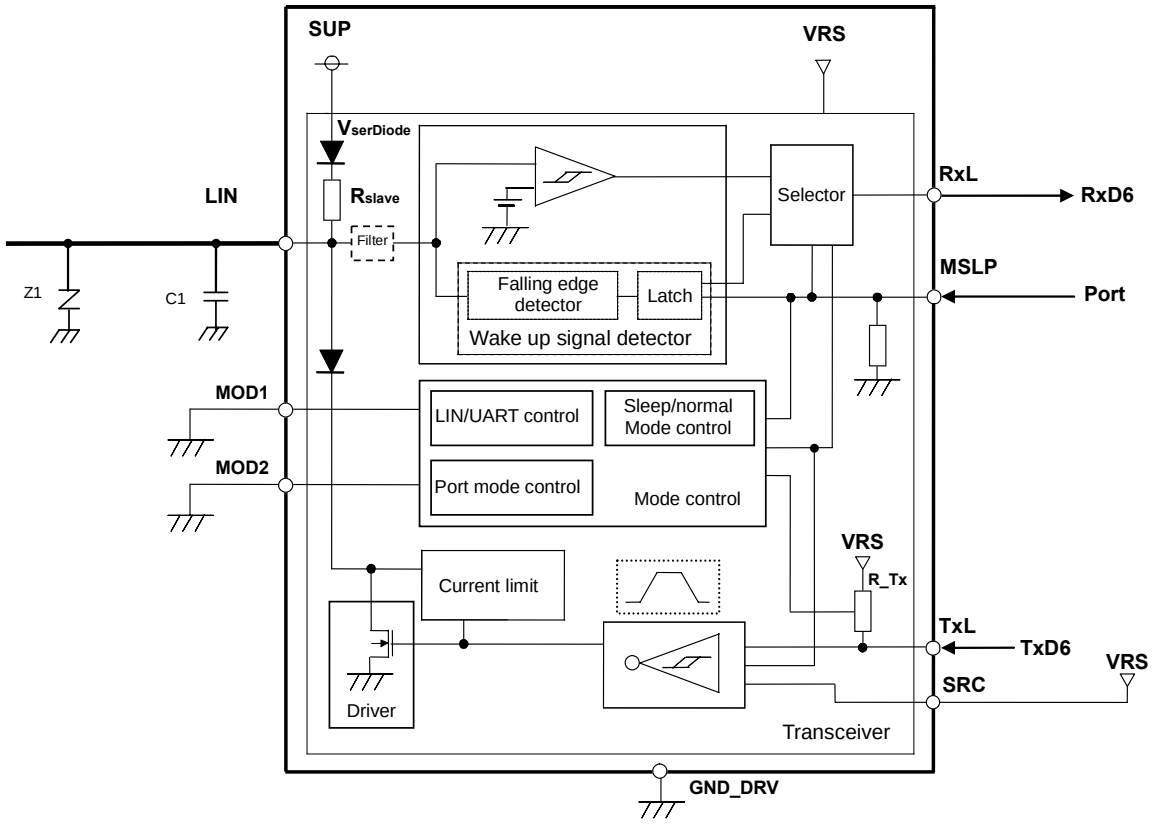
## 6.1 LIN Transceiver Function

<R> The LIN transceiver and external specifications comply with LIN Specifications Rev.2.0, 2.1.

The LIN transceiver has the following functions.

— Sleep function
— Over current protection function

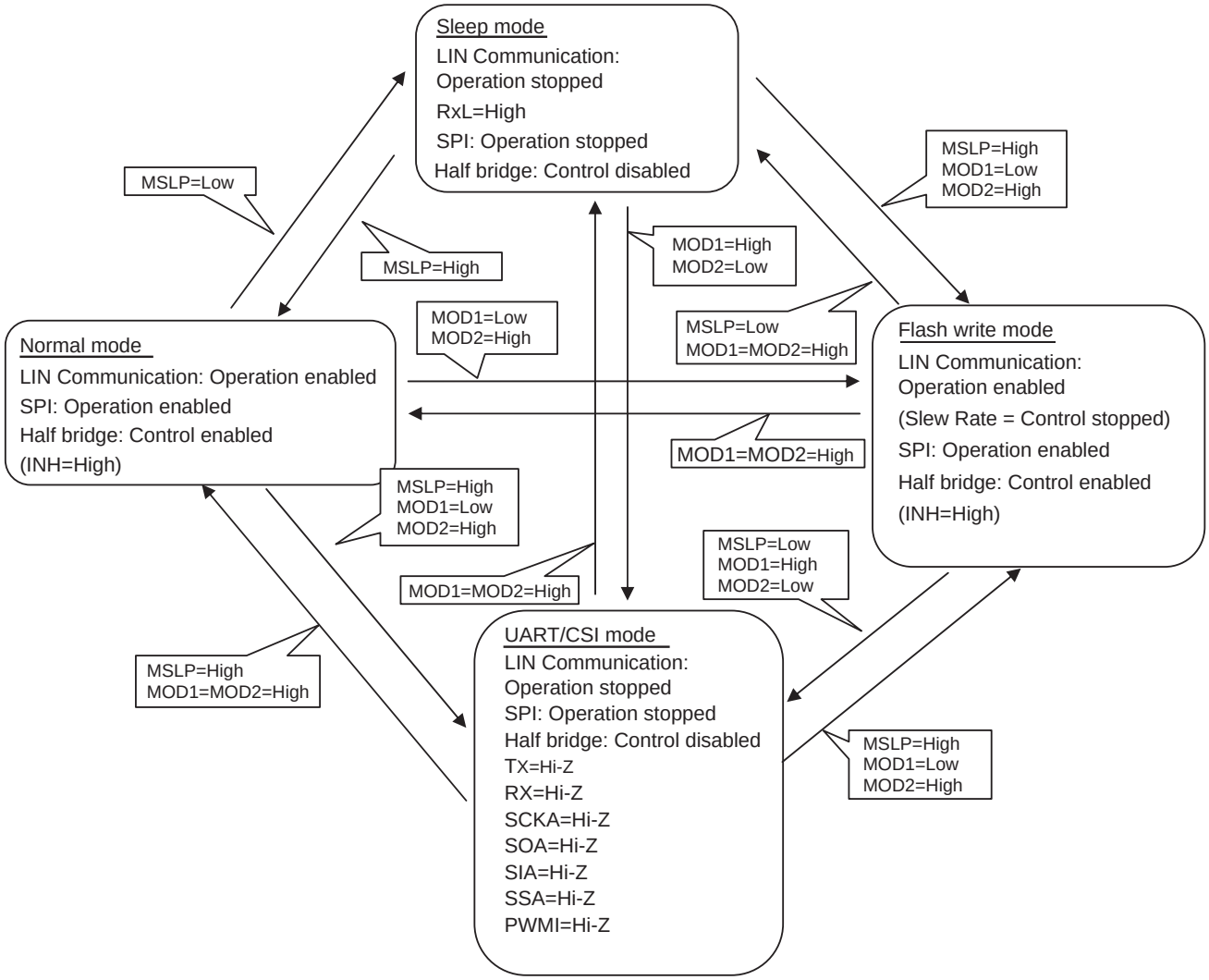
**Figure 6-1. LIN Transceiver Application Example**




Remarks 1. RxL pin is connected to RxD6 and TxL pin is connected to TxD6 in the package.
2. LIN pin includes slave pull-up register and diode.

## 6.2 Operation Modes

<R> **Figure 6-2. Operation Mode Transition Diagram**




<R> **Table 6-1. LIN Operation Mode Setting**

| LIN Operation Mode | Slew Rate | Port Mode[Note] | MSLP | SRC | MOD1 | MOD2 |
|---|---|---|---|---|---|---|
| LIN sleep | - | Port mode A | L | × | H | H |
| LIN normal | Fast | Port mode A | H | H | H | H |
| | Slow | Port mode A | H | L | H | H |
| Flash write | OFF | Port mode A | H | × | L | H |
| UART/CSI mode | - | Port mode B | L | × | H | L |

Note For the pin states in each port mode, refer to table 6-2, Pin States in Each Port Mode.

<R> Caution MOD1 = MOD2 = Low is setting prohibited.

Remark ×: Don't care

<R>

**Table 6-2. Pin States in Each Port Mode**

| Port Mode | INH | SCKA | SOA | SIA | SSA | PWMI | TxL | RxL | States of Analog Functions |
|---|---|---|---|---|---|---|---|---|---|
| Port mode A | Pull-up input | Pull-down input | Output/ Hi-Z (Sleep) | Pull-down input | Pull-up input | Pull-down input | Pull-up input | Output | SPI communication enabled in the normal/flash write mode |
| Port mode B | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | SPI communication, and LIN transceiver stopped (for P10, P11, P12, P13, P14, P15, and P16, only the function of the microcontroller is available). |

<R>

**Table 6-3. Operation States of Each Analog Function Block**

| Function Block | | Normal mode | Sleep mode | UART/CSI mode | Flash write mote |
|---|---|---|---|---|---|
| Power supply circuit | Regulator output | Operation enabled | Operation enabled | Operation enabled | Operation enabled |
| | External sensor power supply output | Control enabled | Control disabled (output state before entering the sleep mode retained) | Control disabled (output state before entering the UART/CSI mode retained) | Control enabled |
| | Low voltage detector | Operation enabled | Operation enabled | Operation enabled | Operation enabled |
| | Over current limiter[Note] | Operation enabled | Operation enabled | Operation enabled | Operation enabled |
| LIN transceiver | | Operation enabled | Operation stopped (LIN: recessive) | Operation stopped (LIN: recessive) | Operation enabled |
| Half-bridge circuit | | INH=High: Control enabled INH=Low: Control disabled (Hi-Z) | Control disabled (when INH = high, output state before entering the sleep mode retained; when INH = low, Hi-Z) | Control disabled (when INH = high, output state before entering the UART/CSI mode retained; when INH = low, Hi-Z) | INH=High: Control disabled INH=Low: Control disabled (Hi-Z) |
| | Over current limiter | Operation enabled | Operation stopped | Operation stopped | Operation enabled |
| SPI & PWM controller | | Control enabled | Operation stopped | Operation stopped | Control enabled |
| Analog power-on clear (POCA) circuit | | Operation enabled | Operation enabled | Operation enabled | Operation enabled |
| Thermal shutdown function | | Operation enabled | Operation stopped | Operation stopped | Operation enabled |

Note Applicable only when the internal P-ch MOS is used for a 5-V output dropper.

- Sleep mode

<R> When MSLP is low and MOD1 and MOD2 are high, the sleep mode is entered (the MSLP pin is internally pulled down).

In the sleep mode, the LIN driver output is off (recessive) regardless of the TxL pin input state, thus leading to the low-power consumption state. In the sleep mode, the LIN bus monitor function is active; when the recessive-to-dominant edge is detected on the LIN bus, the RxL pin goes low from high thus inputting a high level signal to the MSLP pin and is held low until the normal mode is entered.

- Normal mode

<R> When MSLP is high and MOD1 and MOD2 are high, the normal mode is entered.

In the normal mode, driving the TxL pin high turns off the LIN driver output (recessive) and driving the TxL pin low places the LIN driver in the dominant state.

When the LIN bus is in the dominant state, the RxL pin outputs a low level signal and when in the recessive state, the RxL pin outputs a high level signal.

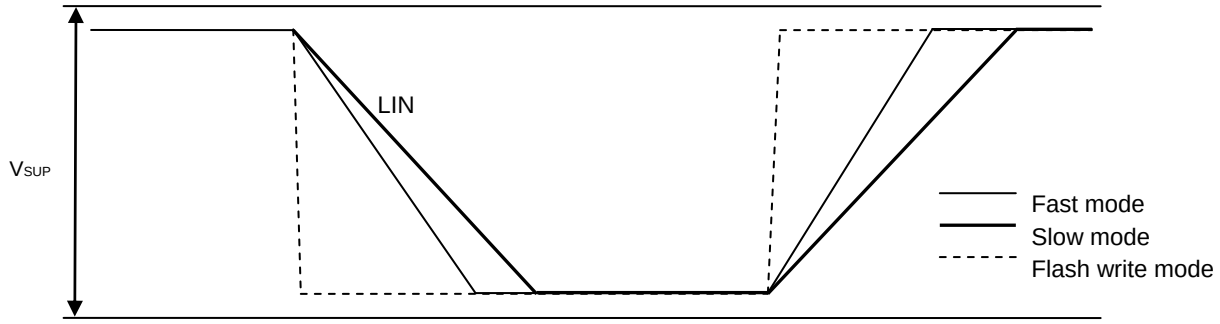
In the normal mode, communication via the LIN bus is enabled.

The slew rates can be switched according to the SRC pin state.

— SRC = High · · · Fast mode
20-Kbps baud rate is supported.

— SRC = Low · · · Slow mode
10.4-Kbps baud rate is supported.

**Figure 6-2. Slew Rate Response Timing**



- Flash write mode

When MSLP is high, MOD1 is low, and MOD2 is high, the flash write mode is entered.

This is a 100-Kbps baud rate mode, in which flash ROM can be programmed at a high speed via the LIN bus.

Caution No slew rate can be set in the flash write mode.

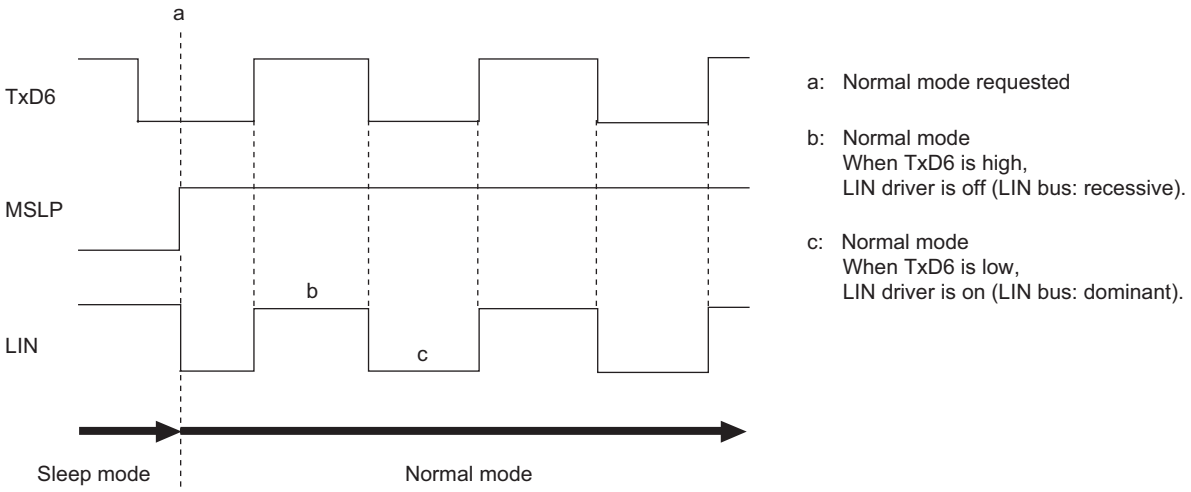
- UART/CSI mode

When MSLP is low, MOD1 is high, and MOD2 is low, the UART/CSI mode is entered.

Flash ROM can be programmed on board via UART6 or CSI10.

**Figure 6-3. Normal Mode Timing Chart**

**(a) Normal mode transmission (TxD6→LIN)**




**(b) Normal mode reception (LIN→RxD6)**

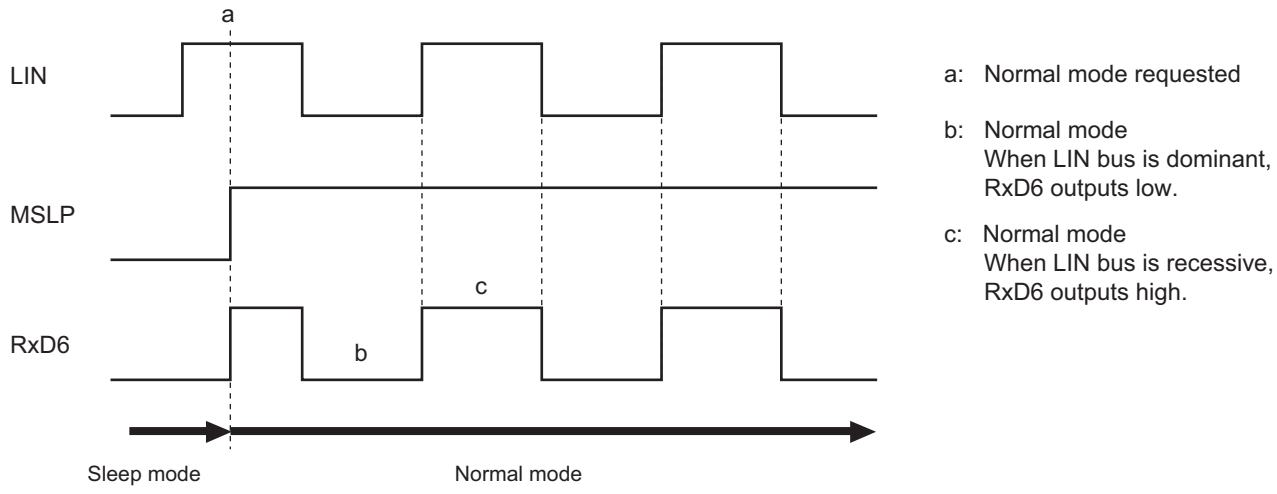
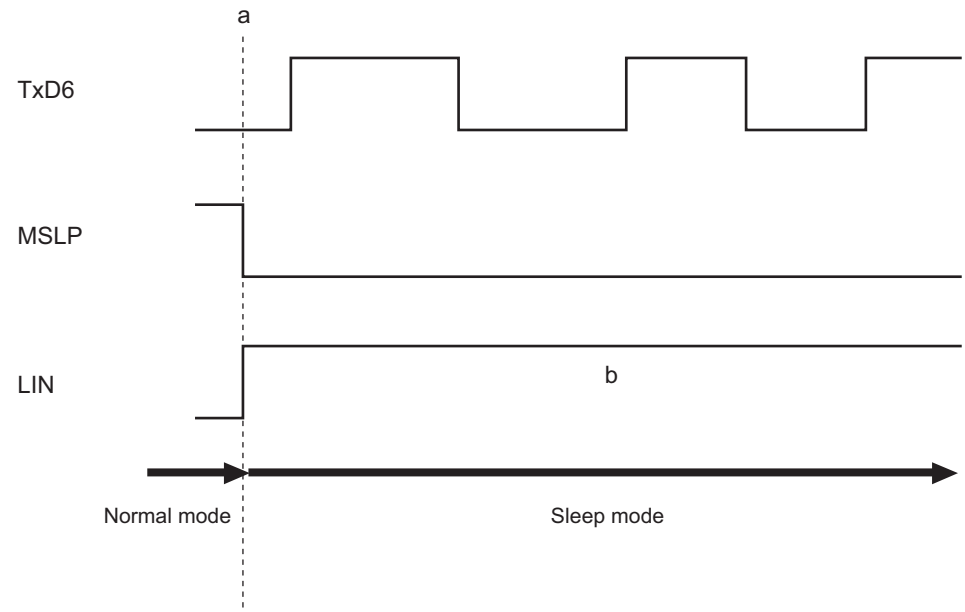


**Figure 6-4. Sleep Mode Timing Chart**

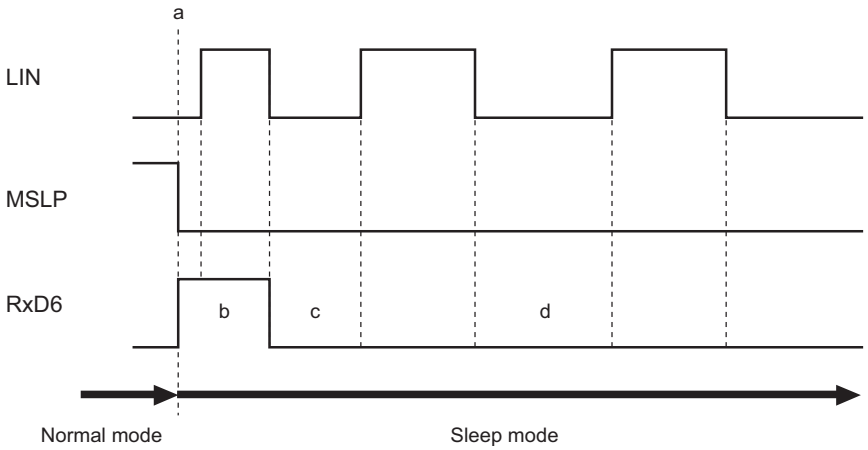
**(a) Sleep mode transmission (TxD6→LIN)**




a: Sleep mode requested

b: LIN driver output is off (LIN bus: recessive).

**(b) Sleep mode reception (LIN→RxD6)**




a: Sleep mode requested

b: Sleep mode
RxD6 outputs high.

c: Sleep mode
RxD6 outputs low
when a LINI falling edge is detected.

d: Sleep mode
RxD6 is held low until the normal mode transition request is received from the microcontroller.

## 6.3 Over Current Limiter

The over current limiter forcibly turns off the LIN driver (recessive) for protection when an over current flows in the LIN driver caused by load short-circuiting. An over current in the LIN driver can be monitored using the LOC bit in the system status register (SS).

After detecting an over current, the LIN bus is held off (recessive); inputting a high level signal to the TxL pin allows the bus to recover.

Current limit: 40 mA (min.)

# 7. Half-Bridge Circuit

The half-bridge circuit incorporates six half-bridge driver channels.

<R> To use the half-bridge circuit, set MSLP to high, INH to high, and port mode to A.

## 7.1 Half-Bridge Drivers

- HBO: 6 channels

Application: Compact motor drivers

The output can be controlled by the system control register (SC), half-bridge control register (HBC), and PWM input control register (PICL) when MSLP and INH are both high. For PWM control of the low-side MOSFET of the half-bridge drivers, the low-side MOSFET to which the PWM control signal is to be input can be selected by the PWM input control register (PICL). The PWM control signal should be input to the PWMI pin.

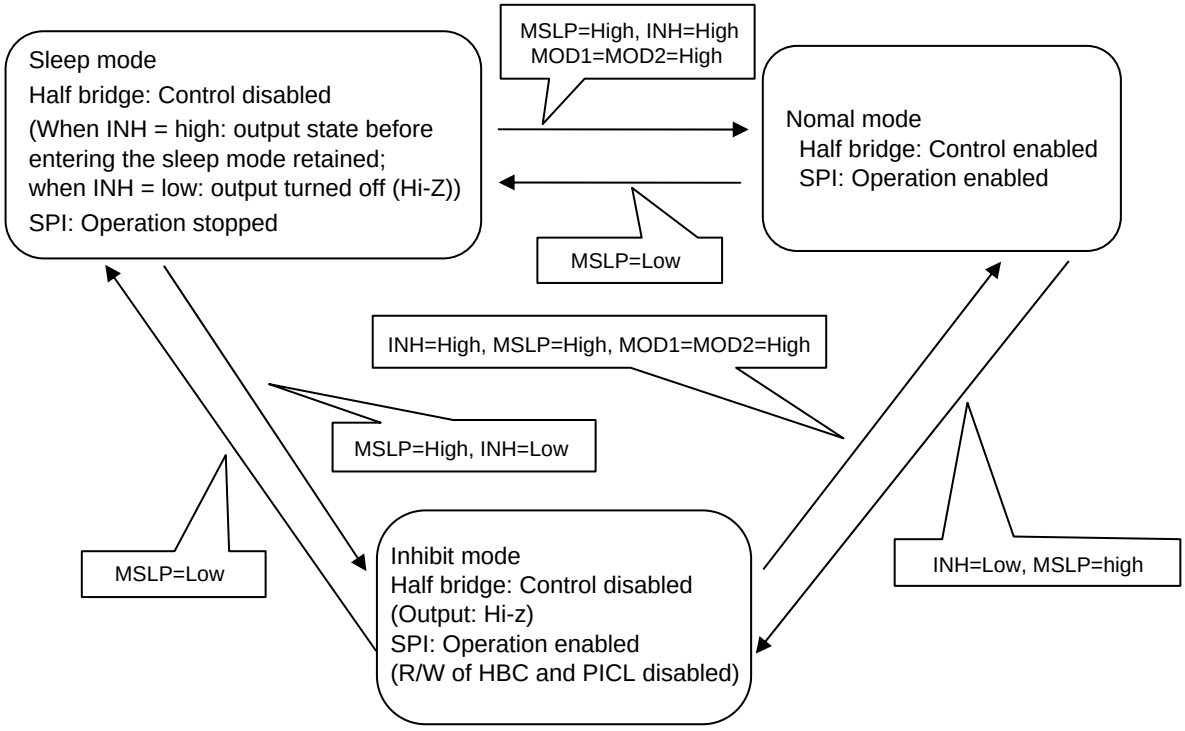
Inputting a low level signal to the INH pin when the pin is high clears the half-bridge control register (HBC) and PWM input control register (PICL), turning off the output of all the half-bridge drivers. Writing to these registers while INH is low is ignored.

In the sleep mode, the half-bridge drivers retain the output state before entering the sleep mode. However, if the sleep mode is entered with the high-side driver turned on, the output of the pertinent half-bridge driver is Hi-Z since the internal charge pump circuit stops during the sleep mode.

Caution To reset the half-bridge control register (HBC) and PWM input control register (PICL) by inputting a low level signal to the INH pin when the pin is high, input a low level signal to the INH pin at least 10 μs.

**Mode transition diagram**

<R>




<R>

**Table 7-1. Operation State in Inhibit Mode**

| Function Block | | Inhibit Mode |
|---|---|---|
| Power supply circuit | Regulator output | Operation enabled |
| | External sensor power supply output | Operation enabled |
| | Low voltage detector | Operation enabled |
| | Over current limiter | Operation enabled |
| LIN transceiver | | Operation enabled |
| <R> Half bridge circuit | | Control disabled (output off (Hi-z)) |
| SPI & PWM controller | | Operation enabled |
| <R> Analog power-on clear (POCA) circuit | | Operation enabled |
| Thermal shutdown function | | Operation enabled |

## 7.2 Over Current Protection Function

The half-bridge drivers incorporate over current limiters to protect the device.

<R> The over current limiter forcibly turns off the half-bridge driver output for protection when the current exceeding the detection value (-1.4 A max. for high-side MOSFET; 1.4 A min. for low-side MOSFET) caused by load short-circuiting is detected in a half-bridge driver. Using the HBOCS bit in the system control register (SC), the driver channels to be protected against an over current can be selected. When the HBOCS bit in the system control register (SC) is 0, if an over current occurs in any of HBO1 to HBO3, bits 4 to 9 in the half-bridge control register (HBC) and bits 2 to 4 in the PWM input control register (PICL) are cleared and the outputs from HBO1 to HBO3 are forcibly turned off. Similarly, if an over current occurs in any of HBO4 to HBO6, bits 10 to 15 in the half-bridge control register (HBC) and bits 5 to 7 in the PWM input control register (PICL) are cleared and the outputs from HBO4 to HBO6 are forcibly turned off. When the HBOCS bit in the system control register (SC) is 1, the half-bridge control register (HBC) and PWM input control register (PICL) are entirely cleared and the outputs from all the half-bridge drivers are forcibly turned off. An over current in the half-bridge drivers can be monitored using the system status register (SS) and half-bridge status register (HBS).

Caution: 1. The over current protection function incorporated in the half-bridge circuit is intended to protect the device in the abnormal situation; use this function only when it is absolutely necessary.

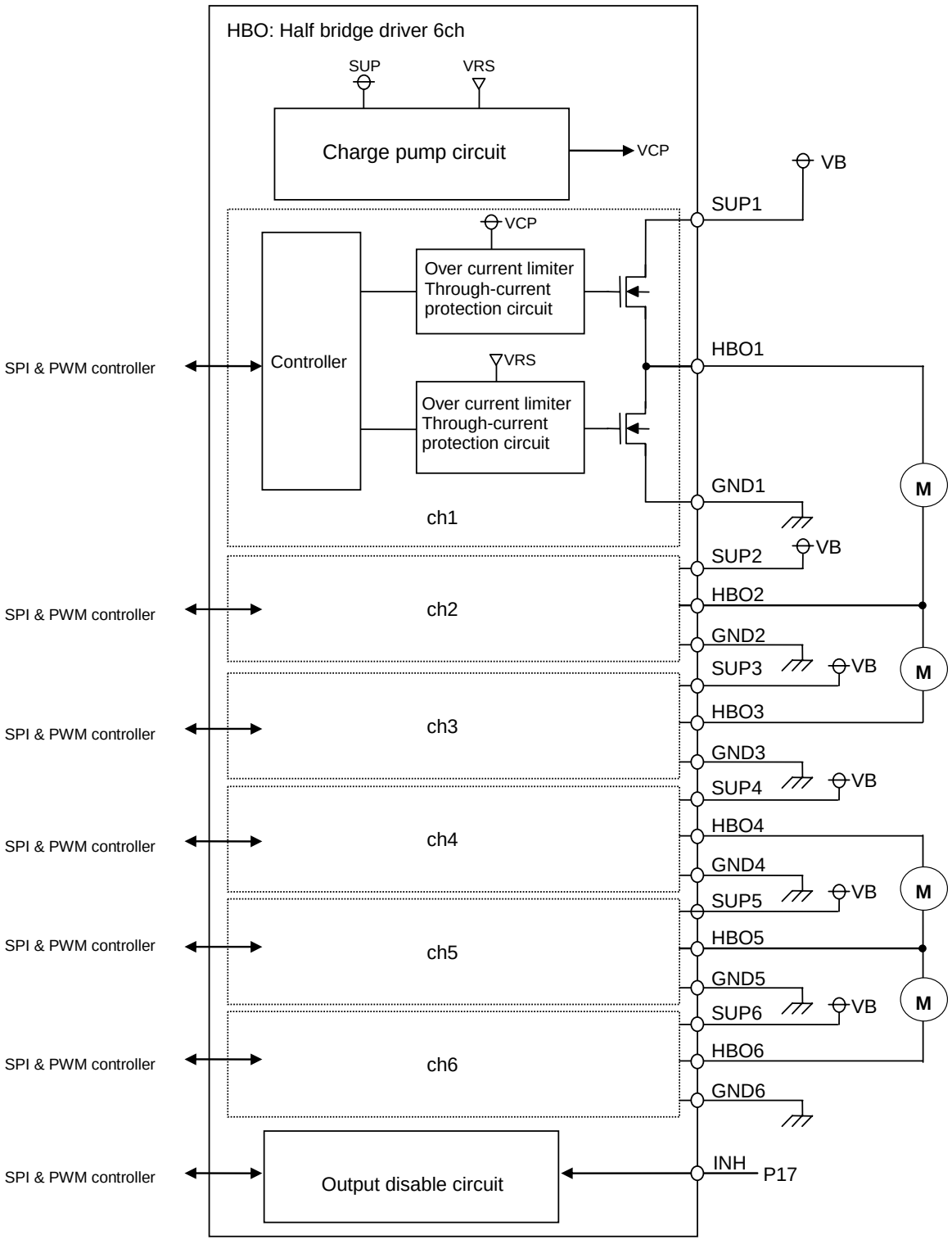
## 7.3 Through-Current Protection Function

The half-bridge drivers incorporate dead time generation circuits to protect the device against a through-current.

The dead time generation circuit receives the data written to the half-bridge control register (HBC) and allows the data to be output from the half-bridge driver after the switching delay time (TBD μs typ.) after data which value changes to 1 from 0 is latched in HBnH and HBnL.

Remark n = 1 to 6

**Figure 7-1. Half-Bridge Circuit Application Example**




Caution The SUP potential should be the same as the SUP1 to SUP6 potential, and the GND potential should be the same as the GND1 to GND6 and GND_DRV potential.

# 8. SPI & PWM Controller

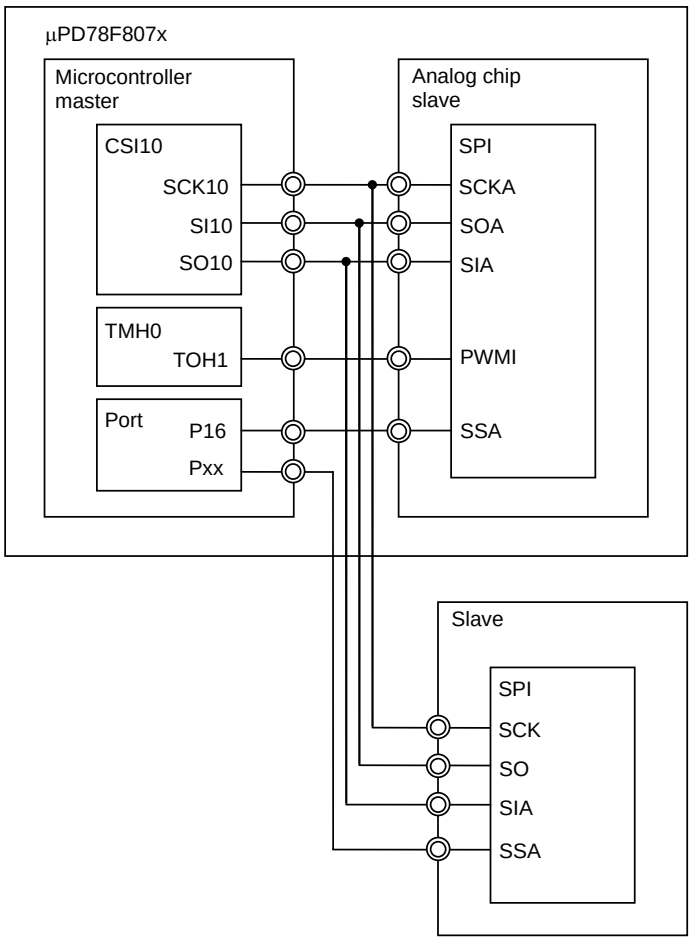
## 8.1 SPI & PWM Controller

The SPI & PWM controller serves as the microcontroller-to-analog chip interface to implement clock synchronous communication using four lines: a serial clock line (SCKA), serial data lines (SIA and SOA), and a slave select input line (SSA) and is also used to control the half-bridge output using the PWM input (PWMI).

[Data transmission and reception]

- Data size in 8-bit units
- MSB first

**Figure 8-1. Configuration Example of SPI & PWM Controller**



## 8.2 SPI Communication

Data is transmitted and received in 8-bit units. When SSA is low, data transmission and reception are enabled. Data is transmitted one bit at one time at the rising edge of a serial clock pulse and is received one bit at one time at the falling edge of a serial clock pulse. When the R/W bit is 1, the parity is checked for the R/W bit and the received address data (A4 to A0) using the even parity bit (P bit). If a parity error is detected, the PE bit in the system status register (SS) is set and writing the next byte is halted. If a parity error is not detected, data is written to the SPI control register after detection of the SSA rising edge, and appropriate operation is executed according to the written data. When the R/W bit is 0, the parity is not checked.

In the sleep mode (MSLP = low), operation is halted.

**Figure 8-2. SPI Communication Timing for 16-Bit Register Access**

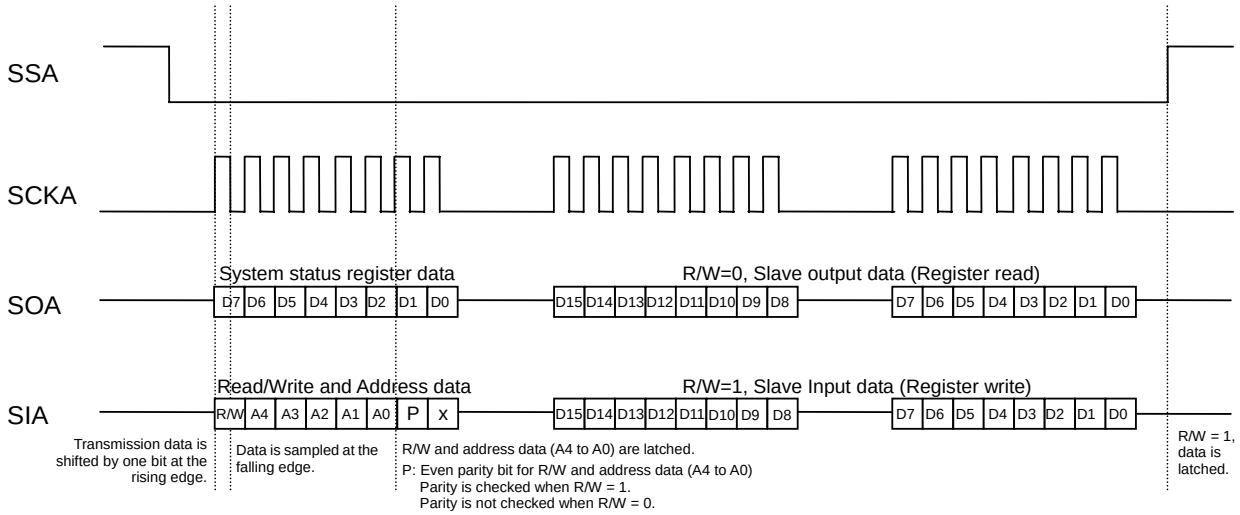


**Figure 8-3. SPI Communication Timing for 8-Bit Register Access**

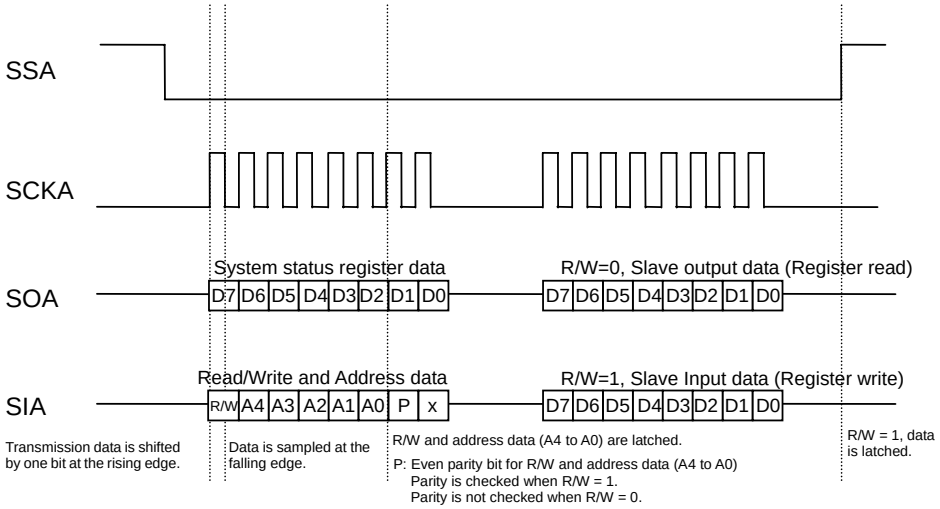



**Figure 8-4. Data Format Example 1 (R/W = 1, Address data = 01110B, Write data = 9990H)**

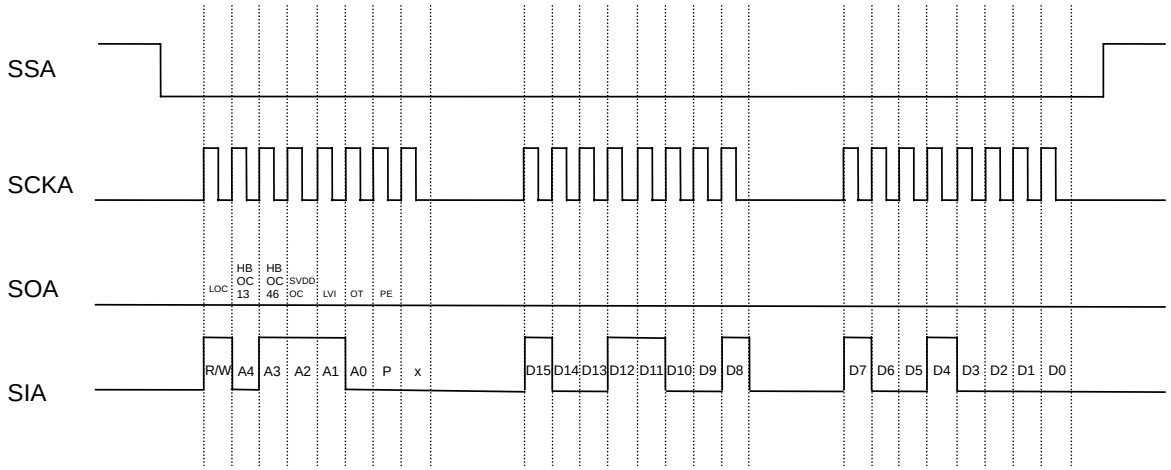
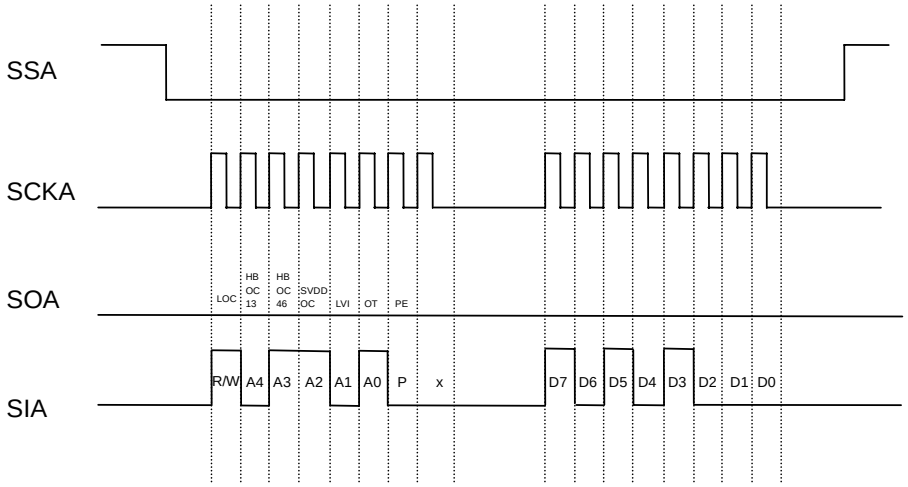



**Figure 8-5. Data Format Example 2 (R/W = 1, Address data = 01101B, Write data = 10101000B)**



## 8.3 SPI Control Registers

The SPI & PWM controller controls the following six registers.

- Reset status register (RS)
- Half-bridge control register (HBC)
- PWM input control register (PICL)
- System status register (SS)
- Half-bridge status register (HBS)
- System control register (SC)

### (1) Reset status register (RS)

The reset status register (RS) indicates the status of a cancellation request for resetting the analog block through the power-on clear (POCA) circuit and the status of a request for resetting the analog block through the external reset pin (RESET_A).

This register is reset to 00H by a request for resetting the analog chip through the power-on clear (POCA) circuit.

**Address: 01111B After POC reset: 00H R/W[Notes 1, 2]**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RS | POC | EXR | 0 | 0 | 0 | 0 | 0 | 0 |

| POC | Cancellation request flag for resetting the analog block through the power-on clear (POCA) circuit |
|---|---|
| 0 | A cancellation request for resetting through POCA has not been generated. |
| 1 | A cancellation request for resetting through POCA has been generated. |
| Being an update-type flag, it is cleared by a reset request through POCA. | |

| EXR | Request flag for resetting the analog block through the external reset pin (RESET_A) |
|---|---|
| 0 | An external request for resetting through RESET_A has not been generated. |
| 1 | An external request for resetting through RESET_A has been generated. |
| Being an accumulate-type flag, it is not cleared until 0 is written to. | |

Notes 1. Bit 7 is a read-only bit.
2. Writing 1 to bit 6 is ignored.

### (2) Half-bridge control register (HBC)

The half-bridge control register (HBC) controls the output of the half-bridge drivers. When the OT bit in the system status register (SS) is 1, the write instruction to the half-bridge control register (HBC) is ignored and the register retains the value before being written to.

This register is reset to 0000H by generation of a reset signal, overheat detection by the thermal shutdown circuit, and low level signal input to the INH pin. The specific bits are cleared upon detection of the over current of the half-bridge drivers.[Note]

**Address: 01110B After reset: 0000H R/W**

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| HBC | HB 6H | HB 6L | HB 5H | HB 5L | HB 4H | HB 4L | HB 3H | HB 3L | HB 2H | HB 2L | HB 1H | HB 1L | 0 | 0 | 0 | 0 |

| HBnH | HBnL | Operation mode |
|---|---|---|
| 0 | 0 | High-side MOSFET and low-side MOSFET are turned off. |
| 0 | 1 | High-side MOSFET is turned off and low-side MOSFET is turned on. |
| 1 | 0 | High-side MOSFET is turned on and low-side MOSFET is turned off. |
| 1 | 1 | Setting prohibited |

Note Depends on the HBOCS bit setting in the system control register (SC).

Caution When both HBnH and HBnL receive data which value changes to 1, HBnH and HBnL retain the values before being written to.

Remark n: Channel number (1 to 6)

### (3) PWM input control register (PICL)

The PWM input control register (PICL) enables or disables PWM signal input to the low-side MOSFET of the half-bridge drivers from the PWM input pin (PWMI). When the OT bit in the system status register (SS) is 1, the write instruction to the PWM input control register (PICL) is ignored and the register retains the value before being written to.

This register is reset to 00H by generation of a reset signal, overheat detection by the thermal shutdown circuit, and low level signal input to the INH pin. The specific bits are cleared upon detection of the over current of the half-bridge drivers.[Note]

**Address: 01101B After reset: 00H R/W**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PICL | PI6L | PI5L | PI4L | PI3L | PI2L | PI1L | 0 | 0 |

| PInL | Operation mode |
|---|---|
| 0 | PWM input is disabled. |
| 1 | PWM input is enabled. |

Note Depends on the HBOCS bit setting in the system control register (SC).

Remark n: Channel number (1 to 6)

### (4) System status register (SS)

The system status register (SS) indicates the status of the over current in the external sensor power supply output function, LIN transceiver, half-bridge drivers; the status of the regulator output voltage (5 V (typ.)); the status of the overheat of the analog chip; and the status of parity error detection.

This register is reset to 00H by generation of a reset signal.

**Address: 01100B After reset: 00H R/W**[Notes 1, 2]

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| SS | LOC | HBOC13 | HBOC46 | SVDDOC | LVI | OT | PE | 0 |

| LOC | Over current flag in LIN transceiver |
|---|---|
| 0 | The LIN driver is not in the over current state. |
| 1 | Over current has been generated in the LIN driver. |
| Being an accumulate-type flag, it is not cleared until 0 is written to. | |

| HBOC13 | Over current flag in half-bridge driver channels 1 to 3 |
|---|---|
| 0 | None of the half-bridge driver channels 1 to 3 are in the over current state. |
| 1 | Over current has been generated in any of the half-bridge driver channels 1 to 3. |
| Being an update-type flag, it is cleared when HB1OC, HB2OC, and HB3OC are all 0.<br>The OR is taken between the HB1OC, HB2OC, and HB3OC bits in the HBS register. | |

| HBOC46 | Over current flag in half-bridge driver channels 4 to 6 |
|---|---|
| 0 | None of the half-bridge driver channels 4 to 6 are in the over current state. |
| 1 | Over current has been generated in any of the half-bridge driver channels 4 to 6. |
| Being an update-type flag, it is cleared when HB4OC, HB5OC, and HB6OC are all 0.<br>The OR is taken between the HB4OC, HB5OC, and HB6OC bits in the HBS register | |

| SVDDOC | Over current flag in external sensor power supply output |
|---|---|
| 0 | The external sensor power supply output is not in the over current state. |
| 1 | Over current has been generated in the external sensor power supply output. |
| Being an accumulate-type flag, it is not cleared until 0 is written to. | |

| LVI | Low voltage flag of regulator output |
|---|---|
| 0 | The regulator output voltage is equal to or larger than the low-voltage detection value (4.2 V (typ.). |
| 1 | The regulator output voltage is smaller than the low-voltage detection value (4.2 V (typ.). |
| Being an update-type flag, it is automatically cleared when the regulator output voltage rises to the detection voltage (4.2 V (typ.)) or larger. | |

Notes 1. Bits 6, 5, and 3 are read-only bits.
2. Writing 1 to bits 7, 4, 2, and 1 is ignored.

Remark The description is continued on the following page.

| OT | Analog chip overheat flag |
|---|---|
| 0 | The overheat detection circuit has not detected the temperature equal to or higher than the overheat detection temperature (150°C (min.)). |
| 1 | The overheat detection circuit has detected the temperature higher than the overheat detection temperature (150°C (min.)). |
| Being an accumulate-type flag, it is not cleared until 0 is written to. | |

| PE | Parity error detection flag |
|---|---|
| 0 | No parity error has been detected. |
| 1 | A parity error has been detected. |
| Being an accumulate-type flag, it is not cleared until 0 is written to.<br>When the R/W bit is 1, this bit is set to 1 when the incorrect parity bit (P) is received. | |

### (5) Half-bridge status register (HBS)

The half-bridge status register (HBS) indicates the over current status of the half-bridge drivers. Since the flag bits in this register are accumulate-type flags, they are not cleared until 0 is written to.

This register is reset to 00H by generation of a reset signal.

**Address: 01011B After reset: 00H R/W** [Note]

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| HBS | HB6OC | HB5OC | HB4OC | HB3OC | HB2OC | HB1OC | 0 | 0 |

| HBnOC | Over current flag in half-bridge driver channels |
|---|---|
| 0 | Not in the over current state. |
| 1 | Over current has been generated. |

Note Writing 1 to bits 7 to 2 is ignored.

Remark n:Channel number (1 to 6)

### (6) System control register (SC)

The system control register (SC) enables or disables output from the external sensor power supply; enables or disables the half-bridge function; and selects the half-bridge driver channels to be protected against over current generated.

This register is reset to 00H by generation of a reset signal.

**Address: 01010B After reset: 00H R/W**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| SC | HBON | SVDDON | HBOCS | 0 | 0 | 0 | 0 | 0 |

| HBON | Half-bridge driver operation mode |
|---|---|
| 0 | Disabled |
| 1 | Enabled |

| SVDDON | External sensor power supply output mode |
|---|---|
| 0 | Off |
| 1 | On |

| HBOCS | Half-bridge driver channels to be protected against over current |
|---|---|
| 0 | When over current occurs in any of half-bridge driver channels 1 to 6, outputs from three channels including the pertinent channel are turned off.<br>• When over current occurs in any of half-bridge driver channels 1 to 3, outputs from channels 1 to 3 are turned off.<br>• When over current occurs in any of half-bridge driver channels 4 to 6, outputs from channels 4 to 6 are turned off |
| 1 | When over current occurs in any of half-bridge driver channels 1 to 6, outputs from all the channels are turned off. |

# 9. Protection Functions

The analog chip in the µPD78F807x incorporates the following protection circuits.

- Thermal shutdown circuit
- Over current limiter

Table 9-1 shows the conditions under which the above protection circuits are activated and deactivated.

**Table 9-1. Conditions of Activating and Deactivating Protection Circuits**

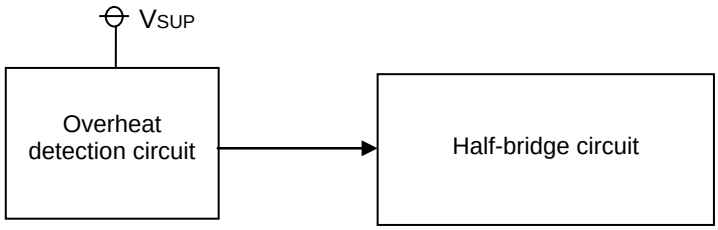
| Function Block | | Protection Circuit | Activating Conditions | Deactivating Conditions |
|---|---|---|---|---|
| Power supply circuit | Regulator output | Over current limiter | Over current occurs in the regulator output. | Over current disappears from the regulator output. |
| | External sensor power supply output | Over current limiter | Over current occurs in the external sensor power supply output. | The SVDDON bit is reset. |
| LIN transceiver | | Over current limiter | Over current occurs in the LIN transceiver | A high level signal is input to the TxL pin. |
| Half-bridge circuit | | Over current limiter | Over current occurs in HBO1 to HBO6. | The HBC register is reset. |
| Thermal shutdown circuit | | Thermal shutdown circuit | A temperature equal to or higher than the overheat detection temperature (150°C min.) is detected. | The OT bit is cleared. |

## 9.1 Thermal Shutdown Circuit Operation

The thermal shutdown circuit prevents the device from destruction and deterioration caused by overheat. When the overheat detection circuit in the analog chip detects the temperature equal to or higher than the overheat detection temperature (150°C min.), the OT bit in the system status register (SS) is set, and the half-bridge control register (HBC) and PWM input control register (PICL) are cleared simultaneously to forcibly turn off the outputs from all the half-bridge drivers in the half-bridge circuit. Clearing the OT bit in the system status register (SS) enables the half-bridge control register (HBC) and PWM input control register (PICL) to control the outputs again.

Caution: The thermal shutdown circuit incorporated in the analog chip is intended to protect the device in the abnormal situation; use this function only when it is absolutely necessary.

**Figure 9-1. Block Diagram of Thermal Shutdown Circuit**



## 9.2 Over Current Limiter Operation

### 9.2.1 Power Supply Circuit

The power supply circuit incorporates over current limiters separately for regulator output and external sensor power supply output. For details, refer to chapter 5 Power Supply Circuit.

### 9.2.2 LIN Transceiver

The LIN transceiver incorporates an over current limiter. For details, refer to chapter 6 LIN Transceiver.

### 9.2.3 Half-Bridge Circuit

The half-bridge circuit incorporates over current limiters. For details, refer to chapter 7 Half-Bridge Circuit.

# 10. Analog Reset Function

The analog chip provides the analog reset function.

Either of the following two methods can be used to generate an analog reset.

**(1) External reset through the RESET_A pin**

**(2) Internal reset according to the comparison result between the power supply voltage and detected voltage of the analog power-on clear (POCA) circuit**

External reset and internal reset are functionally identical; they both initialize the SPI control registers when a reset is generated.

When a low level signal is input to the RESET_A pin or a specific voltage is detected by the POCA circuit, a reset is generated. Tables 10-1 and 10-2 show the reset state of the analog function blocks and interconnected analog function pins in the package. Table 10-3 shows the state of the SPI control registers after reset acceptance.

When a low level signal is input to the RESET_A pin thus generating a reset, and a high level signal is input to the RESET_A pin again, a reset is released and the appropriate operation mode is entered according to the input voltage level to the MSLP, MOD1, and MOD2 pins. Reset through the POCA circuit is released when VDD ≥ VPOCA after a reset and the appropriate operation mode is entered according to the input voltage level to the MSLP, MOD1, and MOD2 pins.

The analog reset source can be monitored using the reset status register (RS).

Caution 1. To generate an external reset, input the low level signal to the RESET_A pin at least 10 µs.

**Table 10–1. Operation State of Analog Function Blocks during Analog Reset**

| Function Block | | State during Reset |
|---|---|---|
| Power supply circuit | Regulator output | Output |
| | External sensor power supply output | Operation stopped |
| | Low voltage detector | Operation stopped |
| | Over current limiter[Note] | Operation stopped |
| LIN transceiver | | Operation enabled |
| Half bridge circuit | | Operation stopped (Hi-Z) |
| | Over current limiter | Operation stopped |
| <R> SPI & PWM controller | | Operation stopped |
| Analog power on clear (POCA) circuit | | Operation enabled |
| Thermal shutdown function | | Operation stopped |

Note Applicable only when the internal P-ch MOS is used for a 5-V output dropper.

**Table 10–2. State of Analog Block Function Pins Interconnected in Package**

| Function Pin | State during Reset |
|---|---|
| SCKA | Pull-down input |
| SIA | Pull-down input |
| SOA | Hi-Z |
| SSA | Pull-up input |
| PWMI | Pull-down input |
| <R> RxL | Output |
| TxL | Pull-up input |
| INH | Pull-up input |

**Table 10–3. State of SPI Control Registers after Reset Acceptance**

| SPI Control register | State after Reset Acceptance |
|---|---|
| Reset status register (RS) | 00H |
| Half-bridge control register (HBC) | 0000H |
| PWM input control register (PICL) | 00H |
| System status register (SS) | 00H |
| Half-bridge status register (HBS) | 00H |
| System control register (SC) | 00H |

# 11. Electrical Specifications ((A) Grade Products)

## 11.1 Absolute Maximum Ratings

<R> **Absolute Maximum Ratings for Microcontroller Block ($T_A$ = 25°C)**

| Parameter | Symbol | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | | -0.5 to +6.5 | V |
| | $V_{SS}$ | | | -0.5 to +0.3 | V |
| | $AV_{REF}$ | | | -0.5 to $V_{DD}$+0.3[Note] | V |
| | $AV_{SS}$ | | | -0.5 to +0.3 | V |
| Input voltage | $V_{I1}$ | P00, P01, P10 to P17, P20 to P24, P30 to P33, P70, P120 to P122, X1, X2, $\overline{\text{RESET}}$, FLMD0 | | -0.3 to $V_{DD}$+0.3 | V |
| | $V_{I2}$ | P60, P61 (N-ch open drain) | | -0.3 to +6.5 | V |
| REGC pin input voltage | $V_{IREGC}$ | | | -0.5 to +3.6 and -0.5 to $V_{DD}$ | V |
| Output voltage | $V_O$ | | | -0.3 to $V_{DD}$+0.3[Note] | V |
| Analog input voltage | $V_{AN}$ | ANI0 to ANI4 | | -0.3 to $AV_{REF}$+0.3[Note] and 0.3 to $V_{DD}$+0.3[Note] | V |
| Output current, high | $I_{OH1}$ | Per pin | P00, P01, P10 to P17, P30 to P33, P70, P120, P130 | -10 | mA |
| | | Total of all pins -80 mA | P00, P01, P120, P130 | -25 | mA |
| | | | P10 to P17, P30 to P33, P70 | -55 | |
| | $I_{OH2}$ | Per pin | P20 to P24 | -0.5 | mA |
| | | Total of all pins | | -2 | |
| | $I_{OH3}$ | Per pin | P121, P122 | -1 | mA |
| | | Total of all pins | | -2 | |
| Output current, low | $I_{OL1}$ | Per pin | P00, P01, P10 to P17, P30 to P33, P60, P61, P70, P120, P130 | 30 | mA |
| | | Total of all pins 200 mA | P00, P01, P120, P130 | 60 | mA |
| | | | P10 to P17, P30 to P33, P60, P61, P70 | 140 | |
| | $I_{OL2}$ | Per pin | P20 to P24 | 1 | mA |
| | | Total of all pins | | 5 | |
| | $I_{OL3}$ | Per pin | P121, P122 | 4 | mA |
| | | Total of all pins | | 8 | |

Note Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of multi-function pins are the same as those of port pins.

**Absolute Maximum Ratings for Analog Block ($T_A$ = 25°C)**

| | Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|---|
| | Supply voltage | $V_{SUP1}$ | SUP, SUP1 to SUP6 | -0.3 to +40 Note 3 | V |
| <R> | Input voltage | $V_{IA1}$ | LIN | -0.3 to +40 Note 3 | V |
| | | $V_{IA2}$ | VRS | -0.3 to +6.5 | V |
| | | $V_{IA3}$ | MOD1, MOD2, MSLP, SRC, TxL, SCKA, SIA, SSA, PWMI, RESET_A | -0.3 to VRS+0.3 Note1 | V |
| | LIN negative input voltage | $V_{ILlin}$ | LIN, 7 V≤$V_{SUP}$≤19 V, 1 s | $V_{SUP}$-40 | V |
| | Output voltage | $V_{OA1}$ | LIN, HBO1 to HBO6 | -0.3 to +40 Note 3 | V |
| | | $V_{OA2}$ | VRO, SVDD | -0.3 to +6.5 | V |
| <R> | | $V_{OA3}$ | RxL, SOA | -0.3 to VRS+0.3 Note1 | V |
| | Output current | $I_{RO1}$ | VRO | Self limit Note2 | mA |
| | | $I_{SVDDO}$ | SVDD | Self limit Note2 | mA |
| | | $I_{LIN}$ | LIN | Self limit Note2 | mA |
| | | $I_{HBO}$ | HBO1 to HBO6 | Self limit Note2 | mA |
| | | $I_{RX}$ | RxL | -10 to +10 | mA |
| | | $I_{SOA}$ | SOA | -10 to +10 | mA |

Notes 1. Must be 6.5 V or lower.

2. The over current limiter is activated when the current exceeds the self limit.

<R> 3. When the input voltage is 25 V or higher, the overcurrent protection circuits for the LIN transceiver and half-bridge circuit operate.

**Absolute Maximum Ratings for Common Item**

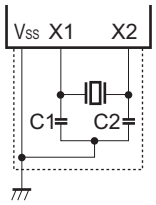
| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Operation ambient temperature | $T_A$ | | -40 to +85 | °C |
| Storage temperature | $T_{stg}$ | | -65 to +150 | °C |
| Junction temperature | $T_{jmax}$ | | 150 | °C |

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

## 11.2 Microcontroller Block Electrical Characteristics

**X1 Oscillator Characteristics**

($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Resonator | Recommended Circuit | Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Ceramic resonator, crystal resonator |  | X1 clock oscillation frequency ($f_X$)Note1 | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1.0Note2 | | 20.0 | MHz |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | 1.0 | | 5.0 | |

Notes 1. Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.
2. It is 2.0 MHz (MIN.) when programming on the board via UART6.

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as $V_{SS}$.
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

2. Since the CPU is started by the internal high-speed oscillation clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

**Internal Oscillator Characteristics**

($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Resonator | Parameter | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| 8 MHz internal oscillator | Internal high-speed oscillation clock frequency ($f_{RH}$)Note | RSTS = 1 | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 7.6 | 8.0 | 8.4 | MHz |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | 7.6 | 8.0 | 10.4 | MHz |
| | | RSTS = 0 | | 2.48 | 5.6 | 9.86 | MHz |
| 240 kHz internal oscillator | Internal low-speed oscillation clock frequency ($f_{RL}$) | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 216 | 240 | 264 | kHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | 192 | 240 | 264 | kHz |

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Remark 1. RSTS: Bit 7 of the internal oscillation mode register (RCM)

2. For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

**DC Characteristics (1/5)**

($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $AV_{REF}$ ≤ $V_{DD}$, $V_{SS}$ = $AV_{SS}$ = 0 V)

| <R> Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, high Note 1 | $I_{OH1}$ | Per pin for P00, P01, P10 to P17, P30 to P33, P70, P120, P130 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | -3.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | -2.5 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | -1.0 | mA |
| | | Total Note 2 of P00, P01, P120, P130 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | -12.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | -7.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | -4.0 | mA |
| | | Total Note 2 of P10 to P17, P30 to P33, P70 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | -18.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | -15.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | -10.0 | mA |
| | | Total Note 2 of all pins | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | -23.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | -20.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | -14.0 | mA |
| | $I_{OH2}$ | Per pin for P20 to P24 | $AV_{REF}$ = $V_{DD}$ | | | -0.1 | mA |
| | | Per pin for P121, P122 | | | | -0.1 | mA |
| Output current, low Note 3 | $I_{OL1}$ | Per pin for P00, P01, P10 to P17, P30 to P33, P70, P120, P130 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 8.5 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 5.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 2.0 | mA |
| | | Per pin for P60, P61 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 15.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 5.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 2.0 | mA |
| | | Total Note 2 of P00, P01, P120, P130 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 20.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 15.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 8.0 | mA |
| | | Total Note 2 of P10 to P17, P30 to P33, P60, P61, P70 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 45.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 35.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 20.0 | mA |
| | | Total Note 2 of all pins | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 65.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 50.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 28.0 | mA |
| | $I_{OL2}$ | Per pin for P20 to P24 | $AV_{REF}$ = $V_{DD}$ | | | 0.4 | mA |
| | | Per pin for P121, P122 | | | | 0.4 | mA |

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from $V_{DD}$ to an output pin.

2. Specification under conditions where the duty factor is 70% (time for which current is output is 0.7 × t and time for which current is not output is 0.3 × t, where t is a specific time). The total output current of the pins at a duty factor of other than 70% can be calculated by the following expression.

- Where the duty factor of $I_{OH}$ is n%: Total output current of pins = ($I_{OH}$ × 0.7)/(n × 0.01)

<R> <Example> Where the duty factor is 50%, $I_{OH}$ = -20.0 mA

Total output current of pins = (-20.0 × 0.7)/(50 × 0.01) = -28.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

3. Value of current at which the device operation is guaranteed even if the current flows from an output pin to GND.

Remark Unless specified otherwise, the characteristics of multi-function pins are the same as those of port pins.

**DC Characteristics (2/5)**

($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $AV_{REF}$ ≤ $V_{DD}$, $V_{SS}$ = $AV_{SS}$ = 0 V)

<R>

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high Note 1 | $V_{IH1}$ | P12, P13, P15, P121, P122 | | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | P00, P01, P10, P11, P14, P16, P17, P30 to P33, P70, P120, RESET, EXCLK | | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH3}$ | P20 to P24 | $AV_{REF}$ = $V_{DD}$ | 0.7$AV_{REF}$ | | $AV_{REF}$ | V |
| | $V_{IH4}$ | P60, P61 | | 0.7$V_{DD}$ | | 6.0 | V |
| Input voltage, high Note 2 | $V_{IH1}$ | P12, P13, P15, P121, P122 | | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | P00, P01, P10, P11, P14, P16, P17, P30 to P33, P70, P120, RESET, EXCLK | | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH3}$ | P20 to P24 | $AV_{REF}$ = $V_{DD}$ | 0.7$AV_{REF}$ | | $AV_{REF}$ | V |
| | $V_{IH4}$ | P60, P61 | | 0.7$V_{DD}$ | | 6.0 | V |
| Input voltage, low Note 1 | $V_{IL1}$ | P12, P13, P15, P60, P61, P121, P122 | | 0 | | 0.3$V_{DD}$ | V |
| | $V_{IL2}$ | P00, P01, P10, P11, P14, P16, P17, P30 to P33, P70, P120, RESET, EXCLK | | 0 | | 0.2$V_{DD}$ | V |
| | $V_{IL3}$ | P20 to P24 | $AV_{REF}$ = $V_{DD}$ | 0 | | 0.3$AV_{REF}$ | V |
| Input voltage, low Note 2 | $V_{IL1}$ | P12, P13, P15, P60, P61, P121, P122 | | 0 | | 0.3$V_{DD}$ | V |
| | $V_{IL2}$ | P00, P01, P10, P11, P14, P16, P17, P30 to P33, P70, P120, RESET, EXCLK | | 0 | | 0.2$V_{DD}$ | V |
| | $V_{IL3}$ | P20 to P24 | $AV_{REF}$ = $V_{DD}$ | 0 | | 0.3$AV_{REF}$ | V |
| Output voltage, high | $V_{OH1}$ | P00, P01, P10 to P17, P30 to P33, P70, P120, P130 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH1}$ = -3.0 mA | $V_{DD}$ - 0.7 | | | V |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, $I_{OH1}$ = -2.5 mA | $V_{DD}$ - 0.5 | | | V |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V, $I_{OH1}$ = -1.0 mA | $V_{DD}$ - 0.5 | | | V |
| | $V_{OH2}$ | P20 to P24 | $AV_{REF}$ = $V_{DD}$, $I_{OH2}$ = -100 μA | $V_{DD}$ - 0.5 | | | V |
| | | P121, P122 | $I_{OH2}$ = -100 μA | $V_{DD}$ - 0.5 | | | V |

Notes 1. Applies to the products with a 48-Kbyte or larger flash memory.
2. Applies to the products with a 32-Kbyte or smaller flash memory.

Remark Unless specified otherwise, the characteristics of multi-function pins are the same as those of port pins.

**DC Characteristics (3/5)**

($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $AV_{REF}$ ≤ $V_{DD}$, $V_{SS}$ = $AV_{SS}$ = 0 V)

<R>

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Output voltage, low | $V_{OL1}$ | P00, P01, P10 to P17, P30 to P33, P70, P120, P130 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL1}$ = 8.5 mA | | | | 0.7 | V |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, $I_{OL1}$ = 5.0 mA | | | | 0.7 | V |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V, $I_{OL1}$ = 2.0 mA | | | | 0.5 | V |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V, $I_{OL1}$ = 1.0 mA | | | | 0.5 | V |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V, $I_{OL1}$ = 0.5 mA | | | | 0.4 | V |
| | $V_{OL2}$ | P20 to P24 | $AV_{REF}$ = $V_{DD}$, $I_{OL2}$ = 0.4 mA | | | | 0.4 | V |
| | | P121, P122 | $I_{OL2}$ = 0.4 mA | | | | 0.4 | V |
| | $V_{OL3}$ | P60, P61 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL3}$ = 15.0 mA | | | | 2.0 | V |
| | | | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL3}$ = 5.0 mA | | | | 0.4 | V |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, $I_{OL1}$ = 5.0 mA | | | | 0.6 | V |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V, $I_{OL1}$ = 3.0 mA | | | | 0.4 | V |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V, $I_{OL1}$ = 2.0 mA | | | | 0.4 | V |
| Input leakage current, high | $I_{LIH1}$ | P00, P01, P10 to P17, P30 to P33, P60, P61, P70, P120, FLMD0, RESET | $V_I$ = $V_{DD}$ | | | | 1 | μA |
| | $I_{LIH2}$ | P20 to P24 | $V_I$ = $AV_{REF}$, $AV_{REF}$ = $V_{DD}$ | | | | 1 | μA |
| | $I_{LIH3}$ | P121, P122 (X1, X2) | $V_I$ = $V_{DD}$ | I/O port mode | | | 1 | μA |
| | | | | OSC mode | | | 20 | μA |
| Input leakage current, low | $I_{LIL1}$ | P00, P01, P10 to P17, P30 to P33, P60, P61, P70, P120, FLMD0, RESET | $V_I$ = $V_{SS}$ | | | | -1 | μA |
| | $I_{LIL2}$ | P20 to P24 | $V_I$ = $V_{SS}$, $AV_{REF}$ = $V_{DD}$ | | | | -1 | μA |
| | $I_{LIL3}$ | P121, P122 (X1, X2) | $V_I$ = $V_{SS}$ | I/O port mode | | | -1 | μA |
| | | | | OSC mode | | | -20 | μA |
| Pull up resistor | $R_U$ | $V_I$ = $V_{SS}$ | | | 10 | 20 | 100 | kΩ |
| FLMD0 supply voltage | $V_{IL}$ | In normal operation mode | | | 0 | | 0.2 $V_{DD}$ | V |
| | $V_{IH}$ | In self-programming mode | | | 0.8 $V_{DD}$ | | $V_{DD}$ | V |

Remark Unless specified otherwise, the characteristics of multi-function pins are the same as those of port pins.

**DC Characteristics (4/5)**

($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $AV_{REF}$ ≤ $V_{DD}$, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operation mode | $f_{XH}$ = 20 MHz Note 2 | $V_{DD}$ = 5.0 V | Square wave input | | 3.2 | 5.5 | mA |
| | | | | | Resonator connection | | 4.5 | 6.9 | |
| | | | | $V_{DD}$ = 3.0 V | Square wave input | | 3.2 | 5.5 | |
| | | | | | Resonator connection | | 4.2 | 6.6 | |
| | | | $f_{XH}$ = 10 MHz Notes 2, 3 | $V_{DD}$ = 5.0 V | Square wave input | | 1.6 | 2.8 | mA |
| | | | | | Resonator connection | | 2.3 | 3.9 | |
| | | | | $V_{DD}$ = 3.0 V | Square wave input | | 1.5 | 2.7 | |
| | | | | | Resonator connection | | 2.2 | 3.2 | |
| | | | $f_{XH}$ = 5 MHz Notes 2, 3 | $V_{DD}$ = 3.0 V | Square wave input | | 0.9 | 1.6 | mA |
| | | | | | Resonator connection | | 1.3 | 2.0 | |
| | | | | $V_{DD}$ = 2.0 V | Square wave input | | 0.7 | 1.4 | mA |
| | | | | | Resonator connection | | 1.0 | 1.6 | |
| | | | $f_{RH}$ = 8 MHz, $V_{DD}$ = 5.0 V Note 4 | | | | 1.4 | 2.5 | mA |
| | $I_{DD2}$ | HALT mode | $f_{XH}$ = 20 MHz Note 2, $V_{DD}$ = 5.0 V | | Square wave input | | 0.8 | 2.6 | mA |
| | | | | | Resonator connection | | 2.0 | 4.4 | |
| | | | $f_{XH}$ = 10 MHz Notes 2, 3, $V_{DD}$ = 5.0 V | | Square wave input | | 0.4 | 1.3 | mA |
| | | | | | Resonator connection | | 1.0 | 2.4 | |
| | | | $f_{XH}$ = 5 MHz Notes 2, 3, $V_{DD}$ = 3.0 V | | Square wave input | | 0.2 | 0.65 | mA |
| | | | | | Resonator connection | | 0.5 | 1.1 | |
| | | | $f_{RH}$ = 8 MHz, $V_{DD}$ = 5.0 V Note 4 | | | | 0.4 | 1.2 | mA |
| | $I_{DD3}$ | STOP mode Note 5 | | | | | 1 | 20 | μA |
| | | | $T_A$ = -40 to +70 °C | | | | 1 | 10 | μA |

Notes
1. Total current flowing into the internal power supply ($V_{DD}$), including the peripheral operation current. Port output current and current flowing through on-chip pull-up resistor are not included. Input leakage current with input pin fixed to $V_{DD}$ or $V_{SS}$ is included.
2. Operational current of the 8-MHz internal oscillator and 240-kHz internal oscillator, the current flowing through the A/D converter, watchdog timer, and LVI are not included.
3. When AMPH (bit 0 of clock operation mode select register (OSCCTL)) = 0.
4. Operational current of the X1 oscillator and 240-kHz internal oscillator, the current flowing through the A/D converter, watchdog timer, and LVI are not included.

5. Operational current of the 240-kHz internal oscillator, the current flowing through the A/D converter, watchdog timer, and LVI are not included.

Remarks 1. $f_{XH}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. $f_{RH}$: Internal high-speed oscillation clock frequency

**DC Characteristics (5/5)**

($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $AV_{REF}$ ≤ $V_{DD}$, $V_{SS}$ = $AV_{SS}$ = 0 V)

| | Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| <R> | A/D converter operating current | $I_{ADC}$ Note 1 | 2.3 V ≤ $AV_{REF}$ ≤ $V_{DD}$, ADCS = 1 | | 0.86 | 1.9 | mA |
| | Watchdog timer operating current | $I_{WDT}$ Note 2 | During 240 kHz internal low speed oscillation clock operation | | 5 | 10 | μA |
| | LVI operating current | $I_{LVI}$ Note 3 | | | 9 | 18 | μA |

Notes 1. Current ($AV_{REF}$) flowing only to the A/D converter. The current value of the microcontroller block is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

<R> 2. Current flowing only to the watchdog timer (including the operating current of the 240 kHz internal oscillator). The current value of the microcontroller block is the sum of $I_{DD2}$ or $I_{DD3}$ and $I_{WDT}$ when the watchdog timer operates.

<R> 3. Current flowing only to the LVI circuit. The current value of the microcontroller block is the sum of $I_{DD2}$ or $I_{DD3}$ and $I_{LVI}$ when the LVI circuit operates.

## AC Characteristics

### (1) Basic operation (1/2)

($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $AV_{REF}$ ≤ $V_{DD}$, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Instruction cycle (minimum instruction execution time) | $T_{CY}$ | Main system clock ($f_{XP}$) operation | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.1 | | 32 | μs |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | 0.4 Note 1 | | 32 | μs |
| <R> Peripheral hardware clock frequency | $f_{PRS}$ | $f_{PRS}$ = $f_{XH}$ (XSEL = 1) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 20 | MHz |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V Note 2 | | | 20 | MHz |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 5 | MHz |
| | | $f_{PRS}$ = $f_{RH}$ (XSEL = 0) | 2.7 V ≤ $V_{DD}$ < 5.5 V | 7.6 | | 8.4 | MHz |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V Note 3 | 7.6 | | 10.4 | MHz |
| External main system clock frequency | $f_{EXCLK}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 1.0 Note 4 | | 20.0 | MHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | 1.0 | | 5.0 | MHz |
| External main system clock input high-level width, low-level width | $t_{EXCLKH}$, $t_{EXCLKL}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 24 | | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | 96 | | | ns |
| TI000, TI010 input high-level width, low-level width | $t_{TIH0}$, $t_{TIL0}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | $2/f_{sam}$ +0.1 Note 5 | | | μs |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | $2/f_{sam}$ +0.2 Note 5 | | | μs |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | $2/f_{sam}$ +0.5 Note 5 | | | μs |
| TI50, TI51 input frequency | $f_{TI5}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | | 10 | MHz |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | | 10 | MHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | | 5 | MHz |

Notes 1. 0.38 μs when operating with the 8 MHz internal oscillator.

2. Applies to the main system clock frequency characteristics. The frequency of the division clock for peripheral functions should be $f_{XH}$/2 (10 MHz) or smaller. However, multiplier/divider can be operated at $f_{XH}$ (20 MHz).

3. Applies to the main system clock frequency characteristics. The frequency of the division clock for peripheral functions should be $f_{RH}$/2 or smaller.

4. It is 2.0 MHz (MIN.) when programming on the board via UART6.

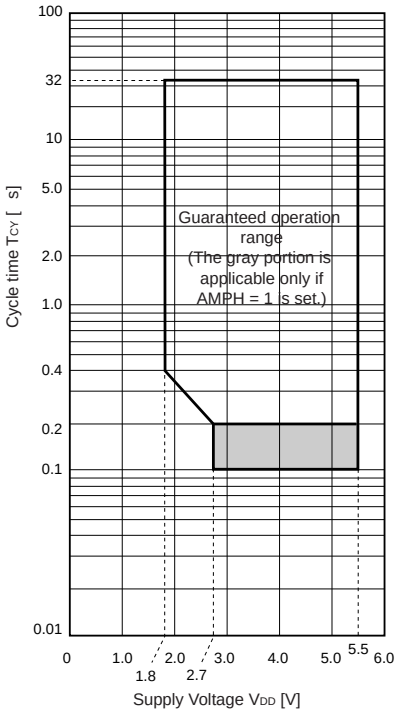
5. Selection of $f_{sam}$ = $f_{PRS}$, $f_{PRS}$/4, or $f_{PRS}$/256 is possible using bits 0 and 1 (PRM000, PRM001) of prescaler mode register 00 (PRM00). Note that when selecting the TI000 valid edge as the count clock, $f_{Sam}$ = $f_{PRS}$.

**(1) Basic operation (2/2)**

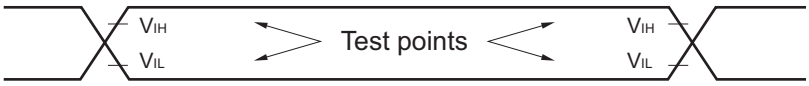
($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $AV_{REF}$ ≤ $V_{DD}$, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| TI50, TI51 input high-level width, low-level width | $t_{TIH5}$, $t_{TIL5}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 50 | | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V | 50 | | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | 100 | | | ns |
| Interrupt input high-level width, low-level width | $t_{INTH}$, $t_{INTL}$ | | 1 | | | μs |
| Key interrupt input low-level width | $t_{KR}$ | | 250 | | | ns |
| $\overline{\text{RESET}}$ low-level width | $t_{RSL}$ | | 10 | | | μs |

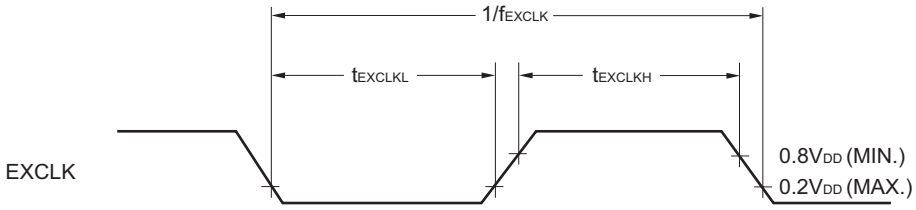
**TCY vs $V_{DD}$ (Main System Clock Operation)**



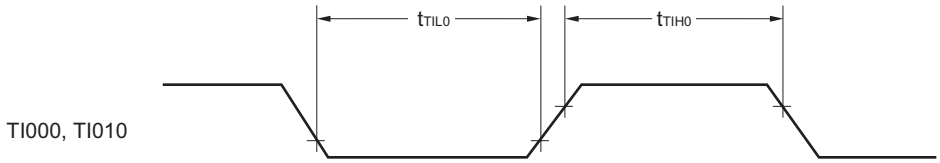
### AC Timing Test Points

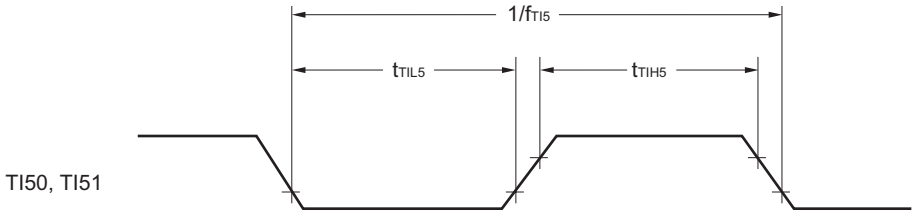



### External Main System Clock Timing

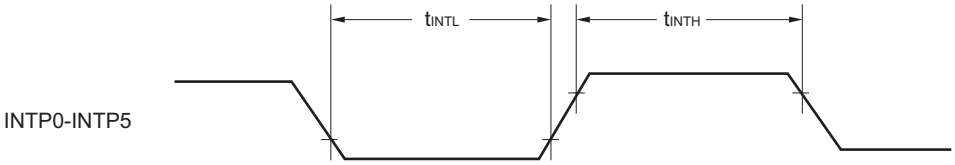



### TI Timing

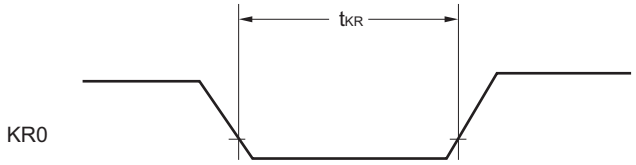


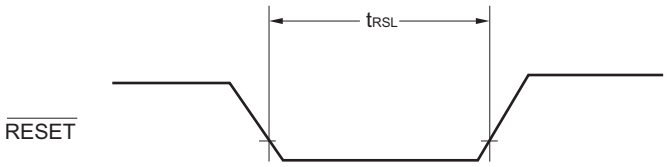

### Interrupt Request Input Timing



**Key Interrupt Input Timing**




**$\overline{\text{RESET}}$ Input Timing**




**(2) Serial interface**

($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $AV_{REF}$ ≤ $V_{DD}$, $V_{SS}$ = $AV_{SS}$ = 0 V)

**(a) UART6 (dedicated baud rate generator output)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | | | | 625 | kbps |

**(b) UART0 (dedicated baud rate generator output)**

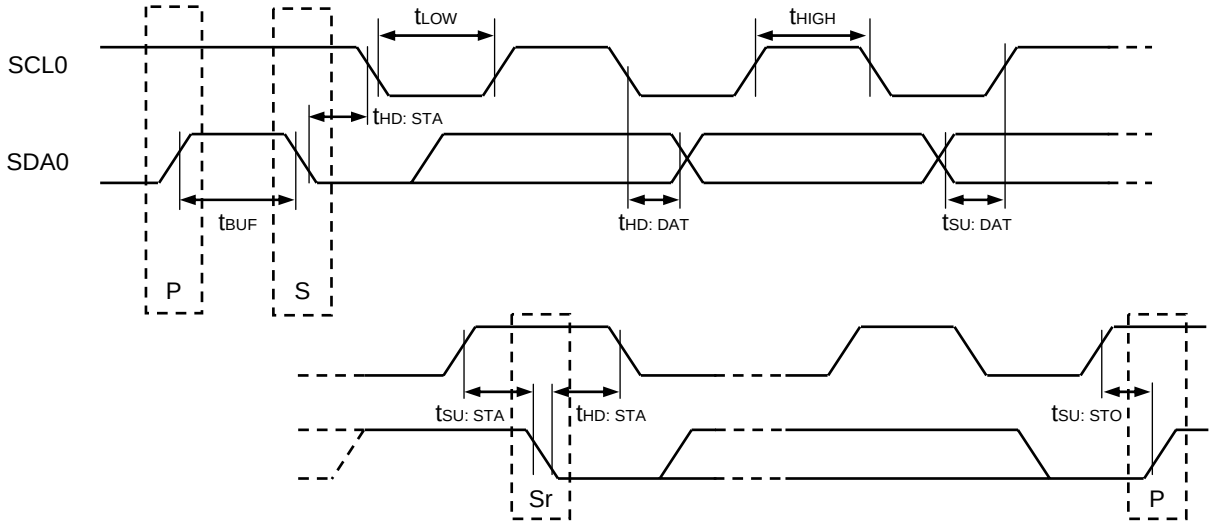
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | | | | 625 | kbps |

**(c) IIC0**

| Parameter | Symbol | Conditions | Standard Mode | | High Speed Mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MIN. | MAX. | MAX. | |
| SCL0 clock frequency | $f_{CLK}$ | | 0 | 100 | 0 | 400 | kHz |
| Restart condition setup time | $t_{SU:STA}$ | | 4.7 | | 0.6 | | μs |
| Hold time Note 1 | $t_{HD:STA}$ | | 4.0 | | 0.6 | | μs |
| Hold time when SCL0 = low | $t_{LOW}$ | Internal clock operation | 4.7 | | 1.3 | | μs |
| Hold time when SCL0 = high | $t_{HIGH}$ | | 4.0 | | 0.6 | | μs |
| Data setup time (reception) | $t_{SU:DAT}$ | | 250 | | 100 | | ns |
| Data hold time (transmission) Note 2 | $t_{HD:DAT}$ | When $f_W = f_{XH}/2^N$ is selected Note 3 or when $f_W = f_{EXSCL0}$ is selected Note 3 | 0 | 3.45 | 0 | 0.9 Note 4 | μs |
| | | | | | | 1.00 Note 5 | μs |
| | | When $f_W = f_{RH}/2^N$ is selected Note 3 | 0 | 3.45 | 0 | 1.05 | μs |
| Stop condition setup time | $t_{SU:STO}$ | | 4.0 | | 0.6 | | μs |
| Bus free time | $t_{HD:BUF}$ | | 4.7 | | 1.3 | | μs |

Notes
1. The first clock pulse is generated after this period when the start/restart condition is detected.
2. The maximum value (MAX.) of $t_{HD:DAT}$ is normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.
3. $f_W$ indicates the IIC0 transfer clock selected by the IICCL0 and IICX0 registers.
4. When $f_W \geq 4.4$ MHz is selected
5. When $f_W < 4.4$ MHz is selected

**IIC0 Transfer Timing**




P: Stop condition
S: Start condition
Sr: Restart condition

**(d) CSI10 (master mode, $\overline{SCK10}$... internal clock output)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $\overline{SCK10}$ cycle time | $t_{KCY1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 200 | | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V | 400 | | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | 600 | | | ns |
| $\overline{SCK10}$ high/low level width | $t_{KH1}$, $t_{KL1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | $t_{KCY1}$/2 - 20 Note 1 | | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V | $t_{KCY1}$/2 - 30 Note 1 | | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | $t_{KCY1}$/2 - 60 Note 1 | | | ns |
| SI10 setup time (to $\overline{SCK10}$↑) | $t_{SIK1}$ | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | 70 | | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.0 V | 100 | | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | 190 | | | ns |
| SI10 hold time (from $\overline{SCK10}$↑) | $t_{KSI1}$ | | 30 | | | ns |
| Delay time from $\overline{SCK10}$↓ to SO10 output | $t_{KSO1}$ | C = 50 pF Note 2 | | | 40 | ns |

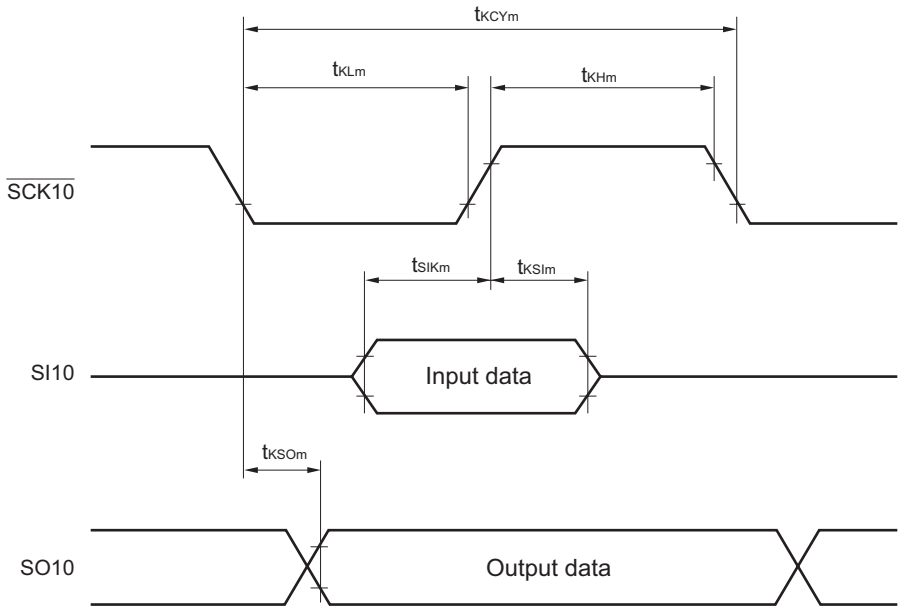
Notes 1. This value is when high-speed system clock ($f_{XH}$) is used.
2. C is the load capacitance of the $\overline{SCK10}$ and SO10 output lines.

**(e) CSI10 (slave mode, $\overline{SCK10}$... external clock input)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK10}$ cycle time | $t_{KCY2}$ | | | 400 | | | ns |
| $\overline{SCK10}$ high-/low-level width | $t_{KH2}$, $t_{KL2}$ | | | $t_{KCY2}$/2 | | | ns |
| SI10 setup time (to $\overline{SCK10}$↑) | $t_{SIK2}$ | | | 80 | | | ns |
| SI10 hold time (from $\overline{SCK10}$↑) | $t_{KSI2}$ | | | 50 | | | ns |
| Delay time from $\overline{SCK10}$↓ to SO10 output | $t_{KSO2}$ | C = 50 pF[Note] | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 120 | ns |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 120 | ns |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 180 | ns |

Note C is the load capacitance of the SO1n output line.

**CSI10 Transfer Timing**




Remark m = 1, 2

### A/D Converter Characteristics

($T_A$ = -0 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, 2.3 V ≤ $AV_{REF}$ ≤ $V_{DD}$, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Resolution | RES | | | | 10 | bit |
| Overall error Notes 1, 2 | AINL | 4.0 V ≤ $AV_{REF}$ ≤ 5.5 V | | | ±0.4 | %FSR |
| | | 2.7 V ≤ $AV_{REF}$ < 4.0 V | | | ±0.6 | %FSR |
| | | 2.3 V ≤ $AV_{REF}$ < 2.7 V | | | ±1.2 | %FSR |
| Conversion time | tCONV | 4.0 V ≤ $AV_{REF}$ ≤ 5.5 V | 6.1 | | 66.6 | μs |
| | | 2.7 V ≤ $AV_{REF}$ < 4.0 V | 12.2 | | 66.6 | μs |
| | | 2.3 V ≤ $AV_{REF}$ < 2.7 V | 27 | | 66.6 | μs |
| Zero-scale error Notes 1, 2 | EZS | 4.0 V ≤ $AV_{REF}$ ≤ 5.5 V | | | ±0.4 | %FSR |
| | | 2.7 V ≤ $AV_{REF}$ < 4.0 V | | | ±0.6 | %FSR |
| | | 2.3 V ≤ $AV_{REF}$ < 2.7 V | | | ±0.6 | %FSR |
| Full-scale error Notes 1, 2 | EFS | 4.0 V ≤ $AV_{REF}$ ≤ 5.5 V | | | ±0.4 | %FSR |
| | | 2.7 V ≤ $AV_{REF}$ < 4.0 V | | | ±0.6 | %FSR |
| | | 2.3 V ≤ $AV_{REF}$ < 2.7 V | | | ±0.6 | %FSR |
| Integral linearity error Note 1 | ILE | 4.0 V ≤ $AV_{REF}$ ≤ 5.5 V | | | ±2.5 | LSB |
| | | 2.7 V ≤ $AV_{REF}$ < 4.0 V | | | ±4.5 | LSB |
| | | 2.3 V ≤ $AV_{REF}$ < 2.7 V | | | ±6.5 | LSB |
| Differential linearity error Note 1 | DLE | 4.0 V ≤ $AV_{REF}$ ≤ 5.5 V | | | ±1.5 | LSB |
| | | 2.7 V ≤ $AV_{REF}$ < 4.0 V | | | ±2.0 | LSB |
| | | 2.3 V ≤ $AV_{REF}$ < 2.7 V | | | ±2.0 | LSB |
| Analog input voltage | VAIN | | $AV_{SS}$ | | $AV_{REF}$ | V |

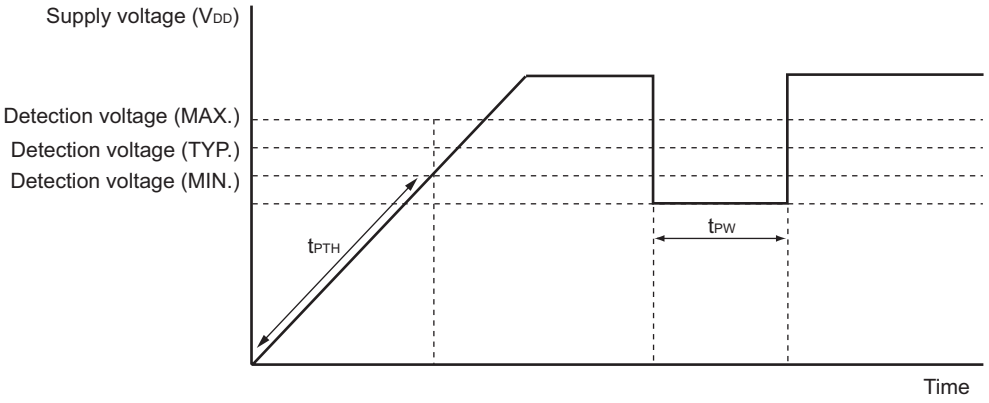
Notes 1. Excludes quantization error (±1/2 LSB).
2. This value is indicated as a ratio (%FSR) to the full-scale value.

### 1.59 V POC Circuit Characteristics

($T_A$ = -40 to +85°C, $V_{SS}$ = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection voltage | VPOC | | 1.44 | 1.59 | 1.74 | V |
| Power voltage rise inclination | tPTH | $V_{DD}$: 0 V → change inclination of $V_{POC}$ | 0.5 | | | V/ms |
| Minimum pulse width | tPW | | 200 | | | μs |

### POC Circuit Timing



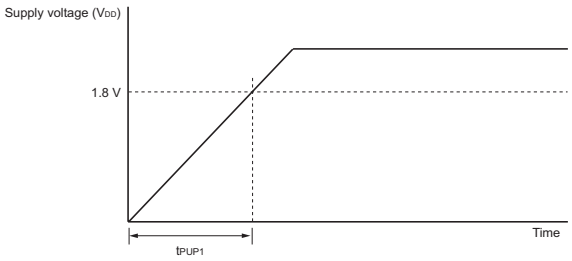

### Supply Voltage Rise Time

(TA = -40 to +85°C, VSS = 0 V)

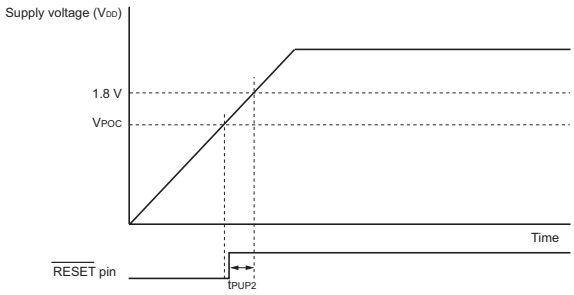
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Maximum time to rise to 1.8 V (VDD (MIN.)) (VDD: 0 V → 1.8 V) | tPUP1 | POCMODE (option byte) = 0, when $\overline{\text{RESET}}$ input is not used | | | 3.6 | ms |
| Maximum time to rise to 1.8 V (VDD (MIN.)) (releasing $\overline{\text{RESET}}$ input → VDD: 1.8 V) | tPUP2 | POCMODE (option byte) = 0, when $\overline{\text{RESET}}$ input is used | | | 1.9 | ms |

### Supply Voltage Rise Time Timing

**• When $\overline{\text{RESET}}$ pin input is not used**




**• When $\overline{\text{RESET}}$ pin input is used**



### 2.7 V POC Circuit Characteristics

($T_A$ = -40 to +85°C, $V_{SS}$ = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection voltage on application of supply voltage | $V_{DDPOC}$ | POCMODE (option bye) = 1 | 2.50 | 2.70 | 2.90 | V |

Remark The operations of the POC circuit are as described below, depending on the POCMODE (option byte) setting

| Option Byte Setting | POC Mode | Operation |
|---|---|---|
| POCMODE = 0 | 1.59 V mode operation | A reset state is maintained until $V_{POC}$ = 1.59 V (TYP.) is reached after the power is turned on, and the reset is released when $V_{POC}$ is exceeded. After that, POC detection is performed at $V_{POC}$, similarly to when the power was turned on. The power supply voltage must be raised at a time of $t_{PUP1}$ or $t_{PUP2}$ when POCMODE is 0. |
| POCMODE = 1 | 2.7 V/1.59 V mode operation | The reset state is maintained until $V_{DDPOC}$ = 2.7 V (TYP.) is reached after the power is turned on, and the reset is released when $V_{DDPOC}$ is exceeded. After that, POC detection is performed at $V_{POC}$ = 1.59 V (TYP.) and not at $V_{DDPOC}$.<br>The use of the 2.7 V/1.59 V POC mode is recommended when the voltage takes longer than $t_{PTH}$ to reach 1.8 V after the power is turned on. |

### LVI Circuit Characteristics

($T_A$ = -40 to +85°C, $V_{POC} \le V_{DD} \le 5.5$ V, $AV_{REF} \le V_{DD}$, $V_{SS}$ = 0 V)

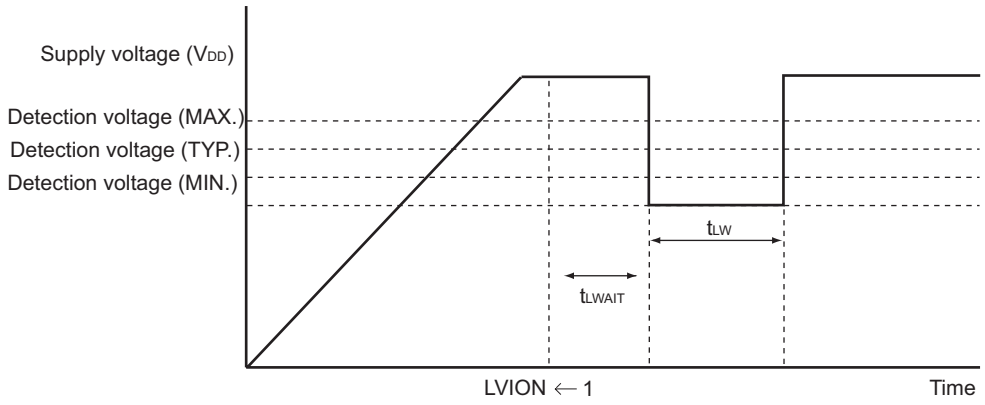
| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Detection voltage | Supply voltage level | $V_{LVI0}$ | | 4.14 | 4.24 | 4.34 | V |
| | | $V_{LVI1}$ | | 3.99 | 4.09 | 4.19 | V |
| | | $V_{LVI2}$ | | 3.83 | 3.93 | 4.03 | V |
| | | $V_{LVI3}$ | | 3.68 | 3.78 | 3.88 | V |
| | | $V_{LVI4}$ | | 3.52 | 3.62 | 3.72 | V |
| | | $V_{LVI5}$ | | 3.37 | 3.47 | 3.57 | V |
| | | $V_{LVI6}$ | | 3.22 | 3.32 | 3.42 | V |
| | | $V_{LVI7}$ | | 3.06 | 3.16 | 3.26 | V |
| | | $V_{LVI8}$ | | 2.91 | 3.01 | 3.11 | V |
| | | $V_{LVI9}$ | | 2.75 | 2.85 | 2.95 | V |
| | | $V_{LVI10}$ | | 2.60 | 2.70 | 2.80 | V |
| | | $V_{LVI11}$ | | 2.45 | 2.55 | 2.65 | V |
| | | $V_{LVI12}$ | | 2.29 | 2.39 | 2.49 | V |
| | | $V_{LVI13}$ | | 2.14 | 2.24 | 2.34 | V |
| | | $V_{LVI14}$ | | 1.98 | 2.08 | 2.18 | V |
| | | $V_{LVI15}$ | | 1.83 | 1.93 | 2.03 | V |
| | External input pin[Note 1] | EXLVI | EXLVI < $V_{DD}$, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 1.11 | 1.21 | 1.31 | V |
| Minimum pulse width | | $t_{LW}$ | | 200 | | | μs |
| Operation stabilization wait time[Note 2] | | $t_{LWAIT}$ | | 10 | | | μs |

Notes 1. The EXLVI/P120/INTP0 pin is used.

2. Time required from setting bit 7 (LVION) in the low-voltage detection register (LVIM) to 1 to operation stabilization

Remark $V_{LVI(n-1)} > V_{LVIn}$: n = 1 to 15

### LVI Circuit Timing

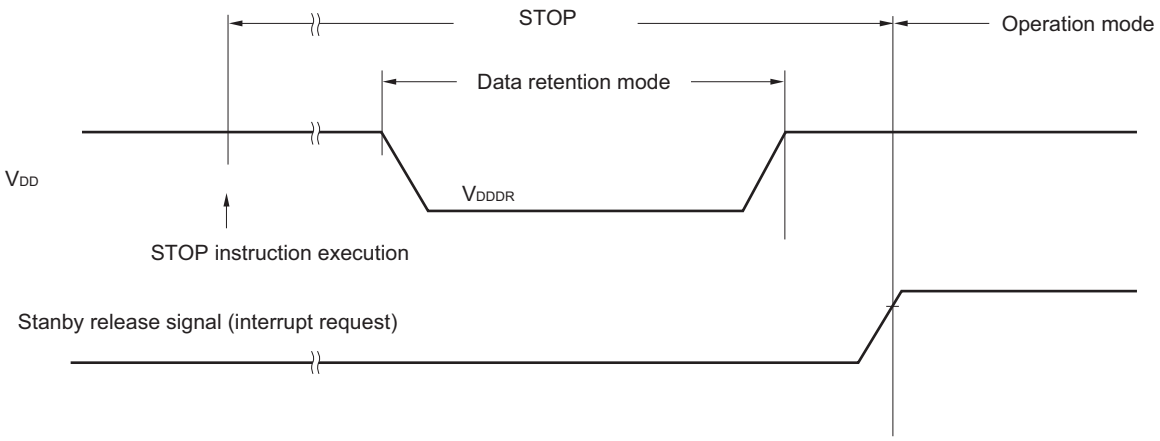


**Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics**

($T_A$ = -40 to +85°C)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.44 Note | | 5.5 | V |

Note The value depends on the POC detection voltage. When the voltage drops, the data is retained until a POC reset is applied, but data is not retained when a POC reset is applied.



### Flash Memory Programming Characteristics

**($T_A$ = -40 to +85°C, 2.7 V ≤ $V_{DD}$ ≤ 5.5 V, $AV_{REF}$ ≤ $V_{DD}$, $V_{SS}$ = $AV_{SS}$ = 0 V)**

**Basic characteristics**

| Parameter | | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DD}$ supply current | | $I_{DD}$ | $f_{XP}$ = 10 MHz (TYP.), 20 MHz (MAX.) | | | | 4.5 | 11.0 | mA |
| Erase time Notes 1, 2 | All blocks | $T_{eraca}$ | | | | | 20 | 200 | ms |
| | Block unit | $T_{erasa}$ | | | | | 20 | 200 | ms |
| Write time (in 8 bit units) Note 1 | | $T_{wrwa}$ | | | | | 10 | 100 | μs |
| Number of rewrites per chip | | $C_{erwr}$ | 1 erase + 1 write after erase = 1 rewrite Note 3 | • When a flash memory programmer is used, and the libraries Note 4 provided by Renesas Electronics are used<br>• For program update | 15 years | 1000 | | | Times |
| | | | | • When the EEPROM emulation libraries Note 5 provided by Renesas Electronics are used<br>• The rewritable ROM size: 4 KB<br>• For data update | 5 years | 10000 | | | Times |
| | | | | Conditions other than the above Note 6 | 10 years | 100 | | | Times |

Notes 1. Characteristic of the flash memory. For the characteristic when a dedicated flash programmer, PG-FP5, is used and the rewrite time during self programming, see 78K0/Kx2 User's Manual (R01UH0008E).
2. The prewrite time before erasure and the erase verify time (writeback time) are not included.
3. When a product is first written after shipment, "erase ? write" and "write only" are both taken as one rewrite.
4. The sample library specified by the 78K0/Kx2 Flash Memory Self Programming User's Manual (U17516E) is excluded.
5. The sample program specified by the 78K0/Kx2 EEPROM Emulation Application Note (U17517E) is excluded.
6. These include when the sample library specified by the 78K0/Kx2 Flash Memory Self Programming User's Manual (U17516E) and the sample program specified by the 78K0/Kx2 EEPROM Emulation Application Note (U17517E) are used.

Remarks 1. $f_{XP}$: Main system clock oscillation frequency
2. For serial write operation characteristics, refer to 78K0/Kx2 Flash Memory Programming (Programmer) Application Note (U17739E).

## 11.3 Analog Block Characteristics

**Power supply circuit characteristics**

(Unless specified otherwise, $T_A$ = -40 to +85°C, 6 V ≤ $V_{SUP}$ ≤ 19 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Output voltage | $V_{CCOUT1}$ | 7 V ≤ $V_{SUP}$ ≤ 19 V<br>$V_{CCOUT}$ = VRO = VRS,<br>$I_{RO}$ = 1 mA to 50 mA | 4.85 | 5 | 5.15 | V |
| | $V_{CCOUT2}$ | 6 V ≤ $V_{SUP}$ ≤ 19 V<br>$V_{CCOUT}$ = VRO = VRS,<br>$I_{RO}$ = 1 mA to 25 mA | 4.85 | 5 | 5.15 | V |
| | $V_{CCOUT3}$ | 19 V < $V_{SUP}$ ≤ 40 V<br>$V_{CCOUT}$ = VRO = VRS,<br>$I_{RO}$ = 1 mA | 4.5 | 5 | 5.5 | V |
| | $V_{CCOUT4}$ | 7 V ≤ $V_{SUP}$ ≤ 19 V, $V_{ccout}$ = VRS<br>External NPN transistor used<br>$I_C$ = 1 mA to 150 mA | 4.85 | 5 | 5.15 | V |
| | $V_{CCOUT5}$ | 19 V ≤ $V_{SUP}$ ≤ 40 V, $V_{ccout}$ = VRS<br>External NPN transistor used<br>$I_C$ = 1 mA | 4.5 | 5 | 5.5 | V |
| | $V_{SVDD1}$ | 6 ≤ $V_{SUP}$ ≤ 19 V<br>$I_{SVDD}$ = 20 mA | VRS-0.3 | | | V |
| | $V_{SVDD2}$ | 7 V ≤ $V_{SUP}$ ≤ 19 V<br>External NPN transistor used<br>$I_{SVDD}$ = 20 mA | VRS-0.3 | | | V |
| <R> | $V_{SVDD3}$ | 6 ≤ $V_{SUP}$ ≤ 19 V<br>SVDD = OFF | | | TBD | V |
| <R> Over current detection current | $I_{ROlim1}$ | 7 V ≤ $V_{SUP}$ ≤ 19 V, VRO | 51 | | 300 | mA |
| <R> | $I_{ROlim2}$ | 6 V ≤ $V_{SUP}$ < 7 V, VRO | 26 | | 300 | mA |
| | $I_{SVDDlim1}$ | 6 V ≤ $V_{SUP}$ ≤ 19 V, SVDD | 21 | 35 | 50 | mA |
| | $I_{SVDDlim2}$ | 7 V ≤ $V_{SUP}$ ≤ 19 V, SVDD<br>External NPN transistor used | 21 | 35 | 50 | mA |
| Short circuit current | $I_{short}$ | | | TBD | | mA |
| Load regulation | $REG_{L1}$ | 1 mA < $I_{RO}$ ≤ 50 mA, $V_{SUP}$ = 14 V | | | 60 | mV |
| | $REG_{L2}$ | 1 mA < $I_C$ ≤ 150 mA, $V_{SUP}$ = 14 V<br>External NPN transistor used | | | 80 | mV |
| Input regulation | $REG_{IN1}$ | 7 V ≤ $V_{SUP}$ ≤ 19 V, $I_{RO}$ = 50 mA | | | 60 | mV |
| | | 6 V ≤ $V_{SUP}$ ≤ 19 V, $I_{RO}$ = 25 mA | | | 60 | mV |
| | $REG_{IN2}$ | 7 V ≤ $V_{SUP}$ ≤ 19 V, $I_C$ = 150 mA<br>External NPN transistor used | | | 60 | mV |

**Supply Current Characteristics**

(Unless specified otherwise, $T_A$ = -40 to +85°C, 6 V ≤ $V_{SUP}$ ≤ 19 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Supply current | $I_{SUP1}$ Notes 1, 2 | $I_{SUP1}$ = $I_{SUP}$, LIN: Sleep, $T_A$ = 25°C, $V_{SUP}$ = 14 V | | 30 | 50 | μA |
| | $I_{SUP2}$ Notes 1, 2 | $I_{SUP2}$ = $I_{SUP}$, LIN: Sleep | | TBD | TBD | μA |
| | $I_{SUP3}$ Notes 1, 2 | $I_{SUP3}$ = $I_{SUP}$, LIN: Normal (LIN bus: Recessive) | | TBD | 3 | mA |

Notes 1. This is the total current flowing to the SUP, SUP1 to SUP6, and VRO internal power supply. However, the current flowing through the port pull-up resistor is not included.

2. $V_{DD}$ current is not included.

For VDD current ($I_{DD}$), refer to the DC characteristics description in chapter 31 Electrical Specifications ((A) Grade Products), of the 78K0/Kx2 User's Manual (R01UH0008E).

### LIN Transceiver Circuit Characteristics

### DC Characteristics

(Unless specified otherwise, $T_A$ = -40 to +85°C, 6 V ≤ $V_{SUP}$ ≤ 19 V)

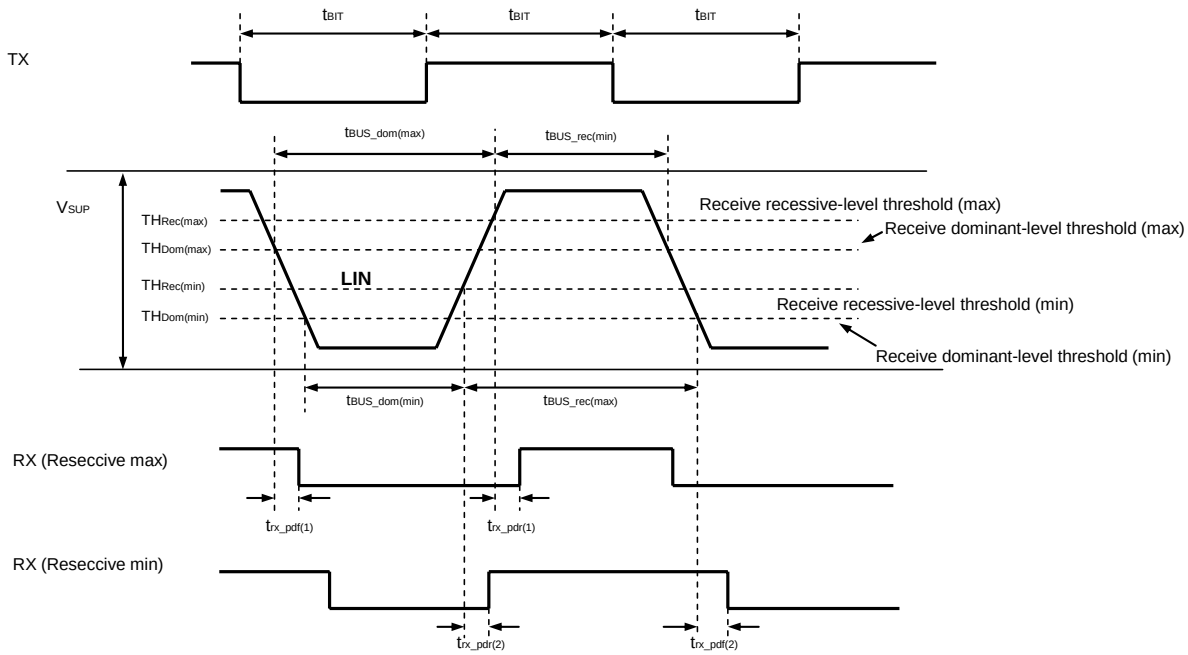
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| LIN Bus dominant leak current | $I_{BUS\_PAS\_dom}$ | $V_{BUS}$ = 0 V, $V_{SUP}$ = 12 V | -1 | | | mA |
| LIN Bus recessive leak current | $I_{BUS\_PAS\_rec}$ | $V_{BUS} \geq V_{SUP}$ | | | 20 | μA |
| LIN Bus current 1 | $I_{BUS\_NO\_GND}$ | 0 V < $V_{BUS}$ < 18 V, $V_{SUP}$ = 12 V | -1 | | 1 | mA |
| LIN Bus current 2 | $I_{BUS}$ | $V_{SUP\_Device}$ = GND, 0 V < $V_{BUS}$ < 18 V | | 1 | 10 | μA |
| Receive dominant-level input voltage | $V_{BUSdom}$ | | | | 0.4 $V_{SUP}$ | V |
| Receive recessive-level Input voltage | $V_{BUSrec}$ | | 0.6 $V_{SUP}$ | | | V |
| Receive center level threshold | $V_{BUS\_CNT}$ | ($V_{th\_dom}$+$V_{th\_rec}$)/2 | 0.475 $V_{SUP}$ | 0.5 $V_{SUP}$ | 0.525 $V_{SUP}$ | V |
| Receive hysteresis | $V_{HYS}$ | | | | 0.175 $V_{SUP}$ | V |
| LIN dominant-level output voltage 1 | $V_{BUSdom\_DRV\_LoSUP}$ | $V_{SUP}$ = 7.3 V, $I_{lin}$ = 15 mA | | | 1.2 | V |
| LIN dominant-level output voltage 2 | $V_{BUSdom\_DRV\_HiSUP}$ | $V_{SUP}$ = 18 V, $I_{lin}$ = 36 mA | | | 2 | V |
| LIN serial diode drop voltage | $V_{SerDiode}$ | $V_{TXD}$ = $V_{RO}$ | 0.4 | 0.7 | 1.0 | V |
| LIN pull-up resistance | $R_{slave}$ | | 20 | 30 | 60 | kΩ |
| MOD1, MOD 2 high level input voltage | $V_{mh}$ | | 0.7$V_{RS}$ | | | V |
| MOD1, MOD2 low level input voltage | $V_{ml}$ | | | | 0.3$V_{RS}$ | V |
| SRC high level input voltage | $V_{srh}$ | | 0.7$V_{RS}$ | | | V |
| SRC low level input voltage | $V_{srl}$ | | | | 0.3$V_{RS}$ | V |
| MSLP high level input voltage | $V_{SLPH}$ | | 0.7$V_{RS}$ | | | V |
| MSLP low level input voltage | $V_{SLPL}$ | | | | 0.3$V_{RS}$ | V |
| MSLP low level input voltage | $V_{SLPL}$ | | | | 0.3$V_{RS}$ | V |
| MSLP pull down resistance | $R_{MSLP}$ | | 50 | 100 | 220 | kΩ |
| LIN driver over current limitation | $I_{const}$ | LIN pin inflow current limit | 40 | 80 | 200 | mA |

**AC Characteristics**

(Unless specified otherwise, $T_A$ = -40 to +85°C, 6 V ≤ $V_{SUP}$ ≤ 19 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Duty_Cycle1<br>(see figure 12-1) | $D_1$ | Cbus; Rbus = 1 nF; 1 kΩ/6.8 nF; 660 Ω/ 10 nF; 500 Ω<br>$t_{BIT}$ = 50 μs<br>$TH_{Rec}$(max) = 0.744×$V_{SUP}$,<br>$TH_{Dom}$(max) = 0.581×$V_{SUP}$<br>$D_1 = t_{BUS\_rec(min)}/(2\times t_{BIT})$<br>7 V ≤ $V_{SUP}$ ≤ 18 V<br>SRC = High | 0.396 | | | - |
| Duty_Cycle2<br>(see figure 12-1) | $D_2$ | $C_{bus}$; $R_{bus}$ = 1 nF; 1 kΩ/6.8 nF; 660 Ω/ 10 nF; 500 Ω<br>$t_{BIT}$ = 50 μs<br>$TH_{Rec(min)}$ = 0.422×$V_{SUP}$,<br>$TH_{Dom(min)}$ = 0.284×$V_{SUP}$<br>$D_2 = t_{BUS\_rec(max)}/(2\times t_{BIT})$<br>7.6 V ≤ $V_{SUP}$ ≤ 18 V<br>SRC = High | | | 0.581 | - |
| Duty_Cycle3<br>(see figure 12-1) | $D_3$ | $C_{bus}$; $R_{bus}$ = 1 nF; 1 kΩ/6.8 nF; 660 Ω/ 10 nF; 500 Ω<br>$t_{BIT}$ = 96 μs<br>$TH_{Rec(max)}$ = 0.778×$V_{SUP}$,<br>$TH_{Dom(max)}$ = 0.616×$V_{SUP}$<br>$D_3 = t_{BUS\_rec(min)}/(2\times t_{BIT})$<br>7 V ≤ $V_{SUP}$ ≤ 18 V<br>SRC = Low | 0.417 | | | - |
| Duty_Cycle4<br>(see figure 12-1) | $D_4$ | $C_{bus}$; $R_{bus}$ = 1 nF; 1 kΩ/6.8 nF; 660 Ω/ 10 nF; 500 Ω<br>$t_{BIT}$ = 96 μs<br>$TH_{Rec(min)}$ = 0.389×$V_{SUP}$,<br>$TH_{Dom(min)}$ = 0.251×$V_{SUP}$<br>$D_3 = t_{BUS\_rec(max)}/(2\times t_{BIT})$<br>7.6 V ≤ $V_{SUP}$ ≤ 18 V<br>SRC = Low | | | 0.590 | - |
| Propagation delay | $t_{rx\_pd}$ | $t_{rx\_pdf(1)}$, $t_{rx\_pdf(2)}$, $t_{rx\_pdr(1)}$, $t_{rx\_pdr(2)}$ | | | 6 | μs |
| LIN rising and falling transmitter delay symmetry | $t_{rx\_sym}$ | $t_{rx\_sym} = t_{rx\_pdf(1)} - t_{rx\_pdr(1)}$,<br>$t_{rx\_sym} = t_{rx\_pdf(2)} - t_{rx\_pdr(2)}$ | -2 | | 2 | μs |

**Figure 11-1. Duty Cycle**



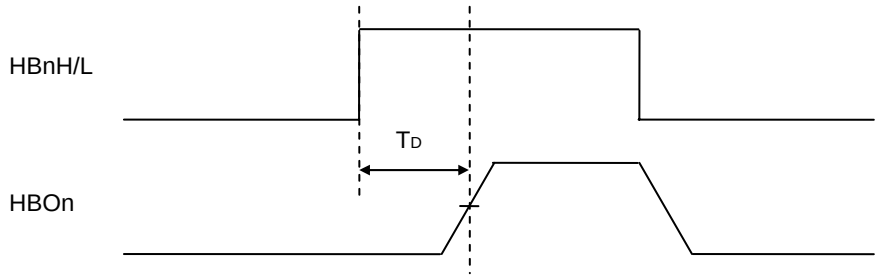
### Half-Bridge Driver Circuit Characteristics

(Unless specified otherwise, $T_A$ = -40 to +85°C, 6 V ≤ ($V_{SUP}$ = SUP = SUP1 to SUP6) ≤ 19 V)

| | Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| | On resistance | $HB_{n\_RONH}$ | $I_O$ = -1.2 A | TBD | TBD | 1.0 | Ω |
| | | $HB_{n\_RONL}$ | $I_O$ = 1.2 A | TBD | TBD | 1.0 | Ω |
| <R> | Over current detection value | $I_{HBOn\_limH}$ | | -2.7 | | -1.4 | A |
| <R> | | $I_{HBOn\_limL}$ | | 1.4 | | 2.7 | A |
| | Output off leak current | $I_{LHBOnH}$ | HBO1 to HBO6 | | | TBD | μA |
| <R> | | $I_{LHBOnL}$ | HBO1 to HBO6 | TBD | | | μA |
| | Switching delay time | $T_D$ | HBO1 to HBO6, High side, Low side | | TBD | | μs |
| <R> | Switching frequency | $f_{PWMIL}$ | Low side, HBO1 to HBO6 | | | TBD | kHz |

Remark n = 1 to 6

### Switching Delay Timing




Remarks 1. n = 1 to 6

2. HBnH/L: The high-side or low-side MOSFET control bits of the half-bridge driver

### SPI & PWM Controller Characteristics

<R> **DC Characteristics**

(Unless specified otherwise, $T_A$ = -40 to +85°C, 6 V ≤ $V_{SUP}$ ≤ 19 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| SCKA, SIA, SSA, PWMI high level input voltage | $V_{IH\_SPI}$ | SCKA, SIA, SSA, PWMI Port mode A | 0.7 VRS | | | V |
| SCKA, SIA, SSA, PWMI low level input voltage | $V_{IL\_SPI}$ | SCKA, SIA, SSA, PWMI Port mode A | | | 0.3 VRS | V |
| SCKA, SIA, SSA, PWMI high level input leak current | $I_{LIH\_SPI}$ | SCKA, SIA, SSA, PWMI, Port mode B | | | 1 | μA |
| SCKA, SIA, SSA, PWMI low level input leak current | $I_{LIL\_SPI}$ | SCKA, SIA, SSA, PWMI, Port mode B | -1 | | | μA |
| SOA high level output leak current | $I_{LOH\_SPI}$ | SOA, Port mode A | | | 1 | μA |
| SOA low level output leak current | $I_{LOL\_SPI}$ | SOA, Port mode A | -1 | | | μA |
| SSA pull up resistance | $R_{SSA}$ | SSA, Port mode A | 50 | 100 | 200 | kΩ |
| SCKA pull down resistance | $R_{SCKA}$ | SCK, Port mode A | 50 | 100 | 200 | kΩ |
| SIA pull down resistance | $R_{SIA}$ | SIA, Port mode A | 50 | 100 | 200 | kΩ |
| PWMI pull down resistance | $R_{PWMI}$ | PWMI, Port mode A | 50 | 100 | 200 | kΩ |

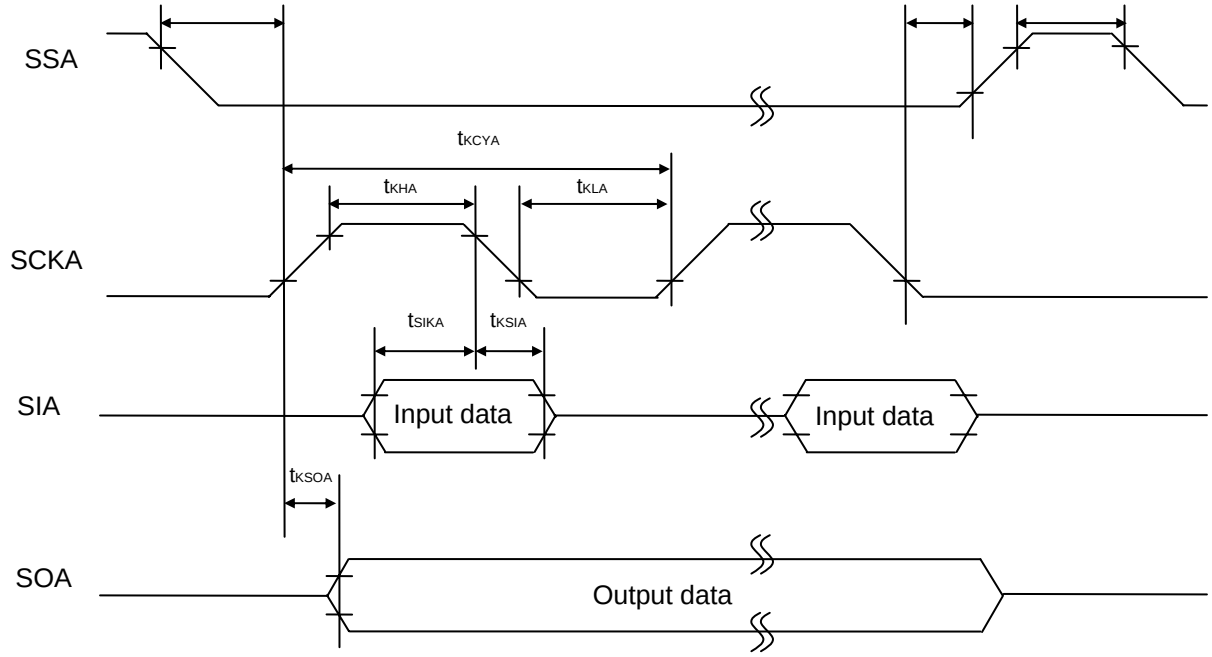
**AC Characteristics**

(Unless specified otherwise, $T_A$ = -40 to +85°C, 6 V ≤ $V_{SUP}$ ≤ 19 V)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| SCKA cycle time | $t_{KCYA}$ | | | 400 | | | ns |
| SCKA high-level width, low-level width | $t_{KHA}$, $t_{KLA}$ | | | $t_{KCYA}$/2 | | | ns |
| SIA setup time (to SCKA↑) | $t_{SIKA}$ | | | 80 | | | ns |
| SIA hold time (to SCKA↓) | $t_{KSIA}$ | | | 50 | | | ns |
| Delay time from SCKA↑ to SOA output | $t_{KSOA}$ | C = 50 pF[Note] | 4.0 V ≤ VRS ≤ 5.25 V | | | 120 | ns |
| | | | 2.7 V ≤ VRS < 4.0 V | | | 120 | ns |
| SSA high-level width | $t_{SHA}$ | | | TBD | | | ns |
| Delay time from SSA↓ to SCKA↑ | $t_{SKA}$ | | | TBD | | | ns |
| Delay time from SCKA↓ to SSA↑ | $t_{KSA}$ | | | TBD | | | ns |

Note C is the load capacitance of the SOA output line.

**SPI Transfer Clock Timing**

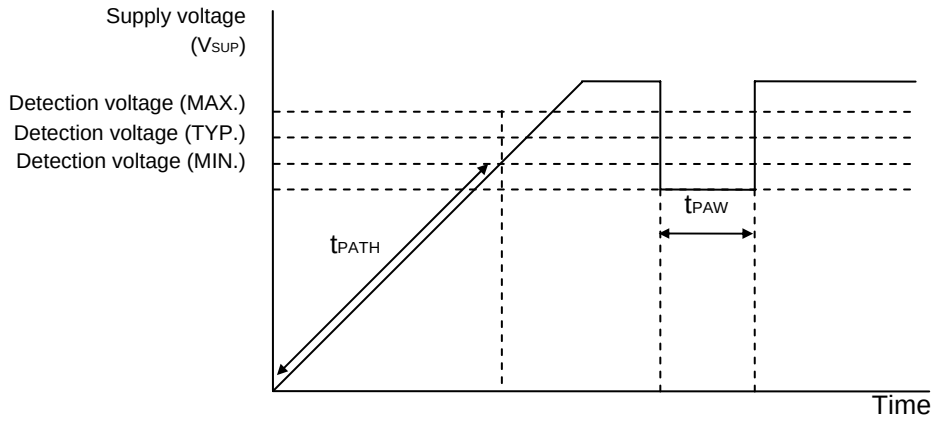



**POCA Circuit Characteristics**

(Unless specified otherwise, $T_A$ = -40 to +85°C, $V_{SS}$ = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection voltage | $V_{POCA}$ | | 2.7 | 3.0 | 3.3 | V |
| Power voltage rise inclination | $t_{PATH}$ | $V_{DD}$: 0 V → change inclination of $V_{POCA}$ | 0.5 | | | V/ms |
| Minimum pulse width | $t_{PAW}$ | | 200 | | | μs |

**POCA Circuit Timing**



<R> **Low Voltage Detection Circuit Characteristics**

(Unless specified otherwise, $T_A$ = -40 to +85°C, 6 V ≤ $V_{SUP}$ ≤ 19 V)

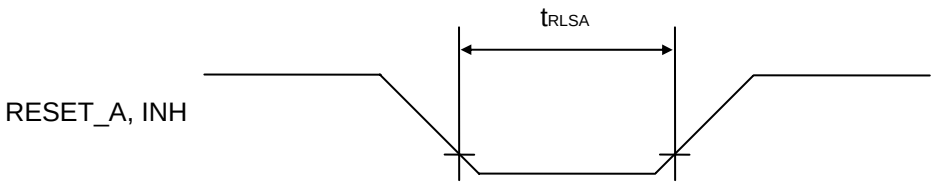
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Low voltage detection voltage | $V_{LVIA}$ | $V_{LVIA}$ = VRS | 4.0 | 4.2 | 4.4 | V |

**Reset Circuit Characteristics**

(Unless specified otherwise, $T_A$ = -40 to +85°C, 6 V ≤ $V_{SUP}$ ≤ 19 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| RESET_A, INH high-level input voltage | $V_{IHW1}$ | RESET_A, INH | 0.7 $V_{RS}$ | | | V |
| RESET_A, INH low-level input voltage | $V_{ILW1}$ | RESET_A, INH | 0 | | 0.3 $V_{RS}$ | V |
| RESET_A, INH minimum low-level width | $t_{RLSA}$ | RESET_A, INH | 10 | | | μs |
| RESET_A, INH high-level input leak current | $I_{LIHW1}$ | RESET_A, INH, $V_I$ = $V_{SUP}$ | | | 3 | μA |
| RESET_A, INH low-level input leak current | $I_{LILW1}$ | RESET_A, INH, $V_I$ = GND | -3 | | | μA |
| RESET_A, INH pull-up resistance | $R_{RESET\_A}$ | RESET_A, INH | 50 | 100 | 200 | kΩ |

**RESET_A, INH Input Timing**




**Overheat Detector Characteristics**

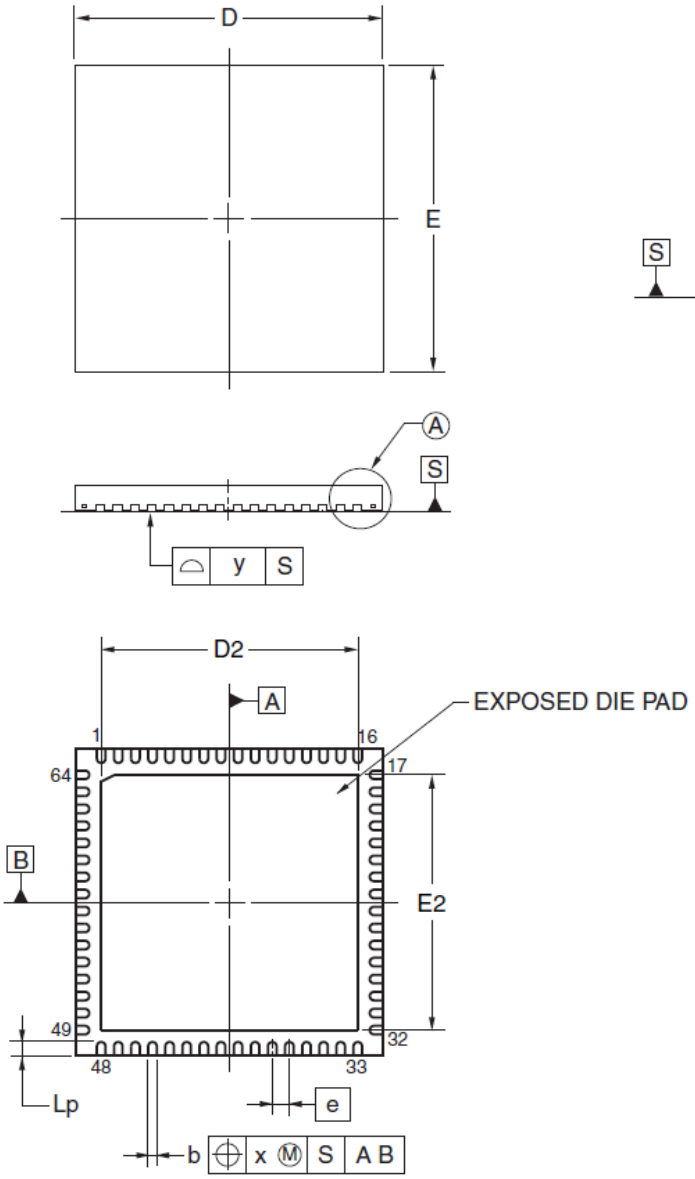
(Unless specified otherwise, $T_A$ = -40 to +85°C, 6 V ≤ $V_{SUP}$ ≤ 19 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Overheat detection temperature | VRth | | (150) | (170) | (200) | °C |

Remark The value in parenthesis is the design target value, and not confirmed by the shipping test.

# 12. Package Drawing

## 64-PIN PLASTIC WQFN(9x9)




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 9.00±0.05 |
| E | 9.00±0.05 |
| A | 0.75±0.05 |
| b | $0.25^{+0.05}_{-0.07}$ |
| e | 0.50 |
| Lp | 0.40±0.10 |
| x | 0.05 |
| y | 0.05 |

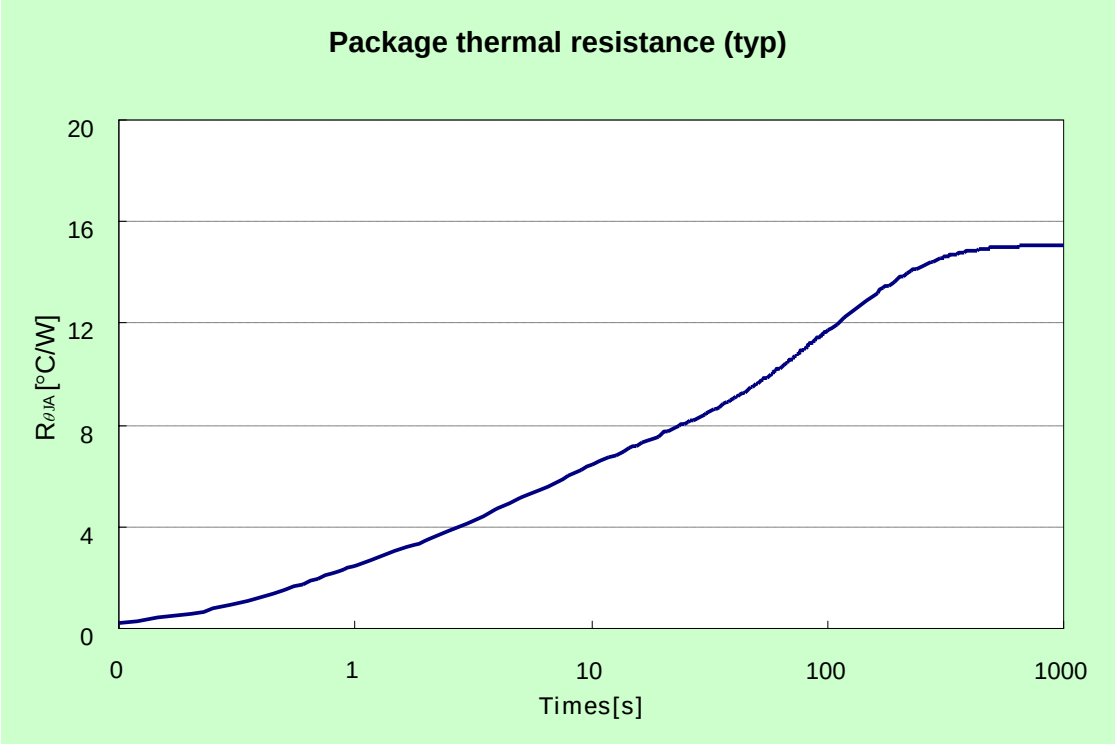
P64K8-50-6B4

| ITEM | | D2 | | | E2 | | |
|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX |
| EXPOSED DIE PAD VARIATIONS | A | 7.45 | 7.50 | 7.55 | 7.45 | 7.50 | 7.55 |

# <R> APPENDIX A PACKAGE THERMAL RESISTANCE

**Conditions**

| | |
|---|---|
| Substrate size: | 76.2 x 114.3 mm, t = 1.60 mm |
| Trace: | Four-layer (thickness of trace: 70 / 35 / 35 / 70 μm) |
| Material: | FR-4 |



# <R> APPENDIX B CALCULATION EXAMPLE OF TOTAL POWER DISSIPATION AND JUNCTION TEMPERATURE

**Calculation example of total power dissipation**

Condition of use

$V_{SUP}$ = 16 V

$I_{RO}$ = 20 mA

LIN = Normal mode (Recessive)

$T_A$ = 85°C

Microcontroller block) VRO = 5 V, $I_{DD1}$ = 3.2 mA

P1 = VRO × $I_{DD1}$ = 16 mW

Power supply circuit. LIN transceiver) $V_{SUP}$ = 16 V, $I_{SUP3}$ = 3 mA

P2 = $V_{SUP}$ × $I_{SUP3}$ = 48 mW

Drop out voltage) $V_{SUP}$ = 16 V, VRO = 5 V, $I_{RO}$ = 20 mA

P3 = ($V_{SUP}$ – VRO) × $I_{RO}$ = 220 mW

Half bridge) Ron = 1 Ω, Iload = 0.5 A, 6 ch

P4 = Ron × $Iload^2$ × 6 = 1.5 W

Total)

PD = P1 + P2 + P3 + P4 = 1.784 W

**Calculation example of junction temperature**

$T_J = (PD \times R_{\theta JA}^{Note}) + T_A$

= 111.47°C

**Note** $R_{\theta JA}$ use a value greater than or equal to 400 sec in Package thermal resistance characteristic (APPENDIX A).

**Caution Use this operation within a range that Tjmax value (150 °C).**

# <R> APPENDIX C REVISION HISTORY

## C.1 Major Revisions in This Edition

(1/2)

| Page | Description |
|---|---|
| **1. Outline** | |
| p.2 | Modification of **1.1 Features** |
| p.4, 5 | Modification of **1.4 Pin Configuration (Top View)** |
| p.6 to 8 | Modification of **1.5 Block Diagram** |
| p.9, 10 | Modification of **1.6 Outline of Functions** |
| **2. Pin Functions** | |
| p.11 | Modification of **2 (1) Port and alternate function pins** |
| p.12 | Modification of **Table 2-1. Pin I/O Buffer Power Supplies** |
| p.12, 13 | Modification of **2.1 (1) Port pins** |
| p.14 | Modification of **2.1 (2) Non-port functions** |
| p.17 | Modification of **2.2 Analog Part Pins** |
| p.20 | Modification of **2.3.3 P20 to P24 (Port 2)** |
| p.24 | Addition of **2.3.8 P130 (port 13)**, Modification of **2.3.9 $AV_{REF}$, $AV_{SS}$, $V_{DD}$, $V_{SS}$** |
| p.26 | Modification of **2.3.19 SWI, 2.3.20 SWO** |
| p.27 | Addition of **2.3.31 IC** |
| p.28-30 | Modification of description and addition of **note 4** in **Table 2-3. Pin I/O Circuit Types** |
| p.31, 33, 34 | Modification of **Figure 2-1. Pin I/O Circuit List** |
| **3. Microcontroller Functions** | |
| p.35 | Modification of **3.1 Differences in Functions between µPD78F807x and 78K0/KC2** |
| p.36 | Modification of **3.2 Differences in Special Function Registers between µPD78F807x and 78K0/KC2** |
| p.38 | Modification of **3.3.1 Port mode register** |
| p.39 | Modification of **3.3.2 Port register**, **3.3.3 Pull-up resistor option register** |
| p.40 | Modification of **3.3.4 Analog input channel specification register** |
| p.41 | Modification of **3.3.5 A/D port configuration register** |
| **4. Writing with Flash Programmer** | |
| p.50 | Modification of **Table 4-1. Wiring Dedicated Flash Programmer** |
| **5. Power Supply Circuit** | |
| p.51 | Modification of description in **5.4 Over Current Protection Function** |
| p.52 | Addition of caution in **5.6 External Dropper Auxiliary Function** |
| p.53 | Modification of **Figure 5-2. Power Supply Circuit Application Example Using On-Chip P-ch MOS** |
| p.54 | Modification of **Figure 5-3. Power Supply Circuit Application Example Using External NPN Transistor** |

(2/2)

| Page | Description |
|---|---|
| **6. LIN Transceiver** | |
| p.55 | Modification of description in **6.1 LIN Transceiver Function** |
| p.56 | Modification of **Figure 6-2. Operation Mode Transition Diagram** and **Table 6-1. LIN Operation Mode Setting**. Addition of caution in **Table 6-1. LIN Operation Mode Setting** |
| p.57 | Modification of **Table 6-2. Pin States in Each Port Mode** |
| p.58 | Modification of **Table 6-3. Operation States of Each Analog Function Block** |
| p.59 | Modification of description in **6.2 Operation Modes** |
| **7. Half-Bridge Circuit** | |
| p.63 | Modification of description in **7. Half-Bridge Circuit** |
| p.64 | Modification of **Mode transition diagram** and **Table 7-1. Operation State in Inhibit Mode** |
| p.65 | Modification of description in **7.2 Over Current Protection Function** |
| **10. Analog Reset Function** | |
| p.80 | Modification of **Table 10–1. Operation State of Analog Function Blocks during Analog Reset** and **Table 10–2. State of Analog Block Function Pins Interconnected in Package** |
| **11. Electrical Specifications ((A) Grade Products)** | |
| p.81, 82 | Modification of **11.1 Absolute Maximum Ratings** |
| p.85-87, 90, 91 | Modification of **11.2 Microcontroller Block Electrical Characteristics** |
| p.104, 109, 110, 112 | Modification of **11.3 Analog Block Characteristics** |
| **APPENDEX A PACKAGE HEAT-DISSIPATION** | |
| p.114 | Addition of **APPENDEX A PACKAGE HEAT-DISSIPATION** |
| **APPENDEX B CALCULATION EXAMPLE OF TOTAL POWER DISSIPATION AND JUNCTION TEMPERATURE** | |
| p.115 | Addition of **APPENDEX B CALCULATION EXAMPLE OF TOTAL POWER DISSIPATION AND JUNCTION TEMPERATURE** |
| **APPENDEX C REVISION HISTORY** | |
| p.116 | Addition of **APPENDEX C REVISION HISTORY** |

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