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April 1st, 2010
Renesas Electronics Corporation

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User's Manual

μPD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA

**8-Bit Single-Chip Microcontroller
With LIN Transceiver & Power Supply**

μPD78F8017A(A)

μPD78F8018A(A)

μPD78F8019A(A)

μPD78F8020A(A)

μPD78F8020DA

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[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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INTRODUCTION

Readers This manual is intended for user engineers who wish to understand the functions of the μ PD78F8017A, 78F8018A, 78F8019A, 78F8020A, and 78F8020DA, and to design and develop application systems and programs for these devices.

Purpose This manual is intended to give users an understanding of the functions described in the **Organization** below.

Organization The μ PD78F8017A, 78F8018A, 78F8019A, 78F8020A, and 78F8020DA's manuals are separated into three manuals: this manual, 78K0/Kx2 User's Manual, and the Instructions edition (common to the 78K0 Series).

μ PD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA User's Manual (This Manual)	78K0/Kx2 User's Manual	78K/0 Series User's Manual Instructions
<ul style="list-style-type: none"> • Pin functions • Internal block functions • On-chip peripheral functions • Electrical specifications 	<ul style="list-style-type: none"> • Pin functions • Internal block functions • Interrupts • Other on-chip peripheral functions • Electrical specifications 	<ul style="list-style-type: none"> • CPU functions • Instruction set • Explanation of each instruction

How to Read This Manual It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

- To gain a general understanding of functions:
 - Read this manual in the order of the **CONTENTS**. The mark <R> shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.
- The notation of the product name
 - Description of (A) is omitted in this manual. "(A)" product names should be read as follows.
 - μ PD78F8017A → μ PD78F8017A(A)
 - μ PD78F8018A → μ PD78F8018A(A)
 - μ PD78F8019A → μ PD78F8019A(A)
 - μ PD78F8020A → μ PD78F8020A(A)

- To know details of the microcontroller part:
→ Refer to the separate document **78K0/Kx2 User's Manual (U18598E)**.

78K0/KE2 microcontroller products	The products corresponding to the 78K0/KE2 microcontroller products
μ PD780534A	μ PD78F8017A
μ PD780535A	μ PD78F8018A
μ PD780536A	μ PD78F8019A
μ PD780537A	μ PD78F8020A
μ PD780537DA	μ PD78F8020DA

- To know details of the 78K0 microcontroller instructions:
→ Refer to the separate document **78K/0 Series Instructions User's Manual (U12326E)**.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representations:	xxx̄ (overscore over pin and signal name)
Note:	Footnote for item marked with Note in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numerical representations:	Binary ... xxxx or xxxxB
	Decimal ... xxx
	Hexadecimal ... xxxH

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μ PD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA User's Manual	This Manual
78K0/Kx2 User's Manual	U18598E
78K/0 Series Instructions User's Manual	U12326E
78K0/Kx2 Flash Memory Programming (Programmer) Application Note	U17739E
78K0 Microcontrollers Self Programming Library Type01 User's Manual	U18274E
78K0 Microcontrollers EEPROM™ Emulation Library Type01 User's Manual	U18275E

Documents Related to Development Tools (Hardware) (User's Manuals)

Document Name	Document No.
QB-78K0KX2 In-Circuit Emulator	U17341E
QB-MINI2 On-Chip Debug Emulator with Programming Function	U18371E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

Documents Related to Development Tools (Software) (User's Manuals)

Document Name		Document No.
RA78K0 Ver.3.80 Assembler Package User's Manual ^{Note 1}	Operation	U17199E
	Language	U17198E
	Structured Assembly Language	U17197E
78K0 Assembler Package RA78K0 Ver.4.01 Operating Precautions (Notification Document) ^{Note 1}		ZUD-CD-07-0181-E
CC78K0 Ver.3.70 C Compiler User's Manual ^{Note 2}	Operation	U17201E
	Language	U17200E
78K0 C Compiler CC78K0 Ver. 4.00 Operating Precautions (Notification Document) ^{Note 2}		ZUD-CD-07-0103-E
ID78K0-QB Ver.2.94 Integrated Debugger User's Manual	Operation	U18330E
ID78K0-QB Ver.3.00 Integrated Debugger User's Manual	Operation	U18492E
PM plus Ver.5.20 ^{Note 3} User's Manual		U16934E
PM+ Ver.6.30 ^{Note 4} User's Manual		U18416E

- Notes**
1. This document is installed into the PC together with the tool when installing RA78K0 Ver. 4.01. For descriptions not included in "78K0 Assembler Package RA78K0 Ver. 4.01 Operating Precautions", refer to the user's manual of RA78K0 Ver. 3.80.
 2. This document is installed into the PC together with the tool when installing CC78K0 Ver. 4.00. For descriptions not included in "78K0 C Compiler CC78K0 Ver. 4.00 Operating Precautions", refer to the user's manual of CC78K0 Ver. 3.70.
 3. PM plus Ver. 5.20 is the integrated development environment included with RA78K0 Ver. 3.80.
 4. PM+ Ver. 6.30 is the integrated development environment included with RA78K0 Ver. 4.01. Software tool (assembler, C compiler, debugger, and simulator) products of different versions can be managed.

Documents Related to Flash Memory Programming

Document Name	Document No.
PG-FP5 Flash Memory Programmer User's Manual	U18865E
PG-FP4 Flash Memory Programmer User's Manual	U15260E

Other Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE – Product and Packages –	X13769X
Semiconductor Device Mount Manual	Note
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E
Review of Quality and Reliability Handbook Information	C12769E

Note See the "Semiconductor Device Mount Manual" website (<http://www.necel.com/pkg/en/mount/index.html>)

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

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CHAPTER 1 OUTLINE

μ PD78F8017A, 78F8018A, 78F8019A, 78F8020A, and 78F8020DA are MCP (Multi-Chip Package) which combined 2 chips in 1 package: an analog chip (including LIN transceiver, power supply, and several drivers) and a microcontroller chip.

8-bit microcontroller block is 78K0/KE2.

1.1 Features

- ROM, RAM capacities

Item \ Part Number	Program Memory (ROM)		Data Memory	
			Internal High-Speed RAM ^{Note}	Internal Expansion RAM ^{Note}
μ PD78F8017A	Flash memory	48 KB ^{Note}	1 KB	1 KB
μ PD78F8018A		60 KB ^{Note}		2 KB
μ PD78F8019A		96 KB ^{Note}		4 KB
μ PD78F8020A, μ PD78F8020DA		128 KB ^{Note}		6 KB

Note The internal flash memory, internal high-speed RAM capacities, and internal expansion RAM capacities can be changed using the internal memory size switching register (IMS) and the internal expansion RAM size switching register (IXS).

- On-chip single-power-supply flash memory
- Self-programming (with boot swap function)
- On-chip debug function (μ PD78F8020DA only)^{Note 1}
- On-chip power-on-clear (POC) circuit and low-voltage detector (LVI)
- On-chip watchdog timer (operable with the on-chip internal low speed oscillation clock)
- On-chip multiplier/divider (16 bits x 16 bits, 32 bits x 16 bits)
- On-chip key interrupt function
- I/O ports: 28 (N-ch open drain: 2)
- Timer: 8 channels
 - 16-bit timer/event counters: 2 channels
 - 8-bit timer/event counters: 2 channels
 - 8-bit timer: 2 channels
 - Watch timer: 1 channel
 - Watch dog timer: 1 channel
- Serial interface: 3 channels
 - UART (LIN (Local Interconnect Network)-bus supported): 1 channel
 - CSI/UART^{Note 2}: 1 channel
 - IIC: 1 channel
- 10-bit resolution A/D converter: 6 channels

Notes 1. The μ PD78F8020DA has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. NEC Electronics is not liable for problems occurring when the on-chip debug function is used.

2. Select either of the functions of these alternate-function pins.

- On-chip power supply circuit
 - Output voltage: $5\text{ V} \pm 3\%$
 - On-chip over current protection circuit
 - On-chip thermal shutdown circuit
- LIN transceiver
 - The LIN transceiver complies with LIN Specifications Rev.2.0
 - Low power consumption achieved with on-chip sleep function
 - On-chip pull-up resistors for slave applications
 - On-chip LIN driver over current protection circuit
 - On-chip LIN driver thermal shutdown circuit
- Driver
 - Low side driver: 3 channels
 - Low side pre driver: 1 channel
 - High side driver: 1 channels
- Package: 64-pin plastic LQFP (fine-pitch) (10×10)
- Operation ambient temperature: $T_A = -40$ to $+85\text{ }^\circ\text{C}$

1.2 Applications

- Automotive equipment
 - System control for body electronic control units
 - Power windows
 - Power slide door
 - Mirror control, etc.

1.3 Ordering Information

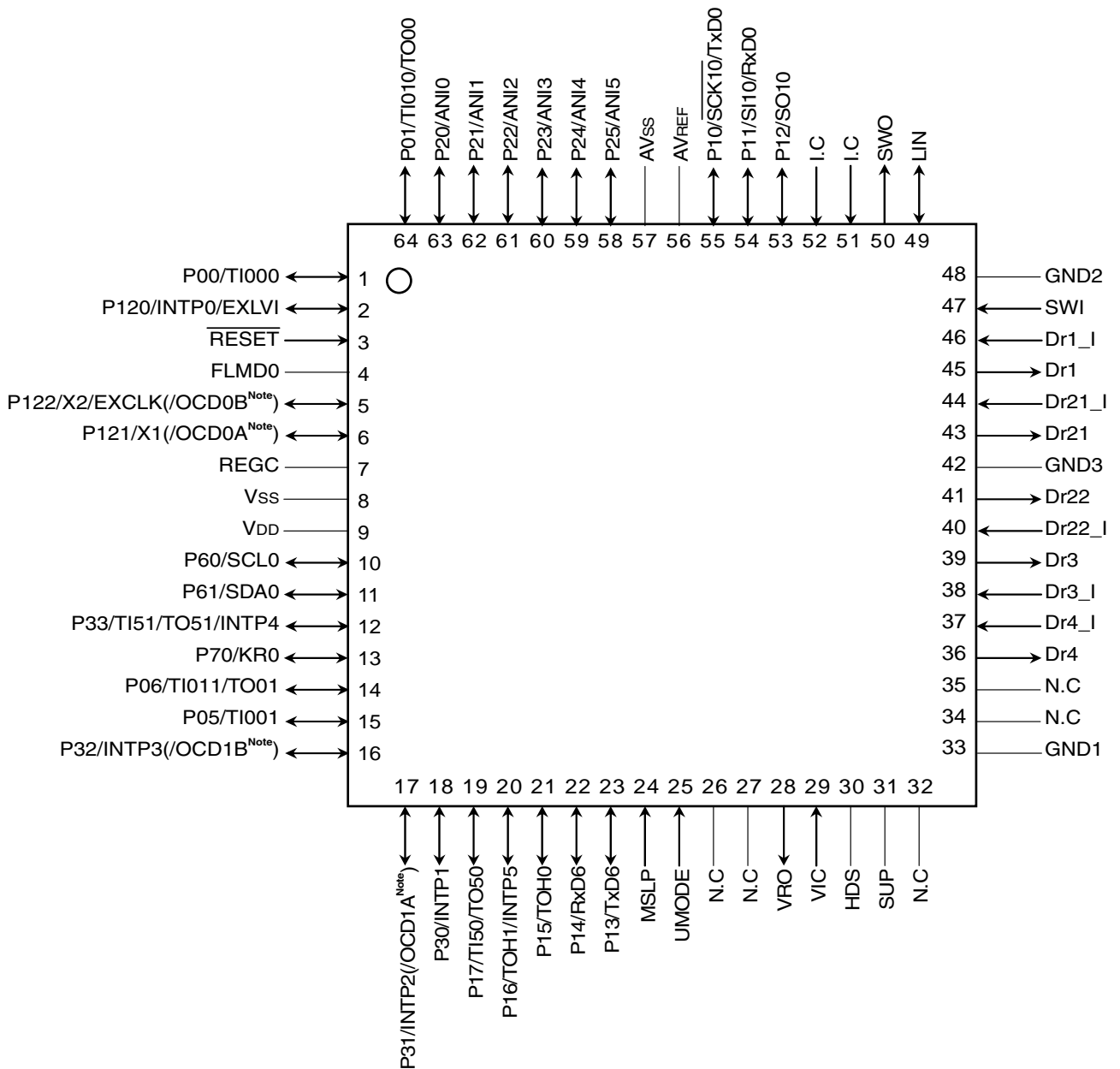
	Part Number	Package	Quality Grade
<R>	μ PD78F8017AGBA-GAH-G ^{Note}	64-pin plastic LQFP (fine pitch) (10×10)	Special
<R>	μ PD78F8018AGBA-GAH-G ^{Note}	64-pin plastic LQFP (fine pitch) (10×10)	Special
<R>	μ PD78F8019AGBA-GAH-G ^{Note}	64-pin plastic LQFP (fine pitch) (10×10)	Special
<R>	μ PD78F8020AGBA-GAH-G ^{Note}	64-pin plastic LQFP (fine pitch) (10×10)	Special
<R>	μ PD78F8020DAGB-GAH-G	64-pin plastic LQFP (fine pitch) (10×10)	Standard

Note (A) grade product

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1.4 Pin Configuration (Top View)

- 64-pin plastic LQFP (fine-pitch) (10x10)



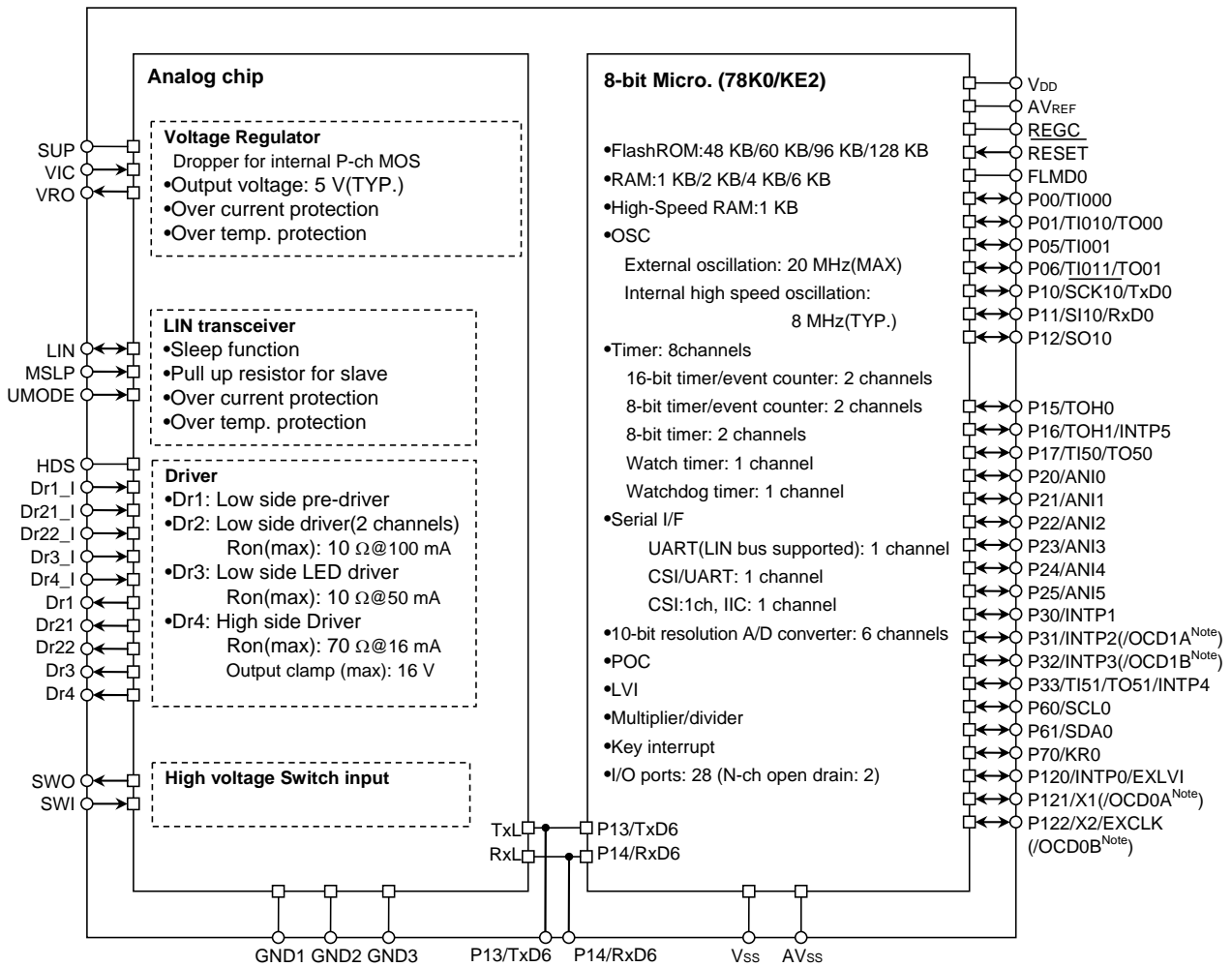
Note μ PD78F8020DA only

- Cautions**
1. Make AV_{SS} the same potential as V_{SS}.
 2. Connect the REGC pin to V_{SS} via a capacitor (0.47 μ F to 1 μ F: recommended).
 3. ANI0/P20 to ANI5/P25 are in the analog input mode after reset release.
 4. Make V_{SS} the same potential as GND1 to GND3.
 5. Make SUP the same potential as HDS.
 6. Make VRO the same potential as V_{DD}.

Pin Identification

ANI0 to ANI5	Analog Input	P30 to P33	Port 3
AV _{REF}	Analog Reference Voltage	P60, P61	Port 6
AV _{SS}	Analog Ground	P70	Port 7
Dr1, Dr21, Dr22,		P120 to P122	Port 12
Dr3, Dr4	Driver Output	REGC	Regulator Capacitance
Dr1_I, Dr21_I,		RESET	Reset
Dr22_I, Dr3_I,		RxD0, RxD6	Receive Data
Dr4_I	Driver Control	SCK10, SCL0	Serial Clock Input/Output
EXCLK	External Clock Input (Main System Clock)	SDA0	Serial Data Input/Output
EXLVI	External potential Input for Low-voltage detector	SI10	Serial Data Input
FLMD0	Flash Programming Mode	SO10	Serial Data Output
GND1 to GND3	Ground	SUP	Power Supply
HDS	High-side Driver Power Supply	SWI	SW Input
I.C	Internal Connect	SWOSW	input signal Output
INTP0 to INTP5	External Interrupt Input	TI000, TI010,	
KR0	Key Return	TI50, TI51	Timer Input
LIN	LIN Bus	TO00,	
MSLP	Sleep Mode	TO50, TO51,	
N.C	Non-connection	TOH0, TOH1	Timer Output
OCD0A, OCD0B,		TxD0, TxD6	Transmit Data
OCD1A, OCD1B	On-Chip Debug Input/Output	UMODE	LIN Mode
P00, P01,		V _{DD}	Power Supply
P05, P06	Port 0	VIC	Power Supply and Current Monitor
P10 to P17	Port 1	VRO	Voltage Regulator Output
P20 to P25	Port 2	V _{SS}	Ground
		X1, X2	Crystal Oscillator (Main System Clock)

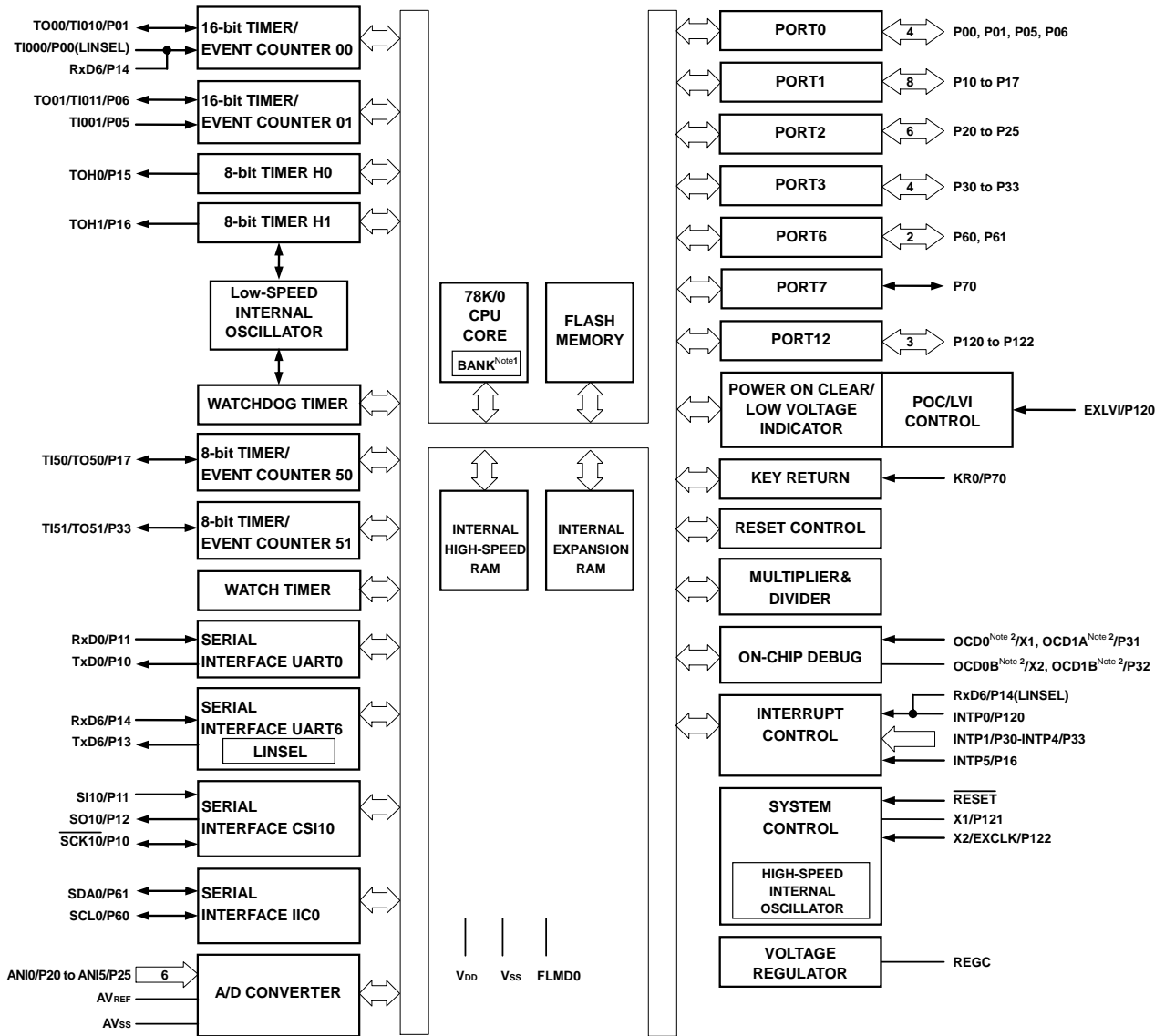
1.5 Block Diagram



Note μ PD78F8020DA only

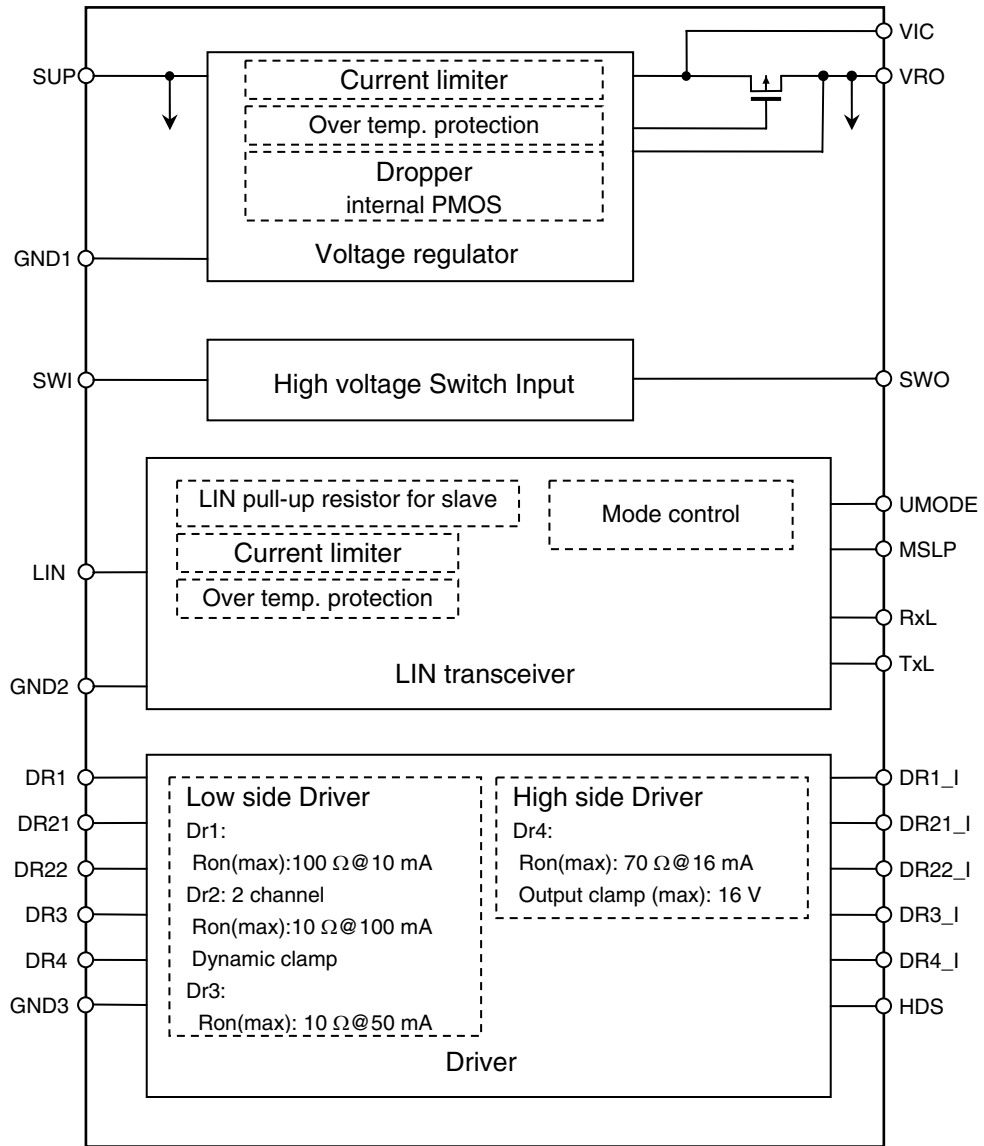
- Cautions 1.** μ PD78F8017A, 78F8018A, 78F8019A, 78F8020A, and 78F8020DA are developed as MCP (Multi-Chip Package) which includes 2 chips in the package, a microcontroller and an analog chip.
- 2.** The P13/TxD6 and P14/RxD6 terminals are connected with the LIN transceiver inside the package.

1.5.1 Microcontroller block diagram



- Notes 1. μ PD78F8019A, 78F8020A, and 78F8020DA only
 2. μ PD78F8020DA only

1.5.2 Analog block diagram



1.6 Outline of Functions

(1/2)

Item	μ PD78F8017A	μ PD78F8018A	μ PD78F8019A	μ PD78F8020A	μ PD78F8020DA
Flash memory (KB)	48	60	96	128	
High-Speed RAM (KB)	1				
Expansion RAM (KB)	1	2	4	6	
Bank (flash memory)	-		4	6	
Power supply voltage	$V_{DD} = 1.8$ to 5.5 V				
Regulator	Provided				
Minimum instruction execution time	0.1 μ s (20 MHz: $V_{DD} = 2.7$ to 5.5 V)/0.4 μ s (5 MHz: $V_{DD} = 1.8$ to 5.5 V)				
Clock	Main	High-speed system	20 MHz: $V_{DD} = 2.7$ to 5.5 V/5 MHz: $V_{DD} = 1.8$ to 5.5 V		
		Internal high-speed oscillation	8 MHz (TYP.): $V_{DD} = 1.8$ to 5.5 V		
	Internal low-speed oscillation	240 kHz (TYP.): $V_{DD} = 1.8$ to 5.5 V			
Port	Total	28			
	N-ch O.D. (6 V tolerance)	2			
Timer	16 bits (TM0)	1 ch			
	8 bits (TM5)	2 ch			
	8 bits (TMH)	2 ch			
	Watch	1 ch			
	WDT	1 ch			
Serial interface	UART/3-wire CSI ^{Note}	1 ch			
	UART supporting LIN-bus	1 ch			
	I ² C bus	1 ch			
10-bit A/D	6 ch				
Interrupt	External	7			
	Internal	18			
Key interrupt	1 ch				
Reset	RESET pin	Provided			
	POC	1.59 V \pm 0.15 V			
	LVI	The detection level of the supply voltage is selectable.			
	WDT	Provided			
Multiplier/divider	Provided				
On-chip debug function	-			Provided	
Operating ambient temperature	$T_A = -40$ to $+85^\circ\text{C}$				

Note Select either of the functions of these alternate-function pins.

Item	μ PD78F8017A	μ PD78F8018A	μ PD78F8019A	μ PD78F8020A	μ PD78F8020DA
Power Supply	<ul style="list-style-type: none"> • Input voltage : $V_{SUP} = 7V$ to 19 V • Include P-ch MOS for dropper • Output voltage: $5 V \pm 3\%$ • On-chip over current protection circuit • On-chip thermal shutdown circuit 				
LIN transceiver	<ul style="list-style-type: none"> • The LIN transceiver complies with LIN Specifications Rev.2.0 • Low power consumption achieved with on-chip sleep function • On-chip pull-up resistors for slave applications • On-chip LIN driver current protection circuit • On-chip LIN driver thermal shutdown circuit 				
Driver	<ul style="list-style-type: none"> • Low side driver[4 channels] <ul style="list-style-type: none"> Pre-driver :1 channel Relay-driver :2 channels (Include dynamic clamp) LED driver :1 channel • High side driver :1 channel (Includes 16 V clamp circuit) 				

An outline of the timer is shown below.

		16-Bit Timer/ Event Counters 00 and 01		8-Bit Timer/ Event Counters 50 and 51		8-Bit Timers H0 and H1		Watch Timer	Watchdog Timer
		TM00	TM01	TM50	TM51	TMH0	TMH1		
Function	Interval timer	1 channel	1 channel	1 channel	1 channel	1 channel	1 channel	1 channel Note 1	–
	External event counter	1 channel	1 channel	1 channel	1 channel	–	–	–	–
	PPG output	1 output	1 output	–	–	–	–	–	–
	PWM output	–	–	1 output	1 output	1 output	1 output	–	–
	Pulse width measurement	2 inputs	2 inputs	–	–	–	–	–	–
	Square-wave output	1 output	1 output	1 output	1 output	1 output	1 output	–	–
	Carrier generator	–	–	–	–	–	1 output Note 2	–	–
	Watch Timer	–	–	–	–	–	–	1 channel Note 1	–
	Watchdog timer	–	–	–	–	–	–	–	1 channel
Interrupt source		2	2	1	1	1	1	1	–

- Notes 1.** The watch timer function and interval timer function of the watch timer can be used simultaneously.
- 2.** TM51 and TMH1 can be used in combination as a carrier generator mode.

CHAPTER 2 PIN FUNCTIONS

The differences in microcontroller pin functions between μ PD78F8017A, 78F8018A, 78F8019A, 78F8020A, and 78F8020DA and the 78K0/KE2 are as follows.

(1) Port and alternate function pins

μ PD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA		78K0/KE2 μ PD78F0534A, 78F0535A, 78F0536A, 78F0537A, 78F0537DA		μ PD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA		78K0/KE2 μ PD78F0534A, 78F0535A, 78F0536A, 78F0537A, 78F0537DA	
Pin name	Alternate function	Pin name	Alternate function	Pin name	Alternate function	Pin name	Alternate function
P00	TI000	P00	TI000	P32	INTP3/OCD1B ^{Note 1}	P32	INTP3/OCD1B ^{Note 2}
P01	TI010/TO00	P01	TI010/TO00	P33	INTP4/TI51/TO51	P33	INTP4/TI51/TO51
–	–	P02	SO11	–	–	P40 to P43	–
–	–	P03	SI11	–	–	P50 to P53	–
–	–	P04	$\overline{\text{SCK}}11$	P60	SCL0	P60	SCL0
P05	TI001	P05	$\overline{\text{SSI}}11/\text{TI001}$	P61	SDA0	P61	SDA0
P06	TI011/TO01	P06	TI011/TO01	–	–	P62	EXSCL0
P10	$\overline{\text{SCK}}10/\text{TxD0}$	P10	$\overline{\text{SCK}}10/\text{TxD0}$	–	–	P63	–
P11	SI10/RxD0	P11	SI10/RxD0	P70	KR0	P70 to P77	KR0 to KR7
P12	SO10	P12	SO10	P120	INTP0/EXLVI	P120	INTP0/EXLVI
P13	TxD6	P13	TxD6	P121	X1/OCD0A ^{Note 1}	P121	X1/OCD0A ^{Note 2}
P14	RxD6	P14	RxD6	P122	X2/EXCLK/ OCD0B ^{Note 1}	P122	X2/EXCLK/ OCD0B ^{Note 2}
P15	TOH0	P15	TOH0	–	–	P123	XT1
P16	TOH1/INTP5	P16	TOH1/INTP5	–	–	P124	XT2/EXCLKS
P17	TI50/TO50	P17	TI50/TO50	–	–	P130	–
P20 to P25	ANI0 to ANI5	P20 to P27	ANI0 to ANI7	–	–	P140	PCL/INTP6
P30	INTP1	P30	INTP1	–	–	P141	BUZ/INTP7
P31	INTP2/OCD1A ^{Note 1}	P31	INTP2/OCD1A ^{Note 2}				

Notes 1. μ PD78F8020DA only

2. μ PD78F0537DA only

(2) Non-port pins

μ PD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA		78K0/KE2 μ PD78F0534A, 78F0535A, 78F0536A, 78F0537A, 78F0537DA		μ PD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA		78K0/KE2 μ PD78F0534A, 78F0535A, 78F0536A, 78F0537A, 78F0537DA	
Pin name	Pin name	Pin name	Pin name	Pin name	Pin name	Pin name	Pin name
V _{DD}	V _{DD}	FLMD0	FLMD0	FLMD0	FLMD0	FLMD0	FLMD0
V _{SS}	V _{SS}	AV _{REF}	AV _{REF}	AV _{REF}	AV _{REF}	AV _{REF}	AV _{REF}
– ^{Note}	EV _{DD}	AV _{SS}	AV _{SS}	AV _{SS}	AV _{SS}	AV _{SS}	AV _{SS}
– ^{Note}	EV _{SS}	REGC	REGC	REGC	REGC	REGC	REGC
RESET	RESET						

Note EV_{DD} and EV_{SS} are connected within package.

2.1 Microcontroller Part Pin Functions

There are two types of pin I/O buffer power supplies: AVREF, and VDD. The relationship between these power supplies and the pins are shown below.

Table 2-1. Pin I/O Buffer Power Supplies

Power Supply	Corresponding Pins
AVREF	P20 to P25
VDD	Pins other than P20 to P25

(1) Port pins

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI000
P01				TI010/TO00
P05				TI001/SS11
P06				TI011/TO01
P10	I/O	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SCK10/TxD0
P11				SI10/RxD0
P12				SO10
P13				TxD6
P14				RxD6
P15				TOH0
P16				TOH1/INTP5
P17				TI50/TO50
P20 to P25	I/O	Port 2. 6-bit I/O port. Input/output can be specified in 1-bit units.	Analog input	ANI0 to ANI5
P30	I/O	Port 3. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP1
P31				INTP2/OCD1A ^{Note}
P32				INTP3/OCD1B ^{Note}
P33				TI51/TO51/INTP4
P60	I/O	Port 6. 2-bit I/O port. Output of P60 to P61 is N-ch open-drain output (6V tolerance). Input/output can be specified in 1-bit units.	Input port	SCL0
P61				SDA0
P70	I/O	Port 7. I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0
P120	I/O	Port 12. 3-bit I/O port. Input/output can be specified in 1-bit units. Only for P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121				X1/OCD0A ^{Note}
P122				X2/EXCLK/ OCD0B ^{Note}

Note μ PD78F8020DA only

(2) Non-port functions (1/2)

Function Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP1				P30
INTP2				P31/OCD1A ^{Note}
INTP3				P32/OCD1B ^{Note}
INTP4				P33/TI51/TO51
INTP5				P16/TOH1
SI10	Input	Serial data input to serial interface	Input port	P11/RxD0
SO10	Output	Serial data output from serial interface	Input port	P12
SDA0	I/O	Serial data I/O for serial interface	Input port	P61
$\overline{\text{SCK10}}$	I/O	Clock input/output for serial interface	Input port	P10/TxD0
SCL0				P60
RxD0	Input	Serial data input to asynchronous serial interface	Input port	P11/SI10
RxD6				P14
TxD0	Output	Serial data output from asynchronous serial interface	Input port	P10/ $\overline{\text{SCK10}}$
TxD6				P13
TI000	Input	External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture registers (CR000, CR010) of 16-bit timer/event counter 00	Input port	P00
TI001		External count clock input to 16-bit timer/event counter 01 Capture trigger input to capture registers (CR001, CR011) of 16-bit timer/event counter 01		P05
TI010		Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00		P01/TO00
TI011		Capture trigger input to capture register (CR001) of 16-bit timer/event counter 01		P06/TO01
TO00	Output	16-bit timer/event counter 00 output	Input port	P01/TO10
TO01		16-bit timer/event counter 01 output		P06/TO11
TI50	Input	External count clock input to 8-bit timer/event counter 50	Input port	P17/TO50
TI51		External count clock input to 8-bit timer/event counter 51		P33/TO51/INTP4

Note μ PD78F8020DA only

(2) Non-port functions (2/2)

Function Name	I/O	Function	After Reset	Alternate Function
TO50	Output	8-bit timer/event counter 50 output	Input port	P17/TI50
TO51		8-bit timer/event counter 51 output		P33/TI51/INTP4
TOH0		8-bit timer H0 output		P15
TOH1		8-bit timer H1 output		P16/INTP5
ANI0 to ANI5	Input	A/D converter analog input	Analog input	P20 to P25
AV _{REF}	Input	A/D converter reference voltage input and positive power supply for P20 to P25 and A/D converter	–	–
AV _{SS}	–	A/D converter ground potential. Make the same potential as EV _{SS} or V _{SS} .	–	–
KR0	Input	Key interrupt input	Input port	P70
REGC	–	Connecting regulator output (2.5 V) stabilization capacitance for internal operation. Connect to V _{SS} via a capacitor (0.47 μ F: target).	–	–
$\overline{\text{RESET}}$	Input	System reset input	–	–
EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
X1	Input	Connecting resonator for main system clock	Input port	P121/OCD0A ^{Note}
X2	–			P122/EXCLK/ OCD0B ^{Note}
EXCLK	Input	External clock input for main system clock	Input port	P122/X2/ OCD0B ^{Note}
V _{DD}	–	Positive power supply (P121 to P122 and except for ports)	–	–
V _{SS}	–	Ground potential (P121 to P122 and except for ports)	–	–
FLMD0	–	Flash memory programming mode setting	–	–
OCD0A ^{Note}	Input	Connection for on-chip debug mode setting pins (μ PD78F8020DA only)	Input port	P121/X1
OCD1A ^{Note}				P31/INTP2
OCD0B ^{Note}	–			P122/X2/EXCLK
OCD1B ^{Note}	–			P32/INTP3

Note μ PD78F8020DA only

2.2 Analog Part Pins

Function Name	I/O	Function
Dr1	Output	Driver 1 output
Dr21	Output	Driver 21 output
Dr22	Output	Driver 22 output
Dr3	Output	Driver 3 output
Dr4	Output	Driver 4 output
Dr1_I	Input	Driver 1 control signal input
Dr21_I	Input	Driver 21 control signal input
Dr22_I	Input	Driver 22 control signal input
Dr3_I	Input	Driver 3 control signal input
Dr4_I	Input	Driver 4 control signal input
GND1	–	Power supply circuit GND
GND2	–	LIN transceiver circuit GND
GND3	–	Driver circuit GND
HDS	–	High side driver power supply
LIN	I/O	LIN Bus connection pin
MSLP	Input	Sleep / Normal mode select for LIN
SUP	–	Power supply connection pin
SWI	Input	High voltage SW input pin
SWO	Output	SW1 signal output pin
UMODE	Input	LIN transceiver function enable / disable selection pin Low: Enable LIN transceiver High: Disable LIN transceiver
VIC	Input	Power supply and current monitor
VRO	Output	Voltage regulator output and monitor

- Cautions**
1. Make GND1, GND2, GND3 the same potential as V_{SS} and AV_{SS}
 2. Make SUP the same potential as HDS.
 3. Make VRO the same potential as V_{DD}.

2.3 Description of Pin Functions

2.3.1 P00, P01, P05, P06 (port 0)

4-bit I/O port. These pins also function as timer I/O.

The following operation modes can be specified in 1-bit units.

(1) Port mode

4-bit I/O port. P00, P01 can be set to input or output port in 1-bit units using port mode register 0 (PM0). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 0 (PU0).

(2) Control mode

P00, P01 function as timer I/O.

(a) TI000, TI001

These are the pins for inputting an external count clock to 16-bit timer/event counters 00 and 01 and are also for inputting a capture trigger signal to the capture registers (CR000, CR010 or CR001, CR011) of 16-bit timer/event counters 00 and 01.

(b) TI010, TI011

These are the pins for inputting a capture trigger signal to the capture register (CR000 or CR001) of 16-bit timer/event counters 00 and 01.

(c) TO00, TO01

These are timer output pins of 16-bit timer/event counters 00 and 01.

2.3.2 P10 to P17 (port 1)

P10 to P17 function as an 8-bit I/O port. These pins also function as pins for external interrupt request input, serial interface data I/O, clock I/O, and timer I/O.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P10 to P17 function as an 8-bit I/O port. P10 to P17 can be set to input or output port in 1-bit units using port mode register 1 (PM1). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 1 (PU1).

(2) Control mode

P10 to P17 function as external interrupt request input, serial interface data I/O, clock I/O, and timer I/O.

(a) SI10

This is a serial data input pin of serial interface CSI10.

(b) SO10

This is a serial data output pin of serial interface CSI10.

(c) $\overline{\text{SCK10}}$

This is a serial clock I/O pin of serial interface CSI10.

(d) RxD0

This is a serial data input pin of serial interface UART0.

(e) RxD6

This is a serial data input pin of serial interface UART6.

(f) TxD0

This is a serial data output pin of serial interface UART0.

(g) TxD6

This is a serial data output pin of serial interface UART6.

(h) TI50

This is the pin for inputting an external count clock to 8-bit timer/event counter 50.

(i) TO50

This is a timer output pin of 8-bit timer/event counter 50.

(j) TOH0, TOH1

These are the timer output pins of 8-bit timers H0 and H1.

(k) INTP5

This is an external interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

2.3.3 P20 to P25 (port 2)

P20 to P25 function as a 6-bit I/O port. These pins also function as pins for A/D converter analog input.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P20 to P25 function as a 6-bit I/O port. P20 to P25 can be set to input or output port in 1-bit units using port mode register 2 (PM2).

(2) Control mode

P20 to P25 function as A/D converter analog input pins (ANI0 to ANI5). When using these pins as analog input pins, see **13.6 Cautions for A/D Converter in 78K0/Kx2 User's Manual (U18598E)**.

(a) ANI0 to ANI5

These are A/D converter analog input pins.

Caution ANI0/P20 to ANI7/P25 are set to analog input mode after reset release.

2.3.4 P30 to P33 (port 3)

P30 to P33 function as a 4-bit I/O port. These pins also function as pins for external interrupt request input and timer I/O.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P30 to P33 function as a 4-bit I/O port. P30 to P33 can be set to input or output port in 1-bit units using port mode register 3 (PM3). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 3 (PU3).

(2) Control mode

P30 to P33 function as external interrupt request input and timer I/O.

(a) INTP1 to INTP4

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) TI51

This is an external count clock input pin to 8-bit timer/event counter 51.

(c) TO51

This is a timer output pin from 8-bit timer/event counter 51.

Caution In the μ PD78F8020DA, be sure to pull down pin P31 before reset release to prevent malfunction.

Remark Only for μ PD78F8020DA, P31 and P32 can be used as on-chip debug mode setting pins (OCD1A, OCD1B) when the on-chip debug function is used. For how to connect an in-circuit emulator supporting on-chip debugging (QB-78K0MINI), see **CHAPTER 28 ON-CHIP DEBUG FUNCTION in 78K0/Kx2 User's Manual (U18598E)**.

2.3.5 P60 to P61 (port 6)

P60 to P61 function as a 2-bit I/O port. These pins also function as pins for serial interface data I/O, clock I/O.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P60 to P61 function as a 2-bit I/O port. P60 to P61 can be set to input port or output port in 1-bit units using port mode register 6 (PM6).

Output of P60 to P61 is N-ch open-drain output (6 V tolerance).

(2) Control mode

P60 to P61 function as serial interface data I/O, clock I/O.

(a) SDA0

This is a serial data I/O pin for serial interface IIC0.

(b) SCL0

This is a serial clock I/O pin for serial interface IIC0.

2.3.6 P70 (port 7)

P70 function as a 1-bit I/O port. These pins also function as key interrupt input pins.

The following operation modes can be specified.

(1) Port mode

P70 function as a 1-bit I/O port. P70 can be set to input or output port using port mode register 7 (PM7). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 7 (PU7).

(2) Control mode

P70 function as key interrupt input pins.

(a) KR0

This is a key interrupt input pins

2.3.7 P120 to P122 (port 12)

P120 to P122 function as a 3-bit I/O port. These pins also function as pins for external interrupt request input, potential input for external low-voltage detection, connecting resonator for main system clock, external clock input for main system clock. The following operation modes can be specified in 1-bit units.

(1) Port mode

P120 to P122 function as a 3-bit I/O port. P120 to P122 can be set to input or output port using port mode register 12 (PM12). Only for P120, use of an on-chip pull-up resistor can be specified by pull-up resistor option register 12 (PU12).

(2) Control mode

P120 to P122 function as pins for external interrupt request input, potential input for external low-voltage detection, connecting resonator for main system clock, external clock input for main system clock.

(a) INTPO

This functions as an external interrupt request input (INTPO) for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) EXLVI

This is a potential input pin for external low-voltage detection.

(c) X1, X2

These are the pins for connecting a resonator for main system clock.

(d) EXCLK

This is an external clock input pin for main system clock.

Remark Only for μ PD78F8020DA, X1 and X2 can be used as on-chip debug mode setting pins (OCD0A, OCD0B) when the on-chip debug function is used. For how to connect an in-circuit emulator supporting on-chip debugging (QB-78K0MINI), see **CHAPTER 28 ON-CHIP DEBUG FUNCTION in 78K0/Kx2 User's Manual (U18598E)**.

2.3.8 AV_{REF}

This is the A/D converter reference voltage input pin and the positive power supply pin of P20 to P25 and A/D converter.

When the A/D converter is not used, connect this pin directly to V_{DD}^{Note}.

Note Make the AV_{REF} pin the same potential as the V_{DD} pin when port 2 is used as a digital port.

2.3.9 AV_{SS}

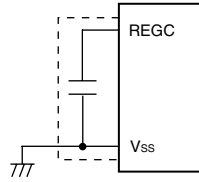
This is the A/D converter ground potential pin. Even when the A/D converter is not used, always use this pin with the same potential as the VSS pin.

2.3.10 $\overline{\text{RESET}}$

This is the active-low system reset input pin.

2.3.11 REGC

This is the pin for connecting regulator output (2.5 V) stabilization capacitance for internal operation. Connect this pin to V_{SS} via a capacitor (0.47 to 1 μ F: recommended).



Caution Keep the wiring length as short as possible for the broken-line part in the above figure.

2.3.12 V_{DD}

V_{DD} is the positive power supply pin for Micro.

2.3.13 V_{SS}

V_{SS} is the ground potential pin.

2.3.14 FLMD0

This is a pin for setting flash memory programming mode.

Connect FLMD0 to V_{SS} in the normal operation mode.

In flash memory programming mode, connect this pin to the flash programmer.

2.3.15 Dr1, Dr21, Dr22, Dr3, Dr4

These are high voltage driver output pin.

Each driver output can control with the Dr1_I, Dr21_I, Dr22_I, Dr3_I, Dr4_I input signal.

(a) Dr1

This is a Low side driver output pin.

(b) Dr21, Dr22

This is a Low side driver output pin.

These pin has dynamic clump function for high voltage protection.

(c) Dr3

This is a Low side driver output pin.

(d) Dr4

This is a High side driver output pin.

This pin has output voltage clump function, over current protection and thermal shutdown function.

2.3.16 Dr1_I, Dr21_I, Dr22_I, Dr3_I, Dr4_I

These are input pins for high voltage driver control.

These pin have a pull-down resistor inside the IC.

Table 2-2. Truth Table

Input		Dr1	Dr21	Dr22	Dr3	Dr4
Dr1_I	High	ON	-	-	-	-
	Low	OFF	-	-	-	-
Dr21_I	High	-	ON	-	-	-
	Low	-	OFF	-	-	-
Dr22_I	High	-	-	ON	-	-
	Low	-	-	OFF	-	-
Dr3_I	High	-	-	-	ON	-
	Low	-	-	-	OFF	-
Dr4_I	High	-	-	-	-	ON
	Low	-	-	-	-	OFF

2.3.17 GND1, GND2, GND3

GND1 is a power supply circuit GND.

GND2 is an LIN transceiver circuit GND.

GND3 is a driver circuit GND.

Connect GND1, GND2, and GND3 to the same potential as V_{ss} and AV_{ss}.

2.3.18 HDS

This is a power supply pin for high side driver.

Connect HDS to the same potential as SUP.

2.3.19 LIN

This is a LIN Bus connection pin.

2.3.20 MSLP

This pin is used to switch the LIN transceiver between normal and sleep mode. In the normal mode the LIN transceiver goes into sleep mode when MSLP is set to low and in the sleep mode the LIN transceiver goes into normal mode when MSLP is set to high.

Moreover, this pin has a pull-down resistor inside the IC.

2.3.21 SUP

SUP is the positive power supply pin.

2.3.22 SWI

SWI is the high voltage input pin for external switch.

2.3.23 SWO

SWO is the SW1 input signal output pin.

2.3.24 UMODE

This pin is used as mode pin to enable/disable the LIN transceiver function. This pin is pulled-down inside the IC.

UMODE	LIN Transceiver Circuit Status	P13/TxD6 Pin Status	P14/RxD6 Pin Status
Low	Active	Output ^{Note} (TxL: Pull up input)	Input ^{Note} (RxL: Output)
High	Non active (Driver OFF)	Input /Output (TxL: Hi-Z)	Input /Output (RxL: Hi-Z)

Note When the LIN transceiver function is enabled, leave the P13/TxD6 and P14/RxD6 pins open. Clear PM13 to 0 (P13/TxD6 output setting) and set PM14 to 1 (P14/RxD6 input setting)

2.3.25 VIC

VIC is the supply voltage and current monitor pin for voltage regulator

2.3.26 VRO

VRO is a voltage regulator output and output voltage monitor.

2.3.27 IC (Internal Connected)

IC pin is pull-down in package. No function.

Always make this terminal open.

2.3.28 N.C (Non-connection)

Connect directly to GND1 or GND3.

PIN Number	GND
26, 27, 32	GND1
34, 35	GND3

2.4 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-3 shows the types of pin I/O circuit and the recommended connections of unused pins. Refer to Figure 2-1 for the configuration of the I/O circuits of each type.

Table 2-3. Pin I/O Circuit Types (1/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/TI000	5-AH	I/O	Input: Connect independently to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P01/TI010/TO00			
P05/TI001			
P06/TI011/TO01			
P10/SCK10/TxD0			
P11/SI10/RxD0			
P12/SO10	5-AG		
P13/TxD6 ^{Note 1}			
P14/RxD6 ^{Note 1}	5-AH		
P15/TOH0	5-AG		
P16/TOH1/INTP5	5-AH		
P17/TI50/TO50			
P20/ANI0 to P25/ANI5 ^{Note 2}	11-G		<Analog setting> Connect to AV_{REF} or AV_{SS} . <Digital setting> Input: Connect independently to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P30/INTP1 to P32/INTP3	5-AH		Input: Connect independently to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P33/TI51/TO51/INTP4			
P60/SCL0	13-AD		Input: Connect to V_{SS} . Output: Leave this pin open at low-level output after clearing the output latch of the port to 0.
P61/SDA0			
P70/KR0	5-AH		Input: Connect independently to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P120/INTP0/EXLVI			
P121/X1 ^{Note 3}	37		Input: Connect independently to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P122/X2/EXCLK ^{Note 3}			
RESET	2	Input	–
FLMD0	38	–	Connect to V_{SS} .
AV_{REF}	–	–	Connect directly to V_{DD} ^{Note 4} .
AV_{SS}	–	–	Connect directly to V_{SS} .

- Notes 1.** This pin has alternate functions as UART pin of the microcontroller or as LIN transceiver function pin. When this pin is used as the LIN transceiver function pin, leave it open. When it is used as microcontroller function pin, the UMODE pin must be externally pulled to V_{DD} with a resistor.
- 2.** P20/ANI0 to P25/ANI5 are in the analog input mode after reset release.
- 3.** Use the recommended connection method described above in I/O port mode when these pins are not used.
- 4.** Use the same potential as the V_{DD} pin when port 2 is used as a digital port.

Table 2-3. Pin I/O Circuit Types (2/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
Dr1	LIN1	Output	Leave open.
Dr21	LIN2		
Dr22			
Dr3	LIN1		
Dr4	LIN3		
Dr1_I	LIN5	Input	Leave open.
Dr21_I	LIN6		
Dr22_I			
Dr3_I	LIN5		
Dr4_I			
SWO	LIN8	Output	Leave open
LIN	LIN9	I/O	
MSLP	LIN5	Input	
SWI	LIN7	Input	Connect directly to GND1, GND2, GND3
UMODE	LIN5	Input	Leave open.
VIC	LIN10	Input	Connect directly to SUP
VRO		Output	Connect directly to V _{DD}
IC	–	–	Leave open.
RxL	LIN11	Output	<small>__Note 1</small>
TxL	LIN12	Input	<small>__Note 2</small>
N.C	–	–	Connect directly to GND

Notes 1. RxL terminal is connected with P14/RxD6 in package.

2. TxL terminal is connected with P13/TxD6 in package.

Figure 2-1. Pin I/O Circuit List (1/4)

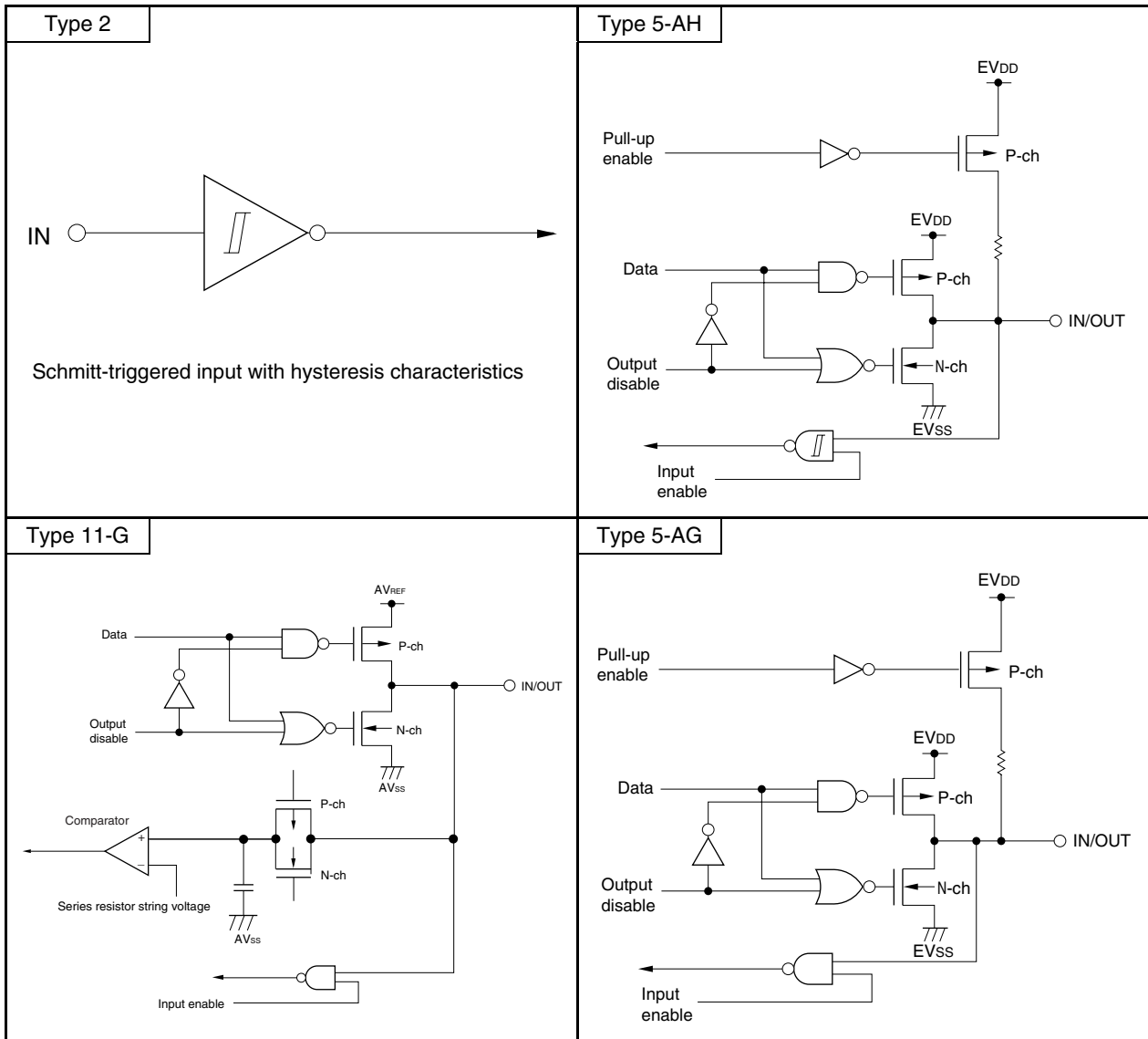


Figure 2-1. Pin I/O Circuit List (2/4)

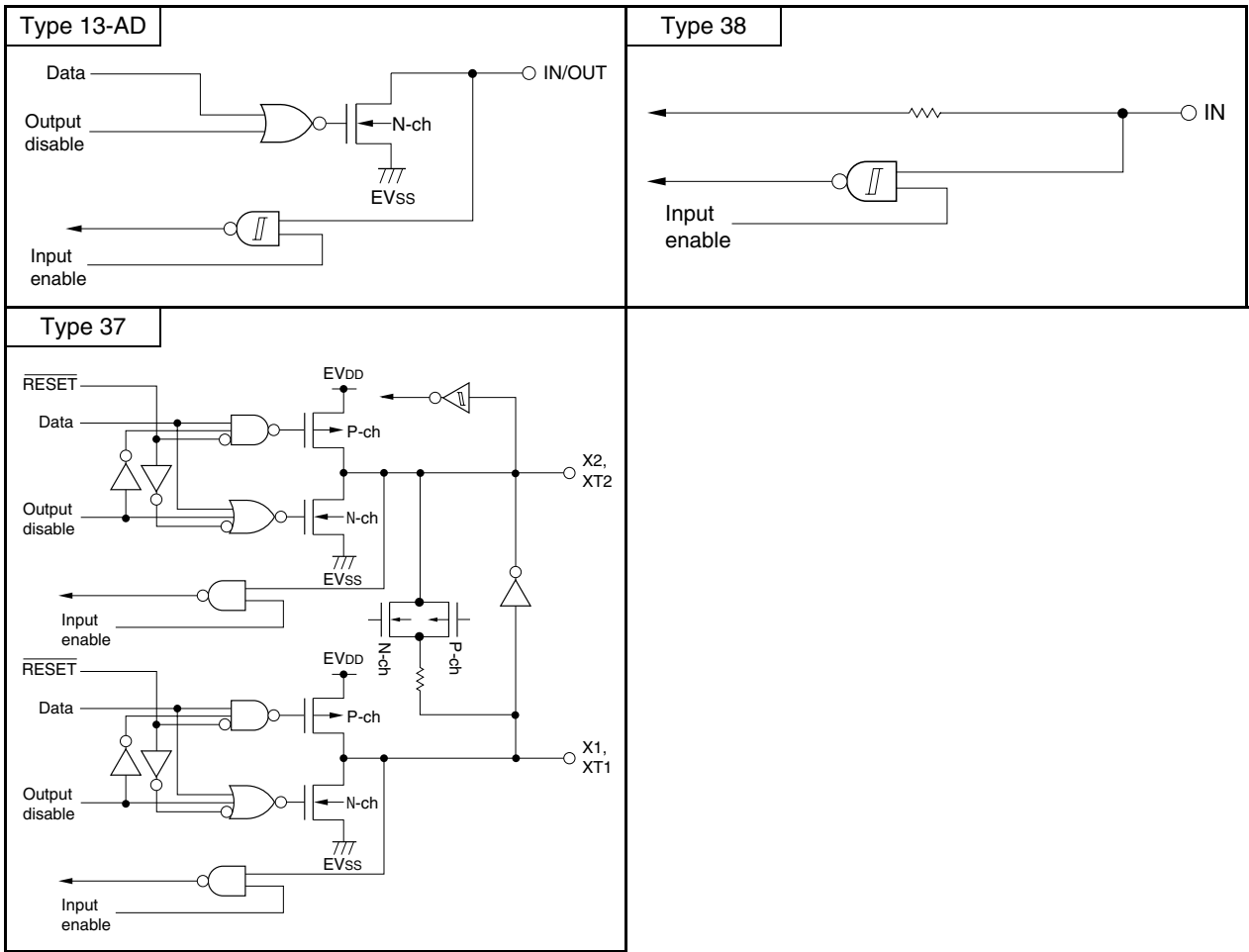


Figure 2-1. Pin I/O Circuit List (3/4)

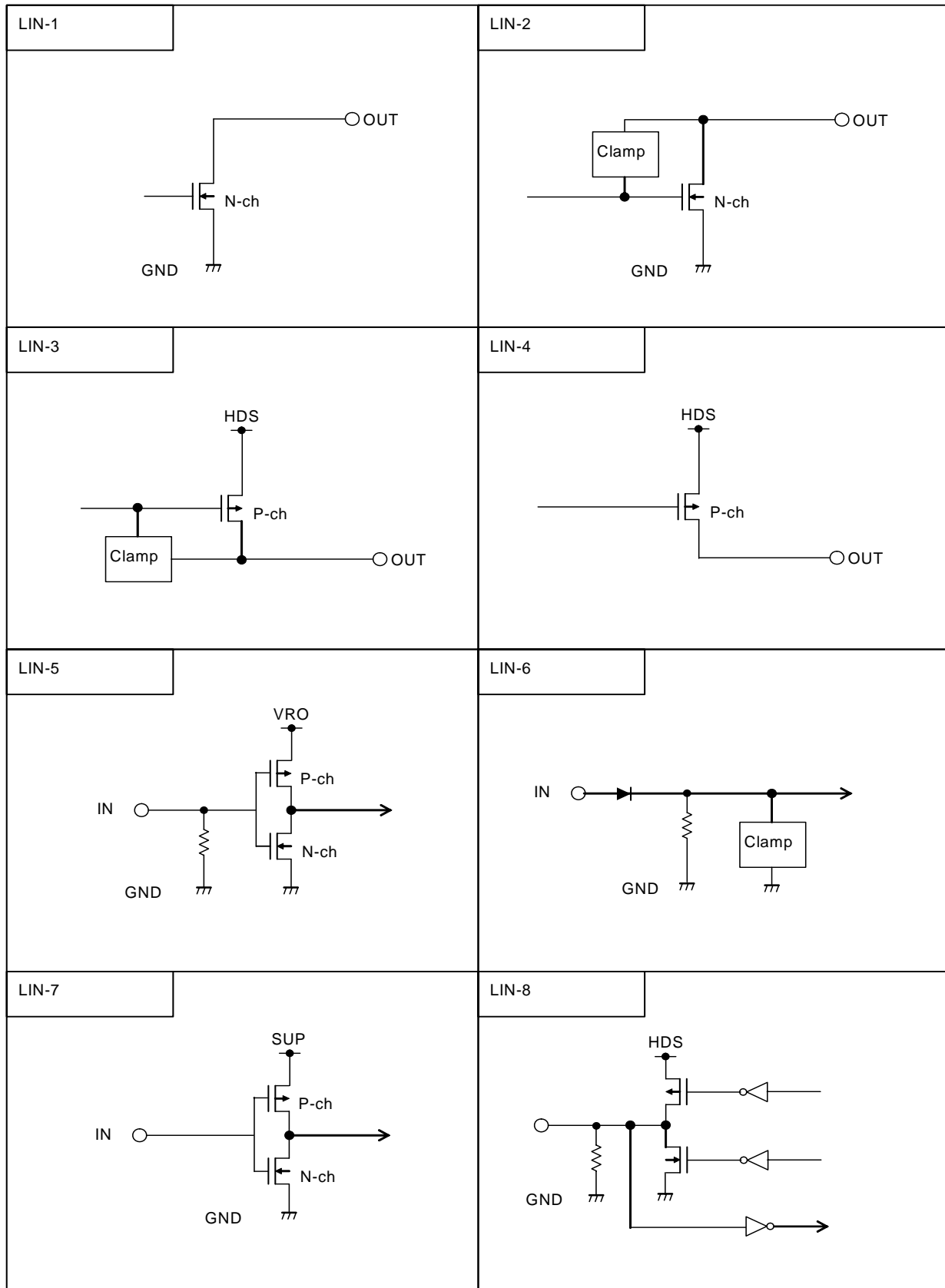
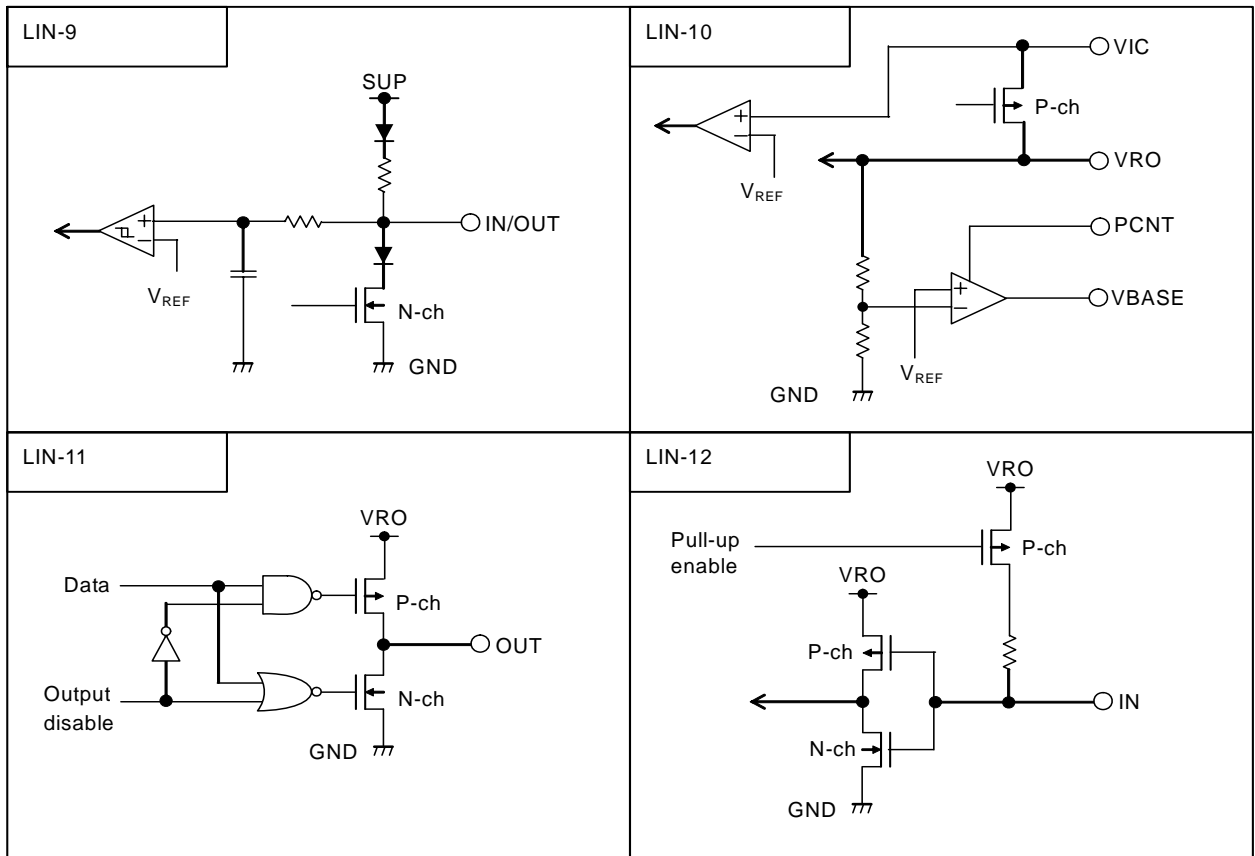


Figure 2-1. Pin I/O Circuit List (4/4)



CHAPTER 3 MICROCONTROLLER FUNCTIONS

The 8-bit microcontroller is same as 78K0/KE2. The supported functions of the μ PD78F8017A, 78F8018A, 78F8019A, 78F8020A and 78F8020DA are different from 78K0/KE2, because the μ PD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA do not support 78K0/KE2 all function pins.

This manual describes the differences of this device function and 78K0/KE2.

See each function of microcontroller parts in **78K0/Kx2 User's Manual (U18598E)**.

3.1 Differences between This Micro's Functions and 78K0/KE2

The differences between the μ PD78F8017A, 78F8018A, 78F8019A, 78F8020A and 78F8020DA function and 78K0/KE2 are as follows.

Item	μ PD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA	78K0/KE2 μ PD78F0534A, 78F0535A, 78F0536A, 78F0537A, 78F0537DA	
Subsystem clock	–	XT1 (crystal) oscillation External subsystem clock input (EXCLK) 32.768 kHz (TYP.) : $V_{DD} = 1.8$ to 5.5 V	
I/O port	<u>Total: 28</u> CMOS I/O: 26 N-ch open-drain I/O (tolerance): 2	<u>Total: 55</u> CMOS I/O: 50 CMOS output: 1 N-ch open-drain I/O (tolerance): 4	
Clock out	–	• 156.25 kHz, 312.5 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (peripheral hardware clock: $f_{PRS} = 20$ MHz operation) • 32.768 kHz (subsystem clock: $f_{SUB} = 32.768$ kHz operation)	
Buzzer output	–	2.44 kHz, 4.88 kHz, 9.77 kHz, 19.54 kHz (peripheral hardware clock: $f_{PRS} = 20$ MHz operation)	
A/D converter	10-bit resolution x 6 channels ($A_{VREF} = 2.3$ to 5.5 V)	10-bit resolution x 8 channels ($A_{VREF} = 2.3$ to 5.5 V)	
Serial interface	<ul style="list-style-type: none"> • UART mode supporting LIN-bus: 1 channel • 3-wire serial I/O mode/URAT: 1 channel • I²C bus: 1 channel 	<ul style="list-style-type: none"> • UART mode supporting LIN-bus: 1 channel • 3-wire serial I/O mode/URAT: 1 channel • 3-wire serial I/O mode: 1 channel • I²C bus: 1 channel 	
Vectored interrupt sources	Internal	18	19
	External	7	9
Key interrupt	Key interrupt (INTKR) occurs by detecting falling edge of key input pins (KR0).	Key interrupt (INTKR) occurs by detecting falling edge of key input pins (KR0 to KR7).	

3.2 Differences between the Special Function Registers and 78K0/KE2

The differences between the μ PD78F8017A, 78F8018A, 78F8019A, 78F8020A and 78F8020DA special function register and 78K0/KE2 are as follows.

(1/2)

Address	μ PD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA		78K0/KE2 μ PD78F0534A, 78F0535A, 78F0536A, 78F0537A, 78F0537DA	
	Special Function Register (SFR) Name	Symbol	Special Function Register (SFR) Name	Symbol
FF00H	Port register 0 ^{Note 1}	P0	Port register 0	P0
FF02H	Port register 2 ^{Note 1}	P2	Port register 2	P2
FF04H	_Note 2	–	Port register 4	P4
FF05H	_Note 2	–	Port register 5	P5
FF06H	Port register 6 ^{Note 1}	P6	Port register 6	P6
FF07H	Port register 7 ^{Note 1}	P7	Port register 7	P7
FF0CH	Port register 12 ^{Note 1}	P12	Port register 12	P12
FF0DH	_Note 2	–	Port register 13	P13
FF0EH	_Note 2	–	Port register 14	P14
FF20H	Port mode register 0 ^{Note 1}	PM0	Port mode register 0	PM0
FF22H	Port mode register 2 ^{Note 1}	PM2	Port mode register 2	PM2
FF24H	_Note 2	–	Port mode register 4	PM4
FF25H	_Note 2	–	Port mode register 5	PM5
FF26H	Port mode register 6 ^{Note 1}	PM6	Port mode register 6	PM6
FF27H	Port mode register 7 ^{Note 1}	PM7	Port mode register 7	PM7
FF29H	Analog input channel specification register ^{Note 1}	ADS	Analog input channel specification register	ADS
FF2CH	Port mode register 12 ^{Note 1}	PM12	Port mode register12	PM12
FF2EH	Port mode register 14 ^{Note 2}	PM14	Port mode register14	PM14
FF2FH	A/D port configuration register ^{Note 1}	ADPC	A/D port configuration register	ADPC
FF30H	Pull-up resistor option register0 ^{Note 1}	PU0	Pull-up resistor option register0	PU0
FF34H	_Note 2	–	Pull-up resistor option register4	PU4
FF35H	_Note 2	–	Pull-up resistor option register5	PU5
FF37H	Pull-up resistor option register7 ^{Note 1}	PU7	Pull-up resistor option register7	PU7
FF3EH	_Note 2	–	Pull-up resistor option register14	PU14
FF40H	_Note 2	–	Clock output selection register	CKS
FF48H	External interrupt rising edge enable register ^{Note 1}	EGP	External interrupt rising edge enable register	EGP
FF49H	External interrupt falling edge enable register ^{Note 1}	EGN	External interrupt falling edge enable register	EGN
FF4AH	_Note 2	–	Serial I/O shift register 11	SIO11
FF4CH	_Note 2	–	Transmit buffer register 11	SOTB11
FF6EH	Key return mode register ^{Note 1}	KRM	Key return mode register	KRM
FF6FH	Watch timer operation mode register ^{Note 1}	WTM	Watch timer operation mode register	WTM

Notes 1. Different in bit setting.

2. Be sure not to write this register.

(2/2)

Address	μ PD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA		78K0/KE2 μ PD78F0534A, 78F0535A, 78F0536A, 78F0537A, 78F0537DA			
	Special Function Register (SFR) Name	Symbol	Special Function Register (SFR) Name	Symbol		
FF88H	– ^{Note 1}	–	Serial operation mode register 11	CSIM11		
FF89H	– ^{Note 1}	–	Serial clock selection register 11	CSIC11		
FF9FH	Clock operation mode selection register ^{Note 2}	OSCCTL	Clock operation mode selection register	OSCCTL		
FFA8H	IIC clock selection register 0 ^{Note 2}	IICCL0	IIC clock selection register 0	IICCL0		
FFE2H	Interrupt request flag register 1L ^{Note 2}	IF1	IF1L	Interrupt request flag register 1L	IF1	IF1L
FFE3H	Interrupt request flag register 1H ^{Note 2}		IF1H	Interrupt request flag register 1H		IF1H
FFE6H	Interrupt request flag register 1L ^{Note 2}	MK1	MK1L	Interrupt request flag register 1L	MK1	MK1L
FFE7H	Interrupt request flag register 1H ^{Note 2}		MK1H	Interrupt request flag register 1H		MK1H
FFEAH	Priority specification flag register 1L ^{Note 2}	PR1	PR1L	Priority specification flag register 1L	PR1	PR1L
FFEBH	Priority specification flag register 1H ^{Note 2}		PR1H	Priority specification flag register 1H		PR1H
FFFBH	Processor clock control register ^{Note 2}	PCC	Processor clock control register	PCC		

- Notes**
1. Be sure not to write this register.
 2. Different in bit setting.

3.3 Differences in Register Bit Setting from 78K0/KE2

3.3.1 Port mode register

μPD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA

Symbol	7	6	5	4	3	2	1	0	address	After reset	R/W
PM0	1	PM06	PM05	1	1	1	PM01	PM00	FF20H	FFH	R/W
PM2	1	1	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W
PM6	1	1	1	1	1	1	PM61	PM60	FF26H	FFH	R/W
PM7	1	1	1	1	1	1	1	PM70	FF27H	FFH	R/W
PM12	1	1	1	1	1	PM122	PM121	PM120	FF2CH	FFH	R/W

- Cautions**
1. Be sure to set '1' on PM0 bit 2 to 4.
 2. Be sure to set '1' on PM2 bit 6 to 7.
 3. Be sure to set '1' on PM6 bit 2 to 3.
 4. Be sure to set '1' on PM7 bit 1 to 7.
 5. Be sure to set '1' on PM12 bit 3 to 4.

78K0/KE2

Symbol	7	6	5	4	3	2	1	0	address	After reset	R/W
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00	FF20H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W
PM6	1	1	1	1	PM63	PM62	PM61	PM60	FF26H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FF27H	FFH	R/W
PM12	1	1	1	PM124	PM123	PM122	PM121	PM120	FF2CH	FFH	R/W

3.3.2 Port register

μPD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA

Symbol	7	6	5	4	3	2	1	0	address	After reset	R/W
P0	0	P06	P05	0	0	0	P01	P00	FF00H	00H (output latch)	R/W
P2	0	0	P25	P24	P23	P22	P21	P20	FF02H	00H (output latch)	R/W
P6	0	0	0	0	0	0	P61	P60	FF06H	00H (output latch)	R/W
P7	0	0	0	0	0	0	0	P70	FF07H	00H (output latch)	R/W
P12	0	0	0	0	0	P122	P121	P120	FF0CH	00H (output latch)	R/W

78K0/KE2

Symbol	7	6	5	4	3	2	1	0	address	After reset	R/W
P0	0	P06	P05	P04	P03	P02	P01	P00	FF00H	00H (output latch)	R/W
P2	P27	P26	P25	P24	P23	P22	P21	P20	FF02H	00H (output latch)	R/W
P6	0	0	0	0	P63	P62	P61	P60	FF06H	00H (output latch)	R/W
P7	P77	P76	P75	P74	P73	P72	P71	P70	FF07H	00H (output latch)	R/W
P12	0	0	0	P124	P123	P122	P121	P120	FF0CH	00H (output latch)	R/W

3.3.3 Pull-up resistor option register

μPD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA

Symbol	7	6	5	4	3	2	1	0	address	After reset	R/W
PU0	0	PU06	PU05	0	0	0	PU01	PU00	FF30H	00H	R/W
PU7	0	0	0	0	0	0	0	PU70	FF37H	00H	R/W

- Cautions**
1. Be sure to clear '0' on PU7 bit 2 to 4.
 2. Be sure to clear '0' on PU7 bit 1 to 7.

78K0/KE2

Symbol	7	6	5	4	3	2	1	0	address	After reset	R/W
PU0	0	PU06	PU05	PU04	PU03	PU02	PU01	PU00	FF30H	00H	R/W
PU7	PU77	PU76	PU75	PU74	PU73	PU72	PU71	PU70	FF37H	00H	R/W

3.3.4 Analog input channel specification register

μPD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA

Address: FF29H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	0	0	0	0	0	ADS2	ADS1	ADS0

ADS2	ADS1	ADS0	Analog input channel specification
0	0	0	ANI0
0	0	1	ANI1
0	1	0	ANI2
0	1	1	ANI3
1	0	0	ANI4
1	0	1	ANI5
1	1	0	Setting prohibited
1	1	1	Setting prohibited

Caution Be sure to clear '0' on bit 3 to 7.

78K0/KE2

address: FF29H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	0	0	0	0	0	ADS2	ADS1	ADS0

ADS2	ADS1	ADS0	Analog input channel specification
0	0	0	ANI0
0	0	1	ANI1
0	1	0	ANI2
0	1	1	ANI3
1	0	0	ANI4
1	0	1	ANI5
1	1	0	ANI6
1	1	1	ANI7

Caution Be sure to clear '0' on bit 3 to 7.

3.3.5 A/D port configuration register

μPD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA

address: FF2FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	0	0	ADPC2	ADPC1	ADPC0

ADPC2	ADPC1	ADPC0	Analog input(A) / Digital I/O (D) switching					
			ANI5/ P25	ANI4/ P24	ANI3/ P23	ANI2/ P22	ANI1/ P21	ANI0/ P20
0	0	0	A	A	A	A	A	A
0	0	1	A	A	A	A	A	D
0	1	0	A	A	A	A	D	D
0	1	1	A	A	A	D	D	D
1	0	0	A	A	D	D	D	D
1	0	1	A	D	D	D	D	D
1	1	0	D	D	D	D	D	D
Other than above			Setting prohibited					

Caution Be sure to clear '0' on bit 3.

78K0/KE2

address: FF2FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	0	ADPC3	ADPC2	ADPC1	ADPC0

ADPC3	ADPC2	ADPC1	ADPC0	Analog input(A) / Digital I/O (D) switching							
				ANI7/ P27	ANI6/ P26	ANI5/ P25	ANI4/ P24	ANI3/ P23	ANI2/ P22	ANI1/ P21	ANI0/ P20
0	0	0	0	A	A	A	A	A	A	A	A
0	0	0	1	A	A	A	A	A	A	A	D
0	0	1	0	A	A	A	A	A	A	D	D
0	0	1	1	A	A	A	A	A	D	D	D
0	1	0	0	A	A	A	A	D	D	D	D
0	1	0	1	A	A	A	D	D	D	D	D
0	1	1	0	A	A	D	D	D	D	D	D
0	1	1	1	A	D	D	D	D	D	D	D
1	0	0	0	D	D	D	D	D	D	D	D
Other than above				Setting prohibited							

3.3.6 External interrupt rising edge enable register

μPD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA

address: FF48H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP	0	0	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0

address: FF49H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN	0	0	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0

Caution Be sure to clear '0' on bit 6 to 7.

78K0/KE2

address: FF48H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP	EGP7	EGP6	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0

address: FF49H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN	EGN7	EGN6	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0

3.3.7 Key return mode register

μPD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA

address: FF6EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM	0	0	0	0	0	0	0	KRM0

Caution Be sure to clear '0' on bit 1 to 7.

78K0/KE2

address: FF6EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM	KRM7	KRM6	KRM5	KRM4	KRM3	KRM2	KRM1	KRM0

3.3.8 Watch timer operation mode register

μPD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA

address: FF6FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
WTM	0	WTM6	WTM5	WTM4	WTM3	WTM2	WTM1	WTM0

Caution Bit 7 must always be set to '0'. It is read-only.

78K0/KE2

address: FF6FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
WTM	WTM7	WTM6	WTM5	WTM4	WTM3	WTM2	WTM1	WTM0

WTM7	Watch timer count clock selection (fw)					
		f _{SUB} = 32.768 kHz	f _{PRS} = 2 MHz	f _{PRS} = 5 MHz	f _{PRS} = 10 MHz	f _{PRS} = 20 MHz
0	f _{PRS} /2 ⁷	–	15.625 kHz	39.062 kHz	78.125 kHz	156.25 kHz
1	f _{SUB}	32.768 kHz	–			

- Remarks**
1. fw: Watch timer clock frequency (f_{PRS}/2⁷ or f_{SUB})
 2. f_{PRS}: Peripheral hardware clock frequency
 3. f_{SUB}: Subsystem clock frequency

3.3.9 Clock operation mode select register

μPD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA

address: FF9FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
OSCCTL	EXCLK	OSCSEL	0	0	0	0	0	AMPH

Caution Be sure to clear '0' on bit 4 to 5.

78K0/KE2

address: FF9FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
OSCCTL	EXCLK	OSCSEL	EXCLKS	OSCSELS	0	0	0	AMPH

3.3.10 Processor clock control register

μPD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA

address: FFFBH After reset: 01H R/W

Symbol	7	6	5	4	3	2	1	0
PCC	0	0	0	0	0	PCC2	PCC1	PCC0

- Cautions**
1. Bit 5 is read-only.
 2. Be sure to clear '0' on bit 4 and bit 6.

78K0/KE2

address: FFFBH After reset: 01H R/W

Symbol	7	6	5	4	3	2	1	0
PCC	0	XTSTART	CLS	CSS	0	PCC2	PCC1	PCC0

Caution Bit 5 is read-only.

3.3.11 IIC clock selection register 0

μPD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA

address: FFA8H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IICCL0	0	0	CLD0	DAD0	SMC0	DFC0	CL01	CL00

Selection Clock Setting

IICX0	IICCL0			Selection Clock (fw)	Transfer Clock (fw/m)	Settable Selection Clock (fw) Range	Operation Mode
Bit 0	Bit 3	Bit 1	Bit 0				
CLX0	SMC0	CL01	CL00				
0	0	0	0	f _{PRS} /2	fw/44	2.00 MHz to 4.19 MHz	Normal mode (SMC0 bit = 0)
0	0	0	1	f _{PRS} /2	fw/86	4.19 MHz to 8.38 MHz	
0	0	1	0	f _{PRS} /4	fw/86		
0	0	1	1	Setting prohibited			
0	1	0	X	f _{PRS} /2	fw/24	4.00 MHz to 8.38 MHz	High-speed mode (SMC0 bit = 1)
0	1	1	0	f _{PRS} /4	fw/24		
0	1	1	1	Setting prohibited			
1	0	x	X	Setting prohibited			
1	1	0	X	f _{PRS} /2	fw/12	4.00 MHz to 4.19 MHz	High-speed mode (SMC0 bit = 1)
1	1	1	0	f _{PRS} /4	fw/12		
1	1	1	1	Setting prohibited			

78K0/KE2

address: FFA8H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IICCL0	0	0	CLD0	DAD0	SMC0	DFC0	CL01	CL00

Selection Clock Setting

IICX0	IICCL0			Selection Clock (fw)	Transfer Clock (fw/m)	Settable Selection Clock (fw) Range	Operation Mode
Bit 0	Bit 3	Bit 1	Bit 0				
CLX0	SMC0	CL01	CL00				
0	0	0	0	f _{PRS} /2	fw/44	2.00 to 4.19 MHz	Normal mode (SMC0 bit = 0)
0	0	0	1	f _{PRS} /2	fw/86	4.19 to 8.38 MHz	
0	0	1	0	f _{PRS} /4	fw/86		
0	0	1	1	f _{EXSCL0}	fw/66	6.4 MHz	
0	1	0	x	f _{PRS} /2	fw/24	4.00 to 8.38 MHz	High-speed mode (SMC0 bit = 1)
0	1	1	0	f _{PRS} /4	fw/24		
0	1	1	1	f _{EXSCL0}	fw/18	6.4 MHz	
1	0	x	x	Setting prohibited			
1	1	0	x	f _{PRS} /2	fw/12	4.00 to 4.19 MHz	High-speed mode (SMC0 bit = 1)
1	1	1	0	f _{PRS} /4	fw/12		
1	1	1	1	Setting prohibited			

- Remarks**
1. x: Don't care
 2. f_{PRS}: Peripheral hardware clock frequency
 3. f_{EXSCL0}: External clock frequency from EXSCL0 pin

3.3.12 Interrupt request flag register

μPD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA

address: FFE2H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IF1L	0	0	WTIF	KRIF	TMIF51	WTIIF	SRIF0	ADIF

address: FFE3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IF1H	0	0	0	0	TMIF011	TMIF001	0	IICIF0 DMUIF

- Cautions**
1. Be sure to clear '0' on IF1H bit 1 and, bit 4 to 7.
 2. Be sure to clear '0' on IF1L bit 6 to 7.

78K0/KE2

address: FFE2H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IF1L	PIF7	PIF6	WTIF	KRIF	TMIF51	WTIIF	SRIF0	ADIF

address: FFE3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IF1H	0	0	0	0	TMIF011	TMIF001	CSIF11	IICIF0 DMUIF

- Caution** Be sure to clear '0' on IF1H bit 1 and, bit 4 to 7.

3.3.13 Interrupt mask flag register

μPD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA

address: FFE6H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
MK1L	1	1	WTMK	KRMK	TMMK51	WTIMK	SRMK0	ADMK

address: FFE7H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
MK1H	1	1	1	1	TMMK011	TMMK001	1	IICMK0 DMUMK

- Cautions**
1. Be sure to clear '0' on MK1H bit 1 and bit 4 to 7.
 2. Be sure to clear '0' on MK1L bit 6 to 7.

78K0/KE2

address: FFE6H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
MK1L	PMK7	PMK6	WTMK	KRMK	TMMK51	WTIMK	SRMK0	ADMK

address: FFE7H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
MK1H	1	1	1	1	TMMK011	TMMK001	CSIMK11	IICMK0 DMUMK

- Caution** Be sure to clear '0' on MK1H bit 1 and bit 4 to 7.

3.3.14 Priority specification flag register

μPD78F8017A, 78F8018A, 78F8019A, 78F8020A, 78F8020DA

address: FFEAH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PR1L	1	1	WTPR	KRPR	TMPR51	WTIPR	SRPR0	ADPR

address: FFE BH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PR1H	1	1	1	1	TMPR011	TMPR001	1	IICPR0 DMUPR

- Cautions**
1. Be sure to clear '0' on PR1H bit 1 and bit 4 to 7.
 2. Be sure to clear '0' on PR1L bit 6 to 7.

78K0/KE2

address: FFEAH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PR1L	PPR7	PPR6	WTPR	KRPR	TMPR51	WTIPR	SRPR0	ADPR

address: FFE BH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PR1H	1	1	1	1	TMPR011	TMPR001	CSIPR11	IICPR0 DMUPR

- Caution** Be sure to set '1' PR1H bit 1 and bit 4 to 7.

CHAPTER 4 WRITING WITH FLASH PROGRAMMER

Data can be written to the flash memory on-board or off-board, by using a dedicated flash programmer.

(1) On-board programming

The contents of the flash memory can be rewritten after the device has been mounted on the target system. The connectors that connect the dedicated flash programmer must be mounted on the target system.

(2) Off-board programming

Data can be written to the flash memory with a dedicated program adapter (FA series) before the device is mounted on the target system.

Remark The FA series is a product of Naito Densai Machida Mfg. Co., Ltd.

Table 4-1. Wiring Dedicated Flash Programmer

Pin Configuration of Dedicated Flash Programmer			With CSI10		With UART6	
Signal Name	I/O	Pin Function	Pin Name	Pin No.	Pin Name	Pin No.
SI/RxD	Input	Receive signal	SO10/P12	53	TxD6/P13	23
SO/TxD	Output	Transmit signal	SI10/RxD0/P11	54	RxD6/P14	22
SCK	Output	Transfer clock	SCK10/TxD0/P10	55	–	–
CLK	Output	Clock to Micro	– <small>Note 1</small>	–	Note 2	Note 2
/RESET	Output	Reset signal	RESET	3	RESET	3
FLMD0	Output	Mode signal	FLMD0	4	FLMD0	4
V _{DD}	I/O	V _{DD} voltage generation/ power monitoring	V _{DD}	9	V _{DD}	9
			AV _{REF}	56	AV _{REF}	56
			SUP	31	SUP	31
			HDS	30	HDS	30
			VIC	29	VIC	29
			VRO	28	VRO	28
			–	–	UMODE	25
V _{SS}	–	GND	V _{SS}	8	V _{SS}	8
			AV _{SS}	57	AV _{SS}	57
			GND1	33	GND1	33
			GND2	48	GND2	48
			GND3	42	GND3	42
			SWI	47	SWI	47

Notes 1. Only the internal high-speed oscillation clock (f_{RH}) can be used when CSI10 is used.

2. Only the X1 clock (f_x) or external main system clock (f_{EXCLK}) can be used when UART6 is used. When using the clock out of the flash programmer, connect CLK and EXCLK of the programmer.

- PG-FP5, FL-PR5, PG-FP4, FL-PR4: Please connect the programmer's CLK to EXCLK/X2/P122 (pin 5)

CHAPTER 5 POWER SUPPLY CIRCUIT

5.1 Power Supply Function

The power supply circuit is a stabilization power supply circuit that generates 5 V (typ.) output voltage from 12 V battery supply voltage.

The power supply circuit has the following function.

- Over current protection function
- Thermal shutdown function

5.2 Power Supply Over Current Protection Function

This circuit protects the dropper by limiting the current if an over current occurs in the power supply line due to a cause such as a load short.

The over current is detected using the potential difference between the SUP pin and VIC pin when the resistor ROCD is connected between both pins. The external resistance ROCD has to be adjusted according to the user system.

The resistor needs to be dimensioned that the maximum current is less than 65 mA between the SUP pin and VIC pin.

$$\text{Current limit} = \text{Over current detect voltage } (V_{\text{SUPlim}}) / R_{\text{OCD}}$$

$$\text{Over current detect voltage } (V_{\text{SUPlim}}) = V_{\text{SUP}} - V_{\text{IC}}$$

$$V_{\text{SUPlim}} = 150 \text{ mV (typ.)}$$

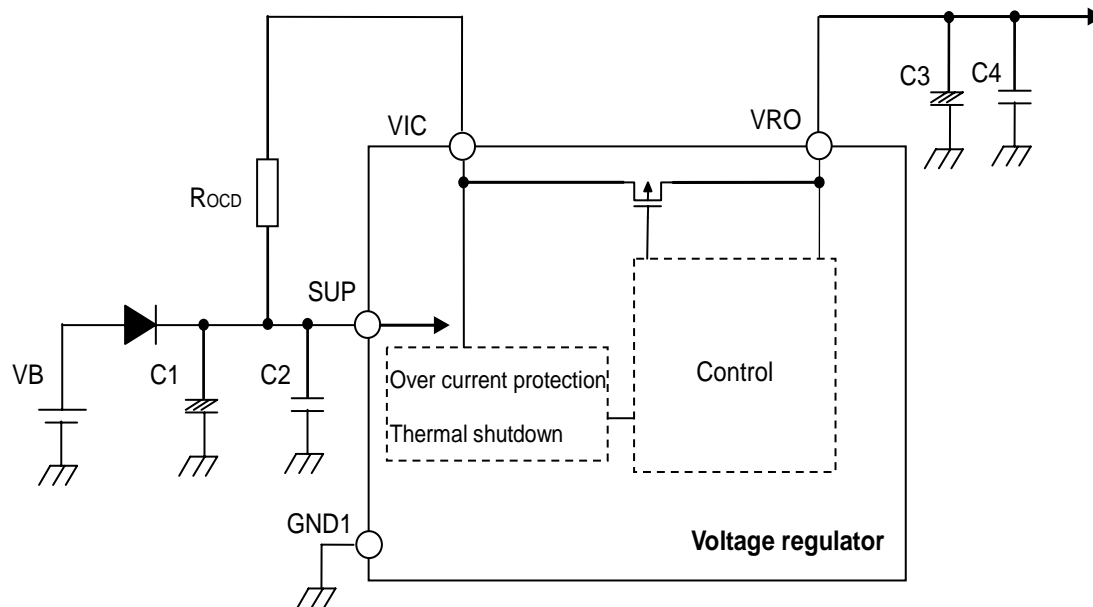
5.3 Power Supply Thermal Shutdown Function

This is a protection circuit for preventing destruction because of over temperature.

The temperature of the internal circuit is monitored and when the temperature exceeds the maximum limit the overheating detection temperature is detected and the internal P-ch MOS is forcibly switched off. After the dropper is forcibly switched off, it automatically switches back on after the temperature declines.

Caution The purpose of the built-in protection functions is to protect the device from abnormal operation. Try to avoid the use of these functions by designing the system properly.

Figure 5-1. Voltage Regulator Circuit Application Example



External parts target

$$C1 \geq 33 \mu\text{F}$$

$$C2 \geq 0.01 \mu\text{F}$$

$$4.7 \mu\text{F} \leq C3 \leq 100 \mu\text{F}$$

$$C4 \geq 0.01 \mu\text{F}$$

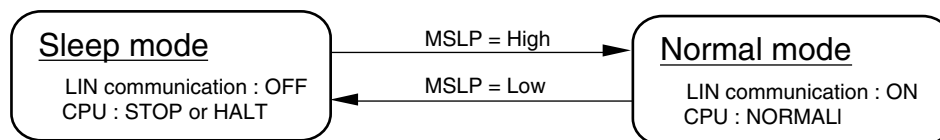
Caution Place the ceramic capacitor (C2, C4) between the SUP and GND pin, the VRO and GND pins adjacent to the SUP, VRO pin and use the shortest possible wiring.

6.2 Operation Mode

(1) UMODE = Low (LIN transceiver in operation mode)

The LIN transceiver has the following two modes.

Figure 6-2. Mode Transition Diagram



- Sleep mode

When MSLP becomes low, the sleep mode is entered.

In the sleep mode, the LIN driver output becomes OFF (recessive) regardless of the Tx pin input state.

To reduce the current consumption, set the microcontroller's operation mode either to HALT or STOP mode.

- Normal mode

When MSLP becomes high, the normal mode is entered. In the normal mode, the Tx input data can be output to the LIN bus.

Cautions 1. When using the LIN transceiver function, leave the UMODE pin open.

(The UMODE pin is pulled down within the IC.)

2. **When not using the LIN transceiver function, directly connect the UMODE pin to V_{DD} and set it to high level. When the UMODE pin is set to high level, the pull-up resistor of the LIN transceiver circuit (R_{Tx}) becomes unconnected.**

3. **The MSLP pin is pulled down within the IC.**

(2) UMODE = High (LIN transceiver not in operation mode)

Unconditionally, LIN communication is OFF.

TxL and RxL are High impedance.

LIN terminal (N-ch open drain output) is OFF.

6.3 Over Current Limiter

The over current limiter prevents the destruction of the device caused by over current during a load short.

When a current occurs that exceeds the over current detection value flows to the LIN driver due to a load short, etc., the output current is limited by inhibiting the gate voltage of the LIN driver.

6.4 Thermal Shutdown Circuit

This is a protection circuit for preventing destruction of the device due to over temperature.

The temperature of the LIN driver is monitored and when a temperature that exceeds the overheating detection temperature (MIN: 150°C) is detected, the LIN driver is forcibly switched off. After the LIN driver is forcibly switched off, it automatically switches back on after the temperature declines.

Caution The purpose of the built-in protection functions is to protect the device from abnormal operation. Try to avoid the use of these functions by designing the system properly.

CHAPTER 7 DRIVER CIRCUIT

The driver circuit has 4 channels of a low side driver and 1 channels of a high side driver circuit.

7.1 Low Side Driver

- **Dr1: 1 ch**

Application: Pre driver for high side driver

The driver control input signal pin is Dr1_I. This pin has a pull-down resistor within the IC.

- **Dr2: 2 ch**

Application: Relay driver

The driver control input signal pins are Dr21_I and Dr22_I. This pin has a pull-down resistor and clamp circuit within the IC.

As driver input of Dr21_I and Dr22_I can either the 5V signal or the battery voltage signal either be used. When the battery voltage is input to Dr21_I and Dr22_I the system needs an external resistor. For details, please refer to the application example.

The drivers Dr21 and Dr22 have a dynamic clamp circuit for high voltage protection. The dynamic clamp circuit does not operate when the supply voltage V_{SUP} is more than 28 V.

- **Dr3: 1 ch**

Application: LED driver

The driver control input signal pin is Dr3_I. This pin has a pull-down resistor within the IC.

7.2 High Side Driver

- **Dr4: 1 ch**

Application: Hall sensor power supply driver

The driver control input signal pin is Dr4_I. This pin has a pull-down resistor within the IC.

The driver Dr4 has an output voltage clump function, an over current protection and a thermal shutdown function.

The over current limiter prevents destruction of the driver caused by an over current during a load short. When a current that exceeds the over current detection value flows to the Dr4 due to a load short, etc. the output current is limited by inhibiting the gate voltage of Dr4.

The temperature of the Dr4 is monitored and when a temperature that exceeds the overheating detection temperature (MIN: 150°C) is detected, the Dr4 is forcibly switched off.

After the Dr4 is forcibly switched off, it automatically switches back on after the temperature declines.

Caution The purpose of the built-in protection functions is to protect the device from abnormal operation.

Try to avoid the use of these functions by designing the system properly.

Table 7-1. Truth Table

Input		Dr1	Dr21	Dr22	Dr3	Dr4
Dr1_I	High	ON	-	-	-	-
	Low	OFF	-	-	-	-
Dr21_I	High	-	ON	-	-	-
	Low	-	OFF	-	-	-
Dr22_I	High	-	-	ON	-	-
	Low	-	-	OFF	-	-
Dr3_I	High	-	-	-	ON	-
	Low	-	-	-	OFF	-
Dr4_I	High	-	-	-	-	ON
	Low	-	-	-	-	OFF

Figure 7-1. Low Side Driver Circuit Application Example

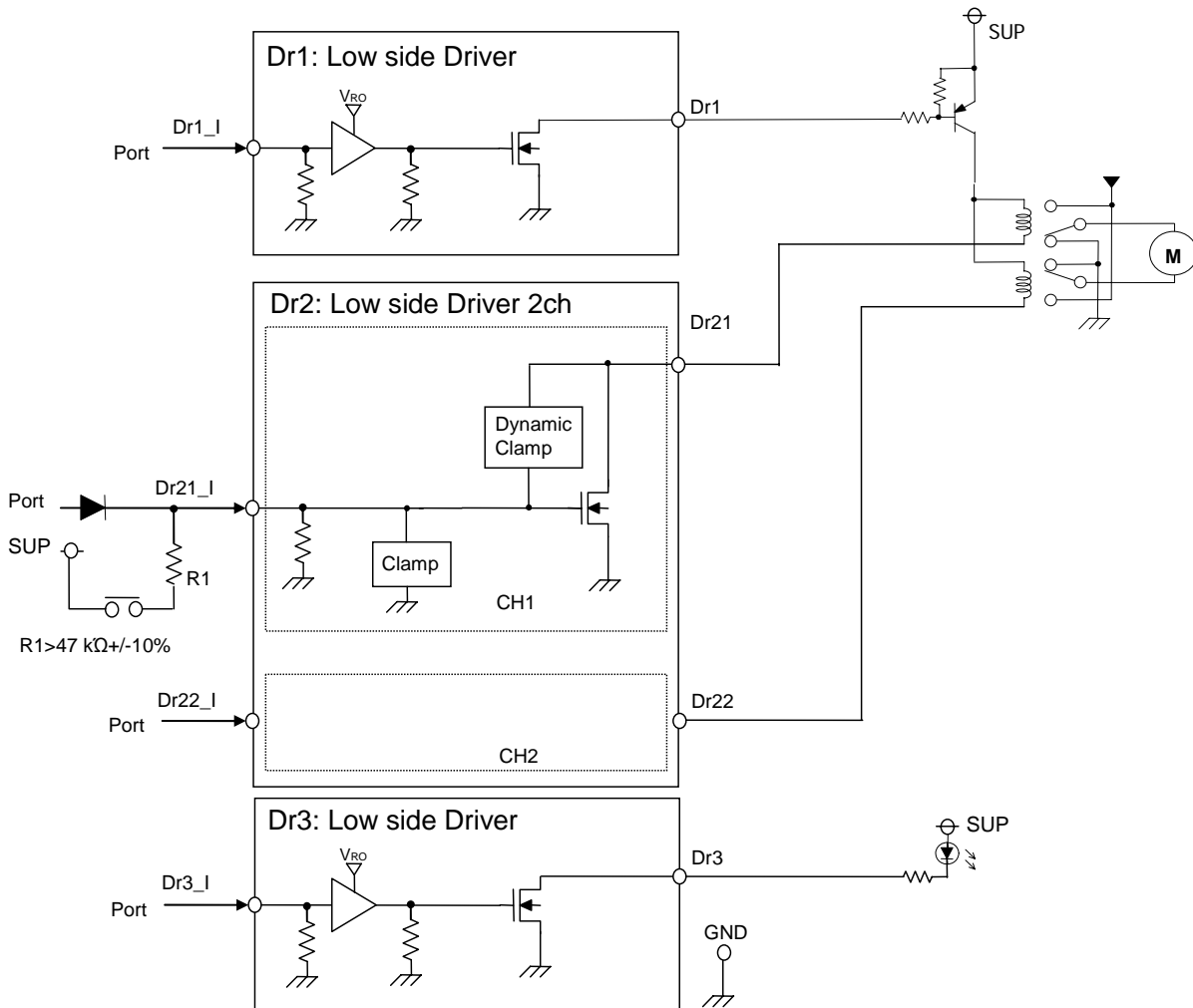
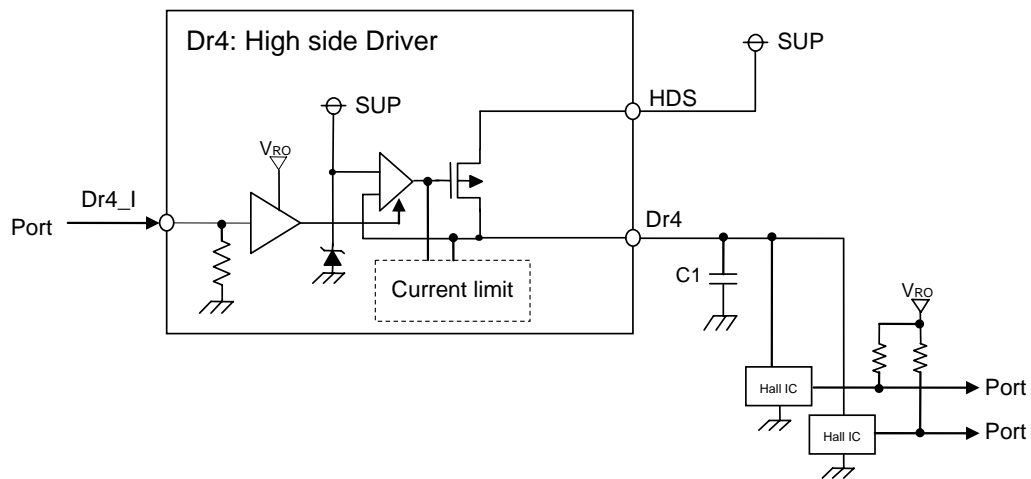


Figure 7-2. High Side Driver Circuit Application Example



CHAPTER 8 HIGH VOLTAGE SWITCH INPUT CIRCUIT

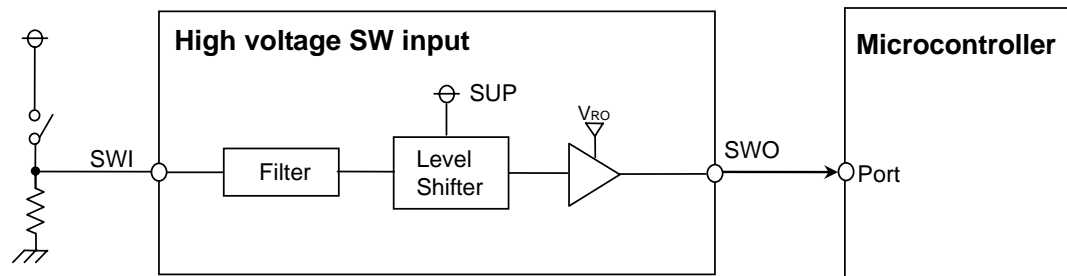
8.1 Switch Input Function

- Switch input circuit can connect 12 V battery directly.
- The signal input to SW1 is converted into 0 V/5 V and output.

Table 8-1. Truth Table

SWI	SWO
High	High
Low	Low

Figure 8-1. Application Example



CHAPTER 9 ELECTRICAL SPECIFICATIONS (A) GRADE PRODUCTS

Caution The μ PD78F0537DA has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. NEC Electronics is not liable for problems occurring when the on-chip debug function is used.

9.1 Absolute Maximum Ratings

Absolute Maximum Ratings for Microcontroller Block (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit	
Supply voltage	V _{DD}		-0.5 to +6.5	V	
	V _{SS}		-0.5 to +0.3	V	
	AV _{REF}		-0.5 to V _{DD} +0.3 ^{Note}	V	
	AV _{SS}		-0.5 to +0.3	V	
Input voltage	V _{I1}	P00, P01, P05, P06, P10 to P17, P20 to P25, P30 to P33, P70, P120 to P122, X1, X2, RESET, FLMD0	-0.3 to V _{DD} +0.3	V	
	V _{I2}	P60, P61 (N-ch open drain)	-0.3 to +6.5	V	
REGC pin input voltage	V _{IREGC}		-0.5 to +3.6 and -0.5 to V _{DD}	V	
Output voltage	V _O		-0.3 to V _{DD} +0.3 ^{Note}	V	
Analog input voltage	V _{AN}	ANI0 to ANI5	-0.3 to AV _{REF} +0.3 ^{Note} and -0.3 to V _{DD} +0.3 ^{Note}	V	
Output current, high	I _{OH1}	Per pin	-10	mA	
		Total of all pins -80 mA	P00, P01, P120	-25	mA
			P05, P06, P10 to P17, P30 to P33, P70	-55	
	I _{OH2}	Per pin	P20 to P25	-0.5	mA
		Total of all pins		-2	
	I _{OH3}	Per pin	P121, P122	-1	mA
		Total of all pins		-4	
	Output current, low	I _{OL1}	Per pin	30	mA
Total of all pins 200 mA			P00, P01, P120	60	mA
			P05, P06, P10 to P17, P30 to P33, P60, P61, P70	140	
I _{OL2}		Per pin	P20 to P24	1	mA
		Total of all pins		5	
I _{OL3}		Per pin	P121, P122	4	mA
		Total of all pins		10	

Note Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute Maximum Ratings for Analog Block (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{SUP1}	VSUP, HDS, 400 ms	-0.3 to +60	V
	V _{SUP2}	VSUP, HDS, 2 min	-0.3 to +28	V
	V _{SUP3}	VSUP, HDS	-0.3 to +20	V
	V _{RO}	VRO	-0.3 to +6.5	V
Input voltage	V _{IA1}	VIC, LIN, SWI, Dr21_I, Dr22_I, 400 ms Dr21_I and Dr22_I are input pin potentials with external 47 kΩ resistors.	-0.3 to +60	V
	V _{IA2}	VIC, LIN, SWI, Dr21_I, Dr22_I, 2 min Dr21_I and Dr22_I are input pin potentials with external 47 kΩ resistors.	-0.3 to +28	V
	V _{IA3}	VIC, LIN, SWI	-0.3 to +20	V
	V _{IA4}	MSLP, UMODE, Dr1_I, Dr3_I, Dr4_I	-0.3 to V _{RO} +0.3 ^{Note}	V
Input current	I _{DRin}	Dr21_I, Dr22_I	1.5	mA
LIN negative voltage	V _{ILin}	LIN, 7 V ≤ V _{SUP} ≤ 19 V, 1 s	V _{SUP} -60	V
Output voltage	V _{OA1}	LIN, Dr1, Dr21, Dr22, Dr3, Dr4, 400 ms	-0.3 to +60	V
	V _{OA2}	LIN, Dr1, Dr21, Dr22, Dr3, Dr4, 2 min	-0.3 to +28	V
	V _{OA3}	LIN, Dr1, Dr21, Dr22, Dr3, Dr4	-0.3 to +20	V
	V _{OA4}	SWO	-0.3 to V _{RO} +0.3 ^{Note}	V
Output current	I _{RO1}	VRO	25	mA
	I _{RO2}	VRO 1 s	65	mA
	I _{LIN}	LIN	200	mA
	I _{Dr1}	Dr1	10	mA
	I _{Dr2}	Dr21, Dr22	150	mA
	I _{Dr3}	Dr3	50	mA
	I _{Dr4}	Dr4	-40	mA
	I _{SWO}	SWO	-10 to +20	mA

Note Must be 6.5 V or lower.

Absolute Maximum Ratings for Common Item (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Operation ambient temperature	T _A		-40 to +85	°C
Storage temperature	T _{stg}		-65 to +150	°C
Junction temperature	T _{jmax}		140	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

9.2 Microcontroller Block Characteristics

X1 Oscillator Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator, crystal resonator		X1 clock oscillation frequency (f_x) ^{Note 1}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.0 ^{Note 2}		20.0	MHz
			$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$	1.0		5.0	

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. It is 2.0 MHz (MIN.) when programming on the board via UART6.

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
 - Do not cross the wiring with the other signal lines.
 - Do not route the wiring near a signal line through which a high fluctuating current flows.
 - Always make the ground point of the oscillator capacitor the same potential as V_{SS} .
 - Do not ground the capacitor to a ground pattern through which a high current flows.
 - Do not fetch signals from the oscillator.
- 2.** Since the CPU is started by the internal high-speed oscillation clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Internal Oscillator Characteristics**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$)**

Resonator	Parameter	Conditions	MIN.	TYP.	MAX.	Unit	
8 MHz internal oscillator	Internal high-speed oscillation clock frequency (f_{RH}) ^{Note 1}	RSTS = 1	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	7.6	8.0	8.4	MHz
			$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$	7.6	8.0	10.4	MHz
		RSTS = 0		2.48	5.6	9.86	MHz
240 kHz internal oscillator	Internal low-speed oscillation clock frequency (f_{RL})		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	216	240	264	kHz
			$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$	192	240	264	kHz

Note Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Remark RSTS: Bit 7 of the internal oscillation mode register (RCM))

DC Characteristics (1/4)

(TA = -40 to +85°C, 1.8 V ≤ VDD ≤ 5.5 V, AVREF ≤ VDD, VSS = AVSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output current, high ^{Note 1}	IOH1	Per pin for P00, P01, P05, P06, P10 to P17, P30 to P33, P70, P120	4.0 V ≤ VDD ≤ 5.5 V		-3.0	mA	
			2.7 V ≤ VDD < 4.0 V		-2.5	mA	
			1.8 V ≤ VDD < 2.7 V		-1.0	mA	
		Total ^{Note 3} of P00, P01, P120	4.0 V ≤ VDD ≤ 5.5 V		-12.0	mA	
			2.7 V ≤ VDD < 4.0 V		-7.0	mA	
			1.8 V ≤ VDD < 2.7 V		-5.0	mA	
		Total ^{Note 3} of P05, P06, P10 to P17, P30 to P33, P70	4.0 V ≤ VDD ≤ 5.5 V		-18.0	mA	
			2.7 V ≤ VDD < 4.0 V		-15.0	mA	
			1.8 V ≤ VDD < 2.7 V		-10.0	mA	
		Total ^{Note 3} of all pins	4.0 V ≤ VDD ≤ 5.5 V		-23.0	mA	
			2.7 V ≤ VDD < 4.0 V		-20.0	mA	
			1.8 V ≤ VDD < 2.7 V		-15.0	mA	
	IOH2	Per pin for P20 to P25	AVREF = VDD			-0.1	mA
		Per pin for P121, P122				-0.1	mA
Output current, low ^{Note 2}	IOL1	Per pin for P00, P01, P05, P06, P10 to P17, P30 to P33, P70, P120	4.0 V ≤ VDD ≤ 5.5 V		8.5	mA	
			2.7 V ≤ VDD < 4.0 V		5.0	mA	
			1.8 V ≤ VDD < 2.7 V		2.0	mA	
		Per pin for P60, P61	4.0 V ≤ VDD ≤ 5.5 V		15.0	mA	
			2.7 V ≤ VDD < 4.0 V		5.0	mA	
			1.8 V ≤ VDD < 2.7 V		2.0	mA	
		Total ^{Note 3} of P00, P01, P120	4.0 V ≤ VDD ≤ 5.5 V		20.0	mA	
			2.7 V ≤ VDD < 4.0 V		15.0	mA	
			1.8 V ≤ VDD < 2.7 V		9.0	mA	
		Total ^{Note 3} of P05, P06, P10 to P17, P30 to P33, P60, P61, P70	4.0 V ≤ VDD ≤ 5.5 V		45.0	mA	
			2.7 V ≤ VDD < 4.0 V		35.0	mA	
			1.8 V ≤ VDD < 2.7 V		20.0	mA	
	Total of all pins ^{Note 3}	4.0 V ≤ VDD ≤ 5.5 V		65.0	mA		
		2.7 V ≤ VDD < 4.0 V		50.0	mA		
		1.8 V ≤ VDD < 2.7 V		29.0	mA		
	IOL2	Per pin for P20 to P25	AVREF = VDD			0.4	mA
		Per pin for P121, P122				0.4	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from VDD to an output pin.

2. Value of current at which the device operation is guaranteed even if the current flows from an output pin to GND.

3. Specification under conditions where the duty factor is 70% (time for which current is output is $0.7 \times t$ and time for which current is not output is $0.3 \times t$, where t is a specific time). The total output current of the pins at a duty factor of other than 70% can be calculated by the following expression.

- Where the duty factor of IOH is n%: Total output current of pins = $(I_{OH} \times 0.7)/(n \times 0.01)$

<Example> Where the duty factor is 50%, IOH = 20.0 mA

$$\text{Total output current of pins} = (20.0 \times 0.7)/(50 \times 0.01) = 28.0 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (2/4)

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V _{IH1}	P12, P13, P15, P121, P122	0.7V _{DD}		V _{DD}	V
	V _{IH2}	P00, P01, P05, P06, P10, P11, P14, P16, P17, P30 to P33, P70, P120, EXCLK, RESET	0.8V _{DD}		V _{DD}	V
	V _{IH3}	P20 to P25	AV _{REF} = V _{DD}		AV _{REF}	V
	V _{IH4}	P60, P61			6.0	V
Input voltage, low	V _{IL1}	P12, P13, P15, P60, P61, P121, P122	0		0.3V _{DD}	V
	V _{IL2}	P00, P01, P05, P06, P10, P11, P14, P16, P17, P30 to P33, P70, P120, EXCLK, RESET	0		0.2V _{DD}	V
	V _{IL3}	P20 to P25	AV _{REF} = V _{DD}		0.3AV _{REF}	V
Output voltage, high	V _{OH1}	P00, P01, P05, P06, P10 to P17, P30 to P33, P70, P120	4.0 V ≤ V _{DD} ≤ 5.5 V, I _{OH1} = -3.0 mA		V _{DD} - 0.7	V
			2.7 V ≤ V _{DD} < 4.0 V, I _{OH1} = -2.5 mA		V _{DD} - 0.5	V
			1.8 V ≤ V _{DD} < 2.7 V, I _{OH1} = -1.0 mA		V _{DD} - 0.5	V
	V _{OH2}	P20 to P25	AV _{REF} = V _{DD} , I _{OH2} = -100 μA		V _{DD} - 0.5	V
			P121, P122	I _{OH2} = -100 μA		V _{DD} - 0.5

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (3/4)

 (T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output voltage, low	V _{OL1}	P00, P01, P05, P06, P10 to P17, P30 to P33, P70, P120	4.0 V ≤ V _{DD} ≤ 5.5 V, I _{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ V _{DD} < 4.0 V, I _{OL1} = 5.0 mA			0.7	V
			1.8 V ≤ V _{DD} < 2.7 V, I _{OL1} = 2.0 mA			0.5	V
			1.8 V ≤ V _{DD} < 2.7 V, I _{OL1} = 0.5 mA			0.4	V
	V _{OL2}	P20 to P25 P121, P122	AV _{REF} = V _{DD} , I _{OL2} = 0.4 mA			0.4	V
			I _{OL2} = 0.4 mA			0.4	V
	V _{OL3}	P60, P61	4.0 V ≤ V _{DD} ≤ 5.5 V, I _{OL3} = 15.0 mA			2.0	V
			4.0 V ≤ V _{DD} ≤ 5.5 V, I _{OL3} = 5.0 mA			0.4	V
			2.7 V ≤ V _{DD} < 4.0 V, I _{OL1} = 5.0 mA			0.6	V
			2.7 V ≤ V _{DD} < 4.0 V, I _{OL1} = 3.0 mA			0.4	V
1.8 V ≤ V _{DD} < 2.7 V, I _{OL1} = 2.0 mA					0.4	V	
Input leakage current, high	I _{LIH1}	P00, P01, P05, P06, P10 to P17, P30 to P33, P60, P61, P70, P120, FLMD0, RESET	V _I = V _{DD}			1	μA
	I _{LIH2}	P20 to P25	V _I = AV _{REF} = V _{DD}			1	μA
	I _{LIH3}	P121, 122 (X1, X2)	V _I = V _{DD} I/O port mode			1	μA
			OSC mode			20	μA
Input leakage current, low	I _{LIL1}	P00, P01, P05, P06, P10 to P17, P30 to P33, P60, P61, P70, P120, FLMD0, RESET	V _I = V _{SS}			-1	μA
	I _{LIL2}	P20 to P25	V _I = V _{SS} , AV _{REF} = V _{DD}			-1	μA
	I _{LIL3}	P121, 122 (X1, X2)	V _I = V _{SS} I/O port mode			-1	μA
			OSC mode			-20	μA
Pull-up resistor	R _U	V _I = V _{SS}	10	20	100	kΩ	
FLMD0 supply voltage	V _{IL}	In normal operation mode	0		0.2 V _{DD}	V	
	V _{IH}	In self-programming mode	0.8 V _{DD}		V _{DD}	V	

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (4/4)

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Supply current ^{Note 1}	I _{DD1}	Operating mode	f _{XH} = 20 MHz ^{Note 2} , V _{DD} = 5.0 V	Square wave input		3.2	5.5	mA
				Resonator connection		4.5	6.9	mA
			f _{XH} = 10 MHz ^{Notes 2, 3} , V _{DD} = 5.0 V	Square wave input		1.6	2.8	mA
				Resonator connection		2.3	3.9	mA
			f _{XH} = 10 MHz ^{Notes 2, 3} , V _{DD} = 3.0 V	Square wave input		1.5	2.7	mA
				Resonator connection		2.2	3.2	mA
			f _{XH} = 5 MHz ^{Notes 2, 3} , V _{DD} = 3.0 V	Square wave input		0.9	1.6	mA
				Resonator connection		1.3	2.0	mA
	f _{XH} = 5 MHz ^{Notes 2, 3} , V _{DD} = 2.0 V	Square wave input		0.7	1.4	mA		
		Resonator connection		1.0	1.6	mA		
			f _{RH} = 8 MHz, V _{DD} = 5.0 V ^{Note 4}		1.4	2.5	mA	
	I _{DD2}	HALT mode	f _{XH} = 20 MHz ^{Note 2} , V _{DD} = 5.0 V	Square wave input		0.8	2.6	mA
				Resonator connection		2.0	4.4	mA
			f _{XH} = 10 MHz ^{Notes 2, 3} , V _{DD} = 5.0 V	Square wave input		0.4	1.3	mA
Resonator connection					1.0	2.4	mA	
f _{XH} = 5 MHz ^{Notes 2, 3} , V _{DD} = 3.0 V			Square wave input		0.2	0.65	mA	
			Resonator connection		0.5	1.1	mA	
		f _{RH} = 8 MHz, V _{DD} = 5.0 V ^{Note 4}		0.4	1.2	mA		
I _{DD3} ^{Note 5}	STOP mode	V _{DD} = 5.0 V			1	20	μA	
		V _{DD} = 5.0 V, T _A = -40 to +70 °C			1	10	μA	
A/D converter operating current	I _{ADC} ^{Note 6}				0.86	1.9	mA	
Watchdog timer operating current	I _{WDT} ^{Note 7}	During 240 kHz internal low-speed oscillation clock operation			5	10	μA	
LVI operating current	I _{LVI} ^{Note 8}				9	18	μA	

Remarks 1. f_{XH}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{RH}: Internal high-speed oscillation clock frequency

(Notes on next page)

- Notes**
1. Total current flowing into the internal power supply (V_{DD}), including the peripheral operation current. Port output current and current flowing through on-chip pull-up resistor are not included. Input leakage current with input pin fixed to V_{DD} or V_{SS} is included.
 2. Operational current of the 8 MHz internal oscillator and 240 kHz internal oscillator is not included. TYP. value indicates current when only the CPU is operating. MAX. value includes peripheral operating current. However, WDT, LVI, and ADC stop ($ADCE = 0$).
 3. When AMPH (bit 0 of clock operation mode select register (OSCCTL)) = 0
 4. Operational current of the X1 oscillator and 240 kHz internal oscillator is not included. TYP. value indicates current when only the CPU is operating. MAX. value includes peripheral operating current. However, WDT, LVI, and ADC stop ($ADCE = 0$).
 5. Operational current of the 240 kHz internal oscillator is not included. MAX. value includes peripheral operating current. However, WDT, LVI, and ADC stop ($ADCE = 0$).
 6. Current flowing only to the A/D converter. The current value of the microcontroller block is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.
 7. Current flowing only to the watchdog timer (including the operating current of the 240 kHz internal oscillator). The current value of the microcontroller block is the sum of I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates in the HALT or STOP mode.
 8. Current flowing only to the LVI circuit. The current value of the microcontroller block is the sum of I_{DD2} or I_{DD3} and I_{LVI} when the LVI circuit operates in the HALT or STOP mode.

AC Characteristics

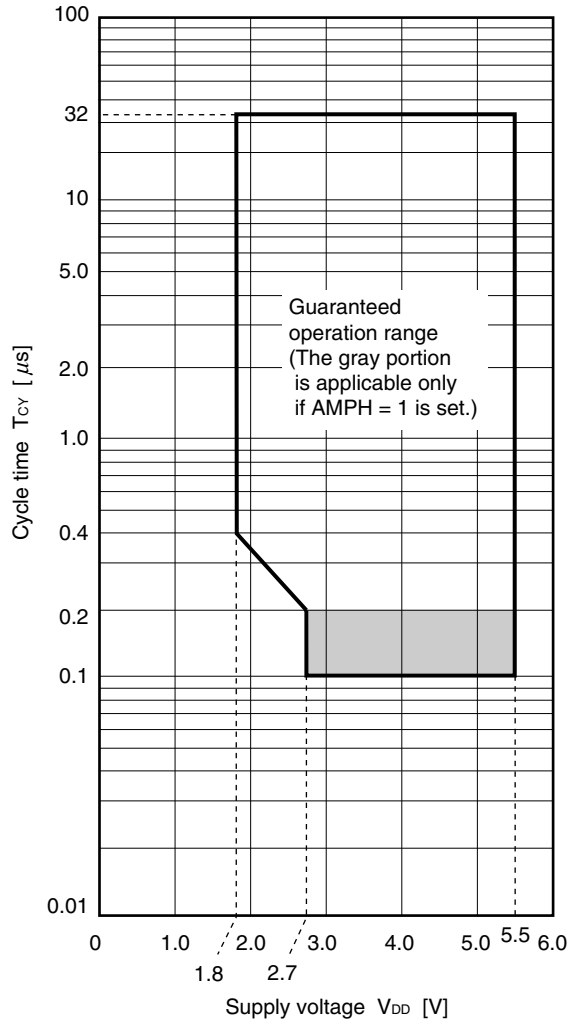
(1) Basic operation

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

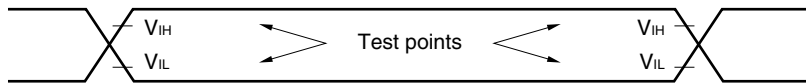
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Instruction cycle (minimum instruction execution time)	T _{CY}	Main system clock (f _{XP}) operation	2.7 V ≤ V _{DD} ≤ 5.5 V	0.1		32	μs
			1.8 V ≤ V _{DD} < 2.7 V	0.4 ^{Note 1}		32	μs
Peripheral hardware clock frequency	f _{PRS}	XSEL = 1	2.7 V ≤ V _{DD} ≤ 5.5 V			20	MHz
			1.8 V ≤ V _{DD} < 2.7 V			5	MHz
		XSEL = 0	2.7 V ≤ V _{DD} < 4.0 V	7.6		8.4	MHz
			1.8 V ≤ V _{DD} < 2.7 V ^{Note 2}	7.6		10.4	MHz
External main system clock frequency	f _{EXCLK}	2.7 V ≤ V _{DD} ≤ 5.5 V	1.0 ^{Note 3}		20.0	MHz	
		1.8 V ≤ V _{DD} < 2.7 V	1.0		5.0	MHz	
External main system clock input high-level width, low-level width	t _{EXCLKH} ,	2.7 V ≤ V _{DD} ≤ 5.5 V	24			ns	
	t _{EXCLKL}	1.8 V ≤ V _{DD} < 2.7 V	96			ns	
TI000, TI010, TI001, TI011 input high-level width, low-level width	t _{TIH0} , t _{TIL0}	4.0 V ≤ V _{DD} ≤ 5.5 V	2/f _{sam} + 0.1 ^{Note 4}			μs	
		2.7 V ≤ V _{DD} < 4.0 V	2/f _{sam} + 0.2 ^{Note 4}			μs	
		1.8 V ≤ V _{DD} < 2.7 V	2/f _{sam} + 0.5 ^{Note 4}			μs	
TI50, TI51 input frequency	f _{TI5}	4.0 V ≤ V _{DD} ≤ 5.5 V			10	MHz	
		2.7 V ≤ V _{DD} < 4.0 V			10	MHz	
		1.8 V ≤ V _{DD} < 2.7 V			5	MHz	
TI50, TI51 input high-level width, low-level width	t _{TIH5} , t _{TIL5}	4.0 V ≤ V _{DD} ≤ 5.5 V	50			ns	
		2.7 V ≤ V _{DD} < 4.0 V	50			ns	
		1.8 V ≤ V _{DD} < 2.7 V	100			ns	
Interrupt input high-level width, low-level width	t _{INTH} , t _{INTL}		1			μs	
Key interrupt input low-level width	t _{KR}		250			ns	
RESET low-level width	t _{RSL}		10			μs	

- Notes**
- 0.38 μs when operating with the 8 MHz internal oscillator.
 - This specification defines the selection clock primary frequency. Therefore, select the division clock that sets the peripheral hardware clock frequency to 5.2 MHz (MAX.).
 - It is 2.0 MHz (MIN.) when programming on the board via UART6.
 - Selection of f_{sam} = f_{PRS}, f_{PRS}/4, f_{PRS}/256, or f_{PRS}, f_{PRS}/16, f_{PRS}/64 is possible using bits 0 and 1 (PRM000, PRM001 or PRM010, PRM011) of prescaler mode registers 00 and 01 (PRM00, PRM01). Note that when selecting the TI000 or TI001 valid edge as the count clock, f_{sam} = f_{PRS}.

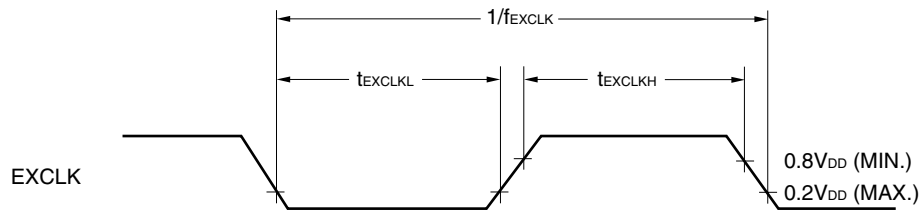
T_{CY} vs. V_{DD} (Main System Clock Operation)



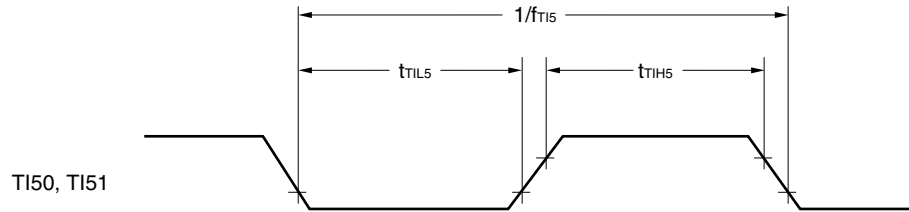
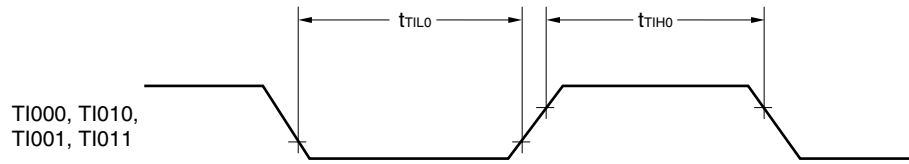
AC Timing Test Points



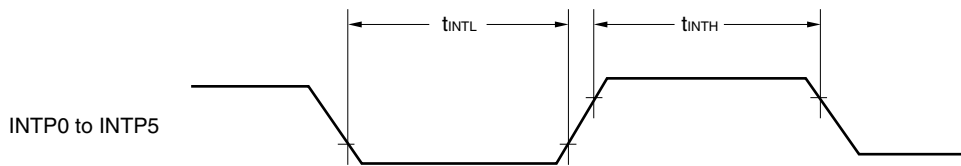
External Main System Clock Timing



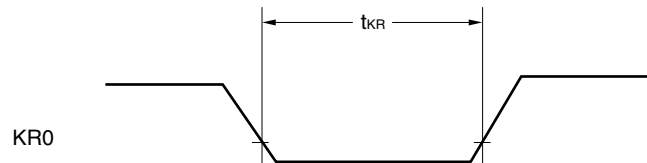
TI Timing



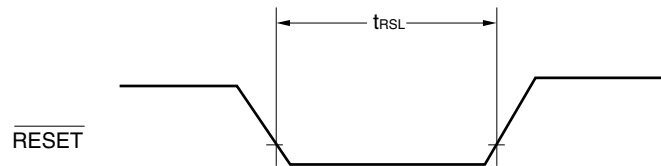
Interrupt Request Input Timing



Key Interrupt Input Timing



RESET Input Timing



(2) Serial interface
 $(T_A = -40 \text{ to } +85^\circ\text{C}, 1.8 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}, AV_{REF} \leq V_{DD}, V_{SS} = AV_{SS} = 0 \text{ V})$
(a) UART6 (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					625	kbps

(b) UART0 (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					625	kbps

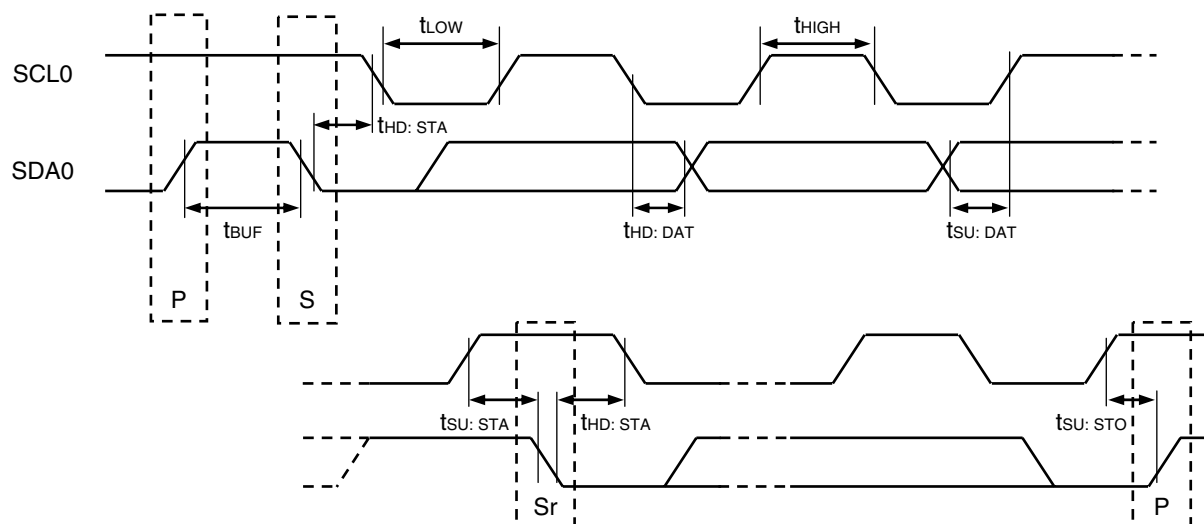
(c) IIC0

Parameter	Symbol	Conditions	Standard Mode		High-Speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency	f_{CLK}		0	100	0	400	kHz
Reset condition setup time	$t_{SU:STA}$		4.7		0.6		μs
Hold time ^{Note 1}	$t_{HD:STA}$		4.0		0.6		μs
Hold time when SCL0 = "L"	t_{LOW}	Internal clock operation	4.7		1.3		μs
Hold time when SCL0 = "H"	t_{HIGH}		4.0		0.6		μs
Data setup time (reception)	$t_{SU:DAT}$		250		100		ns
Data hold time (transmission) ^{Note 2}	$t_{HD:DAT}$	When $f_w = f_{XH}/2^N$ is selected ^{Note 3}	0	3.45	0	0.9 ^{Note 4}	μs
						1.0 ^{Note 5}	μs
		When $f_w = f_{RH}/2^N$ is selected ^{Note 3}	0	3.45	0	1.05	μs
Stop condition setup time	$t_{SU:STO}$		4.0		0.6		μs
Bus free time	t_{BUF}		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/reset condition is detected.

- 2.** The maximum value (MAX.) of $t_{HD:DAT}$ is normal transfer and a wait state is inserted in the \overline{ACK} (acknowledge) timing.
- 3.** f_w indicates the IIC0 transfer clock selected by the IICCL0 and IICX0 registers.
- 4.** When $f_w \geq 4.4 \text{ MHz}$ is selected
- 5.** When $f_w < 4.4 \text{ MHz}$ is selected

IIC0 Transfer Timing



P : Stop condition
 S : Start condition
 Sr : Restart condition

 (d) CSI10 (master mode, $\overline{\text{SCK10}}$ internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK10}}$ cycle time	t_{KCY1}	$4.0 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	200			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.0 \text{ V}$	400			ns
		$1.8 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	600			ns
$\overline{\text{SCK10}}$ high-/low-level width	$t_{\text{KH1}}, t_{\text{KL1}}$	$4.0 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	$t_{\text{KCY1}}/2 - 20^{\text{Note 1}}$			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.0 \text{ V}$	$t_{\text{KCY1}}/2 - 30^{\text{Note 1}}$			ns
		$1.8 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	$t_{\text{KCY1}}/2 - 60^{\text{Note 1}}$			ns
SI10 setup time (to $\overline{\text{SCK10}}\uparrow$)	t_{SIK1}	$4.0 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	70			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.0 \text{ V}$	100			ns
		$1.8 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$	190			ns
SI10 hold time (from $\overline{\text{SCK10}}\uparrow$)	t_{KSI1}		30			ns
Delay time from $\overline{\text{SCK10}}\downarrow$ to SO10 output	t_{KSO1}	$C = 50 \text{ pF}^{\text{Note 2}}$			40	ns

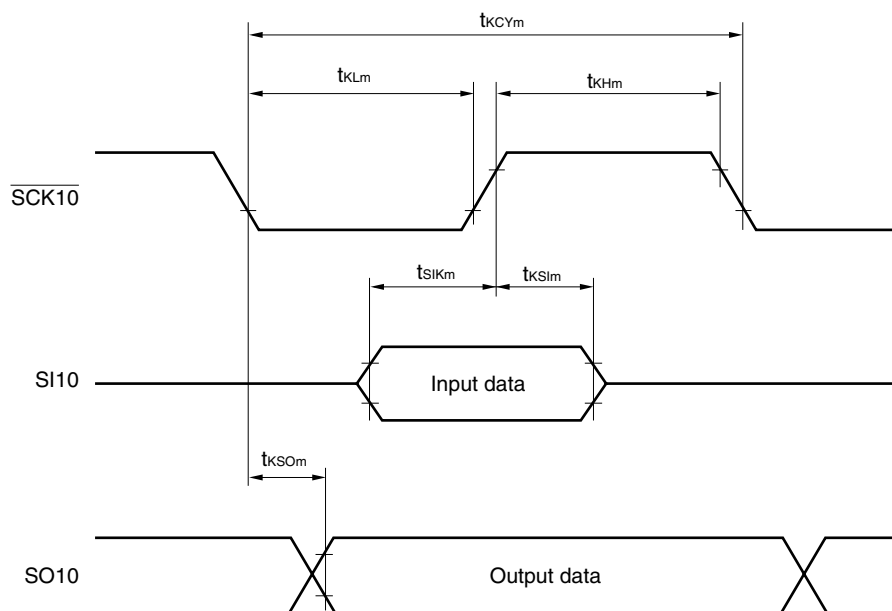
- Notes** 1. This value is when high-speed system clock (f_{XH}) is used.
 2. C is the load capacitance of the $\overline{\text{SCK10}}$ and SO10 output lines.

(e) CSI10 (slave mode, $\overline{\text{SCK10}}$... external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK10}}$ cycle time	t_{KCY2}		400			ns
$\overline{\text{SCK10}}$ high-/low-level width	t_{KH2} , t_{KL2}		$t_{\text{KCY2}}/2$			ns
SI10 setup time (to $\overline{\text{SCK10}}\uparrow$)	t_{SIK2}		80			ns
SI10 hold time (from $\overline{\text{SCK10}}\uparrow$)	t_{SI2}		50			ns
Delay time from $\overline{\text{SCK10}}\downarrow$ to SO10 output	t_{KSO2}	$C = 50 \text{ pF}$ <small>Note</small>	$4.0 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$		120	ns
			$2.7 \text{ V} \leq V_{\text{DD}} < 4.0 \text{ V}$		120	ns
			$1.8 \text{ V} \leq V_{\text{DD}} < 2.7 \text{ V}$		180	ns

Note C is the load capacitance of the SO10 output line.

CSI10 Transfer Timing



Remark m = 1, 2

A/D Converter Characteristics

 ($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.3\text{ V} \leq AV_{REF} \leq V_{DD}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

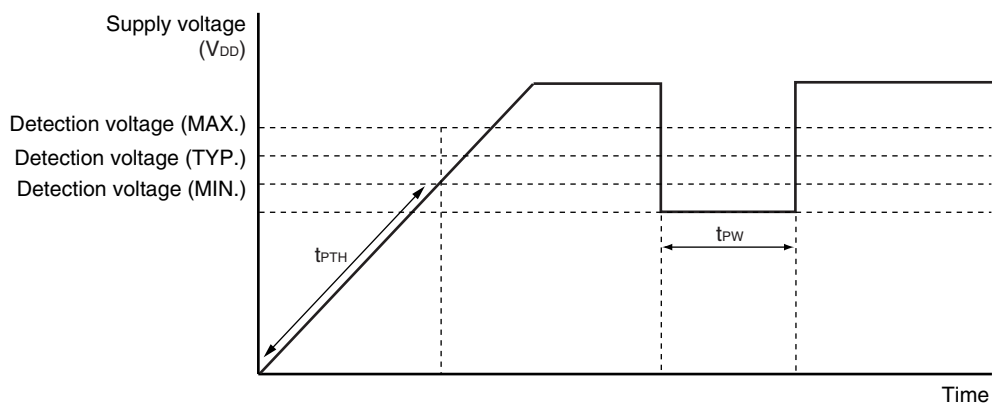
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES				10	bit
Overall error ^{Notes 1, 2}	AINL	$4.0\text{ V} \leq AV_{REF} \leq 5.5\text{ V}$			± 0.4	%FSR
		$2.7\text{ V} \leq AV_{REF} < 4.0\text{ V}$			± 0.6	%FSR
		$2.3\text{ V} \leq AV_{REF} < 2.7\text{ V}$			± 1.2	%FSR
Conversion time	t _{CONV}	$4.0\text{ V} \leq AV_{REF} \leq 5.5\text{ V}$	6.1		66.6	μs
		$2.7\text{ V} \leq AV_{REF} < 4.0\text{ V}$	12.2		66.6	μs
		$2.3\text{ V} \leq AV_{REF} < 2.7\text{ V}$	27		66.6	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	$4.0\text{ V} \leq AV_{REF} \leq 5.5\text{ V}$			± 0.4	%FSR
		$2.7\text{ V} \leq AV_{REF} < 4.0\text{ V}$			± 0.6	%FSR
		$2.3\text{ V} \leq AV_{REF} < 2.7\text{ V}$			± 0.6	%FSR
Full-scale error ^{Notes 1, 2}	E _{FS}	$4.0\text{ V} \leq AV_{REF} \leq 5.5\text{ V}$			± 0.4	%FSR
		$2.7\text{ V} \leq AV_{REF} < 4.0\text{ V}$			± 0.6	%FSR
		$2.3\text{ V} \leq AV_{REF} < 2.7\text{ V}$			± 0.6	%FSR
Integral non-linearity error ^{Note 1}	ILE	$4.0\text{ V} \leq AV_{REF} \leq 5.5\text{ V}$			± 2.5	LSB
		$2.7\text{ V} \leq AV_{REF} < 4.0\text{ V}$			± 4.5	LSB
		$2.3\text{ V} \leq AV_{REF} < 2.7\text{ V}$			± 6.5	LSB
Differential non-linearity error ^{Note 1}	DLE	$4.0\text{ V} \leq AV_{REF} \leq 5.5\text{ V}$			± 1.5	LSB
		$2.7\text{ V} \leq AV_{REF} < 4.0\text{ V}$			± 2.0	LSB
		$2.3\text{ V} \leq AV_{REF} < 2.7\text{ V}$			± 2.0	%FSR
Analog input voltage	V _{AIN}		AV _{SS}		AV _{REF}	V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

1.59 V POC Circuit Characteristics ($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V _{POC}		1.44	1.59	1.74	V
Power voltage rise inclination	t _{PTH}	V _{DD} : 0 V → change inclination of V _{POC}	0.5			V/ms
Minimum pulse width	t _{PW}		200			μs

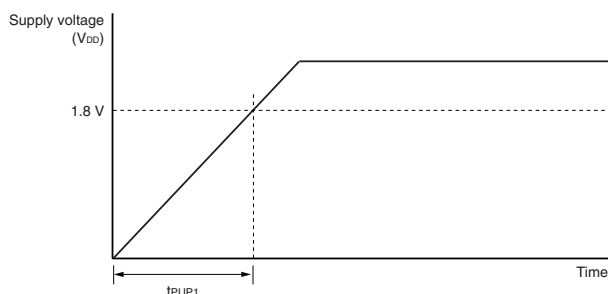
POC Circuit Timing


Supply Voltage Rise Time ($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0$ V)

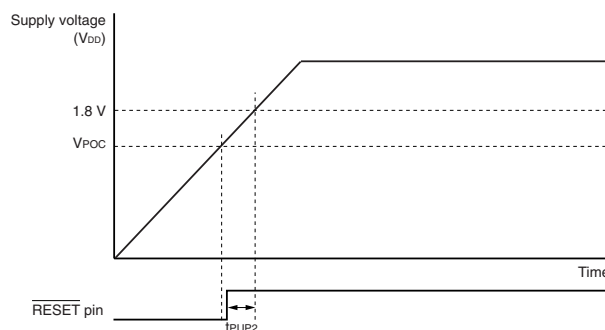
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum time to rise to 1.8 V (V_{DD} (MIN.)) ($V_{DD}: 0$ V \rightarrow 1.8 V)	t_{PUP1}	POCMODE (option byte) = 0, when $\overline{\text{RESET}}$ input is not used			3.6	ms
Maximum time to rise to 1.8 V (V_{DD} (MIN.)) (releasing $\overline{\text{RESET}}$ input \rightarrow $V_{DD}: 1.8$ V)	t_{PUP2}	POCMODE (option byte) = 0, when $\overline{\text{RESET}}$ input is used			1.9	ms

Supply Voltage Rise Time Timing

- When $\overline{\text{RESET}}$ pin input is not used



- When $\overline{\text{RESET}}$ pin input is used


2.7 V POC Circuit Characteristics ($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage on application of supply voltage	V_{DDPOC}	POCMODE (option byte) = 1	2.50	2.70	2.90	V

Remark The operations of the POC circuit are as described below, depending on the POCMODE (option byte) setting.

Option Byte Setting	POC Mode	Operation
POCMODE = 0	1.59 V mode operation	A reset state is retained until $V_{POC} = 1.59$ V (TYP.) is reached after the power is turned on, and the reset is released when V_{POC} is exceeded. After that, POC detection is performed at V_{POC} , similarly as when the power was turned on. The power supply voltage must be raised at a time of t_{PUP1} or t_{PUP2} when POCMODE is 0.
POCMODE = 1	2.7 V/1.59 V mode operation	A reset state is retained until $V_{DDPOC} = 2.7$ V (TYP.) is reached after the power is turned on, and the reset is released when V_{DDPOC} is exceeded. After that, POC detection is performed at $V_{POC} = 1.59$ V (TYP.) and not at V_{DDPOC} . The use of the 2.7 V/1.59 V POC mode is recommended when the rise of the voltage, after the power is turned on and until the voltage reaches 1.8 V, is more relaxed than t_{PTH} .

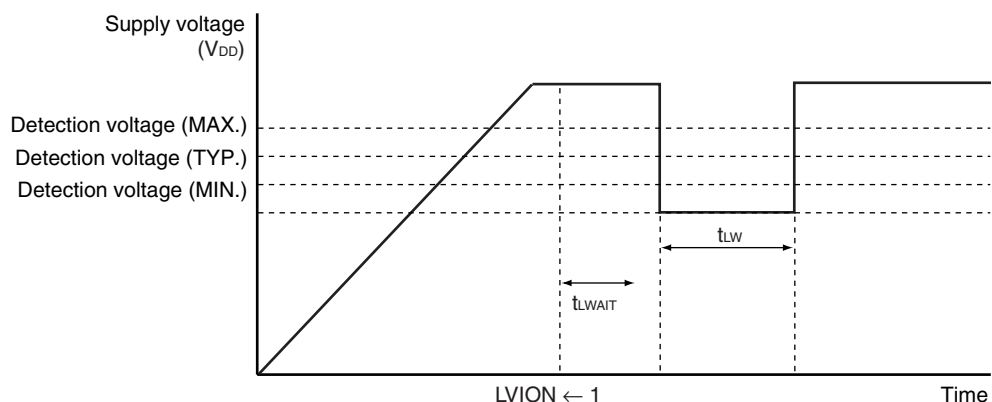
LVI Circuit Characteristics ($T_A = -40$ to $+85^\circ\text{C}$, $V_{POC} \leq V_{DD} \leq 5.5$ V, $AV_{REF} \leq V_{DD}$, $V_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Detection voltage	Supply voltage level	V_{LVI0}		4.14	4.24	4.34	V
		V_{LVI1}		3.99	4.09	4.19	V
		V_{LVI2}		3.83	3.93	4.03	V
		V_{LVI3}		3.68	3.78	3.88	V
		V_{LVI4}		3.52	3.62	3.72	V
		V_{LVI5}		3.37	3.47	3.57	V
		V_{LVI6}		3.22	3.32	3.42	V
		V_{LVI7}		3.06	3.16	3.26	V
		V_{LVI8}		2.91	3.01	3.11	V
		V_{LVI9}		2.75	2.85	2.95	V
		V_{LVI10}		2.60	2.70	2.80	V
		V_{LVI11}		2.45	2.55	2.65	V
		V_{LVI12}		2.29	2.39	2.49	V
		V_{LVI13}		2.14	2.24	2.34	V
		V_{LVI14}		1.98	2.08	2.18	V
V_{LVI15}		1.83	1.93	2.03	V		
External input pin ^{Note 1}	EXLVI	$EXLVI < V_{DD}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.11	1.21	1.31	V	
Minimum pulse width	t_{LW}		200			μs	
Operation stabilization wait time ^{Note 2}	t_{LWAIT}		10			μs	

- Notes**
1. The EXLVI/P120/INTP0 pin is used.
 2. Time required from setting bit 7 (LVION) of the low-voltage detection register (LVIM) to 1 to operation stabilization

Remark $V_{LVI(n-1)} > V_{LVIn}$: $n = 1$ to 15

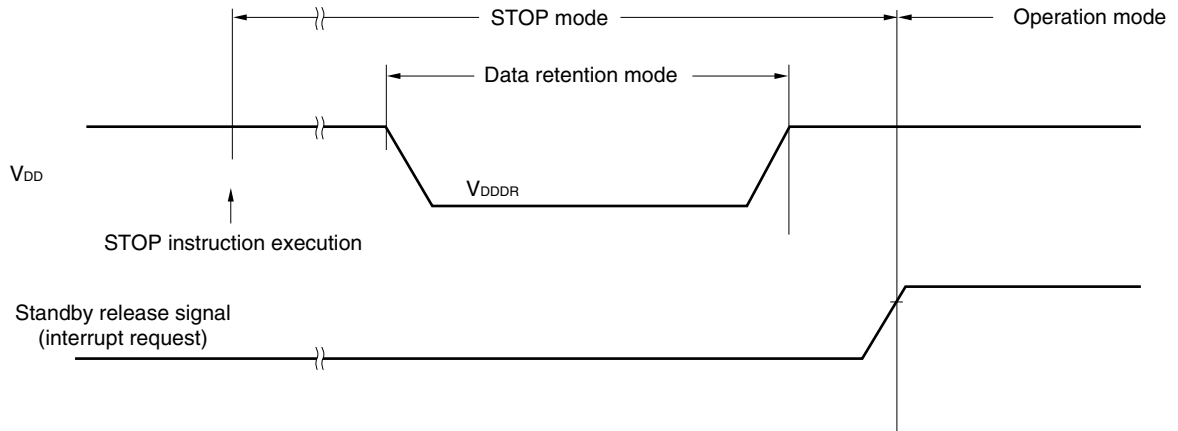
LVI Circuit Timing



Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics ($T_A = -40$ to $+85^\circ\text{C}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 ^{Note}		5.5	V

Note The value depends on the POC detection voltage. When the voltage drops, the data is retained until a POC reset is effected, but data is not retained when a POC reset is effected.



Flash Memory Programming Characteristics(T_A = -40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)• **Basic characteristics**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
V _{DD} supply current	I _{DD}	f _{XP} = 10 MHz (TYP.), 20 MHz (MAX.)		4.5	11.0	mA	
Erase time ^{Notes 1, 2}	All block	T _{eraca}		20	200	ms	
	Block unit	T _{erasa}		20	200	ms	
Write time (in 8-bit units) ^{Note 1}	T _{wrwa}			10	100	μs	
Number of rewrites per chip	C _{erwr}	1 erase + 1 write after erase = 1 rewrite ^{Note 3}	<ul style="list-style-type: none"> When a flash memory programmer is used, and the libraries^{Note 4} provided by NEC Electronics are used For program update 	15 years	1000		Times
			<ul style="list-style-type: none"> When the EEPROM emulation libraries^{Note 5} provided by NEC Electronics are used The rewritable ROM size: 4 KB For data update 	5 years	10000		Times
		Conditions other than the above ^{Note 6}	10 years	100		Times	

Notes 1. Characteristic of the flash memory. For the characteristic when a dedicated flash programmer, PG-FP4 or PG-FP5, is used and the rewrite time during self programming, see **CHAPTER 27 FLASH MEMORY in 78K0/Kx2 User's Manual (U18598E)**.

- The prewrite time before erasure and the erase verify time (writeback time) are not included.
- When a product is first written after shipment, "erase → write" and "write only" are both taken as one rewrite.
- The sample library specified by the **78K0/Kx2 Flash Memory Self Programming User's Manual (U17516E)** is excluded.
- The sample program specified by the **78K0/Kx2 EEPROM Emulation Application Note (U17517E)** is excluded.
- These include when the sample library specified by the **78K0/Kx2 Flash Memory Self Programming User's Manual (U17516E)** and the sample program specified by the **78K0/Kx2 EEPROM Emulation Application Note (U17517E)** are used.

Remarks 1. f_{XP}: Main system clock oscillation frequency

- For serial write operation characteristics, refer to **78K0/Kx2 Flash Memory Programming (Programmer) Application Note (U17739E)**.

9.3 Analog Block Characteristics

Voltage regulator circuit characteristics ($T_A = -40$ to $+85^\circ\text{C}$, $7\text{ V} \leq V_{\text{SUP}} \leq 19\text{ V}$, $I_{\text{RO}} \leq 15\text{ mA}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
REG output voltage	V_{CCOUT1}	$7\text{ V} \leq V_{\text{SUP}} \leq 19\text{ V}$ $V_{\text{CCOUT}} = V_{\text{RO}}$, $I_{\text{RO}} = 15\text{ mA}$	4.85	5	5.15	V
	V_{CCOUT2}	$19\text{ V} < V_{\text{SUP}} \leq 60\text{ V}$ $V_{\text{CCOUT}} = V_{\text{RO}}$, $I_{\text{RO}} = 1\text{ mA}$	(4.5)	(5)	(5.5)	V
Over current detect voltage	V_{SUPlim1}	$7\text{ V} \leq V_{\text{SUP}} \leq 19\text{ V}$ Potential difference of detection resistor connection pin	100	150	230	mV
Load regulation	REG_{L1}	$1\text{ mA} < I_{\text{RO}} \leq 15\text{ mA}$, $V_{\text{SUP}} = 14\text{ V}$			60	mV
Input regulation	REG_{IN1}	$I_{\text{CCOUT}} = 15\text{ mA}$			60	mV
DRPS high level input voltage	V_{IHDRPS}		$0.7V_{\text{SUP}}$		V_{SUP}	V
DRPS low level input voltage	V_{ILDRPS}				$0.3V_{\text{SUP}}$	V
Thermal shutdown	V_{Rth}		(150)			$^\circ\text{C}$

Remark The values in parentheses are based on design for which no outgoing inspection has been performed.

Supply current Characteristics ($T_A = -40$ to $+85^\circ\text{C}$, $4.85\text{ V} \leq V_{\text{RO}} \leq 5.15\text{ V}$, $7\text{ V} \leq V_{\text{SUP}} \leq 19\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current ^{Note}	I_{BAT1}	DR4 :OFF $T_A = 25\text{ }^\circ\text{C}$, $V_{\text{SUP}} = 14\text{ V}$, LIN: Sleep			35	μA
	I_{BAT2}	DR4 :OFF LIN: Sleep			60	μA
	I_{BAT3}	DR4 :OFF LIN: Normal (LIN bus:Recessive)			3	mA

Note This is the total current flowing to the SUP, VRO internal power supply. The peripheral operating current is included. However, the current flow through the port pull-up resistor is not included. V_{DD} current not included. For microcontroller supply current, refer to **78K0/Kx2 User's Manual (U18598E)**.

LIN Transceiver circuit Characteristics

DC Characteristics ($T_A = -40$ to $+85^\circ\text{C}$, $7\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $4.85\text{ V} \leq V_{\text{RO}} \leq 5.15\text{ V}$, $I_{\text{RO}} \leq 15\text{ mA}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LIN Bus dominant leak current	$I_{\text{BUS_PAS_dom}}$	Driver off ($V_{\text{TXD}} = V_{\text{RO}}$), $V_{\text{BUS}} = 0\text{ V}$, $V_{\text{SUP}} = 12\text{ V}$	-1			mA
LIN Bus recessive leak current	$I_{\text{BUS_PAS_rec}}$	Driver off ($V_{\text{TXD}} = V_{\text{RO}}$), $8\text{ V} < V_{\text{SUP}} < 18\text{ V}$, $8\text{ V} < V_{\text{BUS}} < 18\text{ V}$, $V_{\text{BUS}} \geq V_{\text{SUP}}$			20	μA
LIN Bus current 1	$I_{\text{BUS_NO_GND}}$	$\text{GND}_{\text{Device}} = V_{\text{SUP}}$, $0\text{ V} < V_{\text{BUS}} < 18\text{ V}$, $V_{\text{SUP}} = 12\text{ V}$	(-1)		(+1)	mA
LIN Bus current 2	I_{BUS}	$V_{\text{SUP_Device}} = \text{GND}$, $0\text{ V} < V_{\text{BUS}} < 18\text{ V}$		(1)	(10)	μA
Receive dominant-level input voltage	V_{BUSdom}				$0.4 V_{\text{SUP}}$	V
Receive recessive-level Input voltage	V_{BUSrec}		$0.6 V_{\text{SUP}}$			V
Receive centre-level threshold	$V_{\text{BUS_CNT}}$	$(V_{\text{th_dom}} + V_{\text{th_rec}})/2$	$0.475 V_{\text{SUP}}$	$0.5 V_{\text{SUP}}$	$0.525 V_{\text{SUP}}$	V
Receive hysteresis	V_{HYS}				$0.175 V_{\text{SUP}}$	V
LIN dominant-level output voltage 1	$V_{\text{BUSdom_DR}}$ V_{LoSUP}	$V_{\text{SUP}} = 7.3\text{ V}$, $I_{\text{lin}} = 15\text{ mA}$			1.2	V
LIN dominant-level output voltage 2	$V_{\text{BUSdom_DR}}$ V_{HiSUP}	$V_{\text{SUP}} = 18\text{ V}$, $I_{\text{lin}} = 36\text{ mA}$			2	V
LIN serial diode drop voltage	V_{SerDiode}	$V_{\text{TXD}} = V_{\text{RO}}$, $I_{\text{lin}} = -10\ \mu\text{A}$	0.4	0.7	1.0	V
LIN pull-up resistance	R_{slave}		20	30	60	$\text{k}\Omega$
MSLP high level input voltage	V_{slpH}		3.5			V
MSLP low level input voltage	V_{slpL}				1.5	V
MSLP pull-down resistance	R_{mslp}		50		200	$\text{k}\Omega$
UMODE high level input voltage	V_{umh}		$0.7 V_{\text{RO}}$			V
UMODE low level input voltage	V_{uml}				$0.3 V_{\text{RO}}$	V
UMODE pull-down resistance	R_{umode}		50		200	$\text{k}\Omega$
LIN thermal shutdown	LIN_{th}		(150)			$^\circ\text{C}$
LIN over current limitation	I_{CONST}	LIN pin inflow current limited value	40	80	200	mA

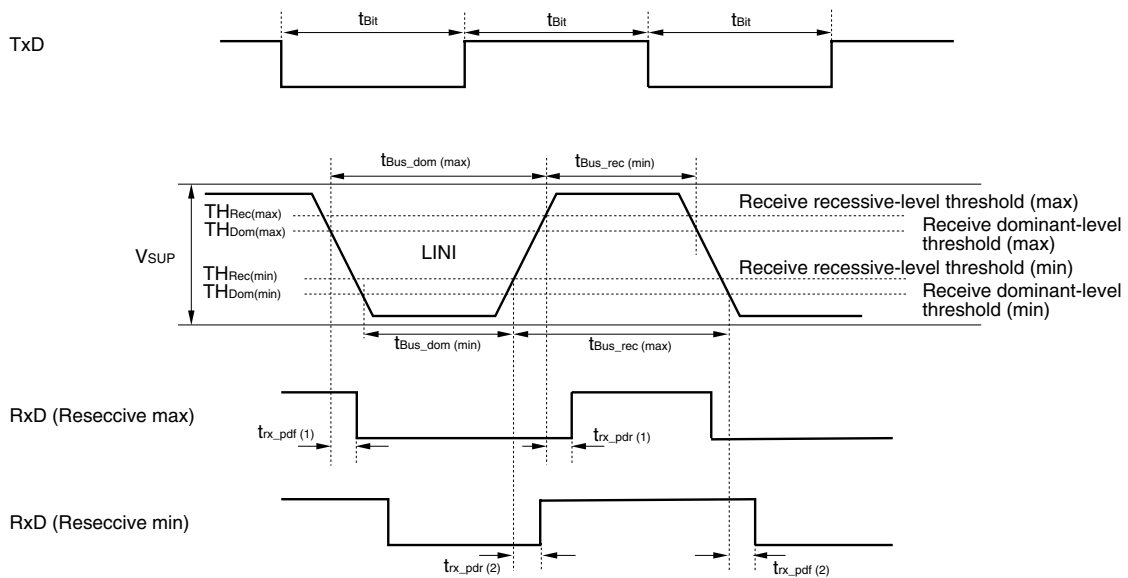
Remark The values in parentheses are based on design for which no outgoing inspection has been performed.

AC Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $7\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $4.85\text{ V} \leq V_{\text{RO}} \leq 5.15\text{ V}$, $I_{\text{RO}} \leq 15\text{ mA}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Duty_Cycle1 (see figure 9-1)	D1	$C_{\text{bus}}, R_{\text{bus}} = 1\text{ nF}; 1\text{ k}\Omega/6.8\text{ nF}; 660\ \Omega/10\text{ nF}; 500\ \Omega$ $t_{\text{BIT}} = 50\ \mu\text{s}$ $\text{TH}_{\text{Rec(max)}} = 0.744 \times V_{\text{SUP}}$, $\text{TH}_{\text{Dom(max)}} = 0.581 \times V_{\text{SUP}}$ $D_1 = t_{\text{BUS_rec(min)}} / (2 \times t_{\text{BIT}})$	0.396			–
Duty_Cycle2 (see figure 9-1)	D2	$C_{\text{bus}}, R_{\text{bus}} = 1\text{ nF}; 1\text{ k}\Omega/6.8\text{ nF}; 660\ \Omega/10\text{ nF}; 500\ \Omega$ $t_{\text{BIT}} = 50\ \mu\text{s}$ $\text{TH}_{\text{Rec(min)}} = 0.422 \times V_{\text{SUP}}$, $\text{TH}_{\text{Dom(min)}} = 0.284 \times V_{\text{SUP}}$ $D_2 = t_{\text{BUS_rec(max)}} / (2 \times t_{\text{BIT}})$ $7.6\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$			0.581	–
Duty_Cycle3 (see figure 9-1)	D3	$C_{\text{bus}}, R_{\text{bus}} = 1\text{ nF}; 1\text{ k}\Omega/6.8\text{ nF}; 660\ \Omega/10\text{ nF}; 500\ \Omega$ $t_{\text{BIT}} = 96\ \mu\text{s}$ $\text{TH}_{\text{Rec(max)}} = 0.778 \times V_{\text{SUP}}$, $\text{TH}_{\text{Dom(max)}} = 0.616 \times V_{\text{SUP}}$ $D_3 = t_{\text{BUS_rec(min)}} / (2 \times t_{\text{BIT}})$	0.417			–
Duty_Cycle4 (see figure 9-1)	D4	$C_{\text{bus}}, R_{\text{bus}} = 1\text{ nF}; 1\text{ k}\Omega/6.8\text{ nF}; 660\ \Omega/10\text{ nF}; 500\ \Omega$ $t_{\text{BIT}} = 96\ \mu\text{s}$ $\text{TH}_{\text{Rec(min)}} = 0.389 \times V_{\text{SUP}}$, $\text{TH}_{\text{Dom(min)}} = 0.251 \times V_{\text{SUP}}$ $D_3 = t_{\text{BUS_rec(max)}} / (2 \times t_{\text{BIT}})$ $7.6\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$			0.590	–
Propagation delay	$t_{\text{rx_pd}}$	$t_{\text{rx_pdf(1)}}, t_{\text{rx_pdf(2)}}, t_{\text{rx_pdr(1)}}, t_{\text{rx_pdr(2)}}$			6	μs
LIN rising and falling transmitter delay symmetry	$t_{\text{rx_sym}}$	$t_{\text{rx_sym}} = t_{\text{rx_pdf(1)}} - t_{\text{rx_pdr(1)}},$ $t_{\text{rx_sym}} = t_{\text{rx_pdf(2)}} - t_{\text{rx_pdr(2)}},$	–2		+2	μs

Figure 9-1. Duty Cycle



Driver circuit Characteristics

(TA = -40 to +85°C, 7 V ≤ V_{SUP} ≤ 19 V, 4.85 V ≤ V_{RO} ≤ 5.15 V, I_{RO} ≤ 15 mA)

Parameter	symbol	conditions	MIN.	TYP.	MAX.	Unit
Ron	Dr1_RON	I _o = 10 mA, Dr1_I = V _{RO}			100	Ω
	Dr2_RON	I _o = 100 mA, Dr2n_I ≥ 4 V			10	Ω
	Dr3_RON	I _o = 50 mA, Dr3_I = V _{RO}			10	Ω
	Dr4_RON	I _o = 16 mA, 7 V ≤ V _{SUP} ≤ 14 V, Dr4_I = V _{RO}			70	Ω
Dr2 dynamic clamp voltage	CLV1	Note 1			32	V
Dr4 output voltage	CLV2	Dr4			16	V
Dr4 limited current	CLi4	Peak Current when I _o increase	(40)			mA
Dr2 input clamp voltage	CLV3	I _n ≤ 400 μA	5		8	V
Pull down resistance	Dr_Rdown	Dr1_I, Dr3_I, Dr4_I	50	100	200	kΩ
High level input voltage	V _{IH_Dr1}	Dr1_I, Dr3_I, Dr4_I	0.7V _{RO}		V _{RO}	V
	V _{IH_Dr2}	Dr2n_I	4		CLV3	V
Low level input voltage	V _{IL_Dr1}	Dr1_I, Dr3_I, Dr4_I	0		0.3V _{RO}	V
	V _{IL_Dr2}	Dr2n_I, I _o ≤ 2 mA	0		1.5	V
High level input leak current ^{Note 2}	I _{LIHD1}	Dr1_I, Dr3_I, Dr4_I, V _i = 5 V			105	μA
	I _{LIHD2}	Dr2n_I, V _i = 5 V			300	μA
Low level input leak current	I _{LILD}	Dr1_I, Dr2n_I, Dr3_I, Dr4_I, V _i = 0 V	-3			μA
Output off leak current	I _{OHD1}	Dr1, Dr2n, Dr3, V _o = 19 V			10	μA
	I _{OHD2}	Dr4, V _o = 0 V	-10			μA

- Notes 1.** When V_{SUP} is more than 28V, turn on or turn off the operation of Dr21 and Dr22 are prohibited, because the dynamic clamp circuit does not operate under this condition.
- 2.** Including the current flowing into the Pull down resistance.

- Remarks 1.** The values in parentheses are design guaranteed values for which no shipping test has been performed.
- 2.** Dr2n_I: n = 1, 2

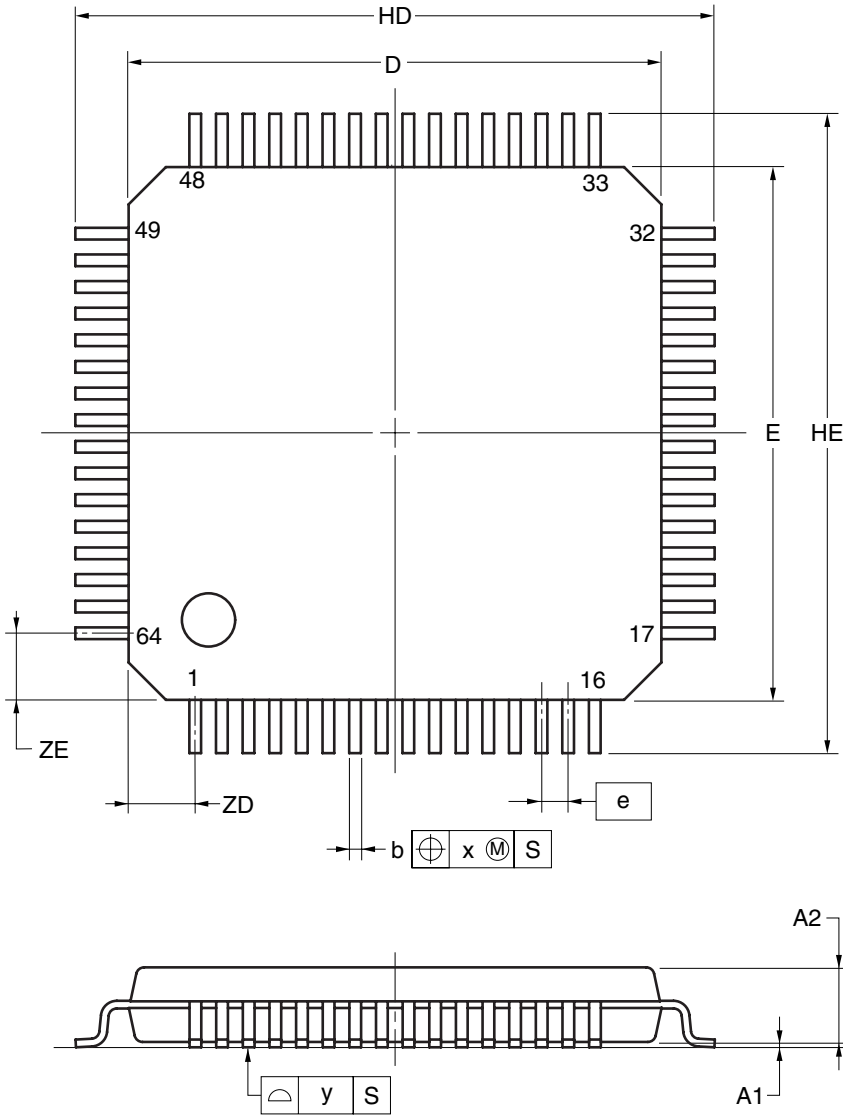
Switch Input Circuit Characteristics

(TA = -40 to +85°C, 7 V ≤ V_{SUP} ≤ 19 V, 4.85 V ≤ V_{RO} ≤ 5.15 V, I_{RO} ≤ 15 mA)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High level input voltage	V _{IHW1}	SWI	0.7V _{SUP}		V _{SUP}	V
Low level input voltage	V _{ILW1}	SWI	0		0.3V _{SUP}	V
High level output voltage	V _{OHW}	ES, I _{oH} = -3 mA	V _{RO} -0.7			V
Low level output voltage	V _{OLW}	ES, I _{oL} = 3 mA			0.7	V
High level input leak current	I _{LIHW1}	SWI, V _i = V _{SUP}			3	μA
Low level input leak current	I _{LILW1}	SWI, V _i = GND	-3			μA

CHAPTER 10 PACKAGE DRAWING

64-PIN PLASTIC LQFP(FINE PITCH)(10x10)



detail of lead end

(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.20 ^{+0.07} _{-0.03}
c	0.125 ^{+0.075} _{-0.025}
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	3° ^{+5°} _{-3°}
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

P64GB-50-GAH

NOTE

Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

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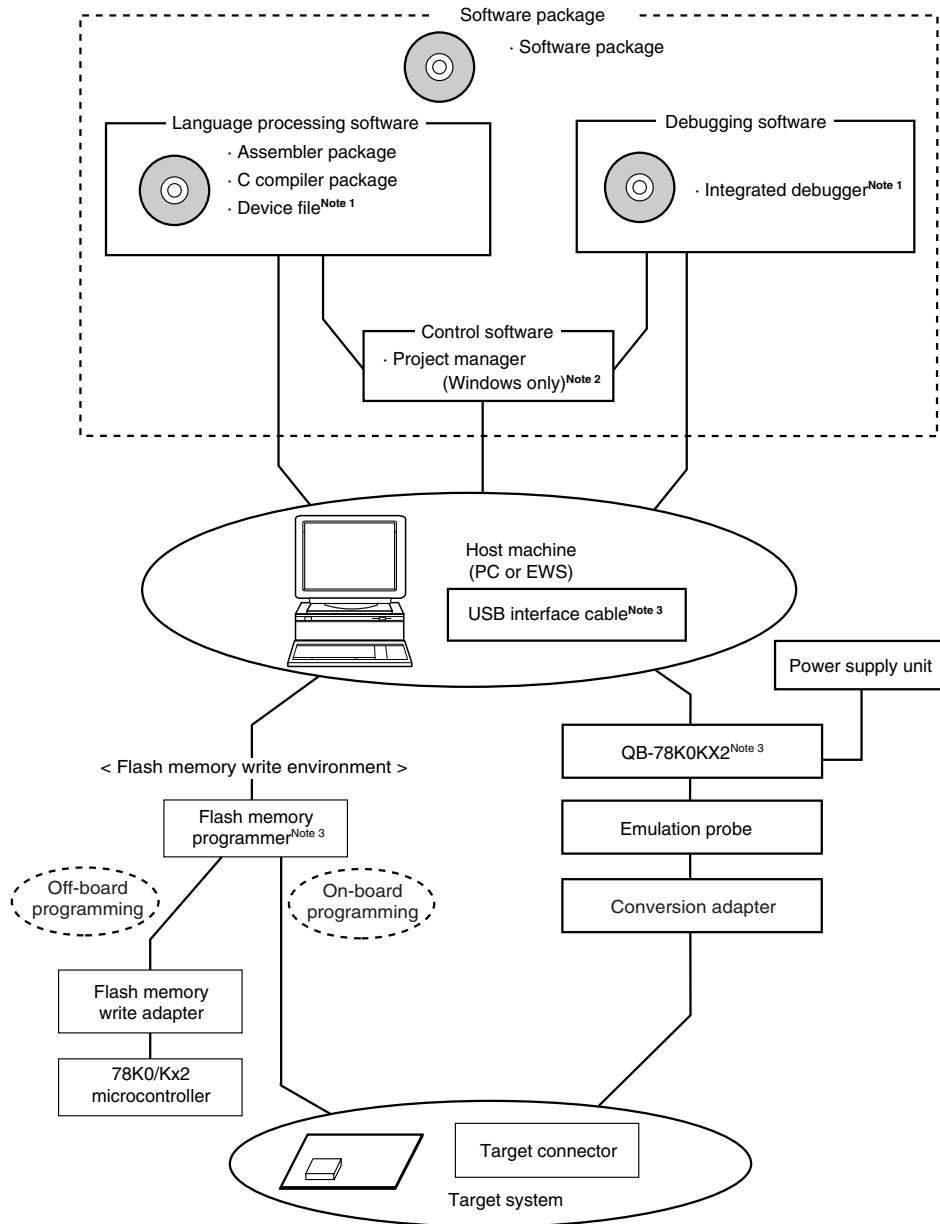
APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for the development of systems that employ the μ PD78F8017A, 78F8018A, 78F8019A, 78F8020A, and 78F8020DA.

Figure A-1 shows the development tool configuration.

Figure A-1. Development Tool Configuration (1/2)

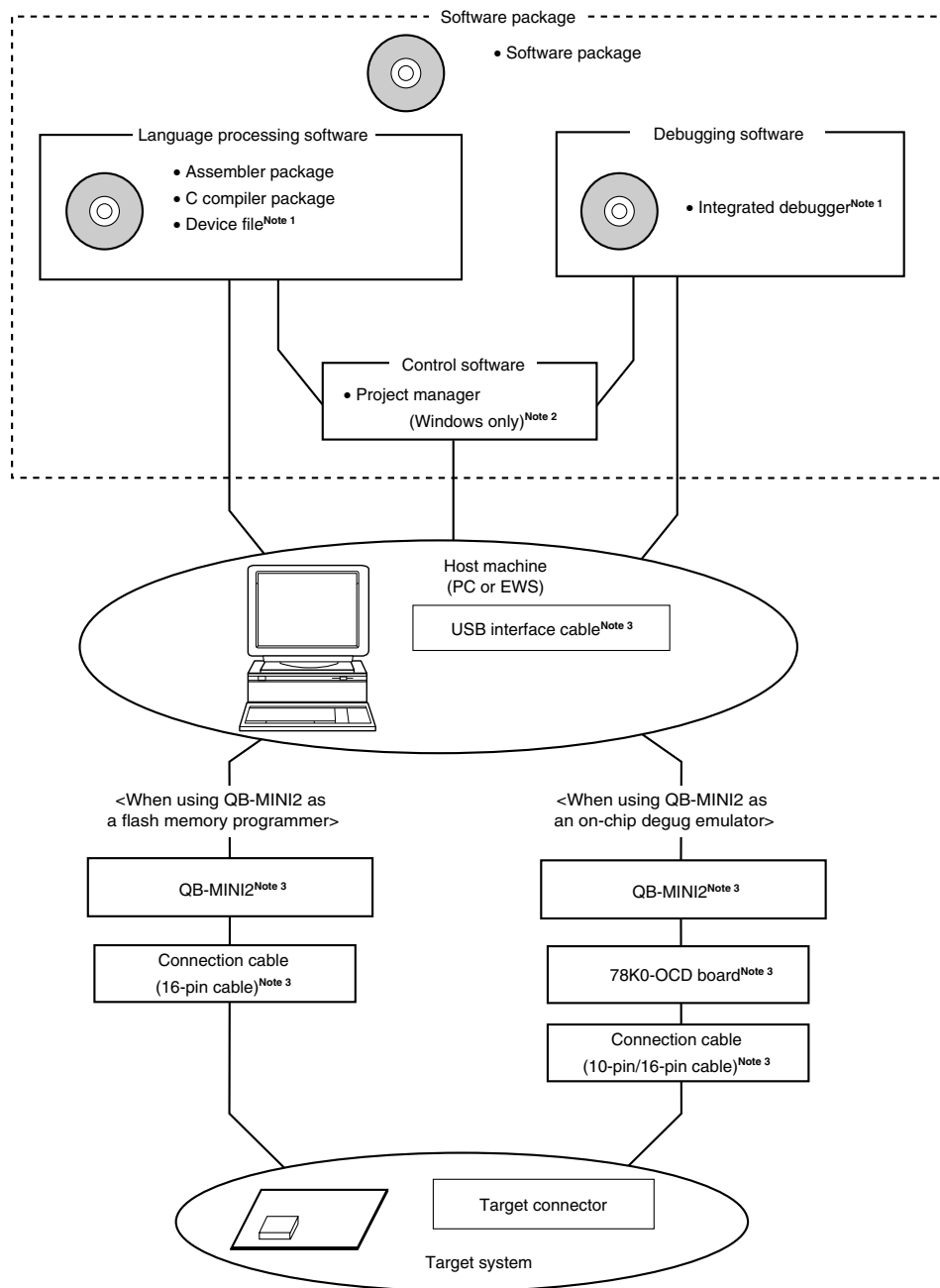
(1) When using the in-circuit emulator QB-78K0KX2



- Notes**
1. Download the device file for μ PD78F8017A, 78F8018A, 78F8019A, 78F8020A, and 78F8020DA (DF788020) and the integrated debugger ID78K0-QB from the download site for development tools (<http://www.necel.com/micro/en/ods/index.html>).
 2. The project manager PM+ is included in the assembler package. PM+ cannot be used other than with Windows™.
 3. QB-78K0KX2 is supplied with the integrated debugger ID78K0-QB, a USB interface cable, the on-chip debug emulator with programming function QB-MINI2, connection cables (10-pin and 16-pin cables), and the 78K0-OCD board. Any other products are sold separately.

Figure A-1. Development Tool Configuration (2/2)

(2) When using the on-chip debug emulator with programming function QB-MINI2



- Notes**
1. Download the device file for μ PD78F8017A, 78F8018A, 78F8019A, 78F8020A, and 78F8020DA (DF788020) and the integrated debugger ID78K0-QB from the download site for development tools (<http://www.necel.com/micro/en/ods/index.html>).
 2. The project manager PM+ is included in the assembler package. PM+ cannot be used other than with Windows.
 3. QB-MINI2 is supplied with USB interface cable, connection cables (10-pin cable and 16-pin cable), and 78K0-OCD board. Any other products are sold separately. In addition, download the software for operating the QB-MINI2 from the download site for development tools (<http://www.necel.com/micro/en/ods/index.html>).

A.1 Software Package

<p>SP78K0 78K0 microcontroller software package</p>	<p>Development tools (software) common to the 78K0 microcontrollers are combined in this package.</p>
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A.2 Language Processing Software

<p>RA78K0 ^{Note 1} Assembler package</p>	<p>This assembler converts programs written in mnemonics into object codes executable with a microcontroller. This assembler is also provided with functions capable of automatically creating symbol tables and branch instruction optimization. This assembler should be used in combination with a device file (DF788020). <Precaution when using RA78K0 in PC environment> This assembler package is a DOS-based application. It can also be used in Windows, however, by using the Project Manager (PM+) on Windows. PM+ is included in assembler package.</p>
<p>CC78K0 ^{Note 1} C compiler package</p>	<p>This compiler converts programs written in C language into object codes executable with a microcontroller. This compiler should be used in combination with an assembler package and device file. <Precaution when using CC78K0 in PC environment> This C compiler package is a DOS-based application. It can also be used in Windows, however, by using the Project Manager (PM+) on Windows. PM+ is included in assembler package.</p>
<p>DF788020 ^{Note 2} Device file</p>	<p>This file contains information peculiar to the device. This device file should be used in combination with a tool (RA78K0, CC78K0, ID78K0-QB, and the system simulator). The corresponding OS and host machine differ depending on the tool to be used.</p>

- Notes**
1. If the versions of RA78K0 and CC78K0 are Ver.4.00 or later, different versions of RA78K0 and CC78K0 can be installed on the same machine.
 2. The DF788020 can be used in common with the RA78K0, CC78K0, ID78K0-QB, and the system simulator. Download the DF788020 from the download site for development tools (<http://www.necel.com/micro/en/ods/index.html>).

A.3 Flash Memory Programming Tools

A.3.1 When using flash memory programmer FG-FP5, FL-PR5, FG-FP4, and FL-PR4

FG-FP5, FL-PR5, PG-FP4 ^{Note} , FL-PR4 Flash memory programmer	Flash memory programmer dedicated to microcontrollers with on-chip flash memory.
FA-78F8020GB-GAH-MX Flash memory programming adapter	Flash memory programming adapter used connected to the flash memory programmer for use. FA-78F8020GB-GAH-MX: For 64-pin plastic LQFP

Note Phase-out

- Remarks 1.** FL-PR5, FL-PR4, and FA-78F8020GB-GAH-MX are products of Naito Densai Machida Mfg. Co., Ltd (<http://www.ndk-m.co.jp/>, TEL: +81-42-750-4172).
- 2.** Use the latest version of the flash memory programming adapter.

A.3.2 When using on-chip debug emulator with programming function QB-MINI2

QB-MINI2 On-chip debug emulator with programming function	This is a flash memory programmer dedicated to microcontrollers with on-chip flash memory. It is available also as on-chip debug emulator which serves to debug hardware and software when developing application systems using the 78K0/Kx2 microcontrollers. When using this as flash memory programmer, it should be used in combination with a connection cable (16-pin cable) and a USB interface cable that is used to connect the host machine.
Target connector specifications	16-pin general-purpose connector (2.54 mm pitch)

- Remarks 1.** The QB-MINI2 is supplied with a USB interface cable and connection cables (10-pin cable and 16-pin cable), and the 78K0-OCD board. A connection cable (10-pin cable) and the 78K0-OCD board are used only when using the on-chip debug function.
- 2.** Download the software for operating the QB-MINI2 from the download site for development tools (<http://www.necel.com/micro/en/ods/index.html>).

A.4 Debugging Tools (Hardware)

A.4.1 When using in-circuit emulator QB-78K0KX2

QB-78K0KX2 In-circuit emulator	This in-circuit emulator serves to debug hardware and software when developing application systems using the 78K0/Kx2 microcontrollers. It supports to the integrated debugger (ID78K0-QB). This emulator should be used in combination with a power supply unit and emulation probe, and the USB is used to connect this emulator to the host machine.
QB-80-EP-01T Emulation probe	This emulation probe is flexible type and used to connect the in-circuit emulator and target system.
QB-788020-EA-01T, Exchange adapter	This exchange adapter is used to perform pin conversion from the in-circuit emulator to target connector. Exchange adapter has the LIN transceiver, voltage regulator and driver functions.
QB-64GB-YS-01T, Space adapter	This space adapter is used to adjust the height between the target system and in-circuit emulator. QB-64GB-YS-01T: 64-pin plastic LQFP
QB-64GB-YQ-01T, YQ connector	This YQ connector is used to connect the target connector and exchange adapter. QB-64GB-YQ-01T: 64-pin plastic LQFP
QB-64GB-HQ-01T, Mount adapter	This mount adapter is used to mount the target device with socket. QB-64GB-HQ-01T: 64-pin plastic LQFP
QB-64GB-NQ-01T, Target connector	This target connector is used to mount on the target system. QB-64GB-NQ-01T: 64-pin plastic LQFP

Remark The QB-78K0KX2 is supplied with the integrated debugger ID78K0-QB, a USB interface cable, the on-chip debug emulator QB-MINI2, connection cables (10-pin and 16-pin cables), and the 78K0-OCD board.

Download the software for operating the QB-MINI2 from the download site for development tools (<http://www.necel.com/micro/en/ods/index.html>) when using the QB-MINI2.

A.4.2 When using on-chip debug emulator with programming function QB-MINI2

QB-MINI2 On-chip debug emulator with programming function	This on-chip debug emulator serves to debug hardware and software when developing application systems using the 78K0/Kx2. It is available also as flash memory programmer dedicated to microcontrollers with on-chip flash memory. When using this as on-chip debug emulator, it should be used in combination with a connection cable (10-pin cable or 16-pin cable), a USB interface cable that is used to connect the host machine, and the 78K0-OCD board.
Target connector specifications	10-pin general-purpose connector (2.54 mm pitch) or 16-pin general-purpose connector (2.54 mm pitch)

Remarks 1. The QB-MINI2 is supplied with a USB interface cable and connection cables (10-pin cable and 16-pin cable), and the 78K0-OCD board. A connection cable (10-pin cable) and the 78K0-OCD board are used only when using the on-chip debug function.

2. Download the software for operating the QB-MINI2 from the download site for development tools (<http://www.necel.com/micro/en/ods/index.html>).

A.5 Debugging Tools (Software)

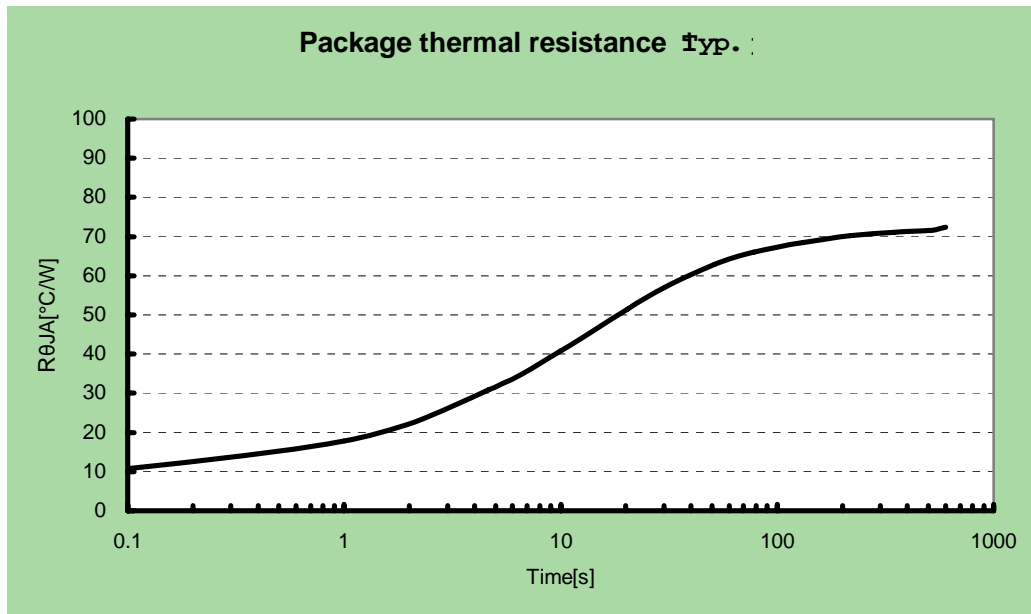
ID78K0-QB ^{Note} Integrated debugger	This debugger supports the in-circuit emulators for the 78K0 microcontrollers. The ID78K0-QB is Windows-based software. It has improved C-compatible debugging functions and can display the results of tracing with the source program using an integrating window function that associates the source program, disassemble display, and memory display with the trace result. It should be used in combination with the device file (DF788020).
--	---

Note Download the ID78K0-QB from the download site for development tools (<http://www.necel.com/micro/en/ods/index.html>).

APPENDIX B PACKAGE THERMAL RESISTANCE

Conditions

Board size : 100 × 100 mm 1.6 mm thickness
Wiring : 2 layers (0.033 mm thickness)
Wiring density : 50%
Material : FR4



APPENDIX C CALCULATION EXAMPLE OF POWER DISSIPATION AND JUNCTION TEMPERATURE

Calculation Example of Total Power Dissipation

Conditions

$$V_{SUP} = 12 \text{ V}$$

$$I_{RO} = 15 \text{ mA}$$

LIN = Normal mode

$$T_A = 85^\circ\text{C}$$

$$P1 = V_{SUP} \times I_{BAT3} = 36 \text{ mW}$$

$$P2 = (V_{SUP} - V_{RO}) \times I_{RO} = 105 \text{ mW}$$

$$P3 = V_{RO} \times I_{DD} = 75 \text{ mW}$$

$R_{ON} \times I_o^2$ does the dissipation of one driver.

If only 1 ch is on for Dr2, P4 will be as the following:

$$P4 = R_{ON} \times I^2$$

$$= Dr1_R_{ON} \times I_o^2 + Dr2_R_{ON} \times I_o^2 + Dr3_R_{ON} \times I_o^2 + Dr4_R_{ON} \times I_o^2$$

$$= 10 \text{ mW} + 100 \text{ mW} + 25 \text{ mW} + 18 \text{ mW}$$

$$= 153 \text{ mW}$$

$$PD = P1 + P2 + P3 + P4 = 369 \text{ mW}$$

Calculation Example of Junction Temperature

$$T_j = PD \times R_{\theta JA}^{\text{Note}} + T_A$$

$$= 113^\circ\text{C}$$

Note $R_{\theta JA}$ uses the value of Package thermal resistance (Appendix B T is more than 400 sec).

Caution Please make sure not to go beyond 140°C.

APPENDIX D REVISION HISTORY

D.1 Main Revisions in this Edition

Page	Description
p.14	Change of Part Number

D.2 Revision History of Preceding Editions

Here is the revision history of the preceding editions. Chapter indicates the chapter of each edition.

(1/3)

Edition	Description	Chapter
2nd	Change of item μ PD78F8020AD→ μ PD78F8020DA	Throughout
	Change of item μ PD78F0534, 78F0535, 78F0536, 78F0537, 78F0537A→ μ PD78F0534A, 78F0535A, 78F0536A, 78F0537A, 78F0537DA	
	Addition of Flash Memory Programmer PG-FP5	
	Change of To know details of the microcontroller part	INTRODUCTION
	Change of Documents Related to Devices	
	Change of Documents Related to Development Tools (Hardware) (User's Manuals)	
	Change of Documents Related to Flash Memory Programming	
	Change of the explanation and Note 1 in 1.1 Features	CHAPTER 1 OUTLINE
	Change of 1.4 Pin Configuration (Top View)	
	Change of Pin Identification	
	Change of 1.5 Block Diagram	
	Change of 1.5.2 Analog block diagram	
	Change of 1.6 Outline of Functions	
	Change of 2.2 Analog Part Pins	CHAPTER 2 PIN FUNCTIONS
	Change of 2.3.3 (2) Control mode	
	Change of Remark in 2.3.4 (2) (c) TO51	
	Change of Remark in 2.3.7 (2) (d) EXCLK	
	Change of 2.3.15 Dr1, Dr21, Dr22, Dr3, Dr4	
	Change of 2.3.16 Dr1_I, Dr21_I, Dr22_I, Dr3_I, Dr4_I and Table 2-2. Truth Table	
	Addition of 2.3.28 N.C (Non-connection)	
	Change of Table 2-3. Pin I/O Circuit Types	CHAPTER 3 MICROCONTROLLER FUNCTIONS
	Change of the explanation in CHAPTER 3 MICROCONTROLLER FUNCTIONS	
	Deletion of Dropper select function in CHAPTER 5 POWER SUPPLY CIRCUIT	CHAPTER 5 POWER SUPPLY CIRCUIT
	Change of 5.2 Power Supply Over Current Protection Function	
	Change of 7.2 High Side Driver and Table 7-1. Truth Table	CHAPTER 7 DRIVER CIRCUIT
	Change of Figure 7-2. High Side Driver Circuit Application Example	

Edition	Description	Chapter
2nd	Addition of Caution 2 in CHAPTER 9 ELECTRICAL SPECIFICATIONS (A) GRADE PRODUCTS (TARGET)	CHAPTER 9 ELECTRICAL SPECIFICATIONS (A) GRADE PRODUCTS (TARGET)
	9.1 Absolute Maximum Ratings Change of Absolute Maximum Ratings for Microcontroller Block ($T_A = 25^\circ\text{C}$) Change of Absolute Maximum Ratings for Analog Block ($T_A = 25^\circ\text{C}$)	
	9.2 Microcontroller Block Characteristics Change of A/D Converter Characteristics Addition of Remark in 2.7 V POC Circuit Characteristics ($T_A = 0$ to $+85^\circ\text{C}$, $V_{SS} = 0$ V) Change of table and Note 1 , addition of Note 4 to 6 in Flash Memory Programming Characteristics	
	9.3 Analog Block Characteristics Change of Voltage regulator circuit characteristics Change of Supply current Characteristics Change of DC Characteristics in LIN Transceiver circuit Characteristics Change of AC Characteristics in LIN Transceiver circuit Characteristics and Figure 9-1. Duty Cycle Change of Driver circuit Characteristics in LIN Transceiver circuit Characteristics Change of Switch Input Circuit Characteristics in LIN Transceiver circuit Characteristics	
	Change of Note 3 in Figure A-1. Development Tool Configuration (1/3) (1) When using the in-circuit emulator QB-78K0KX2	APPENDIX A DEVELOPMENT TOOLS
	Addition of Figure A-1. Development Tool Configuration (3/3) (3) When using the on-chip debug emulator with programming function QB-MINI2	
	Addition of A.4.1 When using flash memory programmer FG-FP5, FL-PR5, FG-FP4, FL-PR4, PG-FPL3, and FP-LITE3	
	Addition of A.4.2 When using on-chip debug emulator with programming function QB-MINI2	
	Change of Note in A.5.1 When using in-circuit emulator QB-78K0KX2	
	Addition of A.5.3 When using on-chip debug emulator with programming function QB-MINI2	APPENDIX C CALCULATION EXAMPLE OF POWER DISSIPATION AND JUNCTION TEMPERATURE
Change of APPENDIX C CALCULATION EXAMPLE OF POWER DISSIPATION AND JUNCTION TEMPERATURE		
Addition of APPENDIX D REVISION HISTORY	APPENDIX D REVISION HISTORY	
3rd	Deletion of QB-78K0MINI, PG-FPL3, and FP-LITE3 (because of discontinued products)	Throughout
	Change of Related Documents	INTRODUCTION
	Change of 1.6 Outline of Functions	CHAPTER 1 OUTLINE
	Change of 2.3.28 N.C (Non-connection)	CHAPTER 2 PIN FUNCTIONS
	Change of Note 2 in Table 4-1. Wiring Dedicated Flash Programmer	CHAPTER 4 WRITING WITH FLASH PROGRAMMER

Edition	Description	Chapter
3rd	Change of explanation in CHAPTER 7 DRIVER CIRCUIT	CHAPTER 7 DRIVER CIRCUIT
	Change of Absolute Maximum Ratings for Analog Block and Absolute Maximum Ratings for Common Item	CHAPTER 9 ELECTRICAL SPECIFICATIONS (A) GRADE PRODUCTS
	Change of X1 Oscillator Characteristics	
	Change of (1) Basic operation in AC Characteristics	
	Change of (c) IIC0 in (2) Serial interface in AC Characteristics	
	Change of LVI Circuit Characteristics	
	Change of Basic characteristics	
	Change of Supply current Characteristics	
	Change of DC Characteristics	
	Change of AC Characteristics	
	Change of Driver circuit Characteristics and Switch Input Circuit Characteristics	
	Change of APPENDIX A DEVELOPMENT TOOLS	APPENDIX A DEVELOPMENT TOOLS
Addition of D.2 Revision History of Preceding Editions	APPENDIX D REVISION HISTORY	

*For further information,
please contact:*

NEC Electronics Corporation
1753, Shimonumabe, Nakahara-ku,
Kawasaki, Kanagawa 211-8668,
Japan
Tel: 044-435-5111
<http://www.necel.com/>

[America]

NEC Electronics America, Inc.
2880 Scott Blvd.
Santa Clara, CA 95050-2554, U.S.A.
Tel: 408-588-6000
800-366-9782
<http://www.am.necel.com/>

[Europe]

NEC Electronics (Europe) GmbH
Arcadiastrasse 10
40472 Düsseldorf, Germany
Tel: 0211-65030
<http://www.eu.necel.com/>

Hanover Office
Podbielskistrasse 166 B
30177 Hannover
Tel: 0 511 33 40 2-0

Munich Office
Werner-Eckert-Strasse 9
81829 München
Tel: 0 89 92 10 03-0

Stuttgart Office
Industriestrasse 3
70565 Stuttgart
Tel: 0 711 99 01 0-0

United Kingdom Branch
Cygnus House, Sunrise Parkway
Linford Wood, Milton Keynes
MK14 6NP, U.K.
Tel: 01908-691-133

Succursale Française
9, rue Paul Dautier, B.P. 52
78142 Velizy-Villacoublay Cédex
France
Tel: 01-3067-5800

Sucursal en España
Juan Esplandiu, 15
28007 Madrid, Spain
Tel: 091-504-2787

Tyskland Filial
Täby Centrum
Entrance S (7th floor)
18322 Täby, Sweden
Tel: 08 638 72 00

Filiale Italiana
Via Fabio Filzi, 25/A
20124 Milano, Italy
Tel: 02-667541

Branch The Netherlands
Steijgerweg 6
5616 HS Eindhoven
The Netherlands
Tel: 040 265 40 10

[Asia & Oceania]

NEC Electronics (China) Co., Ltd
7th Floor, Quantum Plaza, No. 27 ZhiChunLu Haidian
District, Beijing 100083, P.R.China
Tel: 010-8235-1155
<http://www.cn.necel.com/>

Shanghai Branch
Room 2509-2510, Bank of China Tower,
200 Yincheng Road Central,
Pudong New Area, Shanghai, P.R.China P.C:200120
Tel:021-5888-5400
<http://www.cn.necel.com/>

Shenzhen Branch
Unit 01, 39/F, Excellence Times Square Building,
No. 4068 Yi Tian Road, Futian District, Shenzhen,
P.R.China P.C:518048
Tel:0755-8282-9800
<http://www.cn.necel.com/>

NEC Electronics Hong Kong Ltd.
Unit 1601-1613, 16/F., Tower 2, Grand Century Place,
193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: 2886-9318
<http://www.hk.necel.com/>

NEC Electronics Taiwan Ltd.
7F, No. 363 Fu Shing North Road
Taipei, Taiwan, R. O. C.
Tel: 02-8175-9600
<http://www.tw.necel.com/>

NEC Electronics Singapore Pte. Ltd.
238A Thomson Road,
#12-08 Novena Square,
Singapore 307684
Tel: 6253-8311
<http://www.sg.necel.com/>

NEC Electronics Korea Ltd.
11F., Samik Lavied'or Bldg., 720-2,
Yeoksam-Dong, Kangnam-Ku,
Seoul, 135-080, Korea
Tel: 02-558-3737
<http://www.kr.necel.com/>