Supplement

[Document Name]
µPD780816A Subseries User's Manual

[Document No., Date Published]
U16506EE1V0UD00, February 2003

[Published Department]
Technical Product Support, Semiconductors & Displays Business, Unit NEC Electronics (Europe) GmbH

[Description]

(1) **<p.386>** Add Caution below "**Figure 22-3: Self-Programming and Oscillation Control Register Format**"

<Previous>

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
SPOC	0	0	0	0	0	0	HCSEL1	HCSEL0	FF51H	08H	R/W

HCSEL1	HCSEL0	HALT Mode Clock Select
0	0	$f_X/2^4$ (500 KHz)
0	1	$f_X/2^5$ (250 KHz)
1	0	$f_X/2^6$ (125 KHz)
1	1	$f_X/2^7$ (62.5 KHz)

<New>

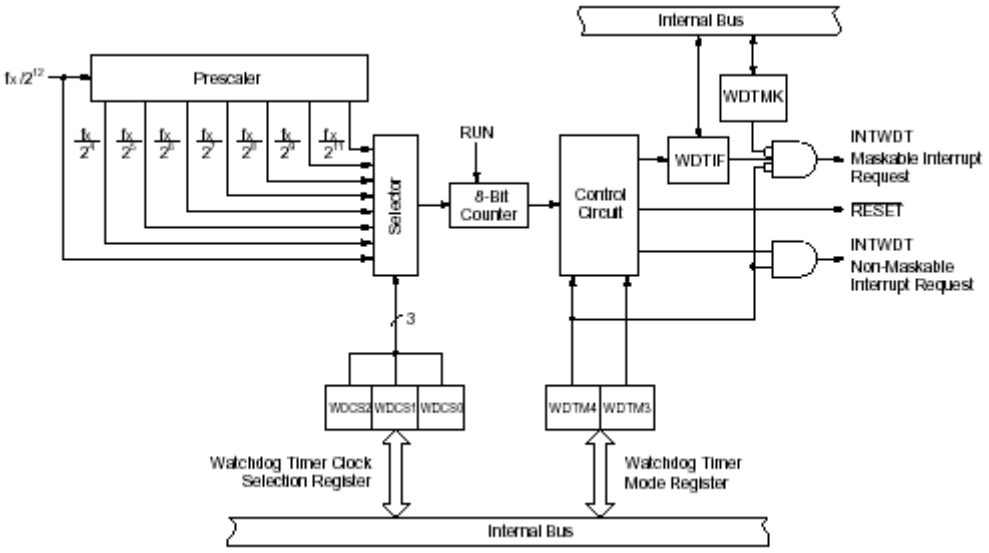
Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
SPOC	0	0	0	0	0	0	HCSEL1	HCSEL0	FF51H	08H	R/W

HCSEL1	HCSEL0	HALT Mode Clock Select
0	0	$f_X/2^4$ (500 KHz)
0	1	$f_X/2^5$ (250 KHz)
1	0	$f_X/2^6$ (125 KHz)
1	1	$f_X/2^7$ (62.5 KHz)

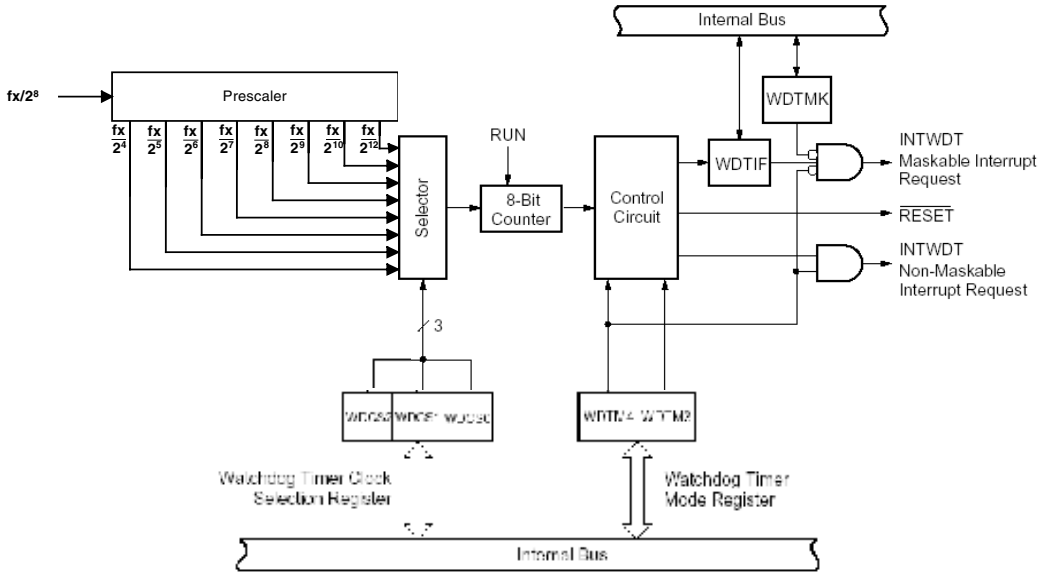
Caution: Be sure to keep bits 2 to 7 = "0".
After Reset the read value of the SPOC register will be 00H.

(2) **<p.191>** Update "**Figure 10-1: Watchdog Timer Block Diagram**"

<Previous>



<New>



(3) **<p.421>** Update "**Target IDD characteristics for µPD780814(A1), µPD780816(A1)**"

<Previous>

(5) µPD780814(A1), µPD780816(A1)
(T_A = -40°C to +110°C, V_{DD} = 4.0 to 5.5 V)

These specifications are only target values and may not be satisfied by mass-produced products.

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Power supply current Note 1	I_{DD1}	f_X = 8 MHz, crystal/ceramic oscillation operating mode (PCC = 00H) Note 2		5.5	11	mA
		f_X = 8 MHz, crystal/ceramic oscillation operating mode (PCC = 00H) Note 3		9.5	19	
	I_{DD2}	f_X = 8 MHz, crystal/ceramic oscillation HALT mode (PCC = 04H) Note 4		0.5	2.0	
		f_X = 8 MHz, crystal/ceramic oscillation HALT mode (PCC = 04H) Note 5		2.5	5.0	
	I_{DD3}	RC oscillation operating mode (f_{XT} = 40 KHz)		150	1560	µA
	I_{DD4}	RC oscillation HALT mode (f_{XT} = 40 KHz)		60	1180	
	I_{DD5}	CL1 = V_{DD} STOP mode		1	1000	

Notes: 1. Current through V_{DD0}, V_{DD1} respectively through V_{SS0}, V_{SS1}.
Excluded is the current through the inside pull-up resistors, through AV_{DD}/AV_{REF}, the port current.

2. CPU is operable.
The other peripherals like: CAN controller, Timer 0, Timer 2, serial interfaces, A/D converter etc. are stopped.

3. CPU and all peripherals (except for the A/D converter) are in operating mode and PCL output is f_X.

4. CPU is in HALT mode and all other peripherals (except Watch timer) are stopped.

5. CPU is in HALT mode, but the following peripherals are active:
Timer 2, all other timers, serial interfaces, and PCL output is f_X.

Remarks: 1. f_X: Main system clock oscillation frequency.

2. f_{XT}: Subsystem clock oscillation frequency.

3. The typical values are with respect to T_A = 25°C.

<New>

(5) μPD780814(A1), μPD780816(A1)
(T_A = -40°C to +110°C, V_{DD} = 4.0 to 5.5 V)

These specifications are only target values and may not be satisfied by mass-produced products.

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Power supply current Note 1	I_{DD1}	f_X = 8 MHz, crystal/ceramic oscillation operating mode (PCC = 00H) Note 2		5.5	**12**	mA
		f_X = 8 MHz, crystal/ceramic oscillation operating mode (PCC = 00H) Note 3		9.5	**20**	
	I_{DD2}	f_X = 8 MHz, crystal/ceramic oscillation HALT mode (PCC = 04H) Note 4		0.5	2.0	
		f_X = 8 MHz, crystal/ceramic oscillation HALT mode (PCC = 04H) Note 5		2.5	**6**	
	I_{DD3}	RC oscillation operating mode (f_{XT} = 40 KHz)		150	1560	μA
	I_{DD4}	RC oscillation HALT mode (f_{XT} = 40 KHz)		60	1180	
	I_{DD5}	CL1 = V_{DD} STOP mode		1	1000	

Notes: 1. Current through V_{DD0}, V_{DD1} respectively through V_{SS0}, V_{SS1}.
Excluded is the current through the inside pull-up resistors, through AV_{DD}/AV_{REF}, the port current.

2. CPU is operable.
The other peripherals like: CAN controller, Timer 0, Timer 2, serial interfaces, A/D converter etc. are stopped.

3. CPU and all peripherals (except for the A/D converter) are in operating mode and PCL output is f_X.

4. CPU is in HALT mode and all other peripherals (except Watch timer) are stopped.

5. CPU is in HALT mode, but the following peripherals are active:
Timer 2, all other timers, serial interfaces, and PCL output is f_X.

Remarks: 1. f_X: Main system clock oscillation frequency.

2. f_{XT}: Subsystem clock oscillation frequency.

3. The typical values are with respect to T_A = 25°C.

(4) **<p.423>** Update "**IDD characteristics for µPD780814(A2), µPD780816(A2)**"

<Previous>

(5) µPD780814(A1), µPD780816(A1)
(T_A = -40°C to +110°C, V_{DD} = 4.0 to 5.5 V)

These specifications are only target values and may not be satisfied by mass-produced products.

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Power supply current Note 1	I_{DD1}	f_X = 8 MHz, crystal/ceramic oscillation operating mode (PCC = 00H) Note 2		5.5	11	mA
		f_X = 8 MHz, crystal/ceramic oscillation operating mode (PCC = 00H) Note 3		9.5	19	
	I_{DD2}	f_X = 8 MHz, crystal/ceramic oscillation HALT mode (PCC = 04H) Note 4		0.5	2.0	
		f_X = 8 MHz, crystal/ceramic oscillation HALT mode (PCC = 04H) Note 5		2.5	5.0	
	I_{DD3}	RC oscillation operating mode (f_{XT} = 40 KHz)		150	1560	µA
	I_{DD4}	RC oscillation HALT mode (f_{XT} = 40 KHz)		60	1180	
	I_{DD5}	CL1 = V_{DD} STOP mode		1	1000	

Notes: 1. Current through V_{DD0}, V_{DD1} respectively through V_{SS0}, V_{SS1}.
Excluded is the current through the inside pull-up resistors, through AV_{DD}/AV_{REF}, the port current.

2. CPU is operable.
The other peripherals like: CAN controller, Timer 0, Timer 2, serial interfaces, A/D converter etc. are stopped.

3. CPU and all peripherals (except for the A/D converter) are in operating mode and PCL output is f_X.

4. CPU is in HALT mode and all other peripherals (except Watch timer) are stopped.

5. CPU is in HALT mode, but the following peripherals are active:
Timer 2, all other timers, serial interfaces, and PCL output is f_X.

Remarks: 1. f_X: Main system clock oscillation frequency.

2. f_{XT}: Subsystem clock oscillation frequency.

3. The typical values are with respect to T_A = 25°C.

<New>

(5) μPD780814(A1), μPD780816(A1)
(T_A = -40°C to +110°C, V_{DD} = 4.0 to 5.5 V)

These specifications are only target values and may not be satisfied by mass-produced products.

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Power supply current Note 1	I_{DD1}	f_X = 8 MHz, crystal/ceramic oscillation operating mode (PCC = 00H) Note 2		5.5	**12**	mA
		f_X = 8 MHz, crystal/ceramic oscillation operating mode (PCC = 00H) Note 3		9.5	**20**	
	I_{DD2}	f_X = 8 MHz, crystal/ceramic oscillation HALT mode (PCC = 04H) Note 4		0.5	2.0	
		f_X = 8 MHz, crystal/ceramic oscillation HALT mode (PCC = 04H) Note 5		2.5	**6**	
	I_{DD3}	RC oscillation operating mode (f_{XT} = 40 KHz)		150	1560	μA
	I_{DD4}	RC oscillation HALT mode (f_{XT} = 40 KHz)		60	1180	
	I_{DD5}	CL1 = V_{DD} STOP mode		1	1000	

Notes: 1. Current through V_{DD0}, V_{DD1} respectively through V_{SS0}, V_{SS1}.
Excluded is the current through the inside pull-up resistors, through AV_{DD}/AV_{REF}, the port current.

2. CPU is operable.
The other peripherals like: CAN controller, Timer 0, Timer 2, serial interfaces, A/D converter etc. are stopped.

3. CPU and all peripherals (except for the A/D converter) are in operating mode and PCL output is f_X.

4. CPU is in HALT mode and all other peripherals (except Watch timer) are stopped.

5. CPU is in HALT mode, but the following peripherals are active:
Timer 2, all other timers, serial interfaces, and PCL output is f_X.

Remarks: 1. f_X: Main system clock oscillation frequency.

2. f_{XT}: Subsystem clock oscillation frequency.

3. The typical values are with respect to T_A = 25°C.

(5) **<p.424>, <p426>, <p428>** Update "**Note 2 of 24.6.1 Basic operation**"

<Previous>

2. f_{SMP2} (sampling clock) = fx/4, fx/6, fx/32, fx/128

<New>

2. f_{SMP2} (sampling clock) = fx/4, fx/**8**, fx/32, fx/128