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RENESAS

User's Manual

μPD71312

LCD Controller/Driver Dedicated to 78K0/Kx2 and 78K0R/Kx3

μPD71312

Document No. U18438EJ2V0UD00 (2nd edition)
Date Published May 2008 NS

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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[MEMO]

INTRODUCTION

Readers

This manual is intended for user engineers who wish to understand the functions of the μPD71312 and design and develop application systems and programs for these devices.

Purpose

This manual is intended to give users an understanding of the functions described in the **Organization** below.

Organization

The μPD71312 manual is divided into the following sections.

μPD71312 **User's Manual**

- Pin functions
- Internal block functions
- Other on-chip peripheral functions
- Electrical specifications

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

- To gain a general understanding of functions:
  → Read this manual in the order of the **CONTENTS**.
- To know details of the 78K/0 microcontrollers instructions:
  → Refer to the separate document **78K/0 Series Instructions User's Manual (U12326E)**.

Conventions

Data significance:	Higher digits on the left and lower digits on the right	
Active low representations:	$\overline{\times\times\times}$ (overscore over pin and signal name)	
Note:	Footnote for item marked with **Note** in the text	
Caution:	Information requiring particular attention	
Remark:	Supplementary information	
Numerical representations:	Binary	···×××× or ××××B
	Decimal	···××××
	Hexadecimal	···××××H

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CHAPTER 1 OUTLINE

1.1 Features

- Operating frequency: 400 kHz (MAX.)
- LCD driver
  Resistance division method/Internal voltage boosting method
  Common signals: 4 (dynamic display)
  Segment signals: 36 (52-pin product), 40 (64-pin product)
- Communication mode: I^2C (400 kbps (MAX.))[Note]
- Power supply voltage: LV_{DD} = 1.8 to 5.5 V
- Operating ambient temperature: T_A = −40 to +85°C

Note Only communication with IIC0 of the 78K0/Kx2 and 78K0R/Kx3 is possible.
It does not support the simplified IIC of the 78K0R/Kx3.

1.2 Applications

APS cameras, digital cameras, AV equipments, and household electrical appliances, etc.

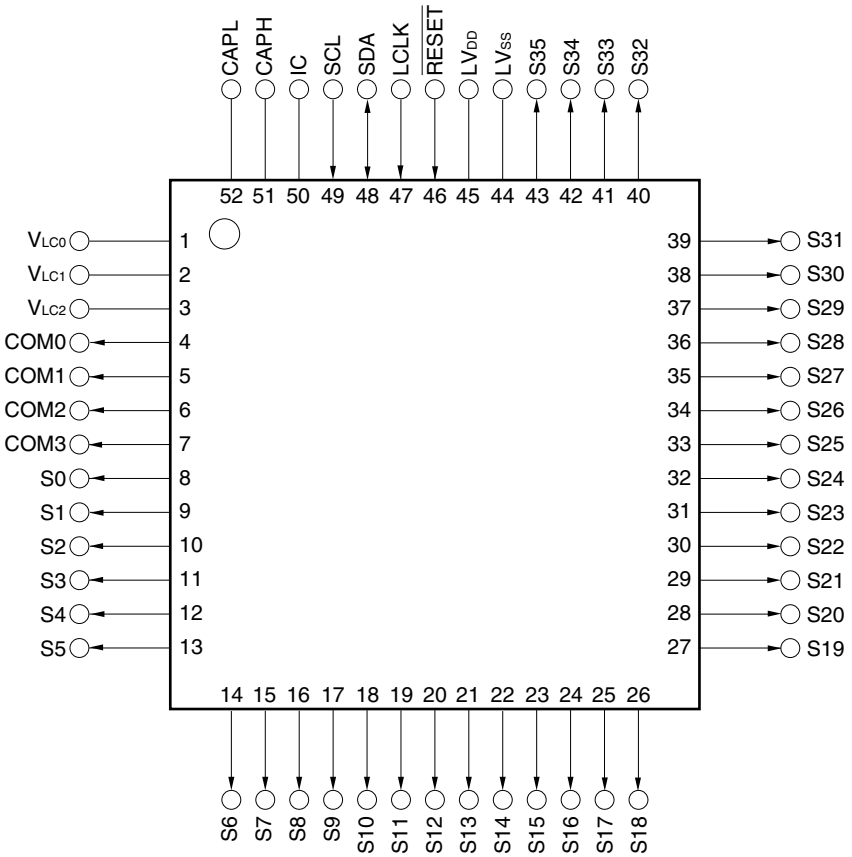
1.3 Ordering Information

- **Flash memory version (Lead-free products)**

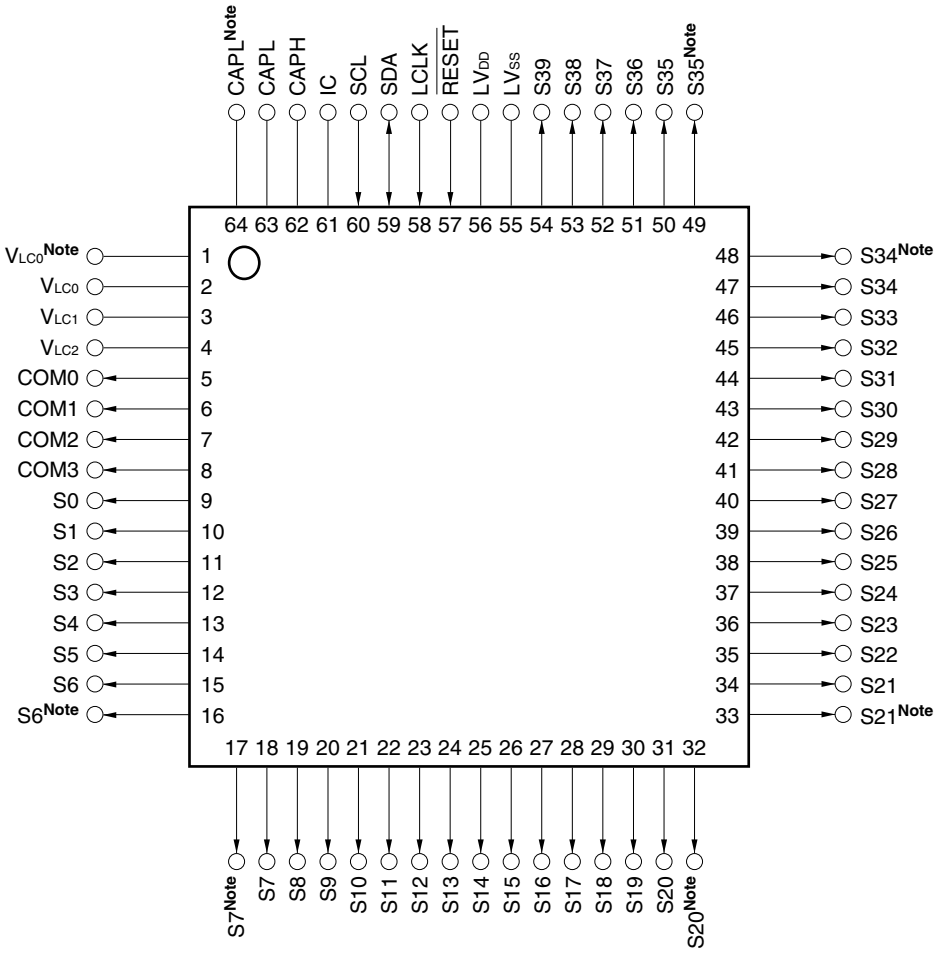
Part Number	Package
μPD71312GB-UET-A	52-pin plastic LQFP (10 × 10)
μPD71312GB-UEU-A	64-pin plastic LQFP (10 × 10)

1.4 Pin Configuration (Top View)

- 52-pin plastic LQFP (10 × 10)



- 64-pin plastic LQFP (10 × 10)



Note Leave open or connect to an identical pin that is adjacent to this pin.

Pin Identification

CAPH, CAPL:	LCD power supply capacitance control	$\overline{\text{RESET}}$:	Reset
COM0 to COM3:	Common output	S0 to S35, S36 to S39[Note]:	Segment output
IC:	Internally connected	SCL:	Serial clock input
LCLK:	Clock input	SDA:	Serial data input/output
LV_{DD}:	Power supply	V_{LC0} to V_{LC2}:	LCD power supply
LV_{SS}:	Ground		

Note 64-pin product only.

CHAPTER 2 PIN FUNCTIONS

2.1 Pin Function List

Table 2-1. Pin Function List

Pin Name	I/O	Function	After Reset
SDA	I/O	Serial data I/O for serial interface	Input
SCL	Input	Clock input for serial interface	Input
S0 to S35, S36 to S39[Note]	Output	LCD controller/driver segment signal outputs	Output
COM0 to COM3	Output	LCD controller/driver common signal outputs	Output
LV_{DD}	–	Positive power supply for LCD controller/driver	–
LV_{SS}	–	Ground potential for LCD controller/driver	–
V_{LC0} to V_{LC2}	–	LCD drive voltage	–
CAPH	–	LCD drive voltage booster capacitor connection	–
CAPL	–		
$\overline{RESET}$	Input	System reset input	–
LCLK	Input	System clock input	Input
IC	–	Internally connected.	–

Note 64-pin product only.

2.2 Description of Pin Functions

2.2.1 SDA

This is a serial data I/O pin for serial interface (N-ch open-drain).

2.2.2 SCL

This is a serial clock input pin for serial interface (N-ch open-drain).

2.2.3 S0 to S35, S36 to S39[Note]

These pins are the segment signal output pins for the LCD controller/driver.

Note 64-pin product only.

2.2.4 COM0 to COM3

These pins are the common signal output pins for the LCD controller/driver.

2.2.5 LV_{DD}

This is the positive power supply pin for the LCD controller/driver.

2.2.6 LV_{SS}

This is the ground potential pin for the LCD controller/driver.

2.2.7 V_{LC0} to V_{LC2}

These pins are the power supply voltage pins for driving the LCD.

2.2.8 CAPH, CAPL

These pins are the capacitor connection pins for driving the LCD.

2.2.9 $\overline{\text{RESET}}$

This is the active-low system reset input pin.

2.2.10 LCLK

This is the system clock input pin.

The internal pull-down resistor is connected during low-level input to $\overline{\text{RESET}}$ pin.

2.2.11 IC

Internally connected. Connect directly to LV_{SS}.

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

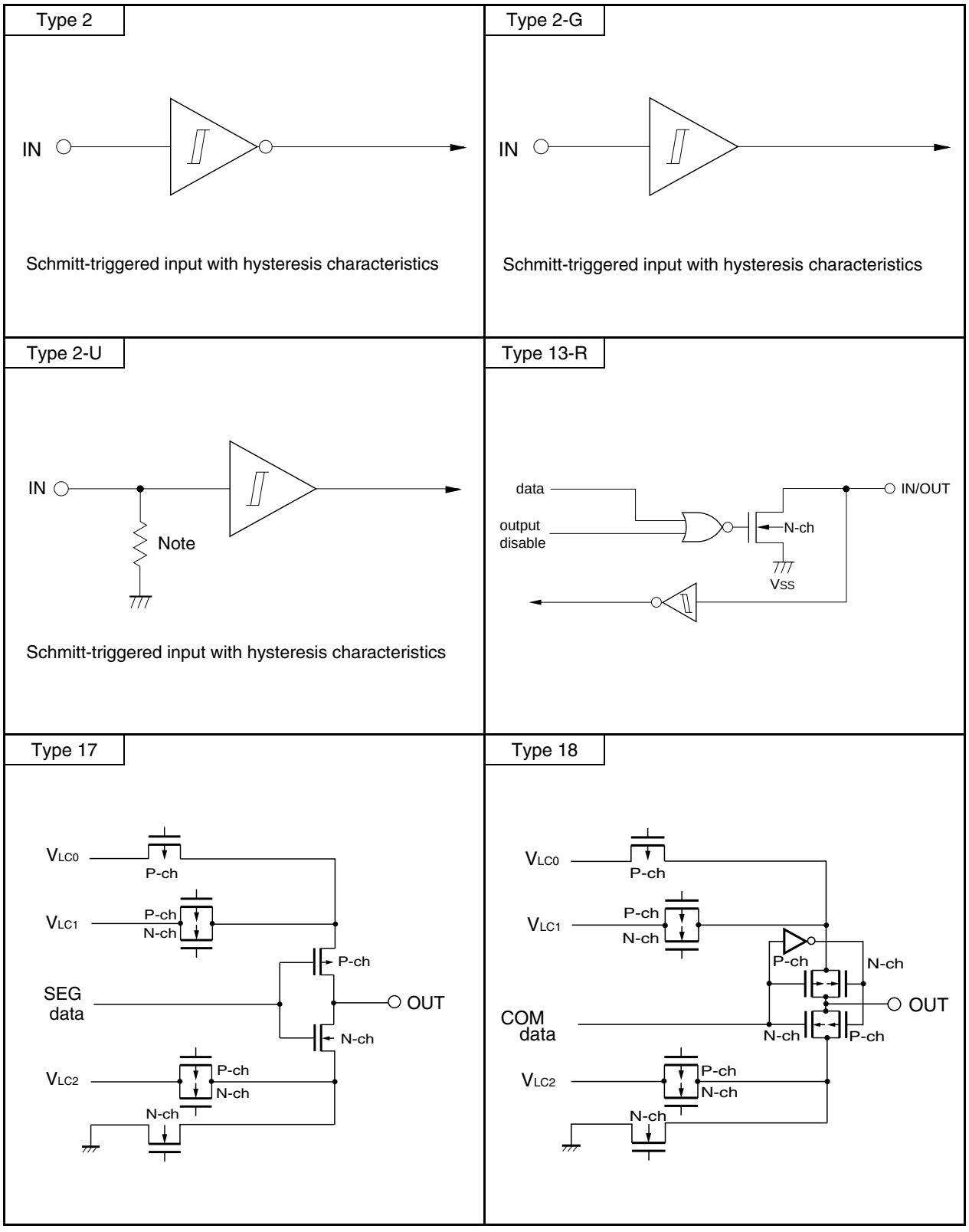
Table 2-2 shows the types of pin I/O circuits and the recommended connections of unused pins.
See **Figure 2-1** for the configuration of the I/O circuit of each type.

Table 2-2. Pin I/O Circuit Types

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
LCLK	2-U	Input	Independently connect to LV_{DD} or LV_{SS} via a resistor.
SCL	2-G		Be sure to pull up externally.
SDA	13-R	I/O	
S0 to S35, S36 to S39[Note]	17	Output	Leave open.
COM0 to COM3	18		
V_{LC0} to V_{LC2}	–	–	
CAPH, CAPL			
$\overline{\text{RESET}}$	2	Input	–
IC	–	–	Connect directly to LV_{SS}.

Note 64-pin product only.

Figure 2-1. Pin I/O Circuit List



Note It is pulled down only during reset.

CHAPTER 3 LCD CONTROLLER/DRIVER

3.1 Functions of LCD Controller/Driver

The functions of the LCD controller/driver in the μPD71312 are as follows.

(1) The LCD driver reference voltage generator can switch internal voltage boosting, external resistance division, and internal resistance division.
(2) Automatic output of segment and common signals based on automatic display data memory read
(3) Five different display modes:
- Static
- 1/2 duty (1/2 bias)
- 1/3 duty (1/2 bias)
- 1/3 duty (1/3 bias)
- 1/4 duty (1/3 bias)

(4) Four different frame frequencies, selectable in each display mode
(5) Segment signal outputs: 36 (S0 to S35) (52-pin product),
40 (S0 to S39) (64-pin product)
Common signal outputs: 4 (COM0 to COM3)

Table 3-1 lists the maximum number of pixels that can be displayed in each display mode.

Table 3-1. Maximum Number of Pixels

(a) 52-pin product

LCD Driver Reference Voltage Generator	Bias Mode	Number of Time Slices	Common Signals Used	Number of Segments	Maximum Number of Pixels
• External resistance division • Internal resistance division	–	Static	COM0 (COM1 to COM3)	36	36 (36 segment signals, 1 common signal)
	1/2	2	COM0, COM1		72 (36 segment signals, 2 common signals)
		3	COM0 to COM2		108 (36 segment signals, 3 common signals)
• Internal voltage boosting • External resistance division • Internal resistance division	1/3	3	COM0 to COM2		
		4	COM0 to COM3		144 (36 segment signals, 4 common signals)

(b) 64-pin product

LCD Driver Reference Voltage Generator	Bias Mode	Number of Time Slices	Common Signals Used	Number of Segments	Maximum Number of Pixels
• External resistance division • Internal resistance division	–	Static	COM0 (COM1 to COM3)	40	40 (40 segment signals, 1 common signal)
	1/2	2	COM0, COM1		80 (40 segment signals, 2 common signals)
		3	COM0 to COM2		120 (40 segment signals, 3 common signals)
• Internal voltage boosting • External resistance division • Internal resistance division	1/3	3	COM0 to COM2		
		4	COM0 to COM3		160 (40 segment signals, 4 common signals)

3.2 Configuration of LCD Controller/Driver

The LCD controller/driver consists of the following hardware.

The LCD controller/driver includes of two blocks: LCDSEG block for controlling segments, and LCDCTL block for controlling LCD register setting and mode setting.

Table 3-2. Configuration of LCD Controller/Driver

Item		Configuration
LCD controller/ driver	Display outputs	Segment signals: 36 (52-pin product), 40 (64-pin product) Common signals: 4 (COM0 to COM3)
	Display block (LCDSEG)	36 byte RAM (52-pin product), 40 byte RAM (64-pin product)
	Control block (LCDCTL)	LCD mode setting register (LCDMD) LCD display mode register (LCDM) LCD clock control register (LCDC) LCD voltage boost control register 0 (VLCG0)

Figure 3-1. Configuration of LCD Controller/Driver

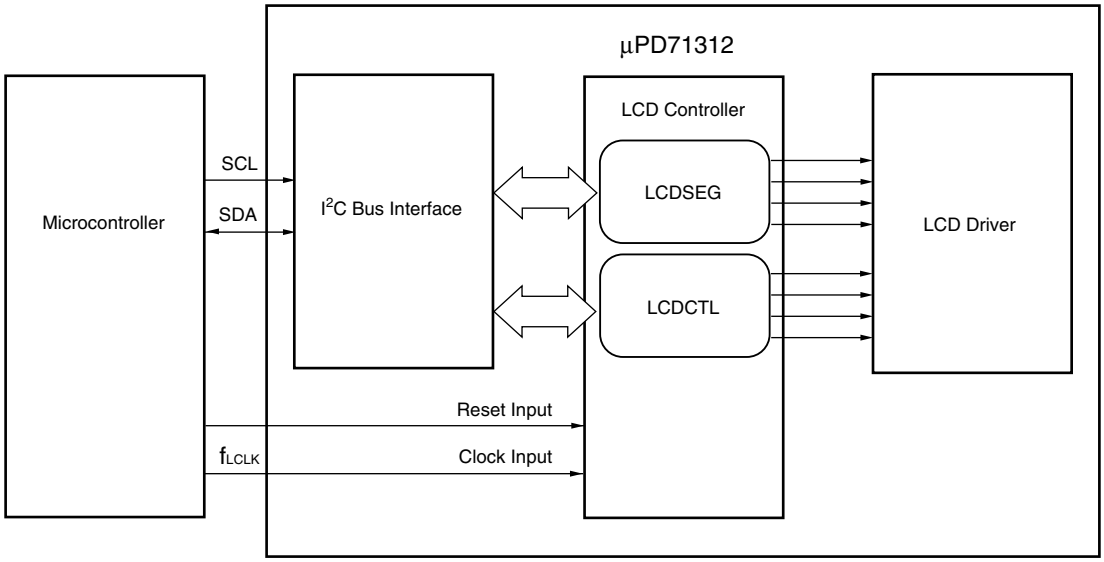
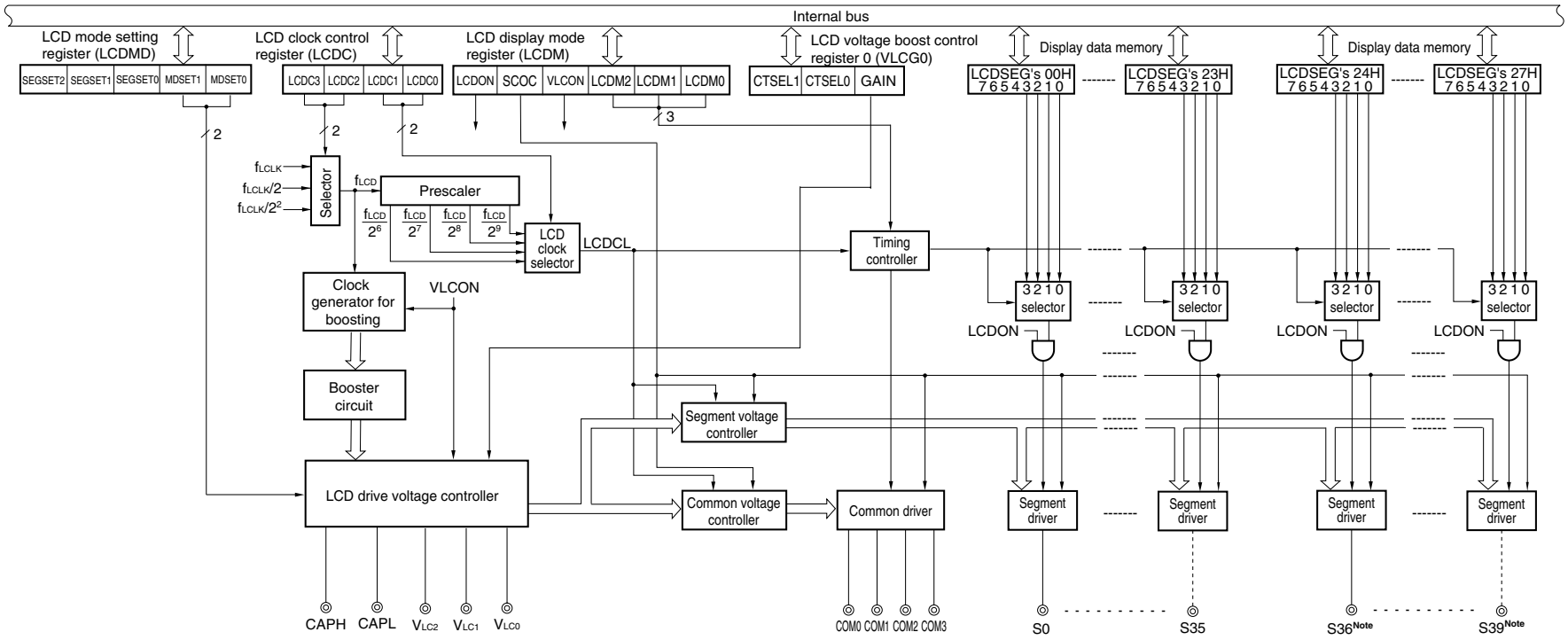


Figure 3-2. Block Diagram of LCD Controller/Driver



Note 64-pin product only.

3.3 Controlling LCD Controller/Driver

LCDCTL (control registers) and LCDSEG (display RAM) have the individual slave ID, and control registers and display RAM have unique addresses. The target control registers and display RAM are accessed by I^2C with these slave ID and addresses.

Table 3-3. Slave ID and Address of LCDCTL and LCDSEG

Block								Control registers/Display RAM	
	Slave ID (7 bits)								Address (8 bits)
LCDCTL (Control block)	0	1	1	1	0	0	0	LCD mode setting register (LCDMD)	00000000
								LCD display mode register (LCDM)	00000001
								LCD clock control register (LCDC)	00000010
								LCD voltage boost control register 0 (VLCG0)	00000011
LCDSEG (Display block)	0	1	1	1	0	0	1	S0 to S35	00000000 to 00100011
								S36 to S39[Note]	00100100 to 00100111

Note 64-pin product only.

Remark For details of communications by I^2C, see **CHAPTER 4 I^2C COMMUNICATIONS**.

Figure 3-3 shows the control register of LCD controller/driver and the memory map of display RAM, and Figure 3-4 shows the LCD display RAM.

Figure 3-3. Control Register of LCD Controller/Driver

Address	Register	Bit 7	6	5	4	3	2	1	0
LCDCTL's 03H	VLCG0	CTSEL1	CTSEL0	0	0	0	0	0	GAIN
02H	LCDC	0	0	0	0	LCDC3	LCDC2	LCDC1	LCDC0
01H	LCDM	LCDON	SCOC	VLCON	0	0	LCDM2	LCDM1	LCDM0
LCDCTL's 00H	LCDMD	SEGSET2	SEGSET1	SEGSET0	0	0	0	MDSET1	MDSET0

Figure 3-4. LCD Display RAM

Address	Bit 7	6	5	4	3	2	1	0	Segment
LCDSEG's 27H[Note]	0	0	0	0					→ S39[Note]
26H[Note]	0	0	0	0					→ S38[Note]
25H[Note]	0	0	0	0					→ S37[Note]
24H[Note]	0	0	0	0					→ S36[Note]
23H	0	0	0	0					→ S35
22H	0	0	0	0					→ S34
21H	0	0	0	0					→ S33
20H	0	0	0	0					→ S32
1FH	0	0	0	0					→ S31
1EH	0	0	0	0					→ S30
1DH	0	0	0	0					→ S29
1CH	0	0	0	0					→ S28
1BH	0	0	0	0					→ S27
1AH	0	0	0	0					→ S26
19H	0	0	0	0					→ S25
18H	0	0	0	0					→ S24
17H	0	0	0	0					→ S23
16H	0	0	0	0					→ S22
15H	0	0	0	0					→ S21
14H	0	0	0	0					→ S20
13H	0	0	0	0					→ S19
12H	0	0	0	0					→ S18
11H	0	0	0	0					→ S17
10H	0	0	0	0					→ S16
0FH	0	0	0	0					→ S15
0EH	0	0	0	0					→ S14
0DH	0	0	0	0					→ S13
0CH	0	0	0	0					→ S12
0BH	0	0	0	0					→ S11
0AH	0	0	0	0					→ S10
09H	0	0	0	0					→ S9
08H	0	0	0	0					→ S8
07H	0	0	0	0					→ S7
06H	0	0	0	0					→ S6
05H	0	0	0	0					→ S5
04H	0	0	0	0					→ S4
03H	0	0	0	0					→ S3
02H	0	0	0	0					→ S2
01H	0	0	0	0					→ S1
LCDSEG's 00H	0	0	0	0					→ S0
					↑	↑	↑	↑	
				Common	COM3	COM2	COM1	COM0	

Note 64-pin product only.

Remark Bits 4 to 7 are fixed to 0.

3.4 Registers Controlling LCD Controller/Driver

The following four registers are used to control the LCD controller/driver.

- LCD mode setting register (LCDMD)
- LCD display mode register (LCDM)
- LCD clock control register (LCDC)
- LCD voltage boost control register 0 (VLCG0)

(1) LCD mode setting register (LCDMD)

LCDMD sets the number of segments and the LCD reference voltage generator.

LCDMD is set using an 8-bit memory manipulation instruction.

Reset signal generation sets LCDMD to 00H.

Figure 3-5. Format of LCD Mode Setting Register

Address: LCDCTL's 00H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
LCDMD	SEGSET2	SEGSET1	SEGSET0	0	0	0	MDSET1	MDSET0

SEGSET2	SEGSET1	SEGSET0	Segment number setting
0	1	1	36 (52-pin product)
0	0	×	40 (64-pin product)
Other than above			Setting prohibited

MDSET1	MDSET0	LCD reference voltage generator selection
0	0	External resistance division method
0	1	Internal resistance division method
1	×	Internal voltage boosting method

Cautions 1. Bits 2 to 4 must be set to 0.

2. LCDMD can be set only once after a reset release.

(2) LCD display mode register (LCDM)

LCDM specifies whether to enable display operation. It also specifies whether to enable segment pin/common pin output, booster circuit operation, and the display mode.

LCDM is set using an 8-bit memory manipulation instruction.

Reset signal generation sets LCDM to 00H.

Figure 3-6. Format of LCD Display Mode Register

Address: LCDCTL's 01H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
LCDM	LCDON	SCOC	VLCON	0	0	LCDM2	LCDM1	LCDM0

LCDON	LCD display enable/disable
0	Display off (all segment outputs are deselected.)
1	Display on

SCOC	Segment pin/common pin output control[Note]
0	Output ground level to segment/common pin
1	Output deselect level to segment pin and LCD waveform to common pin

VLCON	Booster circuit operation enable/disable[Note]
0	No internal voltage boosting
1	Internal voltage boosting enabled

LCDM2	LCDM1	LCDM0	LCD controller/driver display mode selection			
			Resistance division method		Voltage boosting method	
			Number of time slices	Bias mode	Number of time slices	Bias mode
0	0	0	4	1/3	4	1/3
0	0	1	3	1/3	3	1/3
0	1	0	2	1/2	4	1/3
0	1	1	3	1/2	3	1/3
1	0	0	Static		Setting prohibited	
Other than above			Setting prohibited			

Note When the LCD display panel is not used, SCOC and VLCON must be set to 0 to conserve power.

Cautions 1. Bits 3 and 4 must be set to 0.

2. When operating VLCON, follow the procedure described below.

A. To stop voltage boosting after switching display status from on to off:

1) Set to display off status by setting LCDON = 0.

2) Disable outputs of all the segment buffers and common buffers by setting SCOC = 0.

3) Stop voltage boosting by setting VLCON = 0.

B. To stop voltage boosting during display on status:

Setting prohibited. Be sure to stop voltage boosting after setting display off.

C. To set display on from voltage boosting stop status:

1) Start voltage boosting by setting VLCON = 1, then wait for voltage boost wait time (t_{VAWAIT}) (see CHAPTER 5 ELECTRICAL SPECIFICATIONS).

2) Set all the segment buffers and common buffers to non-display output status by setting SCOC = 1.

3) Set display on by setting LCDON = 1.

(3) LCD clock control register (LCDC)

LCDC specifies the LCD source clock and LCD clock.

The frame frequency is determined according to the LCD clock and the number of time slices.

LCDC is set using an 8-bit memory manipulation instruction.

Reset signal generation sets LCDC to 00H.

Figure 3-7. Format of LCD Clock Control Register

Address: LCDCTL's 02H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
LCDC	0	0	0	0	LCDC3	LCDC2	LCDC1	LCDC0

LCDC3	LCDC2	LCD source clock (f_{LCD}) selection[Note]
0	×	f_{LCLK} (Clock input from the LCLK pin)
1	0	$f_{LCLK}/2$
1	1	$f_{LCLK}/2^2$

LCDC1	LCDC0	LCD clock (LCDCL) selection
0	0	$f_{LCD}/2^6$
0	1	$f_{LCD}/2^7$
1	0	$f_{LCD}/2^8$
1	1	$f_{LCD}/2^9$

Note Specify an LCD source clock (f_{LCD}) frequency of at least 32 kHz.

Cautions 1. Bits 4 to 7 must be set to 0.

2. Before changing the LCDC setting, be sure to stop voltage boosting (VLCON = 0).

3. Set the frame frequency to 128 Hz or lower.

(4) LCD voltage boost control register 0 (VLCG0)

VLCG0 controls the voltage boost level during the voltage boost operation.

VLCG0 is set with an 8-bit memory manipulation instruction.

Reset signal generation sets VLCG0 to 00H.

Figure 3-8. Format of LCD Voltage Boost Control Register 0

Address: LCDCTL's 03H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
VLCG0	CTSEL1	CTSEL0	0	0	0	0	0	GAIN

GAIN	Reference voltage (V_{LC2}) level selection[Note1]
0	1.5 V (specification of the LCD panel used is 4.5 V.)
1	1.0 V (specification of the LCD panel used is 3 V.)

CTSEL1	CTSEL0	Contrast adjustment (TYP.)					
		V_{LC0}		V_{LC1}		V_{LC2}	
		GAIN = 0	GAIN = 1	GAIN = 0	GAIN = 1	GAIN = 0	GAIN = 1
1	0	4.89 V[Note2]	3.39 V	3.27 V[Note2]	2.27 V	1.63 V[Note2]	1.13 V
1	1	4.71 V	3.21 V	3.13 V	2.13 V	1.57 V	1.07 V
0	0	4.50 V	3.00 V	3.00 V	2.00 V	1.50 V	1.00 V
0	1	4.29 V	2.79 V	2.87 V	1.87 V	1.43 V	0.93 V

Notes 1. Select the settings according to the specifications of the LCD panel that is used.

2. Operating voltage range: 2.0 V ≤ LV_{DD} < 5.5 V

Cautions 1. Bits 1 to 5 must be set to 0.

2. Before changing the VLCG0 setting, be sure to stop voltage boosting (VLCON = 0).

3. When using the resistance division method, voltage boosting must be stopped (VLCON = 0).

3.5 Setting LCD Controller/Driver

Set the LCD controller/driver using the following procedure.

Remark For details of communications by I^2C, see **CHAPTER 4 I^2C COMMUNICATIONS**.

(1) Voltage boosting method

• Operation flow for transition of reset status to display status in LCD controller/driver

<1> Release the reset status ($\overline{RESET}$ = High level).[Note]
<2> Supply the clock (Input the clock to LCLK).
<3> Set MDSET1 (bit 1 of LCDMD) to 1 to set the internal voltage boosting method
(initial setting: external resistance division method)
<4> Set the initial values to the LCD display data area (bits 0 to 3) in the LCD display RAM.
<5> Set the display mode using LCDM0, LCDM1, and LCDM2 (bits 0, 1, and 2 of LCD display mode register (LCDM)) (1/2 bias mode and static mode cannot be set).
<6> Set the LCD clock using LCD clock control register (LCDC).
<7> Set the voltage boost level and contrasts using LCD voltage boost control register 0 (VLCG0).
GAIN = 0: V_{LC0} = 4.5 V, V_{LC1} = 3 V, V_{LC2} = 1.5 V
GAIN = 1: V_{LC0} = 3 V, V_{LC1} = 2 V, V_{LC2} = 1 V
<8> Set VLCON (bit 5 of LCDM) to 1 to enable voltage boosting.
<9> Wait for voltage boost wait time (t_{VAWAIT}) from setting of VLCON (see **CHAPTER 5 ELECTRICAL SPECIFICATIONS**).
<10> Set SCOC (bit 6 of LCDM) to 1 to output the deselect voltage.
<11> Set LCDON (bit 7 of LCDM) to 1 and set data to the data memory in accordance with the display contents, after the output corresponding to each data memory is started.

Subsequent to this procedure, set the data to be displayed in the data memory.

Note During reset, the internal pull-down resistor is connected to the LCLK pin.
Input the low level to LCLK pin in advance before a reset release, because the internal pull-down resistor is automatically disconnected when a reset is released.

Remark The register can be set in 1-bit units because the I^2C bus is used for setting.

(2) Resistance division method

• Operation flow for transition of reset status to display status in LCD controller/driver

<1> Release the reset status ($\overline{\text{RESET}}$ = High level).[Note]

<2> Supply the clock (Input the clock to LCLK).

<3> Set to the internal voltage boosting method using MDSET0 and MDSET1 (bit 0 and 1 of LCDMD).
(MDSET0, MDSET1 = 0, 0: External resistance division method,
MDSET0, MDSET1 = 0, 1: Internal resistance division method)

<4> Set the initial values to the LCD display data area (bits 0 to 3) in the LCD display RAM.

<5> Set the display mode using LCDM0, LCDM1, and LCDM2 (bits 0, 1, and 2 of LCD display mode register (LCDM)).

<6> Set the LCD clock using LCD clock control register (LCDC).

<7> Set SCOC (bit 6 of LCDM) to 1 to output the deselect voltage.

<8> Set LCDON (bit 7 of LCDM) to 1 and set data to the data memory in accordance with the display contents, after the output corresponding to each data memory is started.

Subsequent to this procedure, set the data to be displayed in the data memory.

Note During reset, the internal pull-down resistor is connected to the LCLK pin.
Input the low level to LCLK pin in advance before a reset release, because the internal pull-down resistor is automatically disconnected when a reset is released.

Caution When using the resistance division method, voltage boosting must be stopped (VLCON = 0).

Remark The register can be set in 1-bit units because the I^2C bus is used for setting.

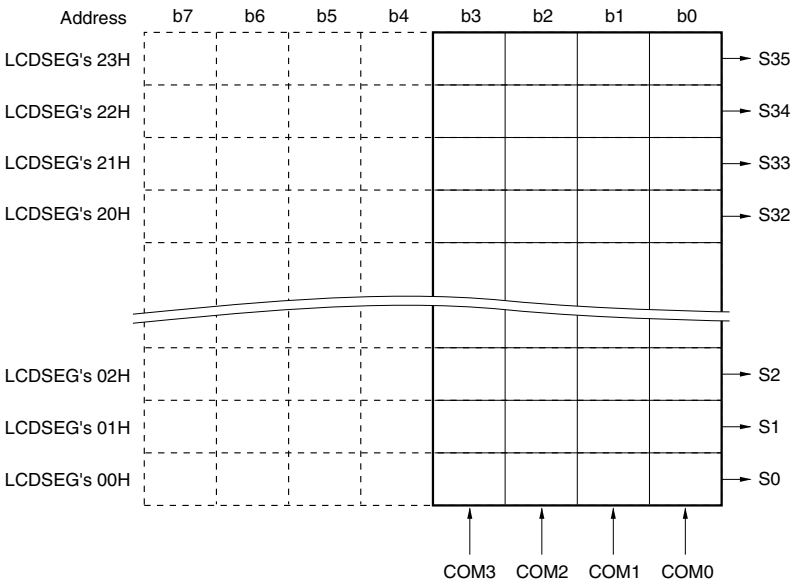
3.6 LCD Display Data Memory

The LCD display data memory is mapped at addresses 00H to 23H of LCDSEG for 52-pin product and addresses 00H to 27H of LCDSEG for 64-pin product. Data in the LCD display data memory can be displayed on the LCD panel using the LCD controller/driver.

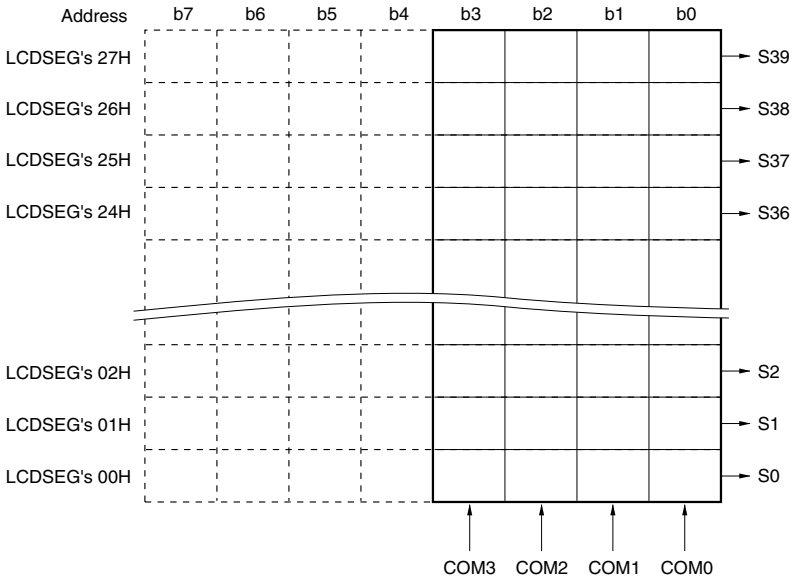
Figure 3-9 shows the relationship between the contents of the LCD display data memory and the segment/common outputs.

Figure 3-9. Relationship Between LCD Display Data Memory Contents and Segment/Common Outputs

(a) 52-pin product



(b) 64-pin product



Caution No memory is allocated to the higher 4 bits of the LCD display data memory. Be sure to set there bits to 0.

3.7 Common and Segment Signals

Each pixel of the LCD panel turns on when the potential difference between the corresponding common and segment signals becomes higher than a specific voltage (LCD drive voltage, V_{LCD}). The pixels turn off when the potential difference becomes lower than V_{LCD}.

Applying DC voltage to the common and segment signals of an LCD panel causes deterioration. To avoid this problem, this LCD panel is driven by AC voltage.

(1) Common signals

Each common signal is selected sequentially according to a specified number of time slices at the timing listed in Table 3-4. In the static display mode, the same signal is output to COM0 to COM3.

In the two-time-slice mode, leave the COM2 and COM3 pins open. In the three-time-slice mode, leave the COM3 pin open.

Table 3-4. COM Signals

COM Signal / Number of Time Slices	COM0	COM1	COM2	COM3
Static display mode				
Two-time-slice mode			Open	Open
Three-time-slice mode				Open
Four-time-slice mode				

(2) Segment signals

(a) 52-pin product

The segment signals correspond to 36 bytes of LCD display data memory (00H to 23H of LCDSEG). Bits 0, 1, 2, and 3 of each byte are read in synchronization with COM0, COM1, COM2, and COM3, respectively. If a bit is 1, it is converted to the select voltage, and if it is 0, it is converted to the deselect voltage. The conversion results are output to the segment pins (S0 to S35).

(b) 64-pin product

The segment signals correspond to 40 bytes of LCD display data memory (00H to 27H of LCDSEG). Bits 0, 1, 2, and 3 of each byte are read in synchronization with COM0, COM1, COM2, and COM3, respectively. If a bit is 1, it is converted to the select voltage, and if it is 0, it is converted to the deselect voltage. The conversion results are output to the segment pins (S0 to S39).

Check, with the information given above, what combination of front-surface electrodes (corresponding to the segment signals) and rear-surface electrodes (corresponding to the common signals) forms display patterns in the LCD display data memory, and write the bit data that corresponds to the desired display pattern on a one-to-one basis.

LCD display data memory bits 1 to 3, bits 2 and 3, and bit 3 are not used for LCD display in the static display, two-time slot, and three-time slot modes, respectively. So these bits can be used for purposes other than display.

LCD display data memory bits 4 to 7 are fixed to 0.

(3) Output waveforms of common and segment signals

The voltages listed in Table 3-5 are output as common and segment signals.

When both common and segment signals are at the select voltage, a display on-voltage of $\pm V_{LCD}$ is obtained.

The other combinations of the signals correspond to the display off-voltage.

Table 3-5. LCD Drive Voltage

(a) Static display mode

Segment Signal / Common Signal	Select Signal Level	Deselect Signal Level
	LV_{SS}/V_{LC0}	V_{LC0}/LV_{SS}
V_{LC0}/LV_{SS}	$-V_{LCD}/+V_{LCD}$	0 V/0 V

(b) 1/2 bias method

Segment Signal / Common Signal		Select Signal Level	Deselect Signal Level
		LV_{SS}/V_{LC0}	V_{LC0}/LV_{SS}
Select signal level	V_{LC0}/LV_{SS}	$-V_{LCD}/+V_{LCD}$	0 V/0 V
Deselect signal level	$V_{LC1} = V_{LC2}$	$-\frac{1}{2}V_{LCD}/+\frac{1}{2}V_{LCD}$	$+\frac{1}{2}V_{LCD}/-\frac{1}{2}V_{LCD}$

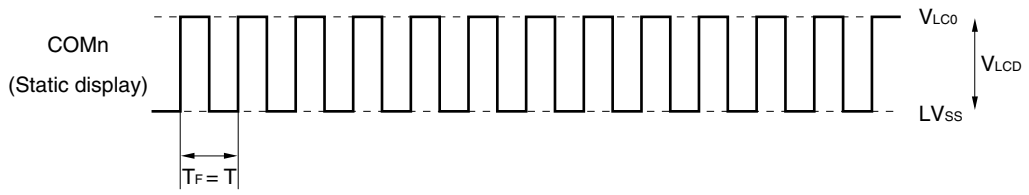
(c) 1/3 bias method

Segment Signal / Common Signal		Select Signal Level	Deselect Signal Level
		LV_{SS}/V_{LC0}	V_{LC1}/V_{LC2}
Select signal level	V_{LC0}/LV_{SS}	$-V_{LCD}/+V_{LCD}$	$-\frac{1}{3}V_{LCD}/+\frac{1}{3}V_{LCD}$
Deselect signal level	V_{LC2}/V_{LC1}	$-\frac{1}{3}V_{LCD}/+\frac{1}{3}V_{LCD}$	$-\frac{1}{3}V_{LCD}/+\frac{1}{3}V_{LCD}$

Figure 3-10 shows the common signal waveforms, and Figure 3-11 shows the voltages and phases of the common and segment signals.

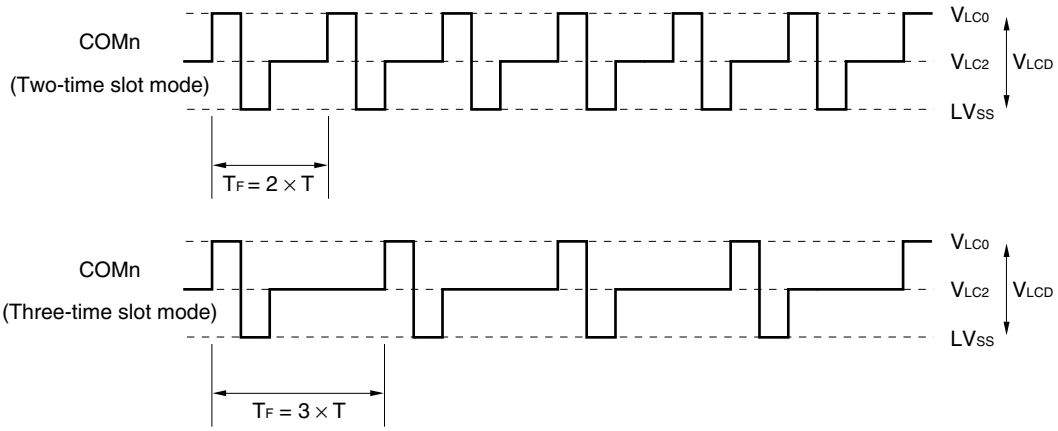
Figure 3-10. Common Signal Waveforms

(a) Static display mode



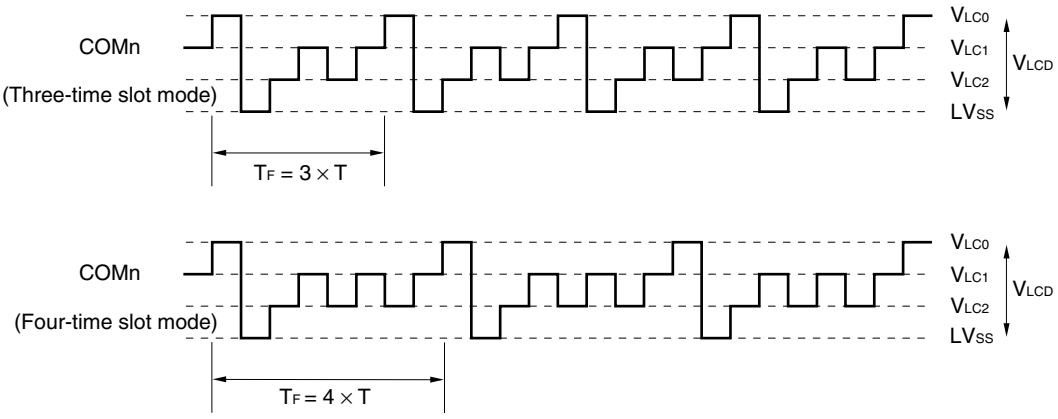
T: One LCD clock period T_F: Frame frequency

(b) 1/2 bias method



T: One LCD clock period T_F: Frame frequency

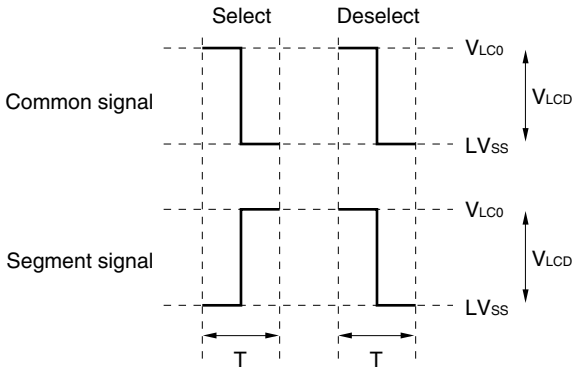
(c) 1/3 bias method



T: One LCD clock period T_F: Frame frequency

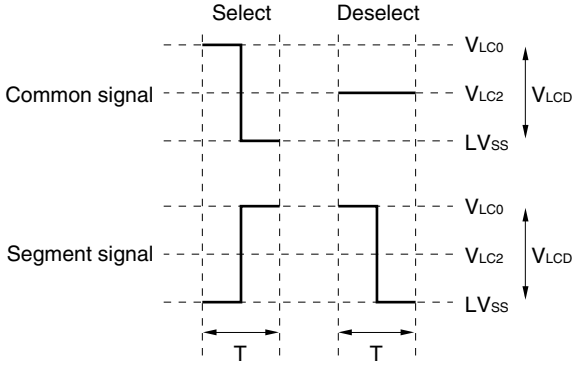
Figure 3-11. Voltages and Phases of Common and Segment Signals

(a) Static display mode



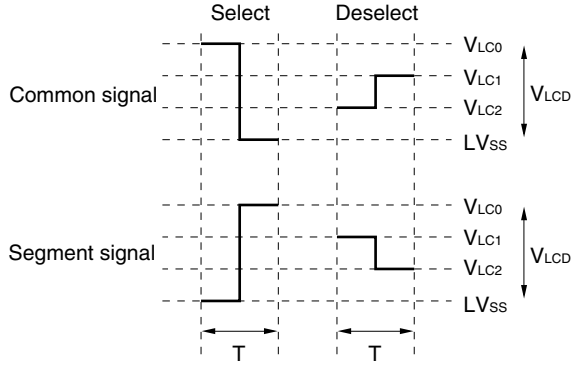
T: One LCD clock period

(b) 1/2 bias method



T: One LCD clock period

(c) 1/3 bias method



T: One LCD clock period

3.8 Display Modes

3.8.1 Static display example

Figure 3-13 shows how the three-digit LCD panel having the display pattern shown in Figure 3-12 is connected to the segment signals (S0 to S23) and the common signal (COM0). This example displays data "12.3" in the LCD panel. The contents of the display data memory (addresses 00H to 17H of LCDSEG) correspond to this display.

The following description focuses on numeral "2." (2.) displayed in the second digit. To display "2." in the LCD panel, it is necessary to apply the select or deselect voltage to the S8 to S15 pins according to Table 3-6 at the timing of the common signal COM0; see Figure 3-12 for the relationship between the segment signals and LCD segments.

Table 3-6. Select and Deselect Voltages (COM0)

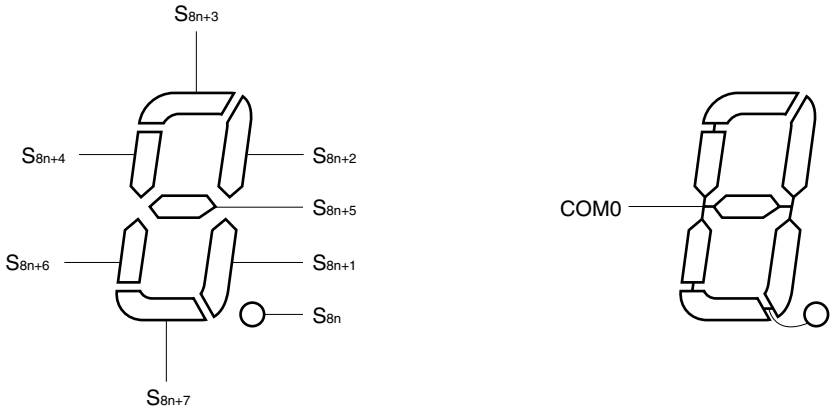
Segment / Common	S8	S9	S10	S11	S12	S13	S14	S15
COM0	Select	Deselect	Select	Select	Deselect	Select	Select	Select

According to Table 3-6, it is determined that the bit-0 pattern of the display data memory locations (08H to 0FH of LCDSEG) must be 10110111.

Figure 3-14 shows the LCD drive waveforms of S11 and S12, and COM0. When the select voltage is applied to S11 at the timing of COM0, an alternate rectangle waveform, $+V_{LCD}/-V_{LCD}$, is generated to turn on the corresponding LCD segment.

COM1 to COM3 are supplied with the same waveform as for COM0. So, COM0 to COM3 may be connected together to increase the driving capacity.

Figure 3-12. Static LCD Display Pattern and Electrode Connections



Remark n = 0 to 2

Figure 3-13. Example of Connecting Static LCD Panel

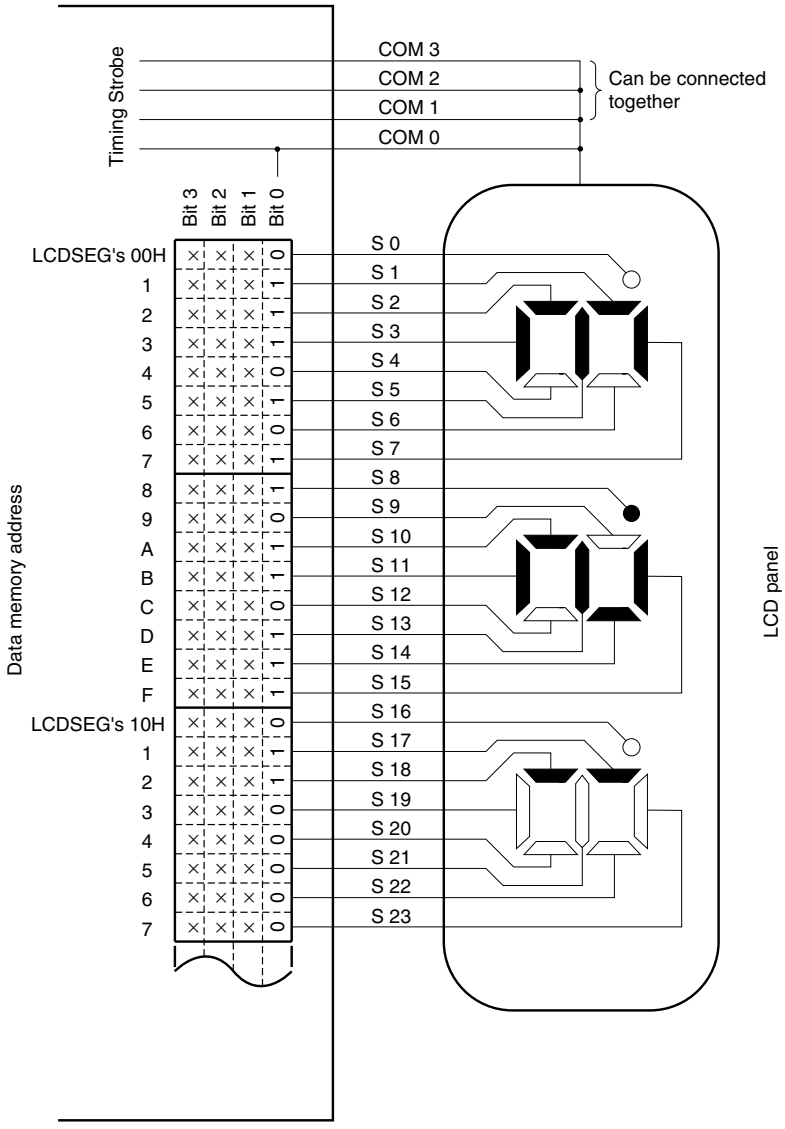
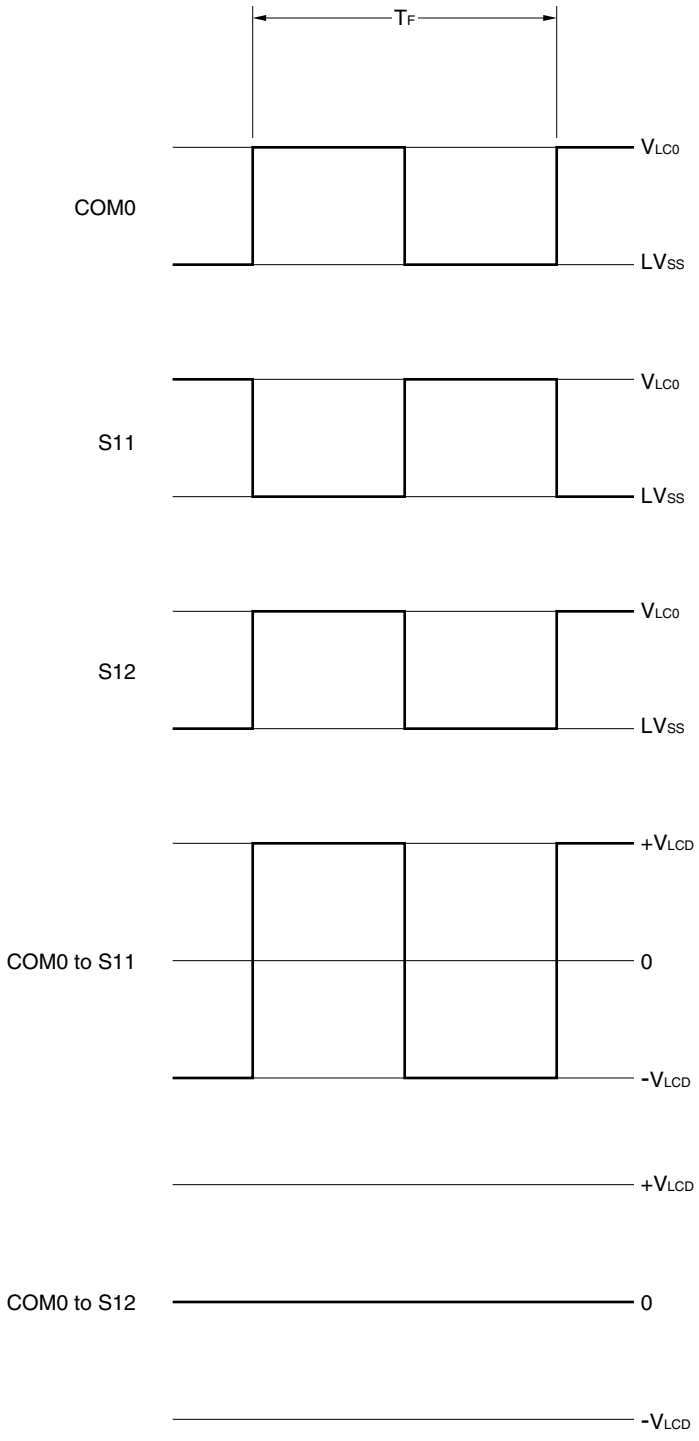


Figure 3-14. Static LCD Drive Waveform Examples



3.8.2 Two-time-slice display example

Figure 3-16 shows how the 6-digit LCD panel having the display pattern shown in Figure 3-15 is connected to the segment signals (S0 to S23) and the common signals (COM0 and COM1). This example displays data "12345.6" in the LCD panel. The contents of the display data memory (addresses 00H to 17H of LCDSEG) correspond to this display.

The following description focuses on numeral "3" (3) displayed in the fourth digit. To display "3" in the LCD panel, it is necessary to apply the select or deselect voltage to the S12 to S15 pins according to Table 3-7 at the timing of the common signals COM0 and COM1; see Figure 3-15 for the relationship between the segment signals and LCD segments.

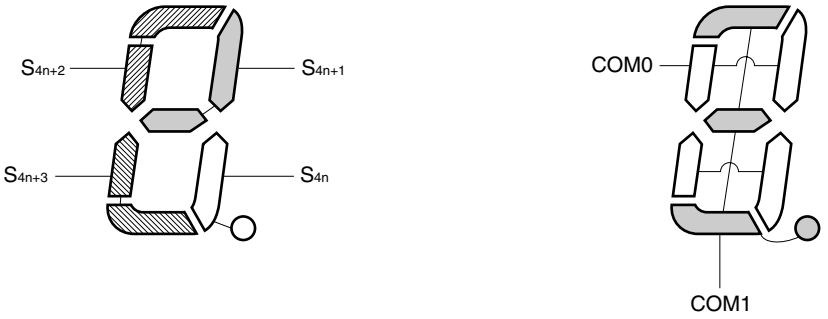
Table 3-7. Select and Deselect Voltages (COM0 and COM1)

Segment / Common	S12	S13	S14	S15
COM0	Select	Select	Deselect	Deselect
COM1	Deselect	Select	Select	Select

According to Table 3-7, it is determined that the display data memory location (0FH of LCDSEG) that corresponds to S15 must contain xx10.

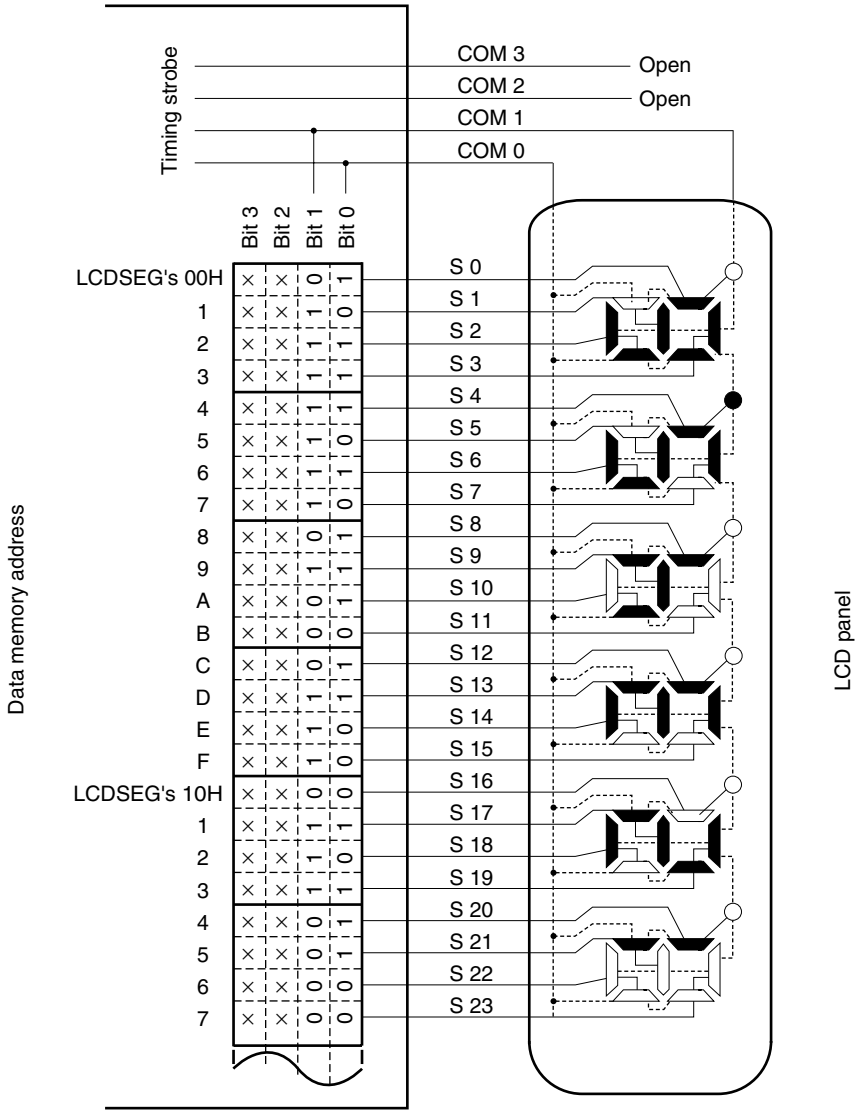
Figure 3-17 shows examples of LCD drive waveforms between the S15 signal and each common signal. When the select voltage is applied to S15 at the timing of COM1, an alternate rectangle waveform, $+V_{LCD}/-V_{LCD}$, is generated to turn on the corresponding LCD segment.

Figure 3-15. Two-Time-Slice LCD Display Pattern and Electrode Connections



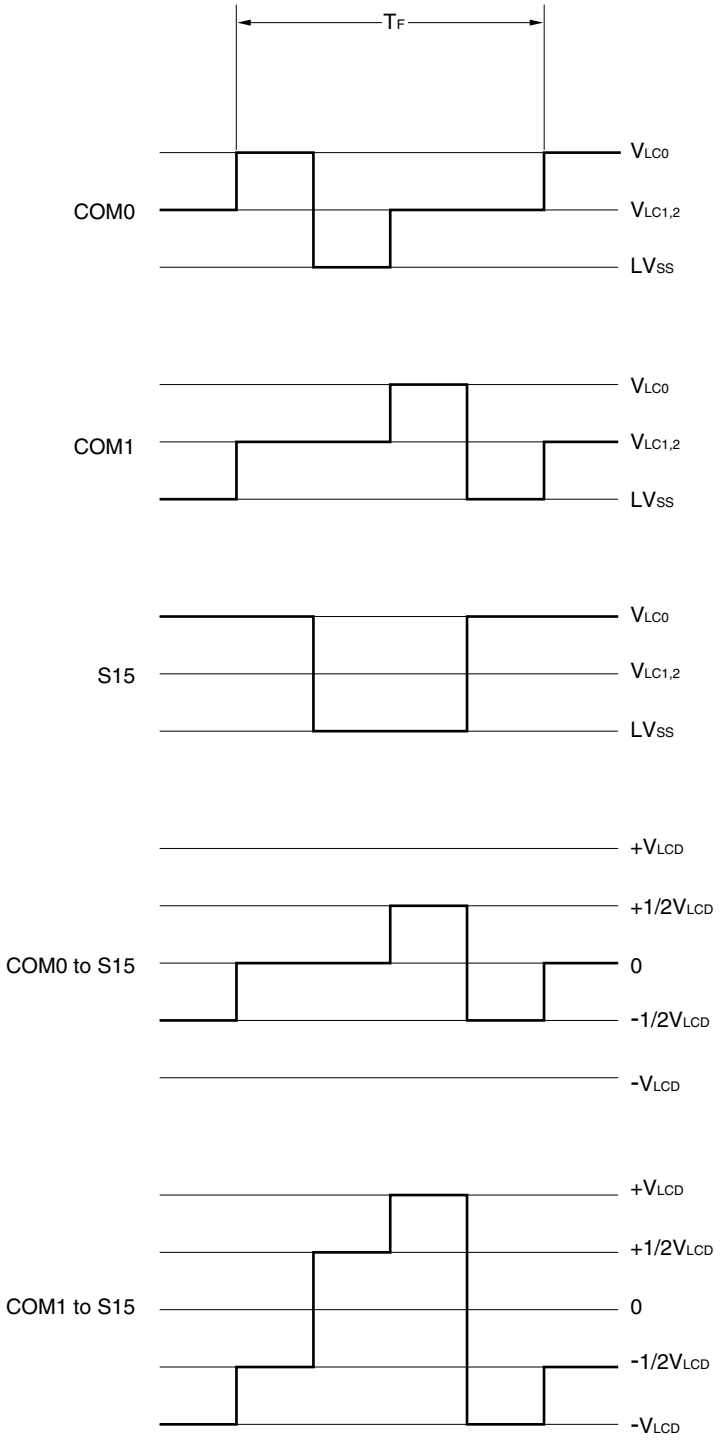
Remark n = 0 to 5

Figure 3-16. Example of Connecting Two-Time-Slice LCD Panel



×: Can always be used to store any data because the two-time-slice mode is being used.

Figure 3-17. Two-Time-Slice LCD Drive Waveform Examples (1/2 Bias Method)



3.8.3 Three-time-slice display example

Figure 3-19 shows how the 8-digit LCD panel having the display pattern shown in Figure 3-18 is connected to the segment signals (S0 to S23) and the common signals (COM0 to COM2). This example displays data "123456.78" in the LCD panel. The contents of the display data memory (addresses 00H to 17H of LCDSEG) correspond to this display.

The following description focuses on numeral "6." (6.) displayed in the third digit. To display "6." in the LCD panel, it is necessary to apply the select or deselect voltage to the S6 to S8 pins according to Table 3-8 at the timing of the common signals COM0 to COM2; see Figure 3-18 for the relationship between the segment signals and LCD segments.

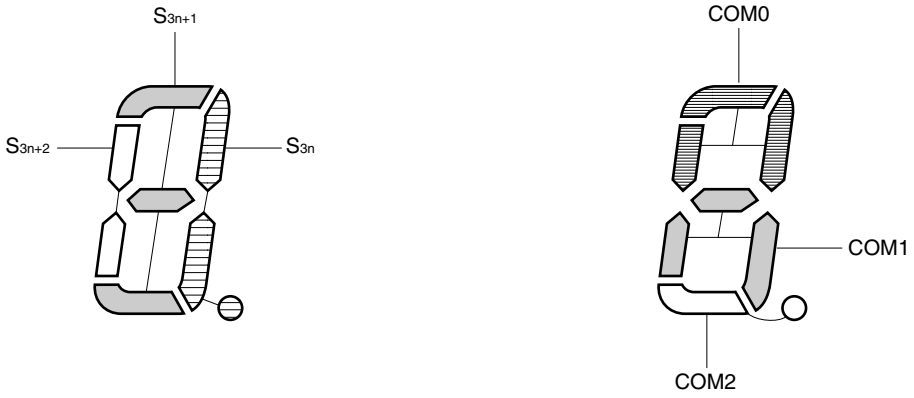
Table 3-8. Select and Deselect Voltages (COM0 to COM2)

Segment / Common	S6	S7	S8
COM0	Deselect	Select	Select
COM1	Select	Select	Select
COM2	Select	Select	–

According to Table 3-8, it is determined that the display data memory location (06H of LCDSEG) that corresponds to S6 must contain x110.

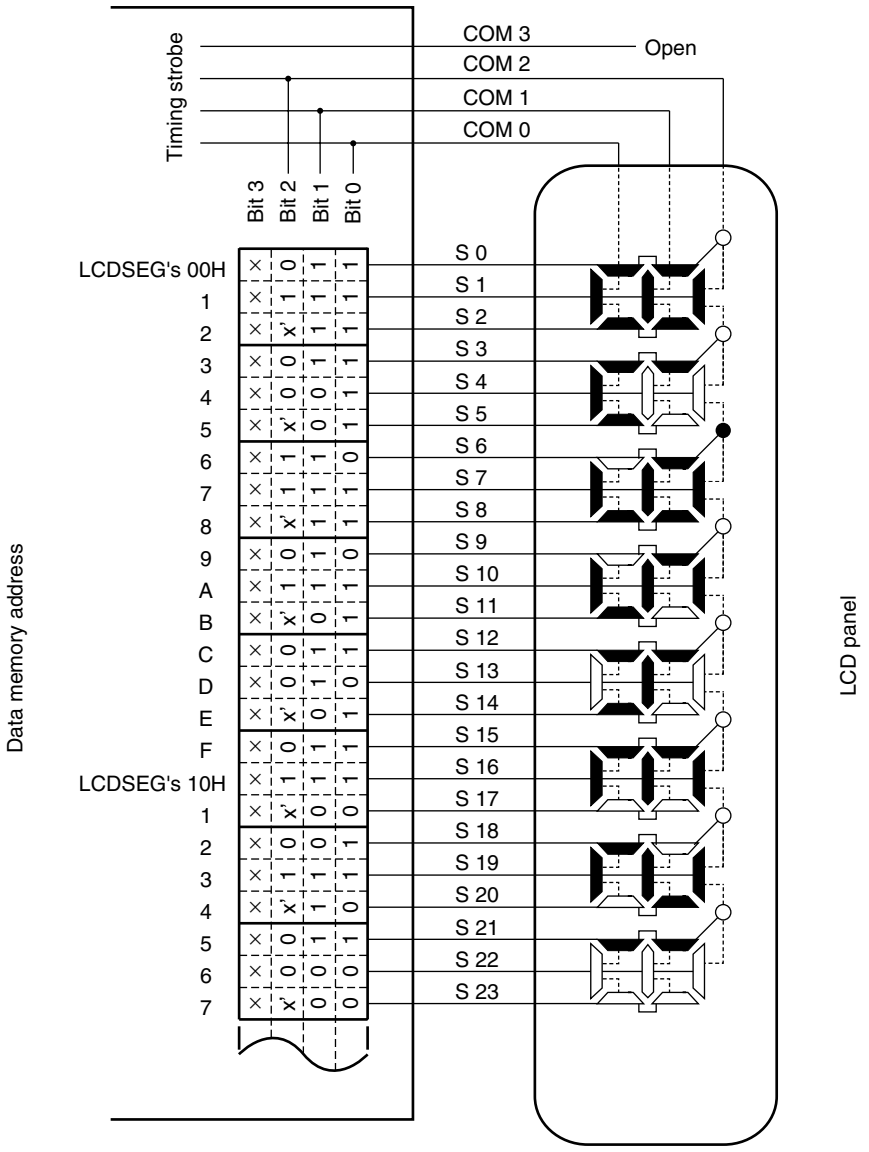
Figures 3-20 and 3-21 show examples of LCD drive waveforms between the S6 signal and each common signal in the 1/2 and 1/3 bias methods, respectively. When the select voltage is applied to S6 at the timing of COM1 or COM2, an alternate rectangle waveform, $+V_{LCD}/-V_{LCD}$, is generated to turn on the corresponding LCD segment.

Figure 3-18. Three-Time-Slice LCD Display Pattern and Electrode Connections



Remark n = 0 to 7

Figure 3-19. Example of Connecting Three-Time-Slice LCD Panel



×': Can be used to store any data because there is no corresponding segment in the LCD panel.

×: Can always be used to store any data because the three-time-slice mode is being used.

Figure 3-20. Three-Time-Slice LCD Drive Waveform Examples (1/2 Bias Method)

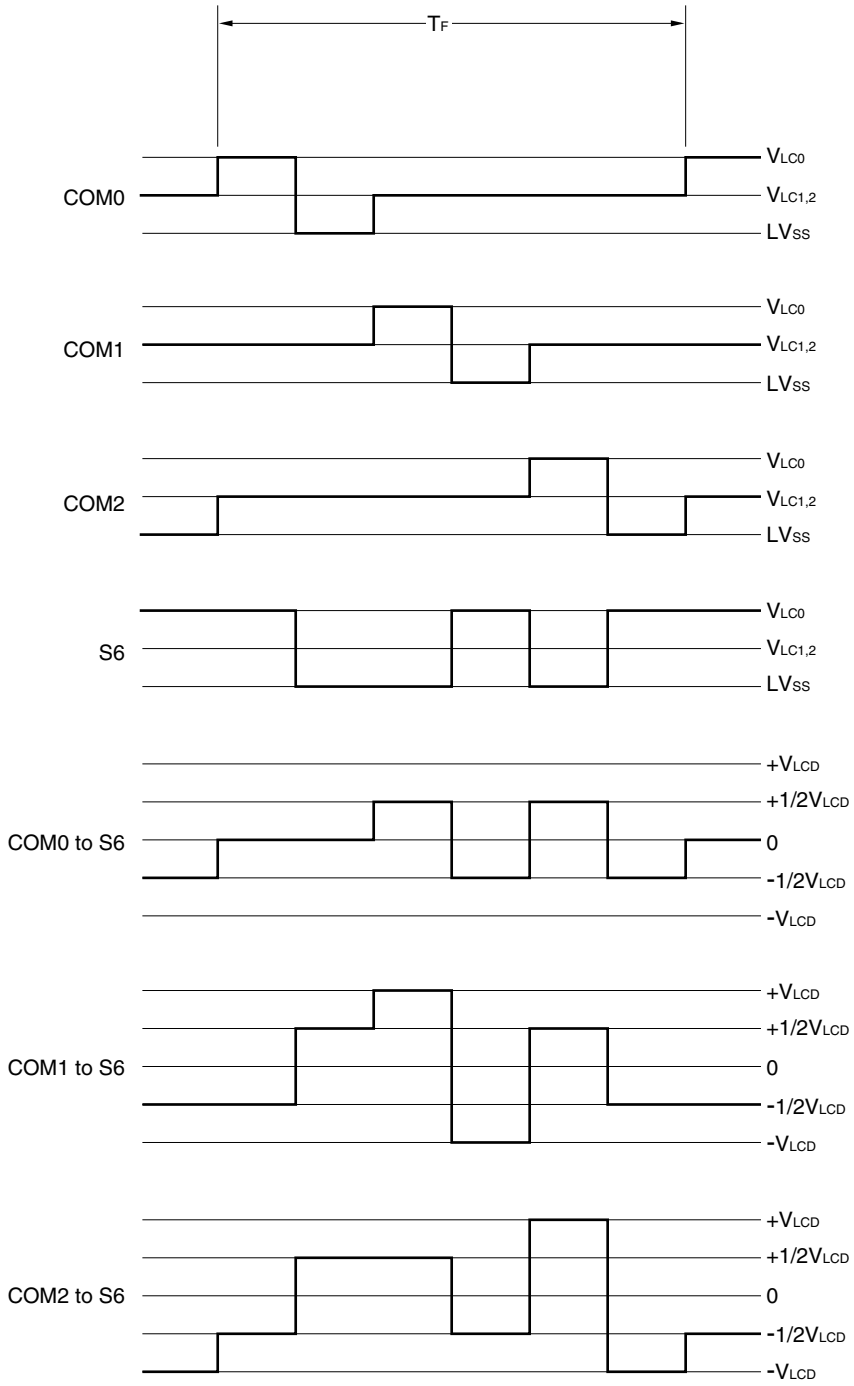
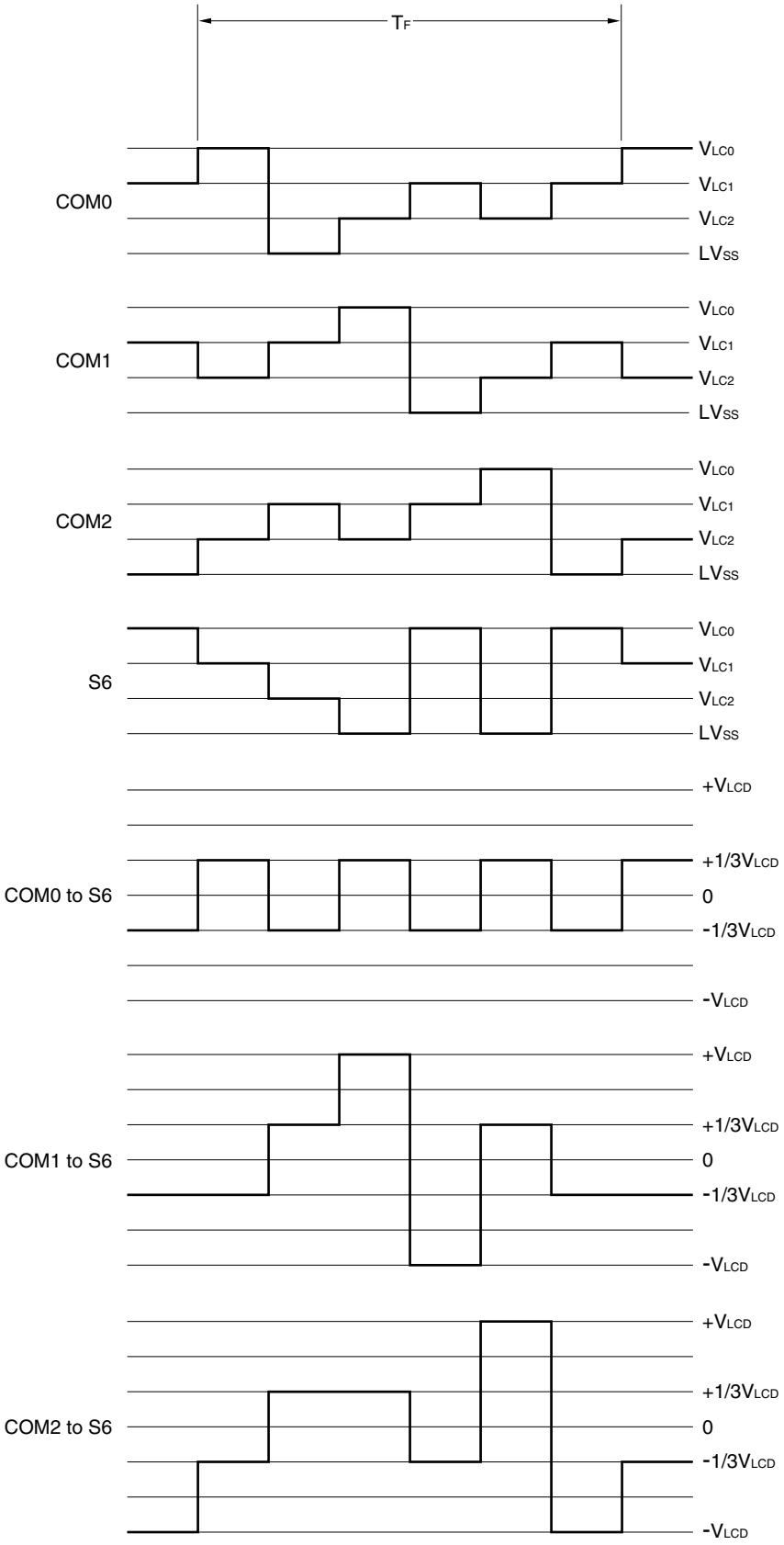


Figure 3-21. Three-Time-Slice LCD Drive Waveform Examples (1/3 Bias Method)



3.8.4 Four-time-slice display example

Figure 3-23 shows how the 12-digit LCD panel having the display pattern shown in Figure 3-22 is connected to the segment signals (S0 to S23) and the common signals (COM0 to COM3). This example displays data "123456.789012" in the LCD panel. The contents of the display data memory (addresses 00H to 17H of LCDSEG) correspond to this display.

The following description focuses on numeral "6." (6.) displayed in the seventh digit. To display "6." in the LCD panel, it is necessary to apply the select or deselect voltage to the S12 and S13 pins according to Table 3-9 at the timing of the common signals COM0 to COM3; see Figure 3-22 for the relationship between the segment signals and LCD segments.

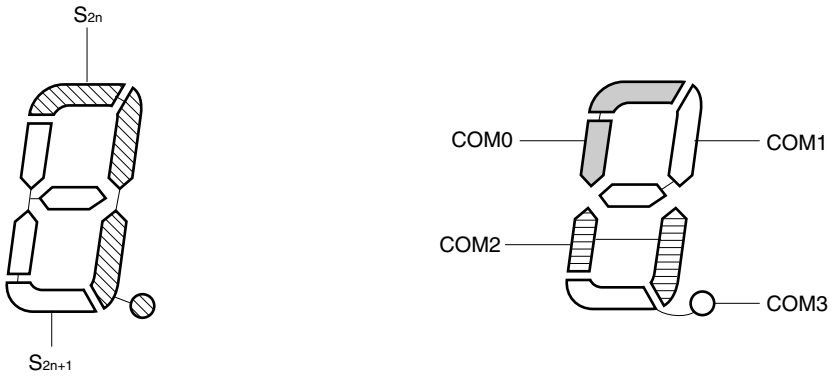
Table 3-9. Select and Deselect Voltages (COM0 to COM3)

Segment / Common	S12	S13
COM0	Select	Select
COM1	Deselect	Select
COM2	Select	Select
COM3	Select	Select

According to Table 3-9, it is determined that the display data memory location (0CH of LCDSEG) that corresponds to S12 must contain 1101.

Figure 3-24 shows examples of LCD drive waveforms between the S12 signal and each common signal. When the select voltage is applied to S12 at the timing of COM0, an alternate rectangle waveform, $+V_{LCD}/-V_{LCD}$, is generated to turn on the corresponding LCD segment.

Figure 3-22. Four-Time-Slice LCD Display Pattern and Electrode Connections



Remark n = 0 to 11

Figure 3-23. Example of Connecting Four-Time-Slice LCD Panel

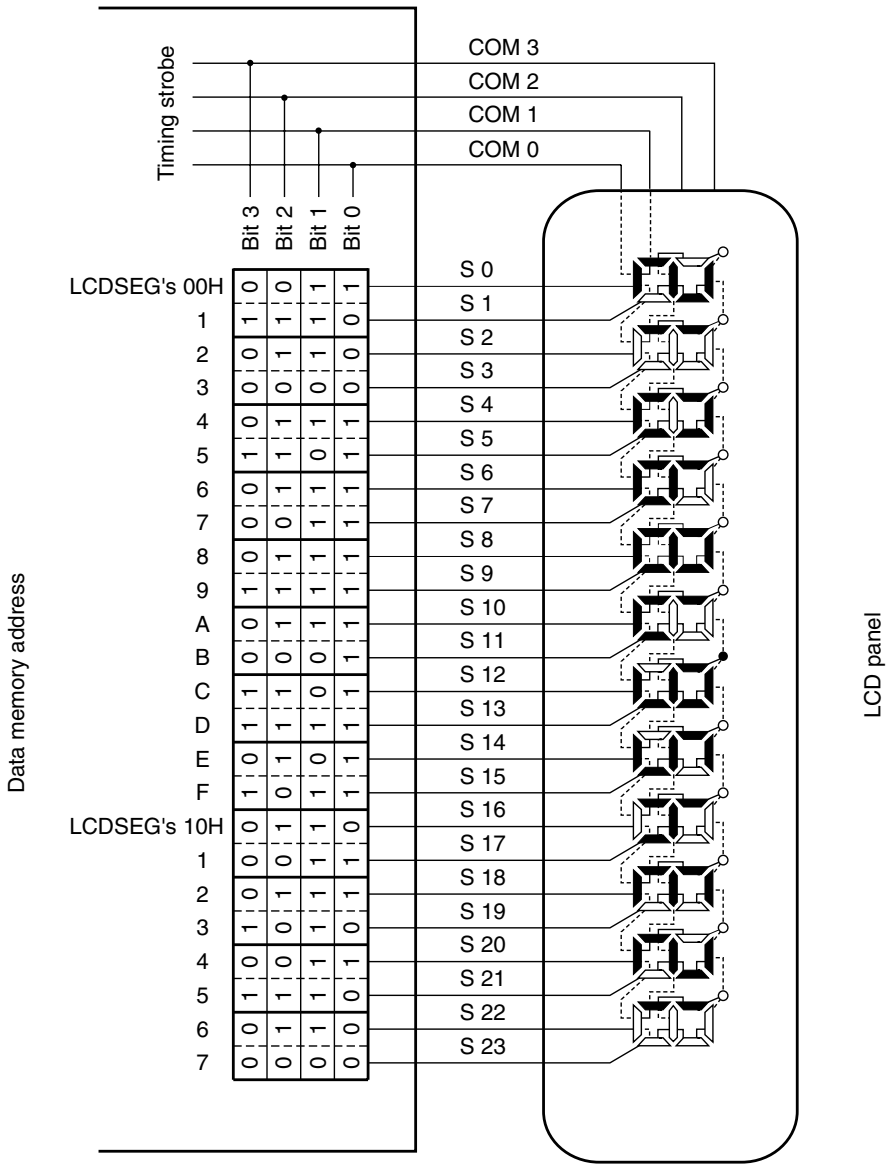
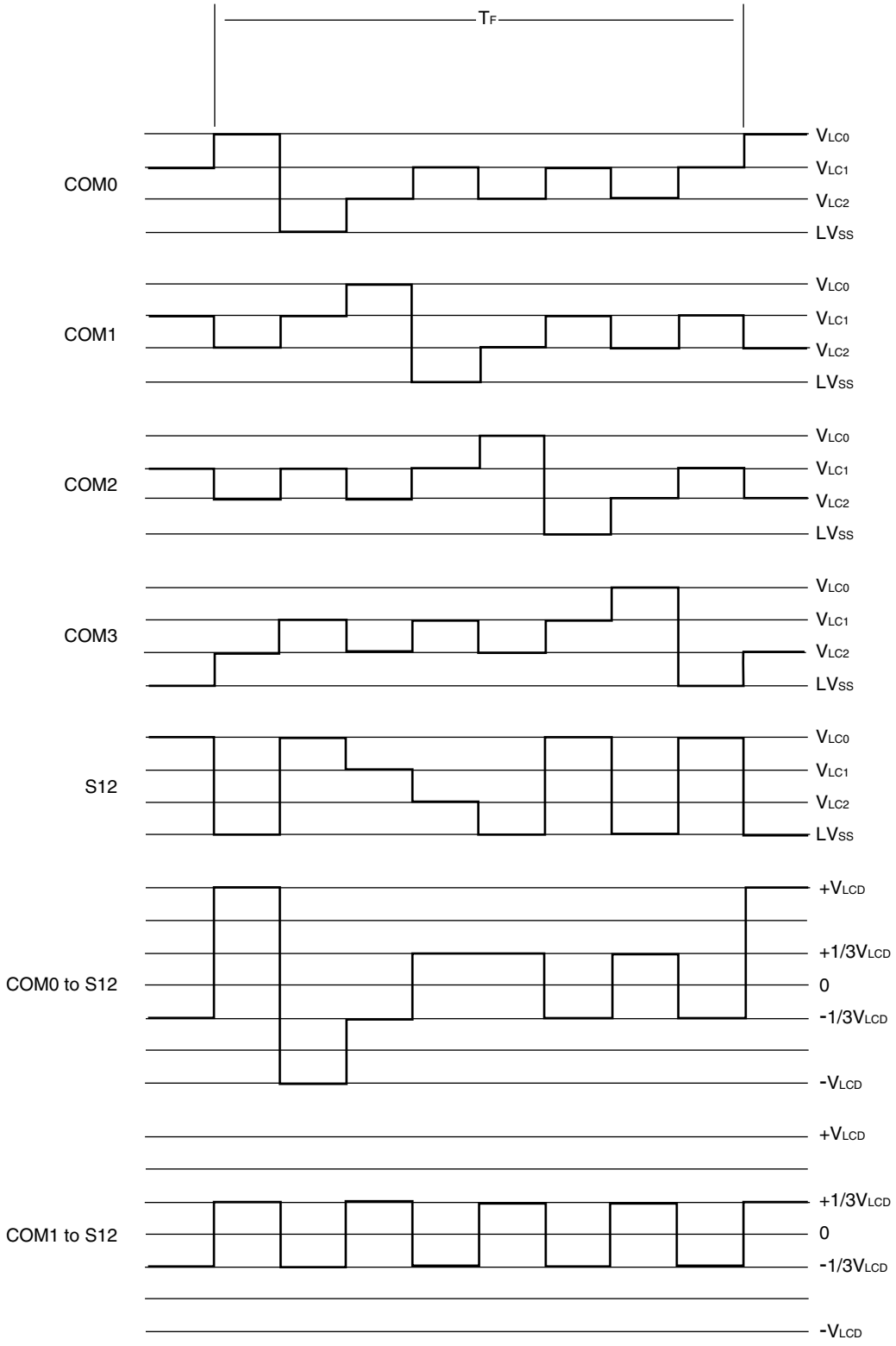


Figure 3-24. Four-Time-Slice LCD Drive Waveform Examples (1/3 Bias Method)



Remark The waveforms for COM2 to S12 and COM3 to S12 are omitted.

3.9 Supplying LCD Drive Voltages V_{LC0}, V_{LC1}, and V_{LC2}

A LCD drive power supply can be generated using either of three types of methods: internal resistance division method, external resistance division method, or internal voltage boosting method.

3.9.1 Internal resistance division method

Voltage divider resistors for generating LCD drive power supplies are incorporated. Using internal voltage divider resistors, a LCD drive power supply that meet each bias method listed in Table 3-10 can be generated, without using external voltage divider resistors.

Table 3-10. LCD Drive Voltages (with On-Chip Voltage Divider Resistors)

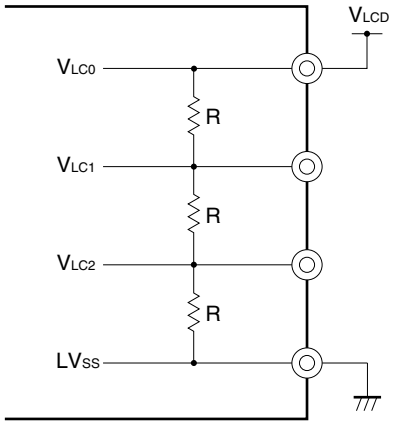
Bias Method / LCD Drive Voltage Pin	No Bias (Static)	1/2 Bias Method	1/3 Bias Method
V_{LC0}	V_{LCD}	V_{LCD}	V_{LCD}
V_{LC1}	$\frac{2}{3}$ V_{LCD}	$\frac{1}{2}$ V_{LCD} Note	$\frac{2}{3}$ V_{LCD}
V_{LC2}	$\frac{1}{3}$ V_{LCD}		$\frac{1}{3}$ V_{LCD}

Note For the 1/2 bias method, it is necessary to connect the V_{LC1} and V_{LC2} pins externally.

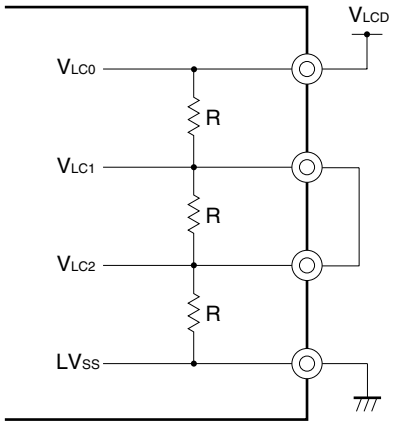
Figure 3-25 shows examples of generating LCD drive voltages internally according to Table 3-10.

Figure 3-25. Examples of LCD Drive Power Connections (Internal Resistance Division Method)

(a) 1/3 bias method and static display mode



(b) 1/2 bias method



Remark It is recommended to use the external resistance division method when using the static display mode, in order to reduce power consumed by the voltage divider resistor.

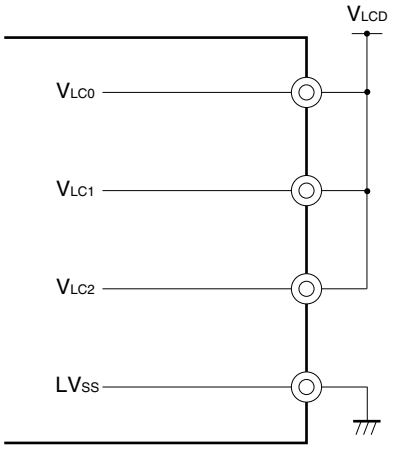
3.9.2 External resistance division method

It is also possible to use external voltage divider resistors for generating LCD drive power supplies, without using internal resistors. Figure 3-26 shows examples of LCD drive voltage connection, corresponding to each bias method.

Figure 3-26. Examples of LCD Drive Power Connections (External Resistance Division Method)

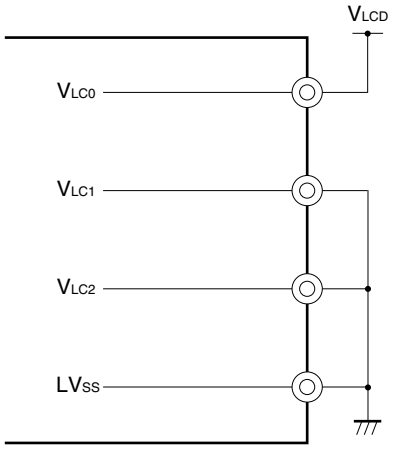
(a) Static display mode

($V_{LCD} = V_{LC0} = V_{LC1} = V_{LC2}$)

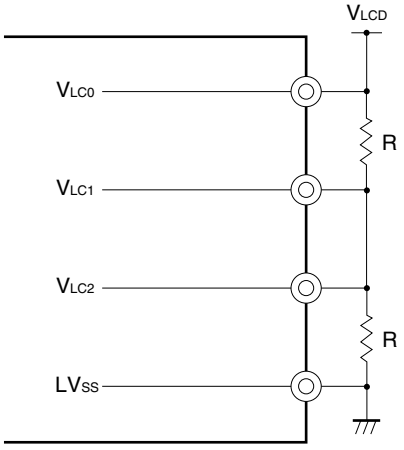


(b) Static display mode

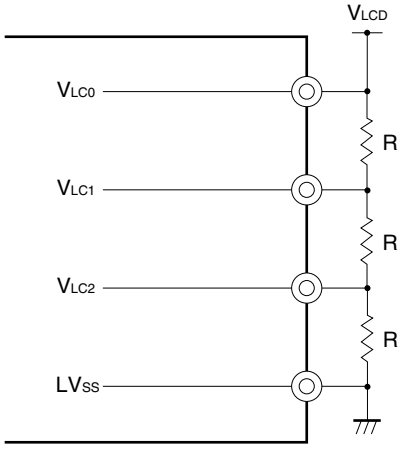
($V_{LC1} = V_{LC2} = LV_{SS}$ = GND)



(c) 1/2 bias method



(d) 1/3 bias method



Remark Both (a) and (b) connection can be used in the static display mode.

3.9.3 Internal voltage boosting method

A booster circuit (×3 only) to generate a supply voltage to drive the LCD is contained. The internal LCD reference voltage is output from the V_{LC2} pin. A voltage two times higher than that on V_{LC2} is output from the V_{LC1} pin and a voltage three times higher than that on V_{LC2} is output from the V_{LC0} pin.

The LCD reference voltage (V_{LC2}) can be specified by setting LCD boost control register 0 (VLCG0).

An external capacitor (0.47 to 1 μF: recommended) is required when the internal voltage boosting method is selected.

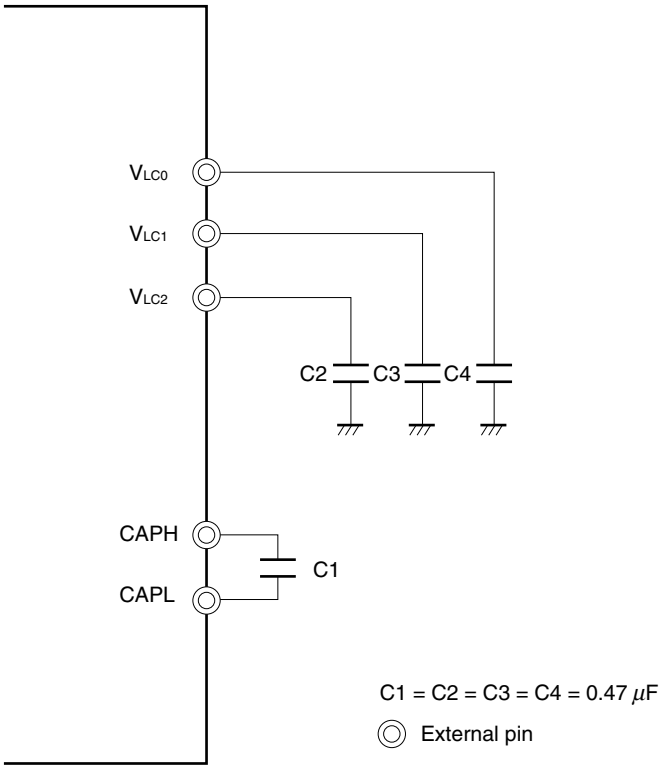
Table 3-11. Output Voltages of V_{LC0} to V_{LC2} Pins

LCD drive power supply pin \ VLCG0	GAIN = 0	GAIN = 1
V_{LC0}	4.5 V	3.0 V
V_{LC1}	3.0 V	2.0 V
V_{LC2} (LCD reference voltage)	1.5 V	1.0 V

Cautions

1. **When using the LCD function, do not leave the V_{LC0}, V_{LC1}, and V_{LC2} pins open. Refer to Figure 3-27 for connection.**
2. **Since the LCD drive voltage is separate from the main power supply, a constant voltage can be supplied regardless of LV_{DD} fluctuation.**

Figure 3-27. Example of Connecting Pins for LCD Driver



Remark Use a capacitor with as little leakage as possible.
In addition, make C1 a nonpolar capacitor.

CHAPTER 4 I²C COMMUNICATIONS

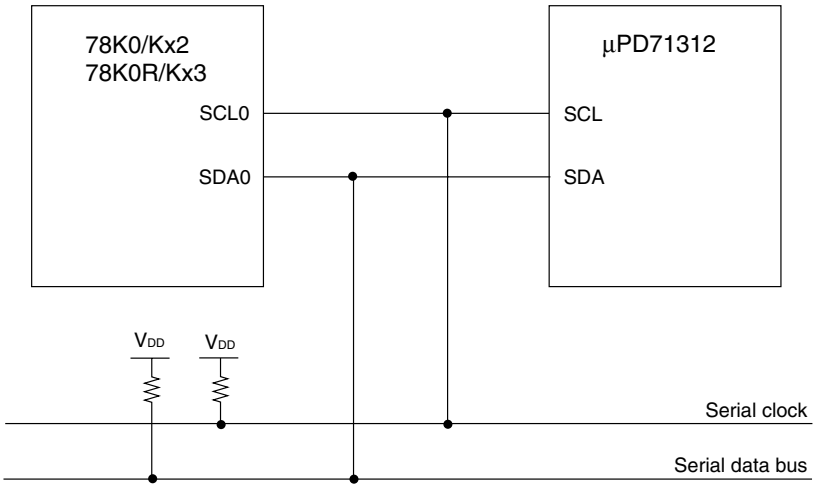
Setting of LCD controller/driver in the μPD71312 is performed by communication of the I²C bus interface. The outline of communication is as follows.

- Communication pins: SCL, SDA
- Communication function: Slave transmission/reception

4.1 System Configuration

The system configuration of the LCD controller/driver is illustrated in Figure 4-1.

Figure 4-1. System Configuration



Caution Only communication with IIC0 of the 78K0/Kx2 and 78K0R/Kx3 is possible. It does not support the simplified IIC of the 78K0R/Kx3.

4.2 Explanation of Operation

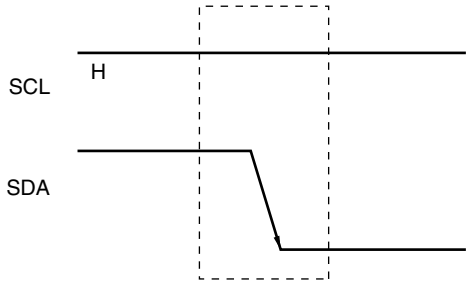
4.2.1 I²C bus function

(a) Start conditions

A start condition is met when the SCL pin is at high level (a serial clock has not been output) and the SDA pin changes from high level to low level.

A start condition is a signal that the master device outputs to the slave device when starting a serial transfer. This I²C bus only supports the slave function.

Figure 4-2. Start Conditions



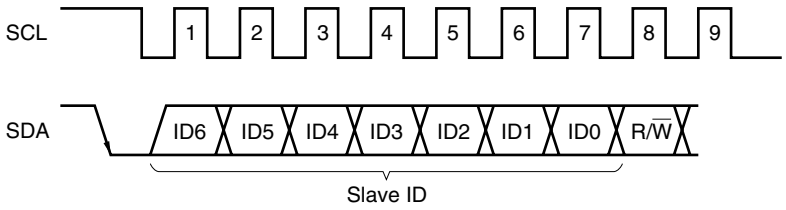
(b) Slave ID

The slave ID is defined by the 7 bits of data that follow the start condition.

This slave ID is used to select a specific slave out of several slaves connected to a bus line. Normally, one slave ID is assigned to one slave. Since the μPD71312 has two internal slave IDs, however, LCDCTL (control register) and LCDSEG (display memory) can be selected as access targets.

A slave detects via hardware that data on the SDA line is a slave ID, and checks whether the 7-bit data matches the slave ID (0111000 or 0111001 in the μPD71312). If the 7-bit data matches the slave ID values, the μPD71312 is selected and communicates with the master device until the master device transmits a start condition or stop condition.

Figure 4-3. Slave ID



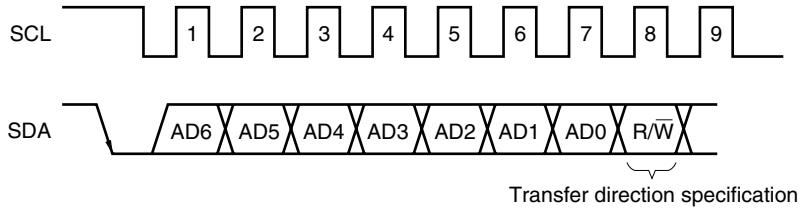
(c) Transfer direction specification

In addition to the 7-bit address data, the master device sends 1 bit that specifies the transfer direction.

Since this I²C bus only has a slave function, this bit is monitored to determine the transfer direction.

When this transfer direction specification bit has a value of “0”, it indicates that the master device is transmitting data to a slave device. When the transfer direction specification bit has a value of “1”, it indicates that the master device is receiving data from a slave device.

Figure 4-4. Transfer Direction Specification



(d) Acknowledge signal ($\overline{\text{ACK}}$)

$\overline{\text{ACK}}$ is a signal for receiving serial data at the transmission and reception sides.

The reception side returns $\overline{\text{ACK}}$ each time it has received 8-bit data. To generate $\overline{\text{ACK}}$, the reception side makes the SDA line low at high level of the ninth clock on the SCL line.

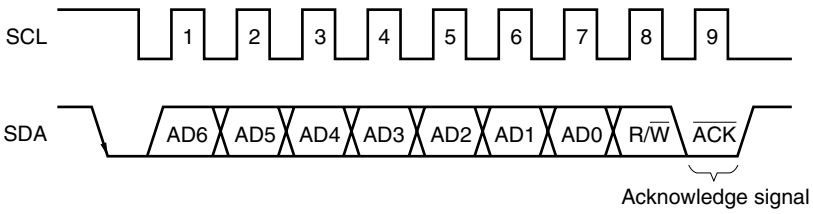
The transmission side detects whether $\overline{\text{ACK}}$ has been received from the reception side after transmitting 8-bit data. When $\overline{\text{ACK}}$ is returned, it is assumed that reception has been correctly performed and processing is continued.

This I²C bus has the following specifications.

When receiving: In normal operation, an $\overline{\text{ACK}}$ is returned upon every data reception.
If the master does not receive an $\overline{\text{ACK}}$, operation is judged as abnormal and a stop condition must be issued or operation must be reset.

When transmitting: By receiving an $\overline{\text{ACK}}$, the next data is transmitted according to the SCL clock.
If an $\overline{\text{ACK}}$ is not received, transfer from the master is judged as completed and the SDA line is released.

Figure 4-5. $\overline{\text{ACK}}$

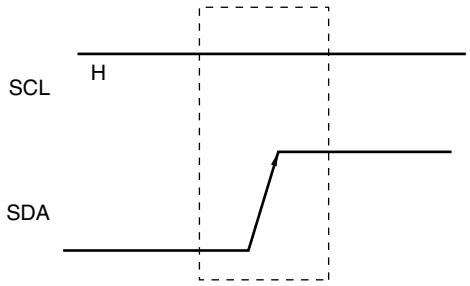


(e) Stop condition

When the SCL pin is at high level (when serial transfer has been completed and a serial clock has not been output), changing the SDA pin from low level to high level generates a stop condition.

A stop condition is a signal that the master device outputs to the slave device when serial transfer has been completed.

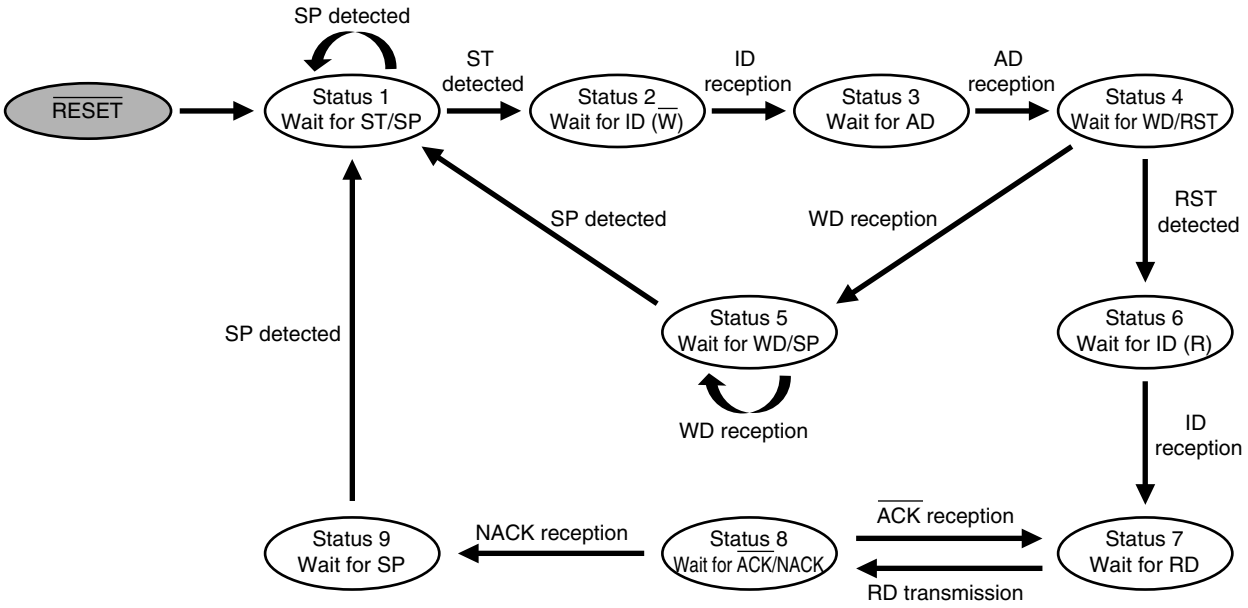
Figure 4-6. Stop Condition



4.2.2 Status transition diagram

Figure 4-7 shows the status transition diagram.

Figure 4-7. Shift Register Operation



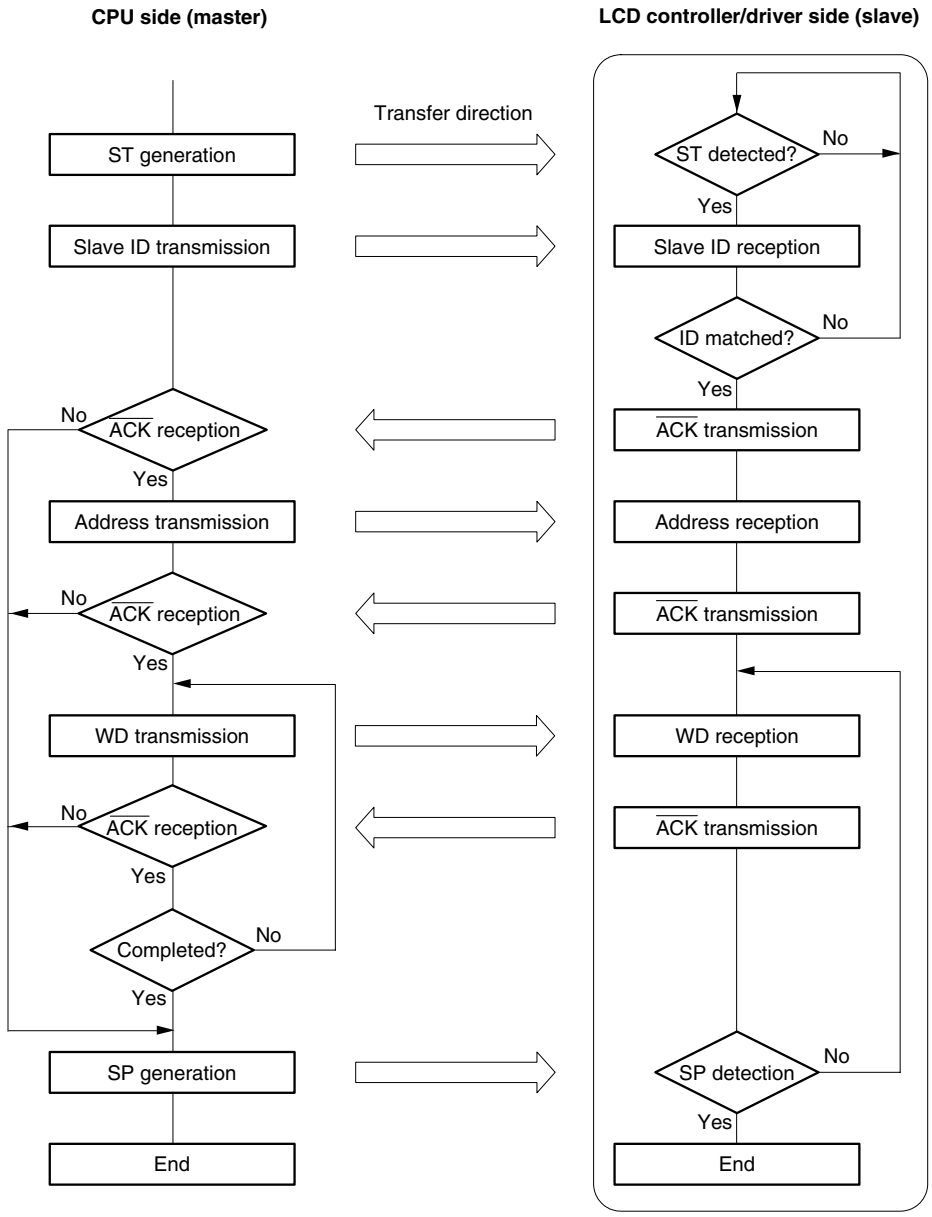
4.3 Write Operation

The processing procedure, format, and operation of writing to the LCD controller/driver via the I²C bus interface are explained below.

The LCD controller/driver register to be accessed can be specified with the slave ID and address (see Figure 3-3).

(1) Processing procedure

Figure 4-8. Processing Procedure of Write Operation



Remark ST: Start condition
RST: Restart condition
SP: Stop condition

(2) Communication format

Write data to each register on the LCD controller/driver starting from the start condition, slave ID, address, write data, then stop condition in that order.

Figure 4-9. Communication Format for Write Operation (When Writing Twice)

Access target	<1> ST	<2> Slave ID							<3> R/$\overline{W}$	<4> $\overline{ACK}$	<5> Address								<6> $\overline{ACK}$
LCDCTL	ST	0	1	1	1	0	0	0	0	$\overline{ACK}$	A7	A6	A5	A4	A3	A2	A1	A0	$\overline{ACK}$
LCDSEG	ST	0	1	1	1	0	0	1	0	$\overline{ACK}$	A7	A6	A5	A4	A3	A2	A1	A0	$\overline{ACK}$

<7> Write data 1								<8> $\overline{ACK}$	<9> Write data 2								<10> $\overline{ACK}$	<11> SP
D7	D6	D5	D4	D3	D2	D1	D0	$\overline{ACK}$	D7	D6	D5	D4	D3	D2	D1	D0	$\overline{ACK}$	SP
D7	D6	D5	D4	D3	D2	D1	D0	$\overline{ACK}$	D7	D6	D5	D4	D3	D2	D1	D0	$\overline{ACK}$	SP

Address
LCDCTL : A7, A6, A5, A4, A3, A2, A1, A0
LCDSEG : A7, A6, A5, A4, A3, A2, A1, A0

Address[Note]
LCDCTL : (A7, A6, A5, A4, A3, A2, A1, A0) + 1
LCDSEG : (A7, A6, A5, A4, A3, A2, A1, A0) + 1

Note The address is incremented by one based on the register read/write start address by continuously performing read/write access from transmissions of the start condition to stop condition. With this function, the address does not need to be set each time.

Cautions 1. Generate a stop condition if an access like the one shown below is made.
- **An access made in a format other than specified**
- **An access made with a slave ID other than specified**

2. When SDA is fixed at the low level output status due to noise, input a reset signal.

Remark ST: Start condition
SP: Stop condition
A7 to A0: Addresses for LCDCTL or LCDSEG

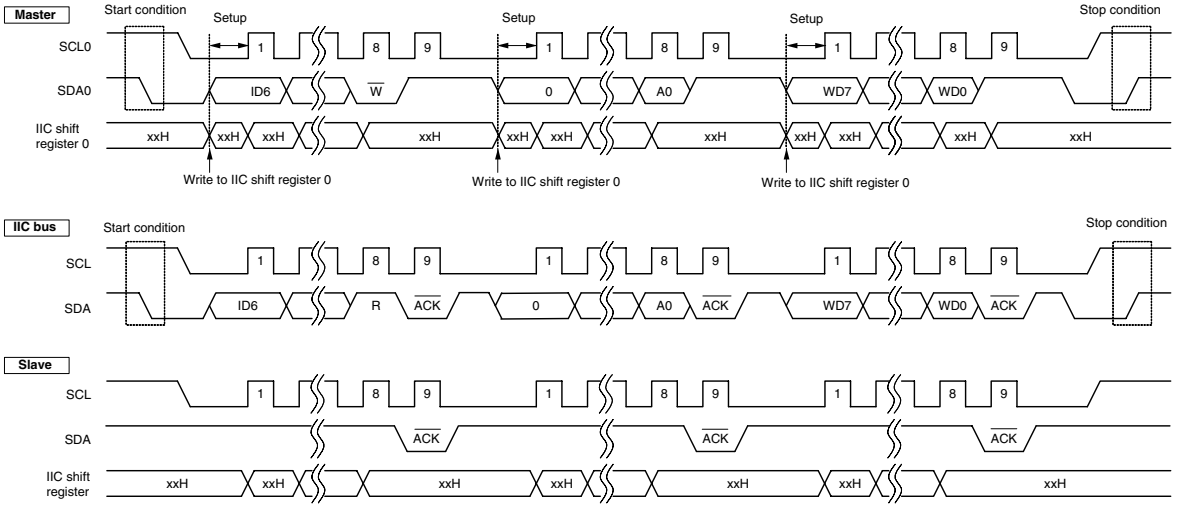
(3) Operation

The operation flow when transmitting write data twice is shown below.
Steps <1> to <11> correspond to <1> to <11> in Figure 4-9.

<1> The start condition is transmitted.
<2> The slave ID is transmitted (from the 1st to 7th clocks).
<3> R/$\overline{W}$ information (0) is transmitted (at the 8th clock).
<4> An acknowledge signal is received (at the rising edge of the 9th clock).
<5> The write start address is transmitted (from the 1st to 8th clocks following <4>).
<6> An acknowledge signal is received (at the rising edge of the 9th clock).
<7> Write data is transmitted (first time) (from the 1st to 8th clocks following <6>).
<8> An acknowledge signal is received (at the rising edge of the 9th clock).
<9> Write data is transmitted (second time) (from the 1st to 8th clocks following <8>).
(The address is automatically incremented by 1.)
<10> An acknowledge signal is received (at the rising edge of the 9th clock).
<11> The stop condition is transmitted.

Figure 4-10 shows the timing chart of the write operation.

Figure 4-10. Timing Chart of Write Operation



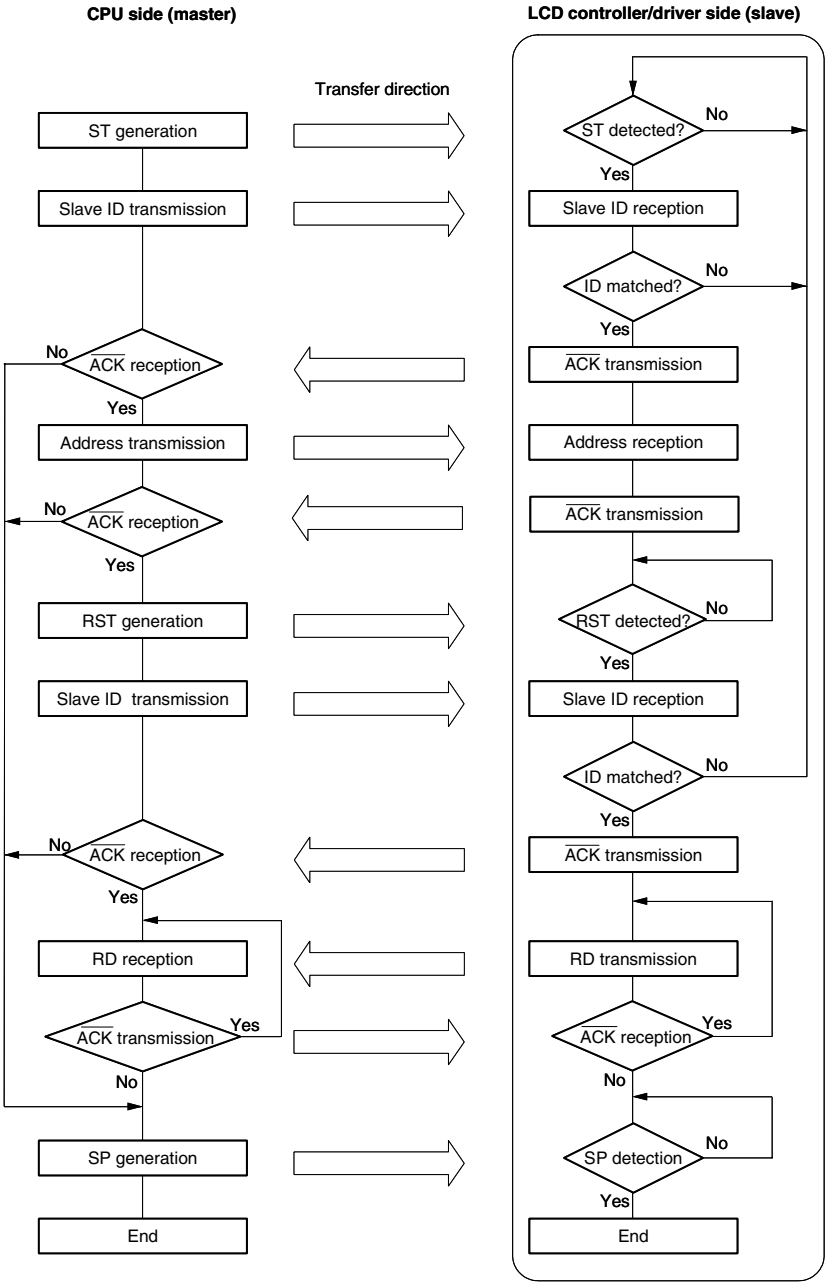
4.4 Read Operation

The processing procedure, format, and operation of reading the LCD controller/driver via the I²C bus interface are explained below.

The LCD controller/driver register to be accessed can be specified with the slave ID and address (see Figure 3-3).

(1) Processing procedure

Figure 4-11. Processing procedure of Read Operation



Remark ST: Start condition
RST: Restart condition
SP: Stop condition

(2) Communication format

Read data from each register on the LCD controller/driver starting from the start condition, slave ID, address, restart condition, slave ID, read data, then stop condition in that order.

Figure 4-12. Communication Format for Read Operation (When Reading Twice)

Access target	<1> ST	<2> Slave ID							<3> R/W	<4> ACK	<5> Address								<6> ACK
LCDCTL	ST	0	1	1	1	0	0	0	0	ACK	A7	A6	A5	A4	A3	A2	A1	A0	ACK
LCDSEG	ST	0	1	1	1	0	0	1	0	ACK	A7	A6	A5	A4	A3	A2	A1	A0	ACK

<7> RST	<8> Slave ID							<9> R/W	<10> ACK	<11> Read dara 1								<12> ACK
RST	0	1	1	1	0	0	0	1	ACK	D7	D6	D5	D4	D3	D2	D1	D0	ACK
RST	0	1	1	1	0	0	1	1	ACK	D7	D6	D5	D4	D3	D2	D1	D0	ACK

Address
LCDCTL : A7, A6, A5, A4, A3, A2, A1, A0
LCDSEG : A7, A6, A5, A4, A3, A2, A1, A0

<13> Read data2								<14> ACK	<15> SP
D7	D6	D5	D4	D3	D2	D1	D0	NACK	SP
D7	D6	D5	D4	D3	D2	D1	D0	NACK	SP

Address[Note]
LCDCTL : (A7, A6, A5, A4, A3, A2, A1, A0) + 1
LCDSEG : (A7, A6, A5, A4, A3, A2, A1, A0) + 1

Note The address is incremented by one based on the register read/write start address by continuously performing read/write access from transmissions of the start condition to stop condition. With this function, the address does not need to be set each time.

Cautions 1. Generate a stop condition if an access like the one shown below is made.
- **An access made in a format other than specified**
- **An access made with a slave ID other than specified**

2. When SDA is fixed at the low level output status due to noise, input a reset signal.

Remark ST: Start condition
RST: Restart condition
SP: Stop condition
A7 to A0: Addresses for LCDCTL or LCDSEG

(3) Operation

The operation flow when receiving read data twice is shown below.

Steps <1> to <15> correspond to <1> to <15> in Figure 4-12.

<1> The start condition is transmitted.

<2> The slave ID is transmitted (first time) (from the 1st to 7th clocks).

<3> R/$\overline{W}$ information (0) is transmitted (at the 8th clock).

<4> An acknowledge signal is received (at the rising edge of the 9th clock).

<5> The read start address is transmitted (from the 1st to 8th clocks following <4>).

<6> An acknowledge signal is received (at the rising edge of the 9th clock).

<7> The restart condition is transmitted.

<8> The slave ID is transmitted (second time) (from the 1st to 7th clocks following <7>).

<9> R/$\overline{W}$ information (1) is transmitted (at the 8th clock).

<10> An acknowledge signal is received (at the rising edge of the 9th clock).

<11> Read data is received (first time) (from the 1st to 8th clocks following <10>).

<12> An acknowledge signal is transmitted (from the falling edge of the 8th clock to the falling edge of the 9th clock).

<13> Read data is received (second time) (from the 1st to 8th clocks following <12>).
(The address is automatically incremented by 1.)

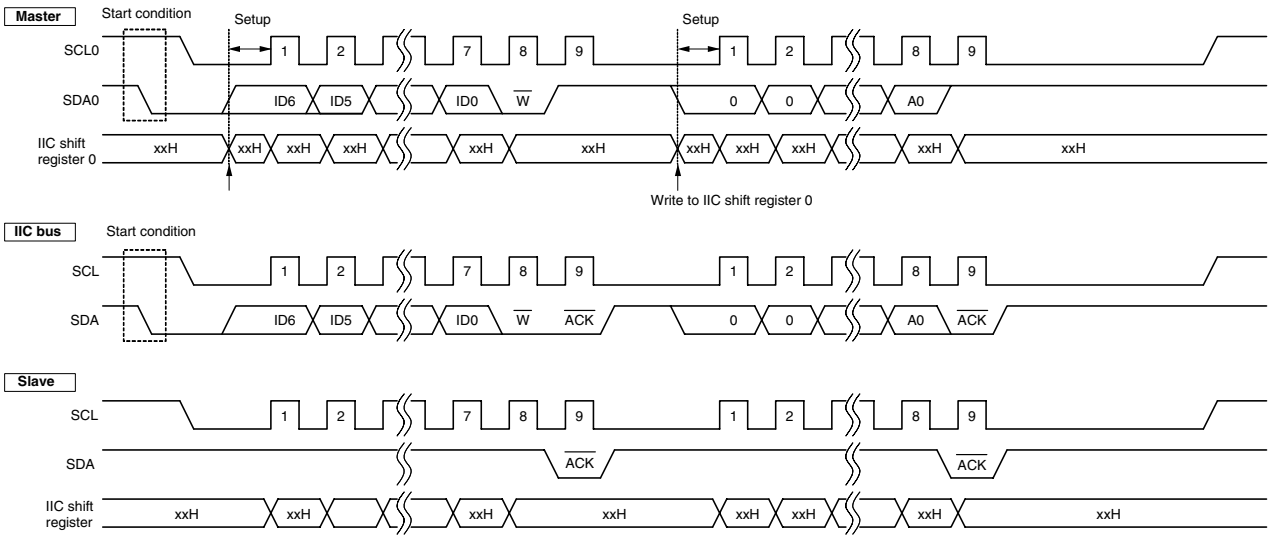
<14> Stop the acknowledge signal transmission.[Note]

<15> The stop condition is transmitted.

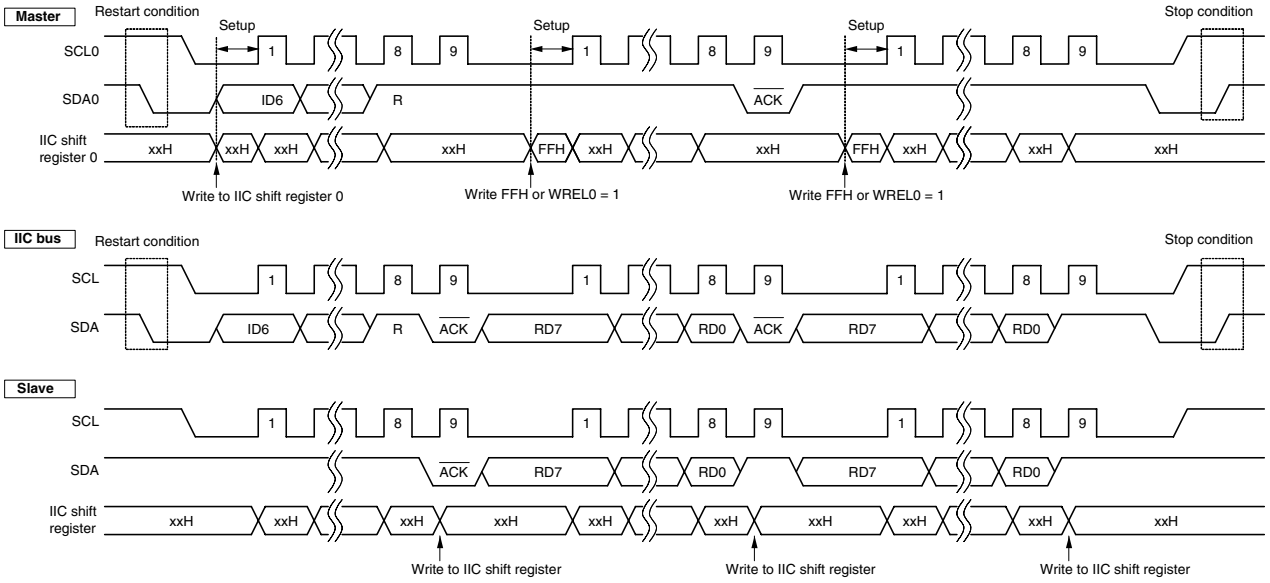
Note Do not transmit the acknowledge signal when completing data reception.

Figures 4-13 shows the timing chart of the read operation.

Figure 4-13. Timing Chart of Read Operation



(Continued from above)



CHAPTER 5 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	LV_{DD}		−0.3 to +6.5	V
	LV_{SS}		−0.3 to +0.3	V
Input voltage	V_{I1}	$\overline{RESET}$, LCLK, SCL, SDA	−0.3 to LV_{DD} + 0.3 Note 1	V
Output voltage	V_{O1}	SDA	−0.3 to LV_{DD} + 0.3 Note 1	V
	V_{O2}	S0 to S35, S36 to S39 Note 2, COM0 to COM3	−0.3 to V_{LC0} + 0.3 Note 1	V
Output current, low	I_{OL}	SDA	30	mA
Operating ambient temperature	T_A		−40 to +85	°C
Storage temperature	T_{stg}		−40 to +125	°C

Notes 1. Must be 6.5 V or lower.

2. 64-pin product only.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ LV_{DD} ≤ 5.5 V, LV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, low	I_{OL}	SDA		4.0 V ≤ LV_{DD} ≤ 5.5 V			15	mA
				2.7 V ≤ LV_{DD} < 4.0 V			3	mA
				1.8 V ≤ LV_{DD} < 2.7 V			0.6	mA
Input voltage, high	V_{IH1}	SCL, SDA		2.7 V ≤ LV_{DD} ≤ 5.5 V	0.7LV_{DD}		LV_{DD}	V
				1.8 V ≤ LV_{DD} < 2.7 V	0.8LV_{DD}		LV_{DD}	V
	V_{IH2}	$\overline{RESET}$, LCLK		2.7 V ≤ LV_{DD} ≤ 5.5 V	0.8LV_{DD}		LV_{DD}	V
				1.8 V ≤ LV_{DD} < 2.7 V	0.85LV_{DD}		LV_{DD}	V
Input voltage, low	V_{IL1}	SCL, SDA		2.7 V ≤ LV_{DD} ≤ 5.5 V	0		0.3LV_{DD}	V
				1.8 V ≤ LV_{DD} < 2.7 V	0		0.2LV_{DD}	V
	V_{IL2}	$\overline{RESET}$, LCLK		2.7 V ≤ LV_{DD} ≤ 5.5 V			0.2LV_{DD}	V
				1.8 V ≤ LV_{DD} < 2.7 V			0.15LV_{DD}	V
Output voltage, low	V_{OL}	SDA	I_{OL} = 15 mA	4.0 V ≤ LV_{DD} ≤ 5.5 V			2.0	V
			I_{OL} = 3 mA				0.4	V
			I_{OL} = 3 mA	2.7 V ≤ LV_{DD} < 4.0 V			0.6	V
			I_{OL} = 2 mA				0.4	V
			I_{OL} = 600 μA	1.8 V ≤ LV_{DD} < 2.7 V			0.4	V
Input leakage current, high	I_{LIH}	V_I = LV_{DD}	SCL, SDA, $\overline{RESET}$, LCLK				3	μA
Input leakage current, low	I_{LIL}	V_I = 0 V	SCL, SDA, $\overline{RESET}$, LCLK				–3	μA
Output leakage current, high	I_{LOH}	V_O = LV_{DD}					3	μA
Output leakage current, low	I_{LOL}	V_O = 0 V					–3	μA
LCLK pull-down resistor	R_{LCLK}	After reset			10	30	100	kΩ
Supply current[Note]	I_{DD1}	When LCD (including booster circuit) is stopped and IIC is operating		LV_{DD} = 5.0 V ±10%		25	50	μA
				LV_{DD} = 3.0 V ±10%		13	30	μA
	I_{DD2}	When only LCD booster circuit is operating and IIC is in standby status		LV_{DD} = 5.0 V ±10%		2	36	μA
				LV_{DD} = 3.0 V ±10%		1.5	16	μA
	I_{DD3}	When LCD display is operating (voltage boosting method) and IIC is in standby status		LV_{DD} = 5.0 V ±10%		5	45	μA
				LV_{DD} = 3.0 V ±10%		4	22	μA
	I_{DD4}	When LCD (including booster circuit) is stopped and IIC is in standby status		LV_{DD} = 5.0 V ±10%		0.1	5	μA
				LV_{DD} = 3.0 V ±10%		0.05	3	μA
	I_{DD5}	When LCD display is operating (resistance division method) and IIC is in standby status		LV_{DD} = 5.0 V ±10%		3.1	14	μA
				LV_{DD} = 3.0 V ±10%		2.55	9	μA

Note Total current flowing into the internal power supply (LV_{DD}), including the input leakage current flowing when the level of the input pin is fixed to LV_{DD} or LV_{SS}. The current flowing into the pull-up resistors of the I^2C communication pins is not included.

AC Characteristics

(1) Basic operation

(T_A = –40 to +85°C, 1.8 V ≤ LV_{DD} ≤ 5.5 V, LV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum operating frequency	LCLK				400	kHz
	SCL				400	kHz
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs

(2) Serial interface (IIC)

(T_A = –40 to +85°C, 1.8 V ≤ LV_{DD} ≤ 5.5 V, LV_{SS} = 0 V)

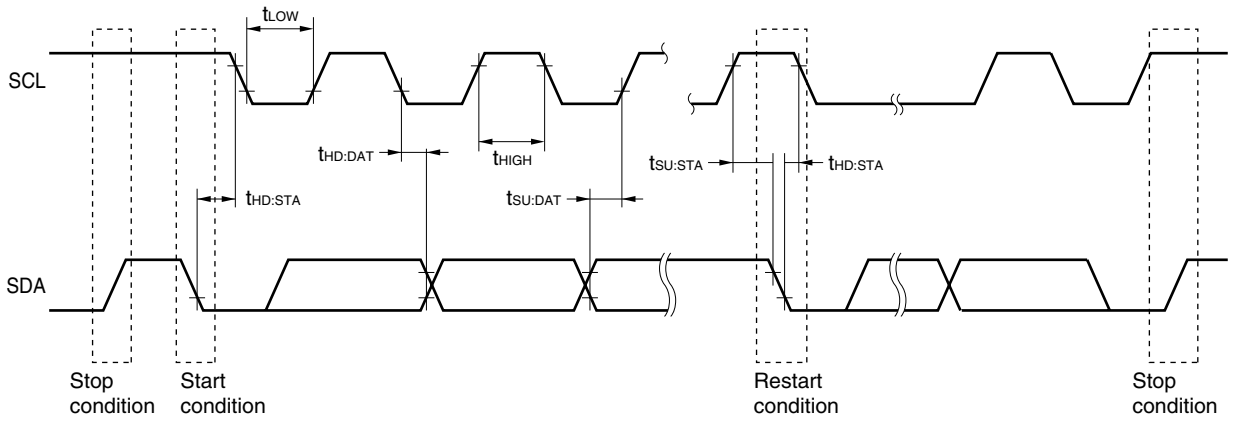
Parameter	Symbol	Standard Mode		High-Speed Mode		Unit
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Setup time of start/restart condition[Note 1]	$t_{SU:STA}$	4.8	–	0.7	–	μs
Hold time	$t_{HD:STA}$	4.1	–	0.7	–	μs
Hold time when SCL = "L"	t_{LOW}	5.0	–	1.25	–	μs
Hold time when SCL = "H"	t_{HIGH}	5.0	–	1.25	–	μs
Data setup time (reception)	$t_{SU:DAT}$	0	–	0	–	μs
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	0.47	4.0	0.23	1.00	μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{\text{ACK}}$ (acknowledge) timing.

Caution Only communication with IIC0 of the 78K0/Kx2 and 78K0R/Kx3 is possible. It does not support the simplified IIC of the 78K0R/Kx3.

Timing Definition on I^2C Bus



LCD Characteristics (T_A = –40 to +85°C)

(1) Resistance division method

(a) Static display mode (2.0 V ≤ LV_{DD} ≤ 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}		2.0		LV_{DD}	V
LCD divider resistor[Note 1]	R_{LCD}		60	100	150	kΩ
LCD output resistor[Note 2] (Common)	R_{ODC}				40	kΩ
LCD output resistor[Note 2] (Segment)	R_{ODS}				200	kΩ
Pull-up resistor[Note 3] between LV_{DD} and V_{LC0}	R_{LU}	LV_{DD} = 5.0 V, V_{LC0} = 3.0 V		7.3		kΩ

(b) 1/3 bias method (2.5 V ≤ LV_{DD} ≤ 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}		2.5		LV_{DD}	V
LCD divider resistor[Note 1]	R_{LCD}		60	100	150	kΩ
LCD output resistor[Note 2] (Common)	R_{ODC}				40	kΩ
LCD output resistor[Note 2] (Segment)	R_{ODS}				200	kΩ
Pull-up resistor[Note 3] between LV_{DD} and V_{LC0}	R_{LU}	LV_{DD} = 5.0 V, V_{LC0} = 3.0 V		7.3		kΩ

(c) 1/2 bias method (2.7 V ≤ LV_{DD} ≤ 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}		2.7		LV_{DD}	V
LCD divider resistor[Note 1]	R_{LCD}		60	100	150	kΩ
LCD output resistor[Note 2] (Common)	R_{ODC}	T_A = –10 to +85°C			40	kΩ
		T_A = –40 to –10°C			60	kΩ
LCD output resistor[Note 2] (Segment)	R_{ODS}				200	kΩ
Pull-up resistor[Note 3] between LV_{DD} and V_{LC0}	R_{LU}	LV_{DD} = 5.0 V, V_{LC0} = 3.0 V		7.3		kΩ

Notes 1. When internal resistors are connected only.

2. The output resistor is a resistor connected between one of the V_{LC0}, V_{LC1}, V_{LC2} and LV_{SS} pins, and either of the SEG and COM pins.

3. Disconnected when LCD mode is entered by setting the LCD mode setting register (LCDMD).

Remark The figures in the above table indicate the values when a 0.47 μF capacitor is connected between V_{LC0} to V_{LC2} and GND.

(2) Internal voltage boosting method (1.8 V ≤ LV_{DD} ≤ 5.5 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{LCD2}	C1 to C4[Note 1] = 0.47 μF[Note 2]	GAIN = 0	CTSEL1 = 0, CTSEL0 = 1	1.35	1.43	1.51	V
				CTSEL1 = 0, CTSEL0 = 0	1.42	1.50	1.58	V
				CTSEL1 = 1, CTSEL0 = 1	1.48	1.57	1.66	V
				CTSEL1 = 1, CTSEL0 = 0	1.54[Note 3]	1.63[Note 3]	1.72[Note 3]	V
			GAIN = 1	CTSEL1 = 0, CTSEL0 = 1	0.87	0.93	1.00	V
				CTSEL1 = 0, CTSEL0 = 0	0.94	1.00	1.06	V
				CTSEL1 = 1, CTSEL0 = 1	1.00	1.07	1.14	V
				CTSEL1 = 1, CTSEL0 = 0	1.06	1.13	1.20	V
Doubler output voltage	V_{LCD1}	C1 to C4[Note 1] = 0.47 μF[Note 2]				2 V_{LCD2}		V
Tripler output voltage	V_{LCD0}	C1 to C4[Note 1] = 0.47 μF[Note 2]				3 V_{LCD2}		V
Voltage boost wait time[Note 4]	t_{VAWAIT}	GAIN = 1	4.5 V ≤ LV_{DD} ≤ 5.5 V		4			s
			1.8 V ≤ LV_{DD} < 4.5 V		0.5			s
		GAIN = 0			0.5			s
LCD output resistor[Note 5] (Common)	R_{ODC}						40	kΩ
LCD output resistor[Note 5] (Segment)	R_{ODS}						200	kΩ

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{LC0} and GND
C3: A capacitor connected between V_{LC1} and GND
C4: A capacitor connected between V_{LC2} and GND

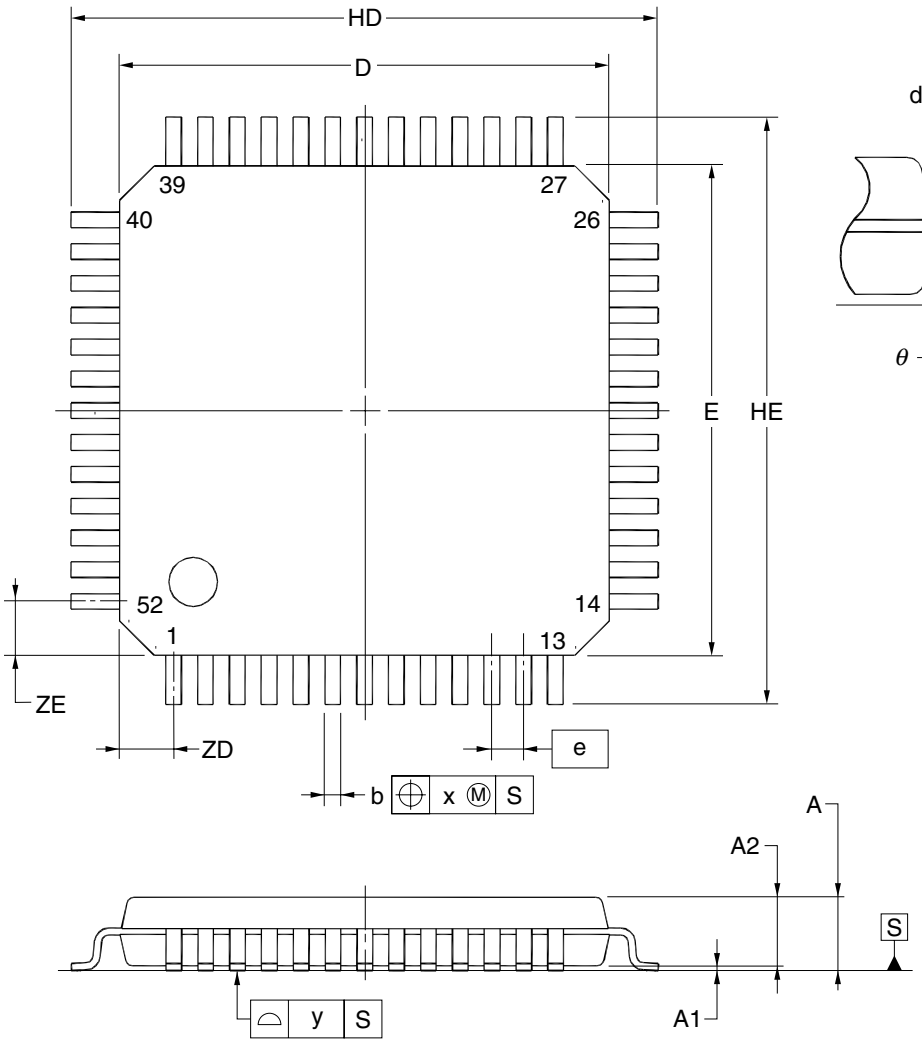
2. When the frame frequency is 128 Hz or lower, the SEG and COM pins are left open, and (LCDON, SCOC, VLCON) = 111B.

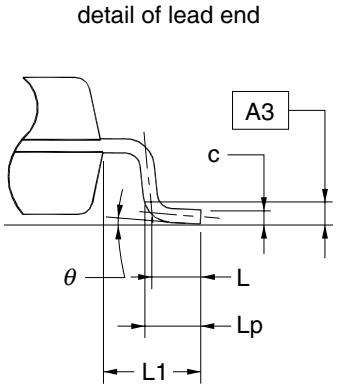
3. When operating voltage range is 2.0 V ≤ LV_{DD} < 5.5 V.

4. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

5. The output resistor is a resistor connected between one of the V_{LC0}, V_{LC1}, V_{LC2} and LV_{SS} pins, and either of the SEG and COM pins.

52-PIN PLASTIC LQFP(10x10)





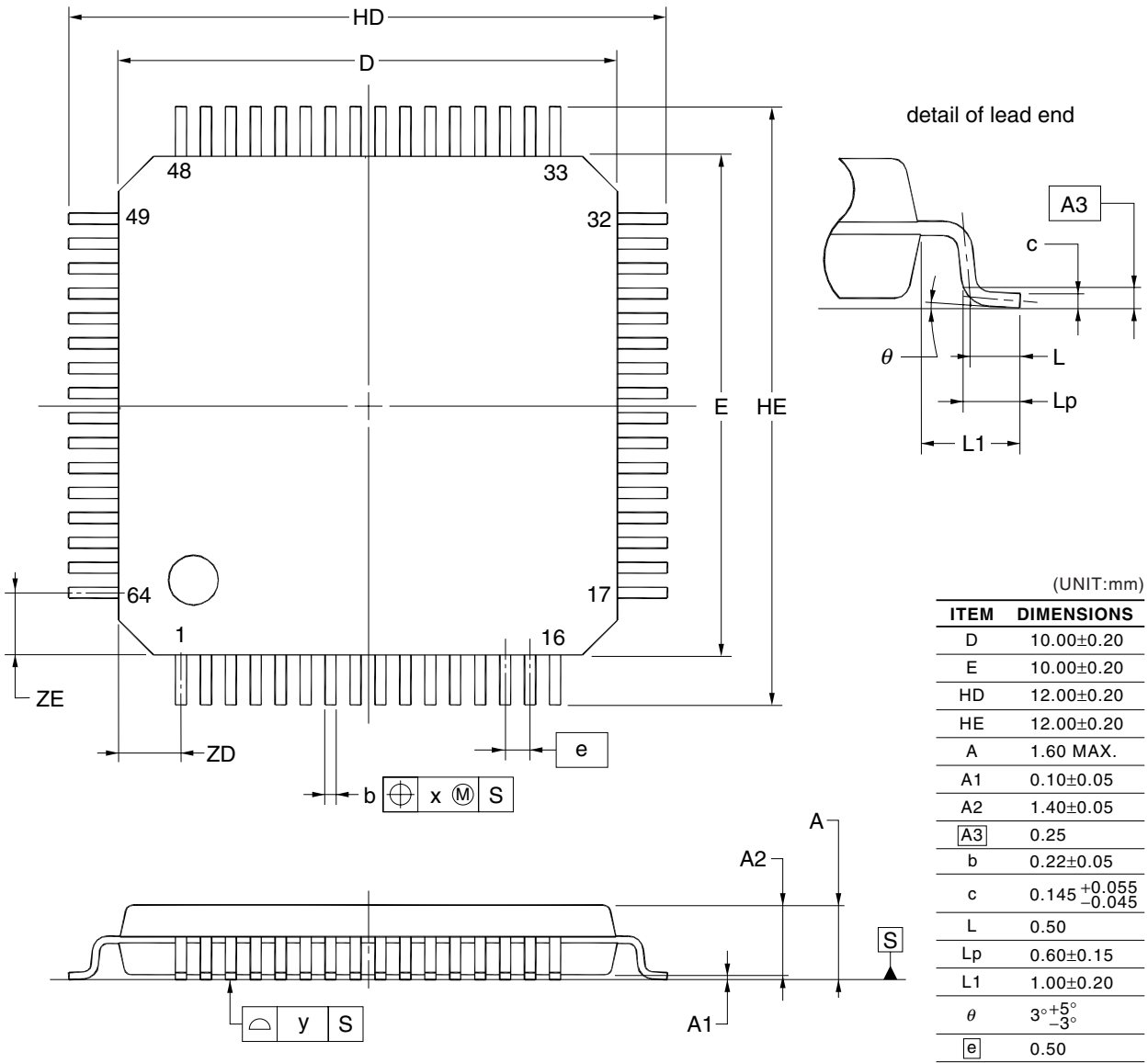
(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.32^{+0.08}_{-0.07}$
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.65
x	0.13
y	0.10
ZD	1.10
ZE	1.10

P52GB-65-UET-1

NOTE
Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

64-PIN PLASTIC LQFP(FINE PITCH)(10x10)



(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

P64GB-50-UEU-1

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

CHAPTER 7 RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Table 7-1. Surface Mounting Type Soldering Conditions

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: Three times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 to 72 hours)	IR60-207-3
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

For further information,
please contact:

NEC Electronics Corporation
1753, Shimonumabe, Nakahara-ku,
Kawasaki, Kanagawa 211-8668,
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Tel: 044-435-5111
http://www.necel.com/

[America]

NEC Electronics America, Inc.
2880 Scott Blvd.
Santa Clara, CA 95050-2554, U.S.A.
Tel: 408-588-6000
800-366-9782
http://www.am.necel.com/

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NEC Electronics (Europe) GmbH
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40472 Düsseldorf, Germany
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http://www.eu.necel.com/

Hanover Office
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81829 München
Tel: 0 89 92 10 03-0

Stuttgart Office
Industriestrasse 3
70565 Stuttgart
Tel: 0 711 99 01 0-0

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France
Tel: 01-3067-5800

Sucursal en España
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28007 Madrid, Spain
Tel: 091-504-2787

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Täby Centrum
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18322 Täby, Sweden
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Tel: 02-667541

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http://www.tw.necel.com/

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Singapore 307684
Tel: 6253-8311
http://www.sg.necel.com/

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11F., Samik Lavied'or Bldg., 720-2,
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Seoul, 135-080, Korea
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