TDHBG1200DC100-KIT

1.2 kW Half-bridge Synchronous Buck or Boost Evaluation Platform

TDHBG1200DC100: 1.2 kW Half-bridge Evaluation Board

Introduction

The TDHBG1200DC100 half-bridge evaluation board provides the elements of a simple buck or boost converter, using the Transphorm Daughter Card TDHB-65H070L-DC for basic study of switching characteristics and efficiency achievable with Transphorm's 650V GaN FETs in the standard 8x8 PQFN package. In either buck or boost mode the circuit can be configured for synchronous rectification. Jumpers allow use of a single logic input or separate hi/lo inputs. The high-voltage input and output can operate at up to 400Vdc, with a power output of up to 1.2kW. The inductor provided is intended for efficient operation at 100kHz, although other inductors and other frequencies may be easily used.

Figure 1A

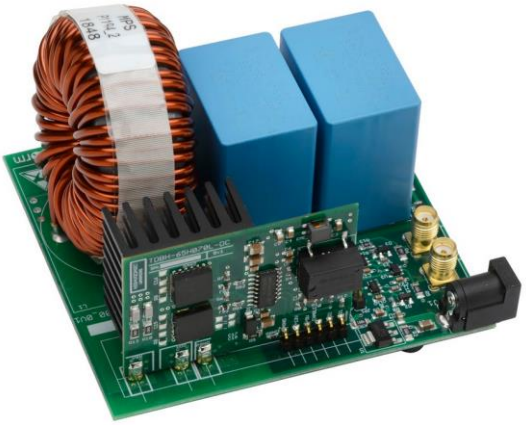

Figure 1B.

TDHBG1200DC100 half-bridge evaluation board

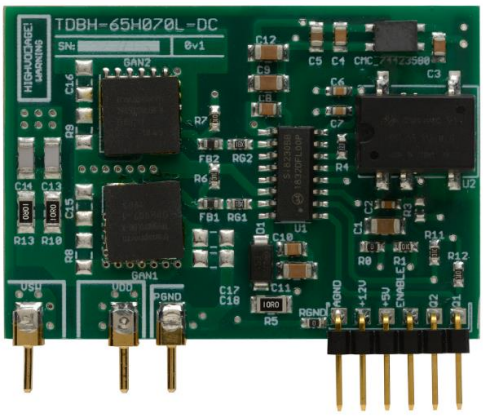

Figure 2

TDHB-65H070L-DC daughter card

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Warnings

TDHGB1200DC100 input/output specifications

High-voltage input/output: 400Vdc max

Auxiliary supply (J1): 10V min, 18V max

Logic inputs: nominal 0V-5V

Pulse-generation circuit: Vlo < 1.5V, Vhi > 3.0V

Direct connection to gate driver: Vlo < 0.8V, Vhi > 2.0V

SMA coaxial connectors

Switching frequency: configuration-dependent

Lower limit determined by peak inductor current

Upper limit determined by desired dead-time and power dissipation

Power dissipation in the GaN FET is limited by the maximum junction temperature. Refer to the TP65H070LxG datasheets.

Circuit description

The circuit comprises a simple half-bridge featuring 1 TP65H070LDG and 1 TP65H070LSG GaN FETs, as indicated in the block diagram of Figure 3. Two high-voltage ports are provided which can serve as either input or output, depending on the configuration—boost or buck. In either case one FET acts as the active power switch while the other carries the freewheeling current. The latter device may be enhanced, as a synchronous rectifier, or not. With GaN FETs the reverse recovery charge is low and there is no need for additional freewheeling diodes. Two input connectors are provided which can be connected to sources of logic-level command signals for the hi/lo gate driver. Both inputs may be driven by off-board signal sources; or alternatively, a single signal source may be connected to an on-board pulse-generator circuit which generates the two non-overlapping pulses. Jumpers determine how the input signals are used.

An inductor is provided as a starting point for investigation. This is a 440μH toroid intended to demonstrate a reasonable compromise between size and efficiency for power up to 1.2kW at a switching frequency of 100kHz.

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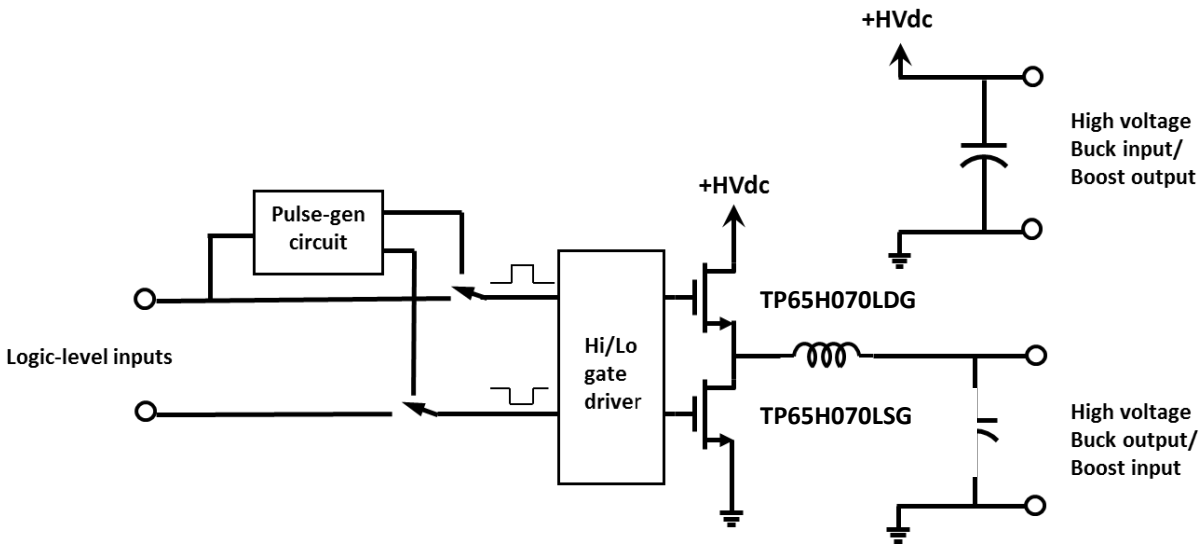

Figure 3. Functional block diagram

Using the evaluation

The mother board and daughter card can be used for evaluation of basic switching functionality in a variety of circuit configurations. It is not a complete circuit, but rather a building block. It can be used in steady-state DC/DC converter mode with output power up to 1.2kW.

When operating the board at high power (>500W), an external fan should be used to cool the heatsink on the daughtercard.

Configurations

Figure 4 shows the basic power connections for buck and boost modes. For buck mode, the HVdc input (terminals J2, J3) is connected to the high-voltage supply and the output is taken from terminals J5 and J7. For boost mode, the connections are reversed.

Note that in boost mode a load must be connected. The load current affects the output voltage up to the transition from DCM to CCM. In buck mode the load may be an open circuit.

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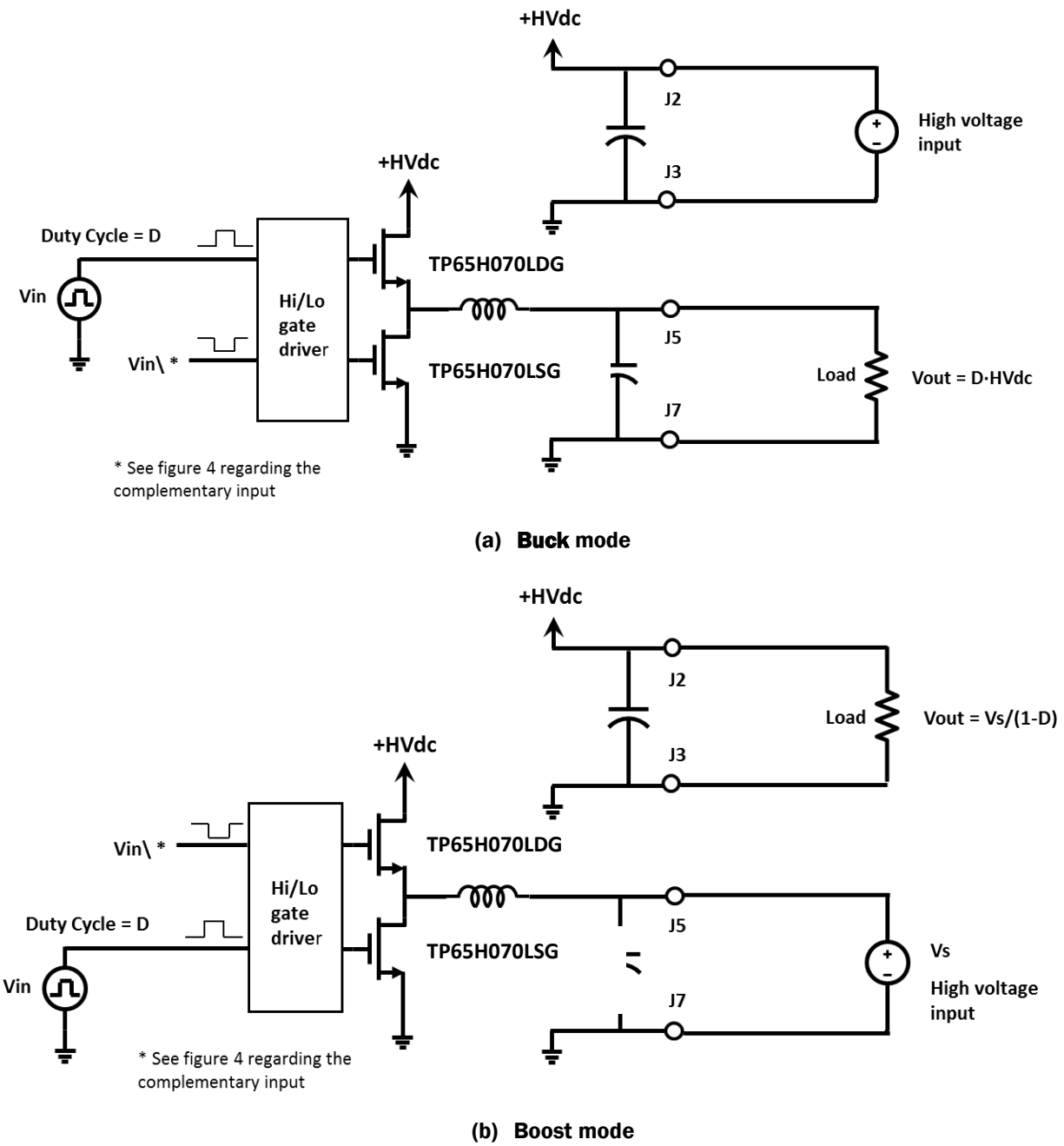

Figure 4. Supply and load connections for buck (a) and boost (b) configurations

Figure 5 shows possible configurations for the gate-drive signals. In Figure 5(a), a single input from an external signal source is used together with the on-board pulse generation circuit. J4 is used, J6 is left open circuit. Jumpers JP1 and JP2 are in the top position, as shown. If the high-side transistor is to be the active switch (e.g. buck mode), then the duty cycle of the input source should simply be set to the desired duty cycle (D). If the low-side transistor is to be the active switch (e.g. boost mode) the duty cycle of the input source should be set to (1-D), where D is the desired duty cycle of the low-side switch. This configuration results in synchronous rectification. If it is desired to let the device carrying the freewheeling current act as a diode, then the appropriate jumper should be placed so that the pull-down resistor is connected to the driver. Figure 5(b) shows a buck-mode

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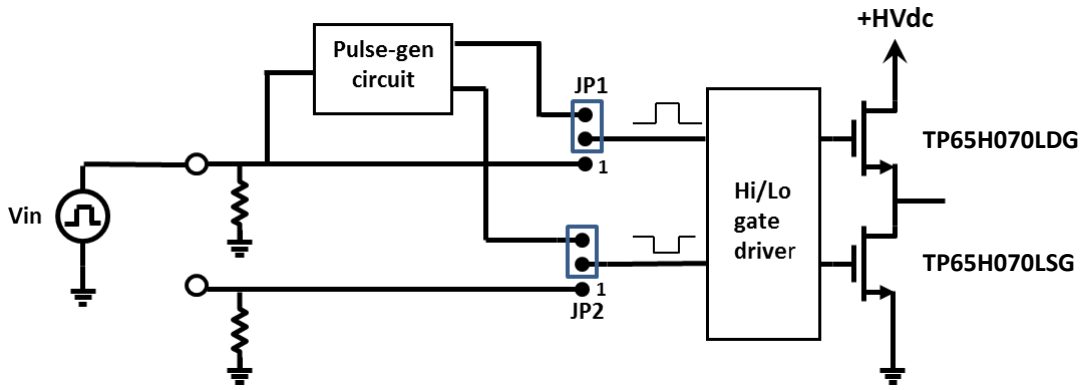
configuration where the low-side device is not enhanced. Finally, Figure 5(c) shows use of two external signal sources as inputs to the gate driver.

For any configuration, an auxiliary supply voltage of 10V-18V must be supplied at connector J1.

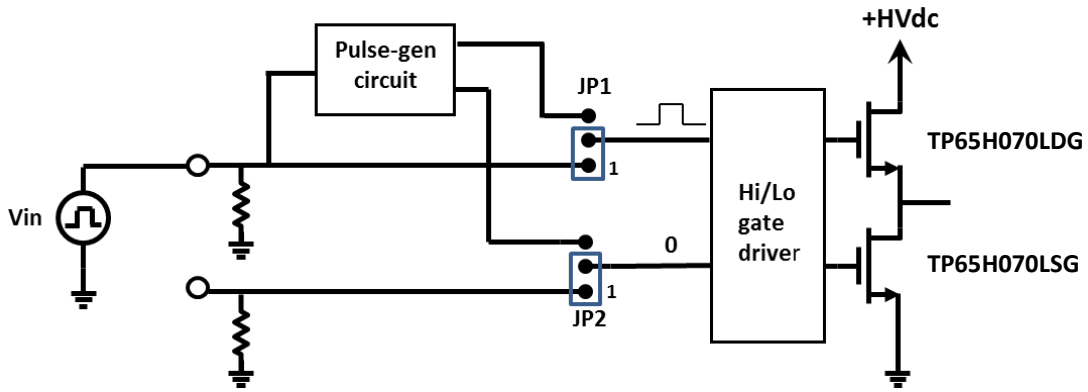
Pull-down resistors R5 and R6 have a value of 4.99k. If a 50Ω signal source is used and 50Ω termination is desired, then R5 and R6 may be replaced (or paralleled) with 1206 size 50Ω resistors.

Boost mode/buck mode operation

For buck mode operation, A typical 400Vin - 200Vout buck operation with 50% duty cycle, 7A max output current is seen at 1200W. On the other hand, for 200Vin - 400Vout boost mode operation at 1.2kW, 7A max output current can be reached with a duty cycle of 50%. Thermal cooling must be enforced for high current switching at all times.



(a)



(b)

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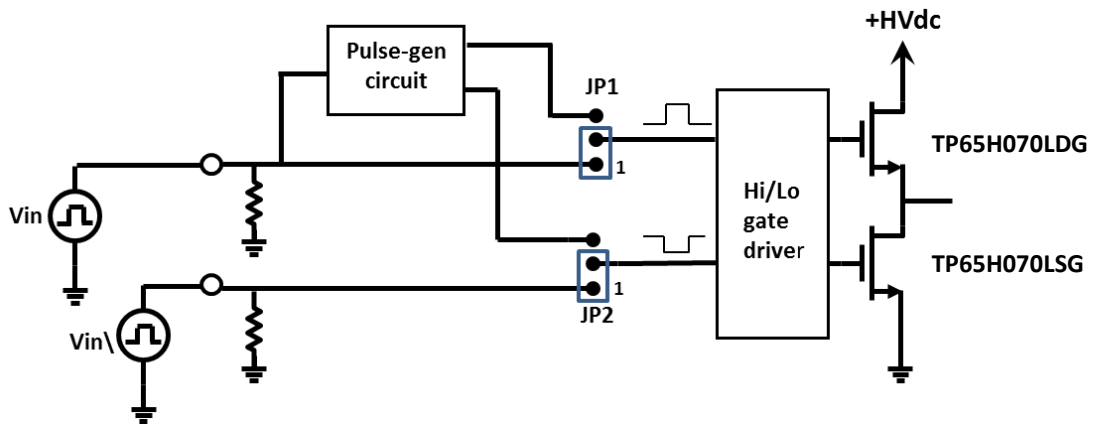

(c)

Figure 5. Input configurations
(a) using a single source for either buck or boost mode
(b) buck mode without synchronous rectification
(c) using two signal sources

Dead time control

The required form of the gate-drive signals is shown in Figure 6. The times marked A are the dead times when neither transistor is driven on. The dead time must be greater than zero to avoid shoot-through currents. The Si8230BB gate drive chip ensures a minimum dead time based on the value of resistor R4, connected to the DT input. The dead time in ns is equal to the resistance in kΩ x 10, so the default value of 12k corresponds to 120ns. This will add to any dead time already present in the input signals. The on-board pulse generator circuit; for example, creates dead times of about 60ns. The resulting dead time at the gate pins of GAN1 and GAN2 is about 240ns. Either shorting or removing R4 will reduce the dead time to 60ns.

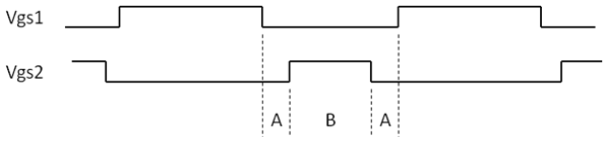

Figure 6. Non-overlapping gate pulses

Design details

See Figure 7 for a detailed circuit schematic and Figure 8 for the PCB layers (also included in the design files). The parts list for TDHBG1200DC100 can be found in Table 1. The parts list for TDHB-65H070L-DC can be found in Table 2.

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Table 1. TDHBG1200DC100 half-bridge evaluation board bill of materials (BOM)

Designator	Qty	Value	Description	Part Number	Manufacturer
U3	1		74LVC1G17DBV	SN74LVC1G17DBVR	Texas Instruments
JP1, JP2	2		JP2E	68001-403HLF	FCI
J2, J3, J5, J7	4		KEYSTONE_7691	7691	Keystone
LED1	1		LEDCHIP-LED0805	SML-211UTT86	Rohm
U1	1		LT3082	LT3082EST#PBF	Linear Technology
J1	1		PJ-002AH	PJ-002AH	CUI
LDS	1		TEKTRONIX-PCB	131-4353-00	Tektronix
C7	1	.1u	C-EUC1812	C1812V104KDRACTU	Kemet
C20, C21, C22	3	.1u	C-USC0603	06033C104JAT2A	AVX
C8, C17	2	.1u	C-USC2225K	VJ2225Y104KXGAT	Vishay
R12	1	0	R-US_R1206	ERJ-8GEY0R00V	Panasonic
R8, R10	2	1k	R-US_R0603	RC0603FR-071KL	Yageo
C2	1	1u	C-EUC0805	CC0805ZRY5V8BB105	Yageo
C3	1	2.2u	C-EUC0805	C2012X5R1E225K125AC	TDK
R13	1	2k	R-US_R0805	RC0805FR-072KL	Yageo
C5, C6	2	4.7n	C-EUC1206	C1206C472KDRACTU	Kemet
R5, R6	2	4.99K	R-US_R1206	RMCF1206FT4K99	Stackpole
R1	1	4.99k	R-US_R1206	RMCF1206FT4K99	Stackpole
R3	1	10MEG	R-US_R1206	06035A101FAT2A	AVX
C9, C25	2	10uF	6U_JC	B32794D2106K	Epcos
C1	1	22u	C-USC1206	CL31A226MOCLNNC	Samsung
U4, U5	2	74AHC1G86DBV	74AHC1G86DBV	SN74AHC1G86DBVR	Texas Instruments
C19, C23	2	100pF	C-USC0603	ESR03EZPJ104	Rohm
L1	1	440uH	440UH_MPP	CWS CWS-1MP-12640	CWS CWS-1MP-12640
R2	1	499k	R-US_R1206	Stackpole	R2
D2, D3	2	BAT54	BAT54	BAT54W	NXP
J4, J6	2	BU-SMA-G	BU-SMA-G	5-1814832-1	TE connectivity
U$1	3	GAN_CARD_CONNECTOR	GAN_CARD_CONNECTOR	a32386-nd	a32386-nd
U$1	1	GAN_CARD_CONNECTOR	GAN_CARD_CONNECTOR	wm8112-nd	wm8112-nd
	1	Daughter card	Daughter card	TDHB65H070L-DC	Transphorm

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Table 2. TDHBG1200DC100 half-bridge evaluation board bill of materials (BOM)

Qty	Value	Device	Parts	Digikey PN
2	0	R-US_R0603	R0, RGND	RMCF0603ZT0R00CT-ND
3	0.1uF	C-USC0603	C2, C6, C7	399-1282-1-ND
4	0.1uF	C-USC0805	C3, C4, C8, C10	732-8109-1-ND
1	1.3uH	CMC_74423580	CMC1	732-4222-1-ND
3	10	R-US_R1206	R5, R10, R13	408-1869-1-ND
1	100k	R-US_R0603	R3	dni
2	100nF	C-USC1206	C17, C18	399-16678-1-ND
5	10k	R-US_R0603	R1, R6, R7, R11, R12	A126331CT-ND
1	10uF	C-USC0805	C5	490-5523-1-ND
3	10uF	C-USC1206	C9, C11, C12	587-2259-1-ND
1	12k	R-US_R0603	R4	RMCF0603JT12K0CT-ND
2	15	R-US_R0603	RG1, RG2	P15GCT-ND
2	15	R-US_R1206	R8, R9	dni
2	180	R-US_R0603	FB1, FB2	490-5263-1-ND
2	22pF	C-USC1206	C15, C16	dni
1	22uF	C-USC1206	C1	1276-1803-1-ND
2	4.7nF	C-USC1206	C13, C14	445-9099-1-ND
1	6PINCONN	6PINCONN	P1	WM8112-ND
1	ESJ1	DIODE-DO214AC	D1	ES1JFSCT-ND
1	TP65H070LSG	TP65H070LSG	GAN2	TP65H070LSG
1	PDS1-S5-S12	PDS1-S5-S12-M-TR	U2	102-2686-1-ND
1	SI8230	SI8230	U1	SI8230BB-D-IS1-ND
1	TP65H070LDG	TP65H150LDG_2	GAN1	TP65H070LDG
3		CONN PC PIN CIRC 0.040DIA GOLD	VSW, VDD, PGND	ED1278-ND
1		HEATSINK	HS	dni

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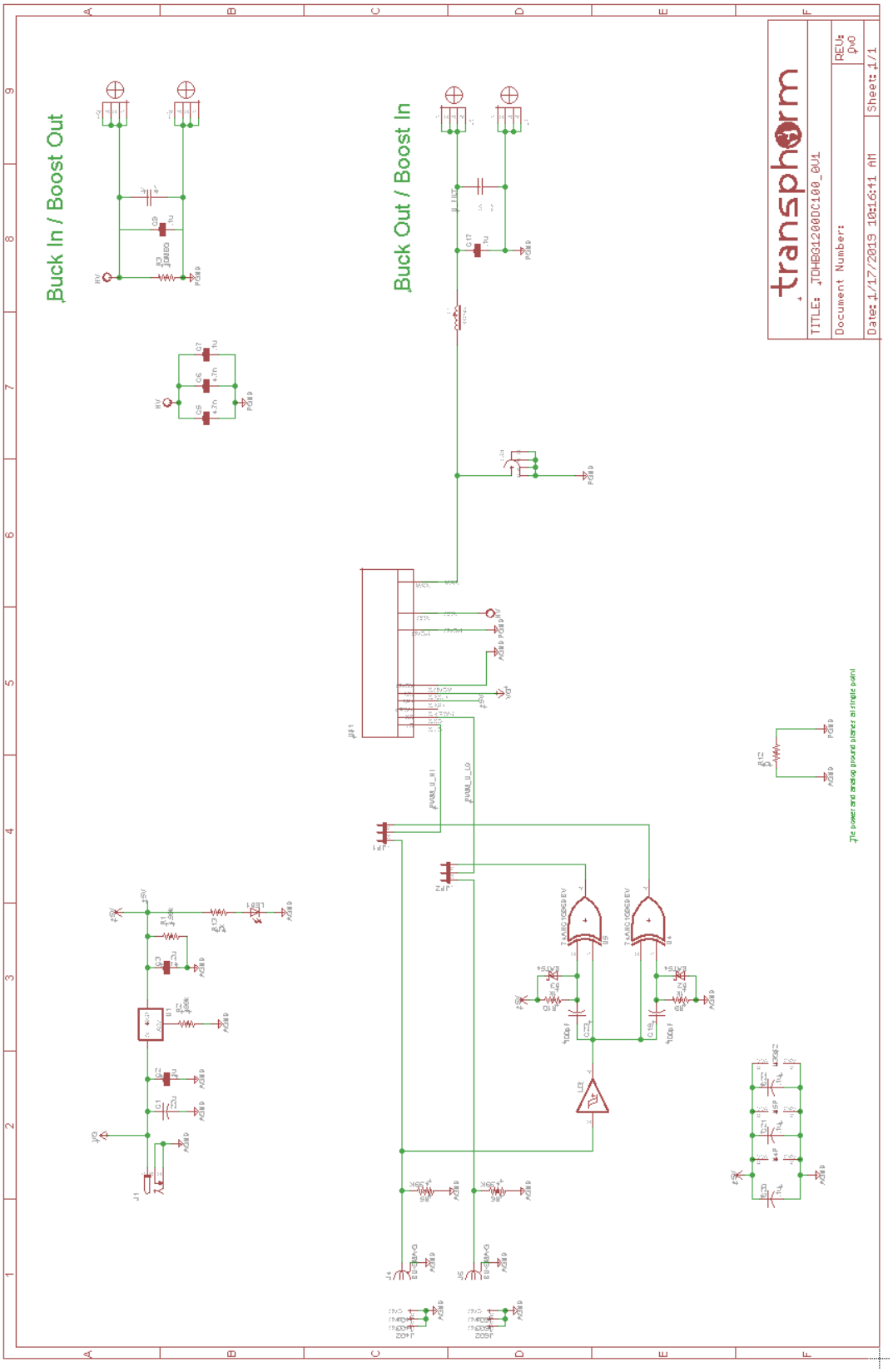

Figure 7a. Detailed circuit schematic (TDHBG1200DC100)

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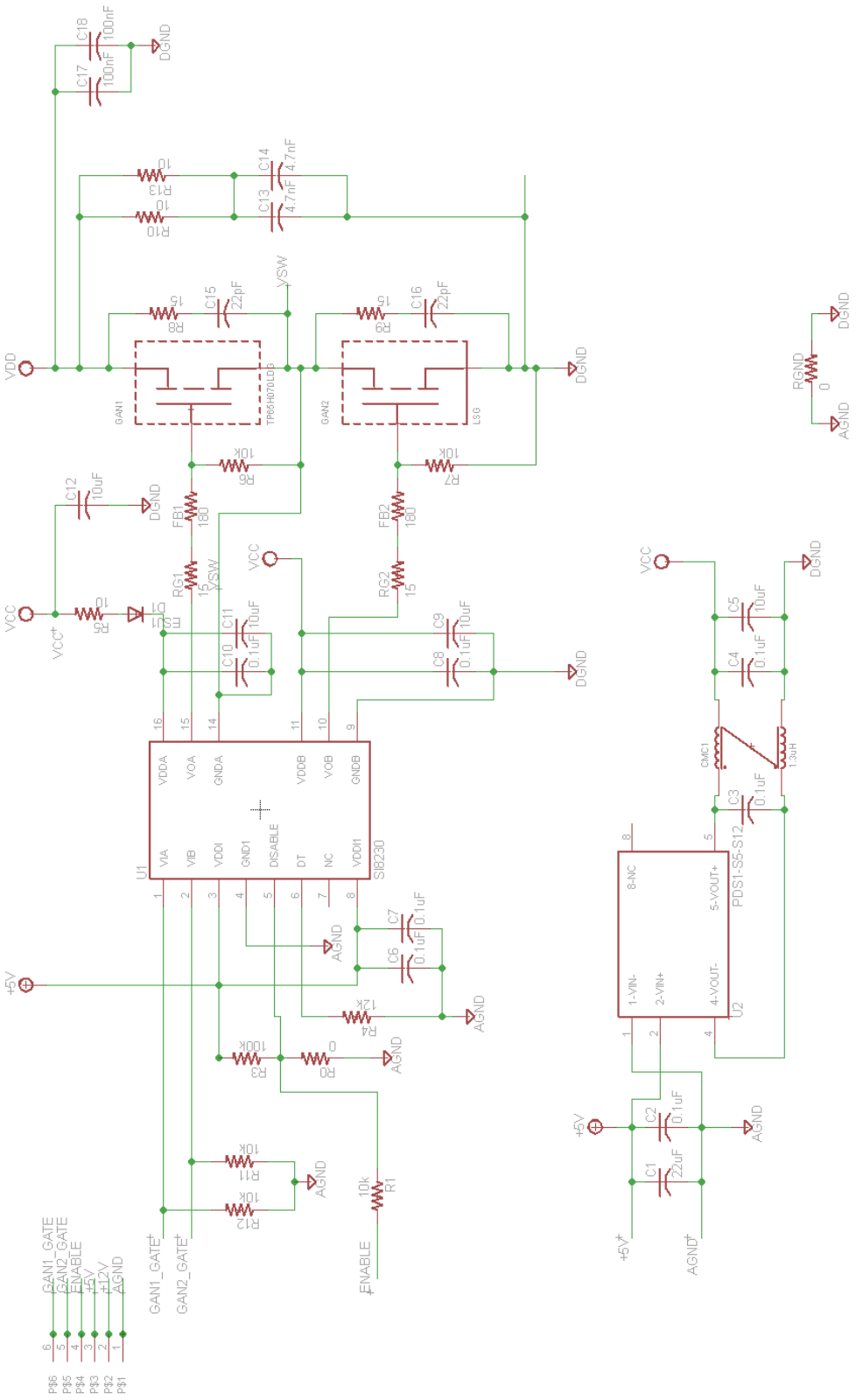

Figure 7b. Detailed circuit schematic (TDHB-65H070-DC)

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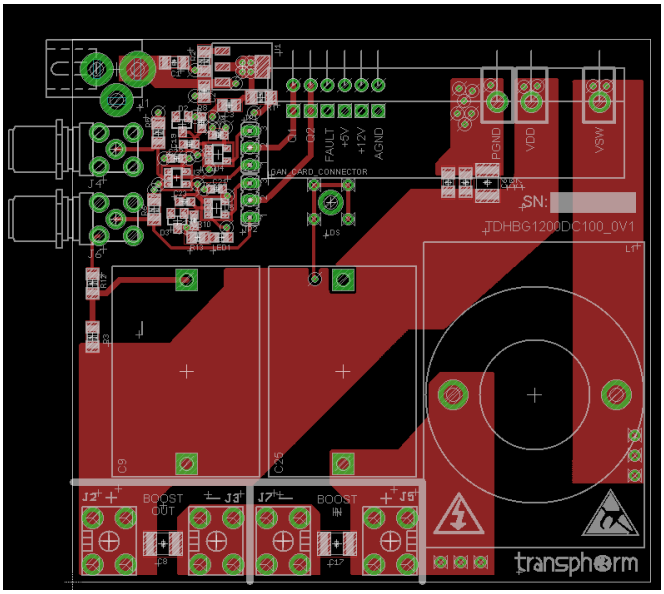
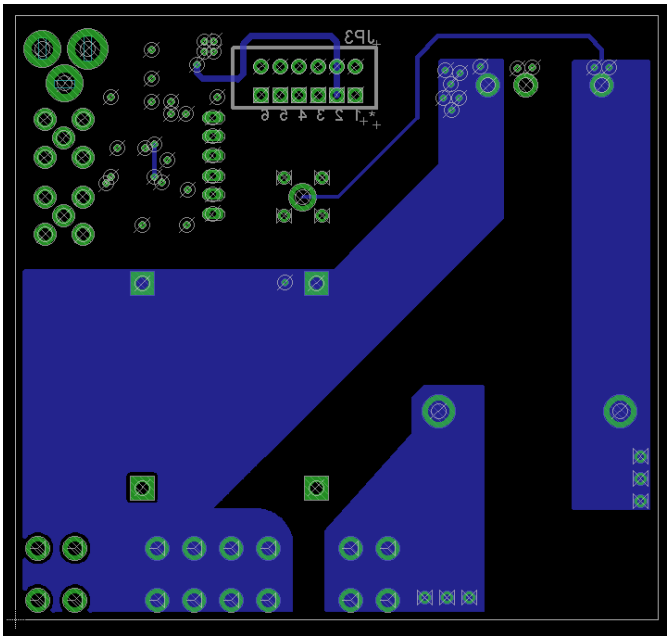


(a) TDHBG1200DC100 PCB top layer



(b) TDHBG1200DC100 PCB bottom layer

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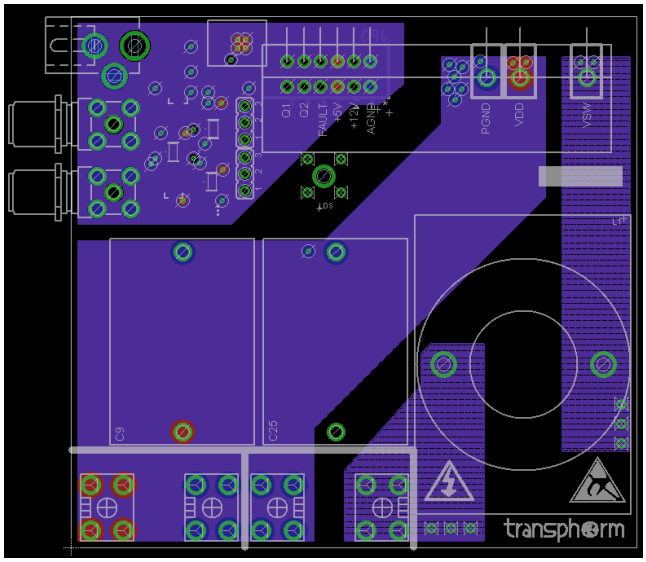
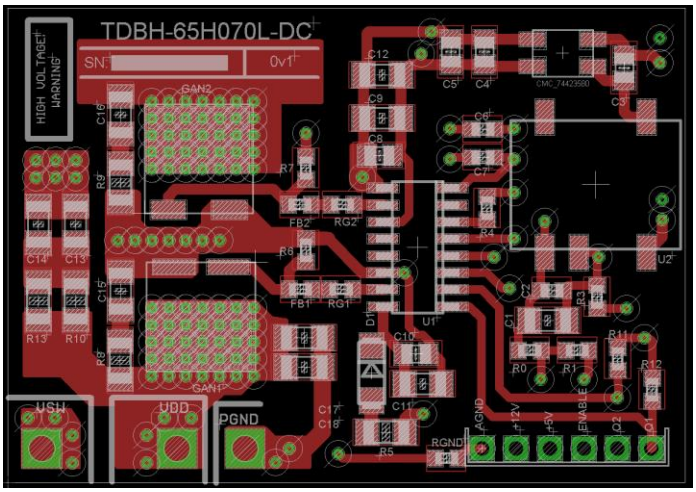


(c) TDHBG1200DC100 PCB inner layer 2 (ground plane) + inner layer 3 (power plane)

Figure 8. TDHBG1200DC100 PCB layers



(a) TDHB-65H070L-DC PCB top layer

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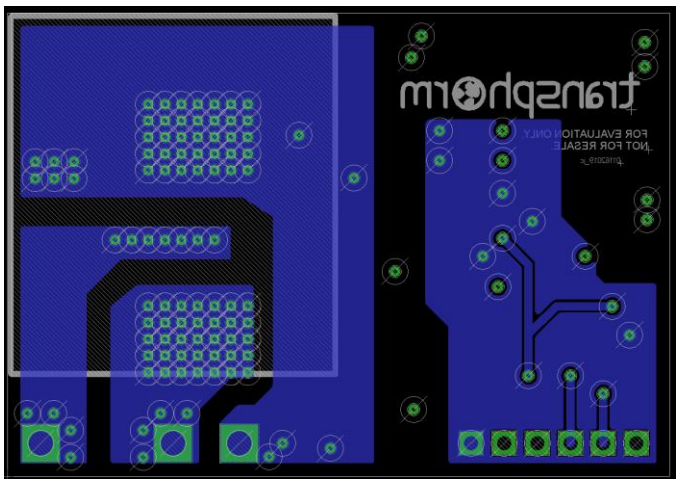
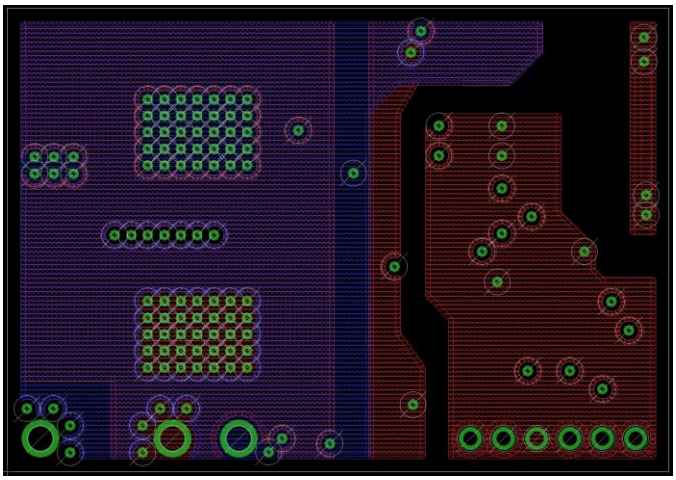


(b) TDHB-65H070L-DC PCB bottom layer



(c) TDHB-65H070L-DC PCB inner layer 2 (ground plane) + inner layer 3 (power plane)

Figure 9. TDHB-65H070L-DC PCB layers

Probing

Plated through-holes labeled test point (LDS) are provided for probing the low-side gate pulse and half-bridge switching node waveform. In order to minimize inductance during measurement, the tip and the ground of the probe should be directly attached to the sensing points to minimize the sensing loop. For safe, reliable and accurate measurement, a scope probe tip may be directly soldered to the low-side FET drain and a short ground wire soldered to the low-side FET source. See Figure 9 for an alternative that does not require soldering the probe tip.

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WARNINGS:

There is no specific protection against over-current or over-voltage on this board.

If the on-board pulse generation circuit is used in boost mode, a zero input corresponds to 100% duty cycle for the active low-side switch.

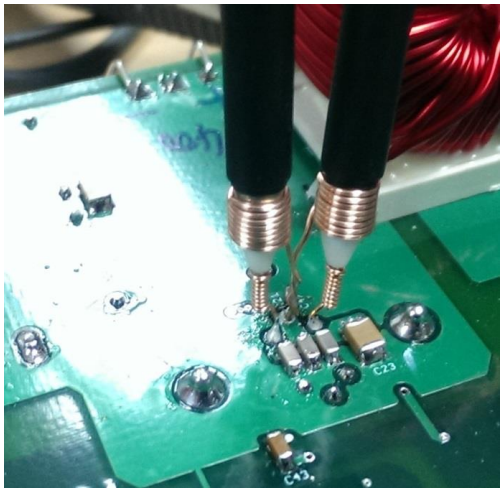

Figure 10. Low-inductance probing of fast, high-voltage signals

Efficiency has been measured for this circuit in boost mode with 200Vdc in and 400Vdc out, switching at 50kHz and 100kHz (Figure 11).

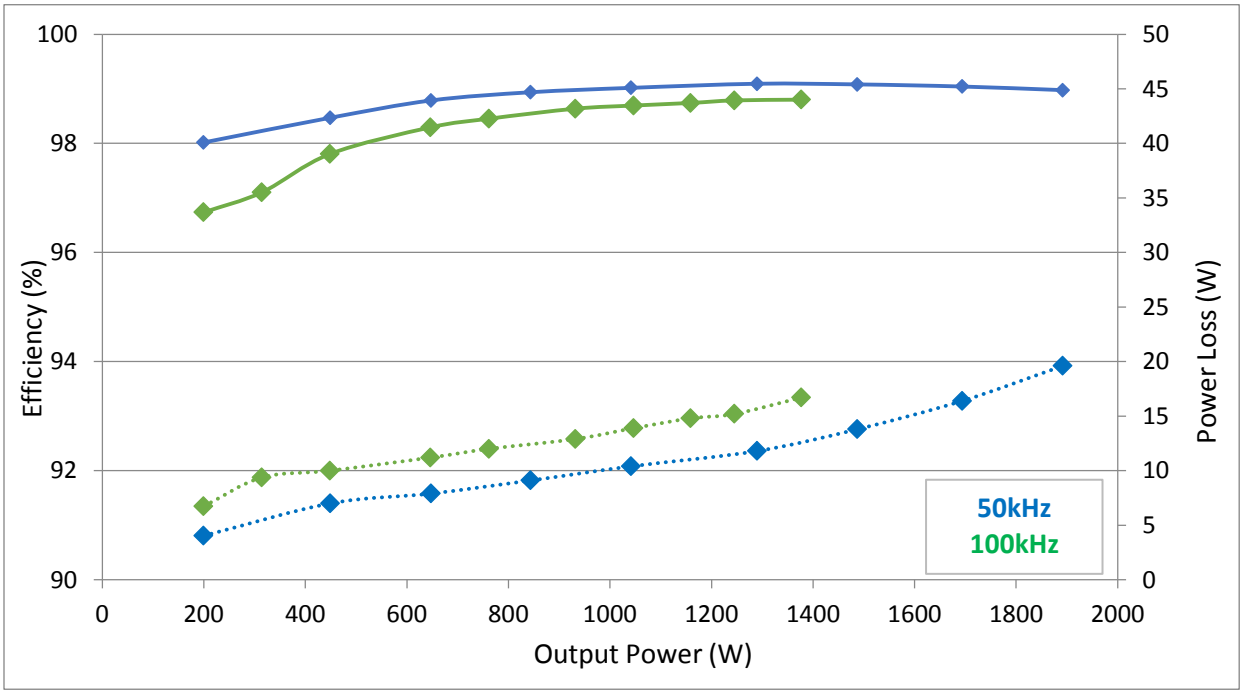

Figure 11. Efficiency for a boost 200V:400V converter

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