

RZ/G3L SMARC Module Board

Evaluation Board Manual

Renesas Microprocessor
RZ Family / RZ/G Series

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

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Precautions

This Evaluation Kit is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area, or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- Ensure attached cables do not lie across the equipment.
- Reorient the receiving antenna.
- Increase the distance between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that which the receiver is connected.
- Power down the equipment when not in use.
- Consult the dealer or an experienced radio/TV technician for help.

Note: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken:

- The user is advised that mobile phones should not be used within 10 m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Evaluation Kit does not represent an ideal reference design for an end product and does not fulfill the regulatory standards for an end product.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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1. Introduction

The RZ/G3L SMARC Module Board (hereinafter referred to as “G3L SMARC Module”) is a platform designed according to the SMARC 2.1.1 Specification providing evaluation of the Renesas RZ/G3L microcontroller R9A08G046L46BG.

Basically, the G3L SMARC Module is connected to the Renesas RZ SMARC Series Carrier Board II (hereinafter referred to as “RZ SMARC Carrier II”) and used as the RZ/G3L SMARC Evaluation Board (hereinafter referred to as “G3L SMARC EVK”).

This guide includes system setup and configuration. This guide also provides detailed information on the overall design and use of the G3L SMARC Module from a hardware system perspective.

For instructions on setting up the G3L SMARC EVK and booting Linux, refer to each Linux solution described in the **RZ/G3L Evaluation Board Kit Quick Start Guide**.

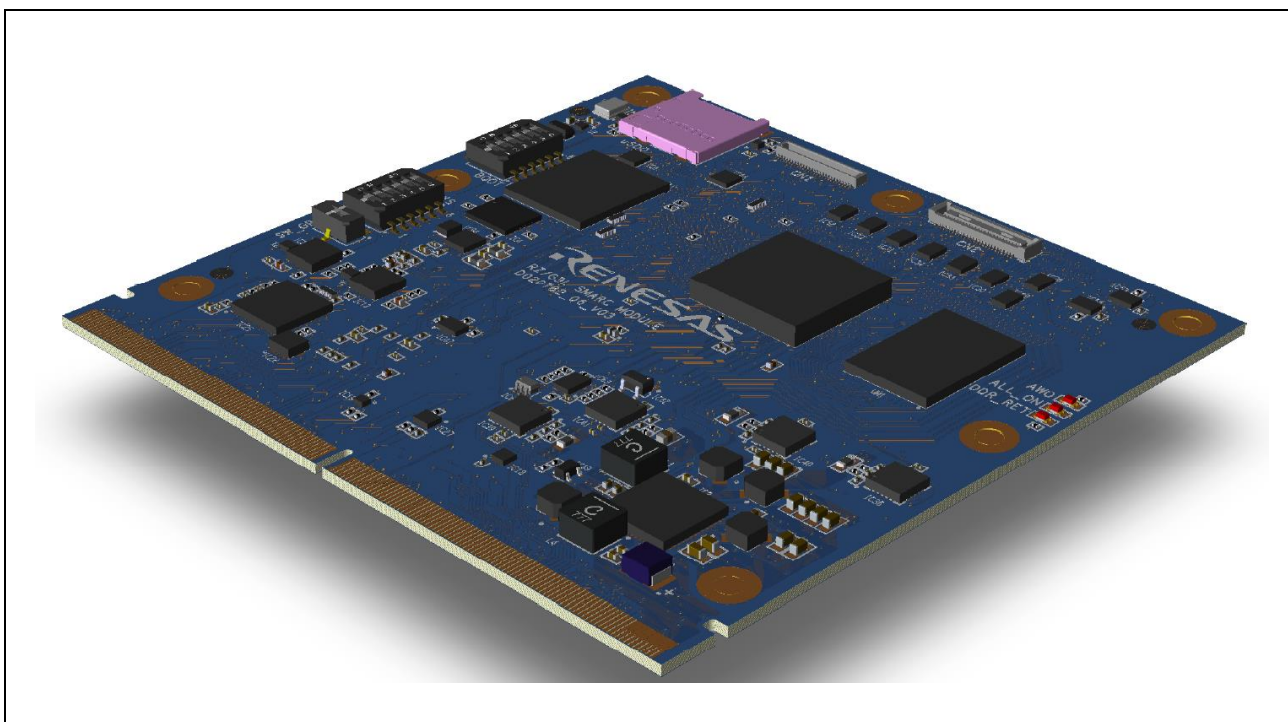


Figure 1.1 RZ/G3L SMARC Module Board

The key features of the G3L SMARC Module are as follows.

Board Features	Details
Processor	RZ/G3L (P/N: R9A09G046L46GBG), 14 mm × 14 mm, 0.5-mm pitch, 400-pin LFBGA
Memory	2 GB of 1Gx16 LPDDR4 SDRAM supporting data rate up to 2133 MT/s
	Micro SD card slot with default, high-speed, UHS-I/SDR50, SDR104, and DDR50 transfer modes support x2
	64-GB eMMC flash with HS400 transfer mode support
	128-Mbit Quad SPI flash memory
Supported interface and peripherals	Supports JTAG connection from a debugger
	Supports ADC connection for 8 channels
	I3C interface
	4x ISL28025FRZ for current monitoring
	2x Gigabit Ethernet Transceiver
	Parallel Output interface
	LVDS/MIPI DSI interface
	MEMS microphone for PDM interface
	9-channel PMIC (P/N: RAA215300A2GNP#HAA)
	6-channel clock generator (P/N: 5L35023B-617NLGI)
	6-channel clock generator (P/N: 5P35023B-789NLGI)
Board dimensions	82 mm (W) * 80 mm (L) * 1.2 mm (H), 10-layer

The G3L SMARC Module may be used in any carrier board which follows the SMARC 2.1.1 Specification; however, Renesas recommends using the Renesas RZ SMARC Carrier II board.

The details of the RZ SMARC Carrier II board are to be found in the [RZ SMARC Series Carrier Board II Evaluation Board Manual](#).

1.1 Kit Contents

If you have purchased the RZ/G3L SMARC Evaluation Board Kit (P/N: RTK9846L46S01000BE), your contents will include:

- RZ/G3L SMARC Module Board*¹
- RZ SMARC Series Breakout Adaptor Board (hereinafter referred to as “SMARC Breakout Adaptor”)
- RZ SMARC Series Parallel to HDMI Adaptor Board (hereinafter referred to as “SMARC RGB-HDMI Adaptor”)
- RZ SMARC Series Carrier Board II
- Fitted with the RZ SMARC Series MIPI DSI to HDMI Adaptor Board connected to DISP0 (hereinafter referred to as “SMARC DSI-HDMI Adaptor”)
- RZ SMARC Series Dual LVDS to HDMI Adaptor Board connected to DISP0 and DISP1 (hereinafter referred to as “SMARC Dual LVDS-HDMI Adaptor”)*²
- RZ SMARC Series Pi Camera Adaptor Board (hereinafter referred to as “SMARC Pi Camera Adaptor”)
- USB Type-A to USB Micro B cable for serial debug
- Accessories bag:
 - 2off M2.5 × 6 mm pan-head machine screws (for securing M.2 cards)
 - 1off 2.5 mm spacer (for securing M.2 key B cards)

NOTE

1. The G3L SMARC EVK is shipped with a Linux image pre-installed on the eMMC. This image is intended to allow users to quickly verify Linux boot operation and is not intended for software evaluation or development.

For software evaluation and development, including graphics features, refer to the **RZ/G3L Evaluation Board Kit Quick Start Guide** and use the latest Linux solutions described therein.

2. The SMARC Dual LVDS-HDMI Adaptor can operate as a single LVDS interface when used with the G3L SMARC EVK.

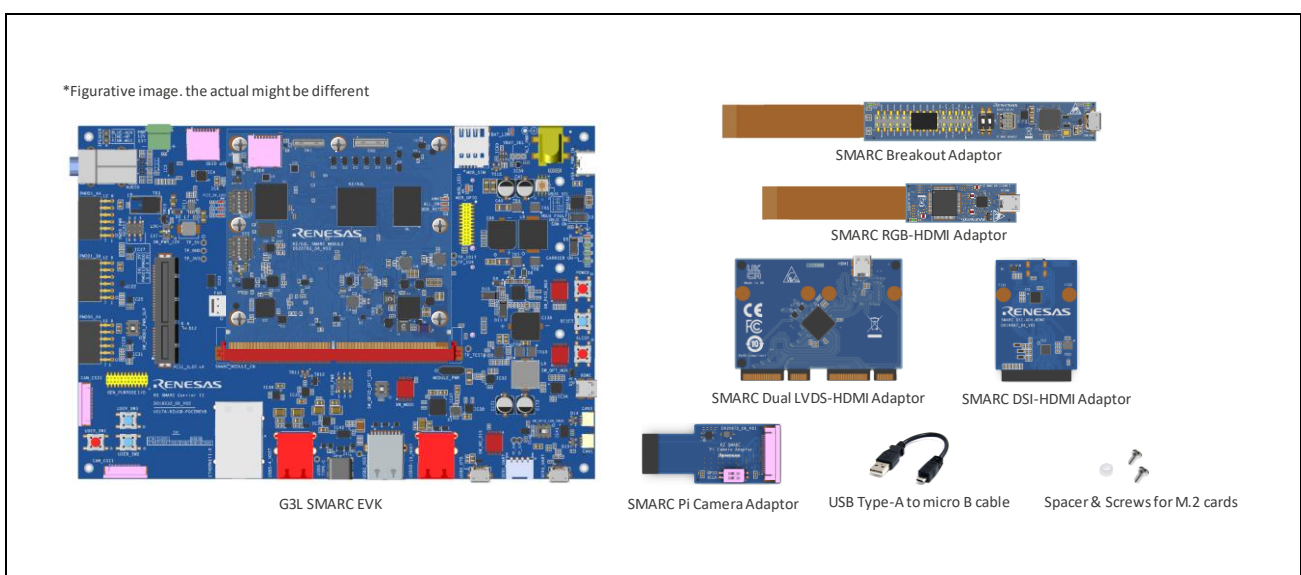


Figure 1.2 RZ/G3L SMARC Evaluation Board Kit Contents

1.2 Module Assembly

The G3L SMARC Module can only be used when fitted to a SMARC compliant Carrier board.

Secure the Module using 7 off M2.5 × 4 mm pan-head machine screws (these are provided with the RZ SMARC Carrier II).

If connections to the JTAG, ADC and I3C interfaces and current monitor functionality are required, it may be necessary to connect the SMARC Breakout Adaptor. Refer to **sections 3.13, ADC, 3.14, I3C, 3.15, JTAG, and 3.16, Current Monitor**.

If connection to the Parallel Output interface is required, it may be necessary to connect the SMARC RGB-HDMI Adaptor. Refer to **section 3.17, Parallel Output**.

1.3 Ordering Information

- G3L SMARC EVK orderable part number:

RTK9846L46S01000BE

RTK9846L46S01000BE is equipped with the R9A08G046L46GBG microprocessor, which supports security features.

Table 1.1 Design Revisions of the G3L SMARC EVK

Device Part Number	S.LOT# on the Outer Box Label	Description
#AC0	0000308367 – 0000309059	Initial release
#BC0		Products with #AC0 or #BC0 in the part number, mounted on the PCBs in this production lot, have limitations in the MIPI DSI feature. For details, contact a Renesas Electronics sales representative. Refer to section 3.20.1 for details.

2. System Description

Figure 2.1 and **Figure 2.2** show photos of the G3L SMARC Module and the positions of various blocks on the board.

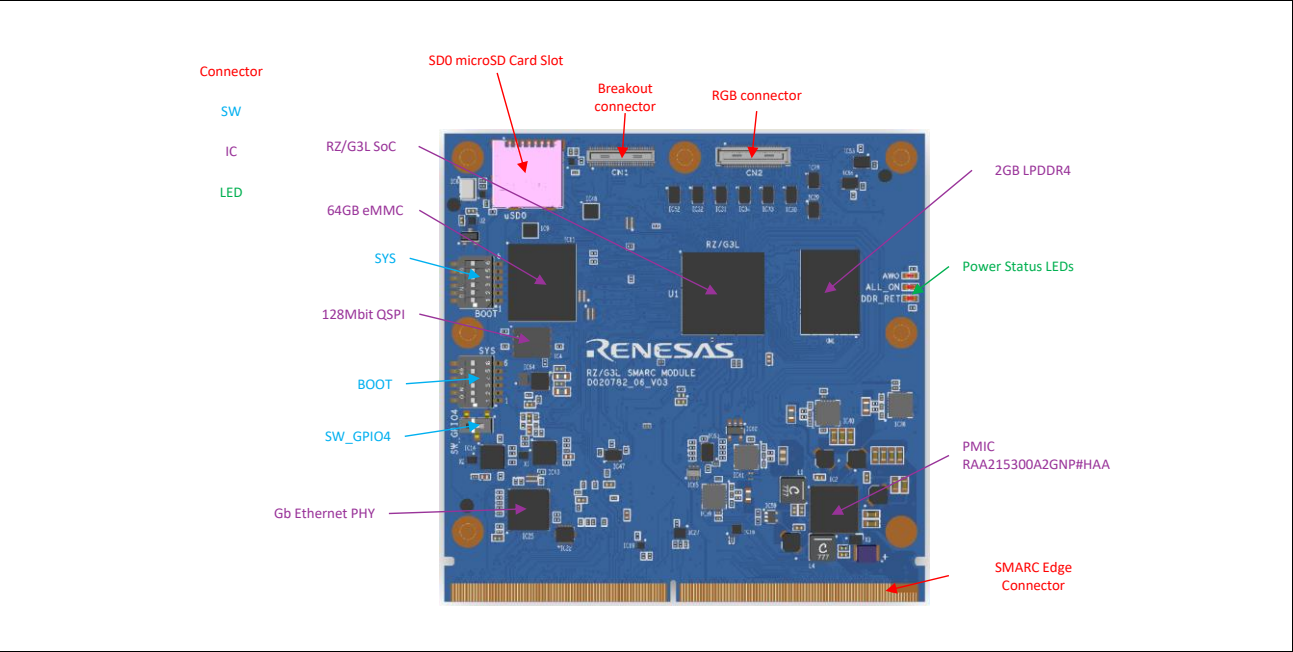


Figure 2.1 RZ/G3L SMARC Module Board Top View

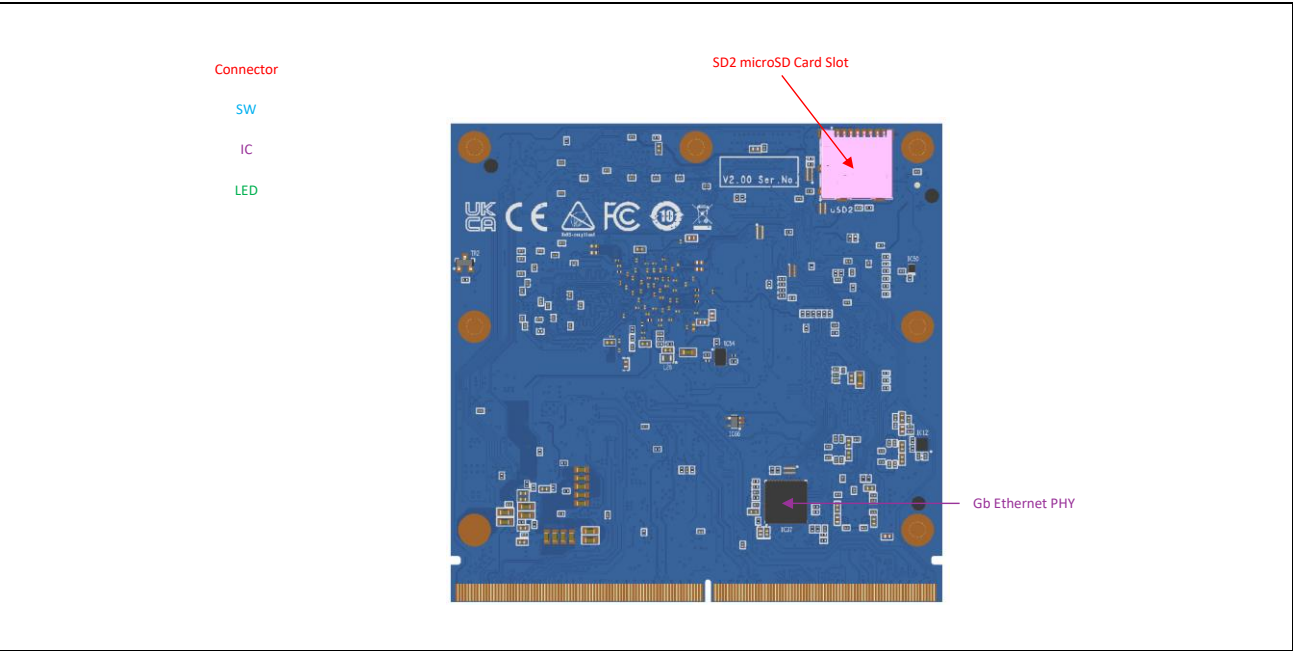


Figure 2.2 RZ/G3L SMARC Module Board Bottom View

The G3L SMARC Module has several switched configuration options and on-board interfaces. These are detailed in the following sections.

The default settings are highlighted.

2.1 G3L SMARC EVK Functional Block

Figure 2.3 shows the functional block diagram of the G3L SMARC EVK. ICs, connectors and switches surrounded by red frame indicate functions used on the G3L SMARC Module.

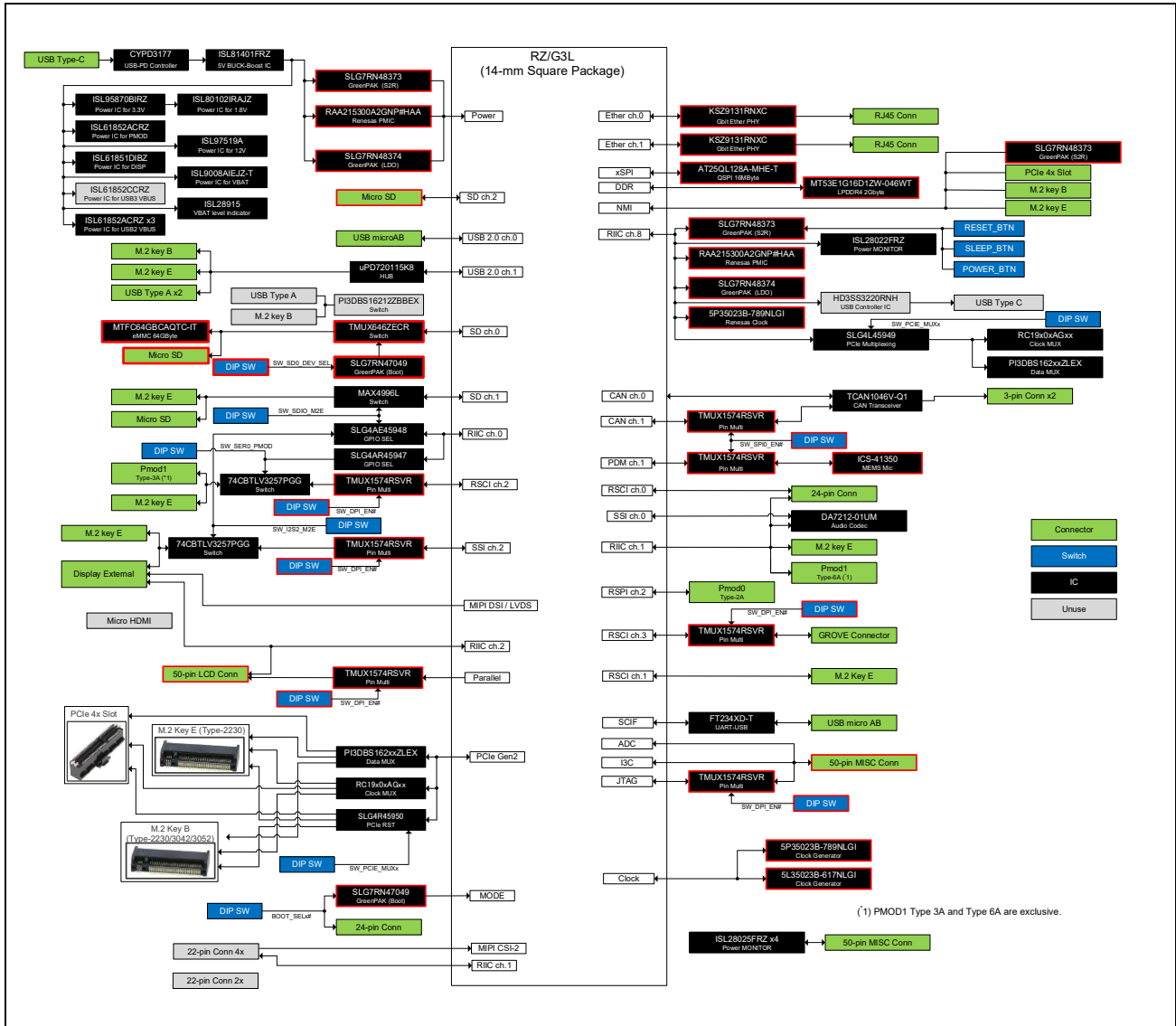


Figure 2.3 G3L SMARC EVK Block Diagram

2.2 G3L SMARC EVK Interface Mapping

Table 2.1 lists the device part numbers used on the G3L SMARC EVK, including ICs mounted on both the G3L SMARC Module and the RZ SMARC Carrier II. Renesas parts are **highlighted**.

The SMARC Interface Name column indicates the interface name on the RZ SMARC Carrier II, and the RZ/G3L I/F column indicates the corresponding interface on the RZ/G3L. For some interfaces, “—” is shown in the SMARC Interface Name column, indicating that the corresponding RZ port pins are not connected to the RZ SMARC Carrier II via the SMARC edge connector and that the interface is implemented entirely within the G3L SMARC Module. On the other hand, for some interfaces, “—” is shown in the RZ/G3L I/F column, indicating that the interface is implemented on the RZ SMARC Carrier II but is not connected to the RZ/G3L on the G3L SMARC Module. Such interfaces are therefore not available on the G3L SMARC EVK.

The rightmost two columns (G3L SMARC Module and RZ SMARC Carrier II) indicate the mounting location of each component. A check mark (✓) indicates that the component is mounted on the corresponding board, while “—” indicates that it is not mounted. Some components are mounted on an adaptor board; in such cases, “—” is indicated in both columns. Refer to the notes in **Table 2.1** for details.

Table 2.1 Interface Mapping (1/3)

SMARC Interface Name	RZ/G3L I/F	Device Part Number	Description	G3L SMARC Module	RZ SMARC Carrier II
USB0	USB2.0 ch0	629105150921	USB2.0 Type-microAB receptacle	—	✓
		SLG4E46290	GreenPAK (USB Logic)	✓	—
USB1	USB2.0 ch1	uPD720115K8-711-BAK-A	USB2.0 Hub IC	—	✓
		72309-8014BLF	USB2.0 Type-A receptacle	—	✓
		SLG4E46290	GreenPAK (USB Logic)	✓	—
USB2	—	692122030100	USB3.0 Type-A receptacle	—	✓
USB3	—	1054500101	USB3.0 Type-C receptacle	—	✓
USB4	—	72309-8014BLF	USB2.0 Type-A receptacle	—	✓
USB5	—	72309-8014BLF	USB2.0 Type-A receptacle	—	✓
CAN0	CAN ch0	TCAN1046VDMTRQ1	CAN transceiver	—	✓
		SM03B-SRSS-TB(LF)(SN)	3-pin connector	—	✓
CAN1	CAN ch1	TCAN1046VDMTRQ1	CAN transceiver	—	✓
		SM03B-SRSS-TB(LF)(SN)	3-pin connector	—	✓
I2S0	SSI ch0	DA7212-01UM	Audio Codec	—	✓
		STX-4335-5BGP-S1	Stereo Headphone, Stereo Mic, Aux for connector	—	✓
		M20-9990246	Pin header for speaker	—	✓
I2S2	SSI ch2	MDT420B01001	M.2 Key E for I2S interface	—	✓
SPI0	RSCI ch0	GRPB122VWQS-RC	24-pin header	—	✓
SPI1	RSPI ch2	SSW-106-02-T-D-RA	PMOD Type-2A connector	—	✓
SER0	RSCI ch2	SSW-106-02-T-D-RA	PMOD Type-3A connector	—	✓
SER1	RSCI ch3	110990037	Grove connector	—	✓
SER2	RSCI ch1	MDT420E01001	M.2 Key E	—	✓
SER3	SCIF ch0	FT234XD-T	USB to UART conversion IC	—	✓
		629105150921	UART Debug for USB2.0 Type-microAB receptacle	—	✓

Table 2.1 Interface Mapping (2/3)

SMARC Interface Name	RZ/G3L I/F	Device Part Number	Description	G3L SMARC Module	RZ SMARC Carrier II
PCIE_A	PCIe Gen2	10061913-111PLF	PCIe 4x Slot	—	√
		MDT420B01001	M.2 Key B	—	√
		MDT420E01001	M.2 Key E	—	√
		78646-3001	SIM card for M.2 Key B	—	√
		SLG4R45950	GreenPAK (PCIe Slot Reset, M.2 Key E Reset, M.2 Key B Reset)	—	√
—	Parallel	DF40C-50DS-0.4V	LCD connector	√	—
		ADV7513BSWZ	Parallel to HDMI conversion IC(*1)	—	—
		46765-1301	Micro HDMI connector(*1)	—	—
SATA	—	GRPB122VWQS-RC	GPIO pin header	—	√
HDMI	—	46765-1301	Micro HDMI connector	—	√
DSI0	MIPI DSI	2041262-1	Mini PCI Express & mSATA connector	—	√
		ADV7535BCBZ-RL	MIPI DSI to HDMI conversion IC(*2)	—	—
		46765-1301	Micro HDMI connector(*2)	—	—
LVDS0	LVDS ch0	2041262-1	Mini PCI Express & mSATA connector	—	√
		IT6263	Dual LVDS to HDMI conversion IC(*3)	—	—
		46765-1301	Micro HDMI connector(*3)	—	—
LVDS1	—	2041262-1	Mini PCI Express & mSATA connector	—	√
CSI0	—	2-1734592-2	22-pin FPC connector	—	√
CSI1	MIPI CSI-2	2-1734592-2	22-pin FPC connector(*4)	—	√
GBE0	Ether ch0	KSZ9131RNXC	Ethernet PHY	√	—
		2301997-7	Stacked RJ45 connector	—	√
GBE1	Ether ch1	KSZ9131RNXC	Ethernet PHY	√	—
		2301997-7	Stacked RJ45 connector	—	√
I2C_GP	RIIC ch3	GRPB122VWQS-RC	GPIO pin header	—	√
		MDT420E01001	M.2 Key E for I2C interface	—	√
		DA7212-01UM	Audio Codec for I2C interface	—	√
		SSW-106-02-T-D-RA	PMOD Type-6A connector	—	√
I2C_PM	RIIC ch0	ISL28022FRZ	Current monitor for measuring SMARC module	—	√
		SLG4L45949	GreenPAK (PCIe Data Multiplexing Control, PCIe Slot Enable, M.2 Key E Enable, M.2 Key B Enable)	—	√
		SLG4AE45947	GreenPAK (GPIO and SER0 Multiplexing Control, M.2 Key B Reset/Power off, M.2 Key E Disable)	—	√
		SLG4AE45948	GreenPAK (M.2 Key B Configuration Decoding, USB2, I2S2 and SDIO Multiplexing Control, USB1 Hub Enable)	—	√
		RAA215300A2GNP#HAA	PMIC	√	—
		SLG7RN48374	GreenPAK (Power Regulator)	√	—
		SLG7RN48373	GreenPAK (Power/Reset control)	√	—
		5P35023B-789NLGI	Clock generator	√	—
I2C_LCD	RIIC ch2	2041262-1	Mini PCI Express & mSATA connector	—	√
		ADV7535BCBZ-RL	MIPI DSI to HDMI conversion IC(*2)	—	—
		IT6263	Dual LVDS to HDMI conversion IC(*3)	—	—
		DF40C-50DS-0.4V	LCD connector	—	√

Table 2.1 Interface Mapping (3/3)

SMARC Interface Name	RZ/G3L I/F	Device Part Number	Description	G3L SMARC Module	RZ SMARC Carrier II
I2C_CAM0	—	2-1734592-2	22-pin FPC connector	—	√
I2C_CAM1	RIIC ch1	2-1734592-2	22-pin FPC connector ^(*4)	—	√
—	SD/MMC ch0	1040310811	microSD card slot	√	—
		MTFC64GBCAQTC-IT	64-GB eMMC memory	√	—
SDIO	SD/MMC ch1	1040310811	microSD card slot	—	√
—	SD/MMC ch2	1040310811	microSD card slot	√	—
—	DDR	MT53E1G16D1ZW-046 WT	2-GB LPDDR4 SDRAM	√	—
—	xSPI	AT25QL128A-MHE	128-Mbit Quad SPI Flash memory	√	—
—	PDM ch1	ICS-41350	MEMS microphone	√	—
—	ADC	DF40C-50DP-0.4V	MISC connector	√	—
		TSM-115-01-L-DV-P-TR	30-pin connector ^(*5)	—	—
—	I3C	DF40C-50DP-0.4V	MISC connector	√	—
		TSM-115-01-L-DV-P-TR	30-pin connector ^(*5)	—	—
—	JTAG	DF40C-50DP-0.4V	MISC connector	√	—
		FTSH-105-01-L-DV-007-K	10-pin connector ^(*5)	—	—
—	CPG	5L35023B-617NLGI	Clock generator	√	—
		5P35023B-789NLGI	Clock generator	√	—
—	(For current monitoring)	ISL28025FRZ	Current monitor for measuring five power rails on the SMARC module	√	—
		DF40C-50DP-0.4V	MISC connector	√	—
		FT232HQ-REEL	USB to I2C conversion IC ^(*5)	—	—
		629105150921	USB2.0 Type-microAB receptacle ^(*5)	—	—
Boot	System	SLG7RN47049	GreenPAK (Boot mode and device selection)	√	—

Note 1. The SMARC RGB-HDMI Adaptor is required. It is bundled with the G3L SMARC EVK.

Note 2. The SMARC DSI-HDMI Adaptor is required. It is fitted with the G3L SMARC EVK.

Note 3. The SMARC Dual LVDS-HDMI Adaptor is required. It is bundled with the G3L SMARC EVK.

Note 4. The SMARC Pi Camera Adaptor is required. It is bundled with the G3L SMARC EVK.

Note 5. The SMARC Breakout Adaptor is required. It is bundled with the G3L SMARC EVK.

2.3 Interface Use Combination List

Table 2.2 shows the usage permission/denial list for each RZ/G3L SMARC EVK interface. A ✓ indicates that simultaneous use by both interfaces is possible, while a × indicates that simultaneous use is not possible.

The light green cell indicates an interface of the RZ/G3L SMARC Module, the grey cell indicates an interface of the RZ SMARC Carrier II, and the light blue cell indicates an interface spanning both boards.

Table 2.2 RZ/G3L SMARC EVK Interface Usage Permission List

Interface	LPDDR4 SDRAM	QSPI Flash Memory	eMMC Memory	microSD0 Card	microSD2 Card	ADC	I3C	JTAG	Parallel Output (Display)	MEMS Microphone	MIPI DSI/LVDS (Display)	MIPI CSI-2 (Camera)	microSD1 Card	Pin header (RSCI)	PMOD0 (RSPi)	Audio Codec	M.2 Key E (SSI)	RIIC ch0 (Power)	RIIC ch1 (Camera)	RIIC ch2 (Display)	RIIC ch3 (General)	PMOD1 (RSCI)	Grove (Spare UART)	M.2 Key E (RSCI)	UART	CANFD ch0	CANFD ch1	USB2.0 ch0 OTG	USB2.0 ch1 Host	PCIe Slot, M.2 Key E/Key B	GPIO0-3 (Camera)	GPIO4-7 (PMOD0)	GPIO8-9 (CANFD, PMOD1)	GPIO10-13 (PMOD1)
LPDDR4 SDRAM		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
QSPI Flash Memory	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
eMMC Memory	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
microSD0 Card	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
microSD2 Card	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
ADC	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
I3C	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
JTAG	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Parallel Output (Display)	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MEMS Microphone	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MIPI DSI/LVDS (Display)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MIPI CSI-2 (Camera)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
microSD1 Card	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Pin header (RSCI)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PMOD0 (RSPi)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Audio Codec	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
M.2 Key E (SSI)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
RIIC ch0 (Power)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
RIIC ch1 (Camera)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
RIIC ch2 (Display)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
RIIC ch3 (General)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PMOD1 (RSCI)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Grove (Spare UART)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
M.2 Key E (RSCI)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
UART	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓
CANFD ch0	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓
CANFD ch1	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓
USB2.0 ch0 OTG	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓
USB2.0 ch1 Host	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓
PCIe Slot, M.2 Key E/Key B	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓
GPIO0-3 (Camera)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓
GPIO4-7 (PMOD0)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓
GPIO8-9 (CANFD, PMOD1)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓
GPIO10-13 (PMOD1)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	

Note 1. When using the SD2 interface, it cannot be used simultaneously with GPIO0 and GPIO2.

Note 2. When using the JTAG interface, it cannot be used simultaneously with GPIO4, which is used for the PMOD0 interface.

Note 3. When using the Parallel Output interface as a display output instead of HDMI, it cannot be used simultaneously with the SD2 interface.

Note 4. When using the Parallel Output interface as a display output instead of HDMI, it cannot be used simultaneously with GPIO0, GPIO2, GPIO8, and GPIO9.

Note 5. When using the pin header for the RSPi interface, the power enable and reset functions of camera modules cannot be controlled for the MIPI CSI-2 interface.

2.4 Configuration and Status

This section provides details of the G3L SMARC Module switch settings.

2.4.1 BOOT

A bank of 4-switches is used to configure operating modes of the Module. The default settings are highlighted.

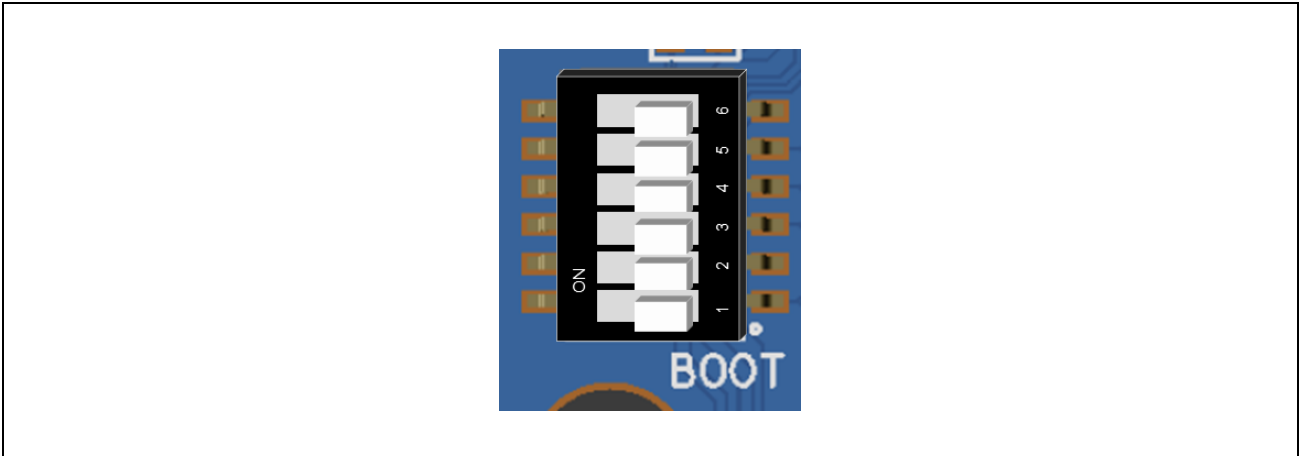


Figure 2.4 The Location and the Default Setting of BOOT

Table 2.3 DIP Switch “BOOT” Settings

BOOT[x]	Signal	ON	OFF
6	SW_SPI0_EN#	Carrier General Purpose IO (SPI0)	Module MEMS microphone (PDM1) Carrier Camera ch1 (GPIO1/3)
5	RZ_SYSCLK_SSCG_EN	SSCG is disabled	SSCG is enabled
4		—	—
3		—	—
2	RZ_BOOT_CPU_SELECT	Cold boot from Cortex-M33	Cold boot from Cortex-A55
1	RZ_BOOT_MODE3	JTAG Debug is disabled Carrier microSD card (SDIO) Carrier PMOD0 (GPIO4)	JTAG Debug is enabled

2.4.2 **SYS**

A bank of 6-switches is used to configure operating modes of the Module. The default settings are highlighted.

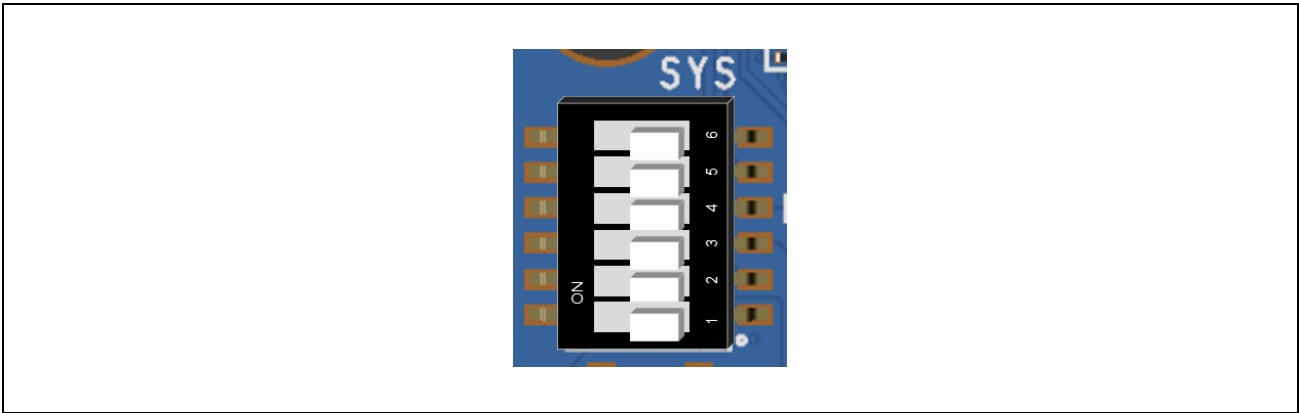


Figure 2.5 The Location and the Default Setting of SYS

Table 2.4 DIP Switch “SYS” Settings

SYS[x]	Signal	ON	OFF
6	SW_DPI_IOVS	3.3 V (VDD_OTHERS)	1.8 V (VDD_OTHERS)
5	SW_DPI_EN#	Module LCD connector	Carrier multiple SMARC interfaces*1
4	SW_SD2_EN#	Module DSI connector (GPIO)	Carrier SER2 (SCI2)
3	SW_I3C_IOVS	Carrier I2S2 (SSI0/9)	Carrier HDMI (SSI0)
2	SW_I3C_EN#	Module DSI connector (DSI)	Carrier HDMI (Converted DSI)
1	SW_SD0_DEV_SEL	SD0 connected to microSD0 card	SD0 connected to eMMC

Note 1. Refer to **section 2.3, Interface Use Combination List**, for restrictions when using the Parallel Output interface.

2.4.3 SW_GPIO4

A bank of 1-switch is used to select the VDD_I3C voltage of the Module. The default setting is highlighted.

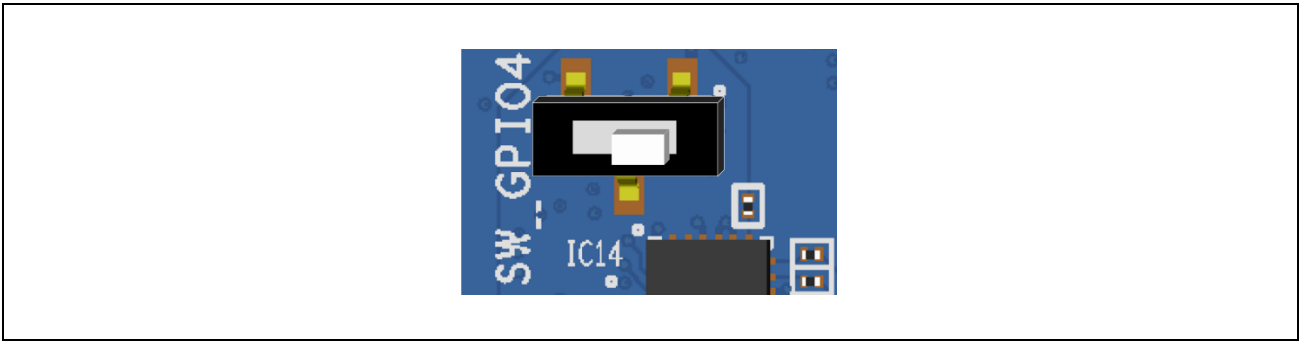


Figure 2.6 The Location and the Default Setting of SW_GPIO4

Table 2.5 DIP Switch “SW_GPIO4” Settings

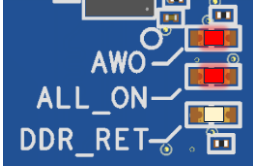
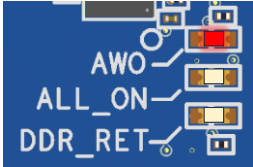
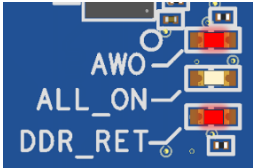
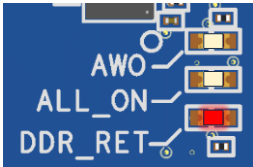
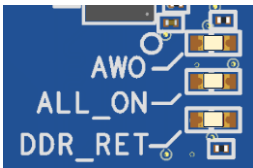
SW_GPIO4	Function
1 – 2	SMARC GPIO4 is connected to the PJ3_AWO pin Note: VBAT_TAMPER is pulled up to VDD_VBATT
2 – 3	SMARC GPIO4 is connected to the VBAT_TAMPER pin

2.5 List of Pin Functions

2.5.1 LED Indicators

The RZ/G3L has the following four power modes depending on the power on/off combination of the power domain. There are three Red LEDs on the G3L SMARC Module to provide indication of the RZ/G3L power modes.

Table 2.6 Indicator LEDs – Power Status

LED Status	Power Mode
	ALL_ON All CPUs and peripheral modules are active
	AWO Cortex-M33 and peripheral modules in the AWO domain are active
	AWO + DDR_Retention Cortex-M33 and peripheral modules in the AWO domain + DDR domain are active
	DDR_Retention Only the DDR domain is active
	ALL_OFF All CPUs and peripheral modules are disabled

2.6 Recommended Operating Condition

Table 2.7 lists operating conditions of the G3L SMARC Module.

Table 2.7 Operating Conditions of G3L SMARC Module

Symbol	Item	Rated Value	Note
VDD_IN	Power voltage*1	3.0 V to 5.25 V	Reference: SMARC 2.1.1 Specification
—	Maximum power consumption	TBD	Reference: SMARC 2.1.1 Specification
T _{opr}	Operating ambient temperature*2	0°C to 40°C	Do not expose to condensation or corrosive gases

Note 1. Supplied from the connected RZ SMARC Carrier II.

Note 2. The ambient temperature is the air temperature at a point as close to the board as possible.

3. Functional Specifications

3.1 Processor

The RZ/G3L (P/N: R9A08G046L46GBG, 14 mm × 14 mm, 0.5-mm pitch, 400-pin) includes a quad ARM Cortex-A55 core with speeds up to 1.2 GHz, and a single Arm Cortex-M33 core with speeds up to 200 MHz.

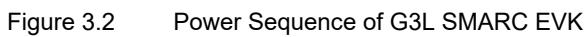
The Arm Mali-G31 as 3D graphics, selectable 1 display interface, and H.264 as video codec are supported for HMI application. Also, low power stand-by/quick wake-up, and low power processing are realized by the Cortex-M33 and RTOS stand alone with Linux. In addition, dual 1-Gbit/s Ethernet controllers, and PCI Express Gen2 drive high speed wireless/wired communications.

The RZ/G3L is useful for application such as:

- Entry-class HMI including edge computing such as industrial HMI, medical HMI, and video conference

For details on the processor, see the **RZ/G3L Group Hardware Manual**.

The G3L SoC power rails are shown in red text. The control signals for PMIC or GreenPAKs are shown in purple. The control signals for the G3L SoC are shown in light green.



3.3 Clock

The clock generators (part numbers 5L35023B-617NLGI and 5P35023B-789NLGI) provide the clock required for the G3L SoC and peripheral interfaces.

The 5L35023B and 5P35023B are Renesas VersaClock 3S programmable clock generators and support 6 unique frequency outputs.

The 5L35023B-617NLGI takes the 24 MHz crystal (part number ECS-240-10-47-CKM) as a reference input and provides one 24 MHz reference clock output for the G3L SoC, one 32.768 kHz clock output for the RTC domain of the G3L SoC, and two 100 MHz LPHSCL clock outputs for the G3L SoC and a PCI Express Card Module.

The 5P35023B-789NLGI takes the 24 MHz crystal (part number ECS-240-10-47-CKM) as a reference input and provides two 11.2896 MHz LVCMOS clock outputs for the G3L SoC and Audio Codec, one 12.2880 MHz clock output for the G3L SoC, and two 25 MHz LVCMOS clock outputs for two Ethernet PHYs.

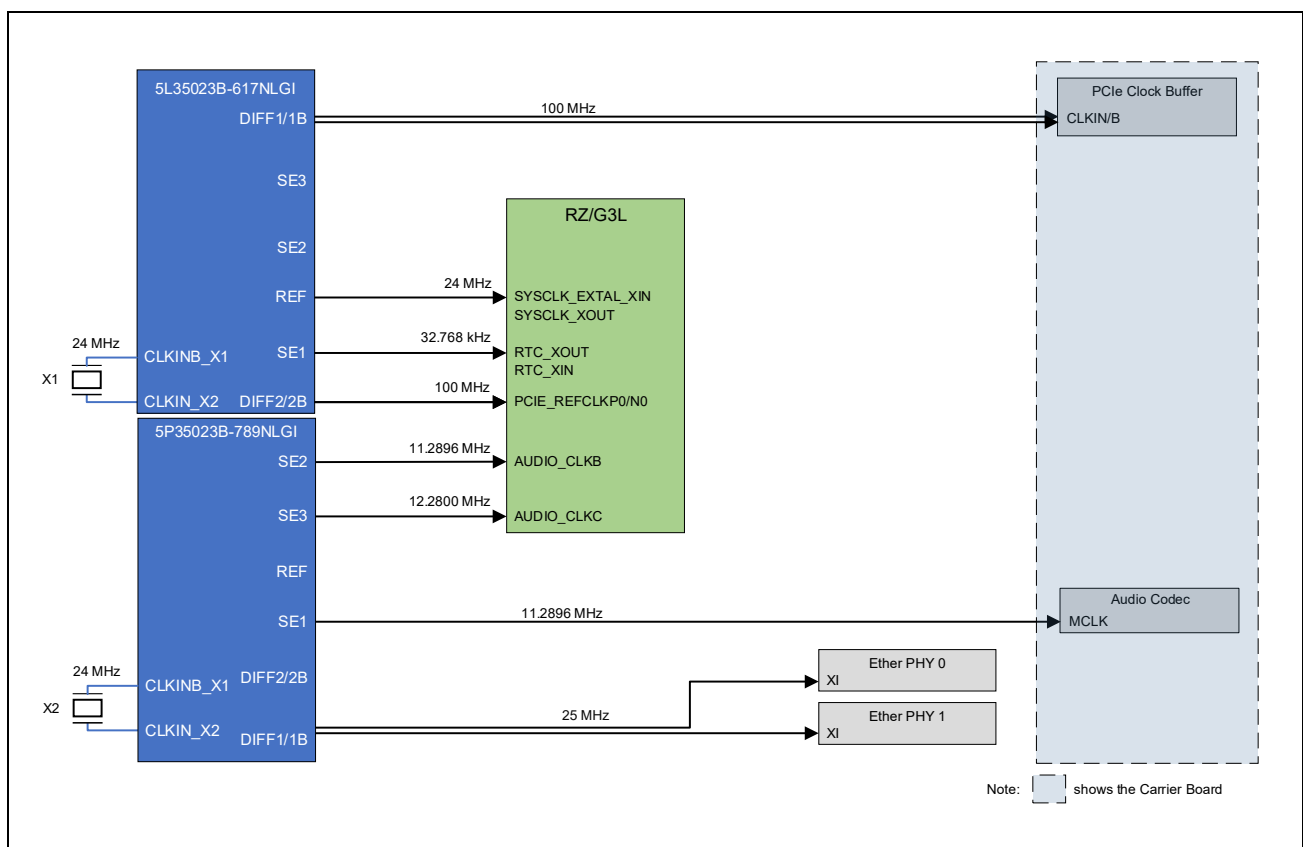


Figure 3.3 Clock Architecture of G3L SMARC EVK

Clock inputs required for peripherals such as FT232HQ, USB Hub, M.2 Key E Card Module, and HDMI Transmitter are generated locally using separate crystals or oscillators. The crystals or oscillators used to provide the reference clocks for the G3L SMARC EVK peripherals are shown in the table below.

Table 3.1 Clock Table

Peripheral	Device Part Number	Frequency
PMIC	ABS06-32.768KHZ-1-T	32.768 kHz
USB Hub* ¹	FL2400022	24.000 MHz
M.2 Key E* ¹	7XZ-32.768KBE	32.768 kHz
FT232HQ Bridge* ²	ECS-120-10-36B-CWY-TR	12.000 MHz
HDMI Transmitter* ³	SIT1602AI-23-18E-12.000000D	12.000 MHz
HDMI Transmitter* ⁴	ABM11-27.000MHZ-D2X	27.000 MHz

Note 1. RZ SMARC Carrier II

Note 2. SMARC Breakout Adaptor

Note 3. SMARC DSI-HDMI Adaptor

Note 4. SMARC Dual LVDS-HDMI Adaptor

3.4 Reset

Figure 3.4 shows a block diagram of reset control for the G3L SMARC EVK.

For the G3L SMARC EVK, the G3L SoC, Ethernet PHY, etc. on the G3L SMARC Module and some modules on the RZ SMARC Carrier II are controlled by the reset signal from the SLG7RN48373 which is programmed as [SLG46533](#).

There are two types of system resets.

- Cold reset by power-on reset
- Warm reset by the reset button switch and software

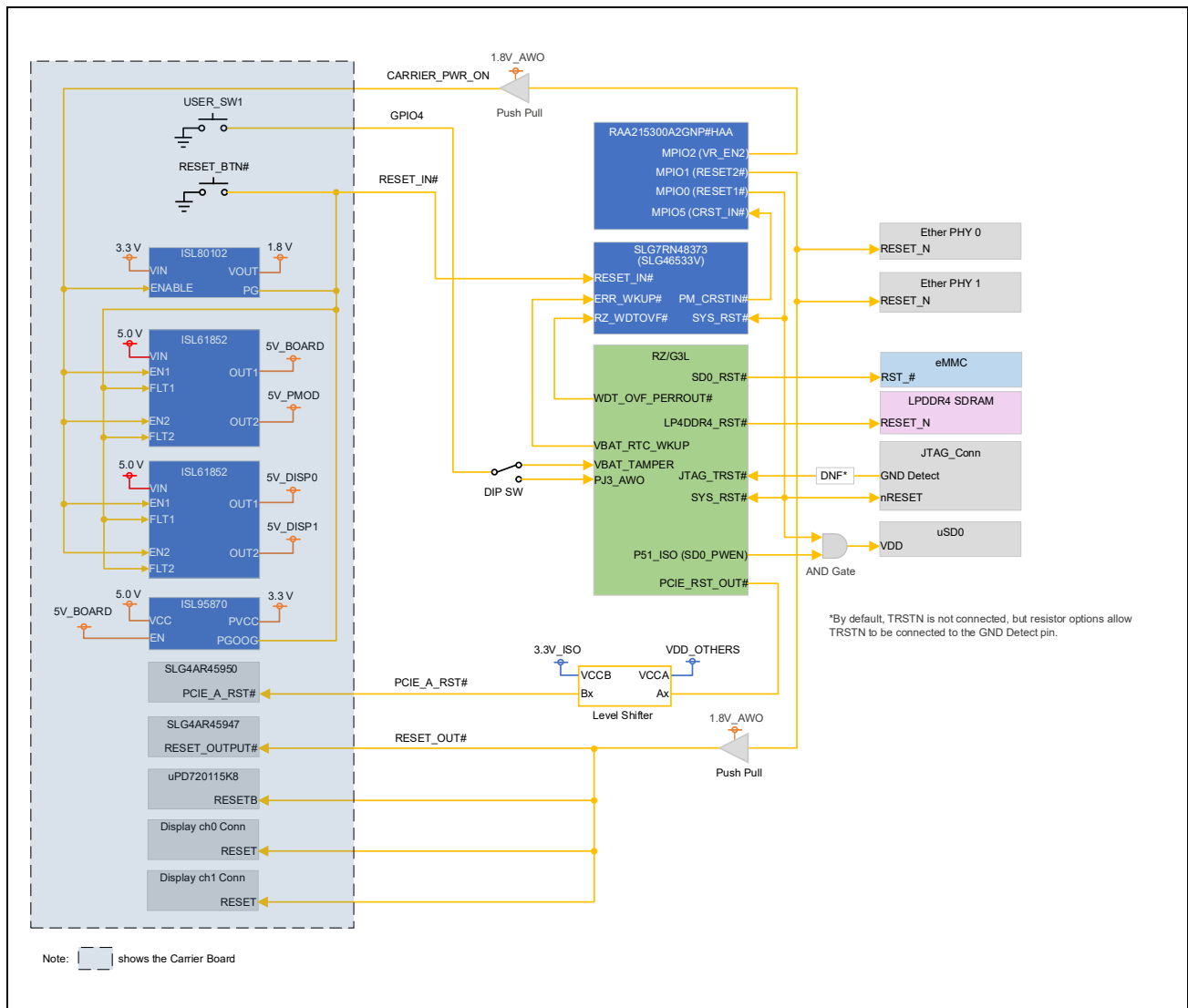


Figure 3.4 Reset Architecture of G3L SMARC EVK

3.5 LPDDR4 SDRAM

The G3L SMARC Module supports LPDDR4 SDRAM. A LPDDR4 SDRAM from Micron Technology (part number MT53E1G16D1ZW-046 WT) is provided for connection to the RZ/G3L DDR IO.

3.6 xSPI Interface

The G3L SMARC Module supports QSPI flash memory for xSPI interfaces. A QSPI flash memory from Renesas (part number AT25QL128A-MHE) is provided for connection to the RZ/G3L xSPI IO.

3.7 eMMC Memory

This eMMC is on the top side of the G3L SMARC Module. An eMMC from Micron Technology (part number MTFC64GBCAQTC-IT) is provided for connection to the RZ/G3L MMC IO. The default settings are highlighted.

The RZ/G3L MMC IO may be used either for eMMC (SYS[1] = OFF) or for the microSD0 Card interface (SYS[1] = ON).

3.8 microSD0 Card Interface

This microSD0 card interface is on the top side of the G3L SMARC Module. Cards must be inserted with the contacts facing down.

The connector is a push-pull type. The default settings are highlighted.

The RZ/G3L SD0 IO may be used either for eMMC (SYS[1] = OFF) or for the microSD0 Card interface (SYS[1] = ON).

Additional control signals of the microSD0 card using the RZG3L port pins are shown below.

Table 3.2 microSD0 Signals

microSD Card Signals	RZ Port Pin	Direction	Function
microSD0 Card Detect	P50_ISO/SD0_CD	Input	0: Card present 1: No card present
microSD0 Card Power Enable	P51_ISO	Output	0: Power disabled 1: Power enabled
microSD0 Card IO Power Select	PL4_AWO	Output	0: 3.3 V 1: 1.8 V

3.9 microSD1 Card Interface

This microSD1 card interface is on the RZ SMARC Carrier II through the SMARC Edge connector. Cards must be inserted with the contacts facing up.

The connector is a push-pull type.

The control signals for the microSD1 card, which utilize RZ/G3L port pins, are listed below. For details on the RZ/G3L SD1 IO, refer to **section 3.20.3, SDIO Card (4-bit) Interface**.

Table 3.3 microSD1 card Signals

microSD Card Signals	RZ Port Pin	Direction	Function
microSD1 Card Detect	PJ0_AWO/JTAG_TMS/SD1_CD	Input	0: Card present 1: No card present
microSD1 Card Power Enable	PJ2_AWO/JTAG_TDO/SD1_PWEN	Output	0: Power disabled 1: Power enabled
microSD1 Card IO Power Select	PJ1_AWO/JTAG_TCK/SD1_IOVS	Output	0: 3.3 V 1: 1.8 V

3.10 microSD2 Card Interface

This microSD2 card interface is on the bottom side of the G3L SMARC Module. Cards must be inserted with the contacts facing up.

The connector is a push-pull type.

The microSD2 card signals, using the RZG3L port pins, are shown below.

Table 3.4 microSD2 card Signals

microSD Card Signals	RZ Port Pin	Direction	Function
microSD2 Data0	PH2_ISO/SD2_DAT0	In/Out	microSD2 data
microSD2 Data1	PH3_ISO/SD2_DAT1	In/Out	microSD2 data
microSD2 Data2	PH4_ISO/SD2_DAT2	In/Out	microSD2 data
microSD2 Data3	PH5_ISO/SD2_DAT3	In/Out	microSD2 data
microSD2 Command	PH1_ISO/SD2_CMD	In/Out	microSD2 CMD
microSD2 Clock	PH0_ISO/SD2_CLK	Output	microSD2 clock
microSD2 Card Detect	PK0_ISO/SD2_CD	Input	0: Card present 1: No card present
microSD2 Card Power Enable	PK2_ISO/SD2_PWEN	Output	0: Power disabled 1: Power enabled
microSD2 Card IO Power Select	PK1_ISO/SD2_IOVS	Output	0: 3.3 V 1: 1.8 V

3.11 Gigabit Ethernet Interface

Two gigabit Ethernet transceivers with RGMII support are mounted on the G3L SMARC Module.

There are RJ45 connectors on the RZ SMARC Carrier II through the SMARC Edge connector. Refer to **section 3.20.12, Ethernet** for pin assignment.

3.12 I2C

There are four I2C interfaces connected to the SMARC Edge connector.

RIIC ch0 is connected to the power management “I2C_PM” interface. RIIC ch1 is connected to the MIPI CSI serial camera “I2C_CAM” interface. RIIC ch2 is connected to the LCD display “I2C_LCD” interface. RIIC ch3 is connected to the general purpose “I2C_GP” interface.

RIIC1 and RIIC3 are not connected to any devices on the G3L SMARC Module.

Table 3.5 Address Mapping for RIIC2

RIIC7 Device	7-bit Address
ADV7535BCBZ-RL (MIPI DSI to HDMI conversion)	0x72
IT6263 (Dual LVDS to HDMI conversion)	0x98

Table 3.6 Address Mapping for RIIC0

RIIC8 Device	7-bit Address
Renesas RAA215300A2GNP#HAA (PMIC)	0x12
Renesas GreenPAK SLG7RN48374 (Power Regulator)	0x28
Renesas GreenPAK SLG7RN48373 (Power/Reset control)	0x38
Renesas 5P35023B-789NLGI (clock generator)	0x68

3.13 ADC

This ADC interface is the FPC-to-Board (CN1) on the top side of the G3L SMARC Module. A 30-pin, 2.54-mm pitch FPC connector from Samtec (part number TSM-115-01-L-DV-P-TR) on the Renesas SMARC Breakout Adaptor is provided for connection to the RZ/G3L ADC IO via the MISC IO which is a 50-pin, 0.4-mm pitch, 1.5 to 4.00 mm height FPC-to-Board connector from Hirose (part number DF40C-50DP-0.4V(51)) on the G3L SMARC Module as shown in **Figure 3.5**.

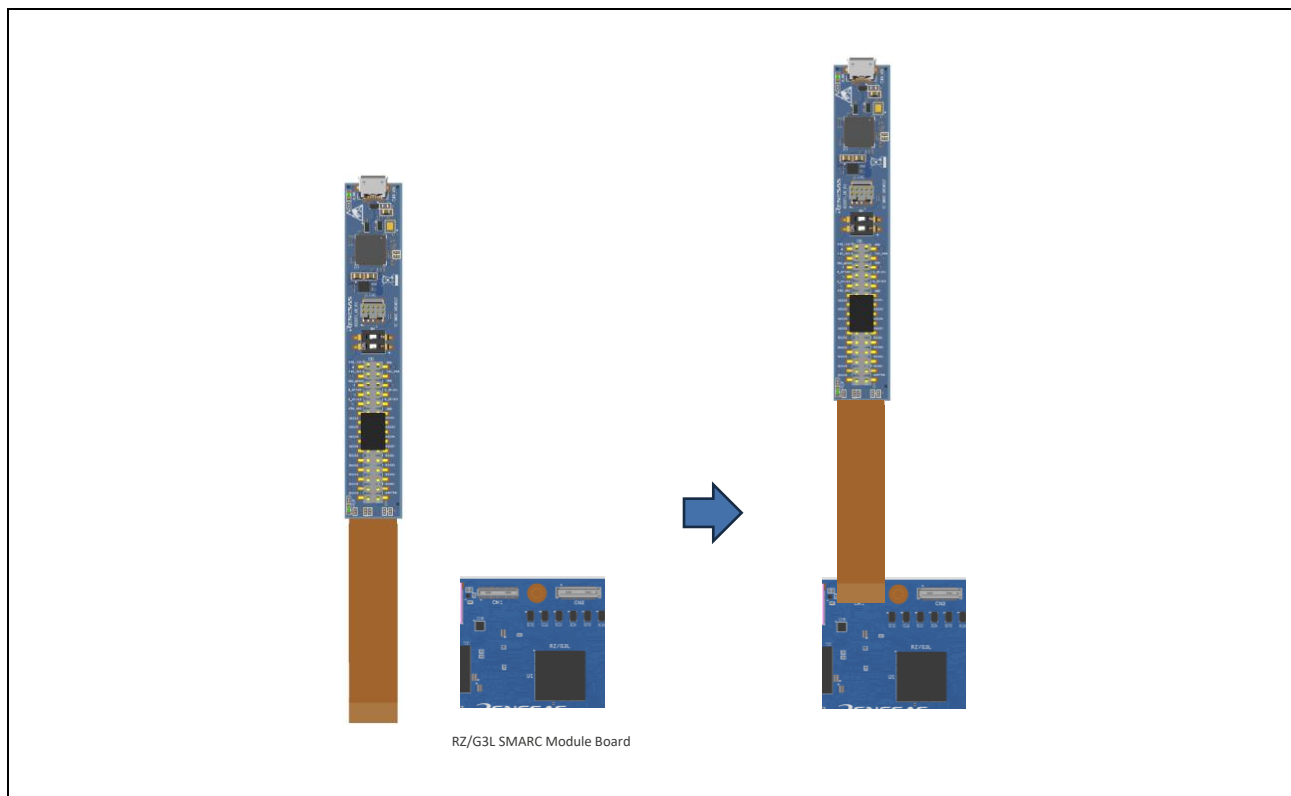


Figure 3.5 SMARC Breakout Adaptor Connection

The ADC interface voltage is 1.8 V. It has a common ground with a digital ground in terms of noise reduction.

Table 3.7 ADC Pin Assignment on the FPC-to Board Connector

Pin Number	Module Connection	Module Connection	Pin Number
1	VDD_OTHERS (3.3 V or 1.8 V)	Ground	2
3	Not connected	Not connected	4
5	Not connected	Not connected	6
7	VDD_IN (5.0 V)	Ground	8
9	VDD_IN (5.0 V)	Ground	10
11	VDD_IN (5.0 V)	Ground	12
13	VDD_IN (5.0 V)	Ground	14
15	VDD_I3C (1.8 V or 1.2 V)	Ground	16
17	P20_ISO/I3C_SCL	P21_ISO/I3C_SDA	18
19	ADC_AVDD (1.8 V)	Ground	20
21	ADC_CH0	RSVD0 (Ground)	22
23	ADC_CH1	RSVD1 (Ground)	24
25	ADC_CH2	RSVD2 (Ground)	26
27	ADC_CH3	RSVD3 (Ground)	28
29	ADC_CH4	RSVD4 (Ground)	30
31	ADC_CH5	RSVD5 (Ground)	32
33	ADC_CH6	RSVD6 (Ground)	34
35	ADC_CH7	RSVD7 (Ground)	36
37	RZ_P36_AWO/ADC_TRG	RSVD8 (Ground)	38
39	1.8V_AWO (1.8 V)	Ground	40
41	PJ4_AWO/JTAG_TRST#	PJ0_AWO/JTAG_TMS	42
43	PJ2_AWO/JTAG_TDO	PJ3_AWO/JTAG_TDI	44
45	PJ1_AWO/JTAG_TCK	SYS_RST# (JTAG_RESET_IN#)	46
47	D3.3V_C	Ground	48
49	FT232H_SCL	FT232H_SDA	50

The ADC interface is realized by using the Renesas SMARC Breakout Adaptor which is included in the kit.

3.14 I3C

This I3C interface is the FPC-to-Board (CN1) on the top side of the G3L SMARC Module. A 30-pin, 2.54-mm pitch FPC connector from Samtec (part number TSM-115-01-L-DV-P-TR) on the Renesas SMARC Breakout Adaptor is provided for connection to the RZ/G3L I3C IO via the MISC IO which is a 50-pin, 0.4-mm pitch, 1.5 to 4.00 mm height FPC-to-Board connector from Hirose (part number DF40C-50DP-0.4V(51)) on the G3L SMARC Module as shown in

Figure 3.5.

Table 3.8 I3C Pin Assignment on the FPC-to Board Connector

Pin Number	Module Connection	Module Connection	Pin Number
1	VDD_OTHERS (3.3 V or 1.8 V)	Ground	2
3	Not connected	Not connected	4
5	Not connected	Not connected	6
7	VDD_IN (5.0 V)	Ground	8
9	VDD_IN (5.0 V)	Ground	10
11	VDD_IN (5.0 V)	Ground	12
13	VDD_IN (5.0 V)	Ground	14
15	VDD_I3C (1.8 V or 1.2 V)	Ground	16
17	P20_ISO/I3C_SCL	P21_ISO/I3C_SDA	18
19	ADC_AVDD (1.8 V)	Ground	20
21	ADC_CH0	RSVD0 (Ground)	22
23	ADC_CH1	RSVD1 (Ground)	24
25	ADC_CH2	RSVD2 (Ground)	26
27	ADC_CH3	RSVD3 (Ground)	28
29	ADC_CH4	RSVD4 (Ground)	30
31	ADC_CH5	RSVD5 (Ground)	32
33	ADC_CH6	RSVD6 (Ground)	34
35	ADC_CH7	RSVD7 (Ground)	36
37	RZ_P36_AWO/ADC_TRG	RSVD8 (Ground)	38
39	1.8V_AWO (1.8 V)	Ground	40
41	PJ4_AWO/JTAG_TRST#	PJ0_AWO/JTAG_TMS	42
43	PJ2_AWO/JTAG_TDO	PJ3_AWO/JTAG_TDI	44
45	PJ1_AWO/JTAG_TCK	SYS_RST# (JTAG_RESET_IN#)	46
47	D3.3V_C	Ground	48
49	FT232H_SCL	FT232H_SDA	50

Note 1. The I3C interface voltage is either 1.8 V (when SW1 = 2-3 short) or 1.2 V (when SW1 = 1-2 short).

The I3C interface is realized by using the Renesas SMARC Breakout Adaptor which is included in the kit.

3.15 JTAG

This JTAG interface is the FPC-to-Board (CN1) on the top side of the G3L SMARC Module. A 10-pin, 1.27-mm pitch Cortex debug connector from Samtec (part number FTSH-105-01-L-DV-007-K) on the Renesas SMARC Breakout Adaptor is provided for connection to the RZ/G3L JTAG IO via the MISC IO which is a 50-pin, 0.4-mm pitch, 1.5 to 4.00 mm height FPC-to-Board connector from Hirose (part number DF40C-50DP-0.4V(51)) on the G3L SMARC Module as shown in **Figure 3.5**.

The JTAG interface voltage is 1.8 V.

Table 3.9 JTAG Pin Assignment on the FPC-to Board Connector

Pin Number	Module Connection	Module Connection	Pin Number
1	VDD_OTHERS (3.3 V or 1.8 V)	Ground	2
3	Not connected	Not connected	4
5	Not connected	Not connected	6
7	VDD_IN (5.0 V)	Ground	8
9	VDD_IN (5.0 V)	Ground	10
11	VDD_IN (5.0 V)	Ground	12
13	VDD_IN (5.0 V)	Ground	14
15	VDD_I3C (1.8 V or 1.2 V)	Ground	16
17	P20_ISO/I3C_SCL	P21_ISO/I3C_SDA	18
19	ADC_AVDD (1.8 V)	Ground	20
21	ADC_CH0	RSVD0 (Ground)	22
23	ADC_CH1	RSVD1 (Ground)	24
25	ADC_CH2	RSVD2 (Ground)	26
27	ADC_CH3	RSVD3 (Ground)	28
29	ADC_CH4	RSVD4 (Ground)	30
31	ADC_CH5	RSVD5 (Ground)	32
33	ADC_CH6	RSVD6 (Ground)	34
35	ADC_CH7	RSVD7 (Ground)	36
37	RZ_P36_AWO/ADC_TRG	RSVD8 (Ground)	38
39	1.8V_AWO (1.8 V)	Ground	40
41	PJ4_AWO/JTAG_TRST#	PJ0_AWO/JTAG_TMS	42
43	PJ2_AWO/JTAG_TDO	PJ3_AWO/JTAG_TDI	44
45	PJ1_AWO/JTAG_TCK	SYS_RST# (JTAG_RESET_IN#)	46
47	D3.3V_C	Ground	48
49	FT232H_SCL	FT232H_SDA	50

Note 1. To use the JTAG interface, RZ_DEBUGEN must be high (**BOOT[1] = OFF**). If RZ_DEBUGEN is low (BOOT[1] = ON), the TRST# pin is held low and the JTAG interface will not function.

The JTAG interface is realized by using the Renesas SMARC Breakout Adaptor which is included in the kit.

3.16 Current Monitor

A current monitoring circuitry that is accessed through the micro-USB connector on the Renesas SMARC Breakout Adaptor is provided via the MISC IO which is a 50-pin, 0.4-mm pitch, 1.5 to 4.00 mm height FPC-to-Board connector from Hirose (part number DF40C-50DP-0.4V(51)) on the G3L SMARC Module as shown in **Figure 3.5**.

The current monitoring circuitry is powered from the USB and is completely independent of all other module and RZ/G3L functions.

A software application is required to execute on a host PC and provides current measurements for

- 1.8V_AWO
- 1.0V_ISO
- 1.0V_AWO
- 1.1V_DDR

Table 3.10 I2C Address Mapping for Current Monitoring

Device	7-bit Address
Renesas ISL28025FR12Z (1.8V_AWO)	0xa0
Renesas ISL28025FR12Z (1.0V_ISO)	0x9c
Renesas ISL28025FR12Z (1.0V_AWO)	0x84
Renesas ISL28025FR12Z (1.1V_DDR)	0x86

Table 3.11 Current Monitor Pin Assignment on the FPC-to Board Connector (1/2)

Pin Number	Module Connection	Module Connection	Pin Number
1	VDD_OTHERS (3.3 V or 1.8 V)	Ground	2
3	Not connected	Not connected	4
5	Not connected	Not connected	6
7	VDD_IN (5.0 V)	Ground	8
9	VDD_IN (5.0 V)	Ground	10
11	VDD_IN (5.0 V)	Ground	12
13	VDD_IN (5.0 V)	Ground	14
15	VDD_I3C (1.8 V or 1.2 V)	Ground	16
17	P20_ISO/I3C_SCL	P21_ISO/I3C_SDA	18
19	ADC_AVDD (1.8 V)	Ground	20
21	ADC_CH0	RSVD0 (Ground)	22
23	ADC_CH1	RSVD1 (Ground)	24
25	ADC_CH2	RSVD2 (Ground)	26
27	ADC_CH3	RSVD3 (Ground)	28
29	ADC_CH4	RSVD4 (Ground)	30
31	ADC_CH5	RSVD5 (Ground)	32
33	ADC_CH6	RSVD6 (Ground)	34
35	ADC_CH7	RSVD7 (Ground)	36
37	RZ_P36_AWO/ADC_TRG	RSVD8 (Ground)	38
39	1.8V_AWO (1.8 V)	Ground	40
41	PJ4_AWO/JTAG_TRST#	PJ0_AWO/JTAG_TMS	42
43	PJ2_AWO/JTAG_TDO	PJ3_AWO/JTAG_TDI	44

Table 3.11 Current Monitor Pin Assignment on the FPC-to Board Connector (2/2)

Pin Number	Module Connection	Module Connection	Pin Number
45	PJ1_AWO/JTAG_TCK	SYS_RST# (JTAG_RESET_IN#)	46
47	D3.3V_C	Ground	48
49	FT232H_SCL	FT232H_SDA	50

The current monitor function is realized by using the Renesas SMARC Breakout Adaptor which is included in the kit.

3.16.1 Breakout Adaptor

The SMARC Breakout Adaptor is required to convert the MISC IO on the G3L SMARC Module to a 30-pin header for the ADC, I3C, and GPIO interfaces, a Cortex debug connector for the JTAG interface, and the current monitoring circuitry.

The current monitoring function can be realized by connecting to the console/terminal via micro-USB with the I2C to USB conversion IC from FTDI (part number FT232HQ).

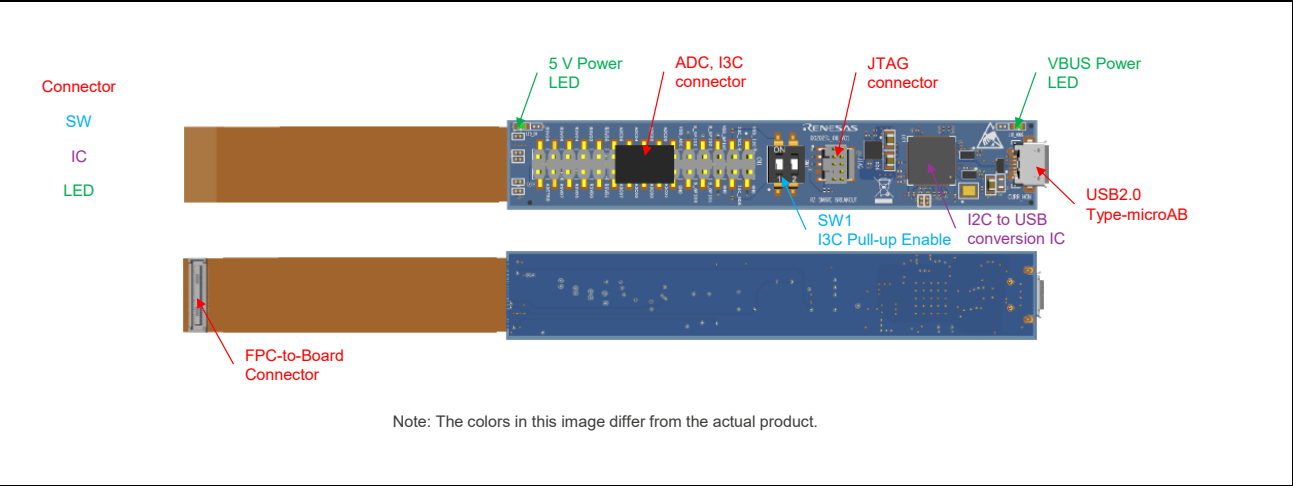


Figure 3.6 SMARC Breakout Adaptor Top and Bottom View

A bank of two switches is used to configure the pull-up functionality of the I3C interface. The default settings are highlighted.

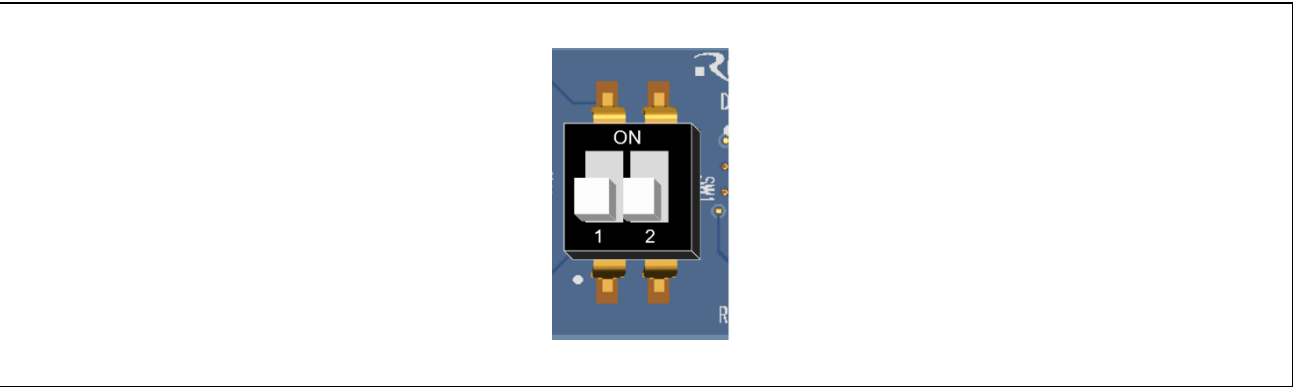


Figure 3.7 The Location and the Default Setting of SW1

Table 3.12 DIP Switch “SW1” Settings

SW1	Signal	ON	OFF
2	I3C_SDA	Pull-up is enabled	Pull-up is disabled
1	I3C_SCL	Pull-up is enabled	Pull-up is disabled

Regarding the connector mating operation of the SMARC Breakout Adaptor, insert the adaptor to the connector in vertical direction. Regarding the connector unmating operation, remove the adaptor from the connector in vertical direction. If vertical removal is difficult, lift up either side in longitudinal, contact pitch direction. Do not unmate the connector in lateral direction; otherwise, the contacts could receive great stress.

Refer to **Appendix A**, for details.

Table 3.13 ADC, I3C, and GPIO Interface Pin Assignment on the 30-pin Header

Pin Number	Module Connection	Module Connection	Pin Number
1	VDD_I3C (1.8 V or 1.2 V)	Ground	2
3	I3C_SCL	I3C_SDA	4
5	VDD_GPIO (3.3 V or 1.8 V)	Ground	6
7	B_GPIO0 (Not connected)	B_GPIO1 (Not connected)	8
9*1	B_GPIO2 (Not connected)	B_GPIO3 (Not connected)	10
11	VDD_ADC (1.8 V)	Ground	12
13	ADC00	ADC01	14
15	ADC02	ADC03	16
17	ADC04	ADC05	18
19	ADC06	ADC07	20
21	RSVD0	RSVD1	22
23	RSVD2	RSVD3	24
25	RSVD4	RSVD5	26
27	RSVD6	RSVD7	28
29	RSVD8	ADCTRG	30

Table 3.14 JTAG Pin Assignment on the Cortex Debug Connector

Pin Number	Module Connection	Module Connection	Pin Number
1	VDD_JTAG (1.8 V)	JTAG_TMS	2
3	Ground	JTAG_TCK	4
5	Ground	JTAG_TDO	6
7	No pin (key)	JTAG_TDI	8
9*1	Ground	JTAG_RESET#	10

Note 1. By default, TRSTN is not connected and pin 9 is ground. However, resistor options allow TRSTN to be connected to pin 9.

3.17 Parallel Output

This Parallel Output interface is CN2 on the top side of the G3L SMARC Module. A 50-pin, 0.4-mm pitch, 1.5 to 4.00 mm height FPC-to-Board connector from Hirose (part number DF40C-50DS-0.4V(51)) is provided for connection to the RZ/G3L Parallel Output IO.

The RZ/G3L Parallel Output IO is assigned to dual-purpose terminals and may be used either for multiple SMARC interfaces on the RZ SMARC Carrier II (**SYS[1] = OFF**) or for the LCD connector on the G3L SMARC Module (SYS[1] = ON). Refer to **section 2.3, Interface Use Combination List**, for restriction when using Parallel Output interface.

The Parallel Output interface is realized by using the Renesas SMARC RGB-HDMI Adaptor which is included in the kit, then connecting to the FPC-to-Board on the G3L SMARC Module as shown in **Figure 3.8**.

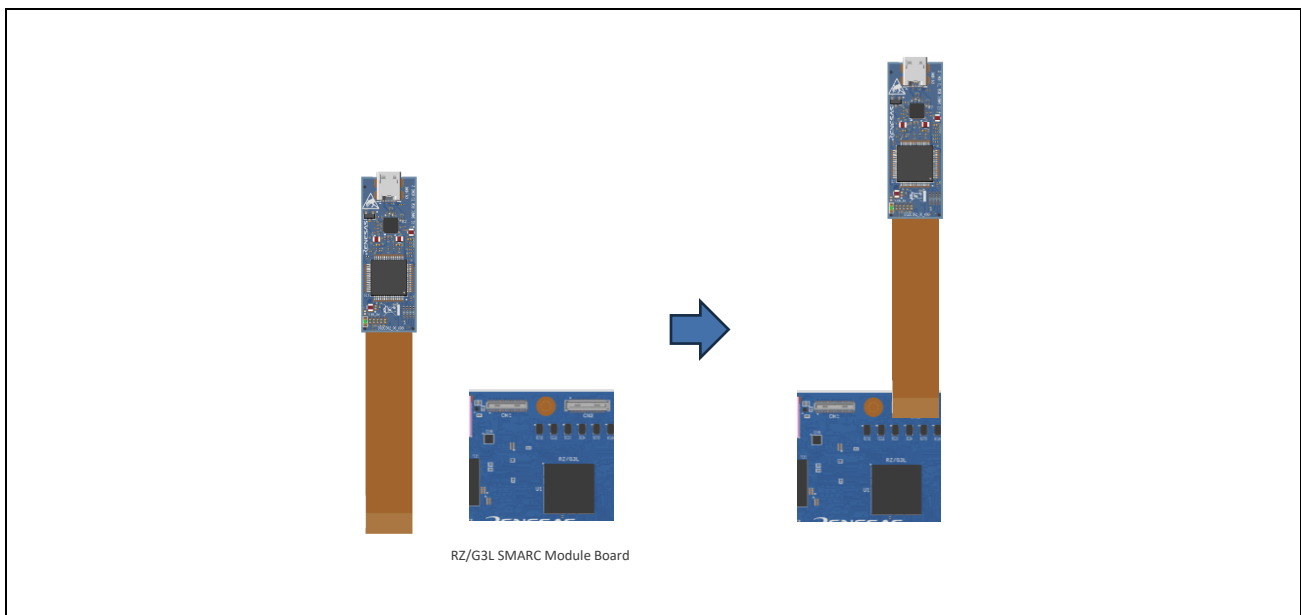


Figure 3.8 SMARC RGB-HDMI Adaptor Connection

The output form of this interface supports HDMI output as default. If you want to output parallel output signals directly to the display panel, this can be realized by developing the custom adaptor board by yourself, then connecting to the FPC-to-Board on the G3L SMARC Module.

Table 3.15 LCD Pin Assignment on the FPC-to Board Connector (1/2)

Pin Number	Module Connection	Module Connection	Pin Number
1	1.8V_ISO (1.8 V)	Ground	2
3	PA4_ISO/RIIC2_SCL (I2C_LCD_SCL)	PA5_ISO/RIIC2_SDA (I2C_LCD_DAT)	4
5	PK3_ISO (DPI_INT#)	PK2_ISO (DPI_RESET#)	6
7	VDD_IN (5.0 V)	Ground	8
9	VDD_IN (5.0 V)	Ground	10
11	VDD_IN (5.0 V)	Ground	12
13	VDD_IN (5.0 V)	Ground	14
15	3.3V_ISO (3.3 V)	Ground	16
17	PK1_ISO (DPI_BKLT_PWM)	PK0_ISO (DPI_VDD_EN)	18
19	3.3V_ISO (3.3 V)	Ground	20
21	DPI_R0	DPI_R1	22

Table 3.15 LCD Pin Assignment on the FPC-to Board Connector (2/2)

Pin Number	Module Connection	Module Connection	Pin Number
23	DPI_R2	DPI_R3	24
25	DPI_R4	DPI_R5	26
27	DPI_R6	DPI_R7	28
29	DPI_G0	DPI_G1	30
31	DPI_G2	DPI_G3	32
33	DPI_G4	DPI_G5	34
35	DPI_G6	DPI_G7	36
37	DPI_B0	DPI_B1	38
39	DPI_B2	DPI_B3	40
41	DPI_B4	DPI_B5	42
43	DPI_B6	DPI_B7	44
45	Ground	DPI_CLK	46
47	DPI_HSYNC	DPI_VSYNC	48
49	DPI_DE	Ground	50

The Parallel Output interface is realized by using the Renesas SMARC RGB-HDMI Adaptor which is included in the kit.

3.17.1 RGB-HDMI Adaptor

The SMARC RGB-HDMI Adaptor is required to convert the RZG3L Parallel Output IO to HDMI output via the RGB to HDMI conversion IC (part number ADV7513BSWZ).

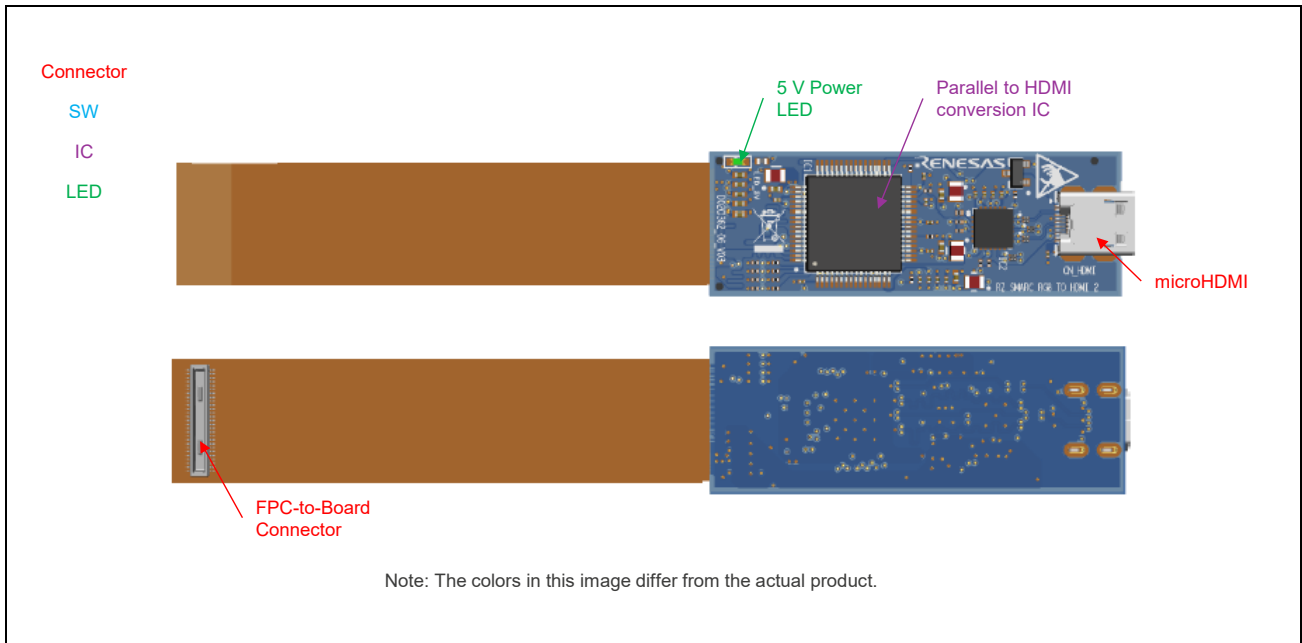


Figure 3.9 SMARC RGB-HDMI Adaptor Top and Bottom View

Regarding the connector mating operation of the SMARC RGB-HDMI Adaptor, insert the adaptor to the connector in vertical direction. Regarding the connector unmating operation, remove the adaptor from the connector in vertical direction. If vertical removal is difficult, lift up either side in longitudinal, contact pitch direction. Do not unmate the connector in lateral direction; otherwise, the contacts could receive great stress.

Refer to **Appendix A**, for details.

3.18 PDM

This MEMS microphone is on the top side of the G3L SMARC Module. A MEMS microphone from TDK InvenSense (part number ICS-41350) is provided for connection to the RZ/G3L PDM IO.

The RZ/G3L PDM IO may be used either for MEMS microphone on the G3L SMARC Module (BOOT[6] = OFF) or for the general purpose IO header on the RZ SMARC Carrier II (BOOT[6] = ON).

3.19 Boot

The GreenPAK used for boot mode and boot device selection on the G3L SMARC Module is listed in **Table 3.16**. GreenPAK is a programmable device, and the SLG7RN47049 is designed based on the [SLG46120V](#).

Table 3.16 Features of the GreenPAK

Part Number	Description
SLG7RN47049	Decodes SMARC-defined boot modes into RZ/G3L-supported boot modes. Selects either a microSD card or eMMC for the SD0 interface. Selects the I/O voltage for the SD0 interface.

The pin configuration and circuit diagram of the GreenPAK are shown below.

Table 3.17 Signal Connections of the SLG7RN47049 (IC18)

Pin	Pin Name	Signal Name	I/O	Buffer	Pin Function																																				
1	VDD	1.8 V_AWO	Power	—	Connected to 1.8 V.																																				
2	RZ_SD0IOVS	RZ_SD0IOVS	I	Input: w/ Schmitt	Selects the I/O voltage for the SD0 I/F.																																				
3	SW_SD0_DEV_SEL	SW_SD0_DEV_SEL	I: PU	Input: w/o Schmitt	Selects the device connected to the SD0 I/F.																																				
4	BOOT_SEL2#	BOOT_SEL2#	I: PU	Input: w/o Schmitt	Connected to SW_MODE-3 on the RZ SMARC Carrier II. Selects the boot mode.																																				
5	BOOT_SEL1#	BOOT_SEL1#	I: PU	Input: w/o Schmitt	Connected to SW_MODE-2 on the RZ SMARC Carrier II. Selects the boot mode.																																				
6	BOOT_SEL0#	BOOT_SEL0#	I: PU	Input: w/o Schmitt	Connected to SW_MODE-1 on the RZ SMARC Carrier II. Selects the boot mode.																																				
7	GND	—	—	—	Connected to ground.																																				
8	RZ_MD_BOOT0	RZ_MD_BOOT0	O	PP	Determines the boot mode.																																				
9	RZ_MD_BOOT1	RZ_MD_BOOT1	O	PP	<table><tr><th colspan="3">MD_BOOT_2 to MD_BOOT_0</th><th>Selected Device</th><th>CA55 Boot</th><th>CM33 Boot</th></tr><tr><td>0</td><td>0</td><td>0</td><td>eSD (3.3-V for execution)</td><td>Supported</td><td>Not supported</td></tr><tr><td>0</td><td>1</td><td>1</td><td>SCIF download</td><td>Supported</td><td>Supported</td></tr><tr><td>1</td><td>0</td><td>0</td><td>USB download</td><td>Supported</td><td>Not supported</td></tr><tr><td>1</td><td>0</td><td>1</td><td>eMMC (1.8-V)</td><td>Supported</td><td>Not supported</td></tr><tr><td>1</td><td>1</td><td>0</td><td>QSPI flash memory (1.8-V)</td><td>Supported</td><td>Supported</td></tr></table>	MD_BOOT_2 to MD_BOOT_0			Selected Device	CA55 Boot	CM33 Boot	0	0	0	eSD (3.3-V for execution)	Supported	Not supported	0	1	1	SCIF download	Supported	Supported	1	0	0	USB download	Supported	Not supported	1	0	1	eMMC (1.8-V)	Supported	Not supported	1	1	0	QSPI flash memory (1.8-V)	Supported	Supported
MD_BOOT_2 to MD_BOOT_0			Selected Device	CA55 Boot		CM33 Boot																																			
0	0	0	eSD (3.3-V for execution)	Supported		Not supported																																			
0	1	1	SCIF download	Supported		Supported																																			
1	0	0	USB download	Supported		Not supported																																			
1	0	1	eMMC (1.8-V)	Supported		Not supported																																			
1	1	0	QSPI flash memory (1.8-V)	Supported	Supported																																				
10	RZ_MD_BOOT2	RZ_MD_BOOT2	O	PP																																					
11	SD0_DEV_SEL	SD0_DEV_SEL	O	PP	Determines the device connected to the SD0 I/F. L: eMMC H: microSD card																																				
12	SD0IOVS	SD0_IOVS	O	PP	Determines the I/O voltage for the SD0 I/F. L: 1.8 V H: 3.3 V																																				

Remarks:

- w/ Schmitt: Digital input with Schmitt trigger
- w/o Schmitt: Digital input without Schmitt trigger
- PP: Push-pull output
- PU: Internal pull-up

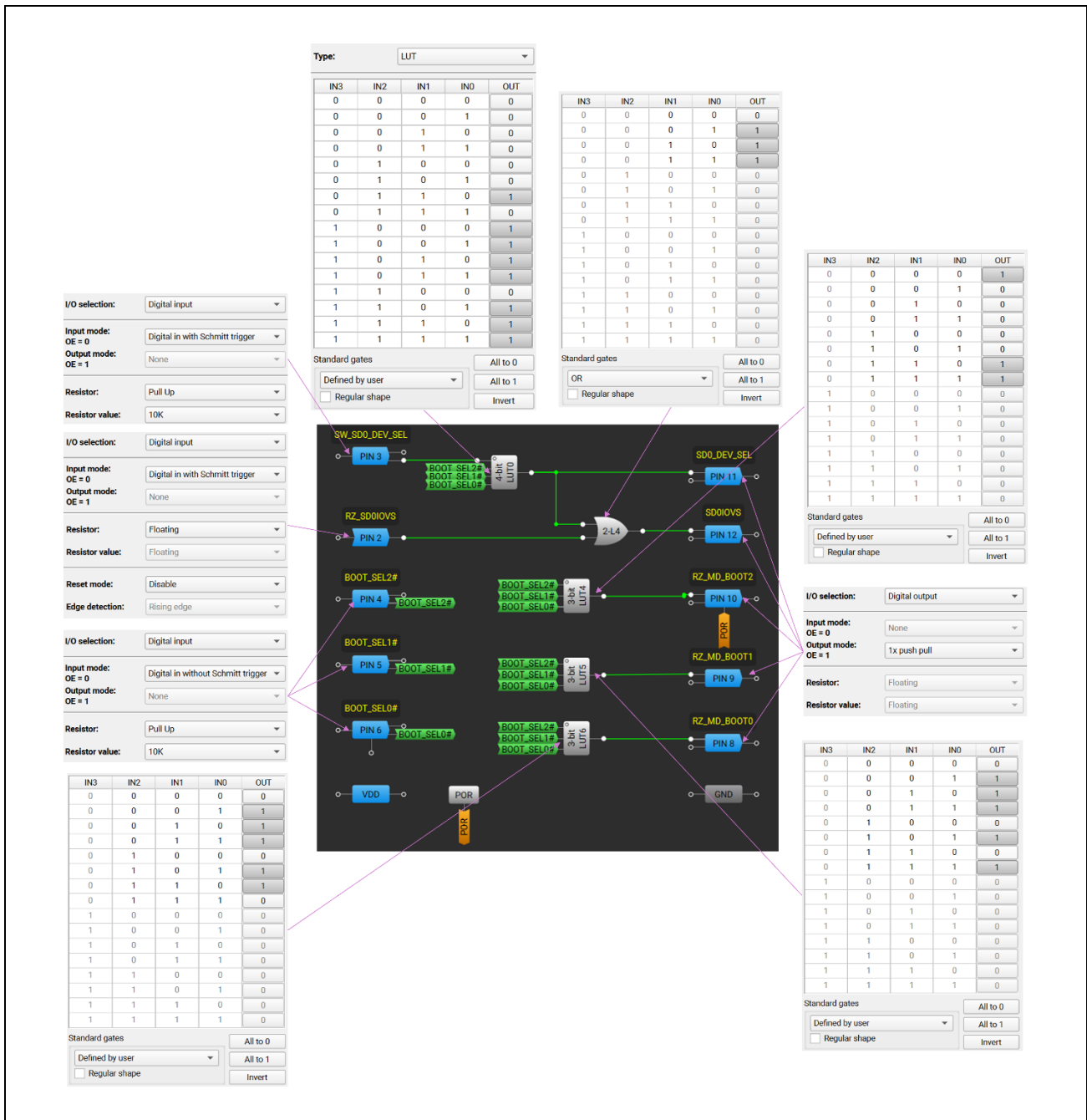


Figure 3.10 Circuit Diagram of the SLG7RN47049

For details, refer to the following datasheet and configuration file included in the **RZ/G3L SMARC Module Board Design Data**. To view the configuration file, download the [Go Configure™ Software Hub](#) from the Renesas website.

- SLG7RN47049_DS_r012_11272023.pdf
- SLG7RN47049_GP_r002U_11022023.gp3

If you design a custom board that does not comply with the SMARC standard and/or does not use the microSD0 card interface, this GreenPAK is not required. The schematic below shows an example implementation in which the BOOT_MODE[x] signals are connected directly to the RZ/G3L SoC. If the SD/MMC Host Channel 0 interface supports only eMMC, signals equivalent to SD0_DEV_SEL and SD0IOVS are not required.

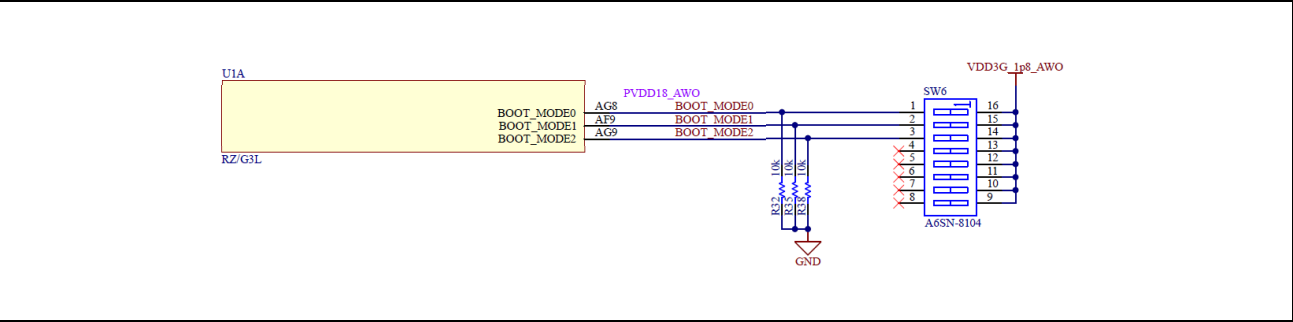


Figure 3.11 Example Connection Without the SLG7RN47049

3.20 SMARC Edge Connector

In the G3L SMARC EVK, the G3L SMARC Module and the RZ SMARC Carrier II are electrically connected through the SMARC edge connector. This section describes the RZ/G3L pins and signals on the G3L SMARC Module that are connected to the SMARC edge connector.

How to Read This Section

This section provides tables, such as **Table 3.18**, that list the connections among the “SMARC Signal Name”, “Pin #”, “RZ Port Pin”, and “Signal” fields. **Figure 3.12** shows these connections on the G3L SMARC Module.

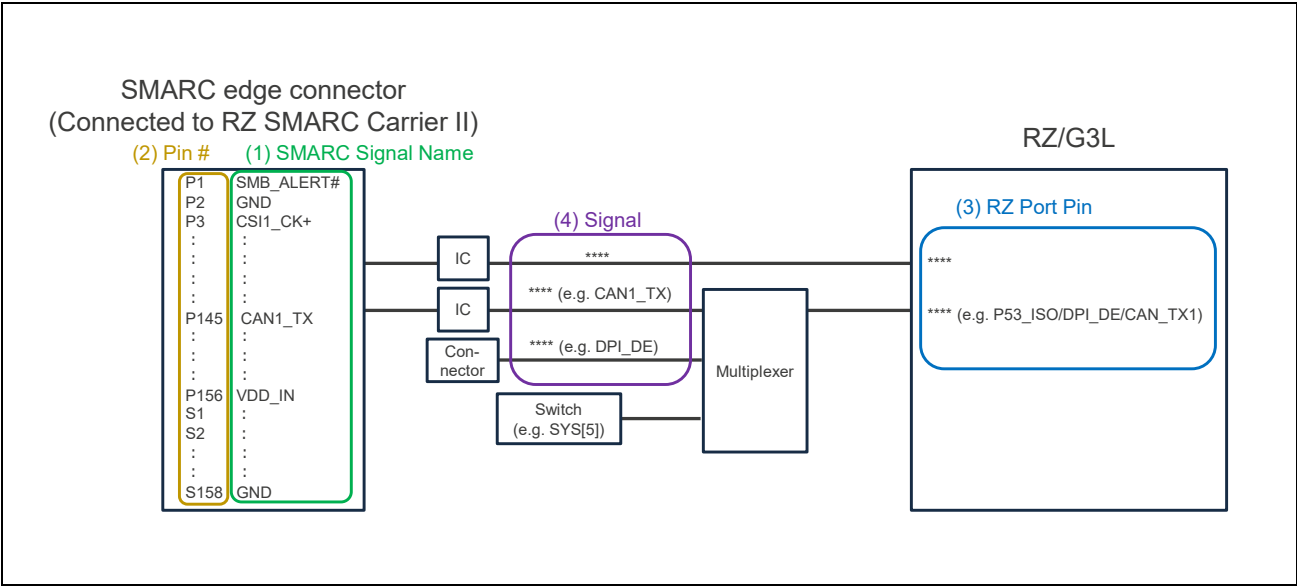


Figure 3.12 Signal Connections on the G3L SMARC Module among the “SMARC Signal Name”, “Pin #”, “RZ Port Pin”, and “Signal” Fields

Table 3.18 Examples of the Connections

(1) SMARC Signal Name	(2) Pin #	(3) RZ Port Pin	(4) Signal*1
CAN0_TX	P143	P33_AWO/CAN_TX0	CAN0_TX
CAN0_RX	P144	P32_AWO/CAN_RX0	CAN0_RX
CAN1_TX	P145	P53_ISO/DPI_DE/CAN_TX1	PDM0_DAT1*2 CAN1_TX*2
CAN1_RX	P146	P52_ISO/DPI_VSYNC/CAN_RX1	PDM0_CLK1*2 CAN1_RX*2

Note 1. Some RZ port pins are connected to a multiplexer, and the signal connected to the RZ port pin depends on the switch setting.

Note 2. The signal connected to the RZ port pin depends on the SYS[5] switch setting on the G3L SMARC Module. The upper entry corresponds to SYS[5] = ON, and the lower entry corresponds to **SYS[5] = OFF**.

The SMARC Edge connector has a Primary side (Pxx) and Secondary side (Sxx). The SMARC signal names and Edge connector pin numbers are listed in the tables below along with the G3L port pin (if applicable) and signal name. The default settings are highlighted.

(1) SMARC Signal Name

“SMARC Signal Name” indicates the signals on the SMARC edge connector. They are described according to the definitions in the SMARC 2.1.1 Specification. Therefore, the signal names do not necessarily correspond to the channel numbers or function names on the RZ/G3L SoC. For example, in **Table 3.18**, the CAN_TX1 function of the RZ/G3L is connected to CAN1_TX (P145) on the SMARC edge connector.

(2) Pin #

The SMARC edge connector consists of two sides: the Primary side and the Secondary side. Pin # refers to the pin numbers on the SMARC edge connector. Pin numbers on the Primary side are denoted as “Pxx”, while those on the Secondary side are denoted as “Sxx”. They are also described according to the definitions in the SMARC 2.1.1 Specification.

(3) RZ Port Pin

“RZ Port Pin” indicates the names of the pins on the RZ/G3L SoC that can be connected to the SMARC edge connector. These pin names correspond to those described in the **RZ/G3L Group Hardware Manual**. Appropriate switch settings may be required to enable the connections.

(4) Signal

“Signal” indicates the names of the signals that can be connected to the RZ port pins on the G3L SMARC Module. These signal names are selected to clearly indicate the function of each signal. Due to the multiplexing configuration, the schematic may be designed so that multiple signal types can be assigned to a single RZ/G3L port pin. In such cases, the configuration corresponding to the default switch settings is highlighted.

3.20.1 Display Interfaces

The RZ/G3L has a combo PHY that integrates LVDS and MIPI DSI. The LVDS0 and DSI0 signals are routed to the SMARC Edge connector. Display interfaces are selectable from the following options, with only one interface usable at a time:

- (1) LVDS*1*2
- (2) MIPI DSI*2*3
- (3) Parallel Output

Control signals for display interfaces (1) and (2) are assigned to dual-purpose terminals. These signals are used either for the mini-PCIe connector on the RZ SMARC Carrier II (SYS[5] = OFF) or for the LCD connector as the Parallel Output interface on the G3L SMARC Module (SYS[5] = ON).

NOTE

1. The LVDS interface is supported by the SMARC Dual LVDS-HDMI Adaptor, which can operate as a single LVDS interface when used with the G3L SMARC EVK.
2. Do not connect the SMARC Dual LVDS-HDMI Adaptor or the SMARC DSI-HDMI Adaptor to the mini-PCIe connector on the RZ SMARC Carrier II during AWO or AWO + DDR_Retention mode.
3. Products with #AC0 or #BC0 in the part number, manufactured in the production lots listed below, have restrictions on MIPI DSI features. For details, contact a Renesas Electronics sales representative.

S.LOT# on the Outer Box Label: 0000308367 – 0000309059

As described in **section 1.1**, the SMARC DSI-HDMI Adaptor is connected by default to the bottom-side connector on the RZ SMARC Carrier II. Because the MIPI DSI and LVDS interfaces on the RZ/G3L share a combo PHY, the LVDS interface can be evaluated by replacing the SMARC DSI-HDMI Adaptor with the SMARC Dual LVDS-HDMI Adaptor.

See **Figure 3.13** for information on installing the SMARC Dual LVDS-HDMI Adaptor.

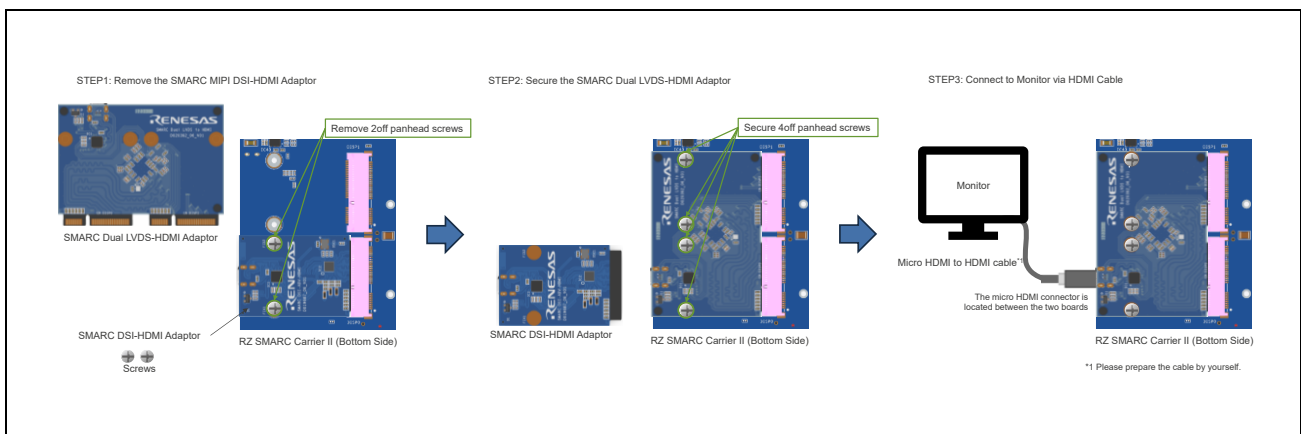


Figure 3.13 Replacing the SMARC DSI-HDMI Adaptor with the SMARC Dual LVDS-HDMI Adaptor

Details of the display interfaces on the RZ SMARC Carrier II board are to be found in the [RZ SMARC Series Carrier Board II Evaluation Board Manual](#).

Table 3.19 LVDS/MIPI Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
LVDS0_0+ / DSI0_D0+	S125	DSI_LVDS0_D0_P	LVDS0_0+
LVDS0_0- / DSI0_D0-	S126	DSI_LVDS0_D0_N	LVDS0_0-
LVDS0_1+ / DSI0_D1+	S128	DSI_LVDS0_D1_P	LVDS0_1+
LVDS0_1- / DSI0_D1-	S129	DSI_LVDS0_D1_N	LVDS0_1-
LVDS0_2+ / DSI0_D2+	S131	DSI_LVDS0_D2_P	LVDS0_2+
LVDS0_2- / DSI0_D2-	S132	DSI_LVDS0_D2_N	LVDS0_2-
LVDS0_3+ / DSI0_D3+	S137	DSI_LVDS0_D3_P	LVDS0_3+
LVDS0_3- / DSI0_D3-	S138	DSI_LVDS0_D3_N	LVDS0_3-
LVDS0_CK+ / DSI0_CLK+	S134	DSI_LVDS0_CLK_P	LVDS0_CK+
LVDS0_CK- / DSI0_CLK-	S135	DSI_LVDS0_CLK_N	LVDS0_CK-
LCD0_VDD_EN	S133	P54_ISO/DPI_G7	DPI_G7* ¹ LCD0_VDD_EN* ¹
LCD0_BKLT_EN	S107	P55_ISO/DPI_B7	DPI_B7* ¹ LCD0_BKLT_EN* ¹
LCD0_BKLT_PWM	S141	P56_ISO/DPI_R7	DPI_R7* ¹ LCD0_BKLT_PWM* ¹
LVDS1_0+ / DSI1_D0+	S111	LVDS1_DATA0P	Not connected
LVDS1_0- / DSI1_D0-	S112	LVDS1_DATA0N	Not connected
LVDS1_1+ / DSI1_D1+	S114	LVDS1_DATA1P	Not connected
LVDS1_1- / DSI1_D1-	S115	LVDS1_DATA1N	Not connected
LVDS1_2+ / DSI1_D2+	S117	LVDS1_DATA2P	Not connected
LVDS1_2- / DSI1_D2-	S118	LVDS1_DATA2N	Not connected
LVDS1_3+ / DSI1_D3+	S120	LVDS1_DATA3P	Not connected
LVDS1_3- / DSI1_D3-	S121	LVDS1_DATA3N	Not connected
LVDS1_CK+ / DSI1_CLK+	S108	LVDS1_CLKP	Not connected
LVDS1_CK- / DSI1_CLK-	S109	LVDS1_CLKN	Not connected
LCD1_VDD_EN	S116	PA6/GPIO	Not connected
LCD1_BKLT_EN	S107	P37/GPIO	Not connected
LCD1_BKLT_PWM	S122	PA7/GPIO	Not connected
I2C_LCD_DAT	S140	PA5/SDA7	I2C_LCD_DAT
I2C_LCD_CK	S139	PA4/SCL7	I2C_LCD_CK

Note 1. SYS[5] switch option on the G3L SMARC Module

3.20.2 Camera Interfaces

The CSI1 signals are routed to the SMARC Edge connector.

The control signals for the camera interface are assigned to dual-purpose terminals. These signals are used either for the 22-pin FPC connector on the RZ SMARC Carrier II (BOOT[6] = OFF) or for the general purpose IO header on the RZ SMARC Carrier II (BOOT[6] = ON).

NOTE

Do not connect the SMARC Pi Camera Adaptor to a 22-pin FPC connector on the RZ SMARC Carrier II during AWO or AWO + DDR_Retention mode.

The details of camera interface of the RZ SMARC Carrier II board are to be found in the [RZ SMARC Series Carrier Board II Evaluation Board Manual](#).

Table 3.20 MIPI CSI Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
CSI1_RX0+	P7	CSI_D0_P	CSI1_RX0+
CSI1_RX0-	P8	CSI_D0_N	CSI1_RX0-
CSI1_RX1+	P10	CSI_D1_P	CSI1_RX1+
CSI1_RX1-	P11	CSI_D2_N	CSI1_RX1-
CSI1_RX2+	P13	—	Not connected
CSI1_RX2-	P14	—	Not connected
CSI1_RX3+	P16	—	Not connected
CSI1_RX3-	P17	—	Not connected
CSI1_CLK+	P3	CSI_CLK_P	CSI1_CLK+
CSI1_CLK-	P4	CSI_CLK_N	CSI1_CLK-
I2C_CAM1_DAT	S2	PA7_ISO/RIIC1_SDA	I2C_CAM1_DAT
I2C_CAM1_CLK	S1	PA6_ISO/RIIC1_SCL	I2C_CAM1_CLK
CAM1_PWR#	P109	PM6_AWO/RSCI0_SCLK	SPI0_CLK* ¹ GPIO1/CAM1_PWR#* ¹
CAM1_RST#	P111	PM7_AWO/RSCI0_SS_CTS#_RTS#	SPI0_CS0#* ¹ GPIO3/CAM1_RST#* ¹
CAM_MCK	S6	—	Not connected

Note 1. BOOT[6] switch option on the G3L SMARC Module

3.20.3 SDIO Card (4-bit) Interface

The SDIO signal is routed to the SMARC Edge connector.

The RZ/G3L SD1 IO is assigned to dual-purpose terminals and is used either for the microSD card slot on the RZ SMARC Carrier II (**BOOT[1] = OFF**) or for the MISC connector as the JTAG interface on the G3L SMARC Module (BOOT[1] = ON).

Table 3.21 SDIO Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
SDIO_D0	P39	PG2_ISO/SD1_DAT0	SDIO_D0
SDIO_D1	P40	PG3_ISO/SD1_DAT1	SDIO_D1
SDIO_D2	P41	PG4_ISO/SD1_DAT2	SDIO_D2
SDIO_D3	P42	PG5_ISO/SD1_DAT3	SDIO_D3
SDIO_WP	P33	—	Not connected
SDIO_CMD	P34	PG1_ISO/SD1_CMD	SDIO_CMD
SDIO_CD#	P35	PJ0_AWO/JTAG_TMS/SD1_CD	RZ_TMS_SWDIO* ¹ SDIO_CD#* ¹
SDIO_CLK	P36	PG0_ISO/SD1_CLK	SDIO_CLK
SDIO_PWR_EN	P37	PJ2_AWO/JTAG_TDO/SD1_PWEN	RZ_TDO* ¹ RZ_SD1_PWEN* ¹
—	—	PJ1_AWO/JTAG_TCK/SD1_IOVS	RZ_TCK_SWCLK* ¹ RZ_SD1_IOVS* ¹

Note 1. BOOT[1] switch option on the G3L SMARC Module

3.20.4 SPI Interfaces

The SPI0 and SPI1 signals are routed to the SMARC Edge connector.

The RZ/G3L RSPI ch0 IO is assigned to dual-purpose terminals and is used either for the MEMS microphone on the RZG3L SMARC Module and the 22-pin FPC connector on the RZ SMARC Carrier II (BOOT[6] = OFF) or for the general purpose IO header on the RZ SMARC Carrier II (BOOT[6] = ON).

The RZ/G3L RSPI ch1 IO is assigned to dual-purpose terminals and is used either for the PMOD0 connector on the RZ SMARC Carrier II (SYS[5] = OFF) or for the LCD connector as the Parallel Output interface on the G3L SMARC Module (SYS[5] = ON).

Table 3.22 SPI0 and SPI1 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal Passing through a Multiplexer
SPI0_CS0#	P43	PM7_AWO/RSCI0_SS_CTS#_RTS#	SPI0_CS0#*1
			GPIO3/CAM1_RST#*1
SPI0_CS1#	P31	—	Not connected
SPI0_CK	P44	PM6_AWO/RSCI0_SCLK	SPI0_CK*1
			GPIO1/CAM1_PWR#*1
SPI0_DIN*1	P45	PM5_AWO/PDM_CLK1/RSCI0_RXD_MISO_SCL	SPI0_DIN*1
			PDM_CLK1*1
SPI0_DO	P46	PM4_AWO/PDM_DAT1/ RSCI0_TXD_MOSI_DAT	SPI0_DO*1
			PDM_DAT1*1
SPI1_CS0#	P54	P63_ISO/DPI_G5/RSPI2_SS1A	DPI_G5*2
			SPI1_CS0#*2
SPI1_CS1#	P55	—	Not connected
SPI1_CK	P56	P62_ISO/DPI_R6/RSPI2_SCK	DPI_R6*2
			SPI1_CK*2
SPI1_DIN	P57	P60_ISO/DPI_G6/RSPI2_MISO	DPI_G6*2
			SPI1_DIN*2
SPI1_DO	P58	P61_ISO/DPI_B6/RSPI2_MOSI	DPI_B6*2
			SPI1_DO*2

Note 1. BOOT[6] switch option on the G3L SMARC Module

Note 2. SYS[5] switch option on the G3L SMARC Module

3.20.5 Audio

The I2S0 and I2S2 signals are routed to the SMARC Edge connector.

The RZ/G3L SSI ch0 IO is assigned to dual-purpose terminals and is used either for audio codec as SSI interface on the RZ SMARC Carrier II (**SYS[4] = OFF**) or for the microSD2 Card interface on the G3L SMARC Module (SYS[4] = ON).

The RZ/G3L SSI ch2 IO is assigned to dual-purpose terminals and is used either for audio codec as SSI interface on the RZ SMARC Carrier II (**SYS[5] = OFF**) or for the LCD connector as the Parallel Output interface on the G3L SMARC Module (SYS[5] = ON).

Table 3.23 I2S0 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
I2S0_LRCK	S39	PH2_ISO/SSIF0_RCK/SD2_DAT0	RZ_SD2DAT0*1 I2S0_LRCK*1
I2S0_SDOUT	S40	PH3_ISO/SSIF0_TXDSD2_DAT1	RZ_SD2DAT1*1 I2S0_SDOUT*1
I2S0_SDIN	S41	PH0_ISO/SSIF0_RXD/SD2_CLK	RZ_SD2CLK*1 I2S0_SDIN*1
I2S0_CK	S42	PH1_ISO/SSIF0_BCK/SD2_CMD	RZ_SD2CMD*1 I2S0_CK*1
AUDIO_MCK	S38	N/A	AUDIO_MCK (clock generator)

Note 1. SYS[4] switch option on the G3L SMARC Module

Table 3.24 I2S2 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
I2S2_LRCK	S50	P72_ISO/DPI_G3/SSIF2_RCK	DPI_G3*1 I2S2_LRCK*1
I2S2_SDOUT	S51	P73_ISO/DPI_B3/SSIF2_TXD	DPI_B3*1 I2S2_SDOUT*1
I2S2_SDIN	S52	P70_ISO/DPI_B4/SSIF2_RXD	DPI_B4*1 I2S2_SDIN*1
I2S2_CK	S53	P71_ISO/DPI_R4/SSIF2_BCK	DPI_R4*1 I2S2_CK*1

Note 1. SYS[5] switch option on the G3L SMARC Module

3.20.6 I2C Interfaces

The I2C_GP, I2C_PM, I2C_CAM1, and I2C_LCD signals are routed to the SMARC Edge connector.

The I2C_CAM0 is not connected to the SMARC Edge connector.

The RZ/G3L RIIC ch3 IO is assigned to dual-purpose terminals and is used either I2C interface (SYS[2] = OFF) or I3C interface (SYS[2] = ON).

Table 3.25 I2C_GP, I2C_PM, I2C_CAM1, and I2C_LCD Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
I2C_CAM1_CK	S1	PA6_ISO/RIIC1_SCL	I2C_CAM1_CK
I2C_CAM1_DAT	S2	PA7_ISO/RIIC1_SDA	I2C_CAM1_DAT
I2C_GP_CK	S48	P20_ISO/I3C_SCL/RIIC3_SCL	RZ_SCL30* ¹ I2C_GP_CK* ¹
I2C_GP_DAT	S49	P21_ISO/I3C_SDA/RIIC3_SDA	RZ_SDA30* ¹ I2C_GP_DAT* ¹
I2C_PM_CK	P121	PL2_AWO/RIIC0_SCL	I2C_PM_CK
I2C_PM_DAT	P122	PL3_AWO/RIIC0_SDA	I2C_PM_DAT
I2C_LCD_CK	S139	PA4_ISO/RIIC2_SCL	I2C_LCD_CK
I2C_LCD_DAT	S140	PA5_ISO/RIIC2_SDA	I2C_LCD_DAT

Note 1. SYS[2] switch option on the G3L SMARC Module

NOTE

RIIC0 bus is also used on the G3L SMARC Module itself for:

- Power/Reset Control: SLG7RN48373
- PMIC: RAA215300A2GNP#HAA
- Power Regulator: SLG7RN48374
- Clock Generator: 5P35023B-789NLGI

3.20.7 Asynchronous Serial Ports

The SER0, SER1, SER2, and SER3 signals are routed to the SMARC Edge connector.

The RZ/G3L RSCI ch2 is assigned to dual-purpose terminals and is used either for the PMOD1 connector on the RZ SMARC Carrier II (SYS[5] = OFF) or for the LCD connector as the Parallel Output interface on the G3L SMARC Module (SYS[5] = ON).

The RZ/G3L RSCI ch3 IO is assigned to dual-purpose terminals and is used either for the Grove connector on the RZ SMARC Carrier II (SYS[5] = OFF) or for the LCD connector as the Parallel Output interface on the G3L SMARC Module (SYS[5] = ON).

Table 3.26 SER0, SER1, SER2, and SER3 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
SER0_TX	P129	P77_ISO/DPI_R2/RSCI2_TXD_MOSI_SDA	DPI_R2*1 SER0_TX*1
SER0_RX*1	P130	P76_ISO/DPI_B2/RSCI2_RXD_MISO_SCL	DPI_B2*1 SER0_RX*1
SER0_RTS#	P131	P81_ISO/DPI_B1/RSCI2_SS_CTS#_RTS#	DPI_B1*1 SER0_RTS#*1
SER0_CTS#	P132	P80_ISO/DPI_G1/RSCI2_CTS	DPI_G1*1 SER0_CTS0#*1
SER1_TX	P134	P83_ISO/DPI_G0/RSCI3_TXD_MOSI_SDA	DPI_G0*1 SER1_TX*1
SER1_RX	P135	P82_ISO/DPI_R1/RSCI3_RXD_MISO_SDA	DPI_R1*1 SER1_RX*1
SER2_TX	P136	PD5_ISO/RSCI1_TXD_MOSI_SDA	SER2_TX
SER2_RX	P137	PD4_ISO/RSCI1_RXD_MISO_SCL	SER2_RX
SER2_RTS#	P138	PD7_ISO/RSCI1_SS_CTS#_RTS#	SER2_RTS#
SER2_CTS#	P139	PD6_ISO/RSCI1_CTS	SER2_CTS#
SER3_TX	P140	SCIF0_TXD	SER3_TX
SER3_RX	P141	SCIF0_RXD	SER3_RX

Note 1. SYS[5] switch option on the G3L SMARC Module

3.20.8 CAN Bus

These signals are routed to the SMARC Edge connector.

The RZ/G3L CAN ch0 and ch1 IO are assigned to dual-purpose terminals and are used either for the CAN transceiver on the RZ SMARC Carrier II (SYS[5] = OFF) or for the LCD connector as the Parallel Output interface on the RZ SMARC Carrier II (SYS[5] = ON).

Table 3.27 CAN0 and CAN1 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
CAN0_TX	P143	P33_AWO/CAN_TX0	CAN0_TX
CAN0_RX	P144	P32_AWO/CAN_RX0	CAN0_RX
CAN1_TX	P145	P53_ISO/DPI_DE/CAN_TX1	DPI_VSYNC*1 CAN1_TX*1
CAN1_RX	P146	P52_ISO/DPI_VSYNC/CAN_RX1	DPI_DE*1 CAN1_RX*1

Note 1. SYS[5] switch option on the G3L SMARC Module

3.20.9 USB Interfaces

The USB ch0, and ch1 signals are routed to the SMARC Edge connector.

The USB ch2, ch3, ch4, and ch5 signals are not connected to the SMARC Edge connector.

Table 3.28 USB0 and USB1 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
USB0+	P60	USB20_DP	USB0+
USB0-	P61	USB20_DM	USB0-
USB0_EN_OC#	P62	P31_AWO/USB20_VBUSEN	RZ_P31_AWO/USB20_VBUSEN* ¹
		P30_AWO/USB20_OVRCUR	RZ_P30_AWO/USB20_OVRCUR* ¹
USB0_VBUS_DET	P63	USB20_VBUSIN	USB0_VBUS_DET
USB0_OTG_ID	P64	USB20_OTGID	USB0_OTG_ID
USB1+	P65	USB21_DP	USB1+
USB1-	P66	USB21_DM	USB1-
USB1_EN_OC#	P67	P35_AWO/USB21_VBUSEN	RZ_P35_AWO/USB21_VBUSEN* ¹
		P34_AWO/USB21_OVRCUR	RZ_P34_AWO/USB21_OVRCUR* ¹

Note 1. Logic circuitry is used to provide independent enable and overcurrent IO.

The VBUS control signals (USBxx_VBUSEN) and overcurrent detection signals (USBxx_OVRCUR#) for the USB interfaces are connected to a VBUS power switch IC (e.g., ISL61852). However, the SMARC standard assigns only one pin (USBx_EN_OC#) for these signals. Therefore, logic circuitry implemented in a GreenPAK on the G3L SMARC Module provides both functions using a single pin, as shown in **Figure 3.14**.

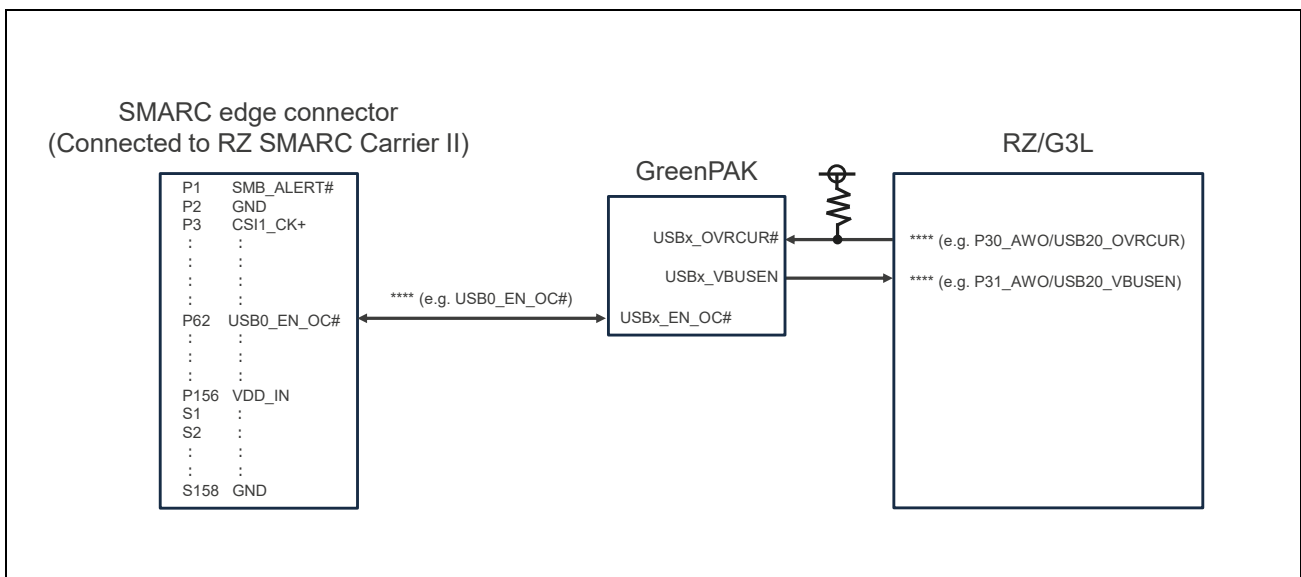


Figure 3.14 USB VBUS Control and Overcurrent Detection Implementation Using a GreenPAK

The GreenPAK is a programmable device, and the SLG4E46290 is designed based on the [SLG46108](#) to provide this function.

The pin configuration and circuit diagram of the GreenPAK are shown below.

Table 3.29 Signal Connections of the SLG4E46290 (IC19)

Pin	Pin Name	Signal Name	I/O	Buffer	Pin Function
1	VDD	3.3 V_ISO	Power	—	Connected to 3.3 V.
2	USB0_VBUSEN	RZ_P01/USB20_VBUSEN	I: PD	LV	VBUS input enable for USB 2.0 channel 0 from the RZ/G3E.
3	USB0_OVRCUR#	RZ_P00/USB20_OVRCURN	O	OD	Outputs the overcurrent detection signal to USB 2.0 channel 0 of the RZ/G3E.
4	USB0_EN_OC#	USB0_EN_OC#	I/O: PU	Input: w/ Schmitt Output: OD	Enables the VBUS output of USB port controller channel 0 (IC35) on the RZ SMARC Carrier II. Overcurrent input: This signal is driven low by channel 0 of the port controller.
5	GND	GND	—	—	Connected to ground.
6	USB1_VBUSEN	RZ_PG3/USB21_VBUSEN	I: PD	LV	VBUS input enable for USB 2.0 channel 1 from the RZ/G3E.
7	USB1_OVRCUR#	RZ_PG6/USB21_OVRCURN	O	OD	Outputs the overcurrent detection signal to USB 2.0 channel 1 of the RZ/G3E.
8	USB1_EN_OC#	USB1_EN_OC#	I/O: PU	Input: w/ Schmitt Output: OD	Not used because this function is handled by the USB hub (IC37) on the RZ SMARC Carrier II.

Remarks:

- LV: Low-voltage digital input
- w/ Schmitt: Digital input with Schmitt trigger
- OD: Open-drain output
- PD: Internal pull-down
- PU: Internal pull-up

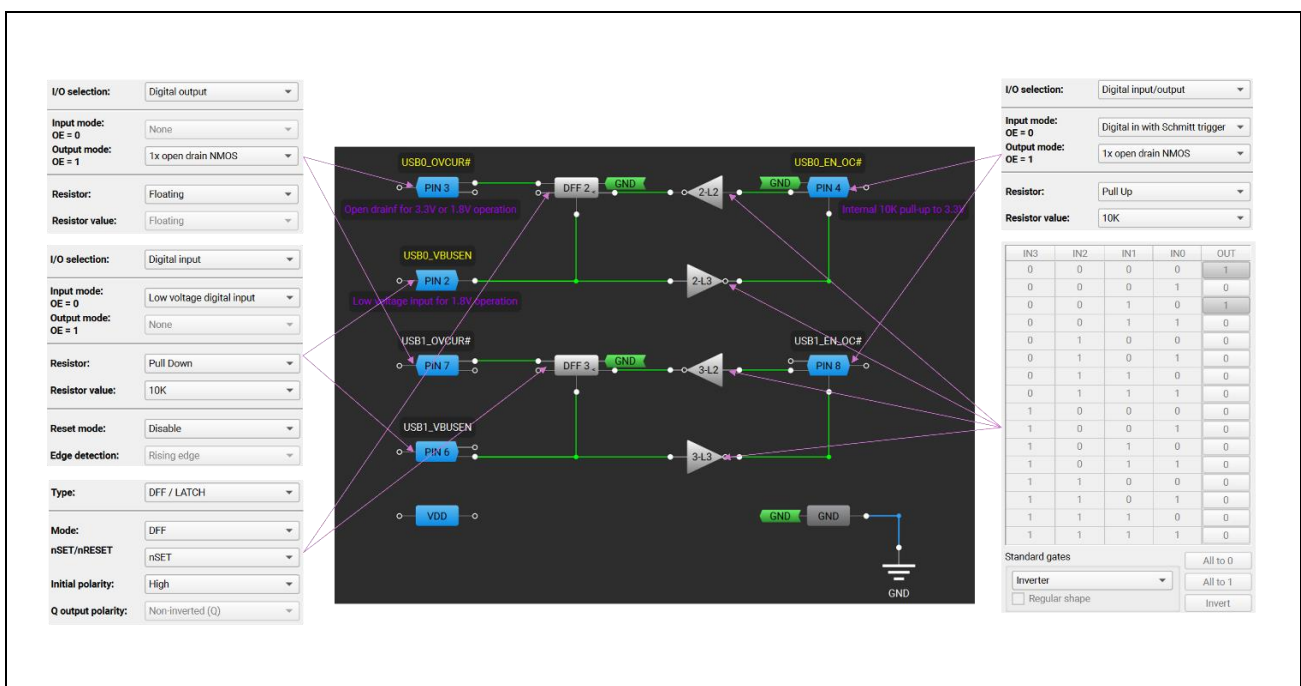


Figure 3.15 Circuit Diagram of the SLG4E46290

For details, refer to the following datasheet and configuration file included in the **RZ/G3L SMARC Module Board Design Data**. To view the configuration file, download the [Go Configure™ Software Hub](#) from the Renesas website.

- SLG4E46290_DS_r011_03312023.pdf
- SLG4E46290_GP_r001U_01242023.gp3

If you design a custom board that does not comply with the SMARC standard, this GreenPAK is not required. The schematic below shows an example implementation in which the VBUS control signal and overcurrent detection signal are connected directly to the VBUS power switch IC.

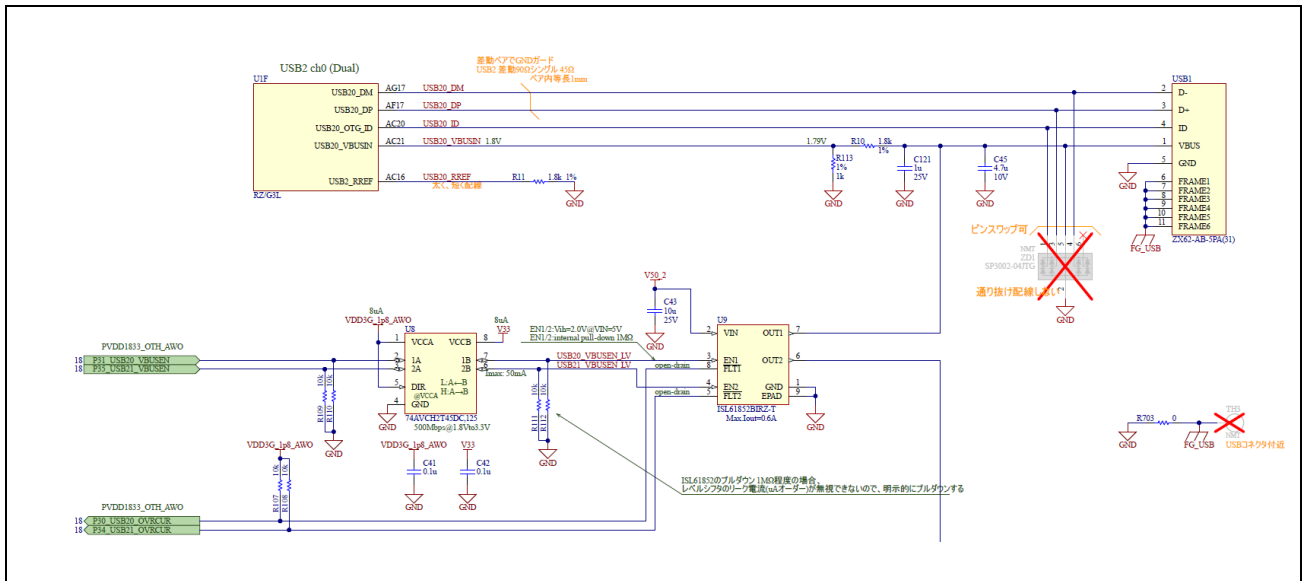


Figure 3.16 Example Connection Without the SLG4E46290

3.20.10 PCI Express

The PCIE_A signal is routed to the SMARC Edge connector.

The PCIE_B, PCIE_C, and PCIE_D signals are not connected to the SMARC Edge connector.

Table 3.30 PCIE_A Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
PCIE_A_TX+	P89	PCIE_TX_P	PCIE_A_TX+
PCIE_A_TX-	P90	PCIE_TX_N	PCIE_A_TX-
PCIE_A_RX+	P86	PCIE_RX_P	PCIE_A_RX+
PCIE_A_RX-	P87	PCIE_RX_N	PCIE_A_RX-
PCIE_A_REFCK+	P83	N/A	PCIE_A_REFCK+ (clock generator)
PCIE_A_REFCK-	P84	N/A	PCIE_A_REFCK- (clock generator)
PCIE_A_RST#	P75	PG7_ISO/PCIE_RST_OUT#	RZ_PG7_ISO/PCIE_RST_OUT#
PCIE_A_CKREQ#	P78	PG6_ISO	RZ_PG6_ISO/PCIE_A_CKREQ#

3.20.11 SATA

The RZG3L does not support SATA interfaces. None of the SATA signals are connected.

3.20.12 Ethernet

These signals are routed to the SMARC Edge connector.

Table 3.31 GBE0 and GBE1 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
GBE0_MDI0+	P30	—	These signals are provided by the Ethernet PHY controlled by the RZ RGMII signals ET0_xxx
GBE0_MDI0-	P29		
GBE0_MDI1+	P27		
GBE0_MDI1-	P26		
GBE0_MDI2+	P24		
GBE0_MDI2-	P23		
GBE0_MDI3+	P20		
GBE0_MDI3-	P19		
GBE0_LINK100#	P21	N/A	ET0_LED2 (ET0 PHY)
GBE0_LINK1000#	P22	N/A	ET0_LED2 (ET0 PHY)
GBE0_LINK_ACT#	P25	N/A	ET0_LED1 (ET0 PHY)
GBE0_CTREF	P28	—	Not connected
GBE0_SDP	P6	—	Not connected
GBE1_MDI0+	S17	—	These signals are provided by the Ethernet PHY controlled by the RZ RGMII signals ET1_xxx
GBE1_MDI0-	S18		
GBE1_MDI1+	S20		
GBE1_MDI1-	S21		
GBE1_MDI2+	S23		
GBE1_MDI2-	S24		
GBE1_MDI3+	S26		
GBE1_MDI3-	S27		
GBE1_LINK100#	S19	N/A	ET1_LED2 (ET1 PHY)
GBE1_LINK1000#	S22	N/A	ET1_LED2 (ET1 PHY)
GBE1_LINK_ACT#	S31	N/A	ET1_LED1 (ET1 PHY)
GBE1_CTREF	S28	—	Not connected
GBE1_SDP	P5	—	Not connected

3.20.13 GPIO

These signals are routed to the SMARC Edge connector.

The GPIO0, GPIO8, GPIO9 are used either for GPIO (SYS[4] = OFF) or for the microSD2 card slot on the G3L SMARC Module (SYS[4] = ON). In addition, if GPIO is selected, these signals are used either for each function on the RZ SMARC Carrier II (SYS[5] = OFF) or for the LCD connector as the Parallel Output interface on the G3L SMARC Module (SYS[5] = ON).

The GPIO4 is used either for the interrupt function of RZ/G3L (BOOT[1] = OFF) or for the MISC connector on the G3L SMARC Module (BOOT[1] = ON). In addition, if interrupt function is selected, this interrupt signal is used either for PMOD0 connector on the RZ SMARC Carrier II (SW_GPIO4 = 1-2) or for the tamper detection function of RZ/G3L (SW_GPIO4 = 2-3).

Table 3.32 GPIO Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal Passing through a Multiplexer	
GPIO0	P108	PK2_ISO/SD2_PWEN	RZ_SD2PWEN* ¹	
			RZ_PK2_ISO* ¹	RZ_PK2_ISO_DPI_RESET#* ²
			GPIO0* ²	
GPIO1	P109	PM6_AWO/RSCIO_SCLK	SPI0_CK* ³	
			GPIO1/CAM1_PWR#* ³	
GPIO2	P110	PK3_ISO	RZ_PK3_ISO_DPI_INT#* ²	
			GPIO2* ²	
GPIO3	P111	PM7_AWO/RSCIO_SS_CTS#_RTS#	SPI0_CS0#* ³	
			GPIO3/CAM1_RST#* ³	
GPIO4	P112	PJ3_AWO/JTAG_TDI/IRQ7	RZ_TDI* ⁴	
			GPIO4* ⁴	RZ_VBAT_TAMPER* ⁵
			GPIO4/GPIO4_TAMPER2* ⁵	
GPIO5	P113	P74_ISO/DPI_R3	DPI_R3* ²	
			GPIO5* ²	
GPIO6	P114	P64_ISO/DPI_B5	DPI_B5* ²	
			GPIO6* ²	
GPIO7	P115	P65_ISO/DPI_R5	DPI_R5* ²	
			GPIO7* ²	
GPIO8	P116	PK0_ISO/SD2_CD	RZ_SD2CD#* ¹	
			RZ_PK0_ISO* ¹	RZ_PK0_ISO_DPI_VDD_EN* ²
			GPIO8* ²	
GPIO9	P117	PK1_ISO/SD2_IOVS	RZ_SD2_IOVS* ¹	
			RZ_PK1_ISO* ¹	RZ_PK1_ISO_DPI_BKLT_PWM* ²
			GPIO9* ²	
GPIO10	P118	P85_ISO/DPI_B0	DPI_B0* ²	
			GPIO10* ²	
GPIO11	P119	P75_ISO/DPI_G2	DPI_G2* ²	
			GPIO11* ²	
GPIO12	S142	P66_ISO/DPI_G4	DPI_G4* ²	
			GPIO12* ²	
GPIO13	S123	P84_ISO/DPI_R0	DPI_R0* ²	
			GPIO13* ²	

Note 1. SYS[4] switch option on the G3L SMARC Module

Note 2. SYS[5] switch option on the G3L SMARC Module

Note 3. BOOT[5] switch option on the G3L SMARC Module

Note 4. SW_GPIO4 switch option on the G3L SMARC Module

Note 5. BOOT[1] switch option on the G3L SMARC Module

4. Certifications

The G3L SMARC Module comprising the G3L SMARC EVK meets the following certification/standards. See page 3 of this evaluation board manual for the disclaimer and precautions.

4.1 EMC/EMI Standards

- FCC Notice (Class A)



This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

[NOTE] — This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/television technician for help.

- Innovation, Science and Economic Development Canada ICES-003 Compliance:
CAN ICES-3 (A)/NMB-3(A)

- CE Class A (EMC)



This product is herewith confirmed to comply with the requirements set out in the Council Directives on the Approximation of the laws of the Member States relating to Electromagnetic Compatibility Directive 2014/30/EU.

[Warning] — This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures to correct this interference.

- UKCA Class A (EMC)



This product is in conformity with the following relevant UK Statutory Instrument(s) (and its amendments): 2016 No. 1091 Electromagnetic Compatibility Regulations 2016.

[Warning] — This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures to correct this interference.

4.2 Material Selection, Waste, Recycling and Disposal Standards

- EU RoHS
- WEEE Directive (2012/19/EU) & The Waste Electrical and Electronic Equipment Regulations 2013



For customers in the UK & European Union the WEEE (Waste Electrical and Electronic Equipment) regulations put responsibilities on producers for the collection and recycling or disposal of electrical and electronic waste. Return of WEEE under these regulations is applicable in the UK and European Union.



This equipment (including all accessories) is not intended for household use. After use the equipment cannot be disposed of as household waste, and the WEEE must be treated, recycled and disposed of in an environmentally sound manner.

Renesas Electronics Europe GmbH can take back end of life equipment. Register for this service at:

<https://www.renesas.com/en/support/regional-customer-support/weee>

4.3 Safety Standards

- UL 94V-0

Appendix A Handling of Breakout and RGB-HDMI Adaptor

The SMARC Breakout Adaptor and SMARC RGB-HDMI Adaptor, shipped with this EVK, use Hirose Electronic [DF40C-50DP-0.4V\(51\)](#) connectors to connect to the SMARC Module – these must be handled with care.

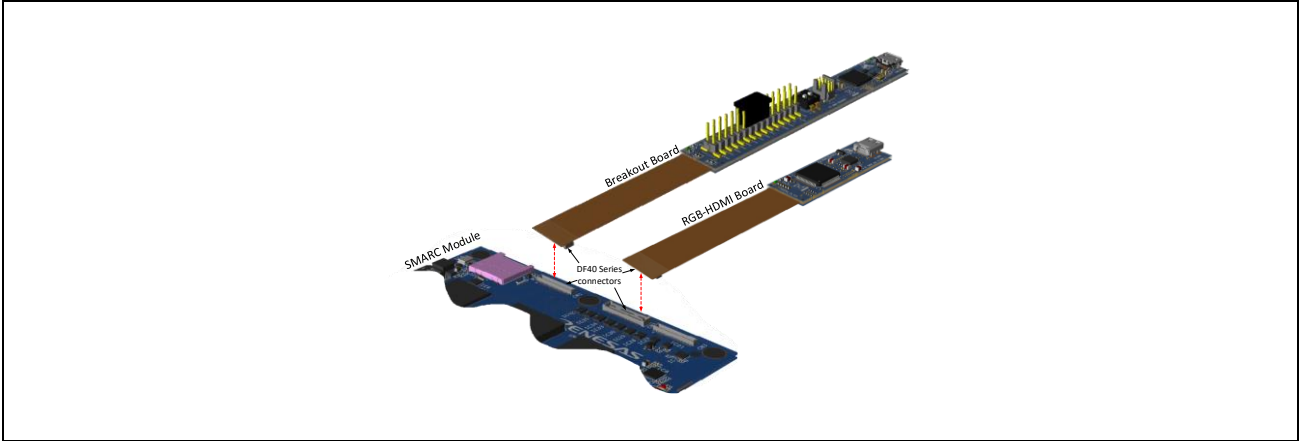


Figure A.1 Connection Between the G3L SMARC Module and Each Adaptor

Insertion: Follow the “[Handling Precautions for Connector Insertion](#)” provided by Hirose:

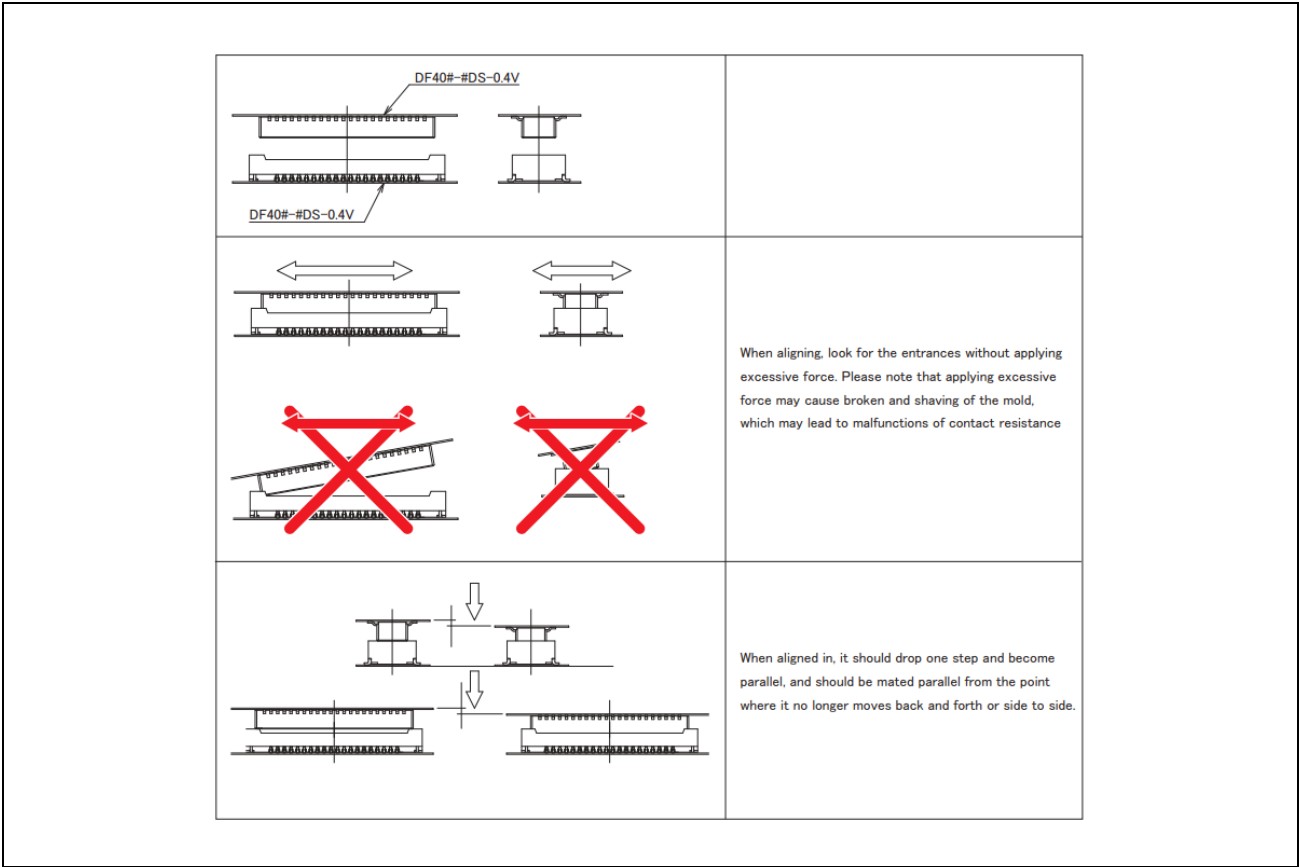


Figure A.2 Caution when Mating Breakout and RGB-HDMI Adaptor to Connector

Removal: To prevent possible damage, it is advisable that these boards are not removed once connected to the Module. However, if it is required, then these boards should be removed following the “[Handling Precautions for Connector Removal](#)” provided by Hirose:

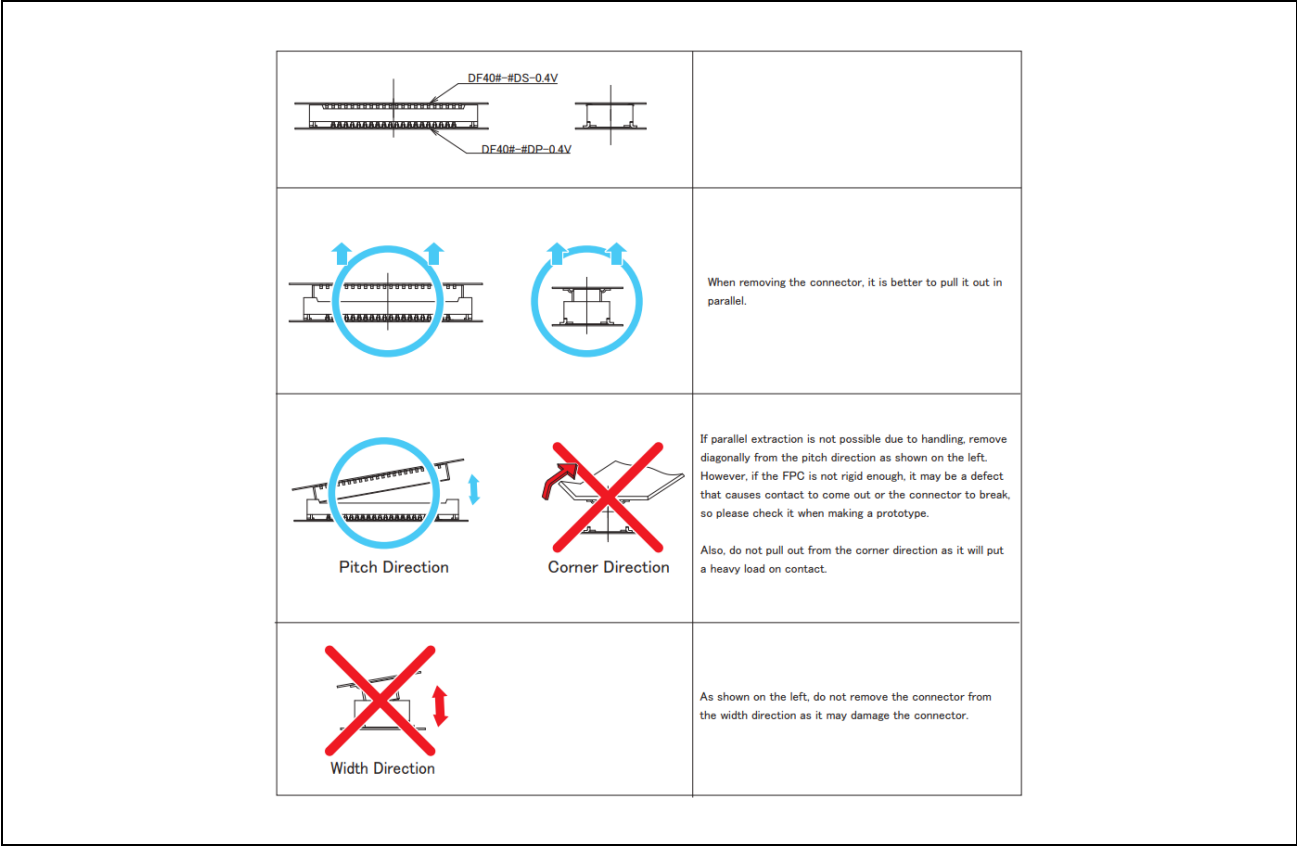


Figure A.3 Caution when Unmating Breakout and RGB-HDMI Adaptor from Connector

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		Page	Summary
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