User's Manual

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RX65W-A Group

User's Manual: Hardware

RENESAS 32-Bit MCU
RX Family／RX600 Series

Renesas Electronics
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.
This manual consists of the following sections.

- Overview
- I/O ports
- Multi-function pin controller (MPC)
- Boundary scan
- RF transceiver
- Electrical characteristics
- Points to note

For details on the CPU, system control, and peripheral functions, see RX65N Group, RX651 Group User's manual: Hardware. For details on the RF transceiver, see R9A06G062GNP Sub-GHz Transceiver User's Manual: Hardware.

Particular attention should be paid to the precautionary notes when using the manual. These notes can be found within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RX65W-A Group. Make sure to refer to the latest versions of these documents. The latest versions of the listed documents are available from the Renesas Electronics website.

Document Type	Description	Document Title	Document No.
User's manual: Hardware	Overview of the product, hardware specifications (I/O ports, multi-function pin controller, boundary scan, RF transceiver, and electrical characteristics), and points to note	RX65W-A Group User's manual: Hardware	This User's manual
	Hardware specifications including CPU, system control, and peripheral functions	RX65N Group, RX651 Group User's manual: Hardware	R01UH0590EJ
	Detailed descriptions of the RF transceiver	R9A06G062GNP Sub-GHz Transceiver User's Manual: Hardware	R02UH0006EJ
User's manual: Software	Detailed descriptions of the CPU and instruction set	RX Family RXv2 Instruction Set Architecture User's Manual: Software	R01US0071EJ
Flash Memory User's Manual: Hardware Interface	Detailed descriptions of the hardware interface of the flash memory	RX65N Group, RX651 Group Flash Memory User's Manual: Hardware Interface	R01UH0602EJ
Application Note	Notes on Printed Circuit Board Patterns	RX Family Hardware Design Guide	R01AN1411EJ
	Information on using peripheral functions and application examples Sample programs	Available from Renesas Electronics website.	
Renesas Technical Update	Preliminary report on the specifications of a product, document, etc.		

2. Notation of Numbers and Symbols

Each register description includes a bit chart, illustrating the arrangement of bits, and a table of bits, describing the meanings of the bit settings. The standard format and notation for bit charts and tables are described below.

X.X.X ... Register

Address(es): xxxx xxxxh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	...[1:0]		...4	—	—	—	...0
Value after reset:	x	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	...0	.....	0: ..... 1: Setting prohibited (3)	R/W (1)
b3 to b1	—	Reserved (2)	These bits are read as 0. The write value should be 0.	R/W
b4	...4	.....	0: 1:	R
b6, b5	...[1:0]	.....	0 0: ..... 0 1: ..... Settings other than above are prohibited. (3)	R/(W)*1
b7	—	Reserved	The read value is undefined. Writing to this bit has no effect.	R

(1) R/W: The bit or field is readable and writable.
R/(W): The bit or field is readable and writable. However, writing to this bit or field has some limitations. For details on the limitations, see the description or notes of respective registers.
R: The bit or field is readable. Writing to this bit or field has no effect.

(2) Reserved.
Use the specified value when writing to this bit or field; otherwise, the correct operation is not guaranteed.

(3) Setting prohibited. The correct operation is not guaranteed if such a setting is performed.

3. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communications Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input / Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Registers
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver / Transmitter
VCO	Voltage Controlled Oscillator

Contents

120-MHz 32-bit RX MCU, on-chip FPU, 240 DMIPS, 2-MB flash memory (supportive of the dual bank function), 640-KB SRAM, RF transceiver compliant to IEEE 802.15.4 and Wi-SUN®, various communications interfaces including Ethernet MAC, SD host interface, SD slave interface, and quad SPI, 12-bit A/D converter, RTC, Encryption functions

Features

■ 32-bit RXv2 CPU core

- Max. operating frequency: 120 MHz
  Capable of 240 DMIPS in operation at 120 MHz
- Single precision 32-bit IEEE-754 floating point
- Two types of multiply-and-accumulation unit (between memories and between registers)
- 32-bit multiplier (fastest instruction execution takes one CPU clock cycle)
- Divider (fastest instruction execution takes two CPU clock cycles)
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions: Ultra-compact code
- Supports the memory protection unit (MPU)
- JTAG and FINE (one-line) debugging interfaces

■ Low-power design and architecture

- Operation from a single 2.7- to 3.6-V supply
- Low power consumption: A product that supports all peripheral functions draws only 0.19 mA/MHz (Typ.).
- RTC is capable of operation from a dedicated power supply.
- Four low-power modes

■ On-chip code flash memory

- 2 Mbytes of ROM
- No wait cycles at up to 50 MHz or when the ROM cache is hit, one-wait state at up to 100 MHz, two-wait state at above 100 MHz
- User code is programmable by on-board programming.
- Programming/erasing as background operations (BGOs)
- A dual-bank structure allows exchanging the start-up bank.

■ On-chip data flash memory

- 32 Kbytes, reprogrammable up to 100,000 times
- Programming/erasing as background operations (BGOs)

■ On-chip SRAM, no wait states

- 640 Kbytes of SRAM (no wait states)
- 8 Kbytes of standby RAM (backup on deep software standby)

■ Data transfer

- DMACAa: 8 channels
- DTCb: 1 channel
- DMAC for the Ethernet controller: 1 channel

■ Reset and supply management

- Power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions

- External crystal resonator or internal PLL for operation at 8 to 24 MHz
- Internal 240-kHz LOCO and HOCO selectable from 16, 18, and 20 MHz
- 120-kHz clock for the IWDTa
- 48-MHz crystal resonator for the RF transceiver

■ Real-time clock

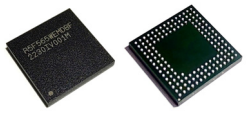
- Adjustment functions (30 seconds, leap year, and error)
- Real-time clock counting and binary counting modes are selectable
- Time capture function
  (for capturing times in response to event-signal input)

■ Independent watchdog timer

- 120-kHz (1/2 LOCO frequency) clock operation

■ Useful functions for IEC60730 compliance

- Oscillation-stoppage detection, frequency measurement, CRCA, IWDTa, self-diagnostic function for the A/D converter, etc.
- Register write protection function can protect values in important registers against overwriting.



PTBG0145KB-A 8 × 8 mm, 0.5-mm pitch

■ Various communications interfaces

- Single RF transceiver compliant to IEEE 802.15.4 and Wi-SUN®
  Covers 863 to 928 MHz, which includes the frequency bands of the various countries
  Supports SUN FSK and SUN OFDM
- Ethernet MAC (1 channel)
- Includes a PHY layer for the full-speed USB 2.0 function controller
- SCIg and SCIh with multiple functionalities (9 channels)
  Choose from among asynchronous mode, clock-synchronous mode, smart-card interface mode, simplified SPI, simplified I^2C, and extended serial mode.
- SCIi with 16-byte transmission and reception FIFOs (2 channels)
- I^2C bus interface for transfer at up to 1 Mbps (2 channels)
- Four-wire QSPI (1 channel) in addition to RSPIc (2 channels)
- SD host interface (1 channel) with a 1- or 4-bit SD bus for use with SD memory or SDIO
- SD slave interface (1 channel) with a 1- or 4-bit SD bus for use with SD host interface

■ Up to 24 extended-function timers

- 16-bit TPUa (5 channels), MTU3a (9 channels)
- 8-bit TMRa (4 channels), 16-bit CMT (4 channels), 32-bit CMTW (2 channels)

■ 12-bit A/D converter

- Two 12-bit units (4 channels for unit 0; 11 channels for unit 1)
- Self diagnosis, detection of analog input disconnection

■ Temperature sensor for measuring temperature within the chip

■ Encryption functions

- Trusted Secure IP (TSIP)

■ Up to 51 pins for general I/O ports

- 5-V tolerance, open drain, input pull-up, switchable driving ability

■ Operating temp. range

- –40°C to +85°C

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline.

Table 1.1 Outline of Specifications (1/7)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers • Basic instructions: 75 • Floating-point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	Code flash memory	• Capacity: 2 Mbytes • 50 MHz ≤ No-wait cycle access 100 MHz ≤ 1-wait cycle access 100 MHz > 2-wait cycle access • Instructions hitting the ROM cache or operand = 120 MHz: No-wait access • On-board programming: Four types • Instructions are executable only for the program stored in the TM target area by using the Trusted Memory (TM) function and protection against data reading is realized. • A dual-bank structure allows programming during reading or exchanging the start-up areas
	Data flash memory	• Capacity: 32 Kbytes • Programming/erasing: 100,000 times
	Unique ID	• 16-byte unique ID for the device
	RAM	• Capacity: 640 Kbytes RAM: 256 Kbytes Expansion RAM: 384 Kbytes • 120 MHz, no-wait access
	Standby RAM	• Capacity: 8 Kbytes • Operation synchronized with PCLKB: Up to 60 MHz, two-cycle access
Operating modes		• Operating modes by the mode-setting pins at the time of release from the reset state Single-chip mode Boot mode (for the SCI interface) Boot mode (for the USB interface) Boot mode (for the FINE interface) • Endian selectable

Table 1.1 Outline of Specifications (2/7)

Classification	Module/Function	Description
Clock	Clock generation circuit	• Main clock oscillator, sub clock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • The peripheral module clocks can be set to frequencies above that of the system clock. • Main-clock oscillation stoppage detection • Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), and flash-IF clock (FCLK) The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 120 MHz Peripheral modules of MTU3, RSPI, SCIi, ETHERC, and EDMAC run in synchronization with PCLKA, which operates at up to 120 MHz. Other peripheral modules run in synchronization with PCLKB: Up to 60 MHz ADCLK in the S12AD (unit 0) runs in synchronization with PCLKC: Up to 60 MHz ADCLK in the S12AD (unit 1) runs in synchronization with PCLKD: Up to 60 MHz Flash IF run in synchronization with the flash-IF clock (FCLK): Up to 60 MHz • Multiplication is possible with using the high-speed on-chip oscillator (HOCO) as a reference clock of the PLL circuit
Reset		Nine types of reset • RES# pin reset: Generated when the RES# pin is driven low. • Power-on reset: Generated when the RES# pin is driven high and VCC = AVCC0 = AVCC1 rises. • Voltage-monitoring 0 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Voltage-monitoring 1 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Voltage-monitoring 2 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Deep software standby reset: Generated in response to an interrupt to trigger release from deep software standby. • Independent watchdog timer reset: Generated when the independent watchdog timer underflows, or a refresh error occurs. • Watchdog timer reset: Generated when the watchdog timer underflows, or a refresh error occurs. • Software reset: Generated by register setting.
Power-on reset		If the RES# pin is at the high level when power is supplied, an internal reset is generated. After VCC = AVCC0 = AVCC1 has exceeded the voltage detection level and the specified period has elapsed, the reset is cancelled.
Voltage detection circuit (LVDA)		Monitors the voltage being input to the VCC = AVCC0 = AVCC1 pins and generates an internal reset or interrupt. • Voltage detection circuit 0 Capable of generating an internal reset The option-setting memory can be used to select enabling or disabling of the reset. Voltage detection level: Selectable from three different levels (2.94 V, 2.87 V, 2.80 V) • Voltage detection circuits 1 and 2 Voltage detection level: Selectable from three different levels (2.99 V, 2.92 V, 2.85 V) Digital filtering (1/2, 1/4, 1/8, and 1/16 LOCO frequency) Capable of generating an internal reset • Two types of timing are selectable for release from reset An internal interrupt can be requested. • Detection of voltage rising above and falling below thresholds is selectable. • Maskable or non-maskable interrupt is selectable Voltage detection monitoring Event linking
Low power consumption	Low power consumption function	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
	Battery backup function	• When the voltage on the VCC pin drops, battery power from the VBATT pin is supplied to keep the real-time clock (RTC) operating.
Interrupt	Interrupt controller (ICUB)	• Peripheral function interrupts: 262 sources • External interrupts: 15 (pins IRQ0 to IRQ14) • Software interrupts: 2 sources • Non-maskable interrupts: 7 sources • Sixteen levels specifiable for the order of priority • Method of interrupt source selection: The interrupt vectors consist of 256 vectors (128 sources are fixed. The remaining 128 vectors are selected from among the other 123 sources.)

Table 1.1 Outline of Specifications (3/7)

Classification	Module/Function	Description
DMA	DMA controller (DMACAa)	• 8 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCb)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Request sources: External interrupts and interrupt requests from peripheral functions • Sequence transfer
I/O ports	Programmable I/O ports	• Total number of pins: 73 I/O pins: 50 Input pin: 1 Pull-up resistors: 50 Open-drain outputs: 50 5-V tolerance: 8
Event link controller (ELC)		• Event signals such as interrupt request signals can be interlinked with the operation of functions such as timer counting, eliminating the need for intervention by the CPU to control the functions. • 83 internal event signals can be freely combined for interlinked operation with connected functions. • Event signals from peripheral modules can be used to change the states of output pins (of ports B and E). • Changes in the states of pins (of ports B and E) being used as inputs can be interlinked with the operation of peripheral modules.
Timers	16-bit timer pulse unit (TPUa)	• (16 bits × 5 channels) × 1 unit • Maximum of 12 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel • Input capture/output compare function • Output of PWM waveforms in up to 15 phases in PWM mode • Support for buffered operation, phase-counting mode (two phase encoder input) and cascade-connected operation (32 bits × 2 channels) depending on the channel. • Capable of generating conversion start triggers for the A/D converters • Digital filtering of signals from the input capture pins • Event linking by the ELC
	Multifunction timer pulse unit (MTU3a)	• 9 channels (16 bits × 8 channels, 32 bits × 1 channel) • Maximum of 24 pulse-input/output and 3 pulse-input possible • Select from among 14 counter-input clock signals for each channel (PCLKA/1, PCLKA/2, PCLKA/4, PCLKA/8, PCLKA/16, PCLKA/32, PCLKA/64, PCLKA/256, PCLKA/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, MTIOC1A) 14 of the signals are available for channel 0, 11 are available for channels 1, 3, 4, 6 to 8, 12 are available for channel 2, and 10 are available for channel 5. • Input capture function • 39 output compare/input capture registers • Counter clear operation (synchronous clearing by compare match/input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous register input/output by synchronous counter operation • Buffered operation • Support for cascade-connected operation • 43 interrupt sources • Automatic transfer of register data • Pulse output mode Toggle/PWM/complementary PWM/reset-synchronized PWM • Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffer configuration • Reset synchronous PWM mode Three phases of positive and negative PWM waveforms can be output with desired duty cycles. • Phase-counting mode: 16-bit mode (channels 1 and 2); 32-bit mode (channels 1 and 2) • Counter functionality for dead-time compensation

Table 1.1 Outline of Specifications (4/7)

Classification	Module/Function	Description
Timers	Multifunction timer pulse unit (MTU3a)	• Generation of triggers for A/D converter conversion • A/D converter start triggers can be skipped • Digital filter function for signals on the input capture and external counter clock pins • Event linking by the ELC
	Port output enable 3 (POE3a)	• Control of the high-impedance state of the MTU3 waveform output pins • 5 pins for input from signal sources: POE0#, POE4#, POE8#, POE10#, POE11# • Initiation on detection of short-circuited outputs (detection of simultaneous PWM output to the active level) • Initiation by oscillation-stoppage detection or software • Additional programming of output control target pins is enabled
	8-bit timers (TMRb)	• (8 bits × 2 channels) × 2 units • Select from among seven internal clock signals (PCLKB/1, PCLKB/2, PCLKB/8, PCLKB/32, PCLKB/64, PCLKB/1024, PCLKB/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Generation of triggers for A/D converter conversion • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12 • Event linking by the ELC
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Event linking by the ELC
	Compare match timer W (CMTW)	• (32 bits × 1 channel) × 2 units • Compare-match, input-capture input, and output-comparison output are available. • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events. • Event linking by the ELC
	Realtime clock (RTCd)*2	• Clock sources: Main clock, sub clock • Selection of the 32-bit binary count in time count/second unit possible • Clock and calendar functions • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Battery backup operation • Time-capture facility for three values • Event linking by the ELC
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLKB/4, PCLKB/64, PCLKB/128, PCLKB/512, PCLKB/2048, PCLKB/8192)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: IWDT-dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256 • Window function: The positions where the window starts and ends are specifiable (the window defines the timing with which refreshing is enabled and disabled). • Event linking by the ELC
Communication function	RF Transceiver	• Single RF transceiver compliant to IEEE 802.15.4 and Wi-SUN® • Covers 863 to 928 MHz, which includes the frequency bands of the various countries • Data rates for SUN FSK: 10, 20, 50, 100, 150, 200 kbps • Data rates for SUN OFDM: Option 1: 100, 200, 400, 800, 1200, 1600, 2400 kbps Option 2: 50, 100, 200, 400, 600, 800, 1200 kbps Option 3: 25, 50, 100, 200, 300, 400, 600 kbps Option 4: 12.5, 25, 50, 100, 150, 200, 300 kbps • Transmission power: +15 dBm for SUN FSK, and +11 dBm for SUN OFDM

Table 1.1 Outline of Specifications (5/7)

Classification	Module/Function	Description
Communication function	Ethernet controller (ETHERC)	• Input and output of Ethernet/IEEE 802.3 frames • Transfer at 10 or 100 Mbps • Full- and half-duplex modes • RMII (Reduced Media Independent Interface) as defined in IEEE 802.3u • Detection of Magic Packets™*1 or output of a “wake-on-LAN” signal (WOL) • Compliance with flow control as defined in IEEE 802.3x standards
	DMA controller for Ethernet controller (EDMACa)	• Alleviation of CPU load by the descriptor control method • Transmission FIFO: 2 Kbytes; Reception FIFO: 2 Kbytes
	USB 2.0 FS function module (USBb)	• Includes a UDC (USB Device Controller) and transceiver for USB 2.0 FS • One port • Compliance with the USB 2.0 specification • Transfer rate: Full speed (12 Mbps) • Both self-powered mode and bus-powered mode are supported • Incorporates 2 Kbytes of RAM as a transfer buffer • External pull-up and pull-down resistors are not required
	Serial communications interfaces (SCIg, SCIh, SCIi)	• 11 channels (SCIg: 8 channels + SCIh: 1 channel + SCIi: 2 channels) • SCIg, SCIh, SCIi Serial communications modes: Asynchronous, clock synchronous (not available in SCI2 or SCI3), and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Start-bit detection: Level or edge detection is selectable. Simple I^2C Simple SPI (not available in SCI2, SCI3, or SCI12) 9-bit transfer mode Bit rate modulation Double-speed mode • SCIg, SCIh Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 Event linking by the ELC (only on channel 5) • SCIh Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format • SCIi Data can be transmitted or received in sequence by the 16-byte FIFO buffers of the transmission and reception unit
	I^2C bus interface (RIICa)	• 2 channels (only channel 0 can be used in fast-mode plus) Communication formats I^2C bus format/SMBus format Supports the multi-master Max. transfer rate: 1 Mbps (channel 0) • Event linking by the ELC
	Serial peripheral interface (RSPIc)	• 2 channels • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) Transit/receive data can be swapped in byte units • Buffered structure Double buffers for both transmission and reception • RSPCK can be stopped with the receive buffer full for master reception. • Event linking by the ELC

Table 1.1 Outline of Specifications (6/7)

Classification	Module/Function	Description
Communication function	Quad serial peripheral interface (QSPI)	• 1 channel • Connectable with serial flash memory equipped with multiple input and output lines (i.e. for single, dual, or quad operation) • Programmable bit length and selectable active sense and phase of the clock signal • Sequential execution of transfer • LSB or MSB first is selectable
SD host interface (SDHI)		• 1 channel • Transfer speed: Supports high-speed mode (25 MB/s) and default speed mode (12.5 MB/s) • One interface for SD memory and I/O cards (supporting 1- and 4-bit SD buses) • SD specifications Part 1: Physical Layer Specification Ver. 3.01 compliant (DDR not supported) Part E1: SDIO Specification Ver. 3.00 • Error checking: CRC7 for commands and CRC16 for data • Interrupt requests: Card access interrupt, SDIO access interrupt, card detection interrupt, SD buffer access interrupt • DMA transfer requests: SD_BUF write and SD_BUF read • Support for card detection and write protection
SD slave interface (SDSI)		• 1 channel • Compliant with the SDIO Card Specification Ver.2.00 (CSA is not supported) • 1-bit SD/4-bit SD/SPI mode • SDIO Proprietary command is supported • SD/SPI Mandatory command is supported • Interrupt requests: 6
12-bit A/D converter (S12ADFa)		• 12 bits × 2 units (unit 0: 4 channels; unit 1: 11 channels) • 12-bit resolution (switchable between 8, 10, and 12 bits) • Conversion time 0.48 µs per channel (for 12-bit conversion) 0.45 µs per channel (for 10-bit conversion) 0.42 µs per channel (for 8-bit conversion) • Operating mode Scan mode (single scan mode, continuous scan mode, or 3 group scan mode) Group priority control (only for 3 group scan mode) • Sample-and-hold function Common sample-and-hold circuit included In addition, channel-dedicated sample-and-hold function (3 channels: in unit 0 only) included • Sampling variable Sampling time can be set up for each channel. • Digital comparison Method: Comparison to detect voltages above or below thresholds and window comparison Measurement: Comparison of two results of conversion or comparison of a value in the comparison register and a result of conversion • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (unit 0: VREFL0, VREFH0 × 1/2, VREFH0; unit 1: AVSS1, AVCC1 × 1/2, AVCC1) • Double trigger mode (A/D conversion data duplicated) • Detection of analog input disconnection • Three ways to start A/D conversion Software trigger, timer (MTU3, TMR, TPU) trigger, external trigger • Event linking by the ELC
Temperature sensor		• 1 channel • Relative precision: ± 1°C • The voltage of the temperature is converted into a digital value by the 12-bit A/D converter (unit 1).

Table 1.1 Outline of Specifications (7/7)

Classification	Module/Function	Description
Safety	Memory protection unit (MPU)	• Protection area: Eight areas (max.) can be specified in the range from 0000 0000h to FFFF FFFFh. • Minimum protection unit: 16 bytes • Reading from, writing to, and enabling the execution access can be specified for each area. • An access exception occurs when the detected access is not in the permitted area.
	Trusted Memory (TM) Function	• Programs in the TM target area in the code flash memory are protected against reading • Instruction fetching by the CPU is the only form of access to these areas when the TM function is enabled.
	Register write protection function	• Protects important registers from being overwritten for in case a program runs out of control.
	CRC calculator (CRCA)	• Generation of CRC codes for 8-/32-bit data 8-bit data Selectable from the following three polynomials $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$ 32-bit data Selectable from the following two polynomials $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$, $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
	Main clock oscillation stop detection	• Main clock oscillation stop detection: Available
	Clock frequency accuracy measurement circuit (CAC)	• Monitors the clock output from the main clock oscillator, sub-clock oscillator, low- and high-speed on-chip oscillators, IWDT-dedicated on-chip oscillator, and PCLKB, and generates interrupts when the setting range is exceeded.
	Data operation circuit (DOC)	• The function to compare, add, or subtract 16-bit data
Encryption function	Trusted Secure IP (TSIP)	• Security algorithm Common key encryption: AES (compliant with NIST FIPS PUB 197), 3DES, ARC4 Non-common key encryption: RSA • Other features TRNG (true-random number generator) Hash value generation: SHA1, SHA224, SHA256, GHASH Prevention from illicit copying of a key
Operating frequency		Up to 120 MHz
Power supply voltage		VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0, V_{BATT} = 2.0 to 3.6 V
Operating temperature		–40 to +85°C
Package		145-pin TFBGA (PTBG0145KB-A)
Debugging interface		JTAG and FINE interfaces

Note 1. Magic Packet™ is a registered trademark of Advanced Micro Devices, Inc.
Note 2. When the realtime clock is not used, initialize the registers in the time clock according to description in section 31.6.7, Initialization Procedure When the Realtime Clock is Not to be Used in the RX65N Group, RX651 Group User's Manual: Hardware.

1.2 Comparison of Functions among Products

Table 1.2 lists the comparison of functions among products.
For details on the CPU, system control, and peripheral functions, see RX65N Group, RX651 Group User's manual: Hardware. For details on the RF transceiver, see R9A06G062GNP Sub-GHz Transceiver User's Manual: Hardware.

Table 1.2 Comparison of Functions among Products (1/2)

Classification	Function	Product Part Number			
		RX65N (R5F565NEHDFC)	RX651 (R5F5651EDDFC)	RX65W-A (R5F565WEADBF)	RX65W-A (R5F565WEMDBF)
Code Flash Memory	Code Flash Memory Capacity	2 Mbytes			
	Dual bank function	Available			
	BGO function	Available			
Data Flash Memory		32 Kbytes			
RAM		640 Kbytes (256 Kbytes + 384 Kbytes of expansion RAM)			
External bus	External bus width	32/16/8 bits		Not available	
	SDRAM area controller	Available		Not available	
External interrupts		NMI, IRQ0 to IRQ15		NMI, IRQ0 to IRQ14	
DMA	DMA controller	Ch. 0 to 7			
	Data transfer controller	Available			
	EXDMA controller	Ch. 0 and 1		Not available	
Timers	16-bit timer pulse unit	Ch. 0 to 5		Ch. 0, 1, 3 to 5	
	Multi-function timer pulse unit 3	Ch. 0 to 8			
	Port output enable 3	Available			
	Programmable pulse generator	Ch. 0 and 1		Not available	
	8-bit timers	Ch. 0 to 3			
	Compare match timer	Ch. 0 to 3			
	Compare match timer W	Ch. 0 and 1			
	Realtime clock	Available			
	Watchdog timer	Available			
	Independent watchdog timer	Available			
Communication function	RF transceiver	Not available		Available	
	Ethernet controller	Ch. 0	Not available	Ch. 0 (only for RMII)	Not available
	DMA Controller for the Ethernet Controller	Ch. 0	Not available	Ch. 0	Not available
	USB 2.0 FS host/function module	Ch. 0		Ch. 0 (only supports the function controller)	
	Serial communications interfaces (SCIg)	Ch. 0 to 9		Ch. 1 to 6, 8, and 9 (clock synchronous mode and simple SPI bus mode are not available in ch. 2 and 3)	
	Serial communications interfaces (SCIh)	Ch. 12		Ch. 12 (simple SPI bus mode is not available)	
	Serial communications interfaces (SCIi)	Ch. 10 and 11			
	I^2C bus interfaces	Ch. 0 to 2		Ch. 0 and 2	
	Serial peripheral interface	Ch. 0 to 2		Ch. 0 and 1	
	CAN module	Ch. 0 and 1		Not available	
	Quad serial peripheral interface	Ch. 0			

Table 1.2 Comparison of Functions among Products (2/2)

Classification	Function	Product Part Number			
		RX65N (R5F565NEHDFC)	RX651 (R5F5651EDDFC)	RX65W-A (R5F565WEADBF)	RX65W-A (R5F565WEMDBF)
Communication function	SD host interface	Available		Available	Not available
	SD slave interface	Available		Available	Not available
	MMC host interface	Available		Not available	
	Parallel data capture unit	Available		Not available	
Graphics	Graphic-LCD controller	Available		Not available	
	2D drawing engine	Available		Not available	
12-bit A/D converter		AN000 to 007 (unit 0: 8 channels)		AN000 to 003 (unit 0: 4 channels)	
		AN100 to 120 (unit 1: 21 channels)		AN100, 102 to 107, 110 to 113 (unit 1: 11 channels)	
12-bit D/A converter		Ch. 0 and 1		Not available	
Temperature sensor		Available			
Safety	Memory-protection unit (MPU)	Available			
	Trusted memory (TM) function	Available			
	Register write protection function	Available			
	CRC calculator	Available			
	Main clock oscillation stop detection	Available			
	Clock frequency accuracy measurement circuit (CAC)	Available			
	Data operation circuit (DOC)	Available			
Encryption	Trusted Secure IP	Available	Not available	Available	Not available
Event link controller		Available			
Off-board programming (parallel programmer mode)		Available		Not available	

1.3 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	ETHERC	SDHI/SDSI	Operating tempera-ture (°C)
RX65W-A	R5F565WEADBF	PTBG0145KB-A	2 M	640 K	32 K	120 MHz	Available	Available	Available	–40 to +85
	R5F565WEMDBF						Not available	Not available	Not available	

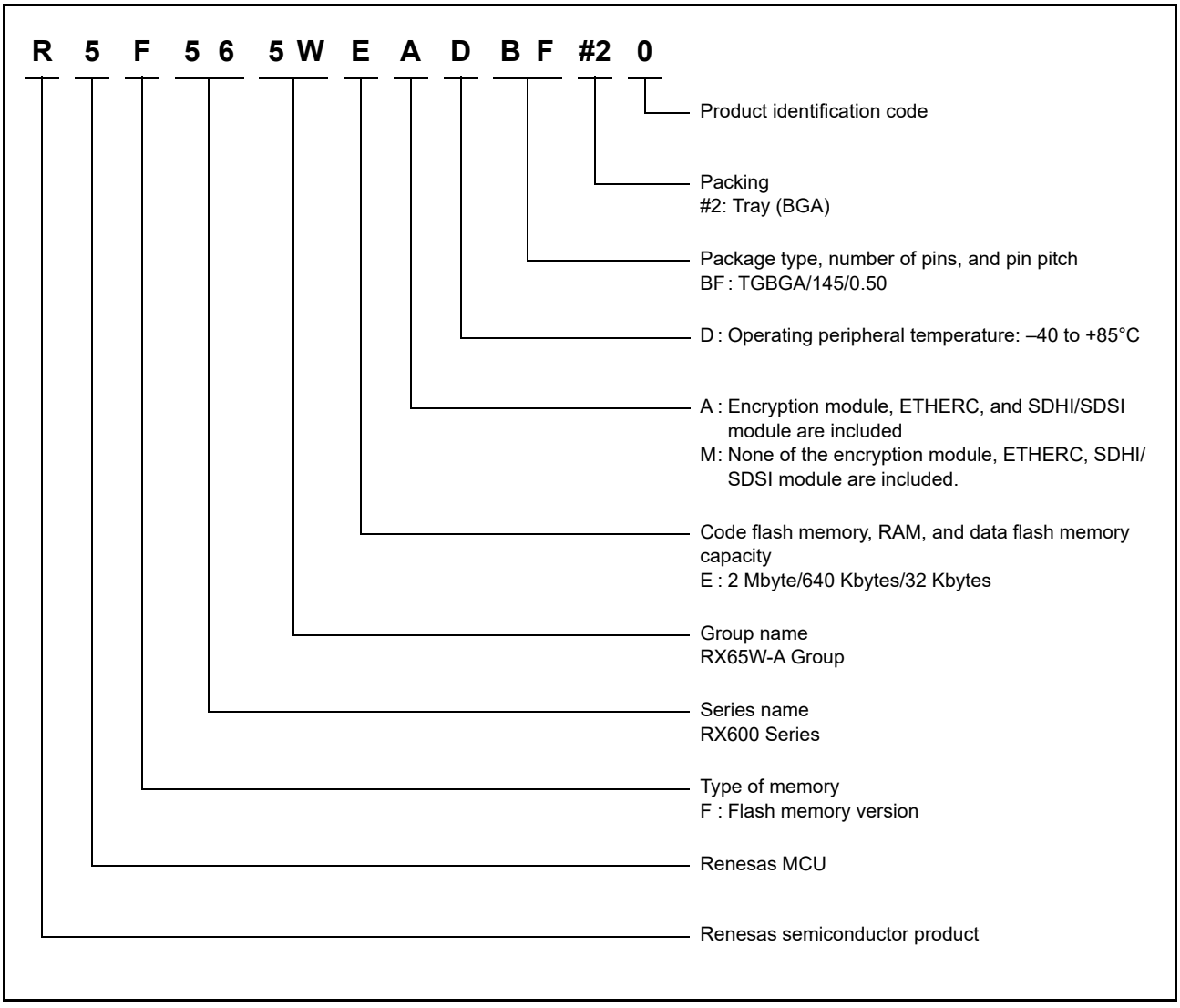


Figure 1.1 How to Read the Product Part Number

1.4 Block Diagram

Figure 1.2 shows a block diagram.

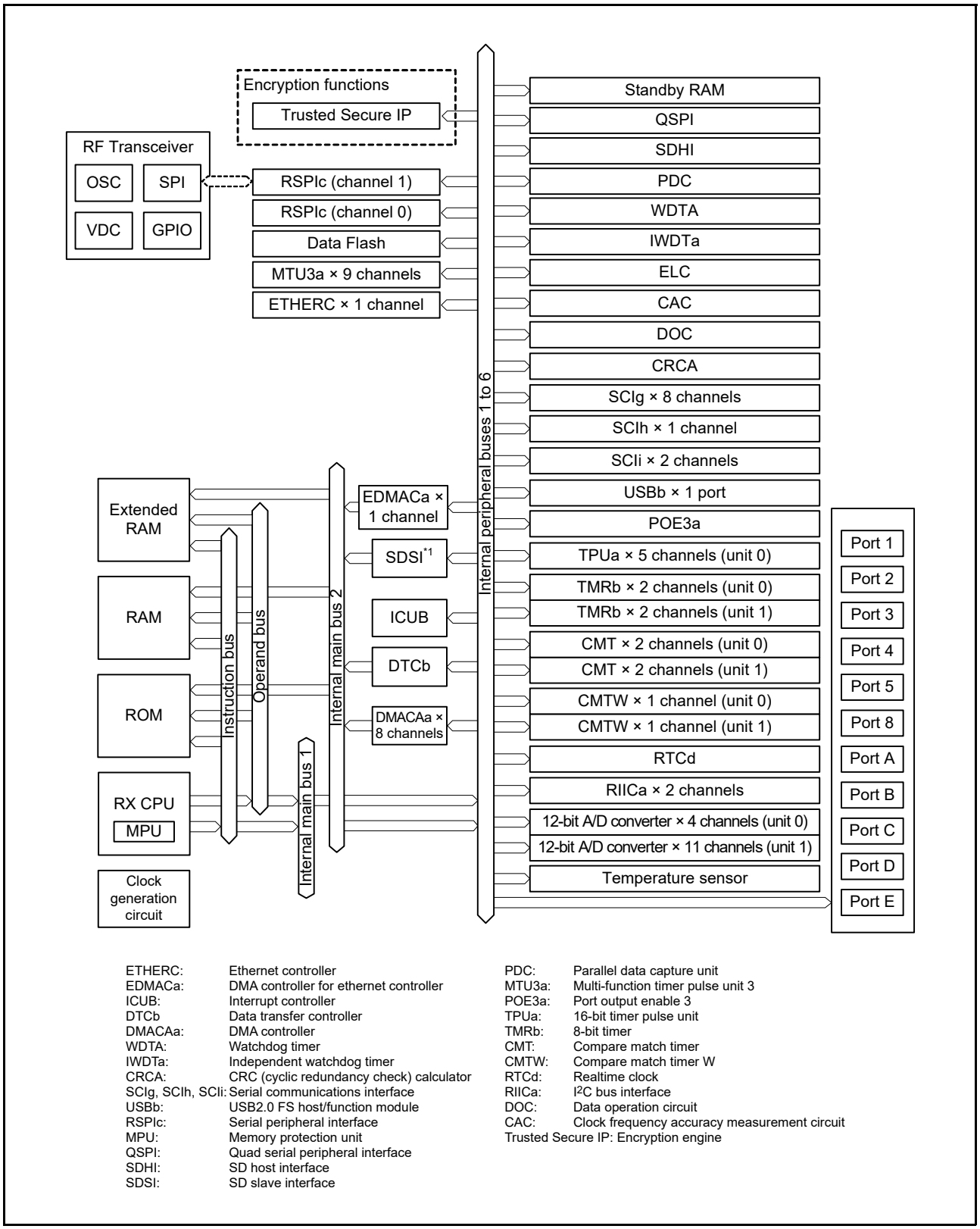


Figure 1.2 Block Diagram

1.5 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/6)

Classifications	Pin Name	I/O	Description
Digital power supply	VCC	Input	Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VCL	Input	Connect this pin to VSS via a 0.22-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin for the digital circuit and RF transceiver. Connect it to the system power supply (0 V).
	VBATT	Input	Backup power pin
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCOUT	Output	Input/output pins for the sub clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCIN	Input	
Clock frequency accuracy measurement	CACREF	Input	Reference clock input pin for the clock frequency accuracy measurement circuit
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation.
	UB	Input	USB boot mode enable pin
	UPSEL	Input	Selects the power supply method in USB boot mode. The low level selects self-powered mode and the high level selects bus-powered mode.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
	BSCANP	Input	Boundary scan enable pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low.
On-chip emulator	FINED	I/O	Fine interface pin
	TRST#	Input	On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ2 to IRQ7, IRQ11 to IRQ14, IRQ0-DS, IRQ1-DS, IRQ4-DS to IRQ11-DS	Input	Maskable interrupt request pins
Multi-function timer pulse unit 3	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins

Table 1.4 Pin Functions (2/6)

Classifications	Pin Name	I/O	Description
Multi-function timer pulse unit 3	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins
	MTIOC6A, MTIOC6C	I/O	The TGRA6 and TGRC6 input capture input/output compare output/PWM output pins
	MTIOC7A, MTIOC7B	I/O	The TGRA7 and TGRB7 input capture input/output compare output/PWM output pins
	MTIOC8A, MTIOC8B, MTIOC8C, MTIOC8D	I/O	The TGRA8 to TGRD8 input capture input/output compare output/PWM output pins
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for external clock signals or for phase counting mode clock signals
Port output enable 3	POE0#, POE4#, POE8#, POE10#, POE11#	Input	Input pins for request signals to place the MTU in the high impedance state
16-bit timer pulse unit	TIOCB0, TIOCD0	I/O	The TGRB0 and TGRD0 input capture input/output compare output/PWM output pins
	TIOCA1, TIOCB1	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins
	TIOCA3, TIOCB3, TIOCC3, TIOCD3	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins
	TIOCA4, TIOCB4	I/O	The TGRA4 and TGRB4 input capture input/output compare output/PWM output pins
	TIOCA5, TIOCB5	I/O	The TGRA5 and TGRB5 input capture input/output compare output/PWM output pins
	TCLKB, TCLKC, TCLKD	Input	Input pins for external clock signals or for phase counting mode clock signals
8-bit timer	TMO0 to TMO3	Output	Compare match output pins
	TMCI0 to TMCI3	Input	Input pins for external clocks to be input to the counter
	TMRI0 to TMRI3	Input	Input pins for the counter reset
Compare match timer W	TIC0 to TIC3	Input	Input pins for CMTW
	TOC0 to TOC2	Output	Output pins for CMTW
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK1, SCK4 to SCK6, SCK8, SCK9	I/O	Input/output pins for the clock
	RXD1 to RXD6, RXD8, RXD9	Input	Input pins for received data
	TXD1 to TXD6, TXD8, TXD9	Output	Output pins for transmitted data
	CTS1#, CTS3# to CTS6#, CTS8#, CTS9#	Input	Input pins for controlling the start of transmission and reception
	RTS1#, RTS3# to RTS6#, RTS8#, RTS9#	Output	Output pins for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL1 to SSCL6, SSCL8, SSCL9	I/O	Input/output pins for the I^2C clock
	SSDA1 to SSDA6, SSDA8, SSDA9	I/O	Input/output pins for the I^2C data
	• Simple SPI mode		
	SCK1, SCK4 to SCK6, SCK8, SCK9	I/O	Input/output pins for the clock
	SMISO1, SMISO4 to SMISO6, SMISO8, SMISO9	I/O	Input/output pins for slave transmission of data
	SMOSI1, SMOSI4 to SMOSI6, SMOSI8, SMOSI9	I/O	Input/output pins for master transmission of data
	SS1#, SS4# to SS6#, SS8#, SS9#	Input	Chip-select input pins

Table 1.4 Pin Functions (3/6)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	• Simple I2C mode		
	SSCL12	I/O	Input/output pin for the I2C clock
	SSDA12	I/O	Input/output pin for the I2C data
	• Extended serial mode		
	RXDX12	Input	Input pin for received data
	TXDX12	Output	Output pin for transmitted data
	SIOX12	I/O	Input/output pin for received or transmitted data
Serial communications interface (SCIi)	• Asynchronous mode/clock synchronous mode		
	SCK10 and SCK11	I/O	Input/output pin for the clock
	RXD10 and RXD11	Input	Input pin for received data
	TXD10 and TXD11	Output	Output pin for transmitted data
	CTS10# and CTS11#	Input	Input pin for controlling the start of transmission and reception
	RTS10# and RTS11#	Output	Output pin for controlling the start of transmission and reception
	• Simple I2C mode		
	SSCL10 and SSCL11	I/O	Input/output pin for the I2C clock
	SSDA10 and SSDA11	I/O	Input/output pin for the I2C data
	• Simple SPI mode		
	SCK10 and SCK11	I/O	Input/output pin for the clock
	SMISO10 and SMISO11	I/O	Input/output pin for slave transmission of data
	SMOSI10 and SMOSI11	I/O	Input/output pin for master transmission of data
	SS10# and SS11#	Input	Chip-select input pin
I2C bus interface	SCL0[FM+], SCL2-DS	I/O	Input/output pins for clocks. Bus can be directly driven by the N-channel open drain
	SDA0[FM+], SDA2-DS	I/O	Input/output pins for data. Bus can be directly driven by the N-channel open drain
Ethernet controller	REF50CK0	Input	50-MHz reference clocks. These pins input reference signals for transmission/reception timings in RMII mode.
	RMII0_CRS_DV	Input	Indicate that there are carrier detection signals and valid receive data on RMII0_RXD1 and RMII0_RXD0 in RMII mode.
	RMII0_TXD0, RMII0_TXD1	Output	2-bit transmit data in RMII mode
	RMII0_RXD0, RMII0_RXD1	Input	2-bit receive data in RMII mode
	RMII0_TXD_EN	Output	Output pins for data transmit enable signals in RMII mode
	RMII0_RX_ER	Input	Indicate an error has occurred during reception of data in RMII mode.
	ET0_LINKSTA	Input	Input link status from the PHY-LSI.
	ET0_WOL	Output	Receive Magic packets.
	ET0_MDC	Output	Output reference clock signals for information transfer via ET0_MDIO.
	ET0_MDIO	I/O	Input or output bidirectional signals for exchange of management information between this MCU and the PHY-LSI.

Table 1.4 Pin Functions (4/6)

Classifications	Pin Name	I/O	Description
USB 2.0 function module	VCC_USB	Input	Power supply pin
	VSS_USB	Input	Ground pin
	USB0_DP	I/O	Input or output USB transceiver D+ data.
	USB0_DM	I/O	Input or output USB transceiver D- data.
	USB0_VBUS	Input	USB cable connection/disconnection detection input pin
Serial peripheral interface	RSPCKA/RSPCKB	I/O	Clock input/output pins
	MOSIA/MOSIB	I/O	Input or output data output from the master
	MISOA/MISOB	I/O	Input or output data output from the slave
	SSLA0/SSLB0	I/O	Input or output pins for slave selection
	SSLA1/SSLB1, SSLA2/SSLB2, SSLB3	Output	Output pins for slave selection
Quad serial peripheral interface	QSPCLK	Output	QSPI clock output pins
	QSSL	Output	QSPI slave output pins
	QMO, QIO0	I/O	Master transmit data/data 0
	QMI, QIO1	I/O	Master input data/data 1
	QIO2, QIO3	I/O	Data 2, data 3
SD host interface	SDHI_CLK	Output	SD clock output pins
	SDHI_CMD	I/O	SD command output, response input signal pins
	SDHI_D0, SDHI_D1, SDHI_D2, SDHI_D3	I/O	SD data bus pins
	SDHI_CD	Input	SD card detection pin
	SDHI_WP	Input	SD write-protect signal
SD slave interface	SDSI_CLK	Input	SD clock input pins
	SDSI_CMD	I/O	SD command input, response output signal pins
	SDSI_D0, SDSI_D1, SDSI_D2, SDSI_D3	I/O	SD data bus pins
Realtime clock	RTCOUT	Output	Output pin for 1-Hz/64-Hz clock
	RTCIC0, RTCIC1	Input	Time capture event input pins
12-bit A/D converter	AN000 to AN003, AN100, AN102 to AN107, AN110 to AN113	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0#, ADTRG1#	Input	Input pins for the external trigger signals that start the A/D conversion
	ANEX0	Output	Extended analog output pin
	ANEX1	Input	Extended analog input pin
Analog power supply	AVCC0*1	Input	Analog voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VCC power supply. Connect the pin to AVSS0 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	AVSS0*1	Input	Analog ground pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VSS ground power supply. Connect the pin to AVCC0 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter (unit 0). Connect this pin to VSS if the 12-bit A/D converter is not to be used.

Table 1.4 Pin Functions (5/6)

Classifications	Pin Name	I/O	Description
Analog power supply	AVCC1*1	Input	Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog voltage to the temperature sensor. Connect this pin to a branch from the VCC power supply. Connect the pin to AVSS1 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	AVSS1*1	Input	Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog ground voltage to the temperature sensor. Connect this pin to a branch from the VSS ground power supply. Connect the pin to AVCC1 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
I/O ports	P12, P13, P16, P17	I/O	4-bit input/output pins
	P26, P27	I/O	2-bit input/output pins
	P30, P31, P34 to P37	I/O	6-bit input/output pins (P35: input pin)
	P40 to P43	I/O	4-bit input/output pins
	P53	I/O	1-bit input/output pins
	P80 to P82	I/O	3-bit input/output pins
	PA1 to PA4	I/O	4-bit input/output pins
	PB0 to PB7	I/O	8-bit input/output pins
	PC0, PC1, PC4 to PC7	I/O	6-bit input/output pins
	PD2 to PD7	I/O	6-bit input/output pins
	PE0 to PE2, PE4 to PE7	I/O	7-bit input/output pins
RF Transceiver	SIN	Input (D)	Serial input
	SOUT	Output (D)	Serial output
	SCLK	Input (D)	Serial clock
	SEN	Input (D)	Serial enable
	VREG_DIG	Output (A)	Internally regulated analog 1.1-V supply output voltage for digital circuits
	GPIO0 to GPIO12	I/O (D)	General-purpose digital I/O pins 0 to 12
	VCC_DA	Input (A)	3.3-V power supply voltage for the digital and analog circuits
	VREG_RF	Output (A)	Internally regulated analog 1.1-V supply output voltage for RF section
	RFIN	Input (A)	RX input
	VSS	Input (A)	Ground pin for the digital circuit and RF transceiver. Connect it to the system power supply (0 V).
	RFOUT	Output (A)	TX output
	VREG_TXPA	Output (A)	Internally regulated analog 1.1-V supply output voltage for the power amplifier (PA)
	VCC_RF	Input (A)	3.3-V RF power supply voltage
	VREG_PLL	Output (A)	Internally regulated analog 1.1-V supply output voltage for PLL
	VREG_VCO	Output (A)	Internally regulated analog 1.1-V supply output voltage for VCO
	REXT	Input (A)	External reference resistor connection port
	VCC_A	Input (A)	3.3-V power supply voltage for the analog circuits
	XIN	Input (A)	Crystal oscillator input
	XOUT	I/O (A)	Crystal oscillator output
	CKOUT	Output (A)	Clock output (16 MHz)
	REGIN	Input (A)	1.4- to 1.8-V DDC_OUT voltage input

Table 1.4 Pin Functions (6/6)

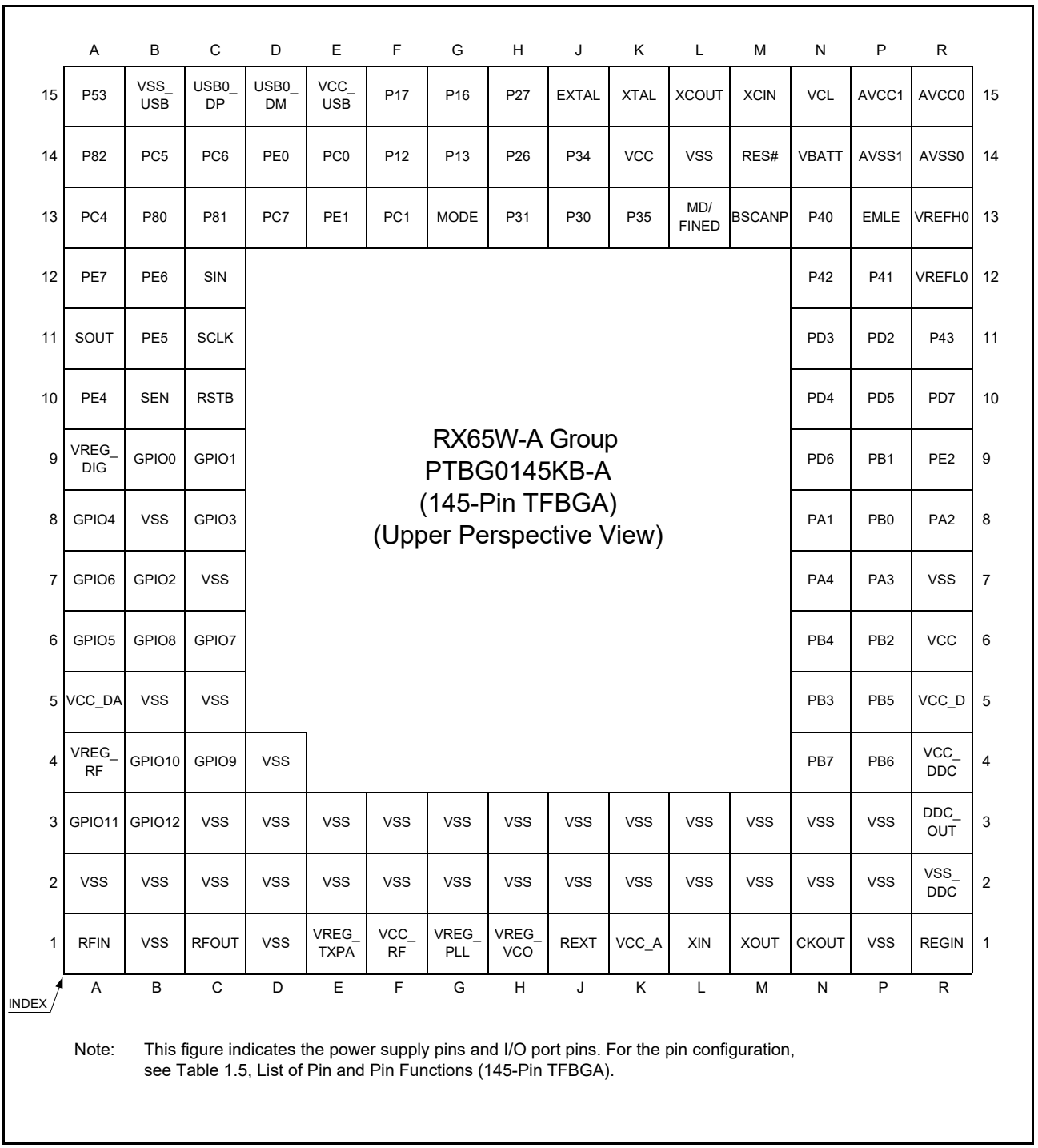
Classifications	Pin Name	I/O	Description
RF Transceiver	VSS_DDC	Input (A)	DC-to-DC converter ground
	DDC_OUT	Output (A)	1.4- to 1.8-V DC-to-DC converter output voltage
	VCC_DDC	Input (A)	3.3-V DC-to-DC converter power supply voltage
	VCC_D	Input (A)	3.3-V power supply voltage for the digital circuits
	RSTB	Input (D)	Reset-bar input (active-low)
	MODE	Input (D)	Mode switch (always low)

(A): Analog, (D): Digital

Note: Note the following regarding pin names. For details, see section 1.6, Pin Assignments.
- When the pin functions have “-DS” appended to their names, they can also be used as triggers for release from deep software standby.
- RIIC pin functions that have [FM+] appended to their names support fast-mode plus.

Note 1. When neither the 12-bit A/D converter nor temperature sensor is to be used, connect the AVCC0 and AVCC1 pins to VCC, and the AVSS0 and AVSS1 pins to VSS.

1.6 Pin Assignments



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	P53	VSS_USB	USB0_DP	USB0_DM	VCC_USB	P17	P16	P27	EXTAL	XTAL	XCOUT	XCIN	VCL	AVCC1	AVCC0	15
14	P82	PC5	PC6	PE0	PC0	P12	P13	P26	P34	VCC	VSS	RES#	VBATT	AVSS1	AVSS0	14
13	PC4	P80	P81	PC7	PE1	PC1	MODE	P31	P30	P35	MD/FINED	BSCANP	P40	EMLE	VREFH0	13
12	PE7	PE6	SIN										P42	P41	VREFL0	12
11	SOUT	PE5	SCLK										PD3	PD2	P43	11
10	PE4	SEN	RSTB										PD4	PD5	PD7	10
9	VREG_DIG	GPIO0	GPIO1										PD6	PB1	PE2	9
8	GPIO4	VSS	GPIO3										PA1	PB0	PA2	8
7	GPIO6	GPIO2	VSS										PA4	PA3	VSS	7
6	GPIO5	GPIO8	GPIO7										PB4	PB2	VCC	6
5	VCC_DA	VSS	VSS										PB3	PB5	VCC_D	5
4	VREG_RF	GPIO10	GPIO9	VSS									PB7	PB6	VCC_DDC	4
3	GPIO11	GPIO12	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DDC_OUT	3
2	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS_DDC	2
1	RFIN	VSS	RFOUT	VSS	VREG_TXPA	VCC_RF	VREG_PLL	VREG_VCO	REXT	VCC_A	XIN	XOUT	CKOUT	VSS	REGIN	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (145-Pin TFBGA).

Figure 1.3 Pin Assignment (145-Pin TFBGA)

1.7 List of Pin and Pin Functions

Table 1.5 List of Pin and Pin Functions (145-Pin TFBGA) (1/5)

Pin Number 145-Pin TFBGA	Power Supply Clock System Control	I/O Port	Timer (MTU, TPU, TMR, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, USB)	Camera Interface (QSPI, SDHI, SDSI)	Interrupt	A/D	RF Transceiver
A1								RFIN
A2	VSS							
A3								GPIO11
A4								VREG_RF
A5	VCC_DA							
A6								GPIO5
A7								GPIO6
A8								GPIO4
A9								VREG_DIG
A10		PE4	MTIOC4D/ MTIOC1A	SSLB0			AN102	
A11								SOUT
A12		PE7	MTIOC6A/TOC1	MISOB	SDHI_WP	IRQ7	AN105	
A13		PC4	MTIOC3D/ MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0				
A14		P82	MTIOC4A	RMII0_TXD1/ SMOSI10/ SSDA10/TXD10				
A15		P53						
B1	VSS							
B2	VSS							
B3								GPIO12
B4								GPIO10
B5	VSS							
B6								GPIO8
B7								GPIO2
B8	VSS							
B9								GPIO0
B10								SEN
B11		PE5	MTIOC4C/ MTIOC2B	REF50CK0/ RSPCKB		IRQ5	AN103	
B12		PE6	MTIOC6C/TIC1	MOSIB	SDHI_CD	IRQ6	AN104	
B13		P80	MTIOC3B	RMII0_TXD_EN/ SCK10/RTS10#	SDHI_WP			
B14		PC5	MTIOC3B/ MTCLKD/TMRI2	SCK8/SCK10/ RSPCKA				
B15	VSS_USB							
C1								RFOUT
C2	VSS							
C3	VSS							
C4								GPIO9
C5	VSS							
C6								GPIO7
C7	VSS							
C8								GPIO3

Table 1.5 List of Pin and Pin Functions (145-Pin TFBGA) (2/5)

Pin Number 145-Pin TFBGA	Power Supply Clock System Control	I/O Port	Timer (MTU, TPU, TMR, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, USB)	Camera Interface (QSPI, SDHI, SDSI)	Interrupt	A/D	RF Transceiver
C9								GPIO1
C10								RSTB
C11								SCLK
C12								SIN
C13		P81	MTIOC3D	RMII0_TXD0/ SMISO10/SSCL10/ RXD10	SDHI_CD			
C14		PC6	MTIOC3C/ MTCLKA/TMCI2/ TIC0	RXD8/SMISO8/ SSCL8/SMISO10/ SSCL10/RXD10/ MOSIA		IRQ13		
C15				USB0_DP				
D1	VSS							
D2	VSS							
D3	VSS							
D4	VSS							
D13	UB	PC7	MTIOC3A/ MTCLKB/TMO2/ TOC0/CACREF	TXD8/SMOSI8/ SSDA8/SMOSI10/ SSDA10/TXD10/ MISOA		IRQ14		
D14		PE0	MTIOC3D	SCK12/SSLB1			ANEX0	
D15				USB0_DM				
E1								VREG_TXPA
E2	VSS							
E3	VSS							
E13		PE1	MTIOC4C/ MTIOC3B	TXD12/SSDA12/ TXDX12/SIOX12/ SSLB2			ANEX1	
E14		PC0	MTIOC3C/TCLKC	CTS5#/RTS5#/ SS5#/SSLA1		IRQ14		
E15	VCC_USB							
F1	VCC_RF							
F2	VSS							
F3	VSS							
F13		PC1	MTIOC3A/TCLKD	SCK5/SSLA2		IRQ12		
F14		P12	MTIC5U/TMCI1	RXD2/SSCL2/ SCL0[FM+]		IRQ2		
F15		P17	MTIOC3A/ MTIOC3B/ MTIOC4B/TIOCB0/ TCLKD/TMO1/ POE8#	SCK1/TXD3/ SSDA3/SDA2-DS		IRQ7	ADTRG1#	
G1								VREG_PLL
G2	VSS							
G3	VSS							
G13								MODE
G14		P13	MTIOC0B/TIOCA5/ TMO3	TXD2/SSDA2/ SDA0[FM+]		IRQ3	ADTRG1#	
G15		P16	MTIOC3C/ MTIOC3D/ TIOCB1/TCLKC/ TMO2/RTCOUT	TXD1/SMOSI1/ SSDA1/RXD3/ SSCL3/SCL2-DS/ USB0_VBUS		IRQ6	ADTRG0#	
H1								VREG_VCO
H2	VSS							

Table 1.5 List of Pin and Pin Functions (145-Pin TFBGA) (3/5)

Pin Number 145-Pin TFBGA	Power Supply Clock System Control	I/O Port	Timer (MTU, TPU, TMR, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, USB)	Camera Interface (QSPI, SDHI, SDSI)	Interrupt	A/D	RF Transceiver
H3	VSS							
H13	TMS	P31	MTIOC4D/TMCI2/ RTCIC1	CTS1#/RTS1#/ SS1#		IRQ1-DS		
H14	TDO	P26	MTIOC2A/TMO1	TXD1/SMOSI1/ SSDA1/CTS3#/ RTS3#				
H15	TCK	P27	MTIOC2B/TMCI3	SCK1				
J1								REXT
J2	VSS							
J3	VSS							
J13	TDI	P30	MTIOC4B/TMRI3/ RTCIC0/POE8#	RXD1/SMISO1/ SSCL1		IRQ0-DS		
J14	TRST#	P34	MTIOC0A/TMCI3/ POE10#	ET0_LINKSTA/ SCK6		IRQ4		
J15	EXTAL	P36						
K1	VCC_A							
K2	VSS							
K3	VSS							
K13	UPSEL	P35				NMI		
K14	VCC							
K15	XTAL	P37						
L1								XIN
L2	VSS							
L3	VSS							
L13	MD/FINED							
L14	VSS							
L15	XCOUT							
M1								XOUT
M2	VSS							
M3	VSS							
M13	BSCANP							
M14	RES#							
M15	XCIN							
N1								CKOUT
N2	VSS							
N3	VSS							
N4		PB7	MTIOC3B/TIOCB5	RMII0_CRS_DV/ TXD9/SMOSI9/ SSDA9/SMOSI11/ SSDA11/TXD11	SDSI_D1			
N5		PB3	MTIOC0A/ MTIOC4A/ TIOCD3/TCLKD/ TMO0/POE11#	RMII0_RX_ER/ SCK4/SCK6	SDSI_D3			
N6		PB4	TIOCA4	RMII0_TXD_EN/ CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11#	SDSI_CMD			
N7		PA4	MTIC5U/MTCLKA/ TIOCA1/TMRI0	ET0_MDC/TXD5/ SMOSI5/SSDA5		IRQ5-DS		
N8		PA1	MTIOC0B/ MTCLKC/ MTIOC7B/TIOCB0	ET0_WOL/SCK5		IRQ11		

Table 1.5 List of Pin and Pin Functions (145-Pin TFBGA) (4/5)

Pin Number 145-Pin TFBGA	Power Supply Clock System Control	I/O Port	Timer (MTU, TPU, TMR, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, USB)	Camera Interface (QSPI, SDHI, SDSI)	Interrupt	A/D	RF Transceiver
N9		PD6	MTIC5V/ MTIOC8A/POE4#		QMO/QIO0/ SDHI_D0	IRQ6	AN106	
N10		PD4	MTIOC8B/POE11#		QSSL/SDHI_CMD	IRQ4	AN112	
N11		PD3	MTIOC8D/TOC2/ POE8#		QIO3/SDHI_D3	IRQ3	AN111	
N12		P42				IRQ10-DS	AN002	
N13		P40				IRQ8-DS	AN000	
N14	VBATT							
N15	VCL							
P1	VSS							
P2	VSS							
P3	VSS							
P4		PB6	MTIOC3D/TIOCA5	RMII0_TXD1/ RXD9/SMISO9/ SSCL9/SMISO11/ SSCL11/RXD11	SDSI_D0			
P5		PB5	MTIOC2A/ MTIOC1B/TIOCB4/ TMRI1/POE4#	RMII0_TXD0/ SCK9/SCK11	SDSI_CLK			
P6		PB2	TIOCC3/TCLKC	REF50CK0/ CTS4#/RTS4#/ SS4#/CTS6#/ RTS6#/SS6#	SDSI_D2			
P7		PA3	MTIOC0D/ MTCLKD/TIOCD0/ TCLKB	ET0_MDIO/RXD5/ SMISO5/SSCL5		IRQ6-DS		
P8		PB0	MTIC5W/TIOCA3	RMII0_RXD1/ RXD4/SMISO4/ SSCL4/RXD6/ SMISO6/SSCL6		IRQ12		
P9		PB1	MTIOC0C/ MTIOC4C/ TIOCB3/TMCI0	RMII0_RXD0/ TXD4/SMOSI4/ SSDA4/TXD6/ SMOSI6/SSDA6		IRQ4-DS		
P10		PD5	MTIC5W/ MTIOC8C/POE10#		QSPCLK/SDHI_CLK	IRQ5	AN113	
P11		PD2	MTIOC4D/TIC2		QIO2/SDHI_D2	IRQ2	AN110	
P12		P41				IRQ9-DS	AN001	
P13	EMLE							
P14	AVSS1							
P15	AVCC1							
R1								REGIN
R2	VSS_DDC							
R3								DDC_OUT
R4	VCC_DDC							
R5	VCC_D							
R6	VCC							
R7	VSS							
R8		PA2	MTIOC7A	RXD5/SMISO5/ SSCL5				
R9		PE2	MTIOC4A/TIC3	RXD12/SSCL12/ RXDX12/SSLB3		IRQ7-DS	AN100	
R10		PD7	MTIC5U/POE0#		QMI/QIO1/SDHI_D1	IRQ7	AN107	
R11		P43				IRQ11-DS	AN003	

Table 1.5 List of Pin and Pin Functions (145-Pin TFBGA) (5/5)

Pin Number 145-Pin TFBGA	Power Supply Clock System Control	I/O Port	Timer (MTU, TPU, TMR, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCI, RSPI, RIIC, USB)	Camera Interface (QSPI, SDHI, SDSI)	Interrupt	A/D	RF Transceiver
R12	VREFL0							
R13	VREFH0							
R14	AVSS0							
R15	AVCC0							

2. I/O Ports

2.1 Overview

The pins of an I/O port function as general I/O port pins, I/O pins for peripheral modules, or interrupt input pins.
Each pin is also configurable as an I/O pin of a peripheral module or an input pin for an interrupt. All pins function as input pins immediately after a reset, and pin functions are switched by register settings. The setting of each pin is specified by the registers for the corresponding I/O port and peripheral modules.
Each port has the port direction register (PDR) that selects input or output direction, the port output data register (PODR) that holds data for output, the port input register (PIDR) that indicates the pin states, the open-drain control register y (ODRy, y = 0, 1) that selects the output type of each pin, the pull-up resistor control register (PCR) that controls on/off of the input pull-up resistors, the drive capacity control register (DSCR, DSCR2) that selects the drive capacity, and the port mode register (PMR) that specifies the pin function of each port.
For details on PMR, refer to section 3, Multi-Function Pin Controller (MPC).
Table 2.1 shows the specifications of I/O ports, Table 2.2 lists the port functions.

Table 2.1 Specifications of I/O Ports

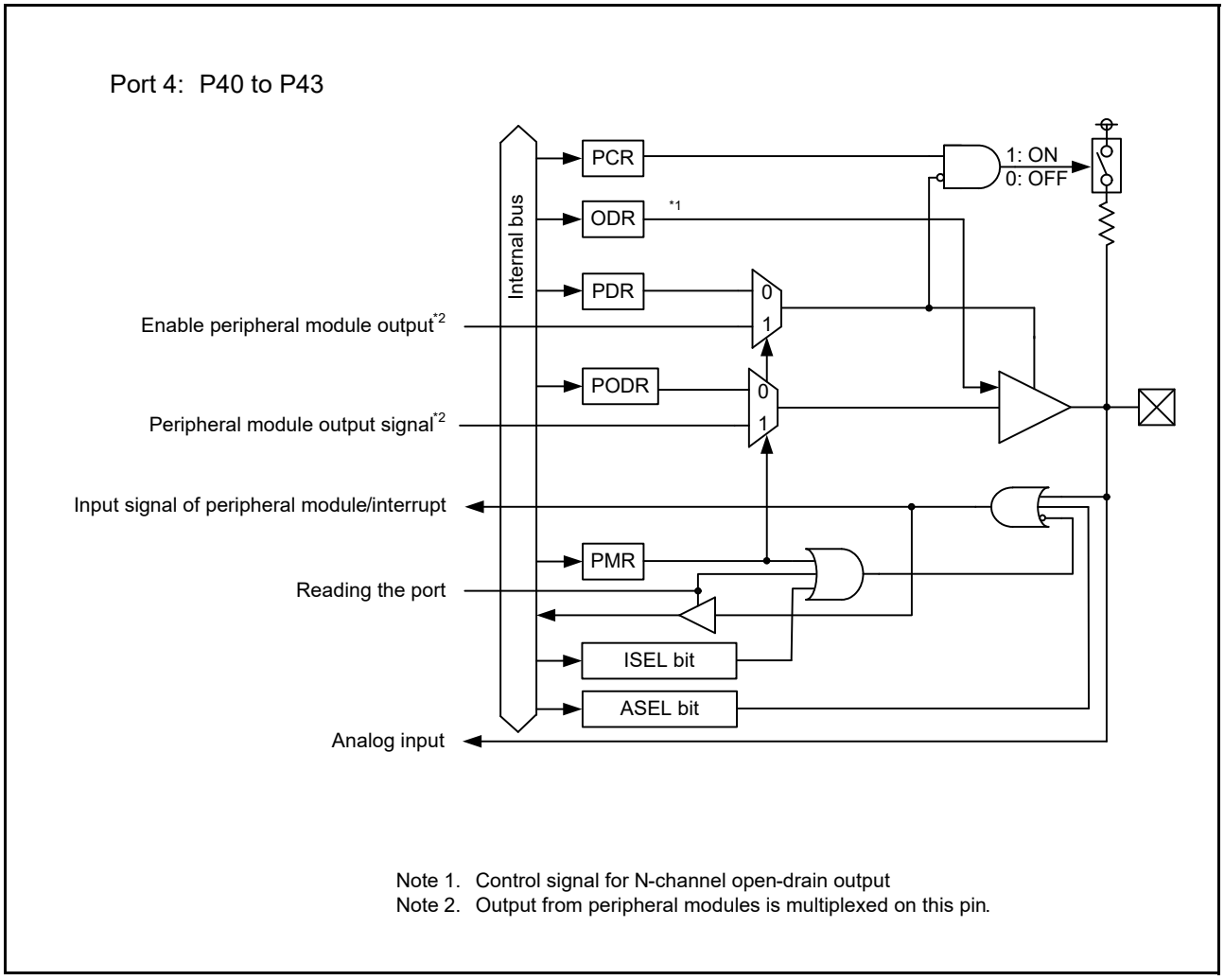
Port	Package	
	73 Pins	Number of Pin
PORT1	P12, P13, P16, P17	4
PORT2	P26, P27	2
PORT3	P30, P31, P34 to P37	6
PORT4	P40 to P43	4
PORT5	P53	1
PORT8	P80 to P82	3
PORTA	PA1 to PA4	4
PORTB	PB0 to PB7	8
PORTC	PC0, PC1, PC4 to PC7	6
PORTD	PD2 to PD7	6
PORTE	PE0 to PE2, PE4 to PE7	7
	Total of pins	51

Table 2.2 Port Functions

Port	Pin	Input Pull-up	Open-Drain Output	Driving Ability Switching	5-V Tolerant
PORT1	P12, P13	✓	✓	Normal drive/high drive/high-speed interface high-drive	✓
	P16	✓	✓	Fixed to high driving ability output	✓
	P17	✓	✓	High drive/high-speed interface high-drive	✓
PORT2	P26	✓	✓	Fixed to high driving ability output	—
	P27	✓	✓	Normal drive/high drive/high-speed interface high-drive	—
PORT3	P30, P31	✓	✓	High drive/high-speed interface high-drive	✓
	P34, P37	✓	✓	Fixed to high driving ability output	—
	P35	—	—	—	—
	P36	✓	✓	Fixed to normal output	—
PORT4	P40 to P43	✓	✓	Fixed to normal output	—
PORT5	P53	✓	✓	High drive/high-speed interface high-drive	—
PORT8	P80 to P82	✓	✓	Normal drive/high drive/high-speed interface high-drive	—
PORTA	PA1 to PA4	✓	✓	Normal drive/high drive/high-speed interface high-drive	—
PORTB	PB0 to PB7	✓	✓	Normal drive/high drive/high-speed interface high-drive	—
PORTC	PC0, PC1	✓	✓	Normal drive/high drive/high-speed interface high-drive	✓
	PC4 to PC7	✓	✓	Normal drive/high drive/high-speed interface high-drive	—
PORTD	PD2 to PD7	✓	✓	Normal drive/high drive/high-speed interface high-drive	—
PORTE	PE0 to PE2, PE4 to PE7	✓	✓	Normal drive/high drive/high-speed interface high-drive	—

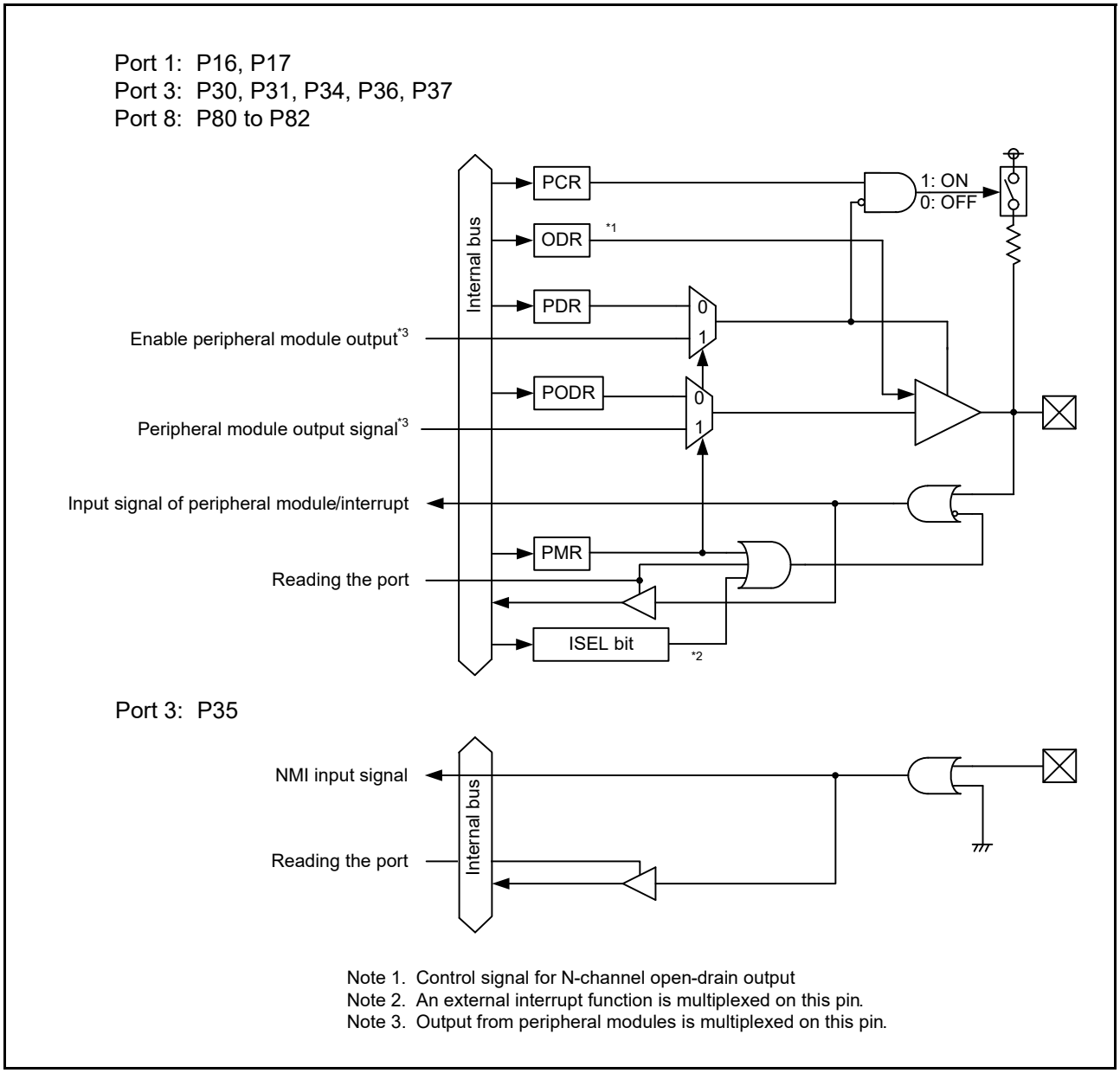
Specifying input pull-up, open-drain output, switching of driving ability, or 5-V tolerance is available for other signals on pins that also function as general I/O pins.

2.2 I/O Port Configuration



Note 1. Control signal for N-channel open-drain output
Note 2. Output from peripheral modules is multiplexed on this pin.

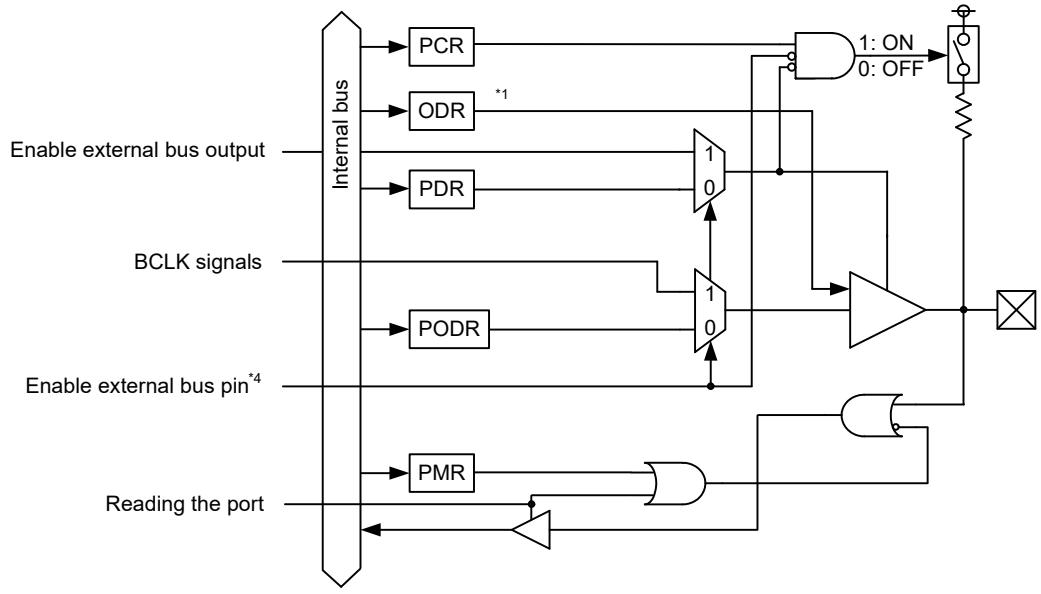
Figure 2.1 I/O Port Configuration (1)



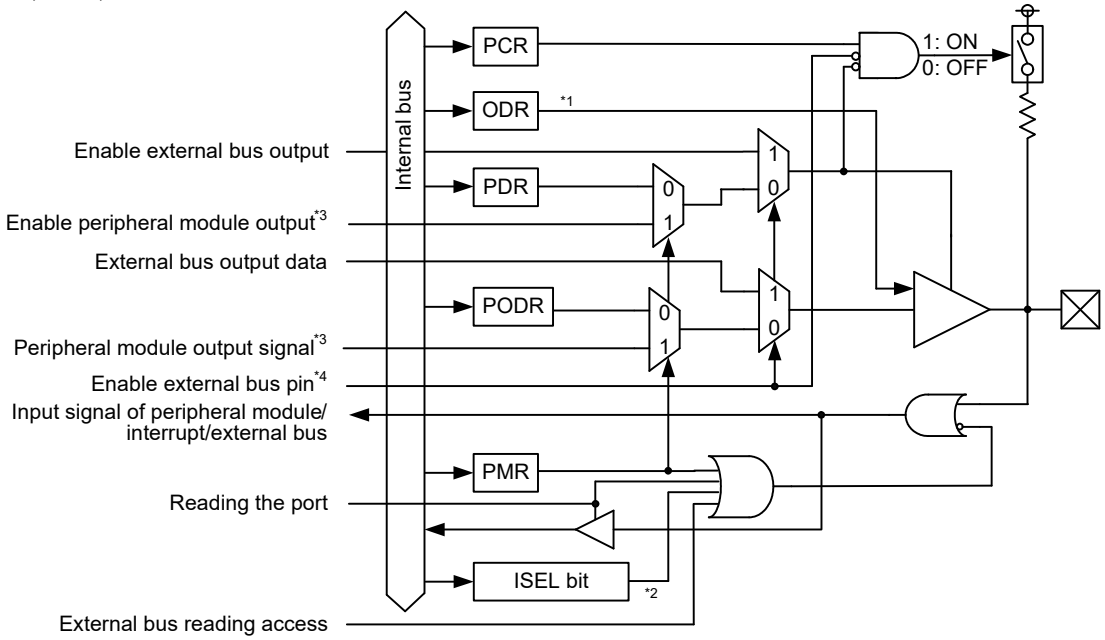
Note 1. Control signal for N-channel open-drain output
Note 2. An external interrupt function is multiplexed on this pin.
Note 3. Output from peripheral modules is multiplexed on this pin.

Figure 2.2 I/O Port Configuration (2)

Port 5: P53



Port 1: P12, P13
Port 2: P26, P27
Port A: PA1 to PA4
Port B: PB0 to PB7
Port C: PC0, PC1, PC4 to PC7



Note 1. Control signal for N-channel open-drain output
Note 2. An external interrupt function is multiplexed on this pin.
Note 3. Output from peripheral modules is multiplexed on this pin.
Note 4. Do not enable the external bus.

Figure 2.3 I/O Port Configuration (3)

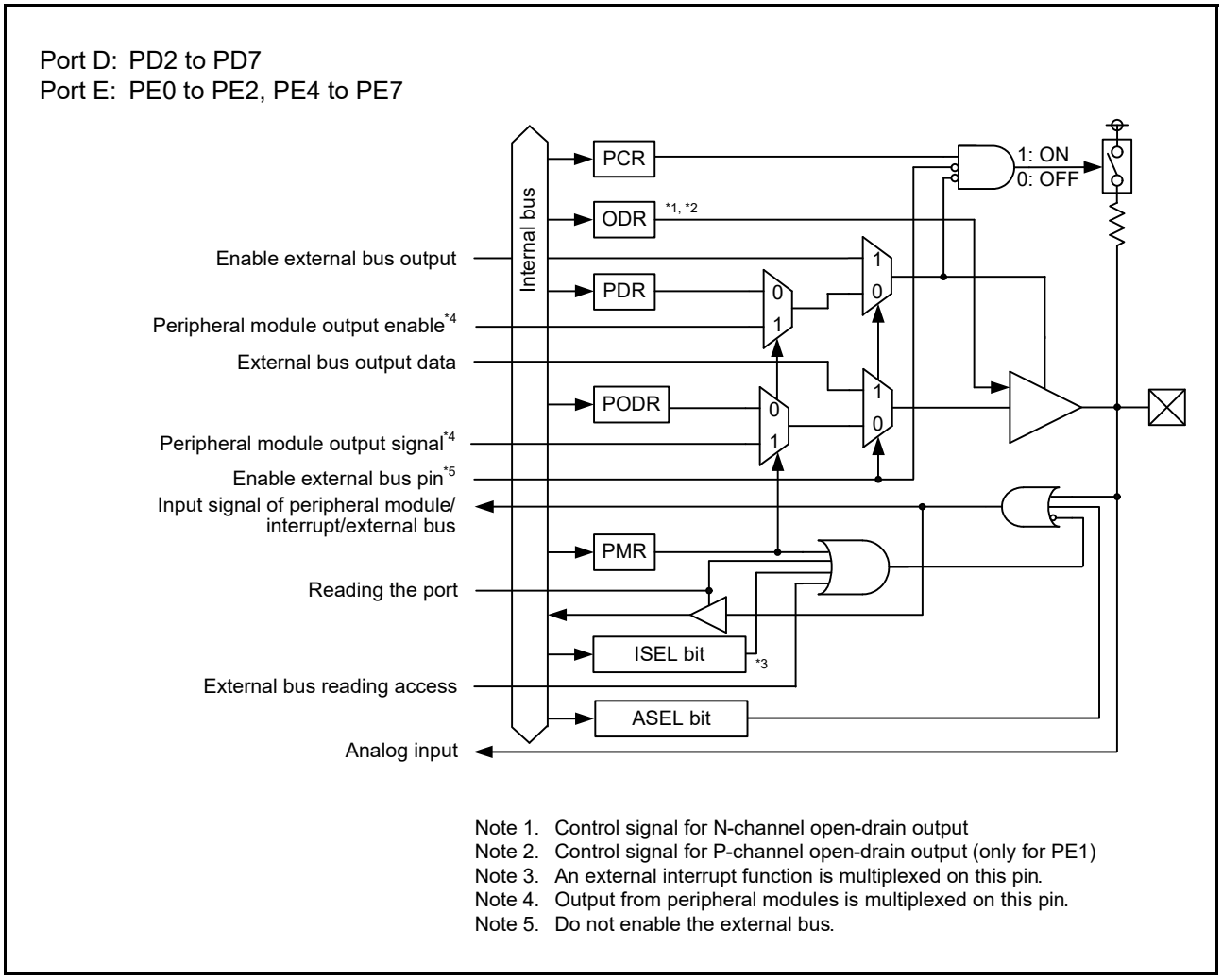


Figure 2.4 I/O Port Configuration (4)

2.3 Register Descriptions

2.3.1 Port Direction Register (PDR)

Address(es): PORT1.PDR 0008 C001h, PORT2.PDR 0008 C002h, PORT3.PDR 0008 C003h, PORT4.PDR 0008 C004h, PORT5.PDR 0008 C005h, PORT8.PDR 0008 C008h, PORTA.PDR 0008 C00Ah, PORTB.PDR 0008 C00Bh, PORTC.PDR 0008 C00Ch, PORTD.PDR 0008 C00Dh, PORTE.PDR 0008 C00Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	B7	B6	B5	B4	B3	B2	B1	B0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0 I/O Select	0: Input (Functions as an input pin.) 1: Output (Functions as an output pin.)	R/W
b1	B1	Pm1 I/O Select		R/W
b2	B2	Pm2 I/O Select		R/W
b3	B3	Pm3 I/O Select		R/W
b4	B4	Pm4 I/O Select		R/W
b5	B5	Pm5 I/O Select		R/W
b6	B6	Pm6 I/O Select		R/W
b7	B7	Pm7 I/O Select		R/W

m = 1 to 5, 8, A to E

PDR is a register which is used to select the input or output direction for individual pins of the corresponding port when the pins are configured as the general I/O pins.

Each bit of PORTm.PDR corresponds to each pin of port m; I/O direction can be specified in 1-bit units.

Note that the bits corresponding to port m that do not exist on a product are reserved. When writing, write 1 (output) to these bits.

Each bit of PDR corresponding to port m that does not exist is reserved. Make settings according to the description in section 2.4, Initialization of the Port Direction Register (PDR).

The B5 bit in PORT3.PDR is reserved, because the P35 pin is input only.

2.3.2 Port Output Data Register (PODR)

Address(es): PORT1.PODR 0008 C021h, PORT2.PODR 0008 C022h, PORT3.PODR 0008 C023h, PORT4.PODR 0008 C024h, PORT5.PODR 0008 C025h, PORT8.PODR 0008 C028h, PORTA.PODR 0008 C02Ah, PORTB.PODR 0008 C02Bh, PORTC.PODR 0008 C02Ch, PORTD.PODR 0008 C02Dh, PORTE.PODR 0008 C02Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	B7	B6	B5	B4	B3	B2	B1	B0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0 Output Data Store	0: Low output 1: High output	R/W
b1	B1	Pm1 Output Data Store		R/W
b2	B2	Pm2 Output Data Store		R/W
b3	B3	Pm3 Output Data Store		R/W
b4	B4	Pm4 Output Data Store		R/W
b5	B5	Pm5 Output Data Store		R/W
b6	B6	Pm6 Output Data Store		R/W
b7	B7	Pm7 Output Data Store		R/W

m = 1 to 5, 8, A to E

PODR is a register which holds the data to be output from the pins used for general I/O.
Bits corresponding to port m that do not exist on a product are reserved. When writing, write 0 (low output) to these bits.
The B5 bit in PORT3.PODR is reserved, because the P35 pin is input only. Data is not output from the corresponding pins even if these bits are set.
The bit corresponding to a pin that does not exist is reserved. A reserved bit is always read as 0. The write value should always be 0.

2.3.3 Port Input Register (PIDR)

Address(es): PORT1.PIDR 0008 C041h, PORT2.PIDR 0008 C042h, PORT3.PIDR 0008 C043h, PORT4.PIDR 0008 C044h, PORT5.PIDR 0008 C045h, PORT8.PIDR 0008 C048h, PORTA.PIDR 0008 C04Ah, PORTB.PIDR 0008 C04Bh, PORTC.PIDR 0008 C04Ch, PORTD.PIDR 0008 C04Dh, PORTE.PIDR 0008 C04Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	B7	B6	B5	B4	B3	B2	B1	B0
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0	0: Low input 1: High input	R
b1	B1	Pm1		R
b2	B2	Pm2		R
b3	B3	Pm3		R
b4	B4	Pm4		R
b5	B5	Pm5		R
b6	B6	Pm6		R
b7	B7	Pm7		R

m = 1 to 5, 8, A to E

PIDR is a register which reflects individual pin states of the port.
The pin states of port m can be read with the PORTm.PIDR, regardless of the values of PORTm.PDR and PORTm.PMR.
The NMI pin state is reflected in the P35 bit. However, the states of pins when the PmnPFS.ASEL bit is set to 1 cannot be read.
The bit corresponding to a pin that does not exist is reserved. A reserved bit is read as undefined, and cannot be modified.

2.3.4 Port Mode Register (PMR)

Address(es): PORT1.PMR 0008 C061h, PORT2.PMR 0008 C062h, PORT3.PMR 0008 C063h, PORT4.PMR 0008 C064h, PORT5.PMR 0008 C065h, PORT8.PMR 0008 C068h, PORTA.PMR 0008 C06Ah, PORTB.PMR 0008 C06Bh, PORTC.PMR 0008 C06Ch, PORTD.PMR 0008 C06Dh, PORTE.PMR 0008 C06Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	B7	B6	B5	B4	B3	B2	B1	B0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0 Pin Mode Control	0: Uses the pin as a general I/O pin. 1: Uses the pin as an I/O port for peripheral modules.	R/W
b1	B1	Pm1 Pin Mode Control		R/W
b2	B2	Pm2 Pin Mode Control		R/W
b3	B3	Pm3 Pin Mode Control		R/W
b4	B4	Pm4 Pin Mode Control		R/W
b5	B5	Pm5 Pin Mode Control		R/W
b6	B6	Pm6 Pin Mode Control		R/W
b7	B7	Pm7 Pin Mode Control		R/W

m = 1 to 5, 8, A to E

PMR is a register which specifies the function of the pins of the port.
Each bit of PORTm.PMR corresponds to each pin of port m; pin function can be specified in 1-bit units.
Note that the bits corresponding to port m that do not exist on a product are reserved. When writing, write 0 (general I/O port) to these bits.
The bit corresponding to a pin that does not exist is reserved. A reserved bit is always read as 0. The write value should always be 0.

2.3.5 Open-Drain Control Register 0 (ODR0)

Address(es): PORT1.ODR0 0008 C082h, PORT2.ODR0 0008 C084h, PORT3.ODR0 0008 C086h, PORT4.ODR0 0008 C088h, PORT5.ODR0 0008 C08Ah, PORT8.ODR0 0008 C090h, PORTA.ODR0 0008 C094h, PORTB.ODR0 0008 C096h, PORTC.ODR0 0008 C098h, PORTD.ODR0 0008 C09Ah, PORTE.ODR0 0008 C09Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	B6	—	B4	B3	B2	—	B0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0 Output Type Select	For pins other than the port PE1 pin	R/W
b1	—	Reserved	Odd bit / Even bit	R/W
b2	B2	Pm1 Output Type Select	X 0: CMOS output	R/W
b3	B3*1	PE1 Output Type Select	X 1: NMOS open-drain output	R/W
b4	B4	Pm2 Output Type Select	(b1, b3, b5, b7: Reserved)	R/W
b5	—	Reserved	For port PE1 pin	R/W
b6	B6	Pm3 Output Type Select	b3 b2	R/W
b7	—	Reserved	0 0: CMOS output	R/W
			0 1: NMOS open-drain output	
			1 0: PMOS open-drain output	
			1 1: Setting prohibited	

m = 1 to 5, 8, A to E

Note 1. The bit for a pin other than PE1 is reserved.

ODR0 is a register which is used to select an output type for the pins of the port.

In the registers other than PORTE.ODR0, the odd bits (b1, b3, b5, and b7) are reserved.

However, the output type of the port PE1 pin is specified by the combination of b3 and b2.

Bits corresponding to port m that do not exist on a product are reserved. When writing, write 0 (CMOS output) to these bits.

The bit corresponding to a pin that does not exist is also reserved. A reserved bit is always read as 0. The write value should always be 0.

2.3.6 Open-Drain Control Register 1 (ODR1)

Address(es): PORT1.ODR1 0008 C083h, PORT2.ODR1 0008 C085h, PORT3.ODR1 0008 C087h, PORT4.ODR1 0008 C089h, PORT5.ODR1 0008 C08Bh, PORT8.ODR1 0008 C091h, PORTA.ODR1 0008 C095h, PORTB.ODR1 0008 C097h, PORTC.ODR1 0008 C099h, PORTD.ODR1 0008 C09Bh, PORTE.ODR1 0008 C09Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	B6	—	B4	—	B2	—	B0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm4 Output Type Select	0: CMOS output 1: NMOS open-drain output	R/W
b1	—	Reserved		R/W
b2	B2	Pm5 Output Type Select		R/W
b3	—	Reserved		R/W
b4	B4	Pm6 Output Type Select		R/W
b5	—	Reserved		R/W
b6	B6	Pm7 Output Type Select		R/W
b7	—	Reserved		R/W

m = 1 to 5, 8, A to E

ODR1 is used to select an output type for each pin of the port.
The odd bits (b1, b3, b5, and b7) in the ODR1 register are reserved.
Bits corresponding to port m that do not exist on a product are reserved. When writing, write 0 (CMOS output) to these bits.
The bit corresponding to a pin that does not exist is also reserved. A reserved bit is always read as 0. The write value should always be 0.

2.3.7 Pull-Up Resistor Control Register (PCR)

Address(es): PORT1.PCR 0008 C0C1h, PORT2.PCR 0008 C0C2h, PORT3.PCR 0008 C0C3h, PORT4.PCR 0008 C0C4h, PORT5.PCR 0008 C0C5h, PORT8.PCR 0008 C0C8h, PORTA.PCR 0008 C0CAh, PORTB.PCR 0008 C0CBh, PORTC.PCR 0008 C0CCh, PORTD.PCR 0008 C0CDh, PORTE.PCR 0008 C0CEh

	b7	b6	b5	b4	b3	b2	b1	b0
	B7	B6	B5	B4	B3	B2	B1	B0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0 Input Pull-Up Resistor Control	0: Disables an input pull-up resistor. 1: Enables an input pull-up resistor.	R/W
b1	B1	Pm1 Input Pull-Up Resistor Control		R/W
b2	B2	Pm2 Input Pull-Up Resistor Control		R/W
b3	B3	Pm3 Input Pull-Up Resistor Control		R/W
b4	B4	Pm4 Input Pull-Up Resistor Control		R/W
b5	B5	Pm5 Input Pull-Up Resistor Control		R/W
b6	B6	Pm6 Input Pull-Up Resistor Control		R/W
b7	B7	Pm7 Input Pull-Up Resistor Control		R/W

m = 1 to 5, 8, A to E

PCR is a register which enables or disables an input pull-up resistor for individual pins of the port.
While a pin is in the input state with the corresponding bit in PORTm.PCR set to 1, the pull-up resistor connected to the pin is enabled.
When a pin is set as a general port output pin or a peripheral module output pin, the pull-up resistor for the pin is disabled regardless of the settings of PCR.
The pull-up resistor is also disabled in the reset state.
The other bits are also reserved because they correspond to pins that do not exist is reserved. A reserved bit is always read as 0. The write value should always be 0.

2.3.8 Drive Capacity Control Register (DSCR)

Address(es): PORT1.DSCR 0008 C0E1h, PORT2.DSCR 0008 C0E2h, PORT5.DSCR 0008 C0E5h, PORT8.DSCR 0008 C0E8h, PORTA.DSCR 0008 C0EAh, PORTB.DSCR 0008 C0EBh, PORTC.DSCR 0008 C0ECh, PORTD.DSCR 0008 C0EDh, PORTE.DSCR 0008 C0EEh

	b7	b6	b5	b4	b3	b2	b1	b0
	B7	B6	B5	B4	B3	B2	B1	B0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0 Drive Capacity Control	0: Normal drive output 1: High-drive output	R/W
b1	B1	Pm1 Drive Capacity Control		R/W
b2	B2	Pm2 Drive Capacity Control		R/W
b3	B3	Pm3 Drive Capacity Control		R/W
b4	B4	Pm4 Drive Capacity Control		R/W
b5	B5	Pm5 Drive Capacity Control		R/W
b6	B6	Pm6 Drive Capacity Control		R/W
b7	B7	Pm7 Drive Capacity Control		R/W

m = 1, 2, 5, 8, A to E

DSCR is a register which is used to switch the drive capacity of the port.
When pins are set for high-speed interface high-drive in the DSCR2 register, the drive capacity cannot be changed. For setting of the drive capacity by the DSCR and DSCR2 registers, refer to Table 2.3, Drive Capacity Setting by DSCR and DSCR2 Registers.
The bit corresponding to a pin whose drive capacity cannot be switched, or to high drive output is readable and writable, but the drive capacity cannot be changed.
The bit corresponding to a pin that does not exist is reserved. A reserved bit is always read as 0. The write value should always be 0.

2.3.9 Drive Capacity Control Register 2 (DSCR2)

Address(es): PORT1.DSCR2 0008 C129h, PORT2.DSCR2 0008 C12Ah, PORT3.DSCR2 0008 C12Bh, PORT5.DSCR2 0008 C12Dh, PORT8.DSCR2 0008 C130h, PORTA.DSCR2 0008 C132h, PORTB.DSCR2 0008 C133h, PORTC.DSCR2 0008 C134h, PORTD.DSCR2 0008 C135h, PORTE.DSCR2 0008 C136h

	b7	b6	b5	b4	b3	b2	b1	b0
	B7	B6	B5	B4	B3	B2	B1	B0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0 Drive Capacity Control 2	0: Normal drive/high-drive output*1 1: High-speed interface high-drive output	R/W
b1	B1	Pm1 Drive Capacity Control 2		R/W
b2	B2	Pm2 Drive Capacity Control 2		R/W
b3	B3	Pm3 Drive Capacity Control 2		R/W
b4	B4	Pm4 Drive Capacity Control 2		R/W
b5	B5	Pm5 Drive Capacity Control 2		R/W
b6	B6	Pm6 Drive Capacity Control 2		R/W
b7	B7	Pm7 Drive Capacity Control 2		R/W

m = 1 to 3, 5, 8, A to E

Note 1. Pins that support switching drive capacity by the DSCR register depend on the setting of the DSCR register.

DSCR2 is a register which is used to switch the drive capacity of the port.

Table 2.3 shows the setting of drive capacity by the DSCR and DSCR2 registers.

The bit corresponding to a pin whose drive capacity cannot be switched, or to high drive output for the high-speed interface is readable and writable, but the drive capacity cannot be changed.

The bit corresponding to a pin that does not exist is reserved. A reserved bit is always read as 0. The write value should always be 0.

Set the register only based on an instruction in the application guide.

Table 2.3 Drive Capacity Setting by DSCR and DSCR2 Registers

PORTm.DSCR2.Bx	PORTm.DSCR.Bx	Drive Capacity*1
0	0	Normal drive output
0	1	High-drive output
1	Don’t care	High-speed interface high-drive output

Note 1. When drive capacity is fixed, or drive capacity of a pin whose drive capacity cannot be switched cannot be changed.

2.4 Initialization of the Port Direction Register (PDR)

Initialize reserved bits in the PDR register according to Table 2.4.

- The blank columns in Table 2.4 indicate the bits corresponding to the pins listed in Table 2.1, Specifications of I/O Ports.
  The corresponding bits should be set to 1 (output) or 0 (input) depending on the user system.
  However, the PORT3.PDR.B5 bit of the input-only P35 pin is reserved.
  This bit should be set to 0 (input).
- The columns other than the blank columns in Table 2.4 indicate reserved bits.
  A reserved bit should be set to 0 (input) or 1 (output) according to Table 2.4.
  When setting a value to a reserved bit, access in byte units.

Table 2.4 PDR Register Settings

	PDR Register							
Port Symbol	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
PORT0	1	1	1	1	1	1	1	1
PORT1			1	1			1	1
PORT2			1	1	1	1	1	1
PORT3			0		1	1		
PORT4	1	1	1	1				
PORT5	1	1	1	1		1	1	1
PORT6	1	1	1	1	1	1	1	1
PORT7	1	1	1	1	1	1	1	1
PORT8	1	1	1	1	1			
PORT9	1	1	1	1	1	1	1	1
PORTA	1	1	1					1
PORTB								
PORTC					1	1		
PORTD							1	1
PORTE					1			
PORTF	1	1	1	1	1	1	1	1
PORTG	1	1	1	1	1	1	1	1
PORTJ	1	1	1	1	1	1	1	1

2.5 Handling of Unused Pins

Details on the handling of unused pins are given in Table 2.5.

Table 2.5 Handling of Unused Pins

Pin Name	Handling
EMLE	Connect this pin to VSS via a resistor (pulling down).
BSCANP	Connect this pin to VSS via a resistor (pulling down).
MD	Use this as a mode pin.
RES#	Connect this pin to VCC via a resistor (pulling up).
VCC_USB	Connect this pin to VCC
VSS_USB	Connect this pin to VSS
USB0_DP	Leave these pins open-circuit.
USB0_DM	
VBATT	Connect this pin to VCC
P35/NMI	Connect this pin to VCC via a resistor (pulling up).
P36/EXTAL	Set the MOSCCR.MOSTP bit to 1 (the main clock oscillator is stopped) when not using the main clock When this pin is not used as port P36, handle as port 1 to 5, 8, A to E.
P37/XTAL	Set the MOSCCR.MOSTP bit to 1 (the main clock oscillator is stopped) when not using the main clock When this pin is not used as port P37, handle as port 1 to 5, 8, A to E When an external clock is input to the EXTAL pin, leave this pin open-circuit.
XCIN	Connect this pin to VSS via a resistor (pulling down).
XCOUT	Leave this pin open-circuit.
Port 1 to 5, 8, A to E	• If the direction setting is for input (PORTn.PDR = 0), the corresponding pin is connected to VCC (pulled up) via a resistor or to VSS (pulled down) via a resistor.*1 • If the direction setting is for output (PORTn.PDR = 1), leave these pins open-circuit.*1, *2
VREFH0	Connect this pin to AVCC0.
VREFL0	Connect this pin to AVSS0.
AVCC0	Connect this pin to VCC when not using the 12-bit A/D converter (unit 0).
AVSS0	Connect this pin to VSS when not using the 12-bit A/D converter (unit 0).
AVCC1	Connect this pin to VCC when not using the 12-bit A/D converter (unit 1).
AVSS1	Connect this pin to VSS when not using the 12-bit A/D converter (unit 1).
GPIO0 to GPIO12	As inputs: Leave these pins open-circuit, or individually connect each pin to VCC_DDC via a resistor.
	As outputs: Leave these pins open-circuit.
CKOUT	Leave this pin open-circuit.

Note 1. Clear the PORTn.PMR bit, the PmnPFS.ISEL bit and the PmnPFS.ASEL bit to 0.
Note 2. In the case of release when the setting is for output, the port is an input over the period from release from the reset state to the pin becoming an output. Since the voltage on the pin is undefined while it is an input, this may lead to an increase in the current drawn.

3. Multi-Function Pin Controller (MPC)

3.1 Overview

The multi-function pin controller (MPC) selects and assigns input/output of peripheral functions and interrupt input signals from multiple ports.
Selecting a single function for multiple pins is prohibited.

Table 3.1 Functions Assigned to Each Multiplexed Pin (1/8)

Module/Function	Channel	Pin Functions	Allocation Port
Interrupt		NMI (input)	P35
Interrupt	IRQ0	IRQ0-DS (input)	P30
	IRQ1	IRQ1-DS (input)	P31
	IRQ2	IRQ2 (input)	P12
			PD2
	IRQ3	IRQ3 (input)	P13
			PD3
	IRQ4	IRQ4-DS (input)	PB1
		IRQ4 (input)	P34
			PD4
	IRQ5	IRQ5-DS (input)	PA4
		IRQ5 (input)	PD5
			PE5
	IRQ6	IRQ6-DS (input)	PA3
		IRQ6 (input)	P16
			PD6
			PE6
	IRQ7	IRQ7-DS (input)	PE2
		IRQ7 (input)	P17
			PD7
			PE7
	IRQ8	IRQ8-DS (input)	P40
	IRQ9	IRQ9-DS (input)	P41
	IRQ10	IRQ10-DS (input)	P42
	IRQ11	IRQ11-DS (input)	P43
		IRQ11 (input)	PA1
	IRQ12	IRQ12 (input)	PB0
			PC1
	IRQ13	IRQ13 (input)	PC6
	IRQ14	IRQ14 (input)	PC0
			PC7

Table 3.1 Functions Assigned to Each Multiplexed Pin (2/8)

Module/Function	Channel	Pin Functions	Allocation Port
Multi-function timer unit 3	MTU0	MTIOC0A (input/output)	P34
			PB3
		MTIOC0B (input/output)	P13
			PA1
		MTIOC0C (input/output)	PB1
		MTIOC0D (input/output)	PA3
	MTU1	MTIOC1A (input/output)	PE4
		MTIOC1B (input/output)	PB5
	MTU2	MTIOC2A (input/output)	P26
			PB5
		MTIOC2B (input/output)	P27
			PE5
Multi-function timer unit 3	MTU3	MTIOC3A (input/output)	P17
			PC1
			PC7
		MTIOC3B (input/output)	P17
			P80
			PB7
			PC5
			PE1
		MTIOC3C (input/output)	P16
			PC0
			PC6
		MTIOC3D (input/output)	P16
			P81
			PB6
			PC4
			PE0
	MTU4	MTIOC4A (input/output)	P82
			PB3
			PE2
		MTIOC4B (input/output)	P17
			P30
		MTIOC4C (input/output)	PB1
			PE1
			PE5
		MTIOC4D (input/output)	P31
			PD2
			PE4
	MTU5	MTIC5U (input)	P12
			PA4
			PD7
		MTIC5V (input)	PD6
		MTIC5W (input)	PB0
			PD5

Table 3.1 Functions Assigned to Each Multiplexed Pin (3/8)

Module/Function	Channel	Pin Functions	Allocation Port
Multi-function timer unit 3	MTU6	MTIOC6A (input/output)	PE7
		MTIOC6C (input/output)	PE6
	MTU7	MTIOC7A (input/output)	PA2
		MTIOC7B (input/output)	PA1
	MTU8	MTIOC8A (input/output)	PD6
		MTIOC8B (input/output)	PD4
		MTIOC8C (input/output)	PD5
		MTIOC8D (input/output)	PD3
	MTU	MTCLKA (input)	PA4
			PC6
		MTCLKB (input)	PC7
		MTCLKC (input)	PA1
			PC4
		MTCLKD (input)	PA3
			PC5
Port output enable 3	POE0	POE0# (input)	PC4
			PD7
	POE4	POE4# (input)	PB5
			PD6
	POE8	POE8# (input)	P17
			P30
			PD3
	POE10	POE10# (input)	P34
			PD5
	POE11	POE11# (input)	PB3
			PD4
16-bit timer pulse unit	TPU0	TIOCB0 (input/output)	P17
			PA1
		TIOCD0 (input/output)	PA3
	TPU1	TIOCA1 (input/output)	PA4
		TIOCB1 (input/output)	P16
	TPU3	TIOCA3 (input/output)	PB0
		TIOCB3 (input/output)	PB1
		TIOCC3 (input/output)	PB2
		TIOCD3 (input/output)	PB3
	TPU4	TIOCA4 (input/output)	PB4
		TIOCB4 (input/output)	PB5
	TPU5	TIOCA5 (input/output)	P13
			PB6
		TIOCB5 (input/output)	PB7

Table 3.1 Functions Assigned to Each Multiplexed Pin (4/8)

Module/Function	Channel	Pin Functions	Allocation Port
16-bit timer pulse unit	TPU (unit 0)	TCLKB (input)	PA3
		TCLKC (input)	P16
			PB2
			PC0
		TCLKD (input)	P17
			PB3
			PC1
8-bit timer	TMR0	TMO0 (output)	PB3
		TMCI0 (input)	PB1
		TMRI0 (input)	PA4
	TMR1	TMO1 (output)	P17
			P26
		TMCI1 (input)	P12
			PC4
		TMRI1 (input)	PB5
	TMR2	TMO2 (output)	P16
			PC7
		TMCI2 (input)	P31
			PC6
		TMRI2 (input)	PC5
	TMR3	TMO3 (output)	P13
		TMCI3 (input)	P27
			P34
		TMRI3 (input)	P30
Compare match timer W	CMTW0	TOC0 (output)	PC7
		TIC0 (input)	PC6
	CMTW1	TOC1 (output)	PE7
		TIC1 (input)	PE6
	CMTW2	TOC2 (output)	PD3
		TIC2 (input)	PD2
	CMTW3	TIC3 (input)	PE2
Ethernet controller	RMII0	REF50CK0 (input)	PB2
			PE5
		RMII0_TXD_EN (output)	P80
			PB4
		RMII0_TXD0 (output)	P81
			PB5
		RMII0_TXD1 (output)	P82
			PB6
		RMII0_CRS_DV (input)	PB7
		RMII0_RXD0 (input)	PB1
		RMII0_RXD1 (input)	PB0
		RMII0_RX_ER (input)	PB3

Table 3.1 Functions Assigned to Each Multiplexed Pin (5/8)

Module/Function	Channel	Pin Functions	Allocation Port
Ethernet controller	MII0	ET0_MDC (output)	PA4
		ET0_MDIO (input/output)	PA3
		ET0_LINKSTA (input)	P34
		ET0_WOL (output)	PA1
Serial communications interface	SCI1	RXD1 (input)/SMISO1 (input/output)/ SSCL1 (input/output)	P30
		TXD1 (output)/SMOSI1 (input/output)/ SSDA1 (input/output)	P16
			P26
		SCK1 (input/output)	P17
			P27
		CTS1# (input)/RTS1# (output)/ SS1# (input)	P31
	SCI2*2	RXD2 (input)/SSCL2 (input/output)	P12
		TXD2 (output)/SSDA2 (input/output)	P13
	SCI3*2	RXD3 (input)/SSCL3 (input/output)	P16
		TXD3 (output)/SSDA3 (input/output)	P17
		CTS3# (input)/RTS3# (output)	P26
	SCI4	RXD4 (input)/SMISO4 (input/output)/ SSCL4 (input/output)	PB0
		TXD4 (output)/SMOSI4 (input/output)/ SSDA4 (input/output)	PB1
		SCK4 (input/output)	PB3
		CTS4# (input)/RTS4# (output)/ SS4# (input)	PB2
	SCI5	RXD5 (input)/SMISO5 (input/output)/ SSCL5 (input/output)	PA2
			PA3
		TXD5 (output)/SMOSI5 (input/output)/ SSDA5 (input/output)	PA4
		SCK5 (input/output)	PA1
			PC1
			PC4
		CTS5# (input)/RTS5# (output)/ SS5# (input)	PC0
	SCI6	RXD6 (input)/SMISO6 (input/output)/ SSCL6 (input/output)	PB0
		TXD6 (output)/SMOSI6 (input/output)/ SSDA6 (input/output)	PB1
		SCK6 (input/output)	P34
			PB3
		CTS6# (input)/RTS6# (output)/ SS6# (input)	PB2
	SCI8	RXD8 (input)/SMISO8 (input/output)/ SSCL8 (input/output)	PC6
		TXD8 (output)/SMOSI8 (input/output)/ SSDA8 (input/output)	PC7
		SCK8 (input/output)	PC5
		CTS8# (input)/RTS8# (output)/ SS8# (input)	PC4

Table 3.1 Functions Assigned to Each Multiplexed Pin (6/8)

Module/Function	Channel	Pin Functions	Allocation Port
Serial communications interface	SCI9	RXD9 (input)/SMISO9 (input/output)/ SSCL9 (input/output)	PB6
		TXD9 (output)/SMOSI9 (input/output)/ SSDA9 (input/output)	PB7
		SCK9 (input/output)	PB5
		CTS9# (input)/RTS9# (output)/ SS9# (input)	PB4
	SCI10	RXD10 (input)/SMISO10 (input/output)/ SSCL10 (input/output)	P81
			PC6
		TXD10 (output)/SMOSI10 (input/output)/ SSDA10 (input/output)	P82
			PC7
		SCK10 (input/output)	P80
			PC5
		RTS10# (output)	P80
		CTS10# (input)/RTS10# (output)/ SS10# (input)	PC4
	SCI11	RXD11 (input)/SMISO11 (input/output)/ SSCL11 (input/output)	PB6
		TXD11 (output)/SMOSI11 (input/output)/ SSDA11 (input/output)	PB7
		SCK11 (input/output)	PB5
		CTS11# (input)/RTS11# (output)/ SS11#(input)	PB4
	SCI12*2	RXD12 (input)/SSCL12 (input/output)/ RXDX12 (input)	PE2
		TXD12 (output)/SSDA12 (input/output)/ TXDX12 (output)/SIOX12 (input/output)	PE1
		SCK12 (input/output)	PE0
I2C bus interface	RIIC0	SCL0[FM+] (input/output)	P12
		SDA0[FM+] (input/output)	P13
	RIIC2	SCL2-DS (input/output)	P16
		SDA2-DS (input/output)	P17
USB 2.0FS function module	USB0	USB0_VBUS (input)	P16
Serial peripheral interface	RSPI0	RSPCKA (input/output)	PC5
		MOSIA (input/output)	PC6
		MISOA (input/output)	PC7
		SSLA0 (input/output)	PC4
		SSLA1 (output)	PC0
		SSLA2 (output)	PC1
	RSPI1	RSPCKB (input/output)	PE5
		MOSIB (input/output)	PE6
		MISOB (input/output)	PE7
		SSLB0 (input/output)	PE4
		SSLB1 (output)	PE0
		SSLB2 (output)	PE1
		SSLB3 (output)	PE2

Table 3.1 Functions Assigned to Each Multiplexed Pin (7/8)

Module/Function	Channel	Pin Functions	Allocation Port
Realtime clock		RTCOUT (output)	P16
		RTCIC0 (input)*1	P30
		RTCIC1 (input)*1	P31
12-bit A/D converter		AN000 (input)*1	P40
		AN001 (input)*1	P41
		AN002 (input)*1	P42
		AN003 (input)*1	P43
		ADTRG0# (input)	P16
		AN100 (input)*1	PE2
		AN102 (input)*1	PE4
		AN103 (input)*1	PE5
		AN104 (input)*1	PE6
		AN105 (input)*1	PE7
		AN106 (input)*1	PD6
		AN107 (input)*1	PD7
		AN110 (input)*1	PD2
		AN111 (input)*1	PD3
		AN112 (input)*1	PD4
		AN113 (input)*1	PD5
		ANEX0 (output)*1	PE0
		ANEX1 (input)*1	PE1
		ADTRG1# (input)	P13
			P17
SD host interface		SDHI_CLK (output)	PD5
		SDHI_CMD (input/output)	PD4
		SDHI_CD (input)	P81
			PE6
		SDHI_WP (input)	P80
			PE7
		SDHI_D0 (input/output)	PD6
		SDHI_D1 (input/output)	PD7
		SDHI_D2 (input/output)	PD2
		SDHI_D3 (input/output)	PD3
SD slave interface		SDSI_CLK (input)	PB5
		SDSI_CMD (input/output)	PB4
		SDSI_D0 (input/output)	PB6
		SDSI_D1 (input/output)	PB7
		SDSI_D2 (input/output)	PB2
		SDSI_D3 (input/output)	PB3
Clock frequency accuracy measurement circuit		CACREF (input)	PC7

Table 3.1 Functions Assigned to Each Multiplexed Pin (8/8)

Module/Function	Channel	Pin Functions	Allocation Port
Quad serial peripheral interface		QSPCLK (output)	PD5
		QSSL (output)	PD4
		QMO/QIO0 (input/output)	PD6
		QMI/QIO1 (input/output)	PD7
		QIO2 (input/output)	PD2
		QIO3 (input/output)	PD3

Note 1. To use this pin function, set the corresponding pin as general input (set the PORTm.PDR.Bn and PORTm.PMR.Bn bits to 0).
Note 2. Serial communications interface is not available in simple SPI mode.

3.2 Register Descriptions

The registers and bits of unsupported pins, depending on the package, are reserved. The write value to the reserved bits is the value after a reset.

3.2.1 Write-Protect Register (PWPR)

Address(es): 0008 C11Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	B0WI	PFSWE	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	PFSWE	PFS Register Write Enable	0: Writing to the PFS register is disabled 1: Writing to the PFS register is enabled	R/W
b7	B0WI	PFSWE Bit Write Disable	0: Writing to the PFSWE bit is enabled 1: Writing to the PFSWE bit is disabled	R/W

PFSWE Bit (PFS Register Write Enable)

Writing to PmnPFS register is enabled only when the PFSWE bit is set to 1.
To set the PFSWE bit to 1, write 1 to the PFSWE bit after writing 0 to the B0WI bit.

B0WI Bit (PFSWE Bit Write Disable)

Writing to the PFSWE bit is enabled only when the B0WI bit is set to 0.

3.2.2 P1n Pin Function Control Register (P1nPFS) (n = 2, 3, 6, 7)

Address(es): P12PFS 0008 C14Ah, P13PFS 0008 C14Bh, P16PFS 0008 C14Eh, P17PFS 0008 C14Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 3.2.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin P12: IRQ2 P13: IRQ3 P16: IRQ6 P17: IRQ7	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 3.2 Register Settings for Input/Output Pin Function

	Pin			
PSEL[5:0] Settings	**P12**	**P13**	**P16**	**P17**
000000b (initial value)	Hi-Z			
000001b	—	MTIOC0B	MTIOC3C	MTIOC3A
000010b	—	—	MTIOC3D	MTIOC3B
000011b	—	TIOCA5	TIOCB1	TIOCB0
000100b	—	—	TCLKC	TCLKD
000101b	TMCI1	TMO3	TMO2	TMO1
000111b	—	—	RTCOUT	POE8#
001000b	—	—	—	MTIOC4B
001001b	—	ADTRG1#	ADTRG0#	ADTRG1#
001010b	RXD2 SSCL2	TXD2 SSDA2	TXD1 SMOSI1 SSDA1	SCK1
001011b	—	—	RXD3 SSCL3	TXD3 SSDA3
001111b	SCL0[FM+]	SDA0[FM+]	SCL2-DS	SDA2-DS
010001b	—	—	USB0_VBUS	—

—: Do not specify this value.

3.2.3 P2n Pin Function Control Register (P2nPFS) (n = 6, 7)

Address(es): P26PFS 0008 C156h, P27PFS 0008 C157h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 3.3.	R/W
b7 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Table 3.3 Register Settings for Input/Output Pin Function

	Pin	
PSEL[5:0] Settings	**P26**	**P27**
000000b (initial value)	Hi-Z	
000001b	MTIOC2A	MTIOC2B
000101b	TMO1	TMCI3
001010b	TXD1 SMOSI1 SSDA1	SCK1
001011b	CTS3# RTS3#	—

—: Do not specify this value.

3.2.4 P3n Pin Function Control Register (P3nPFS) (n = 0, 1, 4)

Address(es): P30PFS 0008 C158h, P31PFS 0008 C159h, P34PFS 0008 C15Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 3.4.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0-DS P31: IRQ1-DS P34: IRQ4	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 3.4 Register Settings for Input/Output Pin Function

	Pin		
PSEL[5:0] Settings	**P30**	**P31**	**P34**
000000b (initial value)	Hi-Z		
000001b	MTIOC4B	MTIOC4D	MTIOC0A
000101b	TMRI3	TMCI2	TMCI3
000111b	POE8#	—	POE10#
001010b	RXD1 SMISO1 SSCL1	—	SCK6
001011b	—	CTS1# RTS1# SS1#	—
010001b	—	—	ET0_LINKSTA

—: Do not specify this value.

3.2.5 P4n Pin Function Control Register (P4nPFS) (n = 0 to 3)

Address(es): P40PFS 0008 C160h, P41PFS 0008 C161h, P42PFS 0008 C162h, P43PFS 0008 C163h

	b7	b6	b5	b4	b3	b2	b1	b0
	ASEL	ISEL	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin P40: IRQ8-DS P41: IRQ9-DS P42: IRQ10-DS P43: IRQ11-DS	R/W
b7	ASEL	Analog Function Select	0: Used other than as analog pin. 1: Used as analog pin. P40: AN000 P41: AN001 P42: AN002 P43: AN003	R/W

3.2.6 P8n Pin Function Control Register (P8nPFS) (n = 0 to 2)

Address(es): P80PFS 0008 C180h, P81PFS 0008 C181h, P82PFS 0008 C182h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 3.5.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Table 3.5 Register Settings for Input/Output Pin Function

	Pin		
PSEL[5:0] Settings	**P80**	**P81**	**P82**
000000b (initial value)	Hi-Z		
000001b	MTIOC3B	MTIOC3D	MTIOC4A
001010b	SCK10	RXD10 SMISO10 SSCL10	TXD10 SMOSI10 SSDA10
001011b	RTS10#	—	—
010010b	RMII0_TXD_EN	RMII0_TXD0	RMII0_TXD1
011010b	SDHI_WP	SDHI_CD	—

—: Do not specify this value.

3.2.7 PAn Pin Function Control Register (PAnPFS) (n = 1 to 4)

Address(es): PA1PFS 0008 C191h, PA2PFS 0008 C192h, PA3PFS 0008 C193h, PA4PFS 0008 C194h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 3.6.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin PA1: IRQ11 PA3: IRQ6-DS PA4: IRQ5-DS	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 3.6 Register Settings for Input/Output Pin Function

	Pin			
PSEL[5:0] Settings	**PA1**	**PA2**	**PA3**	**PA4**
000000b (initial value)	Hi-Z			
000001b	MTIOC0B	—	MTIOC0D	MTIC5U
000010b	MTCLKC	—	MTCLKD	MTCLKA
000011b	TIOCB0	—	TIOCD0	TIOCA1
000100b	—	—	TCLKB	—
000101b	—	—	—	TMRI0
001000b	MTIOC7B	MTIOC7A	—	—
001010b	SCK5	RXD5 SMISO5 SSCL5	RXD5 SMISO5 SSCL5	TXD5 SMOSI5 SSDA5
010001b	ET0_WOL	—	ET0_MDIO	ET0_MDC

—: Do not specify this value.

3.2.8 PBn Pin Function Control Register (PBnPFS) (n = 0 to 7)

Address(es): PB0PFS 0008 C198h, PB1PFS 0008 C199h, PB2PFS 0008 C19Ah, PB3PFS 0008 C19Bh, PB4PFS 0008 C19Ch, PB5PFS 0008 C19Dh, PB6PFS 0008 C19Eh, PB7PFS 0008 C19Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 3.7.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ12 PB1: IRQ4-DS	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 3.7 Register Settings for Input/Output Pin Function

	Pin							
PSEL[5:0] Settings	**PB0**	**PB1**	**PB2**	**PB3**	**PB4**	**PB5**	**PB6**	**PB7**
000000b (initial value)	Hi-Z							
000001b	MTIC5W	MTIOC0C	—	MTIOC0A	—	MTIOC2A	MTIOC3D	MTIOC3B
000010b	—	MTIOC4C	—	MTIOC4A	—	MTIOC1B	—	—
000011b	TIOCA3	TIOCB3	TIOCC3	TIOCD3	TIOCA4	TIOCB4	TIOCA5	TIOCB5
000100b	—	—	TCLKC	TCLKD	—	—	—	—
000101b	—	TMCI0	—	TMO0	—	TMRI1	—	—
000111b	—	—	—	POE11#	—	POE4#	—	—
001010b	RXD4 SMISO4 SSCL4	TXD4 SMOSI4 SSDA4	CTS4# RTS4# SS4#	SCK4	—	SCK9	RXD9 SMISO9 SSCL9	TXD9 SMOSI9 SSDA9
001011b	RXD6 SMISO6 SSCL6	TXD6 SMOSI6 SSDA6	CTS6# RTS6# SS6#	SCK6	CTS9# RTS9# SS9#	—	—	—
010010b	RMII0_RXD1	RMII0_RXD0	REF50CK0	RMII0_RX_ER	RMII0_TXD_EN	RMII0_TXD0	RMII0_TXD1	RMII0_CRS_DV
100011b	—	—	SDSI_D2	SDSI_D3	SDSI_CMD	SDSI_CLK	SDSI_D0	SDSI_D1
100100b	—	—	—	—	CTS11# RTS11# SS11#	SCK11	RXD11 SMISO11 SSCL11	TXD11 SMOSI11 SSDA11

—: Do not specify this value.

3.2.9 PCn Pin Function Control Register (PCnPFS) (n = 0, 1, 4 to 7)

Address(es): PC0PFS 0008 C1A0h, PC1PFS 0008 C1A1h, PC4PFS 0008 C1A4h, PC5PFS 0008 C1A5h, PC6PFS 0008 C1A6h, PC7PFS 0008 C1A7h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 3.8.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin PC0: IRQ14 PC1: IRQ12 PC6: IRQ13 PC7: IRQ14	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 3.8 Register Settings for Input/Output Pin Function

	Pin					
PSEL[5:0] Settings	**PC0**	**PC1**	**PC4**	**PC5**	**PC6**	**PC7**
000000b (initial value)	Hi-Z					
000001b	MTIOC3C	MTIOC3A	MTIOC3D	MTIOC3B	MTIOC3C	MTIOC3A
000010b	—	—	MTCLKC	MTCLKD	MTCLKA	MTCLKB
000011b	TCLKC	TCLKD	—	—	—	—
000101b	—	—	TMCI1	TMRI2	TMCI2	TMO2
000111b	—	—	POE0#	—	—	CACREF
001010b	—	SCK5	SCK5	SCK8	RXD8 SMISO8 SSCL8	TXD8 SMOSI8 SSDA8
001011b	CTS5# RTS5# SS5#	—	CTS8# RTS8# SS8#	—	—	—
001101b	SSLA1	SSLA2	SSLA0	RSPCKA	MOSIA	MISOA
011101b	—	—	—	—	TIC0	TOC0
100100b	—	—	CTS10# RTS10# SS10#	SCK10	RXD10 SMISO10 SSCL10	TXD10 SMOSI10 SSDA10

—: Do not specify this value.

3.2.10 PDn Pin Function Control Register (PDnPFS) (n = 2 to 7)

Address(es): PD2PFS 0008 C1AAh, PD3PFS 0008 C1ABh, PD4PFS 0008 C1ACh, PD5PFS 0008 C1ADh, PD6PFS 0008 C1AEh, PD7PFS 0008 C1AFh

	b7	b6	b5	b4	b3	b2	b1	b0
	ASEL	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 3.9.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin PD2: IRQ2 PD3: IRQ3 PD4: IRQ4 PD5: IRQ5 PD6: IRQ6 PD7: IRQ7	R/W
b7	ASEL	Analog Function Select	0: Used other than as analog pin. 1: Used as analog pin. PD2: AN110 PD3: AN111 PD4: AN112 PD5: AN113 PD6: AN106 PD7: AN107	R/W

Table 3.9 Register Settings for Input/Output Pin Function

	Pin					
PSEL[5:0] Settings	**PD2**	**PD3**	**PD4**	**PD5**	**PD6**	**PD7**
000000b (initial value)	Hi-Z					
000001b	MTIOC4D	—	—	MTIC5W	MTIC5V	MTIC5U
000111b	—	POE8#	POE11#	POE10#	POE4#	POE0#
001000b	—	MTIOC8D	MTIOC8B	MTIOC8C	MTIOC8A	—
011010b	SDHI_D2	SDHI_D3	SDHI_CMD	SDHI_CLK	SDHI_D0	SDHI_D1
011011b	QIO2	QIO3	QSSL	QSPCLK	QIO0 QMO	QIO1 QMI
011101b	TIC2	TOC2	—	—	—	—

—: Do not specify this value.

3.2.11 PEn Pin Function Control Register (PEnPFS) (n = 0 to 2, 4 to 7)

Address(es): PE0PFS 0008 C1B0h, PE1PFS 0008 C1B1h, PE2PFS 0008 C1B2h, PE4PFS 0008 C1B4h, PE5PFS 0008 C1B5h, PE6PFS 0008 C1B6h, PE7PFS 0008 C1B7h

	b7	b6	b5	b4	b3	b2	b1	b0
	ASEL	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For individual pin functions, see Table 3.10.	R/W
b6	ISEL	Interrupt Input Function Select	0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7-DS PE5: IRQ5 PE6: IRQ6 PE7: IRQ7	R/W
b7	ASEL	Analog Function Select	0: Used other than as analog pin. 1: Used as analog pin. PE0: ANEX0 PE1: ANEX1 PE2: AN100 PE4: AN102 PE5: AN103 PE6: AN104 PE7: AN105	R/W

Table 3.10 Register Settings for Input/Output Pin Function

	Pin						
PSEL[5:0] Settings	**PE0**	**PE1**	**PE2**	**PE4**	**PE5**	**PE6**	**PE7**
000000b (initial value)	Hi-Z						
000001b	—	MTIOC4C	MTIOC4A	MTIOC4D	MTIOC4C	—	—
000010b	—	—	—	MTIOC1A	MTIOC2B	—	—
001000b	MTIOC3D	MTIOC3B	—	—	—	MTIOC6C	MTIOC6A
001100b	SCK12	TXD12 SSDA12 TXDX12 SIOX12	RXD12 SSCL12 RXDX12	—	—	—	—
001101b	SSLB1	SSLB2	SSLB3	SSLB0	RSPCKB	MOSIB	MISOB
010010b	—	—	—	—	REF50CK0	—	—
011010b	—	—	—	—	—	SDHI_CD	SDHI_WP
011101b	—	—	TIC3	—	—	TIC1	TOC1

—: Do not specify this value.

3.2.12 Ethernet Control Register (PFENET)

Address(es): 0008 C10Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PHYMODE0	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	PHYMODE0	Ethernet Channel 0 Mode Set	0: RMII mode (ETHERC0)	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

PHYMODE0 Bit (Ethernet Channel 0 Mode Set)

This bit specifies the PHY mode of the ETHERC0.

Select the same mode as the one specified by the pin function select bits (PmnPFS.PSEL[5:0]).

When the signals for the RMII mode have been specified by the PmnPFS.PSEL[5:0] bits, set the PHYMODE bit to 0 (RMII mode).

3.3 Usage Notes

3.3.1 Procedure for Specifying Input/Output Pin Function

Use the following procedure to specify the input/output pin functions.

(1) Clear the port mode register (PMR) for the target pin to 0 to select the general I/O port.
(2) Specify the assignments of input/output signals for peripheral modules to the desired pins.
(3) Enable writing to the Pmn pin function control register (PmnPFS) through the write-protect register (PWPR) setting. (m = 1 to 5, 8, and A to E, n = 0 to 7)
(4) Specify the input/output function for the pin through the PSEL[5:0] bit settings in the PmnPFS register. Only set the PmnPFS registers that control the pin functions present in the product in use.
(5) Clear the PFSWE bit in the PWPR register to 0 to disable writing to the PmnPFS register.
(6) Set the PMR to 1 as necessary to switch to the selected input/output function for the pin.

3.3.2 Notes on MPC Register Setting

(1) Settings of the Pmn pin function control register (PmnPFS) should be made only while the PMR register for the target pin is set to 0. If the PmnPFS register is set while the PMR register is 1, unexpected edges may be input through the input pin or unexpected pulses are output through the output pin.
(2) Only the allowed values (functions) should be specified in the Pmn pin function control registers. If a value that is not allowed for the register is specified, correct operation is not guaranteed.
(3) Do not assign a single function to multiple pins through the MPC settings.
(4) Ports 4, D, and E also function as analog Input/output pins for the A/D converter. When using these ports as analog Input/output pins, set them to general input pins by clearing the corresponding bits in the port mode register (PMR) and port direction register (PDR) to 0 and set the PmnPFS.ASEL bit to 1, to avoid degradation of accuracy.
(5) The initial value of the time capture event input pin enable bit (TCEN) of the time capture control register y (RTCCRy, y = 0 to 2) is undefined after a reset. Therefore, set this bit to 0 to avoid unnecessary input.
(6) Points to note regarding the port mode register (PMR), port direction register (PDR), and the PmnPFS register settings for pins that have multiplexed pin functions are listed in Table 3.11. The pin states are readable if the value of the ASEL bit is 0. Ensure that the PMR.Bj bit is 0 when changes to the PSEL[5:0] bits are made.

Table 3.11 Register Settings

Item	PMR.Bn	PDR.Bn	PmnPFS			Point to Note
			ASEL	ISEL	PSEL[5:0]	
After a reset	0	0	0	0	000000b	Pins function as general input port pins after release from the reset state.
General input ports	0	0	0	0/1	x	Set the PmnPFS.ISEL bit to 1 if these are multiplexed with interrupt inputs.
General output ports	0	1	0	0	x	
Peripheral functions	1	x	0	0/1	Peripheral functions (see Table 3.2 to Table 3.10)	Set the PmnPFS.ISEL bit to 1 if these are multiplexed with interrupt inputs.
Interrupt inputs	0	0	0	1	x	
NMI	x	x	x	x*1	x	Register settings are not required.
Analog inputs and outputs	0	0	1	x*1	x	Set these as general input port pins so that the output buffers are turned off.
Time-capture event-input pins	0	0	x	0/1	x	Set these as general input port pins so that the output buffers are turned off.
JTAG interface	0	x	x	0	x	Set the PMR.Bn bit and the PmnPFS.ISEL bit to 0 and switch the input buffers off.
FINE interface	0	x	x	0	x	Set the PMR.Bn bit and the PmnPFS.ISEL bit to 0 and switch the input buffers off.
EXTAL/XTAL	0	0	x	x*1	x	Set these as general input port pins so that the output buffers are turned off.

x: Setting not required.
0/1: Setting the PmnPFS.ISEL bit to 0 makes the pin incapable of functioning as an IRQ pin.
Setting the PmnPFS.ISEL bit to 1 makes the pin capable of functioning as an IRQ pin (When a IRQ is assigned).
Note 1. Even if the PmnPFS.ISEL bit is set to 1, the pin will not function as an IRQn input pin.

Note:
- The pin state is readable when the PmnPFS.ASEL bit is 0.
- If the value of the PmnPFS.PSEL[5:0] bits is to be changed, do so while the PMR.Bn bit is 0.
- If an RIIC function is assigned to a port pin, clear the PMR.Bn (to 0); pulling up is automatically turned off for outputs from peripheral modules other than the RIIC.
- If an input pin for time-capture events is not in use, clear the time capture event input pin enable bit (TCEN) in time capture control register y (RTCCRy) (y = 0 to 2) to 0 (disabled). The value of the RTCCRy.TCEN bit after a reset is undefined.

3.3.3 Notes on the Use of Analog Functions

To use an analog function, set the corresponding bits in both the port mode register (PMR) and port direction register (PDR) to 0 so that the pin acts as a general input port. After that, set the pin function select bit in the Pmn pin function control register (PmnPFS.ASEL) to 1.

4. Boundary Scan

This MCU has boundary scan function.
The boundary scan is a serial I/O interface based on the JTAG (Joint Test Action Group, IEEE Std.1149.1 and IEEE Standard Test Access Port and Boundary-Scan Architecture).

4.1 Overview

Table 4.1 lists the specifications of boundary scan.
Figure 4.1 shows a block diagram of the boundary scan function.

Table 4.1 Specifications of Boundary Scan

Item	Description
Boundary scan enabled/disabled	Boundary scan is enabled when the RES# pin and the BSCANP pin are driven high and the EMLE pin is driven low.
Dedicated boundary scan pins	The following pins are dedicated for the JTAG, when boundary scan function is enabled (TDO/TCK/TDI/TMS/TRST#). P26/P27/P30/P31/P34
Six test modes	• BYPASS mode • EXTEST mode • SAMPLE/PRELOAD mode • CLAMP mode • HIGHZ mode • IDCODE mode

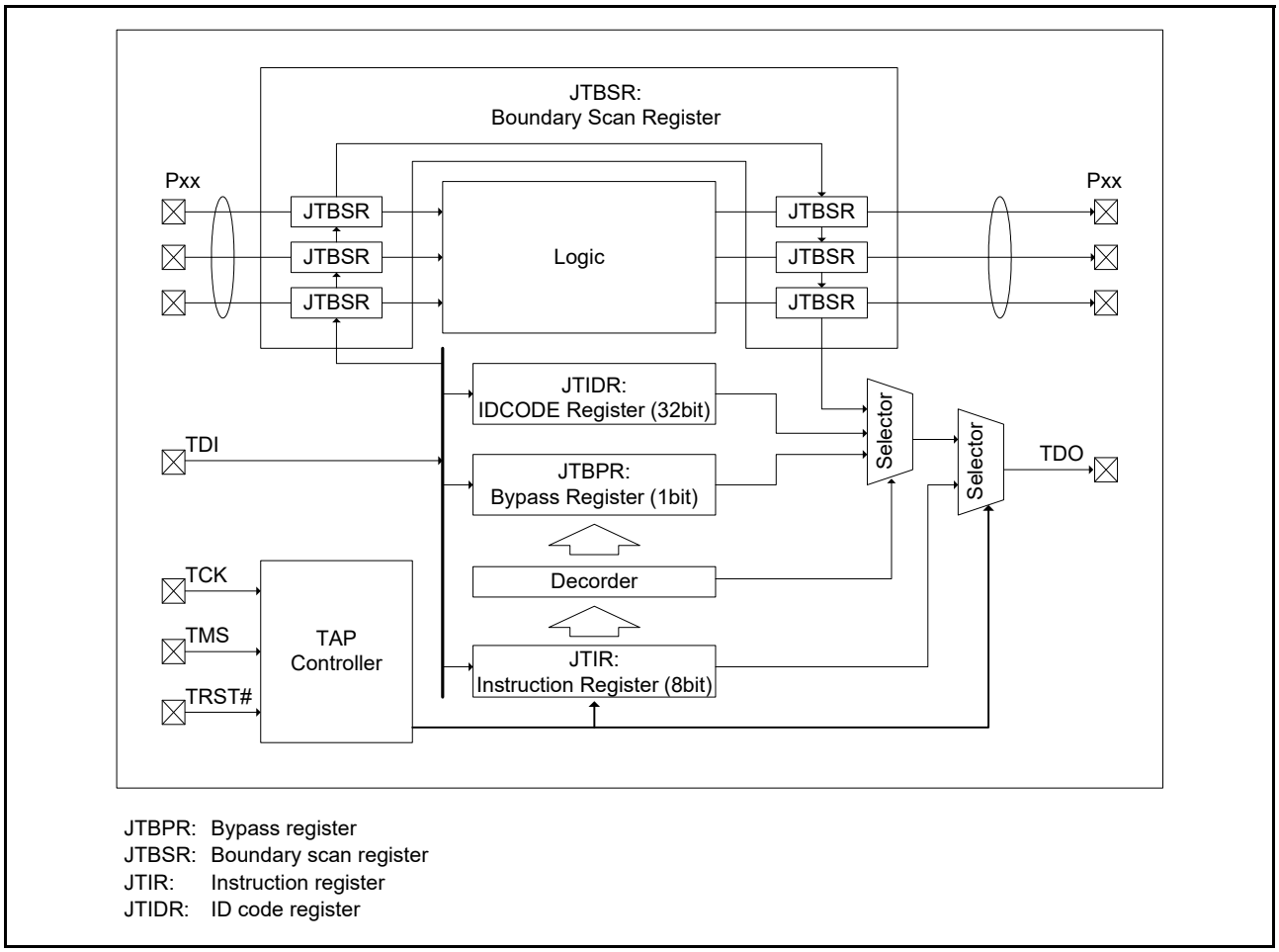


Figure 4.1 Block Diagram of JTAG

Table 4.2 shows the I/O pins used in the boundary scan function.

Table 4.2 Pin Configuration

Pin Name	I/O	Description
TCK	Input	Test clock input pin Clock signal for boundary scan. Input the clock the duty cycle of which is 50 percent when boundary scan function is used.
TMS	Input	Test mode select pin
TDI	Input	Test data input pin
TDO	Output	Test data output pin
TRST#	Input	Test reset input pin

4.2 Register Descriptions

Table 4.3 lists the boundary scan registers.

Table 4.3 List of Boundary Scan Registers

Register Name	Symbol	Value after Reset
Instruction register	JTIR	55h
ID code register	JTIDR	0835 9447h
Bypass register	JTBPR	Undefined
Boundary scan register	JTBSR	Undefined

Instructions can be input to the JTIR register via the TDI pin by serial transfer.
The JTBPR register, which is a 1-bit register, is connected between the TDI and TDO pins in BYPASS mode.
The JTBSR register, which is configured according to Table 4.6, is connected between the TDI and TDO pins when test data are being shifted in.
None of the registers is accessible from the CPU.
Table 4.4 shows the availability of serial transfer for the registers.

Table 4.4 Serial Transfer for the Registers

Register Name	Serial Input	Serial Output
Instruction register (JTIR)	Available	Available
ID code register (JTIDR)	Available	Available
Bypass register (JTBPR)	Available	Available
Boundary scan register (JTBSR)	Available	Available

4.2.1 Instruction Register (JTIR)

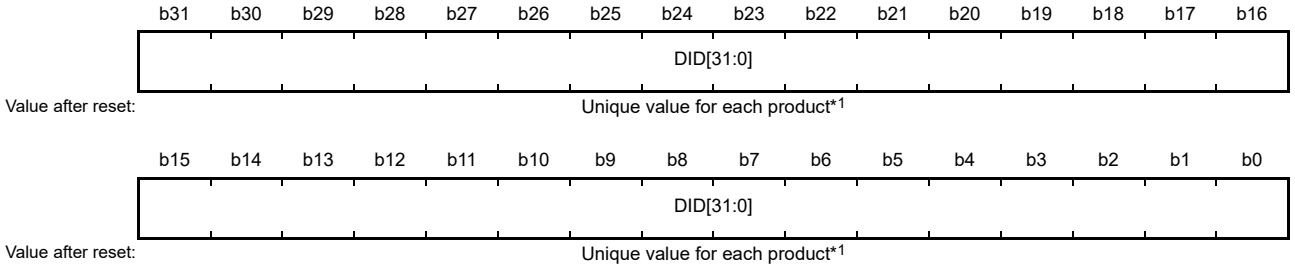
Bit	Symbol	Bit Name	Description	R/W
b7 to b0	TS[7:0]	Test Bit Set	The command configuration is as shown in Table 4.5.	—

Table 4.5 Command Configuration

TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0	Instruction
0	0	0	0	0	0	0	0	EXTEST
0	1	0	0	0	0	0	0	SAMPLE/PRELOAD
0	1	0	1	0	1	0	1	IDCODE (initial value)
1	1	0	1	0	0	0	0	CLAMP
1	0	0	0	0	0	0	0	HIGHZ
1	1	1	1	1	1	1	1	BYPASS
Other than above								Reserved

JTAG instructions can be transferred to the JTIR register by serial input from the TDI pin.
The JTIR register is initialized when the TRST# pin is driven low, or when the TAP controller is in the Test-Logic-Reset state.

4.2.2 ID Code Register (JTIDR)



Bit	Symbol	Bit Name	Description	R/W
b31 to b0	DID[31:0]	Reserved	JTIDR is a register with the fixed value that indicates the device IDCODE.	—

Note 1. For the ID code for each product, refer to Table 4.3, List of Boundary Scan Registers.

JTIDR data is output from the TDO pin when the IDCODE instruction has been executed.

4.2.3 Bypass Register (JTBPR)

The JTBPR register is a 1-bit register and is connected between the TDI and TDO pins when the JTIR register is set to BYPASS mode.
The JTBPR register cannot be read from or written to by the CPU.

4.2.4 Boundary Scan Register (JTBSR)

The JTBSR register is a shift register to control the external input and output pins of this MCU and is distributed across the pads.
The EXTEST, SAMPLE/PRELOAD, CLAMP, and HIGHZ instructions are issued to apply the JTBSR register in boundary-scan testing.
Table 4.6 shows the correspondence between the JTBSR bits and the pins of this MCU.
The value after reset is undefined.

Table 4.6 Boundary Scan Register 145-Pin TFBGA (1/3)

Pin No.	Pin Name	Input/Output	Bit Name
From TDI			
L13	MD	Output	381
		Output enable	380
		Input	379
K13	P35	Input	375
F15	P17	Output	323
		Output enable	322
		Input	321
G15	P16	Output	317
		Output enable	316
		Input	315
G14	P13	Output	305
		Output enable	304
		Input	303
F14	P12	Output	302
		Output enable	301
		Input	300
A15	P53	Output	266
		Output enable	265
		Input	264
D13	PC7	Output	251
		Output enable	250
		Input	249
C14	PC6	Output	248
		Output enable	247
		Input	246
B14	PC5	Output	245
		Output enable	244
		Input	243
A14	P82	Output	242
		Output enable	241
		Input	240
C13	P81	Output	239
		Output enable	238
		Input	237
B13	P80	Output	236
		Output enable	235
		Input	234
A13	PC4	Output	233
		Output enable	232
		Input	231
F13	PC1	Output	212
		Output enable	211
		Input	210

Table 4.6 Boundary Scan Register 145-Pin TFBGA (2/3)

Pin No.	Pin Name	Input/Output	Bit Name
E14	PC0	Output	209
		Output enable	208
		Input	207
N4	PB7	Output	203
		Output enable	202
		Input	201
P4	PB6	Output	200
		Output enable	199
		Input	198
P5	PB5	Output	197
		Output enable	196
		Input	195
N6	PB4	Output	194
		Output enable	193
		Input	192
N5	PB3	Output	191
		Output enable	190
		Input	189
P6	PB2	Output	188
		Output enable	187
		Input	186
P9	PB1	Output	185
		Output enable	184
		Input	183
P8	PB0	Output	176
		Output enable	175
		Input	174
N7	PA4	Output	164
		Output enable	163
		Input	162
P7	PA3	Output	161
		Output enable	160
		Input	159
R8	PA2	Output	155
		Output enable	154
		Input	153
N8	PA1	Output	149
		Output enable	148
		Input	147
A12	PE7	Output	122
		Output enable	121
		Input	120
B12	PE6	Output	119
		Output enable	118
		Input	117

Table 4.6 Boundary Scan Register 145-Pin TFBGA (3/3)

Pin No.	Pin Name	Input/Output	Bit Name
B11	PE5	Output	113
		Output enable	112
		Input	111
A10	PE4	Output	110
		Output enable	109
		Input	108
R9	PE2	Output	104
		Output enable	103
		Input	102
E13	PE1	Output	101
		Output enable	100
		Input	99
D14	PE0	Output	98
		Output enable	97
		Input	96
R10	PD7	Output	80
		Output enable	79
		Input	78
N9	PD6	Output	74
		Output enable	73
		Input	72
P10	PD5	Output	68
		Output enable	67
		Input	66
N10	PD4	Output	65
		Output enable	64
		Input	63
N11	PD3	Output	59
		Output enable	58
		Input	57
P11	PD2	Output	53
		Output enable	52
		Input	51
R11	P43	Output	14
		Output enable	13
		Input	12
N12	P42	Output	11
		Output enable	10
		Input	9
P12	P41	Output	8
		Output enable	7
		Input	6
N13	P40	Output	5
		Output enable	4
		Input	3
To TDO			

4.3 Operations

The boundary scan functionality is valid when the RES# pin is driven high, the EMLE pin is driven low, and the BSCANP pin is driven high.

4.3.1 TAP Controller

Figure 4.2 shows the state transition diagram of the TAP controller.

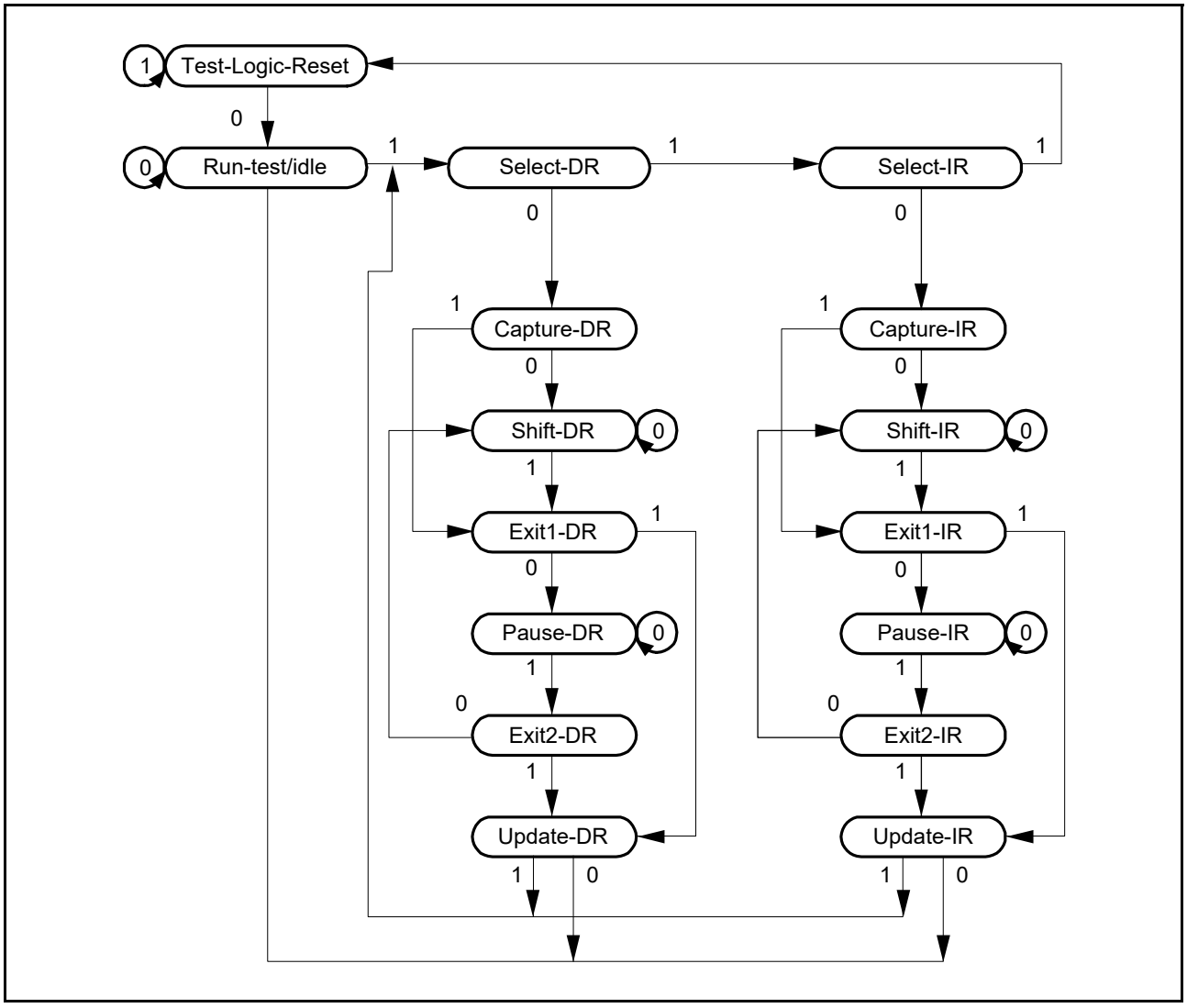


Figure 4.2 State Transition Diagram of TAP Controller

4.3.2 List of Commands

(1) BYPASS [Instruction Code: 1111 1111b]

The BYPASS instruction is an instruction that drives the bypass register (JTBPR). This instruction shortens the shift path, facilitating the transfer of serial data to other LSIs on a printed-circuit board at higher speeds. While this instruction is being executed, the test circuit has no effect on the system circuits.
The bypass register (JTBPR) is connected between the TDI and TDO pins. Bypass operation is initiated from shift-DR operation. The TDO is low in the first clock cycle in the shift-DR state; in the subsequent clock cycles, the TDI signal is output on the TDO pin.

(2) EXTEST [Instruction Code: 0000 0000b]

The EXTEST instruction is used to test external circuits when this LSI is installed on the printed circuit board. If this instruction is executed, output pins are used to output test data (specified by the SAMPLE/PRELOAD instruction) from the boundary scan register to the print circuit board, and input pins are used to input test result.

(3) SAMPLE/PRELOAD [Instruction Code: 0100 0000b]

The SAMPLE/PRELOAD instruction is used to input data from the LSI internal circuits to the boundary scan register, output data from scan path, and reload the data to the scan path. While this instruction is executed, input signals are directly input to the LSI and output signals are also directly output to the external circuits. The LSI system circuit is not affected by this instruction.
In SAMPLE operation, the boundary scan register latches the snap shot of data transferred from input pins to internal circuit or data transferred from internal circuit to output pins. The latched data is read from the scan path. The scan register latches the snap data at the rising edge of the TCK in Capture-DR state. The scan register latches snap shot without affecting the LSI normal operation.
In PRELOAD operation, initial value is written from the scan path to the parallel output latch of the boundary scan register prior to the EXTEST instruction execution. If the EXTEST is executed without executing this PRELOAD operation, undefined values are output from the beginning to the end (transfer to the output latch) of the EXTEST sequence. (In EXTEST instruction, output parallel latches are always output to the output pins.)

(4) IDCODE [Instruction Code: 0101 0101b]

When the IDCODE instruction is selected, IDCODE register value is output to the TDO in Shift-DR state of the TAP controller. In this case, IDCODE register value is output from the LSB. During this instruction execution, test circuit does not affect the system circuit. JTIR is initialized by the IDCODE instruction in Test-Logic-Reset state of the TAP controller.

(5) CLAMP [Instruction Code: 1101 0000b]

When the CLAMP instruction is selected, output pins output the boundary scan register value which was specified by the SAMPLE/PRELOAD instruction in advance. While the CLAMP instruction is selected, the status of boundary scan register is maintained regardless of the TAP controller state.
BYPASS is connected between TDI and TDO, the same operation as BYPASS instruction can be achieved.

(6) HIGHZ [Instruction Code: 1000 0000b]

When the HIGHZ instruction is selected, all output pins enter high-impedance state. While the HIGHZ instruction is selected, the status of boundary scan register is maintained regardless of the state of the TAP controller.
BYPASS is connected between TDI and TDO pins, leading to the same operation as when the BYPASS instruction has been selected.

4.4 Usage Notes

(1) Pin serial transfer, data are input or output in LSB order (refer to Figure 4.3).

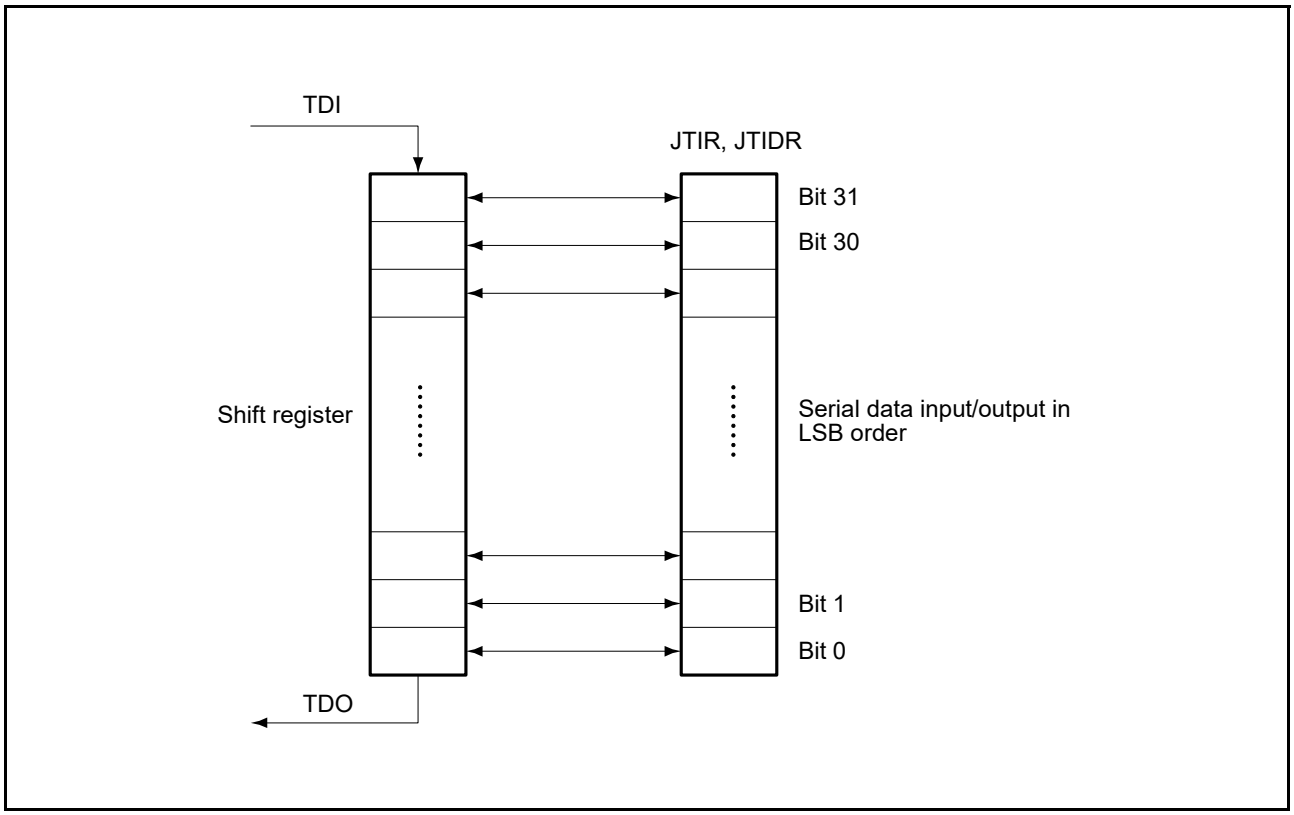


Figure 4.3 Serial Data Input/Output

(2) Pins of the boundary scan (TCK, TDI, TMS, and TRST#) have to be pulled up by pull-up resistors. However, handle the TRST# pin in the way described in the manual for the given on-chip emulator if an on-chip emulator is in use. If the TRST# pin is pulled down but a boundary scan is to proceed, ensure that the TRST# pin is also controllable.

(3) The power supply pins (VCC, VCL, VSS, AVCC0, AVCC1, AVSS0, AVSS1, VCC_USB, VSS_USB, VCC_DA, VCC_RF, VCC_A, VCC_DDC, VSS_DDC, and VCC_D) are not covered by boundary scan.

(4) The analog reference pins (VREFH0, VREFL0, and VBATT) are not covered by boundary scan.

(5) The clock pins (EXTAL, XTAL, XCIN, and XCOUT) are not covered by boundary scan.

(6) The reset pin (RES#) is not covered by boundary scan.

(7) The USB dedicated pins (USB0_DP and USB0_DM) are not covered by boundary scan.

(8) The on-chip emulator enable pin (EMLE) is not covered by boundary scan.

(9) The boundary scan enable pin (BSCANP) is not covered by boundary scan.

(10) The boundary scan pins (TCK, TMS, TRST#, TDI, and TDO) are not covered by boundary scan.

(11) The RF transceiver pins, shown in Table 1.4, Pin Functions, are not covered by boundary scan.

(12) The boundary-scan facility is not available when the chip is in the states below.

- Reset state
- Software standby or deep software standby

(13) For a pin that incorporates open-drain functionality and for which the open-drain function is enabled, if the boundary-scan function sets the corresponding bit in the output scan register and output enable register to 1, executing an EXTEST, CLAMP, or SAMPLE/PRELOAD instruction makes the pin output the high level rather than placing it in the high-impedance state.

(14) Be sure to satisfy the standards for the boundary scan function when multiplex ports are used. Figure 4.4 (1) shows the pin configuration of the port pins on which the RIIC pin functions (P12, P13, P16, and P17) are multiplexed. When the boundary scan function is to be used while pins P12, P13, P16, and P17 are in use as the RIIC pins (SCL0[FM+], SCL2, SDA0[FM+], and SDA2), contention with the open-drain outputs or sneak current might be generated.

(15) Figure 4.4 (2) shows the pin configuration of the pins P40 to P43, PD2 to PD7, PE0 to PE2, and PE4 to PE7. When the boundary scan function is used with pins P40 to P43, PD2 to PD7, PE0 to PE2, and PE4 to PE7 to be used as AD input pins (AN000 to AN003, ANEX0, ANEX1, AN100, AN102 to AN107, and AN110 to AN113), the conflict with the AD input or sneak current might be generated.

(16) The HIGHZ mode option of the MD pin is not available.

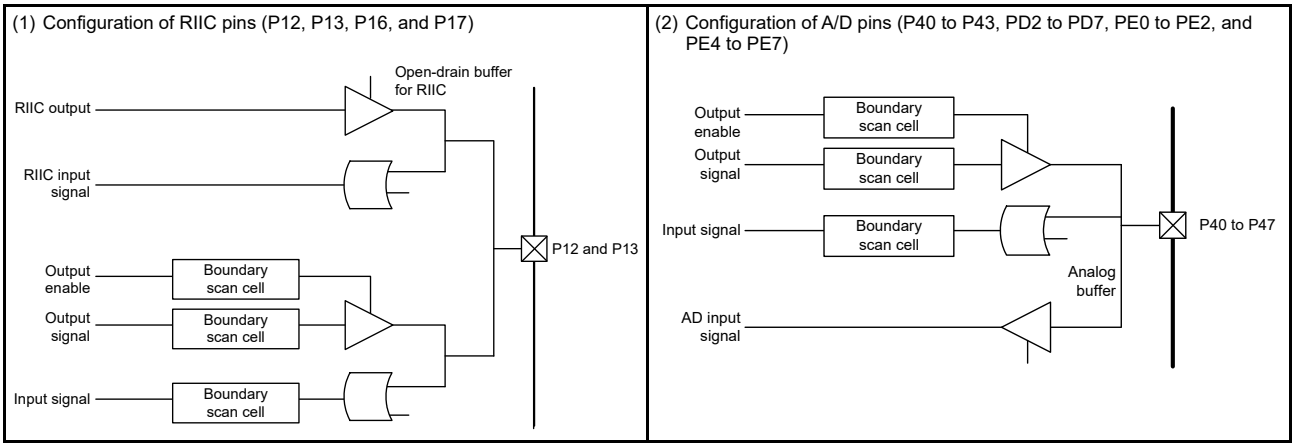


Figure 4.4 Pin Configuration

5. RF Transceiver

Table 5.1 shows the specifications of the RF transceiver. For more details, see the latest user's manual of the RF transceiver (R9A06G062GNP).

5.1 Features

Table 5.1 Specifications of RF Transceiver

Item	Description
Fully integrated radio transceiver	• This fully integrated radio transceiver covers 863 to 928 MHz, which includes the following bands: European band: 863 to 870, and 870 to 876 MHz North American band: 902 to 928 MHz Brazilian band: 902 to 907.5, and 915 to 928 MHz Japanese band: 920 to 928 MHz
Supported types of PHY layer	• SUN FSK Symbol rates: 10, 20, 50, 100, 150, 200 kbps Forward Error Correction (FEC) Modulation methods: 2FSK, GFSK • SUN OFDM Option 1: 100, 200, 400, 800, 1200, 1600, 2400 kbps Option 2: 50, 100, 200, 400, 600, 800, 1200 kbps Option 3: 25, 50, 100, 200, 300, 400, 600 kbps Option 4: 12.5, 25, 50, 100, 150, 200, 300 kbps
MAC	• 32-bit timer • Transmission RAM, reception RAM: 2 Kbytes each • Interrupt • 16- or 32-bit auto CRC • Address filtering with automatic acknowledgement reply • Antenna diversity • Auto CSMA-CA
Transceiver control interface	• Serial peripheral interface (SPI)
Radio transceiver features	• Programmable TX output power up to +15 dBm SUN FSK • Programmable TX output power up to +11 dBm SUN OFDM • Receiver sensitive down to –109 dBm in 50-kbps SUN FSK • Receiver sensitive down to –119 dBm in option-4 MCS0 SUN OFDM • Received signal strength indicator, energy detection • Internal voltage regulators • Operating voltage: 2.7 to 3.6 V • Low power consumption (incl. for baseband processing) Standby: 0.5 µA RX active: 16.7 mA for SUN FSK (2GFSK) at 100 kbps RX active: 21.5 mA for SUN OFDM, option1, MCS6 TX active: 62.0 mA for SUN FSK at +15-dBm output power TX active: 68.0 mA for SUN OFDM at +10-dBm output power

5.2 Applications

- Smart meter (Electricity, gas, water) supporting products
  IEEE 802.15.4, Wi-SUN®
- HEMS controller
- Security and building automation
- Industrial monitoring and control
- Wireless sensor networks
- Energy-harvesting applications, and others

5.3 Block Diagram

Figure 5.1 shows a block diagram of the RF transceiver.

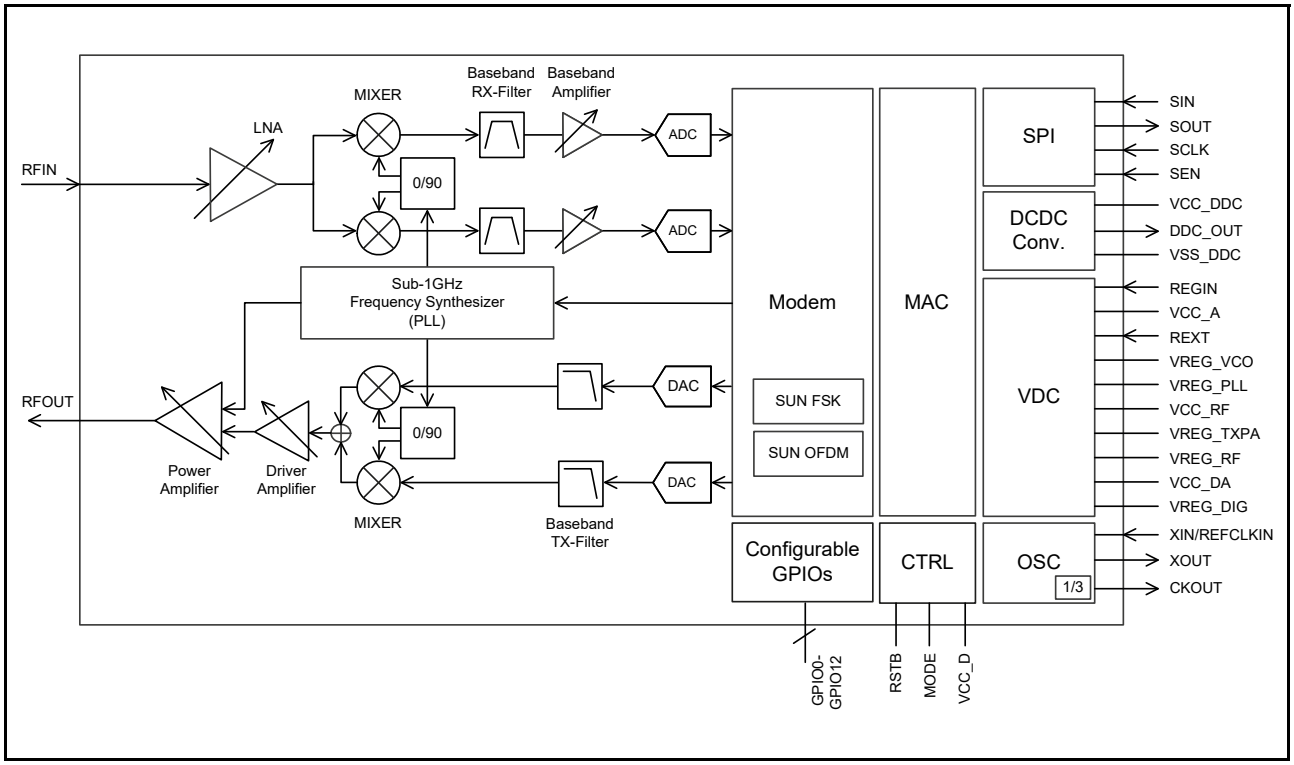


Figure 5.1 Block Diagram of RF Transceiver

(1) Receiver path

The reception architecture applies low intermediate frequency conversion. The received RF signal is amplified by the low-noise amplifier (LNA), and down-converted to the IF range by using orthogonally modulated data I and Q.
The reception path has high linearity, wide dynamic range with programmable gain, and high-level on-chip channel filtering that guarantees robust operation in the sub-GHz frequency band. The auto gain control (AGC) algorithm is realized by using feedback control from the digital circuit that is optimized for high-speed response.
The power detector connected to the outputs of the LNA and baseband amplifiers (BBAs) adjusts the LNA and BBA gains to optimize IM3, frequency channel selectability, and receiver sensitivity.

(2) Transmitter path

The FSK modulation transmitter modulates and synthesizes the RF synthesizer frequency. The RF synthesizer generates the local signal for input to the power amplifier (PA), and the output level is specifiable in 1-dB steps so that the antenna level is within the range from –15 dBm to +15 dBm.
The OFDM modulation transmitter is a zero-IF transmitter in which all circuits required for OFDM modulation transmission are integrated, including a modem and DAC in the digital circuit transmission analog circuit, and a power amplifier. The baseband data for transmission are digitally modulated in the modem block, and up-converted to the sub-GHz frequency band along the transmitter path. The transmitter path handles signal filtering, I/Q up-conversion, high-output power amplification, and RF filtering. The output power level of the result of OFDM modulation is specifiable within the range from –19 dBm to +11 dBm. The maximum output power depends on the modulation and coding scheme (MCS).

(3) Peripheral circuits

- A DC-to-DC converter (DDC) that realizes power conversion efficiency of 87% is incorporated.
- A crystal resonator must be connected between XIN and XOUT for supplying a clock signal to this device. We recommend using the crystal resonator that satisfies the specifications shown in the table below.
  An external clock can also be used to input a suitable signal level to XIN or XOUT.

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Frequency	F_xtal	—	48	—	MHz	
Equivalent series resistance (ESR)	ESR_xtal	—	—	80	Ω	
Load capacitance (CL)	CL_xtal	5	—	9	pF	

- Thirteen GPIO port pins (GPIO0 to GPIO12) are available for use by setting the respective registers.

5.4 Pin Functions

Table 5.2 lists the pin functions.

Table 5.2 Pin Functions

No.	Pin Name	I/O	Analog/Digital	Description
1	SIN	Input	D	Serial input
2	SOUT	Output	D	Serial output
3	SCLK	Input	D	Serial clock
4	SEN	Input	D	Serial enable
5	VREG_DIG	Output	A	Internally regulated analog 1.1-V supply output voltage for digital circuits
6	GPIO0	I/O	D	General-purpose digital I/O 0
7	GPIO1	I/O	D	General-purpose digital I/O 1
8	GPIO2	I/O	D	General-purpose digital I/O 2
9	GPIO3	I/O	D	General-purpose digital I/O 3
10	GPIO4	I/O	D	General-purpose digital I/O 4
11	GPIO5	I/O	D	General-purpose digital I/O 5
12	GPIO6	I/O	D	General-purpose digital I/O 6
13	GPIO7	I/O	D	General-purpose digital I/O 7
14	GPIO8	I/O	D	General-purpose digital I/O 8
15	VCC_DA	Input	A	3.3-V power supply voltage for the digital and analog circuits
16	GPIO9	I/O	D	General-purpose digital I/O 9
17	GPIO10	I/O	D	General-purpose digital I/O 10
18	VREG_RF	Output	A	Internally regulated analog 1.1-V supply output voltage for RF section
19	GPIO11	I/O	D	General-purpose digital I/O 11
20	GPIO12	I/O	D	General-purpose digital I/O 12
21	RFIN	Input	A	RX input
22	VSS	Input	A	Ground pin for the digital circuit and RF transceiver. Connect it to the system power supply (0 V).
23	RFOUT	Output	A	TX output
24	VREG_TXPA	Output	A	Internally regulated analog 1.1-V supply output voltage for the power amplifier (PA)
25	VCC_RF	Input	A	3.3-V RF power supply voltage
26	VREG_PLL	Output	A	Internally regulated analog 1.1-V supply output voltage for PLL
27	VREG_VCO	Output	A	Internally regulated analog 1.1-V supply output voltage for VCO
28	REXT	Input	A	External reference resistor connection port
29	VCC_A	Input	A	3.3-V power supply voltage for the analog circuits
30	XIN	Input	A	Crystal oscillator input
31	XOUT	I/O	A	Crystal oscillator output
32	CKOUT	Output	A	Clock output (16 MHz)
33	REGIN	Input	A	1.4- to 1.8-V DDC_OUT voltage input
34	VSS_DDC	Input	A	DC-to-DC converter ground
35	DDC_OUT	Output	A	1.4- to 1.8-V DC-to-DC converter output voltage
36	VCC_DDC	Input	A	3.3-V DC-to-DC converter power supply voltage
37	VCC_D	Input	A	3.3-V power supply voltage for the digital circuits
38	RSTB	Input	D	Reset-bar input (active-low)
39	MODE	Input	D	Mode switch (always low)

5.5 Compliant Standard

This MCU is compliant with the following standard.
IEEE Std 802.15.4™ -2020: IEEE Standard for Low-Rate Wireless Networks

Table 5.3 SUN FSK

Data Rate [kbps]	Modulation Method	Modulation Index	Descriptions
10	2-GFSK	1.0	
20	2-GFSK	1.0	
50	2-GFSK	0.5	
50	2-GFSK	1.0	
100	2-GFSK	0.5	
100	2-GFSK	1.0	
150	2-GFSK	0.5	
200	2-GFSK	0.5	
200	2-GFSK	1.0	

Table 5.4 SUN OFDM

Parameter	Option 1 Bandwidth: 1200 kHz	Option 2 Bandwidth: 800 kHz	Option 3 Bandwidth: 400 kHz	Option 4 Bandwidth: 200 kHz	Unit	Descriptions
MCS0	100	50	25	12.5	kbps	BPSK CR = 1/2 with 4xFreq. repetition
MCS1	200	100	50	25		BPSK CR = 1/2 with 2xFreq. repetition
MCS2	400	200	100	50		QPSK CR = 1/2 with 2xFreq. repetition
MCS3	800	400	200	100		QPSK CR = 1/2
MCS4	1200	600	300	150		QPSK CR = 3/4
MCS5	1600	800	400	200		16-QAM CR = 1/2
MCS6	2400	1200	600	300		16-QAM CR = 3/4

5.6 Usage Notes

5.6.1 SPI External Connection

Connect the RSPI1 pins (PE6, PE7, PE5, and PE4) to the SPI pins (SIN, SOUT, SCLK, and SEN). Figure 5.2 shows an example of the external connections of the SPI.

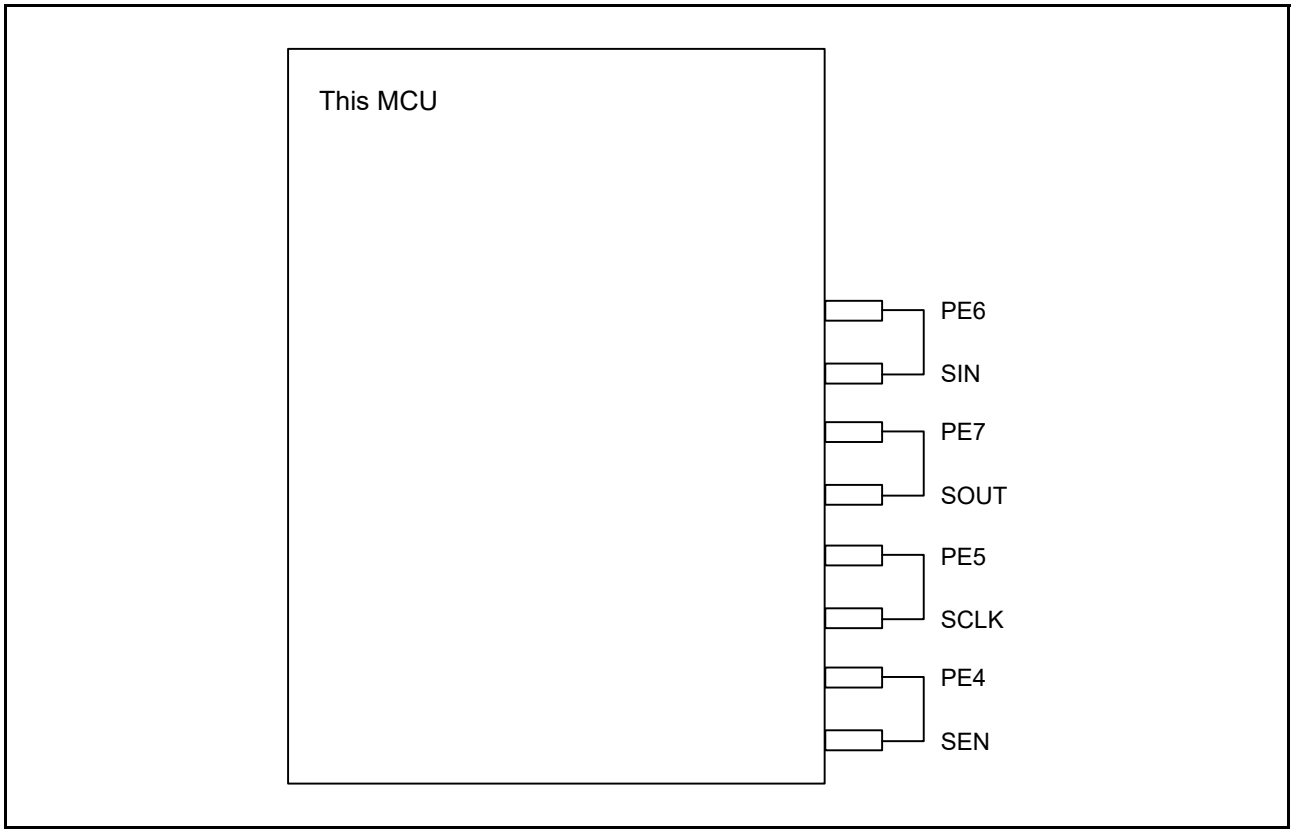
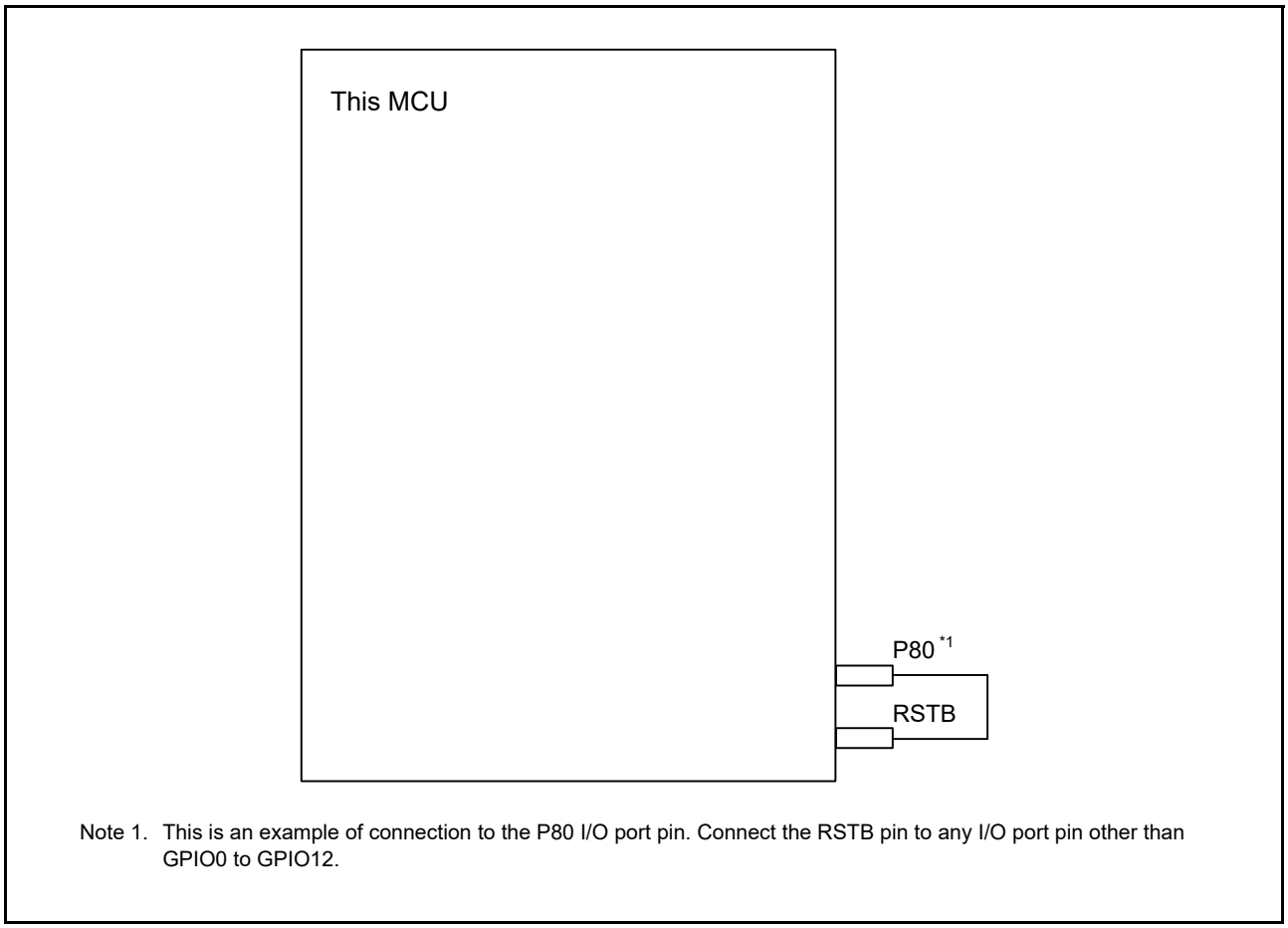


Figure 5.2 Example of the External Connections of the SPI

5.6.2 RSTB External Connection

Connect the RSTB pin to any I/O port pin. Figure 5.3 shows an example of the external connection of the RSTB pin.

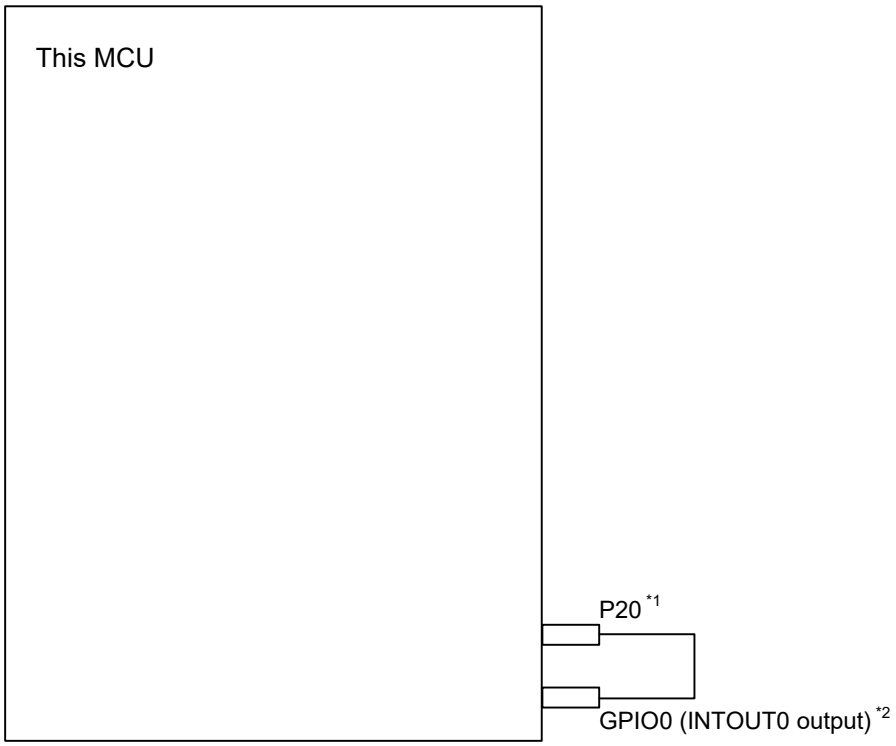


Note 1. This is an example of connection to the P80 I/O port pin. Connect the RSTB pin to any I/O port pin other than GPIO0 to GPIO12.

Figure 5.3 Example of the External Connection of RSTB

5.6.3 External Connection of the INTOUT0 Interrupt Signal

Connect the pin that outputs the INTOUT0 signal to any I/O port pin. Figure 5.4 shows an example of connection of the INTOUT0 interrupt output signal.



Note 1. This is an example of the INTOUT0 connection to the P20 I/O port pin. Connect the INTOUT0 output to any I/O port pin that has an interrupt request function (IRQ).
Note 2. This is an example of connection to GPIO0. Connection should be to any pin from GPIO0 to GPIO12 that has been assigned for use as the INTOUT0 output. For details on the INTOUT0 interrupt output signal, see the latest user's manual of the RF transceiver (R9A06G062GNP).

Figure 5.4 Example of Connection of the INTOUT0 Interrupt Output Signal

5.6.4 Points to Note on Designing the Circuit Board with the RF Transceiver

See the latest user's manual of the RF transceiver (R9A06G062GNP) and Design Guidelines for Circuit Boards with the Sub-GHz Transceiver.

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 6.1 Absolute Maximum Rating

Conditions: VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC, VCC_USB, VCC_DA, VCC_RF, VCC_A, VCC_DDC, VCC_D	–0.3 to +3.8	V
V_{BATT} power supply voltage		V_{BATT}	–0.3 to +3.8	V
Input voltage (except for ports for 5 V tolerant*1)		V_{in}	–0.3 to VCC + 0.3 (up to 3.8)	V
Input voltage (ports for 5 V tolerant*1)		V_{in}	–0.3 to VCC + 4.0 (up to 5.8)	V
Reference power supply voltage		VREFH0	–0.3 to AVCC0 + 0.3 (up to 3.8)	V
Analog power supply voltage		AVCC0, AVCC1*2	–0.3 to +3.8	V
Analog input voltage		V_{AN}	–0.3 to AVCC + 0.3 (up to 3.8)	V
RF Transceiver	Analog input voltage	REGIN	–0.3 to +2.8	V
	Analog output voltage	DDC_OUT	–0.3 to +3.8	V
		VREG_DIG, VREG_RF, VREG_PLL, VREG_VCO	–0.3 to +1.25	V
		VREG_TXPA	–0.3 to +3.8	V
	Voltage on the analog pins	XIN, XOUT, REXT	–0.3 to +1.25	V
	RF input level	RFIN*3	Up to 16	dBm
Junction temperature		T_j	–40 to +105	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. P12, P13, P16, P17, P30, P31, PC0, and PC1 are 5 V tolerant.

Note 2. Connect the AVCC0, AVCC1, and VCC_USB pins to VCC, and the AVSS0, AVSS1, and VSS_USB pins to VSS. When the A/D converter unit 0 is not to be used, connect the VREFH0 pin to VCC and the VREFL0 pin to VSS, respectively. Do not leave these pins open. Insert capacitors of high frequency characteristics between the AVCC0 and AVSS0 pins, or AVCC1 and AVSS1 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces.

Note 3. The listed values are AC ratings. Applying a DC voltage on the RFIN or RFOUT pin is prohibited.

6.2 Recommended Operating Conditions

Table 6.2 Recommended Operating Conditions

Item		Symbol	Min.	Typ.	Max.	Unit
Power supply voltage*1		VCC	2.7	3.3	3.6	V
		VSS	—	0	—	
RF Transceiver	Power supply voltage	VCC_DA	—	VCC	—	V
		VCC_RF	—	VCC	—	
		VCC_A	—	VCC	—	
		VCC_DDC	—	VCC	—	
		VCC_D	—	VCC	—	
		VSS_DDC	—	0	—	
V_{BATT} power supply voltage		V_{BATT}	2.0	—	3.6	V
USB power supply voltage		VCC_USB	—	VCC	—	V
		VSS_USB	—	0	—	
Analog power supply voltage*1, *2		AVCC0	—	VCC	—	V
		AVSS0	—	0	—	
		AVCC1	—	VCC	—	
		AVSS1	—	0	—	
		VREFH0	2.7	—	AVCC0	
		VREFL0	—	0	—	
Input voltage (except for 5 V tolerant ports, except for P40 to P43)*3		V_{in}	–0.3	—	VCC + 0.3	V
Input voltage (P40 to P43)		V_{in}	–0.3	—	AVCC0 + 0.3	V
Input voltage (5 V tolerant: P12, P13, P16, P17, P30, P31, PC0, and PC1)*4		V_{in}	–0.3	—	VCC + 3.6 (up to 5.5)	V
RF Transceiver	Crystal resonator/oscillator oscillation frequency	F_{refclk}	—	48	—	MHz
	Operating frequency	F_{rf}	863	—	928	MHz
	RFIN pin (input impedance)	Z_{in}	—	50	—	Ω
	RFOUT pin (output impedance)	Z_{out}	—	50	—	Ω
Operating temperature		T_{opr}	–40	—	85	°C

Note 1. Comply with the following potential condition:
VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D
Note 2. For details, see section 53.6.11, Voltage Range of Analog Power Supply Pins in the RX65N Group, RX651 Group User's Manual: Hardware.
Note 3. P12, P13, P16, P17, P30, P31, PC0, and PC1 are 5 V tolerant.
Note 4. For P30 and P31, input as follows when the V_{BATT} power supply is selected.
V_{in} Min. = –0.3, Max. = V_{BATT} + 0.3 (V_{BATT} = 2.0 to 3.6 V)

6.3 DC Characteristics

Table 6.3 DC Characteristics (1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin*1 MTU input pin*1 POE3 input pin*1 TPU input pin*1 TMR input pin*1 CMTW input pin*1 SCI input pin*1 CAC input pin*1 ADTRG# input pin*1 QSPI input pin*1 RES#, NMI, TCK	V_{IH}	0.8 × VCC	—	—	V	
		V_{IL}	—	—	0.2 × VCC		
		ΔV_T	0.06 × VCC	—	—		
	RIIC input pin (except for SMBus)	V_{IH}	0.7 × VCC	—	—		
		V_{IL}	—	—	0.3 × VCC		
		ΔV_T	0.05 × VCC	—	—		
	Ports for 5 V tolerant*2	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
	Other input pins excluding ports for 5 V tolerant*3	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
High level input voltage (except for schmitt trigger input pin)	MD pin, EMLE	V_{IH}	0.9 × VCC	—	—	V	
	EXTAL, RSPI input pin, SDHI input pin, SDSI input pin		0.8 × VCC	—	—		
	ETHERC input pin		2.3	—	—		
	RIIC (SMBus)		2.1	—	—		
Low level input voltage (except for schmitt trigger input pin)	MD pin, EMLE	V_{IL}	—	—	0.1 × VCC	V	
	EXTAL, RSPI input pin, ETHERC input pin, SDHI input pin, SDSI input pin		—	—	0.2 × VCC		
	RIIC (SMBus)		—	—	0.8		

Note 1. This does not include the pins, which are multiplexed as ports for 5 V tolerant.
Note 2. P12, P13, P16, P17, P30, P31, PC0, and PC1 are 5 V tolerant.
Note 3. For P30 and P31, input as follows when the V_{BATT} power supply is selected.
V_{IH} Min. = 0.8 × V_{BATT}, V_{IL} Max. = 0.2 × V_{BATT} (V_{BATT} = 2.0 to 3.6 V)

Table 6.4 DC Characteristics (2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 3.3 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
High level input voltage	RSTB, SIN, SCLK, SEN, GPIO0 to GPIO12	V_{IHRF}	2.4	—	VCC	V	
Low level input voltage	RSTB, MODE, SIN, SCLK, SEN, GPIO0 to GPIO12	V_{ILRF}	0	—	0.1 × VCC	V	
High level output voltage	SOUT, GPIO0 to GPIO12	V_{OHRF}	VCC – 0.1	—	VCC	V	I_{OHRF} = 0mA
Low level output voltage	SOUT, GPIO0 to GPIO12	V_{OLRF}	0	—	0.1	V	I_{OLRF} = 0mA
High level output current	SOUT, GPIO0 to GPIO12	I_{OHRF}	—	—	–4	mA	V_{OHRF} = VCC – 0.4V
Low level output current	SOUT, GPIO0 to GPIO12	I_{OLRF}	—	—	4	mA	V_{OLRF} = 0.4V
High level input leakage current 1	RSTB, SIN, SCLK, SEN, GPIO0 to GPIO12	I_{LIHRF1}	—	—	200	µA	V_{in} = VCC
Low level input leakage current 1	SIN, SCLK, SEN, GPIO0 to GPIO12	I_{LILRF1}	—	—	–200	µA	V_{in} = VSS
High level input leakage current 2 (with no pulling-up)	SIN, SCLK, SEN, GPIO0 to GPIO12	I_{LIHRF2}	—	—	10	µA	V_{in} = VCC
Low level input leakage current 2 (with no pulling-up)	SIN, SCLK, SEN, GPIO0 to GPIO12	I_{LILRF2}	—	—	–10	µA	V_{in} = VSS

Table 6.5 DC Characteristics (3)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
High level output voltage	All output pins	V_{OH}	VCC – 0.5	—	—	V	I_{OH} = –1 mA
Low level output voltage	All output pins (except for RIIC pins and ETHERC output pin)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	RIIC output pin		—	—	0.4		I_{OL} = 3.0 mA
			—	—	0.6		I_{OL} = 6.0 mA
	RIIC output pin (only P12 and P13 in channel 0)	V_{OL}	—	—	0.4	V	I_{OL} = 15.0 mA (ICFER.FMPE = 1)
			—	0.4	—		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
	ETHERC output pin	V_{OL}	—	—	0.4	V	I_{OL} = 1.0 mA
Input leakage current	RES#, MD pin, EMLE*1, BSCANP*1, NMI	$\lvert I_{in} \rvert$	—	—	1.0	μA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	Other than ports for 5 V tolerant	$\lvert I_{TSI} \rvert$	—	—	1.0	μA	V_{in} = 0 V V_{in} = VCC
	Ports for 5 V tolerant		—	—	5.0		V_{in} = 0 V V_{in} = 5.5 V
Input pull-up resistor current	Other than P35	I_p	–300	—	–10	μA	VCC = 2.7 to 3.6 V V_{in} = 0 V
Input pull-down resistor current	EMLE, BSCANP	I_p	10	—	300	μA	V_{in} = VCC
Input capacitance	All input pins (except for P12, P13, P16, P17, EMLE, BSCANP, USB0_DP, and USB0_DM)	C_{in}	—	—	8	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz T_a = 25°C
	P12, P13, P16, P17, EMLE, BSCANP, USB0_DP, and USB0_DM		—	—	16		

Note 1. The input leakage current value at the EMLE and BSCANP pins are only when V_{in} = 0 V.

Table 6.6 DC Characteristics (4)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = 2.7 to 3.6 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
$T_a = T_{opr}$

Item				Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Full operation*2		I_{CC}*3	—	60	mA	ICLK = 120 MHz, PCLKA = 120 MHz, PCLKB = 60 MHz, PCLKC = 60 MHz, PCLKD = 60 MHz, FCLK = 60 MHz
		Normal operation	Peripheral module clocks are supplied*4		26	—		
			Peripheral module clocks are stopped *4, *5		13	—		
		CoreMark	Peripheral module clocks are stopped *4, *5		17	—		
		Sleep mode: Peripheral module clocks are supplied *4			20	38		
		All module clock stop mode (reference value)			9	26		
		Increased by BGO operation*8	Reading from the code flash memory while the data flash memory is being programmed		6	—		
			Reading from the code flash memory while the code flash memory is being programmed		7	—		
		Increased by Trusted Secure IP operation			—	12		
	Low-speed operating mode 1: Peripheral module clocks are stopped*4				1.6	—		All clocks 1 MHz
	Low-speed operating mode 2: Peripheral module clocks are stopped*4				1.6	—		All clocks 32.768 kHz
	Software standby mode				1.6	13		
	Deep software standby mode	Power is supplied to the standby RAM and USB resume detecting unit (USB0 only)			15.5	70	μA	
		Power is not supplied to the standby RAM and USB resume detecting unit (USB0 only)	Low power consumption function of the power-on reset circuit is disabled*6		11.5	42		
			Low power consumption function of the power-on reset circuit is enabled*7		4.9	32		
		Increase current by operating RTC	When a low C_L crystal is in use		1	—		
			When a standard C_L crystal is in use		2	—		
	When the RTC is operating while VCC is not supplied (Only the RTC and sub-clock oscillator operate with the battery backup function)		When a low C_L crystal is in use		0.9	—		V_{BATT} = 2.0 V, VCC = 0 V
					1.6	—		V_{BATT} = 3.3 V, VCC = 0 V
			When a standard C_L crystal is in use		1.7	—		V_{BATT} = 2.0 V, VCC = 0 V
					3.3	—		V_{BATT} = 3.3 V, VCC = 0 V
	Inrush current on release from deep software standby mode		Inrush current*9	I_{RUSH}	—	130	mA	
			Total inrush current*9	E_{RUSH}	—	1.0	μC	

Note 1. Supply current values are measured when all output pins are unloaded and all input pull-up resistors are disabled.
Note 2. Peripheral module clocks are supplied.
Note 3. I_{CC} depends on the f (ICLK) as follows (when ICLK/PCLKA : PCLKB/PCLKC/PCLKD = 2 : 1 and EXTAL = 12 MHz).
I_{CC} max = 0.38 × f + 14 (full operation in high-speed operating mode)
I_{CC} typ = 0.18 × f + 4 (normal operation in high-speed operating mode)
I_{CC} typ = 0.1 × f + 1.5 (ICLK 1 MHz max) (low-speed operating mode 1)
I_{CC} max = 0.2 × f + 14 (sleep mode)
Note 4. Whether the peripheral module clocks are supplied or stopped is controlled only by the bit settings in the module stop control registers A to D.
Note 5. When the peripheral module clock is stopped, the settings of the clock frequency are as follows:
ICLK = 120 MHz and PCLKA = PCLKB = PCLKC = PCLKD = FCLK = 3.75 MHz (divided by 64).
Note 6. When the low power consumption function is disabled, the DEEPCUT[1:0] bits are set to 01b.
Note 7. When the low power consumption function is enabled, the DEEPCUT[1:0] bits are set to 11b.

Note 8. These are the increases during programming of the code flash memory after the code flash memory (limitations apply to the combinations of address ranges of the program area and the readable area) or the data flash memory has been programmed or erased.
Note 9. Reference value

Table 6.7 DC Characteristics (5)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = 2.7 to 3.6 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current*1	During 12-bit A/D conversion (unit 0)		AI_{CC}	—	0.8	1	mA	IAVCC0_AD
	During 12-bit A/D conversion (unit 0) with channel dedicated sample-and-hold circuits (3 channels)			—	1.7	2.5		IAVCC0_AD + SH
	During 12-bit A/D conversion (unit 1)			—	0.6	1		IAVCC1_AD
	During 12-bit A/D conversion (unit 1) + temperature sensor			—	0.7	1.1		IAVCC1_AD + TEMP
	Waiting for A/D and temperature sensor conversion (all units)			—	0.9	1.4		IAVCC0 + IAVCC1
	A/D and temperature sensor are in standby mode (all units)			—	1.4	6.7	μA	IAVCC0 + IAVCC1
Reference power supply current	During 12-bit A/D conversion (unit 0)		AI_{REFH}	—	38	60	μA	IVREFH0
	Waiting for 12-bit A/D conversion (unit 0)			—	0.07	0.5		IVREFH0
	12-bit A/D converter in module stop status (unit 0)			—	0.07	0.4		IVREFH0
USB operating current	Full speed	USB0	$I_{CCUSBFS}$	—	4.2	10	mA	VCC_USB
RAM retension voltage			V_{RAM}	2.7	—	—	V	
VCC rising gradient			SrVCC	8.4	—	20000	μs/V	
VCC falling gradient*2			SfVCC	8.4	—	—	μs/V	

Note 1. The reference power supply current is included in the power supply current value for 12-bit A/D converter (unit 1).
Note 2. This applies when V_{BATT} is used.

Table 6.8 DC Characteristics (6)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 3.3 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
Data rate = 100 kbps, 2-FSK, modulation index = 1.0, frequency = 920.6 MHz, T_a = 25°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
SUN-FSK transmission supply current	—	62.0	—	mA	+15.0 dBm
	—	41.0	—		+10.0 dBm
	—	36.0	—		+8.0 dBm
	—	23.0	—		+0.0 dBm

Table 6.9 DC Characteristics (7)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 3.3 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
Data rate = 100 kbps (MCS2), band width = 400 kHz (option 3), frequency = 920.6 MHz, T_a = 25°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
SUN-OFDM transmission supply current	—	68.0	—	mA	+10.0 dBm

Table 6.10 DC Characteristics (8)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 3.3 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
Data rate = 100 kbps, 2-FSK, modulation index = 1.0, frequency = 920.6 MHz, T_a = 25°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
SUN-FSK reception supply current	—	16.7	—	mA	RF input at reception: –95 dBm
	—	16.8	—		No RF input while waiting for reception

Table 6.11 DC Characteristics (9)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 3.3 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
Data rate = 100 kbps (MCS2), band width = 400 kHz (option 3), frequency = 920.6 MHz, T_a = 25°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
SUN-OFDM reception supply current	—	21.5	—	mA	RF input at reception: –95 dBm
	—	21.7	—		No RF input while waiting for reception

Table 6.12 DC Characteristics (10)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 3.3 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
T_a = 25°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
SLEEP	—	0.5	—	µA	
IDLE	—	5.5	—	mA	

Table 6.13 Permissible Output Currents

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	2.0	mA
	All output pins*2	High drive		—	—	3.8	
	All output pins*3	High-speed interface high-drive		—	—	7.5	
Permissible output low current (max. value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	4.0	mA
	All output pins*2	High drive		—	—	7.6	
	All output pins*3	High-speed interface high-drive		—	—	15	
Permissible output low current (total)	Total of all output pins		ΣI_{OL}	—	—	80	mA
Permissible output high current (average value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	–2.0	mA
	All output pins*2	High drive		—	—	–3.8	
	All output pins*3	High-speed interface high-drive		—	—	–7.5	
Permissible output high current (max. value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	–4.0	mA
	All output pins*2	High drive		—	—	–7.6	
	All output pins*3	High-speed interface high-drive		—	—	–15	
Permissible output high current (total)	Total of all output pins		ΣI_{OH}	—	—	–80	mA

Caution: To protect the LSI's reliability, the output current values should not exceed the values in this table.

Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.

Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

Note 3. This is the value when high-speed interface high-driving ability is set with a pin for which high-speed interface high-driving ability is selectable.

6.4 AC Characteristics

Table 6.14 Operating Frequency (High-Speed Operating Mode)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)	f	—	—	120	MHz
	Peripheral module clock (PCLKA)		—	—	120	
	Peripheral module clock (PCLKB)		—	—	60	
	Peripheral module clock (PCLKC)		—	—	60	
	Peripheral module clock (PCLKD)		—	—	60	
	Flash-IF clock (FCLK)		—*1	—	60	

Note 1. The FCLK must run at a frequency of at least 4 MHz when changing the flash memory contents.

Table 6.15 Operating Frequency (Low-Speed Operating Mode 1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)	f	—	—	1	MHz
	Peripheral module clock (PCLKA)		—	—	1	
	Peripheral module clock (PCLKB)		—	—	1	
	Peripheral module clock (PCLKC)*1		—	—	1	
	Peripheral module clock (PCLKD)*1		—	—	1	
	Flash-IF clock (FCLK)		—	—	1	

Note 1. When the 12-bit A/D converter is used, the frequency must be set to at least 1 MHz.

Table 6.16 Operating Frequency (Low-Speed Operating Mode 2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)	f	32	—	264	kHz
	Peripheral module clock (PCLKA)		—	—	264	
	Peripheral module clock (PCLKB)		—	—	264	
	Peripheral module clock (PCLKC)*1		—	—	264	
	Peripheral module clock (PCLKD)*1		—	—	264	
	Flash-IF clock (FCLK)		32	—	264	

Note 1. The 12-bit A/D converter cannot be used.

6.4.1 Reset Timing

Table 6.17 Reset Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	1	—	—	ms	Figure 6.1
	Deep software standby mode	t_{RESWD}	0.6	—	—	ms	Figure 6.2
	Software standby mode, low-speed operating mode 2	t_{RESWS}	0.3	—	—	ms	
	Programming or erasure of the code flash memory, or programming, erasure or blank checking of the data flash memory	t_{RESWF}	200	—	—	µs	
	Other than above	t_{RESW}	200	—	—	µs	
Waiting time after release from the RES# pin reset		t_{RESWT}	54	—	55	t_{Lcyc}	Figure 6.1
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	100	—	108	t_{Lcyc}	

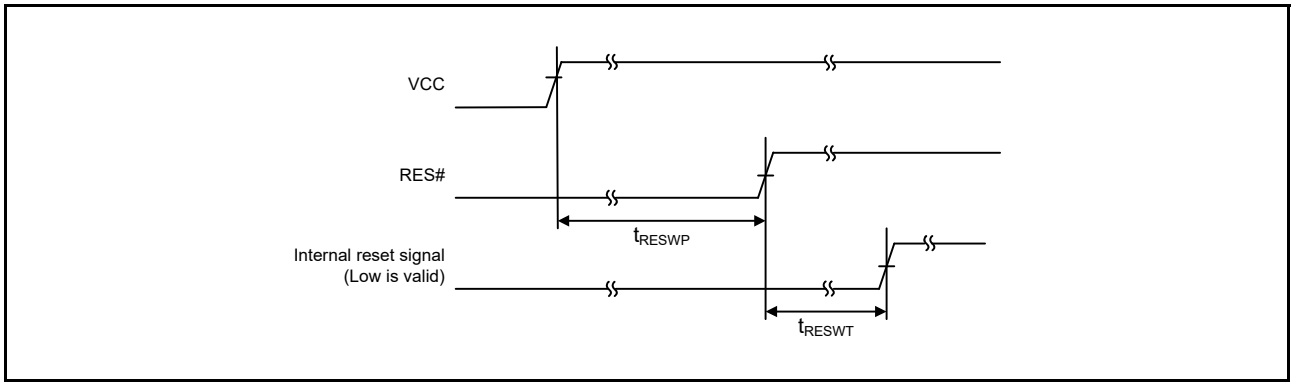


Figure 6.1 Reset Input Timing at Power-On

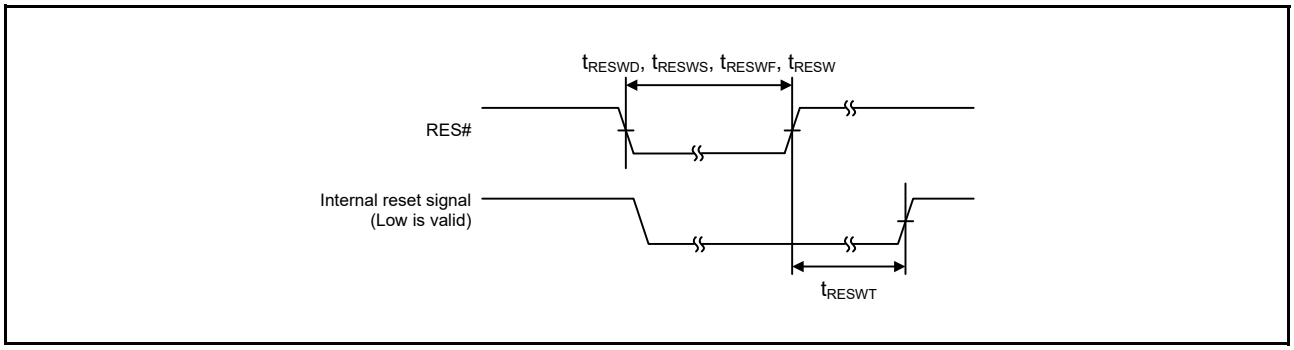


Figure 6.2 Reset Input Timing

6.4.2 Clock Timing

Table 6.18 EXTAL Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{EXcyc}	41.66	—	—	ns	Figure 6.3
EXTAL external clock input frequency	f_{EXMAIN}	—	—	24	MHz	
EXTAL external clock input high pulse width	t_{EXH}	15.83	—	—	ns	
EXTAL external clock input low pulse width	t_{EXL}	15.83	—	—	ns	
EXTAL external clock rising time	t_{EXr}	—	—	5	ns	
EXTAL external clock falling time	t_{EXf}	—	—	5	ns	

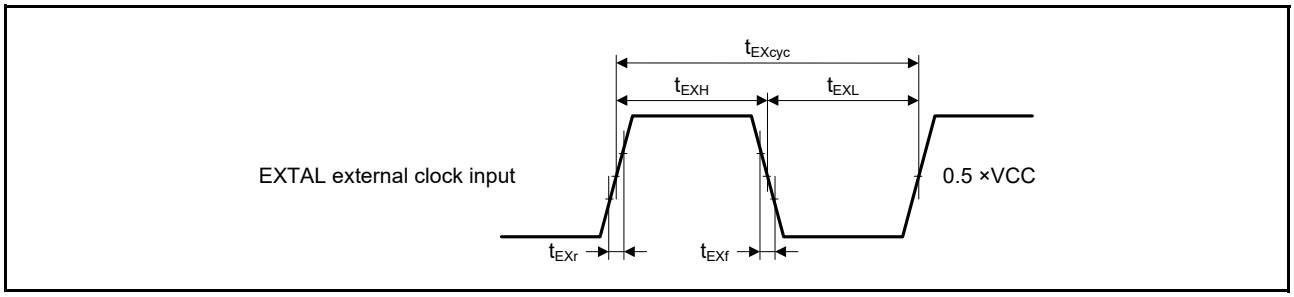


Figure 6.3 EXTAL External Clock Input Timing

Table 6.19 Main Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Main clock oscillation frequency	f_{MAIN}	8	—	24	MHz	
Main clock oscillator stabilization time (crystal)	$t_{MAINOSC}$	—	—	—*1	ms	Figure 6.4
Main clock oscillation stabilization wait time (crystal)	$t_{MAINOSCWT}$	—	—	—*2	ms	

Note 1. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the MOSCWTCR.MSTS[7:0] bits determines the main clock oscillation stabilization wait time in accord with the formula below.
$t_{MAINOSCWT}$ = [(MSTS[7:0] bits × 32) + 10] / f_{LOCO}

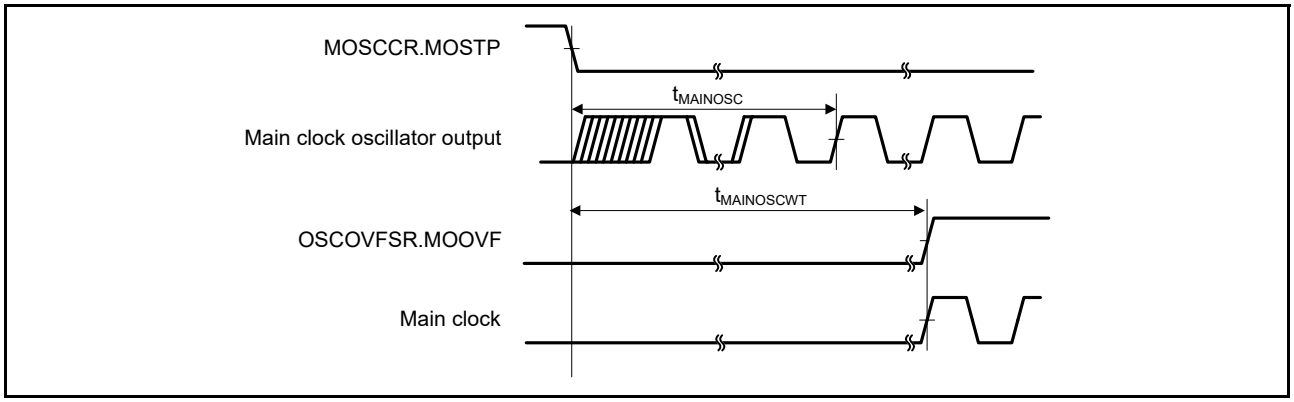


Figure 6.4 Main Clock Oscillation Start Timing

Table 6.20 LOCO and IWDT-Dedicated Low-Speed Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LOCO clock cycle time	t_{Lcyc}	4.63	4.16	3.78	µs	
LOCO clock oscillation frequency	f_{LOCO}	216	240	264	kHz	
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	44	µs	Figure 6.5
IWDT-dedicated low-speed clock cycle time	t_{ILcyc}	9.26	8.33	7.57	µs	
IWDT-dedicated low-speed clock oscillation frequency	f_{ILOCO}	108	120	132	kHz	
IWDT-dedicated low-speed clock oscillation stabilization wait time	$t_{ILOCOWT}$	—	142	190	µs	Figure 6.6

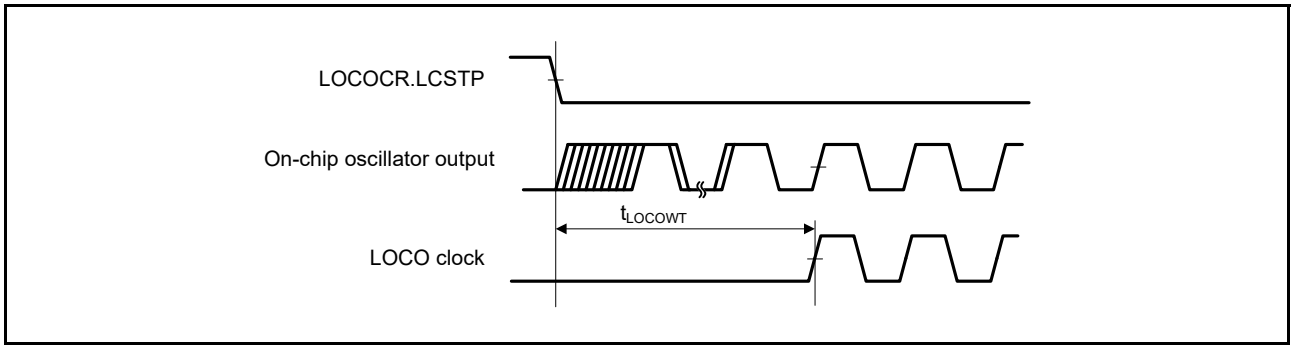


Figure 6.5 LOCO Clock Oscillation Start Timing

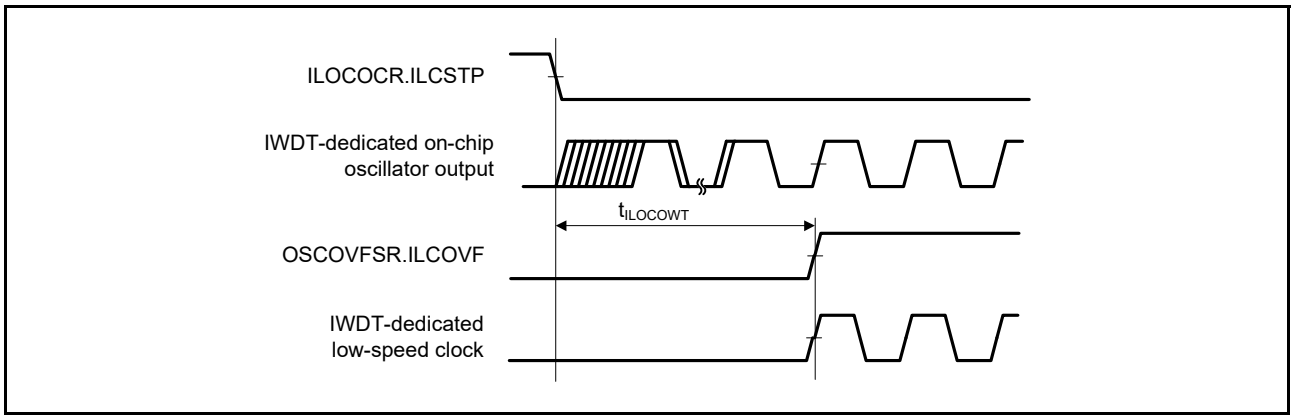


Figure 6.6 IWDT-dedicated Low-Speed Clock Oscillation Start Timing

Table 6.21 HOCO Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
HOCO clock oscillation frequency	f_{HOCO}	15.61	16	16.39	MHz	–20°C ≤ T_a ≤ 85°C
		17.56	18	18.44		
		19.52	20	20.48		
		15.52	16	16.48		–40°C ≤ T_a < –20°C
		17.46	18	18.54		
		19.4	20	20.6		
HOCO clock oscillation stabilization wait time	t_{HOCOWT}	—	105	149	µs	Figure 6.7
HOCO clock power supply stabilization time	t_{HOCOP}	—	—	150	µs	Figure 6.8

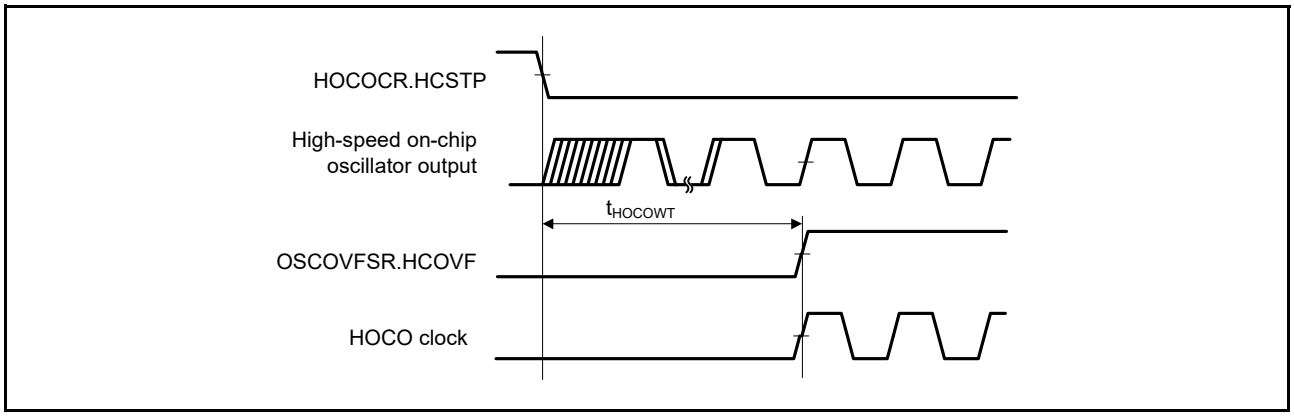


Figure 6.7 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)

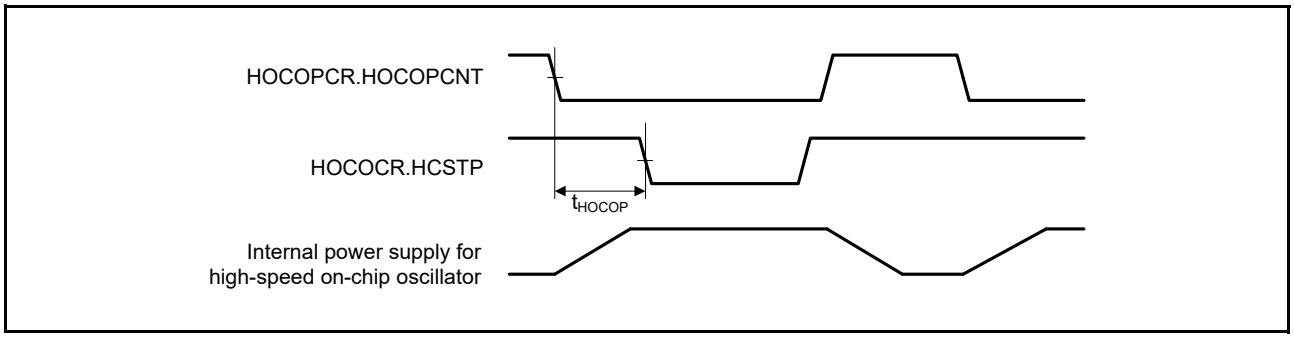


Figure 6.8 High-Speed On-Chip Oscillator Power Supply Control Timing

Table 6.22 PLL Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
PLL clock oscillation frequency	f_{PLL}	120	—	240	MHz	
PLL clock oscillation stabilization wait time	t_{PLLWT}	—	259	320	µs	Figure 6.9

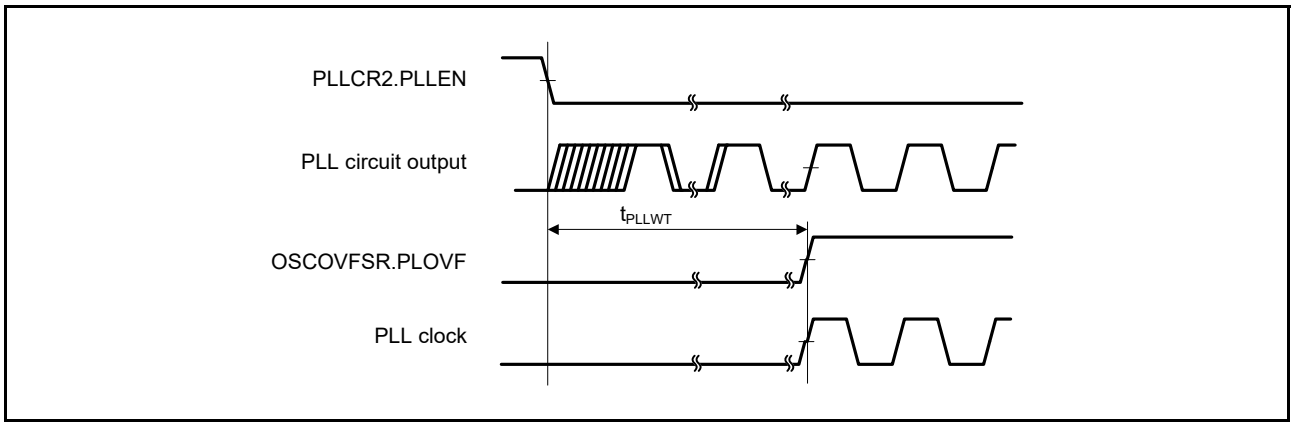


Figure 6.9 PLL Clock Oscillation Start Timing

Table 6.23 Sub-Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = 2.7 to 3.6 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
V_{BATT} = 2.0 to 3.6 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Sub-clock oscillation frequency	f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time	t_{SUBOSC}	—	—	*1	s	Figure 6.10
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	—	—	*2	s	

Note 1. When using a sub-clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the SOSCWTCR.SSTS[7:0] bits determines the sub-clock oscillation stabilization wait time in accord with the formula below.
$t_{SUBOSCWT}$ = [(SSTS[7:0] bits × 16384) + 10] / f_{LOCO}

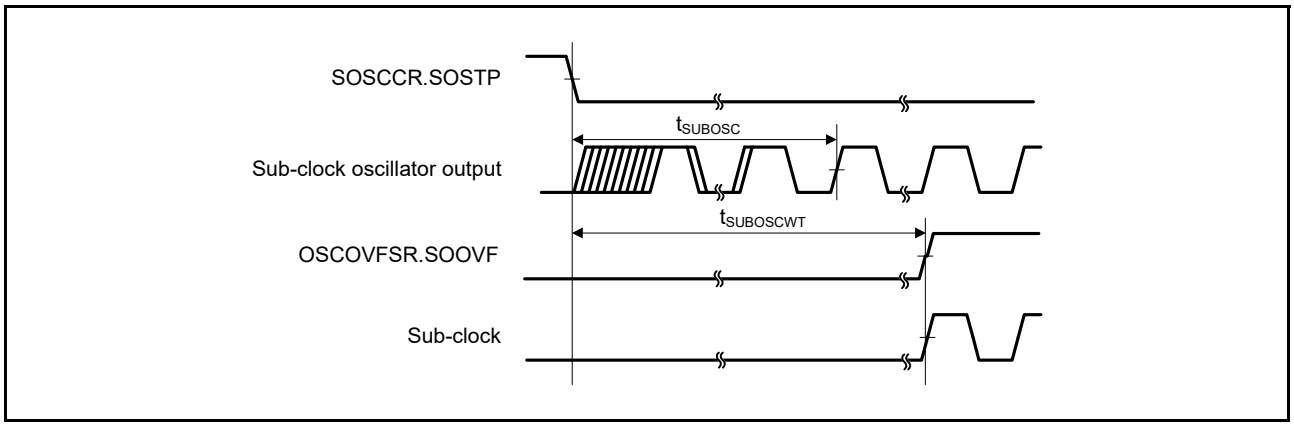


Figure 6.10 Sub-Clock Oscillation Start Timing

6.4.3 Timing of Recovery from Low Power Consumption Modes

Table 6.24 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.		Unit	Test Conditions
						$t_{SBYOSCWT}$*2	t_{SBYSEQ}*3		
Recovery time from software standby mode *1	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t_{SBYMC}	—	—	{(MSTS[7:0] bit × 32) + 76} / 0.216	100 + 7 / f_{ICLK} + 2n / f_{MAIN}	µs	Figure 6.11
		Main clock oscillator and PLL circuit operating	t_{SBYPC}			{(MSTS[7:0] bit × 32) + 138} / 0.216	100 + 7 / f_{ICLK} + 2n / f_{PLL}		
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}			352	100 + 7 / f_{ICLK} + 2n / f_{EXMAIN}		
		Main clock oscillator and PLL circuit operating	t_{SBYPE}			639	100 + 7 / f_{ICLK} + 2n / f_{PLL}		
	Sub-clock oscillator operating		t_{SBYSC}			{(SSTS[7:0] bit × 16384) + 13} / 0.216 + 10 / f_{FCLK}	100 + 4 / f_{ICLK} + 2n / f_{SUE}		
	High-speed on-chip oscillator operating	High-speed on-chip oscillator operating	t_{SBYHO}			454	100 + 7 / f_{ICLK} + 2n / f_{HOCO}		
		High-speed on-chip oscillator operating and PLL circuit operating	t_{SBYPH}			741	100 + 7 / f_{ICLK} + 2n / f_{PLL}		
	Low-speed on-chip oscillator operating*4		t_{SBYLO}			338	100 + 7 / f_{ICLK} + 2n / f_{LOCO}		

Note 1. The time for recovery from software standby mode is determined by the value obtained by adding the oscillation stabilization waiting time ($t_{SBYOSCWT}$) and the time required for operations by the software standby release sequencer (t_{SBYSEQ}).
Note 2. When several oscillators were running before the transition to software standby, the greatest value of the oscillation stabilization waiting time $t_{SBYOSCWT}$ is selected.
Note 3. For n, the greatest value is selected from among the internal clock division settings.
Note 4. This condition applies when f_{ICLK}:f_{FCLK} = 1:1, 2:1, or 4:1.

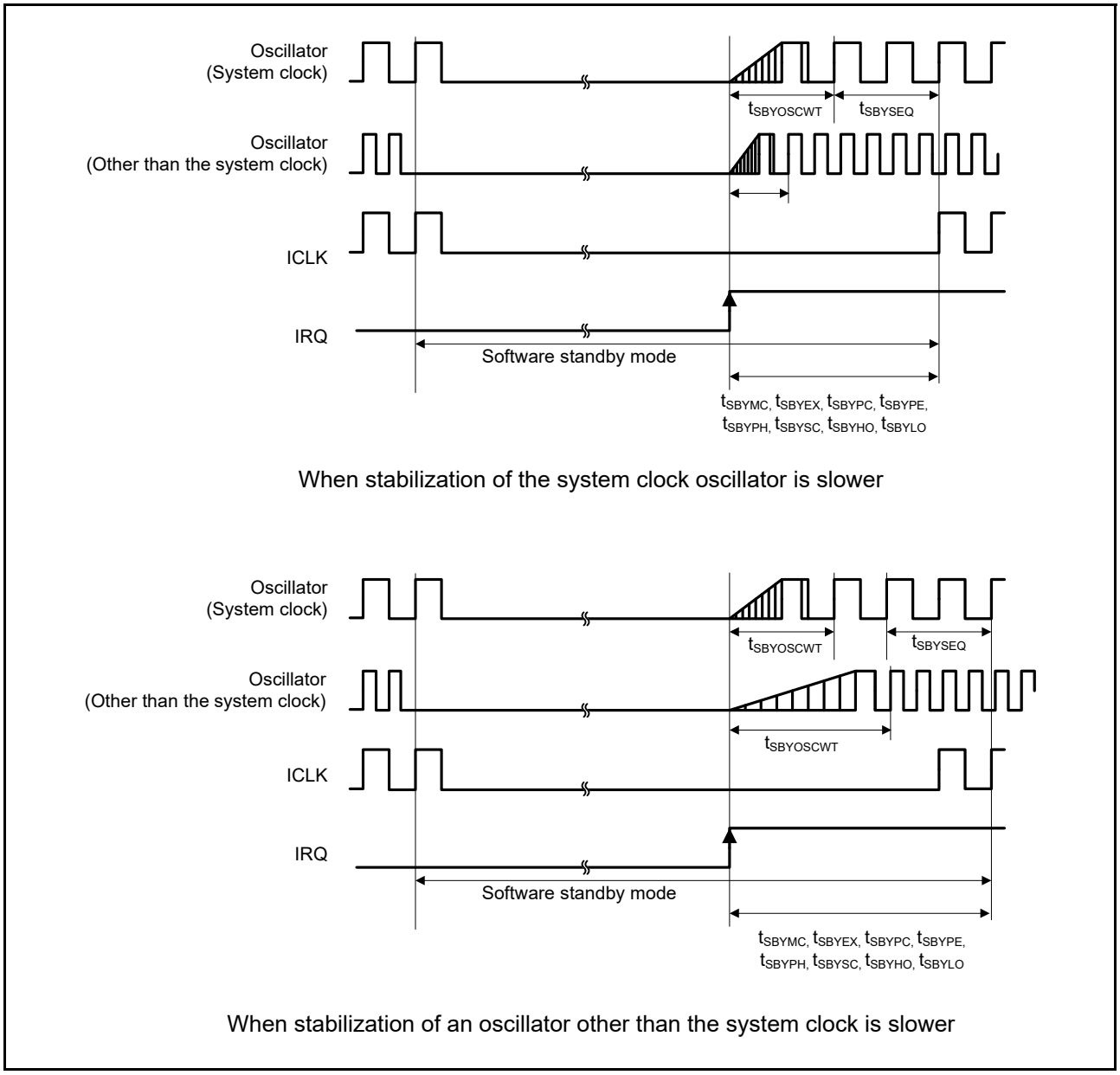


Figure 6.11 Software Standby Mode Recovery Timing

Table 6.25 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep software standby mode	t_{DSBY}	—	—	0.9	ms	Figure 6.12
Wait time after recovery from deep software standby mode	t_{DSBYWT}	23	—	24	t_{Lcyc}	

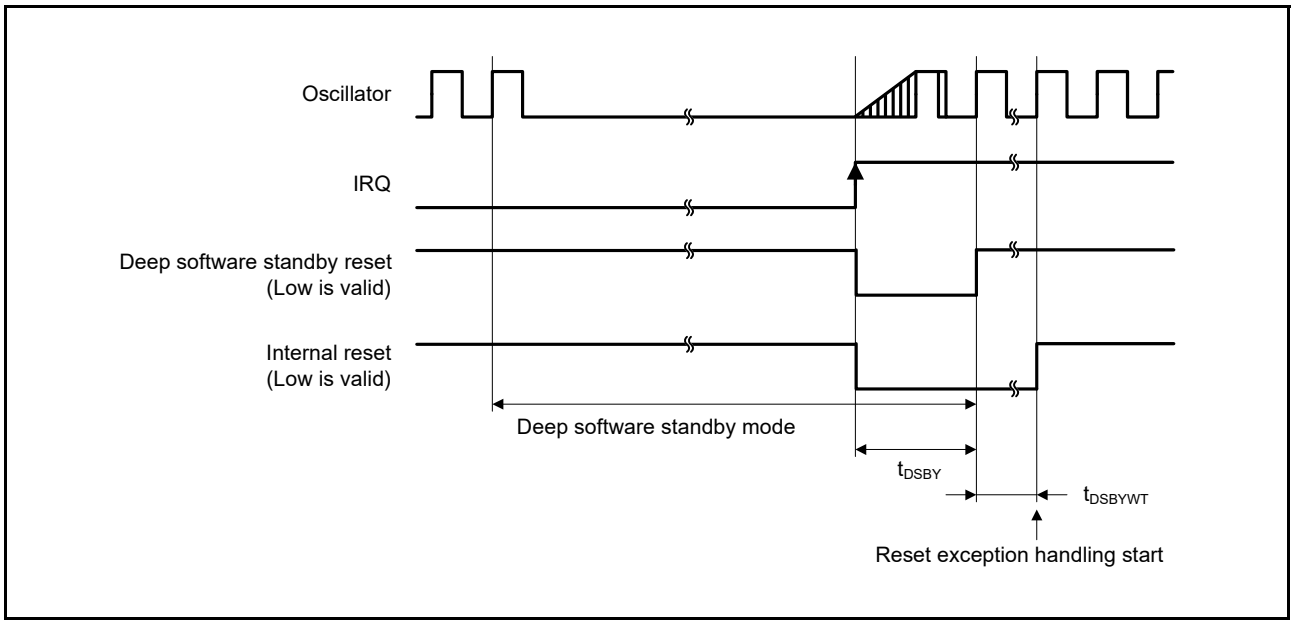


Figure 6.12 Deep Software Standby Mode Recovery Timing

6.4.4 Control Signal Timing

Table 6.26 Control Signal Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.*1	Typ.	Max.	Unit	Test Conditions*1
NMI pulse width	t_{NMIW}	200	—	—	ns	2 × t_{PBcyc} ≤ 200 ns, Figure 6.13
		2 × t_{PBcyc}	—	—		2 × t_{PBcyc} > 200 ns, Figure 6.13
IRQ pulse width	t_{IRQW}	200	—	—	ns	2 × t_{PBcyc} ≤ 200 ns, Figure 6.14
		2 × t_{PBcyc}	—	—		2 × t_{PBcyc} > 200 ns, Figure 6.14

Note 1. t_{PBcyc}: PCLKB cycle

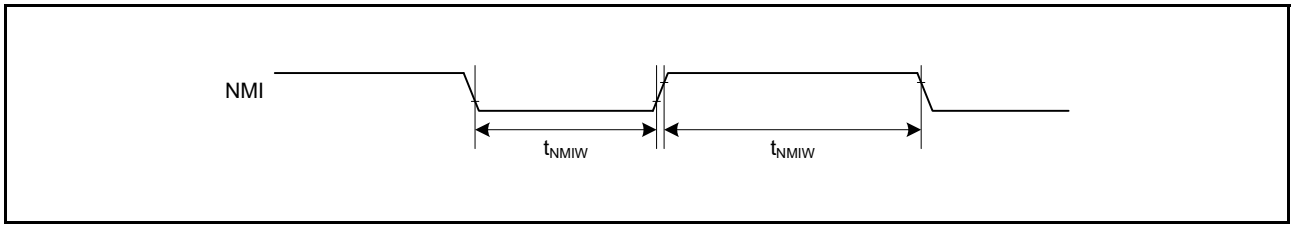


Figure 6.13 NMI Interrupt Input Timing

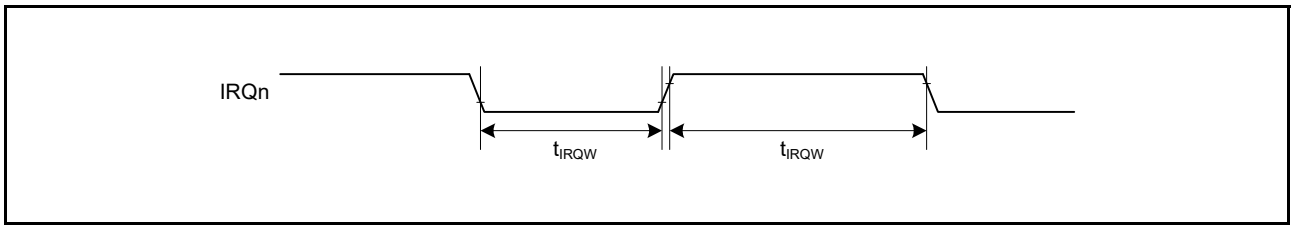


Figure 6.14 IRQ Interrupt Input Timing

6.4.5 Timing of On-Chip Peripheral Modules

6.4.5.1 I/O Port

Table 6.27 I/O Port Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	—	t_{PBcyc}	Figure 6.15

Note 1. t_{PBcyc}: PCLKB cycle

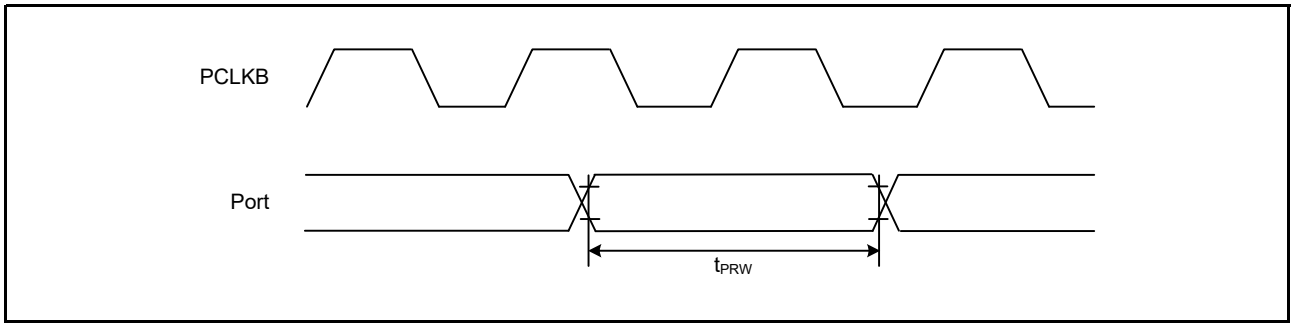


Figure 6.15 I/O Port Input Timing

6.4.5.2 TPU

Table 6.28 TPU Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
TPU	Input capture input pulse width	Single-edge setting	t_{TICW}	1.5	—	t_{PBcyc}	Figure 6.16
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{PBcyc}	Figure 6.17
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

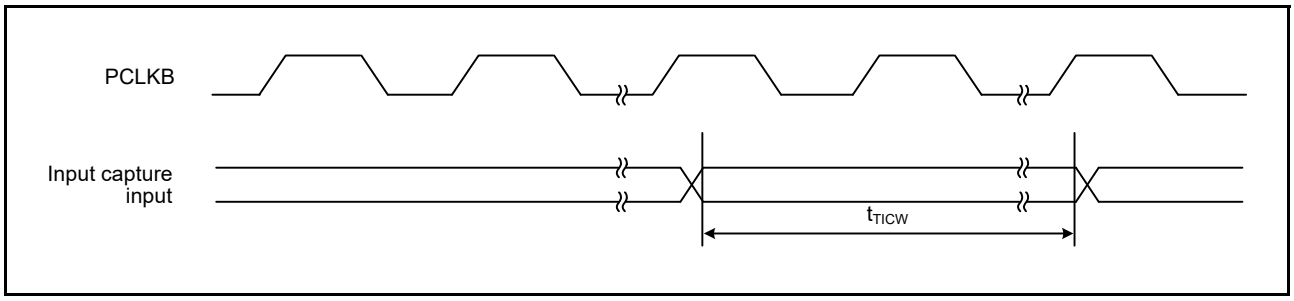


Figure 6.16 TPU Input Capture Input Timing

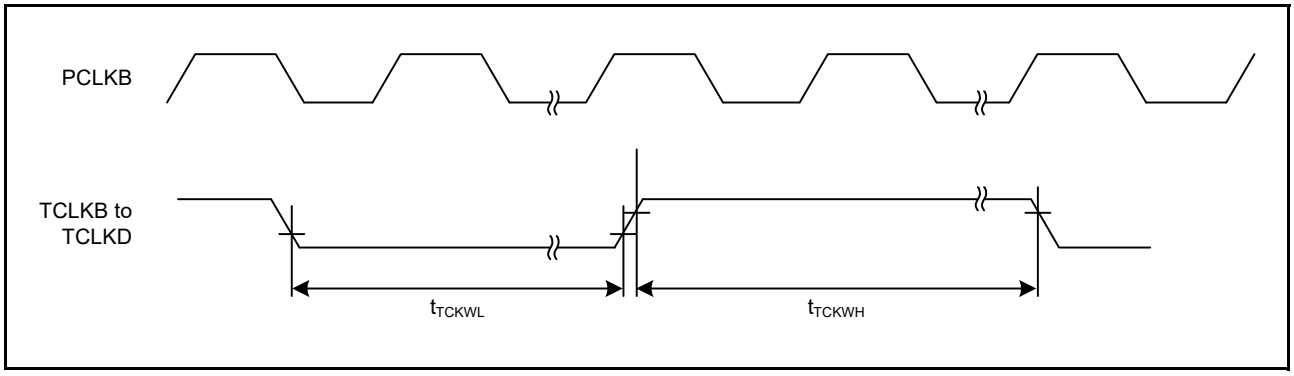


Figure 6.17 TPU Clock Input Timing

6.4.5.3 TMR

Table 6.29 TMR Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{PBcyc}	Figure 6.18
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

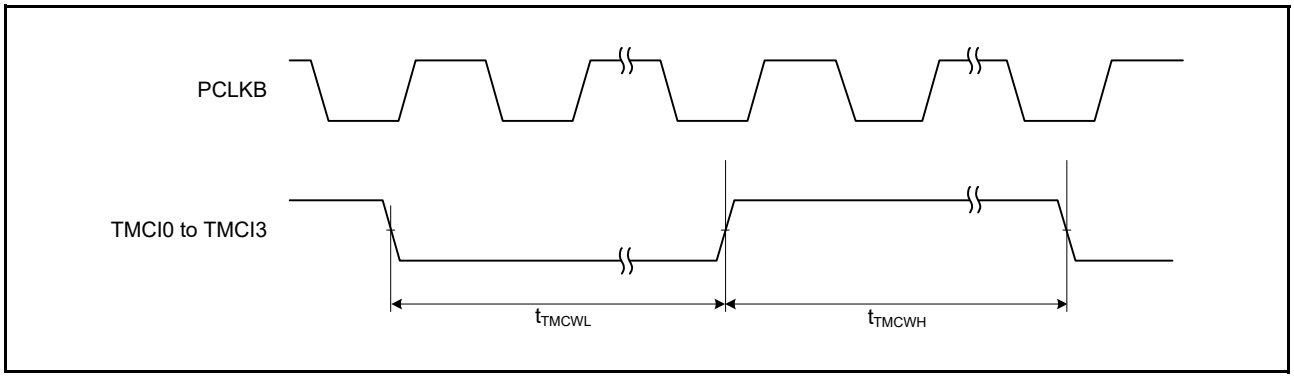


Figure 6.18 TMR Clock Input Timing

6.4.5.4 CMTW

Table 6.30 CMTW Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
CMTW	Input capture input pulse width	Single-edge setting	$t_{CMTWTICW}$	1.5	—	t_{PBcyc}	Figure 6.19
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

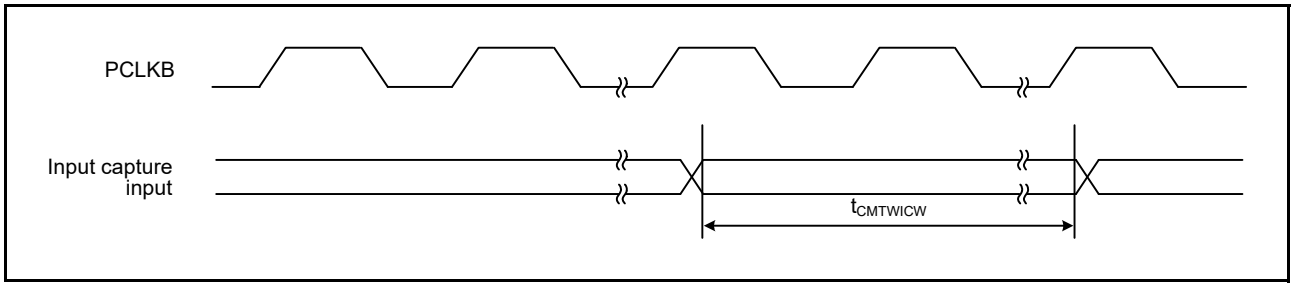


Figure 6.19 CMTW Input Capture Input Timing

6.4.5.5 MTU3

Table 6.31 MTU3 Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
MTU3	Input capture input pulse width	Single-edge setting	t_{MTICW}	1.5	—	t_{PAcyc}	Figure 6.20
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{MTCKWH}, t_{MTCKWL}	1.5	—	t_{PAcyc}	Figure 6.21
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PAcyc}: PCLKA cycle

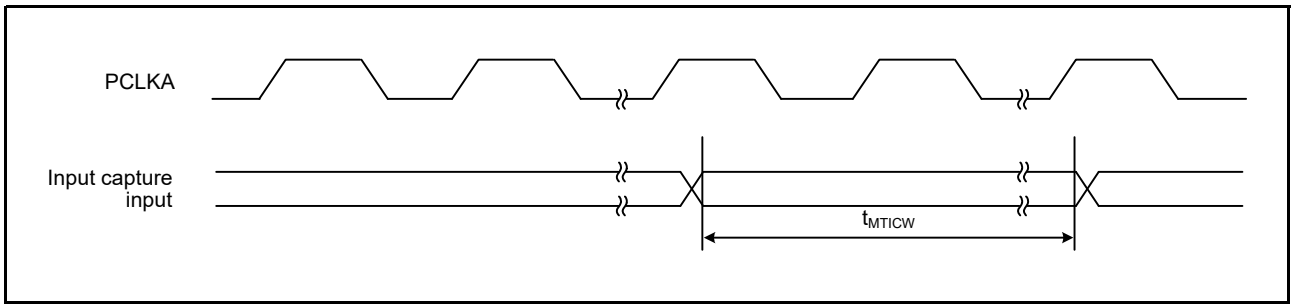


Figure 6.20 MTU3 Input Capture Input Timing

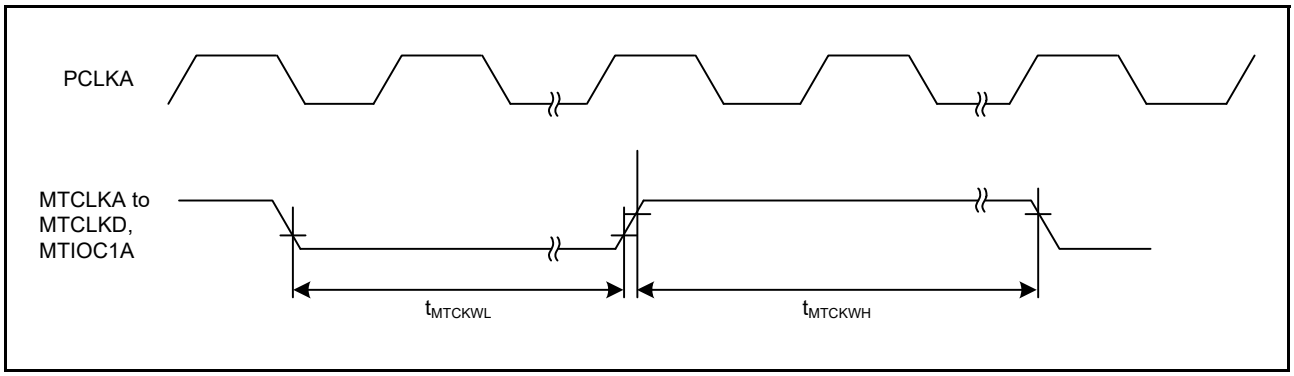


Figure 6.21 MTU3 Clock Input Timing

6.4.5.6 POE3

Table 6.32 POE3 Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
POE	POE# input pulse width	t_{POEW}	1.5	—	t_{PBcyc}	Figure 6.22

Note 1. t_{PBcyc}: PCLKB cycle

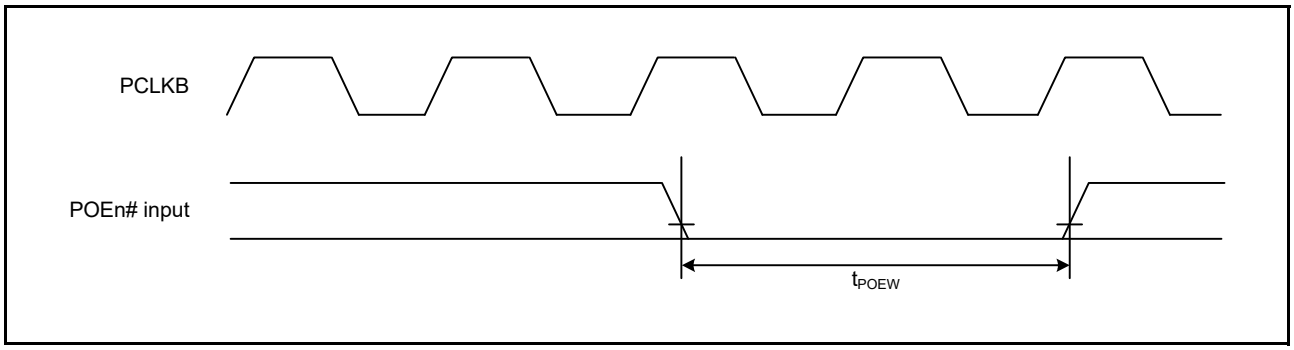


Figure 6.22 POE# Input Timing

6.4.5.7 A/D Converter Trigger

Table 6.33 A/D Converter Trigger Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
A/D converter	A/D converter trigger input pulse width	t_{TRGW}	1.5	—	t_{PBcyc}	Figure 6.23

Note 1. t_{PBcyc}: PCLKB cycle

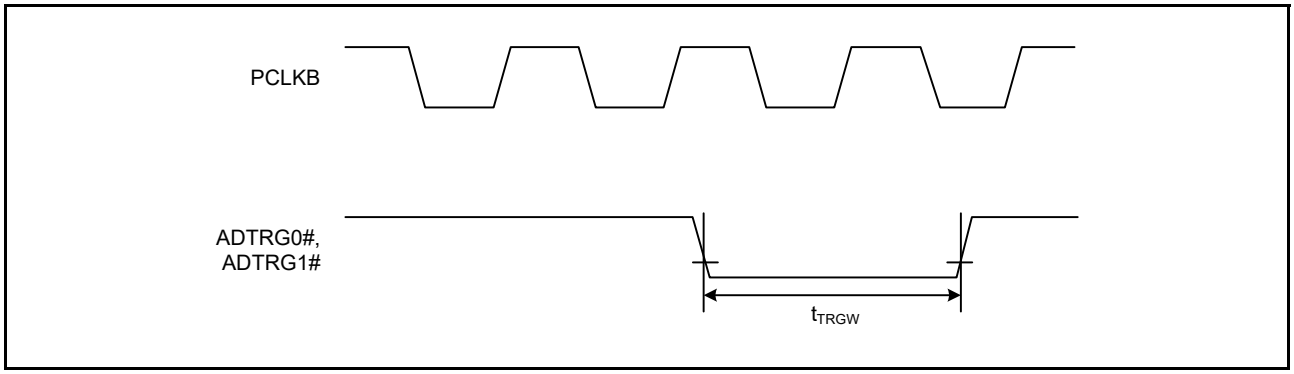


Figure 6.23 A/D Converter Trigger Input Timing

6.4.5.8 CAC

Table 6.34 CAC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item*1, *2			Symbol	Min.*1, *2	Max.	Unit	Test Conditions
CAC	CACREF input pulse width	$t_{PBcyc} \le t_{cac}$	t_{CACREF}	4.5 t_{cac} + 3 t_{PBcyc}	—	ns	
		$t_{PBcyc} > t_{cac}$		5 t_{cac} + 6.5 t_{PBcyc}	—		

Note 1. t_{PBcyc}: PCLKB cycle
Note 2. t_{cac}: CAC count clock source cycle

6.4.5.9 SCI

Table 6.35 SCIg, SCIh, and SCIi Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
SCIg, SCIh	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{PBcyc}	Figure 6.24
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	5	ns	
	Input clock fall time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous*2	t_{Scyc}	8	—	t_{PBcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	5	ns	
	Output clock fall time		t_{SCKf}	—	5	ns	
	Transmit data delay time	Clock synchronous	t_{TXD}	—	28	ns	Figure 6.25
	Receive data setup time	Clock synchronous	t_{RXS}	15	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	5	—	ns	
SCIi	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{PAcyc}	Figure 6.24
		Clock synchronous		12	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	5	ns	
	Input clock fall time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous*2	t_{Scyc}	8	—	t_{PAcyc}	
		Clock synchronous		8	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	5	ns	
	Output clock fall time		t_{SCKf}	—	5	ns	
	Transmit data delay time	Master	t_{TXD}	—	15	ns	Figure 6.25
		Slave		—	28		
	Receive data setup time	Clock synchronous	t_{RXS}	20	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	5	—		

Note 1. t_{PBcyc}: PCLKB cycle; t_{PAcyc}: PCLKA cycle
Note 2. When the SEMR.ABCS and SEMR.BGDM bits are set to 1

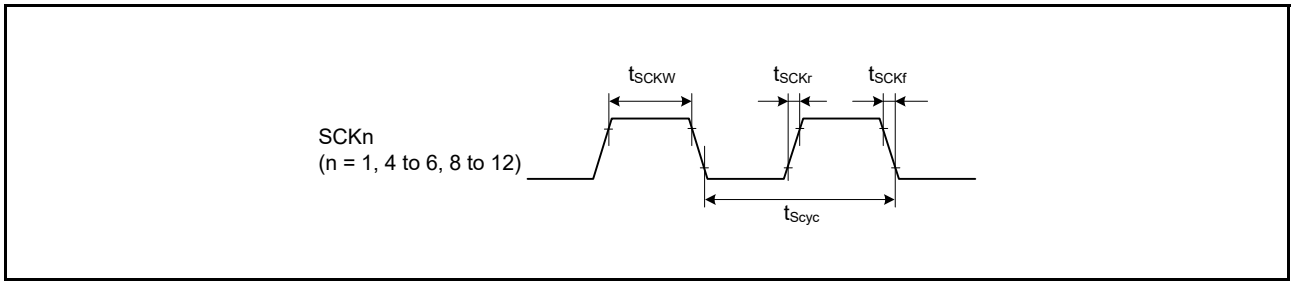


Figure 6.24 SCK Clock Input Timing

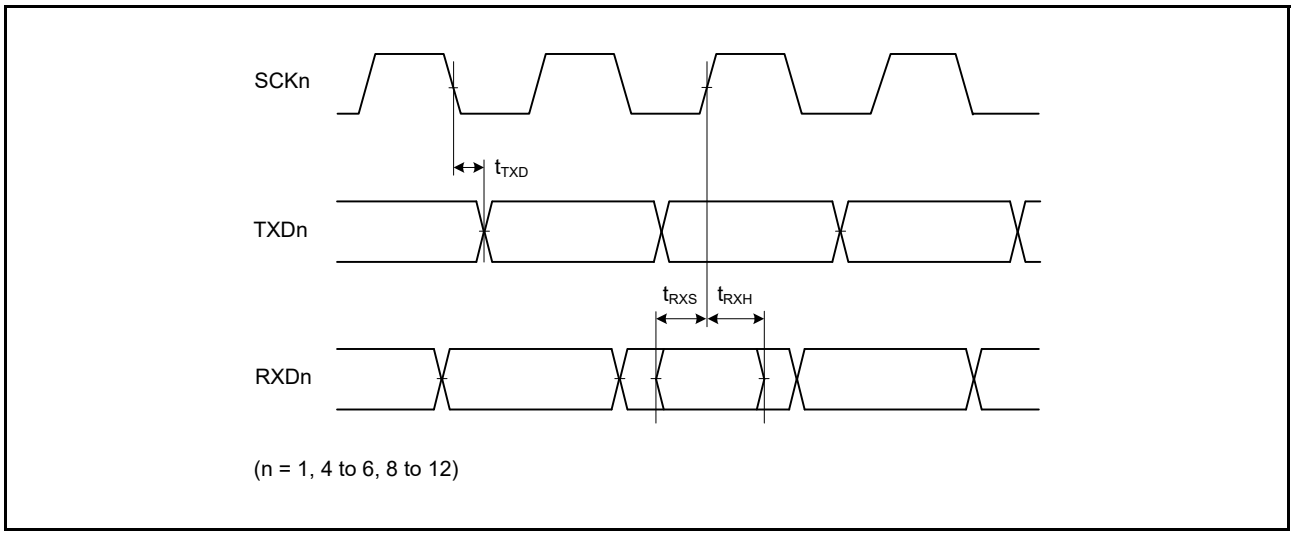


Figure 6.25 SCI Input/Output Timing: Clock Synchronous Mode

Table 6.36 Simple IIC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
Simple IIC (Standard-mode)	SSCL, SSDA input rise time	t_{Sr}	—	1000	ns	Figure 6.26
	SSCL, SSDA input fall time	t_{Sf}	—	300	ns	
	SSCL, SSDA input spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SSCL, SSDA capacitive load	C_b*1	—	400	pF	
Simple IIC (Fast-mode)	SSCL, SSDA input rise time	t_{Sr}	—	300	ns	
	SSCL, SSDA input fall time	t_{Sf}	—	300	ns	
	SSCL, SSDA input spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SSCL, SSDA capacitive load	C_b*1	—	400	pF	

Note: t_{Pcyc} refers to the period of PCLKA in SCI10 and SCI11, and of PCLKB in SCI1 to SCI6, SCI8, SCI9, and SCI12.
Note 1. C_b is the total capacitance of the bus lines.

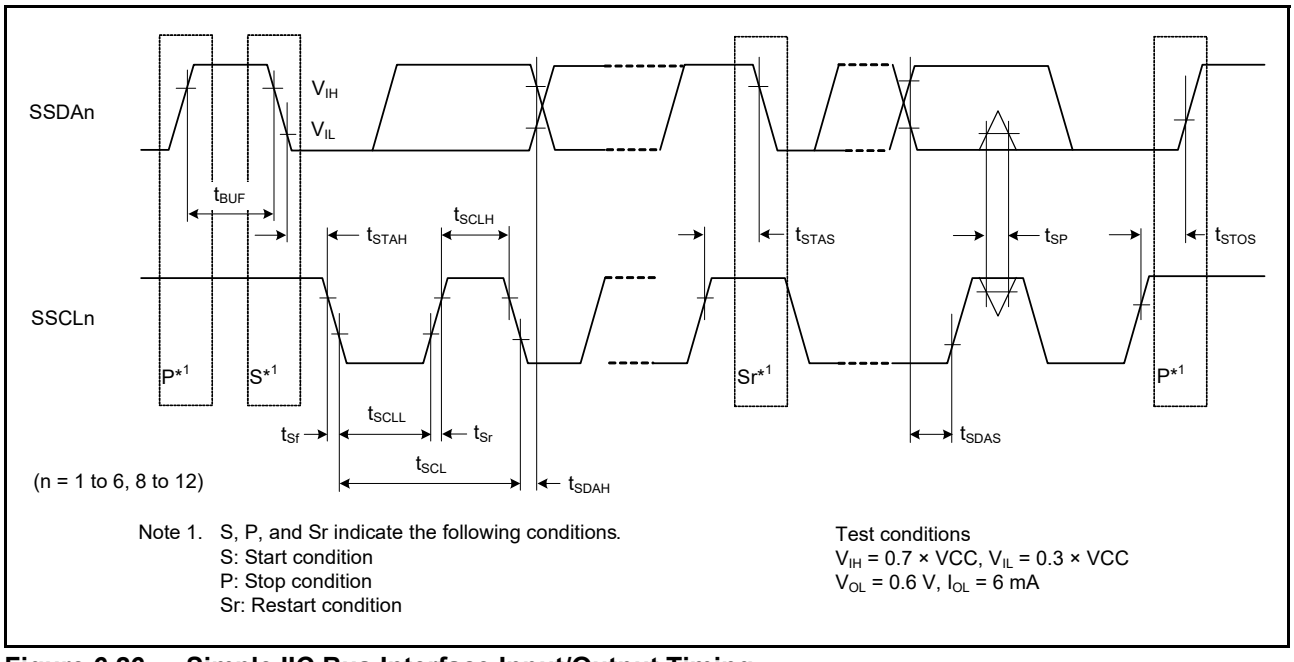


Figure 6.26 Simple IIC Bus Interface Input/Output Timing

Table 6.37 Simple SPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{Pcyc}	Figure 6.27
	SCK clock cycle input (slave)		6	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time	t_{SU}	33.3	—	ns	Figure 6.28 to Figure 6.31
	Data input hold time	t_H	33.3	—	ns	
	SS input setup time	t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time	t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time	t_{OD}	—	33.3	ns	
	Data output hold time	t_{OH}	–10	—	ns	
	Data rise/fall time	t_{Dr}, t_{Df}	—	16.6	ns	
	SS input rise/fall time	t_{SSLr}, t_{SSLf}	—	16.6	ns	
	Slave access time	t_{SA}	—	5	t_{Pcyc}	Figure 6.30, Figure 6.31
	Slave output release time	t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc} refers to the period of PCLKA in SCI10 and SCI11, and of PCLKB in SCI1, SCI4 to SCI6, SCI8, SCI9, and SCI12.

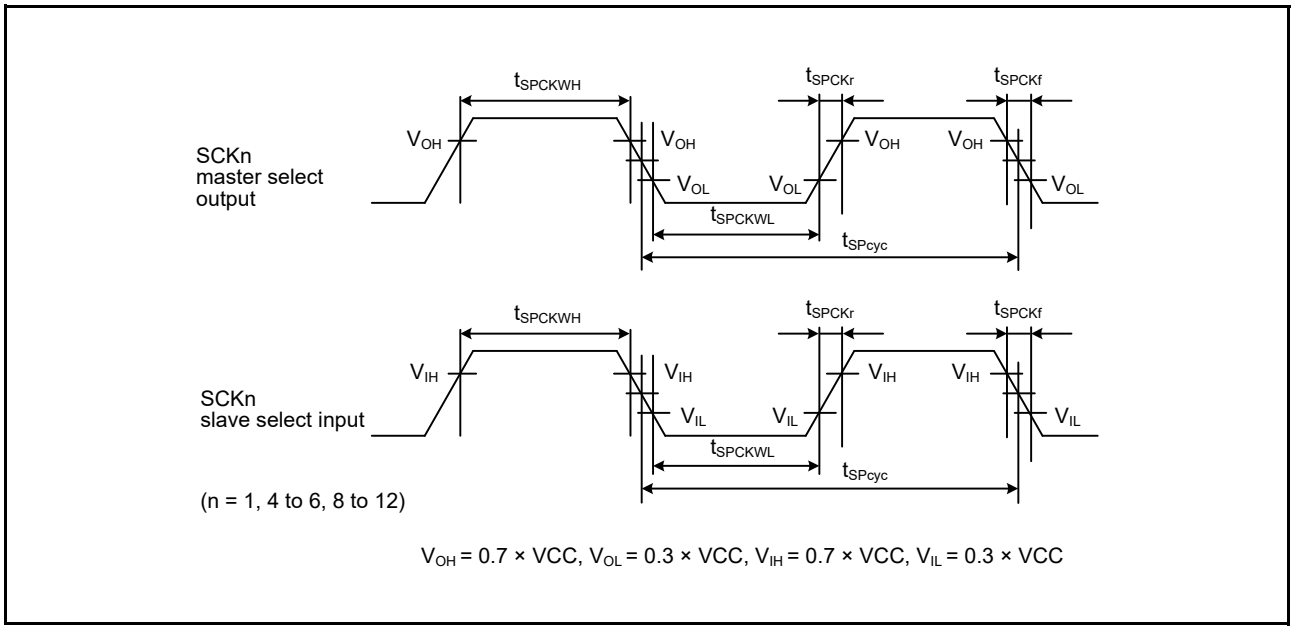


Figure 6.27 Simple SPI Clock Timing

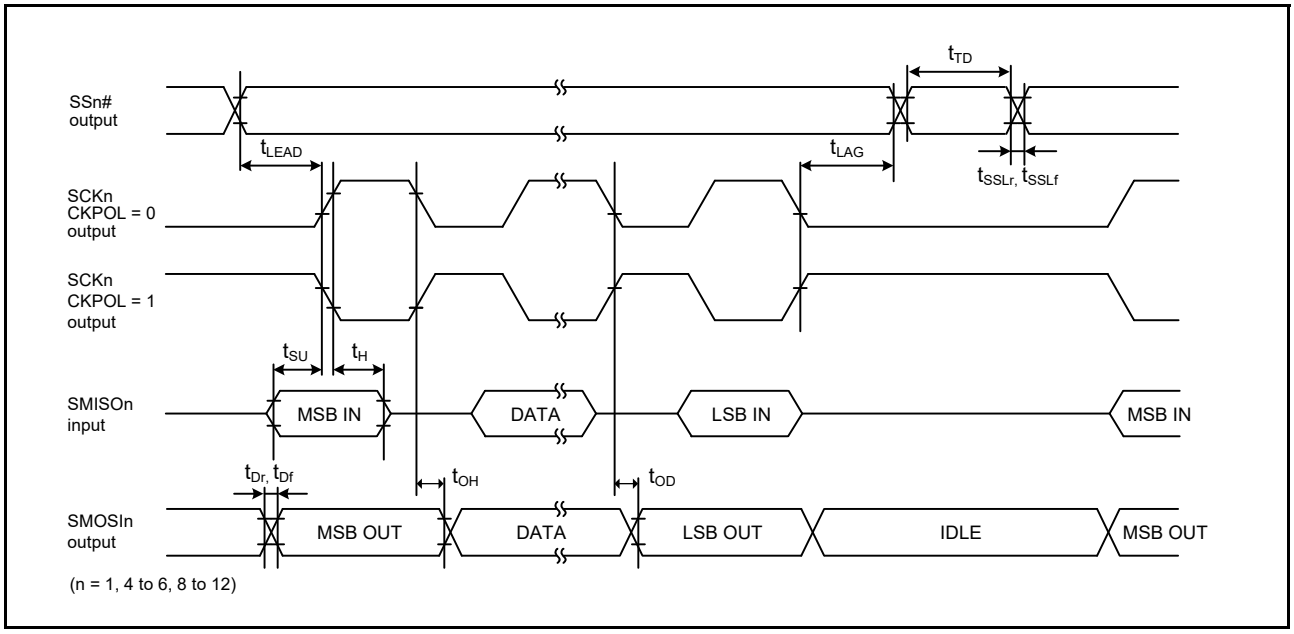


Figure 6.28 Simple SPI Timing (Master, CKPH = 1)

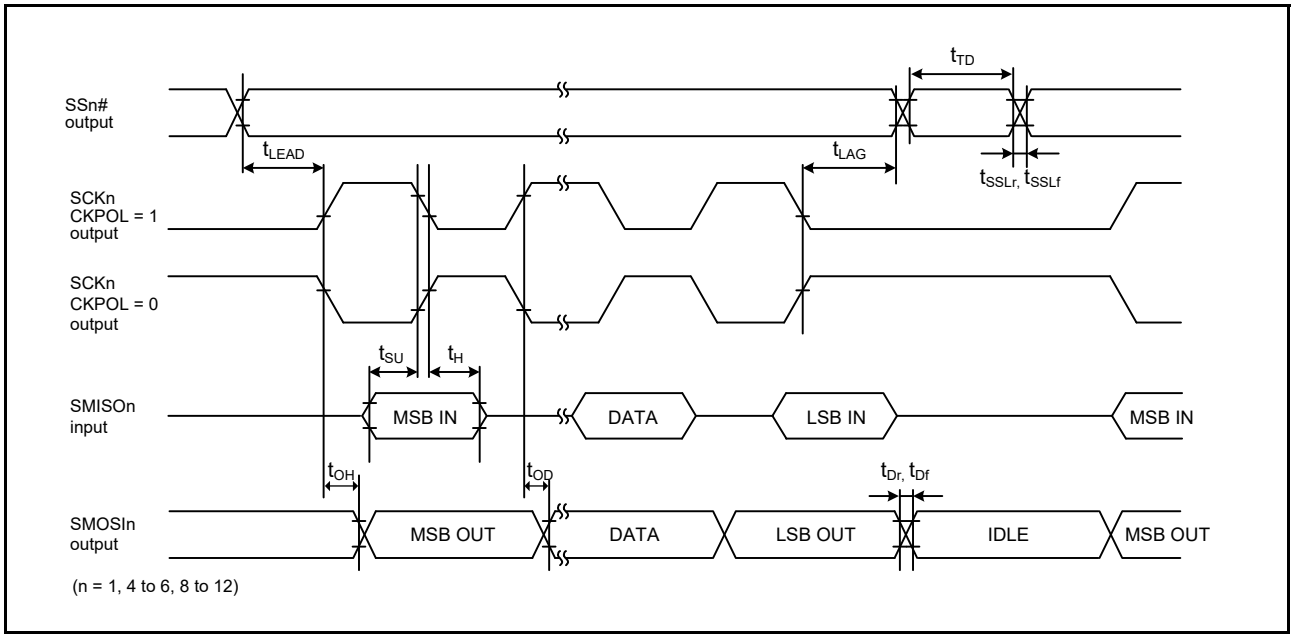


Figure 6.29 Simple SPI Timing (Master, CKPH = 0)

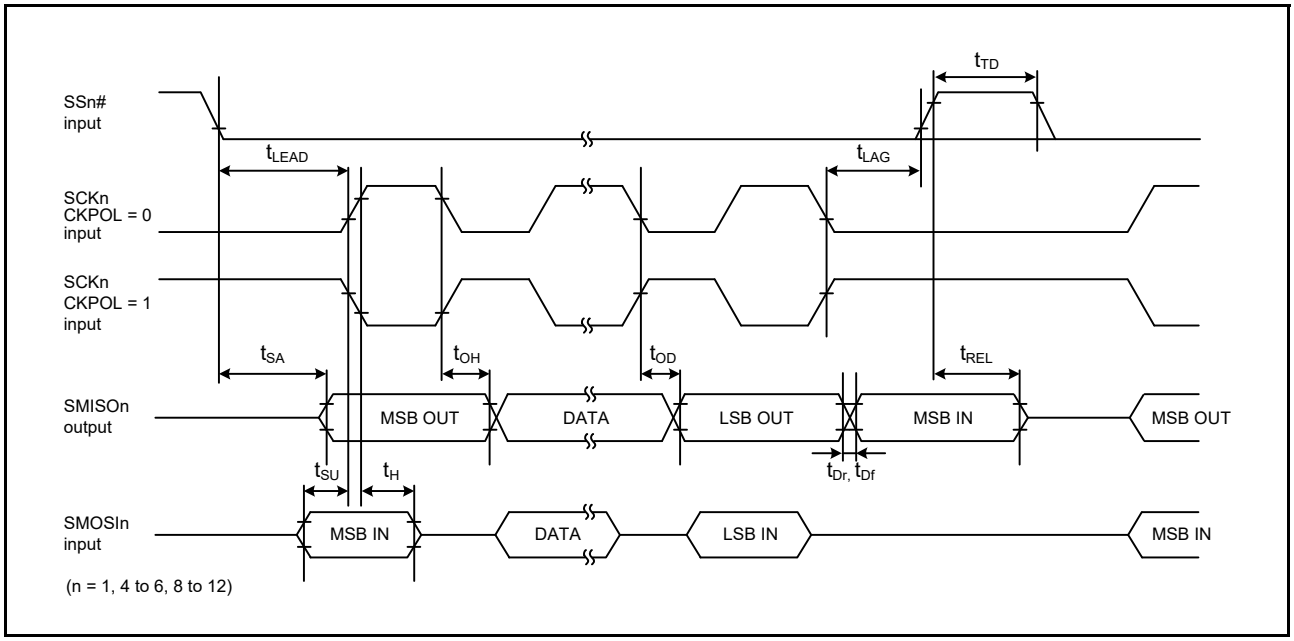


Figure 6.30 Simple SPI Timing (Slave, CKPH = 1)

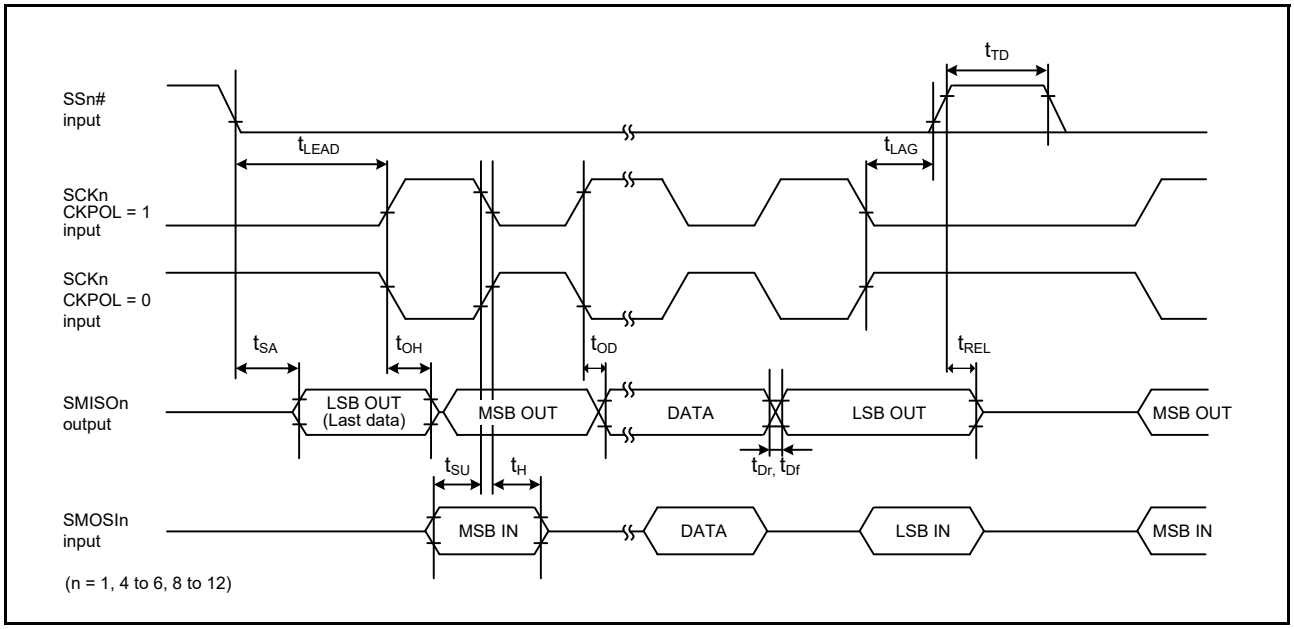


Figure 6.31 Simple SPI Timing (Slave, CKPH = 0)

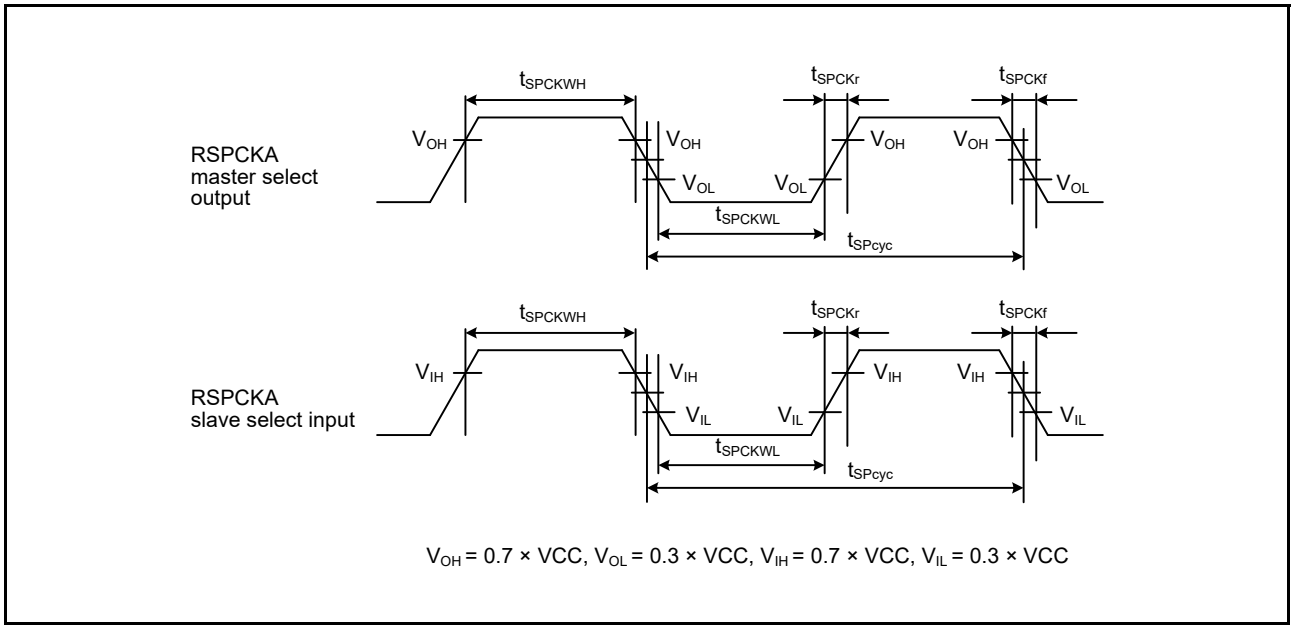
6.4.5.10 RSPI

Table 6.38 RSPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item				Symbol	Min.*1	Max.*1	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{PAcyc}	Figure 6.32
		Slave			4	—		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2$	—		
	RSPCK clock rise/fall time	Output		t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Input			—	1	µs	
	Data input setup time	Master		t_{SU}	6	—	ns	Figure 6.33 to Figure 6.38
		Slave			8.3	—		
	Data input hold time	Master	PCLKA division ratio set to 1/2	t_{HF}	0	—	ns	
			PCLKA division ratio set to a value other than 1/2	t_H	t_{PAcyc}	—		
		Slave			8.3	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			6	—	t_{PAcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			6	—	t_{PAcyc}	
	Data output delay time	Master		t_{OD}	—	6.3	ns	
		Slave			—	28		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{PAcyc}$	$8 \times t_{SPcyc} + 2 \times t_{PAcyc}$	ns	
		Slave			$6 \times t_{PAcyc}$	—		
	MOSI and MISO rise/fall time	Output		t_{Dr}, t_{Df}	—	5	ns	
		Input			—	1	µs	
	SSL rise/fall time	Output		t_{SSLr}, tSSLf	—	5	ns	
		Input			—	1	µs	
	Slave access time			t_{SA}	—	$2 \times t_{PAcyc} + 28$	ns	Figure 6.37, Figure 6.38
	Slave output release time			t_{REL}	—	$2 \times t_{PAcyc} + 28$	ns	

Note 1. t_{PAcyc}: PCLKA cycle



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Figure 6.32 RSPI Clock Timing

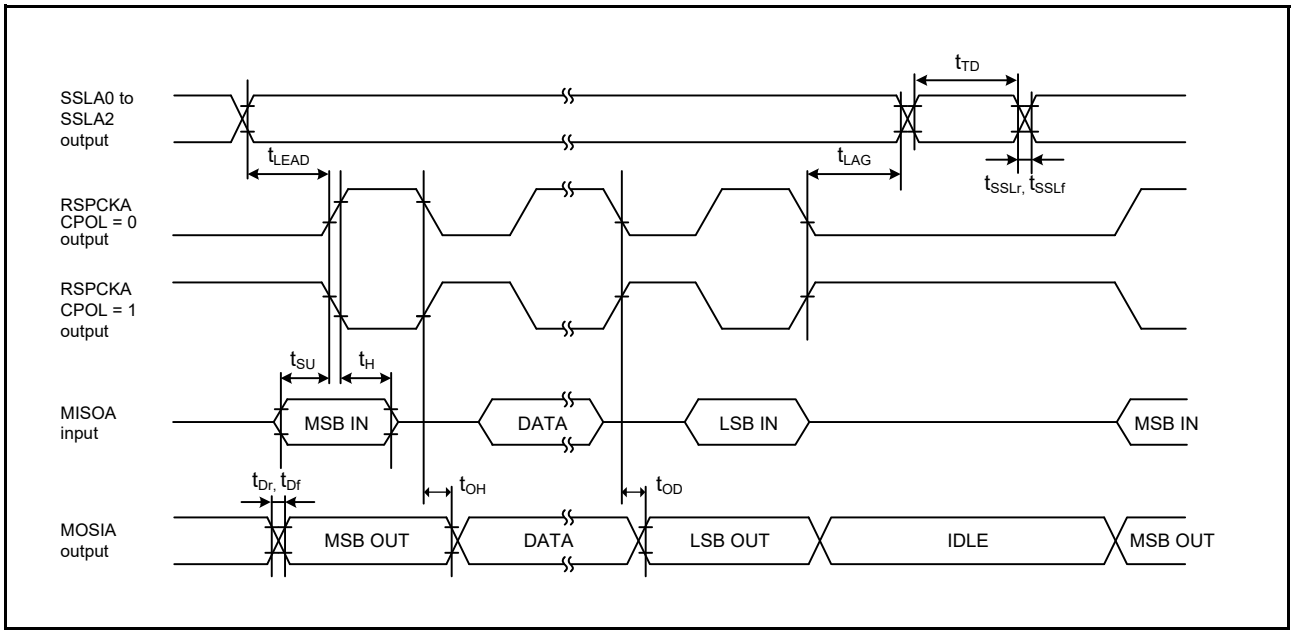


Figure 6.33 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2)

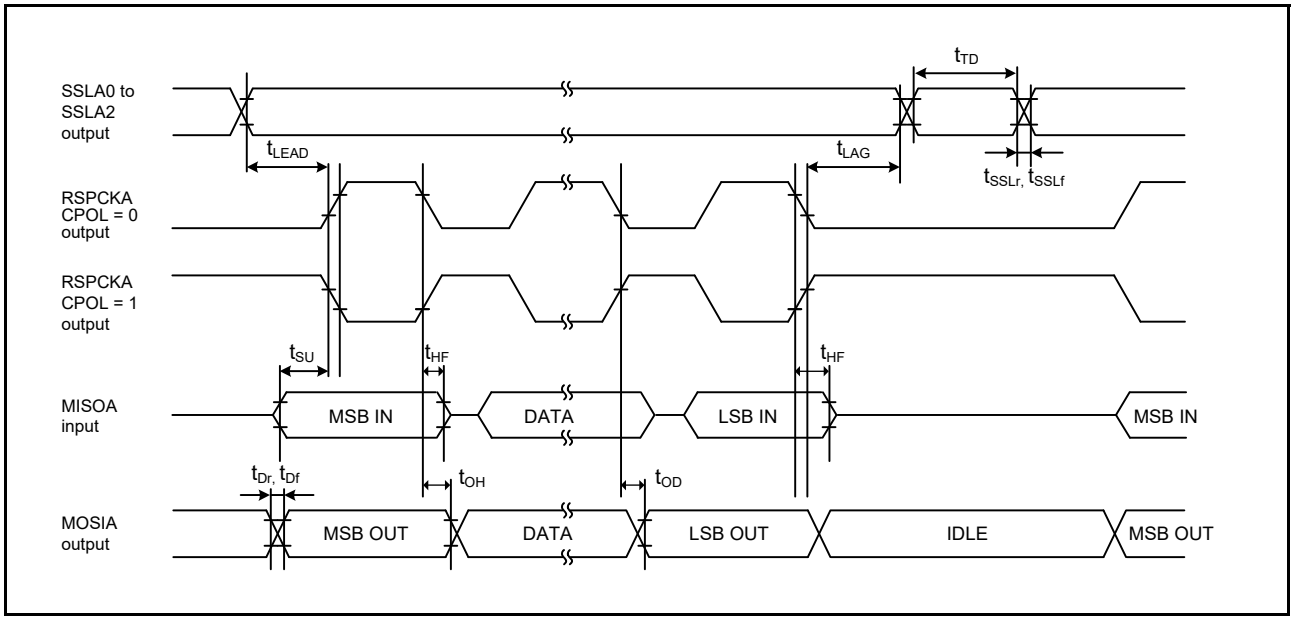


Figure 6.34 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to 1/2)

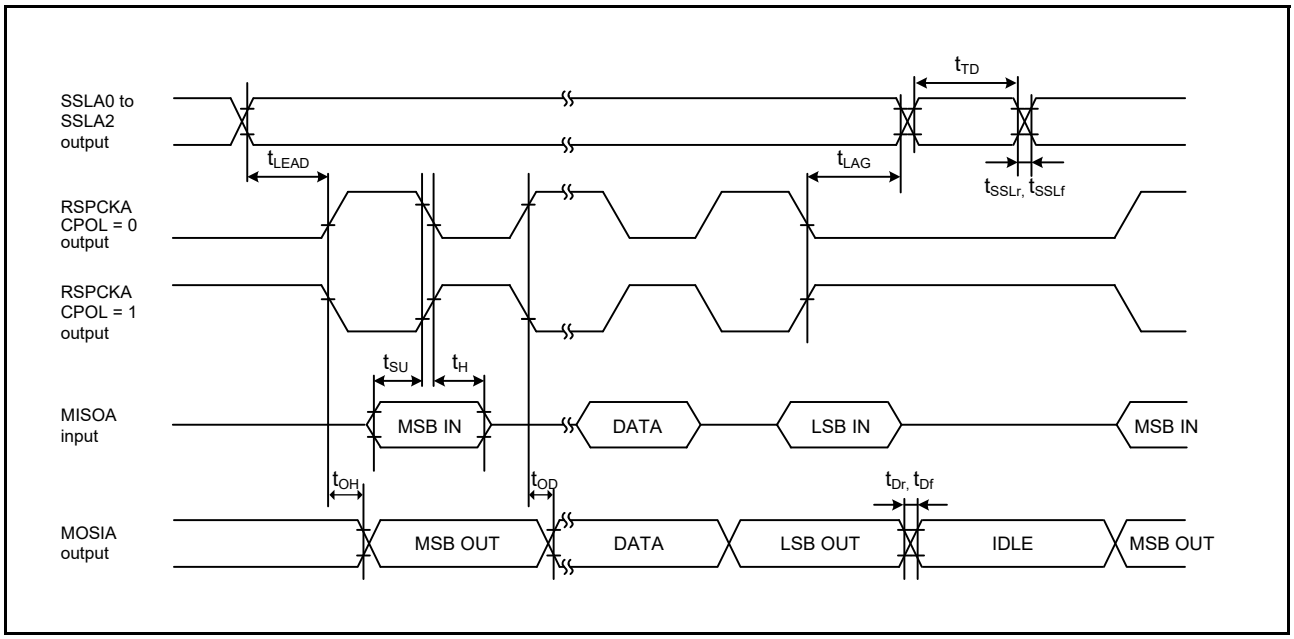


Figure 6.35 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2)

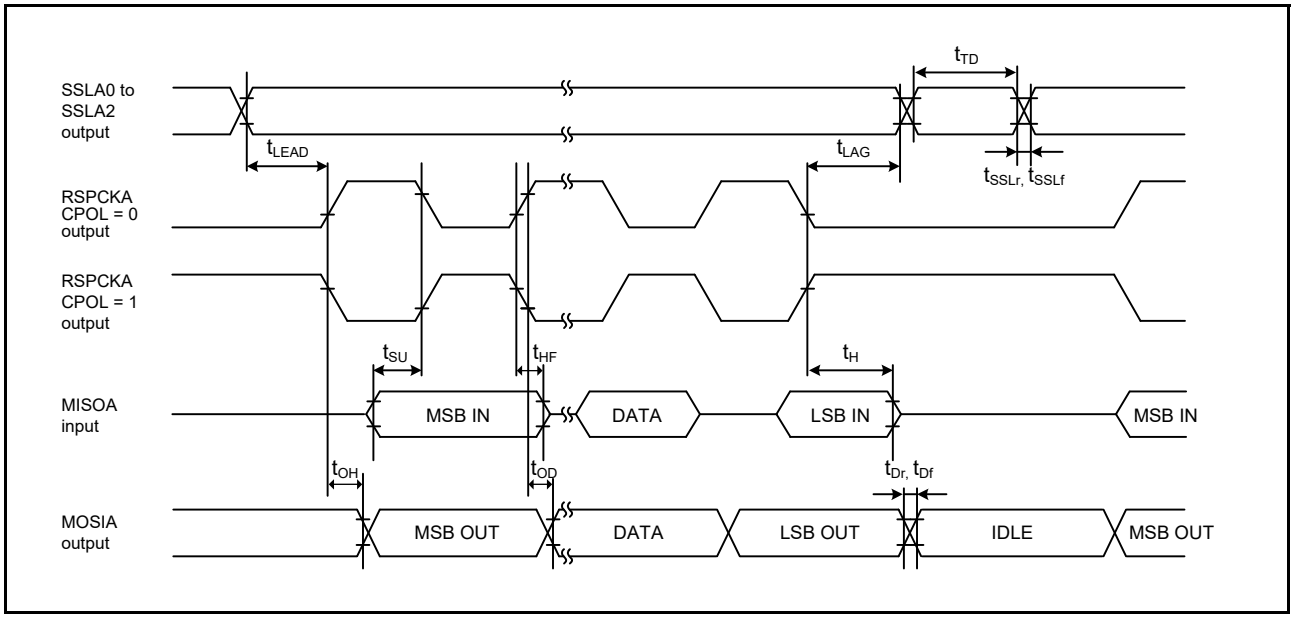


Figure 6.36 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to 1/2)

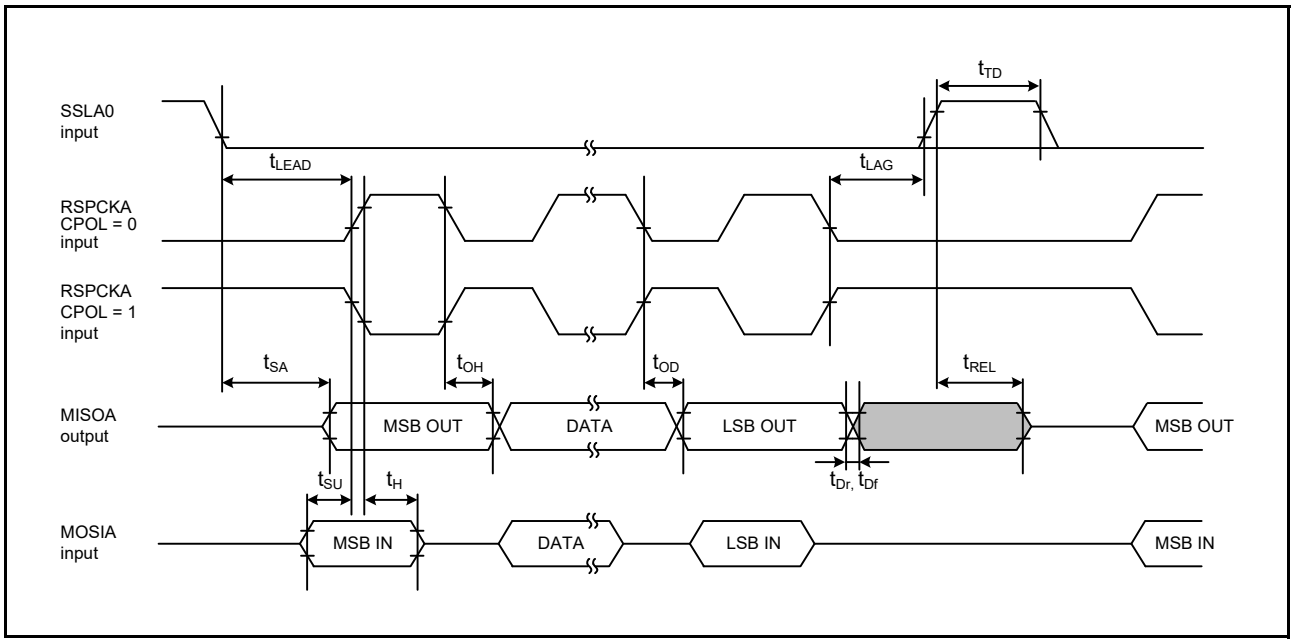


Figure 6.37 RSPI Timing (Slave, CPHA = 0)

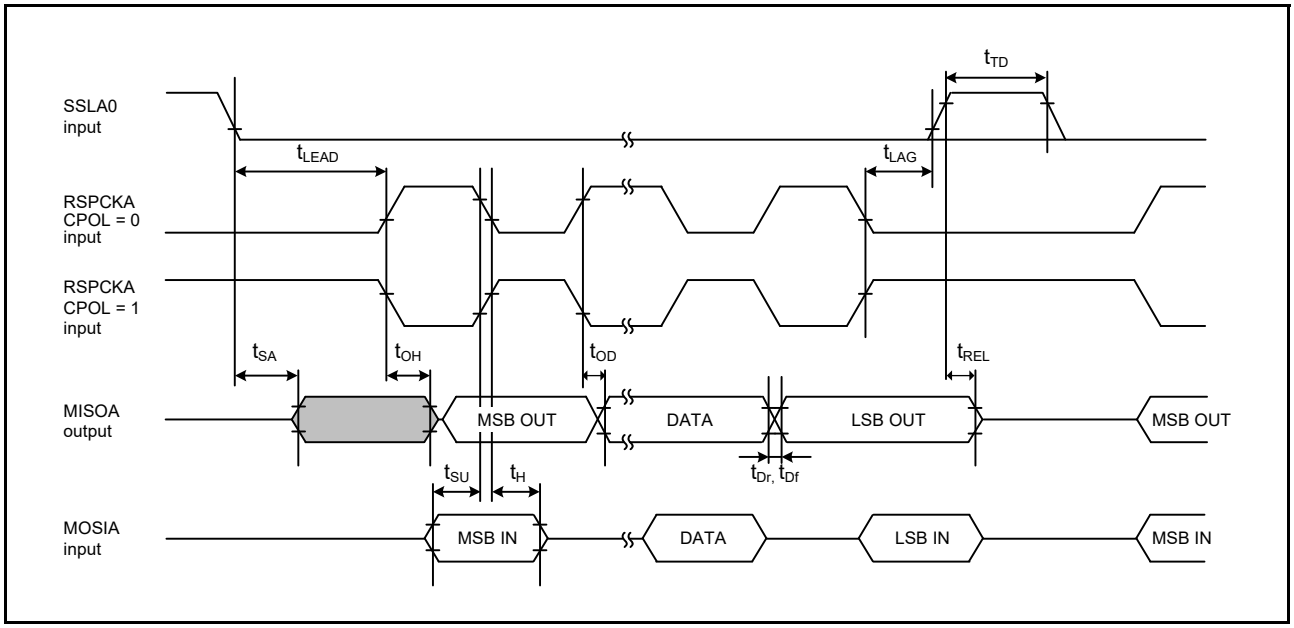


Figure 6.38 RSPI Timing (Slave, CPHA = 1)

6.4.5.11 QSPI

Table 6.39 QSPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
QSPI	QSPCLK clock cycle	t_{QScyc}	2	4080	t_{PBcyc}	Figure 6.39
	Data input setup time	t_{Su}	6.5	—	ns	Figure 6.40, Figure 6.41
	Data input hold time	t_{IH}	5	—	ns	
	SS setup time	t_{LEAD}	1.5	8.5	t_{QScyc}	
	SS hold time	t_{LAG}	1	8	t_{QScyc}	
	Data output delay time	t_{OD}	—	10.0	ns	
	Data output hold time	t_{OH}	–5	—	ns	
	Successive transmission delay time	t_{TD}	1	8	t_{QScyc}	

Note 1. t_{PBcyc}: PCLKB cycle

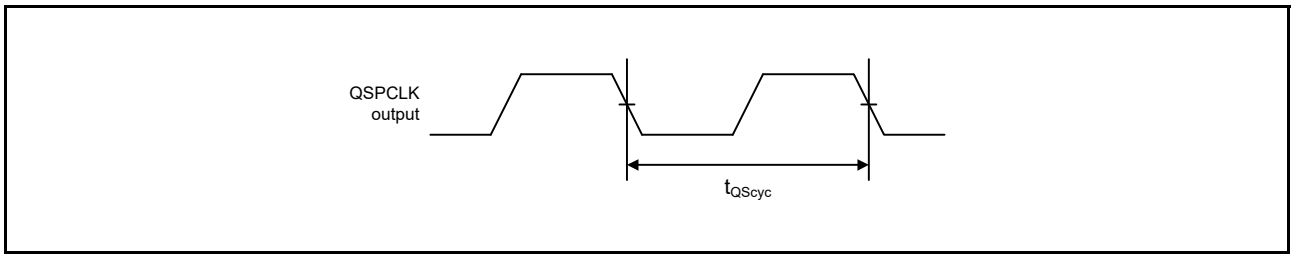


Figure 6.39 QSPI Clock Timing

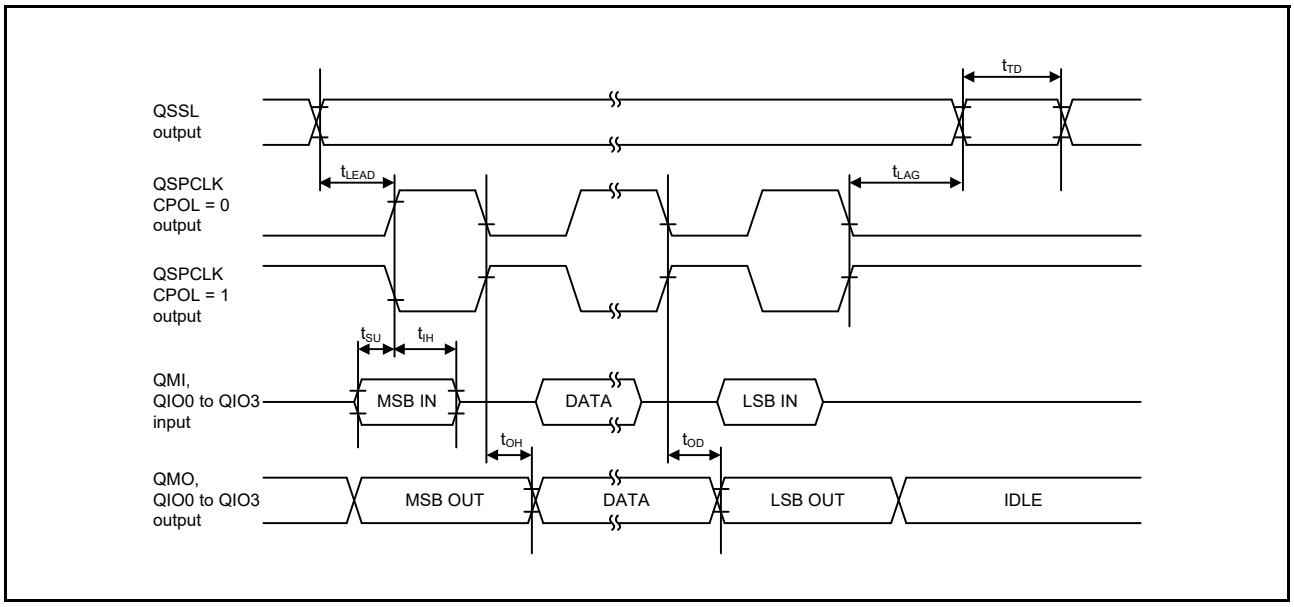


Figure 6.40 Transmit/Receive Timing (CPHA = 0)

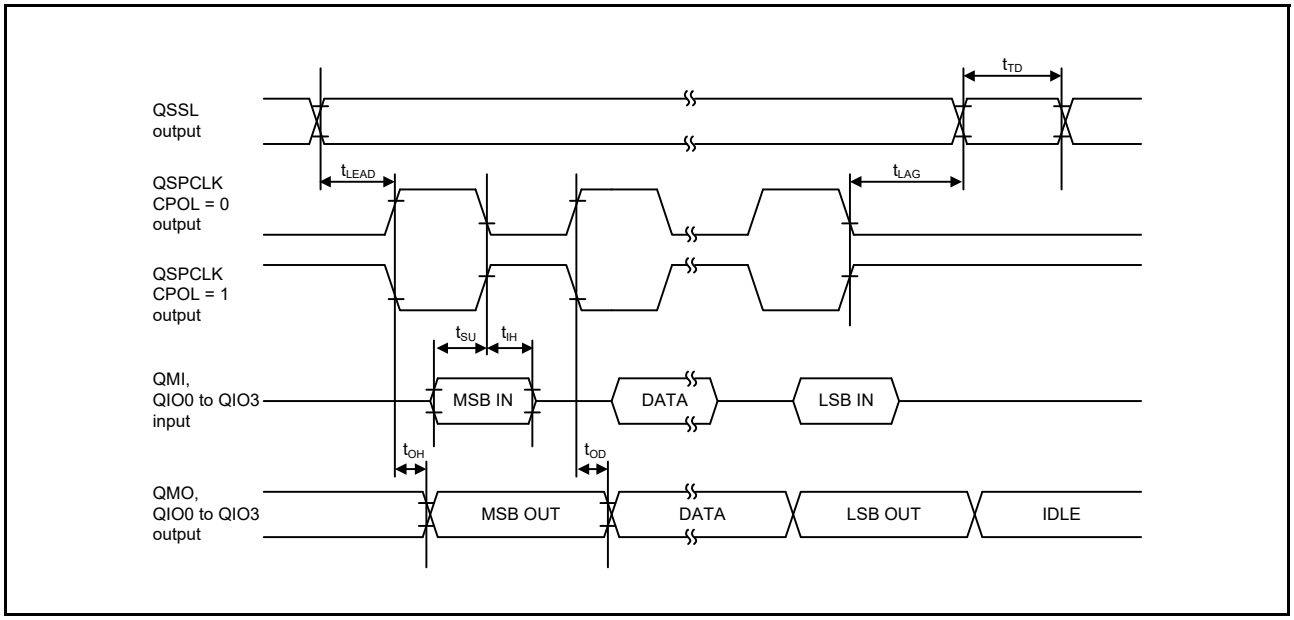


Figure 6.41 Transmit/Receive Timing (CPHA = 1)

6.4.5.12 RIIC

Table 6.40 RIIC Timing (1/2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
RIIC (Standard-mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 6.42
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	
RIIC (Fast-mode) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	20 × (External pull-up voltage/5.5V)	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 × (External pull-up voltage/5.5V)	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	

Table 6.40 RIIC Timing (2/2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
RIIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 240	—	ns	Figure 6.42
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 120	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 120	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	120	ns	
	SCL, SDA input fall time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 120	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 120	—	ns	
	Restart condition input setup time	t_{STAS}	120	—	ns	
	Stop condition input setup time	t_{STOS}	120	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 20	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	550	pF	

Note: t_{IICcyc}: RIIC internal reference clock (IICϕ) cycle
Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 2. C_b is the total capacitance of the bus lines.

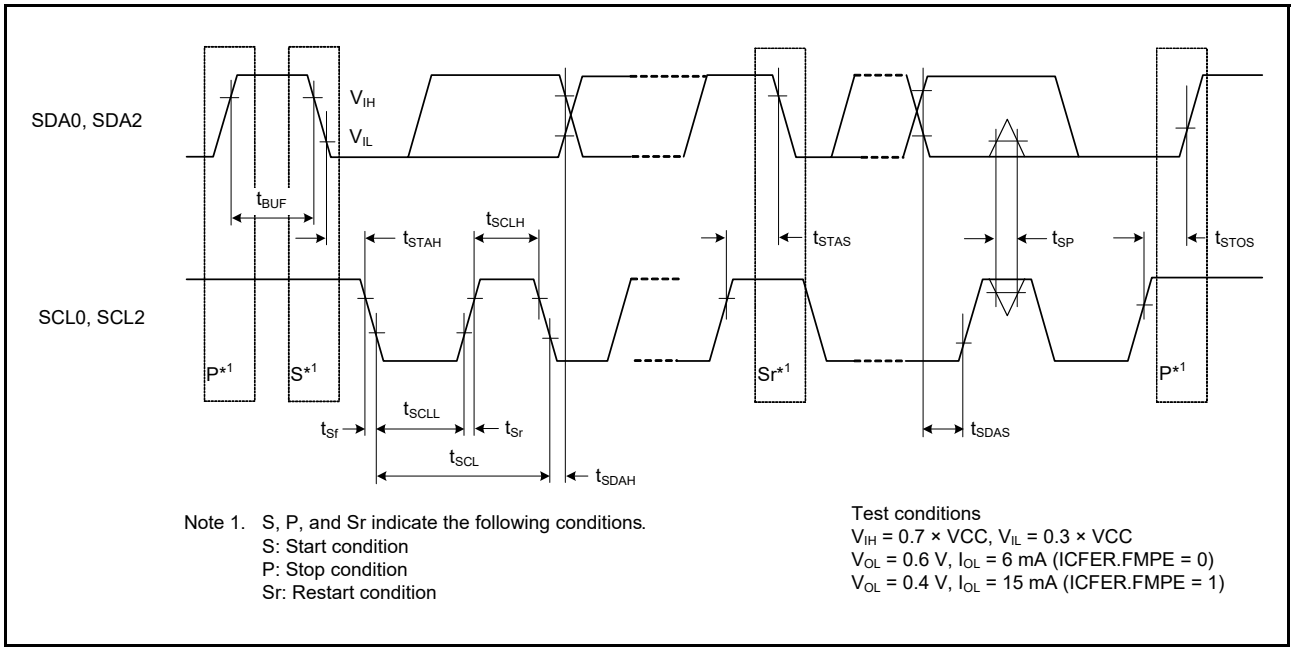


Figure 6.42 RIIC Bus Interface Input/Output Timing

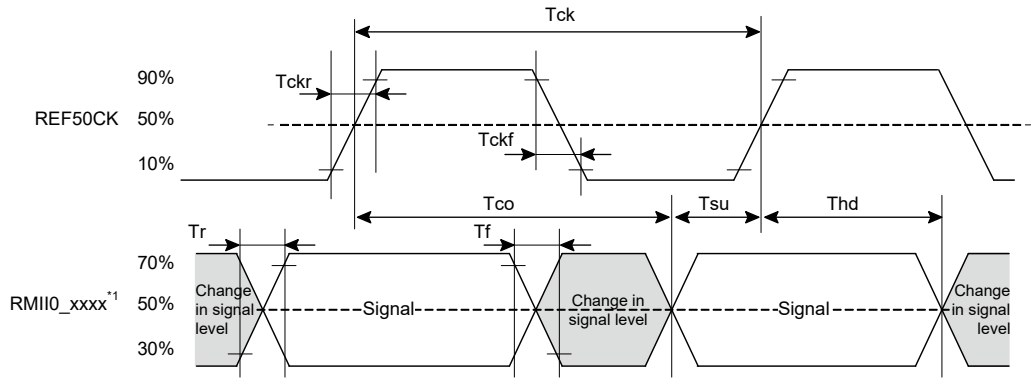
6.4.5.13 ETHERC

Table 6.41 ETHERC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
ETHERC (RMII)	REF50CK cycle time	T_{ck}	20	—	ns	Figure 6.43 to Figure 6.46
	REF50CK frequency Typ. 50 MHz	—	—	50 + 100 ppm	MHz	
	REF50CK duty	—	35	65	%	
	REF50CK rise/fall time	$T_{ckr/ckf}$	0.5	3.5	ns	
	RMII0_xxxx*1 output delay time	T_{co}	2.5	15.0	ns	
	RMII0_xxxx*2 setup time	T_{su}	3	—	ns	
	RMII0_xxxx*2 hold time	T_{hd}	1	—	ns	
	RMII0_xxxx*1, *2 rise/fall time	T_r/T_f	0.5	5	ns	
	ET0_WOL output delay time	t_{WOLd}	1	23.5	ns	Figure 6.47

Note 1. RMII0_TXD_EN, RMII0_TXD1, RMII0_TXD0
Note 2. RMII0_CRS_DV, RMII0_RXD1, RMII0_RXD0, RMII0_RX_ER



Note 1. RMII0_TXD_EN, RMII0_TXD1, RMII0_TXD0, RMII0_CRS_DV, RMII0_RXD1, RMII0_RXD0, RMII0_RX_ER

Figure 6.43 Timing with the REF50CK and RMII Signals

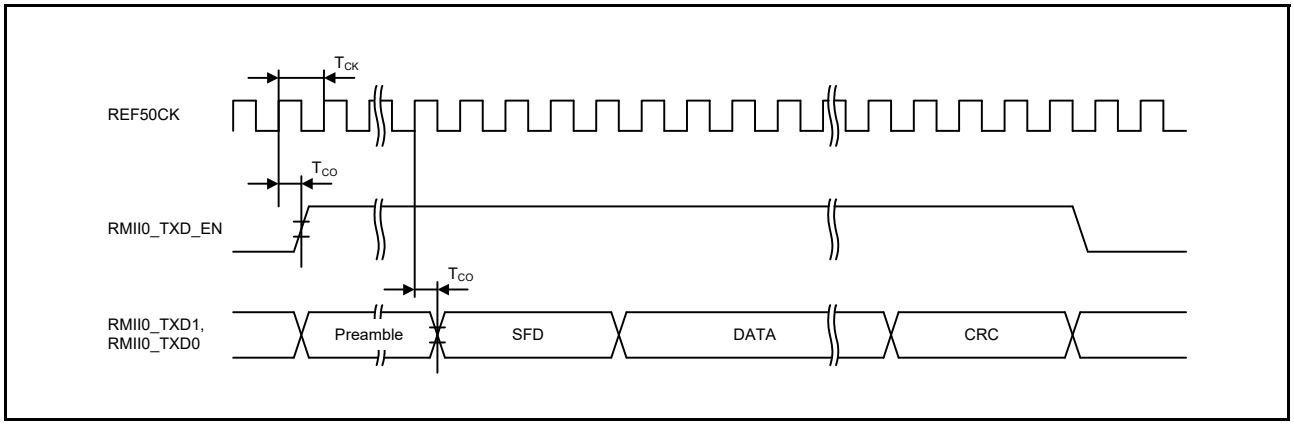


Figure 6.44 RMII Transmission Timing

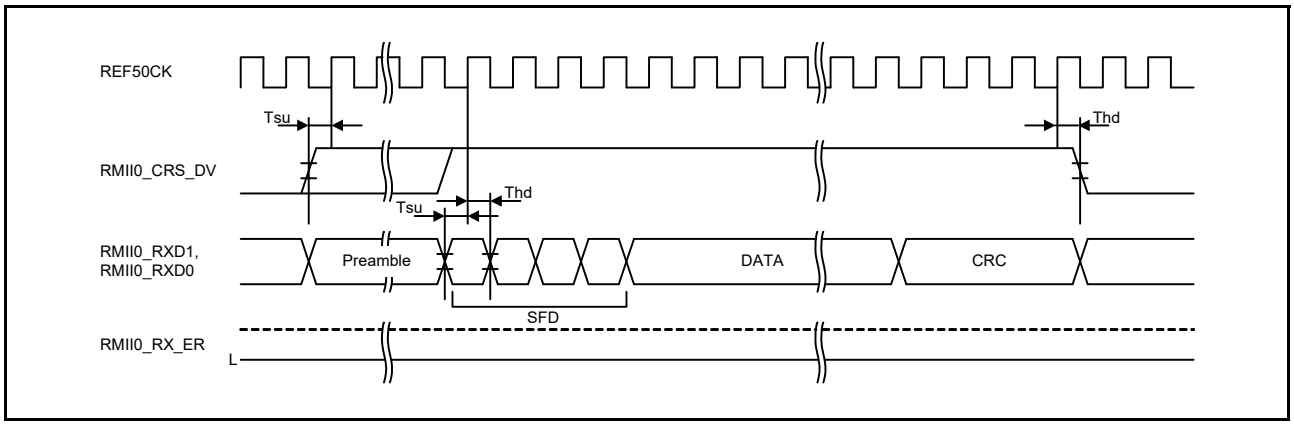


Figure 6.45 RMII Reception Timing (Normal Operation)

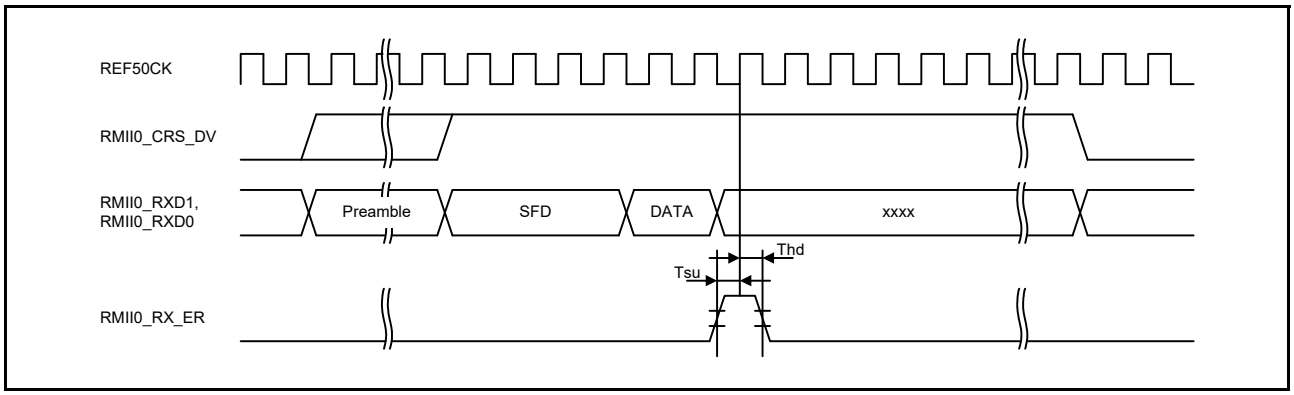


Figure 6.46 RMII Reception Timing (Error Occurrence)

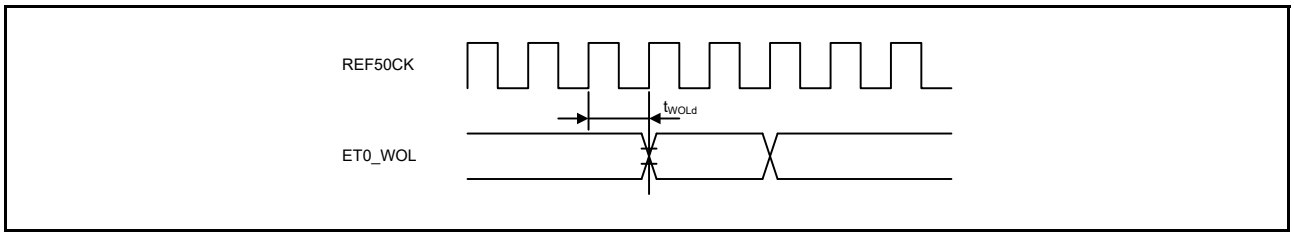


Figure 6.47 WOL Output Timing (RMII)

6.4.5.14 SDHI

Table 6.42 SDHI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
SDHI	SDHI_CLK pin output cycle time	$t_{PP(SD)}$	20	—	ns	Figure 6.48
	SDHI_CLK pin output high pulse width	$t_{WH(SD)}$	0.4 × $t_{PP(SD)}$	—	ns	
	SDHI_CLK pin output low pulse width	$t_{WL(SD)}$	0.4 × $t_{PP(SD)}$	—	ns	
	SDHI_CLK pin output rise time	$t_{TLH(SD)}$	—	3	ns	
	SDHI_CLK pin output fall time	$t_{THL(SD)}$	—	3	ns	
	Output data delay time (data transfer mode) for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ODLY(SD)}$	–6.5	4	ns	
	Input data setup time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ISU(SD)}$	6	—	ns	
	Input data hold time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{IH(SD)}$	2	—	ns	

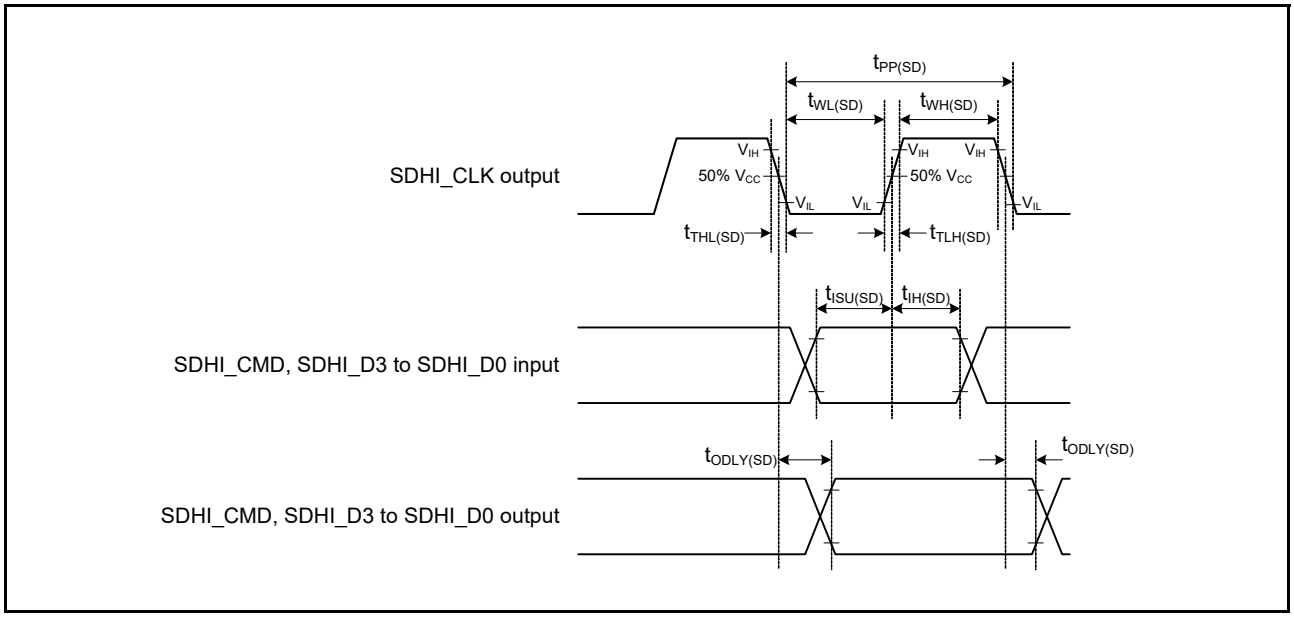


Figure 6.48 SD Host Interface Input/Output Signal Timing

6.4.5.15 SDSI

Table 6.43 SDSI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
SDSI	SDSI_CLK pin input cycle time	$t_{PP(SDSI)}$	20	—	ns	Figure 6.49
	SDSI_CLK pin input high pulse width	$t_{WH(SDSI)}$	0.4 × $t_{PP(SDSI)}$	—	ns	
	SDSI_CLK pin input low pulse width	$t_{WL(SDSI)}$	0.4 × $t_{PP(SDSI)}$	—	ns	
	SDSI_CLK pin input rise time	$t_{TLH(SDSI)}$	—	3	ns	
	SDSI_CLK pin input fall time	$t_{THL(SDSI)}$	—	3	ns	
	Input data setup time for SDSI_CMD and SDSI_D0 to SDSI_D3 pins	$t_{ISU(SDSI)}$	5	—	ns	
	Input data hold time for SDSI_CMD and SDSI_D0 to SDSI_D3 pins	$t_{IH(SDSI)}$	2	—	ns	
	Output data delay time for SDSI_CMD and SDSI_D0 to SDSI_D3 pins (default speed mode)	$t_{ODLY(SDSI)}$	0	14	ns	Figure 6.50
	Output data delay time for SDSI_CMD and SDSI_D0 to SDSI_D3 pins (high speed mode)		2.5	14	ns	Figure 6.51

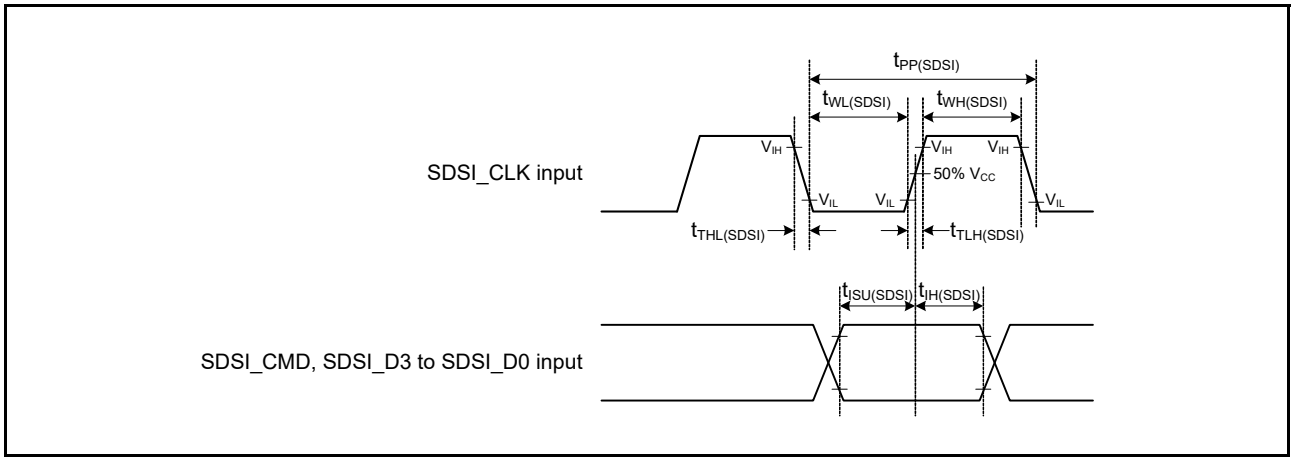


Figure 6.49 SD Slave Interface Input Signal Timing

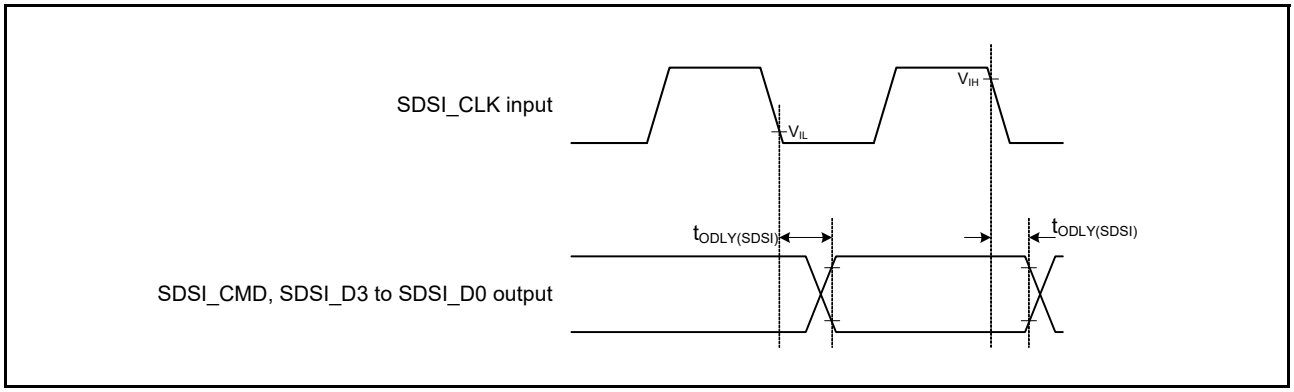


Figure 6.50 SD Slave Interface Output Signal Timing (Default Speed Mode)

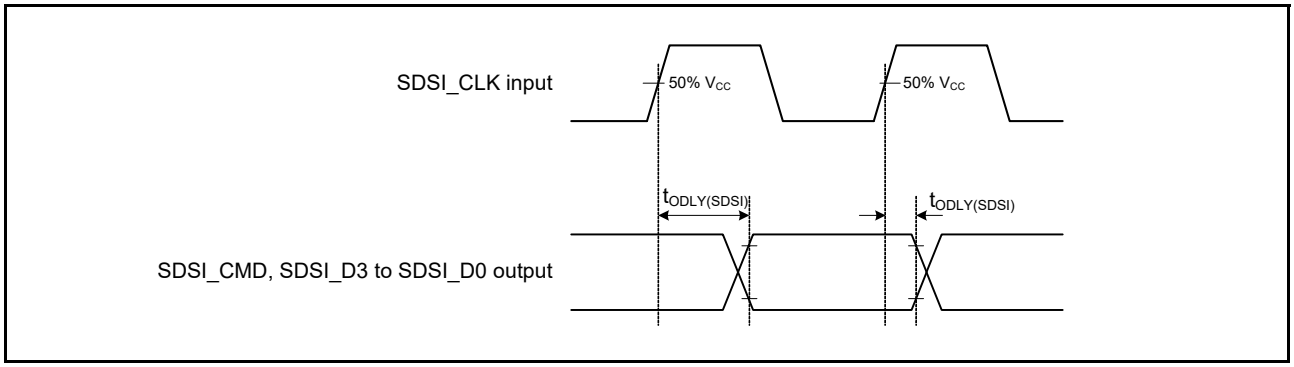


Figure 6.51 SD Slave Interface Output Signal Timing (High Speed Mode)

6.4.5.16 RF Transceiver

Table 6.44 RF Transceiver Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 3.3 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RF Transceiver	SCLK cycle time	t_{sccyc}	41.67	—	—	ns	Figure 6.52
	SCLK high pulse width	t_{sch}	18.5	—	—	ns	
	SCLK low pulse width	t_{scl}	18.5	—	—	ns	
	SIN setup time	t_{sisu}	15	—	—	ns	
	SIN hold time	t_{sihd}	15	—	—	ns	
	SOUT output delay time	t_{sodly}	—	—	14.8	ns	
	SEN setup time	t_{sesu}	33.3	—	—	ns	
	SEN hold time	t_{sehd}	200	—	—	ns	

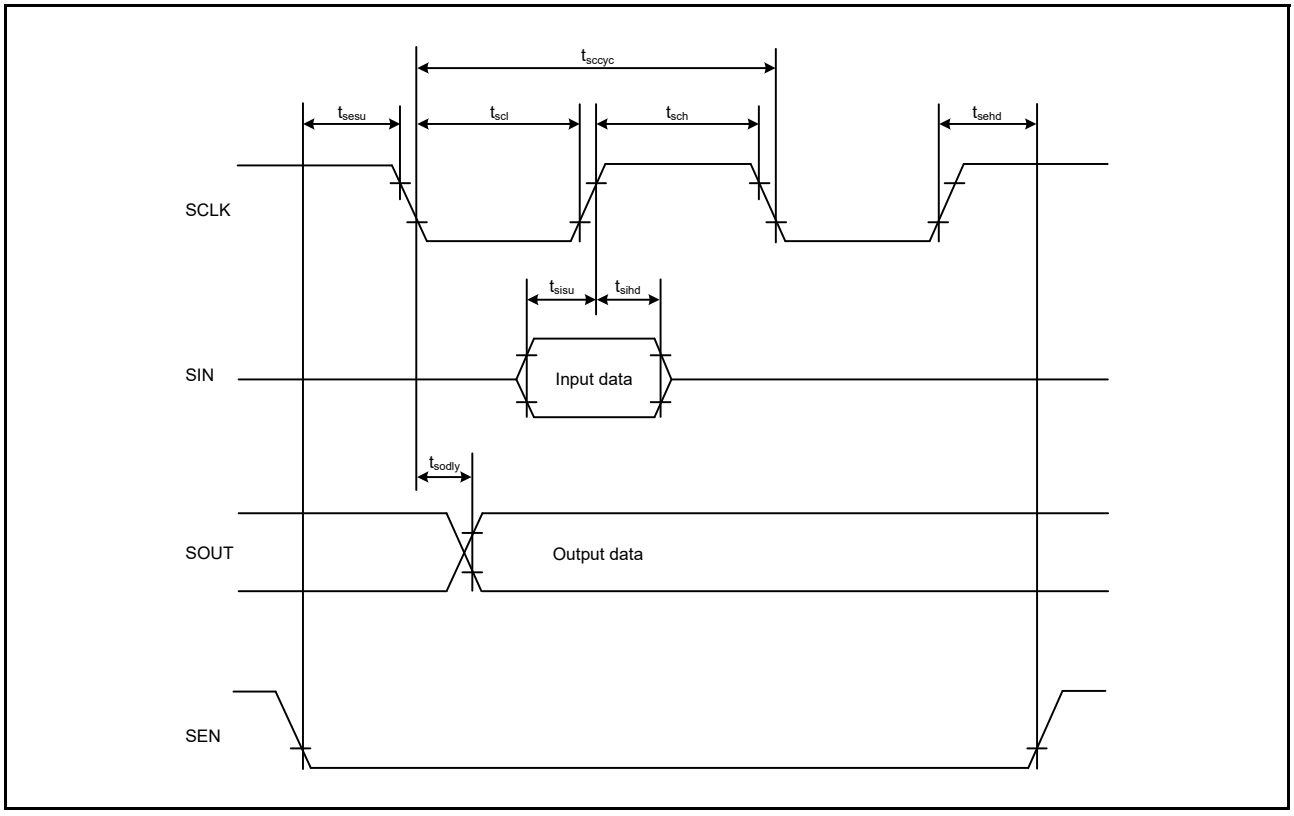


Figure 6.52 RF Transceiver Input/Output Timing

6.5 USB Characteristics

Table 6.45 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 3.0 to 3.6 V, 3.0 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
UCLK = 48 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage	V_{IH}	2.0	—	—	V	
	Input low level voltage	V_{IL}	—	—	0.8	V	
	Differential input sensitivity	V_{DI}	0.2	—	—	V	| DP – DM |
	Differential common mode range	V_{CM}	0.8	—	2.5	V	
Output characteristics	Output high level voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 µA
	Output low level voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 6.53
	Rise time	t_{FR}	4	—	20	ns	
	Fall time	t_{FF}	4	—	20	ns	
	Rise/fall time ratio	t_{FR}/t_{FF}	90	—	111.11	%	t_{FR}/t_{FF}
	Output resistance	Z_{DRV}	28	—	44	Ω	Rs = 27 Ω included
Pull-up and pull-down characteristics	DP pull-up resistance (when the function controller function is selected)	R_{pu}	0.900	—	1.575	kΩ	Idle state
			1.425	—	3.090		At transmission and reception
	DP/DM pull-down resistance (when the host controller function is selected)	R_{pd}	14.25	—	24.80	kΩ	

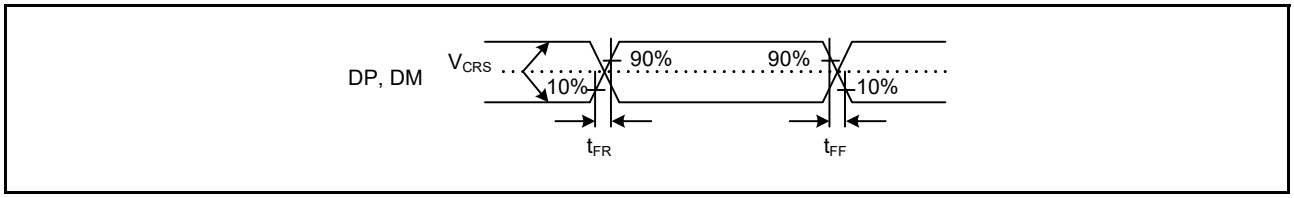


Figure 6.53 DP and DM Output Timing (Full-Speed)

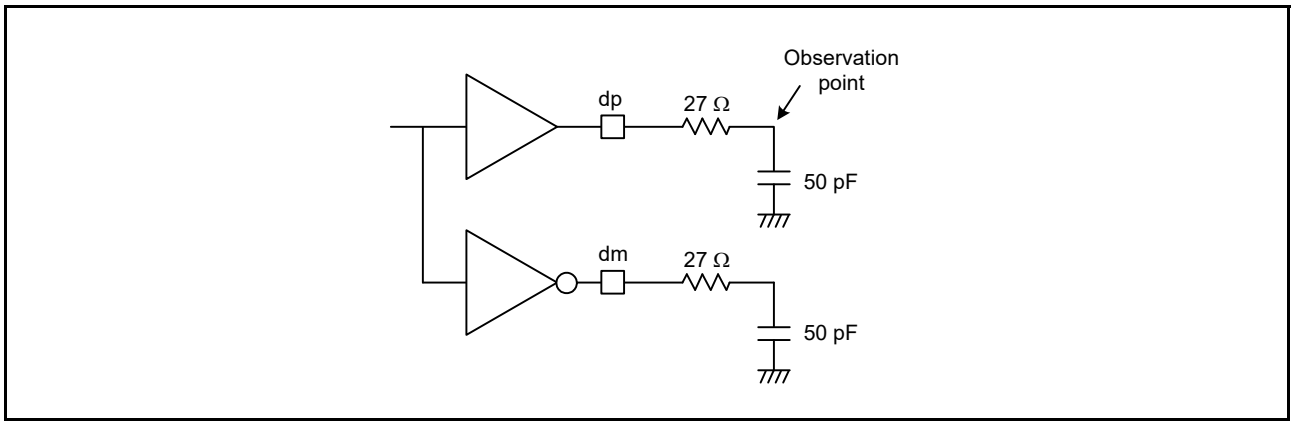


Figure 6.54 Test Circuit (Full-Speed)

6.6 A/D Conversion Characteristics

Table 6.46 12-Bit A/D (Unit 0) Conversion Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
PCLKB = PCLKC = 1 MHz to 60 MHz, $T_a = T_{opr}$,
Source impedance = 1.0 kΩ

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		8	—	12	Bit	
Analog input capacitance		—	—	30	pF	
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002)	Conversion time*1 (Operation at PCLKC = 60 MHz)	1.06 (0.4 + 0.25) *2	—	—	µs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 15 states
	Offset error	—	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error	—	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0 – 0.25 V
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	±3.0	±5.5	LSB	
	DNL differential nonlinearity error	—	±1.0	±2.0	LSB	
	INL integral nonlinearity error	—	±1.5	±3.0	LSB	
	Holding characteristics of sample-and-hold circuits	—	—	20	µs	
	Dynamic range	0.25	—	VREFH0 – 0.25	V	
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN003)	Conversion time*1 (Operation at PCLKC = 60 MHz)	0.48 (0.267)*2	—	—	µs	Sampling in 16 states
	Offset error	—	±1.0	±2.5	LSB	
	Full-scale error	—	±1.0	±2.5	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	±2.5	±4.5	LSB	
	DNL differential nonlinearity error	—	±0.5	±1.5	LSB	
	INL integral nonlinearity error	—	±1.0	±2.5	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The value in parentheses indicates the sampling time.

Table 6.47 12-Bit A/D (Unit 1) Conversion Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
PCLKB = PCLKD = 1 MHz to 60 MHz, $T_a = T_{opr}$,
Source impedance = 1.0 kΩ

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	8	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 60 MHz)	0.88 (0.633)*2	—	—	µs	Sampling in 38 states (ADSAM.SAM = 1)
Conversion time*1 (Operation at PCLKD = 30 MHz)	1 (0.500)*2	—	—	µs	Sampling in 15 states (ADSAM.SAM = 1)
Analog input capacitance	—	—	30	pF	
Offset error	—	±2.0	±3.5	LSB	
Full-scale error	—	±2.0	±3.5	LSB	
Quantization error	—	±0.5	—	LSB	
Absolute accuracy	—	±4.0	±6.0	LSB	
DNL differential nonlinearity error (Operation at PCLKD = 60 MHz)	—	±1.5	±4.0	LSB	
DNL differential nonlinearity error (Operation at PCLKD = 30 MHz)	—	±1.5	±2.5	LSB	
INL integral nonlinearity error (Operation at PCLKD = 60 MHz)	—	±2.0	±4.0	LSB	
INL integral nonlinearity error (Operation at PCLKD = 30 MHz)	—	±2.0	±3.5	LSB	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The value in parentheses indicates the sampling time.

Table 6.48 A/D Internal Reference Voltage Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
PCLKB = PCLKD = 60 MHz, $T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
A/D internal reference voltage	1.13	1.18	1.23	V	

6.7 Temperature Sensor Characteristics

Table 6.49 Temperature Sensor Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
$T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	±1	—	°C	
Temperature slope	—	4	—	mV/°C	
Output voltage	—	1.21	—	V	T_a = 25°C
Temperature sensor start time	—	—	30	µs	
Sampling time*1	4.15	—	—	µs	

Note 1. Set the S12AD1.ADSSTRT register such that the sampling time of the 12-bit A/D converter satisfies this specification.

6.8 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 6.50 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	Low power consumption function disabled*1	V_{POR}	2.5	2.6	2.7	V	Figure 6.55
		Low power consumption function enabled*2		1.8	2.25	2.7		
	Voltage detection circuit (LVD0)		V_{det0_1}	2.84	2.94	3.04		Figure 6.56
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	Voltage detection circuit (LVD1)		V_{det1_1}	2.89	2.99	3.09		Figure 6.57
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	Voltage detection circuit (LVD2)		V_{det2_1}	2.89	2.99	3.09		Figure 6.58
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
Internal reset time	Power-on reset time		t_{POR}	—	4.6	—	ms	Figure 6.55
	LVD0 reset time		t_{LVD0}	—	0.70	—		Figure 6.56
	LVD1 reset time		t_{LVD1}	—	0.57	—		Figure 6.57
	LVD2 reset time		t_{LVD2}	—	0.57	—		Figure 6.58
Minimum VCC down time			t_{VOFF}	200	—	—	µs	Figure 6.55, Figure 6.56
Response delay time			t_{det}	—	—	200	µs	Figure 6.55 to Figure 6.58
LVD operation stabilization time (after LVD is enabled)			$t_{d(E-A)}$	—	—	10	µs	Figure 6.57, Figure 6.58
Hysteresis width (LVD1 and LVD2)			V_{LVH}	—	70	—	mV	

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for the POR/ LVD.
Note 1. The low power consumption function is disabled and DEEPCUT[1:0] = 00b or 01b.
Note 2. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.

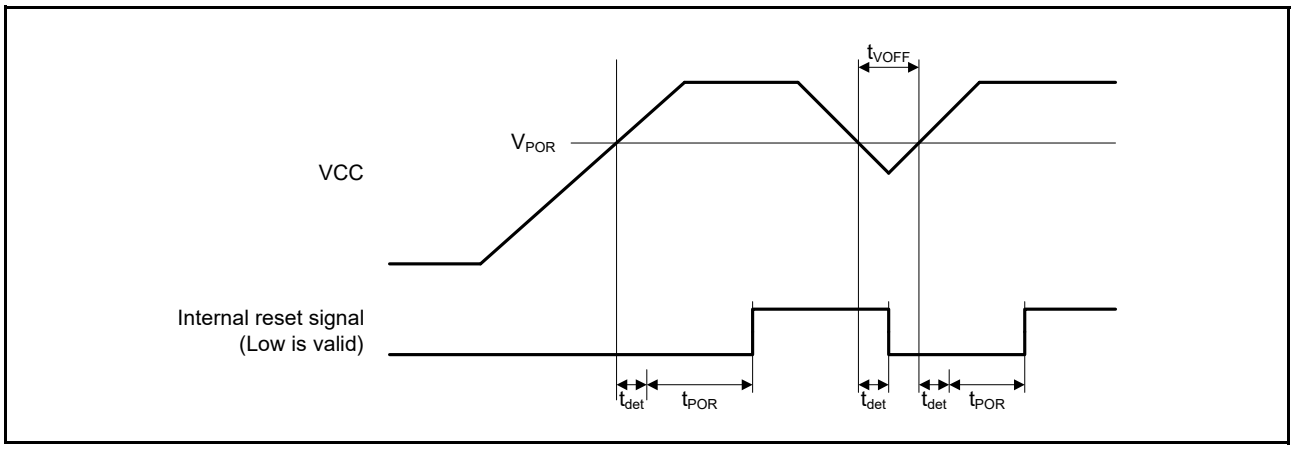


Figure 6.55 Power-on Reset Timing

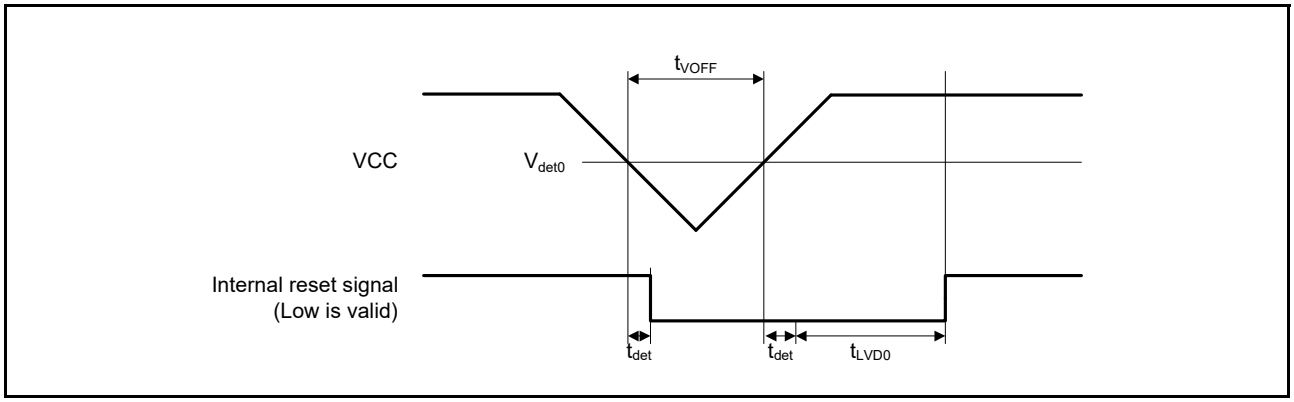


Figure 6.56 Voltage Detection Circuit Timing (V_{det0})

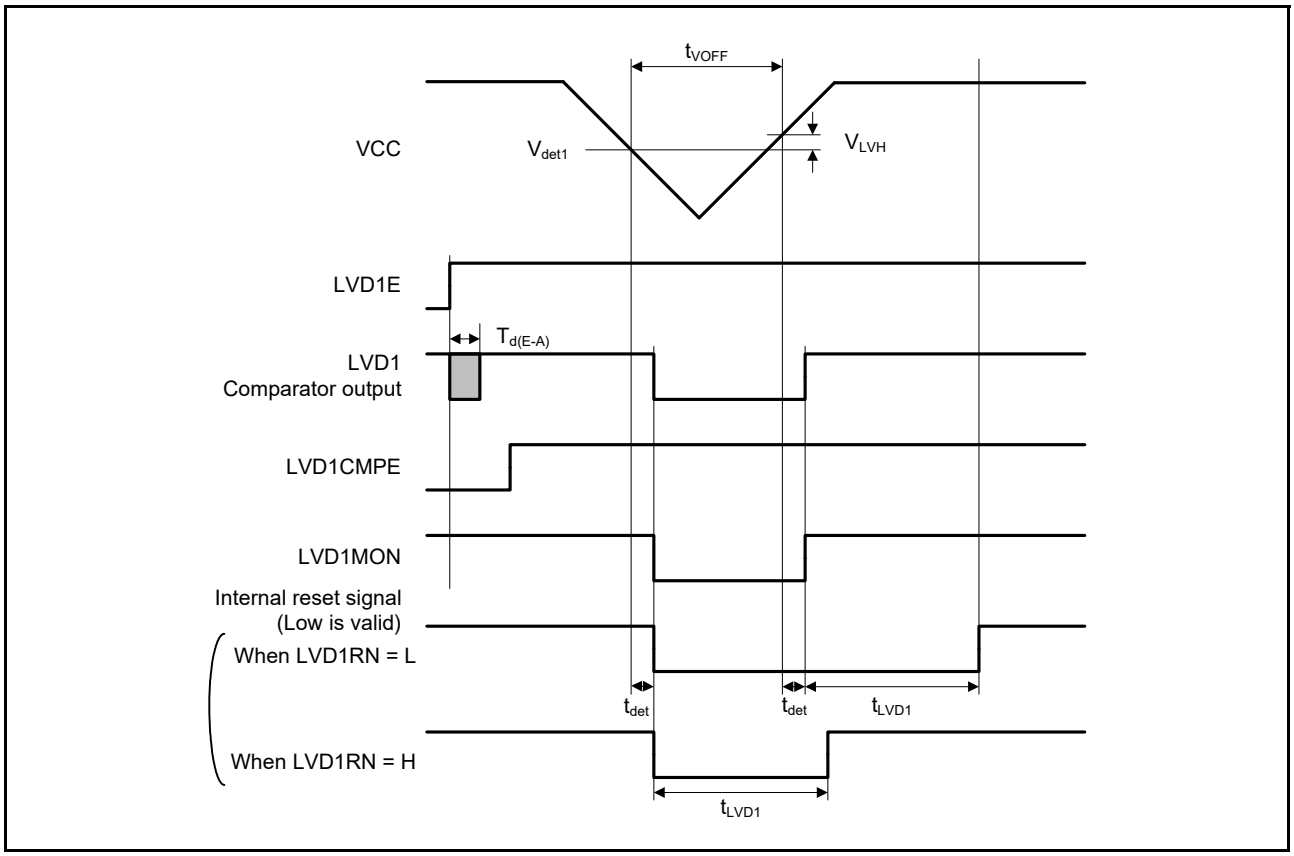


Figure 6.57 Voltage Detection Circuit Timing (V_{det1})

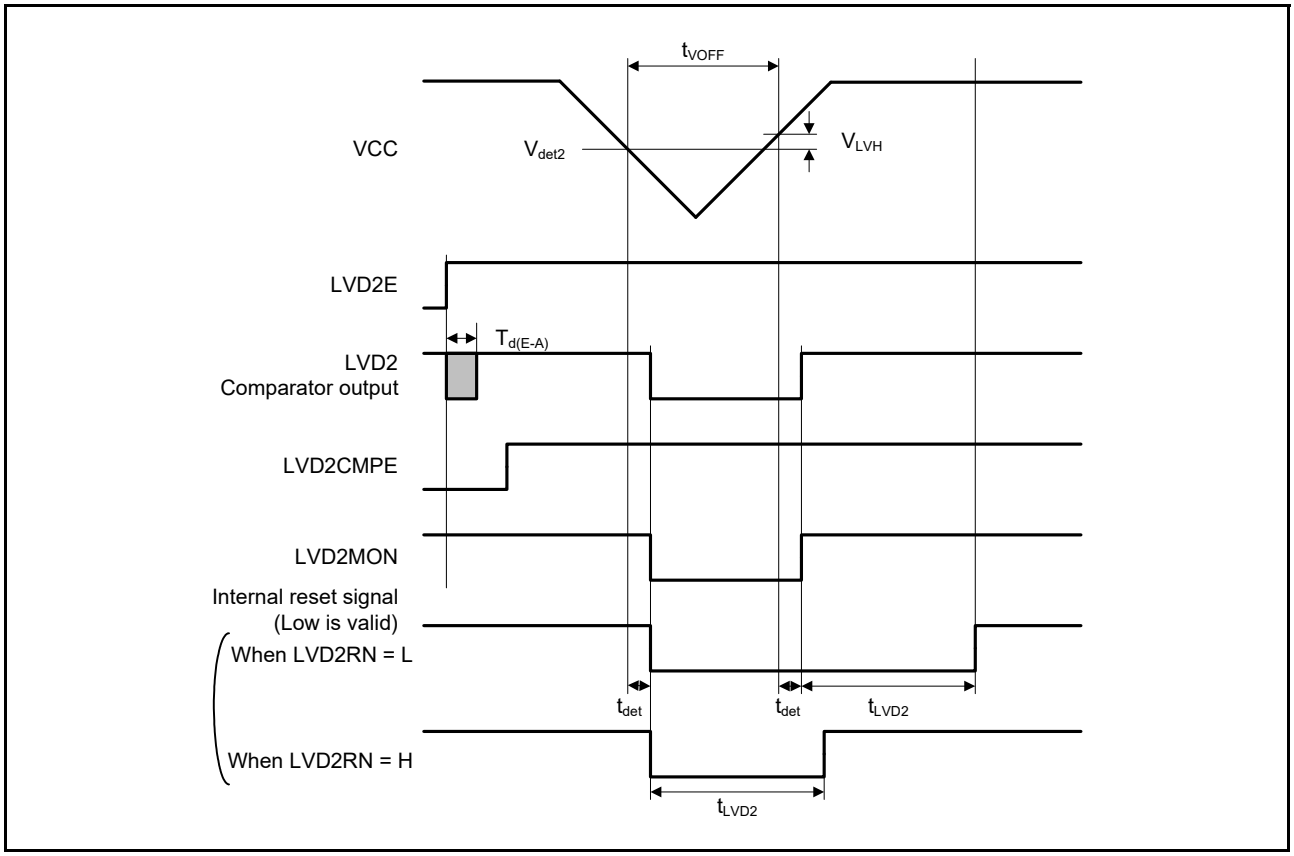


Figure 6.58 Voltage Detection Circuit Timing (V_{det2})

6.9 Oscillation Stop Detection Timing

Table 6.51 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 6.59

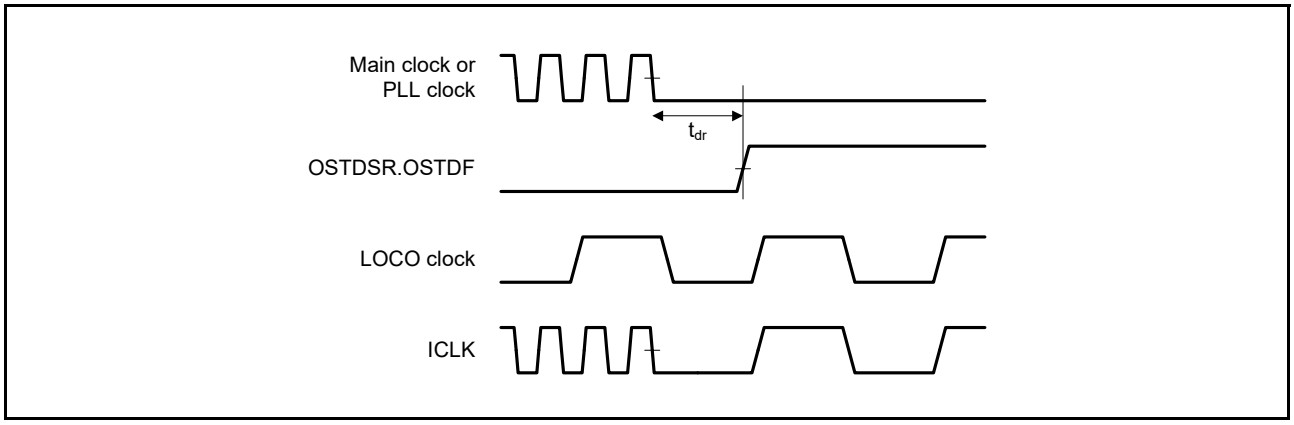


Figure 6.59 Oscillation Stop Detection Timing

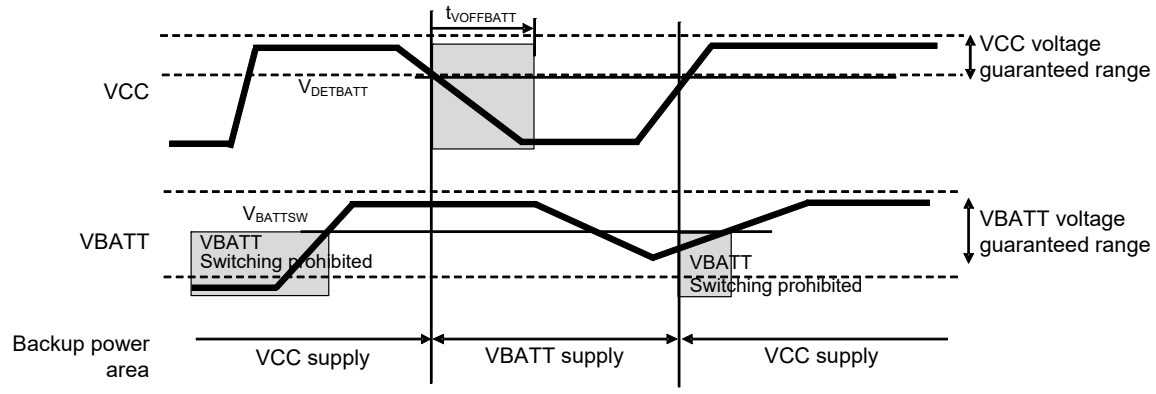
6.10 Battery Backup Function Characteristics

Table 6.52 Battery Backup Function Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = 2.7 to 3.6 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
V_{BATT} = 2.0 to 3.6 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage level for switching to battery backup	$V_{DETBATT}$	2.50	2.60	2.70	V	Figure 6.60
Lower-limit V_{BATT} voltage for power supply switching due to VCC voltage drop	V_{BATTSW}	2.70	—	—		
VCC-off period for starting power supply switching	$t_{VOFFBATT}$	200	—	—	µs	

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).



Note. The VBATT voltage when the supplied power source switches from Vcc to V_{BATT} should not be lower than V_{BATTSW}, the lower-limit VBATT voltage for switching between power supplies due to a drop in the VCC voltage.

Figure 6.60 Battery Backup Function Characteristics

6.11 Flash Memory Characteristics

Table 6.53 Code Flash Memory Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
Temperature range for programming/erasure: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			FCLK = 15 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test Conditions
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Programming time N_{PEC} ≤ 100 times	128 bytes	t_{P128}	—	0.75	13.2	—	0.38	6.6	—	0.34	6	ms	
	8 Kbytes	t_{P8K}	—	49	176	—	25	88	—	22	80	ms	
	32 Kbytes	t_{P32K}	—	194	704	—	97	352	—	88	320	ms	
Programming time N_{PEC} > 100 times	128 bytes	t_{P128}	—	0.91	15.8	—	0.46	8	—	0.41	7.2	ms	
	8 Kbytes	t_{P8K}	—	60	212	—	30	106	—	27	96	ms	
	32 Kbytes	t_{P32K}	—	234	848	—	117	424	—	106	384	ms	
Erasure time N_{PEC} ≤ 100 times	8 Kbytes	t_{E8K}	—	78	216	—	48	132	—	43	120	ms	
	32 Kbytes	t_{E32K}	—	283	864	—	173	528	—	157	480	ms	
Erasure time N_{PEC} > 100 times	8 Kbytes	t_{E8K}	—	94	260	—	58	158	—	52	144	ms	
	32 Kbytes	t_{E32K}	—	341	1040	—	208	632	—	189	576	ms	
Programming/erasure cycle*1		N_{PEC}	10000 *2	—	—	10000 *2	—	—	10000 *2	—	—	Times	
Suspend delay time during programming		t_{SPD}	—	—	264	—	—	132	—	—	120	µs	
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	216	—	—	132	—	—	120	µs	
Second suspend delay time during erasure (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.7	—	—	1.7	ms	
Suspend delay time during erasure (in erasure priority mode)		t_{SEED}	—	—	1.7	—	—	1.7	—	—	1.7	ms	
Forced stop command		t_{FD}	—	—	32	—	—	22	—	—	20	µs	
Data hold time*3, *4		t_{DRP}	20	—	—	20	—	—	20	—	—	Year	T_a ≤ 85°C

Note 1. Definition of program/erase cycle:
The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is n, each block can be erased n times. For instance, when 128-byte program is performed 64 times for different addresses in 8-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).

Note 2. Characteristics are degraded as the number of program/erase increases. This is the minimum value of program/erase cycles to guarantee all characteristics listed in this table.

Note 3. This shows the characteristic when the flash memory writer or self-programming library from Renesas Electronics is in use, and the number of times programming and erasure proceed does not exceed the specified value.

Note 4. These values are based on the results of reliability testing.

Table 6.54 Data Flash Memory Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
Temperature range for programming/erasure: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			FCLK = 15 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test Conditions
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Programming time	4 bytes	t_{DP4}	—	0.36	3.8	—	0.18	1.9	—	0.16	1.7	ms	
Erasure time	64 bytes	t_{DP64}	—	3.1	18	—	1.9	11	—	1.7	10	ms	
	128 bytes	t_{DP128}	—	4.7	27	—	2.9	16	—	2.6	15	ms	
	256 bytes	t_{DP256}	—	8.9	50	—	5.4	31	—	4.9	28	ms	
Blank check time	4 bytes	t_{DBC4}	—	—	84	—	—	33	—	—	30	µs	
	64 bytes	t_{DBC64}	—	—	280	—	—	110	—	—	100	µs	
	2 Kbytes	t_{DBC2K}	—	—	6160	—	—	2420	—	—	2200	µs	
Programming/erasure cycle*1		N_{DPEC}	100000 *2	—	—	100000 *2	—	—	100000 *2	—	—	Times	
Suspend delay time during programming		t_{DSPD}	—	—	264	—	—	132	—	—	120	µs	
First suspend delay time during erasure (in suspend priority mode)	64 bytes	—	—	—	216	—	—	132	—	—	120	µs	
	128 bytes	—	—	—	216	—	—	132	—	—	120	µs	
	256 bytes	—	—	—	216	—	—	132	—	—	120	µs	
Second suspend delay time during erasure (in suspend priority mode)	64 bytes	—	—	—	300	—	—	300	—	—	300	µs	
	128 bytes	—	—	—	390	—	—	390	—	—	390	µs	
	256 bytes	—	—	—	570	—	—	570	—	—	570	µs	
Suspend delay time during erasing (in suspend priority mode)	64 bytes	—	—	—	300	—	—	300	—	—	300	µs	
	128 bytes	—	—	—	390	—	—	390	—	—	390	µs	
	256 bytes	—	—	—	570	—	—	570	—	—	570	µs	
Forced stop command		t_{FD}	—	—	32	—	—	22	—	—	20	µs	
Data hold time*3, *4		t_{DDRP}	20	—	—	20	—	—	20	—	—	Year	T_a ≤ 85°C

Note 1. Definition of program/erase cycle:
The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is n, each block can be erased n times. For instance, when 4-byte program is performed 512 times for different addresses in 2-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).

Note 2. Characteristics are degraded as the number of program/erase increases. This is the minimum value of program/erase cycles to guarantee all characteristics listed in this table.

Note 3. This shows the characteristic when the flash memory writer or self-programming library from Renesas Electronics is in use, and the number of times programming and erasure proceed does not exceed the specified value.

Note 4. These values are based on the results of reliability testing.

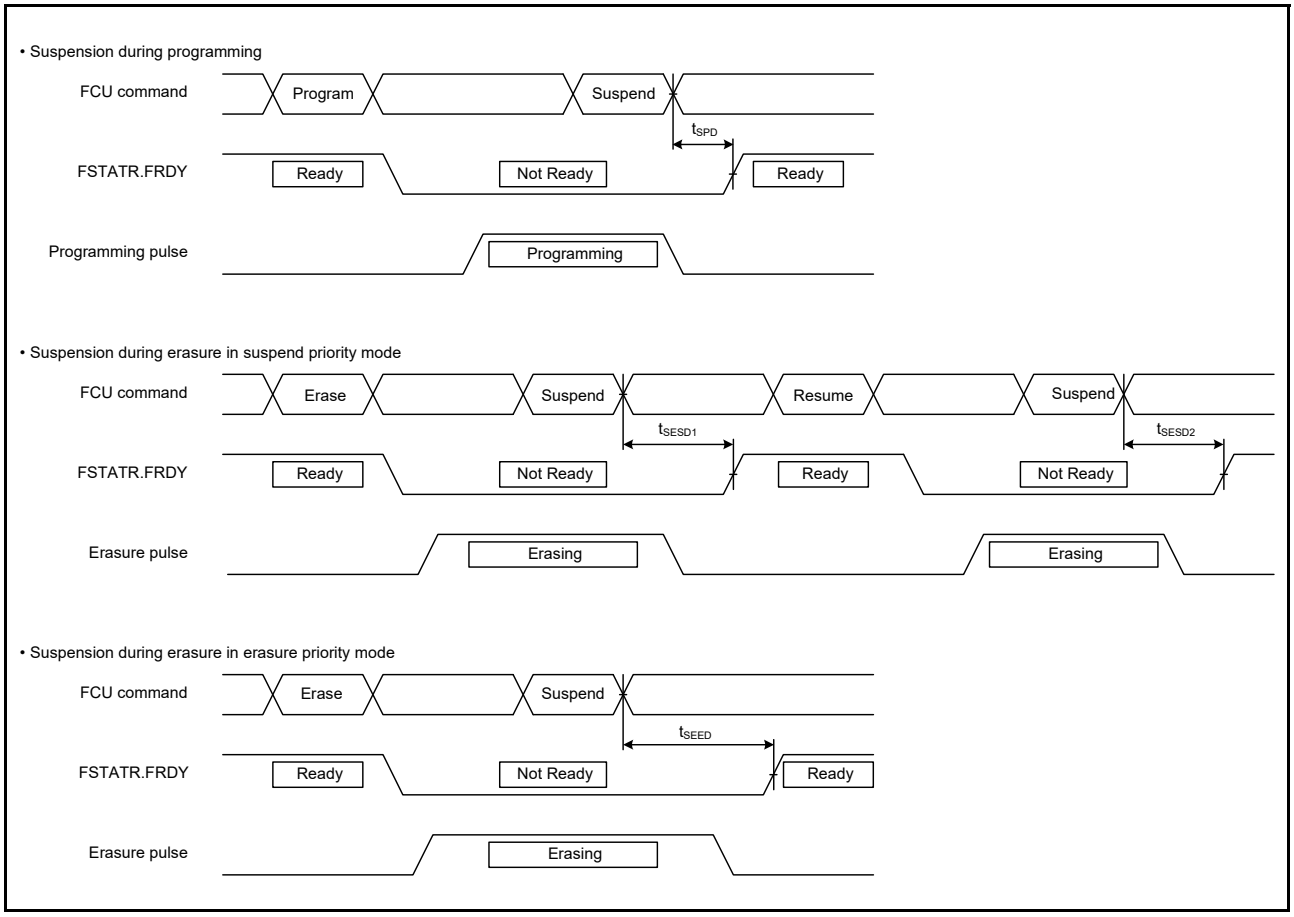


Figure 6.61 Flash Memory Programming/Erasure Suspension Timing

6.12 Boundary Scan

Table 6.55 Boundary Scan Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
$T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the driving ability control register.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
TCK clock cycle time	t_{TCKcyc}	100	—	—	ns	Figure 6.62
TCK clock high pulse width	t_{TCKH}	45	—	—	ns	
TCK clock low pulse width	t_{TCKL}	45	—	—	ns	
TCK clock rise time	t_{TCKr}	—	—	5	ns	
TCK clock fall time	t_{TCKf}	—	—	5	ns	
TRST# pulse width	t_{TRSTW}	20	—	—	t_{TCKcyc}	Figure 6.63
TMS setup time	t_{TMSS}	20	—	—	ns	Figure 6.64
TMS hold time	t_{TMSH}	20	—	—	ns	
TDI setup time	t_{TDIS}	20	—	—	ns	
TDI hold time	t_{TDIH}	20	—	—	ns	
TDO data delay time	t_{TDOD}	—	—	40	ns	

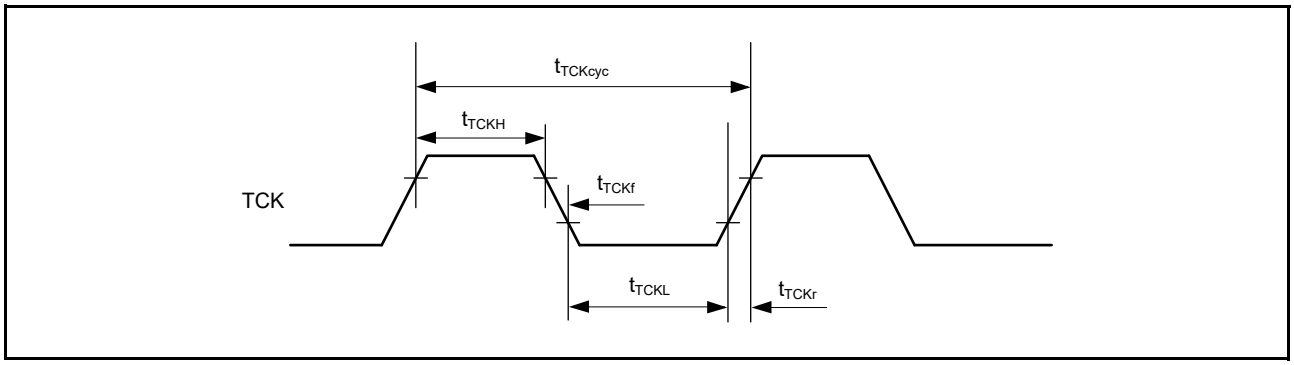


Figure 6.62 Boundary Scan TCK Timing

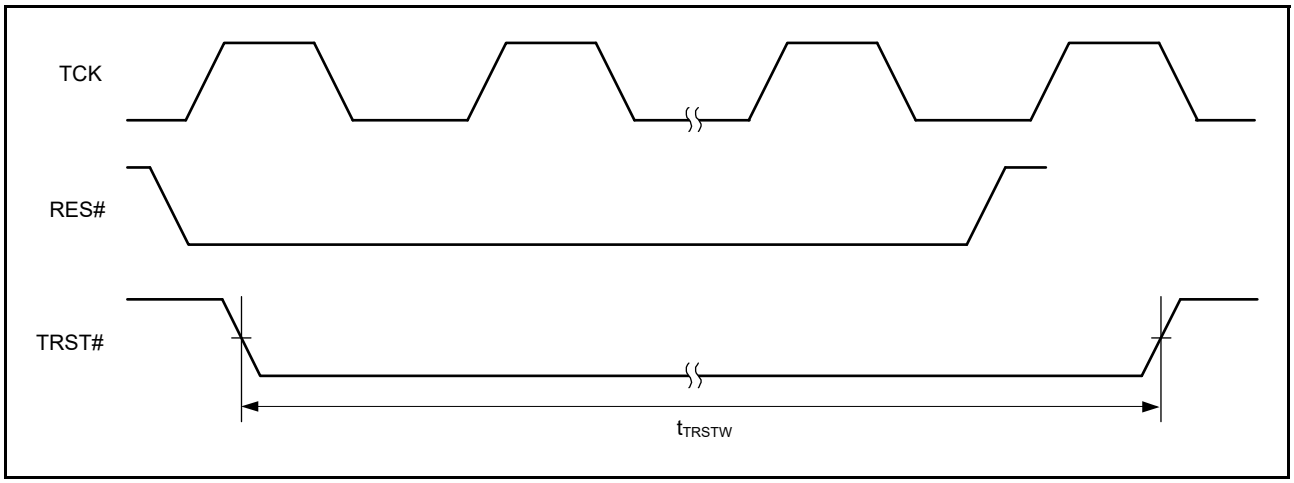


Figure 6.63 Boundary Scan TRST# Timing

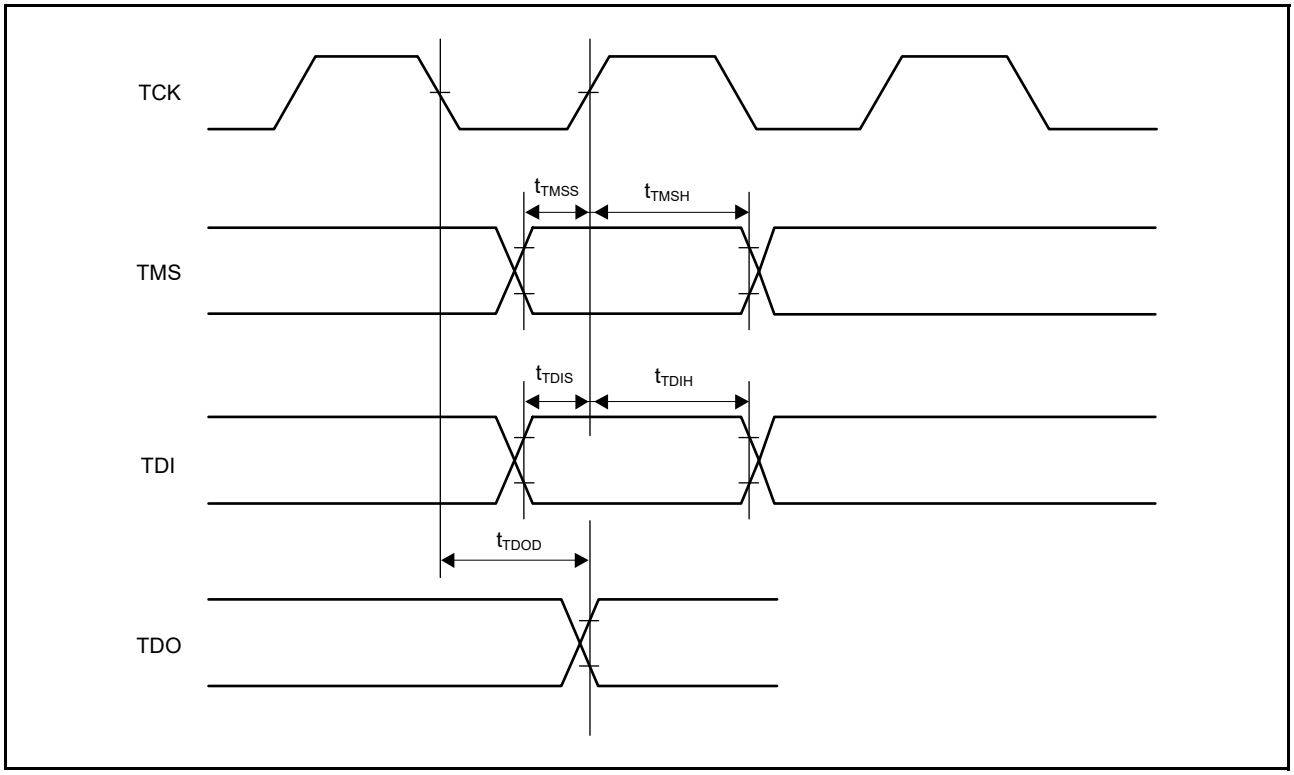


Figure 6.64 Boundary Scan Input/Output Timing

6.13 RF Transceiver Characteristics

6.13.1 Characteristics of the Transceiver Reception

Table 6.56 Reception Sensitivity for SUN FSK

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 3.3 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
Packet length = 250 bytes, packet error rate (PER) = 10%, with no forward error correction (FEC), T_a = 25°C

Modulation Parameter	Channel Spacing [kHz]	Data Rate [kbps]	Modulation Index	Modulation Method	Min.	Typ.	Max.	Unit
North America (Frequency: 920.6 MHz)								
Operating mode #1a	50	10	1	2-GFSK	—	–116	—	dBm
Operating mode #1b	100	20	1	2-GFSK	—	–113	—	dBm
Operating mode #1	200	50	1	2-GFSK	—	–109	—	dBm
Operating mode #2	400	150	0.5	2-GFSK	—	–105	—	dBm
Operating mode #3	400	200	0.5	2-GFSK	—	–104	—	dBm
Europe (Frequency: 863.1 MHz)								
Operating mode #1a	50	10	1	2-GFSK	—	–115	—	dBm
Operating mode #1b	100	20	1	2-GFSK	—	–112	—	dBm
Operating mode #1	100	50	0.5	2-GFSK	—	–109	—	dBm
Operating mode #2	200	100	0.5	2-GFSK	—	–106	—	dBm
Operating mode #3	200	150	0.5	2-GFSK	—	–104	—	dBm
Japan (Frequency: 920.6 MHz)								
Operating mode #1a	50	10	1	2-GFSK	—	–116	—	dBm
Operating mode #1b	100	20	1	2-GFSK	—	–113	—	dBm
Operating mode #1	200	50	1	2-GFSK	—	–109	—	dBm
Operating mode #2	400	100	1	2-GFSK	—	–105	—	dBm
Operating mode #3	600	200	1	2-GFSK	—	–102	—	dBm

Note: The listed values apply when the RF transceiver functions and pins are only in use.

Table 6.57 Adjacent Channel Rejection Ratio for SUN FSK

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 3.3 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
Packet length = 250 bytes, packet error rate (PER) = 10%, with no forward error correction (FEC), T_a = 25°C,
Desired wave input level: sensitivity specified in the standard*1 + 3 dB

Modulation Parameter	Channel Spacing [kHz]	Data Rate [kbps]	Modulation Index	Modulation Method	min (–1 ch/+1 ch)	typ (–1 ch/+1 ch)	max (–1 ch/+1 ch)	Unit
North America (Frequency: 920.6 MHz)								
Operating mode #1a	50	10	1	2-GFSK	—	47/47	—	dB
Operating mode #1b	100	20	1	2-GFSK	—	44/44	—	dB
Operating mode #1	200	50	1	2-GFSK	—	44/44	—	dB
Operating mode #2	400	150	0.5	2-GFSK	—	48/48	—	dB
Operating mode #3	400	200	0.5	2-GFSK	—	41/42	—	dB
Europe (Frequency: 863.1 MHz)								
Operating mode #1a	50	10	1	2-GFSK	—	45/45	—	dBm
Operating mode #1b	100	20	1	2-GFSK	—	42/42	—	dBm
Operating mode #1	100	50	0.5	2-GFSK	—	38/38	—	dBm
Operating mode #2	200	100	0.5	2-GFSK	—	41/40	—	dBm
Operating mode #3	200	150	0.5	2-GFSK	—	34/34	—	dBm
Japan (Frequency: 920.6 MHz)								
Operating mode #1a	50	10	1	2-GFSK	—	47/47	—	dBm
Operating mode #1b	100	20	1	2-GFSK	—	44/44	—	dBm
Operating mode #1	200	50	1	2-GFSK	—	44/45	—	dBm
Operating mode #2	400	100	1	2-GFSK	—	49/49	—	dBm
Operating mode #3	600	200	1	2-GFSK	—	48/49	—	dBm

Note: The listed values apply when the RF transceiver functions and pins are only in use.
Note 1. IEEE Std 802.15.4TM -2020: IEEE Standard for Low-Rate Wireless Networks

Table 6.58 Alternate Channel Rejection Ratio for SUN FSK

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 3.3 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
Packet length = 250 bytes, packet error rate (PER) = 10%, with no forward error correction (FEC), T_a = 25°C,
Desired wave input level: sensitivity specified in the standard*1 + 3 dB

Modulation Parameter	Channel Spacing [kHz]	Data Rate [kbps]	Modulation Index	Modulation Method	min (–2 ch/+2 ch)	typ (–2 ch/+2 ch)	max (–2 ch/+2 ch)	Unit
North America (Frequency: 920.6 MHz)								
Operating mode #1a	50	10	1	2-GFSK	—	48/48	—	dB
Operating mode #1b	100	20	1	2-GFSK	—	49/49	—	dB
Operating mode #1	200	50	1	2-GFSK	—	53/53	—	dB
Operating mode #2	400	150	0.5	2-GFSK	—	57/58	—	dB
Operating mode #3	400	200	0.5	2-GFSK	—	55/55	—	dB
Europe (Frequency: 863.1 MHz)								
Operating mode #1a	50	10	1	2-GFSK	—	45/45	—	dBm
Operating mode #1b	100	20	1	2-GFSK	—	45/46	—	dBm
Operating mode #1	100	50	0.5	2-GFSK	—	44/44	—	dBm
Operating mode #2	200	100	0.5	2-GFSK	—	51/51	—	dBm
Operating mode #3	200	150	0.5	2-GFSK	—	46/38	—	dBm
Japan (Frequency: 920.6 MHz)								
Operating mode #1a	50	10	1	2-GFSK	—	48/48	—	dBm
Operating mode #1b	100	20	1	2-GFSK	—	49/49	—	dBm
Operating mode #1	200	50	1	2-GFSK	—	53/53	—	dBm
Operating mode #2	400	100	1	2-GFSK	—	59/60	—	dBm
Operating mode #3	600	200	1	2-GFSK	—	47/58	—	dBm

Note: The listed values apply when the RF transceiver functions and pins are only in use.
Note 1. IEEE Std 802.15.4TM -2020: IEEE Standard for Low-Rate Wireless Networks

Table 6.59 Characteristics of the SUN-FSK Reception

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 3.3 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
Frequency = 920.6 MHz, 2-GFSK, 50 kbps, modulation index = 1.0, T_a = 25°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Maximum RF input voltage	—	—	10	dBm	Packet length = 250 bytes, Packet error rate (PER) = 10%
RSSI range	–108	—	–5	dBm	
RSSI resolution	—	1	—	dB	
RSSI precision	–5	—	5	dB	
Frequency deviation tolerance	–10	—	10	ppm	Sensitivity degradation: 1 dB
Modulation quality tolerance (fdev_error)	–20	—	20	%	Sensitivity degradation: 3 dB

Note: The listed values apply when the RF transceiver functions and pins are only in use.

Table 6.60 Reception Sensitivity for SUN OFDM

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 3.3 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
Frequency = 920.6 MHz, packet length = 250 bytes, packet error rate (PER) = 10%, T_a = 25°C, typical values

Modulation Parameter	Option 1	Option 2	Option 3	Option 4	Unit
MCS0 (BPSK 1/2 w/ 4xfreq.rep)	–113	–116	–118	–119	dBm
MCS1 (BPSK 1/2 w/ 2xfreq.rep)	–110	–114	–117	–118	dBm
MCS2 (QPSK 1/2 w/ 2xfreq.rep)	–107	–110	–114	–112	dBm
MCS3 (QPSK 1/2)	–104	–107	–111	–111	dBm
MCS4 (QPSK 3/4)	–102	–104	–108	–109	dBm
MCS5 (16QAM 1/2)	–99	–101	–105	–106	dBm
MCS6 (16QAM 3/4)	–95	–98	–101	–103	dBm

Note: The listed values apply when the RF transceiver functions and pins are only in use.

Table 6.61 Adjacent Channel Rejection Ratio for SUN OFDM

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 3.3 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
Frequency = 920.6 MHz, packet length = 250 bytes, packet error rate (PER) = 10%, T_a = 25°C, typical values,
Desired wave input level: sensitivity specified in the standard*1 + 3 dB

Parameter	Option 1	Option 2	Option 3	Option 4	Unit
	–1.2/+1.2 MHz	–0.8/+0.8 MHz	–0.4/+0.4 MHz	–0.2/+0.2 MHz	
MCS0 (BPSK 1/2 w/ 4xfreq.rep)	33/31	44/48	49/45	34/31	dB
MCS1 (BPSK 1/2 w/ 2xfreq.rep)	33/31	43/53	46/44	34/31	dB
MCS2 (QPSK 1/2 w/ 2xfreq.rep)	34/31	40/52	47/45	33/31	dB
MCS3 (QPSK 1/2)	33/31	37/49	42/45	33/31	dB
MCS4 (QPSK 3/4)	31/30	33/46	46/45	33/31	dB
MCS5 (16QAM 1/2)	28/28	31/44	44/42	32/31	dB
MCS6 (16QAM 3/4)	23/23	28/41	41/39	31/30	dB

Note: The listed values apply when the RF transceiver functions and pins are only in use.
Note 1. IEEE Std 802.15.4TM -2020: IEEE Standard for Low-Rate Wireless Networks

Table 6.62 Alternate Channel Rejection Ratio for SUN OFDM

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 3.3 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
Frequency = 920.6 MHz, packet length = 250 bytes, packet error rate (PER) = 10%, T_a = 25°C, typical values,
Desired wave input level: sensitivity specified in the standard*1 + 3 dB

Parameter	Option 1	Option 2	Option 3	Option 4	Unit
	–2.4/+2.4 MHz	–1.6/+1.6 MHz	–0.8/+0.8 MHz	–0.4/+0.4 MHz	
MCS0 (BPSK 1/2 w/ 4xfreq.rep)	50/48	54/58	60/63	49/49	dB
MCS1 (BPSK 1/2 w/ 2xfreq.rep)	47/46	52/62	60/63	50/50	dB
MCS2 (QPSK 1/2 w/ 2xfreq.rep)	54/55	54/58	59/59	48/48	dB
MCS3 (QPSK 1/2)	52/53	52/52	56/56	47/48	dB
MCS4 (QPSK 3/4)	47/51	51/51	53/53	47/48	dB
MCS5 (16QAM 1/2)	46/48	48/50	50/50	47/48	dB
MCS6 (16QAM 3/4)	42/44	45/47	47/47	46/46	dB

Note: The listed values apply when the RF transceiver functions and pins are only in use.
Note 1. IEEE Std 802.15.4TM -2020: IEEE Standard for Low-Rate Wireless Networks

Table 6.63 Co-channel Rejection Ratio for SUN OFDM

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 3.3 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
Frequency = 920.6 MHz, packet length = 250 bytes, packet error rate (PER) = 10%, T_a = 25°C, typical values,
Desired wave input level: sensitivity specified in the standard*1 + 3 dB

Parameter	Option 1	Option 2	Option 3	Option 4	Unit
	±0 kHz	±0 kHz	±0 kHz	±0 kHz	
MCS0 (BPSK 1/2 w/ 4xfreq.rep)	4	3	2	–1	dB
MCS1 (BPSK 1/2 w/ 2xfreq.rep)	2	2	1	–1	dB
MCS2 (QPSK 1/2 w/ 2xfreq.rep)	–2	–2	–3	–9	dB
MCS3 (QPSK 1/2)	–5	–5	–4	–7	dB
MCS4 (QPSK 3/4)	–7	–7	–7	–8	dB
MCS5 (16QAM 1/2)	–10	–12	–10	–11	dB
MCS6 (16QAM 3/4)	–13	–13	–13	–13	dB

Note: The listed values apply when the RF transceiver functions and pins are only in use.
Note 1. IEEE Std 802.15.4TM -2020: IEEE Standard for Low-Rate Wireless Networks

Table 6.64 Characteristics of the SUN-OFDM Reception

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 3.3 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V,
Frequency = 920.6 MHz, option 1, MCS6, T_a = 25°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Maximum RF input voltage	—	5	—	dBm	
RSSI range	–97	—	–5	dBm	
RSSI resolution	—	1	—	dB	
RSSI precision	–5	—	5	dB	
Frequency deviation tolerance	–20	—	20	ppm	Sensitivity degradation: 1 dB
Modulation quality tolerance (degradation of sensitivity)	—	2	—	%	Error vector magnitude (EVM): IEEE802.15.4-2020*1

Note: The listed values apply when the RF transceiver functions and pins are only in use.
Note 1. IEEE Std 802.15.4TM -2020: IEEE Standard for Low-Rate Wireless Networks

6.13.2 Characteristics of the Transceiver Transmission

Table 6.65 Characteristics of the SUN-FSK Transmission

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 3.3 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V, T_a = 25°C,
Frequency = 920.6 MHz

Item		Min.	Typ.	Max.	Unit	Test Conditions	
Maximum transmission output power		—	15	—	dBm	C.W.	
Minimum transmission output power		—	–15	—	dBm	C.W.	
Adjustable step size for transmission output power		—	1	—	dB	C.W.	
Deviation of the output power depending on the temperature		—	—	2	dB	T_a: –40°C to +80°C	
Harmonics	Second	—	–41.3	—	dBm	Output power level = +15 dBm	
	Third	—	–41.3	—			
	Fourth to seventh	—	–41.3	—			
Frequency deviation error		—	—	30	%	Output power level = +15 dBm	
Maximum zero crossing offset		–12.5	—	12.5	%	Output power level = +15 dBm	
Transmission frequency deviation		–20	—	20	ppm	Output power level = +15 dBm	
Adjacent channel leakage ratio		—	–49	—	dB	Output power level = +15 dBm	50 kbps, MI = 0.5
		—	–50	—			50 kbps, MI = 1.0
		—	–50	—			100 kbps, MI = 0.5
		—	–47	—			100 kbps, MI = 1.0

Note: The listed values apply when the RF transceiver functions and pins are only in use.

Table 6.66 Characteristics of the SUN-OFDM Transmission

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_DA = VCC_RF = VCC_A = VCC_DDC = VCC_D = V_{BATT} = 3.3 V,
2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS_DDC = 0 V, T_a = 25°C,
Frequency = 920.6 MHz, option 1

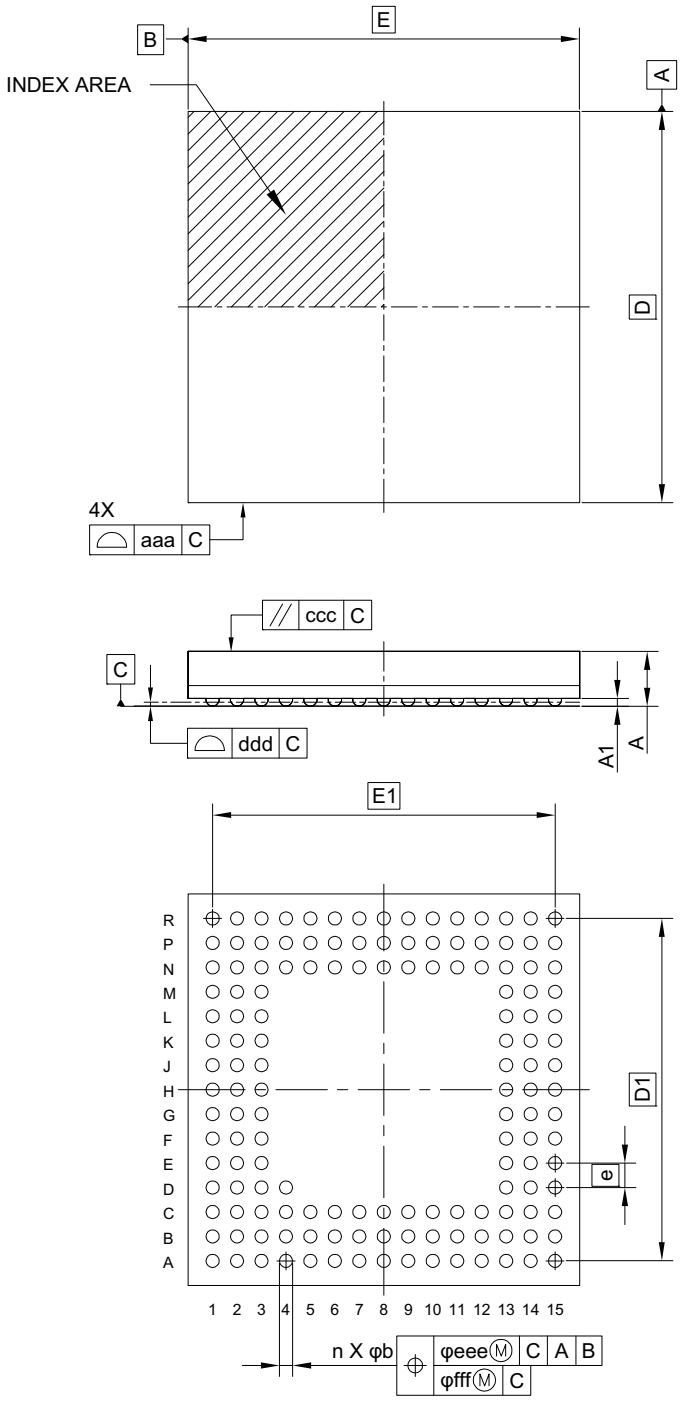
Item		Min.	Typ.	Max.	Unit	Test Conditions
Maximum transmission output power		—	11	—	dBm	BPSK, R = 1/2, (MCS0,1), EVM = –10 dB
		—	10	—		QPSK, R = 1/2, (MCS2,3), EVM = –13 dB
		—	10	—		QPSK, R = 3/4, (MCS4), EVM = –13 dB
		—	9	—		16QAM, R = 1/2, (MCS5), EVM = –19 dB
		—	9	—		16QAM, R = 3/4, (MCS6), EVM = –19 dB
Minimum transmission output power		—	–19	—	dBm	BPSK, R = 1/2, (MCS0,1), EVM = –10 dB
		—	–19	—		QPSK, R = 1/2, (MCS2,3), EVM = –13 dB
		—	–19	—		QPSK, R = 3/4, (MCS4), EVM = –13 dB
		—	–19	—		16QAM, R = 1/2, (MCS5), EVM = –19 dB
		—	–19	—		16QAM, R = 3/4, (MCS6), EVM = –19 dB
Adjustable step size for transmission output power		—	1	—	dB	
Deviation of the output power depending on the temperature		—	2	—	dB	T_a: –40°C to +80°C
Harmonics	Second	—	–41.3	—	dBm	The transmission output power is at its maximum.
	Third	—	–41.3	—		
	Fourth to seventh	—	–41.3	—		
Adjacent channel leakage ratio		—	–29	—	dB	BPSK, R = 1/2 (MCS0,1), +11 dBm output
		—	–31	—		QPSK, R = 1/2 (MCS2,3), +10 dBm output
		—	–31	—		QPSK, R = 3/4 (MCS4), +10 dBm output
		—	–33	—		16QAM, R = 1/2 (MCS5), +9 dBm output
		—	–33	—		16QAM, R = 3/4 (MCS6), +9 dBm output

Note: The listed values apply when the RF transceiver functions and pins are only in use.

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-TFBGA145-8x8-0.50	PTBG0145KB-A	0.15



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	8.00	—
E	—	8.00	—
D1	—	7.00	—
E1	—	7.00	—
A	—	—	1.19
A1	0.11	—	—
b	0.22	0.27	0.32
e	—	0.50	—
aaa	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.08
eee	—	—	0.15
fff	—	—	0.05
n	—	145	—

Figure A 145-Pin TFBGA (PTBG0145KB-A)

REVISION HISTORY	RX65W-A Group User's Manual: Hardware

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Sep 30, 2022	—	First edition, issued	
1.10	Apr 28, 2023	Appendix 1. Package Dimensions		
		159	Figure A 145-Pin TFBGA (PTBG0145KB-A), changed	

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