User's Manual

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RX65N Group, RX651 Group
Flash Memory

User's Manual: Hardware Interface

RENESAS 32-Bit MCU
RX Family / RX600 Series

Renesas Electronics
www.renesas.com

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Contents

1. Features

The features of the hardware interface of the flash memory are described below. Refer to the User's Manual: Hardware for differences in specifications between products with at least 1.5 Mbytes code flash memory and those with 1 Mbyte code flash memory or less, and for information on the capacity, block structure, and addresses of the flash memory in this MCU.

Programming/Erasure

A dedicated sequencer for the flash memory (flash sequencer) executes programming and erasure via internal peripheral bus 6. The flash sequencer also supports the suspension or resumption of programming or erasure, and background operation (BGO).

Security Functions

The flash memory incorporates hardware functions to prevent falsification or unauthorized reading of data in flash memory.

Protection Functions

The flash memory incorporates hardware functions to prevent erroneous rewriting.

Interrupts

The flash memory supports an interrupt to indicate completion of processing by the flash sequencer and an error interrupt to indicate operations that were in error.

2. Module Configuration

Modules related to the flash memory are configured as shown in Figure 2.1. The flash sequencer is configured of the Flash Control Unit (FCU) and Flash Application Command Interface (FACI). The FCU basically controls of overwriting of the flash memory. The FACI receives FACI commands via internal peripheral bus 6 and controls FCU operations accordingly.

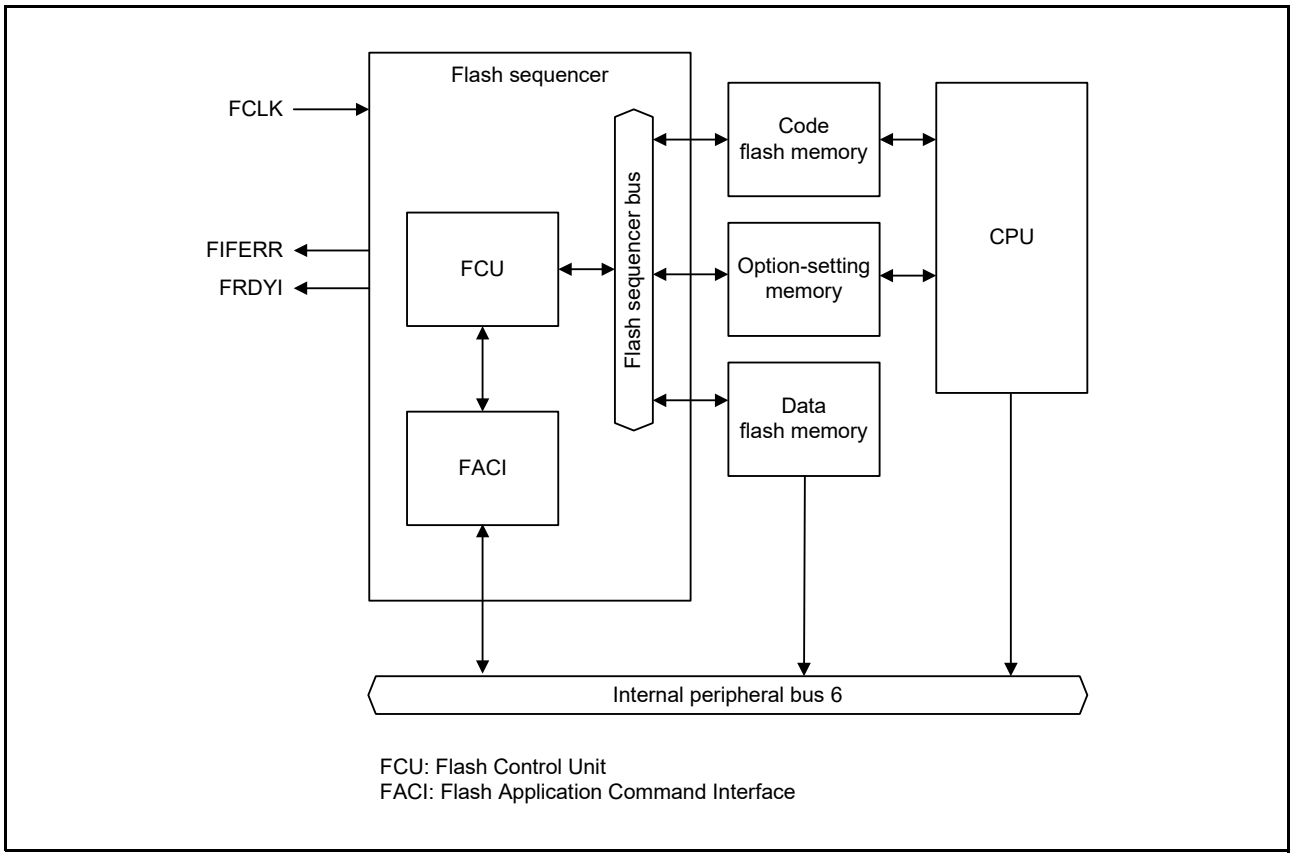


Figure 2.1 Configuration of Flash Memory-Related Modules

3. Address Space

Using the hardware interface with the flash memory requires accessing to the area containing registers of the hardware, that for the issuing of FACI commands. Table 3.1 summarizes information on all of these areas.

Table 3.1 Information on the Hardware Interface Area

Area	Address	Capacity
Area containing the various registers of the hardware	See section 4, Registers.	See section 4, Registers.
FACI command-issuing area	007E 0000h	4 bytes
Option-setting memory (configuration setting area)	FE7F 5D00h to FE7F 5D7Fh	128 bytes

Refer to the User's Manual: Hardware for information on the addresses of the flash memory.

4. Registers

This section contains information on registers to which access is required when using the hardware interface of the flash memory. Reset registers that are not specifically mentioned to their initial states.
For information on the option-setting memory, see the User's Manual: Hardware for the product you are using.

Table 4.1 List of Registers

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Page
						ICLK ≥ PCLKB/FCLK	ICLK < PCLKB/FCLK	
0008 C296h	FLASH	Flash P/E Protect Register	FWEPROR	8	8	4 to 5 PCLKB	2 to 3 ICLK	10
007F E010h	FLASH	Flash Access Status Register	FASTAT	8	8	2 to 4 FCLK	2 to 3 ICLK	11
007F E014h	FLASH	Flash Access Error Interrupt Enable Register	FAEINT	8	8	2 to 4 FCLK	2 to 3 ICLK	13
007F E018h	FLASH	Flash Ready Interrupt Enable Register	FRDYIE	8	8	2 to 4 FCLK	2 to 3 ICLK	14
007F E030h	FLASH	FACI Command Start Address Register	FSADDR	32	32	2 to 4 FCLK	2 to 3 ICLK	15
007F E034h	FLASH	FACI Command End Address Register*1	FEADDR	32	32	2 to 4 FCLK	2 to 3 ICLK	16
007F E080h	FLASH	Flash Status Register	FSTATR	32	32	2 to 4 FCLK	2 to 3 ICLK	17
007F E084h	FLASH	Flash P/E Mode Entry Register	FENTRYR	16	16	2 to 4 FCLK	2 to 3 ICLK	21
007F E08Ch	FLASH	Flash Sequencer Set-Up Initialization Register	FSUINITR	16	16	2 to 4 FCLK	2 to 3 ICLK	22
007F E0A0h	FLASH	FACI Command Register	FCMDR	16	16	2 to 4 FCLK	2 to 3 ICLK	23
007F E0D0h	FLASH	Data Flash Blank Check Control Register*1	FBCCNT	8	8	2 to 4 FCLK	2 to 3 ICLK	27
007F E0D4h	FLASH	Data Flash Blank Check Status Register*1	FBCSTAT	8	8	2 to 4 FCLK	2 to 3 ICLK	28
007F E0D8h	FLASH	Data Flash Programming Start Address Register*1	FPSADDR	32	32	2 to 4 FCLK	2 to 3 ICLK	28
007F E0DCh	FLASH	Flash Access Window Monitor Register	FAWMON	32	32	2 to 4 FCLK	2 to 3 ICLK	26
007F E0E0h	FLASH	Flash Sequencer Processing Switching Register	FCPSR	16	16	2 to 4 FCLK	2 to 3 ICLK	27
007F E0E4h	FLASH	Flash Sequencer Processing Clock Frequency Notification Register	FPCKAR	16	16	2 to 4 FCLK	2 to 3 ICLK	28
007F E0E8h	FLASH	Start-Up Area Control Register	FSUACR	16	16	2 to 4 FCLK	2 to 3 ICLK	29

Note 1. This register is only available for products with at least 1.5 Mbytes of code flash memory.

4.1 Flash P/E Protect Register (FWEPROR)

Address(es): 0008 C296h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	FLWE[1:0]	
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	FLWE[1:0]	Flash Programming and Erasure Enable	Products with at least 1.5 Mbytes of code flash memory: b1 b0 0 0: Programming/erasure and blank checking are disabled 0 1: Programming/erasure and blank checking are enabled 1 0: Programming/erasure and blank checking are disabled 1 1: Programming/erasure and blank checking are disabled Products with 1 Mbyte of code flash memory or less: b1 b0 0 0: Programming/erasure is disabled 0 1: Programming/erasure is enabled 1 0: Programming/erasure is disabled 1 1: Programming/erasure is disabled	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Programming/erasure of the flash memory and blank checking are enabled or disabled by hardware.
This register is initialized by a reset due to the signal on the RES# pin, a power-on reset, a voltage-monitoring 0 reset, an independent watchdog timer reset, a watchdog timer reset, a voltage-monitoring 1 reset, a voltage-monitoring 2 reset, and a software reset, and by transitions to deep software standby and software standby modes.

4.2 Flash Access Status Register (FASTAT)

Address(es): 007F E010h

	b7	b6	b5	b4	b3	b2	b1	b0
	CFAE	—	—	CMDLK	DFAE	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	DFAE	Data Flash Memory Access Violation Flag*2	0: No data flash memory access violation has occurred. 1: A data flash memory access violation has occurred.	R/W*1
b4	CMDLK	Command Lock Flag	0: The flash sequencer is not in the command-locked state. 1: The flash sequencer is in the command-locked state.	R
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	CFAE	Code Flash Memory Access Violation Flag	0: No code flash memory access violation has occurred. 1: A code flash memory access violation has occurred.	R/W*1

Note 1. Only 0 can be written to clear the flag after 1 is read.
Note 2. This bit is reserved for products with 1 Mbyte of code flash memory or less. This bit is read as 0. The write value should be 0.

This register indicates whether a code flash memory or data flash memory access violation has occurred. If either of the CFAE, and DFAE flags is 1, the CMDLK flag is set to 1 and the flash sequencer enters the command-locked state (see section 7.2, Error Protection). To release it from the command-locked state, a status clear command or forced stop command must be issued by the FACI.

DFAE Flag (Data Flash Memory Access Violation Flag)

This flag indicates whether a data flash memory access violation has occurred. If this flag is set to 1, the FSTATR.ILGLERR flag is set to 1, placing the flash sequencer in the command-locked state.
[Setting Condition]

- See Table 7.1, Error Protection Type

[Clearing Condition]

- When 0 is written after reading of 1
- When a status clear command or forced stop command is issued

CMDLK Flag (Command Lock Flag)

This flag indicates that the flash sequencer is in the command-locked state.
[Setting Condition]

- When the flash sequencer detects any of errors listed in Table 7.1, Error Protection Type and transitions to the command-locked state

[Clearing Condition]

- When the flash sequencer starting to process a status clear or forced stop command

CFAE Flag (Code Flash Memory Access Violation Flag)

This flag indicates whether a code flash memory access violation has occurred. If this flag is set to 1, the FSTATR.ILGLERR flag is set to 1, placing the flash sequencer in the command-locked state.
[Setting Conditions]

- See Table 7.1, Error Protection Type

[Clearing Condition]

- When 0 is written after reading of 1
- When a status clear command or forced stop command is issued

4.3 Flash Access Error Interrupt Enable Register (FAEINT)

Address(es): 007F E014h

	b7	b6	b5	b4	b3	b2	b1	b0
	CFAEIE	—	—	CMDLKIE	DFAEIE	—	—	—
Value after reset:	1	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	DFAEIE	Data Flash Memory Access Violation Interrupt Enable*1	0: Generation of an FIFERR interrupt request is disabled when FASTAT.DFAE is set to 1. 1: Generation of an FIFERR interrupt request is enabled when FASTAT.DFAE is set to 1.	R/W
b4	CMDLKIE	Command Lock Interrupt Enable	0: Generation of an FIFERR interrupt request is disabled when FASTAT.CMDLK is set to 1. 1: Generation of an FIFERR interrupt request is enabled when FASTAT.CMDLK is set to 1.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	CFAEIE	Code Flash Memory Access Violation Interrupt Enable	0: Generation of an FIFERR interrupt request is disabled when FASTAT.CFAE is set to 1. 1: Generation of an FIFERR interrupt request is enabled when FASTAT.CFAE is set to 1.	R/W

Note 1. This bit is reserved for products with 1 Mbyte of code flash memory or less. This bit is read as 1. The write value should be 1.

This register enables or disables generation of a flash access error (FIFERR) interrupt request.

DFAEIE Bit (Data Flash Memory Access Violation Interrupt Enable)

This bit enables or disables generation of an FIFERR interrupt request when a data flash memory access violation occurs and the FASTAT.DFAE flag is set to 1.

CMDLKIE Bit (Command Lock Interrupt Enable)

This bit enables or disables generation of an FIFERR interrupt request when the flash sequencer enters the command-locked state and the FASTAT.CMDLK flag is set to 1.

CFAEIE Bit (Code Flash Memory Access Violation Interrupt Enable)

This bit enables or disables generation of an FIFERR interrupt request when a code flash memory access violation occurs and the FASTAT.CFAE flag is set to 1.

4.4 Flash Ready Interrupt Enable Register (FRDYIE)

Address(es): 007F E018h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	FRDYIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FRDYIE	Flash Ready Interrupt Enable	0: Generation of an FRDY interrupt request is disabled. 1: Generation of an FRDY interrupt request is enabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This register enables or disables generation of a flash ready (FRDY) interrupt request.

FRDYIE Bit (Flash Ready Interrupt Enable)

This bit is used to enable or disable generation of an FRDY interrupt request when the FASTAT.FRDY flag is changed from 0 to 1 upon completion of processing by the flash sequencer of programming, erasure, and blank checking command.

4.5 FACI Command Start Address Register (FSADDR)

Address(es): 007F E030h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	FSADDR[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FSADDR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	FSADDR [31:0]	Start Address for FACI Command Processing	Start Address for FACI Command Processing	R/W*1

Note 1. Writing to these bits is possible only when the FSTATR.FRDY flag is 1. Writing to these bits while the FSTATR.FRDY flag = 0 is ignored. Note that b0 and b1 are read-only.

This register specifies the address where the target area for command processing starts when the FACI command for programming, block erasure, multi-block erasure, blank checking, or configuration setting is issued.
The FSADDR register is initialized when the FSUINITR.SUINIT bit is set to 1. It is also initialized by a reset.

FSADDR[31:0] Bits (Start Address for FACI Command Processing)

These bits specify the start address for FACI command processing. Bits 31 to 24 are ignored in FACI command processing for the code flash memory. Bits 31 to 17 are ignored in FACI command processing for the data flash memory. Bits 31 to 10 are ignored in processing of the FACI command for the option-setting memory. Bits that do not reach the address boundaries are also ignored. Table 4.2, Address Boundary for Each of the Commands shows the address boundary for each command.

Table 4.2 Address Boundary for Each of the Commands

Command	Address Boundary
Programming (code flash memory)	128-byte
Programming (data flash memory)	4-byte
Block erase (code flash memory)	8-Kbyte or 32-Kbyte
Block erase (data flash memory)	64-byte
Multi-block erase (data flash memory)	64-, 128-, or 256-byte
Blank check (data flash memory)	4-byte
Configuration setting	16-byte

Refer to the User's Manual: Hardware for the start addresses of the code flash memory area. See Table 6.6, Address Used by Configuration Set Command for the start address of the option-setting memory (configuration setting area).

4.6 FACI Command End Address Register (FEADDR)

Address(es): 007F E034h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	FEADDR[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FEADDR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	FEADDR [31:0]	End Address for FACI Command Processing	The end address for FACI command processing	R/W*1

Note 1. Writing to these bits is possible only when the FSTATR.FRDY flag is 1. Writing to these bits while the FSTATR.FRDY flag = 0 is ignored. Note that b0 and b1 are read-only.

This register is only available for products with at least 1.5 Mbytes of code flash memory.
This register is used to specify the end address of the area targeted for the multi-block erase command and blank checking command handling. When executing the multi-block erase command, the setting value of the register must be the setting of the FEADDR register or lower. If the setting value of the FSADDR register is larger than the FEADDR register setting value, the flash sequencer enters the command locked state.
When the FBCCNT.BCDIR bit is 0, the value of the FSADDR register must be that of this register or less. When the FBCCNT.BCDIR bit is 1, the value of the FSADDR register must be at least that of this register. If the settings of the FBCCNT.BCDIR bit and the FSADDR and FEADDR registers are inconsistent with the above rules, the flash sequencer enters the command-locked state (see section 7.2, Error Protection).
The FEADDR register is initialized when the FSUINITR.SUINIT bit is set to 1. It is also initialized by a reset.

FEADDR [31:0] Bits (End Address for FACI Command Processing)

These bits are used to specify the end address for handling of the multi-block erase command and blank checking command. In command processing, bits 31 to 17 and any bits that do not reach the address boundaries listed in Table 4.2, Address Boundary for Each of the Commands are ignored.
Refer to the User's Manual: Hardware for the end address of the data flash memory area.

4.7 Flash Status Register (FSTATR)

Address(es): 007F E080h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	ILGCOMERR	FESETERR	SECERR	OTERR	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FRDY	ILGLERR	ERSERR	PRGERR	SUSRDY	DBFULL	ERSSPD	PRGSPD	—	FLWEERR	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	FLWEERR	Flash Write/Erase Protect Error Flag	0: An error has not occurred. 1: An error has occurred.	R
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b8	PRGSPD	Programming Suspend Status Flag	0: The flash sequencer is in a state other than those corresponding to the value 1. 1: The flash sequencer is in the programming suspension processing state or the programming suspended state.	R
b9	ERSSPD	Erasure Suspend Status Flag	0: The flash sequencer is in a state other than those corresponding to the value 1. 1: The flash sequencer is in the erasure suspension processing state or the erasure-suspended state.	R
b10	DBFULL	Data Buffer Full Flag	0: The data buffer is empty. 1: The data buffer is full.	R
b11	SUSRDY	Suspend Ready Flag	0: The flash sequencer cannot receive P/E suspend commands. 1: The flash sequencer can receive P/E suspend commands.	R
b12	PRGERR	Programming Error Flag	0: Programming has been completed successfully. 1: An error has occurred during programming.	R
b13	ERSERR	Erasure Error Flag	0: Erasure has been completed successfully. 1: An error has occurred during erasure.	R
b14	ILGLERR	Illegal Error Flag	0: The flash sequencer has not detected an illegal FACI command or illegal flash memory access. 1: The flash sequencer has detected an illegal FACI command or illegal flash memory access.	R
b15	FRDY	Flash Ready Flag	0: Programming, block erase, multi-block erase, P/E suspend, P/E resume, forced stop, blank check, or configuration setting command processing is in progress. 1: None of the above is in progress.	R
b19 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b20	OTERR	Other Error Flag	0: An error has not occurred. 1: An error has occurred.	R
b21	SECERR	Security Error Flag	0: Write protection by the FAW.FSPR bit is not violated 1: Write protection by the FAW.FSPR bit is violated	R
b22	FESETERR	FENTRY Setting Error Flag	0: A setting error in the FENTRYR register has not been detected. 1: A setting error in the FENTRYR register has been detected.	R
b23	ILGCOMERR	Illegal Command Error Flag	0: The flash sequencer has not detected an illegal FACI command error. 1: The flash sequencer has detected an illegal FACI command error.	R

Bit	Symbol	Bit Name	Description	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This register indicates the state of the flash sequencer.

FLWEERR Flag (Flash Write/Erase Protect Error Flag)

This flag indicates a violation of the flash memory overwrite protection setting in the FWEPROR register. When this flag is 1, the flash sequencer is in the command-locked state.

[Setting Condition]

- See Table 7.1, Error Protection Type

[Clearing Condition]

- When the flash sequencer starts processing of a forced stop command

PRGSPD Flag (Programming Suspend Status Flag)

This flag indicates that the flash sequencer is in the processing of suspension of programming or has transitioned to the programming suspended state.

[Setting Condition]

- When the flash sequencer starts processing in response to a programming suspend command

[Clearing Conditions]

- When the flash sequencer has received a P/E resume command
  (after write access to the FACI command-issuing area is completed)
- When the flash sequencer starts processing of a forced stop command

ERSSPD Flag (Erasure Suspend Status Flag)

This flag indicates that the flash sequencer is the processing of erasure suspension or has transitioned to the erasure suspended state.

[Setting Condition]

- When the flash sequencer starts processing in response to an erasure suspend command

[Clearing Conditions]

- Reception of the P/E resume command by the flash sequencer
  (after write access to the FACI command-issuing area is completed)
- When the flash sequencer starts processing of a forced stop command

DBFULL Flag (Data Buffer Full Flag)

This flag indicates the state of the data buffer when a programming command or configuration setting command is issued. The FACI incorporates a buffer for write data (data buffer). When data for writing to the flash memory are issued to the FACI command-issuing area while the data buffer is full, the FACI inserts a wait cycle in the peripheral bus 6.

[Setting Condition]

- When the data buffer becomes full while a programming command or configuration setting command is being issued

[Clearing Condition]

- When the data buffer becomes empty

SUSRDY Flag (Suspend Ready Flag)

This flag indicates whether the flash sequencer can receive a P/E suspend command.

[Setting Condition]

- After starting programming/erasure processing and when the flash sequencer enters a state in which P/E suspend

commands can be received

[Clearing Conditions]

- When the flash sequencer has accepted the P/E suspend command or forced stop command (after write access to the FACI command-issuing area is completed)
- When the flash sequencer enters the command-locked state during programming or erasure
- When programming or erasure has been completed

PRGERR Flag (Programming Error Flag)

This flag indicates the result of programming of the flash memory. If this flag is 1, the flash sequencer is in the command-locked state.

[Setting Condition]

- See Table 7.1, Error Protection Type

[Clearing Condition]

- When the flash sequencer starts processing of a status clear or forced stop command

ERSERR Flag (Erasure Error Flag)

This flag indicates the result of erasure of the flash memory. If this flag is 1, the flash sequencer is in the command-locked state.

[Setting Condition]

- See Table 7.1, Error Protection Type

[Clearing Condition]

- When the flash sequencer starts processing of a status clear or forced stop command

ILGLERR Flag (Illegal Error Flag)

This flag indicates that the flash sequencer has detected an illegal FACI command or flash memory access. When this flag is 1, the flash sequencer is in the command-locked state.

[Setting Condition]

- See Table 7.1, Error Protection Type

[Clearing Condition]

- When the flash sequencer starts processing of a status clear or forced stop command.

FRDY Flag (Flash Ready Flag)

This flag indicates the command processing state of the flash sequencer.

[Setting Conditions]

- When the flash sequencer completes command processing
- When the flash sequencer receives a P/E suspend command and suspends programming or erasure of the flash memory
- When the flash sequencer has received a forced stop command and ended command processing

[Clearing Conditions]

- When the flash sequencer receives the FACI command of the setting of the program and configuration and after the first write access is made to the FACI command-issuing area
- When the flash sequencer receives any FACI command other than of the setting of the program and configuration and after the last write access is made to the FACI command issuing area

OTERR Flag (Other Error Flag)

This flag indicates that an FACI command has been issued when the condition of accepting commands is not satisfied. The OTERR flag is 1, the flash sequencer is in the command-locked state.

[Setting Condition]

- See Table 7.1, Error Protection Type

[Clearing Condition]

- When the flash sequencer starts processing of a status clear or forced stop command

SECERR Flag (Security Error Flag)

This flag indicates that write protection by the FAW.FSPR bit is violated. When the SECERR flag is 1, the flash sequencer is in the command-locked state.

[Setting Condition]

- See Table 7.1, Error Protection Type

[Clearing Condition]

- When the flash sequencer starts processing of a status clear or forced stop command

FESETERR Flag (FENTRY Setting Error Flag)

This flag indicates that a value of AA81h is written in the FENTRYR register or the value in the FENTRYR register differs when P/E is suspended and resumed. When the FESETERR flag is 1, the flash sequencer is in the command-locked state.

[Setting Condition]

- See Table 7.1, Error Protection Type

[Clearing Condition]

- When the flash sequencer starts processing of a status clear or forced stop command

ILGCOMERR Flag (Illegal Command Error Flag)

This flag indicates that the flash sequencer has detected an illegal FACI command. When the ILGCOMERR flag is 1, the flash sequencer is in the command-locked state.

[Setting Condition]

- See Table 7.1, Error Protection Type

[Clearing Condition]

- When the flash sequencer starts processing of a status clear or forced stop command

4.8 Flash P/E Mode Entry Register (FENTRYR)

Address(es): 007F E084h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								FENTRYD	—	—	—	—	—	—	FENTRYC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FENTRYC	Code Flash Memory P/E Mode Entry	0: Code flash memory is in read mode. 1: Code flash memory is in P/E mode.	R/W*1, *2
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	FENTRYD	Data Flash Memory P/E Mode Entry*4	0: Data flash memory is in read mode. 1: Data flash memory is in P/E mode.	R/W*1, *2
b15 to b8	KEY[7:0]	Key Code	Key code	R/W*3

Note 1. Writing to these bits is possible only when the FSTATR.FRDY flag is 1. Writing to these bits while the FSTATR.FRDY flag = 0 is ignored.
Note 2. Writing to this bit is possible only when AAh is written to the KEY bits in 16-bit units.
Note 3. Written values are not retained by these bits. These bits are read as 0.
Note 4. This bit is reserved for products with 1 Mbyte of code flash memory or less. This bit is read as 0. The write value should be 0.

This register is used to specify code flash memory P/E mode and data flash memory P/E mode. To specify code flash memory P/E mode or data flash memory P/E mode so that the flash sequencer can receive FACI commands, set either the FENTRYD or FENTRYC bit to 1 to place the flash sequencer in P/E mode.
Note that writing AA81h in this register causes the FSTATR.ILGLERR and FSTATR.FESETERR flags to be set to 1, and the flash sequencer to enter the command-locked state.
The FENTRYR register is initialized when the FSUINITR.SUINIT bit is set to 1. It is also initialized by a reset.

FENTRYC Bit (Code Flash Memory P/E Mode Entry)

This bit specifies the P/E mode for code flash memory.
[Setting Condition]

- When 1 is written to the FENTRYC bit while writing to the FENTRYR register is enabled and the FENTRYR register is 0000h

[Clearing Conditions]

- When the FENTRYR register is accessed in 8-bit units while the FSTATR.FRDY flag is 1
- When a value other than AAh is specified in the KEY bits and the FENTRYR register is accessed in 16-bit units while the FSTATR.FRDY flag is 1
- When 0 is written to the FENTRYC bit while writing to the FENTRYR register is enabled
- When the FENTRYR register is written while writing to the FENTRYR register is enabled and the value of the FENTRYR register is other than 0000h

FENTRYD Bit (Data Flash Memory P/E Mode Entry)

This bit specifies the P/E mode for data flash memory.
[Setting Condition]

- When 1 is written to the FENTRYR.FENTRYD bit while writing to the FENTRYR register is enabled and the FENTRYR register is 0000h

[Clearing Conditions]

- When the FENTRYR register is written in 8-bit units while the FSTATR.FRDY flag is 1
- When a value other than AAh is specified for the KEY bits while the FSTATR.FRDY flag is 1, and the FENTRYR

register is written in 16-bit units

- When 0 is written to the FENTRYD bit while writing to the FENTRYR register is enabled
- When the FENTRYR register is written while writing to FENTRYR register is enabled and the value of the FENTRYR register is other than 0000h

KEY[7:0] Bits (Key Code)

These bits control permission and prohibition of writing to the FENTRYD and FENTRYC bits.

4.9 Flash Sequencer Set-Up Initialization Register (FSUINITR)

Address(es): 007F E08Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	—	SUINIT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SUINIT	Set-Up Initialization	0: The FEADDR, FCPSR, FSADDR, FENTRYR, and FBCCNT flash sequencer set-up registers keep their current values. 1: The FEADDR, FCPSR, FSADDR, FENTRYR, and FBCCNT flash sequencer set-up registers are initialized.	R/W*1, *2
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	Key code	R/W*3

Note 1. Writing to these bits is possible only when the FSTATR.FRDY flag is 1. Writing to these bits while the FSTATR.FRDY flag = 0 is ignored.
Note 2. Writing to these bits is possible only when 2Dh is written to the KEY bits in 16-bit units.
Note 3. Written values are not retained by these bits. This bit is read as 0.

This register is used for initialization of the flash sequencer set-up.

SUINIT Bit (Set-Up Initialization)

This bit initializes the following flash sequencer set-up registers.

- FEADDR
- FCPSR
- FSADDR
- FENTRYR
- FBCCNT

KEY[7:0] Bits (Key Code)

These bits control permission and prohibition of writing to the SUINIT bit.

4.10 FACI Command Register (FCMDR)

Address(es): 007F E0A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CMDR[7:0]								PCMDR[7:0]							
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	PCMDR[7:0]	Precommand Flag	The command immediately before the latest command is stored.	R
b15 to b8	CMDR[7:0]	Command Flag	The latest command is stored.	R

This register records the two most recent commands accepted by the FACI.

PCMDR[7:0] Flags (Precommand Flag)

These flags indicate the command received immediately before the last command received by the FACI.

CMDR[7:0] Flags (Command Flag)

These flags indicate the latest command received by the FACI.

Table 4.3 States of FCMDR after Receiving Commands

Command	CMDR	PCMDR
Programming	E8h	Previous command
Block erase	D0h	20h
Multi-block erase*1	D0h	21h
P/E suspend	B0h	Previous command
P/E resume	D0h	Previous command
Status clear	50h	Previous command
Forced stop	B3h	Previous command
Blank check*1	D0h	71h
Configuration setting	40h	Previous command

Note 1. This command is only available for products with at least 1.5 Mbytes of code flash memory.

4.11 Data Flash Blank Check Control Register (FBCCNT)

Address(es): 007F E0D0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	BCDIR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	BCDIR	Blank Check Direction	0: Blank checking is executed from lower addresses to higher addresses (incremental mode). 1: Blank checking is executed from higher addresses to lower addresses (decremental mode).	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This register is only available for products with at least 1.5 Mbytes of code flash memory.
This register specifies the addressing mode in processing of a blank check command. The register is initialized when the FSUINITR.SUINIT bit is set to 1. It is also initialized by a reset.

BCDIR Bit (Blank Check Direction)

This bit specifies the addressing mode for blank checking.

4.12 Data Flash Blank Check Status Register (FBCSTAT)

Address(es): 007F E0D4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	BCST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	BCST	Blank Check Status Flag	0: The target area is in the non-programmed state (i.e. is blank; the area has been erased but has not yet been re-programmed). 1: The target area has been programmed with 0s or 1s.	R
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This register is only available for products with at least 1.5 Mbytes of code flash memory.
This register stores the results of checking in response to a blank check command.

BCST Flag (Blank Check Status Flag)

This flag indicates the results of checking in response to a blank check command.
[Setting condition]

- When the blank checking command is issued and data of 0 or 1 is written to the target area

[Clearing condition]

- When the blank checking command is executed and the target area is blank

4.13 Data Flash Programming Start Address Register (FPSADDR)

Address(es): 007F E0D8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PSADR[16]
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PSADR[15:0]															
Value after reset:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b16 to b0	PSADR[16:0]	Programmed Area Start Address	The starting address of the programmed area to be found firstly	R
b31 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This register is only available for products with at least 1.5 Mbytes of code flash memory.
This register indicates the starting address of the programmed area to be found firstly in processing of a blank check command.

PSADR[16:0] Bits (Programmed Area Start Address)

These bits indicate the starting address of the programmed area to be found firstly in processing of a blank check command. The offset value is stored from the first address of the data flash memory. The value of the bits is valid only while the FBCSTAT.BCST bit is 1.

4.14 Flash Access Window Monitor Register (FAWMON)

Address(es): 007F E0DCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BTFLG	—	—	—	FAWE[11:0]											
Value after reset:	The value set by the user*1															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FSPR	—	—	—	FAWS[11:0]											
Value after reset:	The value set by the user*1															

Bit	Symbol	Bit Name	Description	R/W
b11 to b0	FAWS[11:0]	Flash Access Window Start Address	Flash access window start address	R
b14 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	FSPR	Access Window Protection Flag	0: With protection (P/E disabled) 1: Without protection (P/E enabled)	R
b27 to b16	FAWE[11:0]	Flash Access Window End Address	Flash access window end address	R
b30 to b28	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31	BTFLG	Start-Up Area Select Flag*2	0: Startup area 0 is in the range from FFFF C000h to FFFF DFFFh, startup area 1 is in the range from FFFF E000h to FFFF FFFFh. 1: Startup area 1 is in the range from FFFF C000h to FFFF DFFFh, startup area 0 is in the range from FFFF E000h to FFFF FFFFh.	R

Note 1. For products in which the option-setting memory has not been specifically set, the value is FFFF FFFFh. The value will be set by the user.

Note 2. When the FSUACR.SAS[1:0] bits are changed to 1xb, the startup area is dependent on the setting of the FSUACR.SAS[1:0] bits regardless of the setting of this bit.

This register indicates the values of the write protection flag and start-up area select flag for setting the flash access window start/end address, and the access window. When a reset or configuration setting command is executed, the FACI transfers data from the option-setting memory to this register and the setting of the option-setting memory is enabled.

FAWS[11:0] Bits (Flash Access Window Start Address)

These bits are used to verify the access window start address setting value.

FSPR Flag (Access Window Protection Flag)

This flag indicates whether or not protection for a configuration setting command for the access window setting, for a configuration clear command, or for writing to the FSUACR register is available.

FAWE[11:0] Bits (Flash Access Window End Address)

These bits are used to verify the access window end address setting value. The value of these bits indicates the first address of the next P/E-enabled block as configured in the access window.

BTFLG Flag (Start-Up Area Select Flag)

This flag indicates whether the start-up area is switched by using start-up program protection.

4.15 Flash Sequencer Processing Switching Register (FCPSR)

Address(es): 007F E0E0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ESUSPMD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ESUSPMD	Erasure Suspend Mode	0: Suspension priority mode 1: Erasure priority mode	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This register is for selecting the erasure suspension mode.
The register is initialized when the FSUINITR.SUINIT bit is set to 1. It is also initialized by a reset.

ESUSPMD Bit (Erasure Suspend Mode)

This bit is for selecting the erasure suspension mode when a P/E suspend command is issued while the flash sequencer is executing erasure processing (see section 6.3.9, P/E Suspend Command). This bit should be set before issuing a block erase command.

4.16 Flash Sequencer Processing Clock Frequency Notification Register (FPCKAR)

Address(es): 007F E0E4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								PCKA[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	PCKA[7:0]	Flash Sequencer Processing Clock Frequency Notification	These bits are used to set the frequency of the FlashIF clock (FCLK) and notify the flash sequencer of the frequency used	R/W*1, *2
b15 to b8	KEY[7:0]	Key Code	Key code	R/W*3

Note 1. Writing to these bits is possible only when the FSTATR.FRDY flag is 1. Writing to these bits while the FSTATR.FRDY flag = 0 is ignored.
Note 2. Writing to these bits is possible only when 1Eh is written to the KEY[7:0] bits in 16-bit units.
Note 3. Written values are not retained by these bits. These bits are read as 0.

This register specifies the frequency of the FlashIF clock (FCLK) generated in the clock generator and notifies the flash sequencer of the frequency used. The flash sequencer determines the FACI command processing time based on the frequency notified by the FPCKAR register. The initial value is set to the maximum operating frequency of the FCLK.

PCKA[7:0] Bits (Flash Sequencer Processing Clock Frequency Notification)

These bits are used to specify the frequency of the FCLK generated in the clock generator and to notify the flash sequencer of the frequency used. Set the desired frequency in these bits before issuing an FACI command. Specifically, convert the frequency represented in MHz into a binary number and set it in these bits.

Example: When frequency is 35.9 MHz (PCKA[7:0] = 24h)
Round up the first decimal place of 35.9 MHz to a whole number (= 36) and convert it into a binary number.

If the value set in these bits is smaller than the frequency of the FCLK, the rewriting characteristics of the flash memory cannot be guaranteed. Conversely, if the value set in these bits is greater than the frequency of the FCLK, the rewriting characteristics of the flash memory can be guaranteed although the FACI command processing time such as time for rewriting will increase (the FACI command processing time becomes the shortest when the frequency of the FCLK is the same as the value set in the bits).

KEY[7:0] Bits (Key Code)

These bits control permission and prohibition of writing to the PCKA[7:0] bits.

4.17 Start-Up Area Control Register (FSUACR)

Address(es): 007F E0E8h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	SAS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	SAS[1:0]	Start-Up Area Select	b1 b0 0 x: A start-up area is selected based on the setting of the FAW.BTFLG bit. 1 0: The area from FFFF E000h to FFFF FFFFh is selected as the address range for startup area 0, and the area from FFFF C000h to FFFF DFFFh is selected as the address range for startup area 1, regardless of the setting of the FAW.BTFLG bit. 1 1: The area from FFFF E000h to FFFF FFFFh is selected as the address range for startup area 1, and the area from FFFF C000h to FFFF DFFFh is selected as the address range for startup area 0, regardless of the setting of the FAW.BTFLG bit.	R/W*1, *2
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	Key codes	R/W*3

x: Don't care
Note 1. Writable only when the FAW.FSPR bit is 1. When the FAW.FSPR bit is 0, writing to these bits are ignored.
Note 2. Writing to these bits is possible only when 66h is written to the KEY bit in 16-bit units.
Note 3. Written values are not retained by these bits. These bits are read as 0.

This register is used to switch startup areas 0 and 1 by startup program protection.
Do not use this register in dual mode (the MDE.BANKMD[2:0] bits are 000b). In dual mode, starting up proceeds from startup area 0.

SAS[1:0]Bits (Start-Up Area Select)

These bits are used to switch startup areas 0 and 1.

KEY[7:0] Bits (Key Code)

These bits enables or disable overwriting to the SAS[1:0] bits.

5. Operating Modes of the Flash Sequencer

The flash sequencer has three operating modes as shown in Figure 5.1. Transitions between modes are initiated by changing the value of the FENTRYR register.

When the value of the FENTRYR register is 0000h, the flash sequencer is in read mode. In this mode, it does not receive FACI commands. The code flash memory and data flash memory are readable.

When the value of the FENTRYR register is 0001h, the flash sequencer is in code flash memory P/E mode where the code flash memory can be programmed or erased by FACI commands. In this mode, reading from the code flash memory is disabled under the conditions where BGO cannot be used. Under the conditions where BGO can be used, reading from the code flash memory is enabled.

When the value of the FENTRYR register is 0080h, the flash sequencer is in data flash memory P/E mode where the data flash memory can be programmed or erased by FACI commands. In this mode, the data flash memory is not readable. However, the code flash memory is readable.

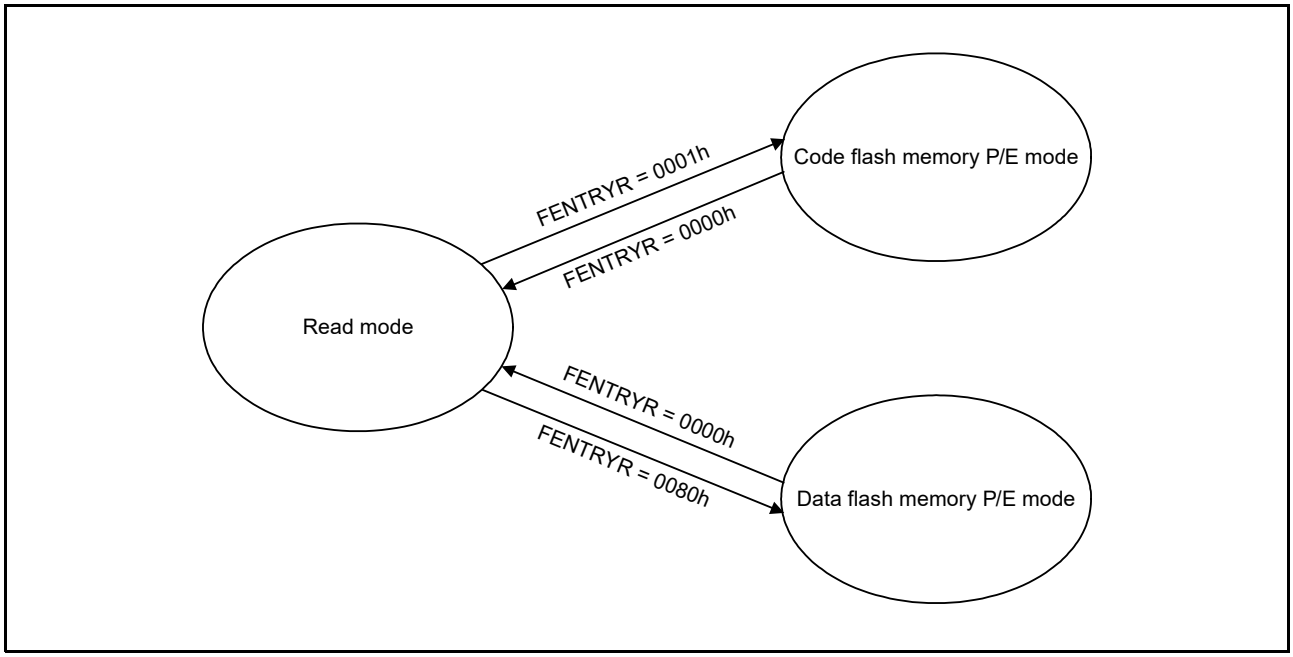


Figure 5.1 Modes of the Flash Sequencer

6. FACI Commands

6.1 List of FACI Commands

Table 6.1 List of FACI Commands

FACI Command	Description
Programming	This is used to program the code or data flash memory. Units of programming are 128 bytes for the code flash memory and 4 bytes for the data flash memory.
Block erase	This is used to erase the code or data flash memory. The unit of erasure is one block. (code flash memory: 8 K or 32 Kbytes, data flash memory: 64 bytes)
Multi-block erase	This is used to erase the data flash memory. The unit of erasure is 64, 128, 256 bytes
P/E suspend	This suspends programming or erasure processing.
P/E resume	This resumes suspended programming or erasure processing.
Status clear	This initializes the ILGLERR, ERSERR, PRGERR, ILGCOMERR, FESETERR, SECERR, and OTERR flags in the FSTATR register and the CMDLK, CFAE, and DFAE flags in the FASTAT releases the flash sequencer from the command-locked state.
Forced stop	This forcibly stops processing of FACI commands and initializes the FASTAT and FSTATR registers.
Blank check	This is used to blank-check the data flash memory. Units of blank checking: 4 bytes to 64 Kbytes (specified in 4-byte units).
Configuration setting	This is used to set the option-setting memory (configuration setting area). Units of setting: 16 bytes.

Refer to the User's Manual: Hardware for the option-setting memory.
The FACI commands are issued by writing to the FACI command-issuing area (see Table 3.1). When write access as shown in Table 6.2 proceeds in the specified state, the flash sequencer executes the processing corresponding to the given command (see section 6.2, Relationship between the Flash Sequencer State and FACI Commands).

Table 6.2 FACI Command Formats

FACI Commands	Number of Write Access	Data to be Written to the FACI Command-Issuing Area			
		1st Access	2nd Access	3rd to (N+2)th Access	(N+3)th Access
Programming (code flash memory) 128-byte programming, N = 64	67	E8h	40h (= N)	WD_1 to WD_{64}	D0h
Programming (data flash memory) 4-byte programming, N = 2	5	E8h	02h (= N)	WD_1 to WD_2	D0h
Block erase (code flash memory)	2	20h	D0h	—	—
Block erase (data flash memory 64-byte)	2	20h	D0h	—	—
Multi-block erase (data flash memory 64-byte/128-byte/256-byte)	2	21h	D0h	—	—
P/E suspend	1	B0h	—	—	—
P/E resume	1	D0h	—	—	—
Status clear	1	50h	—	—	—
Forced stop	1	B3h	—	—	—
Blank check	2	71h	D0h	—	—
Configuration setting N = 8	11	40h	08h (= N)	WD_1 to WD_8	D0h

Note: WD_N (N = 1, 2,…): Nth 16-bit data to be programmed.

The flash sequencer clears the FSTATR.FRDY flag to 0 at the start of processing of a command other than the status clear command and sets this bit to 1 upon completion of command processing.
When the setting of the FRDYIE.FRDYIE bit is 1 and when the FSTATR.FRDY flag is set to 1, a flash ready (FRDY) interrupt is generated.

6.2 Relationship between the Flash Sequencer State and FACI Commands

Each FACI command can be accepted in a specific mode or state of the flash sequencer. FACI commands should be issued after the transition of the flash sequencer to the code flash memory P/E mode or data flash memory P/E mode and checking of the state of the flash sequencer. Use the FSTATR and FASTAT registers to check the state of the flash sequencer. The value of the FASTAT.CMDLK flag is the logical OR of values of the ILGLERR, ILGCOMERR, FESETERR, SECERR, OTERR, ERSERR, PRGERR, and FLWEERR flags in the FSTATR register. Therefore, the occurrence of errors can be checked by reading the value of the FASTAT.CMDLK flag.

Table 6.3 lists the available commands in each operating mode.

Table 6.3 Operating Mode and Available Commands

Operating Mode	FENTRYR Register Value	Available Commands
Read mode	0000h	None
Code flash memory P/E mode	0001h	Programming Block erase P/E suspend P/E resume Status clear Forced stop Configuration setting
Data flash memory P/E mode	0080h	Programming Block erase Multi-block erase P/E suspend P/E resume Status clear Forced stop Blank check

Table 6.4 shows the state of the flash sequencer and acceptable FACI commands. An appropriate mode is assumed to be set before the commands are executed.

Table 6.4 Acceptable FACI Commands and the State of the Flash Sequencer

	Processing of Programming or Erasure	Processing of Configuration Setting	Processing to Suspend Programming or Erasure	Processing of Blank Checking	Programming Suspended	Erasure Suspended	Programming while Erasure is Suspended	Command-Locked State (FRDY = 1)	Command-Locked State (FRDY = 0)	Processing of Forced Stop Command	Other State
FRDY flag	0	0	0	0	1	1	0	1	0	0	1
SUSRDY flag	1	0	0	0	0	0	0	0	0	0	0
ERSSPD flag	0	0	0/1	0/1	0	1	1	0/1	0/1	0	0
PRGSPD flag	0	0	0/1	0/1	1	0	0	0/1	0/1	0	0
CMDLK flag	0	0	0	0	0	0	0	1	1	0	0
Programming	×	× *4	×	×	×	✓ *3	×	×	×	×	✓
Block erase	×	× *4	×	×	×	×	×	×	×	×	✓
Multi-block erase	×	× *4	×	×	×	×	×	×	×	×	✓
P/E suspend	✓	× *4	×	×	×	×	×	—	×	×	—
P/E resume	×	× *4	×	×	✓	✓	×	×	×	×	×
Status clear	×	× *4	×	×	✓	✓	×	✓	×	×	✓
Forced stop	✓	✓ *4	✓	✓	✓	✓	✓	✓	✓	✓	✓
Blank check	×	×	×	×	✓ *1	✓ *1	×	×	×	×	✓ *1
Configuration setting	×	× *4	×	×	×	×	×	×	×	×	✓ *2

✓: Acceptable
×: Not acceptable (the sequencer in the command-locked state)
—: Ignored
Note 1. Acceptable only in data flash memory P/E mode
Note 2. Acceptable only in code flash memory P/E mode
Note 3. Programming is acceptable only for blocks other than blocks where erasure has been suspended.
Note 4. Do not issue a FACI command when configuration setting is being processed and the FSTATR.DBFULL bit is 1.

6.3 Usage of FACI Commands

This section gives an overview of the usage of FACI commands.

6.3.1 Transition to Code Flash Memory P/E Mode

To use the FACI commands for the code flash memory, a transition to code flash memory P/E mode is required. To cause shift to code flash memory P/E mode, set the FENTRYR.FENTRYC bit to 1.

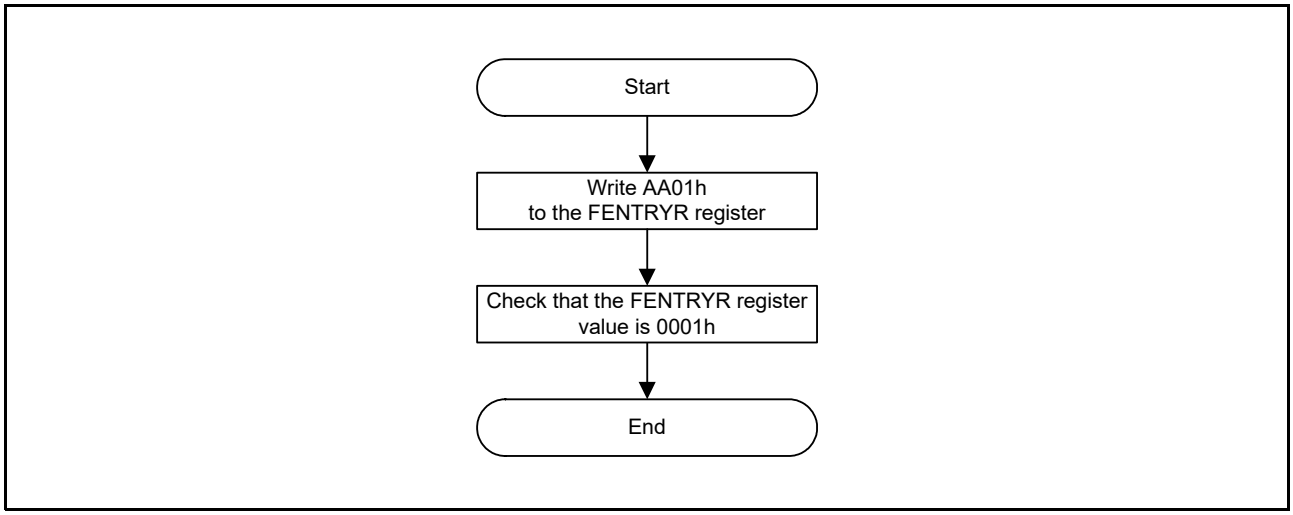


Figure 6.1 Procedure for Transition to Code Flash Memory P/E Mode

6.3.2 Transition to Data Flash Memory P/E Mode

To use the FACI commands for the data flash memory, a transition to data flash memory P/E mode is required. To shift to data flash memory P/E mode, set the FENTRYR.FENTRYRD bit to 1.

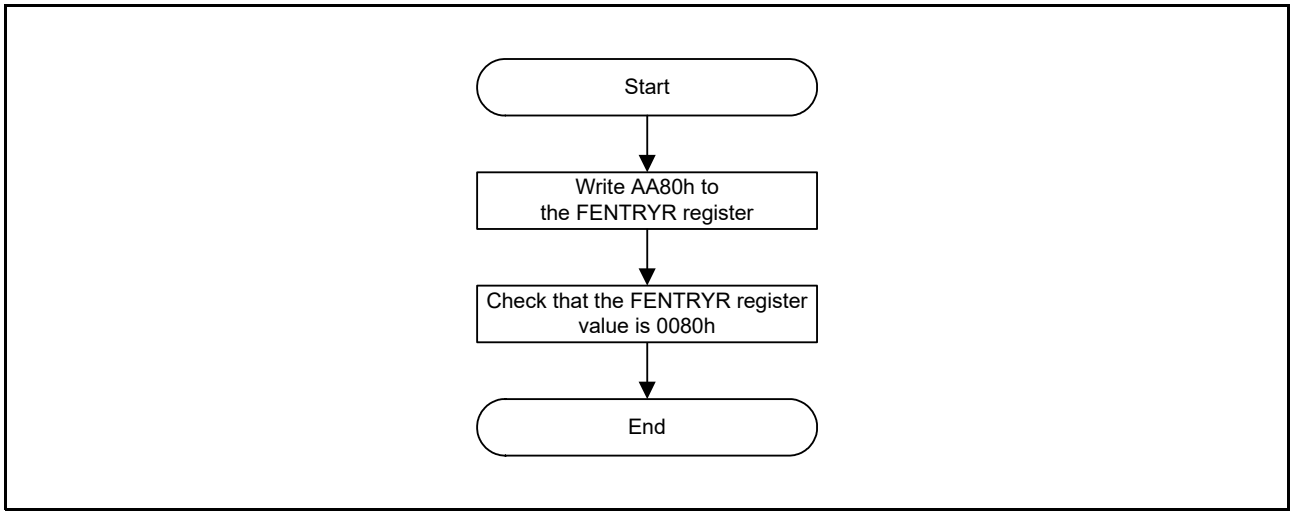
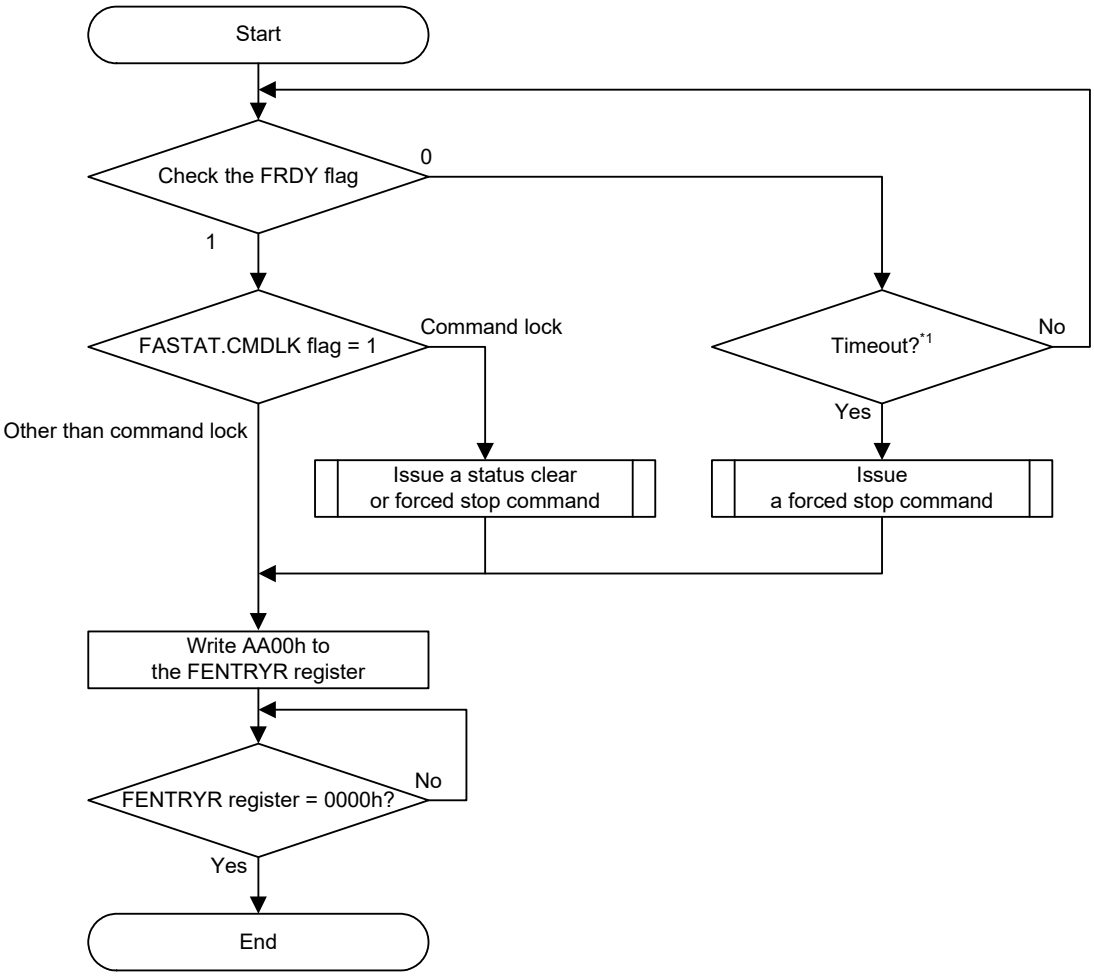


Figure 6.2 Procedure for Transition to Data Flash Memory P/E Mode

6.3.3 Transition to Read Mode

To read the flash memory without using the BGO function, a transition to read mode is required. To shift to read mode, set the FENTRYR register to 0000h. The transition to read mode should be made after processing by the flash sequencer is completed and while operation is in other than in the command-locked state. In addition, operation is started in read mode after release from the reset state.



Note 1. Judgment of the timeout is based on 1.1 times the maximum time for processing of the FACI command that is in progress (refer to the Electrical Characteristics chapter in the User's Manual: Hardware).

Figure 6.3 Procedure for Transition to Read Mode

6.3.4 Overview Flow when FACI Command is Used

Figure 6.4 shows an overview flow when the FACI command is used.
If BGO is enabled, the jump to the internal RAM or external area (other than code flash memory) is not required because an FACI command can be issued for the code or data flash memory by using the rewriting program in the code flash memory.
When the FCLK is changed, changing the FPCKAR register shortens time for processing the FACI command. For details, refer to section 4.16, Flash Sequencer Processing Clock Frequency Notification Register (FPCKAR).

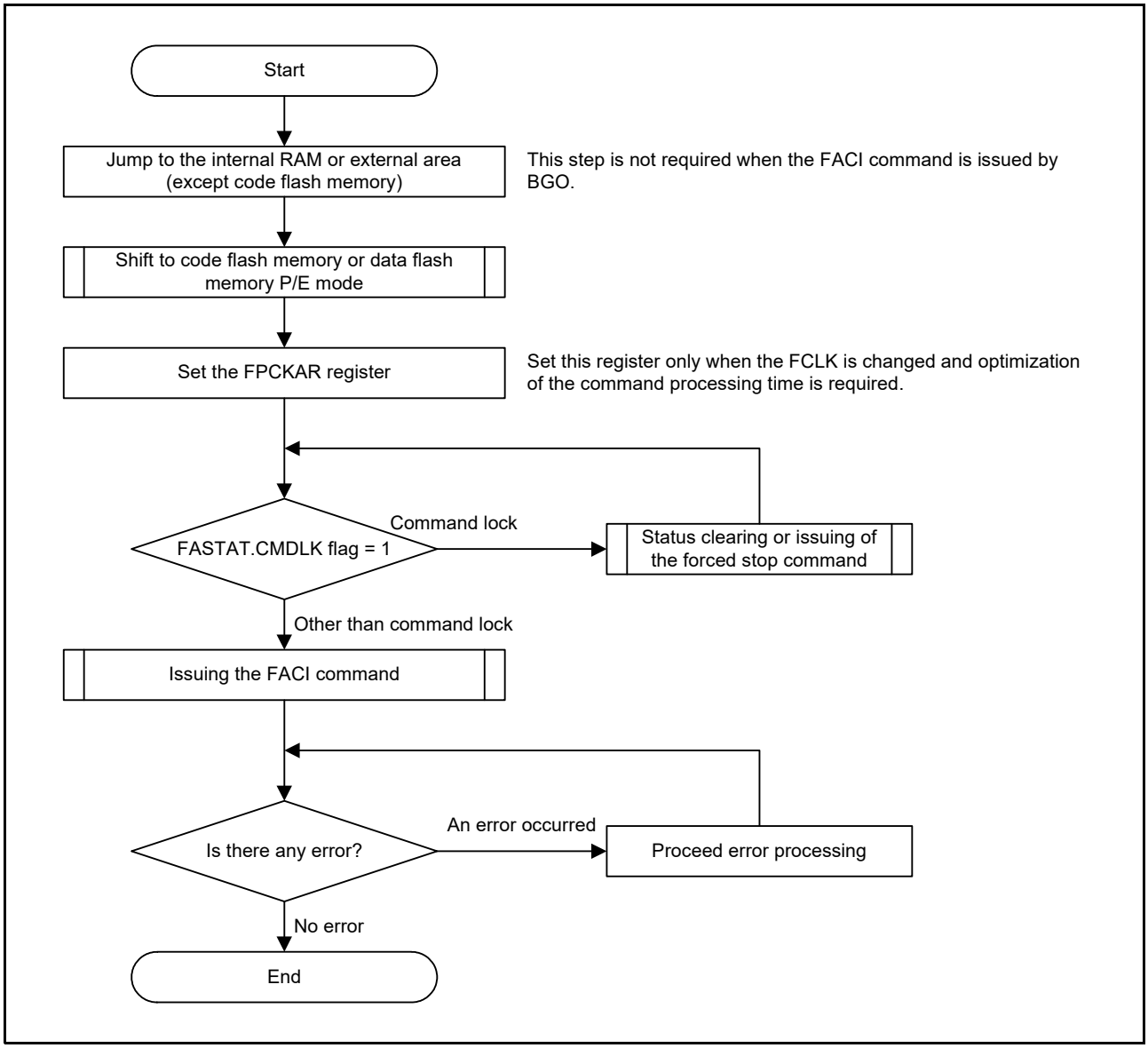
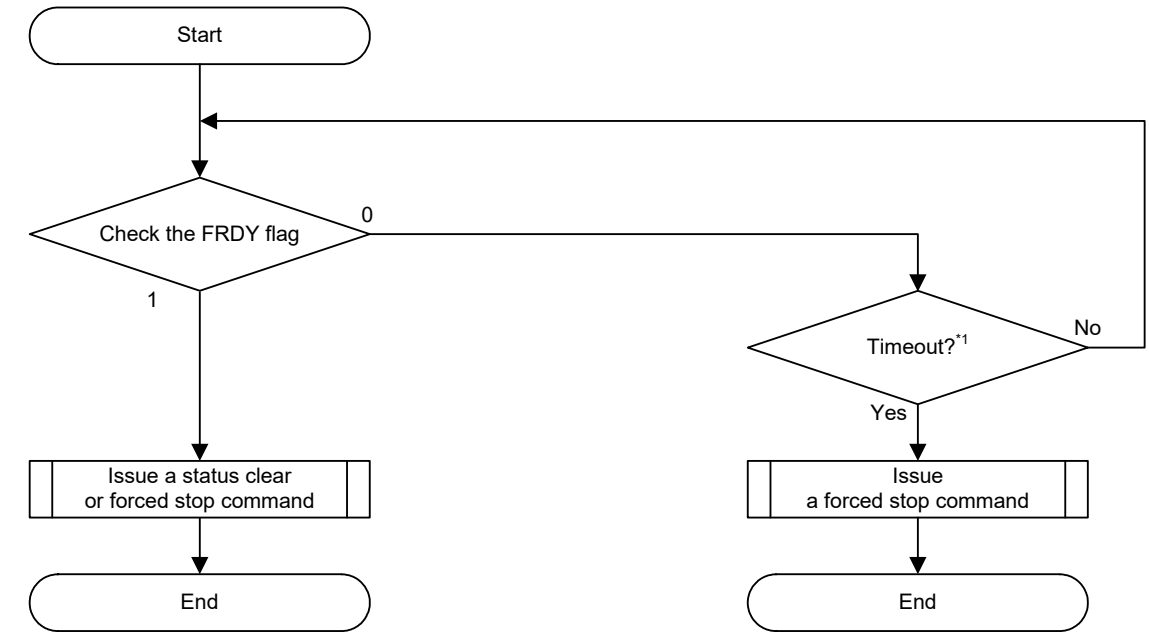


Figure 6.4 Overview Flow when FACI Command is Used

6.3.5 Recovery from the Command-Locked State

When the flash sequencer enters the command-locked state, FACI commands cannot be accepted. To release the sequencer from the command-locked state, use the status clear command, or forced stop command.
When the command-locked state is detected by checking for an error before issuing the P/E suspend command, the FSTATR.FRDY flag may hold 0 as the command processing has not been completed. When the processing is not completed even after time equal to the maximum programming or erasure time specified in the User's Manual: Hardware times 1.1 has elapsed, this is considered a time-out and the flash sequencer should be stopped by the forced stop command.

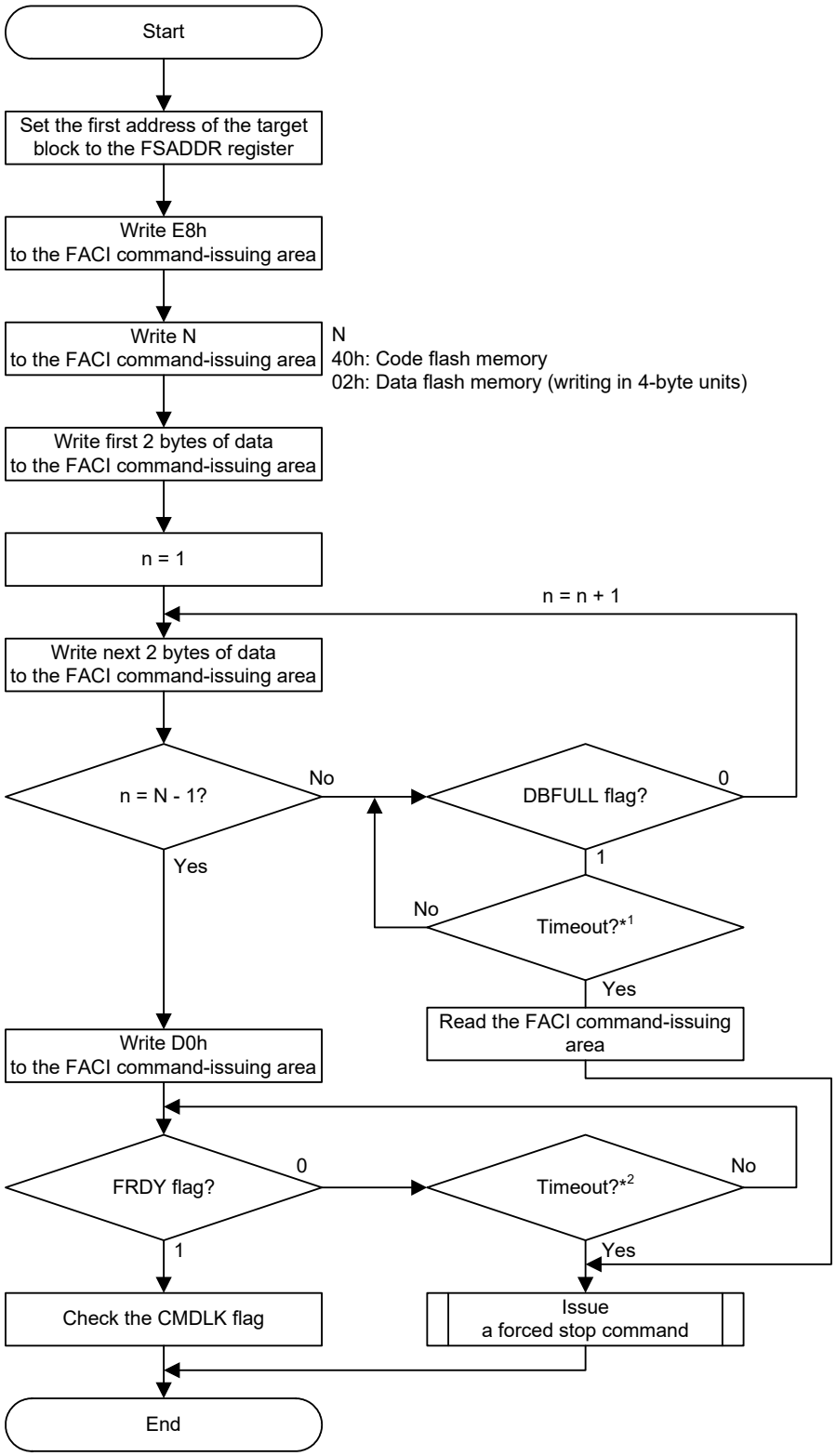


Note 1. Judgment of the timeout is based on 1.1 times the maximum time for processing of the FACI command that is in progress (refer to the Electrical Characteristics chapter in the User's Manual: Hardware).

Figure 6.5 Recovery from the Command-Locked State

6.3.6 Programming Command

A programming command is used for programming the code or data flash memory.
Before issuing a programming command, set the first address of the target block in the FSADDR register.
Writing D0h to the FACI command-issuing area at the final access of the FACI command-issuing starts the programming command processing. Completion of command processing can be checked by reading the FSTATR.FRDY flag. If the target area of programming command processing contains the area not for writing, write FFFFh to the corresponding area.
Issuing a programming command consecutively while the FACI internal data buffer is full leads to a wait on the peripheral bus 6 and this may affect on the bus accesses of the other peripheral IP modules. To avoid the generation of such a wait, issue an FACI command while the FSTATR.DBFULL flag is 0.
In addition, the data buffer never becomes full during programming of the data flash memory.

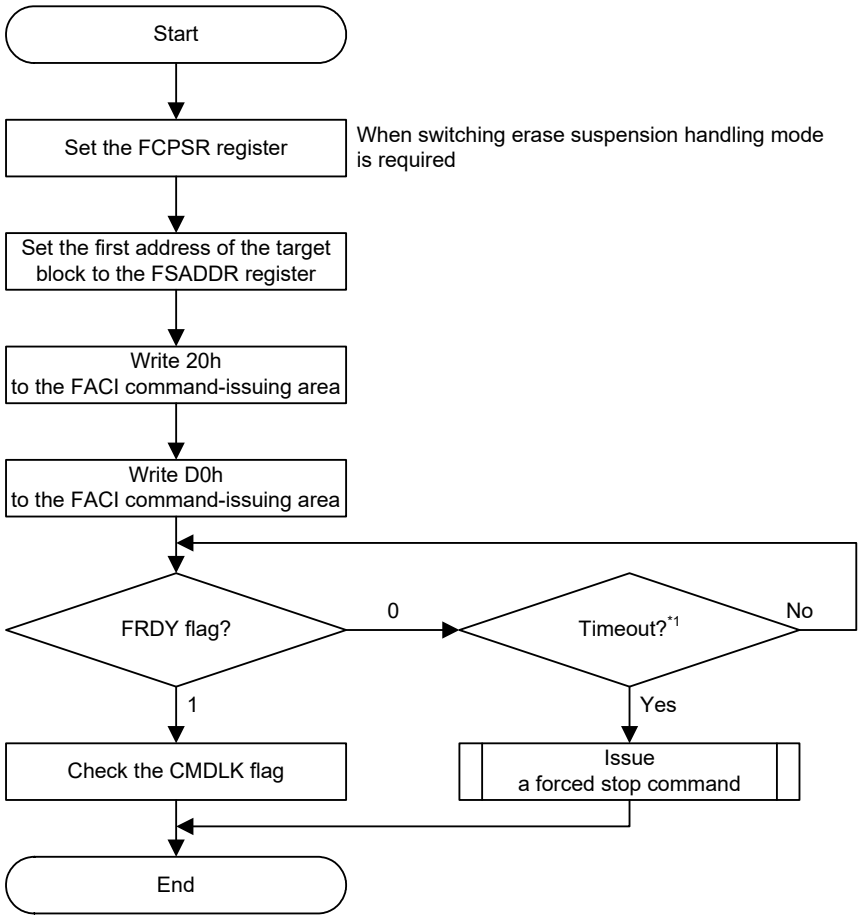


Note 1. Judgment of the timeout is based on 1.4 µs elapsing (when FCLK ≥ 20 MHz)
Note 2. Judgment of the timeout is based on 1.1 times 128-byte programming time (max) for code flash memory.
For data flash memory, judgment is based on 1.1 times 4-byte programming time (max).
For the 128-byte programming time and 4-byte programming time, refer to the Electrical Characteristics chapter in the User's Manual: Hardware.

Figure 6.6 Usage of the Programming Command

6.3.7 Block Erase Command

A block erase command is used to erase the code or data flash memory in single-block units.
Before issuing a block erase command, set the first address of the target block in the FSADDR register. Writing 20h and D0h to the FACI command-issuing area starts processing of a block erase command. Completion of command processing can be confirmed by reading the FSTATR.FRDY flag.
The FCPSR register must be set before issuing the block erase command. The setting of the FCPSR register must be changed to switch the suspending method (suspension priority mode/erasure priority mode) by the P/E suspend command.



Note 1. Judgment of the timeout is based on 1.1 times 32-Kbyte erasure time (max) for code flash memory.
For data flash memory, judgment is based on 1.1 times 64-byte erasure time (max).
For the 32-Kbyte erasure time and 64-byte erasure time, refer to the Electrical Characteristics chapter in the User's Manual: Hardware.

Figure 6.7 Usage of the Block Erase Command

6.3.8 Multi-Block Erase Command

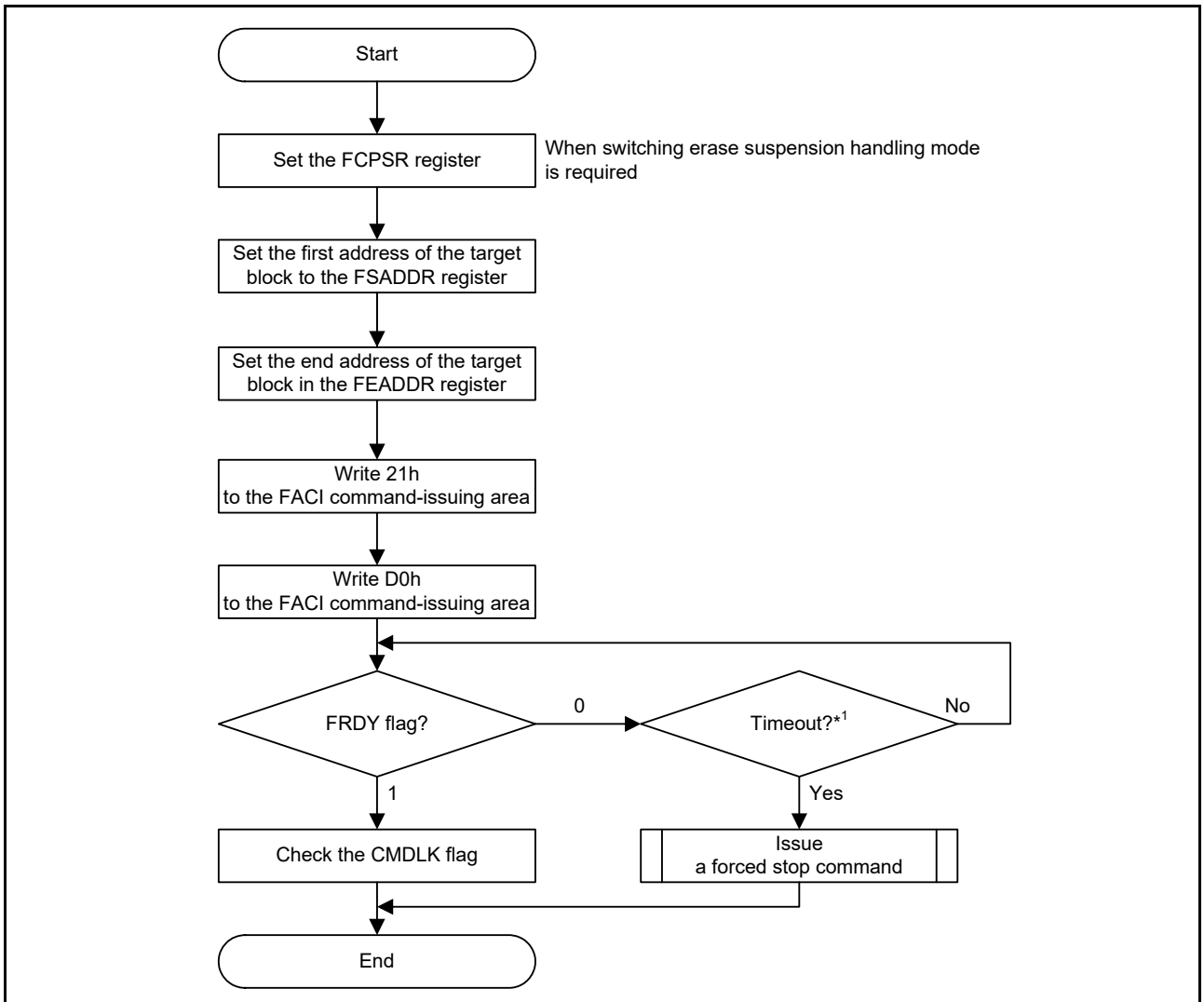
The multi-block erase command can also be issued to erase data in the data flash memory. The unit for erasure is 64, 128, or 256 bytes.

Set the first address of the target area for erasure to the FSADDR register and the end address to the FEADDR register before issuing a multi-block erase command. When 21h and D0h are written to the FACI command issuing area, the process of the multi-block erase command proceeds. The end of command processing can be confirmed by the FSTATR.FRDY flag.

The FCPSR register must be set before issuing the multi-block erase command. The setting of the FCPSR register must be changed when P/E suspension command is used to switch the handling of suspension of erasure (between suspension priority and erasure priority).

Table 6.5 Size Setting for Erasure

Erasure Size	FSADDR	FEADDR
64 bytes	FSA0 to FSA5 = 0 (64-byte boundary)	FSADDR + 3Ch
128 bytes	FSA0 to FSA6 = 0 (128-byte boundary)	FSADDR + 7Ch
256 bytes	FSA0 to FSA7 = 0 (256-byte boundary)	FSADDR + FCh



Note 1. Judgement of the timeout is based on 1.1 times 64-, 128-, or 256-byte erasure time (max).
For each erasure time, refer to the Electrical Characteristics chapter in the User's Manual: Hardware.

Figure 6.8 Usage of the Multi-Block Erase Command

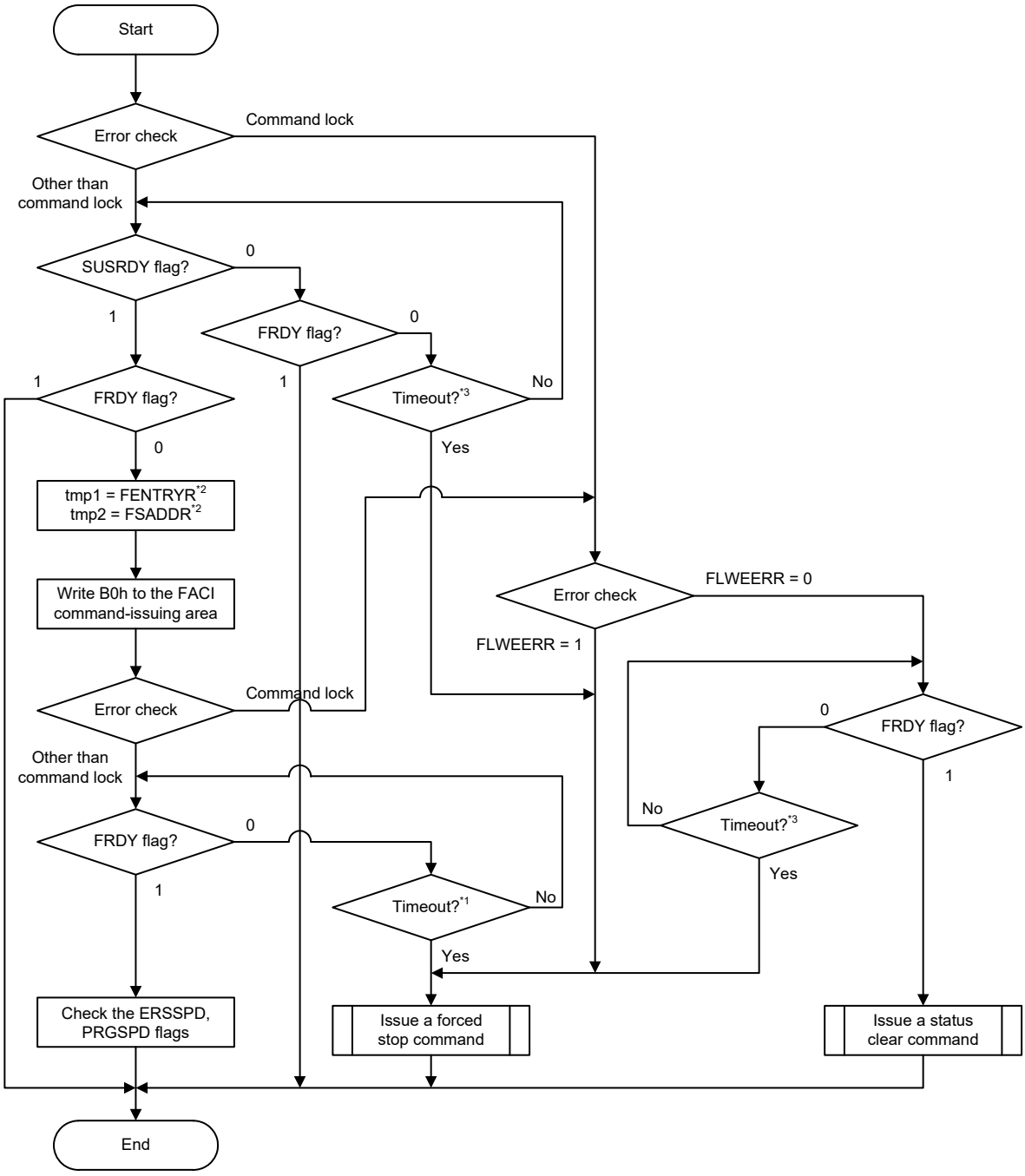
6.3.9 P/E Suspend Command

The P/E suspend command is used to suspend programming or erasure. Before issuing a P/E suspend command, check that the FASTAT.CMDLK flag is 0, and the execution of programming/erasure is normally performed. To confirm that the P/E suspend command can be received, also check that the FSTATR.SUSRDY flag is 1. After issuing a P/E suspend command, read the FASTAT.CMDLK flag to confirm that its value is not 1 (the flash sequencer is not in the command-locked state).

If an error occurs during programming or erasure processing, the FASTAT.CMDLK flag is set to 1. When P/E processing is completed between the FSTATR.SUSRDY flag having been confirmed to be 1 and acceptance of the P/E suspension command, the P/E suspension command is ignored and the flash sequencer does not enter the suspended state (the FSTATR.FRDY flag is 1 and the ERSSPD and PRGSPD flags in the FSTATR register are 0).

When a P/E suspend command is received and then the programming/erasure suspend processing finishes normally, the flash sequencer enters the suspended state, the FSTATR.FRDY flag is set to 1, and the ERSSPD or PRGSPD flag in the FSTATR register is 1. After issuing a P/E suspend command, check that the ERSSPD or PRGSPD flag in the FSTATR register is 1 and the suspended state is entered, and then decide the subsequent flow. If a P/E resume command is issued in the subsequent flow although the suspended state is not entered, an illegal command error occurs and the flash sequencer shifts to the command-locked state (see section 7.2, Error Protection).

If the erasure suspended state is entered, programming to blocks targeted for other than erasure can be performed. Additionally, the programming and erasure suspended states can shift to read mode by clearing the FENTRYR register.



Note 1. Judgment of the timeout is based on 1.1 times the suspend delay time during erasure (max) for both code flash memory and data flash memory.
Note 2. If the FENTRYR and FSADDR registers are not rewritten during suspension, these registers need not be saved.
Note 3. Judgment of the timeout is based on 1.1 times the erasure time (max) for both code flash memory and data flash memory.

For the suspend delay time during erasure and erasure time, refer to the Electrical Characteristics chapter in the User's Manual: Hardware.

Figure 6.9 Usage of the P/E Suspend Command

(1) Suspension during Programming

When issuing a P/E suspend command during the flash memory programming, the flash sequencer suspends programming processing. Figure 6.10 shows the suspend operation of programming. When receiving a programming-related command, the flash sequencer clears the FSTATR.FRDY flag to 0 to start programming. When the flash sequencer enters the state in which the P/E suspend command can be received after starting programming, it sets the FSTATR.SUSRDY flag to 1. When a P/E suspend command is issued, the flash sequencer receives the command and clears the FSTATR.SUSRDY flag to 0. When the flash sequencer receives a P/E suspend command while a programming pulse is being applied, the flash sequencer continues applying the pulse. After the specified pulse application time, the flash sequencer finishes pulse application, and starts the programming suspend processing and sets the FSTATR.PRGSPD flag to 1.

When the suspend processing finishes, the flash sequencer sets the FSTATR.FRDY flag to 1 to enter the programming suspended state. When receiving a P/E resume command in the programming suspended state, the flash sequencer clears the FSTATR.FRDY and FSTATR.PRGSPD flags to 0 and resumes programming.

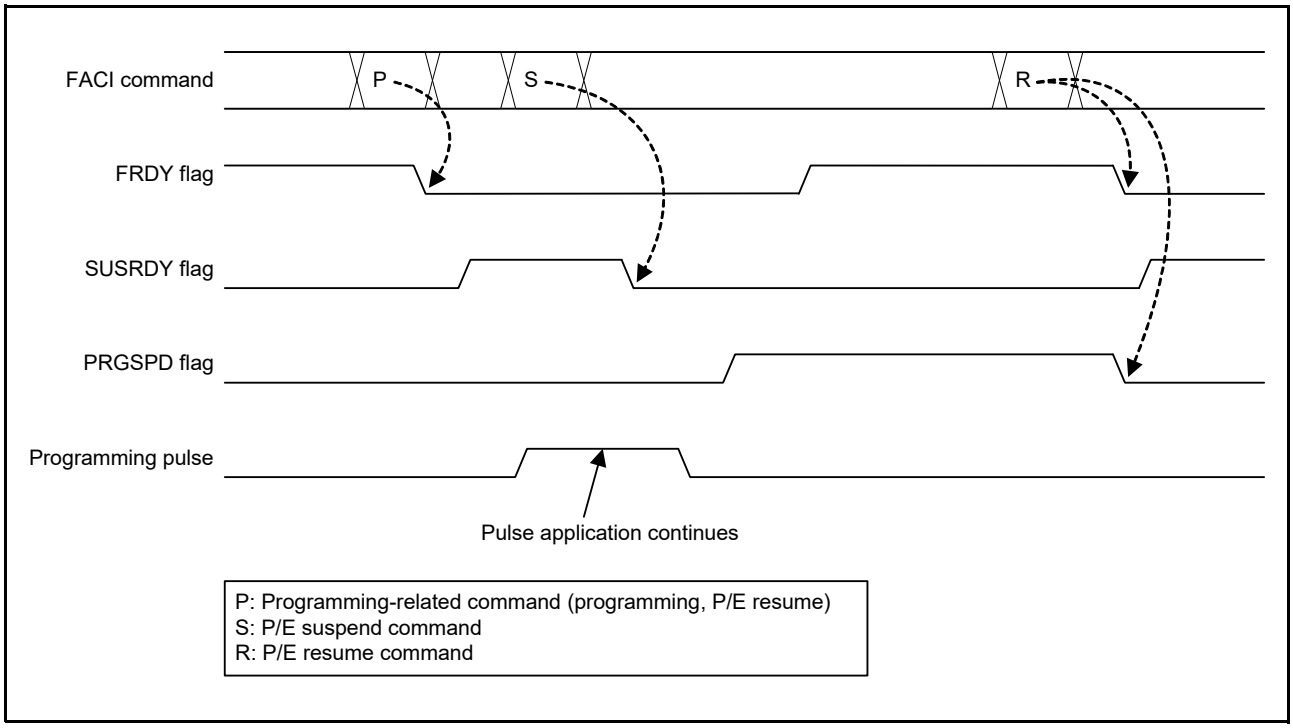


Figure 6.10 Suspension during Programming

(2) Suspension during Erasure (Suspension Priority Mode)

This MCU has a suspension priority mode for the suspension of erasure. Figure 6.11 shows the suspend operation of erasure in suspension priority mode (the FCPSR.ESUSPMD bit is 0).
When receiving an erasure-related command, the flash sequencer clears the FSTATR.FRDY flag to 0 to start erasure. When the flash sequencer enters the state in which the P/E suspend command can be received after starting erasure, it sets the FSTATR.SUSRDY flag to 1. When a P/E suspend command is issued, the flash sequencer receives the command and clears the FSTATR.SUSRDY flag to 0. When receiving a suspend command during erasure, the flash sequencer starts the suspend processing and sets the FSTATR.ERSSPD flag to 1 even if it is applying an erasure pulse. When the suspend processing is completed, the flash sequencer sets the FSTATR.FRDY flag to 1 to enter the erasure suspended state. When receiving a P/E resume command in the erasure suspended state, the flash sequencer clears the FRDY and ERSSPD flags in the FSTATR register to 0 and resumes erasure. Operations of the FRDY, SUSRDY, and ERSSPD flags in the FSTATR register at the suspension and resumption of erasure are the same, regardless of the erasure suspend mode.
The setting of the erasure suspend mode affects the control method of erasure pulses. In suspension priority mode, when receiving a P/E suspend command while erasure pulse A that has never been suspended in the past is being applied, the flash sequencer suspends the application of erasure pulse A and enters the erasure suspended state. When receiving a P/E suspend command while reapplying erasure pulse A after erasure is resumed by a P/E resume command, the flash sequencer continues applying erasure pulse A. After the specified pulse application time, the flash sequencer finishes erasure pulse application and enters the erasure suspended state. When the flash sequencer receives a P/E resume command next and erasure pulse B starts to be newly applied, and then the flash sequencer receives a P/E suspend command again, the application of erasure pulse B is suspended. In suspension priority mode, delay due to suspension can be minimized because the application of an erasure pulse is suspended one time per pulse and priority is given to the suspend processing.

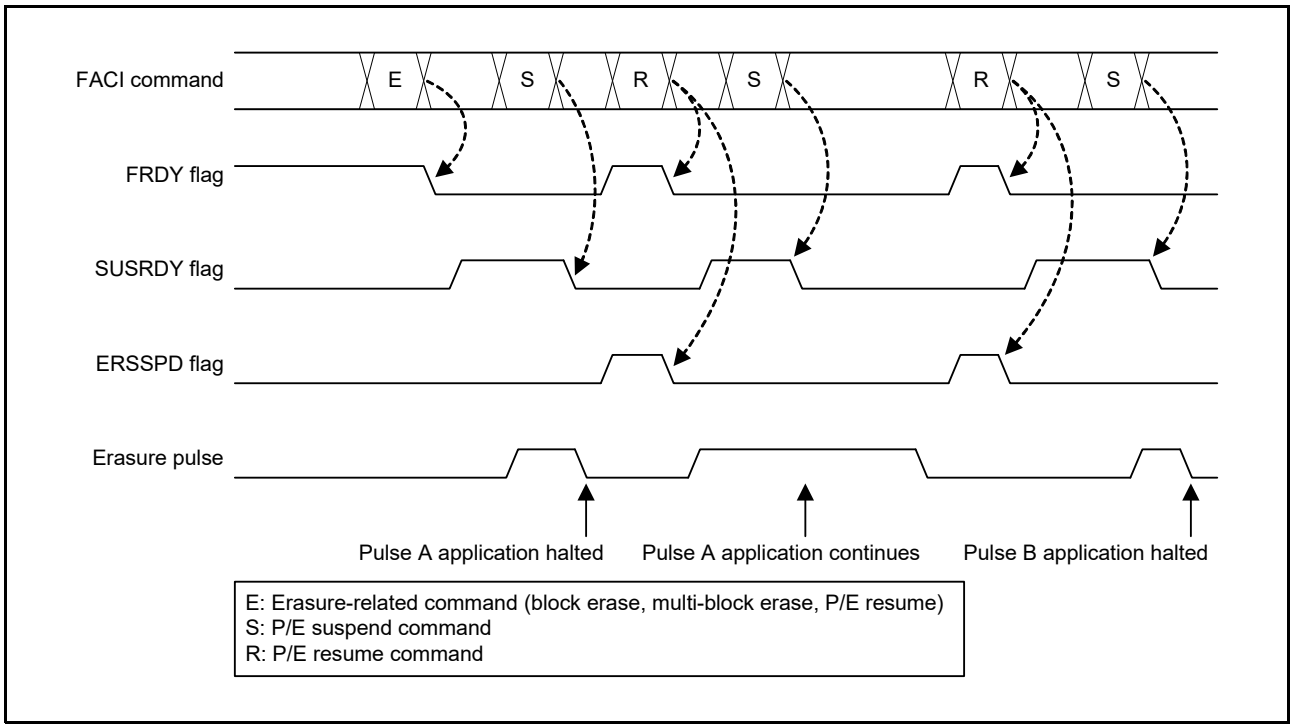


Figure 6.11 Suspension during Erasure (Suspension Priority Mode)

(3) Suspension during Erasure (Erasure Priority Mode)

This MCU has an erasure priority mode for the suspension of erasure.

Figure 6.12 shows the suspend operation of erasure when the erasure suspend mode is set to the erasure priority mode (the FCPSR.ESUSPMD bit is 1). The control method of erasure pulses in erasure priority mode is the same as that of programming pulses for the programming suspend processing.

When the flash sequencer receives a P/E suspend command while an erasure pulse is being applied, the flash sequencer definitely continues applying the pulse. In this mode, the required time for the whole erasure processing can be reduced as compared with the suspension priority mode because the reapplication of erasure pulses does not occur when a P/E resume command is issued.

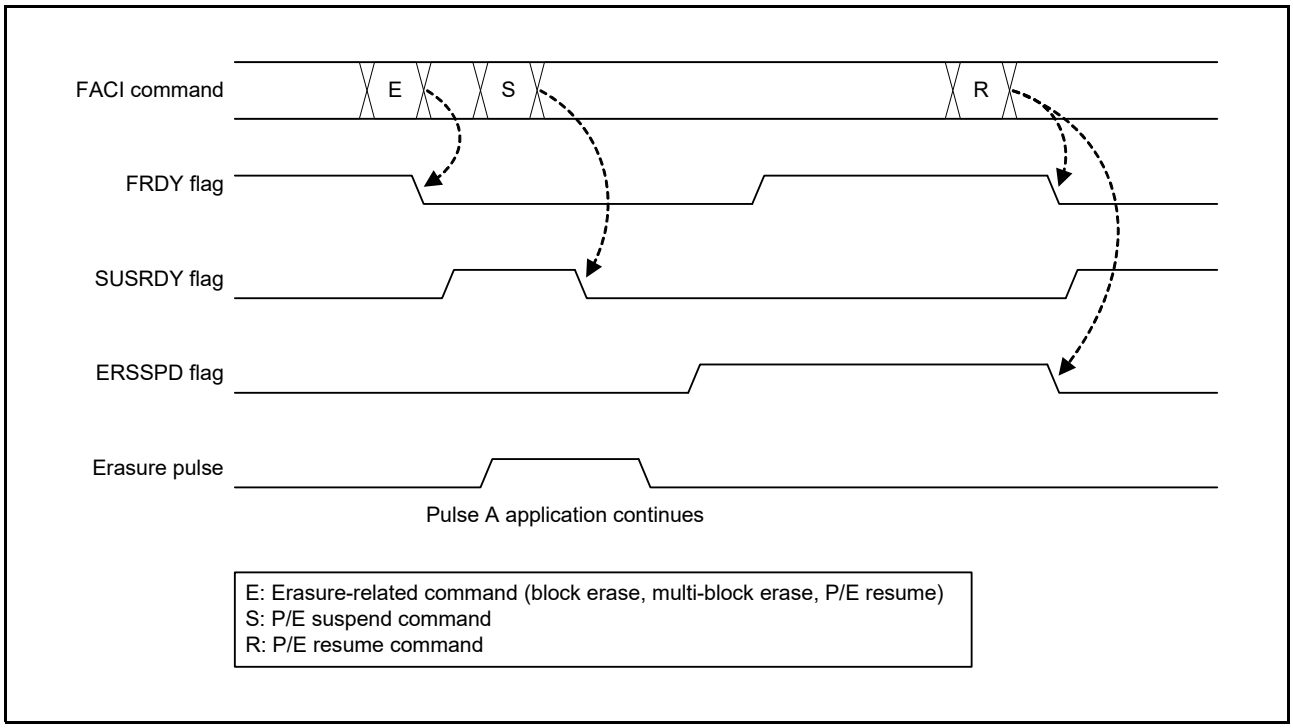
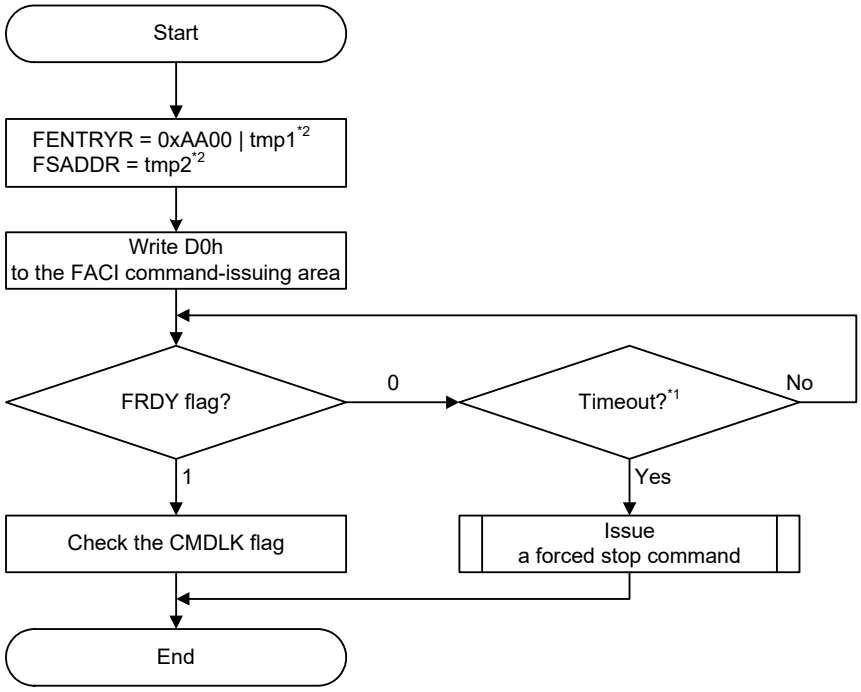


Figure 6.12 Suspension during Erasure (Erasure Priority Mode)

6.3.10 P/E Resume Command

To resume suspended programming or erasure, use the P/E resume command. When the settings of the FENTRYR register are changed during suspension, reset the setting of the FENTRYR register to the value immediately before the P/E suspend command was issued, and then issue a P/E resume command. Completion of processing of the resumed command can be confirmed by reading the FSTATR.FRDY flag.



Note 1. Judgment of the timeout is based on 1.1 times the maximum time for halted processing of the FACI command (refer to the Electrical Characteristics chapter in the User's Manual: Hardware).
Note 2. Restore the FENTRYR and FSADDR registers to the value saved before the P/E suspend command is issued. If these registers are not rewritten during suspension, restore is not needed.

Figure 6.13 Usage of the P/E Resume Command

6.3.11 Status Clear Command

When one of the ILGLERR, ILGCOMERR, FESETERR, SECERR, OTERR, ERSERR, PRGERR, and FLWEERR flag bits in the FSTATR register is set to 1, the flash sequencer enters the command-locked state. When one of the CFAE and DFAE flags in the FASTAT register is set to 1, the flash sequencer also enters the command lock state. In the command-locked state, the flash sequencer can accept only status clearing command or forced end command.
The status clear command is used to clear the command-locked state (see section 6.3.5, Recovery from the Command-Locked State). To clear the CFAE, DFAE, and CMDLK flags in the FASTAT register, and the ILGLERR, ILGCOMERR, FESETERR, SECERR, OTEERR, ERSERR, and PRGERR flags in the FSTATR register in the command-locked state, the status clear command is available.
The FLWEERR flag cannot only be cleared by the status clearing command, but can only be cleared by the forced end command.

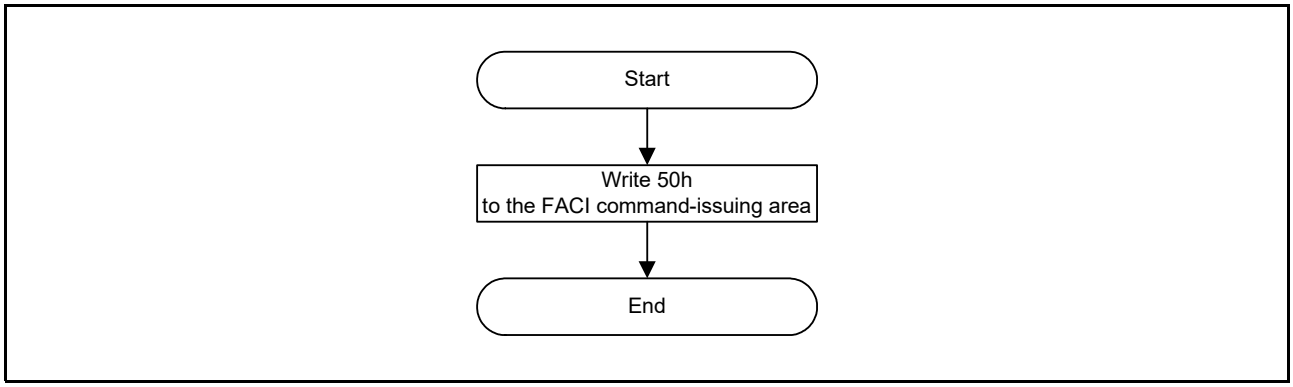
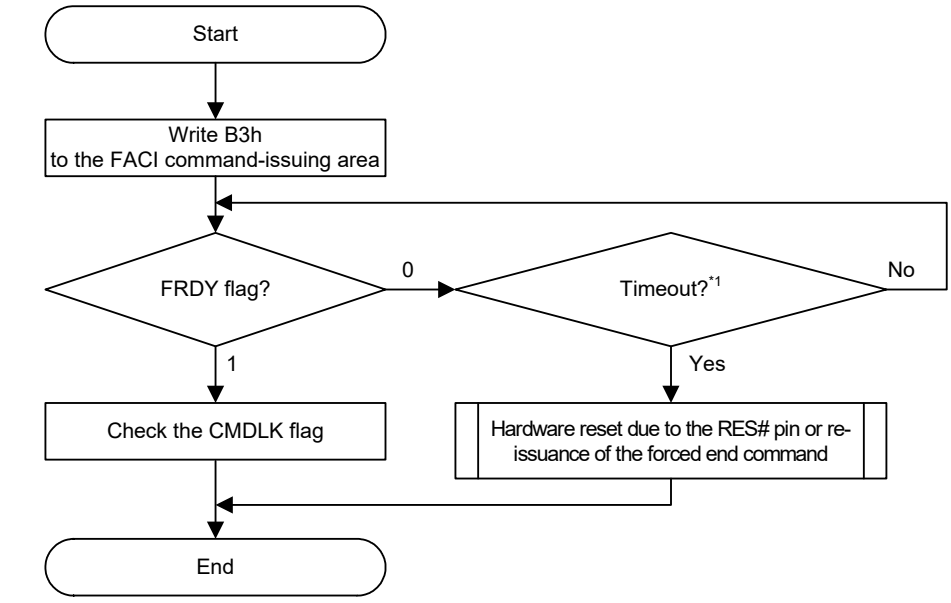


Figure 6.14 Usage of the Status Clear Command

6.3.12 Forced Stop Command

The forced stop command forcibly ends command processing by the flash sequencer. Although this command halts command processing in higher speed than the P/E suspension command, values from the area where programming or erasure was in progress are not guaranteed. Furthermore, resumption of processing is not possible. Processing of programming or erasure that was terminated by the forced stop command is also defined as one round of programming. Executing a forced stop command also initializes the whole FCU and a part of the FACI, and the FASTAT and FSTATR registers. Accordingly, this command can be used in the procedure for recovery from the command-locked state and in processing in response to a time-out of the flash sequencer (see section 6.3.5, Recovery from the Command-Locked State).



Note 1. Judgment of the timeout is based on 1.1 times the maximum time for the forced stop command (refer to the Electrical Characteristics chapter in the User's Manual: Hardware).

Figure 6.15 Usage of the Forced Stop Command

6.3.12.1 How to Use the Forced Stop Command when a Command is being issued

When processing is terminated by the forced stop command while a timeout is generated based on the DBFULL bit judgment of the program command, writing to the FACI command issuing area may be handled as the data written by the program command. In this case, read the FACI command issuing area and generate a command lock intentionally, then issue the forced stop command according to the method of returning from the command lock state. A command lock can be generated although the access size for reading the FACI command issuing area is in 8-, 16-, or 32-bit units.

6.3.13 Blank Check Command

Values read from data flash memory that has been erased but not yet been programming again (i.e. that is in the nonprogrammed state) are undefined. Use the blank check command when you need to confirm that an area is in the nonprogrammed state.

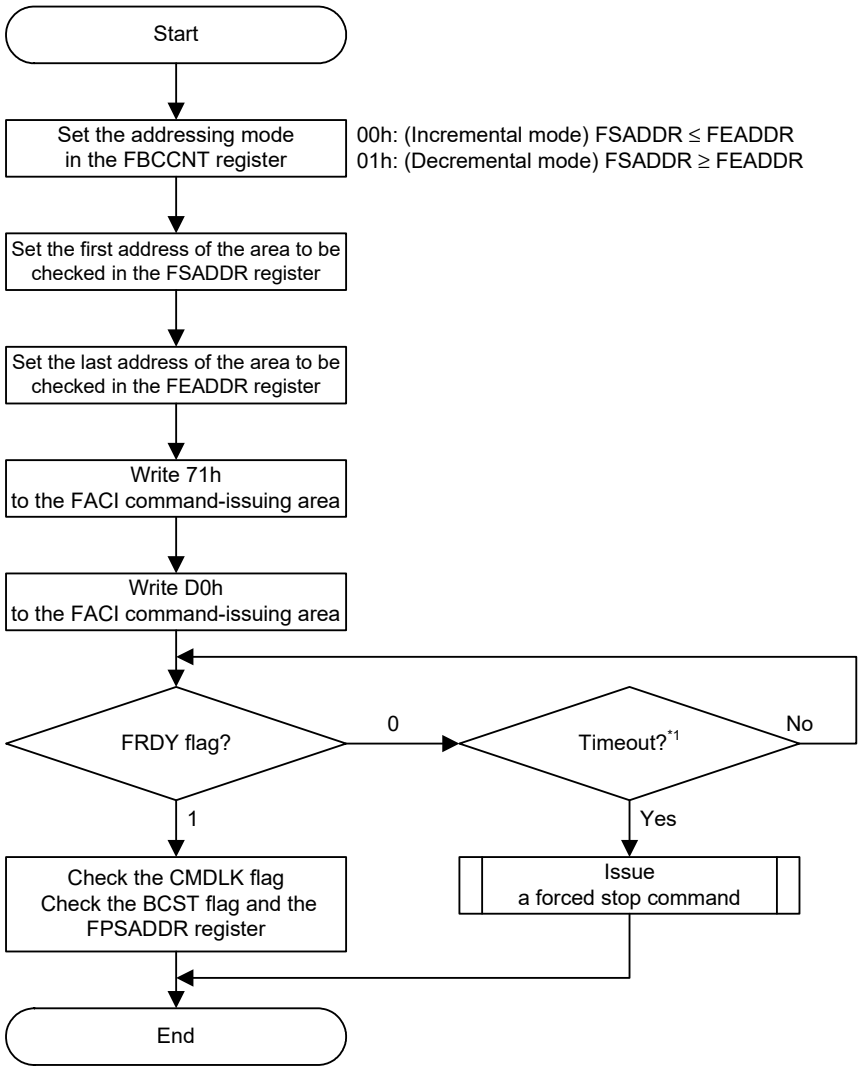
Before issuing a blank check command, set addressing mode, start and end addresses of the target area for blank checking to the FBCCNT, FSADDR, and FEADDR registers.

When the FBCCNT.BCDIR bit is 1, the value specified in the FSADDR register must be set at least the value specified in the FEADDR register.

When the FBCCNT.BCDIR bit is 0, the value specified in the FSADDR register must be the value specified in the FEADDR register or less.

When the settings of the FBCCNT.BCDIR bit, FSADDR register, and FEADDR register are inconsistent, the flash sequencer enters the command-locked state. The size of the target area for blank checking is in the range from 4 bytes to 64 Kbytes and is set in units of 4 bytes.

Write 71h and D0h to the FACI command-issuing area to start blank checking. Completion of processing can be confirmed by the FSTATR.FRDY flag. At the end of processing, the result of blank checking is stored in the FBCSTAT.BCST flag. If the target area for blank checking includes areas where programming has been completed, the flash sequencer stores the address of the programmed data that it first detected in the FPSADDR register.

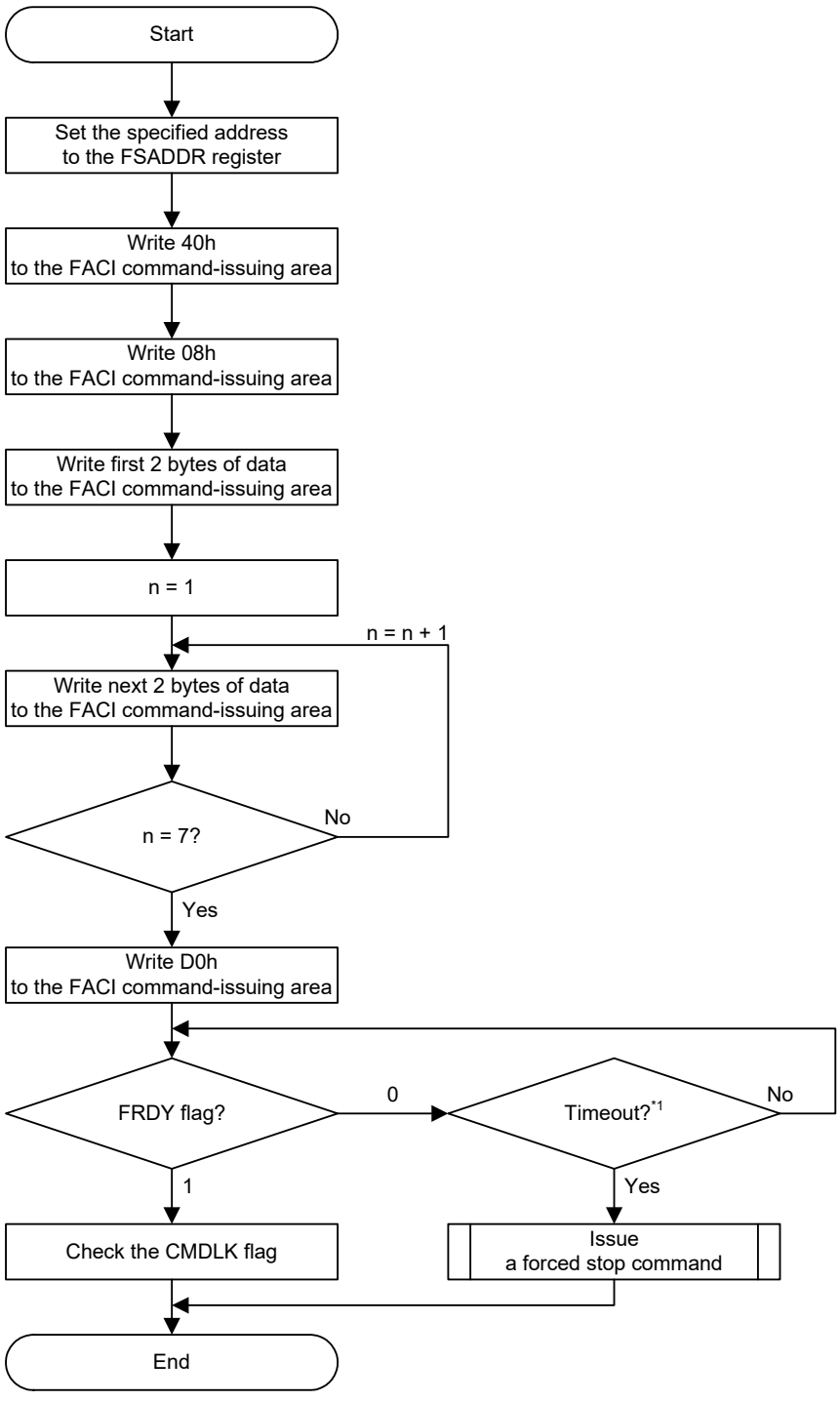


Note 1. Judgment of the timeout is based on 1.1 times the blank checking time (max.) for the entire target area. For the blank checking time, refer to the Electrical Characteristics chapter in the User's Manual: Hardware.

Figure 6.16 Usage of the Blank Check Command

6.3.14 Configuration Set Command

The configuration set command is used to set the option-setting memory (configuration setting area).
Before issuing a configuration set command, set the specified address (shown in Table 6.6) in the FSADDR register.
Writing D0h to the FACI command-issuing area in the final access for issuing the FACI command starts processing of the configuration set command.



Note 1. Timeout is judged to be after 185 ms (when FCLK ≥ 20 MHz), 205 ms (when FCLK = 15 MHz), or 340 ms (when FCLK = 4 MHz).

Figure 6.17 Usage of the Configuration Set Command

The correspondence between the possible target data for configuration setting and the address value set in the FSADDR register is shown in Table 6.6. For details on the FSADDR register, see section 4.5, FACI Command Start Address Register (FSADDR).

Table 6.6 Address Used by Configuration Set Command

Address	FSADDR Register Value	Setting Data	Operation of additional writing		Timing when the Setting is Enabled
			FAW.FSPR bit is 1	FAW.FSPR bit is 0	
FE7F 5D00h	00FF 5D00h	Option function select register 0 (OFS0), option function select register 1 (OFS1), endian select register (MDE)	Writable	Writable	At a reset
FE7F 5D10h	00FF 5D10h	TM identification data register (TMINF)	Writable	Writable	At a reset
FE7F 5D20h	00FF 5D20h	Bank select register (BANKSEL)	Writable	Writable	At a reset
FE7F 5D40h	00FF 5D40h	Serial programmer command control register (SPCC), TM enable flag register (TMEF)	Writable*1 (from 1 to 0 only)	Writable*1 (from 1 to 0 only)	When a reset or command is executed*3
FE7F 5D50h	00FF 5D50h	OCD/serial programmer ID setting register (OSIS)	Writable	Writable	At a reset
FE7F 5D64h	00FF 5D60h	Flash access window setting register (FAW)*2	Writable	Not writable*2	When a reset or command is executed
FE7F 5D70h	00FF 5D70h	ROM code protect register (ROMCODE)	Writable	Writable	At a reset

Note 1. Once these bits are set to 0, the bits cannot be restored to 1 by using the configuration setting command.
Note 2. The FAW.FSPR bit cannot be restored to 1 by using the configuration setting command once it is set to 0. Therefore, setting the access window and start-up area select flags again becomes impossible. (when the configuration setting command is issued to the address of FE7F 5D64h, the command is locked.) Exercise extra caution when handling the FAW.FSPR bit.
Note 3. The setting in the serial programmer command control register (SPCC) is enabled after a reset. The setting of the TM enable flag register (TMEF) is enabled when a reset or command is executed.

7. Protection Function

7.1 Software Protection

Software protection disables programming and erasure for the flash memory through the settings of control registers. If an attempt is made to issue an FACI command against software protection, the flash sequencer enters the command-locked state.

7.1.1 Protection through FWEPROR

Programming cannot proceed in any mode unless the FWEPROR.FLWE[1:0] bits are set to 01b.

7.1.2 Protection through FENTRYR

When the FENTRYR register is set to 0000h, the flash sequencer enters read mode. In read mode, FACI commands cannot be accepted. If an attempt is made to issue an FACI command in read mode, the flash sequencer enters the command-locked state.

7.2 Error Protection

Error protection detects erroneous issuance of FACI commands, unauthorized access, and flash sequencer malfunction. FACI command acceptance is disabled (command-locked state) in response to the detection of these errors. The flash memory cannot be programmed or erased while the flash sequencer is in the command-locked state. For release from the command-locked state, issue a status clear or forced stop command. The status clear command can only be used while the FSTATR.FRDY flag is 1. The forced stop command can be used regardless of the value of the FSTATR.FRDY flag. Generation of a flash access error (FIFERR) interrupt detects malfunction. An FIFERR interrupt is generated under any of the following conditions.

- When the flash sequencer enters the command lock state (when the FASTAT.CMDLK flag is 1) while the FAEINT.CMDLKIE bit is 1
- When violation in access to the data flash memory occurred (the FASTAT.DFAE flag is 1) while the FAEINT.DFAEIE bit is 1
- When violation in access to the code flash memory occurred (when the FASTAT.CFAE flag is 1) while the FAEINT.CFAEIE bit is 1

When the flash sequencer enters the command-locked state in response to a command other than the P/E suspend command during programming or erasure processing, the flash sequencer continues the processing for programming or erasure. In this state, the P/E suspend command cannot be used to suspend the processing for programming or erasure. If a command is issued in the command-locked state, the ILGLERR and ILGCOMERR flags in the FSTATR register becomes 1 and the other flags retain the values set due to previous error detection.
Table 7.1 shows error protection types and status bit values after error detection.

Table 7.1 Error Protection Type (1 / 2)

Error Type	Description	ILGCOMERR	FESETERR	SECERR	OTERR	ILGLERR	ERSERR	PRGERR	FLWEERR	CFAE	DFAE
FENTRYR setting error	The FENTRYR setting is AA81h	0	1	0	0	1	0	0	0	0	0
	The FENTRYR setting at suspension disagrees with that at resumption	0	1	0	0	1	0	0	0	0	0
Illegal command error	Access with an undefined unit was attempted in the first access by the FACI command (not writing of a byte)	1	0	0	0	1	0	0	0	0	0
	Access with an undefined code was attempted in the first access by the FACI command	1	0	0	0	1	0	0	0	0	0
	The value specified in the last access of the multiple-access FACI command is not D0h.	1	0	0	0	1	0	0	0	0	0
	The value “N” (see Table 6.2) specified in the second write access of an FACI command in the programming or configuration setting command is wrong.	1	0	0	0	1	0	0	0	0	0
	When a blank check command has been issued under one of the following conditions • When the FBCCNT.BCDIR bit is 0, and the value in FSADDR > that in FEADDR • When the FBCCNT.BCDIR bit is 1, and the value in FEADDR > that in FSADDR • The setting range of bits 16 to 0 in FEADDR is between 0 8000h and 1 FFFFh	1	0	0	0	1	0	0	0	0	0/1 *1
	When a multi-block erasure command has been issued under one of the following settings. • The value in FSADDR > that in FEADDR • The setting range of bits 16 to 0 in FEADDR is between 0 8000h and 1 FFFFh	1	0	0	0	1	0	0	0	0	0/1 *1
	An FACI command not acceptable in each mode has been issued (see Table 6.3)	1	0	0	0	1	0	0	0	0	0
	Program or block erase command has been issued to the area protected by the area protection	1	0	0	0	1	0	0	0	0	0
	A program command has been issued to the area where the erasure has been suspended during the processing of erase suspension	1	0	0	0	1	0	0	0	0	0
	An FACI command has been issued when command acceptance conditions are not satisfied (see Table 6.4)	0/1 *2	0/1 *2	0/1 *2	0/1 *2	1	0/1 *2	0/1 *2	0/1 *2	0/1 *2	0/1 *2
Erasure error	An error occurs during erasure	0	0	0	0	0	1	0	0	0	0
Programming error	An error occurs during programming	0	0	0	0	0	0	1	0	0	0
Code flash memory access violation	When a program command or block erase command has been issued under the following settings in code flash memory P/E mode Products with at least 1.5 Mbytes of code flash memory: • The setting value of bits 23 to 0 in FSADDR is within the range from 00 0000h to DF FFFFh Products with 1 Mbyte of code flash memory or less: • The setting value of bits 23 to 0 in FSADDR is within the range from 00 0000h to EF FFFFh	0	0	0	0	1	0	0	0	1	0
	When a configuration program command has been issued under the following settings in code flash memory P/E mode • The setting value of bits 9 to 0 in the FSADDR register ranges from 000h to 0FFh, or from 180h to 3FFh	0	0	0	0	1	0	0	0	1	0

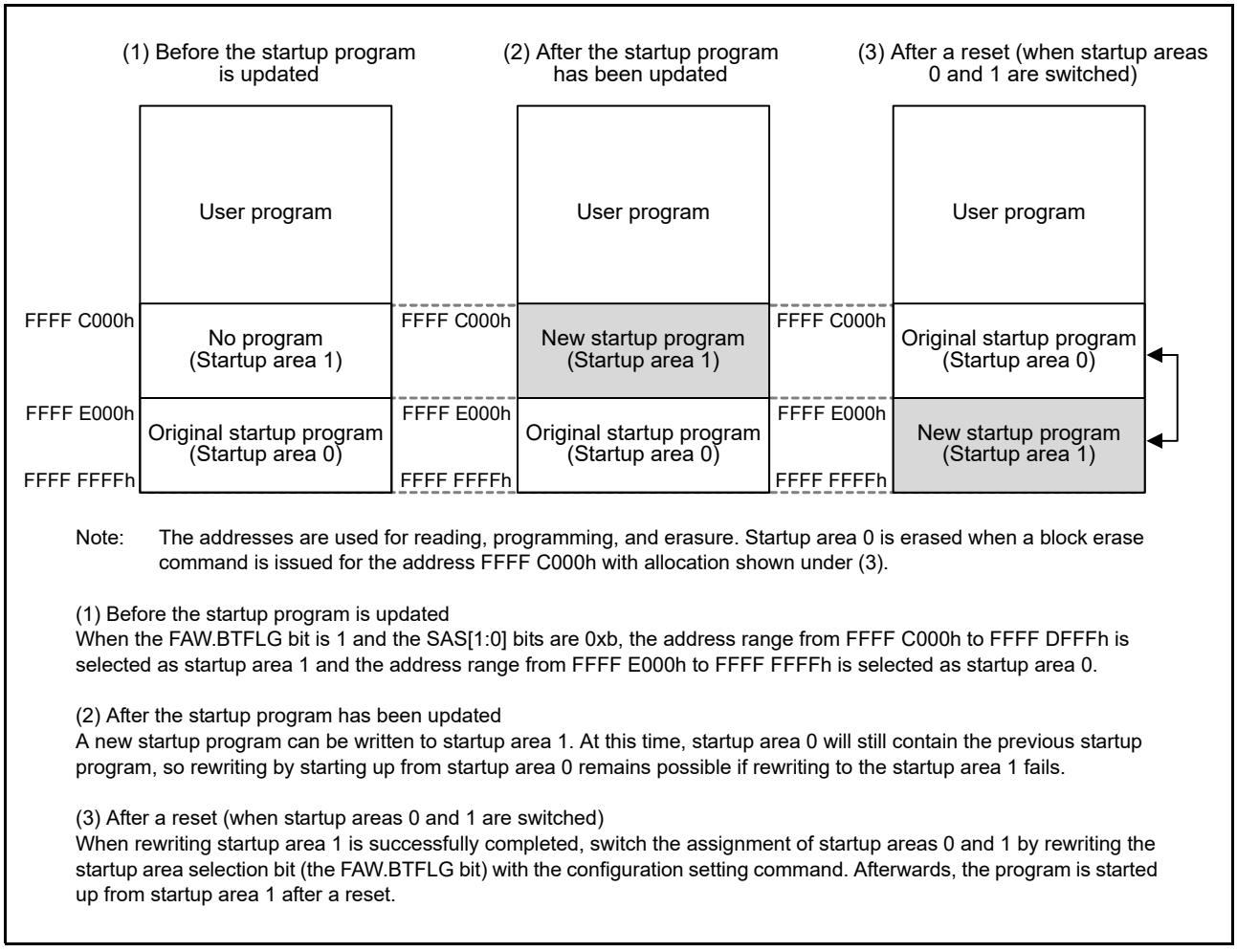
Table 7.1 Error Protection Type (2 / 2)

Error Type	Description	ILGCOMERR	FESETERR	SECERR	OTERR	ILGLERR	ERSERR	PRGERR	FLWEERR	CFAE	DFAE
Data flash memory access violation	When a program command or block erase command has been issued under the following settings in data flash memory P/E mode • The setting value of bits 16 to 0 in FSADDR is within the range from 0 8000h to 1 FFFFh	0	0	0	0	1	0	0	0	0	1
	When a multi-block erase command or blank check command has been issued under the following settings in data flash memory P/E mode • The setting value of bits 16 to 0 in FSADDR is within the range from 0 8000h to 1 FFFFh	1	0	0	0	1	0	0	0	0	1
Security error	When the FAW.FSPR bit is 0, a configuration setting command is issued for the settings of access window and the FAW.BTFLG bit	0	0	1	0	1	0	0	0	0	0
Others	The FACI command-issuing area has been accessed in read mode	0	0	0	1	1	0	0	0	0	0
	The FACI command-issuing area has been read in code flash memory P/E mode or data flash memory P/E mode	0	0	0	1	1	0	0	0	0	0
FLWE error	When the FACI command is processed, disable programming or erasure by using the FWEPROR register*3	0	0	0	0	0	0/1	0/1	1	0	0

Note 1. If the setting value in the FSADDR register matches the condition for violations in access to the data flash memory, the FASTAT.DFAE bit is set to 1.
Note 2. This is the value when a command is executed.
Note 3. For details on the FWEPROR register, see section 4.1, Flash P/E Protect Register (FWEPROR).

7.3 Start-Up Program Protection

Protection of the startup program is for protection of the program to be started after a reset (the startup program). This function provides a way to safely update the startup program when rewriting is suspended during a reset.
The startup area is 8 Kbytes in size and is assigned to the user area in the code flash memory. This function uses the values of the FAW.BTFLG bit and the FSUACR.SAS[1:0] bits to change the area where the startup program is stored in block units (see Figure 7.1 to Figure 7.4).
In protection of the startup program, the state of the selection of the startup area can be fixed by the access window protection bit (FAW.FSPR). However, the FAW.FSPR bit never be restored to 1 once the flag is set to 0. Exercise extra caution when handling the FAW.FSPR bit.
In addition, this protection cannot be used when dual mode is selected by the bank mode switching function (when the MDE.BANKMD[2:0] bits are 000b).



Note: The addresses are used for reading, programming, and erasure. Startup area 0 is erased when a block erase command is issued for the address FFFF C000h with allocation shown under (3).

(1) Before the startup program is updated
When the FAW.BTFLG bit is 1 and the SAS[1:0] bits are 0xb, the address range from FFFF C000h to FFFF DFFFh is selected as startup area 1 and the address range from FFFF E000h to FFFF FFFFh is selected as startup area 0.

(2) After the startup program has been updated
A new startup program can be written to startup area 1. At this time, startup area 0 will still contain the previous startup program, so rewriting by starting up from startup area 0 remains possible if rewriting to the startup area 1 fails.

(3) After a reset (when startup areas 0 and 1 are switched)
When rewriting startup area 1 is successfully completed, switch the assignment of startup areas 0 and 1 by rewriting the startup area selection bit (the FAW.BTFLG bit) with the configuration setting command. Afterwards, the program is started up from startup area 1 after a reset.

Figure 7.1 Concept of Protection of the Startup Program

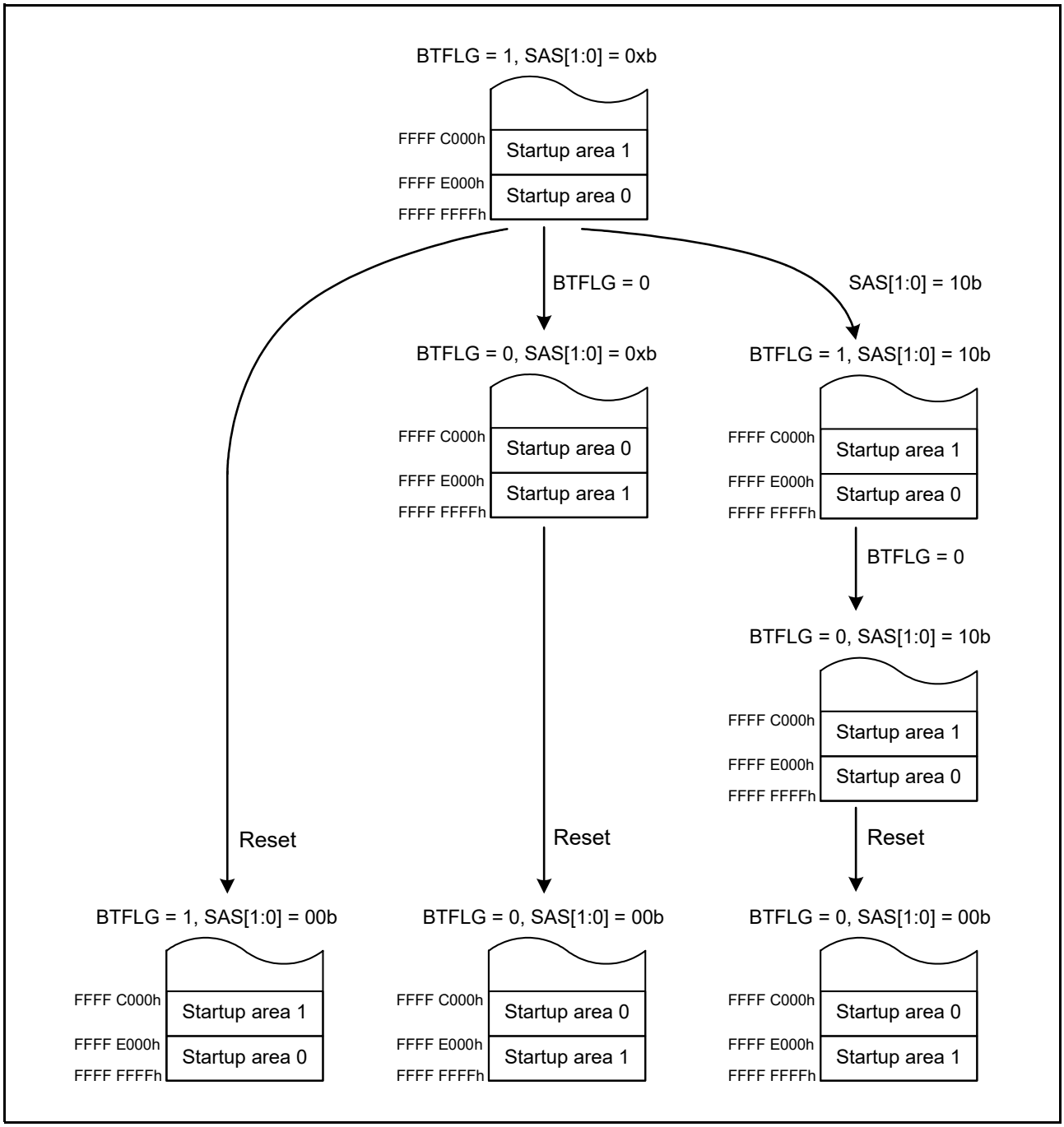


Figure 7.2 Example 1 of Transitions for Startup Program Protection Settings

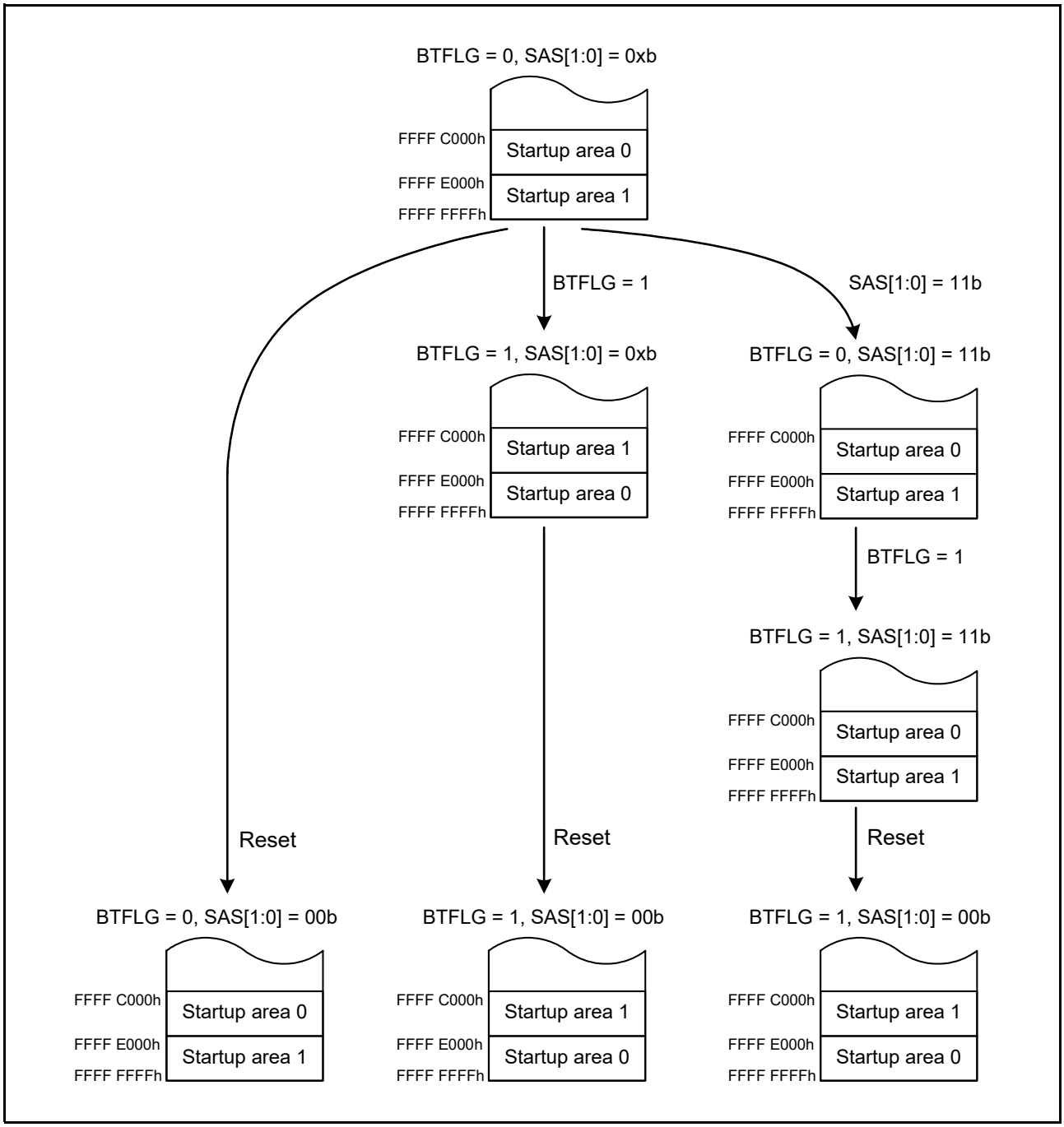


Figure 7.3 Example 2 of Transitions for Startup Program Protection Settings

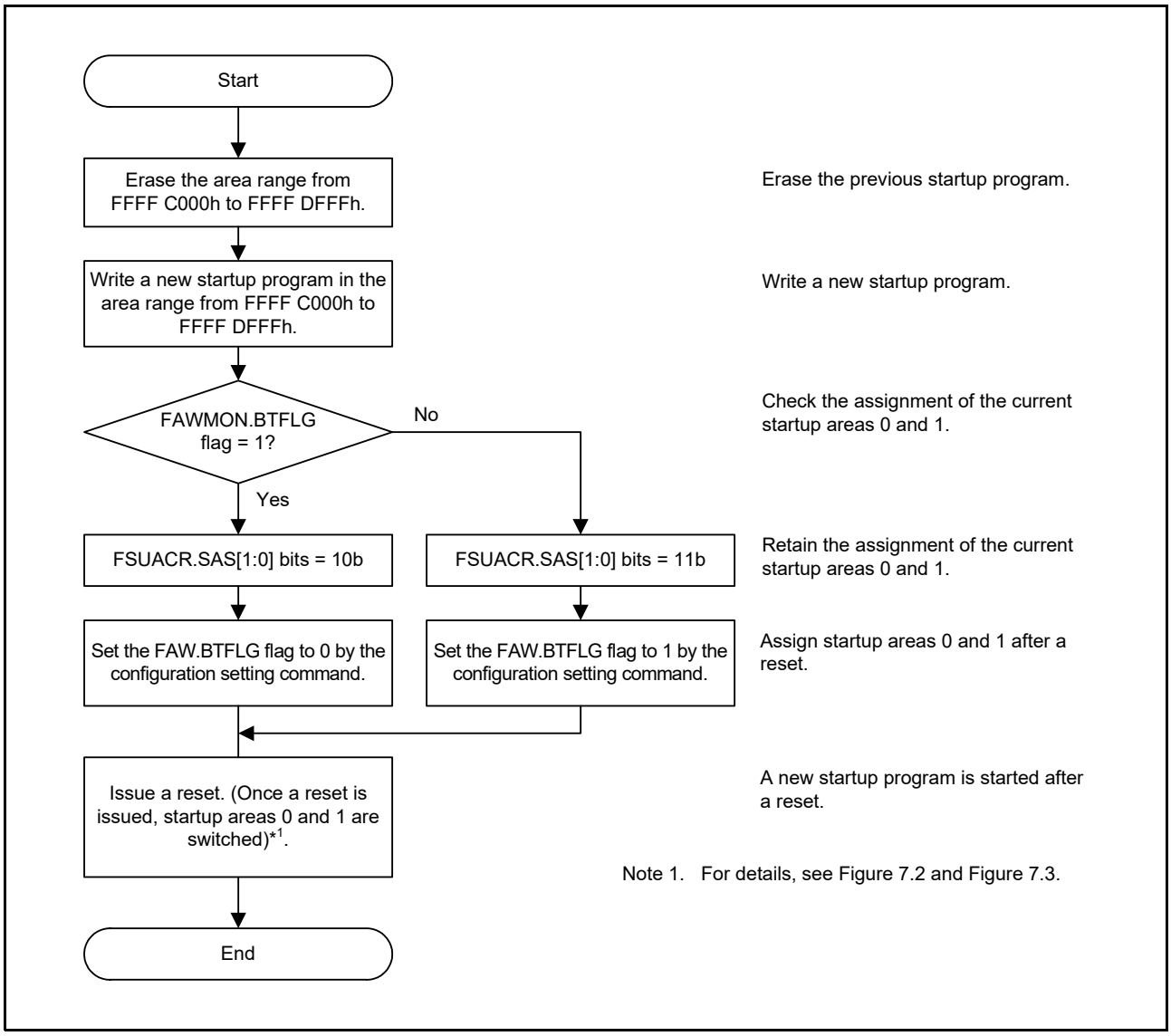


Figure 7.4 Example of Flowchart for Selecting Startup Area

7.4 Protection by Area Protection

Issuing an FACI command that programs or erases the area set outside the access window leads to the command-locked state. The access window is valid only in the user area of the code flash memory. The access window is valid in self-programming mode or serial programming mode.
The access window can be set in block units.
Figure 7.5 shows the Area Protection Overview.

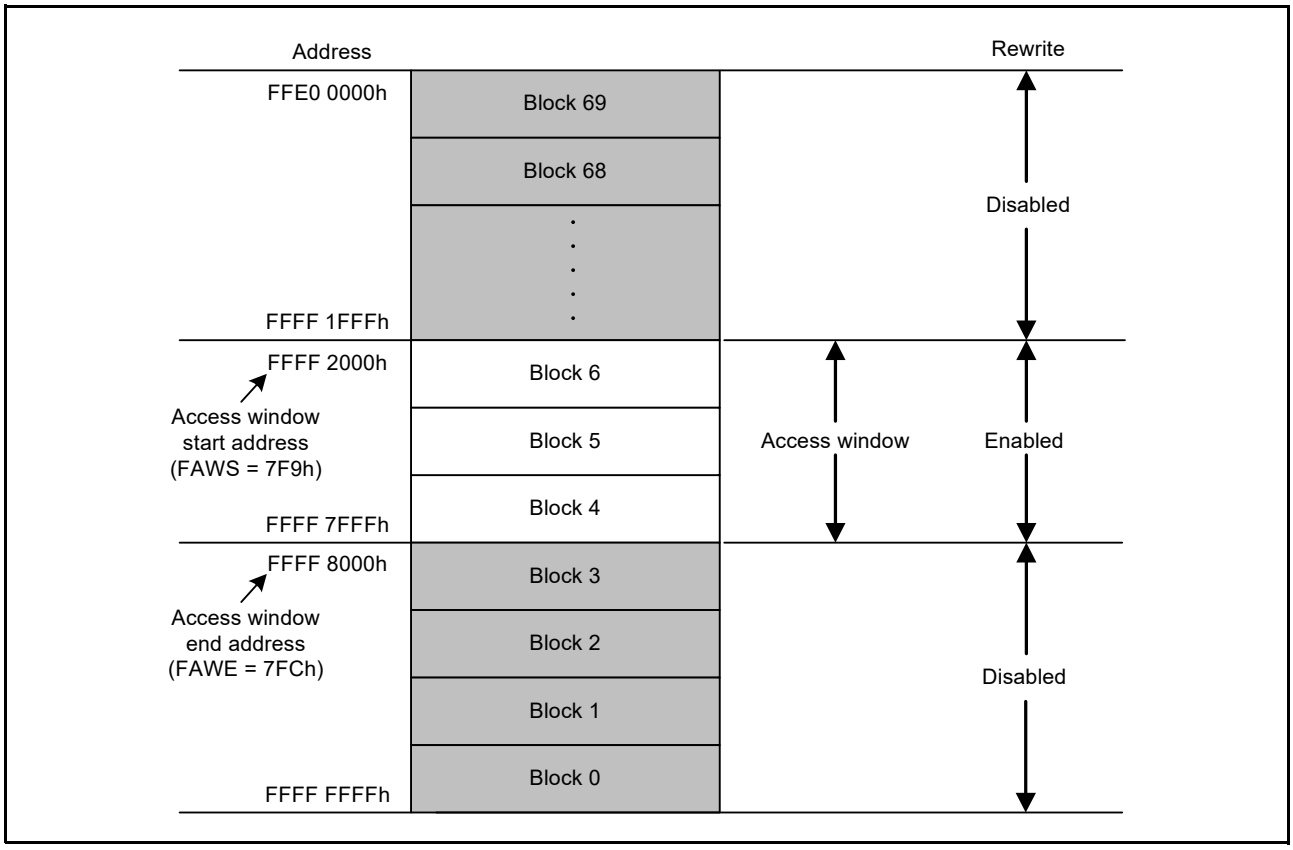


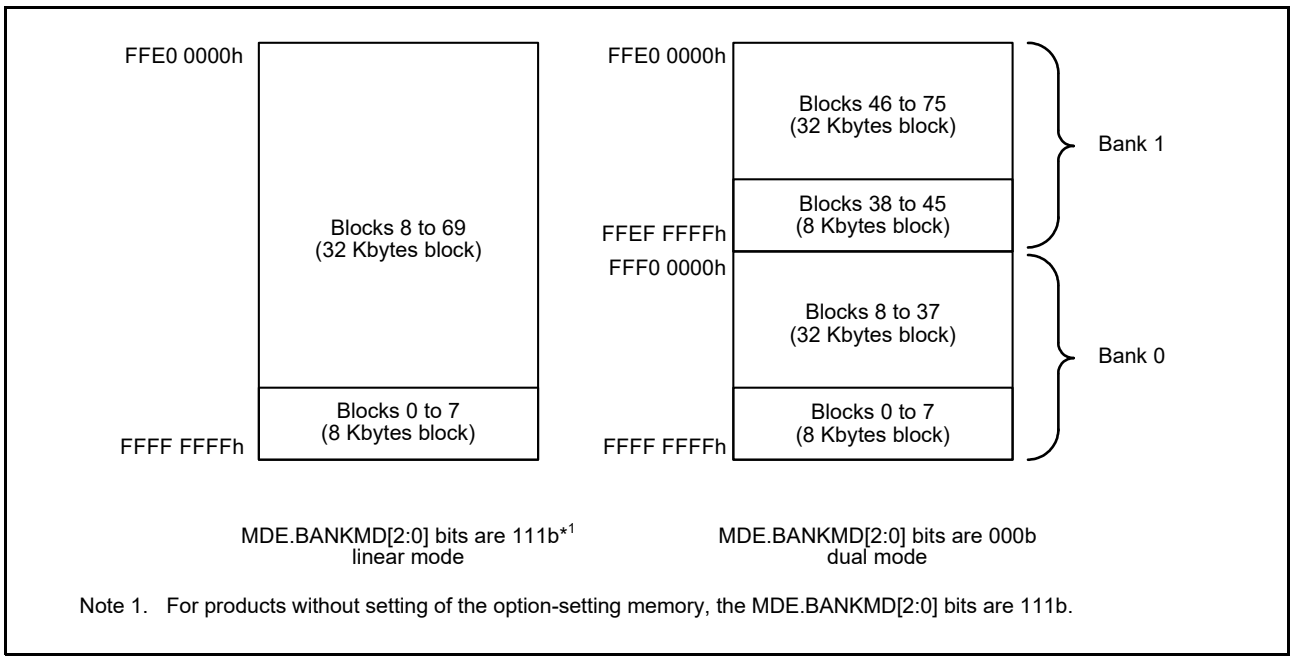
Figure 7.5 Area Protection Overview (When Blocks 4 to 6 are Set as the Access Window in Products with 2 Mbytes of Code Flash Memory)

7.5 Dual Bank Function

This function is only available for products with at least 1.5 Mbytes of code flash memory.
This protection uses the functions of bank mode switching and startup bank selection to update a program while a user program is running and to provide a safe method of updating in cases where programming is suspended during a reset.

7.5.1 Switching Bank Modes

The bank mode switching function selects either linear mode in which the user area in the code flash memory is used as one area, or dual mode in which the user area is divided into two bank areas. Figure 7.6 shows an example of flow of switching bank modes. A reset after setting the MDE.BANKMD[2:0] bits in the option setting memory determines the mode of the bank mode switching function. Selecting dual mode enables the startup bank selection function.
When dual mode is selected by bank mode switching function (the MDE.BANKMD[2:0] bits are 000b), start-up program protection function cannot be used.



Note 1. For products without setting of the option-setting memory, the MDE.BANKMD[2:0] bits are 111b.

Figure 7.6 Example of Flow of Switching Bank Modes (For Products with 2 Mbytes of Code Flash Memory)

7.5.2 Selecting the Startup Bank

Startup bank selection provides a way to safely update the program by selecting a bank area to be started in dual mode (when the MDE.BANKMD[2:0] bits are 000b) when programming is suspended during a reset. Figure 7.7 is a schematic view of startup bank selection and Figure 7.8 shows an example of the flow of startup bank selection. A reset after setting the value of the BANKSEL.BANKSWP[2:0] bits in the option-setting memory changes the addresses of banks 0 and 1 and booting up a program proceeds from the updated area. When the address is switched by using startup bank selection, the P/E target for the FACI commands is also switched. This function is invalid in linear mode.

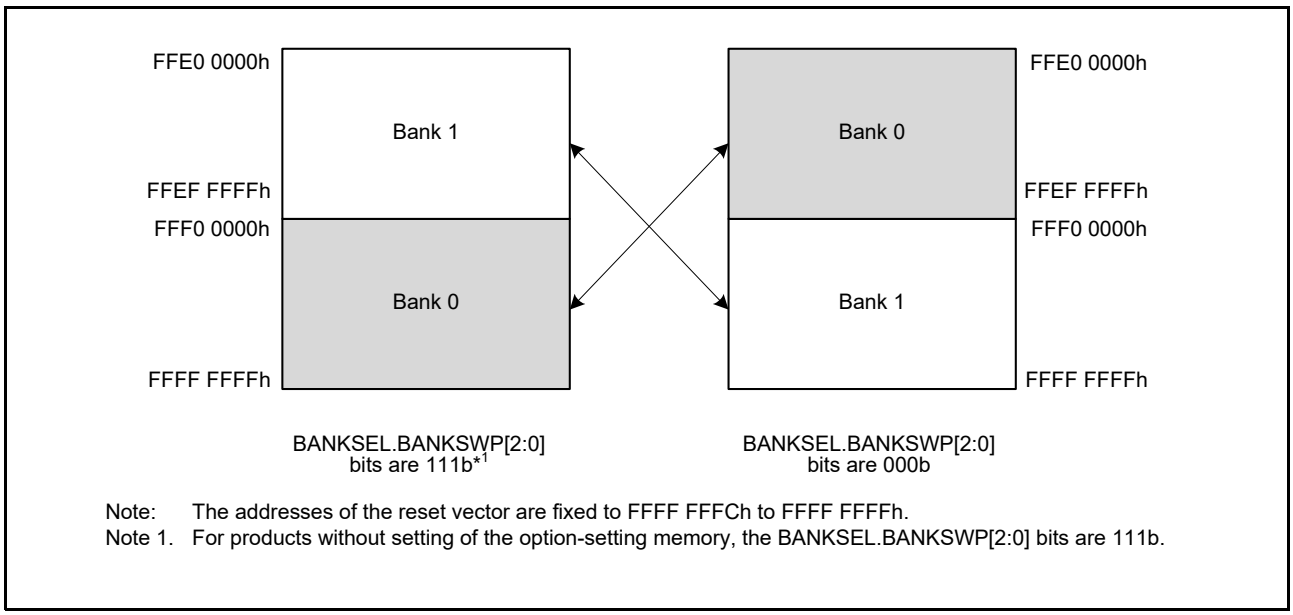
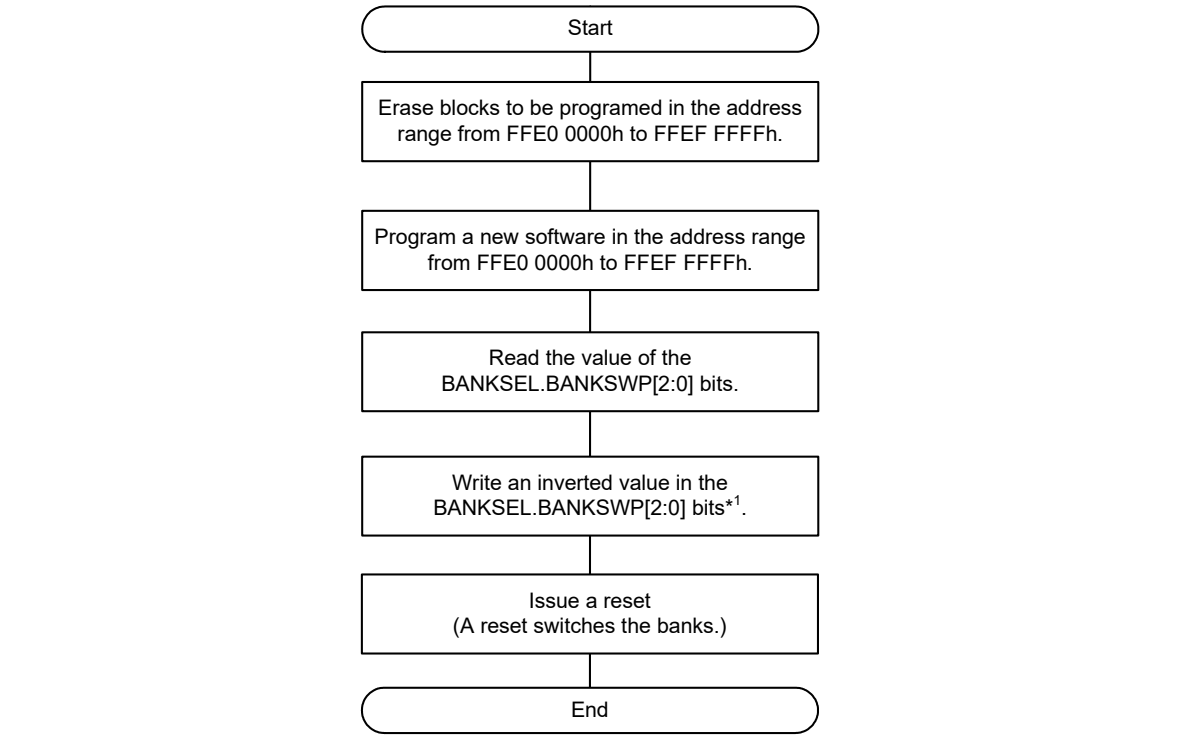


Figure 7.7 Example of Startup Bank Selection (For Products with 2 Mbytes of Code Flash Memory)



Note 1. Set the inverse of the read value of the BANKSEL.BANKSWP[2:0] bits (000b or 111b).

Figure 7.8 Example of Startup Bank Selection Flow (For Products with 2 Mbytes of Code Flash Memory)

8. Usage Notes

(1) Reading Area Where Programming/Erasure has been Forcibly Ended and Area Targeted for Suspension

The data stored in the area where programming/erasure is forcibly ended or the area targeted for suspension are undefined. To avoid faulty operation caused by reading undefined data, take care not to fetch instructions or read data from areas where programming/erasure was forcibly ended and from areas targeted for suspension.

(2) Suspension During Programming/Erasure

When processing of programming/erasure is stopped by issuing the P/E suspend command, the programming/erasure processing can be resumed by issuing the P/E resume command. If the flash sequencer enters the command-locked state for any reason and issues the forced stop command after the suspended processing is normally completed and the ERSSPD flag or PRGSPD flag is set to 1, the suspended processing cannot be resumed. In addition, the values in the area where the processing was suspended are not guaranteed. Erase that area.

(3) Prohibition of Additional Programming

The same area in code or data flash memory cannot be programmed more than once in a row. To program the code or data flash memory where has been programed, erase the target area. Additional writing to the option-setting memory is possible.

(4) Resets During Programming/Erasure, or Blank Checking

In the case of a reset due to the signal on the RES# pin during programming/erasure of the code flash memory and during programming/erasure, or blank checking of the data flash memory, wait for at least t_{RESWF} (see the User's Manual: Hardware for details) of the reset input period once the operating voltage is within the range stipulated in the electrical characteristics, then release the device from the reset state.

(5) Allocation of Vectors for Interrupts and Other Exceptions During Programming/Erasure

Generation of an interrupt or other exception during programming/erasure may lead to fetching of the vector from the code flash memory. Under conditions where BGO cannot be used, set the address of the vector to an address that is not in the code flash memory. Alternatively, make sure that no handling of interrupts or exceptions proceeds during programming/erasure.

(6) Items Prohibited During Programming/Erasure or Blank Checking

High voltage is applied to the flash memory during programming/erasure or blank checking. To prevent damage to the flash memory, do not perform the following operations.

- Have the operating voltage from the power supply go beyond the permitted range.
- Change the FWEPROR.FLWE[1:0] bits.
- Change the SYSCR0.ROME bit.
- Change the OPCCR.OPCM[2:0] bits.
- Change the SCKCR.FCK[3:0] and PCLKB[3:0] bits.
- Change the SCKCR3.CKSEL[2:0] bits.
- Change the RSTCKCR.RSTCKEN bit.
- Transition to the all module clock stop mode, software standby mode, or deep software standby mode.

REVISION HISTORY	RX65N Group, RX651 Group Flash Memory User's Manual: Hardware Interface

Rev.	Date	Description	
		Page	Summary
1.00	Aug 24, 2016	—	First edition, issued
2.00	May 24, 2017	—	Products with at least 1.5 Mbytes of code flash memory added The conventional products indicated as "products with 1 Mbyte of code flash memory or less"
		15	4.5 FACI Command Start Address Register (FSADDR), changed
		26	4.14 Flash Access Window Monitor Register (FAWMON), changed
		29	4.17 Start-Up Area Control Register (FSUACR), changed
		36	6.3.4 Overview Flow when FACI Command is Used, changed
		48	6.3.11 Status Clear Command, changed
		52	6.3.14 Configuration Set Command Figure 6.17 Usage of the Configuration Set Command, Note 1. changed
		53	Table 6.6 Address Used by Configuration Set Command, changed
		54	7.2 Error Protection, changed
		55 to 56	Table 7.1 Error Protection Type, changed
		57 to 60	7.3 Start-Up Program Protection, changed Figure 7.1 Concept of Protection of the Startup Program, added Figure 7.2 Example 1 of Transitions for Startup Program Protection Settings, added Figure 7.3 Example 2 of Transitions for Startup Program Protection Settings, added Figure 7.4 Example of Flowchart for Selecting Startup Area, added
		—	9. Electrical Characteristics, deleted

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
2.10	Jun 20, 2019	6. FACI Commands		
		43	Figure 6.9 Usage of the P/E Suspend Command, changed	TN-RX*-A183B/E
		47	Figure 6.13 Usage of the P/E Resume Command, changed	

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