RTDACHB0000RS-MF-1

Bi-Directional Switch (BDS) GaN Evaluation Board

Introduction

The RTDACHB0000RS-MF-1 evaluation board is designed to evaluate the 650V TP65B110HRU device. The board utilizes the pre-programmed Renesas R5F526TAAGFL#50 MCU to operate the board in a simple plug-and-play method. This document provides a comprehensive design overview and schematic explanation of the RTDACHB0000RS-MF-1 BDS evaluation board.

Caution: The RTDACHB0000RS-MF-1 board is powered by AC main voltage. When powered, this board generates non-insulated high voltages which may produce electrical shock, burn, and/or fire hazards, resulting in risk of property damage, personal injury, and/or death. While the board is powered, never touch it or its electrical circuits since they may be operating at high voltages that can cause an electrical shock hazard.

Contents

Figures

1. Overview

The Renesas Bi-Directional Switch (BDS) GaN conducts current and blocks voltage in both directions with the smallest footprint and a best-in-class switching figure of merit. The device combines a monolithic, bi-directional high-voltage, depletion-mode GaN with normally-off low voltage silicon MOSFETs to provide superior performance, high threshold for standard gate-drive compatibility, easy integration, and robust reliability for advanced power applications. While the Renesas GaN BDS is qualified under AC bias relevant for ordinary field applications, it can also withstand DC bias, a feature not possible with GIT GaN competition. DC blocking capability is a plus, giving customers extra safety during DC fault conditions and extra flexibility during custom start-up or diagnostic sequences where AC bias may not always be available.

The board is designed to showcase the half bridge operation of the BDS devices in an AC-AC conversion. The AC-AC conversion is one of the building blocks for many topologies that are used in industrial, solar, and automotive OBC applications.

Supported topologies and applications using the BDS GaN (see Figure 1) include:

- **Vienna Rectifier** – Non-isolated PFC AC-DC converter for data center applications
- **3-Phase Matrix Converter** – Single Stage AC-DC conversion for on-board charger
- **Cycloconverter** – AC-AC conversion for solar inverters

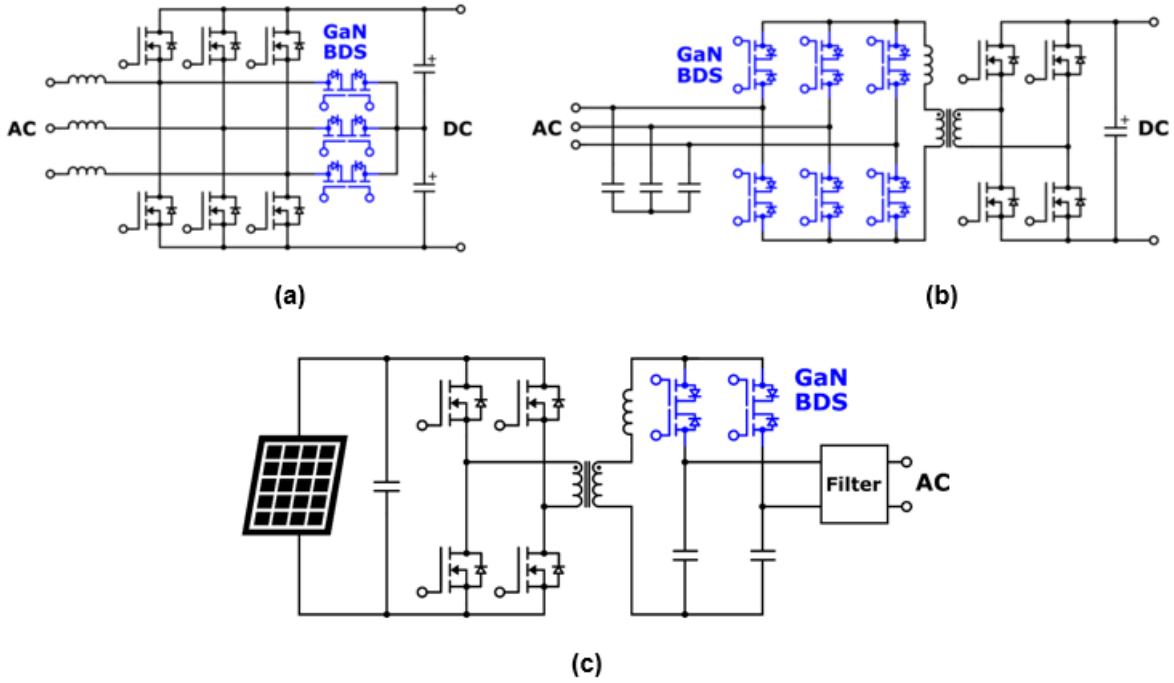


Figure 1. BDS Application Topologies: (a) Vienna Rectifier; (b) 3-Phase Matrix Converter; (c) Cycloconverter

2. BDS GaN Evaluation Board Functionality

The BDS evaluation board is designed to demonstrate the performance of the 650V TP65B110HRU GaN Bi-Directional Switch (BDS) in a half-bridge configuration. Each BDS device provides two source terminals (S1 and S2), two gate terminals (G1 and G2), and dedicated Kelvin source terminals (KS1 and KS2) to support higher speed and more precise gate drive operation. The half-bridge consists of two BDS TOLT devices with an inductive load connected at the output.

The RTDACHB0000RS-MF-1 is controlled by the Renesas R5F526TAAGFL#50 MCU which is programmed to deliver a 50% duty cycle PWM signal at 400kHz during AC operation. As shown in Figure 2, the board includes two primary input connections: the AC input (J3) and the auxiliary power input (CONN3).

An output measurement node is provided across capacitor C71 allowing users to observe the buck step-down conversion from 230VAC to approximately 115VAC. The output is not intended for resistive load operation.

Additionally, an on-board selector switch enables the choice between the internal PWM generator and an external PWM source. In external PWM mode, four independent PWM signals may be applied directly to the gate driver inputs through the straight pin header. In this configuration, the user is responsible for managing dead time and ensuring proper synchronization with the AC input voltage.

2.1 Quick Start Guide

Turn ON Operation:

1. Connect and Supply 12V Aux to CON3.
   a. Verify Positive is connected to 12V, Negative is connected to GND.
2. Verify that SW is set to OB_PWM.
3. Verify that JP1 is shorted.
4. Verify that D6 is blinking.
   a. D4 should remain on as it is the V_{CC} verification.
5. Connect AC power supply to J3 INPUT.
6. Set AC power supply to 230VAC at 50Hz.
7. Turn on AC power supply.
   a. Connect High Voltage Differential probe at TP11+TP12 for V_{SS} of Q2 (High-side BDS device).
   b. Connect High Voltage Differential probe at TP12+TP13 for V_{SS} of Q3 (Low-side BDS device).

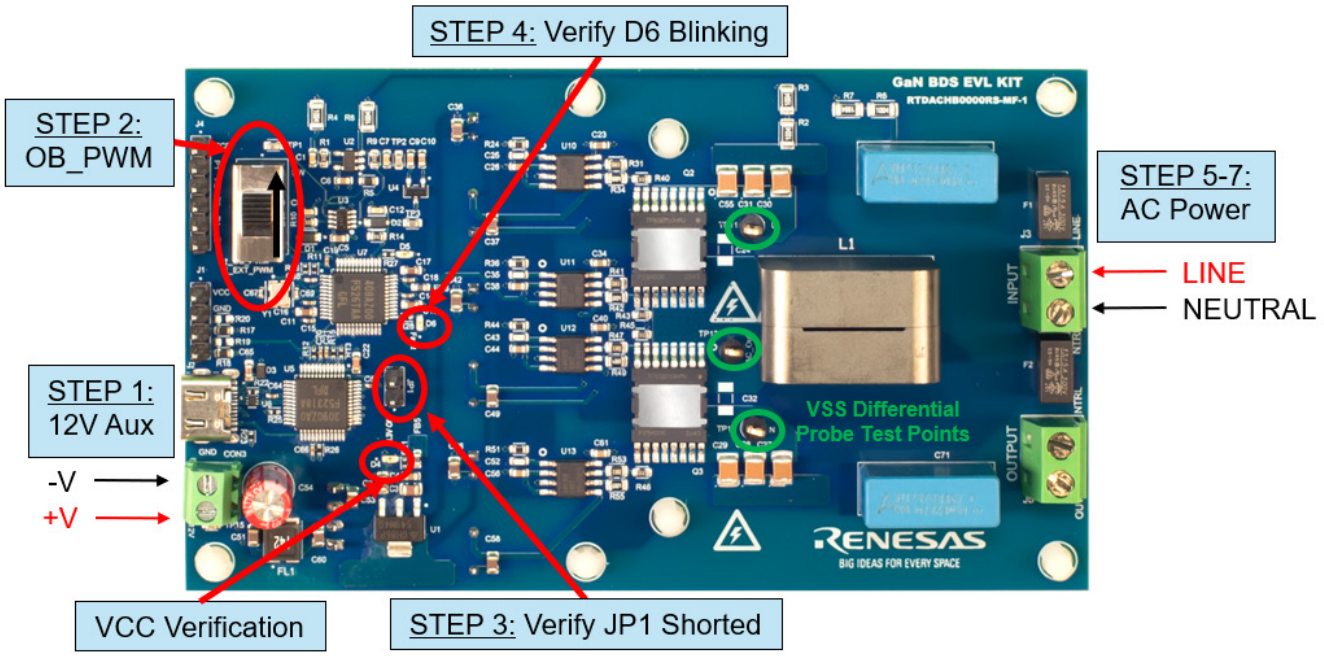


Figure 2. RTDACHB0000RS-MF-1 Evaluation Board – Turn ON Operation

Turn OFF Operation:

1. Turn off AC power supply
2. Turn off Aux power supply

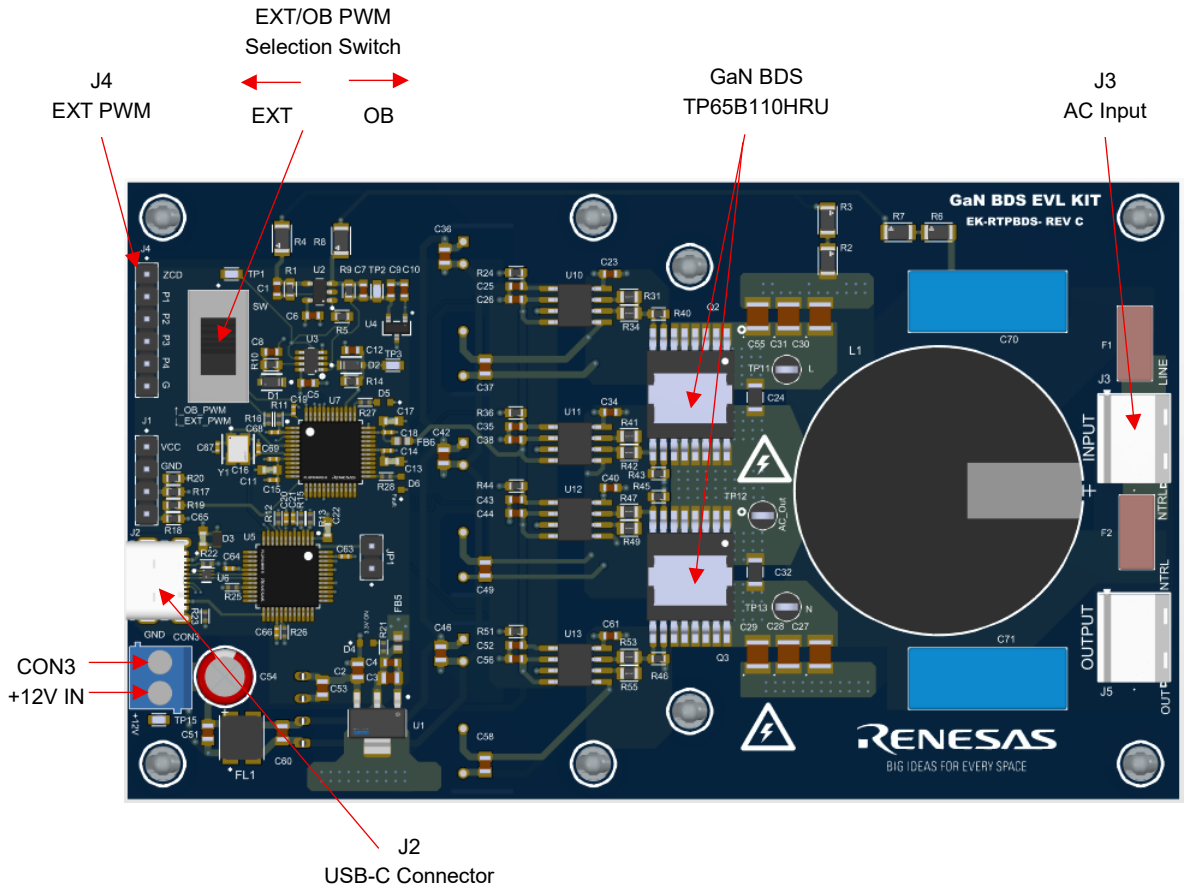


Figure 3. RTDACHB0000RS-MF-1 Evaluation Board – Top View

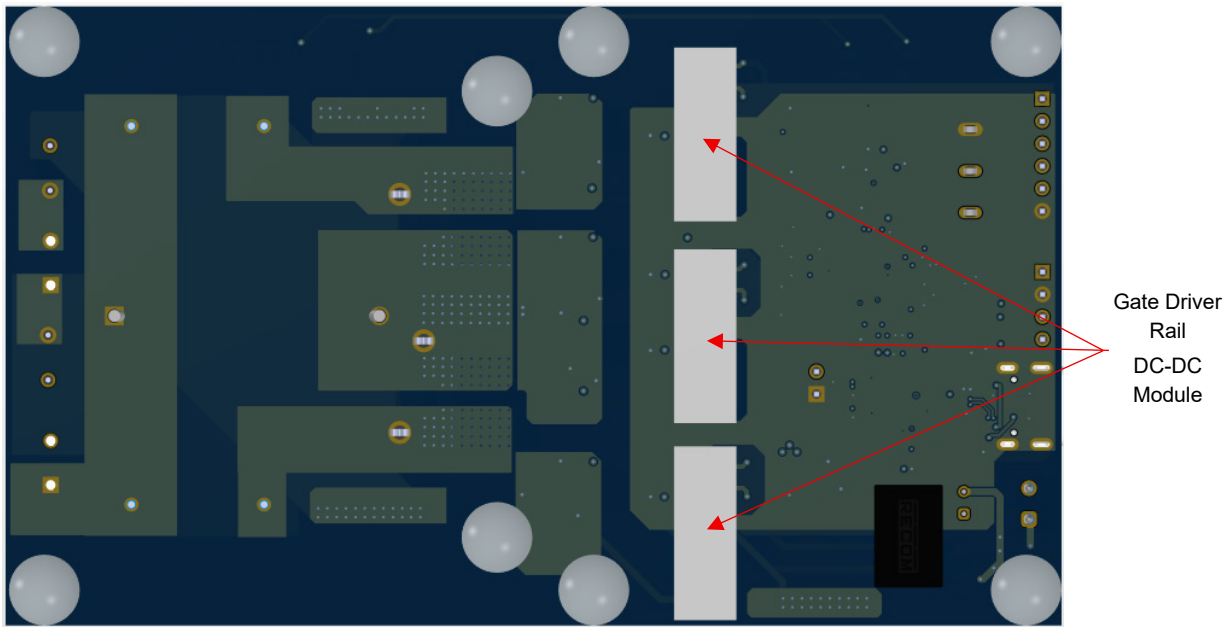


Figure 4. RTDACHB0000RS-MF-1 Evaluation Board – Bottom View

Table 1. BDS GaN Evaluation Board Key Specifications

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
RMS Value of AC Input Voltage	-	80	-	250	V
AC Line Frequency	-	45	-	65	HZ
Switching Frequency	-	-	400	-	kHz
Bias Supply	-	10.8	12	13.2	V
External 4XPWM CON1		0	3.3	3.3	V
V_{IH} (Logic-high input threshold)	-	2	-	-	V
V_{IL} (Logi- low input threshold)	-	-	-	0.8	V
V_{IH} (Logic-high input threshold)	-	3	3.3	4	V
V_{IL} (Logic-low input threshold)	-	-	-	0.8	V

Table 2. BDS GaN Evaluation Board – Key Components and Features

Part Number	Key Features
TP65B110HRU	D-Mode Cascode GaN technology for easy drive, Vth = 3.0V for normally-off operation, TOLT package for enhanced thermal performance with 110mΩ (typical) $R_{DS,ON}$
ISL28134FHZ-T7	Ultra Low Noise, Low drift Precision Op AMP.
ISL21010CFH315Z-T7A	V-Ref Precision 1.5V 25mA 3-Pin SOT-23 T/R
R5F52318ADFL	32-bit Microcontrollers – MCU 32BIT MCU RX231 128K/32K QFP48
R5F526TAAGFL#50	32-bit Microcontroller Optimized for Dual-Motor and PFC Control

3. Schematic Diagrams

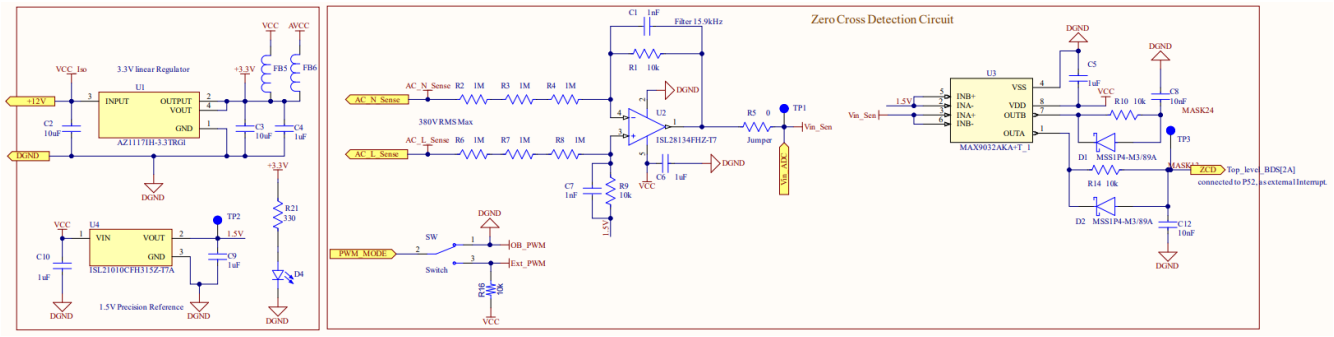


Figure 5. Zero Cross Detection Circuit

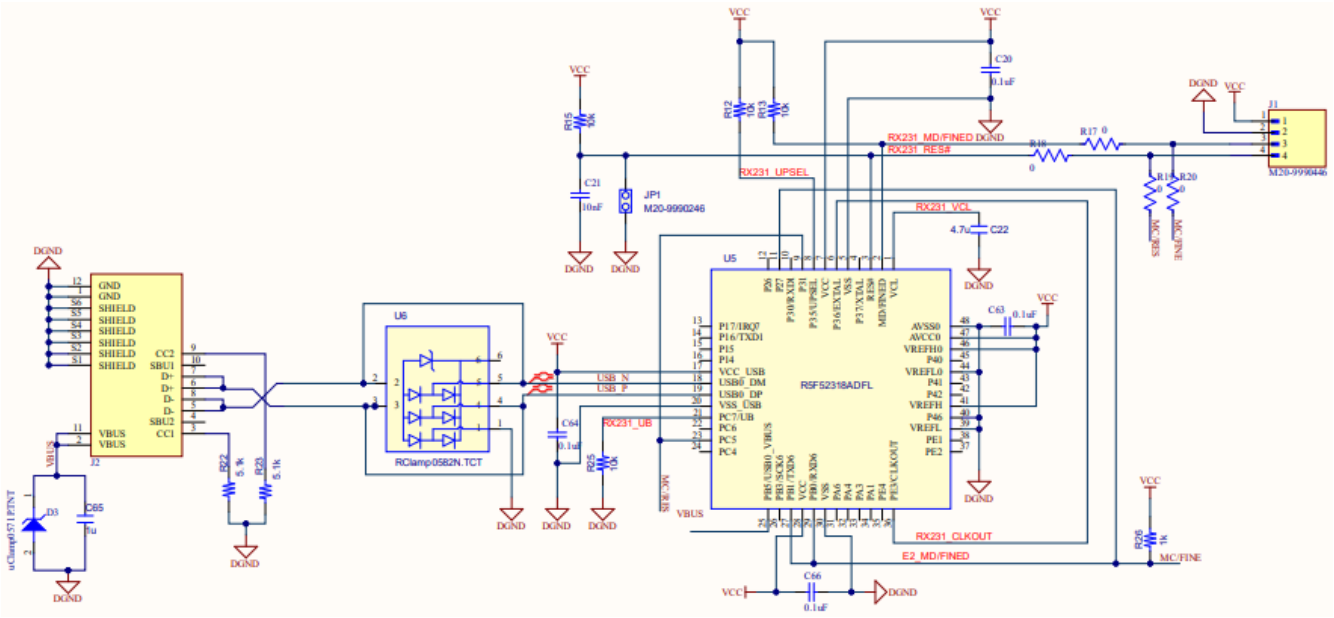


Figure 6. R5F52318ADFL MCU for Programming

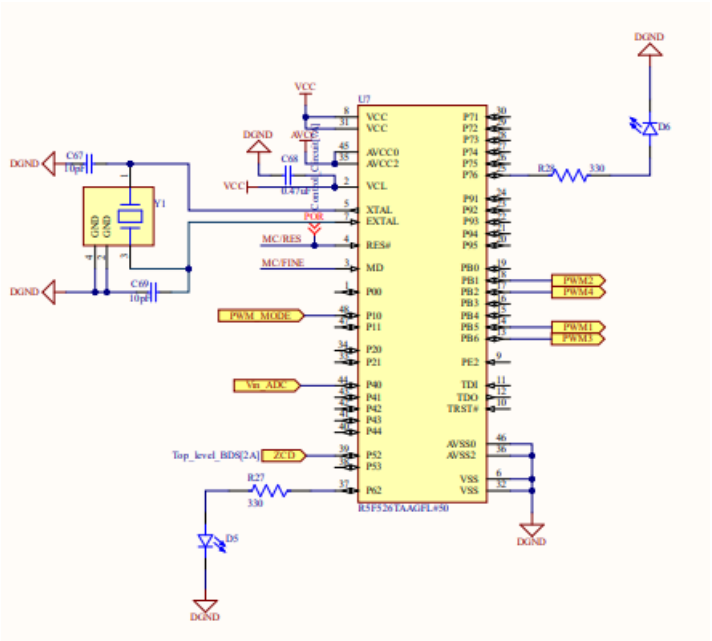


Figure 7. R5F526TAAGFL#50 for Generating PWM and Control Operations

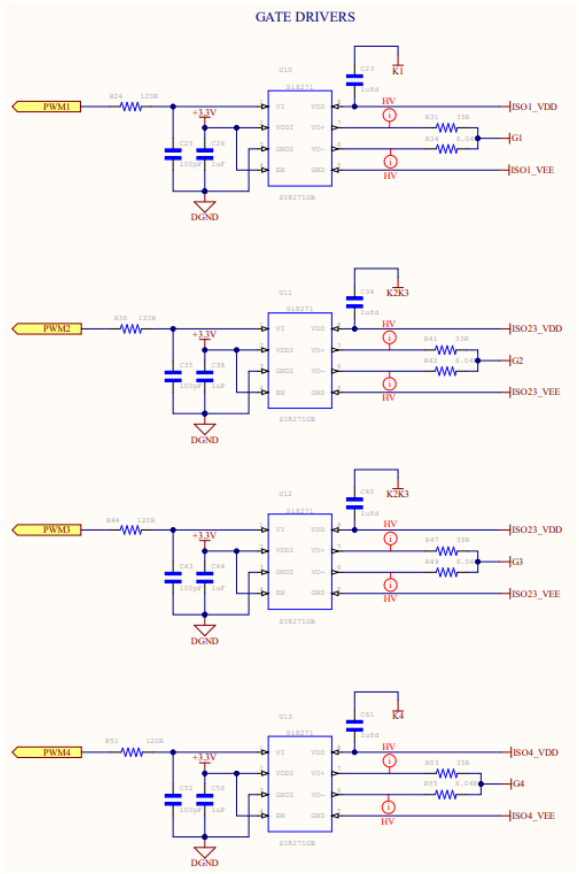


Figure 8. Gate Driver Circuitry

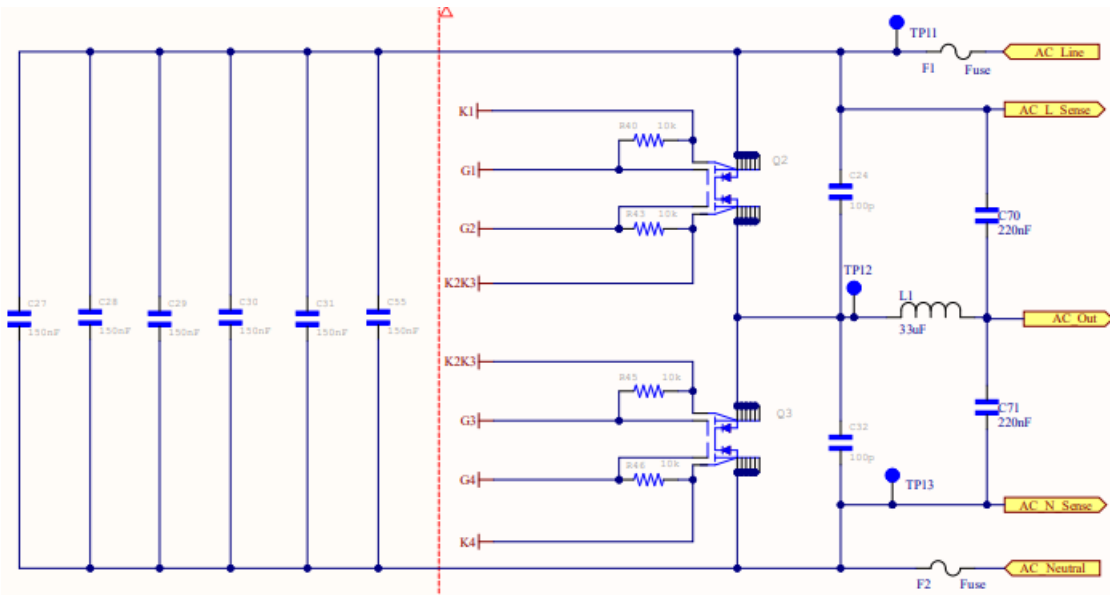


Figure 9. BDS Devices and Inductive Load with AC Input

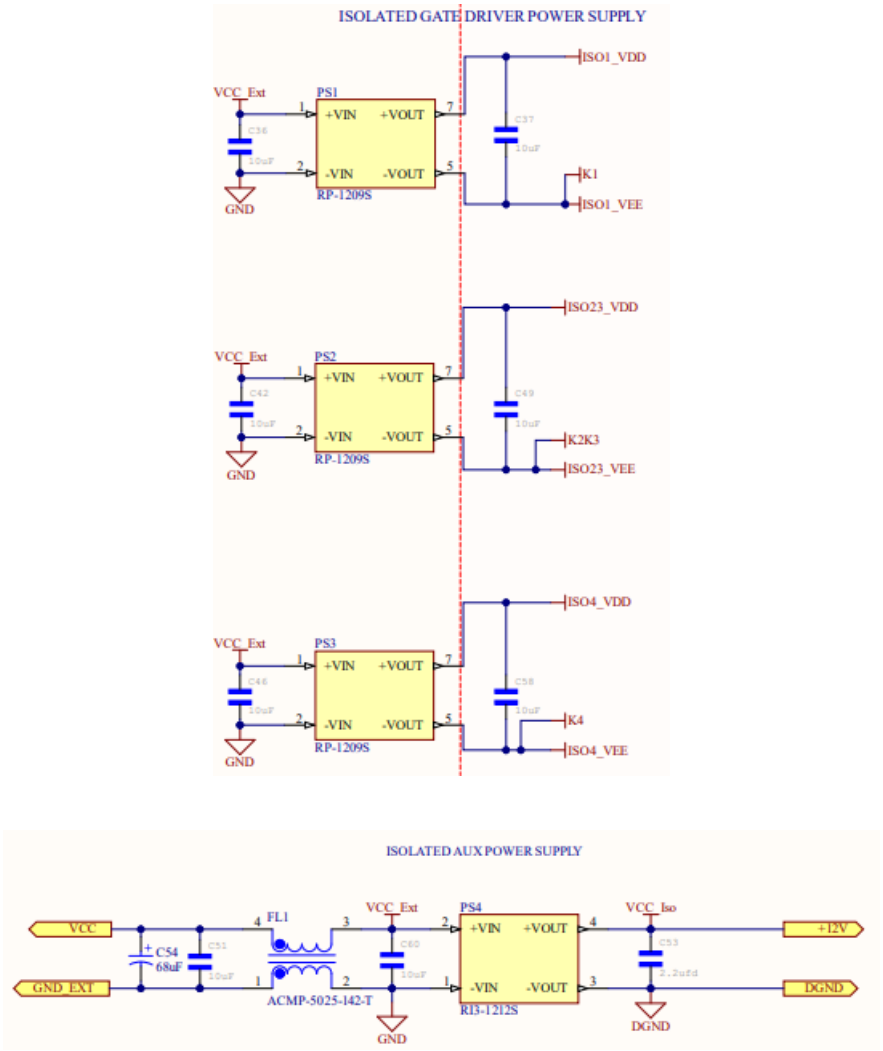


Figure 10. Power Supplies

4. Schematic Descriptions

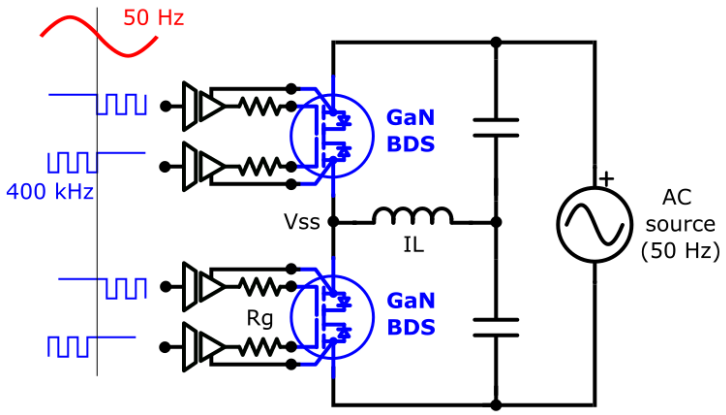


Figure 11. Switching Pattern of GaN BDS Half-Bridge

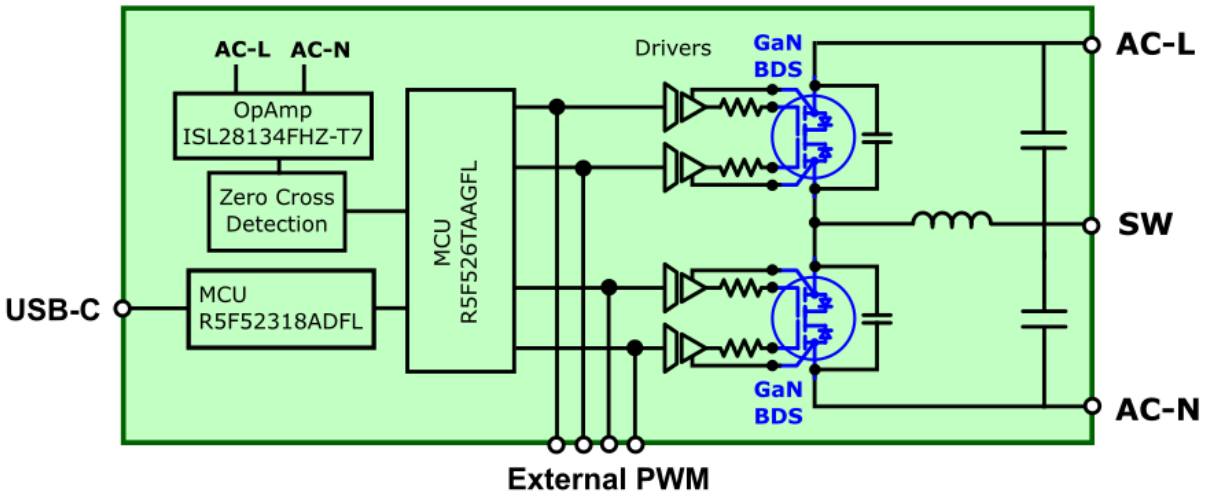


Figure 12. Functional Block Diagram

4.1 Bias Supply

An external 12V ±1.2V supply is required to power the BDS evaluation board, connected to CON3 as shown in Figure 12. The DC-DC module converts the input to an isolated 12V rail, which is then stepped down to 3.3V using a fixed-voltage linear regulator to power the board's components. The 12V rail is also supplied to the gate driver power supplies to generate a 9V output for generating the 0–9V gate to source signals for the BDS devices.

4.2 Zero Cross Detection Circuit

The AC input voltage is differentially sensed and level-shifted to +1.5V using the Renesas low-offset op-amp ISL28134FHZ-T7 (U2). The differential amplifier provides a high input impedance of 3MΩ between the AC input and DGND. A 1.5V reference is generated by the on-board Renesas precision reference IC ISL21010CFH315Z-T7A (U4). The level-shifted signal is compared against this reference to detect the positive and negative half-cycles of the input, respectively.

4.3 On-Board PWM Generator

The on-board PWM generator is powered by the Renesas R5F526TAAGFL#50 (U7). The four PWM signals are generated based on the zero cross detection output. As seen in Figure 11, PWM2 and PWM4 signals are supplied to the gate drivers during the AC positive cycle while PWM1 and PWM3 signals are supplied to the gate drivers during the negative AC cycle.

4.4 External PWM Input

In addition to the on-board PWM generator, the BDS evaluation board provides the option to drive the BDS GaN devices using an external PWM source. The selection between the internal and external PWM inputs is made using switch SW, with the switch positions indicated on the PCB and shown in Figure 3:

- **SW selector on the left**: EXT_PWM is selected

When the external PWM option is selected, the on-board PWM is disconnected from the digital circuitry and the external input is enabled.

Four independent PWM signals along with their corresponding ground connections can be directly supplied to the gate drivers through the 5-pin straight header (J4), bypassing the internal gate conditioning circuitry. In this configuration, the user must handle dead time insertion and ensure synchronization with the input voltage.

4.5 Gate Driver Circuit

The BDS GaN devices are driven by four isolated gate drivers powered by isolated DC-DC that convert a 12V input to 9V isolated output. The gate driver utilizes a pulse from 0V to 9V to generate the gate to source signals. The threshold voltage of the BDS device is 3.3V.

5. Switching Behavior

5.1 Current Direction

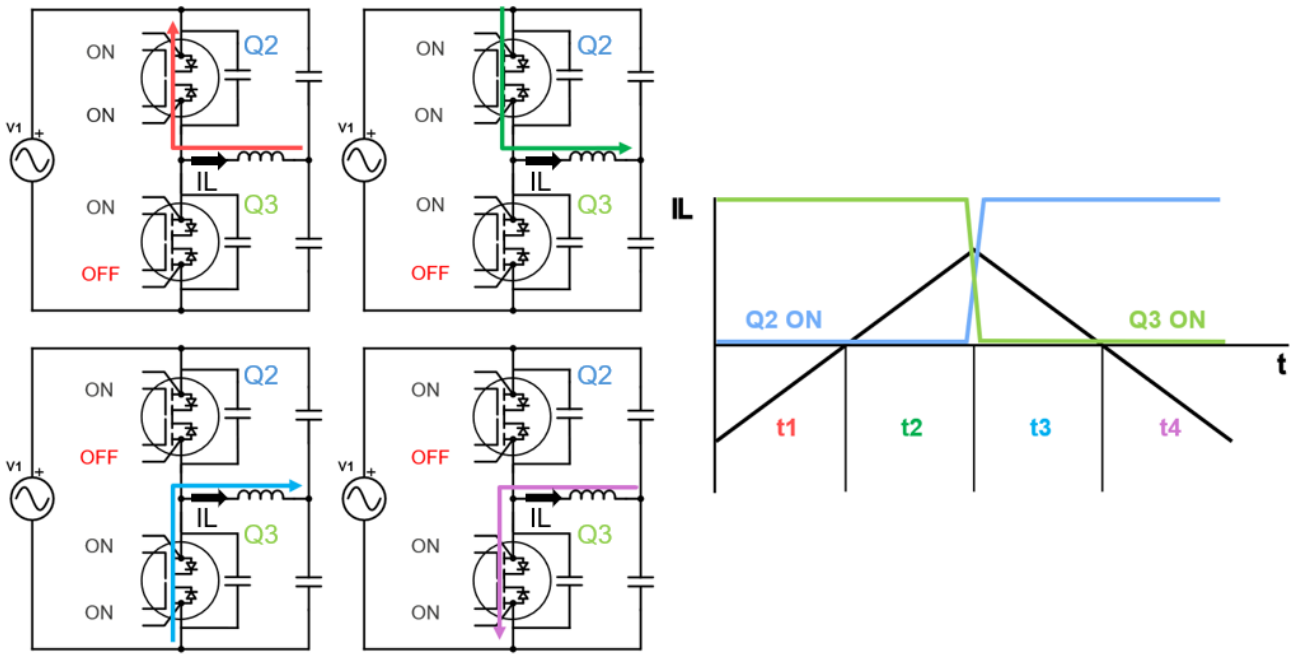


Figure 13. Current Direction during AC Positive Cycle

To provide a clearer understanding of the board's operation, it is useful to review the current flow during the various intervals of the switching cycle. During the positive half of the AC waveform, the source-to-source voltage (V_{SS}) behavior of devices Q2 and Q3 can be examined in relation to the inductor current, as illustrated in Figure 13. In the first interval (t1), device Q2 is conducting and the current flows through the device in the negative direction relative to the measurement reference. While Q2 remains on, the inductor current transitions from negative to positive, establishing the conditions for the subsequent switching intervals.

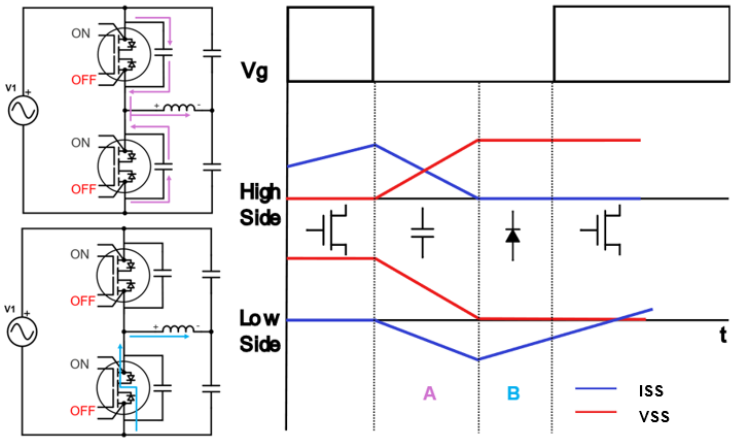


Figure 14. V_{SS} and I_{SS} of High Side and Low Side during Dead Time

As the inductor current reaches its peak positive value, conduction transitions from device Q2 to device Q3. The dead time behavior associated with this transition is illustrated in Figure 14 and can be divided into two distinct intervals: one governed by the charging and discharging of the output capacitors, and another involving the brief conduction of the reverse recovery diode. In the first interval, the output capacitor of Q2 charges while the output capacitor of Q3 discharges. After these capacitors complete their respective transitions, a small leakage current flows through the diode until the current flows into the FET channel. This diode conduction interval results in only minimal energy loss. Under zero voltage switching (ZVS) conditions, turn on losses are effectively eliminated resulting in minimal switching losses. Once the dead time concludes, current begins flowing through Q3 in either direction, corresponding to intervals t3 and t4.

5.2 Soft Switching Proof

To validate that the Renesas BDS devices operate under true zero voltage switching (ZVS), both the V_{GS} (gate-to-source voltage) and V_{SS} are probed during the positive and negative phases of the AC cycle. During the positive cycle, gate signals G2K2K3 and G4K4 are active, while G1K1 and G3K2K3 switch during the negative cycle. As observed during the turn on intervals, the V_{SS} of each device consistently reaches 0V prior to the corresponding V_{GS} exceeding the device's 3V threshold voltage. This timing relationship, confirmed in the waveforms of Figure 15(b), demonstrates proper ZVS operation.

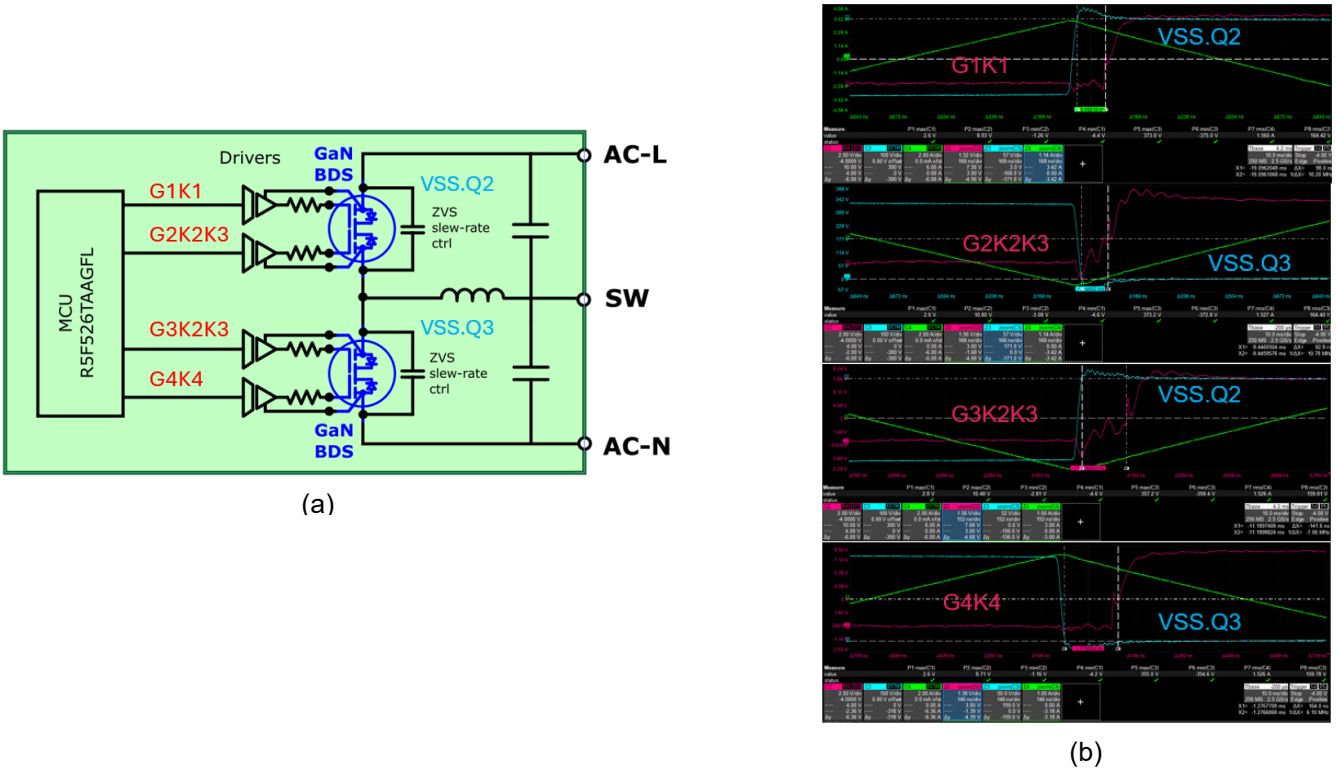


Figure 15. (a) Reference Block Diagram; (b) Soft Switching Proof of BDS Devices

5.3 ZVS Capacitor Slew Rate Control

To reduce the device's slew rate in soft switching operation, a designer may introduce an appropriate high voltage capacitor across the V_{SS} terminals of each BDS device. When populated at positions C24 and C32, this additional capacitance slows down the dv/dt of the device. In the demonstrated example, a 630V, 100pF capacitor was used, resulting in a reduction of the V_{SS} transition rate from approximately 12V/ns to 6V/ns, as illustrated in the corresponding measurement data.

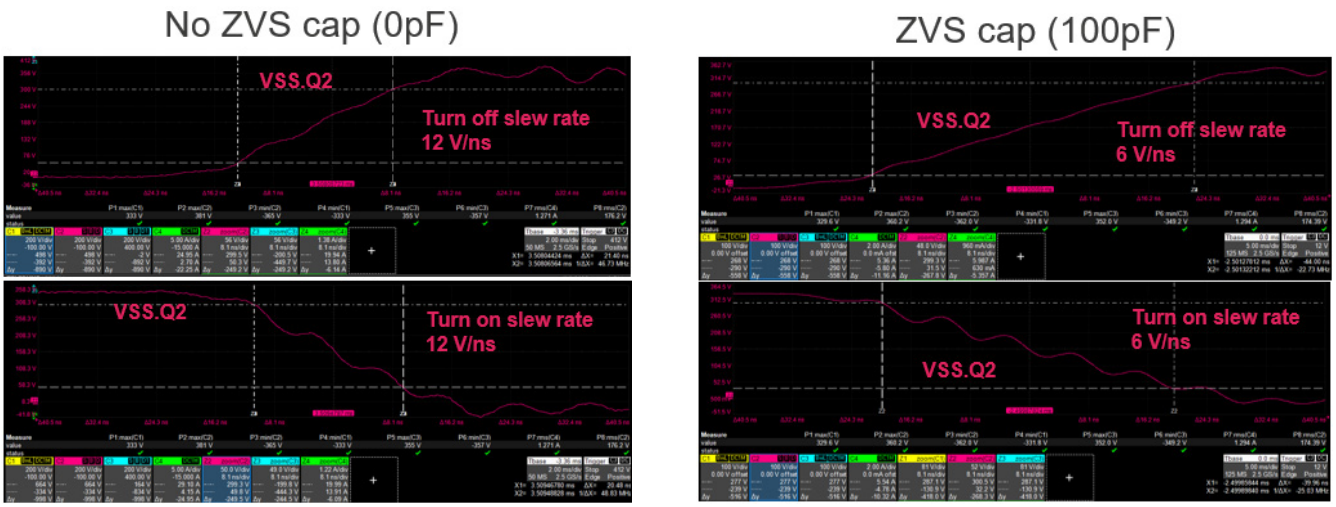


Figure 16. ZVS Capacitor Slew Rate Control

6. Test Results

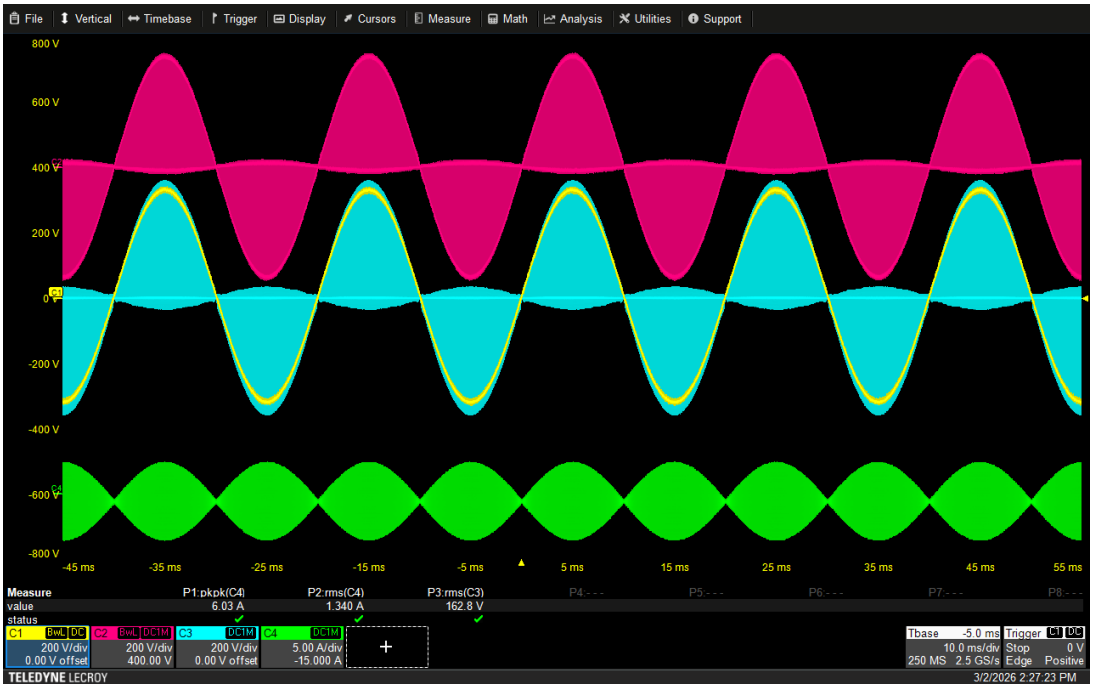


Figure 17. CH1(Yellow)-VAC, CH2(Red)-Q2.VSS, CH3(Blue)-Q3.VSS, CH4(Green)-IL

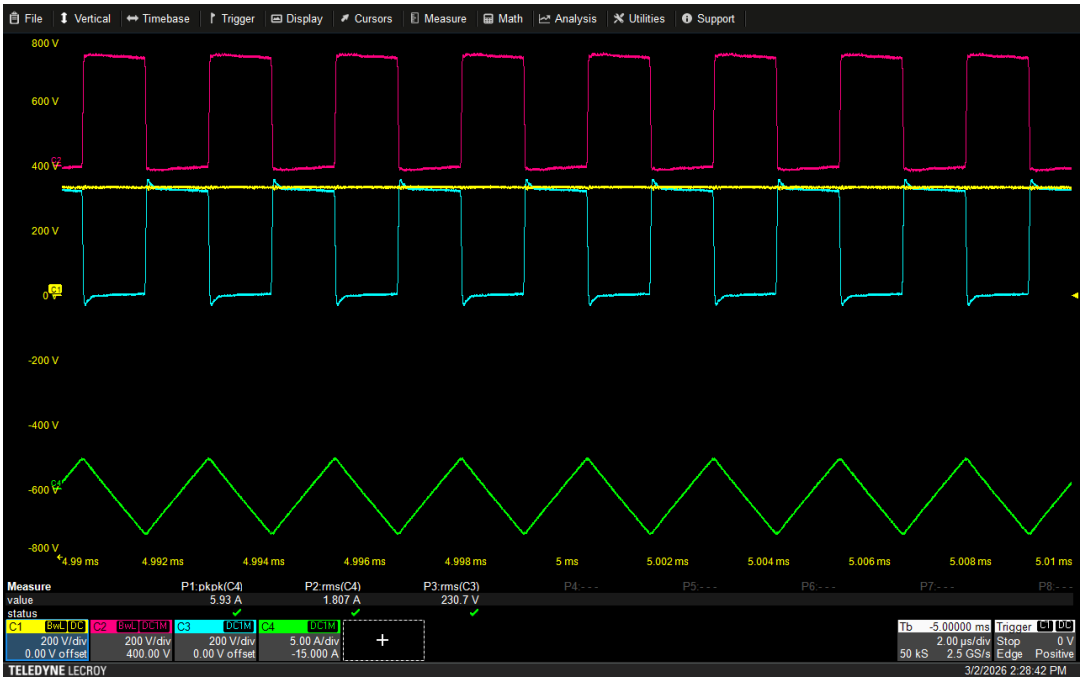


Figure 18. CH1(Yellow)-VAC, CH2(Red)-Q2.VSS, CH3(Blue)-Q3.VSS, CH4(Green)-IL During AC Positive Cycle

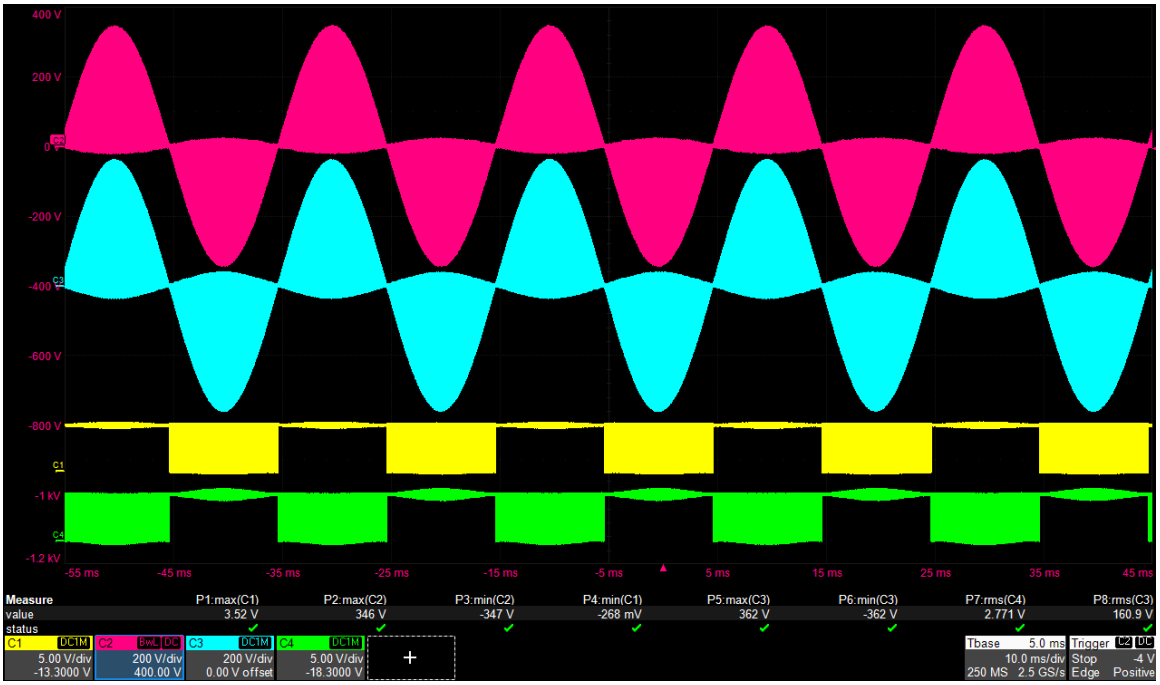


Figure 19. CH1(Yellow)-PWM1, CH2(Red)-Q2.VSS, CH3(Blue)-Q3.VSS, CH4(Green)-PWM2

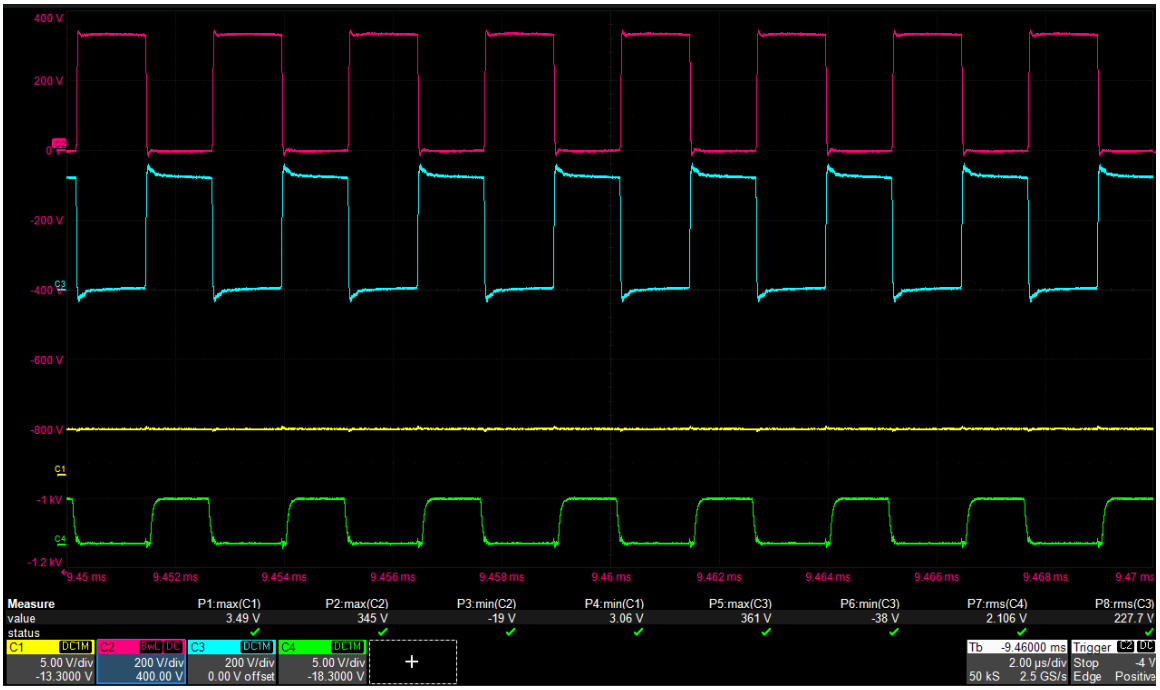


Figure 20. CH1(Yellow)-PWM1, CH2(Red)-Q2.VSS, CH3(Blue)-Q3.VSS, CH4(Green)-PWM2 During AC Positive Cycle

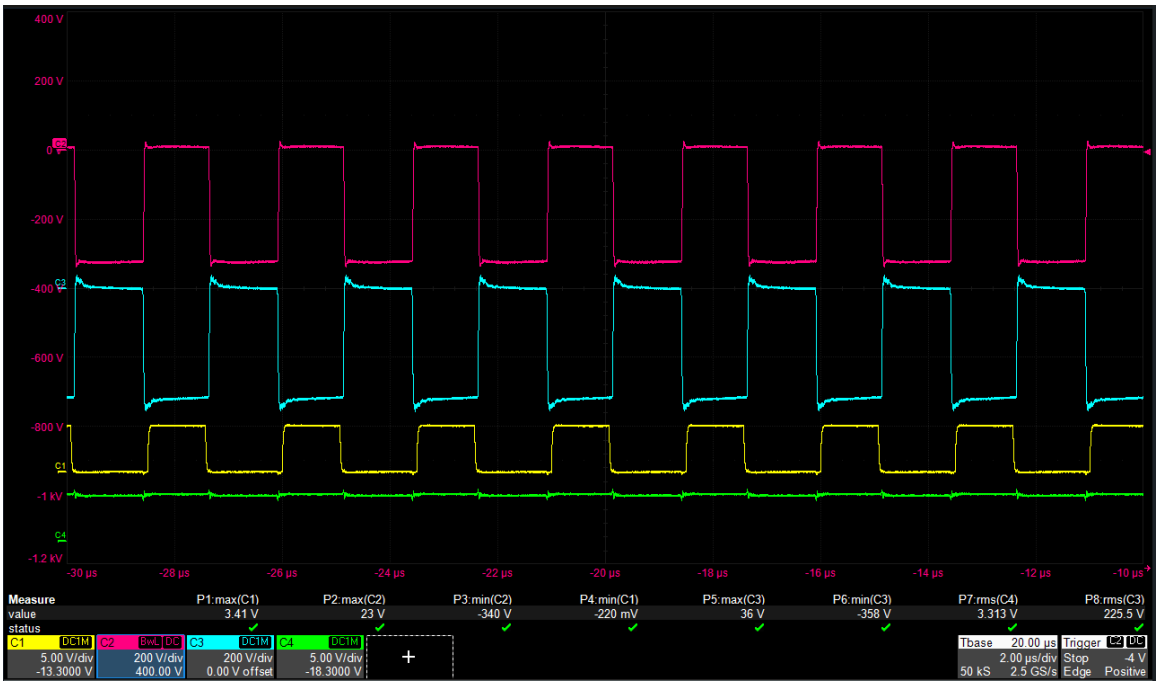


Figure 21. CH1(Yellow)-PWM1, CH2(Red)-Q2.VSS, CH3(Blue)-Q3.VSS, CH4(Green)-PWM2 During AC Negative Cycle

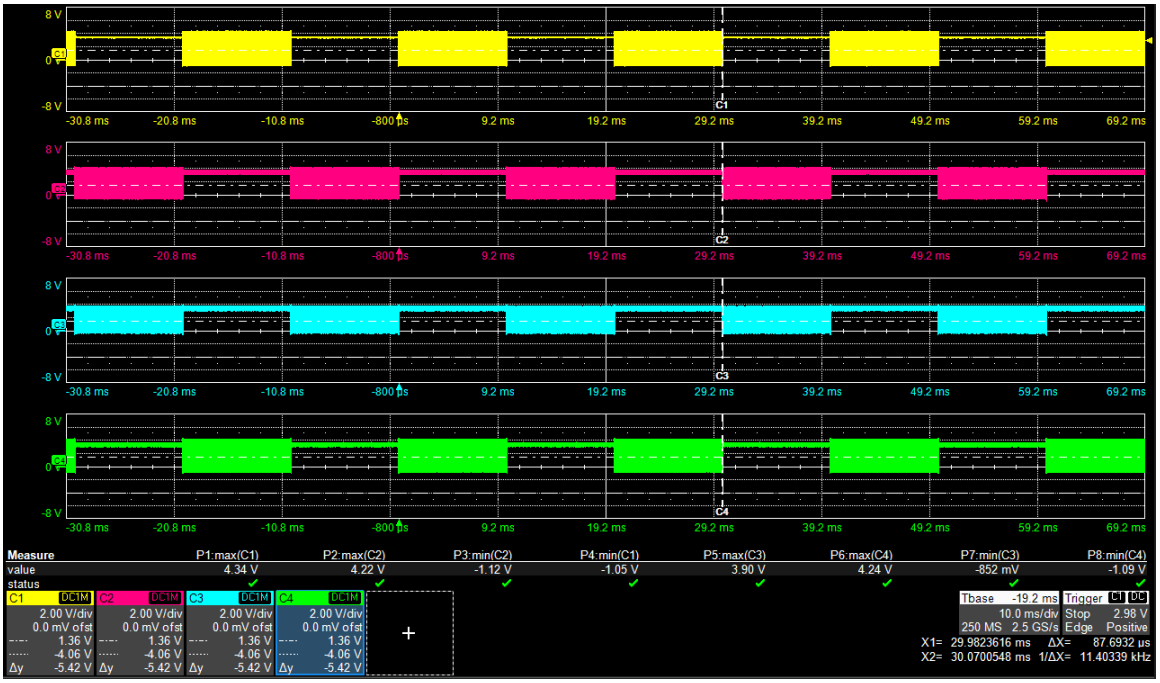


Figure 22. P1-P4 on J4, PWM Signals Supplying Gate Drivers while AC Voltage Supplied

Test Conditions:

VACIN: 230VAC

FGRID: 50Hz

Duty = 50%

FSW = 400kHz

L = 33µH

Operating Conditions: Room temperature, no airflow, no heatsink

7. Drive Circuit Configuration

Renesas High-Voltage BDS GaN devices are high-performance, normally-off devices that do not need a negative gate drive voltage like other wideband gap switch technologies. This makes it easier to implement a simple dual output gate drive circuit with gate resistors for each BDS device.

Figure 23 shows the common drive circuit configuration that can be implemented with a dual output gate driver which provides separate source and sink outputs. This allows the use of dedicated RGON and RGOFF for the respective turn on and turn off operation of gates G1 and G2.

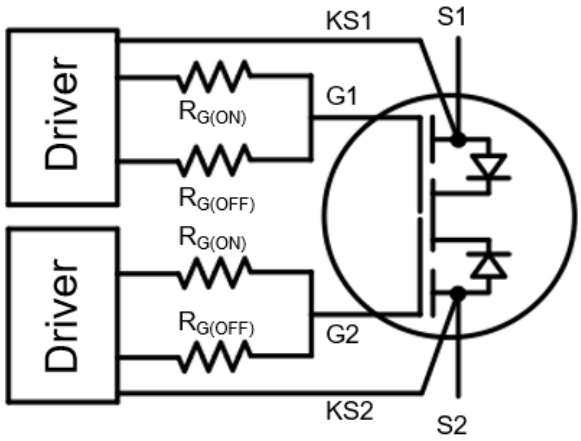


Figure 23. Gate Drive Configuration of Single BDS Device

8. PCB Layout for Low Inductance Design

Due to fast switching nature of GaN devices, minimizing parasitic inductance in the PCB layout is critical to ensuring reliable operation, reducing EMI, and maximizing efficiency. Key strategies include the following:

- Create source shield planes on the layer immediately below the gate driver connected to source or the kelvin source, when available.
- Ensure the source shield plane covers the gate and source terminals (kelvin source if available) and all the gate circuitry components.
- Power loop between high side and low side of a GaN device and the DC bus decoupling capacitor should be as close as possible.
- Use tight component placement and short, wide traces to reduce loop inductance.
- Use a solid ground plane under the half bridge to create a low-inductance return path for switching currents and use flux cancellation techniques.
- Avoid split planes under high-speed switching sections.
- For half-bridge and full-bridge configuration, keep symmetry to balance current paths and reduce EMI.

9. Design Example

9.1 Gate Driver

In Figure 24, the half-bridge topology is implemented using Renesas TP65B110HRU BDS GaN devices. In this configuration, two devices – Q2 (high side) and Q3 (low side) – form the half bridge stage. To drive each BDS device, two dual-output gate drivers are employed, allowing the use of separate turn-on and turn-off resistors to optimize switching behavior.

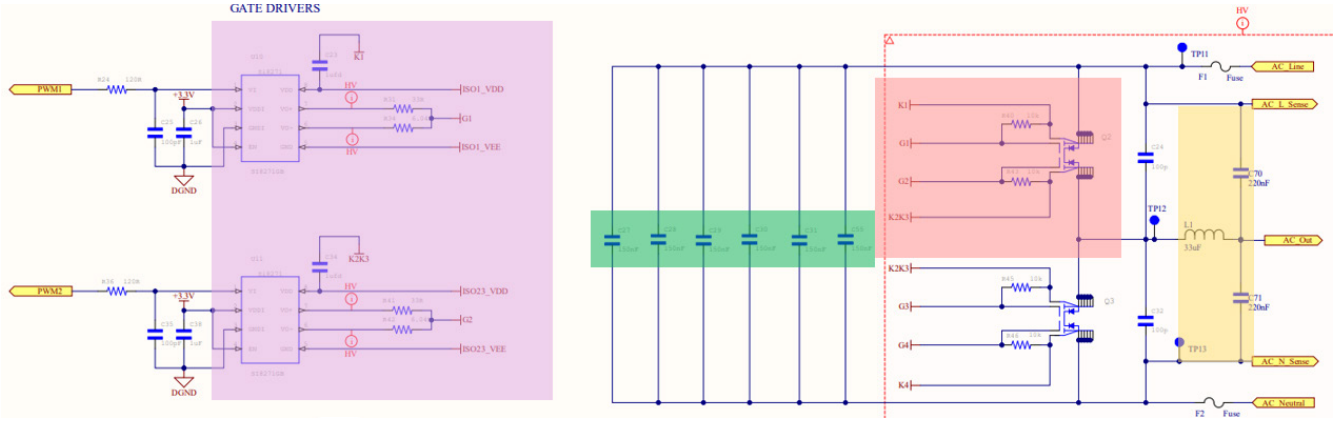


Figure 24. Half-Bridge Schematic

9.2 Critical Component Placement

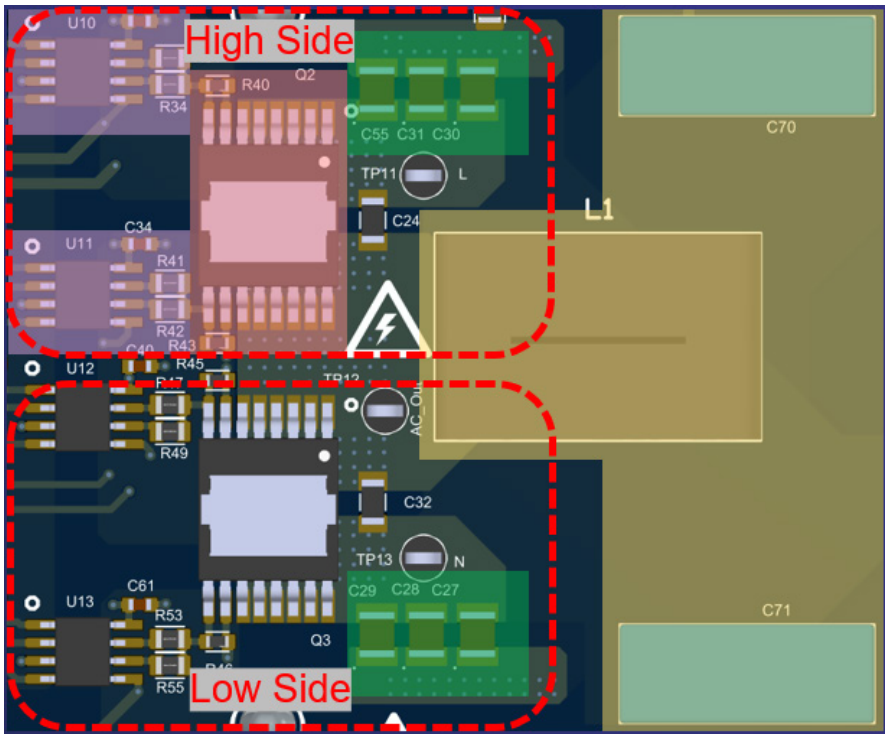


Figure 25. Half-Bridge Layout

In a well-designed half bridge configuration, careful component placement is essential. By keeping the gate drive and power loop components close together and compact, designers can minimize unwanted parasitic inductance and improve overall circuit performance. Highlighting key elements such as gate drivers (purple), BDS devices (red), decoupling capacitors (green), and inductive load (yellow) helps ensure that critical paths are optimized for low inductance and efficient operation.

9.3 Layout Considerations

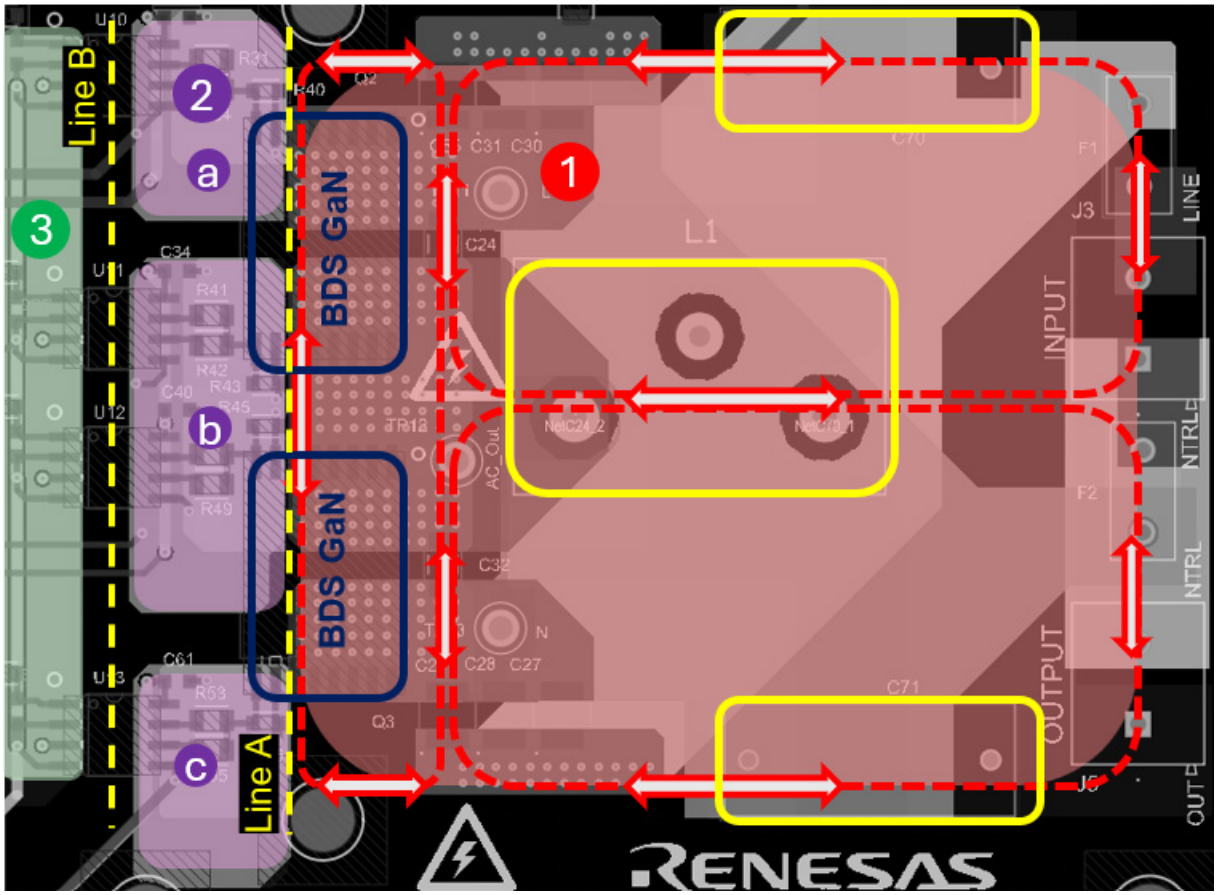


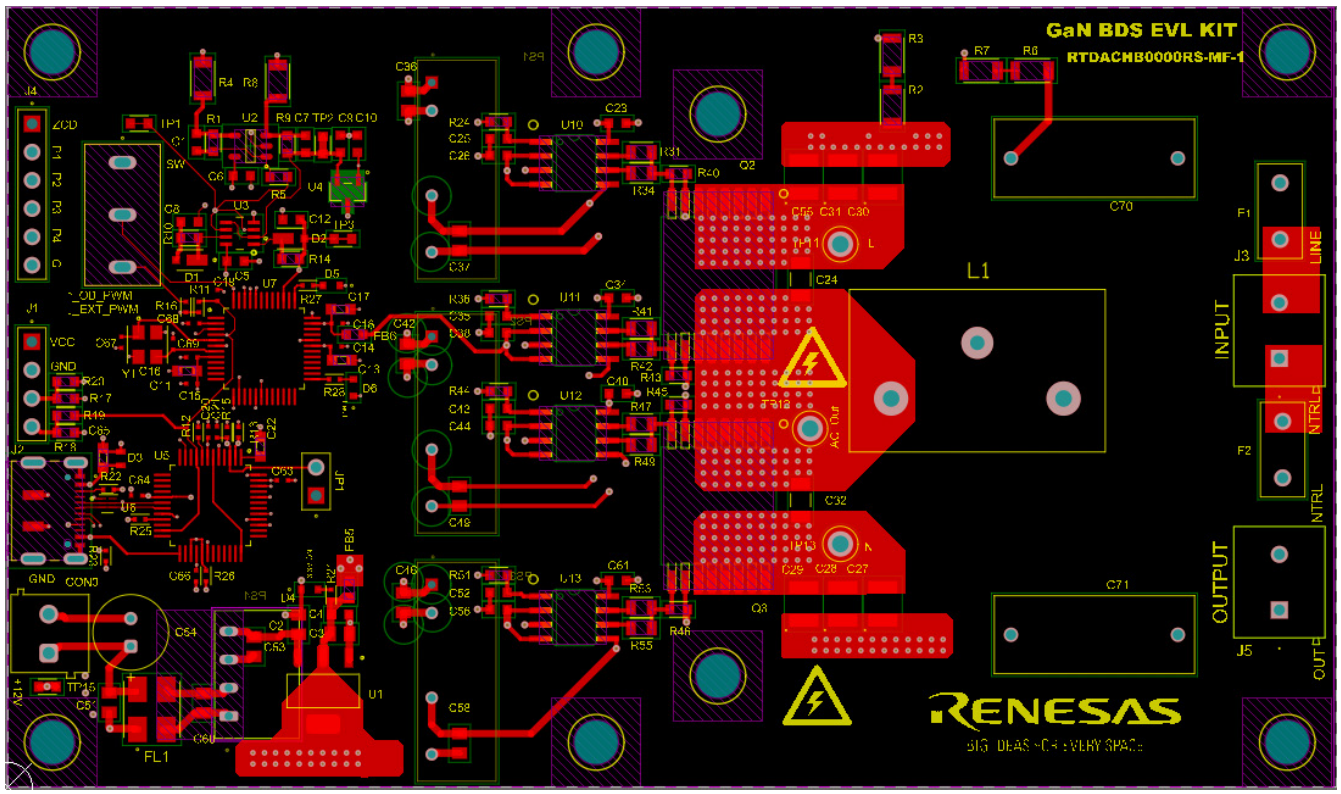
Figure 26. Half-Bridge Layout Description

Figure 26 illustrates key PCB layout placement techniques. A primary design practice is maintaining a compact power loop, shown by the red dotted outline. This loop is intentionally kept small and reasonably symmetrical to minimize parasitic inductance, reduce voltage overshoot, and support efficient switching behavior. A solid ground plane, shown in Figure 27(b), is positioned beneath the half bridge and its associated decoupling capacitors to provide a low impedance return path for high di/dt currents.

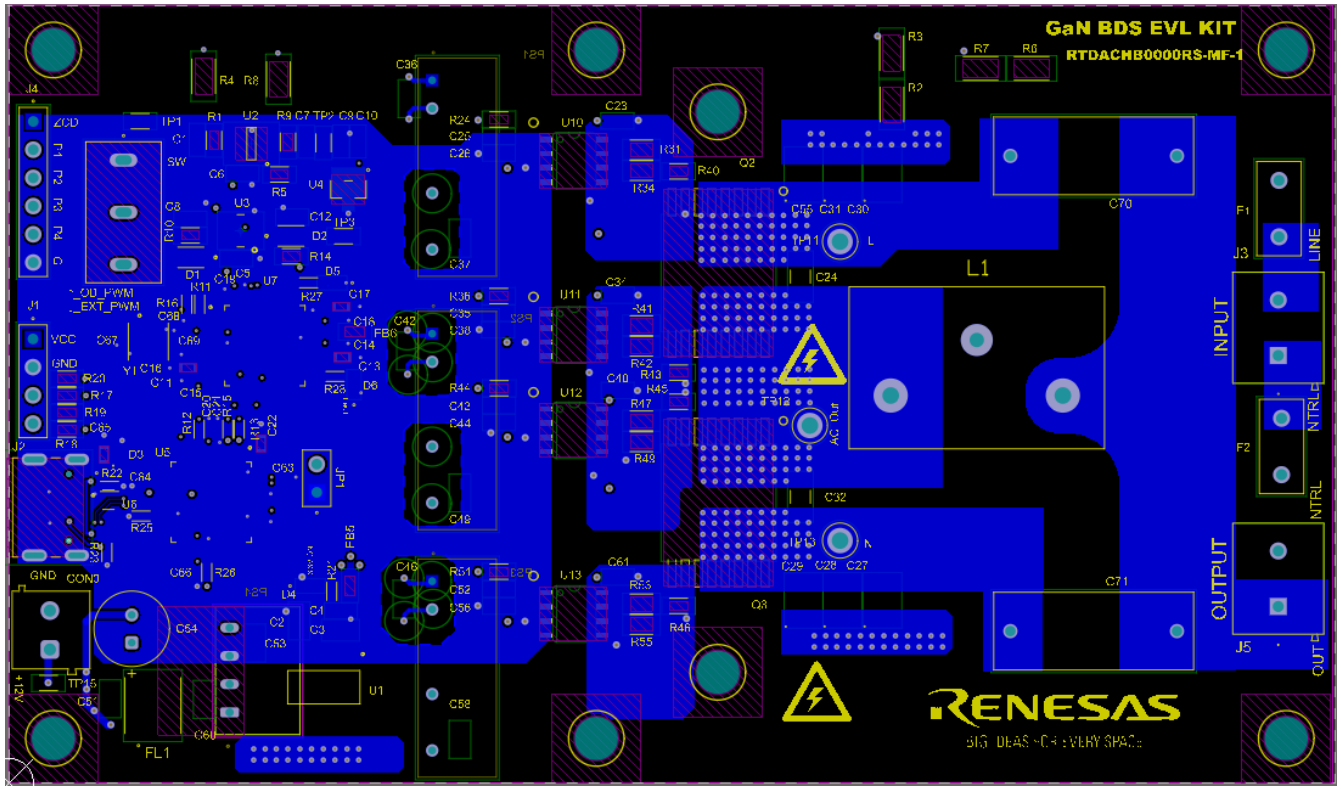
In Figure 26, Line A highlights the separation between the power path (1 Red) and the gate signal return paths (2 Purple). Line B indicates the use of dedicated ground planes for the input side (3 Green) and output side (2 Purple) of the gate driver to maintain signal integrity and ensure proper shielding. The regions labeled (a), (b), and (c) illustrate the intentional segmentation of ground signal traces for the gate drive loops. These design strategies collectively help maintain a low impedance return path, reducing common source inductance, improving signal fidelity, and mitigating electromagnetic interference.

Overall, the PCB layout focuses on minimizing loop areas in both the power and gate drive paths, limiting parasitic effects, and enabling robust, high efficiency performance suitable for high frequency GaN operation.

10. PCB Layout

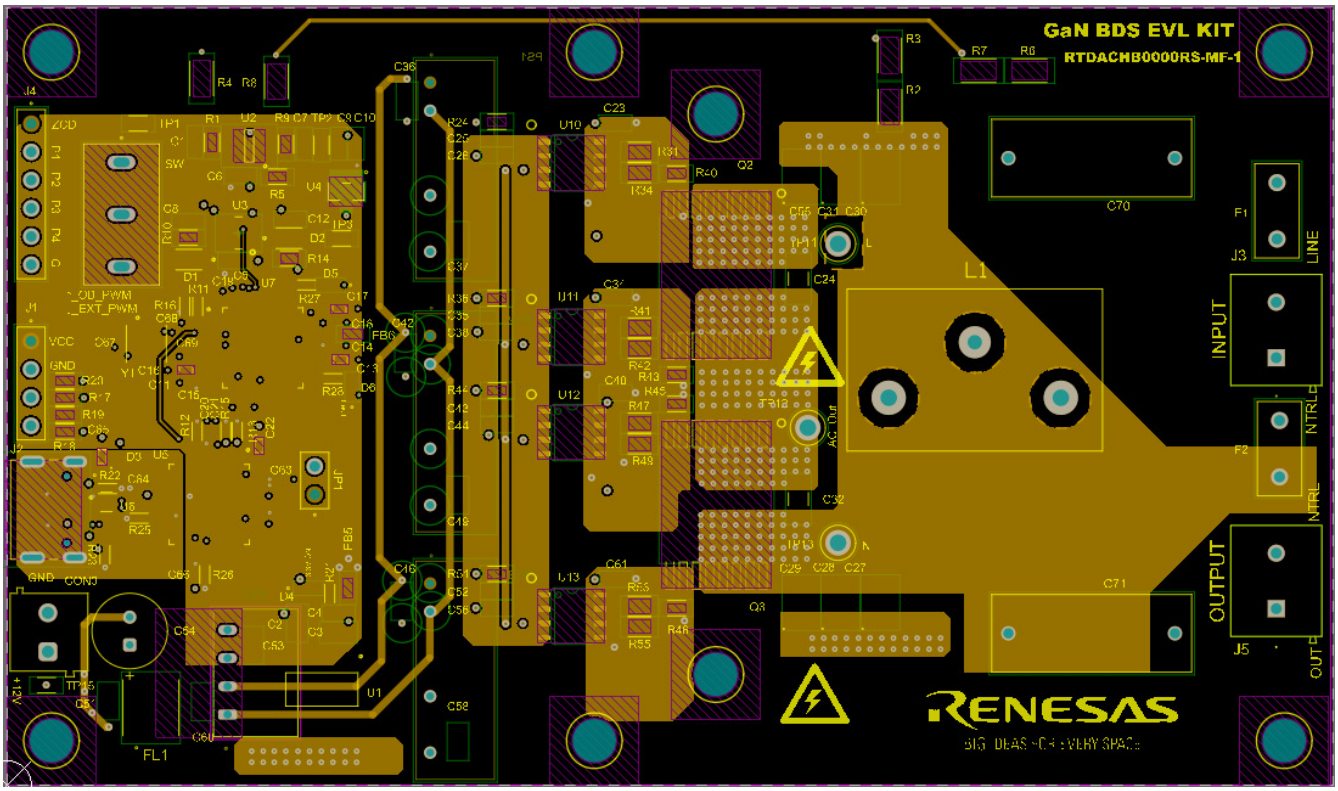


(a)

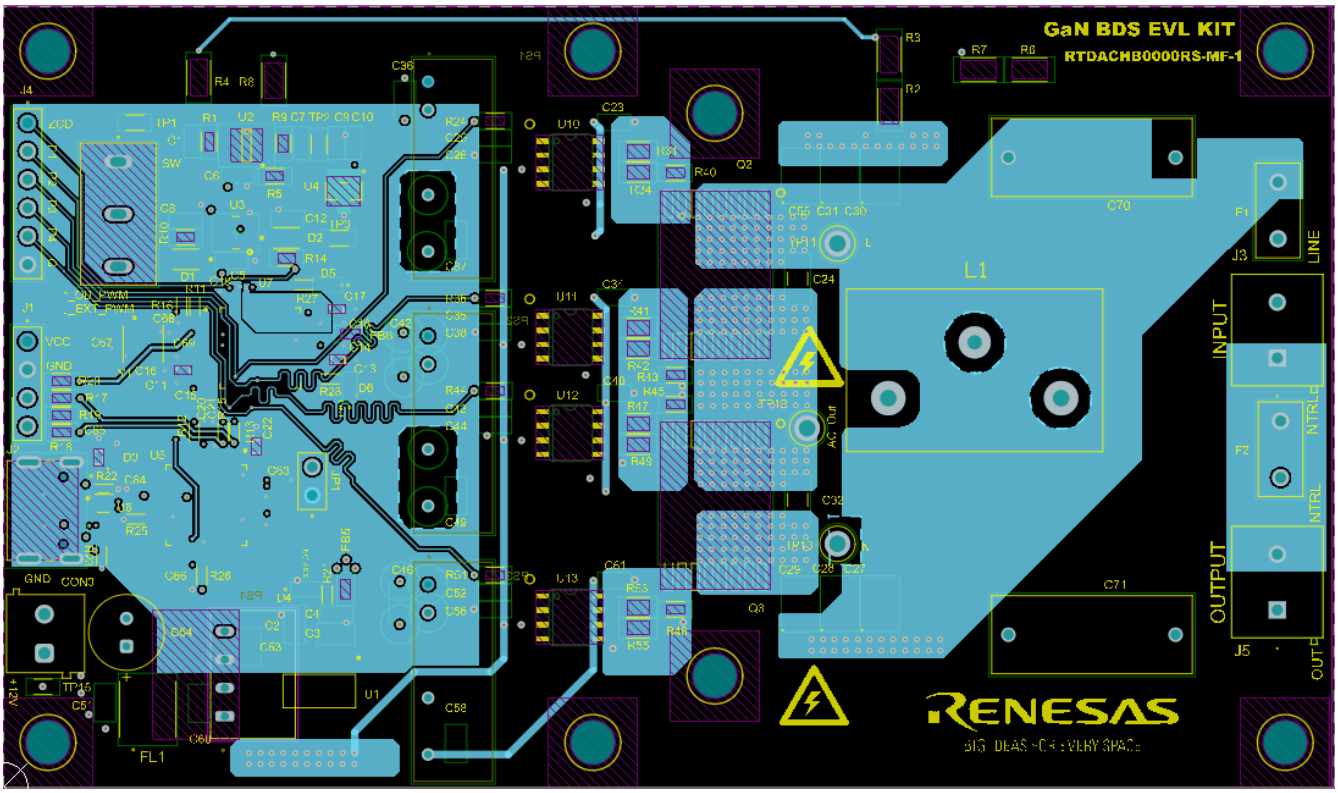


(b)

Figure 27. (a) Layer 1 and (b) Layer 2



(a)



(b)

Figure 28. (a) Layer 2 and (b) Layer 3

11. Thermal Images of BDS Devices

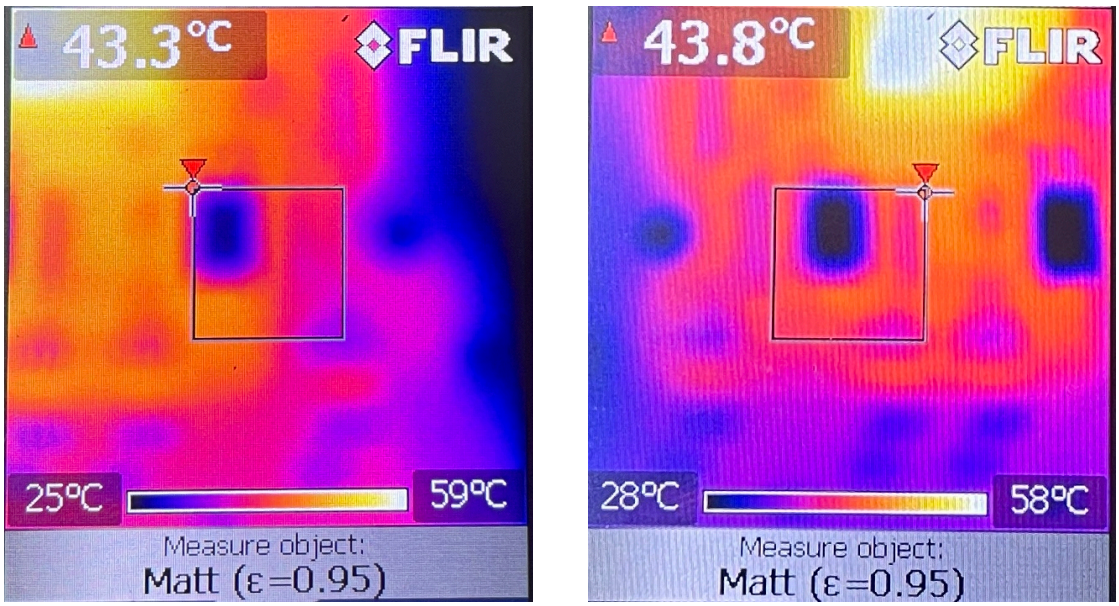


Figure 29. Thermal Images of TP65B110HRU – Low Side (left), High Side (right)

12. Bill of Materials (BOM)

Value	Description	Designator	Quantity	Manufacturer	Part Number
1nF	Capacitor	C1, C7	2	Wurth Elektronik	885012206108
10uF	Capacitor	C2, C3, C36, C37, C42, C46, C49, C51, C58, C60	10	Murata	GRM21BZ71E106KE15K
1uF	Capacitor	C4, C5, C6, C9, C10, C23, C34, C40, C61, C26, C38, C44, C56	13	TDK	C1608X7R1V105K080AC
10nF	Capacitor	C8, C12	2	KEMET	C0603C103M5RACTM
10uF	Capacitor	C11, C13, C17	3	TDK	C1608X7R1A106M080AT
100nF	Capacitor	C14, C15, C16, C18, C20, C63, C64, C66	8	Wurth Elektronik	885012205085
0.01uF	Capacitor	C19, C21	2	Murata	GRT155R71C103KE01D
4.7uF	Capacitor	C22	1	Murata	GMC10X7R475K16NT
100pF	Capacitor	C24, C32	2	Walsin Technologies	1206N101K631CT
100pF	Capacitor	C25, C35, C43, C52	4	Wurth Elektronik	885012206102
150nF	Capacitor	C27, C28, C29, C30, C31, C55	6	TDK	CGA6M1X7T2J154K200AC
2.2uF	Capacitor	C53	1	KYOCERA AVX	08053C225KAT2A
68uF	Capacitor	C54	1	Wurth Elektronik	860020473007
1uF	Capacitor	C65	1	Kyocera	0603YC105KAT2A
10pF	Capacitor	C67, C69	2	TDK	CGA2B2C0G1H100D050BA
0.47uF	Capacitor	C68	1	TDK	CGA2B3X7S1A474K050BB
0.22uF	Capacitor	C70, C71	2	EPCOS	B32922C3224K289
Header, 2-Pin	Header, 2-Pin	CON3	1	Wurth Elektronik	691214110002
40V, 1A	Diode	D1, D2	2	Vishay	MSS1P4-M3/89A
15V	Dioe	D3	1	Semtech	UCLAMP0571P.TNT
1.9V	LED	D4, D5, D6	3	Kingbright	APHD1608LCGCK
Fuse	Fuse	F1, F2	2	Eaton	SS-5H-3.15A-APH
120Ohm	Ferrite Bead	FB5, FB6	2	Murata	BLM18AG121SN1D
1.5A, 1.4KOhm	Common Mode Choke	FL1	1	Abracon	ACMP-5025-142-T
4 Pin Header	4 Pin Header	J1	1	Harwin	M20-9990446
USB-C	USB-C Connector	J2	1	JAE Electronics	DX07S016JA1R1500
Connector	Input/Output Connector	J3, J5	2	TE Connectivity / AMP	1-282836-3
6 Pin Header	6 Pin Header	J4	1	Harwin	M20-9990646
2 Pin Header	2 Pin Header	JP1	1	Harwin	M20-9990246
33uH	Inductor	L1	1	Codaca	CPD2315-330M
Mounting Hole	Mounts	MH1, MH2, MH3, MH4, MH5, MH6, MH7, MH8	8	Wurth Elektronik	709447600
9V	Power Supply	PS1, PS2, PS3	3	Recom Power	RP-1209S
12V	Power Supply	PS4	1	Recom Power	RI3-1212S
110mOhm	BDS	Q2, Q3	2	Renesas	TP65B110HRU
10k Ohm	Resistor	R1	1	KOA Speer	RK73H1JTTP1002F
1M Ohm	Resistor	R2, R3, R4, R6, R7, R8, R9, R10, R14	9	KOA Speer	RK73H2BTTD1004F
0 Ohm	Resistor	R5, R17, R18	3	Vishay	CRCW06030000Z0EI
4.7k Ohm	Resistor	R11	1	Vishay	CRCW04024K70FKEDC
10k Ohm	Resistor	R12, R13, R15, R16, R25, R40, R43, R45, R46	9	KOA Speer	RK73H1ERTTP1002F
330 Ohm	Resistor	R21, R27, R28	3	TE Connectivity	CRGCQ0402F330R
5.1k Ohm	Resistor	R22, R23	2	KOA Speer	RK73H1ETTP5101F
120 Ohm	Resistor	R24, R36, R44, R51	4	Yageo Group	AC0603FR-07120RL
1k Ohm	Resistor	R26	1	Vishay	CRCW04021K00JNED
33 Ohm	Resistor	R31, R41, R47, R53	4	TE Connectivity	CRGP0805F33R
6.04 Ohm	Resistor	R34, R42, R49, R55	4	Yageo Group	RC0805FR-076R04L
Switch	Switch	SW	1	Same Sky	SLW-1276864-4A-D
Test Point	Test Point	TP1, TP2, TP3, TP15	4	TE Connectivity	1625854-3
Test Point	Test Point	TP11, TP12, TP13	3	Keystone	5011
Reg Linear	IC	U1	1	Diodes Inc.	AZ1117IH-3.3TRG1
Op Amp	IC	U2	1	Renesas	ISL28134FHZ-T7
Analog Comparator	IC	U3	1	Analog Devices	MAX9032AKA+T
V-Ref Precision	IC	U4	1	Renesas	ISL21010CFH315Z-T7A
32-bit MCU	MCU	U5	1	Renesas	R5F52318ADFL#30
5V 0.2pF	Diode	U6	1	Semtech	RCLAMP0582N.TCT
32-bit MCU	MCU	U7	1	Renesas	R5F526TAAGFL#50
Gate Driver	Gate Driver	U10, U11, U12, U13	4	Skyworks Solutions	SI8271GB-IS
10 MHZ, 12pF	Crystal	Y1	1	Abracon	ABM8AIG-10.000MHZ-12-2Z-T3

13. References

[1] TP65B110HRU, Product Webpage, Renesas Electronics

14. RoHS Compliance

Renesas Electronics' suppliers certify that its products comply with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

15. General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (Max.) and VIH (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (Max.) and VIH (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system evaluation test for the given product.

16. Revision History

Revision	Date	Description
1.00	Mar 10, 2026	Initial release.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
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