User's Manual

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RH850/F1KM-S4, RH850/F1KM-S2

User's Manual: Hardware

Renesas microcontroller
RH850 Family

Addendum for the high temperature products (Ta=125℃)

Renesas Electronics
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to power supply or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

5. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

6. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

7. Power ON/OFF sequence

   In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises only the addendum portion of Overview and Electrical Characteristics section.

> Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The following documents apply to the RH850/F1KH, RH850/F1KM Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

To understand the overall functions of the RH850/F1KM-S4, RH850/F1KM-S2.

→ The part names of the products added later are shown in this document.

The specification of the products added later for Ta = –40°C to +125°C is same as the product of Ta = –40°C to +105°C which has been already existed in hardware User`s Manual except the specification items shown in this document.

Read the following manuals according to its content.

Document Type	Description	Document Title	Document No.
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description	RH850/F1KH, RH850/F1KM User's Manual: Hardware	R01UH0684EJxxxx

Conventions

Data significance: Higher digits on the left and lower digits on the right

Active low representation: xxx (overscore over pin or signal name)

Memory map address: Higher addresses on the top and lower addresses on the bottom Note: Footnote for item marked with Note in the text

Caution: Information requiring particular attention Remark:

Supplementary information

Numeric representation: Binary ... xxxx or $xxxx_B$

Decimal ... xxxx

Hexadecimal ... $xxxx_H$

Prefix indicating power of 2 (address space, memory capacity):

K (kilo): $2^{10} = 1,024$

M (mega): $2^{20} = 1,024^2$

G (giga): $2^{30} = 1,024^3$

Description of Registers

Each register description includes register access, register address, and register value after a reset, a bit chart, illustrating the arrangement of bits, and a table of bits, describing the meaning of the bit settings.

The standard format for bit charts and tables are described below.

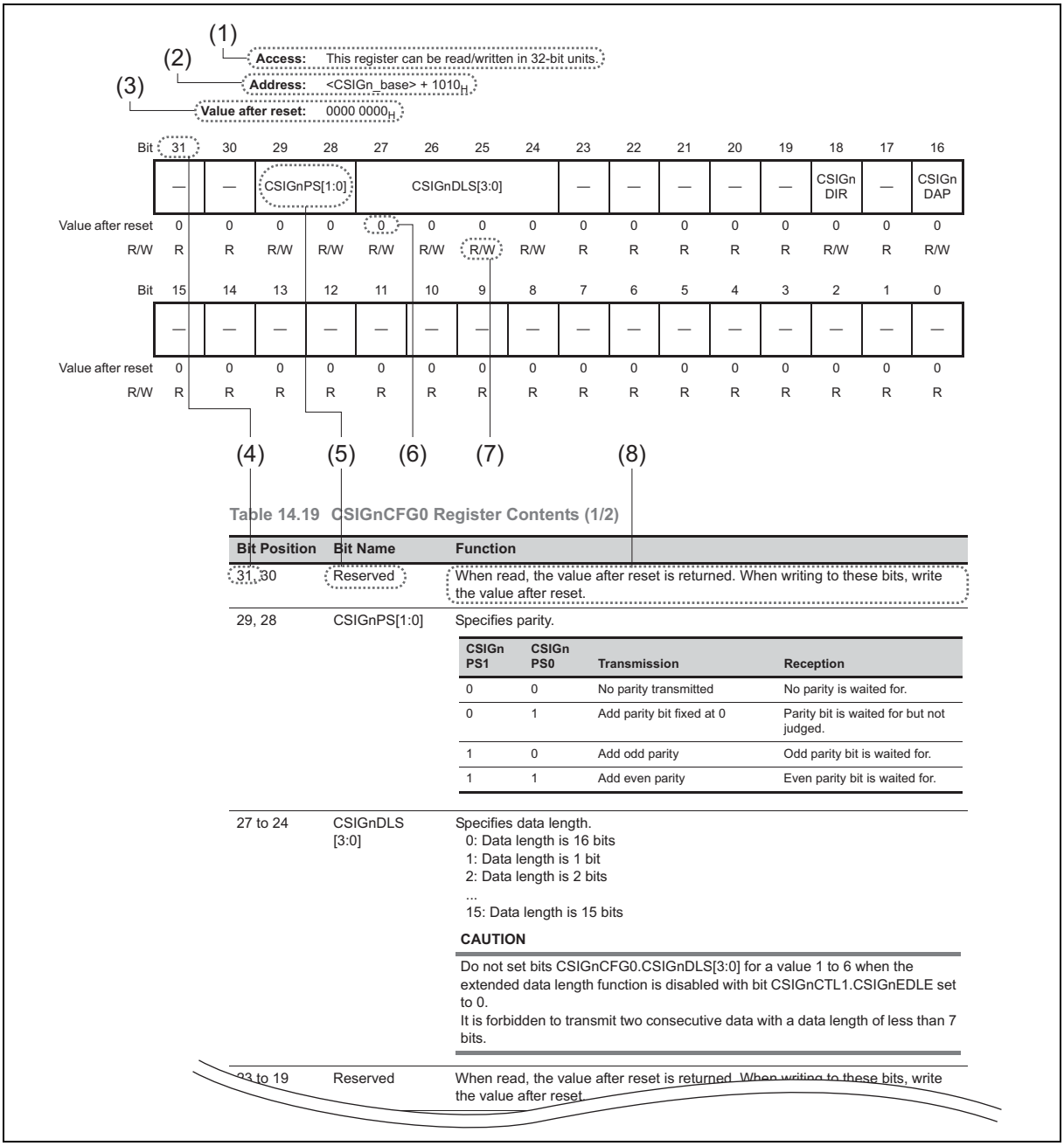

Table 14.19 CSIGnCFG0 Register Contents (1/2)

Bit Position	Bit Name	Function
31, 30	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.
29, 28	CSIGnPS[1:0]	Specifies parity.
27 to 24	CSIGnDLS [3:0]	Specifies data length. 0: Data length is 16 bits 1: Data length is 1 bit 2: Data length is 2 bits ... 15: Data length is 15 bits
23 to 19	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.

CSIGn PS1	CSIGn PS0	Transmission	Reception
0	0	No parity transmitted	No parity is waited for.
0	1	Add parity bit fixed at 0	Parity bit is waited for but not judged.
1	0	Add odd parity	Odd parity bit is waited for.
1	1	Add even parity	Even parity bit is waited for.

CAUTION

Do not set bits CSIGnCFG0.CSIGnDLS[3:0] for a value 1 to 6 when the extended data length function is disabled with bit CSIGnCTL1.CSIGnEDLE set to 0.
It is forbidden to transmit two consecutive data with a data length of less than 7 bits.

(1) Access

The register can be accessed in the bit unit indicated here.

(2) Address

This is the register address.
For base address, see description of base address in each section.

(3) Value after a reset (in hexadecimal notation)

This is the value of all bits of the register after a reset. Values for bytes are given as numbers in the range from 0 to 9 and letters from A to F or as X where they are undefined.

(4) Bit position

This is the bit number.
The bits are numbered from 31 to 0 for 32-bit registers, 15 to 0 for 16-bit registers, and 7 to 0 for 8-bit registers.

(5) Bit name

Bit name or field name is indicated.
When clearly identifying the digits of a bit field is required, do so by using a form such as CSIGnDLS[3:0] above.
Indicate reserved bits by using a dash (—).

(6) Value after a reset (in binary notation)

This is the bit values after a reset.

0	:	The value after a reset is 0.
1	:	The value after a reset is 1.
—	:	The value after a reset is undefined.

(7) R/W

This is the bit attribute of all bits of the register.

R/W	:	The bit or field is readable and writable.
R	:	The bit or field is readable. Note that all reserved bits are indicated as R. When written, the value specified in the bit chart or the value after a reset should be written. In case of writing to writable registers that also include non-reserved bits with the R-attribute, writing to the R-attribute bits will be ignored unless otherwise specified.
W	:	This bit or field is writable. When read, the value is undefined. If a value is indicated in the bit chart, the value is returned.

(8) Function

This is function of the bit.

Section 1 Overview

This specification of the RH850/F1KM-S4, RH850/F1KM-S2 is valid to the specification described in the reference document *RH850/F1KH RH850/F1KM hardware user`s manual*.

Notice:

1. Set Max. value of REGVCC, EVCC & BVCC 3.6 V and A0VREF & A1VREF 5.5 V. If the condition of A0VREF ≥ EVCC & A1VREF ≥ BVCC in Analog input voltage, please refer to the **Section 47B.6, A/D Converter Characteristics** in the *RH850/F1KH, RH850/F1KM User's Manual:*
2. Set Max. Tj value up to 150°C while Max. Ta is 125°C.

1.1 RH850/F1KM Function

Table 1.1 Overview of product

Product Name		RH850/F1KM-S4		
		100 Pins	144 Pins	176 Pins
Voltage supply	Internal supply	VPOC to 3.6 V		
	Input/output buffer supplies	VPOC to 3.6 V		
	A/D Converter supplies	3.0 to 5.5 V		

Table 1.2 Overview of product

Product Name		RH850/F1KM-S2		
		100 Pins	144 Pins	176 Pins
Voltage supply	Internal supply	VPOC to 3.6 V		
	Input/output buffer supplies	VPOC to 3.6 V		
	A/D Converter supplies	3.0 to 5.5 V		

1.2 RH850/F1KM Product Lineup

Table 1.3 Product Lineup

F1KM-S4		Memory						Part Name
Pin Count	CPU Frequency	Code Flash	Data Flash	Local RAM (LRAM)	Global RAM (GRAM)	Retention RAM (RRAM)	Trace RAM	Operating Temperature (Ta) –40°C to +125°C Package
100 pins	240 MHz max.	3 MB	128 KB	192 KB	128 KB	64 KB	Not available	R7F701A554AFP-C LQFP
		4 MB		256 KB	192KB		32 KB	R7F701A564AFP-C LQFP
144 pins	240 MHz max.	3 MB	128 KB	192 KB	128 KB	64 KB	Not available	R7F701A574AFP-C LQFP
		4 MB		256 KB	192KB		32 KB	R7F701A584AFP-C LQFP
176 pins	240 MHz max.	3 MB	128 KB	192 KB	128 KB	64 KB	Not available	R7F701A594AFP-C LQFP
		4 MB		256 KB	192KB		32 KB	R7F701A604AFP-C LQFP

Table 1.4 Product Lineup

F1KM-S2		Memory						Part Name
Pin Count	CPU Frequency	Code Flash	Data Flash	Local RAM (LRAM)	Global RAM (GRAM)	Retention RAM (RRAM)	Trace RAM	Operating Temperature (Ta) –40°C to +125°C Package
100 pins	240 MHz max.	2 MB	128 KB	128 KB	96 KB	32 KB	Not available	R7F701A614AFP-C LQFP
144 pins	240 MHz max.	2 MB	128 KB	128 KB	96 KB	32 KB	Not available	R7F701A624AFP-C LQFP
176 pins	240 MHz max.	2 MB	128 KB	128 KB	96 KB	32 KB	Not available	R7F701A634AFP-C LQFP

Section 2 Flash Memory

2.1 Reading Flash Memory

2.1.1 Reading Data Flash Memory

2.1.1.1 PRDNAMEn — Product Name Storage Register (n = 1 to 3)

This register stores the product name. The product part name is stored in 16-byte ASCII code, and PRDNAME1, PRDNAME2, and PRDNAME3 correspond to the fourth to first bytes, eighth to fifth bytes, and twelfth to ninth bytes of the product part name respectively.

Access: These registers are read-only registers that can be read in 32-bit units.

Address: PRDNAME1: FFCD 00D0$_H$

PRDNAME2: FFCD 00D4$_H$

PRDNAME3: FFCD 00D8$_H$

Value after reset: See Table 2.2 and Table 2.3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PRDNAMEn[31:24]*1								PRDNAMEn[23:16]*1							
Value after reset																
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PRDNAMEn[15:8]*1								PRDNAMEn[7:0]*1							
Value after reset																
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Note 1. n = 1 to 3.

Table 2.1 PRDNAMEn Register Contents

Bit Position	Bit Name	Function
31 to 24	—	Product name fourth byte (PRDNAME1), eighth byte (PRDNAME2) twelfth byte (PRDNAME3)
23 to 16	—	Product name third byte (PRDNAME1), seventh byte (PRDNAME2) eleventh byte (PRDNAME3)
15 to 8	—	Product name second byte (PRDNAME1), sixth byte (PRDNAME2) tenth byte (PRDNAME3)
7 to 0	—	Product name first byte (PRDNAME1), fifth byte (PRDNAME2) ninth byte (PRDNAME3)

Table 2.2 List of Registers Related to Product Information (RH850/F1KM-S4)

Product Part Name	PRDNAME1	PRDNAME2	PRDNAME3
R7F701A55	3746 3752	3541 3130	2020 2035
R7F701A56	3746 3752	3541 3130	2020 2036
R7F701A57	3746 3752	3541 3130	2020 2037
R7F701A58	3746 3752	3541 3130	2020 2038
R7F701A59	3746 3752	3541 3130	2020 2039
R7F701A60	3746 3752	3641 3130	2020 2030

Table 2.3 List of Registers Related to Product Information (RH850/F1KM-S2)

Product Part Name	PRDNAME1	PRDNAME2	PRDNAME3
R7F701A61	3746 3752	3641 3130	2020 2031
R7F701A62	3746 3752	3641 3130	2020 2032
R7F701A63	3746 3752	3641 3130	2020 2033

Section 3 Electrical Characteristics

3.1 General Measurement Conditions

3.1.1 Common Conditions

- Power supply
  - REGVCC = EVCC = VPOC*1 to 3.6 V
  - BVCC = VPOC*1 to REGVCC
  - A0VREF = 3.0 V to 5.5 V
  - A1VREF = 3.0 V to 5.5 V
  - AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V
- Capacitance of the internal regulator
  - CAWOVCL: 0.1 µF ±30%
  - CISOVCL: 0.1 µF ±30% per pin
- Operating temperature
  - Tj = –40 to +150°C @R7F701Aaa4AFP*2

  aa = 55, 56, 57, 58, 59, 60, 61, 62, 63
- Load conditions
  - CL = 30 pF

Note 1. “VPOC” means POC (power-on clear) detection voltage. For more detail, refer to the **Section 47B.4.5.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics** in the *RH850/F1KH, RH850/F1KM User’s Manual:*

Note 2. Regarding operation temperature of each product, see **Section 1.2 RH850/F1KM Product Lineup.**

3.2 Temperature Condition

Table 3.1 Temperature Condition

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Storage temperature	Tstg		–55		150	°C
Junction temperature	Tj	R7F701Aaa4AFP	–40		150	°C

Note: aa = 55, 56, 57, 58, 59, 60, 61, 62, 63

Regarding operation temperature of each product, see **Section 1.2, RH850/F1KM Product Lineup.**

3.3 Operational Condition

Condition: REGVCC = EVCC = VPOC to 3.6 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V,
A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,

The characteristics listed below must satisfy the above operational condition. For more detail, refer to the following section in the *RH850/F1KH, RH850/F1KM User's Manual:*

47B.3.2 Oscillator Characteristics

47B.3.3 Internal Oscillator Characteristics

47B.3.4.1 PLL0 (for CPU, with SSCG) Characteristics

47B.3.4.2 PLL1 (for CPU/Peripheral) Characteristics

47B.4.5.2 Voltage Detector (POC, LVI, VLVI, CVM) Characteristics

47B.4.5.3 Power Up/Down Timing

47B.4.5.4 CPU Reset Release Timing

47B.7.1 Code Flash

47B.7.2 Data Flash

Condition: REGVCC = EVCC = 3.0 V to 3.6 V, BVCC = 3.0 V to 3.6 V, A0VREF = 3.0 V to 5.5 V,
A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,

The characteristics listed below must satisfy the above operational condition. For more detail, refer to the following section in the *RH850/F1KH, RH850/F1KM User's Manual:*

47B.5.8 SFMA Timing

47B.5.15.1 MII Interface

Condition: REGVCC = EVCC = 3.0 V to 3.6 V, BVCC = 3.0 V to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V,

The characteristics listed below must satisfy the above operational condition. For more detail, refer to the following section in the *RH850/F1KH, RH850/F1KM User's Manual:*

47B.5.1 RESET Timing

47B.5.2 Mode Timing

47B.5.3 Interrupt Timing

47B.5.4 Low Power Sampler (DPIN input) Timing

47B.5.5 CSCXFOUT Timing

47B.5.6 MEMC0CLK Timing

47B.5.7.1 MEMC0CLK Asynchronous

47B.5.7.2 MEMC0CLK Synchronous

47B.5.10.1 CSIG Timing

47B.5.10.2 CSIH Timing

47B.5.11 RLIN2/RLIN3 Timing

47B.5.12 RIIC Timing

47B.5.13 RS-CANFD Timing

47B.5.14 Flex-Ray Timing

47B.5.16 RSENT Timing

47B.5.17 Timer Timing

47B.5.18 ADTRG Timing

47B.5.19 Key Return Timing

47B.5.20 DCUTRST Timing

47B.5.21.1 Nexus Interface Timing

47B.5.21.2 LPD (4 Pins) Interface Timing

47B.5.21.3 LPD (1 Pin) Interface Timing

47B.5.21.4 Debug Event Interface Timing

47B.6 A/D Converter Characteristics

47B.7.3.1 Serial Programmer Setup Timing

47B.7.3.2 Flash Programming Interface

3.3.1 Recommended Operating Conditions

Products of CPU frequency 240 MHz max. and 160 MHz max.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power supply	REGVCC	REGVCC = EVCC	VPOC*1		3.6	V
	EVCC					
	BVCC		VPOC*1		REGVCC	V
	A0VREF		3.0		5.5	V
	A1VREF					

Note 1. "VPOC" means POC (power-on clear) detection voltage (TYP. 2.85 V). For more detail, refer to the **Section 47B.4.5.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics** in the *RH850/F1KH, RH850/F1KM User`s Manual: Hardware*.

In addition, the guaranteed operation in DC characteristic.

And AC characteristic is guaranteed when more than 3.0 V.

When the power supply voltage is VPOC to 3.0 V, the device does not malfunction.

3.3.2 Pin Characteristics

Condition: REGVCC = EVCC = VPOC to 3.6 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High level input voltage	VIH	TTL	IOVCC = VPOC to 3.6 V	2.0		IOVCC + 0.3	V

3.3.3 Power Supply Currents

Condition: REGVCC, EVCC, BVCC, A0VREF and A1VREF total current. But the I/O buffer is stopped.

Products of CPU frequency 240 MHz max. (RH850/F1KM-S4)

Item	Symbol	Condition				MIN.	TYP.*1	MAX.	Unit
		CPU	PLL	Tj	Peripheral*2				
RUN mode current	IDDR	Run (240 MHz)	Run	–40 to 150°C	Run (#1)		68	185	mA
				25°C	Stop (#1)		62		mA
RUN mode current (During data/code flash programming)	IDDR3	Run (240 MHz)	Run	–40 to 150°C	Run (#2)		88	205	mA
RUN mode current (With code flash background operation)	IDDRBGO	Run (240 MHz)	Run	–40 to 150°C	Run (#6)		88	205	mA
RUN mode current (HALT state)	IDDH	Run (240 MHz)	Run	–40 to 150°C	Run (#3)		64	183	mA

Products of CPU frequency 240 MHz max. (RH850/F1KM-S2)

Item	Symbol	Condition				MIN.	TYP.*1	MAX.	Unit
		CPU	PLL	Tj	Peripheral*2				
RUN mode current	IDDR	Run (240 MHz)	Run	–40 to 150°C	Run (#1)		56	154	mA
				25°C	Stop (#1)		44		mA
RUN mode current (During data/code flash programming)	IDDR3	Run (240 MHz)	Run	–40 to 150°C	Run (#2)		76	174	mA
RUN mode current (With code flash background operation)	IDDRBGO	Run (240 MHz)	Run	–40 to 150°C	Run (#6)		76	174	mA
RUN mode current (HALT state)	IDDH	Run (240 MHz)	Run	–40 to 150°C	Run (#3)		54	152	mA

Products of CPU frequency 160 MHz max. (RH850/F1KM-S4)

Item	Symbol	Condition				MIN.	TYP.*1	MAX.	Unit
		CPU	PLL	Tj	Peripheral*2				
RUN mode current	IDDR	Run (160 MHz)	Run	–40 to 150°C	Run (#1)		58	173	mA
				25°C	Stop (#1)		52		mA
RUN mode current (During data/code flash programming)	IDDR3	Run (160 MHz)	Run	–40 to 150°C	Run (#2)		78	193	mA
RUN mode current (With code flash background operation)	IDDRBGO	Run (160 MHz)	Run	–40 to 150°C	Run (#6)		78	193	mA
RUN mode current (HALT state)	IDDH	Run (160 MHz)	Run	–40 to 150°C	Run (#3)		54	171	mA

Products of CPU frequency 240 MHz max., 160 MHz max. (RH850/F1KM-S4)

Item	Symbol	Condition				MIN.	TYP.*1	MAX.	Unit
		CPU	PLL	Tj	Peripheral*2				
STOP mode current	IDDS	Stop	Stop	–40 to 90°C	Stop (#2)		1.3	22	mA
				110°C	Stop (#2)			42	mA
				135°C	Stop (#2)			66	mA
DeepSTOP mode current	IDDDS	Power off	Power off	–40 to 85°C	Stop (#3)		50	700	µA
				105°C	Stop (#3)			1280	µA
				125°C	Stop (#3)			1840	µA
Cyclic RUN mode current	IDDCR	Run (HS IntOSC)	Stop	–40 to 90°C	Run (#4)		6.1	28	mA
				115°C	Run (#4)			47	mA
				135°C	Run (#4)			71	mA
Cyclic STOP mode current	IDDCS	Stop	Stop	–40 to 90°C	Run (#5)		1.4	23	mA
				110°C	Run (#5)			42	mA
				135°C	Run (#5)			66	mA

Products of CPU frequency 240 MHz max. (RH850/F1KM-S2)

Item	Symbol	Condition				MIN.	TYP.*1	MAX.	Unit
		CPU	PLL	Tj	Peripheral*2				
STOP mode current	IDDS	Stop	Stop	–40 to 90°C	Stop (#2)		0.9	21	mA
				110°C	Stop (#2)			38	mA
				135°C	Stop (#2)			63	mA
DeepSTOP mode current	IDDDS	Power off	Power off	–40 to 85°C	Stop (#3)		49	670	µA
				105°C	Stop (#3)			1100	µA
				125°C	Stop (#3)			1670	µA
Cyclic RUN mode current	IDDCR	Run (HS IntOSC)	Stop	–40 to 90°C	Run (#4)		4.3	25	mA
				115°C	Run (#4)			43	mA
				135°C	Run (#4)			68	mA
Cyclic STOP mode current	IDDCS	Stop	Stop	–40 to 90°C	Run (#5)		1.1	21	mA
				110°C	Run (#5)			39	mA
				135°C	Run (#5)			64	mA

Note 1. The condition of “TYP.” shows the specification with the following conditions. Also, the value is just for reference only.

- Tj = 25°C
- REGVCC = EVCC = BVCC = 3.3 V
- A0VREF = A1VREF = 5.0 V
- AWOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V

Note 2. For operating condition of each peripheral function, refer to the **Section 47B.4.3 Power Supply Currents** in the *RH850/F1KH, RH850/F1KM User`s Manual: Hardware*.

Caution: It must be ensured that the junction temperature in the Ta range remains below Tj ≤ 150°C and does not exceed its limit under application conditions (thermal resistance, power supply current, peripheral current (if not included in power supply current), port output current and injection current).

3.3.4 Regulator Characteristics

Condition: Condition: REGVCC = EVCC = VPOC to 3.6 V, BVCC = VPOC to REGVCC, A0VREF = 3.0 V to 5.5 V, A1VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = BVSS = A0VSS = A1VSS = 0 V, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage	REGVCC		VPOC*1		3.6	V

Note 1. “VPOC” means POC (power-on clear) detection voltage (typ. 2.85 V). For more detail, refer to the **Section 47B.4.5.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics** in the *RH850/F1KH, RH850/F1KM User’s Manual:*

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