User's Manual

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RH850/F1KM-S1

User's Manual: Hardware

Renesas microcontroller
RH850 Family

Addendum for the high temperature products (Tj=160℃)

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Rev.1.00 August, 2021

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(Rev.5.0-1 October 2020)

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to power supply or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
5. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
6. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
7. Power ON/OFF sequence
   In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.
The manual comprises only the addendum portion of Overview, Clock Controller, Flash Memory and Electrical Characteristics section.

> Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The following documents apply to the RH850/F1KH, RH850/F1KM Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description	RH850/F1KH, RH850/F1KM User's Manual: Hardware	R01UH0684EJxxxx

Conventions

Data significance: Higher digits on the left and lower digits on the right

Active low representation: xxx (overscore over pin or signal name)

Memory map address: Higher addresses on the top and lower addresses on the bottom

Note: Footnote for item marked with Note in the text

Caution: Information requiring particular attention Remark:

Supplementary information

Numeric representation: Binary ... xxxx or $xxxx_B$

Decimal ... xxxx

Hexadecimal ... $xxxx_H$

Prefix indicating power of 2 (address space, memory capacity): K

(kilo): $2^{10} = 1,024$

M (mega): $2^{20} = 1,024^2$

G (giga): $2^{30} = 1,024^3$

Description of Registers

Each register description includes register access, register address, and register value after a reset, a bit chart, illustrating the arrangement of bits, and a table of bits, describing the meaning of the bit settings.

The standard format for bit charts and tables are described below.

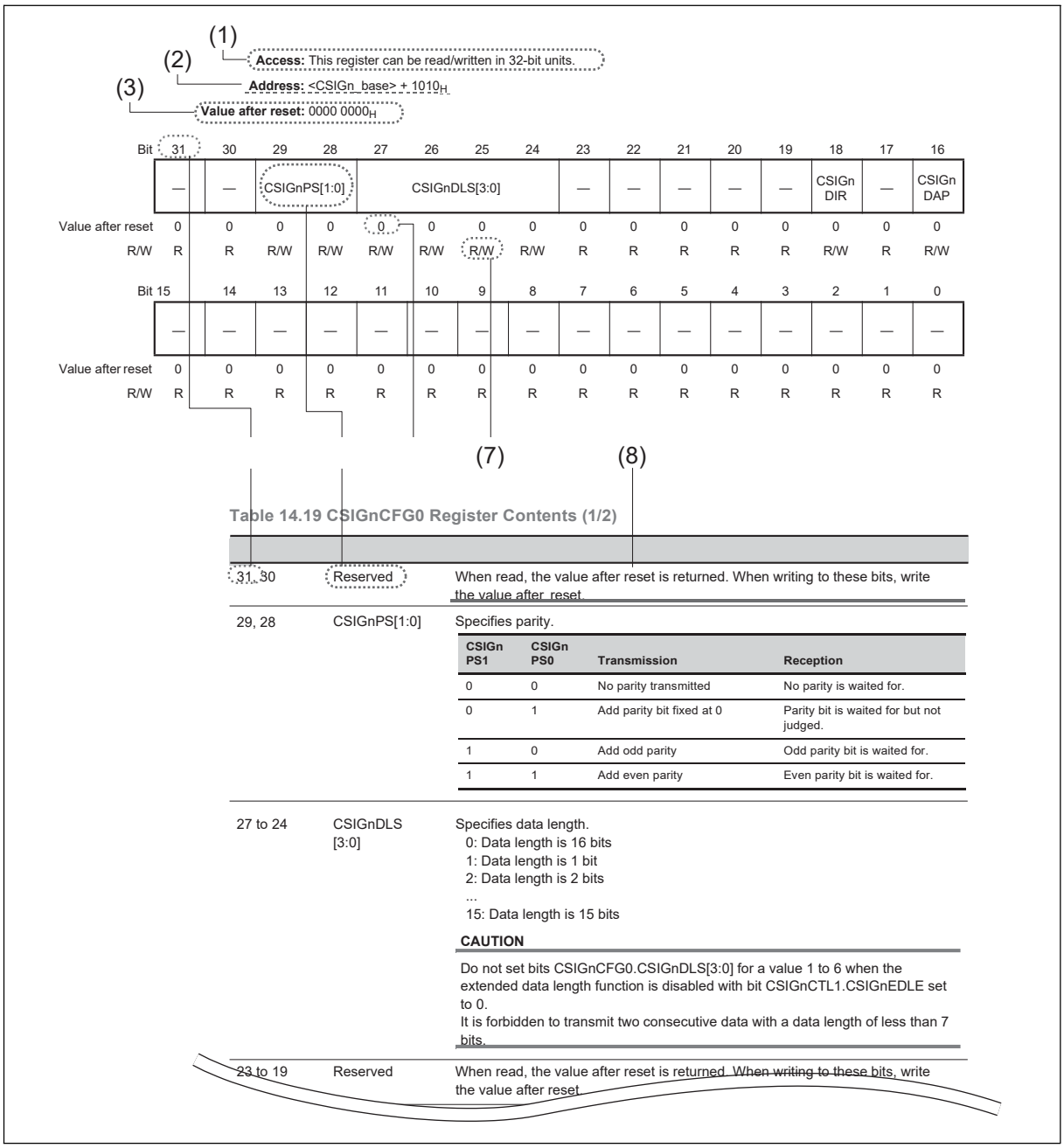

Table 14.19 CSIGnCFG0 Register Contents (1/2)

31, 30	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.
29, 28	CSIGnPS[1:0]	Specifies parity.

CSIGn PS1	CSIGn PS0	Transmission	Reception
0	0	No parity transmitted	No parity is waited for.
0	1	Add parity bit fixed at 0	Parity bit is waited for but not judged.
1	0	Add odd parity	Odd parity bit is waited for.
1	1	Add even parity	Even parity bit is waited for.

27 to 24	CSIGnDLS [3:0]	Specifies data length. 0: Data length is 16 bits 1: Data length is 1 bit 2: Data length is 2 bits ... 15: Data length is 15 bits **CAUTION** Do not set bits CSIGnCFG0.CSIGnDLS[3:0] for a value 1 to 6 when the extended data length function is disabled with bit CSIGnCTL1.CSIGnEDLE set to 0. It is forbidden to transmit two consecutive data with a data length of less than 7 bits.
23 to 19	Reserved	When read, the value after reset is returned. When writing to these bits, write the value after reset.

(1) Access

The register can be accessed in the bit unit indicated here.

(2) Address

This is the register address.
For base address, see description of base address in each section.

(3) Value after a reset (in hexadecimal notation)

This is the value of all bits of the register after a reset. Values for bytes are given as numbers in the range from 0 to 9 and letters from A to F or as X where they are undefined.

(4) Bit position

This is the bit number.
The bits are numbered from 31 to 0 for 32-bit registers, 15 to 0 for 16-bit registers, and 7 to 0 for 8-bit registers.

(5) Bit name

Bit name or field name is indicated.
When clearly identifying the digits of a bit field is required, do so by using a form such as CSIGnDLS[3:0] above.
Indicate reserved bits by using a dash (—).

(6) Value after a reset (in binary notation)

This is the bit values after a reset.

0 : The value after a reset is 0.

1 : The value after a reset is 1.

— : The value after a reset is undefined.

(7) R/W

This is the bit attribute of all bits of the register.

R/W : The bit or field is readable and writable.

R : The bit or field is readable.
Note that all reserved bits are indicated as R. When written, the value specified in the bit chart or the value after a reset should be written.
In case of writing to writable registers that also include non-reserved bits with the R-attribute, writing to the R-attribute bits will be ignored unless otherwise specified.

W : This bit or field is writable. When read, the value is undefined. If a value is indicated in the bit chart, the value is returned.

(8) Function

This is function of the bit.

Section 1 Overview

This specification of the RH850/F1KM-S1 is valid to the specification described in the reference document *RH850/F1KH RH850/F1KM hardware user`s manual*.

1.1 RH850/F1KM Function

Table 1.1 Overview of product

Product Name		RH850/F1KM-S1			
		48 Pins	64 Pins	80 Pins	100 Pins
CPU	CPU frequency	80 MHz max			

1.2 RH850/F1KM Product Lineup

Table 1.2 Product Lineup

F1KM-S1		Memory					Part Name
Pin Count	CPU Frequency	Code Flash	Data Flash	Local RAM (LRAM)	Retention RAM (RRAM)	Trace RAM	Junction Temperature (Tj) –40°C to +160°C Package
100 pins	80 MHz max.	1024 KB	64 KB	96 KB	32 KB	32 KB	R7F701684FAFP-C LQFP
		768 KB		64 KB		Not available	R7F701685FAFP-C LQFP
		512 KB		32 KB		Not available	R7F701686FAFP-C LQFP
80 pins	80 MHz max.	1024 KB	64 KB	96 KB	32 KB	32 KB	R7F701687FAFP-C LQFP
		768 KB		64 KB		Not available	R7F701688FAFP-C LQFP
		512 KB		32 KB		Not available	R7F701689FAFP-C LQFP
64 pins	80 MHz max.	1024 KB	64 KB	96 KB	32 KB	32 KB	R7F701690FAFP-C LQFP
		768 KB		64 KB		Not available	R7F701691FAFP-C LQFP
		512 KB		32 KB		Not available	R7F701692FAFP-C LQFP
48 pins	80 MHz max.	1024 KB	64 KB	96 KB	32 KB	32 KB	R7F701693FAFP-C LQFP
		768 KB		64 KB		Not available	R7F701694FAFP-C LQFP
		512 KB		32 KB		Not available	R7F701695FAFP-C LQFP

Section 2 Clock Controller

2.1 Registers

2.1.1 Clock Oscillator Registers

2.1.1.1 PLL1C — PLL1 Control Register

This register is used to set the PLL1 VCO output clock frequency $f_{VCO1OUT}$, shown in **Section 12C.3.4.1, PLL1 Parameters** in the *RH850/F1KH, RH850/F1KM User`s Manual: Hardware*.

This register can only be written, if the PLL1 is disabled.

This register is initialized by all reset sources (ISORES).

Access: This register can be read or written in 32-bit units.

Address: FFF8 9008$_H$

Value after reset: 0001 133B$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	PLL1M[1:0]		—	—	—	—	—	PLL1N[5:0]					
Value after reset	0	0	0	1	0	0	1	1	0	0	1	1	1	0	1	1
R/W	R	R	R	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 2.1 PLL1C Register Contents

Bit Position	Bit Name	Function
31 to 13	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
12, 11	PLL1M[1:0]	Division ratio Mr is set. For PLL1M[1:0] settings, see **Table 2.2, PLL1 Output Table**.
10 to 6	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
5 to 0	PLL1N[5:0]	Division ratio Nr is set. For PLL1N[5:0] settings, see **Table 2.2, PLL1 Output Table**.

CAUTION

Set this register when PLL1 is stopped.

Table 2.2 PLL1 Output Table

PLL1CLKIN frequency $f_{PLL1CLKIN}$ (MHz)	PLL1C. PLL1M[1:0] (Mr)*5	PLL1C. PLL1N[5:0] (Nr)*5	VCO1OUT frequency $f_{VCO1OUT}$ (MHz)	CPLL1OUT frequency $f_{CPLL1OUT}$ (MHz)*1	PPLLOUT frequency $f_{PPLLOUT}$ (MHz)
				VCO1OUT × 1/6	
8 (MainOSC)	00_B (Mr = 1)	$3B_H$ (Nr = 60)	480.0	80.0	80.0
16 (MainOSC)	01_B (Mr = 2)	$3B_H$ (Nr = 60)	480.0	80.0	80.0
20 (MainOSC)	01_B (Mr = 2)	$2F_H$ (Nr = 48)	480.0	80.0	80.0
24 (MainOSC)	01_B (Mr = 2)	27_H (Nr = 40)	480.0	80.0	80.0
	10_B (Mr = 3)	$3B_H$ (Nr = 60)	480.0	80.0	80.0
8 (HS IntOSC)*2, *4	00_B (Mr = 1)	$3B_H$ (Nr = 60)	480.0	80.0*2, *3	80.0*2

Note 1. The CPLL1OUT frequency is defined by CKSC_CPUCLKD_CTL.CPUCLKDPLL[1:0]. Refer to the CKSC_CPUCLKD_CTL register description.

Note 2. Typical frequencies. User calibration of HS IntOSC is required before setting HS IntOSC as PLL1CLKIN.

Note 3. The limit of CPLL1OUT frequency is 80 MHz (typ.) when HS IntOSC is selected as clock source of PLL1.

Note 4. See **Section 44.10, Usage Notes** in the *RH850/F1KH, RH850/F1KM User`s Manual: Hardware*.

Note 5. Settings other than those shown in this table are prohibited.

2.1.2 Clock Selector Control Register

2.1.2.1 CPU Clock Domain C_ISO_CPUCLK

1. CKSC_CPUCLKD_CTL — C_ISO_CPUCLK Clock Divider Selection Register

The correct write sequence using the PROTCMD1 register is required in order to update this register. For details, see **Section 5, Write-Protected Registers** in the *RH850/F1KH, RH850/F1KM User`s Manual: Hardware.*

This register is initialized by all reset sources (ISORES).

Access: This register can be read or written in 32-bit units.

Address: FFF8 A100$_H$

Value after reset: 0000 0001$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	CPUCLKDPLL [1:0]		CPUCLKDCSID [2:0]		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Table 2.3 CKSC_CPUCLKD_CTL Register Contents

Bit Position	Bit Name	Function
31 to 5	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
4, 3	CPUCLKDPLL[1:0]	Clock Divider CPLLDIV Setting Specifies the CPLLDIV divisor, which determines maximum clock frequency of C_ISO_CPUCLK. 00_B: CPLL1OUT = VCO1OUT × 1/6 (80 MHz) Other than above: Setting prohibited
2 to 0	CPUCLKDCSID[2:0]	Clock Divider Setting for C_ISO_CPUCLK 000_B: Setting prohibited 001_B: CKSC_CPUCLKS_CTL selection /1 (Default) 010_B: CKSC_CPUCLKS_CTL selection /2 011_B: CKSC_CPUCLKS_CTL selection /4 100_B: CKSC_CPUCLKS_CTL selection /8 Other than above: Setting prohibited

2.2 Clock Domain Setting Method

2.2.1 Clock Domain Setting

The following table shows a selectable source clock, a frequency division ratio, and a register to be used for each clock domain.

Table 2.4 List of Selectable Clock

Clock Domain	Clock Name	Selectable Register	Frequency Divided Register			Maximum Frequency	Applicable Unit
C_ISO_CPUCLK	CPUCLK	CKSC_CPUCLKS_CTL[*1] CKSC_CPUCLKD_CTL[*1]	MainOSC	CKSC_CPUCLKD_CTL	**1/1**	80 MHz[*2]	CPU subsystem
			CPLL1OUT (VCO1OUT ×1/6)		1/8		
			EMCLK		—		

Note: The items written in bold are the initial setting clocks for each register.

Note 1. CKSC_CPUCLKS_CTL selects selection of Main OSC, CPLL1OUT and EMCLK.
CKSC_CPUCLKD_CTL.CPUCLKDPLL[1:0]
selects CPLL1OUT clock frequency.

Note 2. For the supported settings, refer to **Table 2.2, PLL1 Output Table**.

CAUTION

To stop the clock source selected for the clock domain before transitioning to STOP/DeepSTOP mode, select “Disable” for that clock domain in advance. Do not stop the source clock of a clock domain for which “Disable” cannot be selected while functions are operating on that clock domain. To stop the clock source selected for the domain by transitioning to STOP/DeepSTOP mode, “Disable” does not need to be selected. Instead of the setting “Disable”, select “Stop” for the clock domain in stand-by mode by using the stop mask register.

Section 3 Flash Memory

3.1 Reading Flash Memory

3.1.1 Reading Data Flash Memory

3.1.1.1 EEPRDCYCL — Data Flash Wait Cycle Control Register

This register is used to specify the number of wait cycles to be inserted when reading the data in the data flash. Set the number of wait cycles to be inserted in the clock cycle when reading the data flash according to the operating clock frequency of the CPU (f_{CPUCLK})

Access: This register can be read or written in 8-bit units.

Address: FFC5 9810$_H$

Value after reset: 0F$_H$

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	WAIT[3:0]			
Value after reset	0	0	0	0	1	1	1	1
R/W	R	R	R	R	R/W	R/W	R/W	R/W

Table 3.1 EEPRDCYCL Register Contents

Bit Position	Bit Name	Function
7 to 4	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
3 to 0	WAIT[3:0]	Number of Wait Cycles RH850/F1KM-S1:

WAIT[3:0]	Number of Wait Cycles	CPU Operation Frequency	
		f_{CPUCLK_M} ≤ 40 MHz	40 MHz < f_{CPUCLK_M} ≤ 80 MHz
0000	1	✓	Setting prohibited
0001	2	✓	✓
0010	3	✓	✓
0011	4	✓	✓
0100	5	✓	✓
0101	6	✓	✓
0110	7	✓	✓
0111	8	✓	✓
1000	9	✓	✓
Other than above	10	✓	✓

NOTES

1. The read access time to the data flash is calculated by the number of wait cycles.
   RH850/F1KM-S1:
   Read access time to the data flash = {17 + (Number of wait cycles × 4)} / CPU operating frequency
   However, the time may be changed depending on the combination of instructions before and after the execution.
2. ✓ indicates the number of wait cycles that can be set.

Section 4 Electrical Characteristics

4.1 General Measurement Condition

4.1.1 Common Condition

- Operating temperature
  - Tj = –40 to +160°C @ R7F7016xxFAFP

    xx = 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95

    Regarding operation temperature of each product, see **Section 1.2, Product Lineup**.

4.2 Absolute Maximum Rating

4.2.1 Temperature Condition

Table 4.1 Temperature Condition

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Storage temperature	Tstg		–55		160	°C
Junction temperature	Tj	R7F7016xxFAFP	–40		160	°C

xx = 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95

Regarding operation temperature of each product, see **Section 1.2, Product Lineup**.

4.3 Operational Condition

4.3.1 Recommended Operating Condition

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CPU clock frequency	f_{CPUCLK_M}				80	MHz
	f_{CPUCLK_L}	for OSTMn			40	MHz

4.4 PLL Characteristics

4.4.1 PLL1 (for CPU/Peripheral) Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V, AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF ±30%, CISOVCL: 0.1 µF ±30%, Tj = –40 to (depend on the product) °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output frequency	$f_{CPLL1OUT}$	MainOSC		80		MHz

4.5 Power Supply Currents

Condition: REGVCC, EVCC, A0VREF total current. But the I/O buffer is stopped.

Item	Symbol	Condition				MIN.	TYP.*1	MAX	Unit
		CPU	PLL	Tj	Peripheral*2				
RUN mode current	IDDR	Run (80 MHz)	Run	–40 to 160°C	Run(#1)		28	80	mA
				25°C	Stop(#1)		19		mA
RUN mode current (During data/code flash programming)	IDDR3	Run (80 MHz)	Run	–40 to 160°C	Run(#2)		39	95	mA
RUN mode current (HALT state)	IDDH	Run (80 MHz)	Run	–40 to 160°C	Run(#3)		22	65	mA

Item	Symbol	Condition				MIN.	TYP.*1	MAX	Unit
		CPU	PLL	Tj	Peripheral*2				
STOP mode current	IDDS	Stop	Stop	–40 to 90°C	Stop(#2)		0.7	12	mA
				110°C	Stop(#2)			17	mA
				135°C	Stop(#2)			31	mA
				145°C	Stop(#2)			40	mA
DeepSTOP mode current	IDDDS	Power off	Power off	–40 to 85°C	Stop(#3)		50	470	μA
				105°C	Stop(#3)			830	μA
				125°C	Stop(#3)			1370	μA
				135°C	Stop(#3)			1750	μA
Cyclic RUN mode current	IDDCR	Run (HS IntOSC)	Stop	–40 to 90°C	Stop(#4)		3.6	21	mA
				115°C	Stop(#4)			28	mA
				135°C	Stop(#4)			40	mA
				145°C	Stop(#4)			65	mA
Cyclic STOP mode current	IDDCS	Stop	Stop	–40 to 90°C	Stop(#5)		1.1	13	mA
				110°C	Stop(#5)			18	mA
				135°C	Stop(#5)			32	mA
				145°C	Stop(#5)			50	mA

Note 1. The condition of “TYP.” shows the specification with the following conditions. Also, the value is just for reference only.
- Tj = 25°C
- REGVCC = EVCC = A0VREF = 5.0 V
- AWOVSS = EVSS = A0VSS = 0 V

Note 2. Operating condition of each peripheral function is shown in the *RH850/F1KH, RH850/F1KM User`s Manual: Hardware*.

CAUTION

It must be ensured that the junction temperature in the Ta range remains below Tj ≤ 160°C and does not exceed its limit under application conditions (thermal resistance, power supply current, peripheral current (if not included in power supply current), port output current and injection current).

RH850/F1KM-S1 User’s Manual: Hardware

Publication Date: Rev.1.00 August 20, 2021

Published by: Renesas Electronics Corporation

RH850/F1KM-S1

Renesas Electronics Corporation

R01UH0956EJ0100