User's Manual

32

RH850/E2M

Electrical Characteristics

User's Manual: Hardware

Renesas microcontroller

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Notes for CMOS devices

(1) Voltage application waveform at input pin: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) Handling of unused input pins: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to power supply or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) Precaution against ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) Status before initialization: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) Power ON/OFF sequence: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) Input of signal during power off state: Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

Table of Contents

Section 1 Electrical Characteristics

1.1 Absolute Maximum Ratings

Table 1.1 lists absolute maximum ratings.

Table 1.1 Absolute Maximum Ratings

Item		Symbol	Rated Value	Unit	Note
Power voltage*[1]	SYSVCC, VCC	VCC	−0.3 to +6.5	V	
	E0VCC, E1VCC, E2VCC	E0VCC, E1VCC, E2VCC	−0.3 to +6.5	V	
	VDD	VDD	–0.3 to +1.8	V	
	LVDVCC	LVDVCC	−0.3 to +6.5	V	
Input voltage	SYSVCC power pin	Vin	−0.3 to SYSVCC +0.3	V	See **Table 1.2**
	VCC power pin	Vin	−0.3 to VCC +0.3	V	
	E0VCC, E1VCC, E2VCC power pins	Vin	−0.3 to E0VCC +0.3 −0.3 to E1VCC +0.3 −0.3 to E2VCC +0.3	V	
	LVDVCC power pin	V_{LVDSIN}	−0.3 to LVDVCC + 0.3	V	
	5 V tolerant pin*[2]	Vin	−0.3 to +5.8	V	
Analog power voltage		A0VCC, A1VCC, A2VCC, A3VCC	−0.3 to +6.5	V	A1VCC, A3VCC is only BGA373 package
		ADSVCC	−0.3 to +6.5	V	
Analog reference voltage		A0VREFH	−0.3 to A0VCC +0.3	V	A1VREFH, A3VREFH is only BGA373 package
		A1VREFH	−0.3 to A1VCC +0.3	V	
		A2VREFH	−0.3 to A2VCC +0.3	V	
		A3VREFH	−0.3 to A3VCC +0.3	V	
		ADSVREFH	−0.3 to ADSVCC +0.3	V	
		ADSVREFL	−0.3 to ADSVSS +0.3	V	
Analog input voltage		V_{AIN}	−0.3 to A0VCC +0.3 −0.3 to A1VCC +0.3 −0.3 to A2VCC +0.3 −0.3 to A3VCC +0.3	V	A1VCC, A3VCC is only BGA373 package
		V_{ADSIN}	−0.3 to ADSVCC +0.3	V	
VSS differential voltage*[3] (Condition: Between any two of VSS, A0VSS, A1VSS, A2VSS, A3VSS, ADSVSS.)			−0.1 to +0.1	V	A1VSS, A3VSS is only BGA373 package
Maximum input current (per pin)	Digital input pin	Imax	−25 to +25	mA	Only 1 pin at a time
	Analog input pin	Imax	−25 to +25	mA	
Junction temperature*[1]		Tj	−40 to +150	°C	
Storage temperature		Tstg	−55 to +150	°C	After mounting

Note 1. Cumulative hours of operation of this LSI with Tj in the range from 125°C to 150°C must be kept to less than 3000 hours.

Note 2. Pins below described as “(5 V tol.)” in **Section 1.2.1, Relationship between Power Name and Pin**.
MD0, MD1, $\overline{\text{RES\_IN}}$, $\overline{\text{TRST}}$, NMI.

Note 3. If it is not necessary to identify E0VCC, E1VCC and E2VCC specifically, it is sometimes described as “EVCC”.

NOTE

Using this LSI without observing these absolute maximum ratings may result in permanent breakdown of the LSI. This product is used with a combination of multiple power voltages simultaneously in some cases. Use this LSI conforming to power pin connections, conditions for combination of power voltages to be applied, voltages that can be applied to pins, and output voltage conditions, which are specified in the manual. Using this LSI with unspecified power connections or voltages may result in permanent breakdown of the LSI or damage to the system that contains this LSI.

1.2 DC Characteristics

1.2.1 Relationship between Power Name and Pin

Regarding the relationship between power name and pin, please refer to each sheet of "E02-01_List of Alternative Functions.xlsx" file.

1.2.2 Operating Conditions

Table 1.2 Operating Conditions

Symbol	Condition	Min.	Typ.	Max.	Unit
SYSVCC		3.0	3.3	3.6	V
		4.5	5.0	5.5	V
VCC		3.0	3.3	3.6	V
		4.5	5.0	5.5	V
VDD		1.2	1.275	1.35	V
E0VCC*4		4.5	5.0	5.5	V
E1VCC*4	Using Ethernet, CSIH only	3.0	3.3	3.6	V
	The others	4.5	5.0	5.5	V
E2VCC*4	Using Ethernet, RHSB, CSIH only	3.0	3.3	3.6	V
	The others	4.5	5.0	5.5	V
LVDVCC*5		3.0	3.3	3.6	V
		4.5	5.0	5.5	V
A0VCC*3, A1VCC*3, A2VCC*3, A3VCC*3		4.5	5.0	5.5	V
ADSVCC*3		4.5	5.0	5.5	V
A0VREFH, A1VREFH, A2VREFH, A3VREFH*1		4.5	5.0	5.5	V
ADSVREFH*2		4.5	5.0	5.5	V
Tj (Junction temperature)		−40 to +150			°C

Note: Supply the specified voltages to all power-supply voltage connections when starting operation. Turn off all power voltages when stopping operation. In power-off standby mode, turn off power voltages other than SYSVCC.

Note 1. Set a value not greater than A0VCC, A1VCC, A2VCC and A3VCC.

Note 2. Set a value not greater than ADSVCC.

Note 3. Operated under the condition of A0VCC = A1VCC = A2VCC = A3VCC = ADSVCC.

Note 4. E0VCC, E1VCC and E2VCC are described as EVCC when it is not necessary to distinguish.

Note 5. The combinations of the power connection about E0VCC and LVDVCC, see *Section 11, Power Supply*, for details.

1.2.3 Input Voltage Characteristics

Table 1.3 DC Characteristics (Input Voltage)

Conditions: Power supply voltages and Tj refer to “**Section 1.2.2, Operating Conditions**”
VSS = A0VSS = A1VSS = A2VSS = A3VSS = ADSVSS = ADSVREFL = 0 V

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement Condition
Schmitt trigger input voltage (RES_IN)	V_T+ (V_{IH})	SYSVCC × 0.75	—	5.5 + 0.3	V	See **Section 1.2.1, Relationship between Power Name and Pin**. (RES_IN SYSVCC = 3.0 to 3.6 V)
Schmitt trigger input voltage (RES_IN)	V_T+ (V_{IH})	SYSVCC × 0.7	—	5.5 + 0.3	V	See **Section 1.2.1, Relationship between Power Name and Pin**. (RES_IN SYSVCC = 4.5 to 5.5 V)
Schmitt trigger input voltage (RES_IN)	V_T- (V_{IL})	−0.3	—	SYSVCC × 0.25	V	See **Section 1.2.1, Relationship between Power Name and Pin**. (RES_IN)
Schmitt trigger input voltage (RES_IN)	V_{HS}	SYSVCC × 0.2	—	—	V	
Schmitt trigger input voltage (Buffer type Sch1)	V_T+ (V_{IH})	E0VCC × 0.65 E1VCC × 0.65 E2VCC × 0.65 A0VCC × 0.65 A2VCC × 0.65 VCC × 0.65	—	E0VCC + 0.3 E1VCC + 0.3 E2VCC + 0.3 A0VCC + 0.3 A2VCC + 0.3 VCC + 0.3	V	See **Section 1.2.1, Relationship between Power Name and Pin**. (Item of Sch1 input buffer type)
Schmitt trigger input voltage (Buffer type Sch1)	V_T- (V_{IL})	−0.3	—	E0VCC × 0.35 E1VCC × 0.35 E2VCC × 0.35 A0VCC × 0.35 A2VCC × 0.35 VCC × 0.35	V	
Schmitt trigger input voltage (Buffer type Sch1)	V_{HS}	0.4	—	—	V	See **Section 1.2.1, Relationship between Power Name and Pin**. (Item of Sch1 input buffer type E0VCC = E1VCC = E2VCC = A0VCC = A2VCC = VCC = 4.5 V to 5.5 V).
Schmitt trigger input voltage (Buffer type Sch1)	V_{HS}	0.3	—	—	V	See **Section 1.2.1, Relationship between Power Name and Pin**. (Item of Sch1 input buffer type E1VCC = E2VCC = VCC = 3.0 V to 3.6 V).
Schmitt trigger input voltage (Buffer type Sch2*2)	V_T+ (V_{IH})	SYSVCC × 0.75 VCC × 0.75	—	5.5 + 0.3	V	See **Section 1.2.1, Relationship between Power Name and Pin**. (Item of Sch2 input buffer type)
Schmitt trigger input voltage (Buffer type Sch2*2)	V_T- (V_{IL})	−0.3	—	SYSVCC × 0.25 VCC × 0.25	V	
Schmitt trigger input voltage (Buffer type Sch2*2)	V_{HS}	SYSVCC × 0.2 VCC × 0.2	—	—	V	

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement Condition
Schmitt trigger input voltage (Buffer type SchMSC*[1])	V_T+ (V_{IH})	E0VCC × 0.6 E2VCC × 0.6	—	E0VCC + 0.3 E2VCC + 0.3	V	See **Section 1.2.1, Relationship between Power Name and Pin**. (Item of SchMSC input buffer type)
	V_T- (V_{IL})	−0.3	—	E0VCC × 0.36 E2VCC × 0.36	V	
	V_{HS}	E0VCC × 0.082 E2VCC × 0.082	—	—	V	
TTL input voltage	V_{IH}	2.2	—	E0VCC + 0.3 E1VCC + 0.3 E2VCC + 0.3 VCC + 0.3	V	See **Section 1.2.1, Relationship between Power Name and Pin**. (Item of TTL input buffer type)
	V_{IL}	−0.3	—	0.8	V	
Clock input voltage (EXTAL)	V_{IH}	VCC × 0.7	—	VCC + 0.3	V	
	V_{IL}	−0.3	—	VCC × 0.2	V	

Note 1. The pins that are supported with the SchMSC input is shown in Appendix file “*E02-01_List of Alternative Functions.xlsx*”.

Note 2. Except for RES_IN.

1.2.4 Input Leakage Current Characteristics

Table 1.4 DC Characteristics (Input Leak Current)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement Condition
Input leakage current	Other than LVDS and A/D port	| Iin |	—	—	1	μA	Vin = 0 V to E0VCC, E1VCC, E2VCC Vin = 0 V to SYSVCC, Vin = 0 V to VCC
	LVDS port	| Iin |	—	—	1	μA	Vin = 0 V to E0VCC, Vin = 0 V to LVDVCC
	A/D port	| Iin |	—	—	0.1	μA	Vin = 0 V to A0VCC, A1VCC, A2VCC, A3VCC Vin = 0 V to ADSVCC

1.2.5 Pull-Up / Pull-Down MOS Current Characteristics

Table 1.5 DC Characteristics (Pull-Up / Pull-Down MOS Current)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement Condition
Input pull-up MOS current	TMS, TDI, TDO, TCK, DRDY (Including use as JTAG port)	$-I_{pu}$	—	—	350	μA	Vin = 0 V VCC = 3.0 to 3.6 V or 4.5 to 5.5 V
	E0VCC, E1VCC, E2VCC power pin (Excluding SchMSC enabled pin)		—	—	350	μA	Vin = 0 V E0VCC = 4.5 to 5.5 V E1VCC = 3.0 to 3.6 V or 4.5 to 5.5 V E2VCC = 3.0 to 3.6 V or 4.5 to 5.5 V
	E0VCC, E2VCC power pin (SchMSC enabled pin*[1])		15	—	90	μA	Vin = 0 V E2VCC = 3.0 to 3.6 V
			40	—	190	μA	Vin = 0 V E0VCC = 4.5 to 5.5 V E2VCC = 4.5 to 5.5 V
Input pull-down MOS current	$\overline{\text{RES\_IN}}$	I_{pd}	—	—	110	μA	Vin = SYSVCC, SYSVCC = 3.0 to 3.6 V or 4.5 to 5.5 V
	$\overline{\text{TRST}}$		—	—	350	μA	Vin = SYSVCC, SYSVCC = 3.0 to 3.6 V or 4.5 to 5.5 V
	TMS, TDI, TDO, TCK, DRDY		—	—	350	μA	Vin = VCC, VCC = 3.0 to 3.6 V or 4.5 to 5.5 V
	MD0, MD1 (SYSVCC power pin)		—	—	350	μA	Vin = SYSVCC, SYSVCC = 3.0 to 3.6 V or 4.5 to 5.5 V
	NMI		—	—	350	μA	Vin = VCC, VCC = 3.0 to 3.6 V or 4.5 to 5.5 V
	E0VCC, E1VCC, E2VCC power pin (Excluding SchMSC enabled pin)		—	—	350	μA	Vin = E0VCC, E0VCC = 4.5 to 5.5 V Vin = E1VCC, E1VCC = 3.0 to 3.6 V or 4.5 to 5.5 V Vin = E2VCC, E2VCC = 3.0 to 3.6 V or 4.5 to 5.5 V
	E0VCC, E2VCC power pin (SchMSC enabled pin*[1])		15	—	120	μA	Vin = E2VCC, E2VCC = 3.0 to 3.6 V
			50	—	240	μA	Vin = E0VCC, E0VCC = 4.5 to 5.5 V Vin = E2VCC, E2VCC = 4.5 to 5.5 V

Note 1. The pins that are supported with the SchMSC input is shown in Appendix file "*E02-01_List of Alternative Functions.xlsx*".

1.2.6 Output Voltage Characteristics

Table 1.6 DC Characteristics (Output Voltage)

Conditions: Power supply voltages refer to "**Section 1.2.2, Operating Conditions**"

IOVCC means the pin are assigned to the power supply (EnVCC, VCC and SYSVCC).

Item	Symbol	Measurement Condition*3	Min.	Typ.	Max.	Unit
Drive Strength 1	V_{OH}	I_{OH} = −1mA per pin (16 pins)	IOVCC − 0.7	—	—	V
	V_{OH}	I_{OH} = −500μA per pin (16 pins)	IOVCC − 0.5	—	—	V
	V_{OL}	I_{OL} = 1mA per pin (16 pins)	—	—	0.7	V
	V_{OL}	I_{OL} = 500μA per pin (16 pins)	—	—	0.5	V
Drive Strength 2	V_{OH}	I_{OH} = −2mA per pin (16 pins)	IOVCC − 0.7	—	—	V
	V_{OH}	I_{OH} = −1mA per pin (16 pins)	IOVCC − 0.5	—	—	V
	V_{OL}	I_{OL} = 2mA per pin (16 pins)	—	—	0.7	V
	V_{OL}	I_{OL} = 1mA per pin (16 pins)	—	—	0.5	V
Drive Strength 3	V_{OH}	I_{OH} = −4mA per pin (8 pins)	IOVCC − 0.8	—	—	V
	V_{OH}	I_{OH} = −2mA per pin (8 pins)	IOVCC − 0.5	—	—	V
	V_{OL}	I_{OL} = 4mA per pin (8 pins)	—	—	0.8	V
	V_{OL}	I_{OL} = 2mA per pin (8 pins)	—	—	0.5	V
Drive Strength 4	V_{OH}	I_{OH} = −4mA per pin (8 pins)	IOVCC − 0.8	—	—	V
	V_{OH}	I_{OH} = −2mA per pin (8 pins)	IOVCC − 0.5	—	—	V
	V_{OL}	I_{OL} = 4mA per pin (8 pins)	—	—	0.8	V
	V_{OL}	I_{OL} = 2mA per pin (8 pins)	—	—	0.5	V
RHSB*1	V_{OH}	I_{OH} = −2mA per pin (5 pins)	IOVCC − 0.4	—	—	V
	V_{OL}	I_{OL} = 2mA per pin (5 pins)	—	—	0.4	V
ERROROUT_M*2	V_{OH}	I_{OH} = −4mA per pin	IOVCC − 0.8	—	—	V
	V_{OH}	I_{OH} = −2mA per pin	IOVCC − 0.5	—	—	V
	V_{OL}	I_{OL} = 4mA per pin	—	—	0.8	V
	V_{OL}	I_{OL} = 2mA per pin	—	—	0.5	V

Note 1. The pins multiplexed with functions RHSBnCSDx (n = 0, 1, x = 0, 1) are used as RHSB functions. It should be set drive strength 4 for RHSB use.

Note 2. The drive strength setting of ERROROUT_M pin is fixed as drive strength 4.

Note 3. Maximum pin counts of simultaneous operation is defined in parentheses, simultaneous operation up to the maximum pin count is available for each group only EnVCC power domain (n = 0 to 2). It has no limits for other power domain.

Group01: P10_4 to 9, P10_11, P13_8 to 14
Group02: P00_1, P02_0 to 6, P02_9, P10_10, P10_12 to 14
Group03: P00_0, P00_2 to 11, P01_3 to 7, P02_7 to 8, P02_10 to 11
Group04: P10_0 to 3
Group05: P13_0 to 3, P14_4 to 5
Group06: P13_4 to 7, P14_2 to 3, P14_8 to 11
Group07: P14_0 to 1, P14_6 to 7, P14_12, P15_0 to 8, P24_10 to 11, P24_14
Group08: P20_2 to 7, P24_12 to 13, P24_15, $\overline{\text{RES\_OUT}}$
Group09: P20_0 to 1, P21_2 to 5, P22_12, P24_8 to 9
Group10: P22_0, P22_2 to 4, P22_6 to 11, P22_13
Group11: P22_1, P22_5, P23_0 to 7, P24_3, P24_6 to 7
Group12: P24_0 to 2, P24_4 to 5, P25_0 to 6, P30_0 to 3, P32_2 to 6
Group13: P32_0 to 1, P33_4, P33_6 to 12
Group14: P33_0 to 3, P33_5, P33_13, P34_0 to 4
Group15: P11_0 to 10
Group16: P12_0 to 9

1.2.7 Allowable Output Current

Table 1.7 DC Characteristics (Allowable Output Current)

Item	Symbol	Min.	Typ.	Max.	Unit
Output low-level allowable current (per pin)	I_{OL}	—	—	4.0	mA
Output low-level allowable current (total)	$\Sigma\ I_{OL}$	—	—	80	mA
Output high-level allowable current (per pin)	I_{OH}	—	—	4.0	mA
Output high-level allowable current (total)	$\Sigma\ I_{OH}$	—	—	80	mA

1.2.8 Injection Current

Table 1.8 DC Characteristics (Injection Current)

Item		Symbol	Min.	Typ.	Max.	Unit
DC injection current (per pin)	Logic pin*1	I_{IC}	−2.0	—	2.0	mA
	Analog pin		−3.0	—	3.0	mA
DC injection current (total)		$\Sigma\ \vert I_{IC}\vert$	−50	—	50	mA

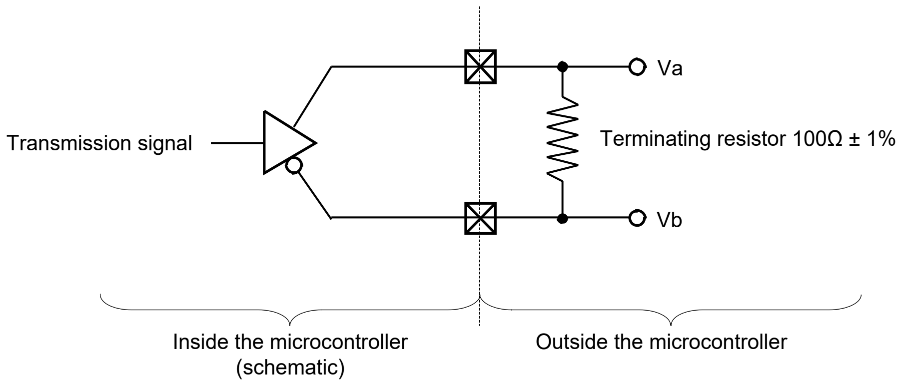
Note 1. Injection current to the logic pin multiplexed with the LVDS function is prohibited when the LVDS function is used. When the LVDS function is not used, Injection current to the logic pin multiplexed with the LVDS function causes at maximum an additional 1 µA leakage current at the complimentary P/N pin. For example, injection current to RHSB0FCLP causes at maximum an additional 1 µA leakage current at RHSB0FCLN.

1.2.9 LVDS Driver

Table 1.9 DC Characteristics (LVDS Driver (ANSI/TIA/EIA-644 standard) Characteristics)

Conditions: E0VCC = 4.5 V to 5.5 V

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement Condition
Output differential voltage	V_{OD}	250	—	450	mV	**Figure 1.1**, **Figure 1.2**
Offset voltage	V_{OS}	1125	—	1375	mV	



Note: Combinations of pins (P) and pins (N)
RHSB*FCLP / RHSB*FCLN
RHSB*SOP / RHSB*SON
HSSPI*_CLKP / HSSPI*_CLKN
HSSPI*_TXDP / HSSPI*_TXDN

Figure 1.1 LVDS Driver Va / Vb Measurement Conditions

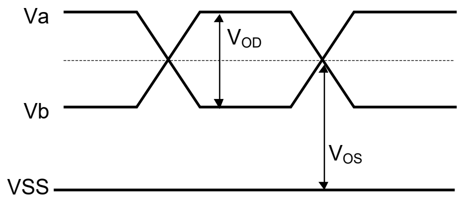
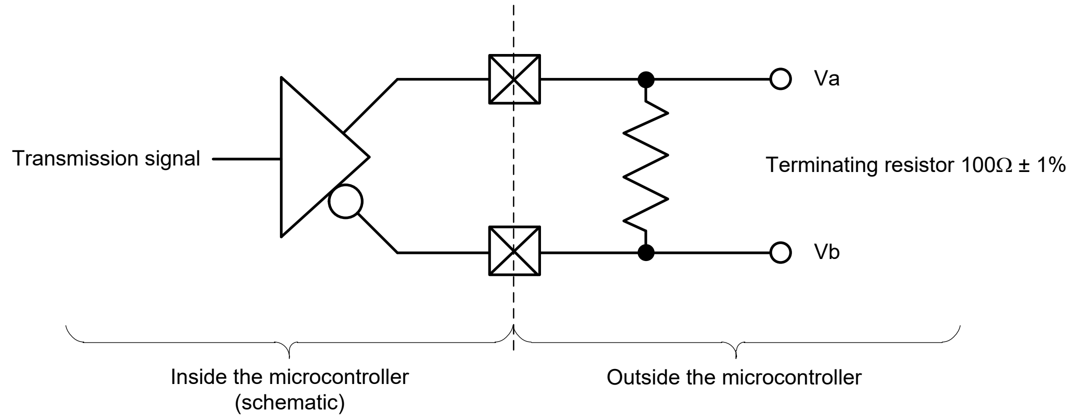


Figure 1.2 Definition of LVDS Driver Symbols

Table 1.10 DC Characteristics (LVDS Driver (based on IEEE 1596.3-1996) Characteristics)

Conditions: LVDVCC = 3.0 V to 3.6 V or 4.5 V to 5.5 V

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement Condition
Output high-level voltage	V_{OH}	—	—	1400	mV	**Figure 1.3**, **Figure 1.4**
Output low-level voltage	V_{OL}	1000	—	—	mV	
Output differential voltage	V_{OD}	150	—	250	mV	
Offset voltage	V_{OS}	1125	—	1275	mV	
Output impedance	R_O	40	—	140	Ω	



Note: Combinations of pins (P) and pins (N)
RHSIF*TXDP / RHSIF*TXDN

Figure 1.3 LVDS Driver Va / Vb Measurement Conditions

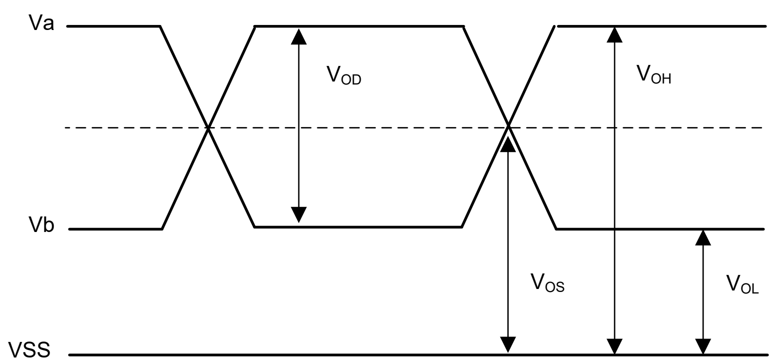


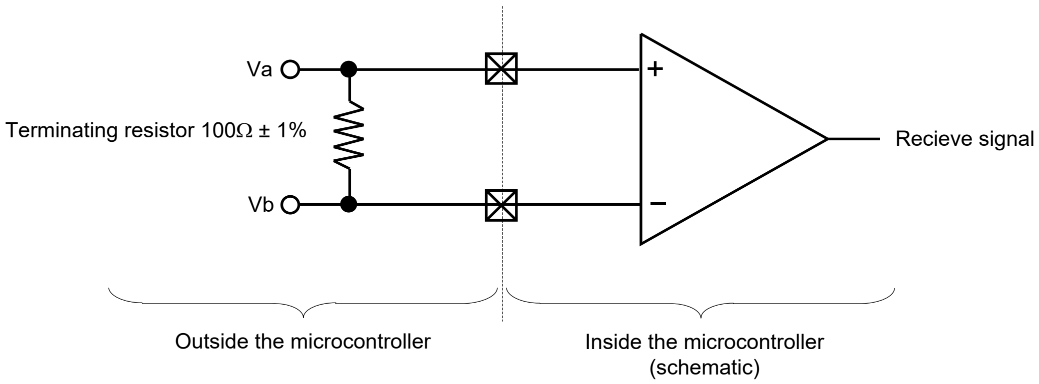
Figure 1.4 Definition of LVDS Driver Symbols

1.2.10 LVDS Receiver

Table 1.11 DC Characteristics (LVDS Receiver (ANSI/TIA/EIA-644 standard) Characteristics)

Conditions: E0VCC = 4.5 V to 5.5 V

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement Condition
Input differential threshold	V_{idth}	−100	—	100	mV	**Figure 1.5**, **Figure 1.6**
Input voltage	V_{in}	0	—	2.4	V	
Input current	$\|I_{ia}\|, \|I_{ib}\|$	—	—	20	μA	
Input differential current	$\|I_a - I_b\|$	—	—	6	μA	



Note: Combinations of pins (P) and pins (N)
HSSPI*_CLKP / HSSPI*_CLKN
HSSPI*_RXDP / HSSPI*_RXDN

Note: Be sure to connect a terminating resistor of the LVDS receiver nearest the microcontroller, because it isn't built in the microcontroller.

Figure 1.5 LVDS Receiver Va / Vb Measurement Conditions

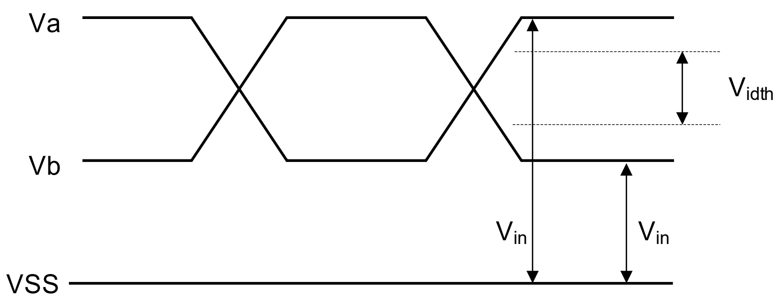
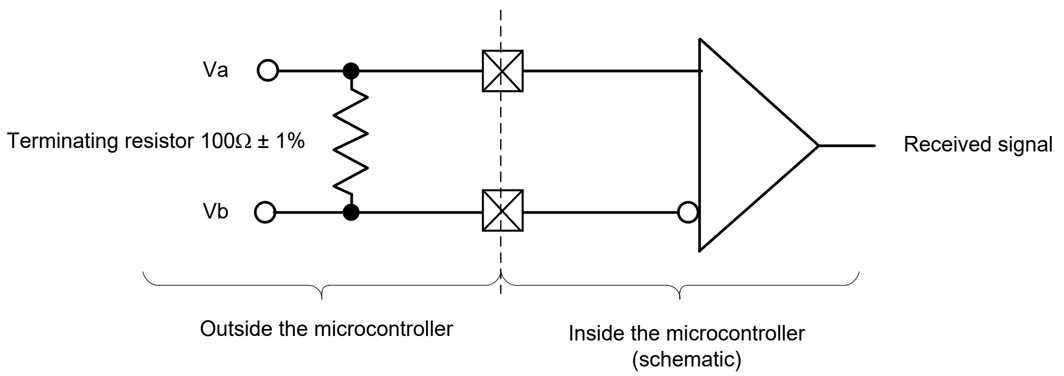


Figure 1.6 Definition of LVDS Receiver Symbols

Table 1.12 DC Characteristics (LVDS Receiver (based on IEEE 1596.3-1996) Characteristics)

Conditions: LVDVCC = 3.0 V to 3.6 V or 4.5 V to 5.5 V

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement Condition
Differential Input threshold voltage	V_{idth}	−100	—	100	mV	**Figure 1.7**, **Figure 1.8**
Common-mode voltage	V_{cm}	825	—	1575	mV	
Input current	$\lvert I_{ia}\rvert$, $\lvert I_{ib}\rvert$	—	—	20	μA	
Input differential current	$\lvert I_a - I_b\rvert$	—	—	6	μA	



Note: Combinations of pins (P) and pins (N)
RHSIF*RXDP / RHSIF*RXDN

Note: Be sure to connect a terminating resistor of the LVDS receiver nearest the microcontroller, because it isn't built in the microcontroller.

Figure 1.7 LVDS Receiver Va / Vb Measurement Conditions

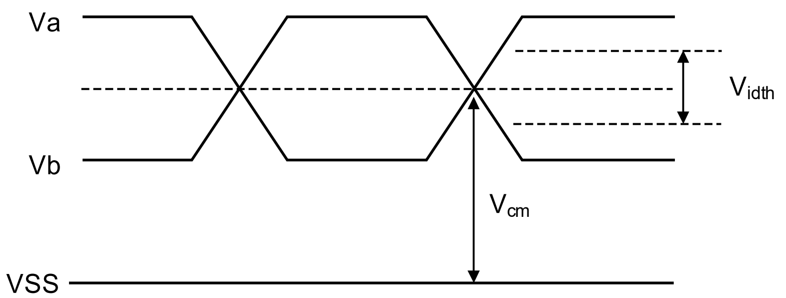


Figure 1.8 Definition of LVDS Receiver Symbols

1.2.11 Input Capacitance

Table 1.13 DC Characteristics (Input Capacitance)

Conditions: E0VCC = E1VCC = E2VCC = 4.5 V to 5.5 V

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement Condition
Input capacitance	All ports*1	C_{in}	—	—	10	pF	Vin = 0 V, f = 1 MHz, Tj = 25°C

Note 1. EXTAL and XTAL are excluded. About EXTAL and XTAL configuration, see *Section 15, Clock Controller*.

1.2.12 Supply Current Characteristics

Table 1.14 DC Characteristics (Supply Current)

Item		Symbol	Min.	Typ.*1	Max.	Unit	Measurement Condition
Core supply current (VDD power)	Normal operation	I_{dd}	—	800	1500	mA	Operation at 400 MHz
	Current during reset	I_{ddrst}	260	340	1100	mA	
VCC supply current	Normal operation (excluding erasure of code flash)	I_{CC}	—	23	65	mA	
	Erasure of code flash	$I_{cc\_cferase}$	—	64	105	mA	
	Current during reset	I_{ccrst}	4	12	45	mA	
System supply current (SYSVCC)	Normal operation	I_{SYS}	—	0.25	1	mA	
	Current during reset	I_{sysrst}	0.1	0.3	2	mA	
E0VCC LVDS supply current	RHSB operation	I_{LVDS}	—	12	17	mA	1 ch
	HSSPI operation	I_{HSSPI}	—	14	20	mA	1 ch
LVDVCC LVDS supply current	RHSIF operation	I_{RHSIF}	—	12	16	mA	1 ch
Analog power current (A0VCC, A1VCC, A2VCC, A3VCC)		I_{AVCC}	—	7	13	mA	Total Channel
Analog power current (ADSVCC)		I_{ADSVCC}	—	14	20	mA	Total Channel
ADC reference power current (A0VREFH, A1VREFH, A2VREFH, A3VREFH)		I_{AVREF}	—	440	1000	μA	Total Channel
ADC reference power current (ADSVREFH)		I_{AVREF_DS}	—	600	1000	μA	Total Channel

Note 1. At Tj = 25°C

CAUTIONS

1. Even if the A/D converter is not used or it is in the standby state, do not open the A0VCC pin, A1VCC pin, A2VCC pin, A3VCC pin, A0VREFH pin, A1VREFH pin, A2VREFH pin, A3VREFH pin, ADSVREFH pin, ADSVREFL pin, A0VSS pin, A1VSS pin, A2VSS pin, A3VSS pin, and ADSVSS pin.
2. Supply current values are with all output pins unloaded when V_{IH}min = VCC − 0.5 V / E0VCC − 0.5 V / E1VCC − 0.5 V / E2VCC − 0.5 V and V_{IL} = 0.5 V.

1.2.13 Standby Current

Table 1.15 DC Characteristics (Standby)

Conditions: SYSVCC = SYSVCCLow, Other power supply voltages = 0 to Operation voltage,
VSS = A0VSS = A1VSS = A2VSS = A3VSS = ADSVSS = ADSVREFL = 0 V

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement Condition
Supply current (SYSVCC)	Power-off standby	I_{SB}	—	—	0.1	mA	−40°C < Tj ≤ 25°C
			—	—	1	mA	25°C < Tj ≤ 105°C
			—	—	1.5	mA	105°C < Tj ≤ 150°C

1.2.14 POC Characteristics

Table 1.16 POC Characteristics*1

Conditions: Tj refer to "**Section 1.2.2, Operating Conditions**"

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection threshold voltage	V_{POC}	—	2.4	2.55	2.7	V

Note 1. POC monitors the SYSVCC supply voltage.

1.2.15 Primary Detection of Voltage Monitor (VMON) Characteristics

Table 1.17 VMON Characteristics

Conditions: Power supply voltages and Tj refer to "**Section 1.2.2, Operating Conditions**"
VSS = A0VSS = A1VSS = A2VSS = A3VSS = ADSVSS = ADSVREFL = 0 V

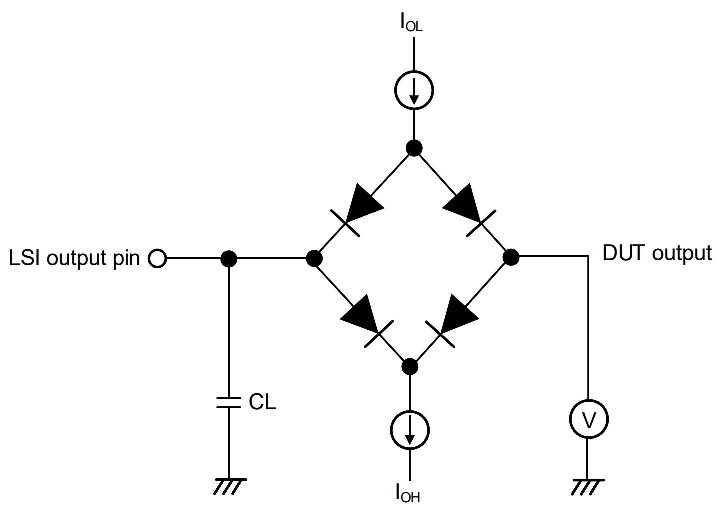
Item	Symbol	Condition	Min.	Max.	Unit
VDD primary high detection level	V_{VDDMH}		1.35	1.45	V
VDD primary low detection level	V_{VDDML}	Assisted by the Delay Monitor (DMON)	1.15	1.2	V
VCC primary high detection level	V_{VCCMH}		5.5	5.9	V
VCC primary low detection level	V_{VCCML}		2.7	3.0	V
E0VCC primary high detection level	V_{EVCCMH}		5.5	5.9	V
E0VCC primary low detection level	V_{EVCCML}		2.7	3.0	V
VMON delay time	t_{DVMON}		—	10	μs

1.3 AC Characteristics

Unless otherwise described, the following timing conditions are applied.

Conditions: Power supply voltages and Tj refer to "**Section 1.2.2, Operating Conditions**"
VSS = A0VSS = A1VSS = A2VSS = A3VSS = ADSVSS = ADSVREFL = 0V

- In the port control register, conditions where all output pins of the module used for the same channel are set to the same driving ability are applied to output pins whose driving ability is selectable. Unless otherwise specified, all driving ability settings are included.
- Unless otherwise described, AC measurement conditions described in AC Measurement Conditions are applied.
  Input reference level
    High level: V_{IH} minimum value; Low level: V_{IL} maximum value
  Output reference level
    High level: 2.0 V; Low level: 0.8 V
  Input rise time, fall time: 1 ns



Note 1. CL is a total value including the capacitance of the measuring equipment.
Each pin setting value, please refer to conditions of each table.

Note 2. I_{OH} = 200 μA, I_{OL} = 1.6 mA

Figure 1.9 AC Measurement Conditions

1.3.1 Power On / Off Timing

Table 1.18 Power On / Off Timing

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset hold time at power-on	t_{RESH1}	Power-up*1	1.3	—	—	ms
Power hold time at reset assertion	t_{PWH}	Power-down*2	2	—	—	µs
Operating mode setup time at power-on	t_{MDS1}	—	t_{RESH1}	—	—	ms
Operating mode setup time at reset assert	t_{MDS2}	—	1	—	—	ms
Operating mode hold time at reset negate	t_{MDH1}	—	1	—	—	ms
Operating mode hold time at power-off	t_{MDH2}	—	0	—	—	µs
$\overline{\text{TRST}}$ setup time at reset	t_{TRMDS}	—	2	—	—	µs
$\overline{\text{TRST}}$ hold time at reset negate*4	t_{TRMDH}	—	30	—	—	ms
$\overline{\text{TRST}}$ hold time at power-on	t_{TRSTH1}	—	1.29	—	—	ms
Oscillator stabilization time	t_{OSC}	—	—	—	5.5	ms
PLL lock in time	t_{PLLL}	*3	—	—	1	ms

Note 1. t_{RESH1} is the reset time required for the supply of internal clock signals to become stable after all power supplies are turned on. There are no restrictions on the rising order of each power supply.

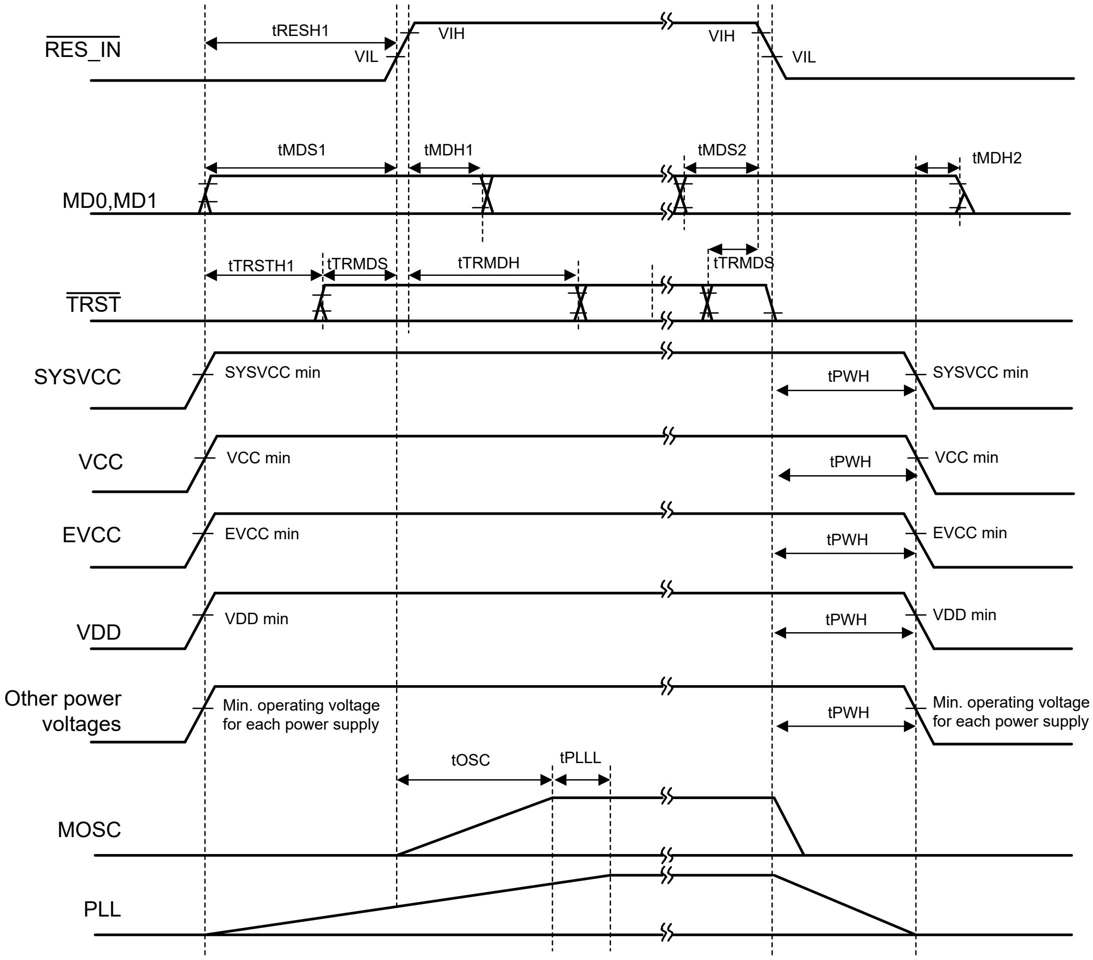
Note 2. t_{PWH} is the time from assertion of the reset signal until any of the power voltages have dropped below the lower-limit voltages. There are no restrictions on the falling order of each power supply.

Note 3. t_{PLLL} is the time required for PLL to lock after MOSC oscillation has become stable.

Note 4. Access by the Nexus, LPD and BSCAN during t_{TRMDH} duration is prohibited. (both of High and low condition of $\overline{\text{TRST}}$)

CAUTION

- The states of I/O pins are not reset during the noise cancellation interval of the reset signal following its assertion while power is being turned off. During that time, do not allow any input of mid-range potential to the pin or contention of output data.
- If power is disconnected during programming or erasure of flash memory, the contents of the flash memory may be destroyed.



Note 1. The MD0 and MD1 pins must not change when $\overline{\text{RES\_IN}}$ is negated and asserted, in order not to change the operation mode at $\overline{\text{RES\_IN}}$ assert.

Figure 1.10 Power On / Off Timing

1.3.2 Standby Transition / Return Timing

Table 1.19 Power-Off Standby Timing

Item	Symbol	Condition	Min.	Max.	Unit
Reset hold time at return from power-off standby mode	t_{RESH2}	—	t_{RESH1}	—	ms
$\overline{\text{TRST}}$ hold time at return from power-off standby mode	t_{TRSTH2}	—	t_{TRSTH1}	—	ms
voltage at transition to power-off standby mode*1	Vstdby1	—	2.6	—	V
SYSVCC voltage in power-off standby mode	SYSVCCLow	—	2.7	5.5	V
Power hold voltage for EVCC power supply	VoltageMin	—	2.7	—	V

Note 1. This is the voltage for transition to power-off standby mode. This value must be equal to or less than the min. Vstdby1 value. Both VCC and EVCC must be less than Vstdby1.

CAUTION

For resetting while flash memory is being programmed or erased, follow the specifications in *the RH850/E2x Flash Memory User's Manual: Hardware Interface*.

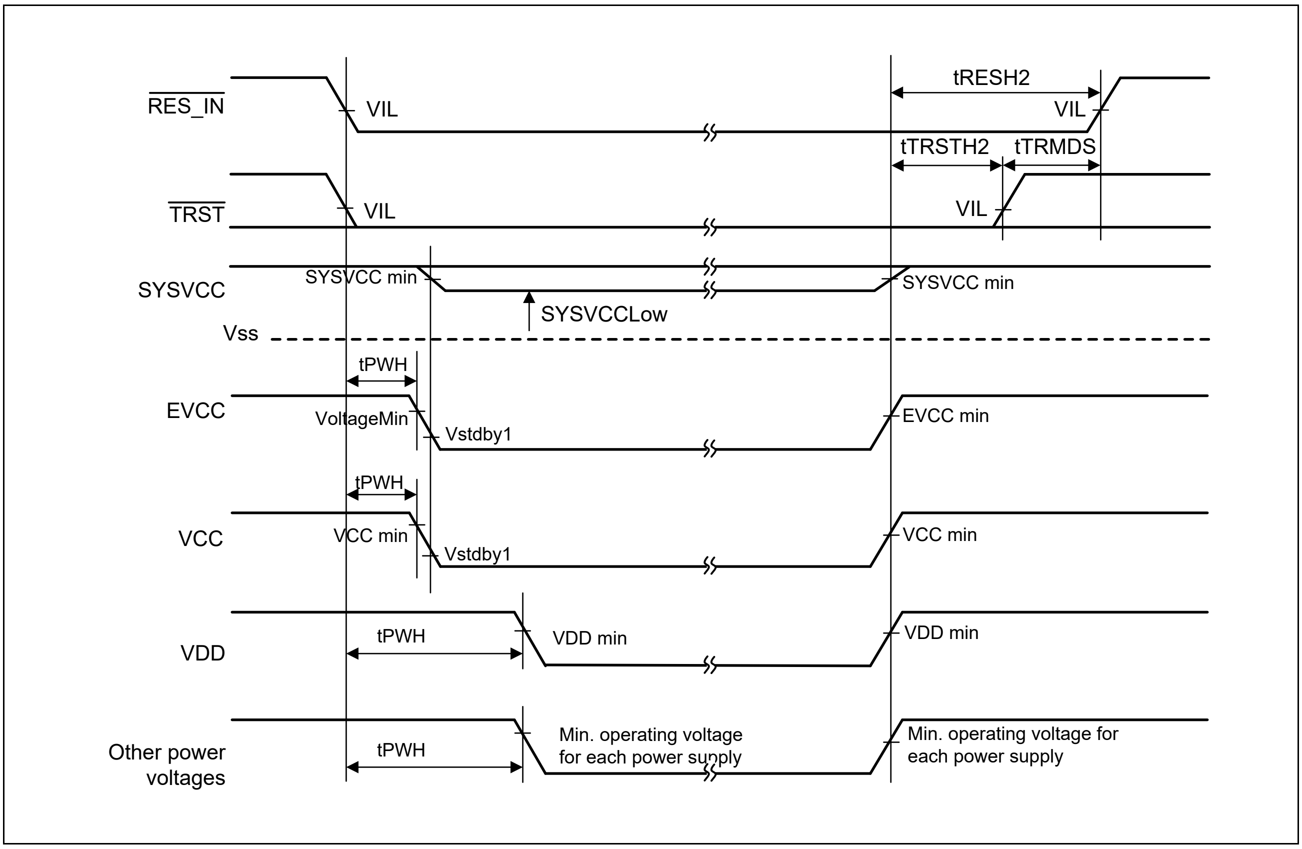


Figure 1.11 Power-Off Standby Timing

1.3.3 Clock Timing

1.3.3.1 Main Oscillator Characteristics

Table 1.20 Main Oscillator Characteristics (1/3)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
MainOsc frequency*1 (OPBT setting)	f_{MOSC}	Crystal (20 MHz)		—	20	—	MHz
MainOsc frequency*1 (OPBT setting)	f_{MOSC}	Crystal (40 MHz)			40		MHz
MainOsc oscillation operating point	V_{MOSCOP}	Crystal		—	0.5 × VCC	—	V
MainOsc oscillation amplitude	$V_{MOSCAMP}$	Crystal		0.295 × VCC	—	—	V
MainOsc oscillation stabilization time	t_{MSTB}	Crystal		—	—	5	ms
MainOsc oscillation amplifier reaction time	$t_{MOSCAMP}$	Crystal		—	—	200	µs
Internal Capacitor size selectable by CAP_SEL setting (OPBT setting)*2	Ccapsel	CAP_SEL[3:0]	= 0000b	*4	0 (4.9), 0 (6.0)*3	*4	pF
			= 0001b	*4	1 (5.7), 1 (6.9)*3	*4	pF
			= 0010b	*4	2 (6.6), 2 (7.8)*3	*4	pF
			= 0011b	*4	3 (7.4), 3 (8.6)*3	*4	pF
			= 0100b	*4	4 (8.3), 4 (9.5)*3	*4	pF
			= 0101b	*4	5 (9.1), 5 (10.3)*3	*4	pF
			= 0110b	*4	6 (10.0), 6 (11.2)*3	*4	pF
			= 0111b	*4	7 (10.9), 7 (12.1)*3	*4	pF
			= 1000b	*4	8 (11.7), 8 (12.9)*3	*4	pF
			= 1001b	*4	9 (12.6), 9 (13.8)*3	*4	pF
			= 1010b	*4	10 (13.4), 10 (14.6)*3	*4	pF
			= 1011b	*4	11 (14.3), 11 (15.5)*3	*4	pF
			= 1100b	*4	12 (15.1), 12 (16.3)*3	*4	pF
Internal damping resistor size selectable by RD_SEL setting (OPBT setting)*2	Rrdsel	RD_SEL[2:0]	= 000b	176	327	621	Ω
			= 001b	365	608	1064	Ω
			= 010b	512	853	1365	Ω
			= 011b	670	1116	1786	Ω
			= 100b	804	1340	2010	Ω
			= 101b	959	1599	2399	Ω
			= 110b	1456	2426	3639	Ω
			= 111b	1916	3194	4472	Ω

Table 1.20 Main Oscillator Characteristics (2/3)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Trans conductance size and Output conductance size selectable by SHTSTBY and AMP_SEL setting (OPBT setting)*2	gm (gds)	{SHTSTBY, AMP_SEL[2:0]} VCC = 3.0 V to 3.6 V	= 0000b	2.1 (0.02)	5.9 (0.13)	10.3 (0.28)	mS
			= 0001b	2.7 (0.03)	7.7 (0.17)	13.5 (0.36)	mS
			= 0010b	3.4 (0.03)	9.5 (0.20)	16.6 (0.44)	mS
			= 0011b	4.0 (0.04)	11.3 (0.24)	19.5 (0.52)	mS
			= 0100b	4.7 (0.05)	13.0 (0.28)	22.4 (0.59)	mS
			= 0101b	5.9 (0.06)	16.3 (0.34)	27.9 (0.73)	mS
			= 0110b	7.1 (0.07)	19.5 (0.41)	33.0 (0.86)	mS
			= 0111b	8.2 (0.08)	22.5 (0.47)	37.8 (0.98)	mS
			= 1000b	4.0 (0.04)	11.3 (0.24)	19.6 (0.52)	mS
			= 1001b	4.7 (0.05)	13.0 (0.27)	22.4 (0.59)	mS
			= 1010b	5.3 (0.05)	14.7 (0.31)	25.2 (0.66)	mS
			= 1011b	5.9 (0.06)	16.3 (0.34)	27.9 (0.73)	mS
			= 1100b	6.5 (0.06)	17.9 (0.37)	30.5 (0.80)	mS
			= 1101b	7.7 (0.07)	21.0 (0.44)	35.5 (0.92)	mS
			= 1110b	8.8 (0.08)	23.9 (0.50)	40.2 (1.04)	mS
			= 1111b	9.9 (0.10)	26.7 (0.56)	44.6 (1.15)	mS
Trans conductance size and Output conductance size selectable by SHTSTBY and AMP_SEL setting (OPBT setting)*2	gm (gds)	{SHTSTBY, AMP_SEL[2:0]} VCC = 4.5 V to 5.5 V	= 0000b	3.4 (0.13)	7.9 (0.30)	12.7 (0.55)	mS
			= 0001b	4.4 (0.17)	10.3 (0.38)	16.4 (0.71)	mS
			= 0010b	5.4 (0.20)	12.5 (0.46)	19.9 (0.85)	mS
			= 0011b	6.3 (0.23)	14.6 (0.54)	23.1 (0.99)	mS
			= 0100b	7.2 (0.27)	16.6 (0.61)	26.1 (1.12)	mS
			= 0101b	8.9 (0.33)	20.4 (0.75)	31.6 (1.35)	mS
			= 0110b	10.5 (0.39)	23.8 (0.87)	36.5 (1.56)	mS
			= 0111b	11.9 (0.45)	26.9 (0.98)	40.9 (1.75)	mS
			= 1000b	6.3 (0.24)	14.6 (0.54)	23.1 (0.99)	mS
			= 1001b	7.2 (0.27)	16.6 (0.61)	26.1 (1.12)	mS
			= 1010b	8.1 (0.30)	18.6 (0.68)	28.9 (1.24)	mS
			= 1011b	8.9 (0.33)	20.4 (0.75)	31.6 (1.35)	mS
			= 1100b	9.7 (0.36)	22.1 (0.81)	34.1 (1.46)	mS
			= 1101b	11.2 (0.42)	25.4 (0.93)	38.7 (1.66)	mS
			= 1110b	12.6 (0.47)	28.3 (1.04)	42.9 (1.84)	mS
			= 1111b	13.9 (0.52)	31.0 (1.14)	46.7 (2.00)	mS

Table 1.20 Main Oscillator Characteristics (3/3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
EXTAL clock input frequency (OPBT setting)	f_{EX}	EXCLK mode (20 MHz)	19.9	—	20	MHz
		EXCLK mode (40 MHz)	39.8	—	40	MHz
EXTAL clock input cycle time	t_{EXCYC}	EXCLK mode f_{EX} = 20 MHz	—	50	—	ns
		EXCLK mode f_{EX} = 40 MHz	—	25	—	ns
EXTAL clock Input low-level pulse width	t_{EXL}	EXCLK mode f_{EX} = 20 MHz	20	—	—	ns
		EXCLK mode f_{EX} = 40 MHz	10	—	—	ns
EXTAL clock Input high-level pulse width	t_{EXH}	EXCLK mode f_{EX} = 20 MHz	20	—	—	ns
		EXCLK mode f_{EX} = 40 MHz	10	—	—	ns
EXTAL clock rise time	t_{EXR}	EXCLK mode f_{EX} = 20 MHz	—	—	4	ns
		EXCLK mode f_{EX} = 40 MHz	—	—	2.5	ns
EXTAL clock fall time	t_{EXF}	EXCLK mode f_{EX} = 20 MHz	—	—	4	ns
		EXCLK mode f_{EX} = 40 MHz	—	—	2.5	ns

Note 1. The following two crystal resonator frequencies are supported: 20 MHz and 40 MHz.

Note 2. Please refer to *Section 15.4.3, Main OSC Configuration and Stabilization Sequence*.

Note 3. The Ccapsel value is “C_{X1} (with parasitic capacitance to ground), C_{X2} (with parasitic capacitance to ground)”.

Note 4. The capacitor tolerance is ±15%.

CAUTION

The oscillation stabilization time differs according the matching with the external resonator circuit. It is recommended to determine the oscillation stabilization time by an oscillator matching test. For recommended crystal resonators, please contact our sales representative.

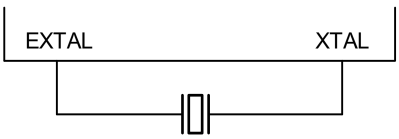


Figure 1.12 Oscillator Circuit Diagram (Crystal without External Components)

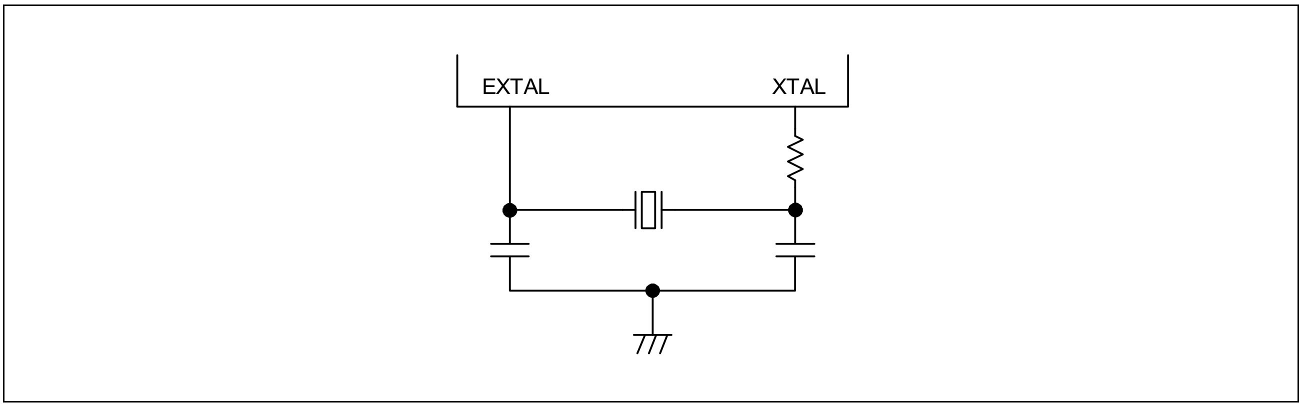


Figure 1.13 Oscillator Circuit Diagram (Crystal with External Components)

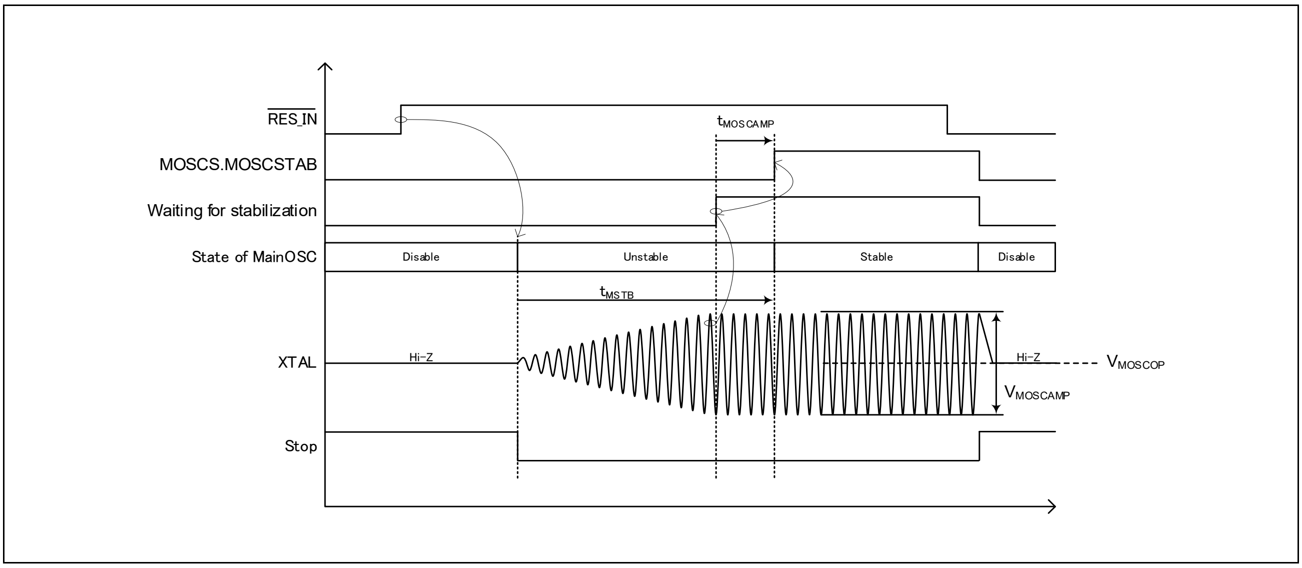


Figure 1.14 Main OSC Stabilization

1.3.3.2 Oscillation Frequency Accuracy of the Internal Oscillator

Table 1.21 Oscillation Frequency Accuracy of Internal Oscillator

Item	Symbol	Min.	Typ.	Max.	Unit
Internal oscillation frequency	f_{IOSC}	95	100	105	MHz

1.3.3.3 Oscillation Frequency Accuracy of the High-voltage Internal Oscillator

Table 1.22 Oscillation Frequency Accuracy of High-voltage Internal Oscillator

Item	Symbol	Min.	Typ.	Max.	Unit
High-voltage Internal Oscillator frequency	f_{HVIOSC}	8	16	24	MHz

1.3.3.4 External Clock Output Timing

Table 1.23 Clock Output Timing

Conditions: CL = 30 pF, Drive strength = 3, E0VCC = 5.0 ± 0.5 V

Item	Symbol	Min.	Typ.	Max.	Unit	Reference
External Clock output frequency	f_{op}	0.4975	0.5	4	MHz	**Figure 1.15**
External Clock output low-level pulse width	t_{CL}	105	—	—	ns	
External Clock output high-level pulse width	t_{CH}	105	—	—	ns	
External Clock output rise time	t_{CR}	—	—	15	ns	
External Clock output fall time	t_{CF}	—	—	15	ns	

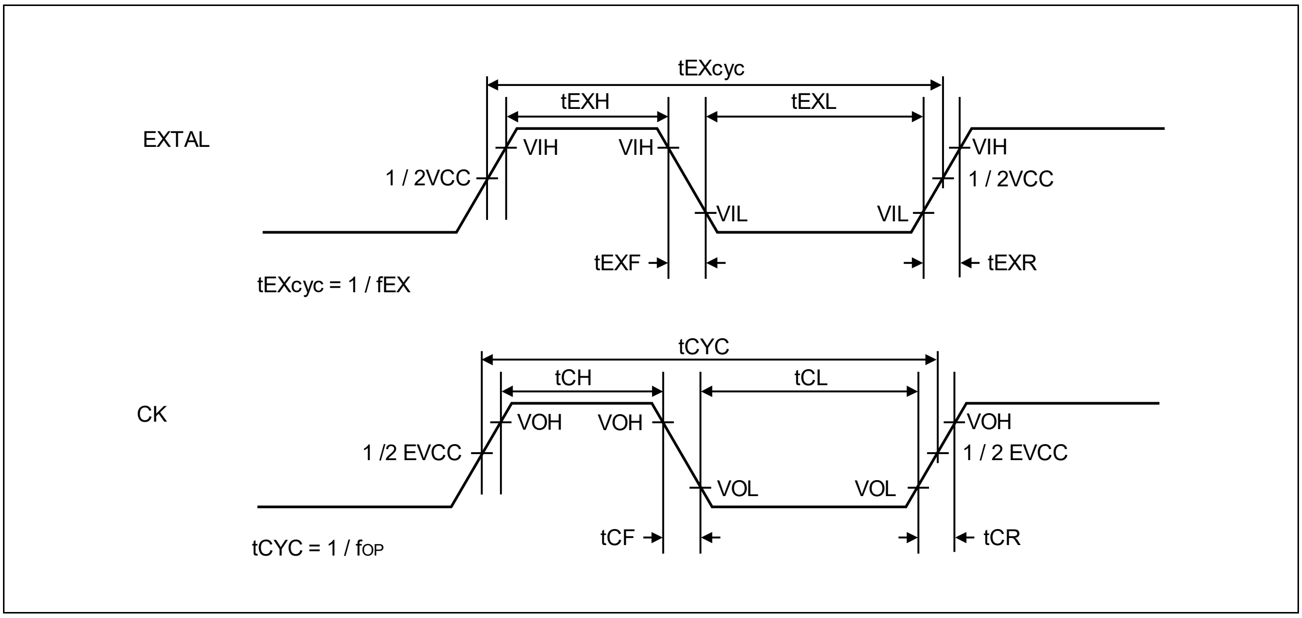


Figure 1.15 EXTAL and External Clock Output Timing

1.3.3.5 PLL Characteristics

Table 1.24 PLL Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
PLL output long term jitter	Tltj	Term=1us	−500	—	500	ps
		Term=10us	−1	—	1	ns
		Term=20us	−2	—	2	ns

Table 1.25 RHSIF PLL Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
PLL lock time	$t_{RHPLLLCT}$		—	—	50	µs

1.3.4 Output Slew Rate

IOVCC means the pin assigned to the power supply (EnVCC, VCC and SYSVCC)

Table 1.26 Drive Strength 1

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output rise time / fall time slew rate	t_R, t_F	CL = 30pF, 20% to 80% IOVCC = 3.0V to 3.6 V	—	12.0	27.0	ns
		CL = 50pF, 20% to 80% IOVCC = 3.0V to 3.6 V	—	20.0	45.0	ns
		CL = 100pF, 20% to 80% IOVCC = 3.0V to 3.6 V	—	40.0	90.0	ns
		CL = 30pF, 20% to 80% IOVCC = 4.5V to 5.5 V	—	9.0	20.3	ns
		CL = 50pF, 20% to 80% IOVCC = 4.5V to 5.5 V	—	15.0	33.8	ns
		CL = 100pF, 20% to 80% IOVCC = 4.5V to 5.5 V	—	30.0	67.5	ns

Table 1.27 Drive Strength 2

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output rise time / fall time slew rate	t_R, t_F	CL = 30pF, 20% to 80% IOVCC = 3.0V to 3.6 V	—	6.0	13.5	ns
		CL = 50pF, 20% to 80% IOVCC = 3.0V to 3.6 V	—	10.0	22.5	ns
		CL = 100pF, 20% to 80% IOVCC = 3.0V to 3.6 V	—	20.0	45.0	ns
		CL = 30pF, 20% to 80% IOVCC = 4.5V to 5.5 V	—	4.6	10.3	ns
		CL = 50pF, 20% to 80% IOVCC = 4.5V to 5.5 V	—	7.5	16.9	ns
		CL = 100pF, 20% to 80% IOVCC = 4.5V to 5.5 V	—	14.8	33.3	ns

Table 1.28 Drive Strength 3

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output rise time / fall time slew rate	t_R, t_F	CL = 30pF, 20% to 80% IOVCC = 3.0V to 3.6 V	—	2.7	7.1	ns
		CL = 50pF, 20% to 80% IOVCC = 3.0V to 3.6 V	—	4.4	11.4	ns
		CL = 100pF, 20% to 80% IOVCC = 3.0V to 3.6 V	—	8.5	22.2	ns
		CL = 30pF, 20% to 80% IOVCC = 4.5V to 5.5 V	—	2.0	5.3	ns
		CL = 50pF, 20% to 80% IOVCC = 4.5V to 5.5 V	—	3.3	8.5	ns
		CL = 100pF, 20% to 80% IOVCC = 4.5V to 5.5 V	—	6.4	16.6	ns

Table 1.29 Drive Strength 4 and ERROROUT_M pin

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output rise time / fall time slew rate	t_R, t_F	CL = 30pF, 20% to 80% IOVCC = 3.0V to 3.6 V	—	1.9	4.9	ns
		CL = 50pF, 20% to 80% IOVCC = 3.0V to 3.6 V	—	3.0	7.8	ns
		CL = 100pF, 20% to 80% IOVCC = 3.0V to 3.6 V	—	5.7	14.8	ns
		CL = 30pF, 20% to 80% IOVCC = 4.5V to 5.5 V	—	1.5	4.4	ns
		CL = 50pF, 20% to 80% IOVCC = 4.5V to 5.5 V	—	2.4	7.0	ns
		CL = 100pF, 20% to 80% IOVCC = 4.5V to 5.5 V	—	4.7	13.5	ns

1.3.5 Control Signal Timing

Table 1.30 Control Signals

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Reference
Reset pulse width	t_{RESW}	[*1]	500	—	—	μs	**Figure 1.16**
Reset noise cancel width	t_{RESNCW}		0.2	0.4	1.2	μs	
Noise cancel width (MD1, MD0, $\overline{\text{TRST}}$, NMI)	t_{NCW}		0.2	0.4	1.2	μs	
IRQ pulse width[*2]	t_{IRQ}		50	—	—	ns	
$\overline{\text{RES\_OUT}}$ width at the time of System Reset 1 (External Reset or Standby Reset)	t_{ROE}	w/o BIST and RAM initialization	580[*3]	—	1200[*3,*4]	μs	
		w/ BIST	—	—	22.2[*4]	ms	**Table 1.31**
		w/ RAM initialization	—	—	1.7[*4]	ms	**Table 1.32**
		w/ BIST and RAM initialization	—	—	22.7[*4]	ms	**Table 1.31** **Table 1.32**
$\overline{\text{RES\_OUT}}$ width at the time of System Reset 1 (VMON Reset)	t_{ROV}	w/o BIST and RAM initialization	130[*3]	—	700[*3,*5]	μs	
		w/ BIST	—	—	21.7[*5]	ms	**Table 1.31**
		w/ RAM initialization	—	—	1.2[*5]	ms	**Table 1.32**
		w/ BIST and RAM initialization	—	—	22.2[*5]	ms	**Table 1.31** **Table 1.32**
$\overline{\text{RES\_OUT}}$ width at the time of System Reset 2	t_{ROS2}	w/o BIST and RAM initialization	130[*3]	—	200[*3]	μs	
		w/ BIST	—	—	21.2	ms	**Table 1.31**
		w/ RAM initialization	—	—	0.7	ms	**Table 1.32**
		w/ BIST and RAM initialization	—	—	21.7	ms	**Table 1.31** **Table 1.32**
$\overline{\text{RES\_OUT}}$ width at the time of Application Reset	t_{ROA}	w/o RAM initialization	100	—	130	μs	
		w/ RAM initialization	—	—	0.7	ms	**Table 1.32**

Note 1. t_{RESW} is the minimum time to complete the external reset state. If a reset is input that is shorter than this time, the external reset state will continue even after reset negation. This microcontroller is completely reset after completion of the external reset state. Reset is accepted with reset input more than the maximum of tRESNCW. If the reset pulse width is less than the minimum value of the reset noise cancel width, the reset cannot be accepted.

Note 2. It is a value when noise removal by the DNF is disabled.

Note 3. It is a value when the BIST and RAM initialization are not executed. For details of the BIST execution, see *Section 38.6.4, Operation*. Also, for details of the RAM initialization, see *Section 10.3.6, RAM Initialization*.

Note 4. The reset pulse low width is the minimum t_{RESW} value.

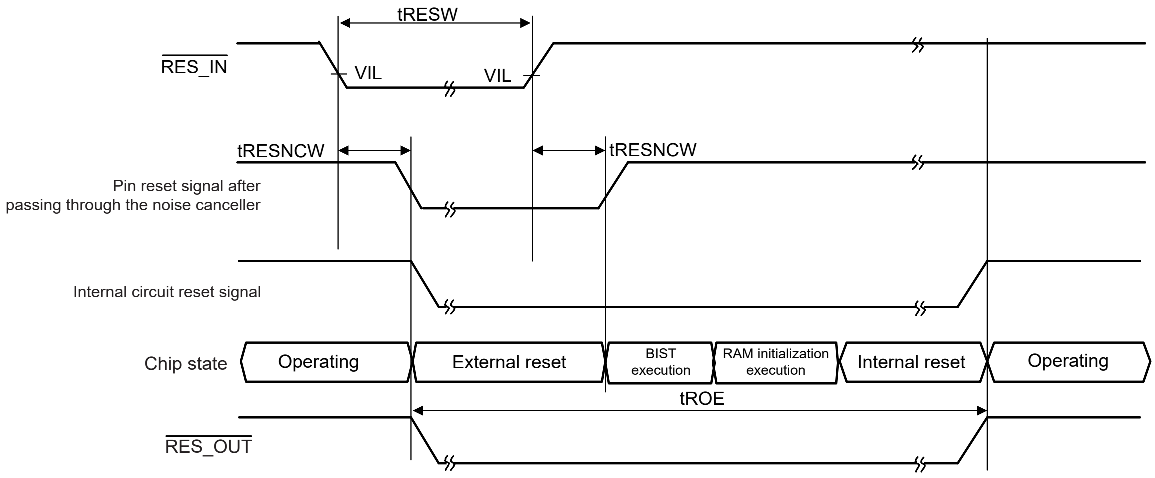
Note 5. It will depend on the power supply detection width.

Table 1.31 BIST Execution Time

BIST	Min.	Typ.	Max.	Unit
BIST scenario 1	—	—	5.25	ms
BIST scenario 2	—	—	10.50	ms
BIST scenario 3	—	—	15.75	ms
BIST scenario 4	—	—	21.00	ms

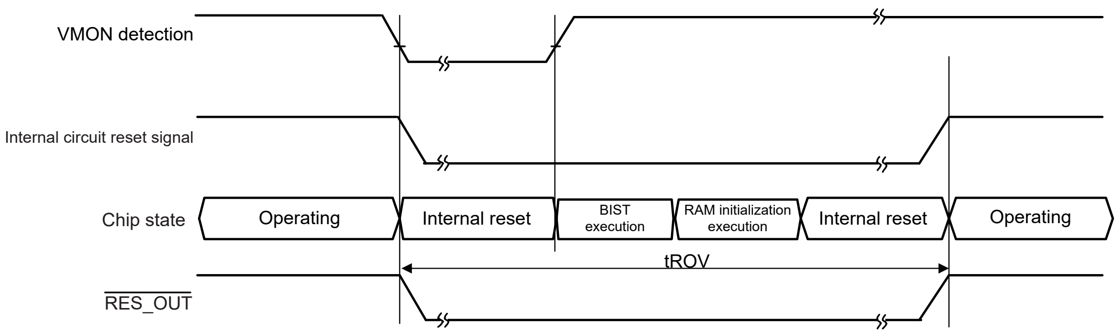
Table 1.32 RAM Initialization Execution Time

Exection Time	Min.	Typ.	Max.	Unit
RAM Initialization Exection Time	—	—	475	µs



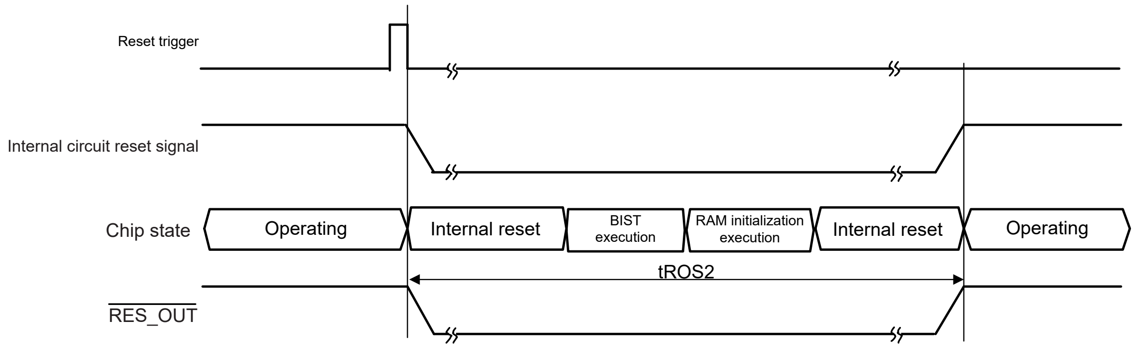
Note: For BIST execution time, See *Section 38.6, BIST*.

Figure 1.16 System Reset 1 Timing (External Reset)



Note: For BIST execution time, See *Section 38.6, BIST*.

Figure 1.17 System Reset 1 Timing (VMON Reset)



Note: For BIST execution time, See *Section 38.6, BIST*.

Figure 1.18 System Reset 2 Timing

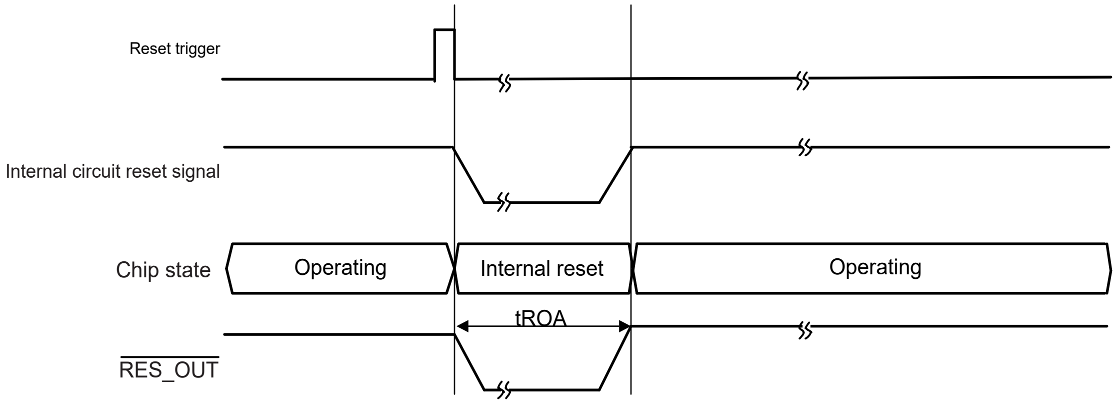


Figure 1.19 Application Reset Timing

1.3.6 CSIH Timing

Table 1.33 CSIH Timing in 5V Master Mode

Conditions: CL = 50 pF, Drive strength = 4, Buffer type Sch1, E0VCC = E1VCC = E2VCC = 5.0 ± 0.5 V

Item	Symbol	Condition	Min.	Max.	Unit	Reference
CSIHnTSCK cycle	t_{KCYM}		100	—	ns	**Figure 1.20**
CSIHnTSCK high-level width	t_{KWHM}		$(t_{KCYM} / 2) - 12$	—	ns	
CSIHnTSCK low-level width	t_{KWLM}		$(t_{KCYM} / 2) - 12$	—	ns	
CSIHnTSI setup time (for CSIHnTSCK)	t_{SSIM}		20	—	ns	
CSIHnTSI hold time (for CSIHnTSCK)	t_{HSIM}		10	—	ns	
CSIHnTSO output delay time (for CSIHnTSCK)	t_{DSOM}		—	16	ns	
CSIHnTSO output hold time (for CSIHnTSCK)	t_{HSOM}		$t_{KWHM} / 2$	—	ns	
CSIHnTRY setup time (for CSIHnTSCK)	t_{SRYI}	HSE = 1	$(2 \times t_{PAck}) + 30$	—	ns	**Figure 1.21**
CSIHnTRY high level width (for CSIHnTSCK)	t_{WRYI}		$(2 \times t_{PAck}) + 5$	—	ns	
CSIHnTCSSx inactive level width	t_{WSCSB}	*1	(CSidle + 0.5) × t_{KCYM} − 20	—	ns	**Figure 1.22**
		Other than above	CSidle × t_{KCYM} – 20	—	ns	
CSIHnTCSSx setup time (for CSIHnTSCK)	t_{SSCSB0}	DAP = 0	CSsetup × t_{KCYM} − 16	—	ns	
	t_{SSCSB1}	DAP = 1	(CSsetup + 0.5) × t_{KCYM} − 16	—	ns	
CSIHnTCSSx hold time (for CSIHnTSCK)	t_{HSCSB0}	SIT = 0	CShold x t_{KCYM} − 10	—	ns	**Figure 1.23**
	t_{HSCSB1}	SIT = 1	(CShold + 0.5) × t_{KCYM} − 10	—	ns	

Note: t_{PAck} is the operating clock cycle of CSIH (CLK_HSB).
n = 0 to 5, x = 0 to 5 (n = 0), x = 0 to 3 (n = 1, 2, 3, 4, 5)
- CSsetup: CSIHnCFGx.CSIHnSPx3-0 set value
- CShold: CSIHnCFGx.CSIHnHDx3-0 set value
- CSidle: CSIHnCFGx.CSIHnIDx2-0 set value
- DAP: CSIHnCFGx.CSIHnDAPx bit
- SIT: CSIHnCTL1.CSIHnSIT bit

Note 1. When the serial clock level is changed during communication and when the idle time is set to 0.5 transmission clock periods.

NOTE

This AC characteristics is limited to specific pin groups. For details, please refer to Appendix file "*Limited_conditions_for_AC_specification.xlsx*".

Table 1.34 CSIH Timing in 3.3V Master Mode

Conditions: CL = 50 pF, Drive strength = 4, Buffer type Sch1, E1VCC = E2VCC = 3.3 ± 0.3 V

Item	Symbol	Condition	Min.	Max.	Unit	Reference
CSIHnTSCK cycle	t_{KCYM}		125	—	ns	**Figure 1.20**
CSIHnTSCK high-level width	t_{KWHM}		$(t_{KCYM} / 2) - 12$	—	ns	
CSIHnTSCK low-level width	t_{KWLM}		$(t_{KCYM} / 2) - 12$	—	ns	
CSIHnTSI setup time (for CSIHnTSCK)	t_{SSIM}		25	—	ns	
CSIHnTSI hold time (for CSIHnTSCK)	t_{HSIM}		15	—	ns	
CSIHnTSO output delay time (for CSIHnTSCK)	t_{DSOM}		—	17	ns	
CSIHnTSO output hold time (for CSIHnTSCK)	t_{HSOM}		$t_{KWHM} / 2$	—	ns	
CSIHnTRY setup time (for CSIHnTSCK)	t_{SRYI}	HSE = 1	$(2 \times t_{PAck}) + 30$	—	ns	**Figure 1.21**
CSIHnTRY high level width (for CSIHnTSCK)	t_{WRYI}		$(2 \times t_{PAck}) + 5$	—	ns	
CSIHnTCSSx inactive level width	t_{WSCSB}	*1	$(CSidle + 0.5) \times t_{KCYM} - 20$	—	ns	**Figure 1.22**
		Other than above	$CSidle \times t_{KCYM} - 20$	—	ns	
CSIHnTCSSx setup time (for CSIHnTSCK)	t_{SSCSB0}	DAP = 0	$CSsetup \times t_{KCYM} - 17$	—	ns	
	t_{SSCSB1}	DAP = 1	$(CSsetup + 0.5) \times t_{KCYM} - 17$	—	ns	
CSIHnTCSSx hold time (for CSIHnTSCK)	t_{HSCSB0}	SIT = 0	$CShold \times t_{KCYM} - 10$	—	ns	**Figure 1.23**
	t_{HSCSB1}	SIT = 1	$(CShold + 0.5) \times t_{KCYM} - 10$	—	ns	

Note: t_{PAck} is the operating clock cycle of CSIH (CLK_HSB).
n = 0 to 5, x = 0 to 5 (n = 0), x = 0 to 3 (n = 1, 2, 3, 4, 5)

- CSsetup: CSIHnCFGx.CSIHnSPx3-0 set value
- CShold: CSIHnCFGx.CSIHnHDx3-0 set value
- CSidle: CSIHnCFGx.CSIHnIDx set value
- DAP: CSIHnCFGx.CSIHnDAPx bit
- SIT: CSIHnCTL1.CSIHnSIT bit

Note 1. When the serial clock level is changed during communication and when the idle time is set to 0.5 transmission clock periods.

NOTE

This AC characteristics is limited to specific pin groups. For details, please refer to Appendix file “*Limited_conditions_for_AC_specification.xlsx*”.

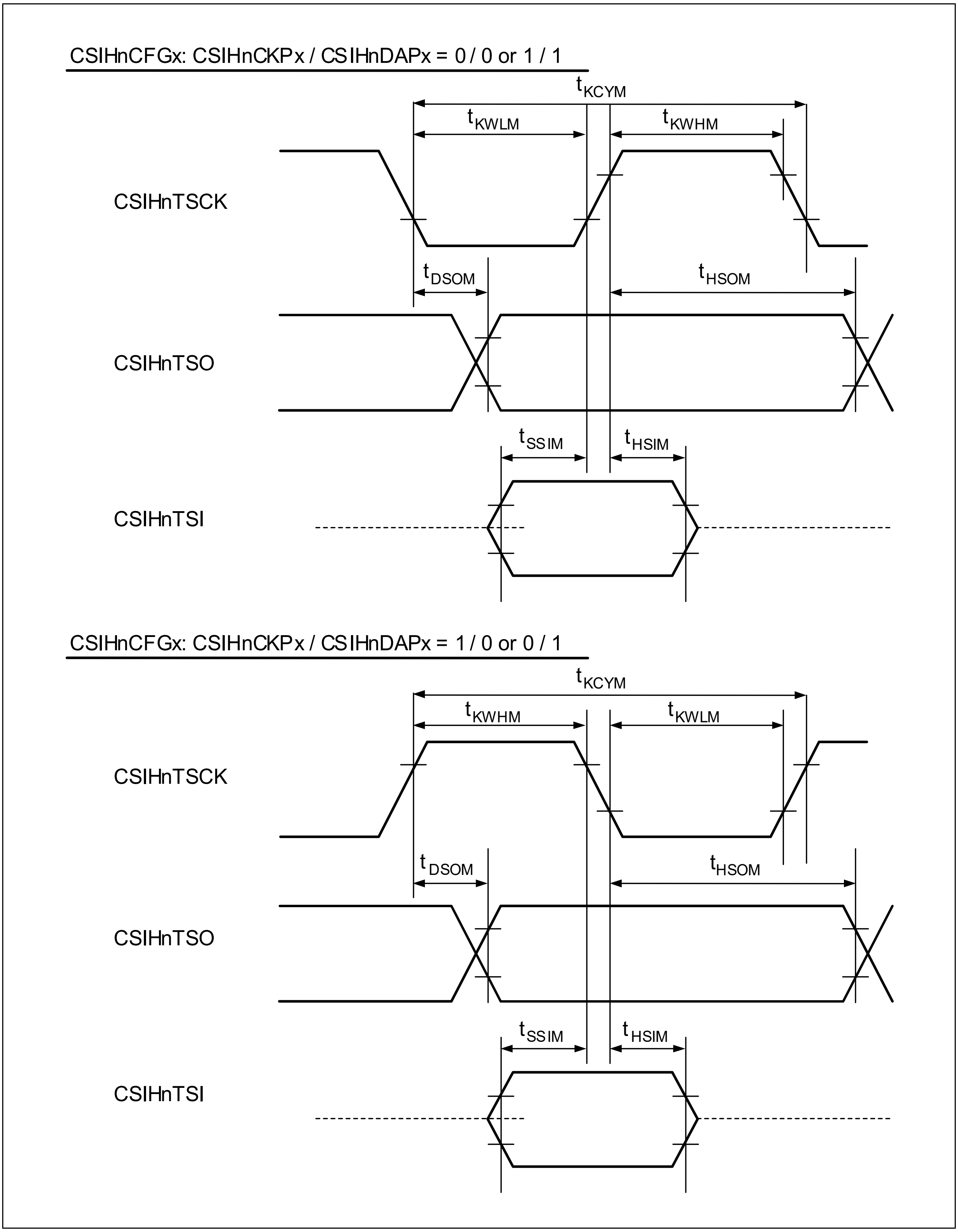


Figure 1.20 CSIH Timing (Master Mode)

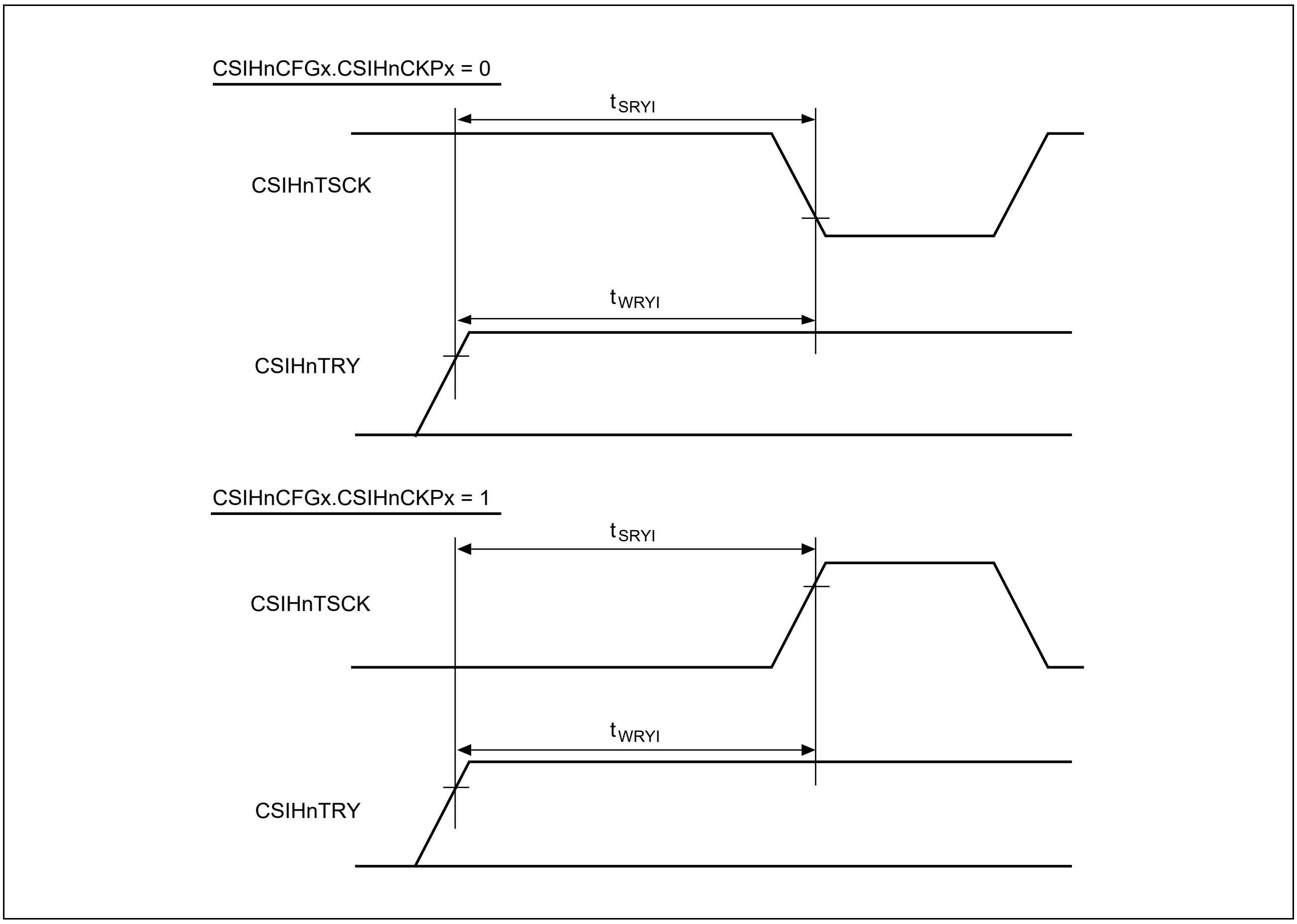


Figure 1.21 CSIH Timing (Master Mode)

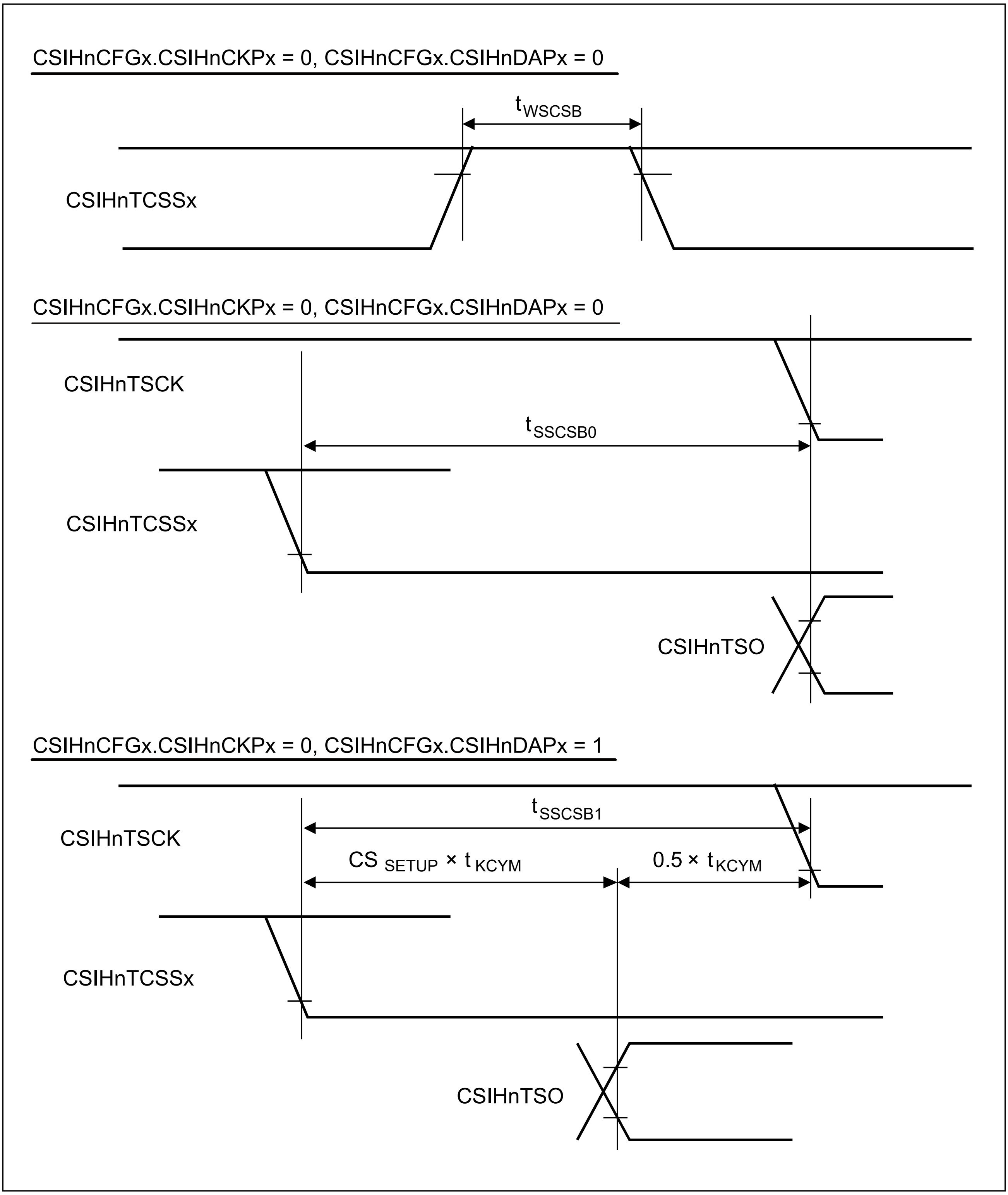


Figure 1.22 CSIH Timing (Master Mode)

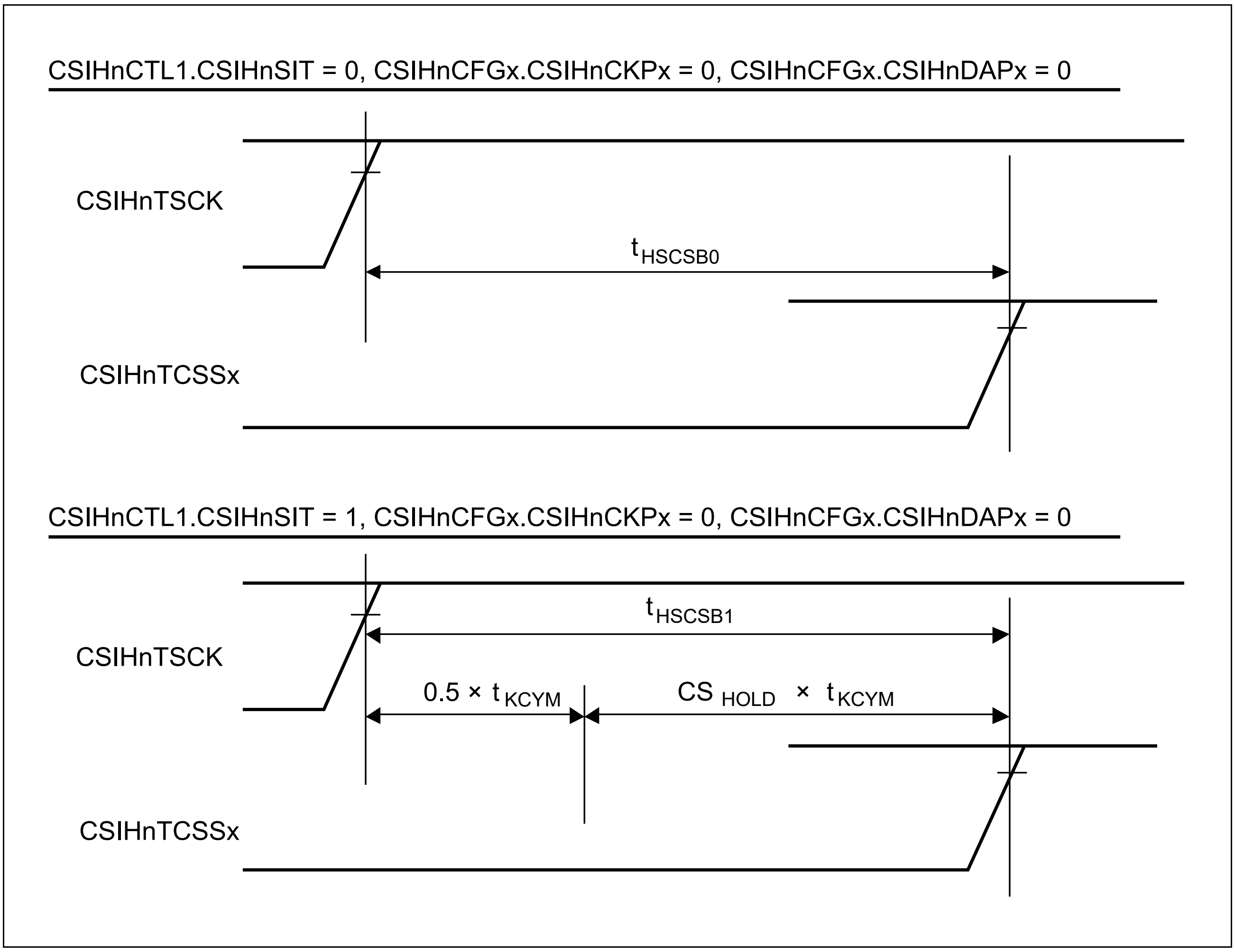


Figure 1.23 CSIH Timing (Master Mode)

Table 1.35 CSIH Timing in 5V Slave Mode

Conditions: CL = 50 pF, Drive strength = 4, Buffer type Sch1, E0VCC = E1VCC = E2VCC = 5.0 ± 0.5 V

Item	Symbol	Condition	Min.	Max.	Unit	Reference
CSIHnTSCK cycle	t_{KCYS}	—	250	—	ns	**Figure 1.24**
CSIHnTSCK high-level width	t_{KWHS}	—	$(t_{KCYS} / 2) - 30$	—	ns	
CSIHnTSCK low-level width	t_{KWLS}	—	$(t_{KCYS} / 2) - 30$	—	ns	
CSIHnTSI setup time (for CSIHnTSCK)	t_{SSIS}	—	15	—	ns	
CSIHnTSI hold time (for CSIHnTSCK)	t_{HSIS}	—	$t_{PAck} + 15$	—	ns	
CSIHnTSO output delay time (for CSIHnTSCK)	t_{DSOS}	—	—	33	ns	
CSIHnTSO output hold time (for CSIHnTSCK)	t_{HSOS}	—	t_{KWHS}	—	ns	
CSIHnTRY output delay time	t_{SRYO}	—	—	30	ns	**Figure 1.25**
CSIHnTSO slave output release time	t_{REL}	—	—	$8 \times t_{PAck}$	ns	
CSIHnTSSI setup time (for CSIHnTSCK)	t_{SSSIS}	—	$0.5 \times t_{KCYS}$	—	ns	**Figure 1.26**
CSIHnTSSI hold time (for CSIHnTSCK)	t_{HSSIS}	—	$t_{PAck} + 30$	—	ns	

Note: t_{PAck} is the operating clock cycle of CSIH (CLK_HSB).

NOTE

This AC characteristics is limited to specific pin groups. For details, please refer to Appendix file "*Limited_conditions_for_AC_specification.xlsx*".

Table 1.36 CSIH Timing in 3.3V Slave Mode

Conditions: CL = 50 pF, Drive strength = 4, Buffer type Sch1, E1VCC = E2VCC = 3.3 ± 0.3 V

Item	Symbol	Condition	Min.	Max.	Unit	Reference
CSIHnTSCK cycle	t_{KCYS}	—	250	—	ns	**Figure 1.24**
CSIHnTSCK high-level width	t_{KWHS}	—	$(t_{KCYS} / 2) - 30$	—	ns	
CSIHnTSCK low-level width	t_{KWLS}	—	$(t_{KCYS} / 2) - 30$	—	ns	
CSIHnTSI setup time (for CSIHnTSCK)	t_{SSIS}	—	15	—	ns	
CSIHnTSI hold time (for CSIHnTSCK)	t_{HSIS}	—	$t_{PAck} + 15$	—	ns	
CSIHnTSO output delay time (for CSIHnTSCK)	t_{DSOS}	—	—	36	ns	
CSIHnTSO output hold time (for CSIHnTSCK)	t_{HSOS}	—	t_{KWHS}	—	ns	
CSIHnTRY output delay time	t_{SRYO}	—	—	30	ns	**Figure 1.25**
CSIHnTSO slave output release time	t_{REL}	—	—	$8 \times t_{PAck}$	ns	
CSIHnTSSI setup time (for CSIHnTSCK)	t_{SSSIS}	—	$0.5 \times t_{KCYS}$	—	ns	**Figure 1.26**
CSIHnTSSI hold time (for CSIHnTSCK)	t_{HSSIS}	—	$t_{PAck} + 30$	—	ns	

Note: t_{PAck} is the operating clock cycle of CSIH (CLK_HSB).

NOTE

This AC characteristics is limited to specific pin groups. For details, please refer to Appendix file "*Limited_conditions_for_AC_specification.xlsx*".

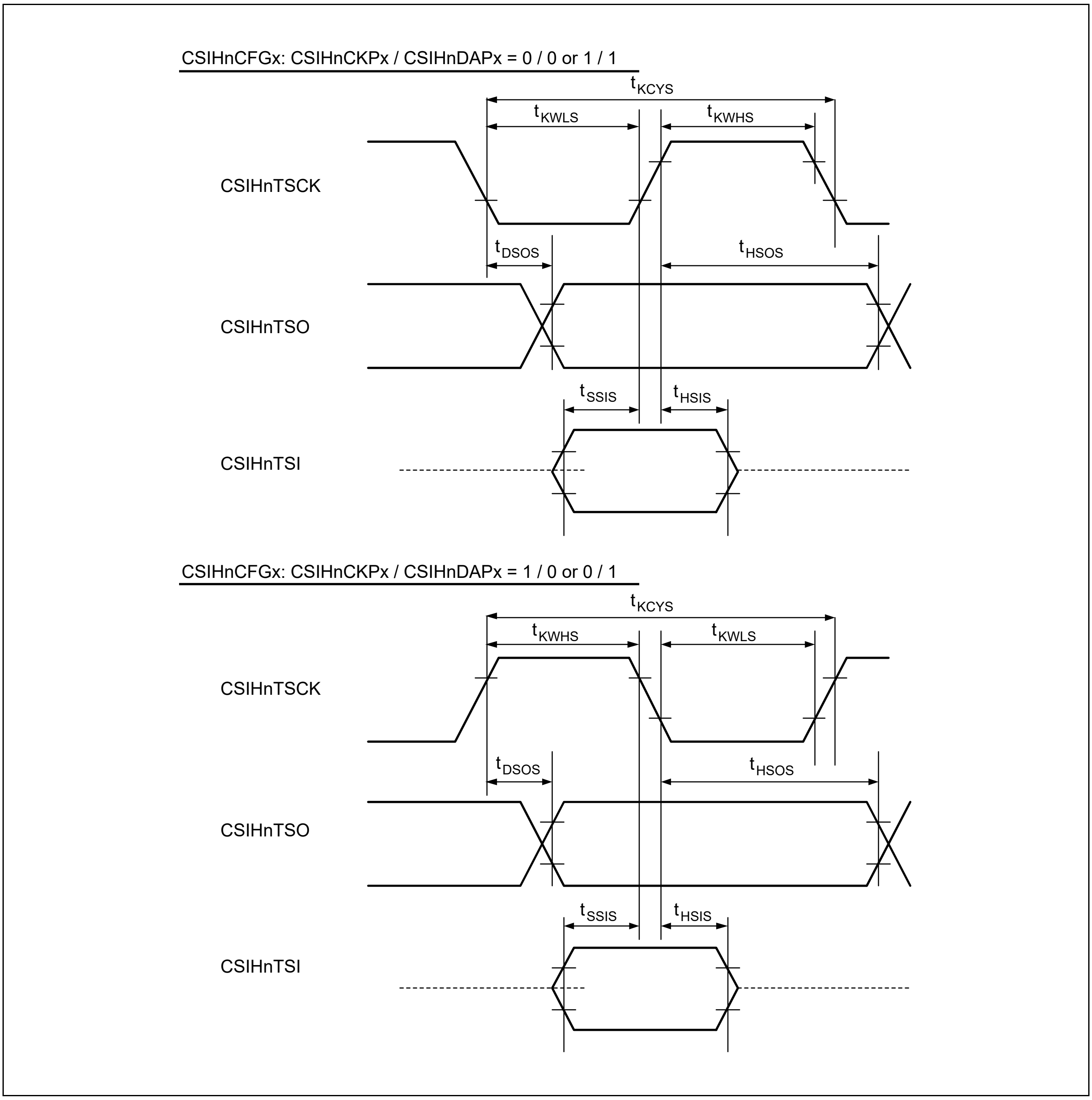


Figure 1.24 CSIH Timing (Slave Mode)

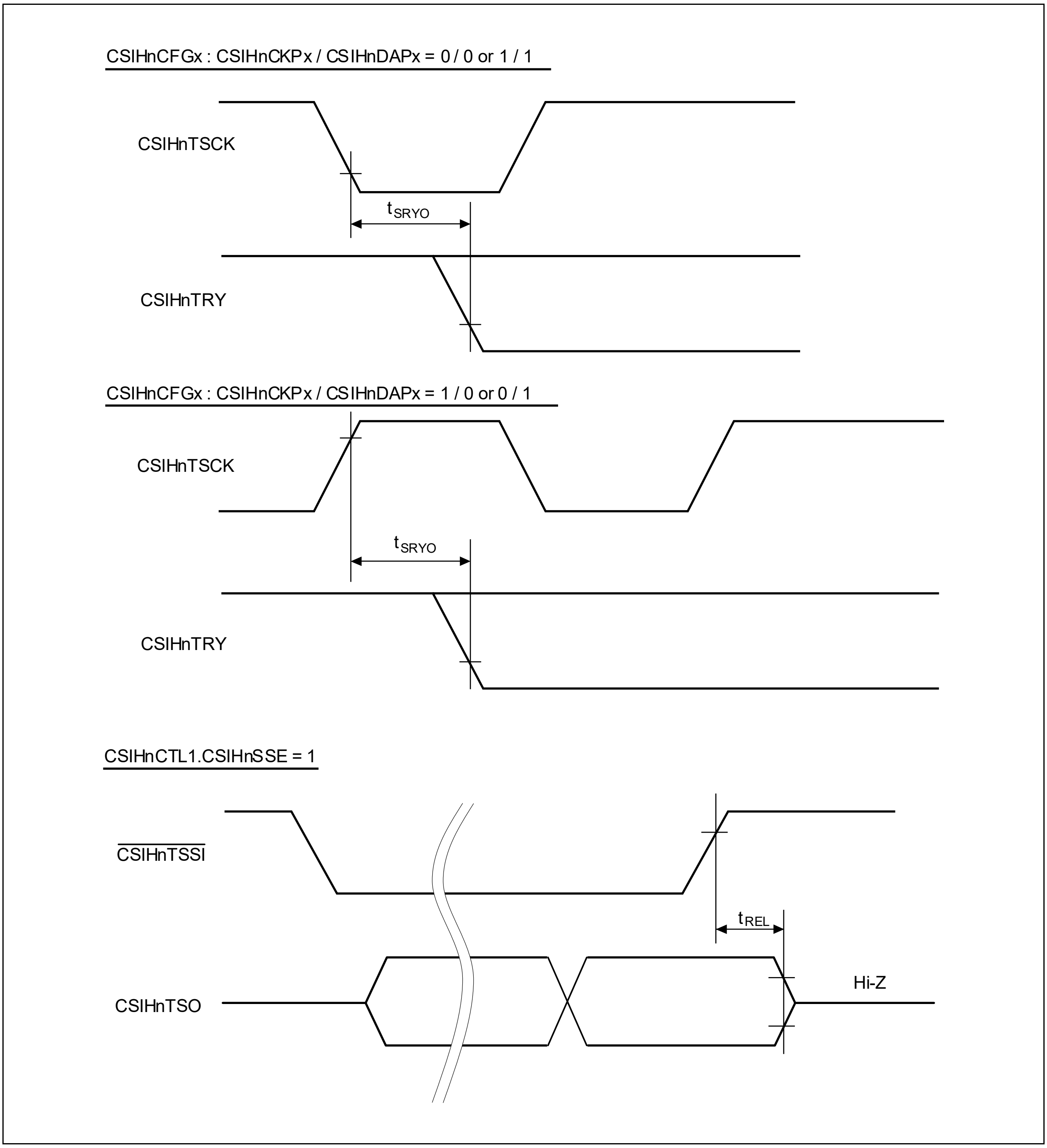


Figure 1.25 CSIH Timing (Slave Mode)

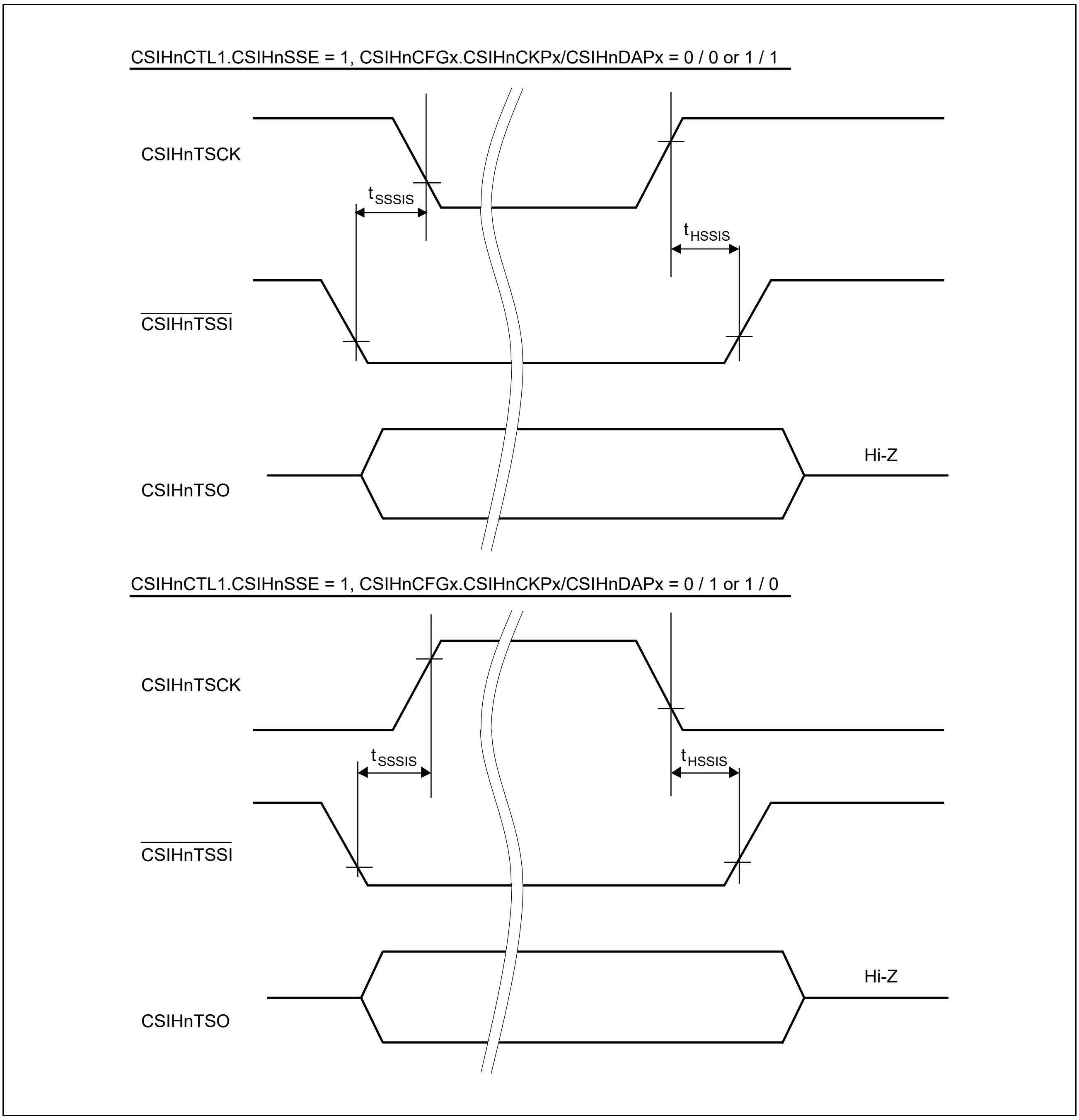


Figure 1.26 CSIH Timing (Slave Mode)

1.3.7 SCI / FLSCI Timing

Table 1.37 SCI3 Timing (Master Mode)

Conditions: CL = 50 pF, Drive strength = 4, Buffer type Sch1, E0VCC = E1VCC = E2VCC = 5.0 ± 0.5 V

Item	Symbol	Condition	Min.	Max.	Unit	Reference
Output clock cycle	t_{Scyc}	Asynchronous	16 × t_{Pck}	—	ns	**Figure 1.27**
		Clock synchronous	8 × t_{Pck}	—	ns	
Output clock pulse width	t_{SCKW}		0.4 × t_{Scyc}	0.6 × t_{Scyc}	ns	
Transmit data delay time	t_{TXD}		−40	40	ns	**Figure 1.28**
Receive data setup time	t_{RXS}	Clock synchronous	2 × t_{Pck}	—	ns	
Receive data hold time	t_{RXH}	Clock synchronous	2 × t_{Pck}	—	ns	

Note: t_{Pck} is the operating clock cycle of SCI (CLK_LSB).

NOTE

This AC characteristics is limited to specific pin groups. For details, please refer to Appendix file "*Limited_conditions_for_AC_specification.xlsx*".

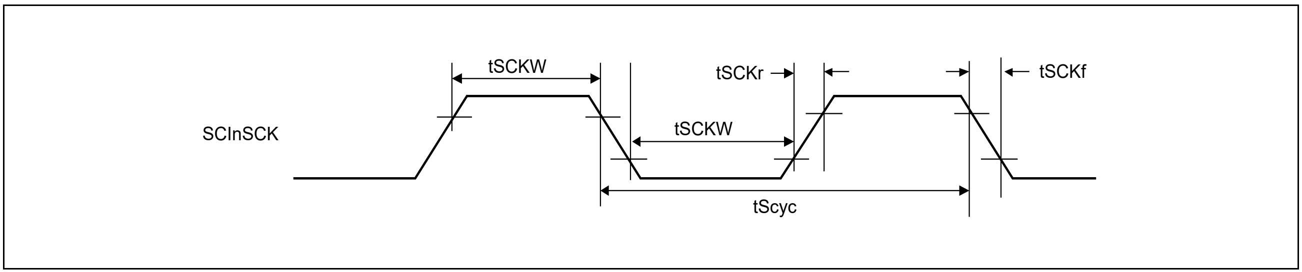


Figure 1.27 SCI Clock Input / Output Timing

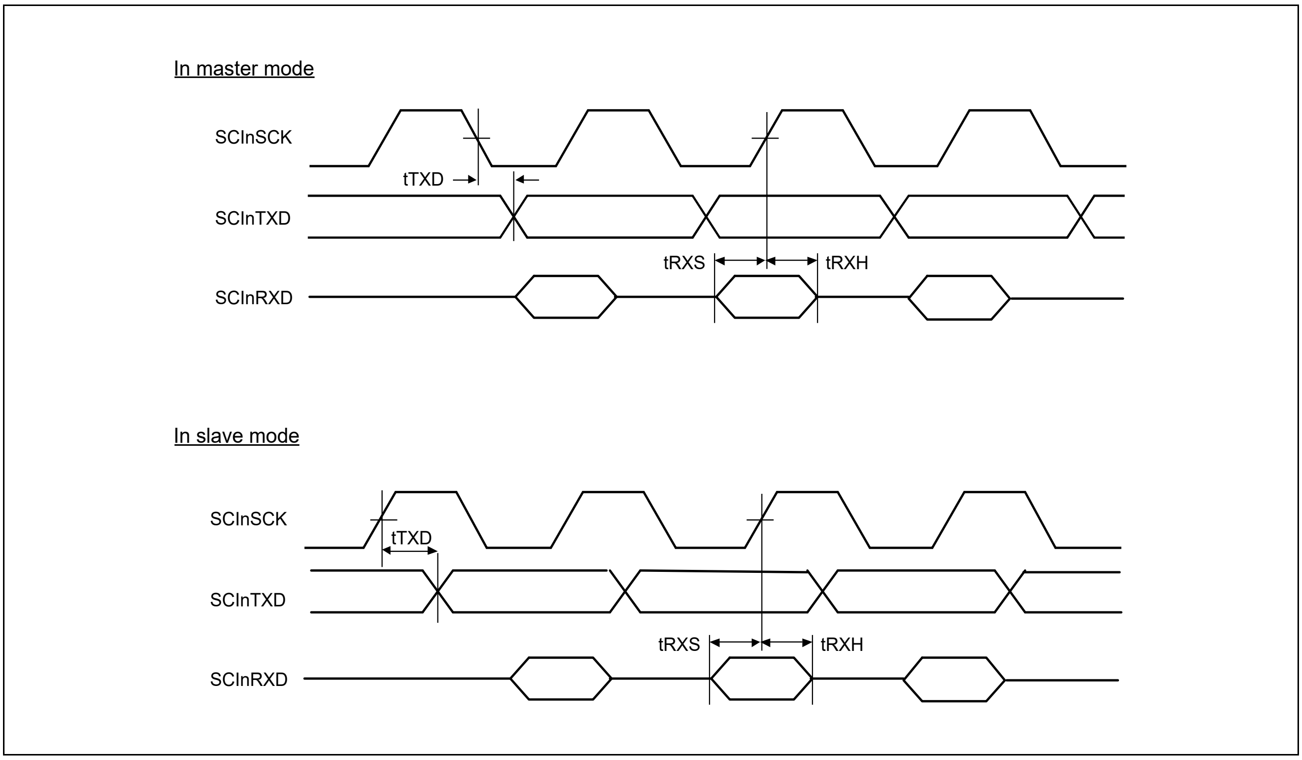


Figure 1.28 SCI Input / Output Timing in Clock Synchronous Mode

Table 1.38 SCI3 Timing (Slave Mode)

Conditions: CL = 50 pF, Drive strength = 4, Buffer type Sch1, E0VCC = E1VCC = E2VCC = 5.0 ± 0.5 V

Item	Symbol	Min.	Max.	Unit	Reference
Input clock cycle	t_{Scyc}	$8 \times t_{Pck}$	—	ns	**Figure 1.27**
Input clock pulse width	t_{SCKW}	$0.4 \times t_{Scyc}$	$0.6 \times t_{Scyc}$	ns	
Input clock rise time	t_{SCKr}	—	20	ns	
Input clock fall time	t_{SCKf}	—	20	ns	
Transmit data delay time	t_{TXD}	$2 \times t_{Pck}$	$50 + 3 \times t_{Pck}$*1	ns	**Figure 1.28**
Receive data setup time	t_{RXS}	$2 \times t_{Pck}$	—	ns	
Receive data hold time	t_{RXH}	$2 \times t_{Pck}$	—	ns	

Note:
- t_{Pck} is the operating clock cycle of SCI3 (CLK_LSB).
- Asynchronous clock input mode is not supported.

Note 1. For data 0 (1st bit) in discontinuous transfer

NOTE

This AC characteristics is limited to specific pin groups. For details, please refer to Appendix file “Limited_conditions_for_AC_specification.xlsx”.

1.3.8 FlexRay Timing

Table 1.39 FlexRay Timing

Conditions: CL = 15 pF, Drive strength = 4, Buffer type Sch1, E0VCC = E1VCC = E2VCC = 5.0 ± 0.5 V

Item	Symbol	Min.	Max.	Unit	Reference
Transfer rate	—	—	10	Mbps	
FRTxD transmit data rise time	t_{CTXr}	—	2.5	ns	**Figure 1.29**
FRTxD transmit data fall time	t_{CTXf}	—	2.5	ns	

NOTE

This AC characteristics is limited to specific pin groups. For details, please refer to Appendix file “*Limited_conditions_for_AC_specification.xlsx*”.

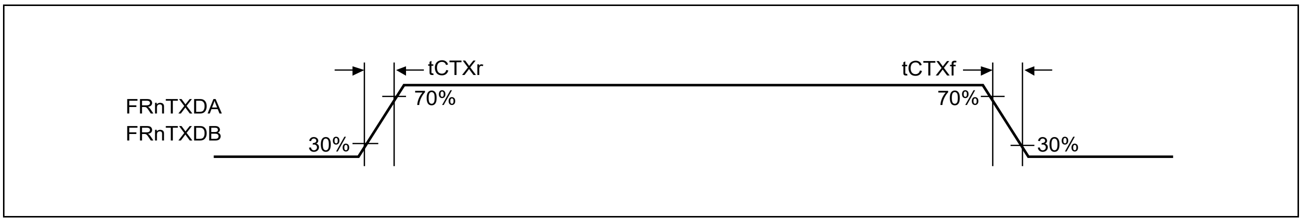


Figure 1.29 FlexRay Timing

1.3.9 RS-CANFD Timing

Table 1.40 RS-CANFD Timing

Conditions: CL = 50 pF, Drive strength = 4, Buffer type Sch1, E0VCC = E1VCC = E2VCC = 5.0 ± 0.5 V

Item	Symbol	Min.	Max.	Unit	Reference
Transmit rate	—	—	8	Mbps	**Figure 1.30**
Internal delay time	t_{NODE}	—	50	ns	

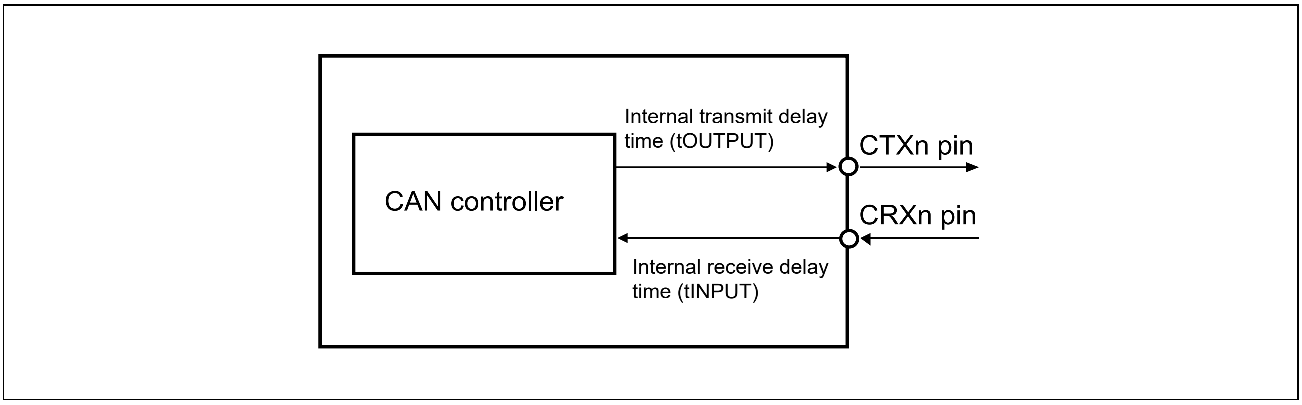


Figure 1.30 Definition of RS-CANFD Internal delay time (t_{NODE}) = t_{OUTPUT} + t_{INPUT}

NOTE

This AC characteristics is limited to specific pin groups. For details, please refer to Appendix file "*Limited_conditions_for_AC_specification.xlsx*".

1.3.10 RHSB Timing

Table 1.41 RHSB Timing in 3.3 V LVDS Mode, Up to 40 Mbps

Conditions: E0VCC = 5.0 ± 0.5 V, E2VCC = 3.3 V ± 0.3 V,
E1VCC = 3.3 V ± 0.3 V(When P11_8 or P11_10 is used in HLQFP package.)
Drive strength = 4

Item	Symbol	Condition	Min.	Max.	Unit	Reference
RHSBnFCL clock cycle	t_{FCLcyc}	CL = 25 pF, CL = 50 pF	25	—	ns	**Figure 1.31**
RHSBnFCL high-level period	t_{FCLWH}	CL = 25 pF, CL = 50 pF	0.45 × t_{FCLcyc}	0.55 × t_{FCLcyc}	ns	
RHSBnFCL low-level period	t_{FCLWL}	CL = 25 pF, CL = 50 pF	0.45 × t_{FCLcyc}	0.55 × t_{FCLcyc}	ns	
RHSBnSO / RHSBnCSDx output delay time	t_{SOD}	CL = 25 pF	−5.9	5.9	ns	
		CL = 50 pF	−7.8	7.8	ns	
RHSBnSI rise time	t_{SIr}	10 to 90%	—	0.5 × t_{FCLcyc}	ns	
RHSBnSI fall time	t_{SIf}	10 to 90%	—	0.5 × t_{FCLcyc}	ns	
RHSBnSI 1-bit length	t_{SIW}		8 × t_{FCLcyc}	—	ns	

NOTE

This AC characteristics is limited to specific pin groups. For details, please refer to Appendix file "*Limited_conditions_for_AC_specification.xlsx*".

Table 1.42 RHSB Timing in 5 V LVDS Mode, Up to 80 Mbps

Conditions: E0VCC = 5.0 ± 0.5 V,
E1VCC = 5.0 ± 0.5 V (When P11_8 or P11_10 is used in HLQFP package.)
Drive strength = 4

Item	Symbol	Condition	Min.	Max.	Unit	Reference
RHSBnFCL clock cycle	t_{FCLcyc}	CL = 5 pF, CL = 25 pF, CL = 50 pF	12.5	—	ns	**Figure 1.31**
RHSBnFCL high-level period	t_{FCLWH}	CL = 5 pF, CL = 25 pF, CL = 50 pF	0.45 × t_{FCLcyc}	0.55 × t_{FCLcyc}	ns	
RHSBnFCL low-level period	t_{FCLWL}	CL = 5 pF, CL = 25 pF, CL = 50 pF	0.45 × t_{FCLcyc}	0.55 × t_{FCLcyc}	ns	
RHSBnSO / RHSBnCSDx output delay time	t_{SOD}	CL = 5 pF	−3.6	3.6	ns	
		CL = 25 pF	−4.4	4.4	ns	
		CL = 50 pF	−5.8	5.8	ns	
RHSBnSI rise time	t_{SIr}	10 to 90%	—	0.5 × t_{FCLcyc}	ns	
RHSBnSI fall time	t_{SIf}	10 to 90%	—	0.5 × t_{FCLcyc}	ns	
RHSBnSI 1-bit length	t_{SIW}		8 × t_{FCLcyc}	—	ns	

NOTE

This AC characteristics is limited to specific pin groups. For details, please refer to Appendix file "*Limited_conditions_for_AC_specification.xlsx*".

Table 1.43 RHSB Timing in Single-ended Mode, Up to 20 Mbps

Conditions: (E0VCC = 5.0 ± 0.5 V, E2VCC = 3.3 V ± 0.3 V) or E0VCC = 5.0 ± 0.5 V
Drive strength = 4, CL = 20 pF

Item	Symbol	Condition	Min.	Max.	Unit	Reference
RHSBnFCL clock cycle	t_{FCLcyc}		50	—	ns	**Figure 1.31**
RHSBnFCL high-level period	t_{FCLWH}		0.45 × t_{FCLcyc}	0.55 × t_{FCLcyc}	ns	
RHSBnFCL low-level period	t_{FCLWL}		0.45 × t_{FCLcyc}	0.55 × t_{FCLcyc}	ns	
RHSBnFCL rise time	t_{FCLr}	10 to 90%	—	0.15 × t_{FCLcyc}	ns	
RHSBnFCL fall time	t_{FCLf}	10 to 90%	—	0.15 × t_{FCLcyc}	ns	
RHSBnSO / RHSBnCSDx output delay time	t_{SOD}		−0.25 × t_{FCLcyc}	0.25 × t_{FCLcyc}	ns	
RHSBnSI rise time	t_{SIr}	10 to 90%	—	0.5 × t_{FCLcyc}	ns	
RHSBnSI fall time	t_{SIf}	10 to 90%	—	0.5 × t_{FCLcyc}	ns	
RHSBnSI 1-bit length	t_{SIW}		8 × t_{FCLcyc}	—	ns	

NOTE

This AC characteristics is limited to specific pin groups. For details, please refer to Appendix file "*Limited_conditions_for_AC_specification.xlsx*".

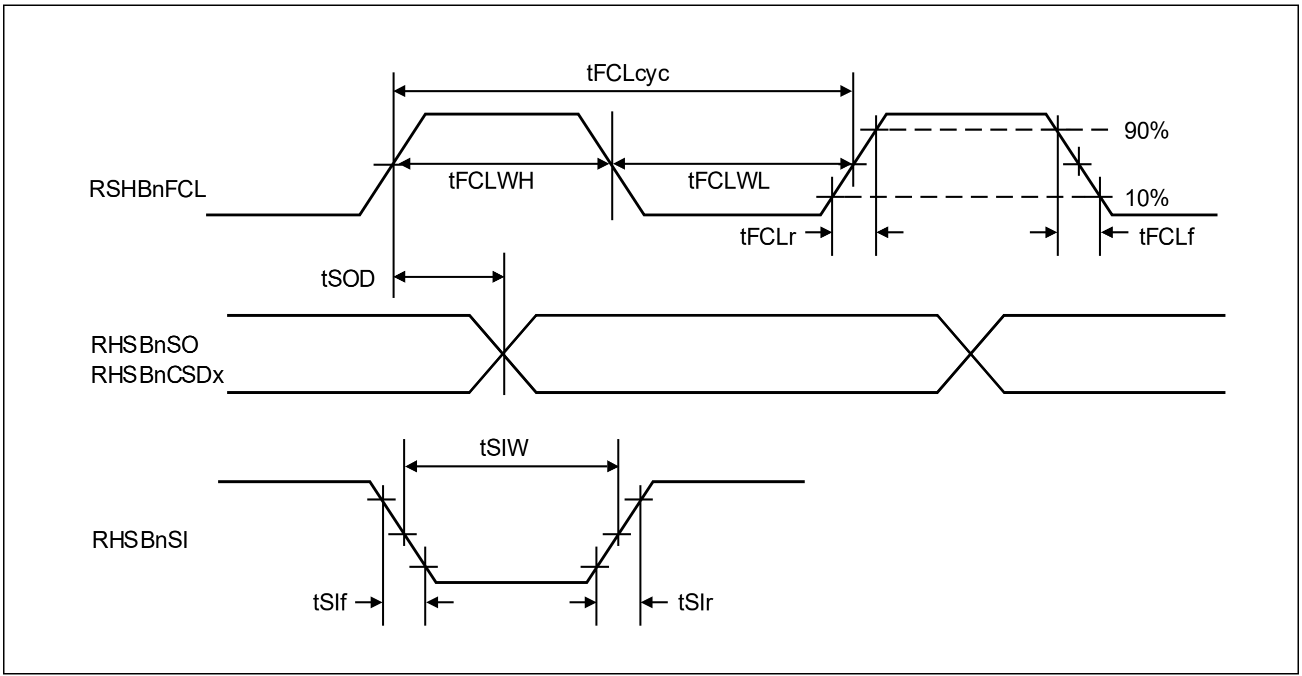


Figure 1.31 RHSB Timing

1.3.11 Ethernet Timing

Table 1.44 Ethernet Timing for MII

Conditions: CL = 15 pF, Drive strength = 4, Buffer type TTL, E1VCC = E2VCC = 3.3 ± 0.3 V

Item	Symbol	Condition	Min.	Max.	Unit	Reference
MII_TX_CLK width	t_{MTC}		40 − 100 ppm	40 + 100 ppm	ns	**Figure 1.32**
MII_TX_CLK high width	t_{MTCH}	*1	14	26	ns	**Figure 1.33**
MII_TX_CLK low width	t_{MTCL}	*1	14	26	ns	
MII_TXD[3:0] delay time	t_{MTXD}		0	25	ns	
MII_TX_EN delay time	t_{MTXE}		0	25	ns	
MII_RX_CLK width	t_{MRC}		40 − 100 ppm	40 + 100 ppm	ns	
MII_RX_CLK high width	t_{MRCH}	*1	14	26	ns	
MII_RX_CLK low width	t_{MRCL}	*1	14	26	ns	
MII_RXD[3:0] setup time	t_{MRXDS}		10	—	ns	
MII_RXD[3:0] hold time	t_{MRXDH}		10	—	ns	
MII_RX_DV, MII_RX_ER setup time	t_{MRDES}		10	—	ns	
MII_RX_DV, MII_RX_ER hold time	t_{MRDEH}		10	—	ns	
WOL delay time	t_{WOL}		1	30	ns	**Figure 1.34**

Note 1. The duty cycle of TXCLK and RXCLK shall be between 35% to 65%. (IEEE802.3)

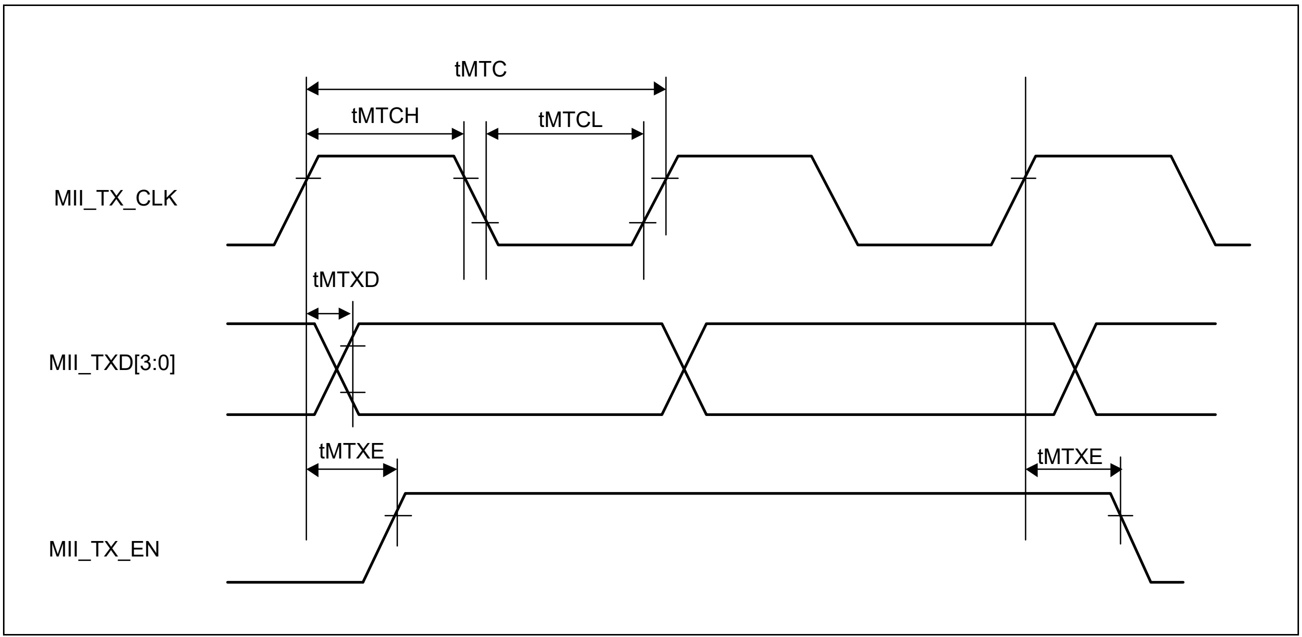


Figure 1.32 Ethernet Timing — MII Transmitter

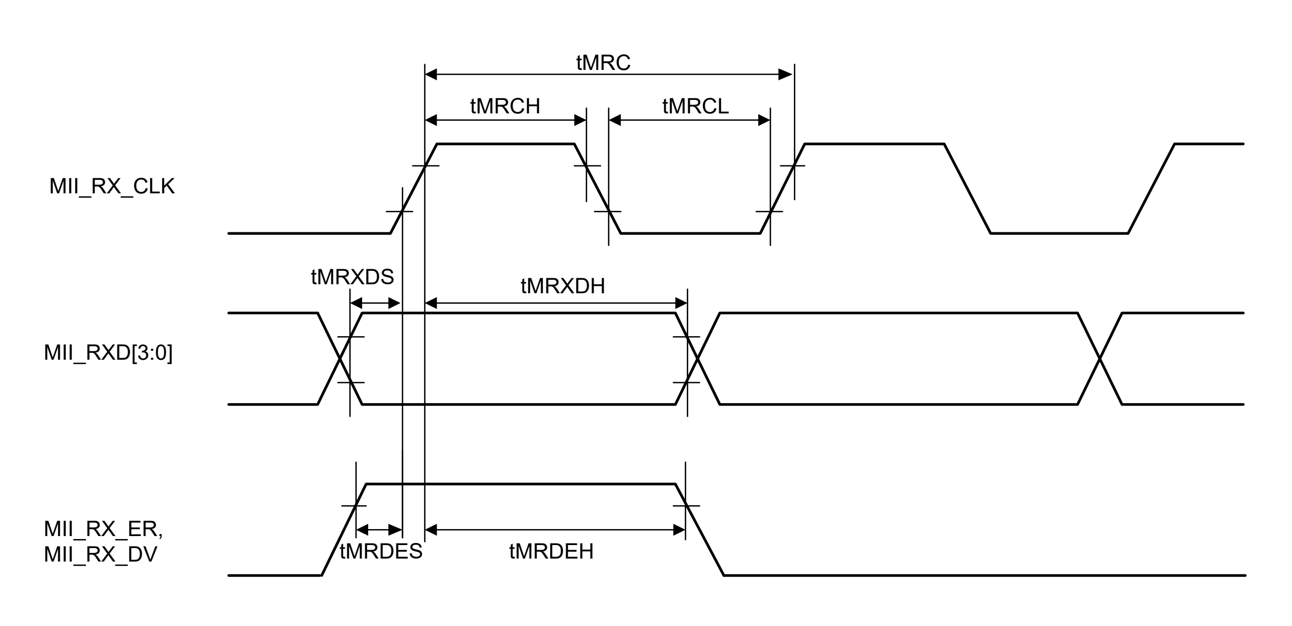


Figure 1.33 Ethernet Timing — MII Receiver

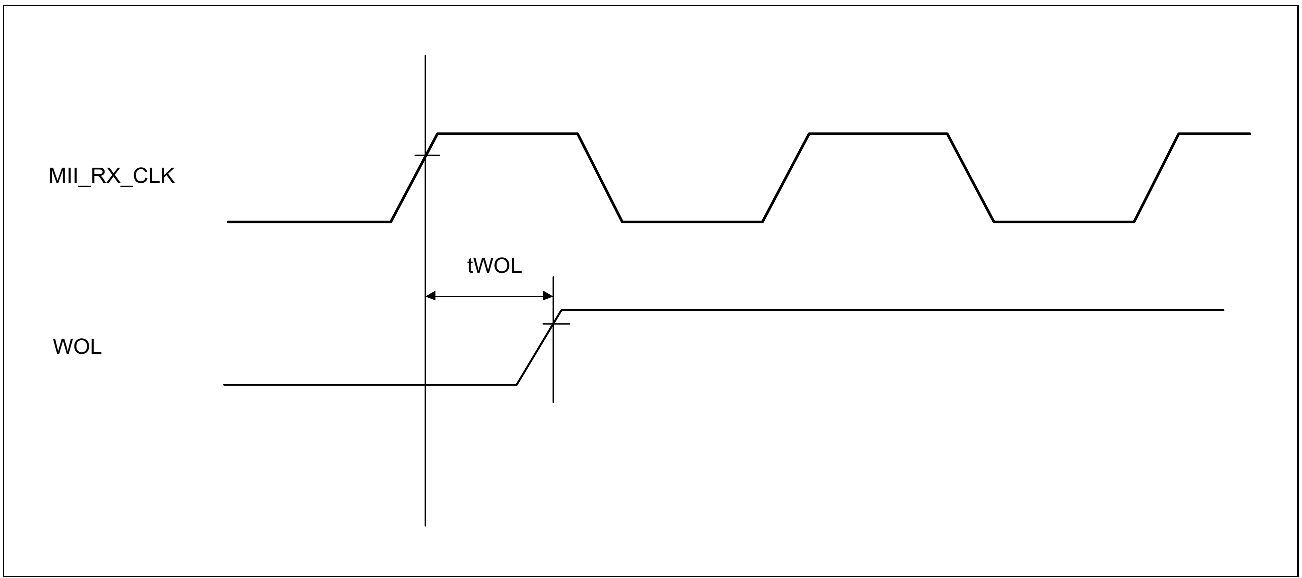


Figure 1.34 WOL Timing — MII

Table 1.45 Ethernet Timing for RMII

Conditions: CL = 15 pF, Drive strength = 4, Buffer type TTL, E1VCC = E2VCC = 3.3 ± 0.3 V

Item	Symbol	Condition	Min.	Max.	Unit	Reference
REF50CK width	t_{RMC}		20 − 50 ppm	20 + 50 ppm	ns	**Figure 1.35**
REF50CK high width	t_{RMCH}	*1	7	13	ns	**Figure 1.36**
REF50CK low width	t_{RMCL}	*1	7	13	ns	
RMII_RXD[1:0], RMII_CRS_DV, and RMII_RX_ER setup time	t_{RMS}		4	—	ns	
RMII_RXD[1:0], RMII_CRS_DV, and RMII_RX_ER hold time	t_{RMH}		6	—	ns	
RMII_TXD[1:0], and RMII_TX_EN delay time	t_{RMD}		2	16	ns	
WOL delay time	t_{WOL}		1	30	ns	**Figure 1.37**

Note 1. The duty cycle of REF50CK shall be between 35% to 65%. (RMII™ specification)

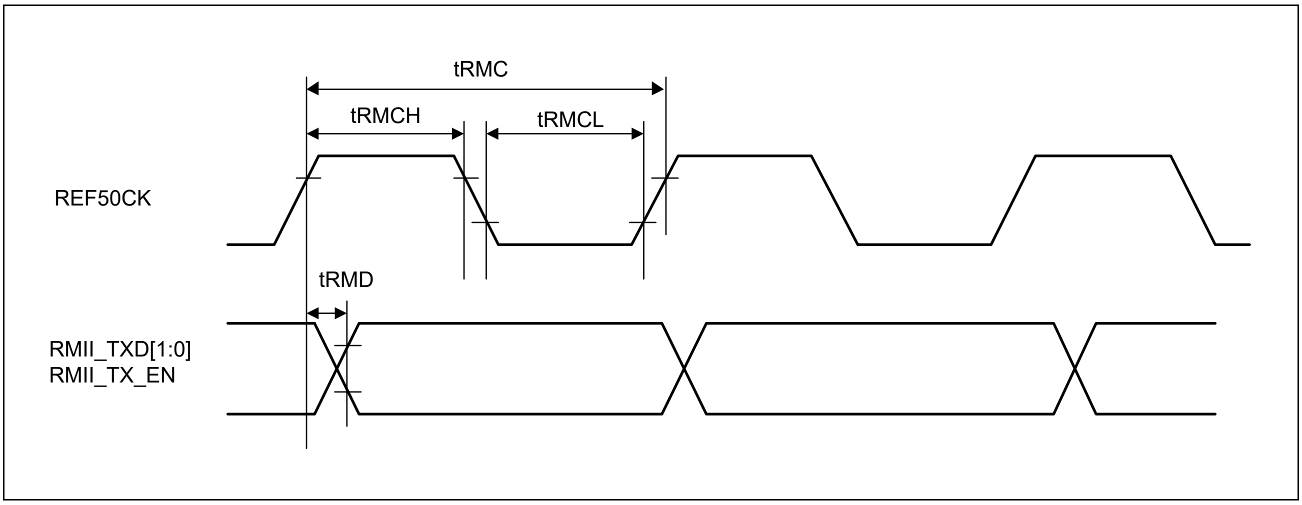


Figure 1.35 Ethernet Timing — RMII Transmitter

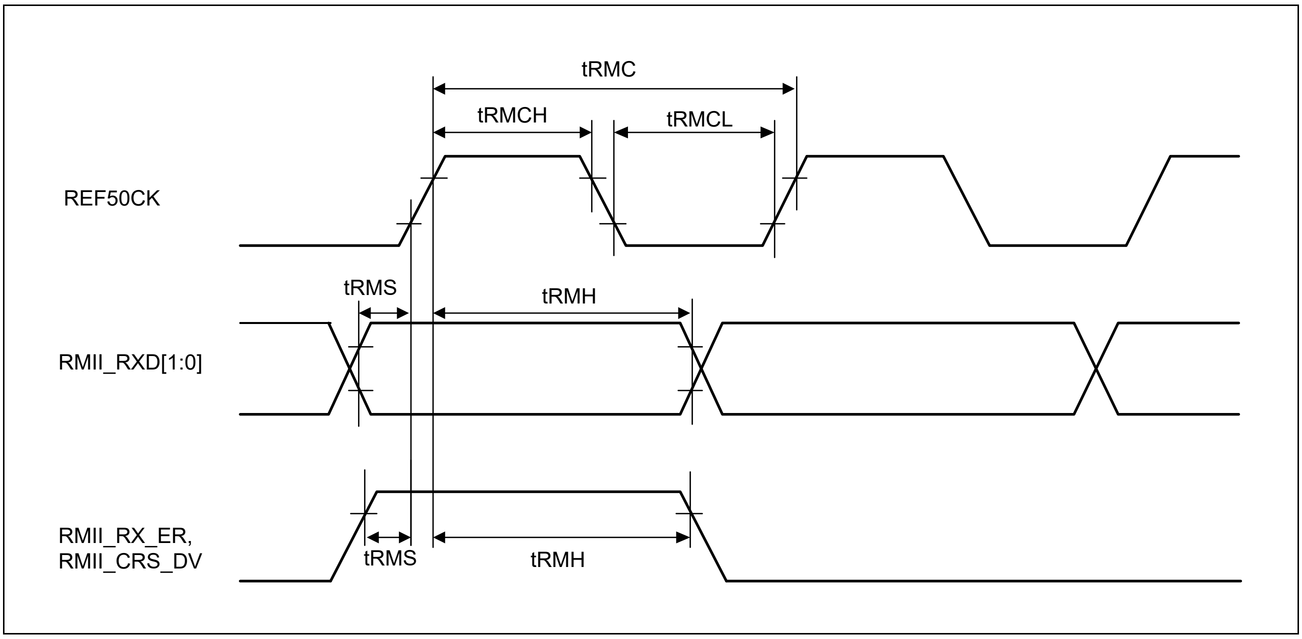


Figure 1.36 Ethernet Timing — RMII Receiver

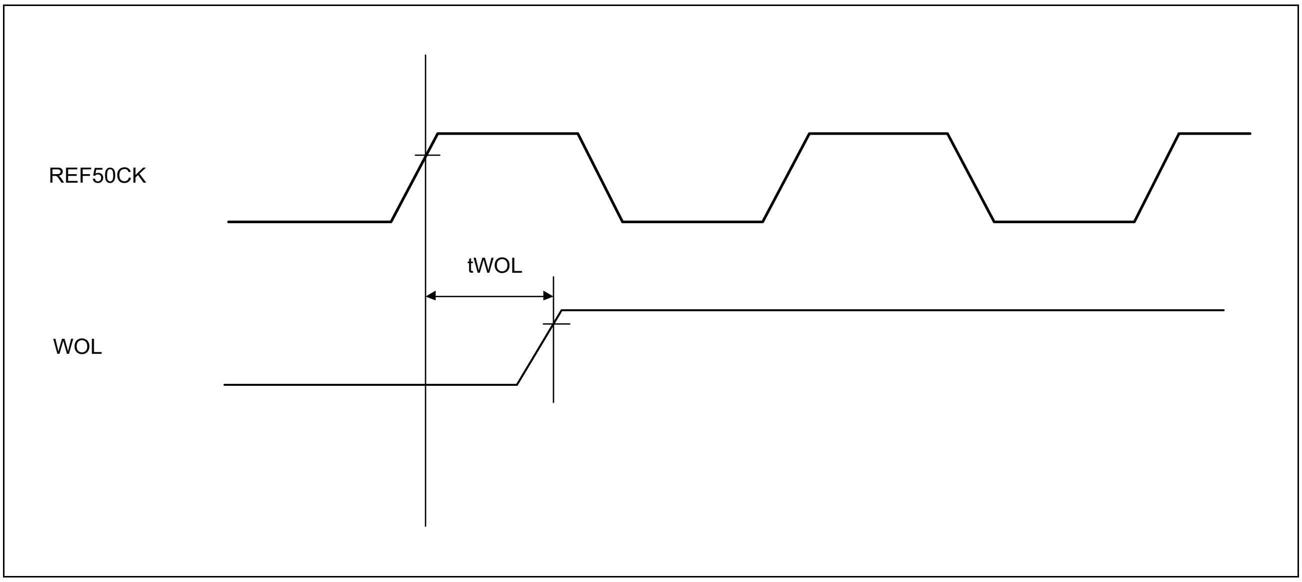


Figure 1.37 WOL Timing — RMII

1.3.12 Debug Interface Mode Timing

Table 1.46 Debug Interface Mode Timing

Conditions: CL = 30 pF

Item	Symbol	Min.	Max.	Unit	Reference
TCK (JP0_2) input timing before $\overline{\text{TRST}}$	$t_{DBGIFSWCK}$	$10 \times t_{LPDCKW}$ $10 \times t_{TCKW}$	—	ns	**Figure 1.38**
TDI (JP0_0) setup time	$t_{DBGIFSWS}$	$10 \times t_{LPDCKW}$ $10 \times t_{TCKW}$		ns	
TDI (JP0_0) hold time	$t_{DBGIFSWH}$	2		µs	

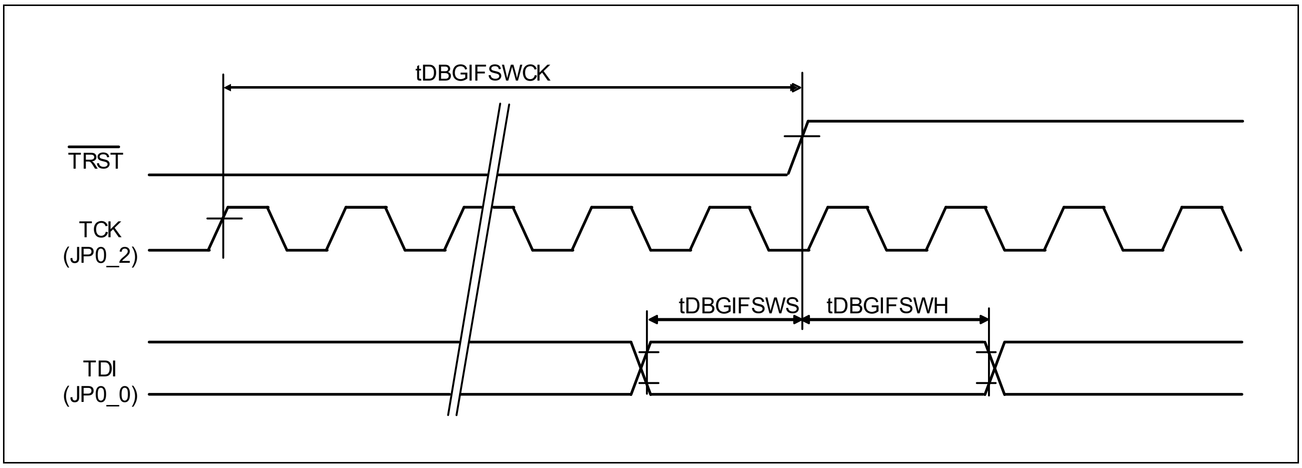


Figure 1.38 Debug Interface Mode Timing

1.3.13 JTAG / Nexus Timing

Table 1.47 JTAG / Nexus Timing

Conditions: CL = 30 pF

Item	Symbol	Condition	Min.	Max.	Unit	Reference
TCK cycle time	t_{TCKW}		25	—	ns	**Figure 1.39**
TCK high-level width	t_{TCKWH}		10	—	ns	
TCK low-level width	t_{TCKWL}		10	—	ns	
TMS / TDI setup time (until TCK ↑)	t_{TISU}		6	—	ns	
TMS / TDI hold time (until TCK ↑)	t_{TIH}		6	—	ns	
TDO output delay time (until TCK ↓)	t_{TDOD}		—	14	ns	
$\overline{\text{DRDY}}$ output delay time (until TCK ↓)	t_{RDYD}		—	14	ns	
$\overline{\text{TRST}}$ low-level width	t_{TRSTWL}		1200	—	ns	
TCK / $\overline{\text{TRST}}$ / TMS / TDI input rise time	t_{TIR}		—	4	ns	
TCK / $\overline{\text{TRST}}$ / TMS / TDI input fall time	t_{TIF}		—	4	ns	

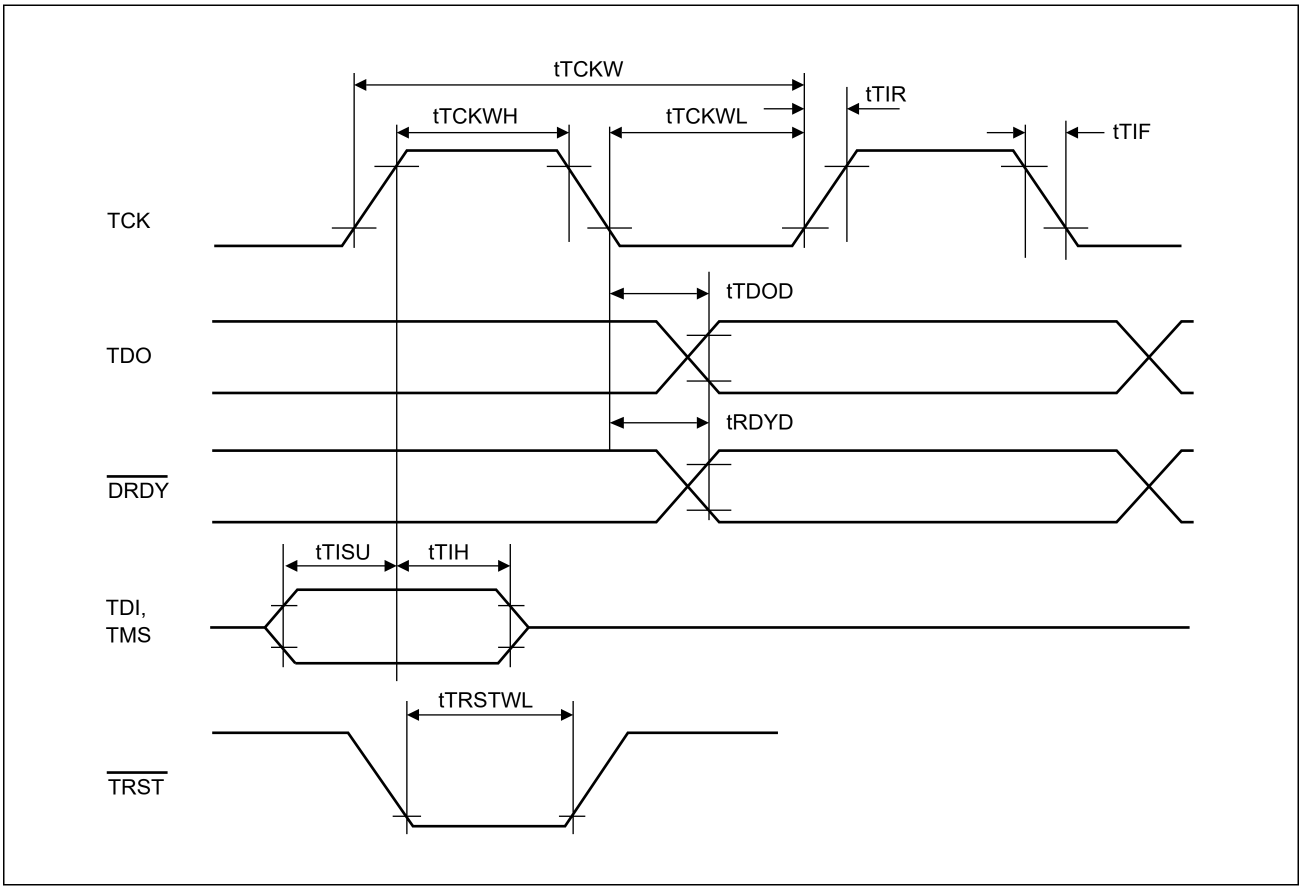


Figure 1.39 JTAG / Nexus Timing

Table 1.48 Boundary-Scan Timing

Conditions: CL = 30 pF

Item	Symbol	Condition	Min.	Max.	Unit	Reference
TCK cycle time	t_{BSTCKW}		100	—	ns	**Figure 1.40**
TCK high-level width	$t_{BSTCKWH}$		0.4	0.6	t_{BSTCKW}	
TCK low-level width	$t_{BSTCKWL}$		0.4	0.6	t_{BSTCKW}	
TMS / TDI setup time (until TCK ↑)	t_{BSTISU}		30	—	ns	
TMS / TDI hold time (until TCK ↑)	t_{BSTIH}		30	—	ns	
TDO output delay time (until TCK ↓)	t_{BSTDOD}		—	35	ns	
$\overline{\text{TRST}}$ low-level width	$t_{BSTRSTWL}$		1200	—	ns	

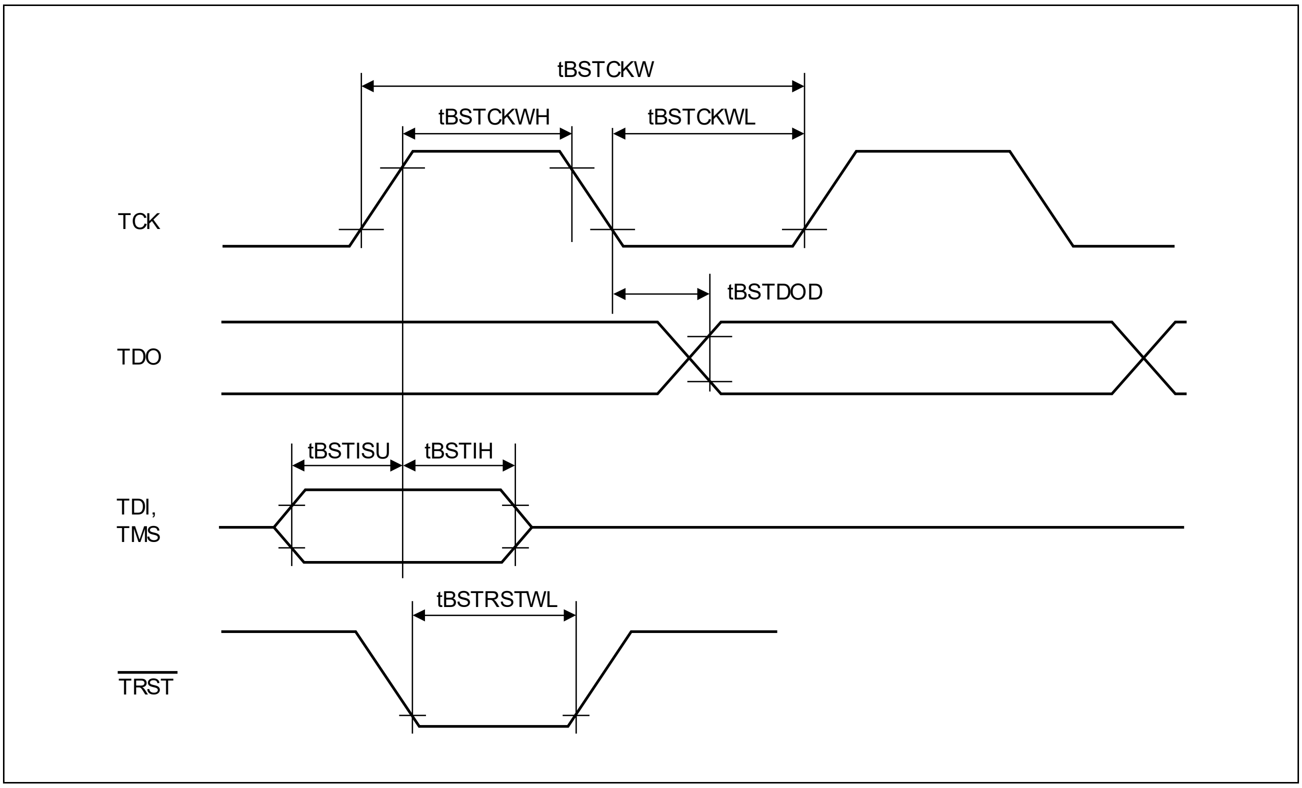


Figure 1.40 Boundary-Scan Timing

1.3.14 LPD (4-pin) Interface Timing

Table 1.49 LPD (4-pin) Interface Timing

Conditions: CL = 30 pF

Item	Symbol	Condition	Min.	Max.	Unit	Reference
LPDCLK cycle time	t_{LPDCKW}		25	—	ns	**Figure 1.41**
LPDCLK high-level width	$t_{LPDCKWH}$		4.5	—	ns	
LPDCLK low-level width	$t_{LPDCKWL}$		4.5	—	ns	
LPDCLK input rise time	t_{LPDCKR}		—	8	ns	
LPDCLK input fall time	t_{LPDCKF}		—	8	ns	
LPDI setup time (until LPDCLK ↑)	t_{LPDSU}		3	—	ns	
LPDI hold time (until LPDCLK ↑)	t_{LPDH}		3	—	ns	
LPDCLKO cycle time	$t_{LPDCKOW}$		25	—	ns	
LPDCLKO high-level width	$t_{LPDCKOWH}$		$t_{LPDCKWH}$ − 2	—	ns	
LPDCLKO low-level width	$t_{LPDCKOWL}$		$t_{LPDCKWL}$ − 2	—	ns	
LPDCLKO rise time	$t_{LPDCKOR}$		—	8	ns	
LPDCLKO fall time	$t_{LPDCKOF}$		—	8	ns	
LPDO output delay (until LPDCLKO ↑)	t_{LPDOD}		0	14	ns	

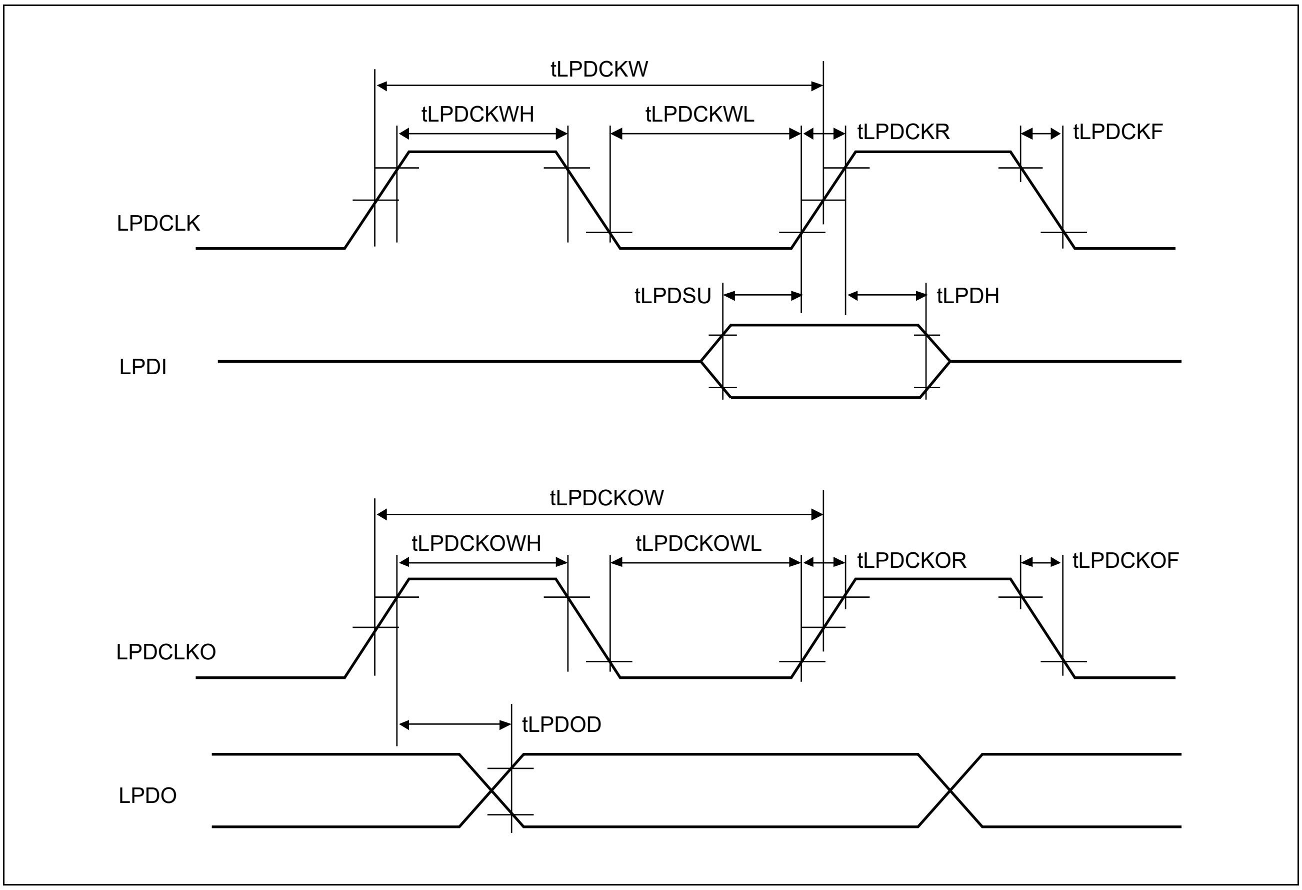


Figure 1.41 LPD (4-pin) Interface Timing

1.3.15 RLIN3 Timing

Table 1.50 RLIN3 Timing

Conditions: CL = 50 pF, Drive strength = 4, Buffer type Sch1, E0VCC = E1VCC = E2VCC = 5.0 ± 0.5 V

Item	Symbol	Condition	Min.	Max.	Unit	Reference
RLIN3 transfer rate	—	LIN mode	—	20	kbps	
	—	UART mode	—	6.6	Mbps	

NOTE

This AC characteristics is limited to specific pin groups. For details, please refer to Appendix file "*Limited_conditions_for_AC_specification.xlsx*".

1.3.16 PSI5-S Timing

Table 1.51 PSI5-S Timing

Conditions: CL = 20 pF, Drive strength = 4, Buffer type Sch1, E0VCC = E1VCC = E2VCC = 5.0 ± 0.5 V

Item	Symbol	Condition	Min.	Max.	Unit	Reference
PSI5-S transfer rate	—	PSI5-S mode	—	5.3	Mbps	
	—	UART mode	—	5.3	Mbps	
Output clock cycle	$t_{PSIScyc}$	PSI5-S mode	37.74	—	ns	**Figure 1.42**
Output clock pulse width	$t_{PSISCKW}$	PSI5-S mode	$0.4 \times t_{PSIScyc}$	$0.6 \times t_{PSIScyc}$	ns	

NOTE

This AC characteristics is limited to specific pin groups. For details, please refer to Appendix file "*Limited_conditions_for_AC_specification.xlsx*".

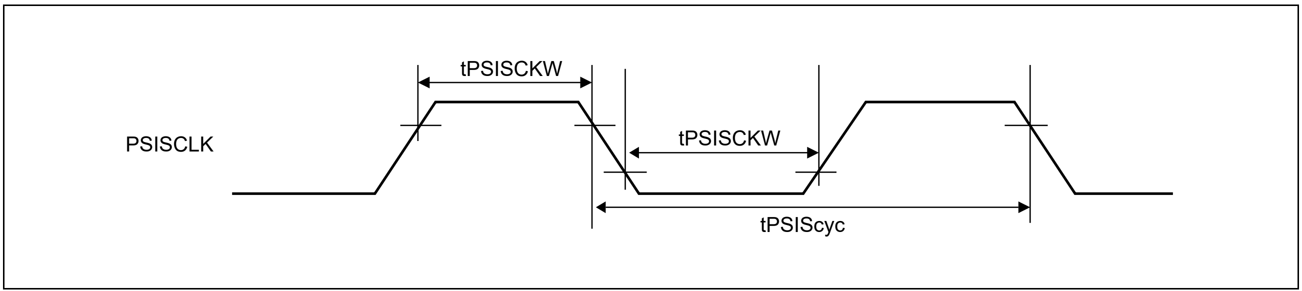


Figure 1.42 PSI5-S Clock Output Timing

1.3.17 HS-SPI Timing

Table 1.52 HS-SPI Timing in Master Mode (LVDS Mode)

Conditions: CL = 20 pF, E0VCC = E1VCC = E2VCC = 5.0 ± 0.5 V

Item	Symbol	Condition	Min.	Max.	Unit	Reference
HSSPInCLKP cycle	t_{HCcyc}		50	—	ns	**Figure 1.43**
HSSPInCLKP high-level width	t_{HCWH}		t_{HCcyc} × 0.45	—	ns	
HSSPInCLKP low-level width	t_{HCWL}		t_{HCcyc} × 0.45	—	ns	
HSSPInRXD setup time	t_{SMI1}	HSPInCPHA = 1	12	—	ns	
HSSPInRXD hold time	t_{HMI1}	HSPInCPHA = 1	0	—	ns	
HSSPInTXD output hold time	t_{HMO1}	HSPInCPHA = 1	t_{HCWH} / 2	—	ns	
HSSPInCLKP to HSSPInTXD delay time	t_{DMO1}	HSPInCPHA = 1	—	7	ns	
HSSPInSSL to HSSPInTXD delay time	t_{DMO3}	HSPInCPHA = 0	—	t_{HCcyc} / 2	ns	
HSSPInRXD setup time	t_{SMI2}	HSPInCPHA = 0	12	—	ns	
HSSPInRXD hold time	t_{HMI2}	HSPInCPHA = 0	0	—	ns	
HSSPInTXD output delay time	t_{DMO2}	HSPInCPHA = 0	—	7	ns	
HSSPInTXD output hold time	t_{HMO2}	HSPInCPHA = 0	t_{HCWH} / 2	—	ns	

Table 1.53 HS-SPI Timing in Master Mode (Single-ended Mode)

Conditions: CL = 20 pF, Drive strength = 4, Buffer type Sch1, E0VCC = E1VCC = E2VCC = 5.0 ± 0.5 V

Item	Symbol	Condition	Min.	Max.	Unit	Reference
HSSPInCLKP cycle	t_{HCcyc}		50	—	ns	**Figure 1.44**
HSSPInCLKP high-level width	t_{HCWH}		t_{HCcyc} × 0.45	—	ns	
HSSPInCLKP low-level width	t_{HCWL}		t_{HCcyc} × 0.45	—	ns	
HSSPInRXD setup time	t_{SMI1}	HSPInCPHA = 1	12	—	ns	
HSSPInRXD hold time	t_{HMI1}	HSPInCPHA = 1	0	—	ns	
HSSPInTXD output hold time	t_{HMO1}	HSPInCPHA = 1	t_{HCWH} / 2	—	ns	
HSSPInCLKP to HSSPInTXD delay time	t_{DMO1}	HSPInCPHA = 1	—	7	ns	
HSSPInSSL to HSSPInTXD delay time	t_{DMO3}	HSPInCPHA = 0	—	t_{HCcyc} / 2	ns	
HSSPInRXD setup time	t_{SMI2}	HSPInCPHA = 0	12	—	ns	
HSSPInRXD hold time	t_{HMI2}	HSPInCPHA = 0	0	—	ns	
HSSPInTXD output delay time	t_{DMO2}	HSPInCPHA = 0	—	7	ns	
HSSPInTXD output hold time	t_{HMO2}	HSPInCPHA = 0	t_{HCWH} / 2	—	ns	

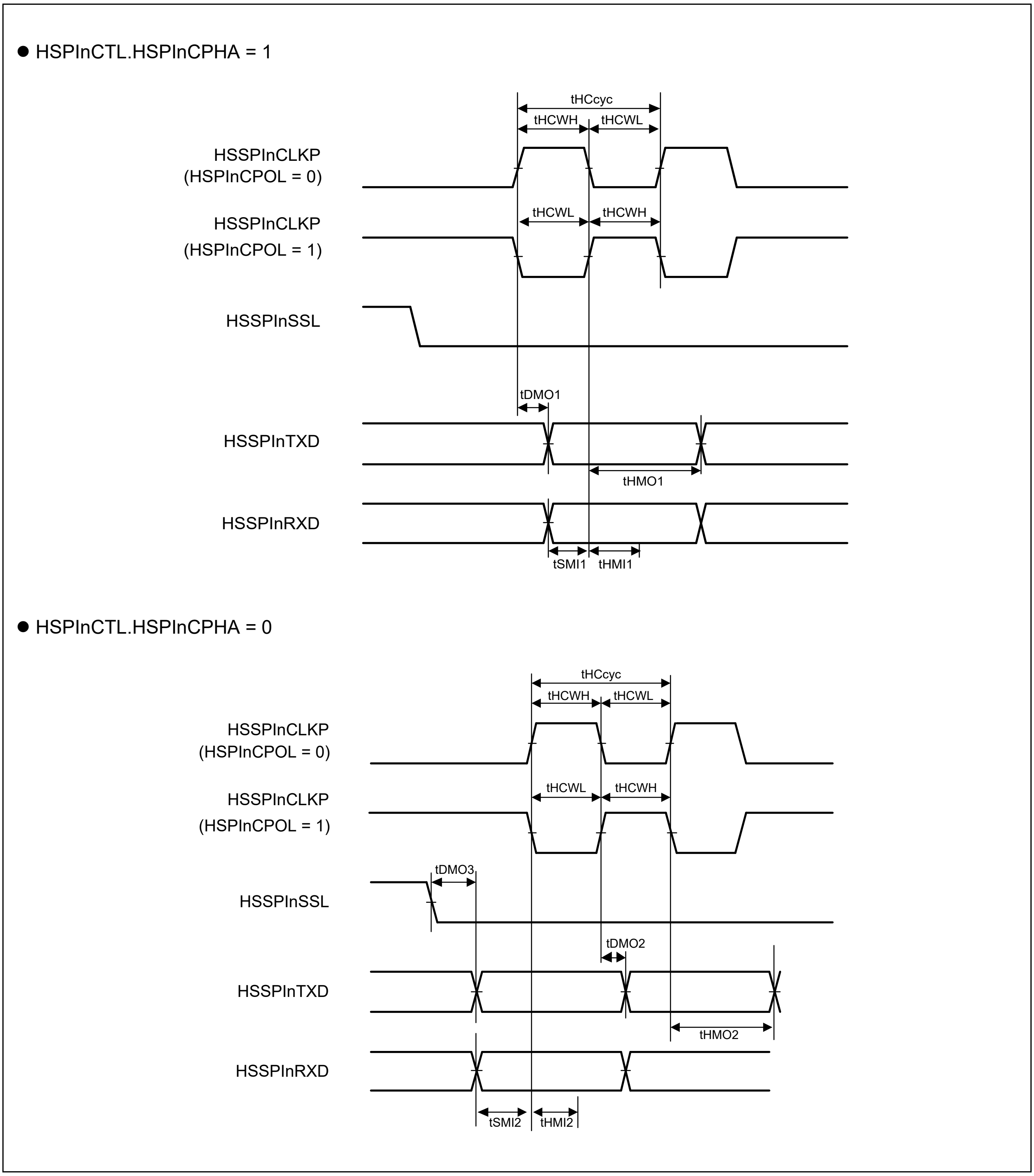


Figure 1.43 HS-SPI Timing in Master Mode (LVDS Mode)

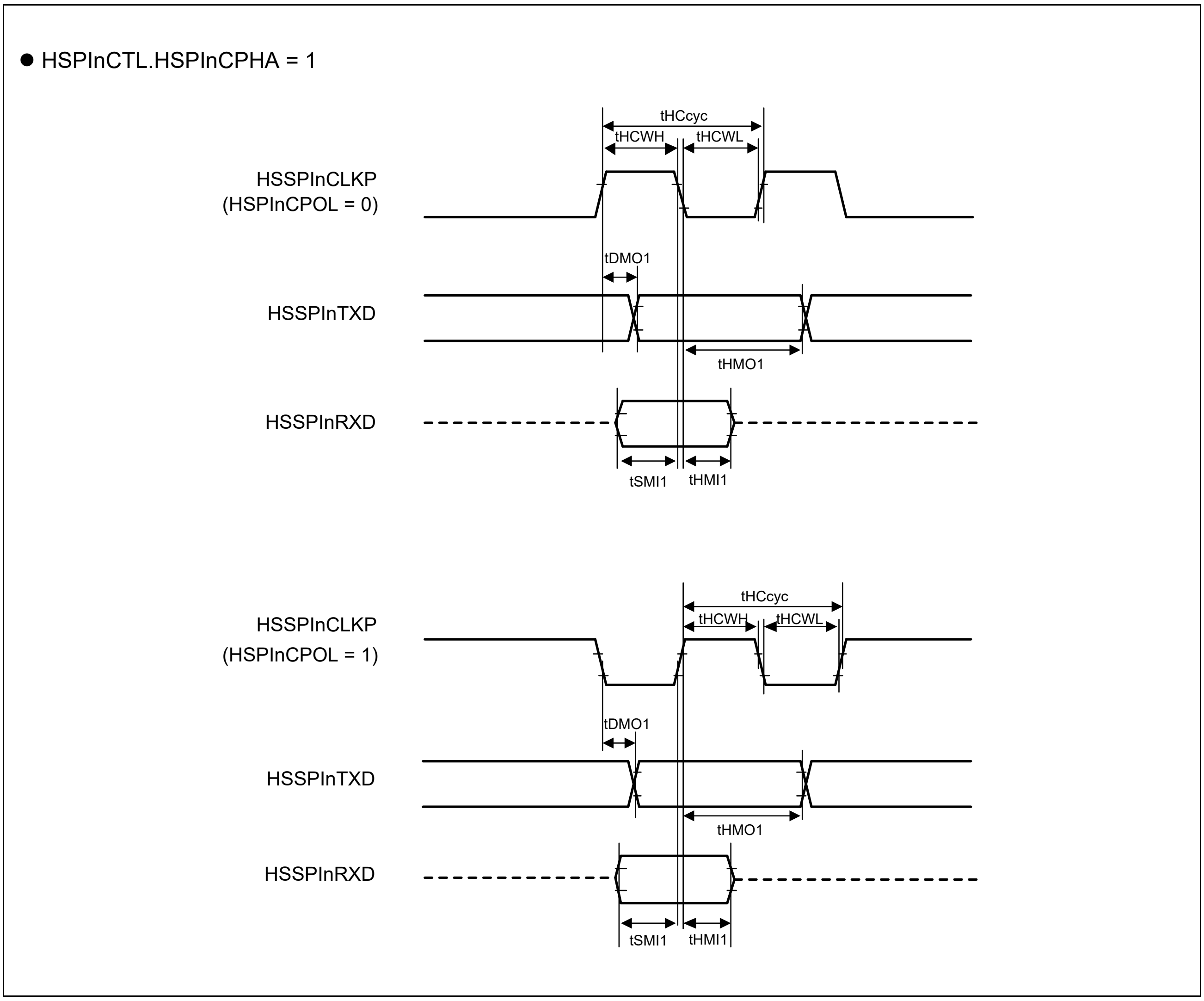


Figure 1.44 HS-SPI Timing in Master Mode (Single-ended Mode) (1/2)

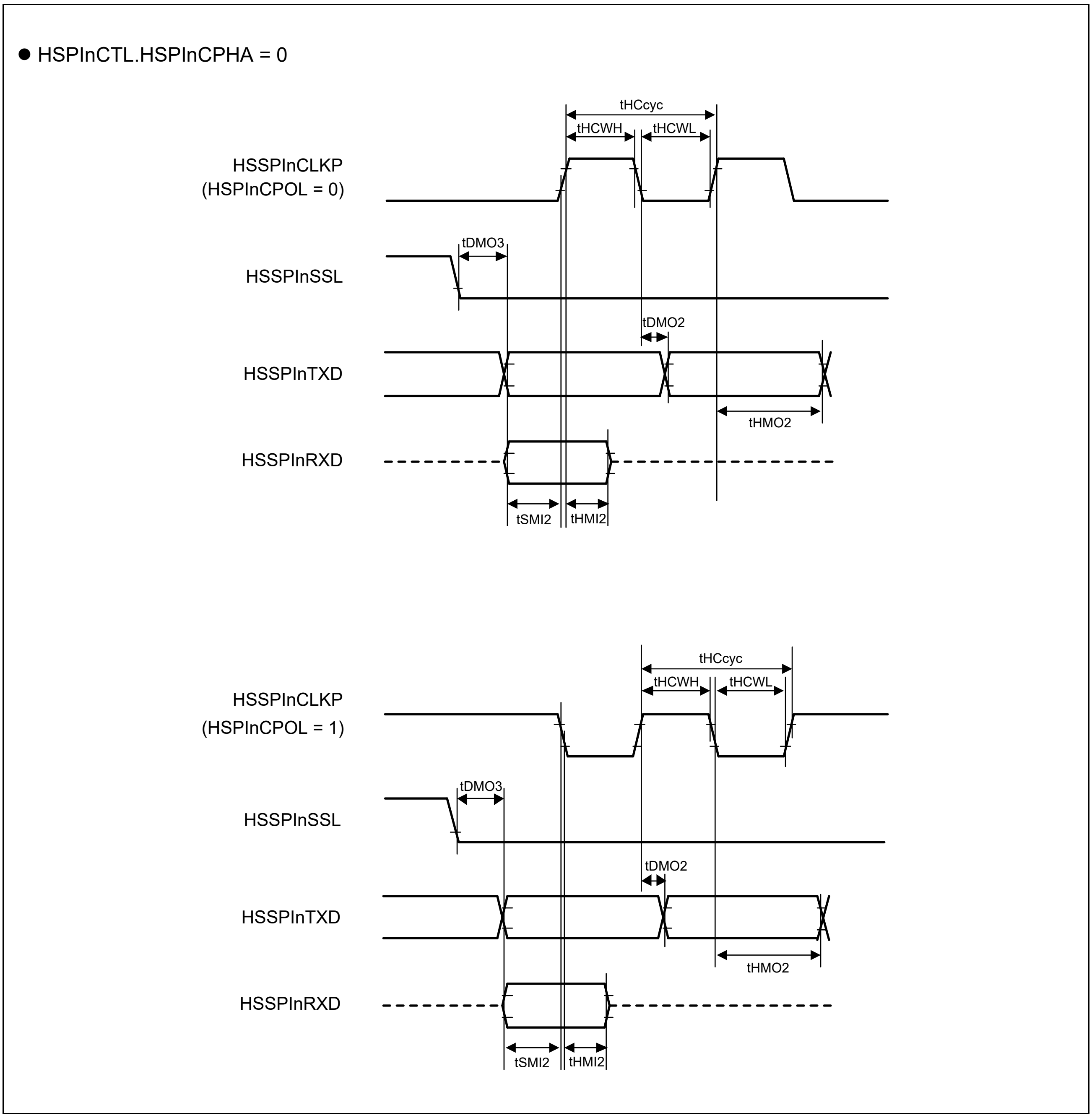


Figure 1.44 HS-SPI Timing in Master Mode (Single-ended Mode) (2/2)

Table 1.54 HS-SPI Timing in Slave Mode (LVDS Mode)

Conditions: CL = 20 pF, E0VCC = E1VCC = E2VCC = 5.0 ± 0.5 V

Item	Symbol	Condition	Min.	Max.	Unit	Reference
HSSPInCLKP cycle	t_{HCcyc}		50	—	ns	**Figure 1.45**
HSSPInCLKP high-level width	t_{HCWH}		t_{HCcyc} × 0.45	—	ns	
HSSPInCLKP low-level width	t_{HCWL}		t_{HCcyc} × 0.45	—	ns	
HSSPInRXD setup time	t_{SSI1}	HSPInCPHA = 1	10	—	ns	
HSSPInRXD hold time	t_{HSI1}	HSPInCPHA = 1	t_{Htxclk} + 5	—	ns	
HSSPInTXD output delay time	t_{DSO1}	HSPInCPHA = 1	—	20	ns	
HSSPInTXD output hold time	t_{HSO1}	HSPInCPHA = 1	t_{HCWH}	—	ns	
HSSPInRXD setup time	t_{SSI2}	HSPInCPHA = 0	10	—	ns	
HSSPInRXD hold time	t_{HSI2}	HSPInCPHA = 0	t_{Htxclk} + 5	—	ns	
HSSPInTXD output delay time	t_{DSO2}	HSPInCPHA = 0	—	20	ns	
HSSPInTXD output hold time	t_{HSO2}	HSPInCPHA = 0	t_{HCWH}	—	ns	
HSSPInSSLI setup time	t_{SSSI}		(t_{HCcyc} / 2) − 10	—	ns	**Figure 1.46**
HSSPInSSLI hold time	t_{HSSI}		t_{HCWH} + 5	—	ns	

Note: t_{Htxclk} is comunication clock cycle of HS-SPI (CLK_HSB).

Table 1.55 HS-SPI Timing in Slave Mode (Single-ended Mode)

Conditions: CL = 20 pF, Drive strength = 4, Buffer type Sch1, E0VCC = E1VCC = E2VCC = 5.0 ± 0.5 V

Item	Symbol	Condition	Min.	Max.	Unit	Reference
HSSPInCLKP cycle	t_{HCcyc}		50	—	ns	**Figure 1.47**
HSSPInCLKP high-level width	t_{HCWH}		t_{HCcyc} × 0.45	—	ns	
HSSPInCLKP low-level width	t_{HCWL}		t_{HCcyc} × 0.45	—	ns	
HSSPInRXD setup time	t_{SSI1}	HSPInCPHA = 1	10	—	ns	
HSSPInRXD hold time	t_{HSI1}	HSPInCPHA = 1	t_{Htxclk} + 5	—	ns	
HSSPInTXD output delay time	t_{DSO1}	HSPInCPHA = 1	—	20	ns	
HSSPInTXD output hold time	t_{HSO1}	HSPInCPHA = 1	t_{HCWH}	—	ns	
HSSPInRXD setup time	t_{SSI2}	HSPInCPHA = 0	10	—	ns	
HSSPInRXD hold time	t_{HSI2}	HSPInCPHA = 0	t_{Htxclk} + 5	—	ns	
HSSPInTXD output delay time	t_{DSO2}	HSPInCPHA = 0	—	20	ns	
HSSPInTXD output hold time	t_{HSO2}	HSPInCPHA = 0	t_{HCWH}	—	ns	
HSSPInSSLI setup time	t_{SSSI}		(t_{HCcyc}/2) − 10	—	ns	**Figure 1.48**
HSSPInSSLI hold time	t_{HSSI}		t_{HCWH} + 5	—	ns	

Note: t_{Htxclk} is comunication clock cycle of HS-SPI (CLK_HSB).

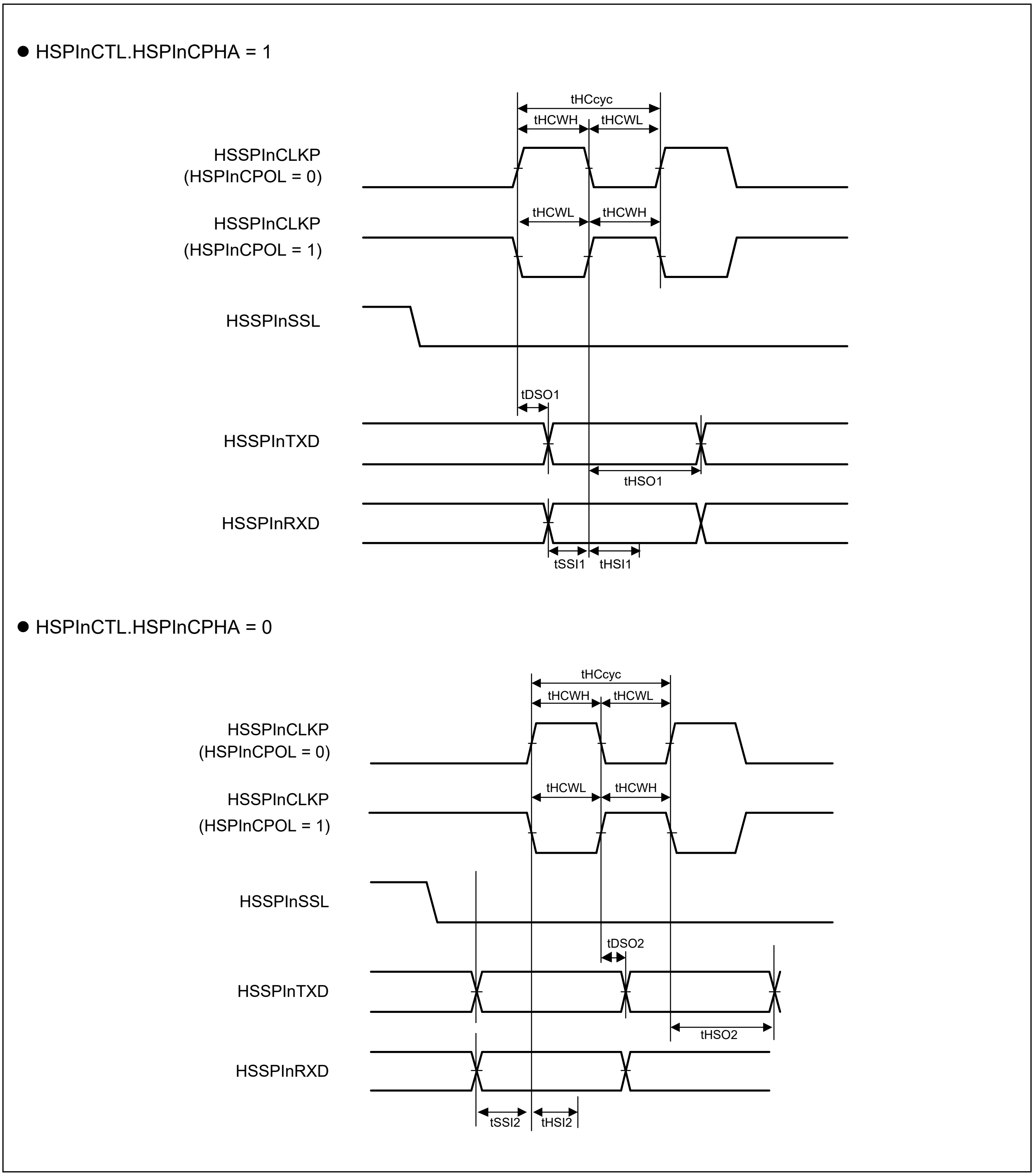


Figure 1.45 HS-SPI Timing in Slave Mode (LVDS Mode)

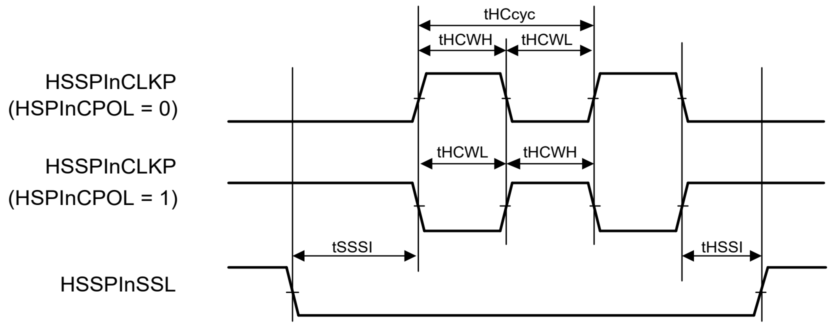


Figure 1.46 HS-SPI SSL Timing in Slave Mode (LVDS Mode)

● HSPInCTL.HSPInCPHA = 1

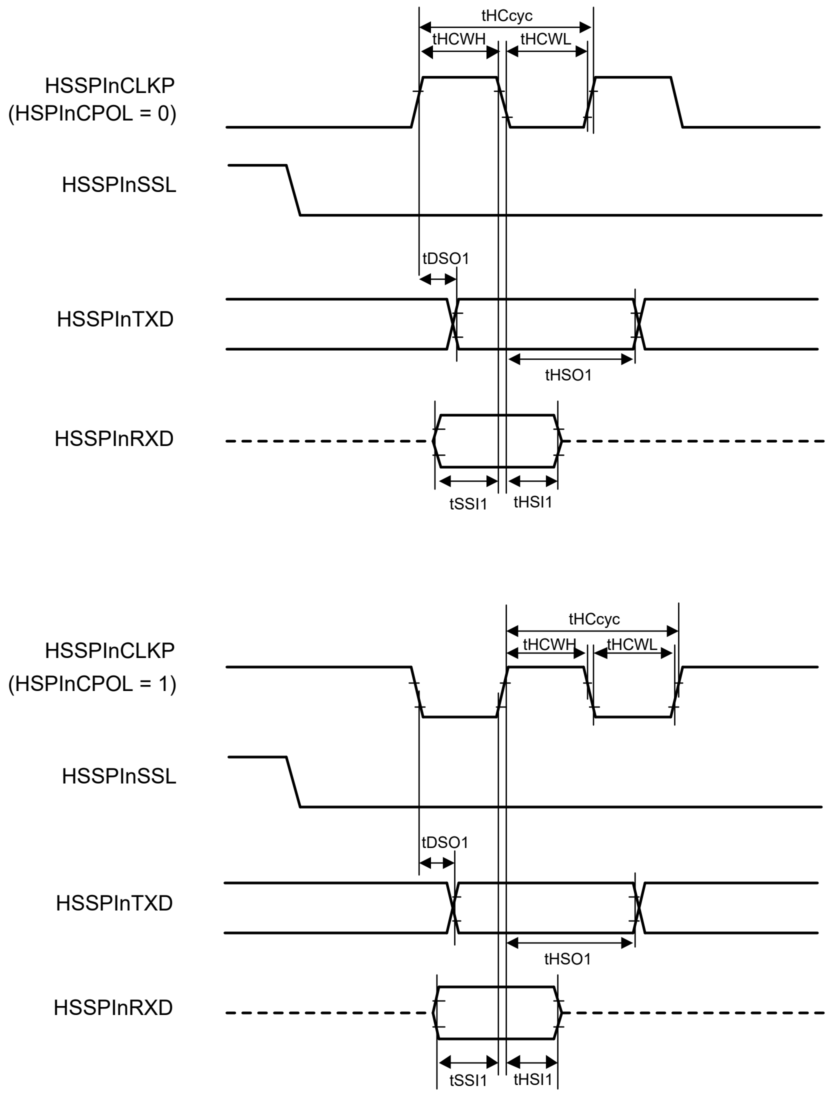


Figure 1.47 HS-SPI Timing in Slave Mode (Single-ended Mode) (1/2)

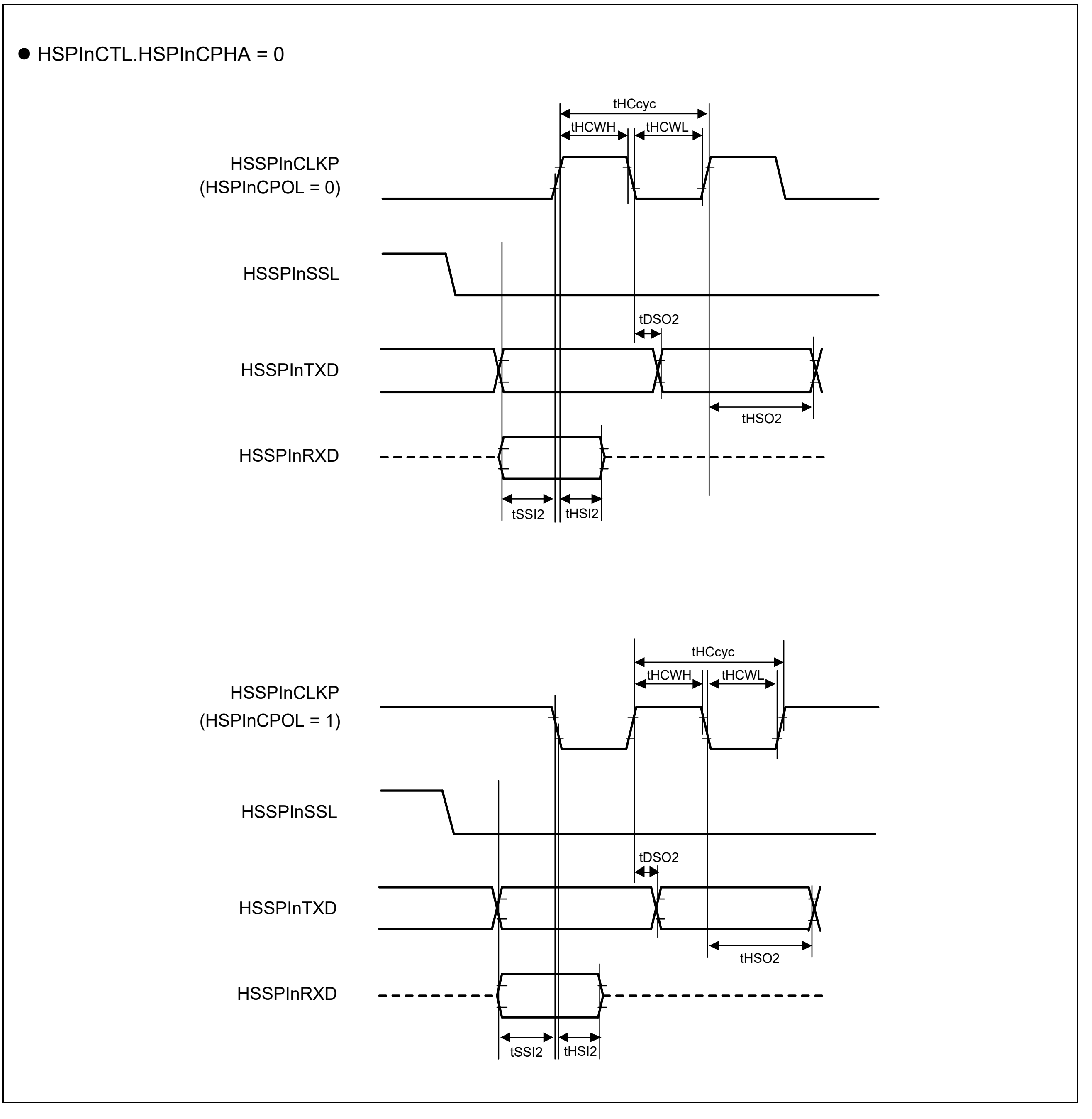


Figure 1.47 HS-SPI Timing in Slave Mode (Single-ended Mode) (2/2)

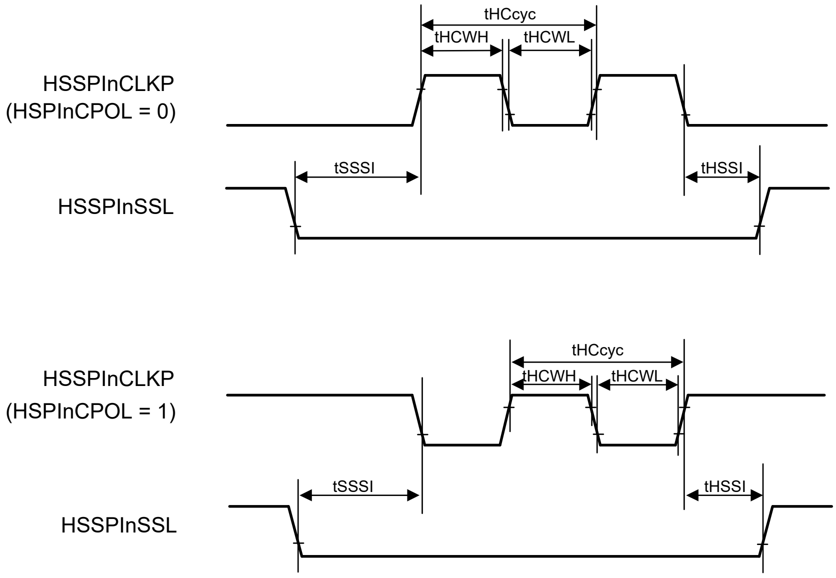


Figure 1.48 HS-SPI SSL Timing in Slave Mode (Single-ended Mode)

1.3.18 RHSIF Timing

Table 1.56 External Reference Clock Input / Output Characteristics

Conditions: CL = 15 pF, Drive strength = 3, Buffer type Sch1, E0VCC = 5.0 ± 0.5 V

Item	Symbol	Min.	Typ.	Max.	Unit	Reference
External Reference Clock Input frequency	f_{REFCKI}	10	—	20	MHz	—
External Reference Clock Input duty cycle	DC_{REFCKI}	35	—	65	%	
External Reference Clock output frequency	f_{REFCKO}	10	—	20	MHz	
External Reference Clock output duty cycle	DC_{REFCKO}	35	—	65	%	

Table 1.57 RHSIF Transmit Data Timing (3.3V)

Conditions: RHSIFnREFCLK CL = 15 pF, Drive strength = 3, E0VCC = 5.0 ± 0.5 V
RHSIFnTXDP CL = 5 pF, LVDVCC = 3.3 ± 0.3 V
RHSIFnTXDN

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Reference
Transmit data cycle	f_{TX}	Slow mode	—	—	5	M Baud	—
		Fast mode	—	—	160	M Baud	—
Transmit data delay time (RHSIFnREFCLK output)	t_{TXDD}	Slow mode RHSIFnREFCLK 20MHz	−20	—	20	ns	**Figure 1.49**
		Slow mode RHSIFnREFCLK 10MHz	15	—	85	ns	**Figure 1.49**
		Fast mode	—	—	—	ns	Asynchronous
Transmit data delay time (RHSIFnREFCLK input)	t_{TXDDI}	Slow mode	0	—	60	ns	**Figure 1.49**
		Fast mode	—	—	—	ns	Asynchronous

Table 1.58 RHSIF Transmit Data Timing (5V)

Conditions: RHSIFnREFCLK CL = 15 pF, Drive strength = 3, E0VCC = 5.0 ± 0.5 V
RHSIFnTXDP CL = 5 pF, LVDVCC = 5.0 ± 0.5 V
RHSIFnTXDN

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Reference
Transmit data cycle	f_{TX}	Slow mode	—	—	5	M Baud	—
		Fast mode	—	—	160	M Baud	—
Transmit data delay time (RHSIFnREFCLK output)	t_{TXDD}	Slow mode RHSIFnREFCLK 20MHz	−20	—	20	ns	**Figure 1.49**
		Slow mode RHSIFnREFCLK 10MHz	15	—	85	ns	**Figure 1.49**
		Fast mode	—	—	—	ns	Asynchronous
Transmit data delay time (RHSIFnREFCLK input)	t_{TXDDI}	Slow mode	0	—	60	ns	**Figure 1.49**
		Fast mode	—	—	—	ns	Asynchronous

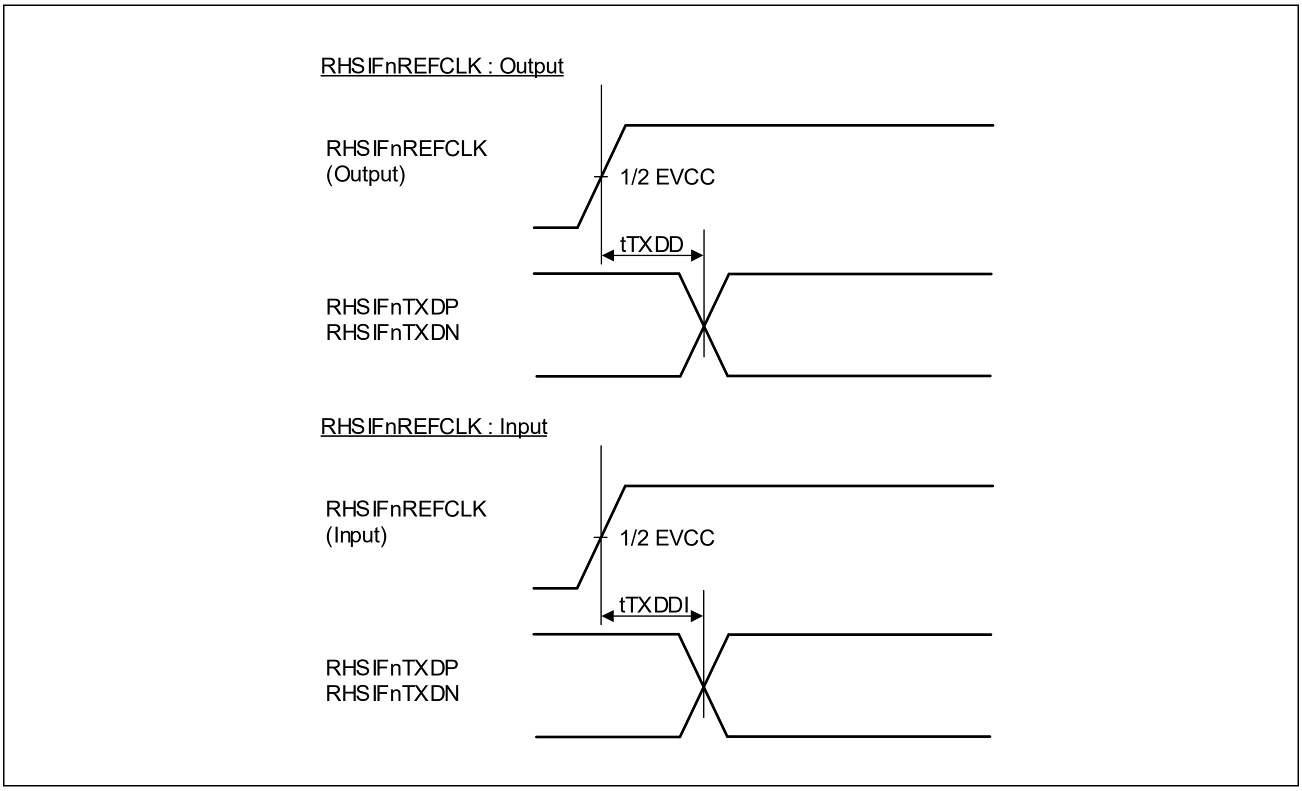
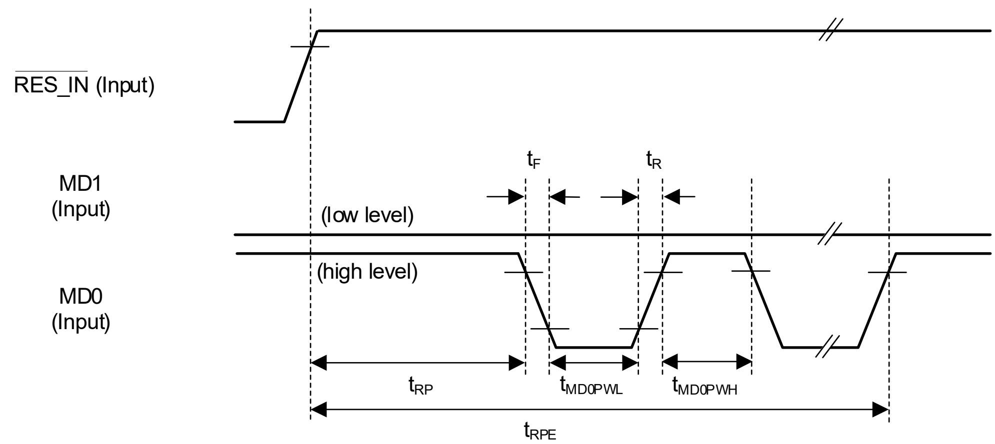


Figure 1.49 RHSIF Transmit Data Timing

1.3.19 Serial Programmer Setup Timing

Table 1.59 Serial Programmer Setup Timing

Item	Symbol	Min.	Typ.	Max.	Unit
MD0 pulse input start time	t_{RP}	1.5	—	—	ms
MD0 pulse input end time	t_{RPE}	—	—	100	ms
MD0 low/high level width	t_{MD0PWL} / t_{MD0PWH}	2	—	—	µs
MD0 rise time	t_R	—	—	20	ns
MD0 fall time	t_F	—	—	20	ns



Note: Input the MD0 pulses between $t_{RP(MIN)}$ and $t_{RPE(MAX)}$.
For MD0 pulses, See *Section 41.6.4, Selection of Communication Method*.

Figure 1.50 Serial Programmer Setup Timing

1.4 A/D Converter Characteristics

1.4.1 SAR A/D Converter Characteristics

Table 1.60 SAR A/D Converter Characteristics

Item		Symbol	Min.	Typ.	Max.	Unit	Reference
Digital resolution		—	10	—	12	bit	
Voltage resolution (12 bit)*1		—	1.10	1.22	1.34	mV	
A/D conversion time		—	—	1.0*4	—	μs	
Integral nonlinearity error		INL	−3.0*2	—	+3.0*2	LSB	
Differential nonlinearity error		DNL	−1.0*2	—	+2.0*2	LSB	
Offset error		OSE	−3.5*2	—	+3.5*2	LSB	
Full scale error		FSE	−3.5*2	—	+3.5*2	LSB	
Quantization error		QE	−0.5	—	+0.5	LSB	
Total unadjusted error		TUE	−4.0*3	—	+4.0*3	LSB	
Self-diagnosis absolute error	Self-diagnosis of internal ADC	—	−8.0	—	+8.0	LSB	
	Pin-level self-diagnosis	—	−40.0	—	+40.0	LSB	
Secondary power supply voltage monitor absolute error*5	VCC, EVCC	—	−16.0	—	+16.0	LSB	
	VDD	—	−10.0	—	+10.0	LSB	
Input capacitance	Waiting	—	—	—	10	pF	
	Sampling	—	—	—	20	pF	
Allowable analog signal source impedance		—	—	—	3	kΩ	
Analog input voltage range		—	0.0	—	AnVREFH	V	

Note 1. When AnVREFH (n = 0, 1, 2, 3) = 4.5 V, the resolution is 1.10 mV.
When AnVREFH (n = 0, 1, 2, 3) = 5.5 V, the resolution is 1.34 mV.

Note 2. Quantization error is not included.

Note 3. Sampling error is not included.

Note 4. This value is t_{SPL} + t_{SAR} which is specified in *Section 34.4.12, Timing Regulations* of *Section 34, Analog to Digital Converter (ADCH)*. And it is decided logically, so it has typical value only.

Note 5. The error depends on the operating conditions, especially for errors in monitoring VDD.

Sampling Errors in the External Circuit of the A/D Convertor

Sampling error is error to which “Errors (Sampling error 1) which depend on input leakage current of analog pin” and “Errors (Sampling error 2) which depend on conversion cycles with charge sharing” were added.

$$\text{Sampling error} = \text{Sampling error 1} + \text{sampling error 2}$$

Figure 1.51 Sampling Error Formula

The external circuits of the A/D pins which become the factor of sampling error (sampling error 1 and sampling error 2) are shown below.

a) Errors (Sampling error 1) which depend on input leakage current of analog pin

The error depends on the input leakage current (ILeak) of analog pin and external resistance (Re), and occurs.

The error which depends on the input leakage current is given by the formula of the following.

$$\text{Sampling error 1 (LSB)} = \text{Re} \times \text{ILeak} \times \frac{4096}{\text{AnVREFH}}$$

Figure 1.52 Sampling Error 1 Formula

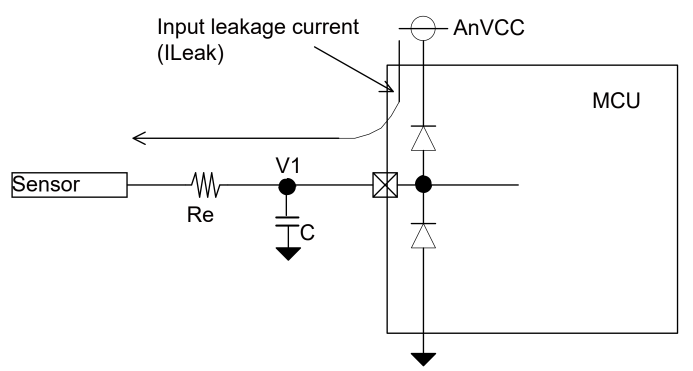


Figure 1.53 Errors (Sampling error 1) which Depend on Input Leakage Current of Analog Pin

b) Errors (Sampling error 2) which depend on conversion cycles with charge sharing

A formula for errors in sampled values due to the external circuit of the A/D converter is given below.

These errors will depend on the input circuit and conversion cycle. The formula given below for the errors is simplified for the calculation of sampling error 2 based on internal stray capacitance, amplifier offset, resistance of the signal source, and conversion cycle. This formula can also be used to calculate the effects of the signal source resistance and conversion cycle on these errors.

The formula gives the error of analog input 2 as shown in the figure below when A/D conversion is performed in the order of analog input 1 then 2.

$$\text{Sampling error 2 (LSB)} = \left[\left(\frac{|V2\text{-}V1| \times CIN1}{Ce+CIN1} + \frac{|Vvfaerr| \times CIN2}{Ce+CIN2}\right) \times \frac{1}{1\text{-}e^{-T1/(Re \times Ce)}} + \left(\frac{1}{T1} \times C1 \times V3 \times Re\right)\right] \times \frac{4096}{Vavrefh}$$

Figure 1.54 Sampling Error 2 Formula

Table 1.61 Definition of the symbols for the Sampling Error Formula

Item	Symbol	Reference	Unit
Common capacitance of the final stage of channel multiplexer	CIN1	1.4	pF
Common capacitance of the final stage of the amplifier	CIN2	10	pF
External capacitor on analog input pin	Ce	Depends on user board	μF
Signal source impedance	Re		KΩ
Conversions cycle of analog Input pins	T1		ms
AnVREFH voltage (n = 0, 1, 2, 3)	Vavrefh		V
Potential difference between V1 and V2	V2-V1		V
Offset voltage of the amplifier	Vvfaerr	50	mV
Parasitic capacitance in the channel multiplexer	C1	2	pF
|AnVCC voltage / 2.5 - measured pin voltage (V2)| (n = 0, 1, 2, 3)	V3	Depends on user board	V

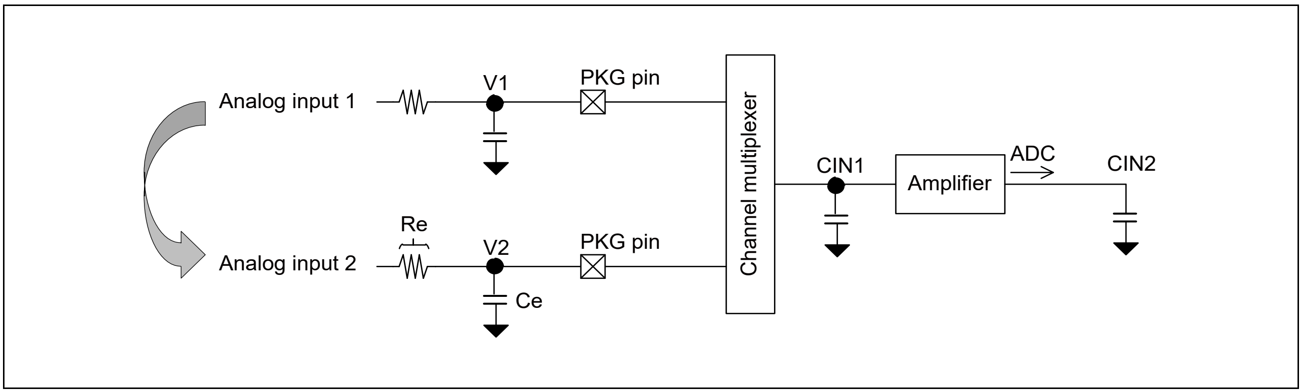


Figure 1.55 Schematic for Sampling Error 2 Formula

- Values for conversion error calculated by using this formula do not include error (absolute error, etc.) specified in the A/D converter characteristics.
- This formula is a desktop formula and is theoretical. When the signal source has an extremely high resistance or when the conversion cycle is too short, calculated and measured values may differ. Actual error depends on the external capacitor, external resistor, capacitance and resistance of board wiring, so please evaluate and verify the error on the user board is no greater than the value produced by this formula (Condition of this formula is “Re < 1.5 MΩ and T1 ≥ 10 μs”, or “1.5 MΩ ≤ Re ≤ 2 MΩ and T1 ≥ 512 μs”).

1.4.2 Delta-Sigma A/D Converter Characteristics

Table 1.62 Delta-Sigma A/D Converter Characteristics (High resolution mode) (ENOB, SNDR, input Impedance)

Item	Symbol	Conditions			Value			Unit
		Input	Filter Type	Gain	Min.	Typ.	Max.	
ENOB*1	ENOB	differential	F1a, F1b, F2, F3a, F3b, F4	×1	13	—	—	bit
SNDR*2	SNDR	differential	F1a, F1b, F2, F3a, F3b, F4	×1	80	—	—	dB
				×2	80	—	—	dB
			F5	×1	65	—	—	dB
				×2	65	—	—	dB
			F6	×1	62	—	—	dB
				×2	62	—	—	dB
			F7	×1	56	—	—	dB
				×2	56	—	—	dB
		single-ended (reference of ADSVREFH/2)	F1a, F1b, F2, F3a, F3b, F4	×1	75	—	—	dB
				×2	80	—	—	dB
			F5	×1	59	—	—	dB
				×2	65	—	—	dB
			F6	×1	56	—	—	dB
				×2	62	—	—	dB
			F7	×1	50	—	—	dB
				×2	56	—	—	dB
		single-ended (reference of ADSVREFL)	F1a, F1b, F2, F3a, F3b, F4	×1	75	—	—	dB
				×2	75	—	—	dB
			F5	×1	59	—	—	dB
				×2	59	—	—	dB
			F6	×1	56	—	—	dB
				×2	56	—	—	dB
			F7	×1	50	—	—	dB
				×2	50	—	—	dB
Input impedance	—	—		×1	200	—	—	kΩ
				×2	100	—	—	kΩ

Note 1. Effective Number of Bits.

Note 2. Signal-to-Noise and Distortion Ratio.

Table 1.63 Delta-Sigma A/D Converter Characteristics (High resolution mode) (Offset error)

Item	Symbol	Conditions			Value			Unit
		Calibration	Input	Gain	Min.	Typ.	Max.	
Offset error *1	OSE	w/o calibration	differential	×1	−10.0	—	+10.0	mV
				×2	−10.0	—	+10.0	mV
			single-ended	×1	−10.0	—	+10.0	mV
				×2	−10.0	—	+10.0	mV
		w/ calibration*2	differential	×1	−5.0	—	+5.0	mV
				×2	−5.0	—	+5.0	mV
			single-ended	×1	−5.0	—	+5.0	mV
				×2	−5.0	—	+5.0	mV

Note 1. Quantization error is not included.

Note 2. Temperature change after calibration is less than 50°C. (−50°C < Temperature change < +50°C).

Table 1.64 Delta-Sigma A/D Converter Characteristics (High impedance mode) (ENOB, SNDR, input Impedance) (1/2)

Item	Symbol	Conditions			Value			Unit
		Input	Filter Type	Gain	Min.	Typ.	Max.	
ENOB*1	ENOB	differential	F1a, F1b, F2, F3a, F3b, F4	×1	12	—	—	bit
SNDR*2	SNDR	differential	F1a, F1b, F2, F3a, F3b, F4	×1	75	—	—	dB
				×2	75	—	—	dB
				×4	75	—	—	dB
				×8	69	—	—	dB
			F5	×1	65	—	—	dB
				×2	65	—	—	dB
				×4	65	—	—	dB
				×8	59	—	—	dB
			F6	×1	62	—	—	dB
				×2	62	—	—	dB
				×4	62	—	—	dB
				×8	56	—	—	dB
			F7	×1	50	—	—	dB
				×2	50	—	—	dB
				×4	50	—	—	dB
				×8	44	—	—	dB
		single-ended (reference of ADSVREFH/ 2)	F1a, F1b, F2, F3a, F3b, F4	×1	69	—	—	dB
				×2	75	—	—	dB
				×4	75	—	—	dB
				x8	69	—	—	dB
			F5	×1	59	—	—	dB
				×2	65	—	—	dB
				×4	65	—	—	dB
				×8	59	—	—	dB
			F6	×1	56	—	—	dB
				×2	62	—	—	dB
				×4	62	—	—	dB
				×8	56	—	—	dB
			F7	×1	44	—	—	dB
				×2	50	—	—	dB
				×4	50	—	—	dB
				×8	44	—	—	dB

Table 1.64 Delta-Sigma A/D Converter Characteristics (High impedance mode) (ENOB, SNDR, input Impedance) (2/2)

Item	Symbol	Conditions			Value			Unit
		Input	Filter Type	Gain	Min.	Typ.	Max.	
SNDR*2	SNDR	single-ended (reference of ADSVREFL)	F1a, F1b, F2, F3a, F3b, F4	×1	69	—	—	dB
				×2	69	—	—	dB
				×4	69	—	—	dB
				x8	63	—	—	dB
			F5	×1	59	—	—	dB
				×2	59	—	—	dB
				×4	59	—	—	dB
				×8	53	—	—	dB
			F6	×1	56	—	—	dB
				×2	56	—	—	dB
				×4	56	—	—	dB
				×8	50	—	—	dB
			F7	×1	44	—	—	dB
				×2	44	—	—	dB
				×4	44	—	—	dB
				×8	38	—	—	dB
Input impedance	—	—		×1	1000	—	—	kΩ
				×2	500	—	—	kΩ
				×4	250	—	—	kΩ
				×8	125	—	—	kΩ

Note 1. Effective Number of Bits.

Note 2. Signal-to-Noise and Distortion Ratio.

Table 1.65 Delta-Sigma A/D Converter Characteristics (High impedance mode) (Offset error)

Item	Symbol	Conditions			Value			Unit
		Calibration	Input	Gain	Min.	Typ.	Max.	
Offset error*1	OSE	w/o calibration	differential	×1	−25.0	—	+25.0	mV
				×2	−12.5	—	+12.5	mV
				×4	−10.0	—	+10.0	mV
				×8	−10.0	—	+10.0	mV
			single-ended	×1	−25.0	—	+25.0	mV
				×2	−12.5	—	+12.5	mV
				×4	−10.0	—	+10.0	mV
				×8	−10.0	—	+10.0	mV
		w/ calibration*2	differential	×1	−5.0	—	+5.0	mV
				×2	−5.0	—	+5.0	mV
				×4	−5.0	—	+5.0	mV
				×8	−5.0	—	+5.0	mV
			single-ended	×1	−5.0	—	+5.0	mV
				×2	−5.0	—	+5.0	mV
				×4	−5.0	—	+5.0	mV
				×8	−5.0	—	+5.0	mV

Note 1. Quantization error is not included.

Note 2. Temperature change after calibration is less than 50°C. (−50°C < Temperature change < +50°C).

Table 1.66 Delta-Sigma A/D Converter Characteristics (Gain error)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Gain error*1,*2,*3	GE	DC input w/o calibration	−1.0	—	+1.0	%
		DC input w/ calibration*4	−0.1	—	+0.1	%

Note 1. The gain error of F1a, F1b, F2, F3a, F3b or F4 specified in this table are the gain error of A/D conversion result corrected by software processing or by DFE.
For correcting method, refer to *Section 35.6.10, A/D Conversion Result Error Correction Processing* of *Section 35, Delta-Sigma Analog to Digital Converter (DSADC)*.

Note 2. Excluding the influence of external input resistors.

Note 3. Quantization error is not included.

Note 4. Temperature change after calibration is less than 50°C. (−50°C < Temperature change < +50°C).

Table 1.67 Delta-Sigma A/D Converter Post Filter Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Passband bandwidth	BW	Fs = 100 ksps, Ripple within ±1%	—	—	30	kHz
		Fs = 200 ksps, Ripple within ±1%*1	—	—	30	kHz
		Fs = 200 ksps, Ripple within ±1%*2	—	—	60	kHz
		Fs = 400 ksps, Fc = −3dB	—	—	90	kHz
		Fs = 800 ksps, Fc = −3dB	—	—	100	kHz
		Fs = 1600 ksps, Fc = −3dB	—	—	200	kHz
Initial delay	—	Fs = 100/200 ksps, BW = 30 kHz	—	—	65	μs
		Fs = 200 ksps, BW = 60 kHz	—	—	65	μs
		Fs = 400 ksps	—	—	8.75	μs
		Fs = 800 ksps	—	—	7.5	μs
		Fs = 1600 ksps	—	—	3.75	μs
Group delay	—	Fs = 100/200 ksps, BW = 30 kHz, Min. phase (Fin < 10 kHz)	—	—	15	μs
		Fs = 200 ksps, BW = 60 kHz, Min. phase (Fin < 10 kHz)	—	—	10	μs
		Fs = 100/200 ksps, BW = 30 kHz, Linear phase	—	—	32	μs
		Fs = 200 ksps, BW = 60 kHz, Linear phase	—	—	32	μs
		Fs = 400 ksps, Linear phase	—	—	4.5	μs
		Fs = 800 ksps, Linear phase	—	—	3.88	μs
		Fs = 1600 ksps, Linear phase	—	—	2.025	μs

Note 1. Filter type is 2nd Stage Use Case 2(F1b). Refer to *Section 35.6.2, Filter Type Setting* of *Section 35, Delta-Sigma Analog to Digital Converter (DSADC)*.

Note 2. Filter type is 2nd Stage Use Case 3(F2). Refer to *Section 35.6.2, Filter Type Setting* of *Section 35, Delta-Sigma Analog to Digital Converter (DSADC)*.

Table 1.68 Delta-Sigma A/D Converter Analog Input Voltage Range Specifications

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Reference
Input voltage specification with a single-ended reference of ADSVREFH/2	Vain	Gain = ×1	ADSVREFL	—	ADSVREFH	V	
		Gain = ×2	ADSVREFL	—	ADSVREFH	V	
		Gain = ×4	ADSVREFH × (1/4)	—	ADSVREFH × (3/4)	V	
		Gain = ×8	ADSVREFH × (3/8)	—	ADSVREFH × (5/8)	V	
Input voltage specification with a single-ended reference of ADSVREFL	Vain	Gain = ×1	ADSVREFL	—	ADSVREFH	V	
		Gain = ×2	ADSVREFL	—	ADSVREFH × (1/2)	V	
		Gain = ×4	ADSVREFL	—	ADSVREFH × (1/4)	V	
		Gain = ×8	ADSVREFL	—	ADSVREFH × (1/8)	V	
Input voltage specification with differential input*1	Vain	Gain = ×1	−ADSVREFH	—	ADSVREFH	V	
		Gain = ×2	−ADSVREFH × (1/2)	—	ADSVREFH × (1/2)	V	
		Gain = ×4	−ADSVREFH × (1/4)	—	ADSVREFH × (1/4)	V	
		Gain = ×8	−ADSVREFH × (1/8)	—	ADSVREFH × (1/8)	V	

Note 1. These indicates a difference voltage of the P side input voltage and N side input voltage (P side input voltage - N side input voltage). The respective input voltage range are ADSVREFL to ADSVREFH.

1.4.3 Cyclic A/D Converter Characteristics

Table 1.69 Cyclic A/D Converter Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
ENOB*1	ENOB	differential, w/ averaging, Fs = 1000 ksps (Fin ≤ 10 kHz)	12*3	—	—	bit
		single-ended, w/ averaging, Fs = 1000 ksps (Fin ≤ 10 kHz)	11*3	—	—	bit
SNDR*2	SNDR	differential, w/ averaging, Fs = 1000 ksps (Fin ≤ 10 kHz)	74*3	—	—	dB
		single-ended, w/ averaging, Fs = 1000 ksps (Fin ≤ 10 kHz)	68*3	—	—	dB
Input impedance	—	Fs = 1000 ksps, w/ averaging	100	—	—	kΩ
Offset error*5	OSE	Fs = 1000 ksps, w/ averaging	−5.0*3	—	+5.0*3	mV
Gain error*4,*5	GE	Fs = 1000 ksps, w/ averaging, DC input	−1.0*3	—	+1.0*3	%
Passband bandwidth	BW	Fs = 1000 ksps, w/ averaging, Fc = −3dB	—	—	500	kHz
Initial delay	—	Fs = 1000 ksps, w/ averaging	—	—	25.0	μs
Group delay	—	Fs = 1000 ksps, w/ averaging, Linear phase	—	—	1.25	μs

Note 1. Effective Number of Bits.

Note 2. Signal-to-Noise and Distortion Ratio.

Note 3. These characteristics values are after calibration.

Note 4. Excluding the influence of external input resistors.

Note 5. Quantization error is not included.

Table 1.70 Cyclic A/D Converter Analog Input Voltage Range Specifications

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Reference
Input voltage specification with a single-ended reference of ADSVREFH/2	Vain		ADSVREFL	—	ADSVREFH	V	
Input voltage specification with a single-ended reference of ADSVREFL	Vain		ADSVREFL	—	ADSVREFH	V	
Input voltage specification with differential input*1	Vain		−ADSVREFH	—	ADSVREFH	V	

Note 1. These indicates a difference voltage of the P side input voltage and N side input voltage (P side input voltage - N side input voltage). The respective input voltage range are ADSVREFL to ADSVREFH.

1.4.4 Shared Analog and Digital Input Characteristics

Table 1.71 Digital Input Timing in Analog Input Pins

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Reference
ANDI*1 rising time	t_{ANDIr}	10 to 90%	1000	—	—	ns	
ANDI*1 falling time	t_{ANDIf}	90 to 10%	1000	—	—	ns	

Note 1. ANDI means digital input (general input or SENT input) in analog input pins.

CAUTION

When this regulation isn’t maintained, A/D accuracy may be degraded.

1.5 Code Flash Characteristics

This subsection explains the electrical characteristics when the hardware interface is used with the serial programming.

Note that these electrical characteristics differ from those of when the self-programming is used.

When executing self-programming, see *the RH850/E2x Flash Memory User's Manual: Hardware Interface* which this product targets.

Table 1.72 Code Flash Basic Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Programming endurance*1	CWRT	Retained for 20 years*2	1000	—	—	Times
Temperature range of programming	TPRG	Tj	−40	—	+150	°C
Temperature range of reading	TREAD	Tj	−40	—	+150	°C

Note 1. Programming endurance is defined as the number of times each block is erased. Where programming endurance is n times (n = 1000 in this case), each block is erasable n times. For example, given a memory device that has 64-Kbyte erasure blocks, programming in the address range of each 512-byte programming block (128 programming operations, one for each block) in an erasure block and then erasing the block counts as one time in terms of programming endurance. However, programming of a given address range more than once after erasure is not possible (overwriting after programming is prohibited).

Note 2. This is the case when the average Ta is 85°C. This retained period is from when the erasure of the code flash memory has been normally completed.

Table 1.73 Code Flash Programming Characteristics

Item	Condition	Block Size	Min.	Typ.	Max.	Unit
Programming time	Programming endurance < 100 times	512 B	—	0.4*1	6*1	ms
		64 KB	—	80	360	ms
	Programming endurance ≥ 100 times	512 B	—	0.5*1	7.2*1	ms
		64 KB	—	96	432	ms
Erasing time	Programming endurance < 100 times	16 KB	—	39	120	ms
		64 KB	—	141	480	ms
	Programming endurance ≥ 100 times	16 KB	—	47	144	ms
		64 KB	—	169	576	ms

Note 1. Values are only for processing by hardware. Software overhead is not taken into account.

1.6 Data Flash Characteristics

This subsection explains the electrical characteristics when the hardware interface is used with the serial programming.

Note that these electrical characteristics differ from those of when the self-programming is used.

When executing self-programming, see *the RH850/E2x Flash Memory User's Manual: Hardware Interface* which this product targets.

Table 1.74 Data Flash Basic Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Programming endurance*1	CWRT	Retained for 20 years*2	125000	—	—	Times
(Data area)		Retained for 3 years*2	250000	—	—	Times
Temperature range of programming	TPRG	Tj	−40	—	+150	°C
Temperature range of reading	TREAD	Tj	−40	—	+150	°C

Note 1. Programming endurance is defined as the number of times each block is erased. Where programming endurance is n times (n = 125000 in this case), each block is erasable n times. For example, given a memory device that has 64-byte erasure blocks, programming in the address range of each 4-byte programming block (16 programming operations, one for each block) in an erasure block and then erasing the block counts as one time in terms of programming endurance. However, programming of a given address range more than once after erasure is not possible (overwriting after programming is prohibited).

Note 2. This is the case when the average Ta is 85°C. This retained period is from when the erasure of the data flash memory has been normally completed.

Table 1.75 Data Flash Programming Characteristics

Item	Block Size	Min.	Typ.	Max.	Unit
Programming time	4 B	—	0.16*1	1.7*1	ms
	64 B	—	2.6*1	13*1	ms
Erasing time	64 B	—	1.7*1	10*1	ms
Setting of Security Settings	4 B / 32 B*2	—	33*1	273*1	ms
Setting of Configuration Settings	4 B	—	16*1	124*1	ms
Setting of Block Protection	4 B	—	16*1	124*1	ms

Note 1. Values are only for processing by hardware. Software overhead is not taken into account.

Note 2. When the ID storage address at the Security Setting area is configured, the block size becomes a 32 B unit.

1.7 Temperature Sensor Characteristics

Table 1.76 Temperature Sensor (OTS) Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Temperature range	TTS1	—	−36	—	+148	°C
Temperature accuracy*1	ACCTS1	(−36°C to 140°C)	−4	—	+4	°C
	ACCTS2	(140°C to 148°C)	−2	—	+2	°C
Temperature update period	t_{TSUP}	—	10	—	—	ms
Stand-by return time	t_{TSSB1}	—	—	—	200	μs

Note 1. It does not include accuracy of measuring equipment.

1.8 Thermal Characteristics

1.8.1 Thermal Characteristics Parameter

Table 1.77 Thermal Characteristics in RH850/E2M

Package	Parameter	Estimate	Unit	Remark
P-FBGA373-21x21-0.80 (with vias on the board)	θja	13.8	°C / W	JESD51-9 compliant (4 layers)
	θjb	8.4	°C / W	JESD51-9 compliant (4 layers)
	θjc	5.8	°C / W	JESD51-9 compliant (4 layers)
	θjcbot	5.3	°C / W	JESD51-9 compliant (4 layers)
	Ψjb	8.0	°C / W	JESD51-9 compliant (4 layers)
	Ψjt	0.14	°C / W	JESD51-9 compliant (4 layers)
	4Lθja	16.3	°C / W	L board (4 layers)
	4Lθjb	9.9	°C / W	L board (4 layers)
	4LΨjb	8.1	°C / W	L board (4 layers)
	4LΨjmb	4.4	°C / W	L board (4 layers)
	4LΨjt	0.17	°C / W	L board (4 layers)
	4LTb_inc	8.3	°C / W	L board (4 layers)
P-FBGA292-17x17-0.80 (with vias on the board)	θja	13.2	°C / W	JESD51-9 compliant (4 layers)
	θjb	7.1	°C / W	JESD51-9 compliant (4 layers)
	θjc	5.5	°C / W	JESD51-9 compliant (4 layers)
	θjcbot	4.8	°C / W	JESD51-9 compliant (4 layers)
	Ψjb	6.8	°C / W	JESD51-9 compliant (4 layers)
	Ψjt	0.14	°C / W	JESD51-9 compliant (4 layers)
	4Lθja	15.9	°C / W	L board (4 layers)
	4Lθjb	8.4	°C / W	L board (4 layers)
	4LΨjb	7.9	°C / W	L board (4 layers)
	4LΨjmb	4.2	°C / W	L board (4 layers)
	4LΨjt	0.17	°C / W	L board (4 layers)
	4LTb_inc	8.0	°C / W	L board (4 layers)

1.8.2 Assumed Board

Table 1.78 JESD51-9 Compliant Board (4 layers)

	Board Size (mm)		Area (mm^2)
	X	Y	
Board Size	101.5	114.5	11621.75
Remaining copper rate		Conductor thickness	
50 – 95 – 95 – 50 %		70 – 35 – 35 – 70 µm	

Table 1.79 L board (4 layers)

	Board Size (mm)		Area (mm^2)
	X	Y	
Board Size	90	160	14400
Remaining copper rate		Conductor thickness	
30 – 80 – 80 – 30 %		35 – 35 – 35 – 35 µm	

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Electrical Characteristics

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