User's Manual

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RH850/D1x

Flash Memory

User's Manual: Hardware Interface

Renesas microcontroller

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Notes for CMOS devices

(1) Voltage application wafeform at input pin:

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) Handling of unused input pins:

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) Precaution against ESD:

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) Status before initialization:

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) Power ON/OFF sequence:

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) Input of signal during power off state:

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

Table of Contents

Section 1 Features

The features of the flash memory are described below. See the user's manual for information on the capacity, block configuration, and addresses of the flash memory in a given product.

Flash Memory Programming/Erasure

A dedicated sequencer for the flash memory (flash sequencer) executes programming and erasure via the P-Bus. Directly controlling the flash sequencer can provide better response and performance during self-programming than using the self-programming library (code flash and data flash). The flash sequencer also supports the program/processing suspend/resume and BGO (background operation)*1.

Note 1. This can be used during overwriting of the data flash memory and reading of the code flash memory.

Security Functions

The flash memory incorporates hardware functions to prevent illicit tampering.

Protection Functions

The flash memory incorporates hardware functions to prevent erroneous writing.

Interrupts

The flash memory supports an interrupt to indicate completion of processing by the flash sequencer and an error interrupt to indicate erroneous operations.

DMA

The flash memory supports DMA writing to the data flash memory.

Section 2 Module Configuration

Modules related to the flash memory are configured as shown in **Figure 2.1**. The flash sequencer is configured of the FCU and FACI. The FCU executes basic control of overwriting of the flash memory. The FCURAM/ROM is the storage of firmware to control execution by the FCU. The FACI receives FACI commands via the P-Bus and controls FCU operations accordingly.

In the transfer operations in response to a reset, the FACI transfers the data from flash memory to the option byte storage registers in the ID control section (FACI reset transfer). The ID control section compares the ID transferred from the flash memory with the value in the SELFID0 to SELFID3 registers. Data set in the option bytes of the flash memory can be read out from the option byte storage registers via the P-Bus.

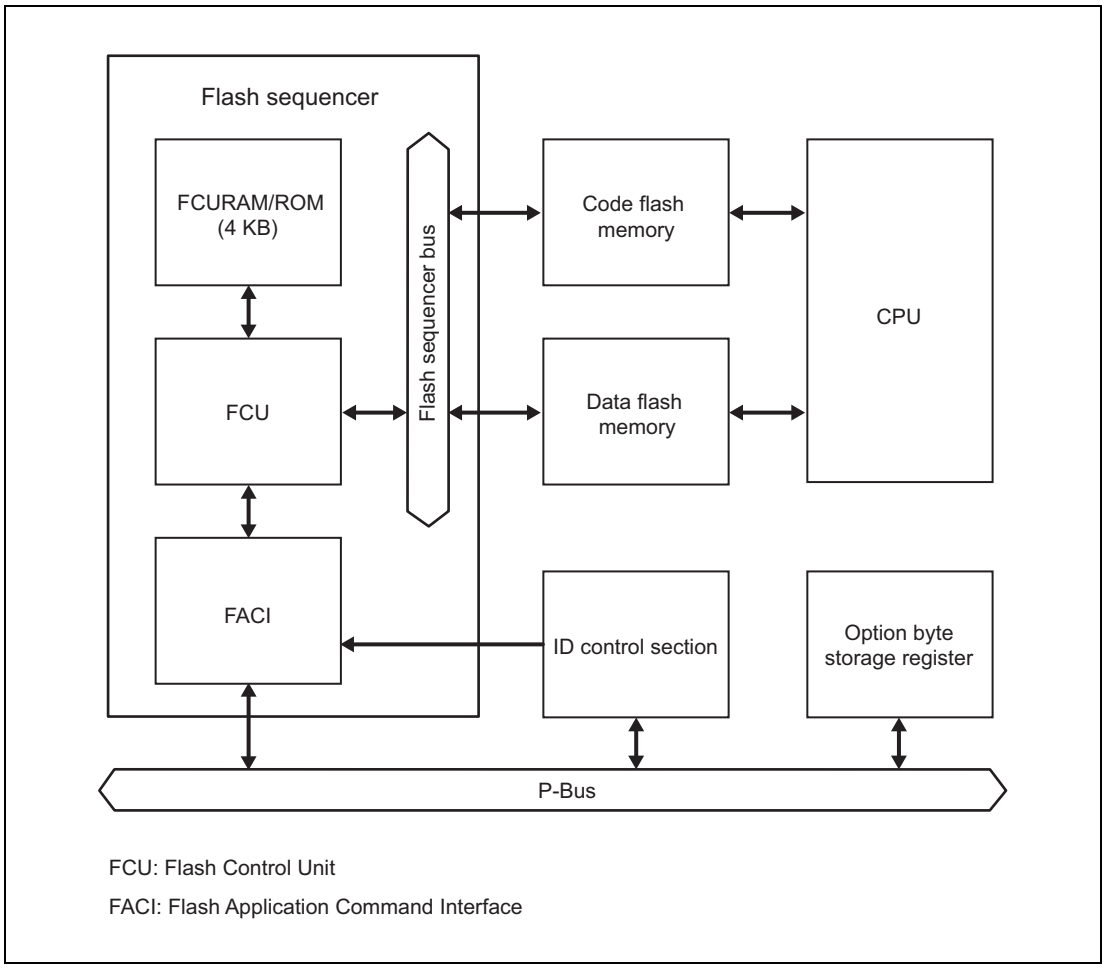


Figure 2.1 Configuration of Flash Memory Related Modules

FCURAM/ROM implementeation is different at device type.

FCU firmware is implemented in FCUROM. Therefore, FCUROM devices don't need to transfer FCU firmware to this memory. Meanwhile, write operation in FCUROM device does not affect its behavior, for the written data is ignored and error is not generated.

FCURAM devices: D1L1, D1L2 (H), D1M1 (H), D1M2 (H)

FCUROM devices: D1M1A, D1M1-V2

Section 3 Address Map

Using the hardware interface with the flash memory requires access to an address space consisting of more addresses than when the self-programming library is used. Specifically, access to the following additional areas is required: the area containing all registers of the hardware, the area for issuing of the FACI commands, the FCURAM area, the area for storage of the FCU firmware, the area for configuration settings, and the area for OTP settings. When reading the areas where the FCU firmware is stored, for configuration settings, and for OTP settings, set the FCUFSEL bit in the FCUFAREA register to 1. **Table 3.1** gives information on all of these areas.

Table 3.1 Information on the Hardware Interface Area

Area	Address	Capacity	PBUS Group	Module*2
Registers described in **Section 4.1** to **Section 4.28**	See **Section 4, Registers**	—	PBUS0	FACI
Register described in **Section 4.29**	See **Section 4, Registers**	—	PBUS0	SYSCTRL
Registers described in **Section 4.30**, **Section 4.31**	See **Section 4, Registers**	—	PBUS5	SELF
FACI command-issuing area	FFA2 0000_H	4 bytes	PBUS0	FACI command-issuing area
FCU firmware	0001 7000_H to 0001 $7FFF_H$	4 Kbytes	—	—
FCURAM/ROM area*1	FFA1 2000_H to FFA1 $2FFF_H$	4 Kbytes	PBUS0	FCURAM area
Configuration setting area	FF30 0040_H to FF30 $008F_H$	80 bytes	PBUS0	Data Flash
OTP setting area	FF38 0040_H to FF38 $009F_H$	96 bytes	PBUS0	Data Flash

Note 1. This area is read only in FCUROM devices.

Note 2. For PBUS guard channel information, see *the Table 14.17 PBUS structure* of *Section 14.5 PBUS structure* in *the User's Manual*.

See the user's manual for information on the addresses of the flash memory etc., and on the areas that are also accessed when the self-programming library is used.

Section 4 Registers

Using the hardware interface with the flash memory requires access to more registers than using the self-programming library. This section gives information on the additional registers to which access is required. For registers that are not specifically mentioned, only reset them to their initial states.

For information on the registers that are accessed when the self-programming library is used, including option byte storage registers, see the user's manual of each product.

4.1 Flash Pin Monitor Register (FPMON)

FPMON indicates the state of the FLMD0 pin.

Access: This register can only be read in 8-bit units.

Address: FFA1 0000_H

Value after reset: The value varies depending on the status of the FLMD0 pin.

Bit	7	6	5	4	3	2	1	0
	FWE	—	—	—	—	—	—	—
Value after reset	0/1	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Table 4.1 FPMON Register Contents

Bit Position	Bit Name	Function
7	FWE	Flash Write Enable Monitors the level on the FLMD0 pin. The value of the FWE bit indicates whether transitions to the code flash programming/erasure mode are enabled or disabled. 0: Transitions to the code flash program/erasure mode are disabled. 1: Transitions to the code flash program/erasure mode are enabled.
6 to 0	Reserved	When read, the value after reset is read.

4.2 Flash Access Status Register (FASTAT)

FASTAT indicates access error status for code/data flash. If either of CFAE/CMDLK/DFAE bits in FASTAT is set to 1, flash sequencer enters “Command Lock” state. To cancel “Command Lock” state, set the CFAE and DFAE bits in the FASTAT register to 0, and then issue a “Status Clear” or a “Forced Stop” command to FACI.

Access: This register can be read/written in 8-bit units.

Address: FFA1 0010$_H$

Value after reset: 00$_H$

Bit	7	6	5	4	3	2	1	0
	CFAE	—	—	CMDLK	DFAE	—	—	ECRCT
Value after reset	0	0	0	0	0	0	0	0
R/W	R/W*1	R	R	R	R/W*1	R	R	R

Note 1. Only “0” can be written to clear flag after “1” is read.

Table 4.2 FASTAT Register Contents (1/2)

Bit Position	Bit Name	Function
7	CFAE	Code Flash Access Error Indicates whether or not code flash access error has been generated. If this bit becomes “1”, ILGLERR bit in FSTATR is set to “1” and flash sequencer enters “Command Lock” state. 0: No code flash access error has occurred. 1: Code flash access error has occurred. [Setting Condition] • An FACI command has been issued when the setting of bits 23 to 0 in FSADDR is outside the range of valid addresses*2 in code flash P/E mode. [Clearing Condition] • “0” is written after reading “1” from this bit.
6, 5	Reserved	When read, the value after reset is read. When writing, write the value after reset.
4	CMDLK	Command Lock Indicates whether flash sequencer is in “Command Lock” state. 0: Flash sequencer is not in “Command Lock” state. 1: Flash sequencer is in “Command Lock” state. [Setting Condition] • FACI detects error and enters “Command Lock” state. [Clearing Condition] • The flash sequencer starts processing of the status clear or forced stop command while the CFAE and DFAE bits in the FASTAT register are set to 0.
3	DFAE	Data Flash Access Error Indicates whether or not data flash access error has been generated. If this bit becomes “1”, ILGLERR bit in FSTATR is set to “1” and flash sequencer enters “Command Lock” state. 0: No data flash access error has occurred. 1: Data flash access error has occurred. [Setting Condition] • An FACI command has been issued when the setting of bits 18 to 0 in FSADDR is outside the range of valid addresses*2 in data flash P/E mode. [Clearing Condition] “0” is written after reading “1” from this bit.
2, 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.

Table 4.2 FASTAT Register Contents (2/2)

Bit Position	Bit Name	Function
0	ECRCT	Error Correction Indicates that a 1-bit error has been corrected when the flash sequencer reads the flash memory (configuration setting, overwrite parameters, and OTP setting) or the FCURAM. This error is not generated in FCUROM devices. 0: 1-bit error has not been corrected. 1: 1-bit error has been corrected. [Clearing conditions] • The flash sequencer starts the “Status Clear” or “Forced Stop” command processing when bits CFGCRCT, TBLCRCT, and OTPCRCT in FSTATR are 1. • The flash sequencer starts the “Forced Stop” command processing when the FRCRCT bit in FSTATR is 1.

Note 2. For the range of valid addresses when issuing an FACI command, see **Section 4.5, FACI Command Start Address Register (FSADDR)** and **Section 4.6, FACI Command End Address Register (FEADDR)**.

4.3 Flash Access Error Interrupt Enable Register (FAEINT)

FAEINT enables or disables output of flash access error (“FLERR”) interrupt.

Flash access error interrupt is handled as an interrupt source of INTC and an error source of ECM with this product.

Access: This register can be read/written in 8-bit units.

Address: FFA1 0014$_H$

Value after reset: 99$_H$

Bit	7	6	5	4	3	2	1	0
	CFAEIE	—	—	CMDLKIE	DFAEIE	—	—	ECRCTIE
Value after reset	1	0	0	1	1	0	0	1
R/W	R/W	R	R	R/W	R/W	R	R	R/W

Table 4.3 FAEINT Register Contents

Bit Position	Bit Name	Function
7	CFAEIE	Code Flash Access Error Interrupt Enable Enables or disables “FLERR” interrupt request when code flash access error occurs and CFAE bit in FASTAT becomes “1”. 0: Does not generate “FLERR” interrupt request when CFAE = “1”. 1: Generates “FLERR” interrupt request when CFAE = “1”.
6, 5	Reserved	When read, the value after reset is read. When writing, write the value after reset.
4	CMDLKIE	Command Lock Interrupt Enable Enables or disables “FLERR” interrupt request when flash sequencer enters “Command Lock” state and CMDLK bit in FASTAT becomes “1”. 0: Does not generate “FLERR” interrupt request when CMDLK = “1”. 1: Generates “FLERR” interrupt request when CMDLK = “1”.
3	DFAEIE	Data Flash Access Error Interrupt Enable Enables or disables “FLERR” interrupt request when data flash access error occurs and DFAE bit in FASTAT becomes “1”. 0: Does not generate “FLERR” interrupt request when DFAE = “1”. 1: Generates “FLERR” interrupt request when DFAE = “1”.
2, 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	ECRCTIE	Error Correction Interrupt Enable Enables or disables the “FLERR” interrupt request when a 1-bit error has been corrected and the ECRCT bit in FASTAT has been set to 1 on the flash memory read (configuration setting, overwrite parameters, and OTP setting) or the FCURAM read by the flash sequencer. This interrupt is not generated in FCUROM devices. 0: Does not generate the “FLERR” interrupt request when ECRCT = 1. 1: Generates the “FLERR” interrupt request when ECRCT = 1.

4.4 Code Flash Memory Area Select Register (FAREASELC)

FAREASELC selects the code flash memory area as the target for handling of commands by the FACI.

When the SUINIT bit in the FSUINITR register is set to 1, FAREASELC is initialized. This register is also initialized by a reset.

Access: This register can be read/written in 16-bit units.

Address: FFA1 0020_H

Value after reset: 0000_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								—	—	—	—	—	—	CFAS	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R	R	R	R	R	R/W *2,*3	R

Note 1. Written data is not stored in this bit. This bit is always read as 00_H.

Note 2. This bit can be written when the FRDY bit in the FSTATR register is “1”. Writing to this bit while the FRDY bit is “0” is ignored.

Note 3. Writing to this bit is enabled only when $3B_H$ is written to the KEY[7:0] bits.

Table 4.4 FAREASELC Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits enable or disable CFAS bit modification.
7 to 2	Reserved	When read, the value after reset is read. When writing, write the value after reset.
1	CFAS	Code Flash Memory Area Select Selects the area of code flash memory that is to be the target for handling of commands by the FACI. 0: User area is selected 1: Extended user area is selected.
0	Reserved	When read, the value after reset is read. When writing, write the value after reset.

4.5 FACI Command Start Address Register (FSADDR)

FSADDR specifies the start address of the target area for command processing when the FACI command “Program”, “DMA Program”, “Block Erase”, “Blank Check”, “Config Program”, “Lock Bit Program”, “Lock Bit Read”, or “OTP Set” is issued.

FSADDR value is initialized when SUINIT bit in FSUINITR is set to “1”. It is also initialized by a reset.

Access: This register can be read/written in 32-bit units.

Address: FFA1 0030_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FSADDR[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FSADDR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R

Note 1. This bit can be written when the FRDY bit in the FSTATR register is “1”. Writing to this bit while the FRDY bits is “0” is ignored.

Table 4.5 FSADDR Register Contents

Bit Position	Bit Name	Function
31 to 0	FSADDR[31:0]	Start Address of FACI Command Processing These bits specify the start address of the FACI command processing. Bits 31 to 24 are ignored in the FACI command processing for the code flash memory. Bits 31 to 19 are ignored in the FACI command processing for the data flash memory. Lower address bits for smaller address than boundary below are also ignored. Command — Address Boundary Program (code flash memory): 256 bytes Program (data flash memory): 4-byte write: 4 bytes DMA Program: 4 bytes Block Erase (code flash memory): 8 Kbytes or 32 Kbytes Block Erase (data flash memory): 64 bytes Blank Check: 4 bytes Config Program: 16 bytes Lock Bit Program: 8 Kbytes or 32 Kbytes Lock Bit Read: 8 Kbytes or 32 Kbytes OTP Set: 16 bytes

4.6 FACI Command End Address Register (FEADDR)

This register specifies the end address in the target area in Blank Check command processing. When blank check addressing mode is set to incremental mode (i.e. FBCCNT.BCDIR = “0”), address specified in FSADDR should be smaller than or equal to address in FEADDR. Conversely, address in FSADDR should be larger than or equal to address in FEADDR when blank check addressing mode is set to decremental mode (i.e. FBCCNT.BCDIR = “1”). If setting of BCDIR, FSADDR, and FEADDR are inconsistent, FACI detects error and flash sequencer enters “Command Lock” state. (See **Section 8.3, Error Protection**.)

FEADDR value is initialized when SUINIT bit in FSUINITR is set to “1”. It is also initialized by a reset.

Access: This register can be read/written in 32-bit units.

Address: FFA1 0034$_H$

Value after reset: 0000 0000$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FEADDR[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FEADDR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R

Note 1. This bit can be written when the FRDY bit in the FSTATR register is “1”. Writing to this bit while the FRDY bits is “0” is ignored.

Table 4.6 FEADDR Register Contents

Bit Position	Bit Name	Function
31 to 0	FEADDR[31:0]	End Address of FACI Command Target Area Specifies end address of target area in “Blank Check” command. Bits 31 to 19, 1 and 0 are ignored in the command processing.

4.7 FCURAM Enable Register (FCURAME)

FCURAME enables or disables access to FCURAM area.

This register is not available in FCUROM devices.

Access: This register can be read/written in 16-bit units.

Address: FFA1 0054_H

Value after reset: 0000_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								—	—	—	—	—	—	FRAMTRAN	FCRME
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R	R	R	R	R	R/W*2	R/W*2

Note 1. Written data is not stored in this bit. This bit is always read as 00_H.

Note 2. Writing to this bit is enabled only when $C4_H$ is written to the KEY[7:0] bits.

Table 4.7 FCURAME Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits enable or disable FRAMTRAN bit and FCRME bit modification.
7 to 2	Reserved	When read, the value after reset is read. When writing, write the value after reset.
1	FRAMTRAN	FCURAM Transfer Mode Specifies the FCURAM transfer mode. 0: Normal transfer mode Both read and write accesses to FCURAM are possible. 1: High-speed write mode High-speed writing to the FCURAM is possible. However, reading from the FCURAM is not possible.
0	FCRME	FCURAM Enable Enables or disables access to the FCURAM. Before writing to the FCURAM, clear FENTRYR to 0000_H to stop the flash sequencer. 0: Disables access to FCURAM. 1: Enables access to FCURAM.

4.8 Flash Status Register (FSTATR)

FSTATR indicates flash sequencer status.

Access: This register can only be read in 8-, 16-, or 32-bit units.

Address: FFA1 0080_H

Value after reset: $0000\ 8000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	EBFULL	OTPDTCT	OTPCRCT
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRDY	ILGLERR	ERSERR	PRGERR	SUSRDY	DBFULL	ERSSPD	PRGSPD	—	—	CFGDTCT	CFGCRCT	TBLDTCT	TBLCRCT	FRDTCT	FRCRCT
Value after reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.8 FSTATR Register Contents (1/5)

Bit Position	Bit Name	Function
31 to 19	Reserved	When read, the value after reset is read.
18	EBFULL	FDMYECC Buffer Full Indicates the ECC buffer status when issuing “Program”. The FACI incorporates a buffer for ECC bit (ECC buffer). While the ECCDISE bit in FECCTMD is 1, FDMYECC can be used as the ECC buffer. When FDMYECC is written to while the EBFULL bit is 1, the FACI inserts a wait in the P-Bus. 0: The ECC buffer is empty. 1: The ECC buffer is full. [Setting condition] • The ECC buffer becomes full while issuing “Program” command. [Clearing condition] • The ECC buffer becomes empty.
17	OTPDTCT	2-Bit Error Detection Monitor (OTP Set) Indicates that a 2-bit error has been detected on reading the OTP value. The FACI reads the OTP value in “Program”, “Block Erase”, “Lock Bit Program”, “Lock Bit Read”, and “OTP Set” for the code flash memory. When this bit is 1, the flash sequencer is in “Command Lock” state. 0: No 2-bit error has been detected. 1: A 2-bit error has been detected. [Clearing condition] • The flash sequencer starts “Status Clear” or “Forced Stop” command processing.
16	OTPCRCT	1-Bit Error Correction Monitor (OTP Set) Indicates that a 1-bit error has been corrected on reading the OTP value. The FACI reads the OTP value in “Program”, “Block Erase”, “Lock Bit Program”, “Lock Bit Read”, and “OTP Set” for the code flash memory. When this bit is 1, the flash sequencer continues the command processing and does not enter “Command Lock” state. 0: 1-bit error has not been corrected. 1: 1-bit error has been corrected. [Clearing condition] • The flash sequencer starts “Status Clear” or “Forced Stop” command processing.

Table 4.8 FSTATR Register Contents (2/5)

Bit Position	Bit Name	Function
15	FRDY	Flash Ready Indicates the processing state in flash sequencer. 0: Processing of the command “Program”, “DMA Program”, “Block Erase”, “Program/Erasure Suspend”, “Program/Erasure Resume”, “Forced Stop”, “Blank Check”, “Config Program”, “Lock Bit Program”, “Lock Bit Read”, or “OTP Set” is in progress. 1: None of the above is in progress. [Setting Conditions] • Flash sequencer completes processing. • Flash sequencer suspends processing by “Program/Erase Suspend” command. • Flash sequencer terminates processing by “Forced Stop” command. [Clearing Conditions] • When the flash sequencer accepts the FACI command • For “Program”, “DMA Program”, “Config Program”, or “OTP Set” command, after the first write access to the FACI command issuing area. • For other commands, after the last write access to the FACI command issuing area.
14	ILGLERR	Illegal Command Error Indicates that flash sequencer has detected an illegal command or illegal flash memory access. When this bit is “1”, flash sequencer is in “Command Lock” state. 0: Flash sequencer has not detected any illegal command or illegal flash memory access. 1: Flash sequencer has detected an illegal command or illegal flash memory access [Setting conditions] • Flash sequencer has detected an illegal command. • Flash sequencer has detected an illegal flash memory access. • FENTRYR setting is illegal. [Clearing condition] • “Status Clear” or “Forced Stop” command processing is started while the DFAE or CFAE bits in the FASTAT register is 0. If the flash sequencer completes processing of “Status Clear” or “Forced Stop” command while the CFAE or DFAE bit in the FASTAT register is 1, this bit is set to 1. This bit is temporarily set to 0 during processing of “Forced Stop” command, and is re-set to 1 when the CFAE or DFAE bit is detected as 1 on completion of command processing.
13	ERSERR	Erasure Error Indicates result of code or data flash erasure by flash sequencer. When this bit is “1”, flash sequencer is in “Command Lock” state. 0: Erasure processing has been completed successfully 1: An error has occurred during erasure [Setting conditions] • An error has occurred during erasure. • “Block Erase” command has been issued for the area protected by lock bit. [Clearing condition] • “Status Clear” or “Forced Stop” command processing is started.

Table 4.8 FSTATR Register Contents (3/5)

Bit Position	Bit Name	Function
12	PRGERR	Programming Error Indicates the result of code or data flash programming by flash sequencer. When this bit is “1”, flash sequencer is in “Command Lock” state. 0: Programming has been completed successfully 1: An error has occurred during programming [Setting conditions] • An error has occurred during programming. • “Program” or “Lock Bit Program” command has been issued for the area protected by lock bit. [Clearing condition] • “Status Clear” or “Forced Stop” command processing is started.
11	SUSRDY	Suspend Ready Indicates whether flash sequencer is ready to accept a “Program/Erase Suspend” command. 0: Flash sequencer cannot accept “Program/Erase Suspend” command. 1: Flash sequencer can accept “Program/Erase Suspend” command. [Setting condition] • After initiating programming or erasure, FACI entered a state where it is ready to accept “Program/Erase Suspend” command. [Clearing conditions] • FACI has accepted “Program/Erase Suspend” or “Forced Stop” command. (after the write access to the FACI command issuing area is completed) • Flash sequencer has entered “Command Lock” state during programming or erasure. • Programming/erasure processing is completed.
10	DBFULL	Data Buffer Full Indicates the data buffer status when issuing “Program”. The FACI incorporates a buffer for write data (data buffer). When issuing the flash memory write data to the FACI command issue area while the data buffer is full, the FACI inserts a wait in the P-Bus. 0: The data buffer is empty. 1: The data buffer is full. [Setting condition] • The data buffer becomes full while issuing “Program”. [Clearing condition] • The data buffer becomes empty.
9	ERSSPD	Erasure-Suspended Status Indicates that flash sequencer has entered “Erase” command suspension process or erasure-suspended status. 0: Flash sequencer is in status other than the below mentioned. 1: Flash sequencer is in erasure suspension process or erasure-suspended status. [Setting condition] • Flash sequencer has initiated “Program/Erase Suspend” command during “Erase” command processing. [Clearing conditions] • Flash sequencer has accepted “Program/Erase Resume” command. (after the write access to the FACI command issuing area is completed) • “Forced Stop” command processing is started.

Table 4.8 FSTATR Register Contents (4/5)

Bit Position	Bit Name	Function
8	PRGSPD	Programming-Suspended Status Indicates that flash sequencer has entered “Program” command suspension process or programming suspended status. 0: Flash sequencer is in status other than the below mentioned. 1: Flash sequencer is in programming suspension process or programming-suspended status. [Setting condition] • Flash sequencer has initiated “Program/Erase Suspend” command during “Program” command processing. [Clearing condition] • Flash sequencer has accepted “Program/Erase Resume” command. (after the write access to the FACI command issuing area is completed) • “Forced Stop” command processing is started.
7	Reserved	When read, the value after reset is read.
6	Reserved	When read, the value after reset is read.
5	CFGDTCT	2-Bit Error Detection Monitor (Config Program) Indicates that a 2-bit error has been detected on reading the Config Program value. The FACI reads the Config Program value in “Config Program”. When this bit is 1, the flash sequencer is in “Command Lock” state. 0: No 2-bit error has been detected. 1: A 2-bit error has been detected. [Clearing condition] • The flash sequencer starts “Status Clear” or “Forced Stop” command processing.
4	CFGCRCT	1-Bit Error Correction Monitor (Config Program) Indicates that a 1-bit error has been corrected on reading the Config Program value. The FACI reads the Config Program value in “Config Program”. When this bit is 1, the flash sequencer continues command processing and does not enter “Command Lock” state. 0: 1-bit error has not been corrected. 1: 1-bit error has been corrected. [Clearing condition] • The flash sequencer starts “Status Clear” or “Forced Stop” command processing.
3	TBLDTCT	2-Bit Error Detection Monitor (Overwrite Parameter Table) Indicates that a 2-bit error has been detected on reading the overwrite parameter table. The FACI reads the overwrite parameter table in “Program”, “DMA Program”, “Block Erase”, “Blank Check”, “Config Program”, “Lock Bit Program”, and “OTP Set” for the flash memory. When this bit is 1, the flash sequencer is in “Command Lock” state. 0: No 2-bit error has been detected. 1: A 2-bit error has been detected. [Clearing condition] • The flash sequencer starts “Status Clear” or “Forced Stop” command processing.
2	TBLCRCT	1-Bit Error Correction Monitor (Overwrite Parameter Table) Indicates that a 1-bit error has been corrected on reading the overwrite parameter table. The FACI reads the overwrite parameter table in “Program”, “DMA Program”, “Block Erase”, “Blank Check”, “Config Program”, “Lock Bit Program”, and “OTP Set” for the flash memory. When this bit is 1, the flash sequencer does not enter “Command Lock” state. 0: 1-bit error has not been corrected. 1: 1-bit error has been corrected. [Clearing condition] • The flash sequencer starts “Status Clear” or “Forced Stop” command processing.

Table 4.8 FSTATR Register Contents (5/5)

Bit Position	Bit Name	Function
1	FRDTCT	2-Bit Error Detection Monitor (FCURAM) Indicates that 2-bit error has been detected in FCURAM read by the FCU. When the FRDTCT bit is “1”, the flash sequencer enters “Command Lock” state. 0: No 2-bit error has been detected. 1: A 2-bit error has been detected. [Clearing condition] • After the flash sequencer starts “Forced Stop” command processing After “Forced Stop” command is issued and the FCU is initialized, reload the FCU firmware to the FCURAM.
0	FRCRCT	1-Bit Error Correction Monitor (FCURAM) Indicates that a 1-bit error has been corrected when the FCU reads the FCURAM. When this bit is 1, the flash sequencer does not enter “Command Lock” state. 0: 1-bit error has not been corrected. 1: 1-bit error has been corrected. [Clearing condition] • After the flash sequencer starts “Forced Stop” command processing After “Forced Stop” command is issued and the FCU is initialized, reload the FCU firmware to the FCURAM.

4.9 Flash P/E Mode Entry Register (FENTRYR)

FENTRYR specifies “Program/Erasure Mode” for code flash or data flash. To specify “Program/Erasure Mode” for code flash or data flash so that flash sequencer can accept FACI commands, set either of FENTRYD or FENTRYC bit to “1”.

Note that if this register is set to other than 0000_H, 0001_H, and 0080_H, ILGLERR bit in the FSTATR register will be set and flash sequencer will enter “Command Lock” state.

FENTRYR value is initialized when SUINIT bit in FSUINITR is set to “1”. It is also initialized by a reset.

Access: This register can be read/written in 16-bit units.

Address: FFA1 0084_H

Value after reset: 0000_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								FENTRYD	—	—	—	—	—	—	FENTRYC
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W *2,*3	R	R	R	R	R	R	R/W *2,*3, *4

Note 1. Written data is not stored in this bit. This bit is always read as 00_H.

Note 2. This bit can be written when the FRDY bit in the FSTATR register is “1”. Writing to this bit while the FRDY bits is “0” is ignored.

Note 3. Writing to this bit is enabled only when AA_H is written to the KEY[7:0] bits.

Note 4. Writing to this bit is enabled only when the FEW bit in the FPMON register is “1”.

Table 4.9 FENTRYR Register Contents (1/2)

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits enable or disable FENTRYD and FENTRYC bits modification.
7	FENTRYD	Data Flash Program/Erasure Mode Entry This bit specifies the Program/Erasure mode for data flash. 0: Data flash is in “Read Mode” 1: Data flash is in “Program/Erasure Mode” [Setting condition] • “1” is written to FENTRYD while write enabling conditions are satisfied and FENTRYR is 0000_H. [Clearing conditions] • A value other than AA_H is written to KEY[7:0] in FENTRYR while FRDY bit is “1”. • “0” is written to FENTRYD while the write enabling conditions are satisfied. • FENTRYR is written to while FENTRYR is not 0000_H and the write enabling conditions are satisfied.
6 to 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.

Table 4.9 FENTRYR Register Contents (2/2)

Bit Position	Bit Name	Function
0	FENTRYC	Code Flash Program/Erasure Mode Entry This bit specifies the Program/Erasure mode for code flash. 0: Code flash is in “Read Mode” 1: Code flash is in “Program/Erasure Mode” [Setting condition] • “1” is written to FENTRYC while write enabling conditions are satisfied and FENTRYR is 0000_H. [Clearing conditions] • A value other than AA_H is written to KEY[7:0] in FENTRYR while FRDY bit is “1”. • The FWE bit in FPMON is set to “0” while the FRDY bit is “1”. • “0” is written to FENTRYC while the write enabling conditions are satisfied. • FENTRYR is written to while FENTRYR is not 0000_H and the write enabling conditions are satisfied.

4.10 Code Flash Protect Register (FPROTR)

FPROTR enables or disables protection function through lock bits against programming and erasure. FPROTR value is initialized when SUINIT bit in FSUINITR is set to “1”. It is also initialized by a reset.

Access: This register can be read/written in 16-bit units.

Address: FFA1 0088_H

Value after reset: 0000_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								—	—	—	—	—	—	—	FPROTCN
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R	R	R	R	R	R	R/W*2

Note 1. Written data is not stored in this bit. This bit is always read as 00_H.

Note 2. Writing to this bit is enabled only when 55_H is written to the KEY[7:0] bits.

Table 4.10 FPROTR Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits enable or disable FPROTCN bit modification.
7 to 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	FPROTCN	Lock Bit Protect Cancel Enables or disables protection through lock bits against programming and erasure. 0: Enables protection through lock bits 1: Disables protection through lock bits [Setting condition] • “1” is written to FPROTCN while write enabling conditions are satisfied and FENTRYR is not 0000_H. [Clearing conditions] • A value other than 55_H is written to KEY[7:0] in FPROTR. • “0” is written to FPROTCN while the write enabling conditions are satisfied. • FENTRYR register value is 0000_H.

4.11 Flash Sequencer Set-Up Initialize Register (FSUINITR)

FSUINITR register is used for initialization of flash sequencer set-up.

Access: This register can be read/written in 16-bit units.

Address: FFA1 008C$_H$

Value after reset: 0000$_H$

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								—	—	—	—	—	—	—	SUINIT
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R	R	R	R	R	R	R/W *2,*3

Note 1. Written data is not stored in this bit. This bit is always read as 00$_H$.

Note 2. This bit can be written when the FRDY bit in the FSTATR register is “1”. Writing to this bit while the FRDY bits is “0” is ignored.

Note 3. Writing to this bit is enabled only when 2DH is written to the KEY[7:0] bits.

Table 4.11 FSUINITR Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits enable or disable SUINIT bit modification.
7 to 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	SUINIT	Set-up Initialization Initializes the flash sequencer set-up registers (FEADDR, FPROTR, FCPSR, FSADDR, FENTRYR, FBCCNT, and FAREASELC). 0: The above flash sequencer set-up registers retain their current values. 1: The above flash sequencer set-up registers are initialized.

4.12 Lock Bit Status Register (FLKSTAT)

FLKSTAT indicates lock bit status which is read through “Lock Bit Read” command execution.

Access: This register can only be read in 8-bit units.

Address: FFA1 0090_H

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	FLOCKST
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Table 4.12 FLKSTAT Register Contents

Bit Position	Bit Name	Function
7 to 1	Reserved	When read, the value after reset is read.
0	FLOCKST	Lock Bit Status Reflects the lock bit status read through “Lock Bit Read” command execution. When FRDY bit becomes “1” after “Lock Bit Read” command is issued, effective data is reflected in FLOCKST bit. This bit value is retained until next “Lock Bit Read” command is completed. 0: Protected state 1: Non-protected state

4.13 FCURAM First Error Address Register (FRFSTEADR)

FRFSTEADR indicates an address where the first ECC error has occurred on reading the FCURAM.

This register is not available in FCUROM devices.

Access: This register can only be read in 32-bit units.

Address: FFA1 0094_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	FRFSTEADR[11:0]											
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.13 FRFSTEADR Register Contents

Bit Position	Bit Name	Function
31 to 12	Reserved	When read, the value after reset is read.
11 to 0	FRFSTEADR[11:0]	FCURAM First Error Address Indicate the first ECC error address on reading the FCURAM. An address offset from the top address of the FCURAM is stored.

4.14 FACI Reset Transfer Status Register (FRTSTAT)

FRTSTAT indicates error status for the FACI reset transfer.

Access: This register can only be read in 8-bit units.

Address: FFA1 0098_H

Value after reset: The value varies depending on the status of the FLMD0 pin.

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	RTEDTCT	RTECRCT
Value after reset	0	0	0	0	0	0	0/1	0/1
R/W	R	R	R	R	R	R	R	R

Table 4.14 FRTSTAT Register Contents

Bit Position	Bit Name	Function
7 to 2	Reserved	When read, the value after reset is read.
1	RTEDTCT	FACI reset transfer error detection Indicates that a 2-bit error has been detected during the FACI reset transfer. When RTEDTCT is “1”, the flash sequencer does not enter the “Command Lock” state. 0: No 2-bit error has been detected. 1: A 2-bit error has been detected. The RTEDTCT bit is cleared when a 2-bit error is not detected during the FACI reset transfer after a reset of the microcomputer.
0	RTECRCT	FACI reset transfer error correction Indicates that a 1-bit error has been corrected during the FACI reset transfer. When RTECRCT is “1”, the flash sequencer does not enter the “Command Lock” state. 0: No 1-bit error has been corrected. 1: A 1-bit error has been corrected. The RTECRCT bit is cleared when a 1-bit error is not corrected during the FACI reset transfer after a reset of the microcomputer.

4.15 FACI Reset Transfer Error Interrupt Enable Register (FRTEINT)

FRTEINT enables or disables generation of an interrupt request of the FACI reset transfer error (FRTERR). FACI reset transfer error interrupt is handled as an error source of ECM with this product.

Access: This register can be read/written in 8-bit units.

Address: FFA1 009C$_H$

Value after reset: 03$_H$

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	RTEDIE	RTECIE
Value after reset	0	0	0	0	0	0	1	1
R/W	R	R	R	R	R	R	R/W	R/W

Table 4.15 FRTEINT Register Contents

Bit Position	Bit Name	Function
7 to 2	Reserved	When read, the value after reset is read. When writing, write the value after reset.
1	RTEDIE	FACI reset transfer error detection interrupt enable Enables or disables generation of an “FRTERR” interrupt when a 2-bit error is detected during the FACI reset transfer and the RTEDTCT bit in FRTSTAT is set to “1” 0: No FRTERR interrupt is generated when FRTSTAT.RTEDTCT = “1” 1: An FRTERR interrupt is generated when FRTSTAT.RTEDTCT = “1”
0	RTECIE	FACI reset transfer error correction interrupt enable Enables or disables generation of an “FRTERR” interrupt when a 1-bit error is corrected during the FACI reset transfer and the RTECRCT bit in FRTSTAT is set to “1” 0: No FRTERR interrupt is generated when FRTSTAT.RTECRCT = “1” 1: An FRTERR interrupt is generated when FRTSTAT.RTECRCT = “1”

4.16 FACI Command Register (FCMDR)

FCMDR stores commands that FACI has accepted.

Access: This register can only be read in 16-bit units.

Address: FFA1 00A0$_H$

Value after reset: FFFF$_H$

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMDR[7:0]								PCMDR[7:0]							
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.16 FCMDR Register Contents

Bit Position	Bit Name	Function
15 to 8	CMDR[7:0]	Command These bits store the latest command accepted by FACI.
7 to 0	PCMDR[7:0]	Previous Command These bits store previous command accepted by FACI.

Table 4.17 States of FCMDR after Acceptance of the Various Commands

Command	CMDR[7:0]	PCMDR[7:0]
Program	E8$_H$	Previous command
DMA Program	EA$_H$	Previous command
Block Erase	D0$_H$	20$_H$
Program/Erase Suspend	B0$_H$	Previous command
Program/Erase Resume	D0$_H$	Previous command
Status Clear	50$_H$	Previous command
Forced Stop	B3$_H$	Previous command
Blank Check	D0$_H$	71$_H$
Config Program	40$_H$	Previous command
Lock Bit Program	D0$_H$	77$_H$
Lock Bit Read	D0$_H$	71$_H$
OTP Set	45$_H$	Previous command

4.17 FCURAM ECC Control Register (FRAMECCR)

FRAMECCR register enables the ECC test function for FCURAM.

This register is not available in FCUROM devices.

Access: This register can be read/written in 16-bit units.

Address: FFA1 00B0$_H$

Value after reset: 0000$_H$

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY								—	—	FRECCDISE	FRECCSEL	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R	R/W*2	R/W*2	R	R	R	R

Note 1. Written data is not stored in this bit. This bit is always read as 00$_H$.

Note 2. Writing to this bit is enabled only when CC$_H$ is written to the KEY bits.

Table 4.18 FRAMECCR Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY	Key Code These bits enable or disable modification of the FRECCDISE and FRECCSEL bits.
7, 6	Reserved	When read, the value after reset is read. When writing, write the value after reset.
5	FRECCDISE	FCURAM ECC Disable Enables or disables the FCURAM error detection and correction. 0: Enables the FCURAM ECC. 1: Disables the FCURAM ECC.
4	FRECCSEL	FCURAM ECC Area Select Enables or disables the FCURAM error detection and correction. 0: Writes a coded ECC to the FCURAM. The decoded data and the ECC are read out on reading the FCURAM. 1: Performs a direct write to and read from the ECC area.
3 to 0	Reserved	When read, the value after reset is read. When writing, write the value after reset.

4.18 Flash P/E Status Register (FPESTAT)

FPESTAT indicates the result of programming or erasure to the flash memory.

Access: This register can only be read in 16-bit units.

Address: FFA1 $00C0_H$

Value after reset: 0000_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	PEERRST[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.19 FPESTAT Register Contents

Bit Position	Bit Name	Function
15 to 8	Reserved	When read, the value after reset is read.
7 to 0	PEERRST[7:0]	Program/Erasure Error Status Indicates the source of error that occurs during programming/erasure for code flash or data flash. The value of the PEERRST[7:0] bits is only valid if PRGERR or ERSERR bit value in FSTATR register is 1, while FRDY bit in FSTATR register is “1”. When ERSERR and PRGERR are “0”, the PEERRST[7:0] bits retain the value to indicate the source of error that previously occurred. 00_H: No error 01_H: A write attempt made to an area protected by the lock bits 02_H: A write error caused by other source than the above 11_H: An erase attempt made to an area protected by the lock bits 12_H: An erase error caused by other source than the above Other than above: Reserved

4.19 Data Flash Blank Check Control Register (FBCCNT)

FBCCNT specifies addressing mode in “Blank Check” command processing. FBCCNT value is initialized when SUINIT bit in FSUINITR is set to “1”. It is also initialized by a reset.

Access: This register can be read/written in 8-bit units.

Address: FFA1 00D0$_H$

Value after reset: 00$_H$

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	BCDIR
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W

Table 4.20 FBCCNT Register Contents

Bit Position	Bit Name	Function
7 to 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	BCDIR	Blank Check Direction Specifies addressing mode in blank check operation. 0: Blank check is executed from smaller address to larger address. (Incremental mode) 1: Blank check is executed from larger address to smaller address. (Decremental mode)

4.20 Data Flash Blank Check Status Register (FBCSTAT)

FBCSTAT stores check results by executing “Blank Check” command.

Access: This register can only be read in 8-bit units.

Address: FFA1 00D4$_H$

Value after reset: 00$_H$

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	BCST
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Table 4.21 FBCSTAT Register Contents

Bit Position	Bit Name	Function
7 to 1	Reserved	When read, the value after reset is read.
0	BCST	Blank Check Status Indicates the result of “Blank Check” command. 0: The target area is in the non-programmed state*1. (Nothing has been written to the area after erasure. The area is blank.) 1: The target area is filled with 0s and/or 1s.

Note 1. See **(5) Abnormal termination during program/erasure** in **Section 9, Usage Notes**.

4.21 Data Flash Programming Start Address Register (FPSADDR)

FPSADDR indicates address of the first programmed data which is found in “Blank Check” command execution.

Access: This register can only be read in 32-bit units.

Address: FFA1 00D8$_H$

Value after reset: 0000 0000$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	PSADR[18:16]		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PSADR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.22 FPSADDR Register Contents

Bit Position	Bit Name	Function
31 to 19	Reserved	When read, the value after reset is read.
18 to 0	PSADR[18:0]	Programmed Area Start Address Indicates address of the first programmed data which is found in “Blank Check” command execution. These bits stores address offset from the top address in the data flash memory. The value of the PSADR[18:0] bits is only valid if BCST bit value in FBCSTAT register is 1, while FRDY bit in FSTATR register is “1”. When BCST bit is “0”, the PSADR[18:0] bits hold the address that previously checked.

4.22 Flash Sequencer Process Switch Register (FCPSR)

FCPSR selects erasure-suspended mode. FCPSR value is initialized when SUINIT bit in FSUINITR is set to “1”. It is also initialized by a reset.

Access: This register can be read/written in 16-bit units.

Address: FFA1 00E0$_H$

Value after reset: 0000$_H$

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ESUSPMD
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Table 4.23 FCPSR Register Contents

Bit Position	Bit Name	Function
15 to 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	ESUSPMD	Erasure-Suspended Mode Selects erasure-suspended mode to be entered when “Program/Erase Suspend” command is issued while flash sequencer is erasing flash memory. ESUSPMD bit should be set before issuing “Block Erase” command. 0: Suspension-priority mode 1: Erasure-priority mode

4.23 Flash Sequencer Processing Clock Notify Register (FPCKAR)

FPCKAR specifies the operating frequency of the flash sequencer while processing an FACI command. After a reset, each product is set to its maximum operating frequency.

Access: This register can be read/written in 16-bit units.

Address: FFA1 00E4$_H$

Value after reset: Maximum operating frequency of the FACI in the given product.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								PCKA[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W *2,*3	R/W *2,*3	R/W *2,*3	R/W *2,*3	R/W *2,*3	RR/W *2,*3	R/W *2,*3	R/W *2,*3

Note 1. Written data is not stored in this bit. This bit is always read as 00$_H$.

Note 2. This bit can be written when the FRDY bit in the FSTATR register is “1”. Writing to this bit while the FRDY bits is “0” is ignored.

Note 3. Writing to this bit is enabled only when 1E$_H$ is written to the KEY[7:0] bits.

Table 4.24 FPCKAR Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits enable or disable the PCKA[7:0] bit modification.
7 to 0	PCKA[7:0]	Flash Sequencer Operating Clock Notify Specifies the operating frequency of the flash sequencer while processing an FACI command. Set the desired frequency in these bits before issuing an FACI command. Specifically, convert the frequency represented in MHz into a binary number and set it in these bits. Example: Frequency is 35.9 MHz (PCKA[7:0] = 24$_H$) Round up the first decimal place of 35.9 MHz to a whole number (= 36) and convert it into a binary number. If the value set in these bits is smaller than the operating frequency of the flash sequencer, the flash memory overwrite characteristics cannot be guaranteed. If the value set in these bits is greater than the operating frequency of the flash sequencer, the flash memory overwrite characteristics can be guaranteed with the increased FACI command processing time such as overwrite time. (The minimum FACI command processing time is available when the operating frequency of the flash sequencer is the same as the PCKA[7:0] value.) When SSCG is used, convert the center value of the operating frequency as described in the above example, and set the resulting value.

4.24 Flash Emulation Control Register (FLEMU)

FLEMU specifies error/timing emulation functions. The number of flash memory overwrite and data hold feature are not guaranteed for the chip that has been once used in the error emulation or timing emulation function.

Access: This register can be read/written in 8-bit units.

Address: FFA1 00F0$_H$

Value after reset: 00$_H$

Bit	7	6	5	4	3	2	1	0
	EMMODE	ERREMU	—	—	EMSQMD3	EMSQMD2	EMSQMD1	EMSQMD0
Value after reset	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R	R	R/W*1	R/W*1	R/W*1	R/W*1

Note 1. This bit can be written in emulation mode.

Table 4.25 FLEMU Register Contents

Bit Position	Bit Name	Function
7	EMMODE	Emulation mode Specifies the emulation mode. In the emulation mode, error emulation function or timing emulation function can be used. 0: Normal mode 1: Emulation mode
6	ERREMU	Error emulation Specifies the error emulation function. When the error emulation function is set, an error is always generated after processing of the FACI command specified for emulation. When the error emulation function is not set, the FACI command specified for emulation is completed after maximum processing time is elapsed (timing emulation function). Occurrence or non-occurrence of an error depends on the actual processing result. 0: Error emulation function is disabled. (Timing emulation function is enabled). 1: Error emulation function is enabled.
5, 4	Reserved	When read, the value after reset is read. When writing, write the value after reset.
3 to 0	EMSQMD3 to EMSQMD0	FACI Command processing for emulation Specify the FACI commands for emulation. 0$_H$: Program command for code flash memory 1$_H$: Block erase command for code flash memory 2$_H$: Program command for data flash memory 3$_H$: Block erase command for data flash memory 4$_H$: Blank check command 5$_H$: DMA program command

4.25 Flash Emulation Address Specify Register (FLEAD)

FLEAD specifies an address that generates an error during the error emulation function. FLEAD is used by the “DMA Program” and “Blank Check” commands. The number of flash memory overwrite and data hold feature are not guaranteed for the chip that has been once used in the error emulation or timing emulation function.

Access: This register can be read/written in 32-bit units.

Address: FFA1 00F4$_H$

Value after reset: 0000 0000$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FLAPE[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FLAPE[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R

Note 1. This bit can be written in emulation mode.

Table 4.26 FLEAD Register Contents

Bit Position	Bit Name	Function
31 to 0	FLAPE[31:0]	Emulation address Specify an address that generates an error during error emulation of the “DMA Program” and “Blank Check” commands. The settings in the bits 31 to 19 are ignored.

4.26 Flash ECC Encoder Monitor Register (FECCEMON)

FECCEMON monitors the outputs from the ECC encoder.

Access: This register can only be read in 16-bit units.

Address: FFA1 0100_H

Value after reset: $FFFF_H$

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	FECCM08	FECCM07	FECCM06	FECCM05	FECCM04	FECCM03	FECCM02	FECCM01	FECCM00
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.27 FECCEMON Register Contents

Bit Position	Bit Name	Function
15 to 9	Reserved	When read, the value after reset is read.
8 to 0	FECCM08 to FECCM00	ECC Monitor Indicates the ECC encoder output. • In code flash program/erasure mode The FECCM08 to FECCM00 bits indicate the ECC encoder output for the code flash memory. • In data flash program/erasure mode The FECCM08 and FECCM07 bits are fixed to 1. The FECCM06 to FECCM00 bits indicate the ECC encoder output for the data flash memory.

4.27 Flash ECC Test Mode Register (FECCTMD)

FECCTMD sets the ECC test function for the flash memory.

Access: This register can be read/written in 16-bit units.

Address: FFA1 0104_H

Value after reset: 0030_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								—	—	CECCVE	DECCVE	—	—	—	ECCDISE
Value after reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R	R/W*2	R/W*2	R	R	R	R/W*2

Note 1. Written data is not stored in this bit. This bit is always read as 00_H.

Note 2. Writing to this bit is enabled only when $A6_H$ is written to the KEY[7:0] bits.

Table 4.28 FECCTMD Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits enable or disable modification of the CECCVE, DECCVE, and ECCDISE bits.
7, 6	Reserved	When read, the value after reset is read. When writing, write the value after reset.
5	CECCVE	Code Flash Memory ECC Area Verify Enable Specifies the verify operation on overwriting the code flash memory. 0: Verifies the data area only. 1: Verifies the data area and the ECC area.
4	DECCVE	Data Flash Memory ECC Area Verify Enable Specifies the verify operation on overwriting the data flash memory. 0: Verifies the data area only. 1: Verifies the data area and the ECC area.
3 to 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	ECCDISE	ECC Encoder Disable Disables the ECC encoder. If the ECC encoder is disabled, the FDMYECC value is written to the flash memory. 0: The ECC encoder is enabled. 1: The ECC encoder is disabled.

4.28 Flash Dummy ECC Register (FDMYECC)

FDMYECC specifies the ECC value to be written into the flash memory when the ECCDISE bit in the FECCTMD register is 1. The bit functions in code flash program/erasure mode are different from those in data flash program/erasure mode as shown below.

Access: This register can be read/written in 16-bit units.

Address: FFA1 0108$_H$

Value after reset: FFFF$_H$

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DMYECC[8:0]								
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 4.29 FDMYECC Register Contents (in Code Flash Program/Erasure Mode)

Bit Position	Bit Name	Function
15 to 9	Reserved	When read, the value after reset is read. When writing, write the value after reset.
8 to 0	DMYECC[8:0]	Dummy ECC Specify the ECC value when the ECCDISE bit is 1.

Table 4.30 FDMYECC Register Contents (in Data Flash Program/Erasure Mode)

Bit Position	Bit Name	Function
15 to 9	Reserved	When read, the value after reset is read. When writing, write the value after reset.
8, 7	DMYECC[8:7]	Reserved When read, the value after reset is read. When writing, write the value after reset.
6 to 0	DMYECC[6:0]	Dummy ECC Specify the ECC value when the ECCDISE bit is 1.

4.29 FCU Firmware Area Select Register (FCUFAREA)

FCUFAREA selects the FCU firmware storage area.

Access: This register can be read/written in 8-bit units.

Address: FFC5 9008_H

Value after reset: *1

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	FCUFSEL
Value after reset	0	0	0	0	0	0	0	*1
R/W	R	R	R	R	R	R	R	R/W

Note 1. This bit is set to 1 when booted in serial programming mode, and cleared to 0 when booted in normal operating mode.

Table 4.31 FCUFAREA Register Contents

Bit Position	Bit Name	Function
7 to 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	FCUFSEL	Firmware Storage Area Select This bit switches the assigned area in 0001_7000_H to 0001_7FFF_H. In addition, when the configuration area and OTP setting area are read, the FCUFSEL bit must be set to “1”. 0: The user area is assigned to $0001\ 7000_H$ to $0001\ 7FFF_H$. 1: The firmware storage area is assigned to $0001\ 7000_H$ to $0001\ 7FFF_H$. (The portion of the Code Flash memory other than above is reserved.)

4.30 Self-Programming ID Input Registers (SELFID0 to SELFID3)

SELFID is for the input of an ID for use in authentication at the time of self-programming. The ID is authenticated by comparing the 128-bit ID that has been set in advance in a particular range of flash memory with the value in the SELFID0 to SELFID3 registers. The ID which is stored in a particular range of the flash memory can be set by the security settings with the on-board/off-board programming and the self-programming library, or by “Config Program” command for the FACI.

Access: This register can be read/written in 32-bit units.

Address: FFA0 8000_H (SELFID0)
FFA0 8004_H (SELFID1)
FFA0 8008_H (SELFID2)
FFA0 $800C_H$ (SELFID3)

Value after reset: 0000 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SELFIDn[31:16]*1															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SELFIDn[15:0]*1															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note 1. n = 0 to 3

Table 4.32 SELFID0 to SELFID3 Register Contents

Bit Position	Bit Name	Function
31 to 0	SELFIDn[31:0]	ID for Use in Authentication of Self-Programming The ID for use in authentication at the time of self-programming is input to these bits. Authentication of the ID is executed by comparing the 128-bit ID that has been set in advance in a particular range of flash memory with the value in the SELFIDn[31:0] bits. The 128-bit ID is arranged in the respective sets of SELFIDn[31:0] bits in the way listed below. ID[31:0]: SELFID0[31:0] ID[63:32]: SELFID1[31:0] ID[95:64]: SELFID2[31:0] ID[127:96]: SELFID3[31:0]

4.31 Self-Programming ID Authentication Status Register (SELFIDST)

SELFIDST indicates the result of authentication of an ID at the time of self-programming. That is, the SELFIDST register indicates the result of comparing the 128-bit ID that has been set in advance in a particular range of flash memory with the value in the SELFID0 to SELFID3 registers. The ID which is stored in a particular range of the flash memory can be set by the security settings with the on-board/ off-board programming and the self-programming library, or by “Config Program” command for the FACI.

Access: This register can only be read in 8-, 16-, or 32-bit units.

Address: FFA0 8010$_H$

Value after reset: 0000 000X$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IDST
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.33 SELFIDST Register Contents

Bit Position	Bit Name	Function
31 to 1	Reserved	When read, the value after reset is read.
0	IDST	ID Authentication Status This bit indicates the result of comparing the 128-bit ID that has been set in advance in a particular range of flash memory with the value in the SELFID0 to SELFID3 registers. 0: The IDs match (ID-based security is unlocked). 1: The IDs do not match (ID-based security is locked).

Section 5 Flash Sequencer Modes

5.1 Operating Modes of the Flash Sequencer

The flash sequencer has three operating modes as shown in **Figure 5.1**. The mode is shifted by the write to the FENTRYR register.

When the FENTRYR register is 0000_H, the flash sequencer is in read mode. In this mode, it does not accept the FACI command. The code flash memory and the data flash memory are both readable.

When the FENTRYR register is 0001_H, the flash sequencer is in code flash program/erasure mode where the code flash memory can be programmed/erased by the FACI command. In this mode, the data flash memory is not readable. In addition, the code flash memory is not readable under the condition where the BGO operation is disabled. Under the condition where the BGO operation is enabled, the code flash memory is readable. As for the condition to enable the BGO operation, refer to the user's manual for this product.

When the FENTRYR register is 0080_H, the flash sequencer is in data flash program/erasure mode where the data flash memory can be programmed/erased by the FACI command. In this mode, the data flash memory is not readable. However, the code flash memory is readable.

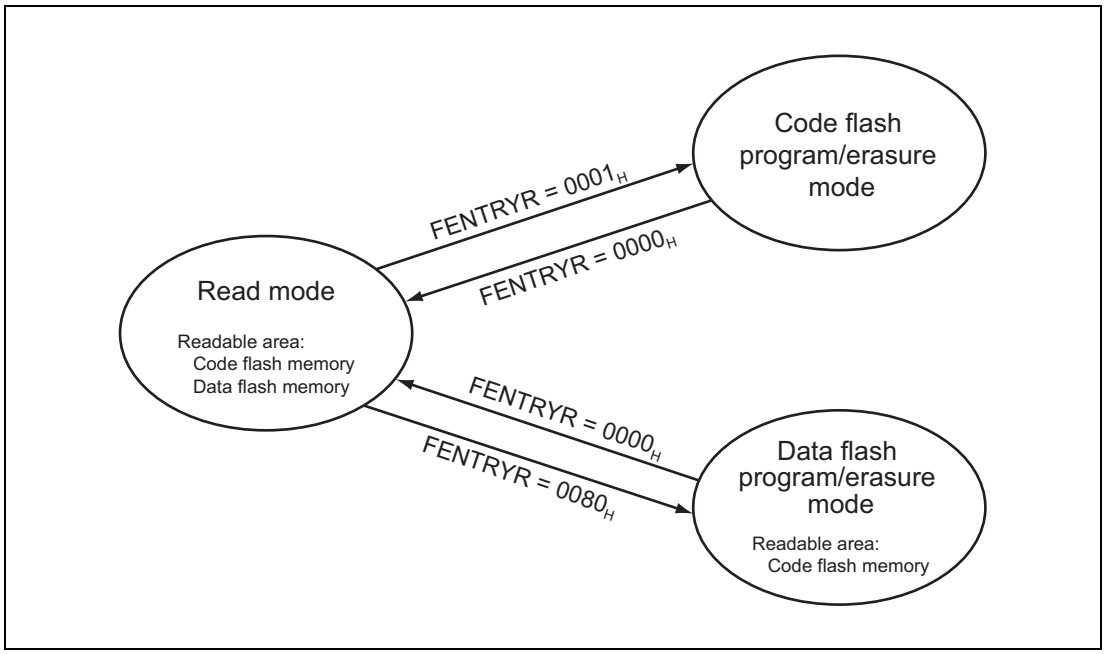


Figure 5.1 Flash Sequencer Modes

Section 6 FACI Command

6.1 List of FACI Commands

Table 6.1 List of FACI Commands

FACI Command	Function
Program	User area, extended user area, and data area can be programmed. The unit of programming is 256 bytes for user area and extended user area. The unit of programming is 4 bytes for data area.
DMA Program	Data area can be programmed by linkage with the DMA controller. The unit of programming is 4 to 64 Kbytes (specified in 4-byte units).
Block Erase	User area, extended user area, lock bit, and data area can be erased. The unit of erasing is one block.
Program/Erasure Suspend	“Program” or “Erasure” command operation can be suspended.
Program/Erasure Resume	Suspended “Program” or “Erasure” command operation can be resumed.
Status Clear	FSTATR.OTPDTCT, OTPCRCT, ILGLERR, ERSERR, PRGERR, CFGDTCT, CFGCRCT, TBLDTCT, TBLCRCT bits are initialized and flash sequencer is released from “Command Lock” state.
Forced Stop	FACI command operation can be forcibly stopped and FSTATR register is to be initialized.
Blank Check	Data area can be checked. The unit of blank checking is 4 to 64K bytes (4 bytes step).
Config Program	ID, security function, safety function, and option byte are set. The unit of programming is 16 bytes.
Lock Bit Program	The lock bit for user area and extended user area is programmed. The unit of programming is one bit (the lock bit for one block).
Lock Bit Read	The lock bit for user area and extended user area is read out and stored in the FLKSTAT register. The unit of reading is one bit (the lock bit for one block).
OTP (One Time Programming) Set	OTP is selected for the user area or extended user area. The unit of setting is 16 bytes (OTP settings for 128 blocks).

The FACI commands are issued by the write access to the FACI command issue area (see **Table 3.1**). When the write access as shown in **Table 6.2** is issued in the specified state, the flash sequencer executes the processing corresponding to each command (see **Section 6.2, Relationship between Flash Sequencer Status and FACI Commands**).

Table 6.2 Flash Sequencer Command Format

FACI Command	Number of write access	Write Data to "FACI Command Issue Area"			
		1st access	2nd access*1	3rd to (N+2)th access	(N+3)th access
Program (user area and extended user area) 256-byte programming: N = 128	131	$E8_H$	80_H (=N)	WD_1 to WD_{128}	$D0_H$
Program (data area) 4-byte programming: N = 2	N+3	$E8_H$	02_H (=N)	WD_1 to WD_N	$D0_H$
DMA Program N = 2 to 32768 (even number only)	N+2	EA_H	N	WD_1 to WD_N	—
Block Erase	2	20_H	$D0_H$	—	—
Program/Erasure Suspend	1	$B0_H$	—	—	—
Program/Erasure Resume	1	$D0_H$	—	—	—
Status Clear	1	50_H	—	—	—
Forced Stop	1	$B3_H$	—	—	—
Blank Check	2	71_H	$D0_H$	—	—
Config Program N = 8	11	40_H	08_H (=N)	WD_1 to WD_8	$D0_H$
Lock Bit Program	2	77_H	$D0_H$	—	—
Lock Bit Read	2	71_H	$D0_H$	—	—
OTP Set N = 8	11	45_H	08_H (=N)	WD_1 to WD_8	$D0_H$

Note: WD_N (N = 1, 2,…): Nth 16-bit data to be programmed.

Note 1. For a command other than the DMA program command, 8-bit data is written. For the DMA program command, 16-bit data is written.

The flash sequencer clears the FRDY bit of the FSTATR register to 0 when the processing for a command other than the status clear command is started, and sets the FRDY bit to 1 when the command processing finishes (see **Section 4.8, Flash Status Register (FSTATR)**).

If the FRDY bit changes from 0 to 1, a flash ready (FRDY) interrupt occurs.

6.2 Relationship between Flash Sequencer Status and FACI Commands

The FACI commands are accepted according to the mode/state of the flash sequencer. The FACI command should be issued after the shift of the flash sequencer to the code flash program/erasure mode or data flash program/erasure mode and checking that the flash sequencer has shifted to the mode. To check the state of flash sequencer, use the FSTATR and FASTAT registers. In addition, error occurrence can be checked by the CMDLK bit in the FASTAT register. It is the logical OR of the OTPDTCT/ ILGLERR/ERSERR/PRGERR/CFGDTCT/TBLDTCT/FRDTCT bits of the FSTATR register.

Table 6.3 summarizes available flash sequencer commands in each operating mode.

Table 6.3 Flash Sequencer Operation Mode and Available Commands

Operating Mode	FENTRYR	Available Command
Read mode	0000_H	No command is available.
Code flash program/erasure mode	0001_H	“Program” “Block Erase” “Program/Erasure Suspend” “Program/Erasure Resume” “Status Clear” “Forced Stop” “Lock Bit Program” “Lock Bit Read”
Data flash program/erasure mode	0080_H	“Program” “DMA Program” “Block Erase” “Program/Erasure Suspend” “Program/Erasure Resume” “Status Clear” “Forced Stop” “Blank Check” “Config Program” “OTP Set”

Table 6.4 shows the flash sequencer state and the acceptable FACI commands. The table assumes appropriate flash sequencer operation mode is set before issuing the command.

Table 6.4 Flash Sequencer State and Acceptable FACI Commands

	"Program" or "Erasure" command processing	"Config Program" or "OTP Set" command processing	"Program" or "Erasure" command suspension	"Blank Check" or "Lock Bit Read" command processing	"DMA Program" command processing	While suspend "Program" command	While suspend "Erasure" command	While suspend "Erasure" command,and "Program" command processing	"Command Lock" state (FRDY = 1)	"Command Lock" state (FRDY = 0)	"Lock Bit Program" command processing	"Forced Stop" command processing	Other
FRDY bit	0	0	0	0	0	1	1	0	1	0	0	0	1
SUSRDY bit	1	0	0	0	0	0	0	0	0	0	0	0	0
ERSSPD bit	0	0	0/1	0/1	0	0	1	1	0/1	0/1	0	0	0
PRGSPD bit	0	0	0/1	0/1	0	1	0	0	0/1	0/1	0	0	0
CMDLK bit	0	0	0	0	0	0	0	0	1	1	0	0	0
Program	—	—	—	—	—	—	√ *3	—	—	—	—	—	√
DMA Program	—	—	—	—	—	—	√ *1, *3	—	—	—	—	—	√ *1
Block Erase	—	—	—	—	—	—	—	—	—	—	—	—	√
Program/Erasure Suspend	√	—	—	—	—	—	—	—	X	—	—	—	X
Program/Erasure Resume	—	—	—	—	—	√	√	—	—	—	—	—	—
Status Clear	—	—	—	—	—	√	√	—	√	—	—	—	√
Forced Stop	√	√	√	√	√	√	√	√	√	√	√	√	√
Blank Check	—	—	—	—	—	√ *1	√ *1	—	—	—	—	—	√ *1
Config Program	—	—	—	—	—	—	—	—	—	—	—	—	√ *1
Lock Bit Program	—	—	—	—	—	—	—	—	—	—	—	—	√ *2
Lock Bit Read	—	—	—	—	—	√ *2	√ *2, *4	—	—	—	—	—	√ *2
OTP Set	—	—	—	—	—	—	—	—	—	—	—	—	√ *1

√: Acceptable, —: Not acceptable (due to the "Command Lock" state), X: Ignored

Note 1. Acceptable only in data flash program/erasure mode.
Note 2. Acceptable only in code flash program/erasure mode.
Note 3. Acceptable when programming area is other than erase suspending sector.
Note 4. Undefined value is read out when lock bit read command is issued to erase suspending sector.

6.3 Use FACI Command

This section describes the overview of FACI command usage.

6.3.1 Overview of the Command Usage in Code Flash P/E Mode

The overview of the FACI command usage in code flash program/erasure mode is shown below. **Table 6.3** lists the available commands in code flash program/erasure mode. Note that security should be released by ID authentication before FACI commands are used for code flash memory.

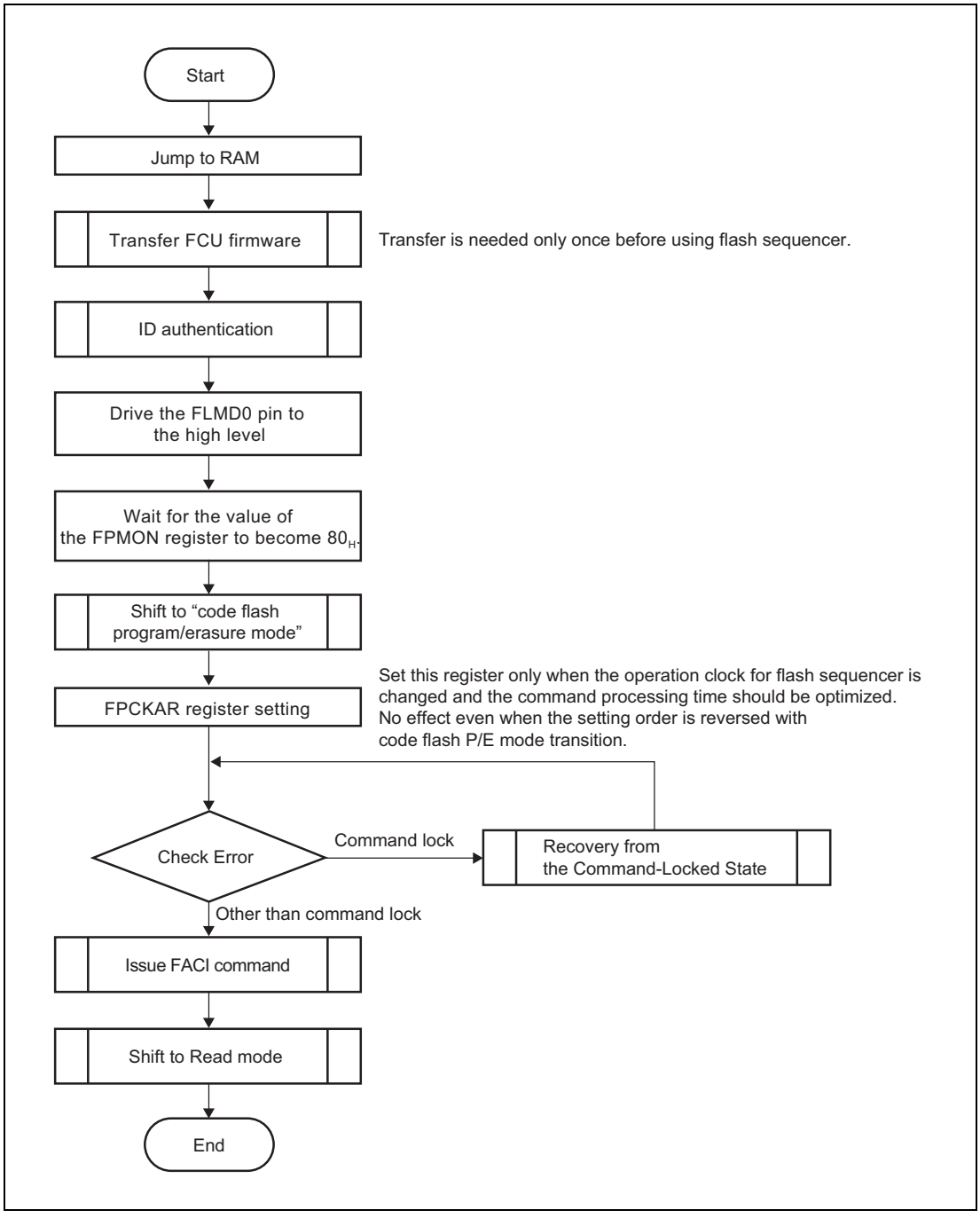


Figure 6.1 Overview of Command Usage in Code Flash Program/Erasure Mode

6.3.2 Overview of the Command Usage in Data Flash P/E Mode

The overview of the FACI command usage in data flash program/erasure mode is shown below. As for the available commands in data flash program/erasure mode, refer to **Table 6.3**.

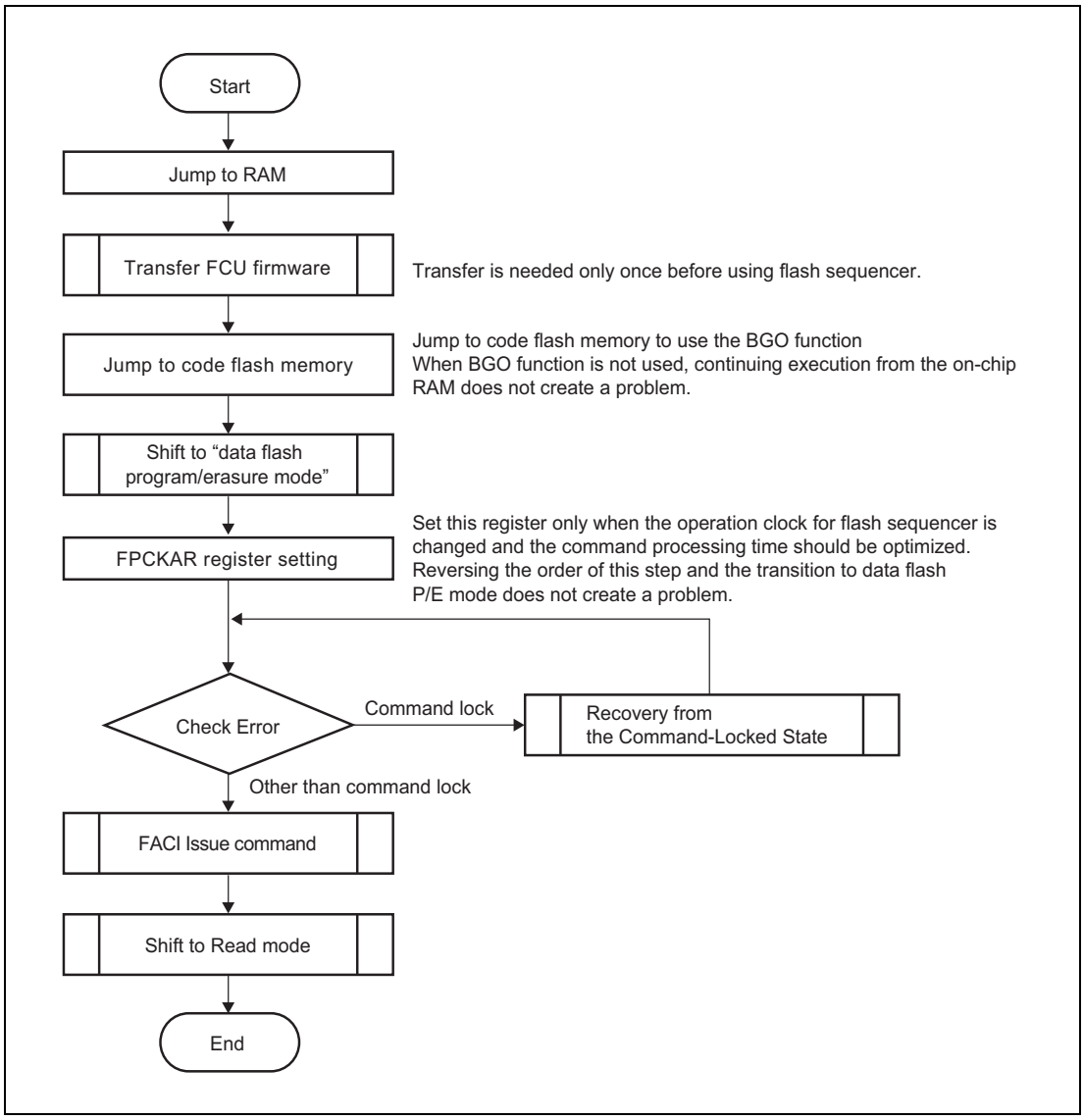


Figure 6.2 Overview of Command Usage in Data Flash Program/Erasure Mode

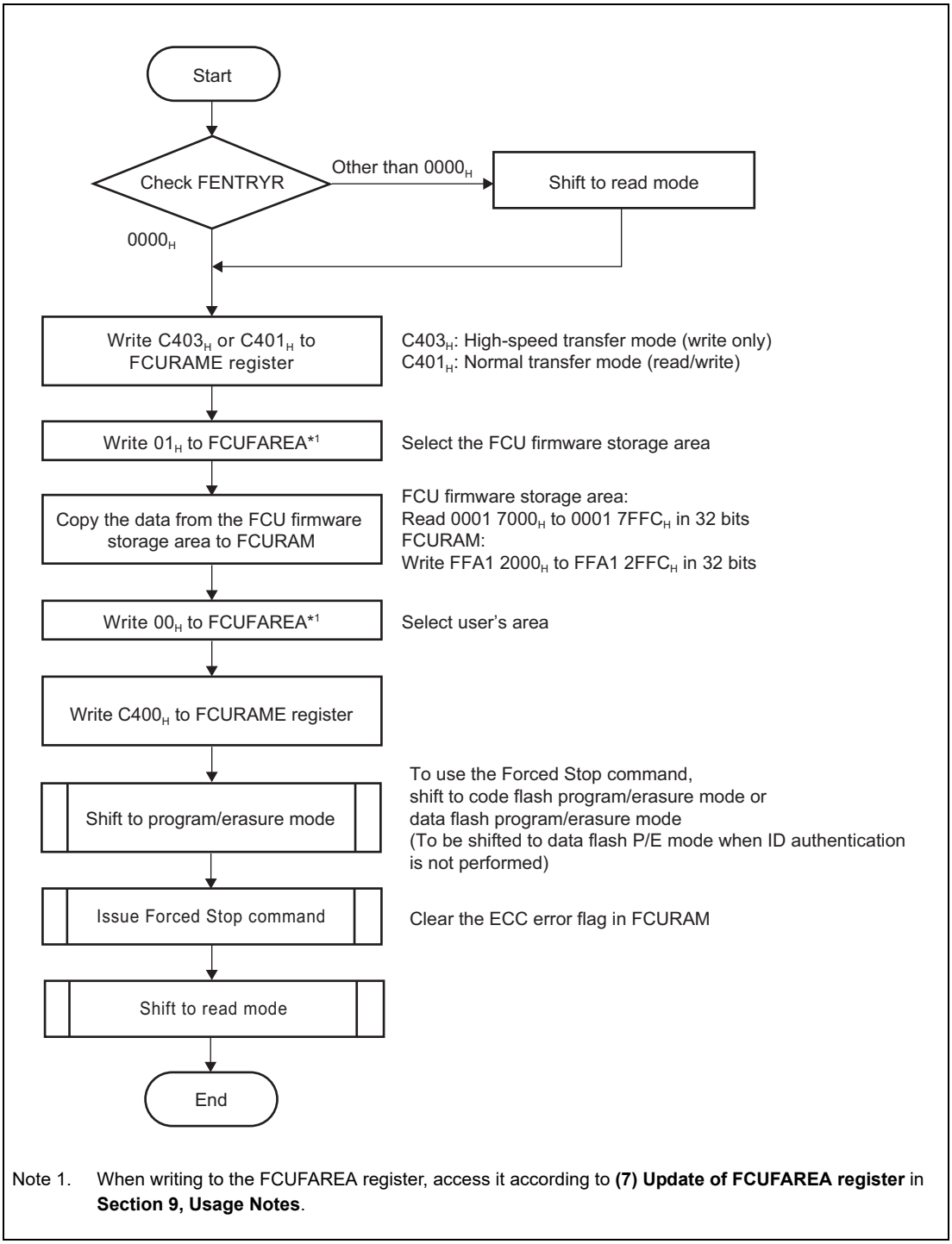
6.3.3 FCU Firmware Transfer (Only FCURAM Devices)

To use the flash sequencer, the FCU firmware should be stored in FCURAM. As the FCU firmware is not stored in FCURAM at power on is executed, it is required to copy the FCU firmware from the FCU firmware storage area to FCURAM. This copy operation is required only once before the flash sequencer is used. You do not have to update FCURAM again because executing the FACI command does not update FCURAM.

As the FCURAM storage data is undefined at power on, an ECC error is generated by the write to FCURAM. After copying the FCU firmware, issue Forced Stop command to initialize the FRCRCT and FRDTCT bits in the FSTATR register.

Processing of a “Forced Stop” command is all implemented in the hardware. Before the FCU firmware is stored or when copying of the firmware is completed unsuccessfully, it is possible to execute “Forced Stop” command normally.

This FCU Firmware transfer is not required in FCUROM devices.



Note 1. When writing to the FCUFAREA register, access it according to **(7) Update of FCUFAREA register** in **Section 9, Usage Notes**.

Figure 6.3 Transfer Flow of FCU Firmware

Figure 6.4 shows the configuration of the FCU firmware. The area from 0001 7000_H to #CODE_END holds the instruction codes to be executed by the FCU. The area from #CODE_END + 4 to 0001 $7FF7_H$ is reserved. In addition, when copying the data from the FCU firmware storage area to FCURAM, it is necessary to copy 4-Kbyte data including the reserved area. Location 0001 $7FF8_H$ holds the number of bytes in the code area divided by 4. Location 0001 $7FFC_H$ holds a checksum, which is the two-byte result of adding all values in the code area. After the FCU firmware is transferred to the FCURAM from the FCU firmware storage area, check the contents of the FCURAM by calculating the checksum of the code area (FFA1 2000_H to #CODE_END_RAM) in the FCURAM and comparing it with the checksum stored at address 0001 $7FFC_H$ of the FCU firmware storage area.

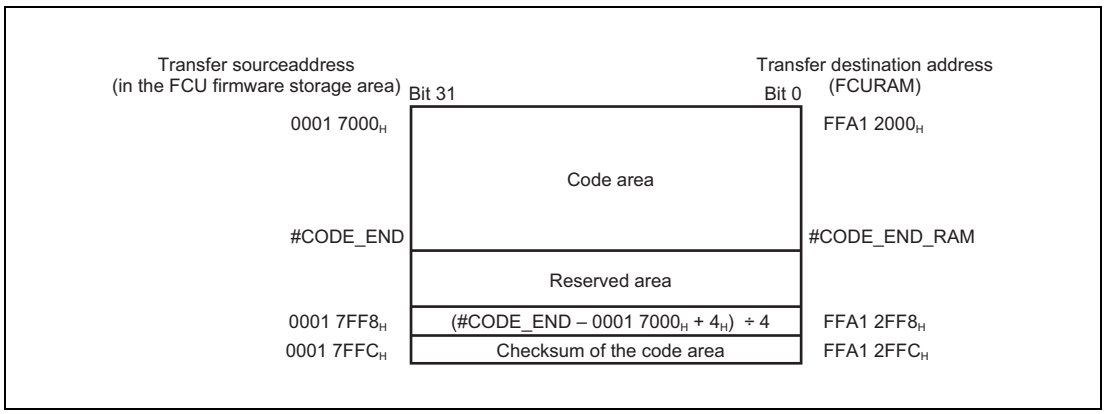


Figure 6.4 Configuration of FCU Firmware

6.3.4 Shift to Code Flash Program/Erasure Mode

To use the FACI commands relating the code flash memory, operation should be shifted to the code flash program/erasure mode. Set the FENTRYRC bit in the FENTRYR to 1 to shift to the code flash program/erasure mode.

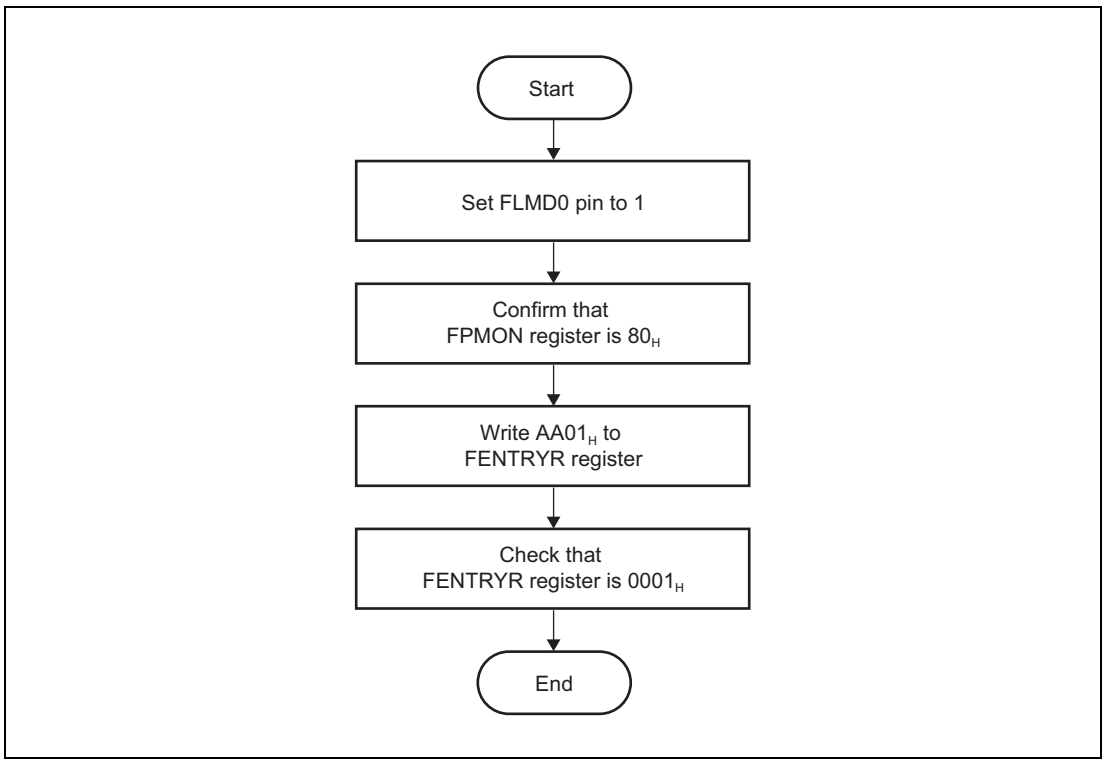


Figure 6.5 Flow of Shift to Code Flash Program/Erasure Mode

6.3.5 Shift to Data Flash Program/Erasure Mode

To use the FACI commands relating the data flash memory, operation should be shifted to the data flash program/erasure mode. Set the FENTRYRD bit in the FENTRYR to 1 to shift to the data flash program/erasure mode.

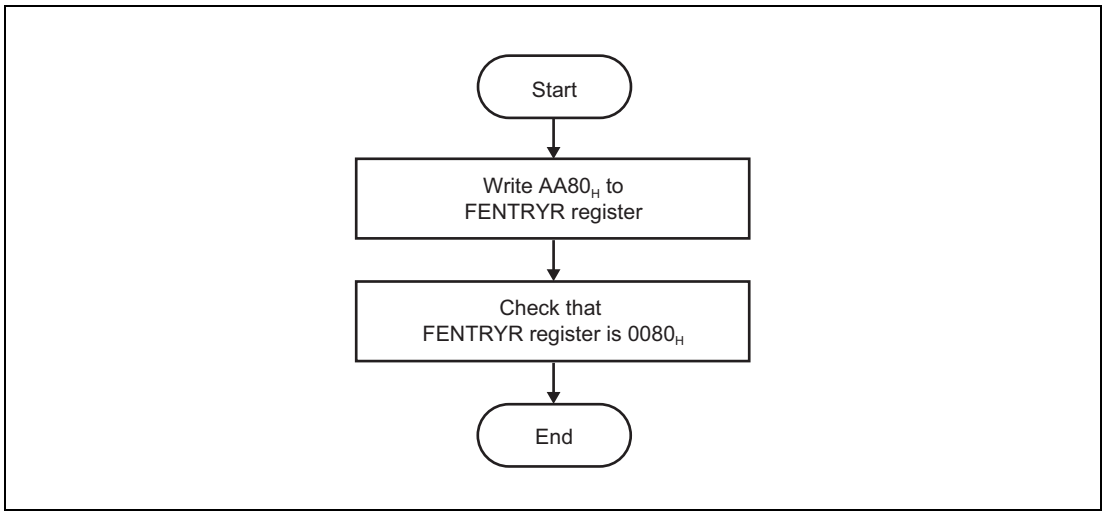
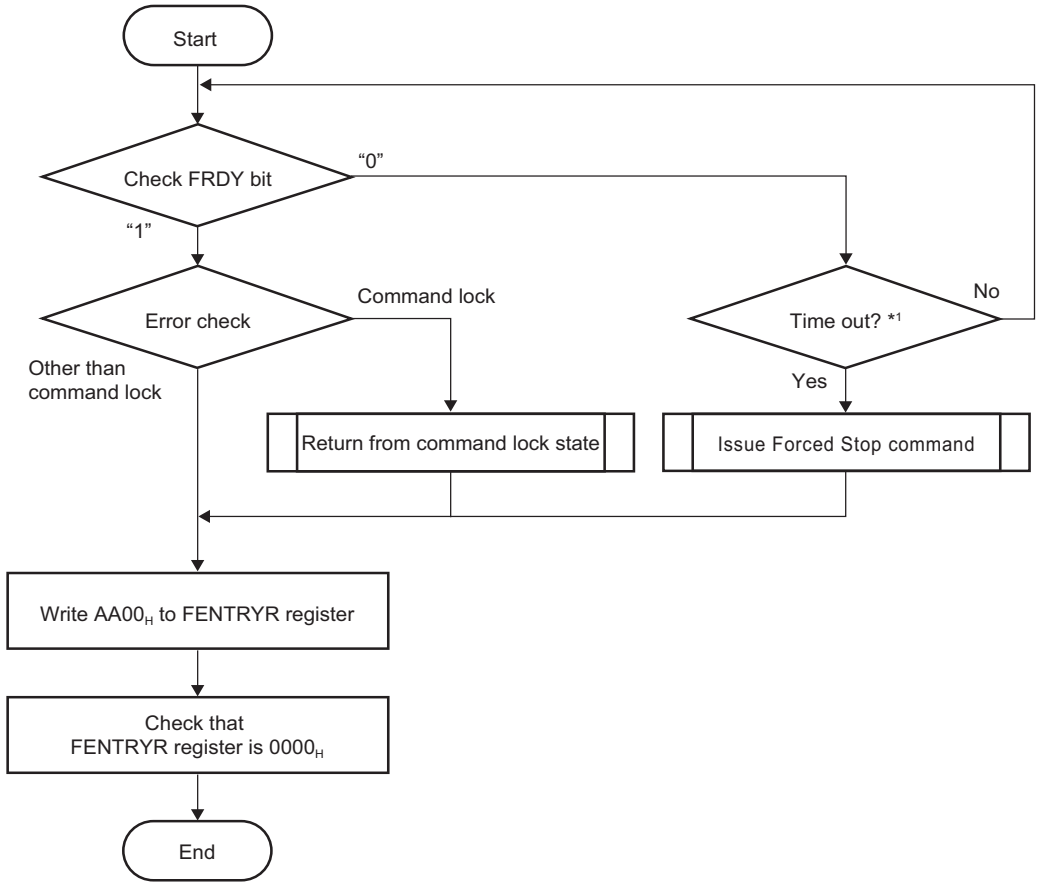


Figure 6.6 Flow of Shift to Data Flash Program/Erasure Mode

6.3.6 Shift to Read Mode

To read the flash memory without using the BGO function, the operation should be shifted to the read mode. To shift to the read mode, set the FENTRYR register to 0000_H. When entering the read mode, the flash sequencer processing should be completed and the operation is in other than command lock state.



Note 1. Determined based on 1.1 times of the maximum time for 32-Kbyte erasing (see *Table 1.96 Timing characteristics* in *Section 1.13.1 Code Flash*, in *the Electrical Target Specification*).

Figure 6.7 Flow of Shift to Read Mode

6.3.7 ID Authentication

To use the FACI command in code flash program/erasure mode, release security by ID authentication and set 0 to the IDST bit in the SELFIDST register. When the IDST bit is 1, the FACI command is not accepted. **Figure 6.8** shows the ID compare method using SELFID0 to SELFID3, and how the compare result is checked by SELFIDST.

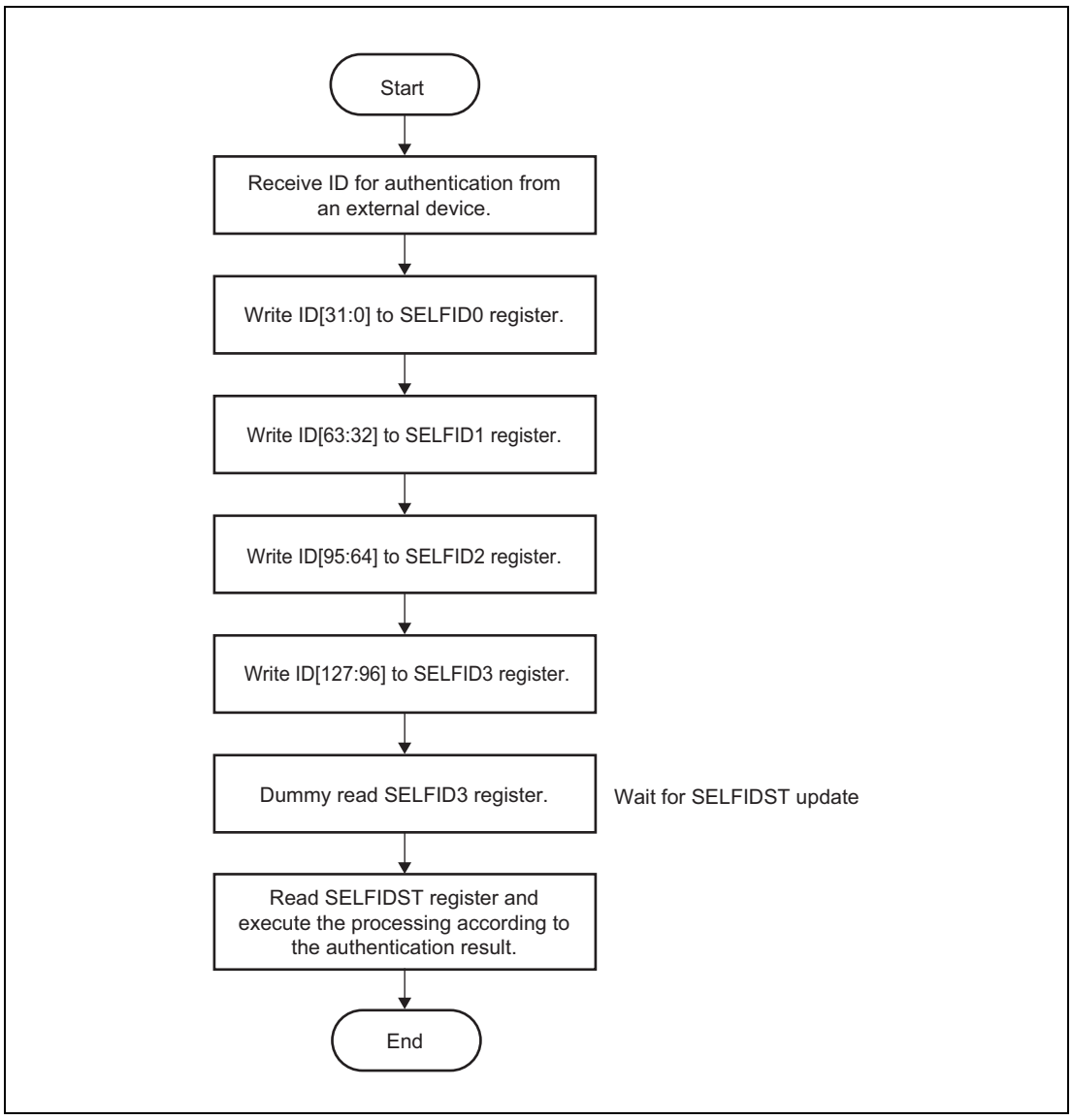


Figure 6.8 Flow of ID Compare

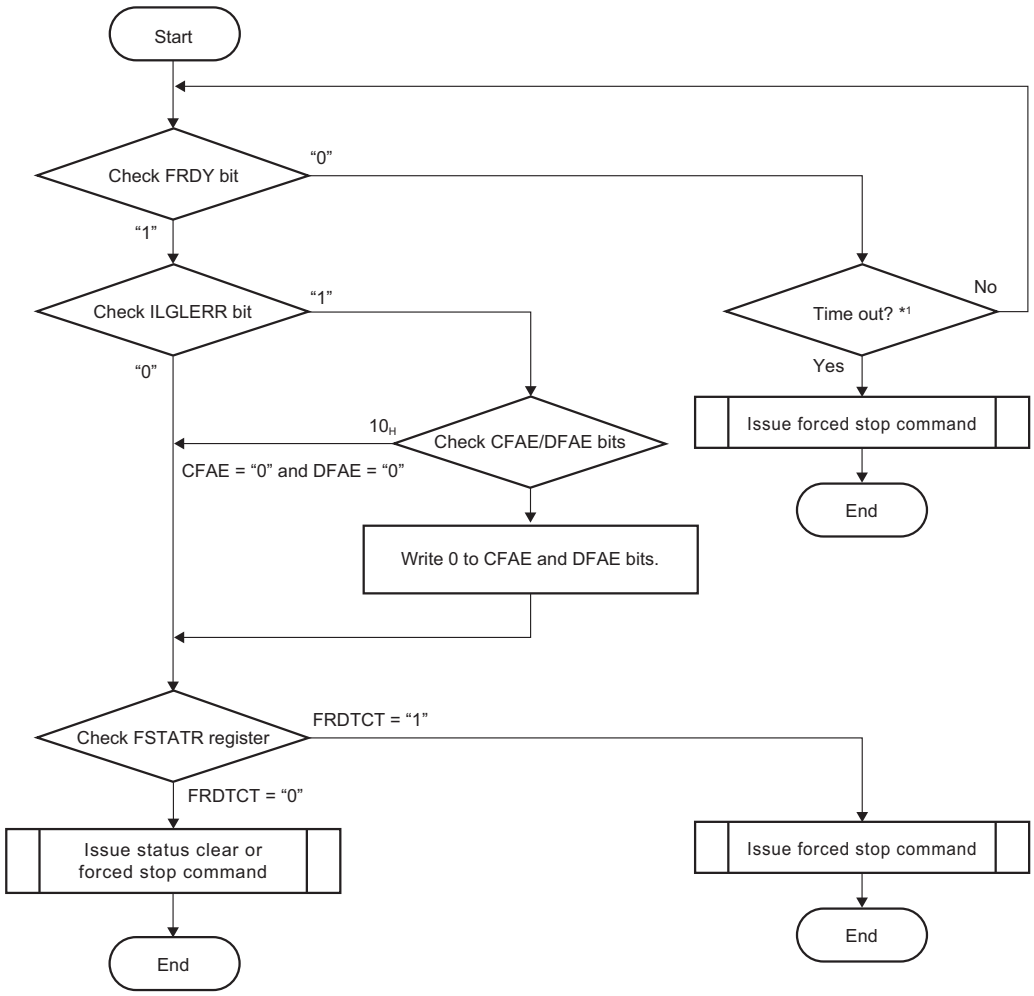
6.3.8 Return from Command Lock State

When the flash sequencer enters the command lock state, FACI commands cannot be accepted. To release the command lock state, use the status clear command, forced stop command, or FASTAT register.

When the command lock state is detected by checking an error before issuing the program/erasure suspend command, the FRDY bit in the FSTATR register may hold 0 without completing the command processing. If the processing is not completed within the maximum program/erasure time specified by electrical characteristics, it is determined as time out and the flash sequencer should be stopped by the forced stop command.

When the ILGLERR bit in the FSTATR register is 1, check the FASTAT value. If the CFAE or DFAE bit in the FASTAT register is 1, the command lock state cannot be released by the status clear or forced stop command.

The FRDTCT bit in the FSTATR register are not changed from 1 to 0 by the status clear command. When these bits are set to 1, use the forced stop command to release the command lock state. The other bits to be the command lock source can be changed from 1 to 0 by the status clear or forced stop command.



Note 1. Determined based on 1.1 times of the maximum time for 32-Kbyte erasing (see *Table 1.96 Timing characteristics* in *Section 1.13.1 Code Flash*, in *the Electrical Target Specification*).

Figure 6.9 Return from Command Lock State

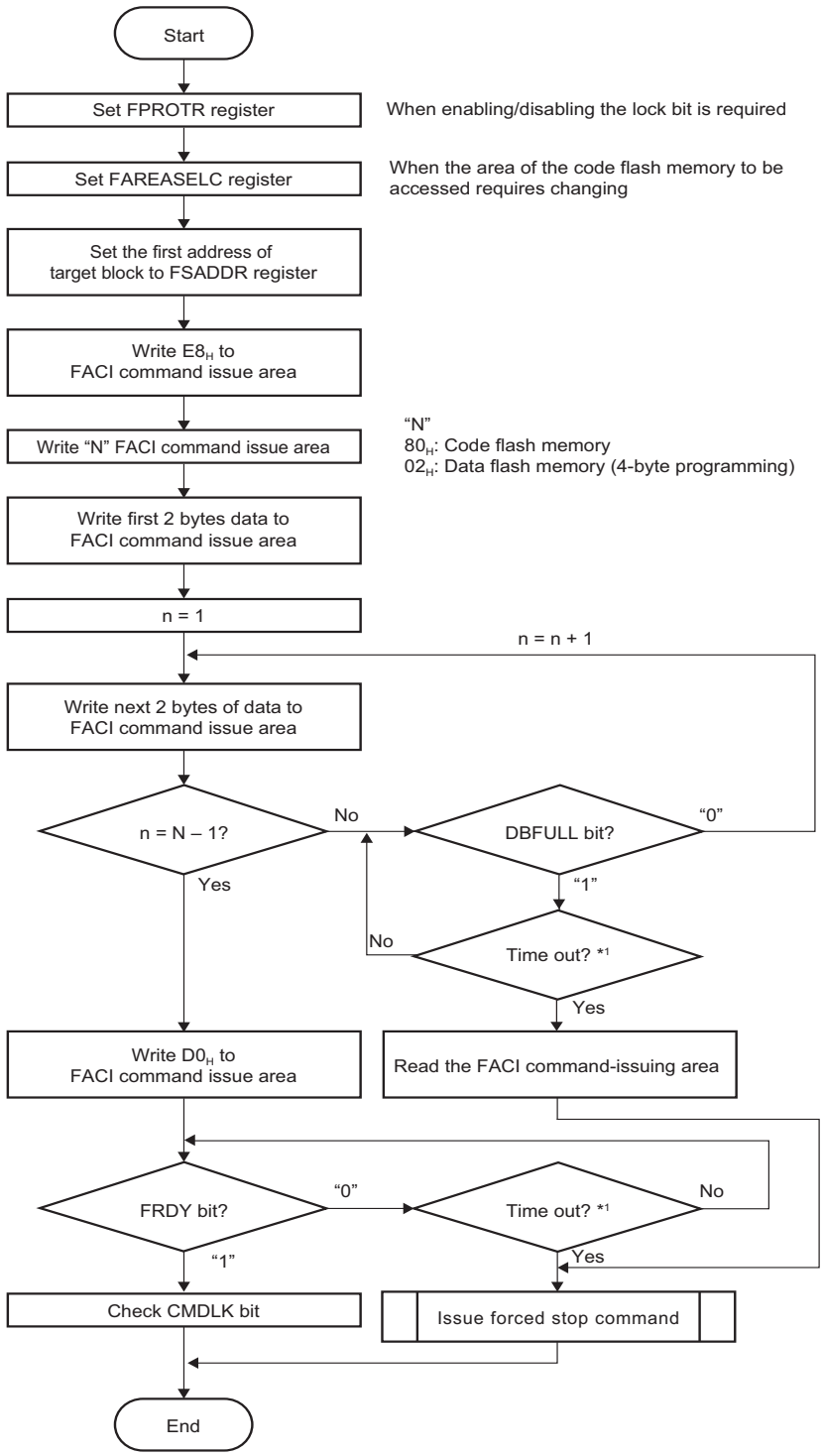
6.3.9 Program Command Issue

"Program" command is used to write to user area, extended user area, and data area.

Before issuing "Program" command, set the first address of target block to the FSADDR register. Writing $D0_H$ to the FACI command issue area at the final access of the FACI command issue starts the "Program" command processing. If the target area of program command processing contains the area not for writing, write $FFFF_H$ to the corresponding area.

Set the FPROTR and FAREASELC registers before issuing the "Program" command. To set the FPROTR register is required to switch enabling/disabling the lock bit. To set the FAREASELC register is required to switch to the area for overwriting the code flash memory.

If issuing the "Program" command is kept while the FACI internal data buffer is full, wait is generated in the P-Bus and it may affect the communication performance of other peripheral IPs. To avoid the wait generation, the DBFULL bit in FSTATR should be 0 when FACI commands are issued. In addition, writing to data area does not make the data buffer full.



Note 1. For the code flash memory, time out is determined based on 1.1 times of the time for 256-byte writing (see *Table 1.96 Timing Characteristics* in *Section 1.13.1 Code Flash*, in *the Electrical Target Specification*). For the data flash memory, time out is determined based on 1.1 times of the time for 4-byte writing (see *Table 1.98 Timing Characteristics* in *Section 1.13.2 Data Flash*, in *the Electrical Target Specification*). If common processing is used, time out is determined based on 1.1 times of the maximum time for 256-byte writing to the code flash memory.

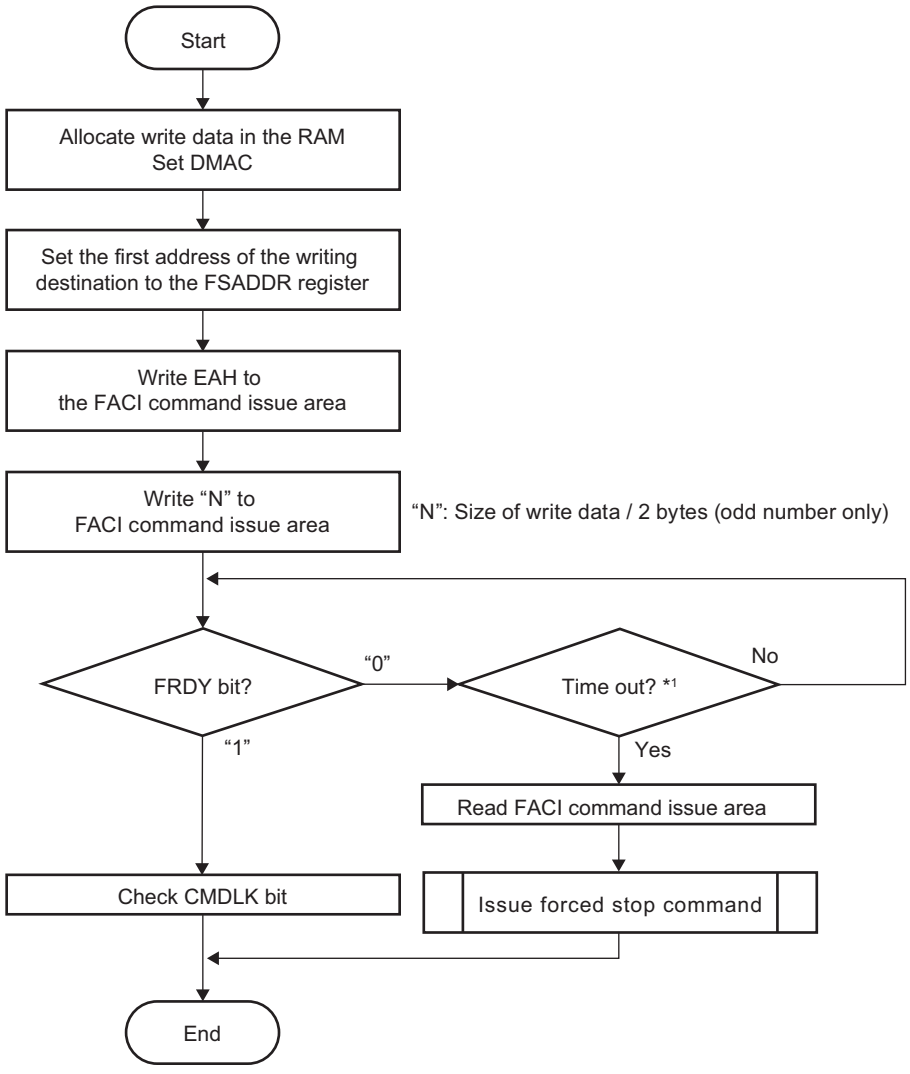
Note 2. Determined based on 5 µs.

Figure 6.10 Program Command Usage

6.3.10 DMA Program Command

"DMA Program" command is used to write multiple 4-byte data sets (which is transferred from DMAC) to the data area, reducing CPU load caused by a large amount of serially written data.

Before issuing the "DMA Program" command, set the first address of the writing destination to the FSADDR register. Also, allocate (in the RAM) the data to be written, and set DMAC to enable DMA transfer from the relevant area to the FACI command issue area. FACI requests DMAC to transfer data immediately after the "DMA Program" command is received and each time 4-byte data writing finishes. Set DMAC to transfer 2-byte data twice for one data transfer request. For details about how to use DMAC, see the user's manual for the relevant product.



Note 1. Determined based on the sum of the maximum time for 4-byte write to the data flash memory (see *Table 1.98 Timing Characteristics* in *Section 1.13.2 Data Flash*, in *the Electrical Target Specification*) x "N"/2 × 1.1 and the time required for DMA transfer for the write data.

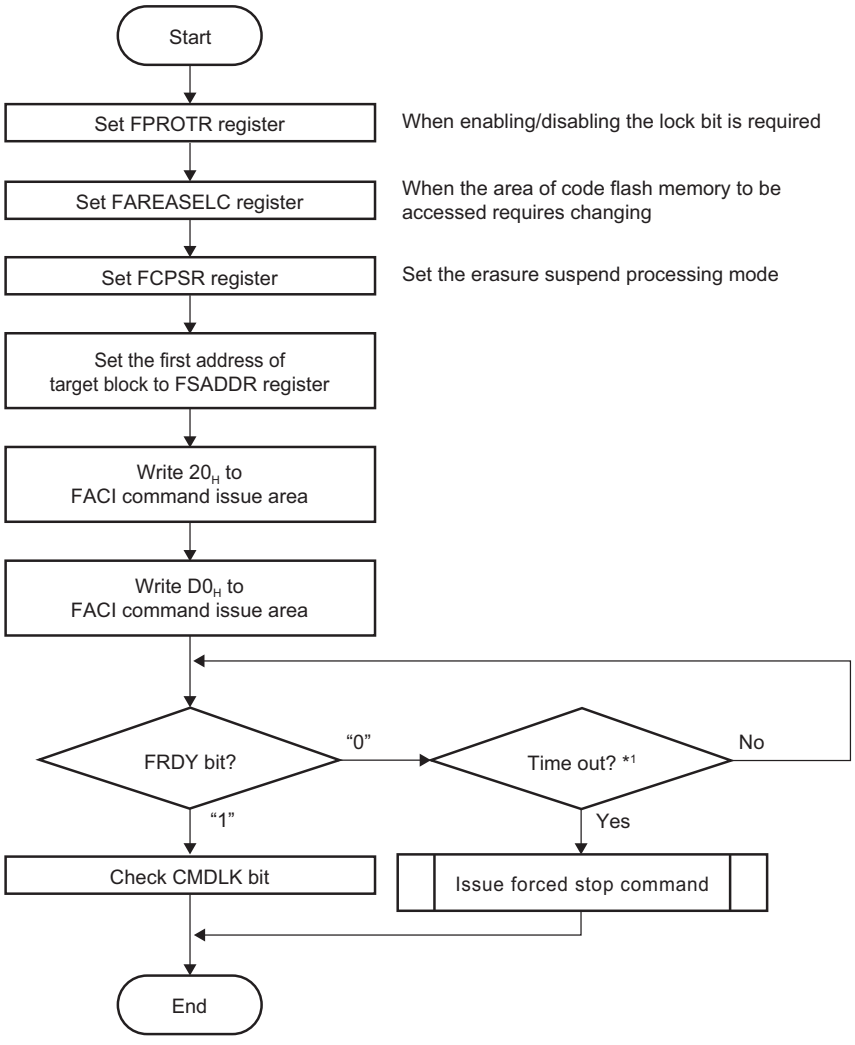
Figure 6.11 DMA Program Command Usage

6.3.11 Block Erase Command

"Block Erase" command is used to erase the user area, extended user area, lock bit, and data area.

Before issuing "Block Erase" command, set the first address of target block to the FSADDR register. Writing 20_H and $D0_H$ to the FACI command issue area starts the "Block Erase" command processing.

Set the FPROTR, FAREASELC, and FCPSR registers before issuing the "Block Erase" command. To set the FPROTR register is required to switch enabling/disabling the lock bit. To erase the lock bit, issue the "Block Erase" command while the FPROTCN bit in the FPROTR register is 1. To set the FAREASELC register is required to switch to the area for overwriting the code flash memory. To set the FCPSR register is required to switch the suspending method by the program/erasure suspend command (suspend priority mode/erasure priority mode).



Note 1. For the code flash memory, time out is determined based on 1.1 times of the maximum erase time for 32-Kbyte block of the code flash memory (see *Table 1.96 Timing Characteristics* in *Section 1.13.1 Code Flash*, in *the Electrical Target Specification*). For the data flash memory, time out is determined based on 1.1 times of the maximum erase time for 64-byte block (see *Table 1.98 Timing Characteristics* in *Section 1.13.2 Data Flash*, in *the Electrical Target Specification*). If common processing is used, time out is determined based on 1.1 times of the maximum erase time for 32-Kbyte block of the code flash memory.

Figure 6.12 Block Erase Command Usage

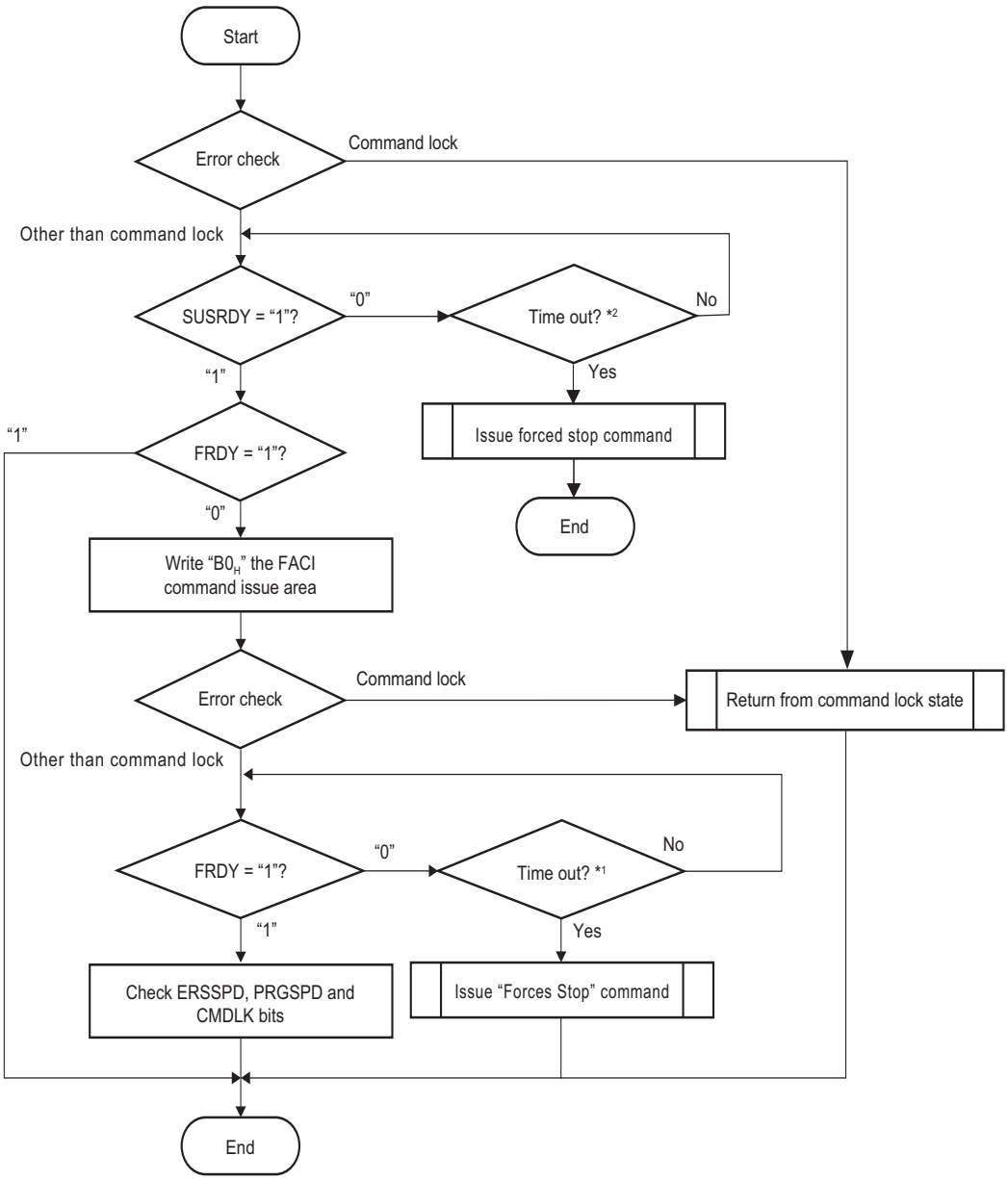
6.3.12 Program/Erasure Suspend Command

"Program/Erasure Suspend" command is used for suspending "Program" or "Erasure" command processing. Before issuing "Program/Erasure Suspend" command, check that CMDLK bit is "0" to ensure that "Program" or "Erasure" command processing is being performed correctly. In addition, check that the SUSRDY bit is "1" to ensure that "Program/Erasure Suspend" command is acceptable. After issuing "Program/Erasure Suspend" command, check CMDLK bit to ensure no error has occurred.

If an error has occurred, the CMDLK bit is set to "1". If "Program" or "Erasure" command processing is complete within the period from when the SUSRDY bit is ensured to be "1" until "Program/Erasure Suspend" command is accepted, no error occurs, hence no transition to a suspended state (the FRDY bit is "1" and both ERSSPD and PRGSPD bits are "0").

Once "Program/Erasure Suspend" command is accepted and "Program" or "Erasure" command processing is normally suspended, flash sequencer enters a suspended state and that FRDY bit is "1" and ERSSPD or PRGSPD bit is "1". After issuing "Program/Erasure Suspend" command and ensuring that flash sequencer has entered suspend state, determine which operation to perform in the succeeding process. If "Program/Erasure Resume" command is issued in the succeeding process while flash sequencer has not entered a suspended state, an illegal command error occurs and flash sequencer shifts to "Command Lock" state.

If the erasure suspended state is entered, programming to blocks other than an erasure target can be performed. Additionally, the programming and erasure suspended states can shift to read mode by clearing the FENTRYR register.



Note 1. Determined based on 1.87 ms.
Note 2. Determined based on 13 µs.

Figure 6.13 "Program/Erasure Suspend" Command Usage

(1) Suspend program command

"Program/Erasure suspend" command is issued during programming operation to the flash memory, flash sequencer stops the operation. **Figure 6.14** gives an overview of operation for suspending "Program" command processing. Upon accepting "Program" command, FACI clears FRDY bit to "0" and starts programming. Once FACI enters a state where it is ready to accept "Program/Erasure Suspend" command after the start of programming, SUSRDY bit is set to "1". When "Program/Erase Suspend" command is issued, FACI accepts the command and clears SUSRDY bit. If "Program/Erase Suspend" command is issued while applying a write pulse, FCU continues applying the pulse. After a specified pulse application time has elapsed, FCU completes applying the pulse, suspends programming, and sets PRGSPD bit to "1". Once the process completes, FACI sets FRDY bit to "1" and enters programming suspended state. If FACI accepts "Program/Erasure Resume" command in this state, FACI clears FRDY and PRGSPD bits to "0" and restarts programming.

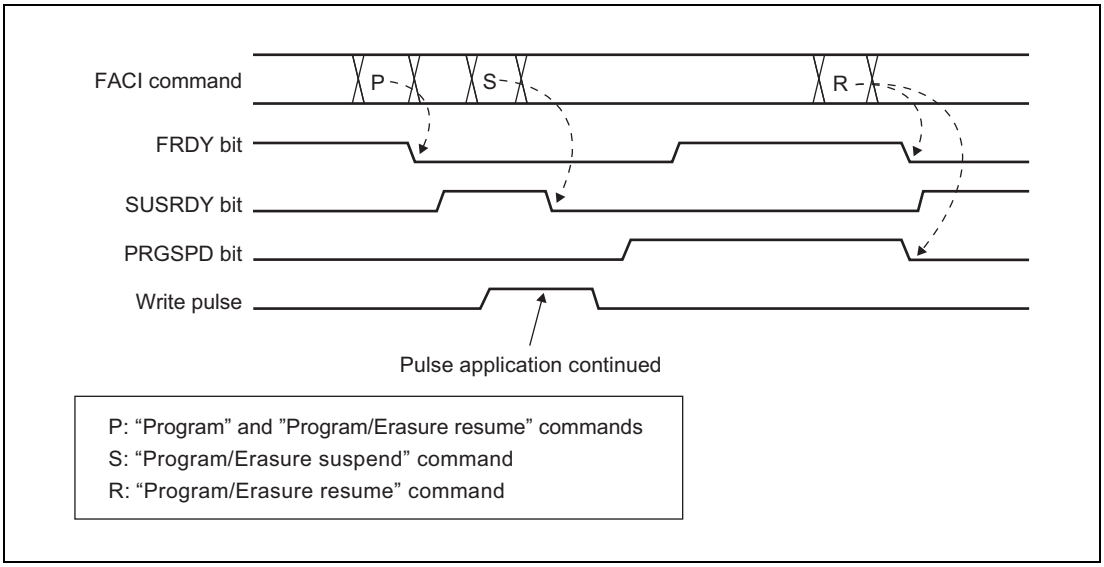


Figure 6.14 Suspend "Program" Command

(2) Suspend erase command in suspension-priority mode

As the method of suspend during erase operation, suspension-priority mode is provided. **Figure 6.15** shows the operation for suspending “Erasure” command processing in suspension-priority mode (FCPSR.ESUSPMD = “0”). Upon accepting an “Erase” command, FACI clears the FRDY bit to “0” and starts erasing. Once FACI enters a state where it is ready to accept “Program/Erase Suspend” command after the start of erasing, the SUSRDY bit is set to “1”. When “Program/Erase Suspend” command is issued, FACI accepts the command and clears the SUSRDY bit. If FCU accepts the command during its erasing operation, FCU starts a suspending process even while applying a pulse and sets ERSSPD bit to “1”. Once the suspending process completes, FACI sets FRDY bit to “1” and enters erasing suspended state. If FACI accepts “Program/Erase Resume” command in this state, FACI clears FRDY and ERSSPD bits to “0” and restarts erasing. The operations of FRDY, SUSRDY, and ERSSPD bits are independent of the erasure-suspended mode.

The setting for erasure-suspended mode affects the control methods for erasure pulse. In suspension-priority mode, if FACI accepts “Program/Erase Suspend” command while applying erasure pulse A, which has not been suspended previously, FCU suspends the pulse application, and FACI enters an erasure-suspended state. After FACI resumes erasing by accepting a “Program/Erasure Resume” command, FCU accepts resume request while applying erasing pulse A, FCU continues applying the pulse. After a specified pulse application time has elapsed, FCU completes applying the pulse, and FACI enters an erasure-suspended state. Next, after FACI accepts “Program/Erasure Resume” command, and FCU starts applying a new pulse B, if FCU accepts “Program/Erase Suspend” command, FCU suspends the pulse application. In suspension priority mode, delay due to suspension can be minimized because the application of an erasure pulse is suspended one time per pulse and priority is given to the suspend processing.

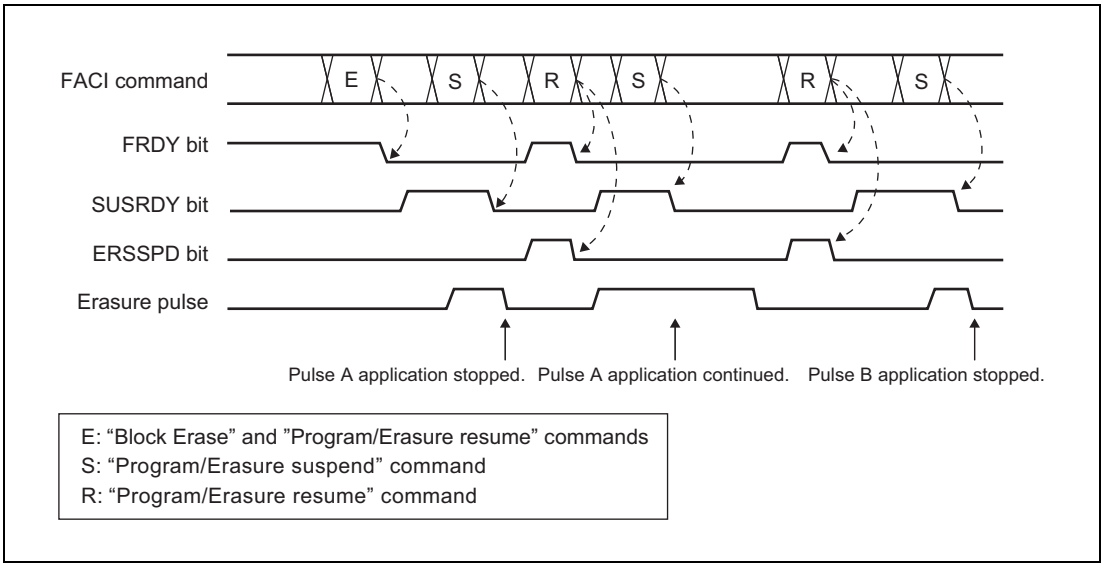


Figure 6.15 Suspend “Erase” Command (Suspension-Priority Mode)

(3) Suspend erase command in erasure-priority mode

As the method of suspend during erase operation, erasure-priority mode (FCPSR.ESUSPMD = “1”) is provided. The operation for suspending “Erasure” command processing in erasure-priority mode is equivalent to that for suspending programming processing. In erasure-priority mode, if FACI accepts “Program/Erasure Suspend” command while applying an erasing pulse, FCU always continues applying the pulse. As processing to reapply an erasing pulse never takes place in this mode, the total time required for “Erase” command processing is shorter than in suspension-priority mode.

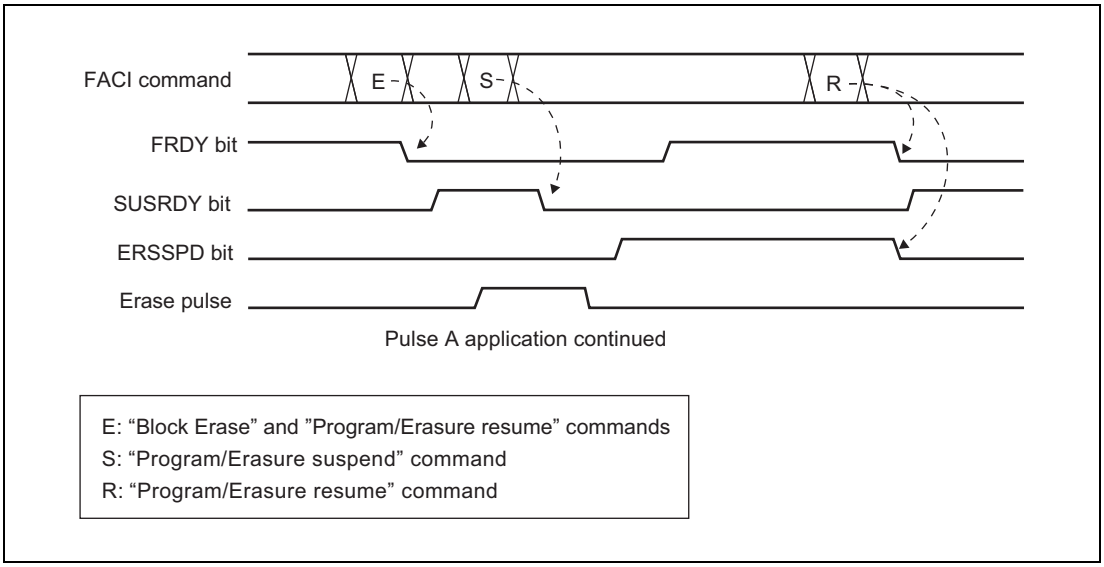
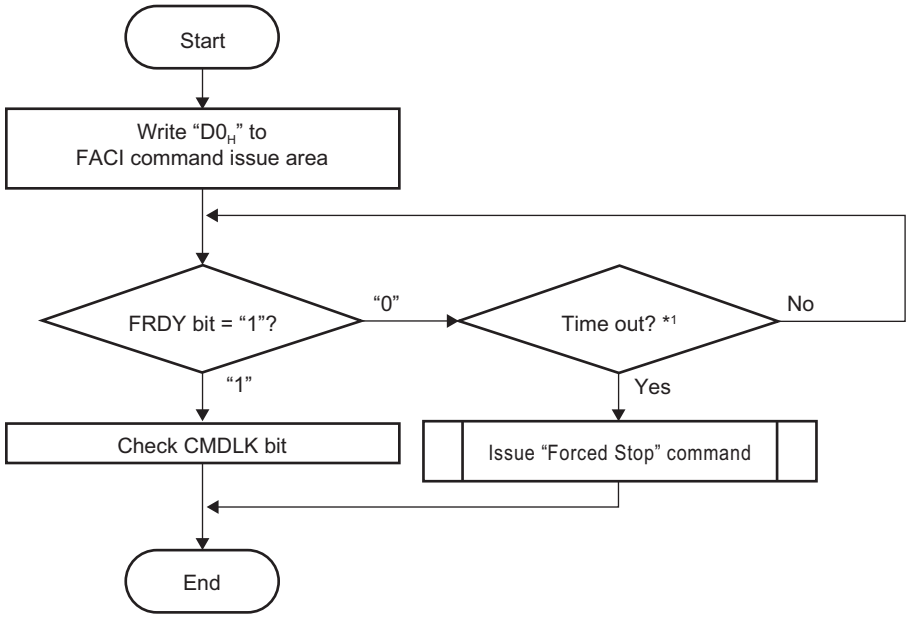


Figure 6.16 Suspend “Erase” Command (Erasure-Priority Mode)

6.3.13 Program/Erasure Resume Command

To resume a suspended programming/erasure processing, use the “Program/Erasure Resume” command. When the settings of the FENTRYR register are changed during suspension, return FENTRYR value to which has been set immediately before the “Program/Erasure Suspend” command was issued, and then issue a “Program/Erasure Resume” command.



Note 1. Determined based on 1.1 times of the maximum time for 32-Kbyte erasing (see *Table 1.96 Timing characteristics* in *Section 1.13.1 Code Flash*, in *the Electrical Target Specification*).

Figure 6.17 “Program/Erasure Resume” Command Usage

6.3.14 Status Clear Command

The status clear command is used to clear the command lock state. (See **Section 6.3.8, Return from Command Lock State**.) To clear the OTPDTCT/ILGLERR/ERSERR/PRGERR/CFGDTCT/TBLDTCT bit in the FSTATR register in the command lock state, the status clear command is available. In addition, to clear 1-bit correction flags (the OTPCRCT, CFGCRCT, and TBLCRCT bits), which do not cause transitions to the command lock state (except for FCURAM), the status clear command is available. All status clear command processing is incorporated in the hardware. Therefore, the status clear command can be properly executed even if the FCU firmware is invalid.

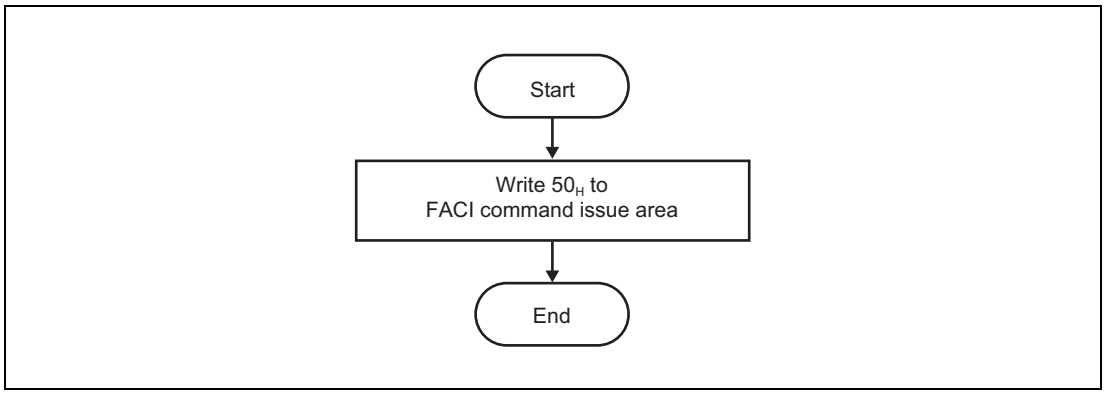
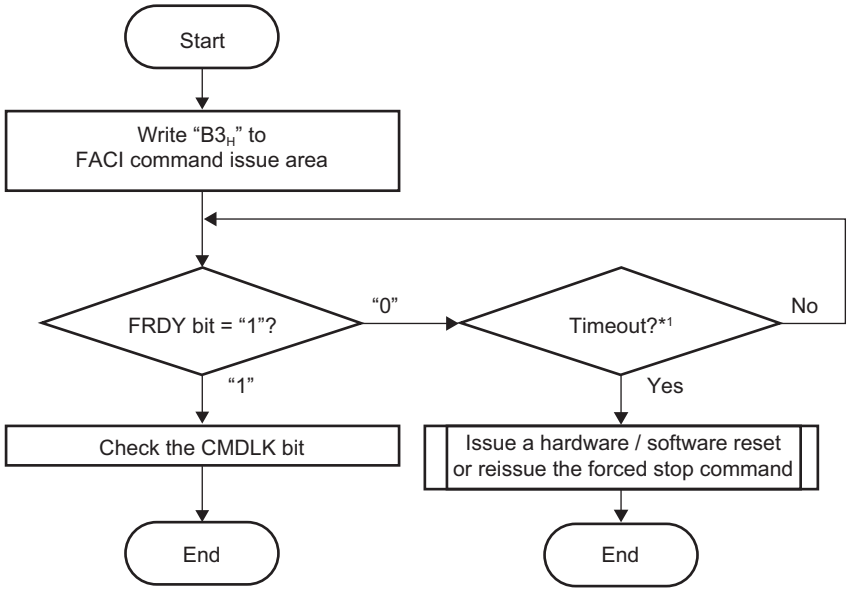


Figure 6.18 "Status Clear" Command Usage

6.3.15 Forced Stop Command

"Forced Stop" command provides the shortest latency when user wants to stop a flash sequencer command processing. However, after issuing "Forced Stop" command, flash sequencer does not guarantee any result of stopped command operation such as data in programmed or erased area. And, suspended operation can not be resumed. The "Program/Erasure" command operation which is suspended by "Forced Stop" command is defined as 1 programming count.

When "Forced Stop" command is issued, whole FCU and a part of FACI are initialized. "Forced Stop" command can be used in order to resume from the command lock state or for timeout process of flash sequencer operation. (See **Section 6.3.8, Return from Command Lock State**.) Processing of a "Forced Stop" command is all implemented in the hardware. Even when the FCU firmware is illegal, it is possible to execute "Forced Stop" command normally.



Note: When SWRES is issued, RESF register cannot be checked or cleared until SWRES released.

Note 1. Determined based on 25 µs.

Figure 6.19 "Forced Stop" Command Usage

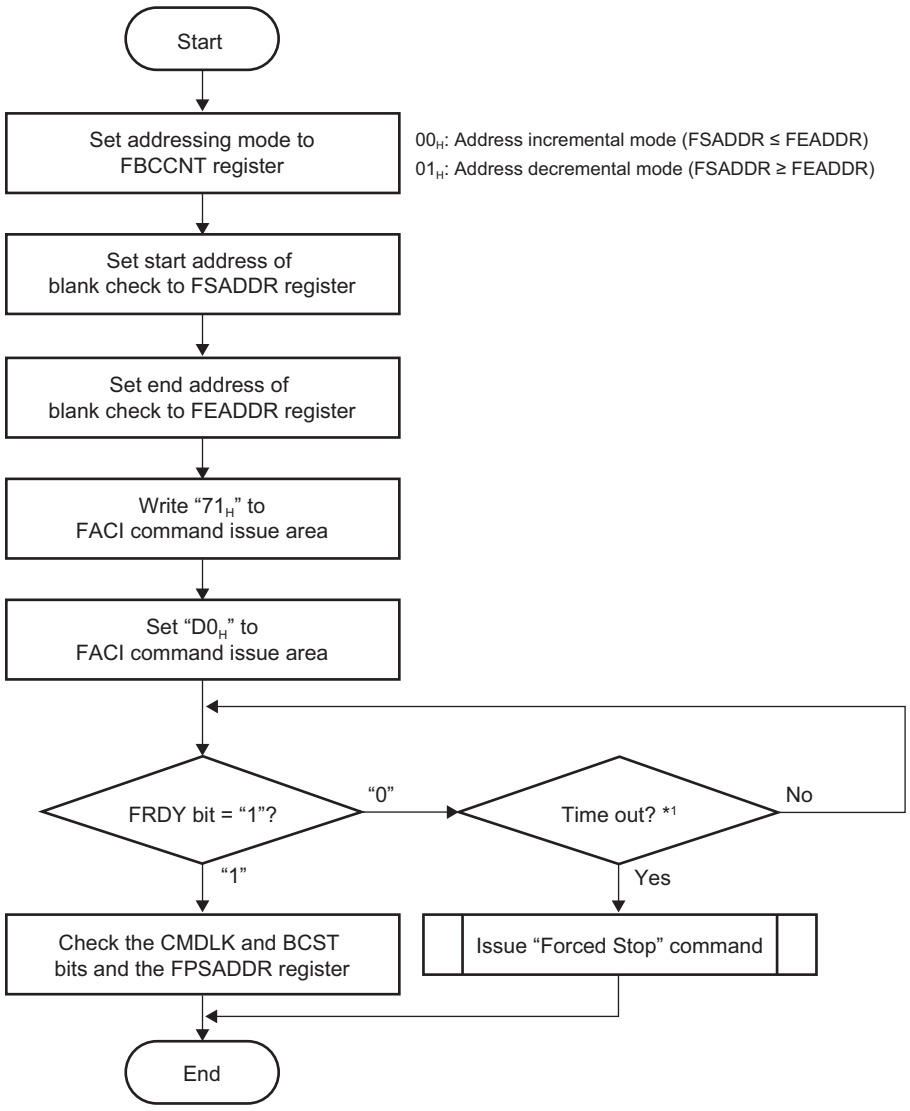
6.3.16 Blank Check Command

Values read from data flash memory that has been erased but not yet been programmed again are undefined. Use the “Blank Check” command when you need to confirm that an area is in the non-programmed state. For the method for the code flash memory, See **Section 8.4, Blank Checking of Code Flash Memory**.

Before issuing “Blank Check” command, set addressing mode, start address, and end address to FBCCNT, FSADDR, and FEADDR register, respectively. When blank check addressing mode is set to decremental mode (i.e. FBCCNT.BCDIR = “1”), address specified in FSADDR should be larger than or equal to address in FEADDR. Conversely, address in FSADDR should be smaller than or equal to address in FEADDR when blank check addressing mode is set to incremental mode (i.e. FBCCNT.BCDIR = “0”). If setting of BCDIR, FSADDR, and FEADDR are inconsistent, FACI detects error and flash sequencer enters “Command Lock” state. Blank check unit can be set by 4 bytes unit, range from 4 bytes to 64 Kbytes.

Write 71_H and $D0_H$ to the FACI command issue area to start “Blank Check” command processing. Completion of command processing can be confirmed by FRDY bit of FSTATR register. At the end of processing, the result of “Blank Check” is stored in the BCST bit in the FBCSTAT register. If non-blank data exists within blank checked area, address of non-blank data is indicated to FPSADDR register.

“Blank Check” is the function to check the erasure state of the area where erasure operation is normally completed. When erasure operation is aborted due to reset input or power off, this function cannot be used to check the erasure state.

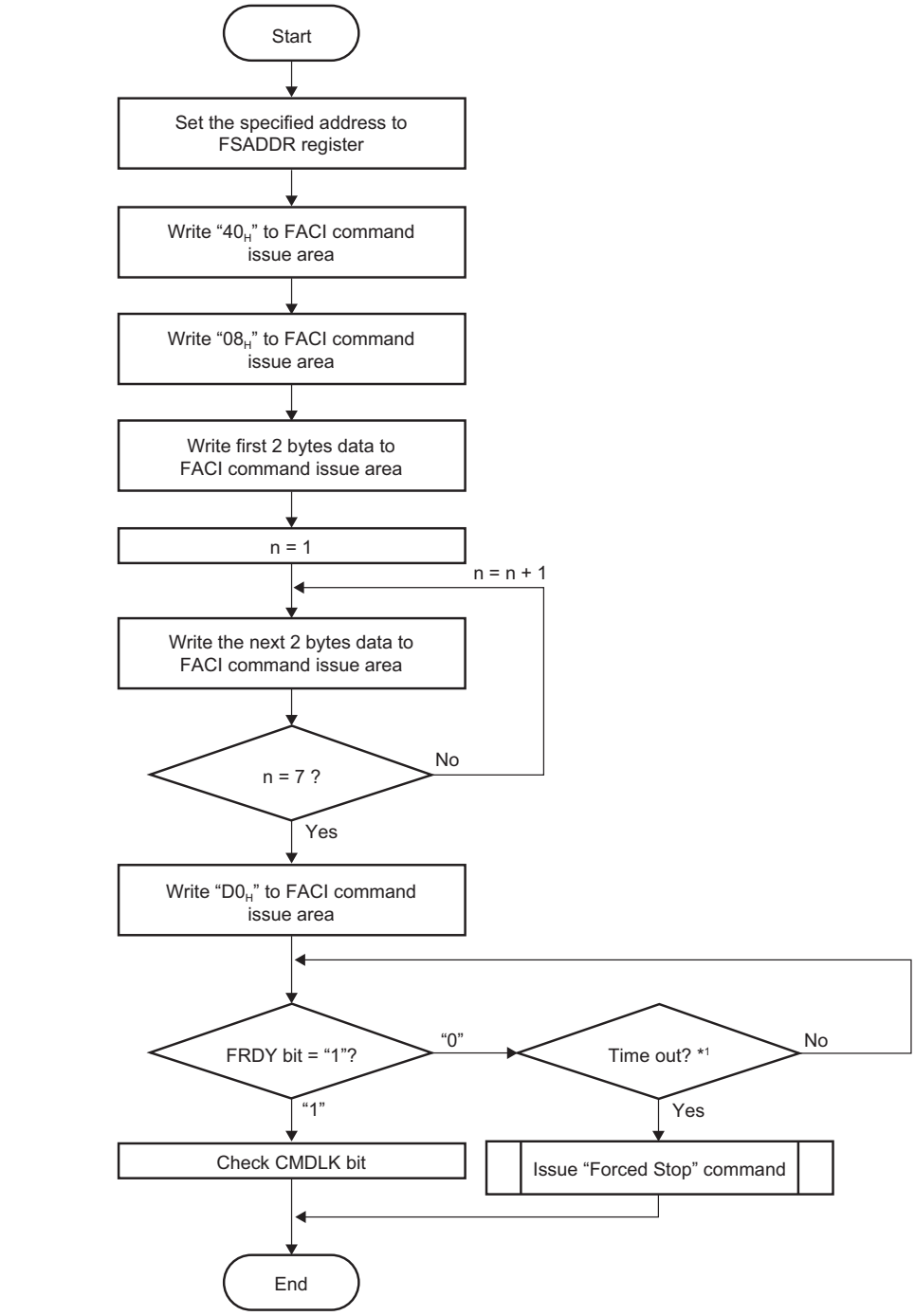


Note 1. Determined based on 1.1 times of the maximum blank check time (see *Table 1.98 Timing Characteristics* in *Section 1.13.2 Data Flash*, in *the Electrical Target Specification*)

Figure 6.20 "Blank Check" Command Usage

6.3.17 Config Program Setting Command

"Config Program" command is used to set the ID, security function, safety function, and option byte. Before issuing the Config Program command, set the specified address (shown in **Table 6.5**) to the FSADDR register. Writing $D0_H$ to the FACI command issue area at the final access of the FACI command issue starts the Config Program command processing.



Note 1. Determined based on 170 ms.

Figure 6.21 "Config Program" Command Usage

As for the Configuration Program settable data and the address value to be set in the FSADDR register, refer to **Table 6.5**. Once 0 is set as data in the security setting area, it cannot be changed to 1. Data in other areas can be change to any value each time the Configuration Program command is executed.

Table 6.5 Address Used by Configuration Program Command

Address	Setting Data
FF30 0070$_H$	Option byte
FF30 0060$_H$	Variable reset vector
FF30 0050$_H$	ID for authentication
FF30 0040$_H$	Security

Table 6.6 lists the security setting data when various security functions are enabled.

Table 6.6 List of Security Setting Data

Security Functions	Security Setting Data (16 bytes)
ID authentication enabled in serial programming mode	FFFF FFFF FFFF FFFF FFFF FFFF 1EFF FFFF$_H$
Serial programmer connection disabled	FFFF FFFF FFFF FFFF FFFF FFFF F7FF FFFF$_H$
Block erasure command disabled	FFFF FFFF FFFF FFFF FFFF FFFF DFFF FFFF$_H$
Program command disabled	FFFF FFFF FFFF FFFF FFFF FFFF BFFF FFFF$_H$
Read command disabled	FFFF FFFF FFFF FFFF FFFF FFFF 7FFF FFFF$_H$

See the section of the *option bytes* in the *User's Manual* regarding the details for the target registers.

6.3.18 Reading the Configuration Setting Area

When reading the configuration setting area to check the value written by “Config Program” command, set the FCUFSEL bit in the FCUFAREA register to “1”. Setting the FCUFSEL bit to “1” disables reading of the user area. The software that reads the configuration setting area must be executed on the internal RAM. For the address map for the area for configuration settings, see **Table 6.5**.
A configuration setting “authentication ID” stored area cannot be read without SELF ID authentication.

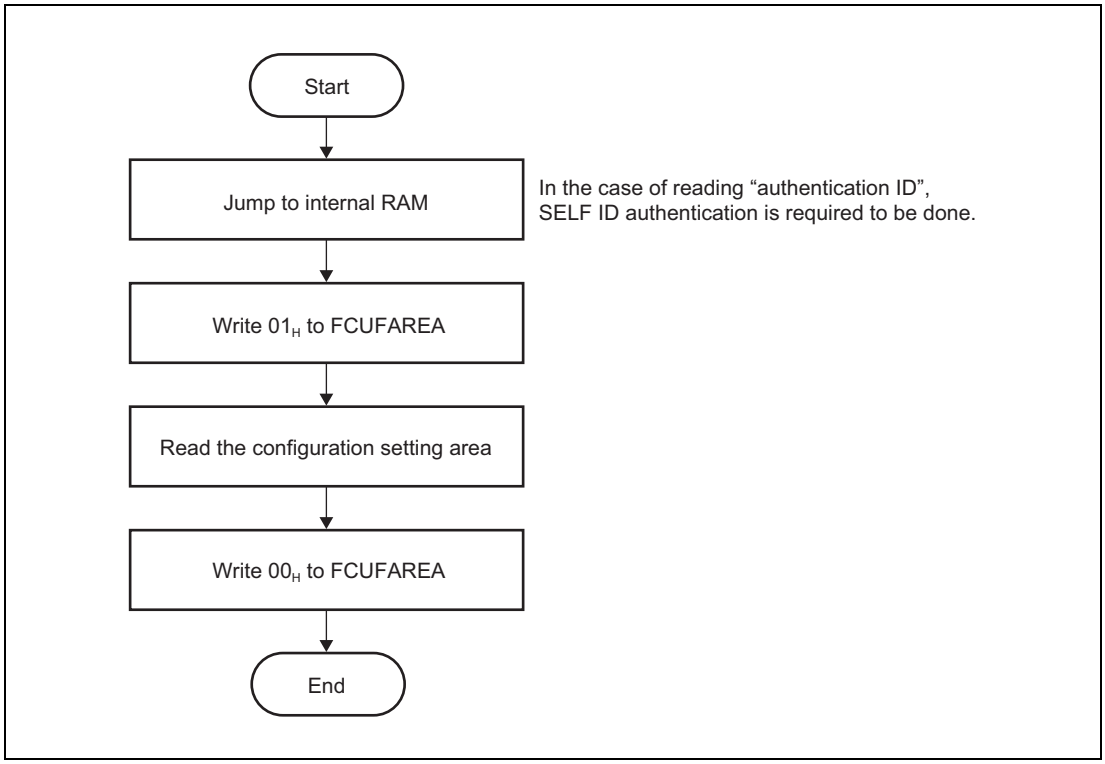


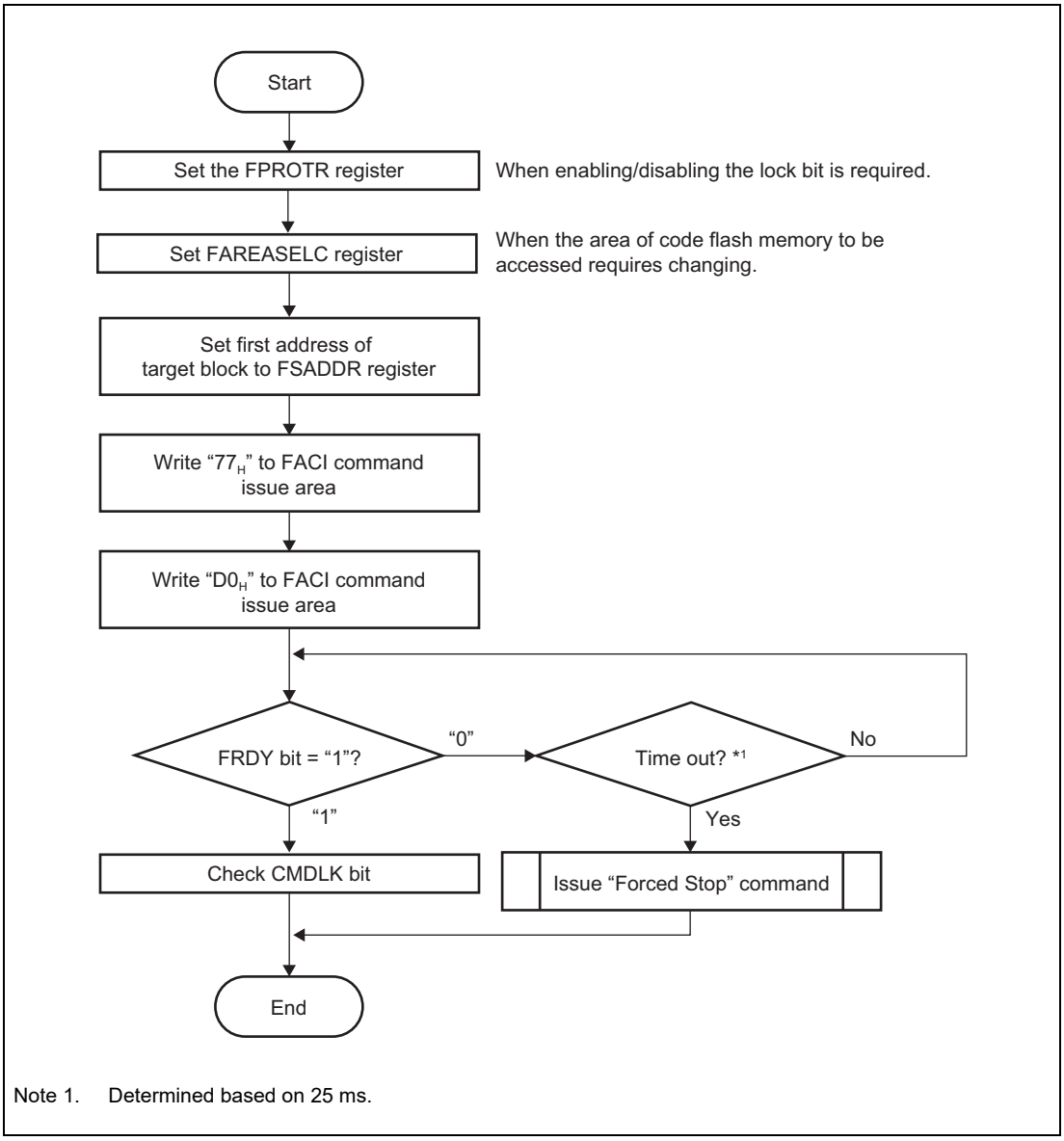
Figure 6.22 Flow of Reading of the Configuration Setting Area

6.3.19 Lock Bit Program Command

"Lock Bit Program" command is used for programming lock bit. For the erasure of lock bits, use the block erasure command. (See **Section 6.3.11, Block Erase Command**.)

Before issuing "Lock Bit Program" command, set first address of target block to FSADRR register. Writing "77_H" and "$D0_H$" to FACI command issue area starts the "Lock Bit Program" command processing.

Set the FPROTR register before issuing the lock bit program command. To set the FPROTR and FAREASELC registers is required to switch enabling/disabling the lock bit. To set the FAREASELC register is required to switch the area for overwriting the code flash memory.



Note 1. Determined based on 25 ms.

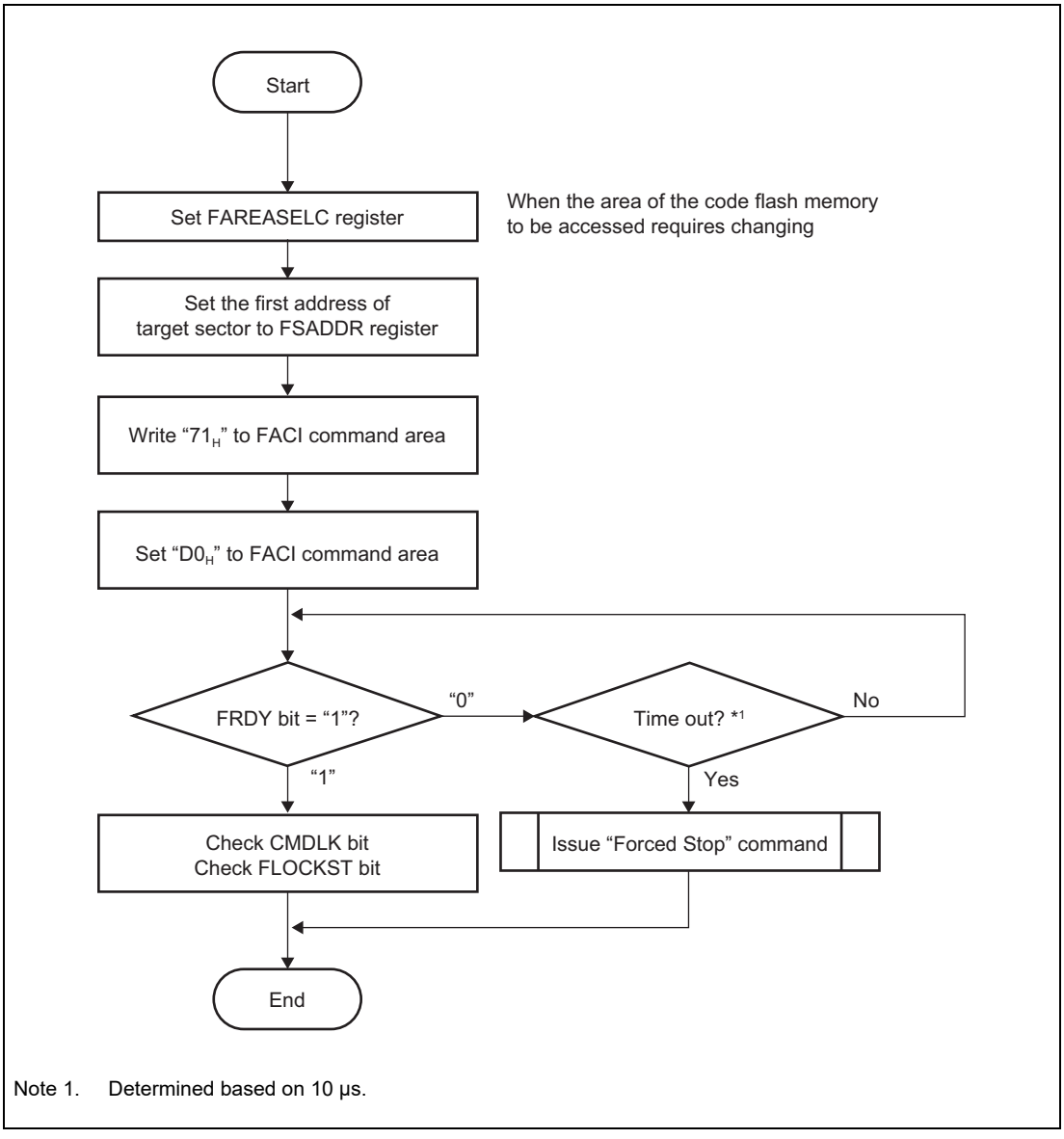
Figure 6.23 "Lock Bit Program" Command Usage

6.3.20 Lock Bit Read Command

"Lock Bit Read" command is used for read lock bit.

Before issuing "Lock Bit Read" command, set first address of target block to FSADRR register. Writing "71_H" and "$D0_H$" to FACI command issue area starts "Lock Bit Read" command processing. Completion of command processing can be confirmed by FRDY bit of FSTATR register. After "Lock Bit Read" command processing is completed normally, the FLOCKST bit in the FLKSTAT register will hold the result of reading the lock bit.

The FAREASELC register must be set before a "Lock Bit Read" command is issued. To set the FAREASELC register is required to switch the area for overwriting the code flash memory.

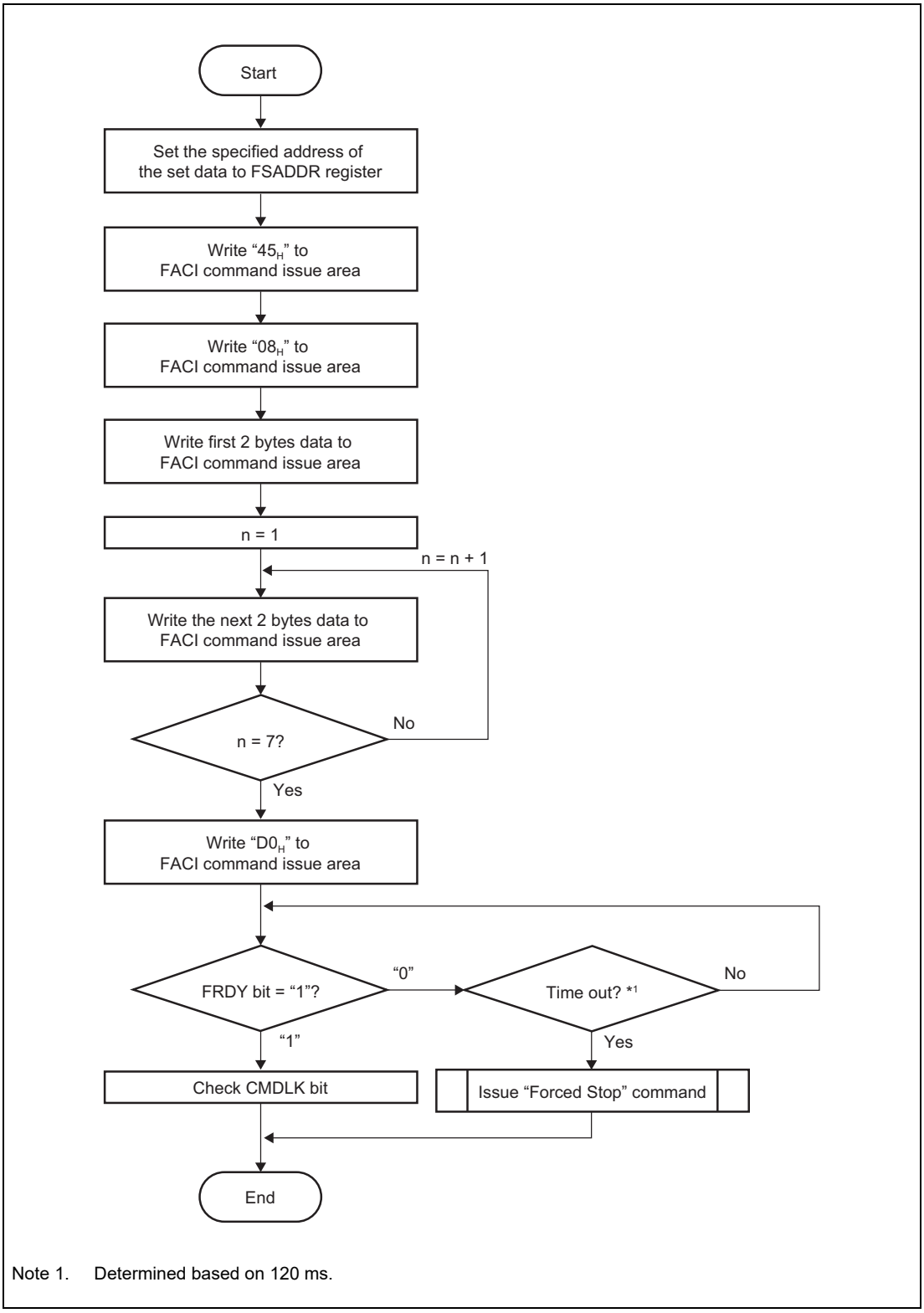


Note 1. Determined based on 10 µs.

Figure 6.24 "Lock Bit Read" Command Usage

6.3.21 OTP Set Command

"OTP Set" command is used to set OTP. Before issuing "OTP Set" command, set the specified address of the set data (shown in **Table 6.7**) to FSADRR register. Writing $D0_H$ to the FACI command issue area at the final access of the FACI command issue starts the OTP Set command processing.



Note 1. Determined based on 120 ms.

Figure 6.25 "OTP Set" Command Usage

Figure 6.26 shows the relationship between the user area blocks and OTP setting flags. An OTP setting flag (OTPF0 to OTPF165) is allocated to each user area block (8 Kbytes × 8 blocks and 32 Kbytes × 158 blocks). The number of blocks that are actually implemented differs from product to product. See the section on flash memory in the user's manual.

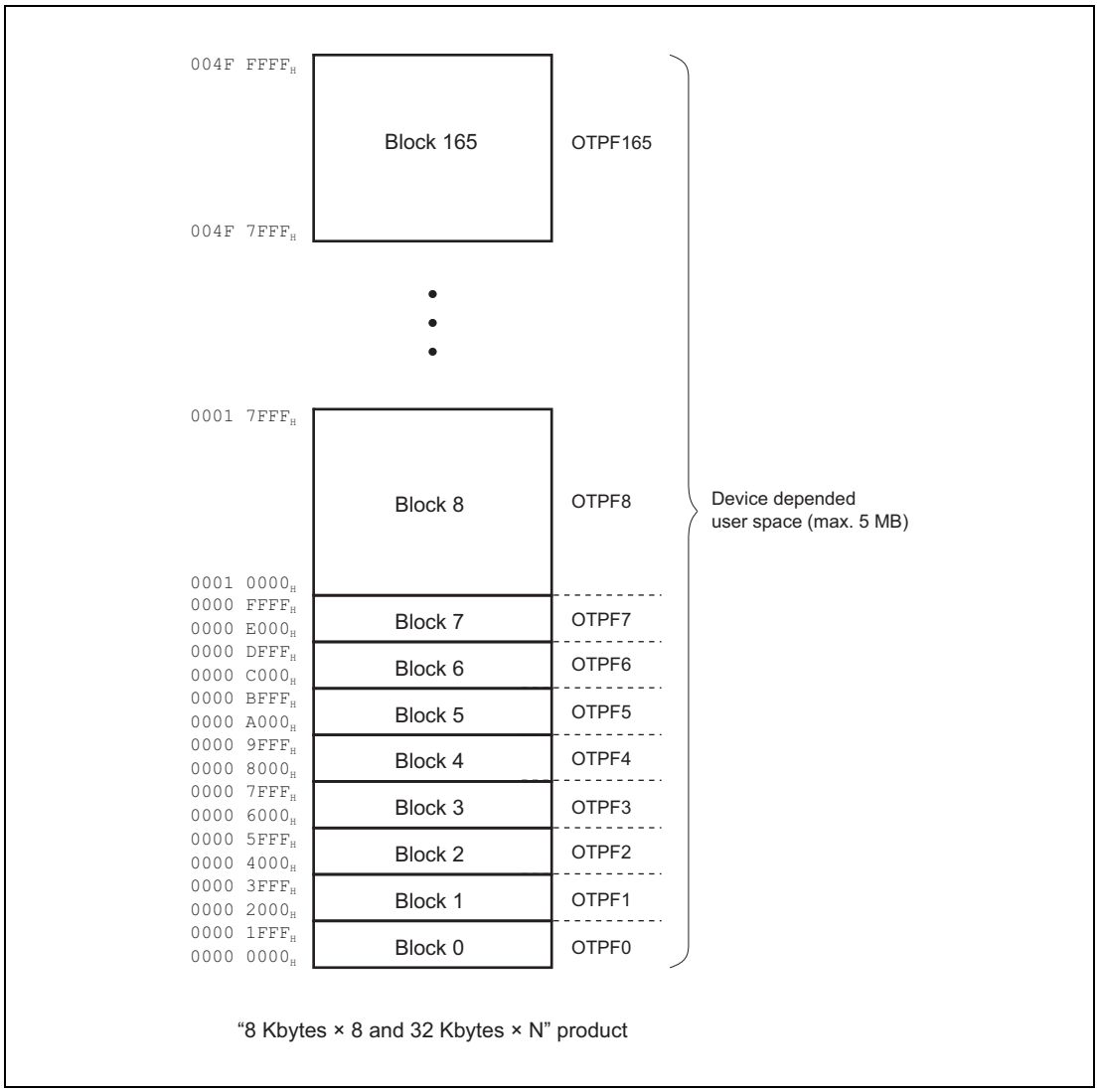


Figure 6.26 Relationship between User Area Blocks and OTP Setting Flags

Table 6.7 shows the addresses to be used for the OTP Set command. When 0 is set to a flag, OTP is set for the corresponding block. Once 0 is set to a flag, it cannot be changed to 1.

Table 6.7 Address to be Used for OTP Set Command

Address	Set Data
FF38 0090H	OTP flag for extended user area (bit 0)
FF38 0080H	Reserved area*1
FF38 0070H	Reserved area*1
FF38 0060H	Reserved area*1
FF38 0050H	Reserved area*1 (bit 127 to 38), OTPF165 (bit 37) to OTPF128 (bit 0)
FF38 0040H	OTPF127 (bit 127) to OTPF0 (bit 0)

Note 1. Do not set "0" to the reserved areas. The operation with the reserved area set to 0 is not guaranteed.

6.3.22 Reading the OTP Setting Area

When reading the OTP setting area to check the value written by “OTP Set” command, set the FCUFSEL bit in the FCUFAREA register to “1”. Setting the FCUFSEL bit to “1” disables reading of the user area. The software that reads the OTP setting area must be executed on the internal RAM. For the address map for the area of OTP settings, see **Table 6.7**.

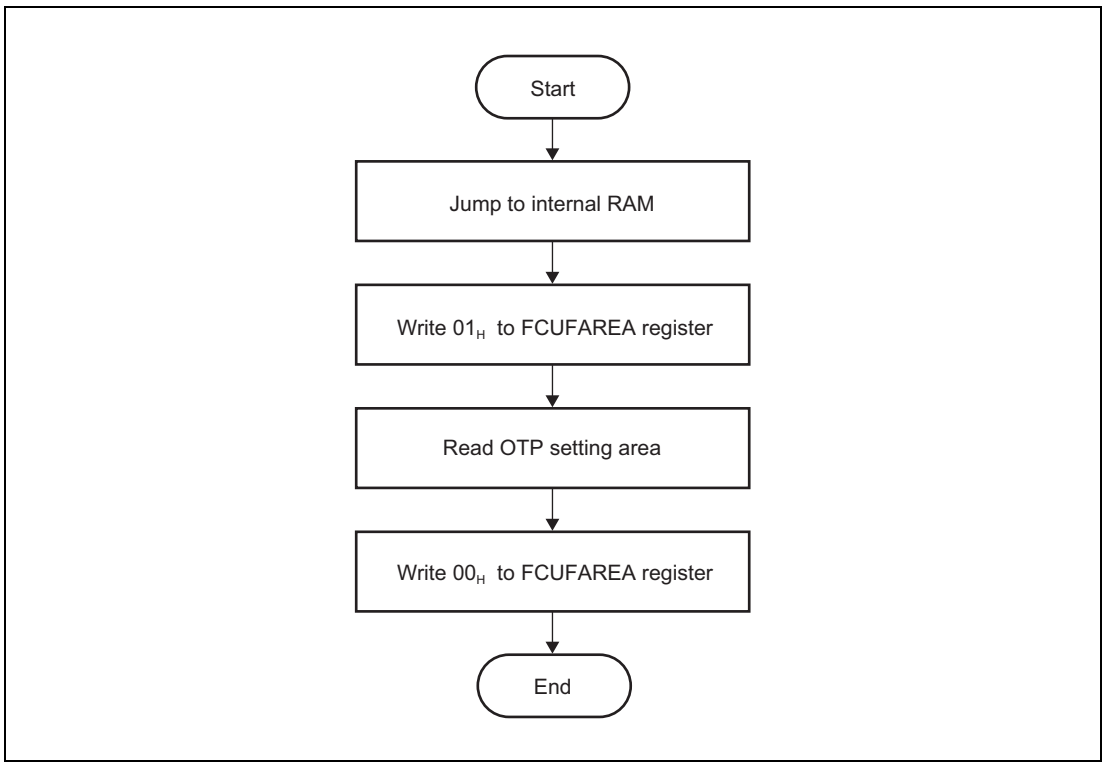


Figure 6.27 Flow of Reading the OTP Setting Area

6.3.23 Injecting ECC Errors for the Flash Memory

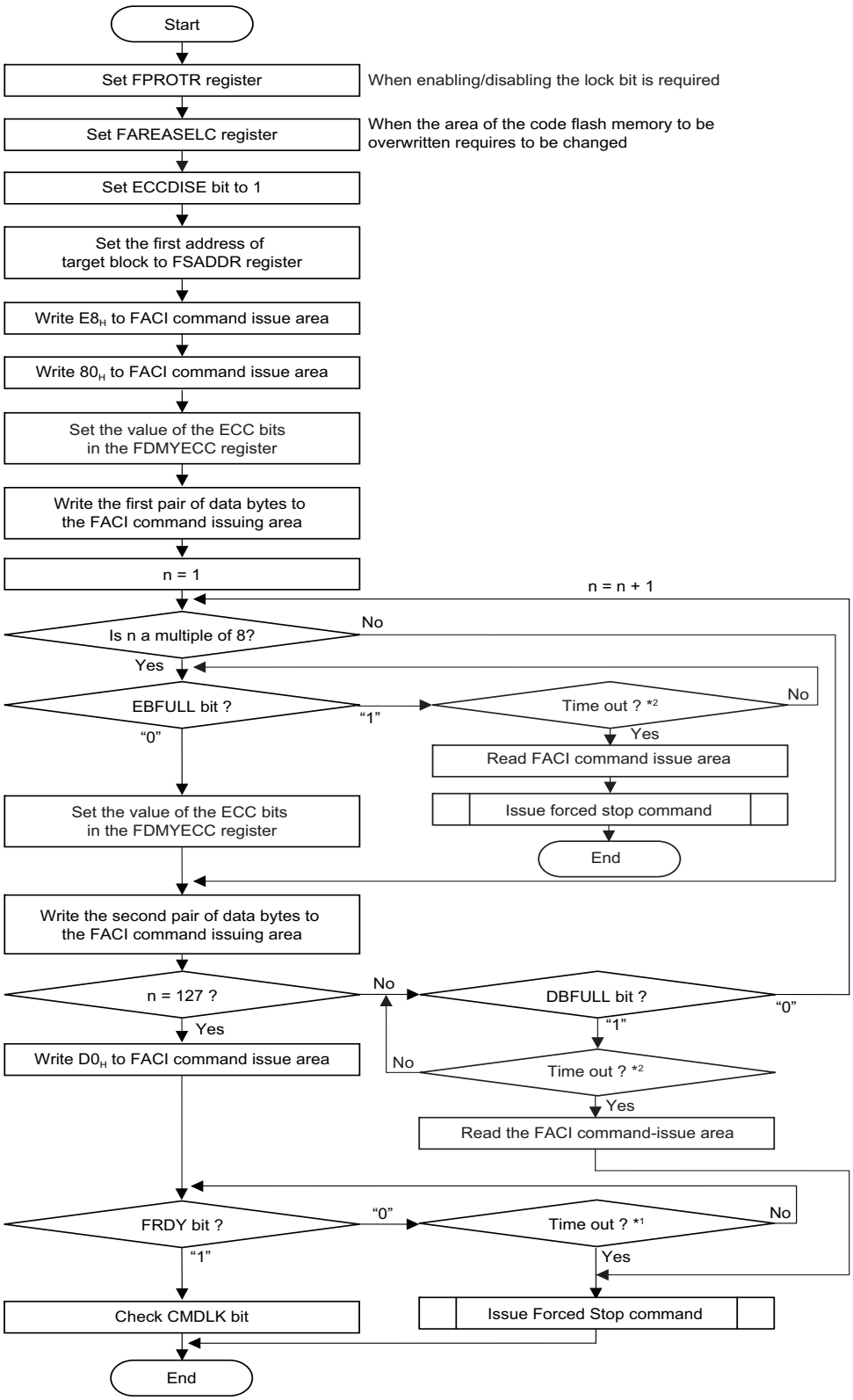
Any value of the ECC bits in the FDMYECC register can be written to the flash memory by using a programming command. Injecting an ECC error for the data area requires a four-byte programming command.

Before writing the value set in the FDMYECC register to the flash memory, set the ECCDISE bit in the FECCTMD register to 1. In addition, set the values for the ECC bits in the FDMYECC register before writing the data to the FACI command issuing area.

In the case of the code flash memory, the unit (256 bytes) for writing in response to the programming command differs from the unit (16 bytes) for which the ECC bits are to be added for the data. Therefore, every time 16 bytes of data are written to the FACI command issuing area, change the setting in the FDMYECC register.

In the case of the data flash memory, since the unit (4 bytes) for writing by the programming command is the same as that for the unit (4 bytes) of data for which the ECC bits are to be added, only change the setting in the FDMYECC register once before issuing the programming command.

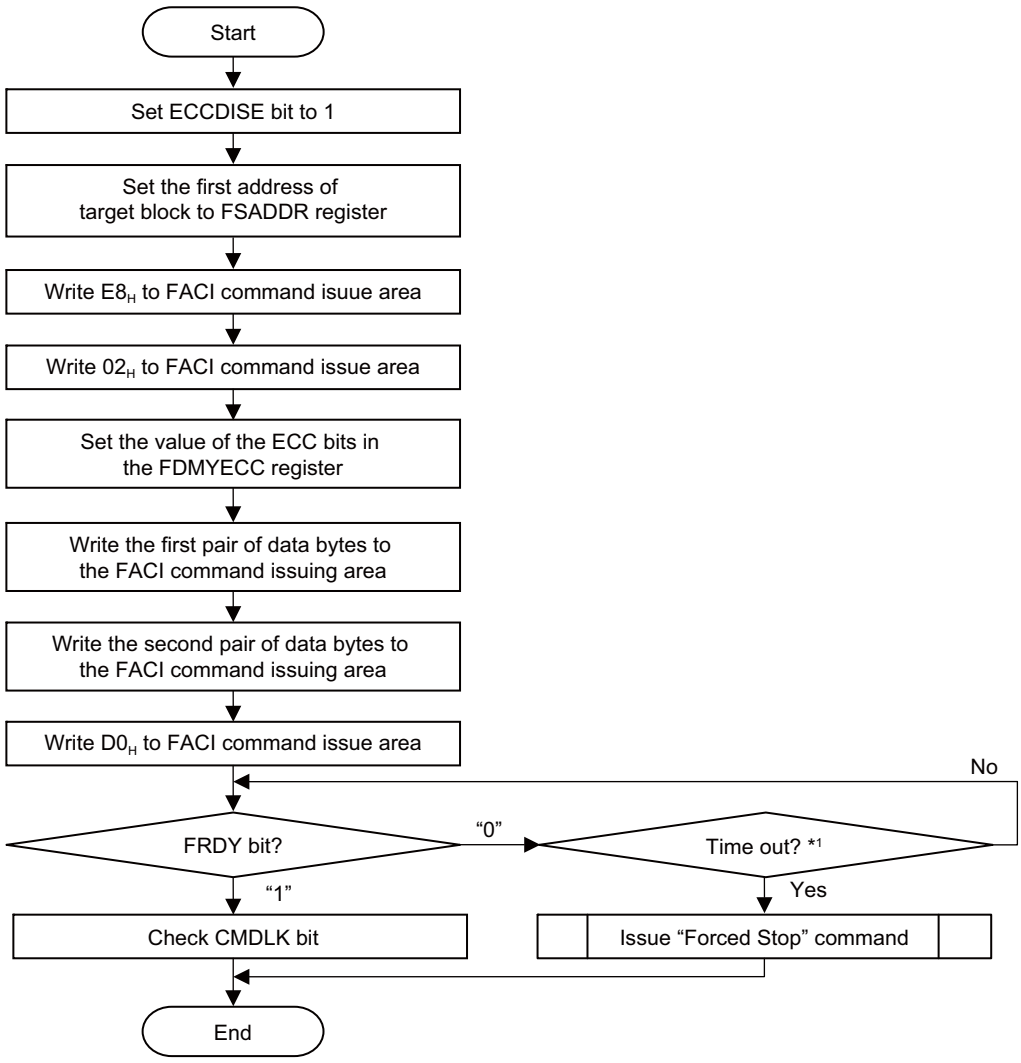
If the command for writing to the FDMYECC register is issued repeatedly while the EBFULL bit in the FSTATR register is “1”, a wait is generated in the P-Bus, which will affect performance in communication with other peripheral IP modules. To avoid the generation of such a wait, write to the FDMYECC register while the EBFULL bit in the FSTATR register is 0.



Note 1. Determined based on 1.1 times of the maximum time for 256-byte writing (see *Table 1.96 Timing Characteristics* in *Section 1.13.1 Code Flash*, in *the Electrical Target Specification*).

Note 2. Determined based on 5 µs.

Figure 6.28 Injecting an ECC Error for the Code Flash Memory



Note 1. Determined based on 1.1 times of the maximum time for 4-byte writing (see *Table 1.98 Timing Characteristics* in *Section 1.13.2 Data Flash*, in *the Electrical Target Specification*).

Figure 6.29 Injecting an ECC Error for the Data Flash Memory

Section 7 Security Function

7.1 FACI Command Protection by ID

In code flash program/erasure mode, FACI commands can be used after security is released by the ID authentication. When the FACI command is issued while the IDST bit in the SELFIDST register is set to 1 (security lock state), the flash sequencer enters the command lock state. As for the security releasing method by the ID authentication, see **Section 6.3.7, ID Authentication**.

The ID used for authentication of Code Flash P/E mode is shared with the OCD connection and serial programmer connection (when ID authentication is enabled).

In data flash program/erasure mode, FACI commands can be used regardless of the IDST bit setting.

7.2 OTP for Code Flash Memory

OTP can be set independently for each block in the code flash memory. Once an OTP is set, it cannot be canceled. If Program, Block Erase, or Lock Bit Program command is issued to an OTP set block, the flash sequencer enters the command lock state.

In the D1x products except D1M1A and D1M1-V2, the variable reset vector can be set in the corresponding area by a “Config Program” command while OTP configuration command has been executed.

In D1M1A and D1M1-V2, once an OTP configuration command has been executed for a chip, the variable reset vector cannot be set in the corresponding area by a “Config Program” command. Even when an OTP configuration command for a reserved area in the code flash memory is completed normally or execution of an OTP configuration command with all bits set to 1 is completed normally, the variable reset vector cannot be set in the corresponding area.

Section 8 Protection Function

8.1 Hardware Protection

While the low level is being input to the FLMD0 pin, the setting of the FWE bit in the FPMON register is 0. When the FWE bit is 0, writing 1 to the FENTRYC bit in the FENTRYR register is disabled. Since a transition to code flash programming/erasure mode is not possible, programming and erasing the code flash memory are prohibited. When the FRDY bit is 1 while the FLMD0 pin is at the low level, the flash sequencer clears the FENTRYC bit to disable programming and erasing of the code flash memory.

When the FLMD0 pin is changed to the low-level while the FRDY bit in the FSTATR register is 0, the flash sequencer continues processing of a command that is in progress. Even while command processing continues, however, the flash sequencer can accept requests to suspend programming and erasure.

To restart the programming or erasure, set the FENTRYC bit again and issue the programming/erasure resume command.

If the programming/erasure command is issued to the code flash memory in contradiction of protection by the FLMD0 pin, the flash sequencer enters the command lock state.

8.2 Software Protection

Software protection function disables flash sequencer command operation according to register settings or lock bit settings. If an attempt is made to issue flash sequencer command against software protection, flash sequencer enters “Command Lock” state.

8.2.1 Protection by FENTRYR

When FENTRYR register is set to “0000_H”, flash sequencer is set to read mode. In read mode, FACI commands cannot be accepted. If an attempt is made to issue FACI command in read mode, flash sequencer enters “Command Lock” state.

8.2.2 Protection by Lock Bit

Each block in user area and extended user area have lock bits. When the FPROTCN bit in the FPROTR register is 0, programming/erasing the block where the corresponding lock bit is 0 is disabled. To program/erase the block where the corresponding lock bit is 0 is disabled, set the FPROTCN bit to 1. If an attempt is made to issue program/block erase/lock bit program command against protection by lock bits, the flash sequencer enters the command lock state.

8.3 Error Protection

Error protection function detects an illegal FACI command issued, an illegal access, or a flash sequencer malfunction, and disables FACI command acceptance (“Command Lock” state). While flash sequencer is in “Command Lock” state, flash memory cannot be programmed or erased. To cancel “Command Lock” state, issue “Status Clear” or “Forced Stop” command while the CFAE and DFAE bits in the FASTAT register is “0”. “Status Clear” command can be used only when FRDY bit is “1”. “Forced Stop” Command can be used regardless of FRDY bit value. While the CMDLKIE bit in FAEINT register is “1”, flash access error (FLERR) interrupt is generated if flash sequencer enters “Command Lock” state (FASTAT.CMDLK = 1).

If flash sequencer enters “Command Lock” state during programming or erasure processing by the command other than Program/Erasure suspend, the flash sequencer continues programming or erasure processing, In this state, programming or erasure processing cannot be suspended by the Program/ Erasure suspend command. If a command is issued in “Command Lock” state, ILGLERR bit becomes “1” and the other bits retain the values set due to the previous error detection.

Table 8.1 shows error protection types and status bit values after error detection.

Table 8.1 Error Protection Type (1/2)

Error Type	Description	OTPDTCT	ILGLERR	ERSERR	PRGERR	CFGDTCT	TBLDTCT	FRDTCT	CFAE	DFAE
FENTRYR setting error	The value set in FENTRYR is not 0000_H, 0001_H, or 0080_H.	0	1	0	0	0	0	0	0	0
	The FENTRYR setting for resuming operation does not match that for suspending operation.	0	1	0	0	0	0	0	0	0
Illegal command error	An undefined code has been written in the first access of FACI command.	0	1	0	0	0	0	0	0	0
	The value specified in the last access of the multiple-access FACI command is not $D0_H$ (except for “DMA Program”).	0	1	0	0	0	0	0	0	0
	The value (N) specified in the second write access of FACI command in the “Program”, “DMA Program”, “Config Program”, or “OTP Set” command is wrong (odd number is wrong for “DMA Program”).	0	1	0	0	0	0	0	0	0
	“Blank Check” command has been issued with inconsistent BCDIR, FSADDR, and FEADDR settings. (See **Section 4.6, FACI Command End Address Register (FEADDR)**.)	0	1	0	0	0	0	0	0	0
	FACI command has been issued against FACI command not acceptable mode. (See **Table 6.3**.)	0	1	0	0	0	0	0	0	0
	FACI command has been issued when command acceptance conditions are not satisfied. (See **Table 6.4**)	0/1	1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Erase error	An error has occurred during flash memory erasure.	0	0	1	0	0	0	0	0	0
	“Block Erase” command has been issued against lock bit protection.	0	0	1	0	0	0	0	0	0
Program error	An error has occurred during flash memory program.	0	0	0	1	0	0	0	0	0
	“Program” or “Lock Bit Program” command has been issued against lock bit protection.	0	0	0	1	0	0	0	0	0
FCURAM ECC error	A 2-bit error has been detected when FCURAM is read.	0	0	0	0	0	0	1	0	0
Code flash access error	FACI command has been issued to reserved user area in code flash program/erasure mode. (See **Section 4.2, Flash Access Status Register (FASTAT)**).	0	1	0	0	0	0	0	1	0
	FACI command has been issued to reserved extended user area in code flash program/erasure mode. (See **Section 4.2, Flash Access Status Register (FASTAT)**).	0	1	0	0	0	0	0	1	0
Data flash access error	FACI command has been issued to reserved data area in data flash program/erasure mode. (See **Section 4.2, Flash Access Status Register (FASTAT)**).	0	1	0	0	0	0	0	0	1
	“Config Program” command has been issued to reserved area. (See **Section 4.2, Flash Access Status Register (FASTAT)**).	0	1	0	0	0	0	0	0	1
	“OTP Setting” command has been issued to reserved area. (See **Section 4.2, Flash Access Status Register (FASTAT)**).	0	1	0	0	0	0	0	0	1

Table 8.1 Error Protection Type (2/2)

Error Type	Description	OTPDTCT	ILGLERR	ERSERR	PRGERR	CFGDTCT	TBLDTCT	FRDTCT	CFAE	DFAE
Security	“Program”, “Block Erase”, or “Lock Bit Program” command has been issued against OTP setting.	0	1	0	0	0	0	0	0	0
	“Config Program” command was issued for the variable reset vector due to OTP being set for the code flash memory.	0	0/1 *1	0	0	0	0	0	0	0
	FACI command has been issued in code flash program/erasure mode against security not-released state by ID authentication.	0	1	0	0	0	0	0	0	0
Other	FACI command issue area has been accessed in read mode.	0	1	0	0	0	0	0	0	0
	FACI command issue area has been read in code flash program/ erasure mode or data flash program/erasure mode.	0	1	0	0	0	0	0	0	0
OTP Set ECC error	A 2-bit error has been detected when OTP setting is read.	1	0	0	0	0	0	0	0	0
Config Program ECC error	2-bit error has been detected when Config Program value is read.	0	0	0	0	1	0	0	0	0
Overwrite parameter ECC error	2-bit error has been detected when overwrite parameter table is read.	0	0	0	0	0	1	0	0	0

Note 1. Other than D1M1A and D1M1-V2: 0
D1M1A and D1M1-V2: 1

8.3.1 Variable Reset Vector

Using a “Config Program” command to change the value of the variable reset vector area may change the reset vector of the CPU. Using the variable reset vector when the boot program in the code flash memory is updated makes safe rewriting possible.

In the D1x products except D1M1A and D1M1-V2, the variable reset vector can be set in the corresponding area by a “Config Program” command while OTP configuration command has been executed.

In D1M1A and D1M1-V2, once an OTP configuration command has been executed for a chip, the variable reset vector cannot be set in the corresponding area by a “Config Program” command. Even when an OTP configuration command for a reserved area in the code flash memory is completed normally or execution of an OTP configuration command with all bits set to 1 is completed normally, the variable reset vector cannot be set in the corresponding area.

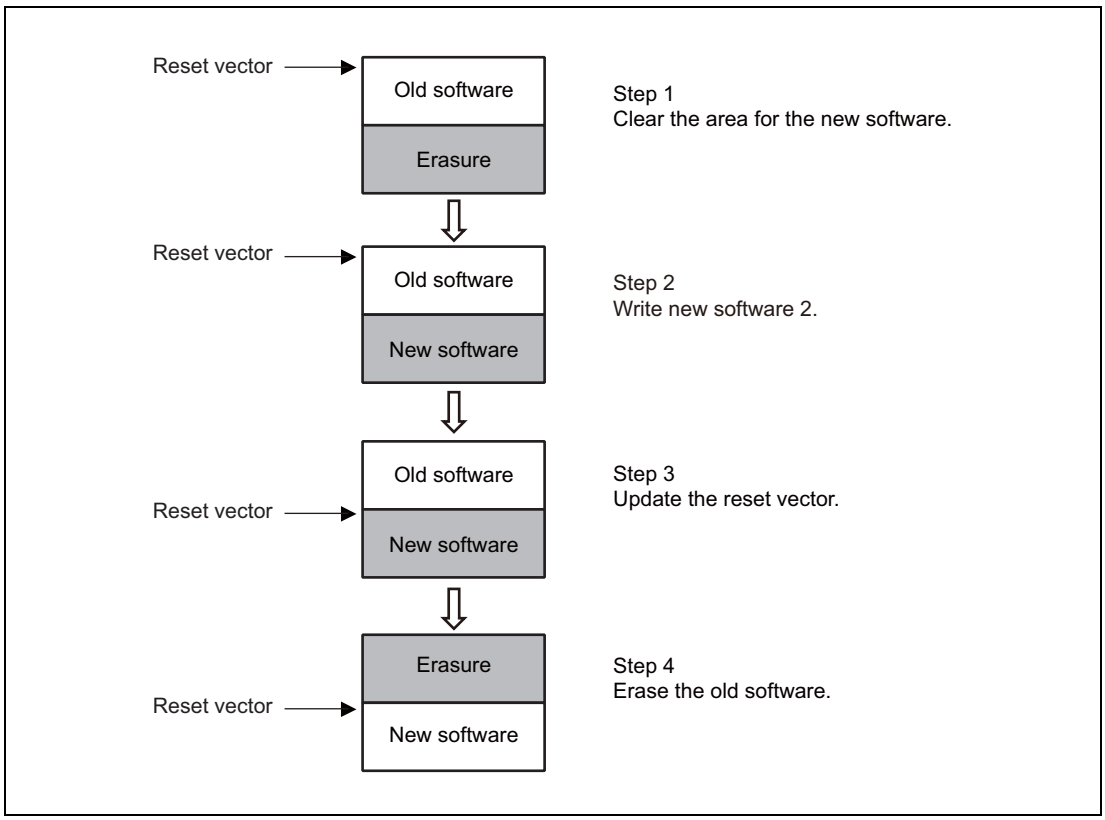


Figure 8.1 Software Update using the Variable Reset Vector

8.4 Blank Checking of Code Flash Memory

Reading from an area of the code flash memory that has been erased but to which no new data has been written (an area in the non-written state) leads to an exception since an ECC error will be detected. In addition, as the values of the data are not guaranteed when an ECC error has occurred, confirm that the area is in the non-written state by checking whether all data bits and ECC bits for the code flash memory are set to 1. For usage notes on the ECC function for the code flash memory, see the section on safety features in the user's manual for the given product.

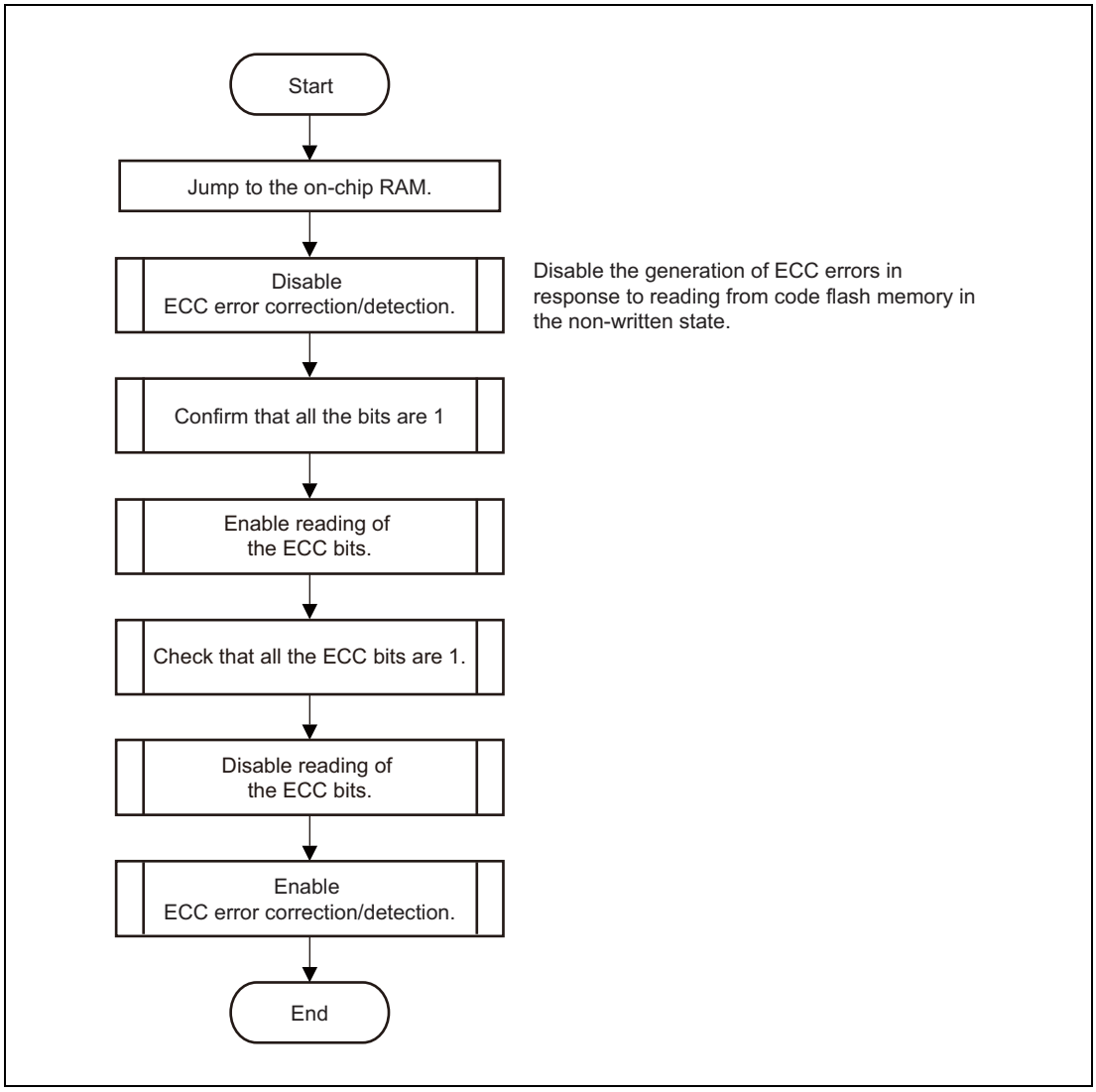


Figure 8.2 Blank Checking of Code Flash Memory

Section 9 Usage Notes

(1) Reading areas where programming or erasure was interrupted

When programming or erasure of an area of flash memory is interrupted, the data stored in the area become undefined. To avoid undefined data that are read out becoming the source of faulty operation, take care not to fetch instructions or read data from areas where programming or erasure was interrupted.

(2) Prohibition of additional write

Writing the same area more than once is prohibited. To write again the flash memory area where data has already been written to, be sure to erase the corresponding area in advance.

(3) Reset during program/erasure

In the case generated a reset by the $\overline{\text{RESET}}$ pin during program/erasure, release the reset after the reset input period of at least the minimum low-level width of the $\overline{\text{RESET}}$ input signal, within the operating voltage range specified by electrical characteristics.

(4) Interrupt/exception vector allocation during program/erasure

When an interrupt/exception is generated during program/erasure, vector fetch may be generated from the code flash memory. Under the condition where the BGO function is not used, set the address of vector fetch to the area other than code flash memory. For how to change the vector address of the exception handler, see "*RH850G3M User's Manual: Software*".

(5) Abnormal termination during program/erasure

Even if programming/erasure ends abnormally due to the generation of an external reset or power shutoff, the programming/erasure state of the flash memory with undefined data cannot be verified or checked. For the area where programming/erasure ends abnormally, the blank check function cannot judge whether the area is erased successfully or not. Erase the area again to prove that the corresponding area is completely erased before using.

If programming and erasure of code flash memory are not completed normally, the lock bit for the target area may be enabled (locked). In such cases, erase the block to erase the lock bit while the lock bit is in the disabled state (the area is not locked).

(6) Prohibition during program/erasure/blank checking

Do not perform the following operations during program/erasure/blank checking.

- Set the power supply voltage outside the operating voltage range.

(7) Update of FCUFAREA register

When setting FCUFAREA register and switching CodeFlash areas, it is necessary to synchronize process before and after that and a switching CodeFlash areas. Synchronization flows for updating FCUFAREA register in 3 cases are as below.

(a) Synchronization process for updating FCUFAREA register

When FCUFAREA register is updated, it is necessary to wait for completion of FCUFAREA register update before read instruction to CodeFlash or FCU firmware storage area (LD.W, etc.). To ensure that, after updating FCUFAREA register, "Execute dummy read of FCUFAREA register first, and next SYNCP instruction", then insert read instruction.

(b) Synchronization process before switching to CodeFlash user area/extended user area

For switching to CodeFlash areas after completion of reading FCU firmware storage area, after final read instruction of FCU firmware storage area (LD.W, etc.), with executing SYNCP instruction, rewrite FCUFAREA register in the procedure noted above (a).

(c) Synchronization process after switching to CodeFlash user area/extended user area

In order to avoid code execution of CodeFlash read before the switching, “Execute dummy read of FCUFAREA register first, next SYNCP instruction, finaly SYNCI instruction”, after updating FCUFAREA register but before executing CodeFlash instruction.
In addition, after switching areas of Code Flash, clear instruction cache and data buffer.

(8) Notes on selecting the FCU firmware storage area

To transfer the FCU firmware, and read the configuration setting area and the OTP setting area, set the FCUFAREA register to select the FCU firmware storage area. When selecting the FCU firmware storage area, prevent access to the FCU firmware storage area due to interrupts by placing the vector addresses of the exception handlers for the CPU in the on-chip RAM. For changing the vector addresses of the exception handlers, see “*RH850G3M User’s Manual: Software*”.

(9) Maintenance of coherency after the code flash memory is overwritten

When executing an instruction for the code flash memory after the code flash memory area is overwritten, clear the instruction cache and clear the data buffer, in order to maintain coherency (see *Usage Notes* in *the section of the CPU system* in *the User’s Manual: Hardware*).

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Rev.	Date	Description	
		Page	Summary
0.40	Sep 04, 2014	—	First Edition issued
1.00	Apr 10, 2015	Section 4 Registers	
		11, 12	Table 4.2 FASTAT Register Contents, description of the CFAE bit and DFAE bit corrected, Note 2 added.
		16	4.6 FACI Command End Address Register (FEADDR), description corrected
		17	Table 4.7 FCURAME Register Contents, description of the KEY[7:0] bits and FRAMTRAN bit corrected
		18	4.8 Flash Status Register (FSTATR), bit 7 in the bit chart changed to a reserved bit
		19, 21	Table 4.8 FSTATR Register Contents, bit 7 changed to a reserved bit, description of the reserved bits, description of the EBFULL bit, ERSERR bit, TBLDTCT bit, and the TBLCRCT bit corrected
		23	4.9 Flash P/E Mode Entry Register (FENTRYR), description corrected
		24	Table 4.9 FENTRYR Register Contents, description of the FENTRYC bit corrected
		25	Table 4.10 FPROTR Register Contents, description of the FPROTCN bit corrected
		27	Table 4.12 FLKSTAT Register Contents, description of the FLOCKST bit corrected
		28	4.13 FCURAM First Error Address Register (FRFSTEADR), value after reset of bit 15 in the bit chart corrected (1 → 0)
		35	Table 4.21 FBCSTAT Register Contents, description of the BCST bit corrected, Note 1 added
		36	Table 4.22 FPSADDR Register Contents, erroneous bit position of the PSADR[18:0] bit corrected
		37	4.22 Flash Sequencer Process Switch Register (FCPSR), description corrected
		38	Table 4.24 FPCKAR Register Contents, description of the PCKA[7:0] bits corrected.
		44	4.29 FCU Firmware Area Select Register (FCUFAREA), value after reset of bits 5 and 4 in the bit chart corrected (1 → 0), description of Note 1 corrected
		45	4.30 Self-Programming ID Input Registers (SELFID0 to SELFID3), R/W of bits 1 and 0 in the bit chart corrected (R → R/W)
		Section 6 FACI Command	
		48	Table 6.1 List of FACI Commands, corrected
		49	Table 6.2 Flash Sequencer Command Format, corrected, Note 2 added
		50	6.2 Relationship between Flash Sequencer Status and FACI Commands, description corrected
		50	Table 6.3 Flash Sequencer Operation Mode and Available Commands, corrected
		52	Figure 6.1 Overview of Command Usage in Code Flash Program/Erasure Mode, corrected
		53	Figure 6.2 Overview of Command Usage in Data Flash Program/Erasure Mode, corrected
		54	6.3.3 FCU Firmware Transfer, description corrected
		58	Figure 6.7 Flow of Shift to Read Mode, corrected
		59	6.3.7 ID Authentication, description corrected
		60	6.3.8 Return from Command Lock State, description corrected
		61	Figure 6.9 Return from Command Lock State, corrected
		63	Figure 6.10 Program Command Usage, corrected
		64	Figure 6.11 DMA Program Command Usage, corrected
		65	Figure 6.12 Block Erase Command Usage, corrected
		67	Figure 6.13 "Program/Erasure Suspend" Command Usage, corrected
		68	6.3.12 Program/Erasure Suspend Command, (1) Suspend program command, description corrected
		69	6.3.12 Program/Erasure Suspend Command, (2) Suspend erase command in suspension-priority mode, description corrected
		69	Figure 6.15 Suspend "Erase" Command (Suspension-Priority Mode), corrected
		71	Figure 6.17 "Program/Erasure Resume" Command Usage, corrected

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1.00	Apr 10, 2015	70	6.3.12 Program/Erasure Suspend Command, (3) Suspend erase command in erasure-priority mode, description corrected
		70	Figure 6.16 Suspend “Erase” Command (Erasure-Priority Mode), corrected
		73	6.3.15 Forced Stop Command, description corrected
		74	6.3.16 Blank Check Command, description corrected
		75	Figure 6.20 “Blank Check” Command Usage, corrected
		76	Figure 6.21 “Config Program” Command Usage, corrected
		78	6.3.18 Reading the Configuration Setting Area, description corrected
		78	Figure 6.22 Flow of Reading of the Configuration Setting Area, corrected
		82	6.3.21 OTP Set Command, description corrected
		82	Figure 6.26 Relationship between User Area Blocks and OTP Setting Flags, corrected
		82	Table 6.7 Address to be Used for OTP Set Command, corrected
		79	6.3.19 Lock Bit Program Command, description corrected
		85	Figure 6.28 Injecting an ECC Error for the Code Flash Memory, corrected
			Figure 6.29 Injecting an ECC Error for the Data Flash Memory, corrected
		Section 8 Protection Function	
		89	8.3 Error Protection, description corrected
		89, 90	Table 8.1 Error Protection Type, corrected (“FCUERR” column deleted)
		Section 9 Usage Notes	
		93	(3) Reset during program/erasure, description corrected
		93	(4) Interrupt/exception vector allocation during program/erasure, description corrected
		93	(5) Abnormal end during program/erasure, description corrected
		93, 94	(8) Notes on selecting the FCU firmware storage area, description added
		94	(9) Maintenance of coherency after the code flash memory is overwritten, description corrected
1.10	May 31, 2017	Section 2 Module Configuration	
		7	Description of “(FACI reset transfer)” added, description changed by additional line-up (D1M1A)
		7	Figure 2.1 Configuration of Flash Memory Related Modules: Changed by additional line-up (D1M1A)
		Section 3 Address Map	
		8	Table 3.1 Information on the Hardware Interface Area: Changed by additional line-up (D1M1A), PBUS group and module name added
		Section 4 Registers	
		11, 12	Table 4.2 FASTAT Register Contents: Erroneous functional description on bit 4 (CMDLK) corrected, functional description on bit 0 (ECRCT) changed by additional line-up (D1M1A)
		13	4.3 Flash Access Error Interrupt Enable Register (FAEINT): Description added
		13	Table 4.3 FAEINT Register Contents: Functional description on bit 0 (ECRCTIE) changed by additional line-up (D1M1A)
		14	4.4 Code Flash Memory Area Select Register (FAREASELC): Note 1 in a bit chart corrected
		15	Table 4.5 FSADDR Register Contents: Functional description on bits 31 to 0 (FSADDR[31:0]), corrected
		17	4.7 FCURAM Enable Register (FCURAME): Description changed by additional line-up (D1M1A), erroneous Note 1 in a bit chart corrected
		19, 22	Table 4.8 FSTATR Register Contents: Functional description on bit 15 (FRDY) and bit 1 (FRDTCT), corrected
		23	4.9 Flash P/E Mode Entry Register (FENTRYR): Description and Note 1 in a bit chart, corrected
		25	4.10 Code Flash Protect Register (FPROTR): Note 1 in a bit chart corrected
		26	4.11 Flash Sequencer Set-Up Initialize Register (FSUINITR): Note 1 in a bit chart corrected
		28	4.13 FCURAM First Error Address Register (FRFSTEADR): Description changed by additional line-up (D1M1A)
		29	Table 4.14 FRTSTAT Register Contents: Functional description on bit 0 (RTECRCT), corrected

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		Page	Summary
1.10	May 31, 2017	30	4.15 FACI Reset Transfer Error Interrupt Enable Register (FRTEINT): Description added
		32	4.17 FCURAM ECC Control Register (FRAMECCR): Description changed by additional line-up (D1M1A), erroneous Note 1 in a bit chart corrected
		37	Table 4.23 FCPSR Register Contents: Table title corrected
		38	4.23 Flash Sequencer Processing Clock Notify Register (FPCKAR): Note 1 in a bit chart corrected
		41	4.26 Flash ECC Encoder Monitor Register (FECCEMON): Description and bit 9 in a bit chart, corrected
		41	Table 4.27 FECCEMON Register Contents: Bit name of bit 9 deleted
		42	4.27 Flash ECC Test Mode Register (FECCTMD): Note 1 in a bit chart corrected
		42	Table 4.28 FECCTMD Register Contents: Functional description on bit 0 (ECCDISE), corrected
		43	4.28 Flash Dummy ECC Register (FDMYECC): Description corrected, bit name and R/W (bit 9) corrected
		43	Table 4.29 FDMYECC Register Contents (in Code Flash Program/Erasure Mode): Bit name of bit 9 deleted
		43	Table 4.30 FDMYECC Register Contents (in Data Flash Program/Erasure Mode): Bit name of bit 9 deleted
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		49	Table 6.2 Flash Sequencer Command Format: Corrected
		53	Figure 6.2 Overview of Command Usage in Data Flash Program/Erasure Mode: Corrected
		54	6.3.3 FCU Firmware Transfer (Only FCURAM Devices): Section title and description changed by additional line-up (D1M1A)
		57	Figure 6.5 Flow of Shift to Code Flash Program/Erasure Mode: Corrected
		63	Figure 6.10 Program Command Usage: Corrected
		64	6.3.10 DMA Program Command: Description corrected
		64	Figure 6.11 DMA Program Command Usage: Corrected
		66	6.3.12 Program/Erasure Suspend Command: Description corrected
		67	Figure 6.13 “Program/Erasure Suspend” Command Usage: Corrected
		69	(2) Suspend erase command in suspension-priority mode: Corrected
		69	Figure 6.15 Suspend “Erase” Command (Suspension-Priority Mode): Corrected
		71	6.3.13 Program/Erasure Resume Command: Description corrected
		73	Figure 6.19 “Forced Stop” Command Usage: Corrected
		74	6.3.16 Blank Check Command: Description corrected
		75	Figure 6.20 “Blank Check” Command Usage: Corrected
		76	Figure 6.21 “Config Program” Command Usage: Corrected
		79	6.3.19 Lock Bit Program Command: Description corrected
		81	Figure 6.25 “OTP Set” Command Usage: Corrected
		84	6.3.23 Injecting ECC Errors for the Flash Memory: Description corrected
		85	Figure 6.28 Injecting an ECC Error for the Code Flash Memory: Corrected
		Section 7 Security Function	
		87	7.2 OTP for Code Flash Memory: Description amended
		Section 8 Protection Function	
		89, 90	Table 8.1 Error Protection Type: Corrected
		91	8.3.1 Variable Reset Vector: Description amended
		92	8.4 Blank Checking of Code Flash Memory: Description corrected
		92	Figure 8.2 Blank Checking of Code Flash Memory: Corrected
		Section 9 Usage Notes	
		93	(1) Reading from area where program/erasure is suspended: Description corrected
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		93	(5) Abnormal termination during program/erasure: Description corrected
		93	(6) Prohibition during program/erasure/blank checking: Section title and description, amended
		93, 94	(7) Update of FCUFAREA register: Description corrected
		94	(8) Notes on selecting the FCU firmware storage area: Description corrected

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