User's Manual

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RH850/C1M-A

Flash Memory

User's Manual: Hardware Interface

Renesas microcontroller

Renesas Electronics
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Notes for CMOS devices

(1) Voltage application wafeform at input pin:

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) Handling of unused input pins:

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) Precaution against ESD:

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) Status before initialization:

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) Power ON/OFF sequence:

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) Input of signal during power off state:

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

Table of Contents

Section 1 Features

The features of the flash memory are described below. See the user's manual for information on the capacity, block configuration, and addresses of the flash memory in a given product.

Flash Memory Programming/Erasure

A dedicated sequencer for the flash memory (flash sequencer) executes programming and erasure via the peripheral bus. The flash sequencer also supports the program/processing suspend/resume and BGO (background operation)*1.

Note 1. This can be used during overwriting of the data flash memory and reading of the code flash memory.

Security Functions

The flash memory incorporates hardware functions to prevent illicit tampering.

Protection Functions

The flash memory incorporates hardware functions to prevent erroneous writing.

Interrupts

The flash memory supports an interrupt to indicate completion of processing by the flash sequencer and an error interrupt to indicate erroneous operations.

DMA

The flash memory supports DMA writing to the data flash memory.

Section 2 Module Configuration

Modules related to the flash memory are configured as shown in **Figure 2.1**. The flash sequencer is configured of the FCU and FACI. The FCU executes basic control of overwriting of the flash memory. The FCURAM is RAM for the storage of firmware to control execution by the FCU. The FACI receives FACI commands via the peripheral bus and controls FCU operations accordingly.

In the transfer operations in response to a reset, the FACI transfers the data from flash memory to the option byte storage registers in the ID control section (FACI reset transfer). The ID control section compares the ID transferred to the flash memory with the value in the SELFID0 to SELFID3 registers. Data set in the option bytes of the flash memory can be read out from the option byte storage registers via the peripheral bus.

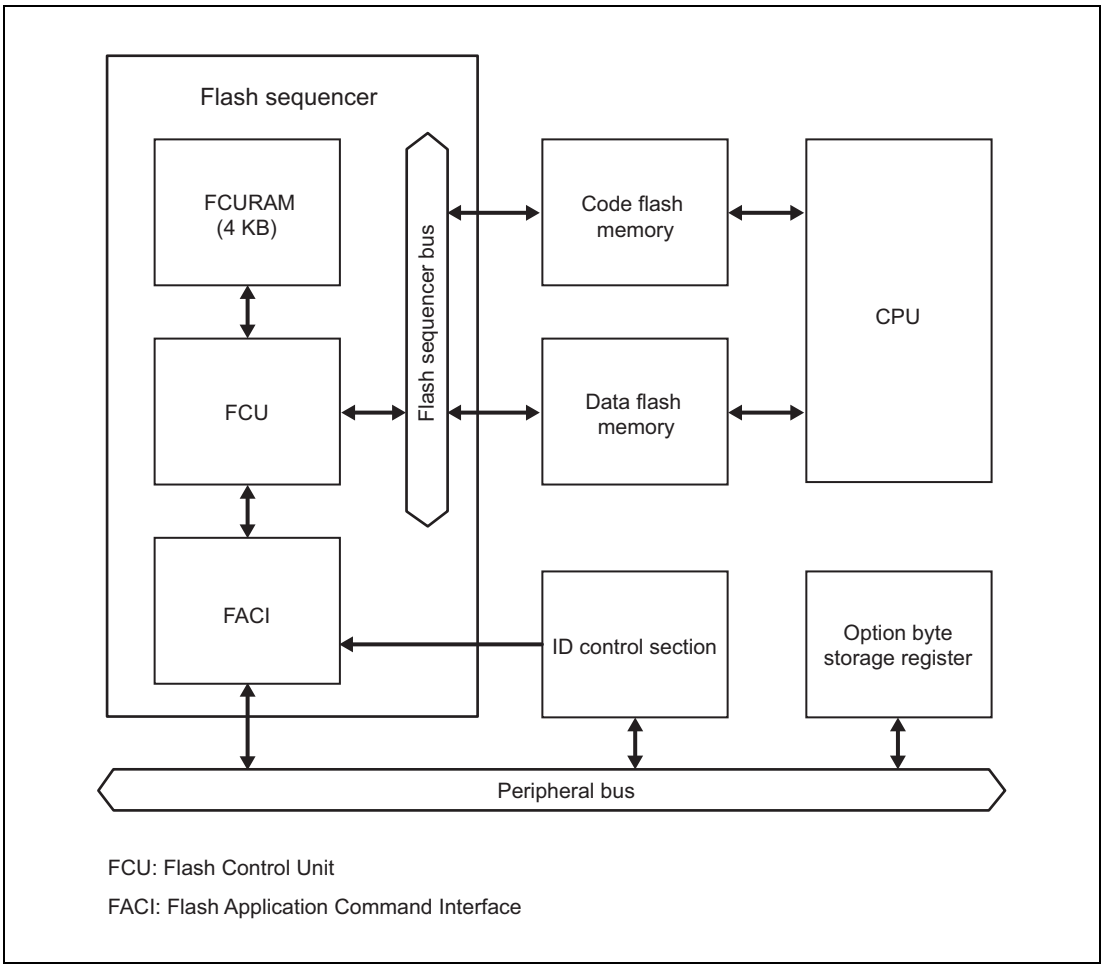


Figure 2.1 Configuration of Flash Memory Related Modules

Section 3 Address Map

When reading the areas for configuration settings, and for OTP settings set the FCUFSEL bit in the FCUFAREA register to 1. Address of the area where the FCU firmware is stored depends on the value of the FCUFSEL bit. **Table 3.1** gives information on all of these areas.

Table 3.1 Information on the Hardware Interface Area

Area	Address	Capacity	Peripheral Group
Area containing the various registers of the hardware	See Section 4, Registers	See Section 4, Registers	*1
FACI command-issuing area	FFA2 0000_H	4 bytes	3
Area for storage of the FCU firmware	$0001\ 7000_H$ to $0001\ 7FFF_H$ (When FCUFAREA.FCUFSEL = 1_B) $0103\ 7000_H$ to $0103\ 7FFF_H$ (When FCUFAREA.FCUFSEL = 0_B)	4 Kbytes	—
FCURAM area	FFA1 2000_H to FFA1 $2FFF_H$	4 Kbytes	3
Configuration setting area	FF30 0040_H to FF30 $008F_H$	80 bytes	0
OTP setting area	FF38 0040_H to FF38 $009F_H$	96 bytes	0

Note 1. For the relationship between the peripheral groups and modules, see *Section 3.1.2, Configuration of Peripheral Groups* in *the RH850/C1M-A User's Manual: Hardware*.

See the user's manual for information on the addresses of the flash memory etc.

Section 4 Registers

This section gives information on the registers. For registers that are not specifically mentioned, only reset them to their initial states.

For information on the registers that are accessed when the self-programming library is used, including option byte storage registers, see the user's manual of each product.

Table 4.1 lists the registers related to flash memory.

Table 4.1 Flash Memory Related Registers

Module	Register	Symbol	Address
FACI	Flash access status register	FASTAT	FFA1 0010$_H$
FACI	Flash access error interrupt enable register	FAEINT	FFA1 0014$_H$
FACI	FACI command start address register	FSADDR	FFA1 0030$_H$
FACI	FACI command end address register	FEADDR	FFA1 0034$_H$
FACI	FCURAM enable register	FCURAME	FFA1 0054$_H$
FACI	Flash status register	FSTATR	FFA1 0080$_H$
FACI	Flash programming/erasure mode entry register	FENTRYR	FFA1 0084$_H$
FACI	Code flash protect register	FPROTR	FFA1 0088$_H$
FACI	Flash sequencer set-up initialize register	FSUINITR	FFA1 008C$_H$
FACI	Lock bit status register	FLKSTAT	FFA1 0090$_H$
FACI	FCURAM first error address register	FRFSTEADR	FFA1 0094$_H$
FACI	FACI reset transfer status register	FRTSTAT	FFA1 0098$_H$
FACI	FACI reset transfer error interrupt enable register	FRTEINT	FFA1 009C$_H$
FACI	FACI command register	FCMDR	FFA1 00A0$_H$
FACI	Flash programming/erasure status register	FPESTAT	FFA1 00C0$_H$
FACI	Data flash blank check control register	FBCCNT	FFA1 00D0$_H$
FACI	Data flash blank check status register	FBCSTAT	FFA1 00D4$_H$
FACI	Data flash programming start address register	FPSADDR	FFA1 00D8$_H$
FACI	Flash sequencer processing switch register	FCPSR	FFA1 00E0$_H$
FACI	Flash sequencer processing clock notify register	FPCKAR	FFA1 00E4$_H$
FACI	Flash ECC encoder monitor register	FECCEMON	FFA1 0100$_H$
FACI	Flash ECC test mode register	FECCTMD	FFA1 0104$_H$
FACI	Flash dummy ECC register	FDMYECC	FFA1 0108$_H$
FACI	FCU firmware area select register	FCUFAREA	FFC5 9008$_H$
FLASH	Self-programming ID input register 0	SELFID0	FFA0 8000$_H$
FLASH	Self-programming ID input register 1	SELFID1	FFA0 8004$_H$
FLASH	Self-programming ID input register 2	SELFID2	FFA0 8008$_H$
FLASH	Self-programming ID input register 3	SELFID3	FFA0 800C$_H$
FLASH	Self-programming ID authentication status register	SELFIDST	FFA0 8010$_H$

4.1 FASTAT — Flash Access Status Register

FASTAT indicates access error status for code/data flash. If either of CFAE/CMDLK/DFAE bits in FASTAT is set to 1, the flash sequencer enters the command-locked state. To release the sequencer from the command-locked state, set the CFAE and DFAE bits in the FASTAT register to 0, and then issue a “Status Clear” or a “Forced Stop” command to FACI.

Access: This register can be read/written in 8-bit units.

Address: FFA1 0010_H

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	CFAE	—	—	CMDLK	DFAE	—	—	ECRCT
Value after reset	0	0	0	0	0	0	0	0
R/W	R/W*1	R	R	R	R/W*1	R	R	R

Note 1. Only “0” can be written to clear flag after “1” is read.

Table 4.2 FASTAT Register Contents (1/2)

Bit Position	Bit Name	Function
7	CFAE	Code Flash Access Error Indicates whether or not code flash access error has been generated. If this bit becomes “1”, ILGLERR bit in FSTATR is set to “1” and flash sequencer enters the command-locked state. 0: No code flash access error has occurred. 1: Code flash access error has occurred. [Setting condition] An FACI command with the following setting having been issued in code flash programming and erasure mode: The setting for bits 23 to 0 in FSADDR is for an address in the reserved portion of the user area, i.e. is in the range from 40_0000_H to FF_FFFF_H. [Clearing condition] “0” is written after reading “1” from this bit.
6, 5	Reserved	When read, the value after reset is read. When writing, write the value after reset.
4	CMDLK	Command Lock Indicates whether flash sequencer is in the command-locked state. 0: Flash sequencer is not in the command-locked state. 1: Flash sequencer is in the command-locked state. [Setting condition] Flash sequencer detects error and enters the command-locked state. [Clearing condition] The flash sequencer starts the “Status Clear” or “Forced Stop” command processing while the CFAE and DFAE bits in the FASTAT register are 0.

Table 4.2 FASTAT Register Contents (2/2)

Bit Position	Bit Name	Function
3	DFAE	Data Flash Access Error Indicates whether or not data flash access error has been generated. If this bit becomes “1”, ILGLERR bit in FSTATR is set to “1” and flash sequencer enters the command-locked state. 0: No data flash access error has occurred. 1: Data flash access error has occurred. [Setting conditions] Commands have been issued in data flash programming/erasure mode under the following settings. • FACI command has been issued when the setting of bits 18 to 0 in the FSADDR register is 1_0000_H to 7_FFFF_H (reserved area for the data area). • The configuration setting command has been issued when the setting of bits 18 to 0 in the FSADDR register is 0_0000_H to 0_003F_H or 0_0100_H to 7_FFFF_H. • “OTP Set” command has been issued when the settings for bits 18 to 0 in FSADDR are 0_0000_H to 0_003F_H or 0_00A0_H to 7_FFFF_H. [Clearing condition] “0” is written after reading “1” from this bit.
2, 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	ECRCT	Error Correction Indicates that a 1-bit error has been corrected when the flash sequencer reads the flash memory (configuration setting, overwrite parameters, and OTP setting) or the FCURAM. 0: 1-bit error has not been corrected. 1: 1-bit error has been corrected. [Clearing conditions] • The flash sequencer starts the “Status Clear” or “Forced Stop” command processing when bits CFGCRCT, TBLCRCT, and OTPCRCT in FSTATR are 1. • The flash sequencer starts the “Forced Stop” command processing when the FRCRCT bit in FSTATR is 1.

4.2 FAEINT — Flash Access Error Interrupt Enable Register

FAEINT enables or disables output of flash access error (“FLERR”) interrupt.

In this product, a flash access error interrupt is handled as an error source for the ECM.

Access: This register can be read/written in 8-bit units.

Address: FFA1 0014$_H$

Value after reset: 99$_H$

Bit	7	6	5	4	3	2	1	0
	CFAEIE	—	—	CMDLKIE	DFAEIE	—	—	ECRCTIE
Value after reset	1	0	0	1	1	0	0	1
R/W	R/W	R	R	R/W	R/W	R	R	R/W

Table 4.3 FAEINT Register Contents

Bit Position	Bit Name	Function
7	CFAEIE	Code Flash Access Error Interrupt Enable Enables or disables “FLERR” interrupt request when code flash access error occurs and CFAE bit in FASTAT becomes “1”. 0: Does not generate “FLERR” interrupt request when FASTAT.CFAE = 1. 1: Generates “FLERR” interrupt request when FASTAT.CFAE = 1.
6, 5	Reserved	When read, the value after reset is read. When writing, write the value after reset.
4	CMDLKIE	Command Lock Interrupt Enable Enables or disables “FLERR” interrupt request when flash sequencer enters the command-locked state and CMDLK bit in FASTAT becomes “1”. 0: Does not generate “FLERR” interrupt request when FASTAT.CMDLK = 1. 1: Generates “FLERR” interrupt request when FASTAT.CMDLK = 1.
3	DFAEIE	Data Flash Access Error Interrupt Enable Enables or disables “FLERR” interrupt request when data flash access error occurs and DFAE bit in FASTAT becomes “1”. 0: Does not generate “FLERR” interrupt request when FASTAT.DFAE = 1. 1: Generates “FLERR” interrupt request when FASTAT.DFAE = 1.
2, 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	ECRCTIE	Error Correction Interrupt Enable Enables or disables the “FLERR” interrupt request when a 1-bit error has been corrected and the ECRCT bit in FASTAT has been set to 1 on the flash memory read (configuration setting, overwrite parameters, and OTP setting) or the FCURAM read by the flash sequencer. 0: Does not generate the “FLERR” interrupt request when FASTAT.ECRCT = 1. 1: Generates the “FLERR” interrupt request when FASTAT.ECRCT = 1.

4.3 FSADDR — FACI Command Start Address Register

FSADDR specifies the start address of the target area for command processing when the FACI command “Programming”, “DMA Programming”, “Block Erase”, “Blank Check”, “Configuration Set”, “Lock Bit Programming”, “Lock Bit Read”, or “OTP Set” is issued.

FSADDR value is initialized when SUINIT bit in FSUINITR is set to “1”. It is also initialized by a reset.

Access: This register can be read/written in 32-bit units.

Address: FFA1 0030$_H$

Value after reset: 0000 0000$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FSADDR[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FSADDR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R

Note 1. This bit can be written when the FRDY bit in the FSTATR register is “1”. Writing to this bit while the FRDY bits is “0” is ignored.

Table 4.4 FSADDR Register Contents

Bit Position	Bit Name	Function
31 to 0	FSADDR[31:0]	Start Address of FACI Command Processing These bits specify the start address of the FACI command processing. Bits 31 to 24 are ignored in the FACI command processing for the code flash memory. Bits 31 to 19 are ignored in the FACI command processing for the data flash memory. Lower address bits for smaller address than boundary below are also ignored. Bits 24 to 4 are used to generate the address parity. Command — Address Boundary Programming (code flash memory): 256 bytes Programming (data flash memory): 4-byte write: 4 bytes DMA Programming: 4 bytes Block Erase (code flash memory): 8 Kbytes or 32 Kbytes Block Erase (data flash memory): 64 bytes Blank Check: 4 bytes Configuration Set: 16 bytes Lock Bit Programming: 8 Kbytes or 32 Kbytes Lock Bit Read: 8 Kbytes or 32 Kbytes OTP Set: 16 bytes

4.4 FEADDR — FACI Command End Address Register

This register specifies the end address in the target area in Blank Check command processing. When blank check addressing mode is set to incremental mode (i.e. FBCCNT.BCDIR = “0”), address specified in FSADDR should be smaller than address in FEADDR. Conversely, address in FSADDR should be larger than address in FEADDR when blank check addressing mode is set to decremental mode (i.e. FBCCNT.BCDIR = “1”). If setting of BCDIR, FSADDR, and FEADDR are inconsistent, FACI detects error and flash sequencer enters the command-locked state. (See **Section 8.2, Error Protection**.)

FEADDR value is initialized when SUINIT bit in FSUINITR is set to “1”. It is also initialized by a reset.

Access: This register can be read/written in 32-bit units.

Address: FFA1 0034$_H$

Value after reset: 0000 0000$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FEADDR[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FEADDR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R

Note 1. This bit can be written when the FRDY bit in the FSTATR register is “1”. Writing to this bit while the FRDY bits is “0” is ignored.

Table 4.5 FEADDR Register Contents

Bit Position	Bit Name	Function
31 to 0	FEADDR[31:0]	FACI Command End Address Specifies end address of target area in “Blank Check” command. Bits 31 to 19, 1 and 0 are ignored in the command processing.

4.5 FCURAME — FCURAM Enable Register

FCURAME enables or disables access to FCURAM area.

Access: This register can be read/written in 16-bit units.

Address: FFA1 0054_H

Value after reset: 0000_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								—	—	—	—	—	—	FRAMTRAN	FCRME
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R	R	R	R	R	R/W*2	R/W*2

Note 1. The written value is not stored in this bit. The value read is always 00_H.

Note 2. Writing to this bit is enabled only when $C4_H$ is written to the KEY[7:0] bits.

Table 4.6 FCURAME Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits enable or disable FRAMTRAN bit and FCRME bit modification.
7 to 2	Reserved	When read, the value after reset is read. When writing, write the value after reset.
1	FRAMTRAN	FCURAM Transfer Mode Specifies the FCURAM transfer mode. 0: Normal transfer mode Both read and write accesses to FCURAM are possible. 1: High-speed write mode High-speed writing to the FCURAM is possible.
0	FCRME	FCURAM Enable Enables or disables access to the FCURAM. Before writing to the FCURAM, clear FENTRYR to 0000_H to stop the flash sequencer. 0: Disables access to FCURAM. 1: Enables access to FCURAM.

4.6 FSTATR — Flash Status Register

FSTATR indicates flash sequencer status.

Access: This register can only be read in 8-, 16-, or 32-bit units.

Address: FFA1 0080_H

Value after reset: $0000\ 8000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	EBFULL	OTPDTCT	OTPCRCT
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRDY	ILGLERR	ERSERR	PRGERR	SUSRDY	DBFULL	ERSSPD	PRGSPD	—	FLWEERR	CFGDTCT	CFGCRCT	TBLDTCT	TBLCRCT	FRDTCT	FRCRCT
Value after reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.7 FSTATR Register Contents (1/5)

Bit Position	Bit Name	Function
31 to 19	Reserved	When read, the value after reset is read.
18	EBFULL	ECC Buffer Full Indicates the ECC buffer status when issuing the programming command. The FACI incorporates a buffer for ECC bit (ECC buffer). While the ECCDISE bit in FECCTMD is 1, FDMYECC can be used as the ECC buffer. When FDMYECC is written to while the EBFULL bit is 1, the FACI inserts a wait in the peripheral bus. 0: The ECC buffer is empty. 1: The ECC buffer is full. [Setting condition] • The ECC buffer becomes full while issuing the programming command. [Clearing condition] • The ECC buffer becomes empty.
17	OTPDTCT	2-Bit Error Detection Monitor (OTP Set) Indicates that a 2-bit error has been detected on reading the OTP value. The FACI reads the OTP value in “Programming”, “Block Erase”, “Lock Bit Programming”, “Lock Bit Read”, and “OTP Set” for the code flash memory. When this bit is 1, the flash sequencer is in the command-locked state. 0: No 2-bit error has been detected. 1: A 2-bit error has been detected. [Clearing condition] • The flash sequencer starts “Status Clear” or “Forced Stop” command processing.
16	OTPCRCT	1-Bit Error Correction Monitor (OTP Set) Indicates that a 1-bit error has been corrected on reading the OTP value. The FACI reads the OTP value in “Programming”, “Block Erase”, “Lock Bit Programming”, “Lock Bit Read”, and “OTP Set” for the code flash memory. When this bit is 1, the flash sequencer continues the command processing and does not enter the command-locked state. 0: 1-bit error has not been corrected. 1: 1-bit error has been corrected. [Clearing condition] • The flash sequencer starts “Status Clear” or “Forced Stop” command processing.

Table 4.7 FSTATR Register Contents (2/5)

Bit Position	Bit Name	Function
15	FRDY	Flash Ready Indicates the processing state in flash sequencer. 0: Processing of the command “Programming”, “DMA Programming”, “Block Erase”, “Programming/Erasure Suspend”, “Programming/Erasure Resume”, “Forced Stop”, “Blank Check”, “Configuration Set”, “Lock Bit Programming”, “Lock Bit Read”, or “OTP Set” is in progress. 1: None of the above is in progress. [Setting conditions] • Flash sequencer completes processing. • Flash sequencer suspends processing by “Programming/Erasure Suspend” command. • Flash sequencer terminates processing by “Forced Stop” command. [Clearing conditions] • When the flash sequencer accepts the FACI command • For “Programming”, “DMA Programming”, “Configuration Set”, or “OTP Set” command, after the first write access to the FACI command issuing area. • For other commands, after the last write access to the FACI command issuing area.
14	ILGLERR	Illegal Command Error Indicates that flash sequencer has detected an illegal command or illegal flash memory access. When this bit is “1”, flash sequencer is in the command-locked state. 0: Flash sequencer has not detected any illegal command or illegal flash memory access. 1: Flash sequencer has detected an illegal command or illegal flash memory access [Setting conditions] • Flash sequencer has detected an illegal command. • Flash sequencer has detected an illegal flash memory access. • FENTRYR setting is illegal. [Clearing condition] • “Status Clear” or “Forced Stop” command processing is started while the DFAE or CFAE bits in the FASTAT register is 0. If the flash sequencer completes processing of “Status Clear” or “Forced Stop” command while the CFAE or DFAE bit in the FASTAT register is 1, this bit is set to 1. This bit is temporarily set to 0 during processing of “Forced Stop” command, and is re-set to 1 when the CFAE or DFAE bit is detected as 1 on completion of command processing.
13	ERSERR	Erasure Error Indicates result of code or data flash erasure by flash sequencer. When this bit is “1”, flash sequencer is in the command-locked state. 0: Erasure processing has been completed successfully 1: An error has occurred during erasure [Setting conditions] • An error has occurred during erasure. • “Block Erase” command has been issued for the area protected by lock bit. [Clearing condition] • “Status Clear” or “Forced Stop” command processing is started.

Table 4.7 FSTATR Register Contents (3/5)

Bit Position	Bit Name	Function
12	PRGERR	Programming Error Indicates the result of code or data flash programming by flash sequencer. When this bit is “1”, flash sequencer is in the command-locked state. 0: Programming has been completed successfully 1: An error has occurred during programming [Setting conditions] • An error has occurred during programming. • The programming or lock-bit programming command has been issued for the area protected by lock bit. [Clearing condition] • “Status Clear” or “Forced Stop” command processing is started.
11	SUSRDY	Suspend Ready Indicates whether flash sequencer is ready to accept a “Programming/Erasure Suspend” command. 0: Flash sequencer cannot accept “Programming/Erasure Suspend” command. 1: Flash sequencer can accept “Programming/Erasure Suspend” command. [Setting condition] • After initiating programming or erasure, the flash sequencer entered a state where it is ready to accept “Programming/Erasure Suspend” command. [Clearing conditions] • Flash sequencer has accepted “Programming/Erasure Suspend” or “Forced Stop” command. (after the write access to the FACI command issuing area is completed) • Flash sequencer has entered the command-locked state during programming or erasure. • Programming/erasure processing is completed.
10	DBFULL	Data Buffer Full Indicates the data buffer status when issuing the programming command. The FACI incorporates a buffer for write data (data buffer). When issuing the flash memory write data to the FACI command issue area while the data buffer is full, the FACI inserts a wait in the peripheral bus. 0: The data buffer is empty. 1: The data buffer is full. [Setting condition] • The data buffer becomes full while issuing the programming command. [Clearing condition] • The data buffer becomes empty.
9	ERSSPD	Erasure-Suspended Status Indicates that flash sequencer has entered “Erase” command suspension process or erasure-suspended status. 0: Flash sequencer is in status other than the below mentioned. 1: Flash sequencer is in erasure suspension process or erasure-suspended status. [Setting condition] • Flash sequencer has initiated “Programming/Erasure Suspend” command during “Erase” command processing. [Clearing conditions] • Flash sequencer has accepted “Programming/Erasure Resume” command. (after the write access to the FACI command issuing area is completed) • “Forced Stop” command processing is started.

Table 4.7 FSTATR Register Contents (4/5)

Bit Position	Bit Name	Function
8	PRGSPD	Programming-Suspended Status Indicates that flash sequencer has entered the programming command suspension process or programming suspended status. 0: Flash sequencer is in status other than the below mentioned. 1: Flash sequencer is in programming suspension process or programming-suspended status. [Setting condition] • Flash sequencer has initiated “Programming/Erasure Suspend” command during programming command processing. [Clearing conditions] • Flash sequencer has accepted “Programming/Erasure Resume” command. (after the write access to the FACI command issuing area is completed) • “Forced Stop” command processing is started.
7	Reserved	This bit is always read as 0. Write value should always be 0.
6	FLWEERR	Flash write erase protect error Indicates a violation of the flash memory overwrite protection due to FHVE3 register. When the FLWEERR bit is set to 1, the flash sequencer enters the command-locked state. 0: No error has occurred 1: An error has occurred [Clearing condition] • The flash sequencer starts processing of a “Forced Stop” command.
5	CFGDTCT	2-Bit Error Detection Monitor (Configuration Set) Indicates that a 2-bit error has been detected on reading the Configuration Set value. The FACI reads the Configuration Set value in “Configuration Set”. When this bit is 1, the flash sequencer is in the command-locked state. 0: No 2-bit error has been detected. 1: A 2-bit error has been detected. [Clearing condition] • The flash sequencer starts “Status Clear” or “Forced Stop” command processing.
4	CFGCRCT	1-Bit Error Correction Monitor (Configuration Set) Indicates that a 1-bit error has been corrected on reading the Configuration Set value. The FACI reads the Configuration Set value in “Configuration Set”. When this bit is 1, the flash sequencer continues command processing and does not enter the command-locked state. 0: 1-bit error has not been corrected. 1: 1-bit error has been corrected. [Clearing condition] • The flash sequencer starts “Status Clear” or “Forced Stop” command processing.
3	TBLDTCT	2-Bit Error Detection Monitor (Overwrite Parameter Table) Indicates that a 2-bit error has been detected on reading the overwrite parameter table. The FACI reads the overwrite parameter table in “Programming”, “DMA Programming”, “Block Erase”, “Blank Check”, “Configuration Set”, “Lock Bit Programming”, and “OTP Set” for the flash memory. When this bit is 1, the flash sequencer is in the command-locked state. 0: No 2-bit error has been detected. 1: A 2-bit error has been detected. [Clearing condition] • The flash sequencer starts “Status Clear” or “Forced Stop” command processing.

Table 4.7 FSTATR Register Contents (5/5)

Bit Position	Bit Name	Function
2	TBLCRCT	1-Bit Error Correction Monitor (Overwrite Parameter Table) Indicates that a 1-bit error has been corrected on reading the overwrite parameter table. The FACI reads the overwrite parameter table in “Programming”, “DMA Programming”, “Block Erase”, “Blank Check”, “Configuration Set”, “Lock Bit Programming”, and “OTP Set” for the flash memory. When this bit is 1, the flash sequencer does not enter the command-locked state. 0: 1-bit error has not been corrected. 1: 1-bit error has been corrected. [Clearing condition] • The flash sequencer starts “Status Clear” or “Forced Stop” command processing.
1	FRDTCT	2-Bit Error Detection Monitor (FCURAM) Indicates that 2-bit error has been detected in FCURAM read by the FCU. When the FRDTCT bit is “1”, the flash sequencer enters the command-locked state. 0: No 2-bit error has been detected. 1: A 2-bit error has been detected. [Clearing condition] • After the flash sequencer starts “Forced Stop” command processing
0	FRCRCT	1-Bit Error Correction Monitor (FCURAM) Indicates that a 1-bit error has been corrected when the FCU reads the FCURAM. When this bit is 1, the flash sequencer does not enter the command-locked state. 0: 1-bit error has not been corrected. 1: 1-bit error has been corrected. [Clearing condition] • After the flash sequencer starts “Forced Stop” command processing

4.7 FENTRYR — Flash Programming/Erasure Mode Entry Register

FENTRYR specifies “Programming/Erasure Mode” for code flash or data flash. To specify “Programming/Erasure Mode” for code flash or data flash so that flash sequencer can accept FACI commands, set either of FENTRYD or FENTRYC bit to “1”.

Note that if this register is set to other than 0000_H, 0001_H, and 0080_H, the ILGLERR bit in the FSTATR register will be set and flash sequencer will enter the command-locked state.

FENTRYR value is initialized when SUINIT bit in FSUINITR is set to “1”. It is also initialized by a reset.

Access: This register can be read/written in 16-bit units.

Address: FFA1 0084_H

Value after reset: 0000_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								FENTRYD	—	—	—	—	—	—	FENTRYC
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*2,*3	R	R	R	R	R	R	R/W*2,*3

Note 1. The written value is not stored in this bit. The value read is always 00_H.

Note 2. This bit can be written when the FRDY bit in the FSTATR register is “1”. Writing to this bit while the FRDY bits is “0” is ignored.

Note 3. Writing to this bit is enabled only when AA_H is written to the KEY[7:0] bits.

Table 4.8 FENTRYR Register Contents (1/2)

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits enable or disable FENTRYD and FENTRYC bits modification.
7	FENTRYD	Data Flash Programming/Erasure Mode Entry This bit specifies the Programming/Erasure mode for data flash. 0: Data flash is in “Read Mode” 1: Data flash is in “Programming/Erasure Mode” [Setting condition] • “1” is written to FENTRYD while write enabling conditions are satisfied and FENTRYR is 0000_H. [Clearing conditions] • A value other than AA_H is written to KEY[7:0] in FENTRYR while FRDY bit is “1”. • “0” is written to FENTRYD while the write enabling conditions are satisfied. • FENTRYR is written to while FENTRYR is not 0000_H and the write enabling conditions are satisfied.
6 to 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.

Table 4.8 FENTRYR Register Contents (2/2)

Bit Position	Bit Name	Function
0	FENTRYC	Code Flash Programming/Erasure Mode Entry This bit specifies the Programming/Erasure mode for code flash. 0: Code flash is in “Read Mode” 1: Code flash is in “Programming/Erasure Mode” [Setting condition] • “1” is written to FENTRYC while write enabling conditions are satisfied and FENTRYR is 0000_H. [Clearing conditions] • A value other than AA_H is written to KEY[7:0] in FENTRYR while FRDY bit is “1”. • 0 is written to the FENTRYC bit while writing to FENTRYR is enabled. • FENTRYR is written to while FENTRYR is not 0000_H and the write enabling conditions are satisfied.

4.8 FPROTR — Code Flash Protect Register

FPROTR enables or disables protection function through lock bits against programming and erasure. FPROTR value is initialized when SUINIT bit in FSUINITR is set to “1”. It is also initialized by a reset.

Access: This register can be read/written in 16-bit units.

Address: FFA1 0088_H

Value after reset: 0000_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								—	—	—	—	—	—	—	FPROTCN
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R	R	R	R	R	R	R/W*2

Note 1. The written value is not stored in this bit. The value read is always 00_H.

Note 2. Writing to this bit is enabled only when 55_H is written to the KEY[7:0] bits.

Table 4.9 FPROTR Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits enable or disable FPROTCN bit modification.
7 to 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	FPROTCN	Lock Bit Protect Cancel Enables or disables protection through lock bits against programming and erasure. 0: Enables protection through lock bits 1: Disables protection through lock bits [Setting condition] • “1” is written to FPROTCN while write enabling conditions are satisfied and FENTRYR is not 0000_H. [Clearing conditions] • A value other than 55_H is written to KEY[7:0] in FPROTR. • 0 is written to the FPROTCN bit while writing to FPROTR is enabled. • FENTRYR register value is 0000_H.

4.9 FSUINITR — Flash Sequencer Set-Up Initialize Register

FSUINITR register is used for initialization of flash sequencer set-up.

Access: This register can be read/written in 16-bit units.

Address: FFA1 008C$_H$

Value after reset: 0000$_H$

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								—	—	—	—	—	—	—	SUINIT
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R	R	R	R	R	R	R/W *2,*3

Note 1. The written value is not stored in this bit. The value read is always 00$_H$.

Note 2. This bit can be written when the FRDY bit in the FSTATR register is “1”. Writing to this bit while the FRDY bits is “0” is ignored.

Note 3. Writing to this bit is enabled only when 2D$_H$ is written to the KEY[7:0] bits.

Table 4.10 FSUINITR Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits enable or disable SUINIT bit modification.
7 to 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	SUINIT	Set-up Initialization Initializes the flash sequencer set-up registers (FEADDR, FPROTR, FCPSR, FSADDR, FENTRYR, and FBCCNT). 0: The above flash sequencer set-up registers retain their current values. 1: The above flash sequencer set-up registers are initialized.

4.10 FLKSTAT — Lock Bit Status Register

FLKSTAT indicates lock bit status which is read through “Lock Bit Read” command execution.

In this product, an FACI reset transfer error interrupt is handled as an error source for the ECM.

Access: This register can only be read in 8-bit units.

Address: FFA1 0090_H

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	FLOCKST
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Table 4.11 FLKSTAT Register Contents

Bit Position	Bit Name	Function
7 to 1	Reserved	When read, the value after reset is read.
0	FLOCKST	Lock Bit Status Reflects the lock bit status read through “Lock Bit Read” command execution. After a lock bit reading command is issued and when the FSTATR.FRDY bit is set to 1, valid data is stored in the FLOCKST bit. This bit value is retained until the next lock bit reading command is completed. 0: Protected state 1: Non-protected state

4.11 FRFSTEADR — FCURAM First Error Address Register

FRFSTEADR indicates an address where the first ECC error has occurred on reading the FCURAM.

Access: This register can only be read in 32-bit units.

Address: FFA1 0094_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	FRFSTEADR[11:0]											
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.12 FRFSTEADR Register Contents

Bit Position	Bit Name	Function
31 to 12	Reserved	When read, the value after reset is read.
11 to 0	FRFSTEADR[11:0]	FCURAM First Error Address Indicate the first ECC error address on reading the FCURAM. An address offset from the top address of the FCURAM is stored.

4.12 FRTSTAT — FACI Reset Transfer Status Register

FRTSTAT indicates error status for the FACI reset transfer.

If the setting of the RTEDTCT or RTECRCT bit is 1, an “FACI reset transfer error” source condition for the ECM occurs. Operation of the device is not guaranteed if the FACI reset transfer error has occurred. Whether the FACI reset transfer error has occurred can be checked by reading the status register in the ECM. For details of the ECM, see *Section 30, Error Control Module (ECM)* in *the RH850/C1M-A User’s Manual: Hardware*.

Access: This register can only be read in 8-bit units.

Address: FFA1 0098_H

Value after reset: The value varies depending on the status of the FLMD0 pin.

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	RTEDTCT	RTECRCT
Value after reset	0	0	0	0	0	0	0/1	0/1
R/W	R	R	R	R	R	R	R	R

Table 4.13 FRTSTAT Register Contents

Bit Position	Bit Name	Function
7 to 2	Reserved	When read, the value after reset is read.
1	RTEDTCT	FACI reset transfer error detection Indicates that a 2-bit error has been detected during the FACI reset transfer. When RTEDTCT is “1”, the flash sequencer does not enter the command-locked state. 0: No 2-bit error has been detected. 1: A 2-bit error has been detected. The RTEDTCT bit is cleared when a 2-bit error is not detected during the FACI reset transfer after a reset of the microcomputer.
0	RTECRCT	FACI reset transfer error correction Indicates that a 1-bit error has been corrected during the FACI reset transfer. When RTECRCT is “1”, the flash sequencer does not enter the command-locked state. 0: No 1-bit error has been corrected. 1: A 1-bit error has been corrected. The RTECRCT bit is cleared when a 1-bit error is not corrected during the FACI reset transfer after a reset of the microcomputer.

4.13 FRTEINT — FACI Reset Transfer Error Interrupt Enable Register

CAUTIONS

Although the FRTEINT register is provided in the product, the settings of this register are not required since an interrupt is not generated in this product.

FRTEINT enables or disables generation of an interrupt request of the FACI reset transfer error (FRTERR).

In this product, an FACI reset transfer error interrupt is handled as an error source for the ECM.

Access: This register can be read/written in 8-bit units.

Address: FFA1 009C$_H$

Value after reset: 03$_H$

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	RTEDIE	RTECIE
Value after reset	0	0	0	0	0	0	1	1
R/W	R	R	R	R	R	R	R/W	R/W

Table 4.14 FRTEINT Register Contents

Bit Position	Bit Name	Function
7 to 2	Reserved	When read, the value after reset is read. When writing, write the value after reset.
1	RTEDIE	FACI reset transfer error detection interrupt enable Enables or disables generation of an “FRTERR” interrupt when a 2-bit error is detected during the FACI reset transfer and the RTEDTCT bit in FRTSTAT is set to “1” 0: No FRTERR interrupt is generated when FRTSTAT.RTEDTCT = “1” 1: An FRTERR interrupt is generated when FRTSTAT.RTEDTCT = “1”
0	RTECIE	FACI reset transfer error correction interrupt enable Enables or disables generation of an “FRTERR” interrupt when a 1-bit error is corrected during the FACI reset transfer and the RTECRCT bit in FRTSTAT is set to “1” 0: No FRTERR interrupt is generated when FRTSTAT.RTECRCT = “1” 1: An FRTERR interrupt is generated when FRTSTAT.RTECRCT = “1”

4.14 FCMDR — FACI Command Register

FCMDR stores commands that FACI has accepted.

Access: This register can only be read in 16-bit units.

Address: FFA1 00A0$_H$

Value after reset: FFFF$_H$

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMDR[7:0]								PCMDR[7:0]							
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.15 FCMDR Register Contents

Bit Position	Bit Name	Function
15 to 8	CMDR[7:0]	Command These bits store the latest command accepted by FACI.
7 to 0	PCMDR[7:0]	Previous Command These bits store previous command accepted by FACI.

Table 4.16 States of FCMDR after Acceptance of the Various Commands

Command	CMDR[7:0]	PCMDR[7:0]
Programming	$E8_H$	Previous command
DMA Programming	EA_H	Previous command
Block Erase	$D0_H$	20_H
Programming/Erasure Suspend	$B0_H$	Previous command
Programming/Erasure Resume	$D0_H$	Previous command
Status Clear	50_H	Previous command
Forced Stop	$B3_H$	Previous command
Blank Check	$D0_H$	71_H
Configuration Set	40_H	Previous command
Lock Bit Programming	$D0_H$	77_H
Lock Bit Read	$D0_H$	71_H
OTP Set	45_H	Previous command

4.15 FPESTAT — Flash Programming/Erasure Status Register

FPESTAT indicates the result of programming or erasure to the flash memory.

Access: This register can only be read in 16-bit units.

Address: FFA1 00C0$_H$

Value after reset: 0000$_H$

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	PEERRST[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.17 FPESTAT Register Contents

Bit Position	Bit Name	Function
15 to 8	Reserved	When read, the value after reset is read.
7 to 0	PEERRST[7:0]	Programming/Erasure Error Status Indicates the source of error that occurs during programming/erasure for code flash or data flash. The value of the PEERRST[7:0] bits is only valid if PRGERR or ERSERR bit value in FSTATR register is 1, while FRDY bit in FSTATR register is “1”. When ERSERR and PRGERR are “0”, the PEERRST[7:0] bits retain the value to indicate the source of error that previously occurred. 00$_H$: No error 01$_H$: A programming error attempt made to an area protected by the lock bits 02$_H$: A programming error caused by other than lock bits 11$_H$: An erasing error attempt made to an area protected by the lock bits 12$_H$: An erasing error caused by other than lock bits Other than above: Reserved

4.16 FBCCNT — Data Flash Blank Check Control Register

FBCCNT specifies addressing mode in “Blank Check” command processing. FBCCNT value is initialized when SUINIT bit in FSUINITR is set to “1”. It is also initialized by a reset.

Access: This register can be read/written in 8-bit units.

Address: FFA1 00D0$_H$

Value after reset: 00$_H$

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	BCDIR
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W

Table 4.18 FBCCNT Register Contents

Bit Position	Bit Name	Function
7 to 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	BCDIR	Blank Check Direction Specifies addressing mode in blank check operation. 0: Blank check is executed from smaller address to larger address. (Incremental mode) 1: Blank check is executed from larger address to smaller address. (Decremental mode)

4.17 FBCSTAT — Data Flash Blank Check Status Register

FBCSTAT stores check results by executing “Blank Check” command.

Access: This register can only be read in 8-bit units.

Address: FFA1 00D4$_H$

Value after reset: 00$_H$

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	BCST
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Table 4.19 FBCSTAT Register Contents

Bit Position	Bit Name	Function
7 to 1	Reserved	When read, the value after reset is read.
0	BCST	Blank Check Status Indicates the result of “Blank Check” command. 0: The target area is not filled with data (i.e. is in the blank state, where no data have been written after erasure). 1: The target area is filled with 0s and/or 1s.

4.18 FPSADDR — Data Flash Programming Start Address Register

FPSADDR indicates address of the first programmed data which is found in “Blank Check” command execution.

Access: This register can only be read in 32-bit units.

Address: FFA1 00D8$_H$

Value after reset: 0000 0000$_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	PSADR[18:16]		
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PSADR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.20 FPSADDR Register Contents

Bit Position	Bit Name	Function
31 to 19	Reserved	When read, the value after reset is read.
18 to 0	PSADR[18:0]	Programmed Area Start Address Indicates address of the first programmed data which is found in “Blank Check” command execution. These bits stores address offset from the top address in the data flash memory. The value of the PSADR[18:0] bits is only valid if BCST bit value in FBCSTAT register is 1, while FRDY bit in FSTATR register is “1”. When BCST bit is “0”, the PSADR[18:0] bits hold the address that previously checked.

4.19 FCPSR — Flash Sequencer Processing Switch Register

FCPSR selects erasure-suspended mode. FCPSR value is initialized when SUINIT bit in FSUINITR is set to “1”. It is also initialized by a reset.

Access: This register can be read/written in 16-bit units.

Address: FFA1 00E0$_H$

Value after reset: 0000$_H$

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ESUSPMD
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Table 4.21 FCPCR Register Contents

Bit Position	Bit Name	Function
15 to 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	ESUSPMD	Erasure-Suspended Mode Selects erasure-suspended mode to be entered when “Programming/Erasure Suspend” command is issued while flash sequencer is erasing flash memory. ESUSPMD bit should be set before issuing “Block Erase” command. 0: Suspension-priority mode 1: Erasure-priority mode

4.20 FPCKAR — Flash Sequencer Processing Clock Notify Register

FPCKAR specifies the operating frequency of the flash sequencer while processing an FACI command. After a reset, each product is set to its maximum operating frequency.

Access: This register can be read/written in 16-bit units.

Address: FFA1 00E4$_H$

Value after reset: Maximum operating frequency of the FACI in the given product.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								PCKA[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W *2,*3	R/W *2,*3	R/W *2,*3	R/W *2,*3	R/W *2,*3	RR/W *2,*3	R/W *2,*3	R/W *2,*3

Note 1. The written value is not stored in this bit. The value read is always 00$_H$.

Note 2. This bit can be written when the FRDY bit in the FSTATR register is “1”. Writing to this bit while the FRDY bits is “0” is ignored.

Note 3. Writing to this bit is enabled only when 1E$_H$ is written to the KEY[7:0] bits.

Table 4.22 FPCKAR Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits enable or disable the PCKA[7:0] bit modification.
7 to 0	PCKA[7:0]	Flash Sequencer Operating Clock Notify Specifies the operating frequency of the flash sequencer while processing an FACI command. Set the desired frequency in these bits before issuing an FACI command. Specifically, convert the frequency represented in MHz into a binary number and set it in these bits. Example: Frequency is 35.9 MHz (PCKA[7:0] = 24$_H$) Round up the first decimal place of 35.9 MHz to a whole number (= 36) and convert it into a binary number. If the value set in these bits is smaller than the operating frequency of the flash sequencer, the flash memory overwrite characteristics cannot be guaranteed. If the value set in these bits is greater than the operating frequency of the flash sequencer, the flash memory overwrite characteristics can be guaranteed with the increased FACI command processing time such as overwrite time. (The minimum FACI command processing time is available when the operating frequency of the flash sequencer is the same as the PCKA[7:0] value.) When SSCG is used, convert the center value of the operating frequency as described in the above example, and set the resulting value.

4.21 FECCEMON — Flash ECC Encoder Monitor Register

FECCEMON monitors the outputs from the address parity generator and ECC encoder.

Access: This register can only be read in 16-bit units.

Address: FFA1 0100_H

Value after reset: $FFFF_H$

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	FAPARM	FECCM8	FECCM7	FECCM6	FECCM5	FECCM4	FECCM3	FECCM2	FECCM1	FECCM0
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.23 FECCEMON Register Contents

Bit Position	Bit Name	Function
15 to 10	Reserved	When read, the value after reset is read.
9	FAPARM	Address Parity Monitor Indicates the output from the address parity generator. • In code flash programming/erasure mode This bit indicates the output from the address parity generator. • In data flash programming/erasure mode This bit is fixed to 1.
8 to 0	FECCM8 to FECCM0	ECC Monitor Indicates the ECC encoder output. • In code flash programming/erasure mode The FECCM8 to FECCM0 bits indicate the ECC encoder output for the code flash memory. • In data flash programming/erasure mode The FECCM8 and FECCM7 bits are fixed to 1. The FECCM6 to FECCM0 bits indicate the ECC encoder output for the data flash memory.

4.22 FECCTMD — Flash ECC Test Mode Register

FECCTMD sets the ECC test function for the flash memory.

Access: This register can be read/written in 16-bit units.

Address: FFA1 0104_H

Value after reset: 0030_H

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	KEY[7:0]								—	—	CECCVE	DECCVE	—	—	—	ECCDISE
Value after reset	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
R/W	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R	R/W*2	R/W*2	R	R	R	R/W*2

Note 1. The written value is not stored in this bit. The value read is always 00_H.

Note 2. Writing to this bit is enabled only when $A6_H$ is written to the KEY[7:0] bits.

Table 4.24 FECCTMD Register Contents

Bit Position	Bit Name	Function
15 to 8	KEY[7:0]	Key Code These bits enable or disable modification of the CECCVE, DECCVE, and ECCDISE bits.
7, 6	Reserved	When read, the value after reset is read. When writing, write the value after reset.
5	CECCVE	Code Flash Memory ECC Area Verify Enable Specifies the verify operation on overwriting the code flash memory. 0: Verifies the data area only. 1: Verifies the data area and the ECC area.
4	DECCVE	Data Flash Memory ECC Area Verify Enable Specifies the verify operation on overwriting the data flash memory. 0: Verifies the data area only. 1: Verifies the data area and the ECC area.
3 to 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	ECCDISE	ECC Encoder Disable Disables the address parity generator and the ECC encoder. If the address parity generator and the ECC encoder are disabled, the FDMYECC value is written to the flash memory. 0: The address parity generator and the ECC encoder are enabled. 1: The address parity generator and the ECC encoder are disabled.

4.23 FDMYECC — Flash Dummy ECC Register

FDMYECC specifies the address parity and ECC value to be written into the flash memory when the ECCDISE bit in the FECCTMD register is 1. The bit functions in code flash programming/erasure mode are different from those in data flash programming/erasure mode as shown below.

Access: This register can be read/written in 16-bit units.

Address: FFA1 0108_H

Value after reset: $FFFF_H$

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	DMYAPAR	DMYECC[8:0]								
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 4.25 FDMYECC Register Contents (in Code Flash Programming/Erasure Mode)

Bit Position	Bit Name	Function
15 to 10	Reserved	When read, the value after reset is read. When writing, write the value after reset.
9	DMYAPAR	Dummy Address Parity Specifies the address parity value when the ECCDISE bit is 1.
8 to 0	DMYECC[8:0]	Dummy ECC Specify the ECC value when the ECCDISE bit is 1.

Table 4.26 FDMYECC Register Contents (in Data Flash Programming/Erasure Mode)

Bit Position	Bit Name	Function
15 to 10	Reserved	When read, the value after reset is read. When writing, write the value after reset.
9	DMYAPAR	Reserved When read, the value after reset is read. When writing, write the value after reset.
8, 7	DMYECC[8:7]	Reserved When read, the value after reset is read. When writing, write the value after reset.
6 to 0	DMYECC[6:0]	Dummy ECC Specify the ECC value when the ECCDISE bit is 1.

4.24 FCUFAREA — FCU Firmware Area Select Register

FCUFAREA selects the FCU firmware storage area.

Access: This register can be read/written in 8-bit units.

Address: FFC5 9008_H

Value after reset: *1

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	FCUFSEL
Value after reset	0	0	0	0	0	0	0	*1
R/W	R	R	R	R	R	R	R	R/W

Note 1. This bit is set to 1 when booted in serial programming mode, and cleared to 0 when in user boot mode.

Table 4.27 FCUFAREA Register Contents

Bit Position	Bit Name	Function
7 to 1	Reserved	When read, the value after reset is read. When writing, write the value after reset.
0	FCUFSEL	Firmware Storage Area Select This bit switches the assigned area in 0001_7000_H to 0001_$7FFF_H$. In addition, when the configuration area and OTP setting area are read, the FCUFSEL bit must be set to “1”. 0: The address range from 0001 7000_H to 0001 $7FFF_H$ is assigned to the user area.*1 1: The address range from 0001 7000_H to 0001 $7FFF_H$ is assigned to the area where the firmware is stored. (The portion of the Code Flash memory other than above is reserved.)

Note 1. The address range from 0103 7000_H to 0103 $7FFF_H$ is assigned to the area where the firmware is stored.

4.25 SELFID0 to SELFID3 — Self-Programming ID Input Registers 0 to 3

SELFID is for the input of an ID for use in authentication at the time of self-programming. The ID is authenticated by comparing the 128-bit ID that has been set in advance in a particular range of flash memory with the value in the SELFID0 to SELFID3 registers. The ID which is stored in a particular range of the flash memory can be set by the configuration setting command for the FACI.

Access: This register can be read/written in 32-bit units.

Address: FFA0 8000_H (SELFID0)
FFA0 8004_H (SELFID1)
FFA0 8008_H (SELFID2)
FFA0 $800C_H$ (SELFID3)

Value after reset: 0000 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SELFIDn[31:16]*1															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SELFIDn[15:0]*1															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note 1. n = 0 to 3

Table 4.28 SELFID0 to SELFID3 Register Contents

Bit Position	Bit Name	Function
31 to 0	SELFIDn[31:0]	ID for Use in Authentication of Self-Programming The ID for use in authentication at the time of self-programming is input to these bits. Authentication of the ID is executed by comparing the 128-bit ID that has been set in advance in a particular range of flash memory with the value in the SELFIDn[31:0] bits. The 128-bit ID is arranged in the respective sets of SELFIDn[31:0] bits in the way listed below. ID[31:0]: SELFID0[31:0] ID[63:32]: SELFID1[31:0] ID[95:64]: SELFID2[31:0] ID[127:96]: SELFID3[31:0]

4.26 SELFIDST — Self-Programming ID Authentication Status Register

SELFIDST indicates the result of authentication of an ID at the time of self-programming. That is, the SELFIDST register indicates the result of comparing the 128-bit ID that has been set in advance in a particular range of flash memory with the value in the SELFID0 to SELFID3 registers. The ID which is stored in a particular range of the flash memory can be set by the configuration setting command for the FACI.

Access: This register can only be read in 8-, 16-, or 32-bit units.

Address: FFA0 8010_H

Value after reset: 0000 $000X_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IDST
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 4.29 SELFIDST Register Contents

Bit Position	Bit Name	Function
31 to 1	Reserved	When read, the value after reset is read.
0	IDST	ID Authentication Status This bit indicates the result of comparing the 128-bit ID that has been set in advance in a particular range of flash memory with the value in the SELFID0 to SELFID3 registers. 0: The IDs match (ID-based security is unlocked). 1: The IDs do not match (ID-based security is locked).

4.27 Other Registers Related to Protecting the Flash Memory against Programming and Erasure

Other registers related to protecting the flash memory against programming and erasure are listed in **Table 4.30**.

Table 4.30 Other Registers Related to Protecting the Flash Memory against Programming and Erasure

Register Name	Symbol	R/W	Initial Value	Address	Access Size
FHVE15 control register	FHVE15	R/W	0000 0000_H	FFF8 $A430_H$	32
FHVE3 control register	FHVE3	R/W	0000 0000_H	FFF8 2410_H	32

For details, see the User's Manual: Hardware.

Section 5 Flash Sequencer Modes

5.1 Operating Modes of the Flash Sequencer

The flash sequencer has three operating modes as shown in **Figure 5.1**. The mode is shifted by the write to the FENTRYR register.

When the FENTRYR register is 0000_H, the flash sequencer is in read mode. In this mode, it does not accept the FACI command. The code flash memory and the data flash memory are both readable.

When the FENTRYR register is 0001_H, the flash sequencer is in code flash programming/erasure mode where the code flash memory can be programmed/erased by the FACI command. In this mode, the data flash memory is not readable. In addition, the code flash memory is not readable under the condition where the BGO operation is disabled. Under the condition where the BGO operation is enabled, the code flash memory is readable. As for the condition to enable the BGO operation, refer to the user's manual for this product.

When the FENTRYR register is 0080_H, the flash sequencer is in data flash programming/erasure mode where the data flash memory can be programmed/erased by the FACI command. In this mode, the data flash memory is not readable. However, the code flash memory is readable.

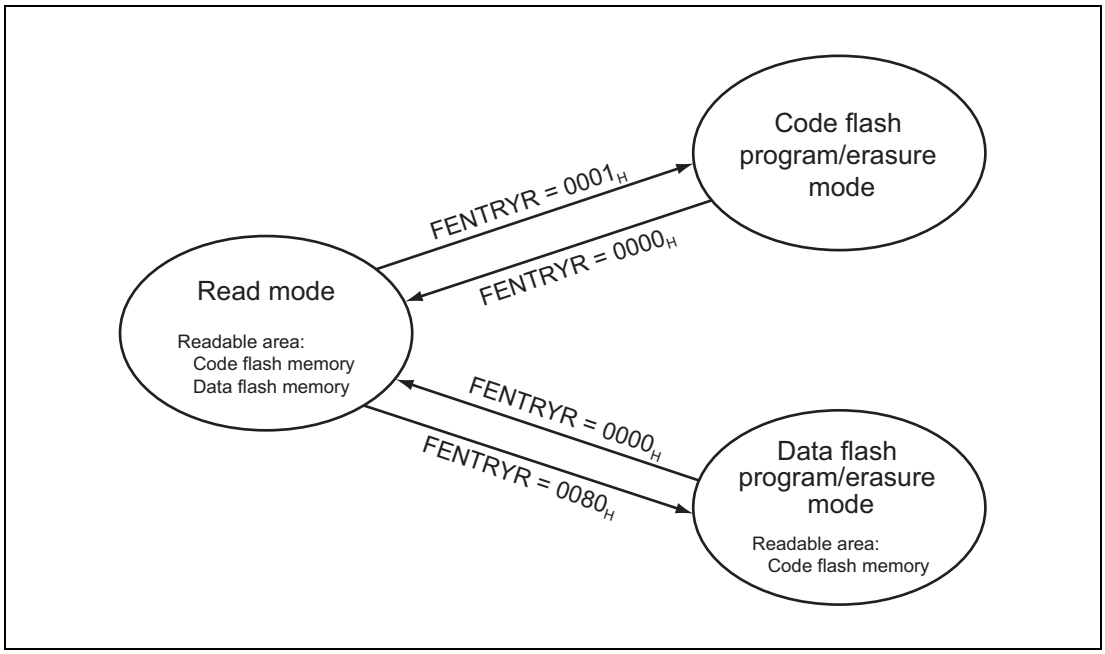


Figure 5.1 Flash Sequencer Modes

Section 6 FACI Command

6.1 List of FACI Commands

Table 6.1 List of FACI Commands

FACI Command	Function
Programming	User area and data area can be programmed. The unit of programming is 256 bytes for user area. The unit of programming is 4 bytes for data area.
DMA Programming	Data area can be programmed by linkage with the DMA controller. The unit of programming is 4 to 64 Kbytes (specified in 4-byte units).
Block Erase	User area, lock bit, and data area can be erased. The unit of erasing is one block.
Programming/Erasure Suspend	“Programming” or “Erasure” command operation can be suspended.
Programming/Erasure Resume	Suspended “Programming” or “Erasure” command operation can be resumed.
Status Clear	FSTATR.OTPDTCT, OTPCRCT, ILGLERR, ERSERR, PRGERR, CFGDTCT, CFGCRCT, TBLDTCT, TBLCRCT bits are initialized and flash sequencer is released from the command-locked state.
Forced Stop	FACI command operation is forcibly stopped and the FSTATR register is initialized.
Blank Check	Data area can be checked. The unit of blank checking is 4 to 64K bytes (4 bytes step).
Configuration Set	ID, security function, safety function, and option byte are set. The unit of programming is 16 bytes.
Lock Bit Programming	The lock bit for user area is programmed. The unit of programming is one bit (the lock bit for one block).
Lock Bit Read	The lock bit for user area is read out and stored in the FLKSTAT register. The unit of reading is one bit (the lock bit for one block).
OTP (One Time Programming) Set	OTP is selected for the user area or user boot area. The unit of setting is 16 bytes (OTP settings for 128 blocks).

The FACI commands are issued by the write access to the FACI command issue area (see **Table 3.1**). When the write access as shown in **Table 6.2** is issued in the specified state, the flash sequencer executes the processing corresponding to each command (see **Section 6.2, Relationship between Flash Sequencer Status and FACI Commands**).

Table 6.2 Flash Sequencer Command Format

FACI Command	Number of write access	Write Data to "FACI Command Issue Area"			
		1st access	2nd access*1	3rd to (N+2)th access	(N+3)th access
Programming (user area) 256-byte programming: N = 128	131	$E8_H$	80_H (=N)	WD_1 to WD_{128}	$D0_H$
Programming (data area) 4-byte programming: N = 2	N+3	$E8_H$	02_H (=N)	WD_1 to WD_N	$D0_H$
DMA Programming N = 2 to 32768 (even number only)	N+2	EA_H	N	WD_1 to WD_N	—
Block Erase	2	20_H	$D0_H$	—	—
Programming/Erasure Suspend	1	$B0_H$	—	—	—
Programming/Erasure Resume	1	$D0_H$	—	—	—
Status Clear	1	50_H	—	—	—
Forced Stop	1	$B3_H$	—	—	—
Blank Check	2	71_H	$D0_H$	—	—
Configuration Set N = 8	11	40_H	08_H (=N)	WD_1 to WD_8	$D0_H$
Lock Bit Programming	2	77_H	$D0_H$	—	—
Lock Bit Read	2	71_H	$D0_H$	—	—
OTP Set N = 8	11	45_H	08_H (=N)	WD_1 to WD_8	$D0_H$

Note: WD_N (N = 1, 2,…): Nth 16-bit data to be programmed.

Note 1. For a command other than the DMA programming command, 8-bit data is written. For the DMA programming command, 16-bit data is written.

The flash sequencer clears the FRDY bit of the FSTATR register to 0 when the processing for a command other than the status clear command is started, and sets the FRDY bit to 1 when the command processing finishes (see **Section 4.6, FSTATR — Flash Status Register**).

If the FRDY bit changes from 0 to 1, a flash ready (FRDY) interrupt occurs.

6.2 Relationship between Flash Sequencer Status and FACI Commands

The FACI commands are accepted according to the mode/state of the flash sequencer. The FACI command should be issued after the shift of the flash sequencer to the code flash programming/erasure mode or data flash programming/erasure mode and checking that the flash sequencer has shifted to the mode. To check the state of flash sequencer, use the FSTATR and FASTAT registers. In addition, error occurrence can be checked by the CMDLK bit in the FASTAT register. It is the logical OR of the OTPDTCT/ILGLERR/ERSERR/PRGERR/FLWEERR/CFGDTCT/TBLDTCT/FRDTCT bits of the FSTATR register.

Table 6.3 summarizes available flash sequencer commands in each operating mode.

Table 6.3 Flash Sequencer Operation Mode and Available Commands

Operating Mode	FENTRYR	Available Command
Read mode	0000_H	No command is available.
Code flash programming/erasure mode	0001_H	“Programming” “Block Erase” “Programming/Erasure Suspend” “Programming/Erasure Resume” “Status Clear” “Forced Stop” “Lock Bit Programming” “Lock Bit Read”
Data flash programming/erasure mode	0080_H	“Programming” “DMA programming” “Block Erase” “Programming/Erasure Suspend” “Programming/Erasure Resume” “Status Clear” “Forced Stop” “Blank Check” “Configuration Set” “OTP Set”

Table 6.4 shows the flash sequencer state and the acceptable FACI commands. The table assumes appropriate flash sequencer operation mode is set before issuing the command.

Table 6.4 Flash Sequencer State and Acceptable FACI Commands

	"Programming" or "Erasure" command processing	"Configuration Set" or "OTP Set" command processing	"Programming" or "Erasure" command suspension processing	"Blank Check" or "Lock Bit Read" command processing	"DMA Programming" command processing	While "Programming" command is suspended	While "Erasure" command is suspended	"Programming" command processing while "Erasure" command is suspended	Command-locked state (FRDY = 1)	Command-locked state (FRDY = 0)	"Lock Bit Programming" command processing	"Forced Stop" command processing	Other
FRDY bit	0	0	0	0	0	1	1	0	1	0	0	0	1
SUSRDY bit	1	0	0	0	0	0	0	0	0	0	0	0	0
ERSSPD bit	0	0	0/1	0/1	0	0	1	1	0/1	0/1	0	0	0
PRGSPD bit	0	0	0/1	0/1	0	1	0	0	0/1	0/1	0	0	0
CMDLK bit	0	0	0	0	0	0	0	0	1	1	0	0	0
Programming	—	—	—	—	—	—	√ *3	—	—	—	—	—	√
DMA programming	—	—	—	—	—	—	√ *1, *3	—	—	—	—	—	√ *1
Block Erase	—	—	—	—	—	—	—	—	—	—	—	—	√
Programming/Erasure Suspend	√	—	—	—	—	—	—	—	X	—	—	—	X
Programming/Erasure Resume	—	—	—	—	—	√	√	—	—	—	—	—	—
Status Clear	—	—	—	—	—	√	√	—	√	—	—	—	√
Forced Stop	√	√	√	√	√	√	√	√	√	√	√	√	√
Blank Check	—	—	—	—	—	√ *1	√ *1	—	—	—	—	—	√ *1
Configuration Set	—	—	—	—	—	—	—	—	—	—	—	—	√ *1
Lock Bit Programming	—	—	—	—	—	—	—	—	—	—	—	—	√ *2
Lock Bit Read	—	—	—	—	—	√ *2	√ *2, *4	—	—	—	—	—	√ *2
OTP Set	—	—	—	—	—	—	—	—	—	—	—	—	√ *1

√: Acceptable, —: Not acceptable (due to the command-locked state), X: Ignored

Note 1. Acceptable only in data flash programming/erasure mode.
Note 2. Acceptable only in code flash programming/erasure mode.
Note 3. Acceptable when programming area is other than erase suspending sector.
Note 4. Undefined value is read out when lock bit read command is issued to erase suspending sector.

6.3 Use FACI Command

This section describes the overview of FACI command usage.

6.3.1 Overview of the Command Usage in Code Flash P/E Mode

The overview of the FACI command usage in code flash programming/erasure mode is shown below. **Table 6.3** lists the available commands in code flash programming/erasure mode. Note that security should be released by ID authentication before FACI commands are used for code flash memory.

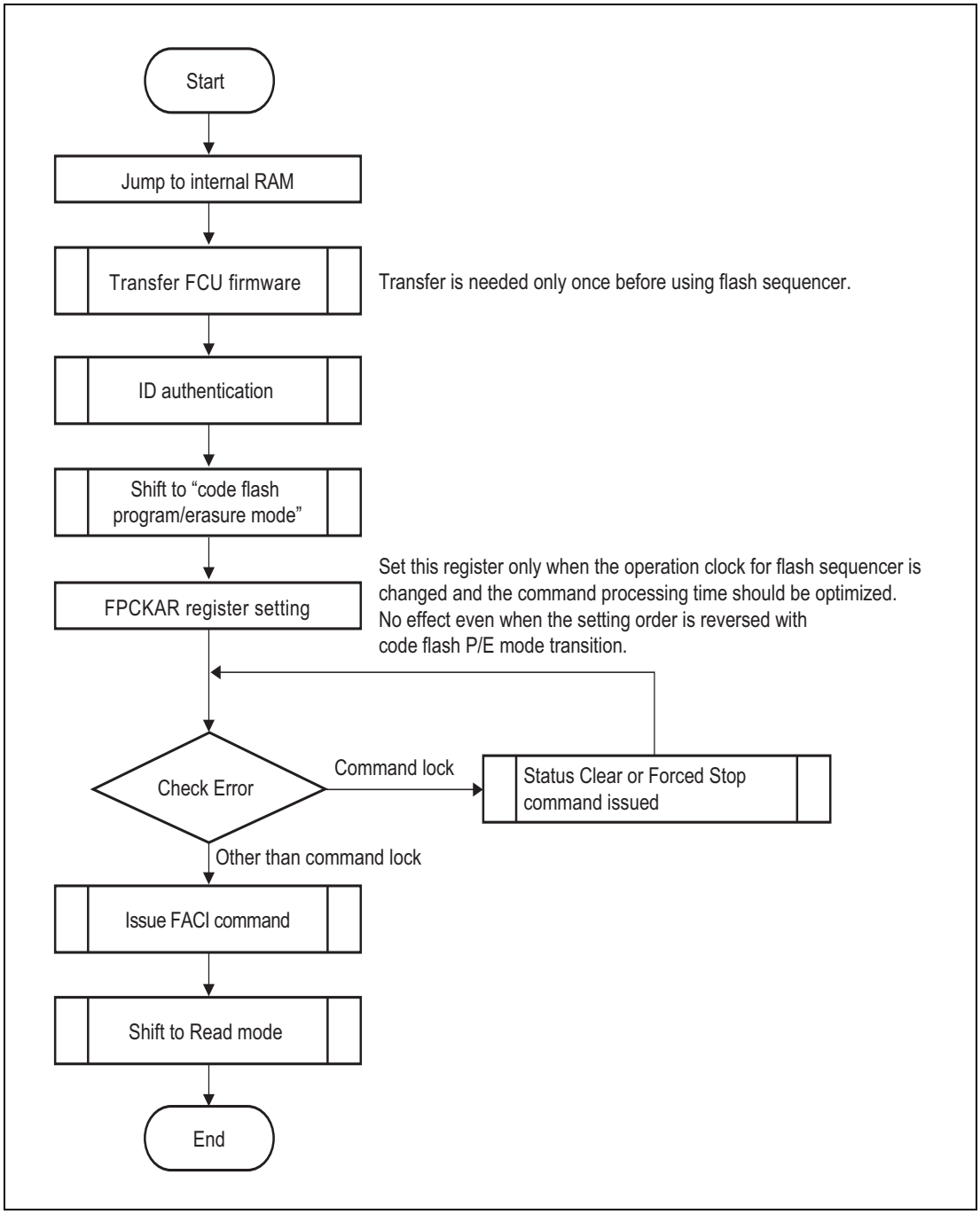


Figure 6.1 Overview of Command Usage in Code Flash Programming/Erasure Mode

6.3.2 Overview of the Command Usage in Data Flash P/E Mode

The overview of the FACI command usage in data flash programming/erasure mode is shown below. As for the available commands in data flash programming/erasure mode, refer to **Table 6.3**.

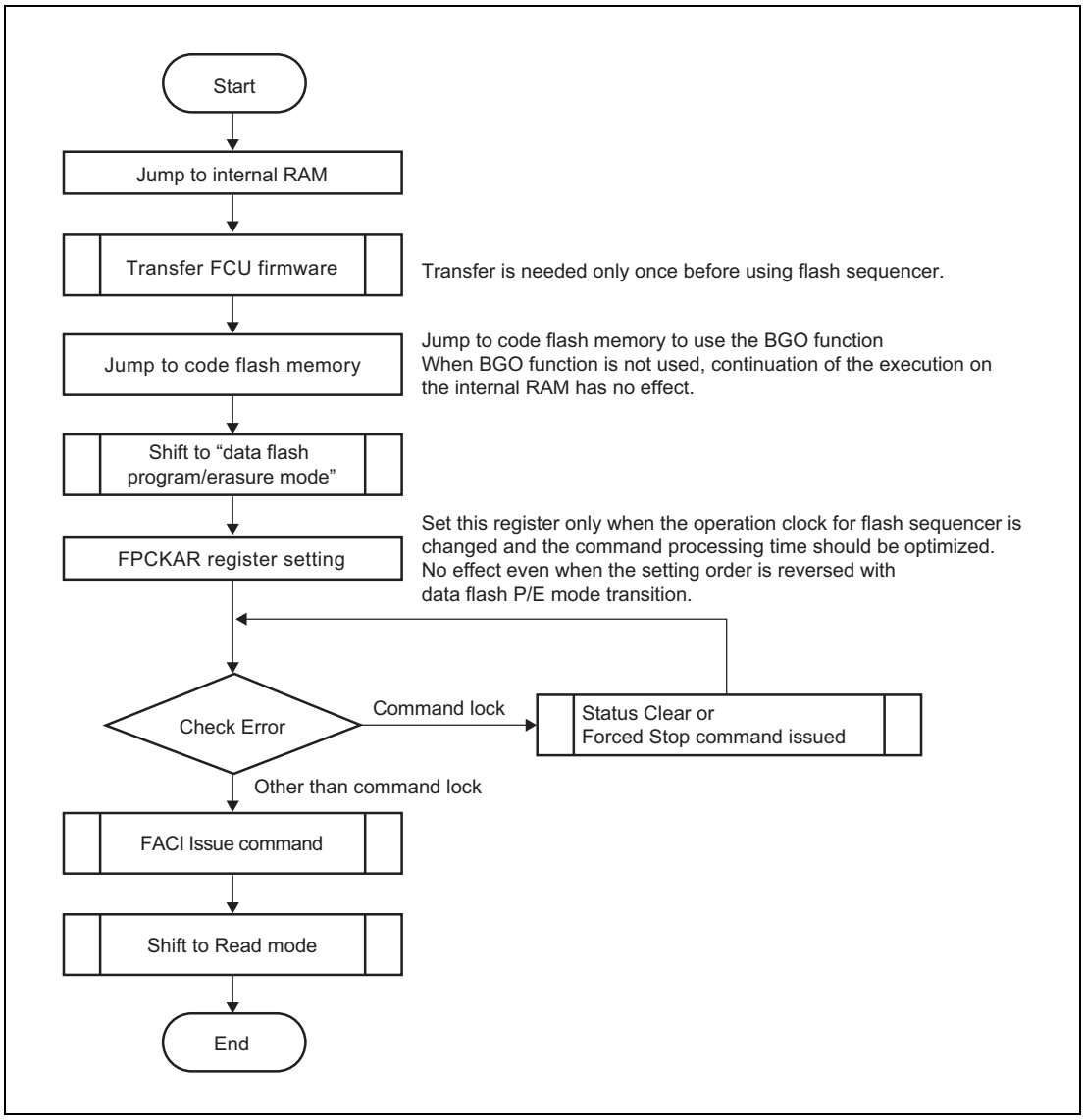


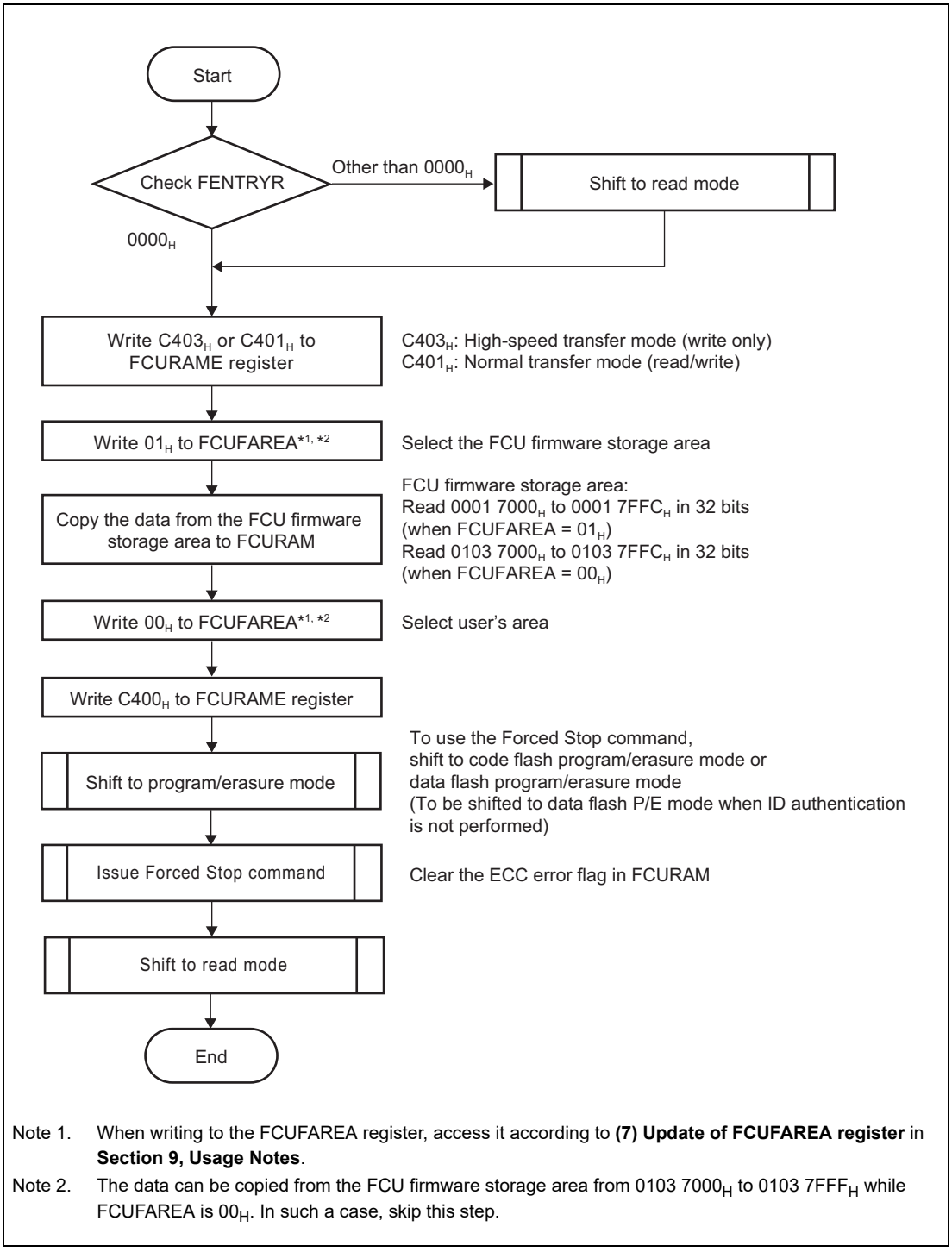
Figure 6.2 Overview of Command Usage in Data Flash Programming/Erasure Mode

6.3.3 FCU Firmware Transfer

To use the flash sequencer, the FCU firmware should be stored in FCURAM. As the FCU firmware is not stored in FCURAM at power on, it is required to copy the FCU firmware from the FCU firmware storage area to FCURAM. This copy operation is required only once before the flash sequencer is used. You do not have to update FCURAM again because executing the FACI command does not update FCURAM.

As the FCURAM storage data is undefined at power on, an ECC error is generated by the write to FCURAM. After copying the FCU firmware, issue Forced Stop command to initialize the FRCRCT and FRDTCT bits in the FSTATR register. In this case, reloading the FCU firmware after issuance of the forced end command is unnecessary.

Processing of a “Forced Stop” command is all implemented in the hardware. Before the FCU firmware is stored or when copying of the firmware is completed unsuccessfully, it is possible to execute “Forced Stop” command normally. In addition, an ECM “flash access error” source is generated by an ECC error in the FCURAM. Clear the error source by writing 1 to the ECMCLSSE106 bit in the ECMESSTC1 register. The ECMESSTC1 register is protected against unauthorized writing.



Note 1. When writing to the FCUFAREA register, access it according to **(7) Update of FCUFAREA register** in **Section 9, Usage Notes**.

Note 2. The data can be copied from the FCU firmware storage area from 0103 7000H to 0103 7FFFH while FCUFAREA is 00H. In such a case, skip this step.

Figure 6.3 Transfer Flow of FCU Firmware

Figure 6.4 shows the configuration of the FCU firmware. The area from FCU_BASE + 0001 7000_H to #CODE_END holds the instruction codes to be executed by the FCU. The area from #CODE_END + 4 to FCU_BASE + 0001 $7FF7_H$ is reserved. In addition, when copying the data from the FCU firmware storage area to FCURAM, it is necessary to copy 4-Kbyte data including the reserved area. Location FCU_BASE + 0001 $7FF8_H$ holds the number of bytes in the code area divided by 4. Location FCU_BASE + 0001 $7FFC_H$ holds a checksum, which is the two-byte result of adding all values in the code area. After the FCU firmware is transferred to the FCURAM from the FCU firmware storage area, check the contents of the FCURAM by calculating the checksum of the code area (FFA1 2000_H to #CODE_END_RAM) in the FCURAM and comparing it with the checksum stored at address FCU_BASE + 0001 $7FFC_H$ of the FCU firmware storage area.

NOTE

FCU_BASE depends on the setting of the FCUFAREA.FCUFSEL bit.

- When FCUFAREA.FCUFSEL is 0_B, FCU_BASE = 0102 0000_H
- When FCUFAREA.FCUFSEL is 1_B, FCU_BASE = 0000 0000_H

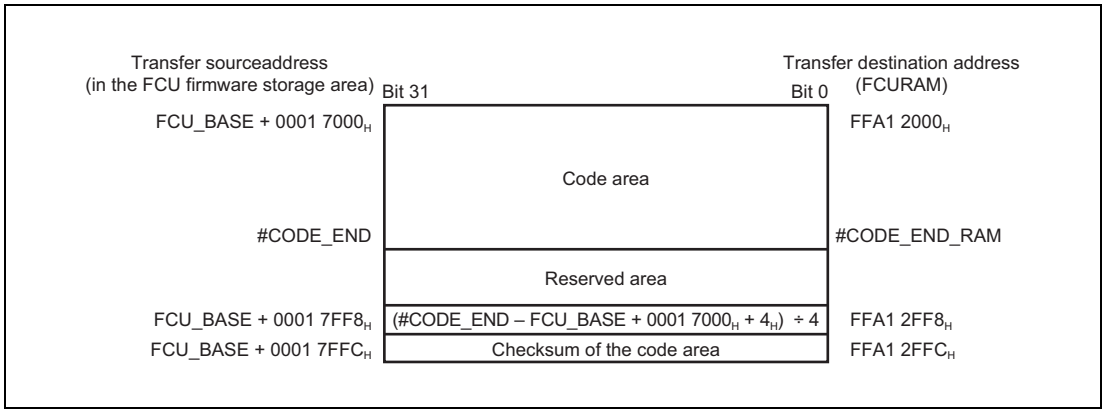


Figure 6.4 Configuration of FCU Firmware

6.3.4 Shift to Code Flash Programming/Erasure Mode

To use the FACI commands relating the code flash memory, operation should be shifted to the code flash programming/erasure mode. Set the FENTRYRC bit in the FENTRYR to 1 to shift to the code flash programming/erasure mode.

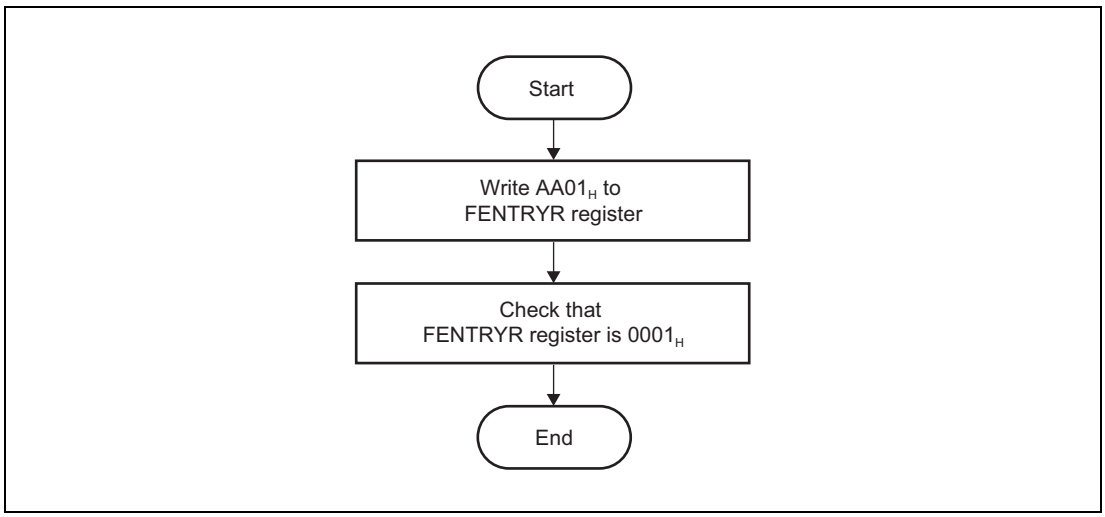


Figure 6.5 Flow of Shift to Code Flash Programming/Erasure Mode

6.3.5 Shift to Data Flash Programming/Erasure Mode

To use the FACI commands relating the data flash memory, operation should be shifted to the data flash programming/erasure mode. Set the FENTRYRD bit in the FENTRYR to 1 to shift to the data flash programming/erasure mode.

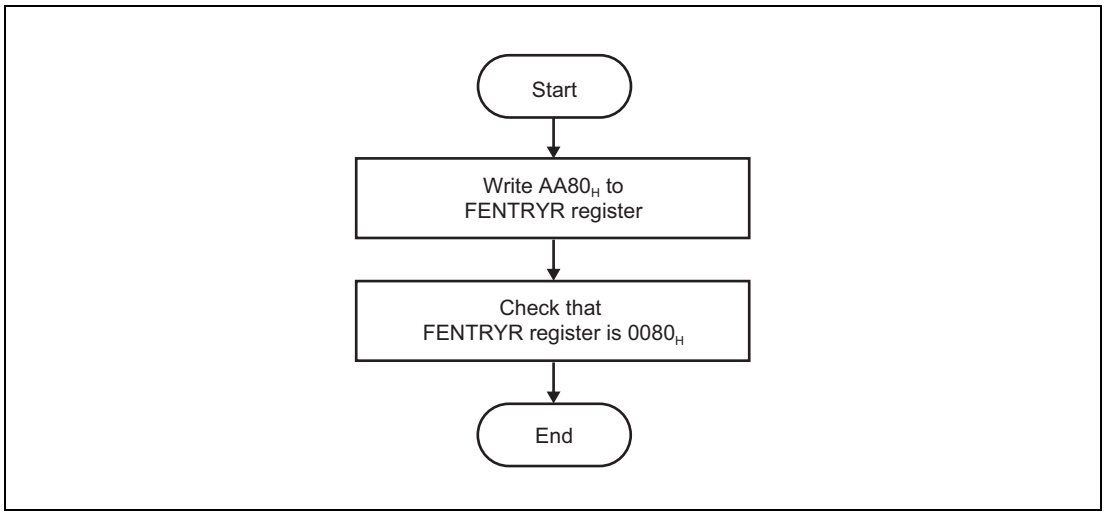
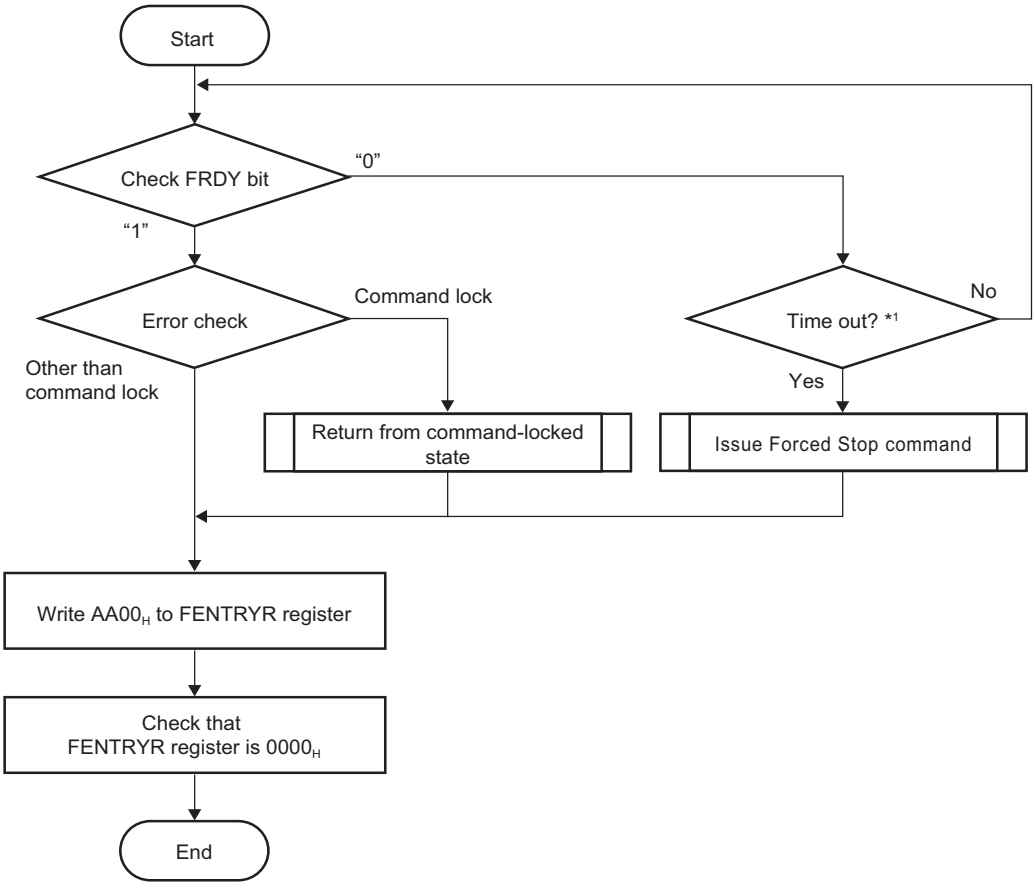


Figure 6.6 Flow of Shift to Data Flash Programming/Erasure Mode

6.3.6 Shift to Read Mode

To read the flash memory without using the BGO function, the operation should be shifted to the read mode. To shift to the read mode, set the FENTRYR register to 0000_H. When entering the read mode, the flash sequencer processing should be completed and the operation is in other than the command-locked state.



Note 1. The time reaching 634 ms is judged as a timeout.

Figure 6.7 Flow of Shift to Read Mode

6.3.7 ID Authentication

To use the FACI command in code flash programming/erasure mode, release from the security by ID authentication and write 0 to the SELFIDST.IDST bit. When the IDST bit is 1, the FACI command is not accepted. **Figure 6.8** shows the ID compare method using SELFID0 to SELFID3, and how the compare result is checked by SELFIDST.

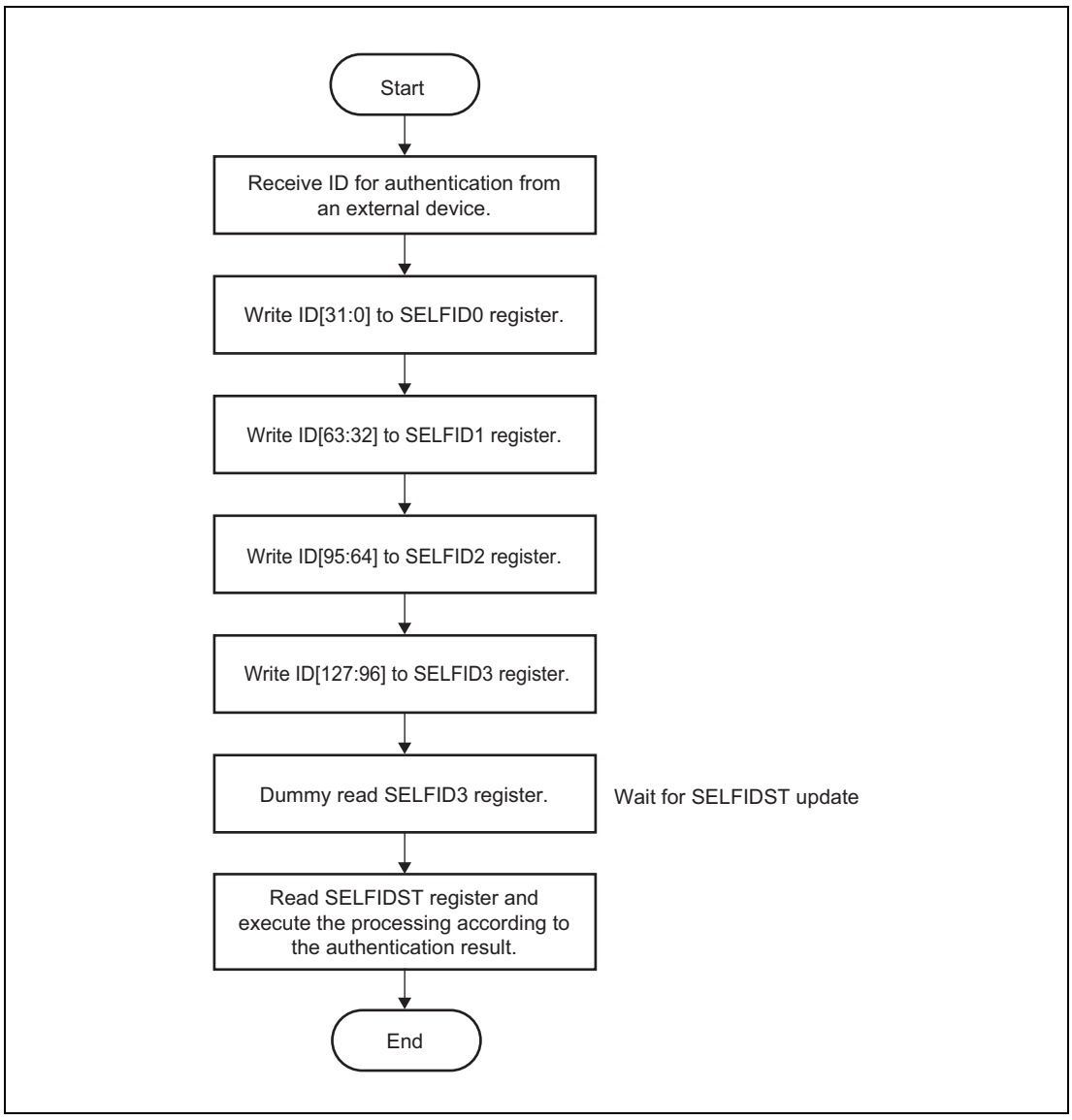


Figure 6.8 Flow of ID Compare

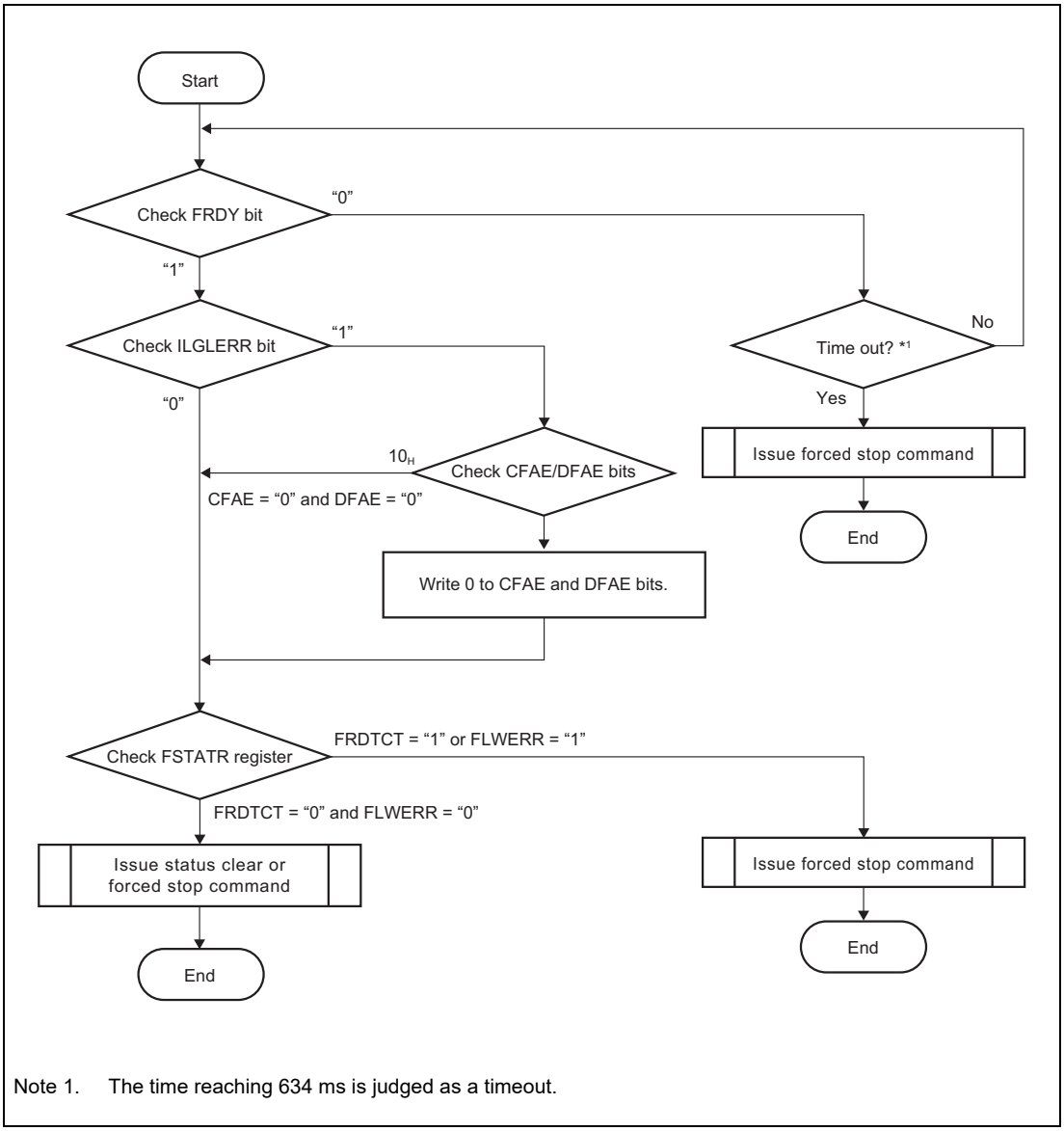
6.3.8 Return from Command-Locked State

When the flash sequencer enters the command-locked state, FACI commands cannot be accepted. To release the command-locked state, use the status clear command, forced stop command, or FASTAT register.

When the command-locked state is detected by checking an error before issuing the programming/erasure suspend command, the FRDY bit in the FSTATR register may hold 0 without completing the command processing. If the processing is not completed within the maximum programming/erasure time specified by electrical characteristics, it is determined as time out and the flash sequencer should be stopped by the forced stop command.

When the ILGLERR bit in the FSTATR register is 1, check the FASTAT value. If the CFAE or DFAE bit in the FASTAT register is 1, the command-locked state cannot be released by the status clear or forced stop command.

The FRDTCT and FLWERR bits in the FSTATR register are not changed from 1 to 0 by the status clear command. When these bits are set to 1, use the forced stop command to release the command-locked state. The other bits to be the source for locking commands can be changed from 1 to 0 by the status clear or forced stop command.



Note 1. The time reaching 634 ms is judged as a timeout.

Figure 6.9 Return from Command-Locked State

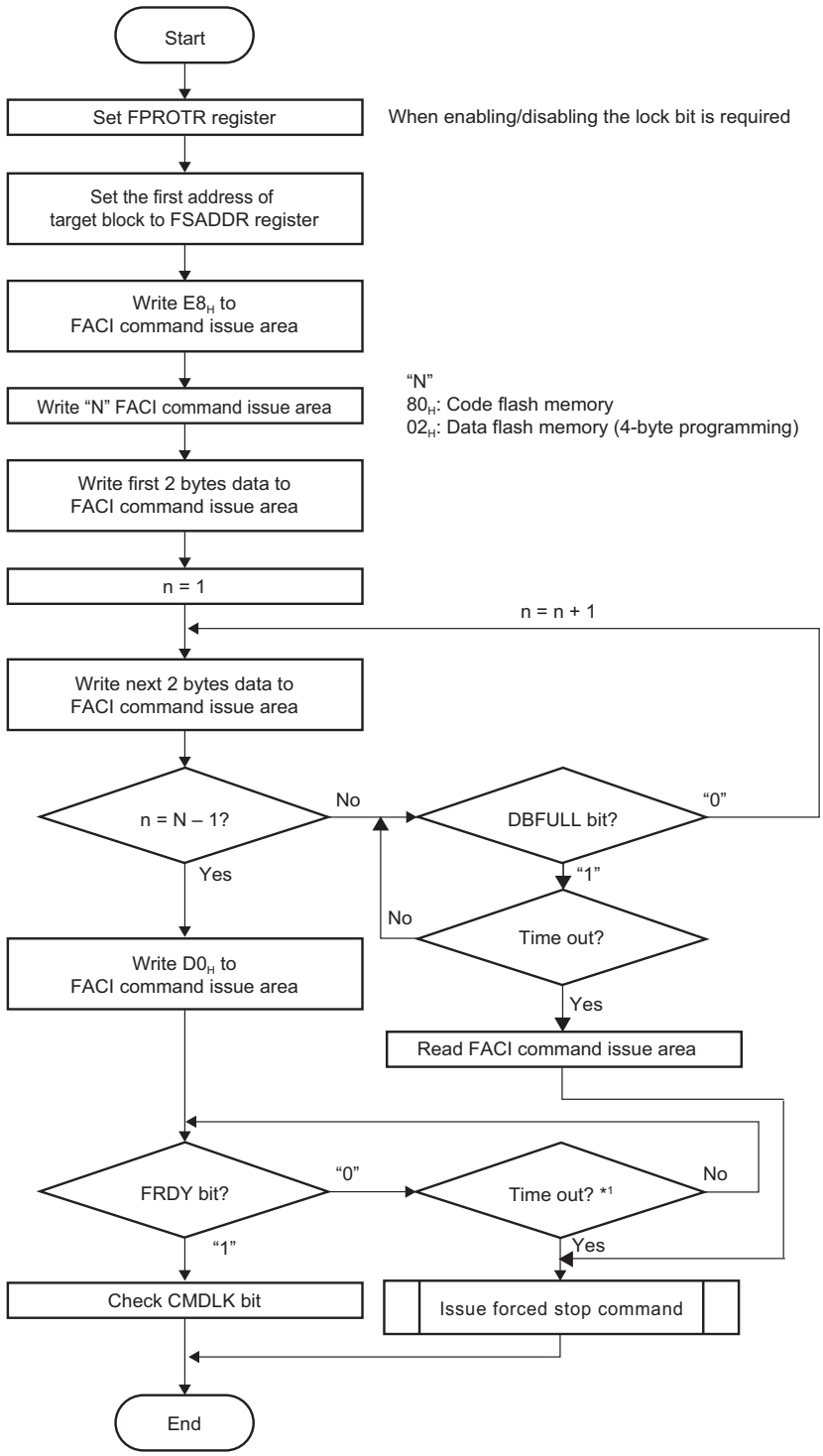
6.3.9 Issuing the Programming Command

The programming command is used to write to user area and data area.

Before issuing the programming command, set the first address of target block to the FSADDR register. Writing $D0_H$ to the FACI command issue area at the final access of the FACI command issue starts the programming command processing. If the target area of programming command processing contains the area not for writing, write $FFFF_H$ to the corresponding area.

Set the FPROTR register before issuing the programming command. To set the FPROTR register is required to switch enabling/disabling the lock bit.

If issuing the programming command is kept while the FACI internal data buffer is full, wait is generated in the peripheral bus and it may affect the communication performance of other peripheral IPs. To avoid the wait generation, the DBFULL bit in FSTATR should be 0 when FACI commands are issued. In addition, writing to data area does not make the data buffer full.



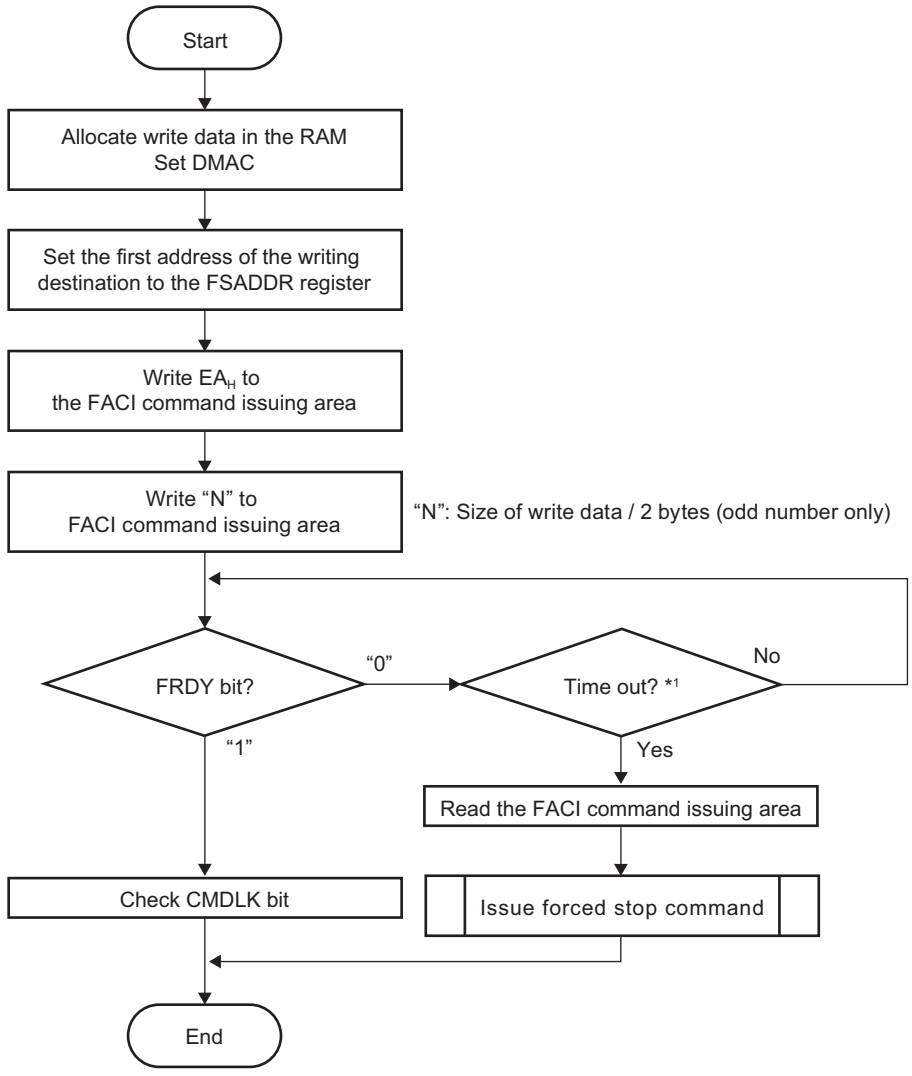
Note 1. For the code flash memory, the time of 256-byte programming (see *Code Flash Programming Characteristics* in *Section 39.6, Code Flash Characteristics*, in *the RH850/C1M-A User's Manual: Hardware*) reaching 1.1 times is judged as a timeout. For the data flash memory, the time of 4-byte programming (see *Data Flash Programming Characteristics* in *Section 39.7, Data Flash Characteristics*, in *the RH850/C1M-A User's Manual: Hardware*) reaching 1.1 times is judged as a timeout. If common processing is used, the time of 256-byte programming (the maximum time) of the code flash memory reaching 1.1 times is judged as a timeout.

Figure 6.10 Programming Command Usage

6.3.10 DMA Programming Command

The DMA programming command is used to write multiple 4-byte data sets (which is transferred from DMAC) to the data area, reducing CPU load caused by a large amount of serially written data.

Before issuing the DMA programming command, set the first address of the writing destination to the FSADDR register. Also, allocate (in the RAM) the data to be written, and set DMAC to enable DMA transfer from the relevant area to the FACI command issue area. FACI requests DMAC to transfer data immediately after the DMA programming command is received and each time 4-byte data writing finishes. Set DMAC to transfer 2-byte data twice for one data transfer request. For details about how to use DMAC, see the user's manual for the relevant product.



Note 1. Judged based on the sum of the time of 4-byte programming of the data flash memory (the maximum time: see *Data Flash Programming Characteristics* in *Section 39.7, Data Flash Characteristics*, in *the RH850/C1M-A User's Manual: Hardware*) x "N"/2 × 1.1 and the time required for DMA transfer of write data.

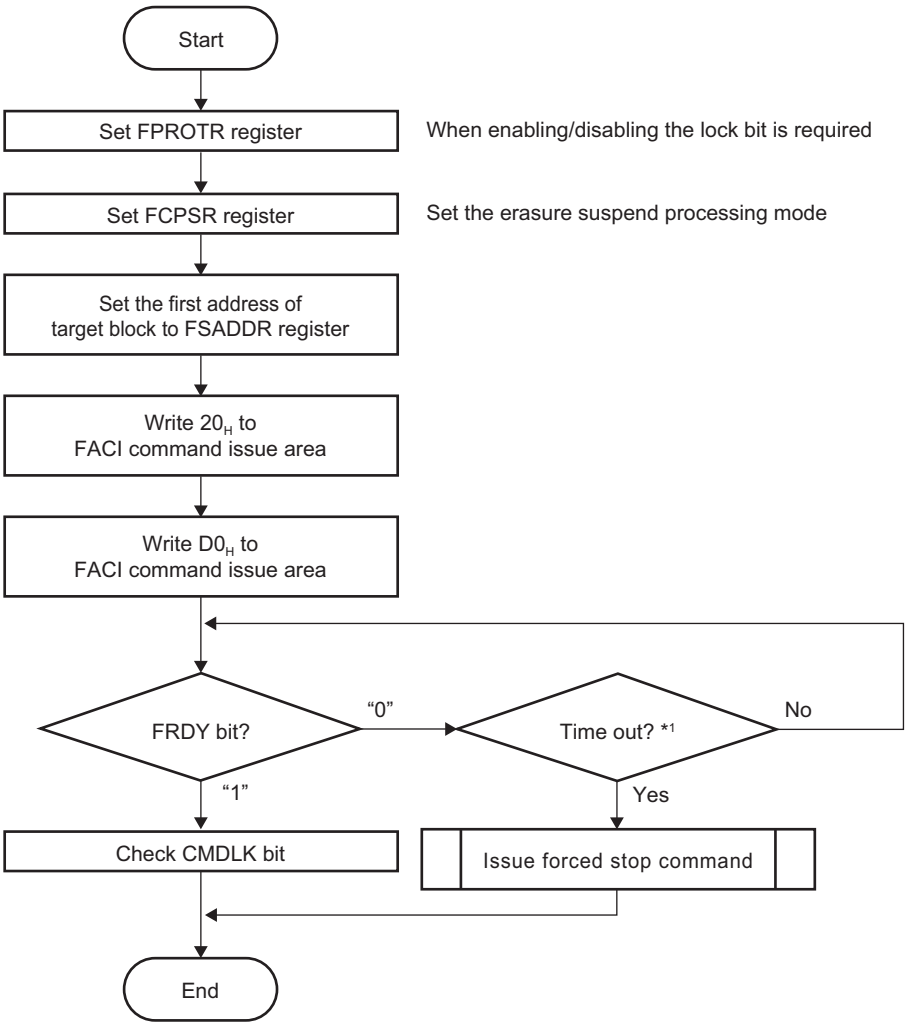
Figure 6.11 DMA Programming Command Usage

6.3.11 Block Erase Command

"Block Erase" command is used to erase the user area, lock bit, and data area.

Before issuing "Block Erase" command, set the first address of target block to the FSADDR register. Writing 20_H and $D0_H$ to the FACI command issue area starts the "Block Erase" command processing.

Set the FPROTR and FCPSR registers before issuing the "Block Erase" command. To set the FPROTR register is required to switch enabling/disabling the lock bit. To erase the lock bit, issue the "Block Erase" command while the FPROTCN bit in the FPROTR register is 1. To set the FCPSR register is required to switch the suspending method by the programming/erasure suspend command (suspend priority mode/erasure priority mode).



Note 1. For the code flash memory, the time of erasure of a 32-Kbyte block (the maximum time: see *Code Flash Programming Characteristics* in *Section 39.6, Code Flash Characteristics*, in *the RH850/C1M-A User's Manual: Hardware*) reaching 1.1 times is judged as a timeout. For the data flash memory, the time of erasure of a 64-byte block (the maximum time: see *Data Flash Programming Characteristics* in *Section 39.7, Data Flash Characteristics*, in *the RH850/C1M-A User's Manual: Hardware*) reaching 1.1 times is judged as a timeout. If common processing is used, the time of erasure of a 32-Kbyte block (the maximum time) of the code flash memory reaching 1.1 times is judged as a timeout.

Figure 6.12 Block Erase Command Usage

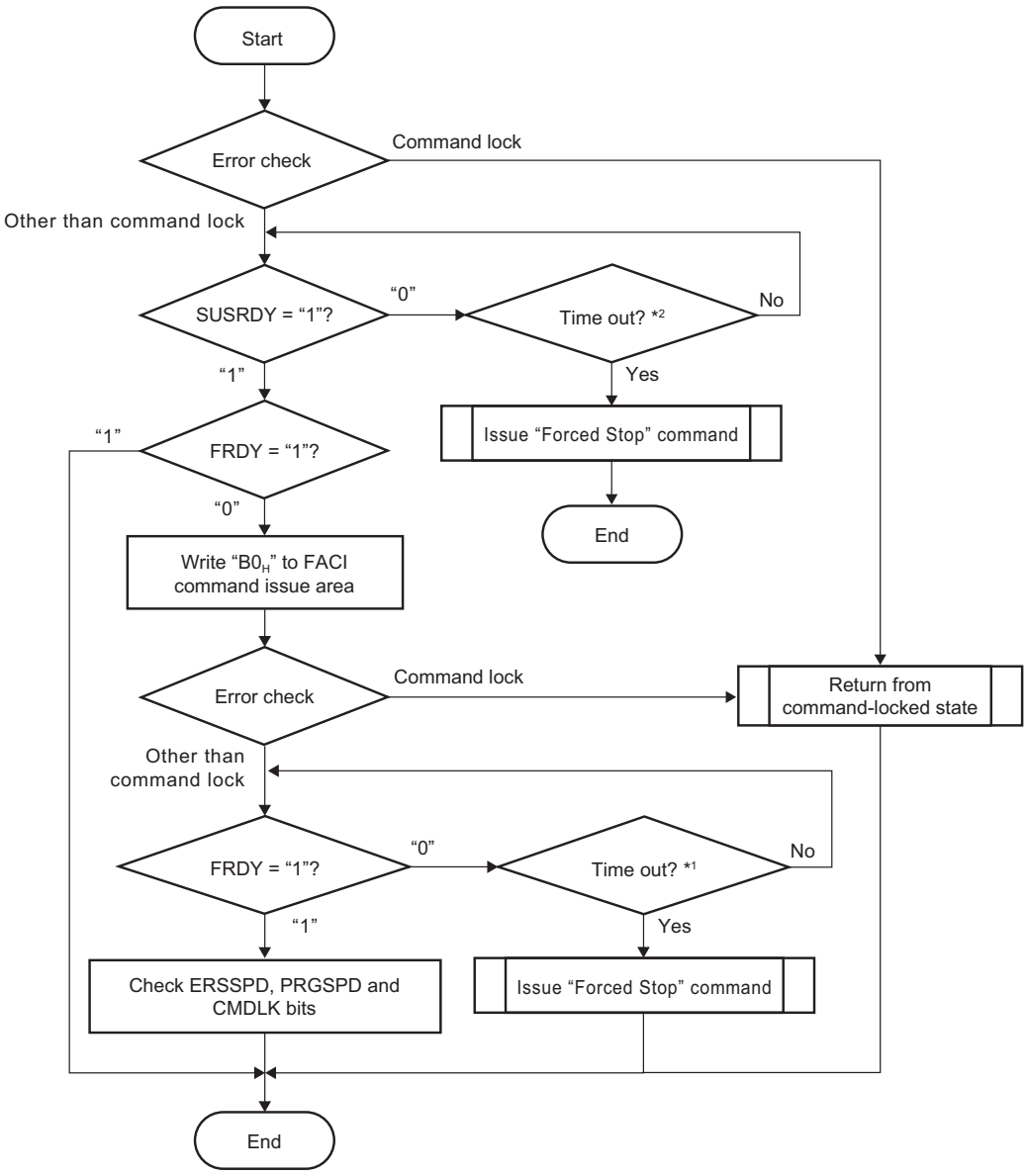
6.3.12 Programming/Erasure Suspend Command

"Programming/Erasure Suspend" command is used for suspending "Programming" or "Erasure" command processing. Before issuing "Programming/Erasure Suspend" command, check that CMDLK bit is "0" to ensure that "Programming" or "Erasure" command processing is being performed correctly. In addition, check that the SUSRDY bit is "1" to ensure that "Programming/Erasure Suspend" command is acceptable. After issuing "Programming/Erasure Suspend" command, check CMDLK bit to ensure no error has occurred.

If an error has occurred, the CMDLK bit is set to "1". If "Programming" or "Erasure" command processing is complete within the period from when the SUSRDY bit is ensured to be "1" until "Programming/Erasure Suspend" command is accepted, no error occurs, hence no transition to a suspended state (the FRDY bit is "1" and both ERSSPD and PRGSPD bits are "0").

Once "Programming/Erasure Suspend" command is accepted and "Programming" or "Erasure" command processing is normally suspended, flash sequencer enters a suspended state and that FRDY bit is "1" and ERSSPD or PRGSPD bit is "1". After issuing "Programming/Erasure Suspend" command and ensuring that flash sequencer has entered suspend state, determine which operation to perform in the succeeding process. If "Programming/Erasure Resume" command is issued in the succeeding process while flash sequencer has not entered a suspended state, an illegal command error occurs and flash sequencer shifts to the command-locked state.

When the operation shifts to the erase suspend state, writing to a block other than those targeted for erasure is enabled. In addition, when the FENTRYR register is cleared in the programming/erasure suspend state, the operation can shift to the read mode.



Note 1. The time reaching 1.87 ms is judged as a timeout.
Note 2. The time reaching 13 µs is judged as a timeout.

Figure 6.13 "Programming/Erasure Suspend" Command Usage

(1) Suspend programming command

If “Programming/Erase Suspend” command is issued while the flash memory is being programmed, the flash sequencer suspends programming. **Figure 6.14** gives an overview of operation for suspending programming. Upon accepting “Programming” command, the flash sequencer clears the FSTATR.FRDY bit to 0 and starts programming. Once the flash sequencer enters a state where it is ready to accept “Programming/Erasure Suspend” command after the start of programming, the FSTATR.SUSRDY bit is set to 1. If “Programming/Erase Suspend” command is issued, the flash sequencer accepts the command and clears the SUSRDY bit to 0. If the flash sequencer accepts “Programming/Erasure Suspend” command while applying a write pulse, the flash sequencer continues applying the pulse. After a specified pulse application time has elapsed, the flash sequencer completes applying the pulse, starts suspending the program, and sets the FSTATR.PRGSPD bit to 1.

Once the suspension process is complete, the flash sequencer sets the FRDY bit to 1 and enters programming suspended state. If the flash sequencer accepts “Programming/Erasure Resume” command in this state, the flash sequencer clears the FRDY and PRGSPD bits to 0 and restarts programming.

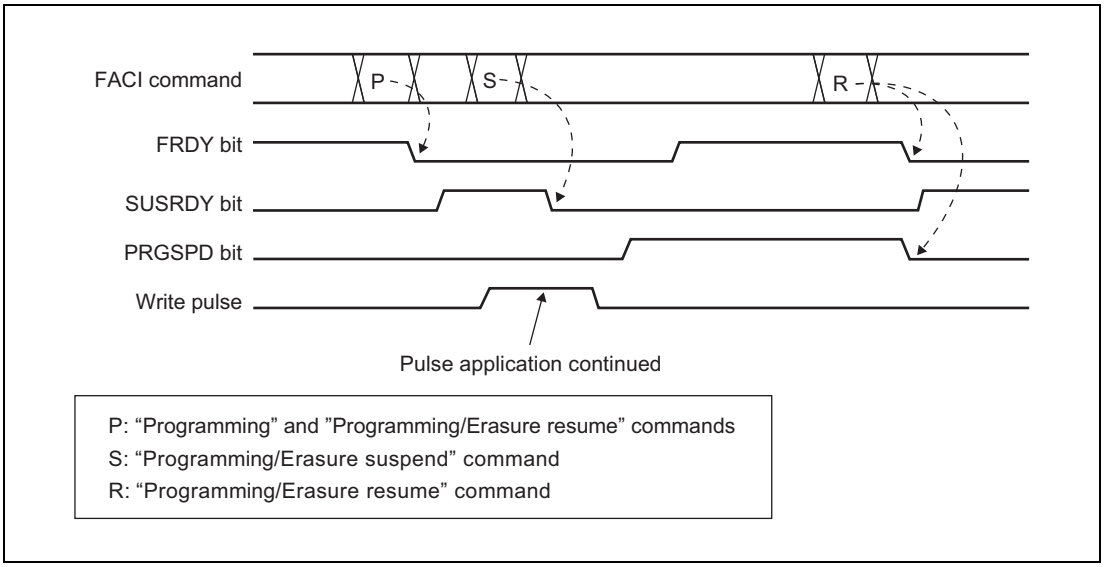


Figure 6.14 Suspend Programming Command

(2) Suspend erase command in suspension-priority mode

Suspension-priority mode is supported as a suspension method during erasure processing. **Figure 6.15** shows the operation for suspending “Erasure” command processing in suspension-priority mode (FCPSR.ESUSPMD = “0”). Upon accepting an “Erase” command, the flash sequencer clears the FSTATR.FRDY bit to 0 and starts erasing. Once FCU enters a state where it is ready to accept “Programming/Erase Suspend” command after the start of erasing, the FSTATR.SUSRDY bit is set to 1. If “Programming/Erase Suspend” command is issued, the flash sequencer accepts the command and clears the SUSRDY bit to 0. If the flash sequencer accepts a suspension command during its erasing operation, the flash sequencer starts a suspending process even while applying a pulse and sets the FSTATR.ERSSPD bit to 1. Once the suspending process is complete, the flash sequencer sets the FRDY bit to 1 and enters erasing suspended state. If the flash sequencer accepts “Programming/Erase Resume” command in this state, the flash sequencer clears the FRDY and ERSSPD bits to 0 and restarts erasing. The operations of FRDY, SUSRDY, and ERSSPD bits are independent of the erasure-suspended mode.

The setting for erasure-suspended mode affects the control methods for erasure pulse. In suspension-priority mode, if the flash sequencer accepts “Programming/Erase Suspend” command while applying an erasing pulse A, which has not been suspended previously, the flash sequencer suspends the pulse application and enters the erasure-suspended state. After the flash sequencer resumes erasing by accepting a “Programming/Erasure Resume” command, the flash sequencer accepts the “Programming/Erase Suspend” command while applying an erasing pulse A, the flash sequencer continues applying the pulse. After a specified pulse application time has elapsed, the flash sequencer completes applying the pulse and enters an erasure-suspended state. Next, after the flash sequencer accepts “Programming/Erasure Resume” command and starts applying a new pulse B, if the flash sequencer accepts “Programming/Erase Suspend” command again, the flash sequencer suspends the pulse application. In suspension-priority mode, application of the erasure pulse is suspended once every pulse application and suspension process takes precedence, delay caused by suspension can be minimized.

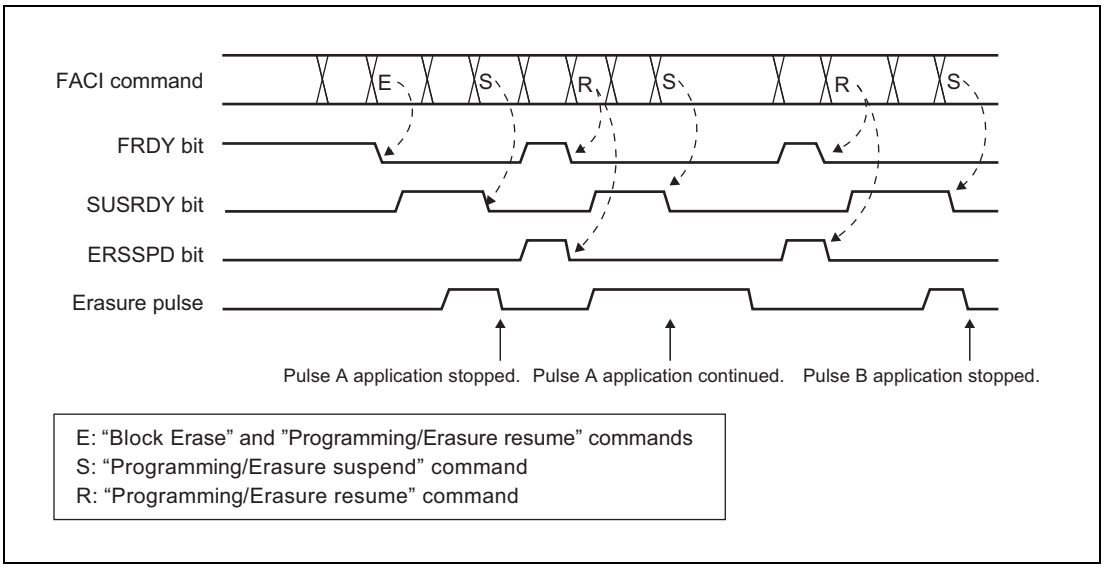


Figure 6.15 Suspend “Erase” Command (Suspension-Priority Mode)

(3) Suspend erase command in erasure-priority mode

Erasure-priority mode is supported as a suspension method during erasure processing. **Figure 6.16** shows the operation for suspending “Erasure” command processing in erasure-priority mode (FCPSR.ESUSPMD = 1). The control method of erasure pulse in erasure-priority mode is the same as that of programming pulse during programming suspension processing. In erasure-priority mode, if the flash sequencer accepts “Programming/Erasure Suspend” command while applying an erasing pulse, FCU always continues applying the pulse. As processing to reapply an erasing pulse never takes place in this mode, the total time required for “Erase” command processing is shorter than in suspension-priority mode.

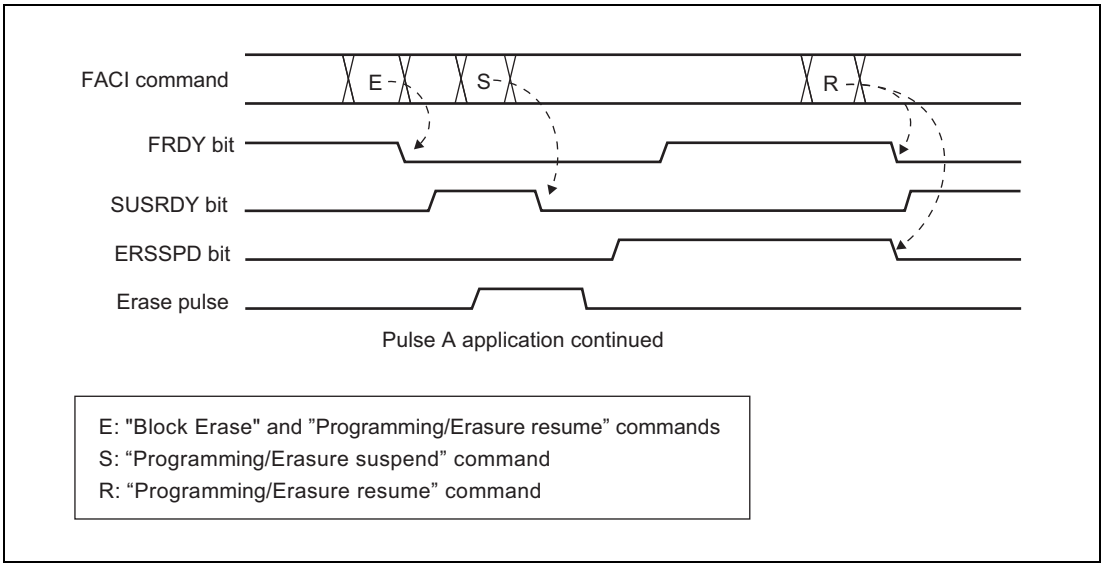
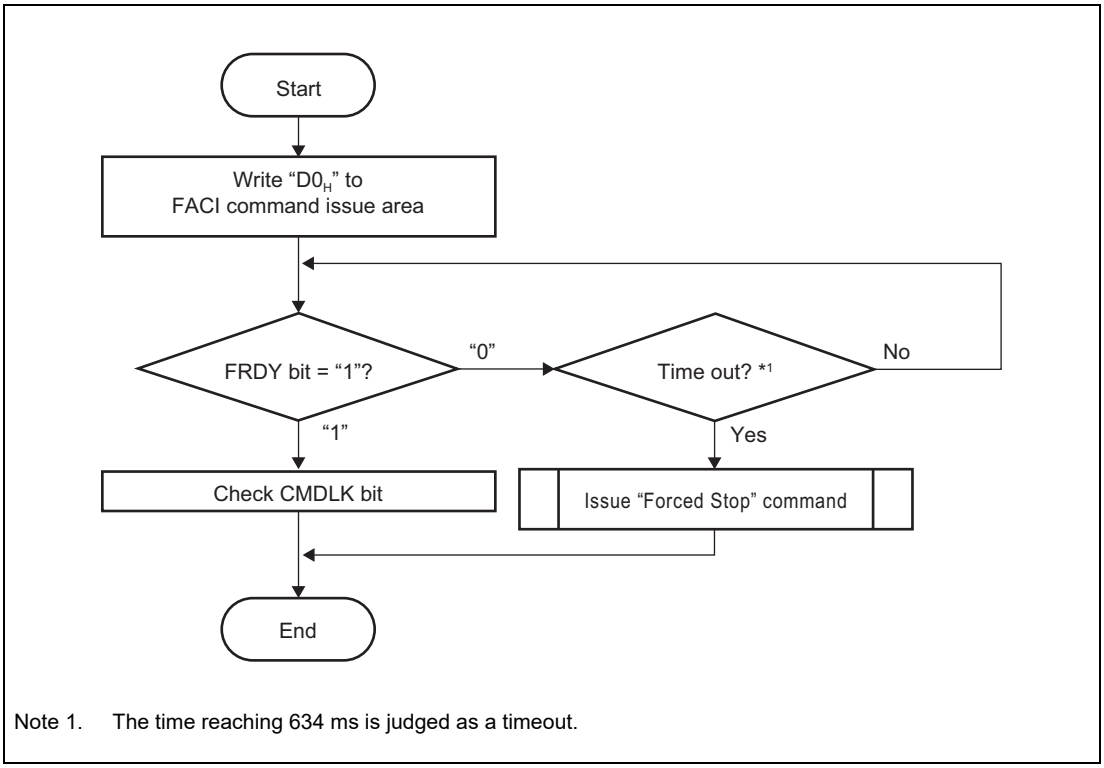


Figure 6.16 Suspend “Erase” Command (Erasure-Priority Mode)

6.3.13 Programming/Erasure Resume Command

"Programming /Erase Resume" command is used for resuming "Programming" or "Erasure" command processing that has been suspended. FENTRYR setting has been modified during suspension, issue "Programming/Erasure Resume" command only after resetting FENTRYR to the previous value that was held before the "Programming/Erasure Suspend" command was issued.



Note 1. The time reaching 634 ms is judged as a timeout.

Figure 6.17 "Programming/Erasure Resume" Command Usage

6.3.14 Status Clear Command

The status clear command is used to clear the command-locked state. (See **Section 6.3.8, Return from Command-Locked State**.) To clear the OTPDTCT/ILGLERR/ERSERR/PRGERR/ CFGDTCT/TBLDTCT bit in the FSTATR register in the command-locked state, the status clear command is available. In addition, to clear 1-bit correction flags (the OTPCRCT, CFGCRCT, and TBLCRCT bits), which do not cause transitions to the command-locked state (except for FCURAM), the status clear command is available. All status clear command processing is incorporated in the hardware. Therefore, the status clear command can be properly executed even if the FCU firmware is invalid.

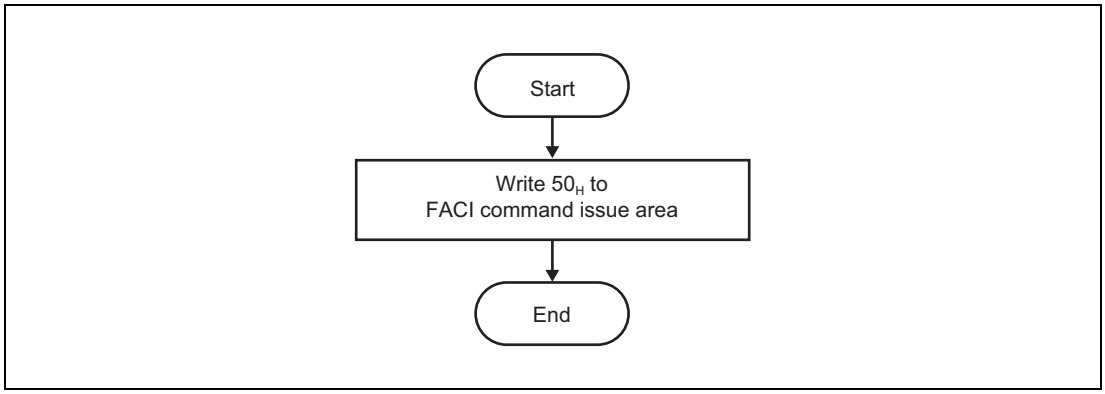
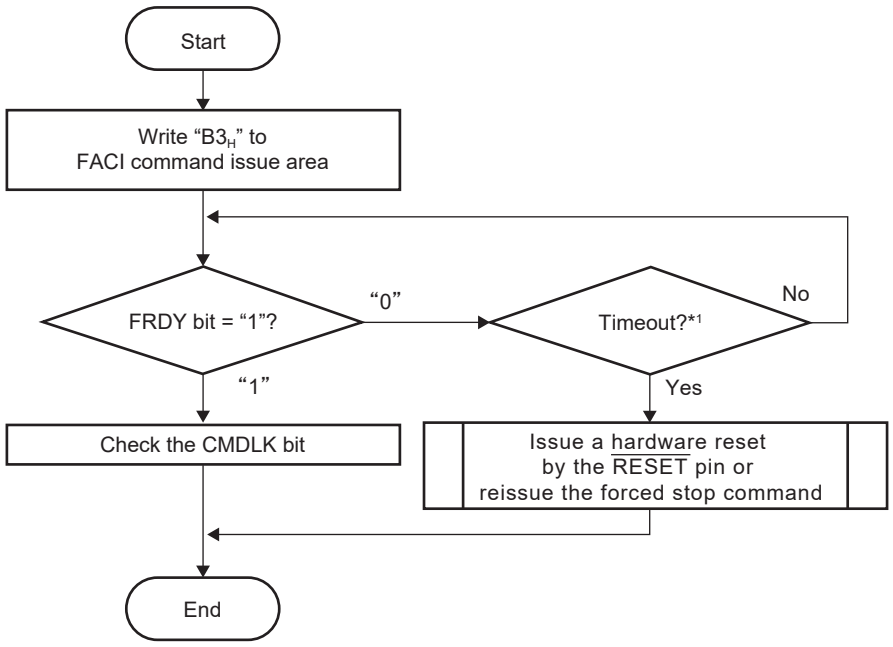


Figure 6.18 “Status Clear” Command Usage

6.3.15 Forced Stop Command

"Forced Stop" command provides the shortest latency when user wants to stop a flash sequencer command processing. The command can stop command operation more speedy than the programming/ erasure suspension command. However, the flash sequencer does not guarantee any result of stopped command operation such as data in programmed or erased area, or cannot resume the stopped command operation. Programmed or erased processing by using the "Forced Stop" command is defined as one programming.

When "Forced Stop" command is issued, the whole FCU and a part of FACI are initialized. Also, the FSTATR register is initialized. Therefore, the "Forced Stop" command can be used for returning from the command-locked state, or handling timeout of the flash sequencer operation. (See **Section 6.3.8, Return from Command-Locked State**.)



Note 1. The forced stop command latency (the maximum time: see **Section 10, Electrical Characteristics**) reaching 1.1 times is judged as a timeout.

Figure 6.19 "Forced Stop" Command Usage

- Issuing the Forced Stop Command while Another Command is Being Issued

  If a timeout of the programming command occurs when checking the DBFULL bit, a timeout occurs when checking the DBFULL or EBFULL bit when an ECC error is injected, or the forced stop command is used to suspend processing when a timeout of the DMA programming command occurs, writing to the FACI command-issuing area may be handled as writing of data by the programming command. If this is the case, read the FACI command-issuing area to intentionally lock commands and issue the forced stop command by following the procedure for returning from the command-locked state. Locking commands is possible in any case where the unit for reading the FACI command issuing area is 8, 16, or 32 bits.

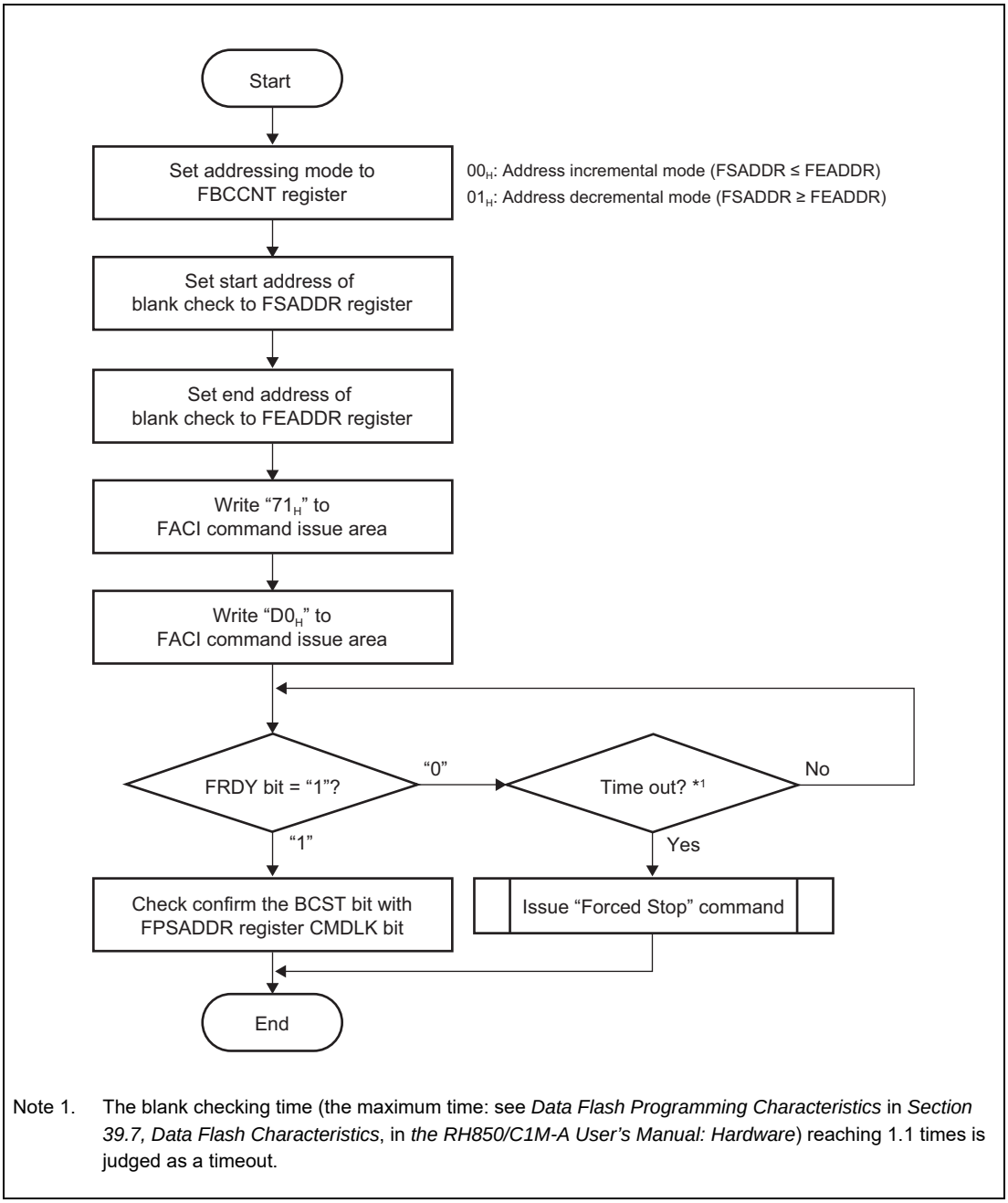
6.3.16 Blank Check Command

Values read from data flash memory that has been erased but not yet been programming again are undefined. Use the “Blank Check” command when you need to confirm that an area is in the non-programmed state. For the method for the code flash memory, See **Section 8.4, Blank Checking of Code Flash Memory**.

Before issuing “Blank Check” command, set addressing mode, start address, and end address to FBCCNT, FSADDR, and FEADDR register, respectively. When blank check addressing mode is set to decremental mode (i.e. FBCCNT.BCDIR = “1”), address specified in FSADDR should be larger than address in FEADDR. Conversely, address in FSADDR should be smaller than address in FEADDR when blank check addressing mode is set to incremental mode (i.e. FBCCNT.BCDIR = “0”). If setting of BCDIR, FSADDR, and FEADDR are inconsistent, the flash sequencer enters the command-locked state. Blank check unit can be set from 4 bytes to 64 Kbytes in 4-byte units.

Write 71_H and $D0_H$ to the FACI command issue area to start “Blank Check” command processing. Completion of command processing can be confirmed by FRDY bit of FSTATR register. At the end of processing, the result of “Blank Check” is stored in the BCST bit in the FBCSTAT register. If non-blank data exists within area for blank checking, the flash sequencer stores the address of the programmed data that was first detected in the FPSADDR register. In this case, address of non-blank data is indicated to FPSADDR register.

“Blank Check” is the function to check the erasure state of the area where erasure operation is normally completed. When erasure operation is aborted due to reset input or power off, this function cannot be used to check the erasure state.

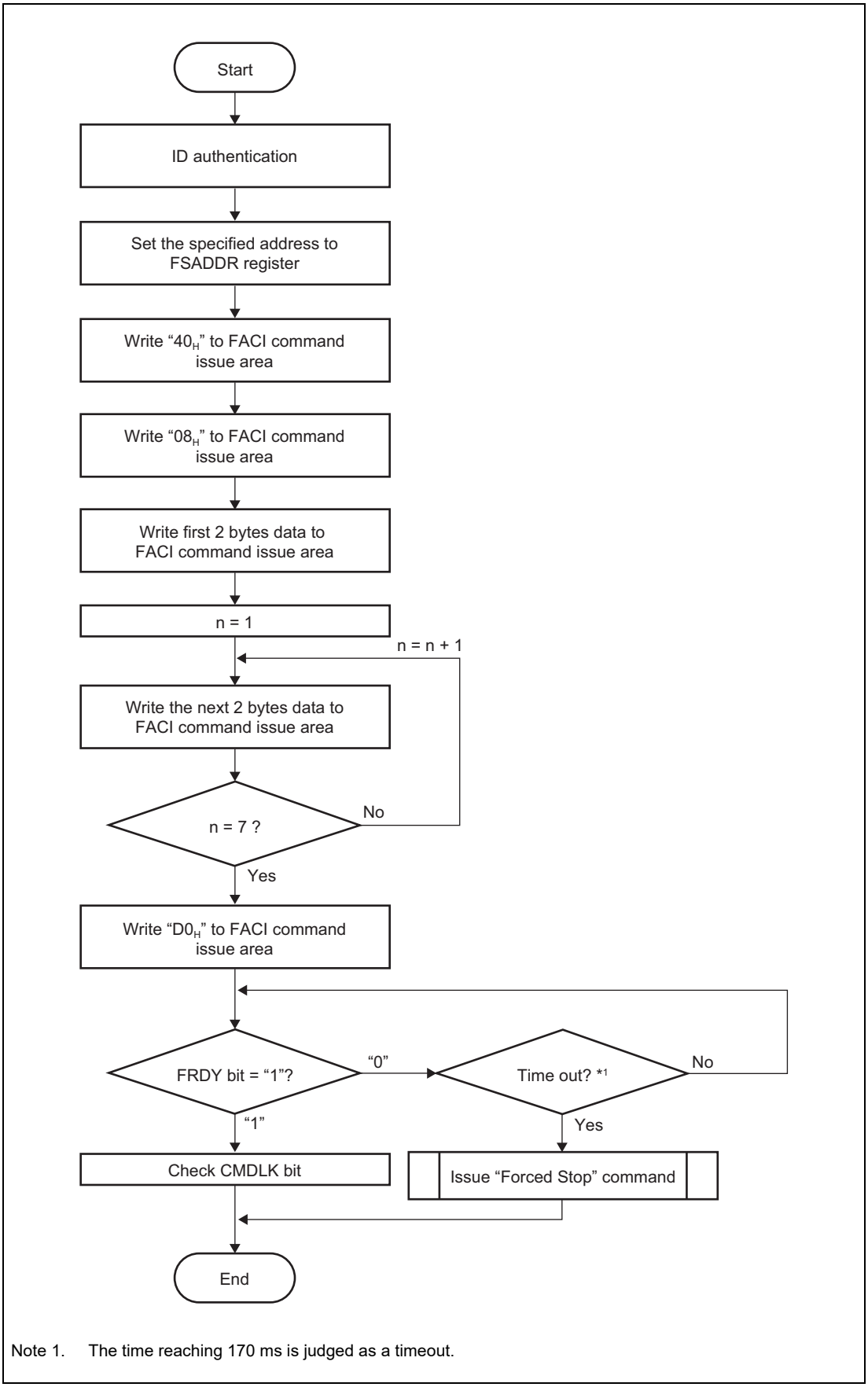


Note 1. The blank checking time (the maximum time: see *Data Flash Programming Characteristics* in *Section 39.7, Data Flash Characteristics*, in *the RH850/C1M-A User's Manual: Hardware*) reaching 1.1 times is judged as a timeout.

Figure 6.20 "Blank Check" Command Usage

6.3.17 Configuration Set Command

"Configuration Set" command is used to set the ID, security function, safety function, and option byte. Before issuing the Configuration Set command, perform an ID authentication and set the specified address (shown in **Table 6.5**) to the FSADDR register. Writing $D0_H$ to the FACI command issue area at the final access of the FACI command issue starts the Configuration Set command processing.



Note 1. The time reaching 170 ms is judged as a timeout.

Figure 6.21 "Configuration Set" Command Usage

As for the data for configuration setting and the address value to be set in the FSADDR register, refer to **Table 6.5**. Once 0 is set as data in the security setting area, it cannot be changed to 1. Data in other areas can be change to any value each time the Configuration Set command is executed.

Table 6.5 Address Used by Configuration Set Command

Address	Setting Data
FF30 0080$_H$	Option byte 32 to 17
FF30 0070$_H$	Option byte 16 to 1
FF30 0050$_H$	ID for authentication
FF30 0040$_H$	Security

Table 6.6 lists the security setting data when various security functions are enabled.

Table 6.6 List of Security Setting Data

Security Functions	Security Setting Data (16 bytes)
ID authentication enabled in serial programming mode	FFFF FFFF FFFF FFFF FFFF FFFF 1EFF FFFF$_H$
Serial programmer connection disabled	FFFF FFFF FFFF FFFF FFFF FFFF F7FF FFFF$_H$
Block erasure command disabled	FFFF FFFF FFFF FFFF FFFF FFFF DFFF FFFF$_H$
Programming command disabled	FFFF FFFF FFFF FFFF FFFF FFFF BFFF FFFF$_H$
Read command disabled	FFFF FFFF FFFF FFFF FFFF FFFF 7FFF FFFF$_H$

For details on the target registers, see *Section 35.9, Option Bytes* in *the RH850/C1M-A User's Manual: Hardware*.

6.3.18 Reading the Configuration Setting Area

When reading the configuration setting area to check the value written by “Configuration Set” command, set the FCUFSEL bit in the FCUFAREA register to “1”. Setting the FCUFSEL bit to “1” disables reading of the user area. The software that reads the configuration setting area must be executed on the internal RAM. For the address map in the configuration setting areas, see **Table 6.5**. Configuration setting “ID for authentication” storage area can be read only after SELF ID authentication is complete.

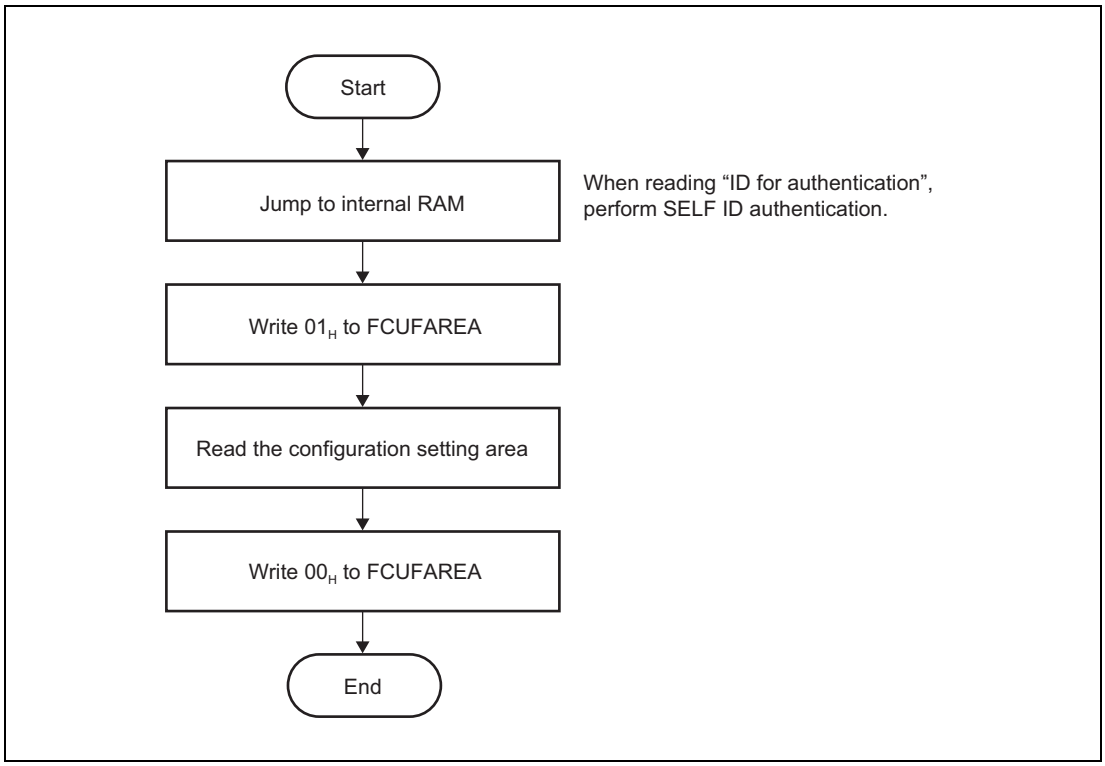


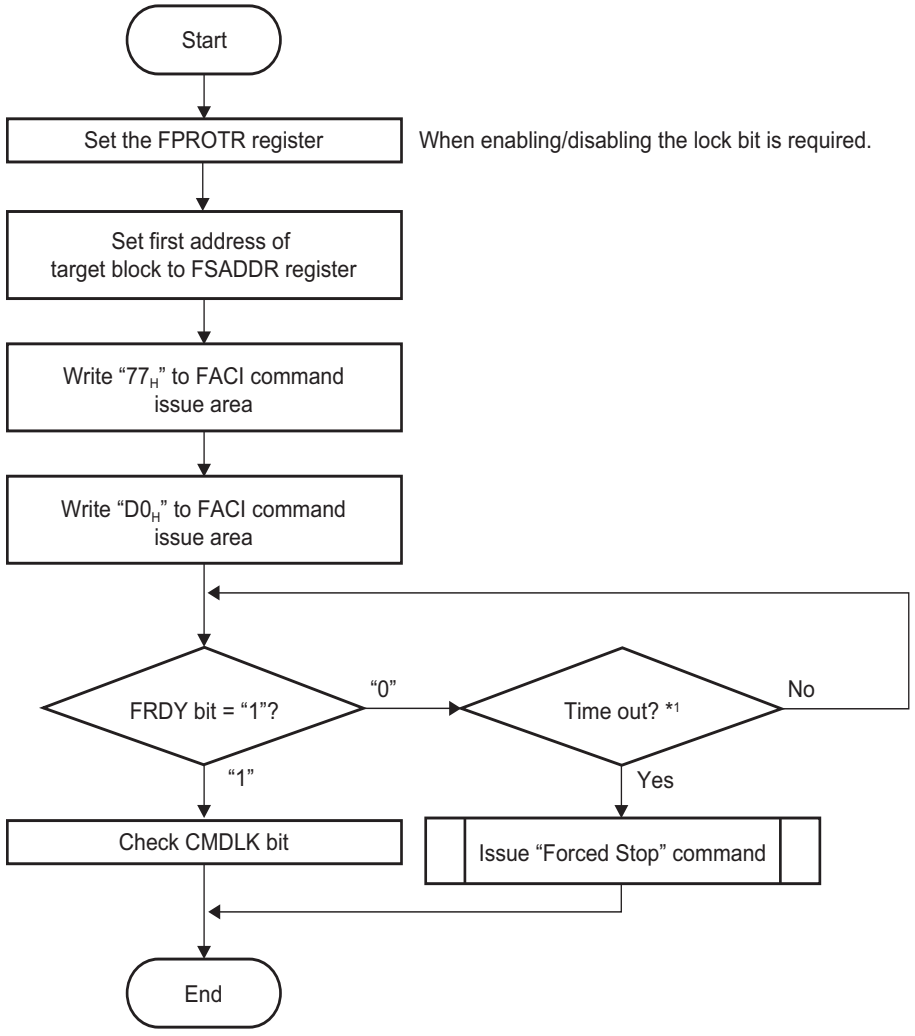
Figure 6.22 Flow of Reading of the Configuration Setting Area

6.3.19 Lock Bit Programming Command

The lock bit programming command is used for programming lock bit. For the erasure of lock bits, use the block erasure command. (See **Section 6.3.11, Block Erase Command**.)

Before issuing a lock bit programming command, set first address of target block to FSADRR register. Writing "77_H" and "$D0_H$" to FACI command issue area starts the lock bit programming command processing.

Set the FPROTR register before issuing the lock-bit programming command. To set the FPROTR register is required to switch enabling/disabling the lock bit.



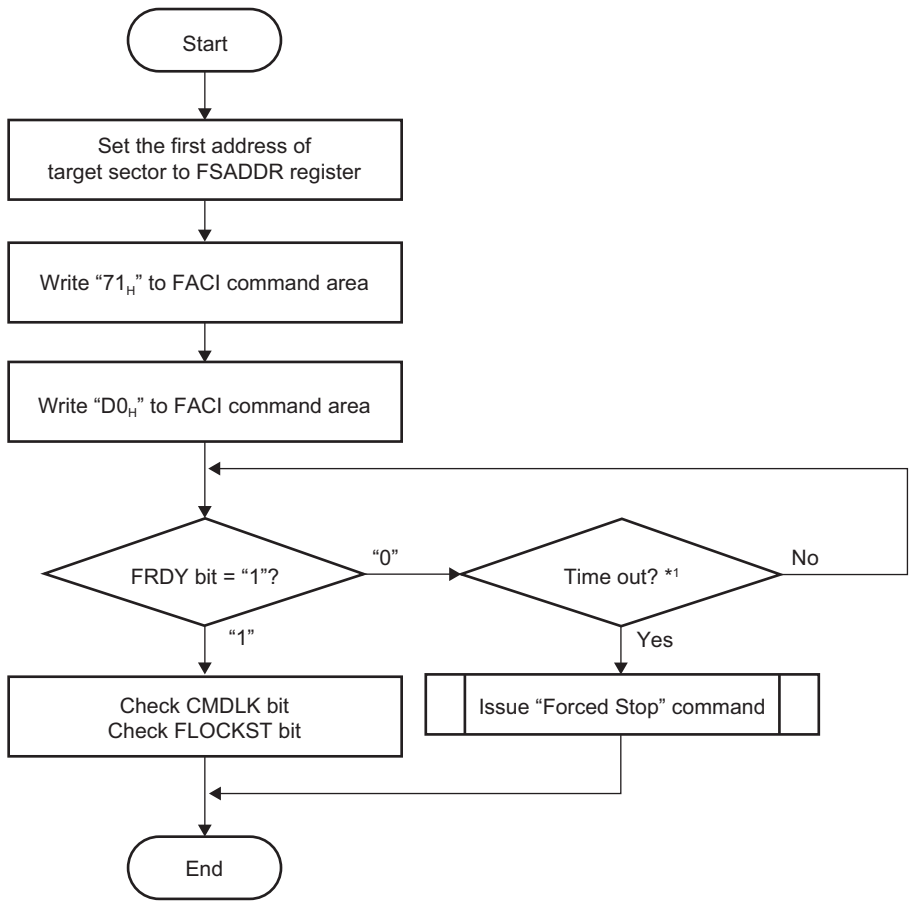
Note 1. The time reaching 25 ms is judged as a timeout.

Figure 6.23 "Lock Bit Programming" Command Usage

6.3.20 Lock Bit Read Command

"Lock Bit Read" command is used for read lock bit.

Before issuing "Lock Bit Read" command, set first address of target block to FSADRR register. Writing "71_H" and "$D0_H$" to FACI command issue area starts "Lock Bit Read" command processing. Completion of command processing can be confirmed by FRDY bit of FSTATR register. After "Lock Bit Read" command processing is completed normally, the FLOCKST bit in the FLKSTAT register will hold the result of reading the lock bit.

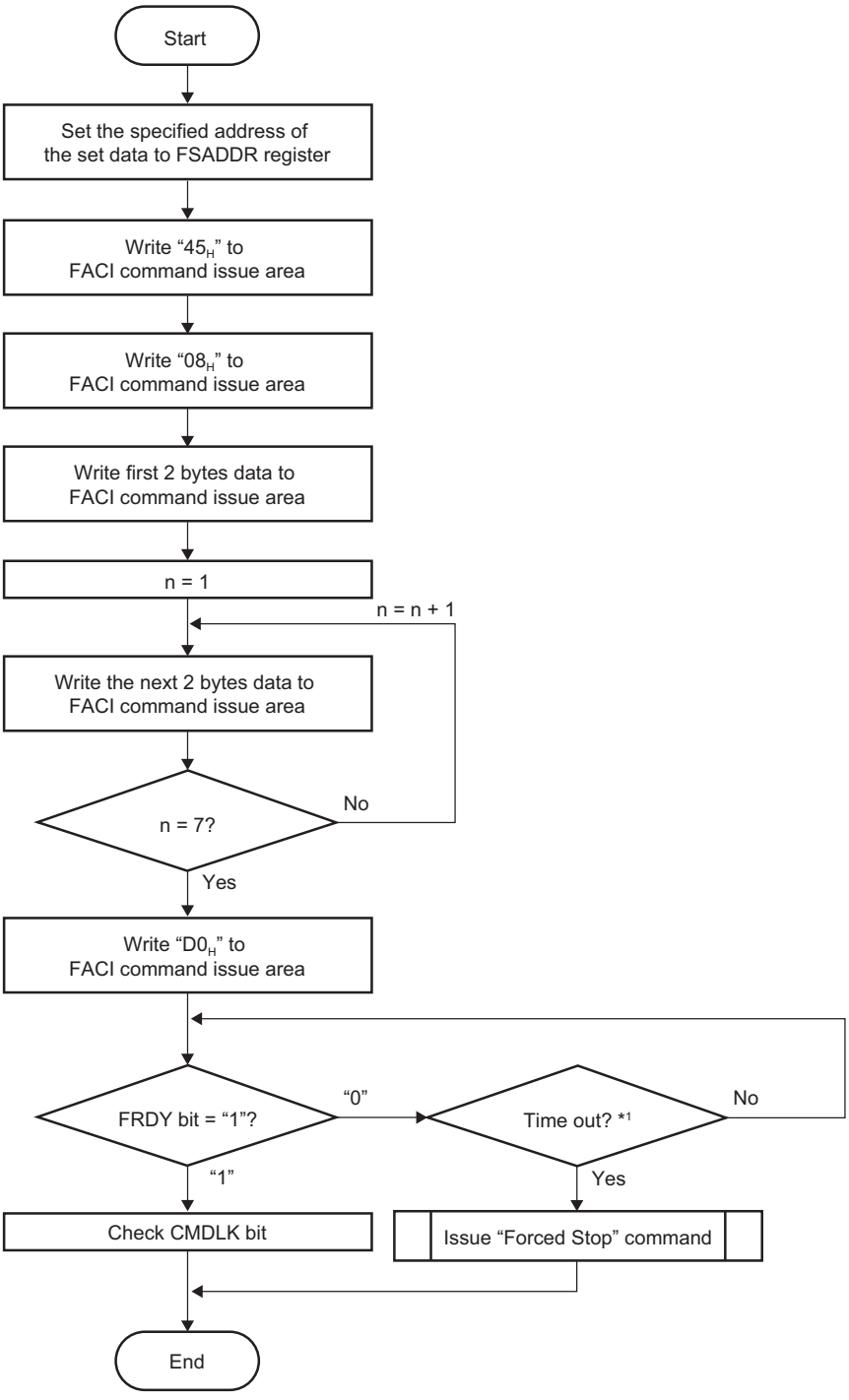


Note 1. The time reaching 10 µs is judged as a timeout.

Figure 6.24 "Lock Bit Read" Command Usage

6.3.21 OTP Set Command

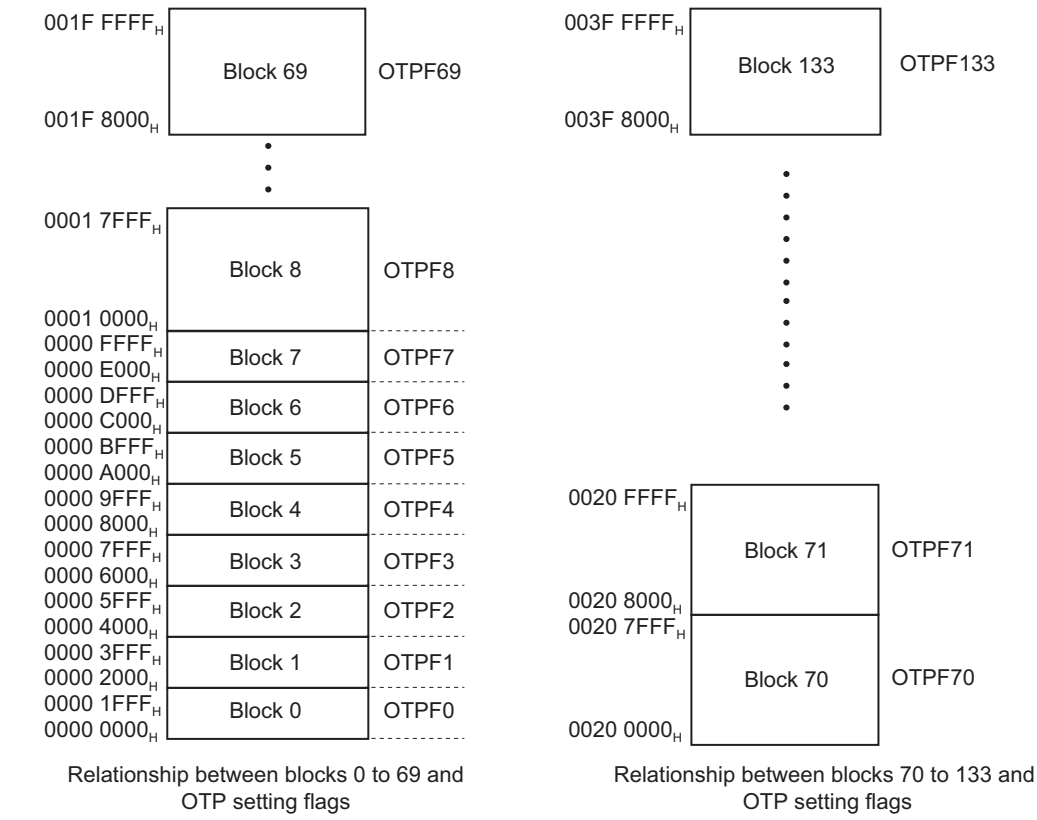
"OTP Set" command is used to set OTP. Before issuing "OTP Set" command, set the specified address of the set data (shown in **Table 6.7**) to FSADRR register. Writing $D0_H$ to the FACI command issue area at the final access of the FACI command issue starts the OTP Set command processing.



Note 1. The time reaching 120 ms is judged as a timeout.

Figure 6.25 "OTP Set" Command Usage

Figure 6.26 shows the relationship between the user area blocks and OTP setting flags. An OTP setting flag (OTPF0 to OTPF69) is allocated to each user area block (8 Kbytes × 8 blocks and 32 Kbytes × 62 blocks).



Note 1. Mounting areas vary in each product. For details, refer to *RH850/C1M-A User's Manual: Hardware*.

Figure 6.26 Relationship between User Area Blocks and OTP Setting Flags

Table 6.7 shows the addresses to be used for the OTP Set command. When 0 is set to a flag, OTP is set for the corresponding block. Once 0 is set to a flag, it cannot be changed to 1.

Table 6.7 Address to be Used for OTP Set Command

Address	Set Data
FF38 0090$_H$	OTP flag for user boot area (bit 0)
FF38 0080$_H$	Reserved area*1
FF38 0070$_H$	Reserved area*1
FF38 0060$_H$	Reserved area*1 (bit 127 to 70), OTPF133 (bit 69) to OTPF70 (bit 6)
FF38 0050$_H$	Reserved area*1
FF38 0040$_H$	Reserved area*1 (bit 127 to 70), OTPF69 (bit 69) to OTPF0 (bit 0)

Note 1. Do not set “0” to the reserved areas. The operation with the reserved area set to 0 is not guaranteed.

6.3.22 Reading the OTP Setting Area

When reading the OTP setting area to check the value written by “OTP Set” command, set the FCUFSEL bit in the FCUFAREA register to “1”. Setting the FCUFSEL bit to “1” disables reading of the user area. The software that reads the OTP setting area must be executed on the internal RAM. For the address map for the area of OTP settings, see **Table 6.7**.

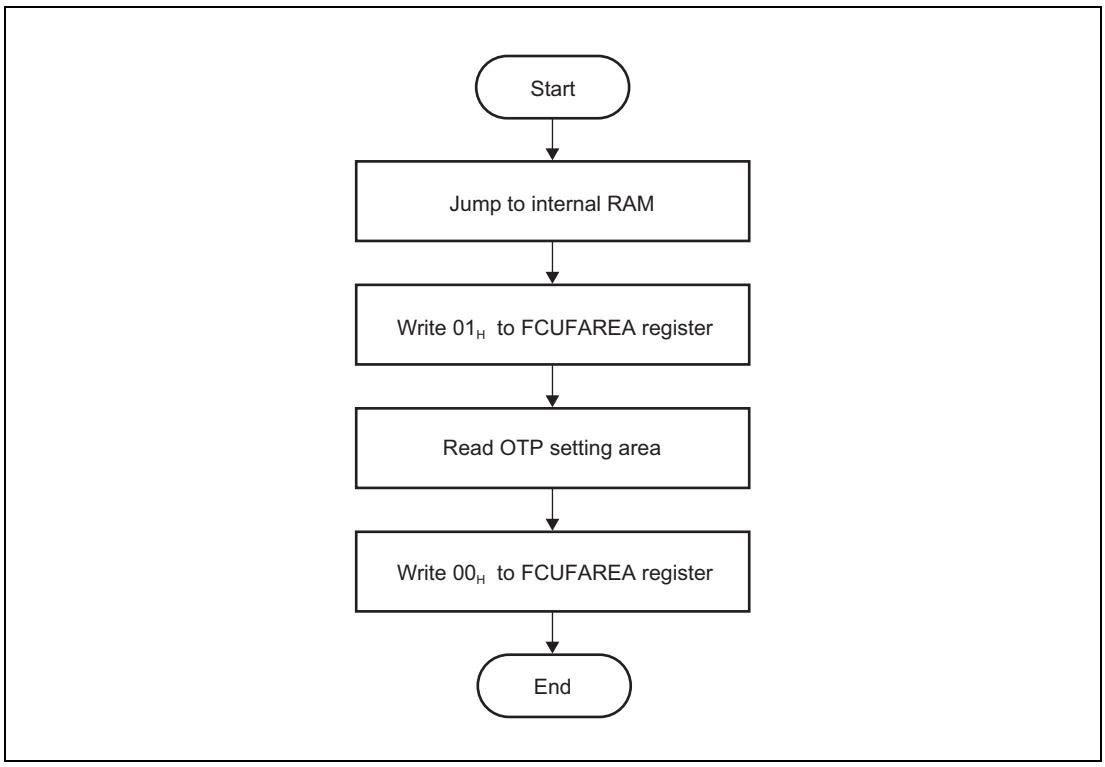


Figure 6.27 Flow of Reading the OTP Setting Area

6.3.23 Injecting ECC Errors for the Flash Memory

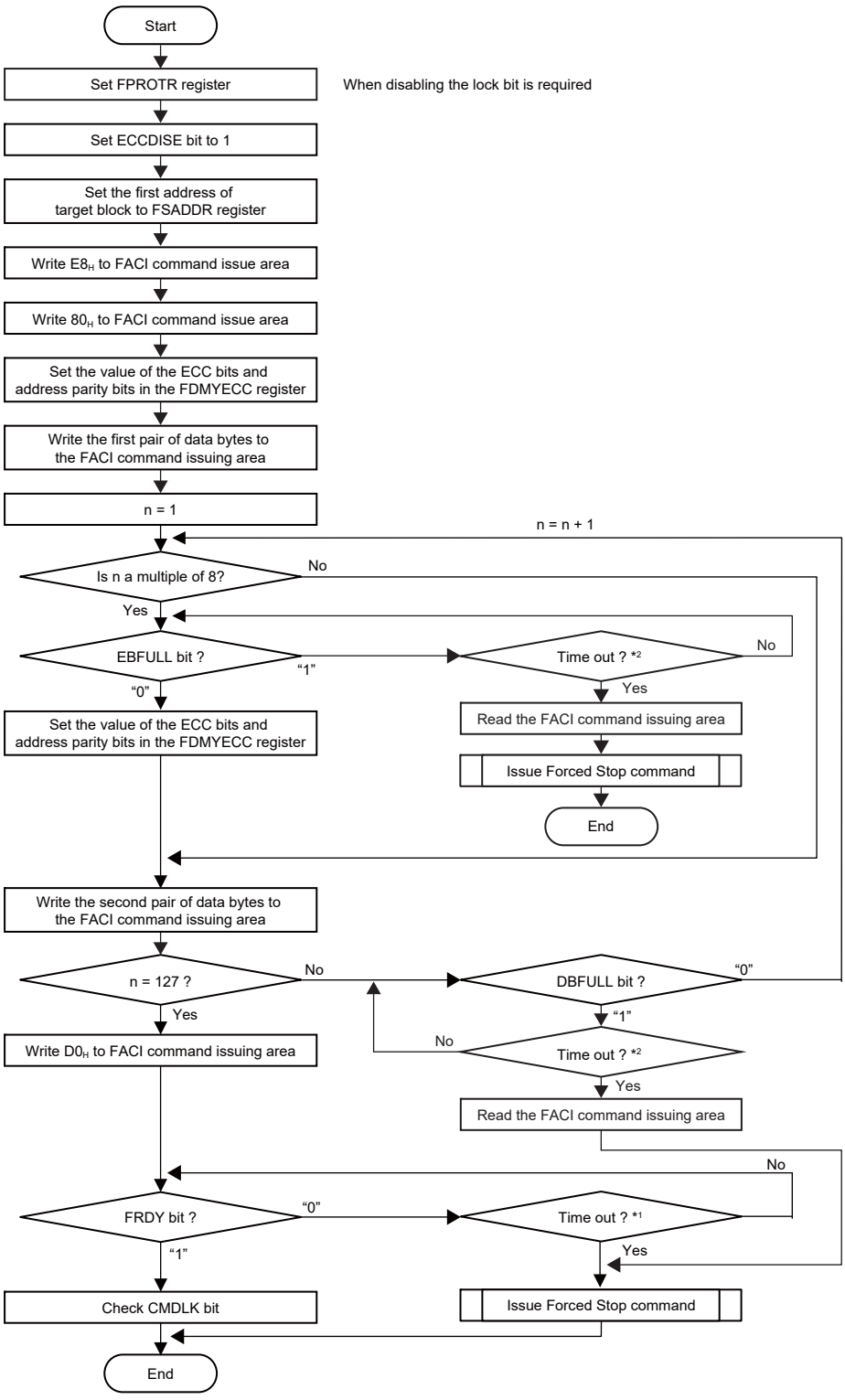
Any value of the ECC bits and address parity bits in the FDMYECC register can be written to the flash memory by using a programming command. Injecting an ECC error for the data area requires a four-byte programming command.

Before writing the value set in the FDMYECC register to the flash memory, set the ECCDISE bit in the FECCTMD register to 1. In addition, set the values for the ECC bits and address parity bits in the FDMYECC register before writing the data to the FACI command issuing area.

In the case of the code flash memory, the unit (256 bytes) for writing in response to the programming command differs from the unit (16 bytes) for which the ECC bits and address parity bits are to be added for the data. Therefore, every time 16 bytes of data are written to the FACI command issuing area, change the setting in the FDMYECC register.

In the case of the data flash memory, since the unit (4 bytes) for writing by the programming command is the same as that for the unit (4 bytes) of data for which the ECC bits are to be added, only change the setting in the FDMYECC register once before issuing the programming command.

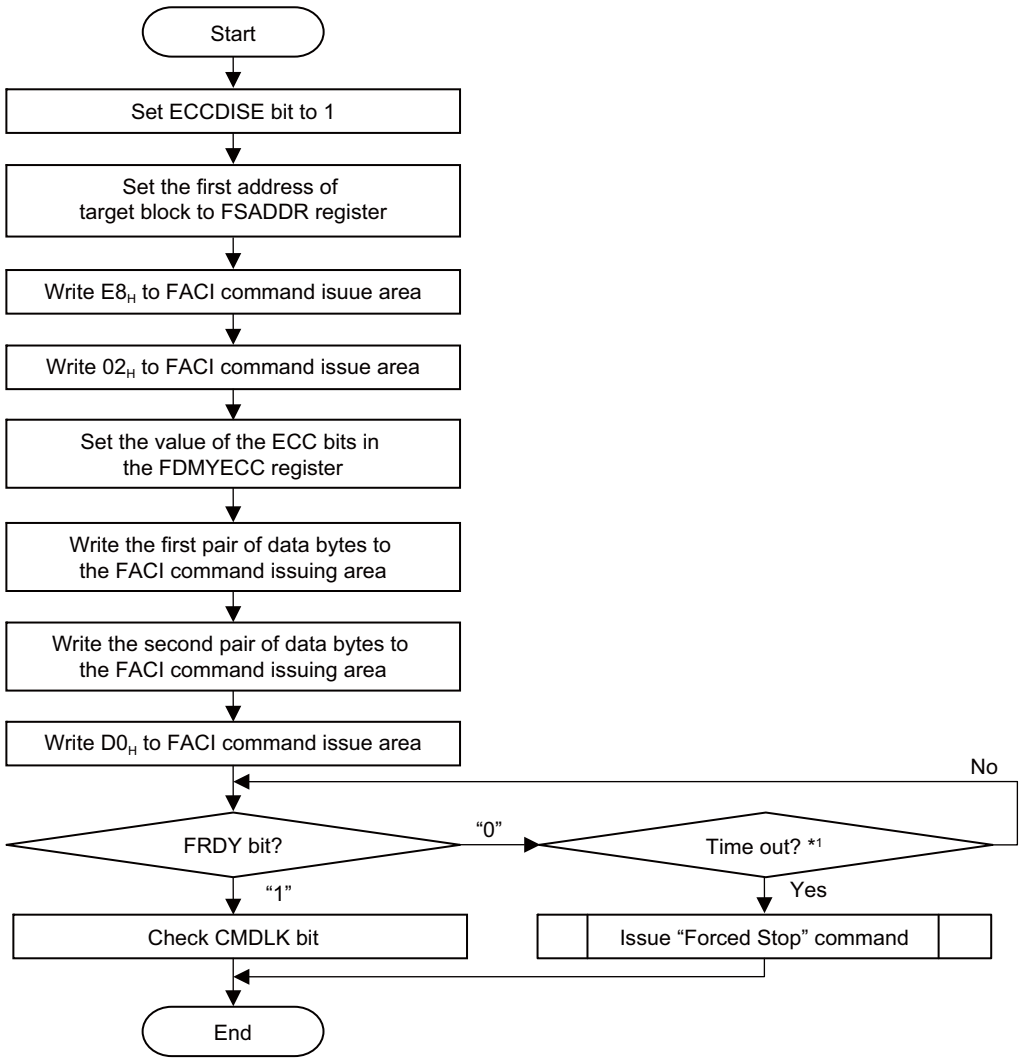
If the command for writing to the FDMYECC register is issued repeatedly while the EBFULL bit in the FSTATR register is “1”, a wait is generated in the peripheral bus, which will affect performance in communication with other peripheral IP modules. To avoid the generation of such a wait, write to the FDMYECC register while the EBFULL bit in the FSTATR register is 0.



Note 1. The time of 256-byte programming (the maximum time: see *Code Flash Programming Characteristics* in *Section 39.6, Code Flash Characteristics*, in *the RH850/C1M-A User's Manual: Hardware*) reaching 1.1 times is judged as a timeout.

Note 2. The time reaching 5 µs is judged as a timeout.

Figure 6.28 Injecting an ECC Error for the Code Flash Memory



Note 1. The time of 4 byte programming (the maximum time: see *Data Flash Programming Characteristics* in *Section 39.7, Data Flash Characteristics*, in *the RH850/C1M-A User's Manual: Hardware*) reaching 1.1 times is judged as a timeout.

Figure 6.29 Injecting an ECC Error for the Data Flash Memory

Section 7 Security Function

7.1 Command Protection by ID Authentication

In code flash programming/erasure mode, FACI commands can be used after security is released by the ID authentication. As well, in data flash programming/erasure mode, configuration setting commands can be used after security is released by the ID authentication. When a FACI command is issued in code flash programming/erasure mode or when a configuration command is issued in data flash programming/erasure mode while the IDST bit in the SELFIDST register is set to 1 (security lock state), the flash sequencer enters the command-locked state. The transition to code flash programming/erasure mode also places the flash sequencer in the command-locked state. If the flash sequencer enters the command-locked state while security is not released by ID authentication, release from the command-locked state is not possible even if the forced stop command is used. As for the security releasing method by the ID authentication, see **6.3.7, ID Authentication**.

The ID used for authentication in code flash programming/erasure mode or in data flash programming/erasure mode is shared with the OCD connection and serial programmer connection (when ID authentication is enabled).

In data flash programming/erasure mode, FACI commands can be used regardless of the IDST bit setting.

7.2 OTP for Code Flash Memory

OTP can be set independently for each block in the code flash memory. Once an OTP is set, it cannot be canceled. If Programming, Block Erase, or Lock Bit Programming command is issued to an OTP set block, the flash sequencer enters the command-locked state.

Once an OTP configuration command has been executed for a chip, the variable reset vector cannot be set in the corresponding area by a “Configuration Set” command. Even when an OTP configuration command for a reserved area in the code flash memory is completed normally or execution of an OTP configuration command with all bits set to 1 is completed normally, the variable reset vector cannot be set in the corresponding area.

Section 8 Protection Function

8.1 Software Protection

Software protection function disables flash sequencer command operation according to register settings or lock bit settings. If an attempt is made to issue flash sequencer command against software protection, flash sequencer enters the command-locked state.

8.1.1 Protection by FENTRYR

When FENTRYR register is set to "0000_H", flash sequencer is set to read mode. In read mode, FACI commands cannot be accepted. If an attempt is made to issue FACI command in read mode, flash sequencer enters the command-locked state.

8.1.2 Protection by Lock Bit

Each block in user area and user boot area have lock bits. When the FPROTCN bit in the FPROTR register is 0, programming/erasing the block where the corresponding lock bit is 0 is disabled. To program/erase the block where the corresponding lock bit is 0 is disabled, set the FPROTCN bit to 1. If an attempt is made to issue programming/block erase/lock bit programming command against protection by lock bits, the flash sequencer enters the command-locked state.

8.2 Error Protection

Error protection function detects an illegal FACI command issued, an illegal access, or a flash sequencer malfunction, and disables FACI command acceptance (command-locked state). While flash sequencer is in the command-locked state, flash memory cannot be programmed or erased. To cancel the command-locked state, issue “Status Clear” or “Forced Stop” command while the CFAE and DFAE bits in the FASTAT register is “0”. “Status Clear” command can be used only when FRDY bit is “1”. “Forced Stop” Command can be used regardless of FRDY bit value. When the flash sequencer enters the command-locked state (the FASTAT.CMDLK bit is 1) while the FAEINT.CMDLKIE bit is 1, a flash access error (FLERR) interrupt is generated.

If flash sequencer enters the command-locked state during programming or erasure processing by the command other than Programming/Erasure suspend, the flash sequencer continues programming or erasure processing, In this state, programming or erasure processing cannot be suspended by the Programming/Erasure suspend command. If a command is issued in the command-locked state, ILGLERR bit becomes “1” and the other bits retain the values set due to the previous error detection.

Table 8.1 shows error protection types and status bit values after error detection.

Table 8.1 Error Protection Type (1/2)

Error Type	Description	OTPDTCT	ILGLERR	ERSERR	PRGERR	FLWEERR	CFGDTCT	TBLDTCT	FRDTCT	CFAE	DFAE
FENTRYR setting error	The value set in FENTRYR is not 0000_H, 0001_H, or 0080_H.	0	1	0	0	0	0	0	0	0	0
	The FENTRYR setting for resuming operation does not match that for suspending operation.	0	1	0	0	0	0	0	0	0	0
Illegal command error	An undefined code has been written in the first access of FACI command.	0	1	0	0	0	0	0	0	0	0
	The value specified in the last access of the multiple-access FACI command is not $D0_H$ (except for “DMA Programming”).	0	1	0	0	0	0	0	0	0	0
	The value (N) specified in the second write access of FACI command in the “Programming”, “DMA Programming”, “Configuration Set”, or “OTP Set” command is wrong (odd number is wrong for “DMA Programming”).	0	1	0	0	0	0	0	0	0	0
	“Blank Check” command has been issued with inconsistent BCDIR, FSADDR, and FEADDR settings. (See **Section 4.4, FEADDR — FACI Command End Address Register**.)	0	1	0	0	0	0	0	0	0	0
	FACI command has been issued against FACI command not acceptable mode. (See **Table 6.3**.)	0	1	0	0	0	0	0	0	0	0
	FACI command has been issued when command acceptance conditions are not satisfied. (See **Table 6.4**)	0/1	1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Erase error	An error has occurred during flash memory erasure.	0	0	1	0	0	0	0	0	0	0
	“Block Erase” command has been issued against lock bit protection.	0	0	1	0	0	0	0	0	0	0
Program error	An error has occurred during flash memory program.	0	0	0	1	0	0	0	0	0	0
	“Programming” or “Lock Bit Programming” command has been issued against lock bit protection.	0	0	0	1	0	0	0	0	0	0
FCURAM ECC error	A 2-bit error has been detected when FCURAM is read.	0	0	0	0	0	0	0	1	0	0
Code flash access error	FACI command has been issued to reserved user area in code flash programming/erasure mode. (See **Section 4.1, FASTAT — Flash Access Status Register**).	0	1	0	0	0	0	0	0	1	0
	FACI command has been issued to reserved user boot area in code flash programming/erasure mode. (See **Section 4.1, FASTAT — Flash Access Status Register**).	0	1	0	0	0	0	0	0	1	0

Table 8.1 Error Protection Type (2/2)

Error Type	Description	OTPDTCT	ILGLERR	ERSERR	PRGERR	FLWEERR	CFGDTCT	TBLDTCT	FRDTCT	CFAE	DFAE
Data flash access error	FACI command has been issued to reserved data area in data flash programming/erasure mode. (See **Section 4.1, FASTAT — Flash Access Status Register**).	0	1	0	0	0	0	0	0	0	1
	“Configuration Set” command has been issued to reserved area. (See **Section 4.1, FASTAT — Flash Access Status Register**).	0	1	0	0	0	0	0	0	0	1
	“OTP Setting” command has been issued to reserved area. (See **Section 4.1, FASTAT — Flash Access Status Register**).	0	1	0	0	0	0	0	0	0	1
Security	“Programming”, “Block Erase”, or “Lock Bit Programming” command has been issued against OTP setting.	0	1	0	0	0	0	0	0	0	0
	Code flash programming/erasure mode is entered or a configuration setting command was issued in data flash programming/erasure mode while security has not been released by ID authentication.	0	1	0	0	0	0	0	0	0	0
Other	FACI command issue area has been accessed in read mode.	0	1	0	0	0	0	0	0	0	0
	FACI command issue area has been read in code flash programming/erasure mode or data flash programming/erasure mode.	0	1	0	0	0	0	0	0	0	0
OTP Set ECC error	A 2-bit error has been detected when OTP setting is read.	1	0	0	0	0	0	0	0	0	0
FHVE set error	The value of the FHVE3CNT bit in the FHVE3 register has changed to 0 during command processing by the flash sequencer.	0	0	0/1	0/1	1	0	0	0	0	0
Configuration Set ECC error	2-bit error has been detected when Configuration Set value is read.	0	0	0	0	0	1	0	0	0	0
Overwrite parameter ECC error	2-bit error has been detected when overwrite parameter table is read.	0	0	0	0	0	0	1	0	0	0

8.3 Boot Program Protection

8.3.1 User Boot Protection

The user boot area can be overwritten by the serial programming. Since this area is usually write-protected for the self-programming, it can be used to store programs such as a boot program safely.

8.4 Blank Checking of Code Flash Memory

Reading from an area of the code flash memory that has been erased but to which no new data has been written (an area in the non-written state) leads to an exception since an ECC error will be detected. In addition, as the values of the data are not guaranteed when an ECC error has occurred, confirm that the area is in the non-written state by checking whether all data bits, ECC bits, and address parity bits for the code flash memory are set to 1. For usage notes on the ECC function for the code flash memory, see the section on safety features in the user's manual for the given product.

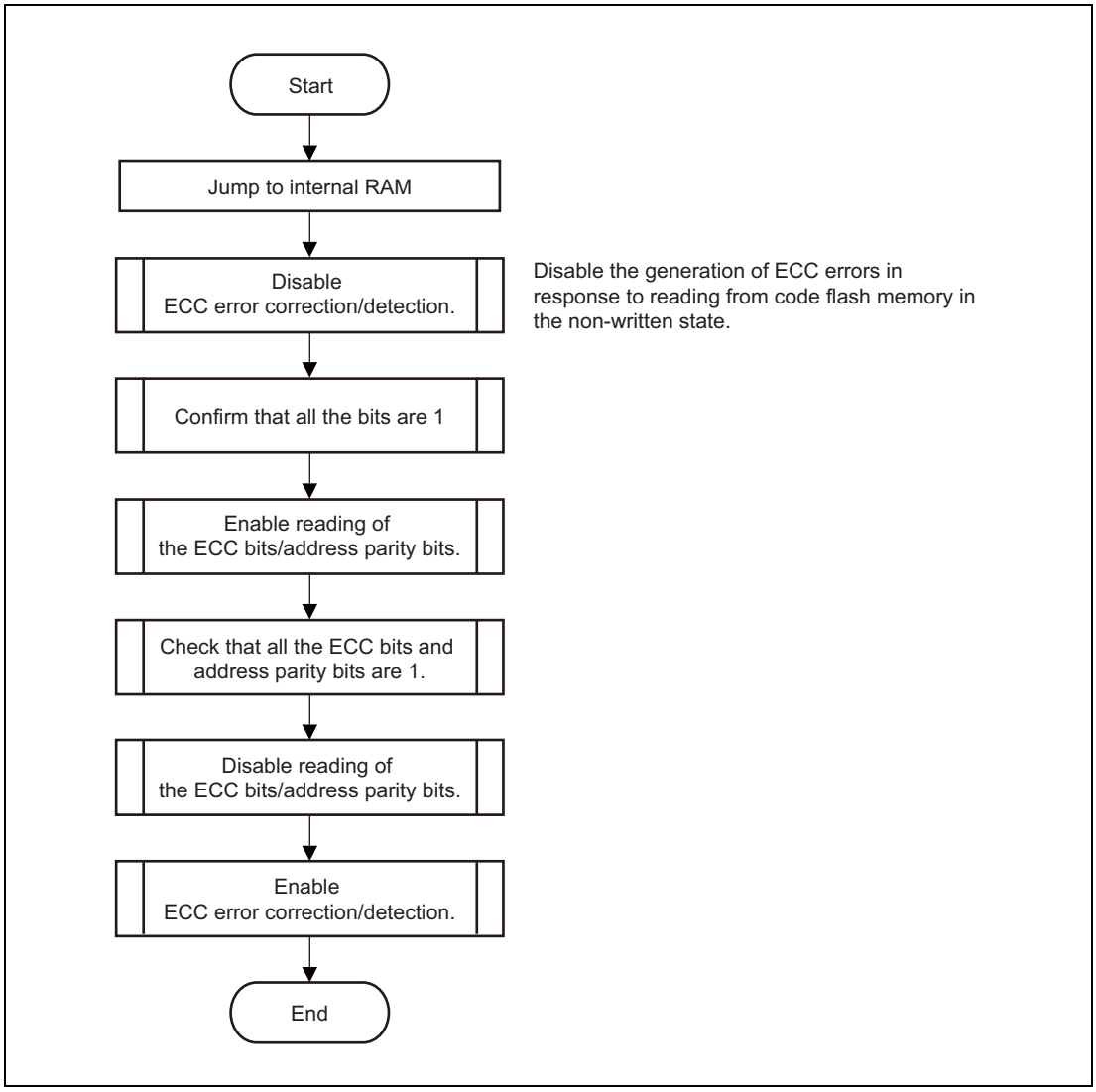


Figure 8.1 Blank Checking of Code Flash Memory

Section 9 Usage Notes

(1) Reading from area where programming/erasure is suspended

The data stored in the flash memory area where programming/erasure is suspended is undefined. To avoid the malfunction caused by reading undefined data, do not make an attempt to fetch the instruction or read the data in the area where programming/erasure is suspended.

(2) Prohibition of additional write

Writing the same area more than once is prohibited. To write again the flash memory area where data has already been written to, be sure to erase the corresponding area in advance.

(3) Reset during programming/erasure

To generate a reset by the $\overline{\text{RESET}}$ pin during programming/erasure, release the reset after the reset input period of more than the minimum value of the reset pulse width, within the operating voltage range specified by electrical characteristics.

(4) Interrupt/exception vector allocation during programming/erasure

When an interrupt/exception is generated during programming/erasure, vector fetch may be generated from the code flash memory. Under the condition where the BGO function is not used, set the address of vector fetch to the area other than code flash memory. For how to change the address of vector fetch, see *Section 3, CPU System* and *Section 6, Interrupts* in t*he RH850/C1M-A User's Manual: Hardware*.

(5) Abnormal end during programming/erasure

Verification of the write or erasure state cannot be provided for a flash memory area where write or erasure is abnormally ended and data is undefined, for example due to external reset or power off. For the area where write or erasure is abnormally ended, the blank check function is not enough to check the erasure state. Before using the corresponding area again, completely erase the area by the erasure processing.

When programming/erasing the code flash memory is not ended normally, the lock bit may be enabled. In this case, erase the corresponding block and erase the lock bit while lock bits are disabled.

(6) Items prohibited during programming, erasure, and blank checking

Do not perform the following operations during programming, erasure, or blank checking of the flash memory.

- Set the power supply voltage outside the operating voltage range.
- Update the FHVE15 and FHVE3 values.
- Change the operating frequency of the peripheral clock.

(7) Update of FCUFAREA register

When the code flash area is switched by setting the FCUFAREA register, previous and subsequent processing and switching of the area must be synchronized.

The flow of synchronization when updating the FCUFAREA register is described in the following three cases.

[1] Processing for synchronization when updating the FCUFAREA register:

After an update of the register, dummy-read the FCUFAREA register and execute the SYNCP instruction before a read instruction for the code flash memory or FCU firmware storage area (LD.W, etc.) to wait for the update of the FCUFAREA register.

[2] Processing for synchronization before switching to the code flash user area or user boot area:

For switching to the code flash area following the completion of reading the FCU firmware storage area, execute the SYNCP instruction after the last read instruction (LD.W, etc.) for the FCU firmware storage area, and then follow step [1] above to change the value of the FCUFAREA register.

[3] Processing for synchronization after switching to the code flash user area or user boot area:

To prevent execution of code flash codes that have been read before switching, dummy-read the FCUFAREA register and execute the SYNCP and SYNCI instructions after an update of the FCUFAREA register before executing the code flash instruction.

After the code flash area has been switched, clear the instruction cache and data buffer.

(8) Point for caution on selecting the FCU firmware storage area

For transfer of the FCU firmware or for reading of the configuration setting area or OTP setting area, the FCU firmware storage area must be selected by setting the FCUFAREA register. When the FCU firmware storage area is selected, place the exception handler vector address for the CPU in the internal RAM to avoid any access to the FCU firmware storage area due to the generation of an interrupt. For how to change the exception handler vector address, see *Section 3, CPU System* and *Section 6, Interrupts* in *the RH850/C1M-A User's Manual: Hardware*.

(9) Maintenance of coherency after the code flash memory is overwritten

When executing an instruction for the code flash memory after the code flash memory area is overwritten, clear the instruction cache and the data buffer, in order to maintain coherency (see *Section 3.4.3, Ensure Coherency after Rewriting the Code Flash*, in *Section 3, CPU Systems* in *the RH850/C1M-A User's Manual: Hardware*).

Section 10 Electrical Characteristics

This section explains the electrical characteristics when the hardware interface is used with the selfprogramming described in this manual.

Note that these electrical characteristics differ from those of when the serial programming is used.

10.1 Code Flash Characteristics

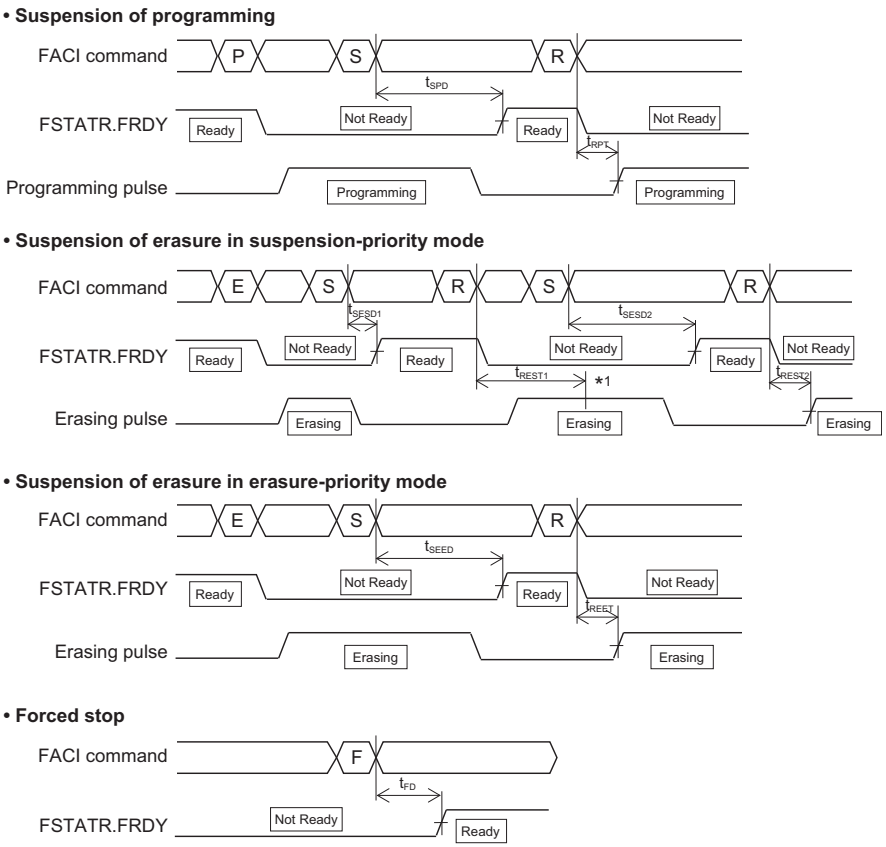
For the code flash basic characteristics and the code flash programming characteristics, refer to *Code Flash Basic Characteristics*, and *Code Flash Programming Characteristics*, in *Section 39.6, Code Flash Characteristics*, in t*he RH850/C1M-A User's Manual: Hardware*.

Table 10.1 Suspension/Resumption/Forced Stop

Conditions: SYSVCC = VCC = 4.5 V to 5.5 V, VDD = 1.15 V to 1.35 V,
A0VCC, A1VCC, A2VCC = 4.5 V to 5.5 V, A0VREFH = 4.5 V to A0VCC, A1VREFH = 4.5 V to A1VCC,
A2VREF = 4.5 V to A2VCC, RVCC = 4.5 V to 5.5 V, VSS = A0VSS = A1VSS = A2VSS = RVSS = 0 V,
Tj = –40°C to 150°C

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Suspend latency during programming	t_{SPD}	—	—	—	120	µs
Programming resume time*1	t_{RPT}	—	—	—	50	µs
Suspend latency during erasing	t_{SESD1}	Priprity on suspension The 1st suspend for the same pulse	—	—	120	µs
	t_{SESD2}	Priprity on suspension The 2nd suspend for the same pulse	—	—	1.7	ms
	t_{SEED}	Priority on erasure	—	—	1.7	ms
Erasing resume time*1	t_{REST1}	Priprity on suspension Resume after the 1st suspend for the same pulse	—	—	1.7	ms
	t_{REST2}	Priprity on suspension Resume after the 2nd suspend for the same pulse	—	—	80	µs
	t_{REET}	Priority on erasure	—	—	80	µs
Forced stop command latency	t_{FD}	—	—	—	20	µs

Note 1. The time taken for resumption includes an overhead for the resumption of programming or erasure.
In suspension-priority mode, a time for reapplication of the erasing pulse that was cut off at the time of suspension is also required.
Resume time is defined as time added by programming or erasing due to those sources.



Note: P: Programming command, E: Block erasure command
S: P/E suspension command, R: P/E resumption command, F: Forced stop command

Note 1. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.

Figure 10.1 Timing of Suspension/Resumption/Forced Stop

10.2 Data Flash Characteristics

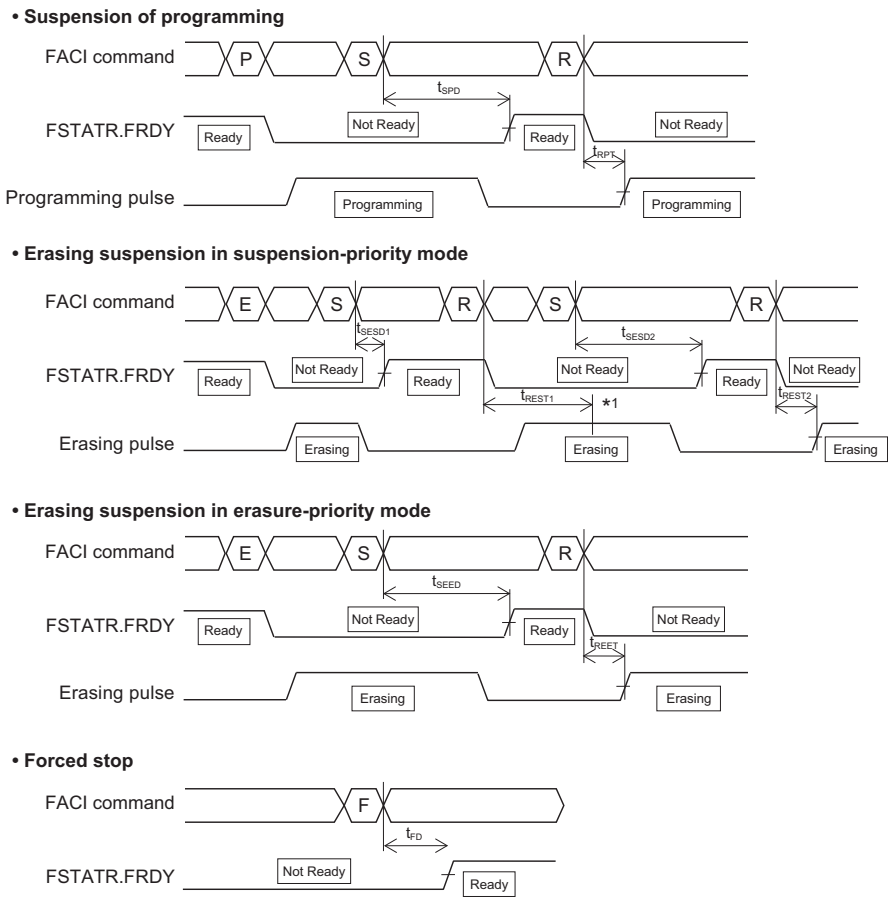
For the data flash basic characteristics and the data flash programming characteristics, refer to *Data Flash Basic Characteristics*, and *Data Flash Programming Characteristics*, in *Section 39.7, Data Flash Characteristics*, in *the RH850/C1M-A User's Manual: Hardware*.

Table 10.2 Suspension/Resumption/Forced Stop

Conditions: SYSVCC = VCC = 4.5 V to 5.5 V, VDD = 1.15 V to 1.35 V,
A0VCC, A1VCC, A2VCC = 4.5 V to 5.5 V, A0VREFH = 4.5 V to A0VCC, A1VREFH = 4.5 V to A1VCC,
A2VREFH = 4.5 V to A2VCC, RVCC = 4.5 V to 5.5 V, VSS = A0VSS = A1VSS = A2VSS = RVSS = 0 V,
Tj = –40°C to 150°C

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Suspension latency during programming	t_{SPD}	—	—	—	120	µs
Programming resume time*1	t_{RPT}	—	—	—	50	µs
Suspension latency during erasure	t_{SESD1}	Priority on suspension The 1st suspension for the same pulse	—	—	120	µs
	t_{SESD2}	Priority on suspension The 2nd suspension for the same pulse	—	—	300	µs
	t_{SEED}	Priority on erase	—	—	300	µs
Erasing resume time*1	t_{REST1}	Priority on suspension Resumption after the 1st suspension for the same pulse	—	—	300	µs
	t_{REST2}	Priority on suspension Resumption after the 2nd suspension for the same pulse	—	—	70	µs
	t_{REET}	Priority on erasure	—	—	70	µs
Forced stop command latency	t_{FD}	—	—	—	20	µs

Note 1. The time taken for resumption includes an overhead for the resumption of programming or erasure.
In suspension-priority mode, a time for reapplication of the erasing pulse that was cut off at the time of suspension is also required.
Resume time is defined as time added by programming or erasing due to those sources.



Note: P: Programming command, E: Block erasure command
S: P/E suspension command, R: P/E resumption command, F: Forced stop command

Note 1. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.

Figure 10.2 Timing of Suspension/Resumption/Forced Stop

REVISION HISTORY	RH850/C1M-A Flash Memory User's Manual: Hardware Interface

Rev.	Date	Description	
		Page	Summary
0.50	Apr 18, 2016	—	First Edition issued
1.00	Jun 28, 2017	Section 2 Module Configuration	
		7	Description modified
		Section 3 Address Map	
		8	Table 3.1 Information on the Hardware Interface Area: The address of the FCU firmware storage area changed, the Peripheral Group column added, Note 1 added.
		Section 4 Registers	
		9	Table 4.1 Flash Memory Related Registers, added
		10	Table 4.2 FASTAT Register Contents (1/2): Functional description of the CFAE bit modified
		12	4.2 FAEINT — Flash Access Error Interrupt Enable Register: Description of the register modified
		15	4.5 FCURAME — FCURAM Enable Register: Note 1 in the bit chart modified
		19	Table 4.7 FSTATR Register Contents (4/5): Functional description of the FLWEERR bit modified (FHVE15/FHVE3 register → FHVE3 register)
		21	4.7 FENTRYR — Flash Programming/Erasure Mode Entry Register: Description of the register modified (the value added: 0000_H), Note 1 in the bit chart modified
		23	4.8 FPROTR — Code Flash Protect Register: Note 1 in the bit chart modified
		23	Table 4.9 FPROTR Register Contents: Name of the FPROTCN bit corrected (FPROTRCN bit → FPROTCN bit)
		24	4.9 FSUINITR — Flash Sequencer Set-Up Initialize Register: Note 1 in the bit chart modified
		25	4.10 FLKSTAT — Lock Bit Status Register: Description of the register modified
		28	4.13 FRTEINT — FACI Reset Transfer Error Interrupt Enable Register: Description of the register modified
		36	4.20 FPCKAR — Flash Sequencer Processing Clock Notify Register: Note 1 in the bit chart modified
		38	4.22FECCTMD — Flash ECC Test Mode Register: Note 1 in the bit chart modified
		Section 6 FACI Command	
		52	Figure 6.3 Transfer Flow of FCU Firmware: Note 2 added, description of the FCU firmware storage area modified
		61	Figure 6.11 DMA Programming Command Usage: The box for "Read the FACI command issuing area" added
		64	Figure 6.13 "Programming/Erasure Suspend" Command Usage: The flow of "Issue "Forced Stop" command" added, Note 2 added
		70	Figure 6.19 "Forced Stop" Command Usage: Flow added
		70	6.3.15 Forced Stop Command: "Issuing the Forced Stop Command while Another Command is Being Issued" added
		75	6.3.17 Configuration Set Command: The section number of the reference manual changed
		79	Figure 6.25 "OTP Set" Command Usage: Note 1 added for the judgment of timeout
		83	Figure 6.28 Injecting an ECC Error for the Code Flash Memory: Flow added
		Section 8 Protection Function	
		87	Table 8.1 Error Protection Type (1/2): Description of the FENTRYR setting error modified, FCU error deleted
		88	Table 8.1 Error Protection Type (2/2): Description of the FHVE set error modified
		Section 9 Usage Notes	
		91	(6) Items prohibited during programming, erasure, and blank checking: Blank checking added
		92	(7) Update of FCUFAREA register: Description modified

Rev.	Date	Description	
		Page	Summary
1.00	Jun 28, 2017	Section 10 Electrical Characteristics	
		93	Table 10.1 Suspension/Resumption/Forced Stop: Entries in the MAX. column changed
		94	Figure 10.1 Timing of Suspension/Resumption/Forced Stop: “Suspension of erasure in erasure-priority mode” changed to “Suspension of programming”
		95	Table 10.2 Suspension/Resumption/Forced Stop: Entries in the MAX. column changed
		96	Figure 10.2 Timing of Suspension/Resumption/Forced Stop: “Erasing suspension in erasure-priority mode” changed to “Suspension of programming”
1.10	May 31, 2018	Section 4 Registers	
		27	4.12 FRTSTAT — FACI Reset Transfer Status Register: Description added
		28	4.13 FRTEINT — FACI Reset Transfer Error Interrupt Enable Register: Caution added
		Section 7 Security Function	
		85	7.1 Command Protection by ID Authentication: Description added
		Section 8 Protection Function	
		88	Table 8.1 Error Protection Type (2/2): Description of security corrected

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