RC38312A

The RC38312A Evaluation Board (EVB) is designed to support users evaluating high performance synthesizer and jitter attenuator applications. This document describes the following:

- Basic hardware and GUI setup using Renesas IC Toolbox (RICBox™) software
- Board power-up instructions
- Instructions to get active output signals using a provided configuration file
- Hardware modifications required for different conditions

Board Contents

- RC38312A evaluation board
- EVB manual
- Configuration software (installable plugin for RICBox)
- Configuration example file for four built-in device settings
- Board schematic and BOM

Features

- Four differential clock inputs
- Twelve differential clock outputs
- On-board EEPROM stores startup-configuration data
- XIN terminal can use laboratory signal generator or OCXO/TCXO/XO components and board
- Laboratory power supply connectors
- USB-C power supply
- Serial port for configuration and register read out

Computer Requirements

- USB 2.0 or USB 3.0 interface
- Processor: minimum 1GHz
- Memory: minimum 512MB; recommended 1GB
- Available disk space: minimum 600MB (1.5GB 64-bit); recommended 1GB (2GB 64-bit)

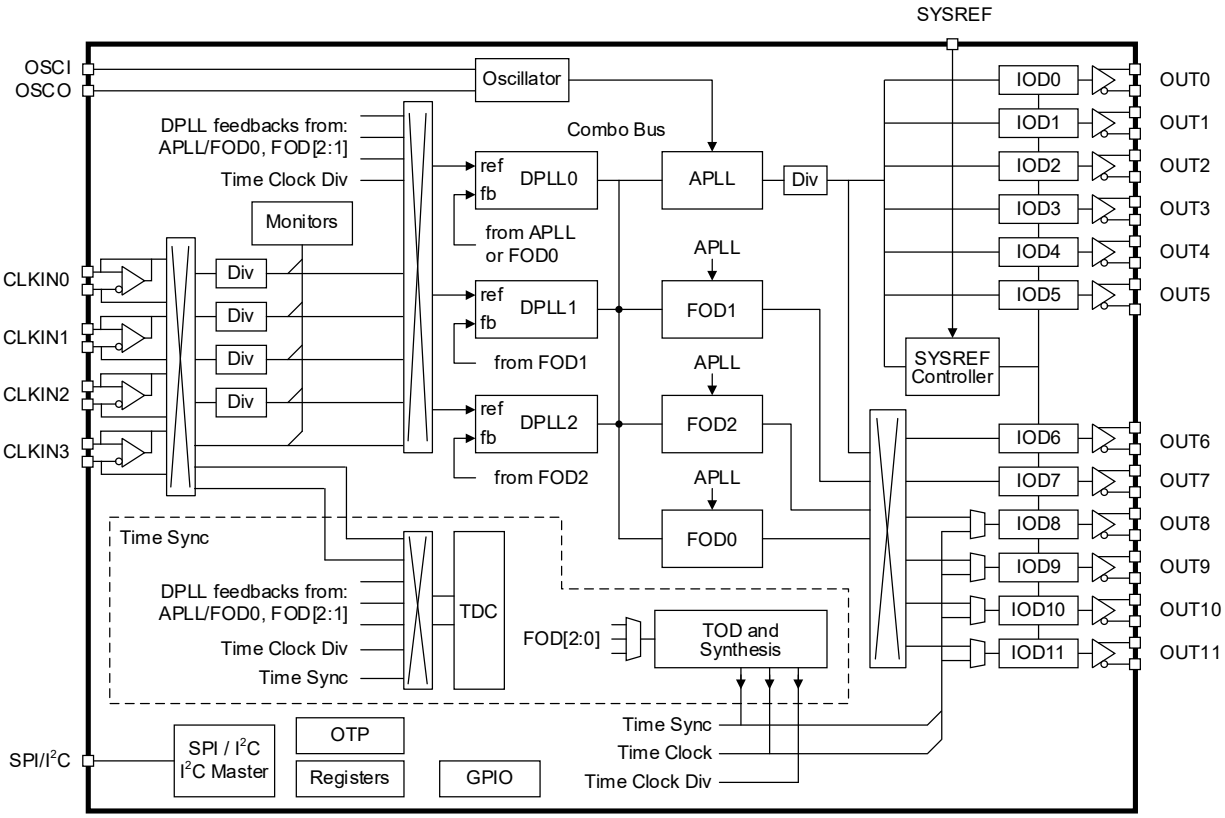


Figure 1. RC38312A Block Diagram

Contents

Figures

1. Functional Description

The evaluation kit is used to demonstrate the RC38312A, a fully integrated clock synthesizer/generator and clock jitter attenuator. The kit can be used to evaluate major parameters including phase noise, spurious attenuation, clock frequency, output skew, phase alignment, device timing, and the signal waveform. The device on the board accepts any input frequency from 1kHz to 1GHz.

The RC38312A consists of a single APLL and three DPLLs design that allows for multiple separate frequency domains. The APLL can be used independently of the DPLL to generate synthesized clocks at the outputs that track the frequency of the input at the XIN pin. The DPLL can be used for jitter attenuation, clock filtering, and frequency translation while tracking clocks from the CLKIN pins. The DPLLs provide a programmable bandwidth and a DCO function for real-time frequency/phase adjustment.

1.1 Operational Characteristics

The board is equipped with on-board LDOs that require a 5V supply. If connecting to a high-speed USB interface, the evaluation board may be powered directly from the USB connection. The board is designed to operate over the industrial temperature range from -40°C to +85°C, ambient temperature.

It is recommended to use proper grounding during board operations to avoid ESD damage to the EVB.

1.2 Hardware Setup and Configuration

The following sections describe the crystal, input clock, serial, GPIO, and output and power functions used for setting up device testing. The jumper setup example is shown in Figure 2.

- **I^2C/SPI Interface**

  SPI 4 wire interface in this example.

- **Power Supply**

  Use 5V_VDD with on-board LDO to generate 1.8V power rail. See Figure 2 for power select jumper settings (the J90 VDD = 1.8V setting is not used this example).

- **CLKx Inputs**

  The CLKx inputs are AC-coupled by default and can accept either differential input or single-ended input.

  Assume the signal source (for example, lab equipment requires 50Ω to GND termination at the receiver), the **CLK0, CLK1, CLK3** inputs have on-board terminations of 50Ω to GND with AC-coupling. The CLK0 input shows a 1.8V LVCMOS single-ended input with AC-coupling setting.

  CLK2 input has no on-board 50Ω termination. Sense connectors are provided for lab equipment monitoring (for example, scope with 50Ω input for monitoring the CLK input signal). If the sense connector is not used, then a dummy 50Ω load is required (see Figure 2).

- **Outputs**

  The outputs are AC-coupled without on-board pull-down or pull-up resistors. When setting the output to an HCSL driver, the on-chip pull-down needs to be enabled. If setting the CML, the on-chip pull-up needs to be enabled. Otherwise, the outputs will not present a signal.

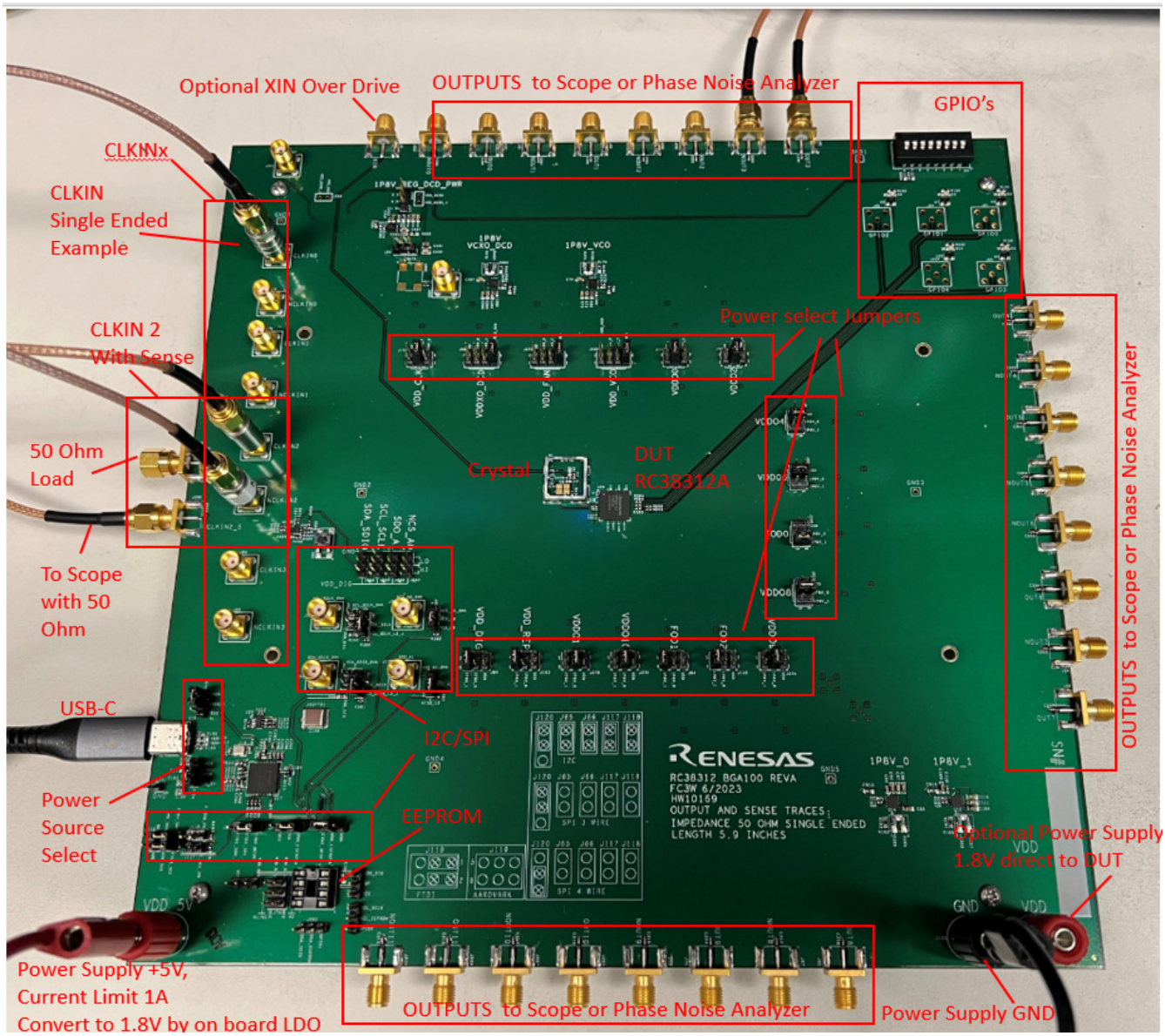


Figure 2. Evaluation Board – General Setup

Note: 1P8V_0, 1P8V_1, 1P8_VDDXO_DCD and 1P8_VCO refer to separate LDO's supply on the board. They can be used to isolate pin supplies from each other for performance optimization.

1.2.1. Power and USB-C Connections to Computer Host

The EVB is connected to a computer host via the USB3.0 to USB-C cable. It is recommended that the cable is connected to a USB3.0 port. However, a USB2.0 port is acceptable for the RC38312A to I^2C/SPI communications only. The USB-C provides +5V as power source to the on-board regulators. The on-board regulators support 3.3V and 1.8V voltages to the entire EVB. These voltages can be set by various jumpers found around the RC38312A.

The RC38312A voltage source can be derived from the on-board voltage regulators for 3.3V, 1.8V, or directly from the J90 banana connector with an external supply. The J90 connection can be used to measure total supply current into pins as reference. When jumpers are used to select power from J90 connector, the USB connection will still be required to connect to RICBox.

- Power Connection
  - Set the power supply voltage to 5V and the current limit to 1A
  - +5V (J123) = +5V
  - GND (J125) = GND
- Expected Current Draw: ~ 0.7A
  - After programming the device ~0.6A to ~1A during normal operation (device configuration dependent)

1.2.1.1. Power the Device with USB Connection

- Set jumper on J124 between pins 1 and 2
- Ensure that the EVB connects to a USB 3.0 (or newer) port

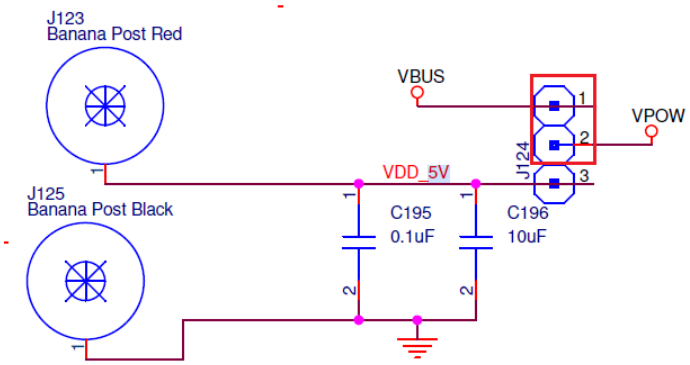


Figure 3. USB Power Jumpers

1.2.1.2. Power the Device with External Power Supply Connection and On-board Voltage Regulators

- Set jumper on J124 between pins 2 and 3
- Set jumper on J250 between pins 2 and 3
- Ensure 5V at banana jack J123 and GND connection

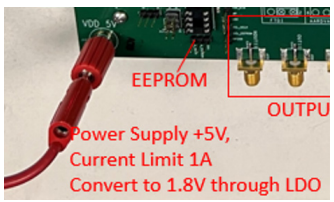


Figure 4. External 5V Board Input

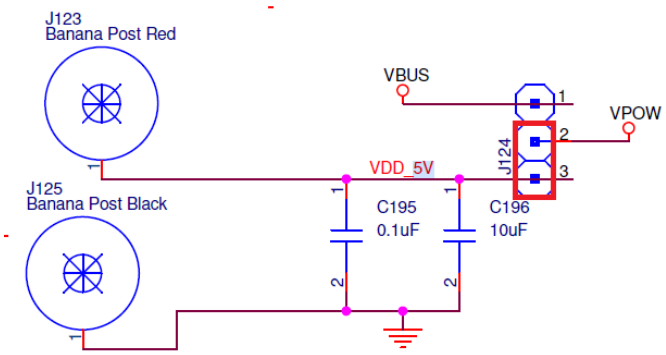


Figure 5. External 5V Schematic

Note: Allow for up to 2A of current with direct power supply. The device current will be increased during register write and calibration.

1.2.1.3. Power the Device Pins with External Power Supply Connection J90

- Ensure 1.8V or 3.3V at banana jack J90 and GND connection depending on the power pin
- Change the corresponding domain jumper selection to V_{DD}

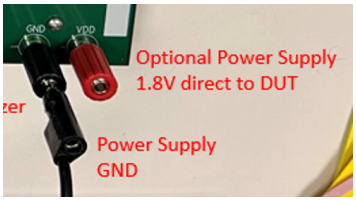


Figure 6. J90 Board Input

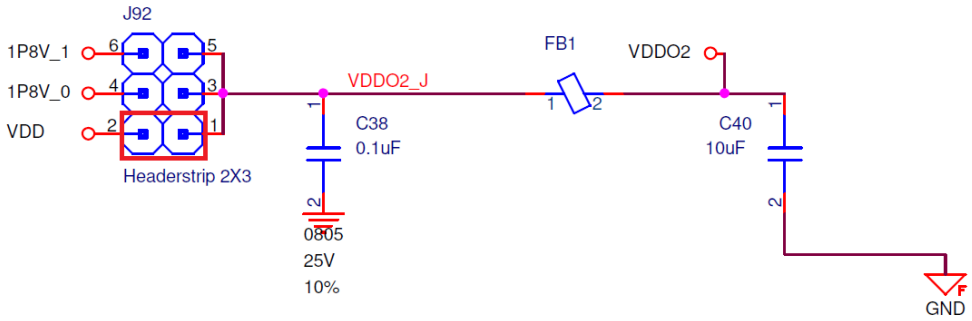


Figure 7. V_{DD} Jumper Bypass Schematic

Note: J90 can supply voltage for the entire device if all voltage pin jumper settings are configured for V_{DD} and the input voltage is 1.8V.

Important: All individual voltage domains run at 1.8V. Only VDD_DIG compatible with 3.3V. Supplying 3.3V to any other domain may cause damage to the RC38312A device.

1.2.2. Overdrive the XIN with an External Signal

The RC38312A device can support between 25MHz–80MHz on the XIN (crystal oscillator input) pin. There are several options for providing an input signal to the device XIN pin:

- An external signal (J2 SMA connector) typically from a signal generator
- An on-board crystal mount (U3); see section 1.2.3
- Two on-board XO mounts (U27, U29); see section 1.2.4

The following steps and Figure 8 describe how to overdrive XIN with an external signal:

1. Populate C1 with 0.1µF capacitor to ensure that J2 has a connected path to the RC38312A device.
2. Depopulate R570 and R569 (near DUT XOUT pin) to ensure that excess trace is not used.
3. Populate R4 with 50Ω for input termination (ensure signal is less than 1.3V amplitude).
4. Place input clock signal at J2 and ensure that the signal is within specification for the XIN pin.

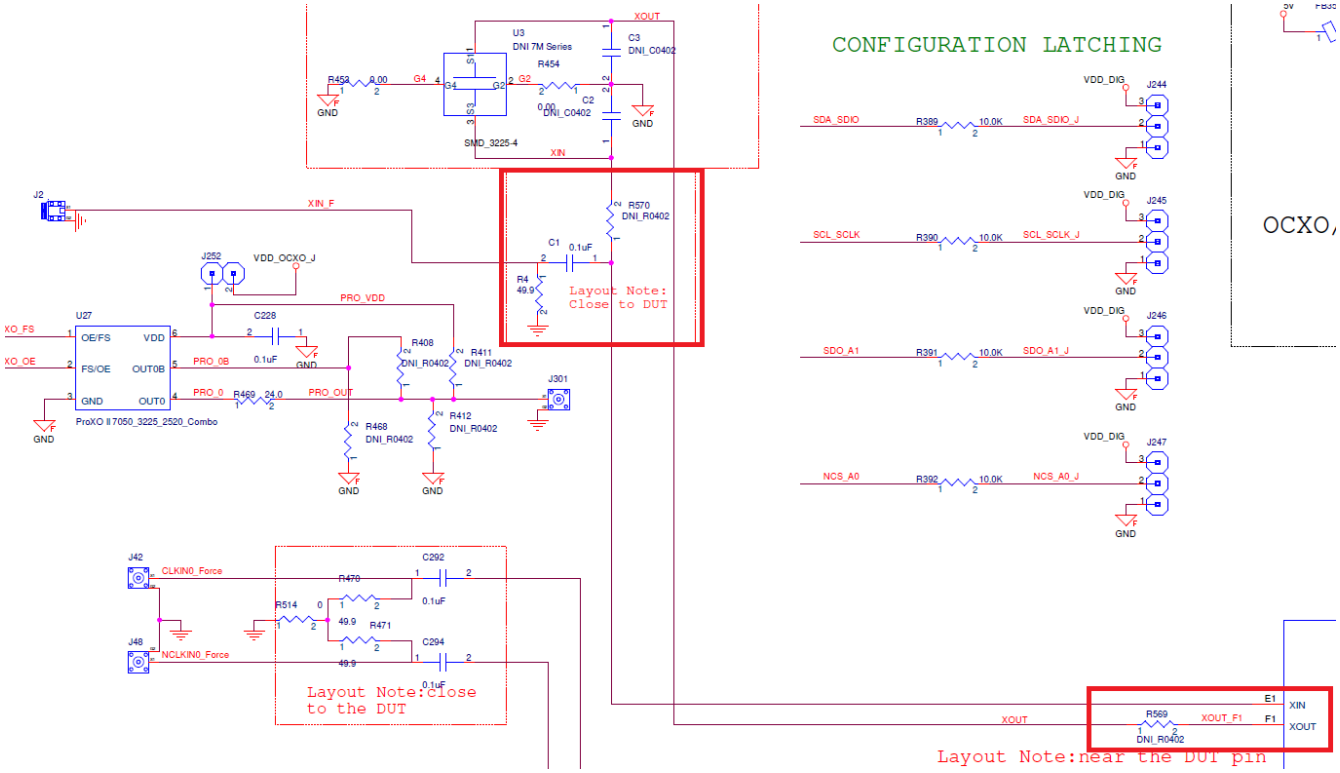


Figure 8. XIN Pin Overdrive Schematic

1.2.3. On-board Crystal Mount

The crystal mounting position can only be used if there is no other signal present on the XIN path (see Figure 9). To setup the evaluation board for crystal input:

1. Depopulate C1 to ensure there is no excess trace in the XIN pin.
2. Populate 0 Ohm to R570 and R569
3. Populate C2 and C3 to externally tune the input crystal frequency (if needed).

Note: The EVB stray capacitance is measured to be ~8.24pF.

4. Mount the crystal to U3.

Note: Crystal pin assignment can be varied. Check the pin assignment of the crystal being used. Remove R452 and R454 if needed.

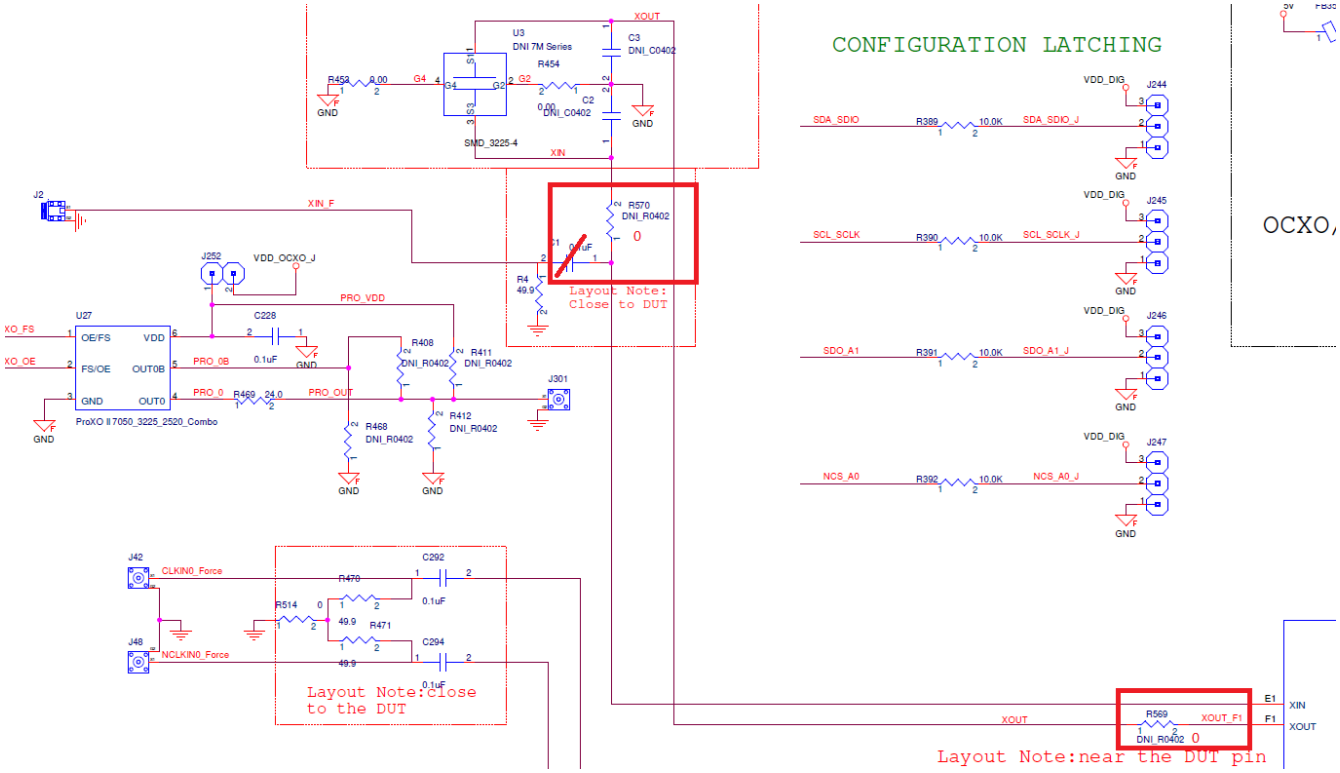


Figure 9. Crystal Mount Schematic

1.2.4. On-board XO Mount

The evaluation board contains an independent XO circuit with an SMA connector output. The U27 XO footprint located at the bottom of the board can be either 4-pin or 6-pin. The footprints are in parallel and should only be used one at a time. The J301 SMA connector is the output of the XO. Connect this output to overdrive the J2 XIN through a 50Ω coax cable. To ensure the proper operation of the XO, use the following steps and refer to Figure 10, Figure 11, Figure 12, and Figure 13.

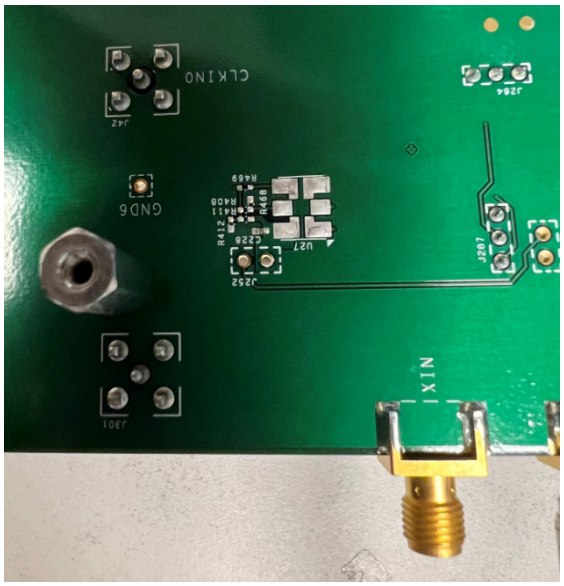


Figure 10. EVB XO Pads

1. Set J287 to proper LDO power supply voltage for the XO (3.3V, 2.5V or 1.8V)
2. Install jumper J252 to power-up the XO.

3. Set to Overdrive XIN.

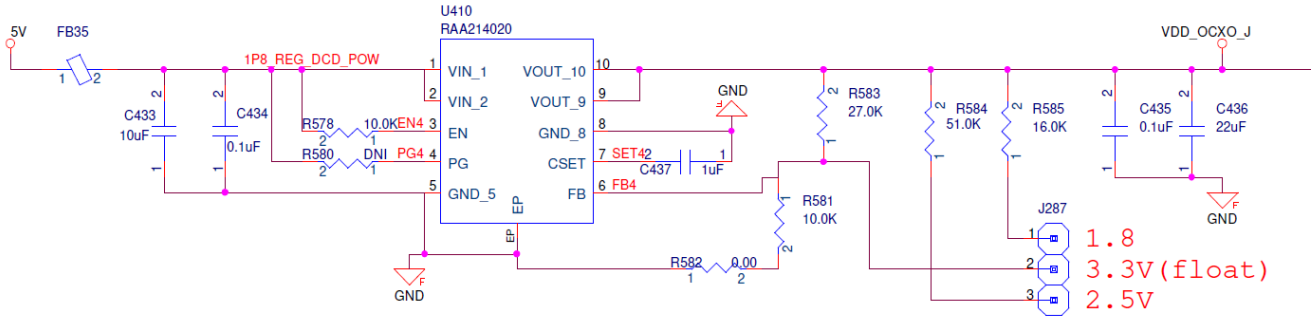


Figure 11. LDO Power Supply for XO and OCXO Connection Schematic

4. If the XO is a single-ended LVCMOS driver, ensure that the XO output is below the ~1.3V amplitude signal in order to support proper XIN pin characteristics. R469 can be populated with a resistor (for example, 24Ω or higher depending on the output impedance of the XO) to reduce the XO output amplitude.

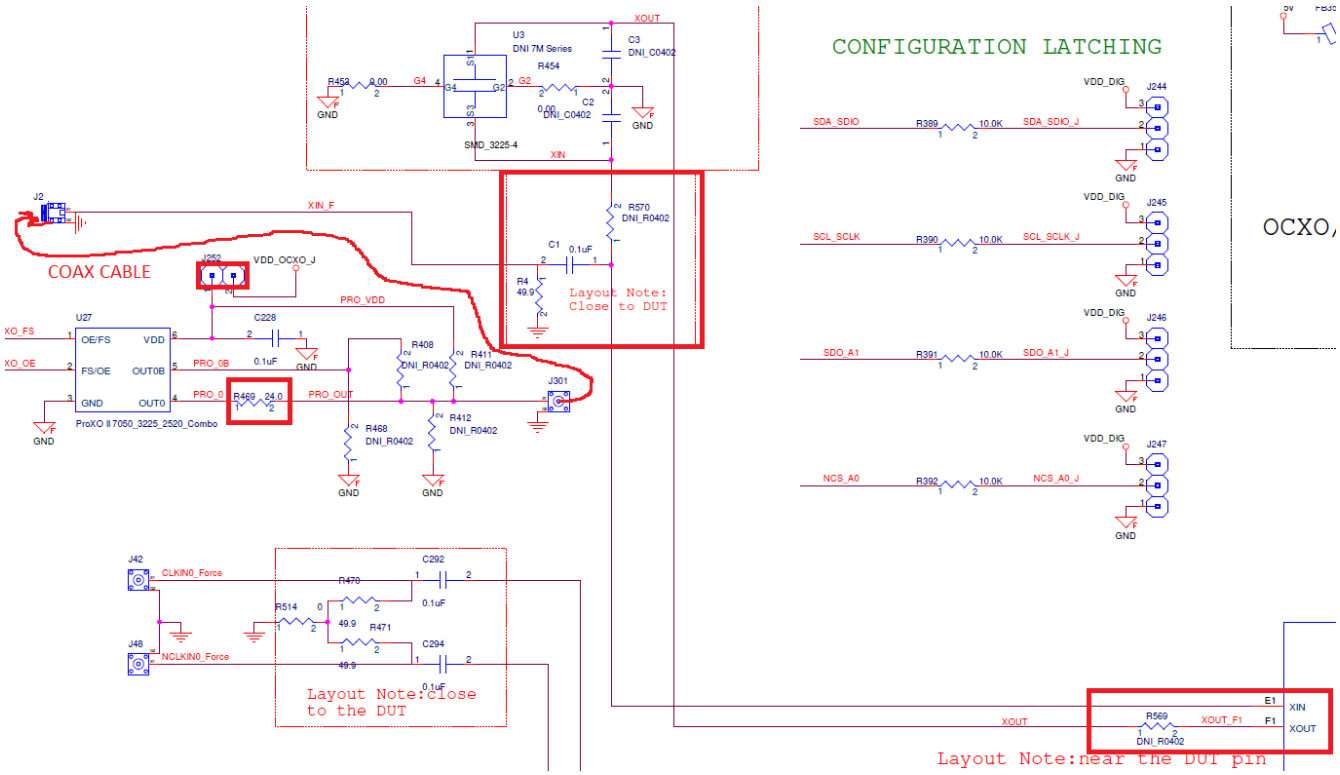


Figure 12. XO Schematic

5. Set the DIP switch SW1 S7 and S8 to pull the XO output enable pin high or low depending on the XO datasheet.
6. If the XO is a differential output driver, check the termination requirement of the XO. The spare footprint can be used for LVPECL, LVDS, HCSL drivers. In most cases, only one side of the differential driver is required to overdrive the XIN.

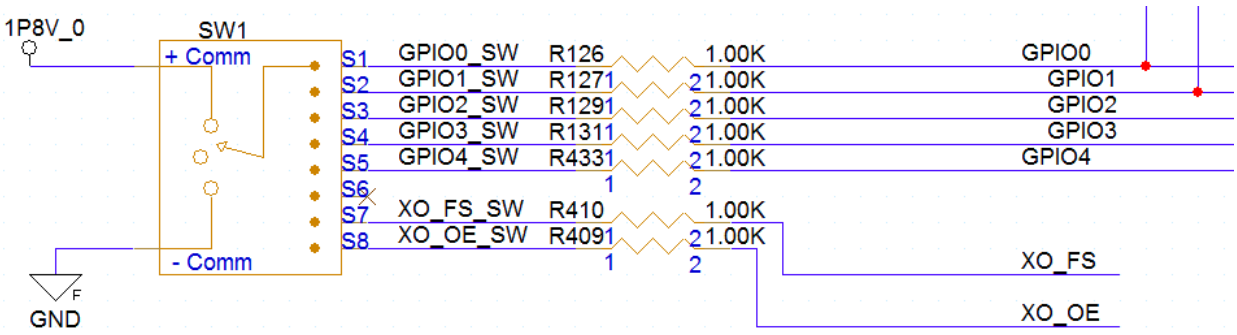


Figure 13. XO_OE and XO_FS Pins DIP Switch Schematic

1.2.5. Clock Inputs

The RC38312A can accept four differential clock inputs to be used as a jitter attenuator source. To enable proper connection, make sure the input termination resistor setup corresponds to the input signal that is connected. The evaluation board CLK0/nCLK0, CLK1/nCLK1 and CLK3/nCLK3, default termination setup has 50Ω to GND at each leg a shown in Figure 14.

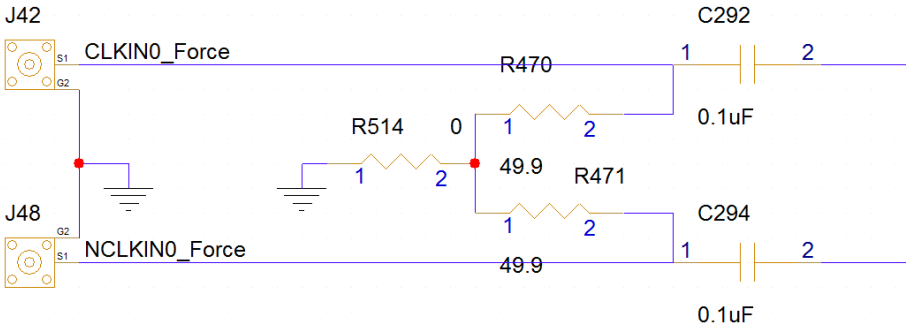


Figure 14. Input Clock Termination Schematic

The RC38312A contains internal AC-coupling for LVDS, HCSL, LVCMOS signals. Supported frequency ranges of the clock inputs are 1kHz to 1GHz in differential mode, and 1kHz to 250MHz in single-ended mode.

CLKIN2 input has a sense line for input to output phase measurement (see Figure 15). By default, the Sense SMA connectors J285 and J286 need 50Ω loading using either a dummy 50Ω load or a connection to a 50Ω scope for signal monitoring.

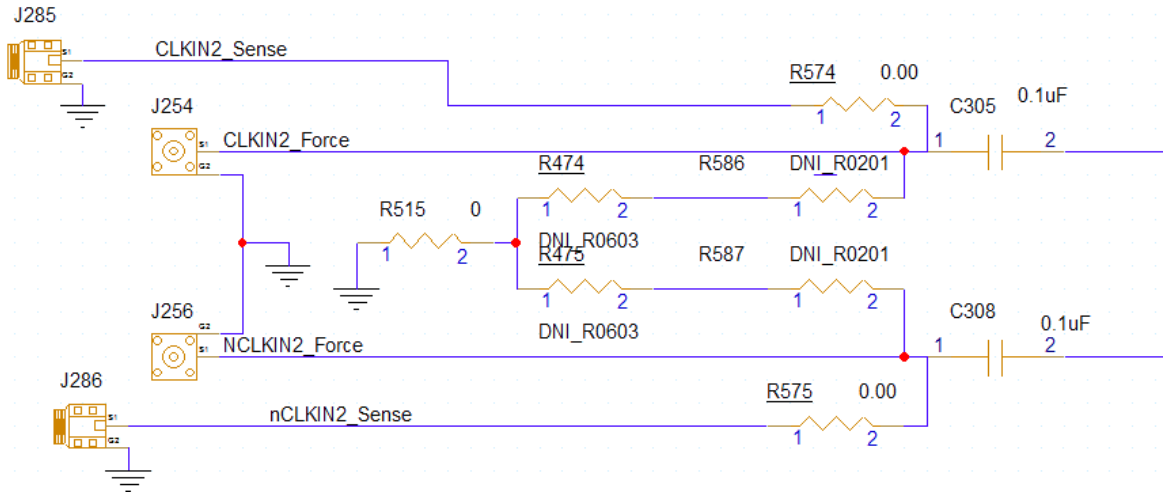


Figure 15. Input Clock with Sense Schematic

Note: Clock inputs are only used with **RC38312A** devices.

1.2.6. Clock Outputs

Each of the 12 differential output pairs can be programmed to LVDS, HCSL or CML logic type. The OUT8 to OUT11 can also be programmed to CMOS logic type.

- The HCSL mode supports HCSL by default and can be modified to support other modes by changing the amplitude and enabling/disabling the internal termination.
- The CML mode supports CML signal. The driver can be configured to enabling/disabling the internal termination and changing the amplitude.
- LVDS outputs can be configured to 350mV or 400mV swing up to 1V common mode voltage.
- Each output can also be tri-stated when not being used.
- For CMOS output type, output phase of each pin can be programmed to be 180 degrees out-of-phase, in-phase, or single-pin output.

The evaluation board does not provide an on-board pull-up for a CML driver or a pull-down for an HCSL driver.

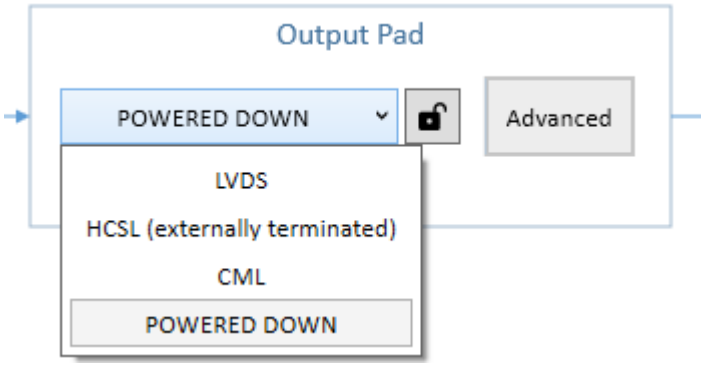


Figure 16. Output Type Options

The clock outputs of the evaluation board are AC-coupled without board level termination before the AC-coupling (see Figure 17). To achieve the output signal, the HCSL outputs need to enable the `<Internal pull-down>` through the registers. For evaluation, the monitor equipment (scope, phase noise system, etc.) receivers normally have 50Ω to GND for end termination.

For a CML driver, the driver can also be set to External Termination or Internal Termination. To achieve the output signal, the CML outputs need to enable the `<Internal pull-up>` through the registers.

For an LVDS driver, there is no option of Internal or Extermination termination. The output will switch without board level termination. It only requires 50Ω termination to GND at the monitor equipment.

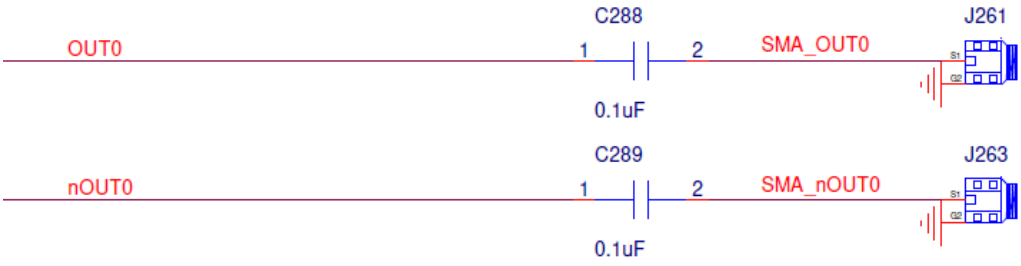


Figure 17. Output Clock AC-Coupling

1.2.7. Serial Connection

The EVB can be connected to a computer via a USB3.0 to USB-C connector. The on-board USB-to-MPSSE Bridge (FTDI FT232HQ) can handle the data communication. The +5V from the USB-C powers the on-board regulators (see section 1.2.1.1).

The Bus Source connector J119 is used to select the source of the communication bus. The bus will be 4 wire SPI for most communication but can also be I²C for specific tests. Pins 1 and 2 in J119 are SDA and SCL from the FTDI chip. Pins 3 and 4 pass the SDA and SCL to the I²C level shifter. To use the on-board FTDI chip, install jumpers on pins 1–3 and 2–4. The board will be shipped with these jumpers installed. Theoretically, any I²C adapter can be connected to pins 3 and 4 for SDA and SCL. Pin 6 can be used as the ground connection for the I²C connection. Pins 3, 4, 5 and 6 are arranged such that a Total Phase I²C Host Adapter (part number: TP240141) can be plugged onto pins 3, 4, 5 and 6 only (see Figure 18).

For default I²C operation, jumpers are installed on pins 1–3 and 2–4 (see jumper J119).

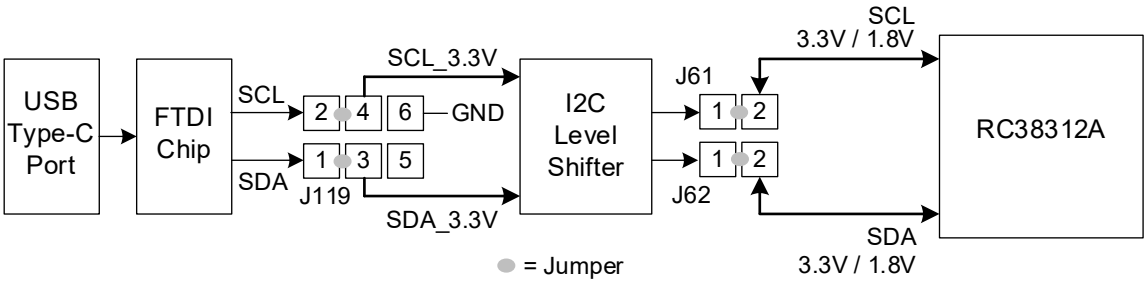


Figure 18. Communication Setup for I²C Mode

Note: For I²C operation instructions, contact Renesas support.

1.2.8. On-board EEPROM

The EVB also supports an external EEPROM IC for loading of an RC38312A configuration programmed into the EEPROM as an option. To load the configurations from EEPROM, the EEPROM load enable bit must be set in device OTP. If the enable bit is not set, the EEPROM load will be skipped.

The EVB provides a socket of 8-lead DIP8 SOIC-8 socket (Figure 19) so other EEPROM devices of different memory size can be tested.

Figure 19. EEPROM in Socket

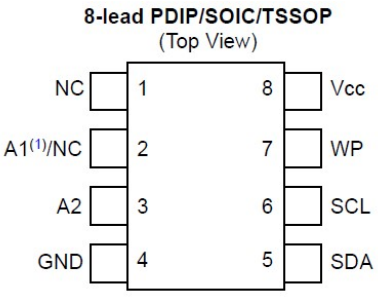


Figure 20. EEPROM Pin Description

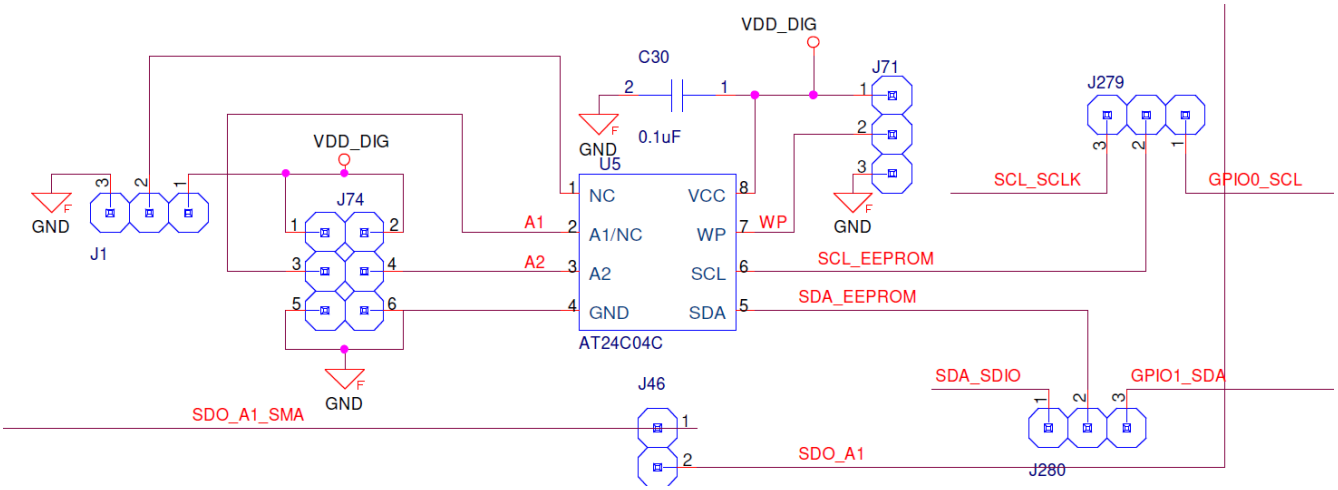


Figure 21. EEPROM Schematic

The A0(Pin 1), A1(Pin2) and A2 (Pin 3) are the EEPROM address inputs that can be pull either high or low using jumpers at J74 and J1 to define the device address. By default, jumpers can be removed so that A0, A1 and A2 are left floating as they are internally pulled down to GND in most EEPROM devices.

The WP pin is the write-protect input. When the WP pin is pulled down to GND (Low), the EEPROM can have normal write operations. When it is pulled up directly to V_{CC} (High), all write operations are inhibited. The WP pin can be controlled with a jumper at J71.

To establish a connection to the EEPROM, the SDA and SCL traces must be connected to the RC38312 SCL_SCLK/SDA_SDIO or GPIO0 and GPIO1 pins communication path through setting J279 and J280 as shown in Figure 22.

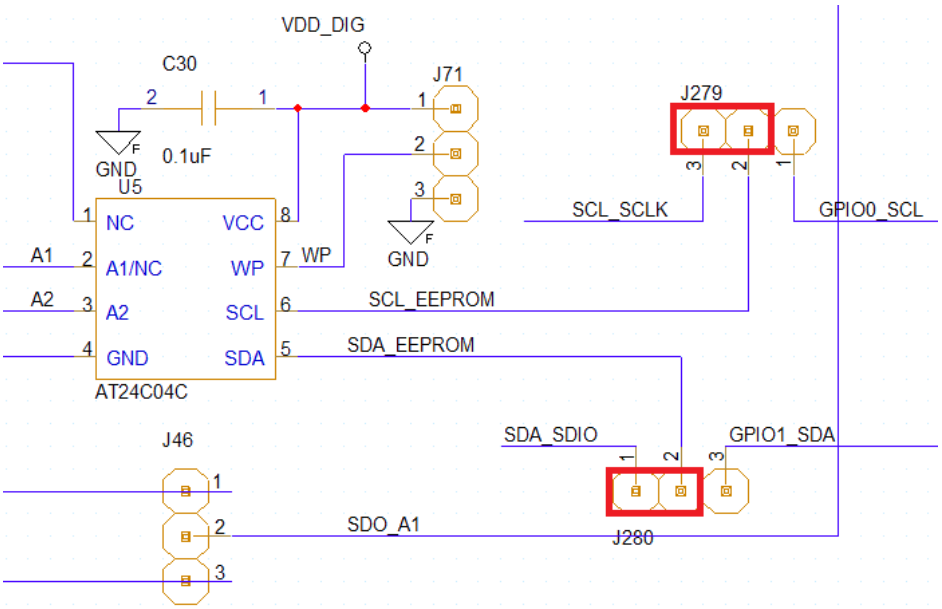


Figure 22. EEPROM Connection Jumpers for RC38312A SCL_SCLK and SDA_SDIO

For the EEPROM connected to the RC38312 GPIO0 and GPIO1 pins communication path through setting J279 and J280 as shown in Figure 23. Install 0 Ohm on R567 and R568. Remove R562 and R563.

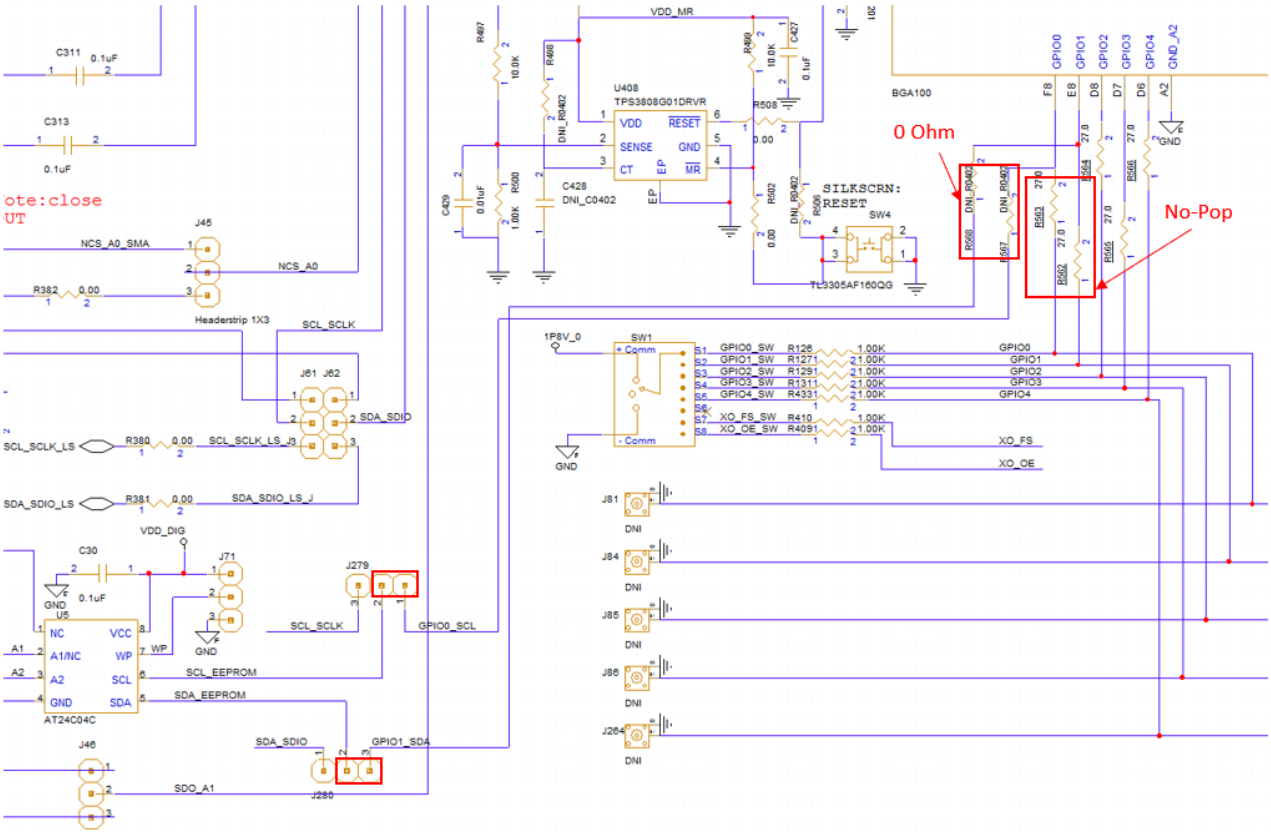


Figure 23. EEPROM Connection Jumpers for RC38312A GPIO

1.2.9. GPIO DIP Switch Selectors

The EVB has one DIP switch set (SW1) to support GPIO pins on RC38312A device. GPIOs 0–6 can support a two-level input (low/high). The middle position of the DIP switches leaves the pin open so GPIOs can be controlled with internal pull-up and pull-down resistors. Move to the '+' side to pull the pin high and move to the '-' side to pull the pin low. LEDs correspond to each GPIO to show the pin state.

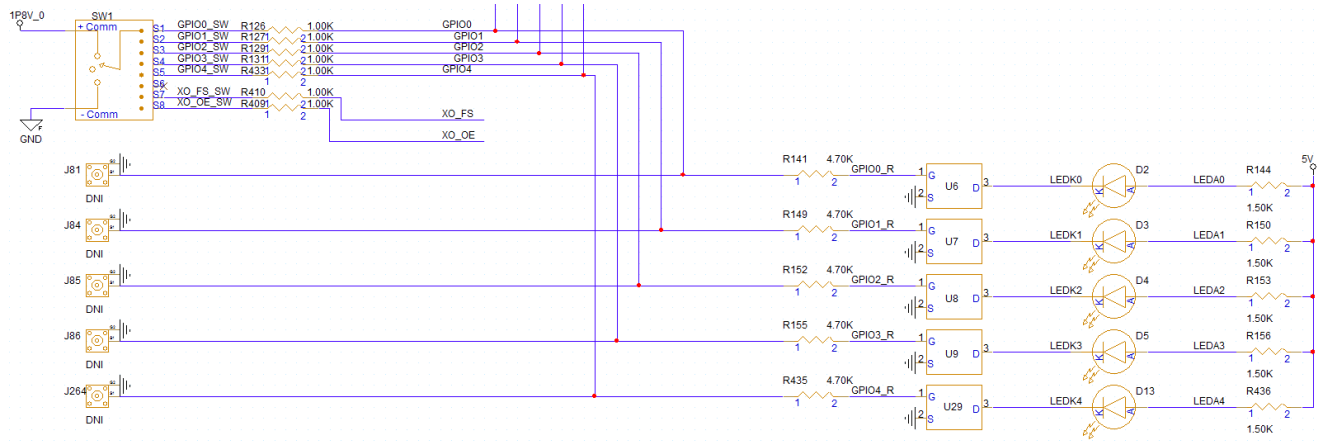


Figure 24. GPIO Schematic and EVB DIP Switches

2. Software Setup and Configuration

2.1.1. Prepare the Software

For software installation instructions, see the Renesas IC Toolbox Software Manual, sections 1 and 11.

2.1.2. Launch the GUI

After installing the Renesas IC Toolbox software, launch the software from the Windows *Start* menu at the bottom-left corner of the screen.

1. Click *Start* > *RICBox* to open the initial RICBox window.
2. Click *Create new project*.

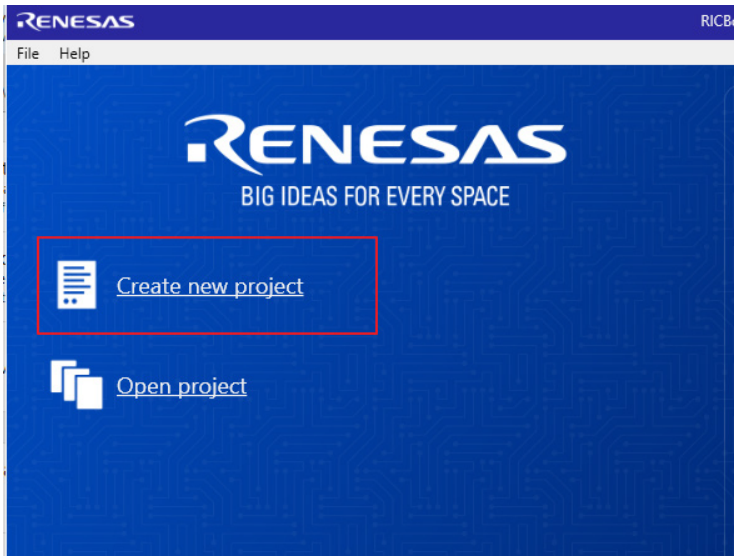


Figure 25. Create New Project in RICBox

3. Select *FemtoClock3* from the “Select a Product Family” list.
4. Select the product variant to evaluate, then click *OK*. In this example, the *RC38312A2* is selected.

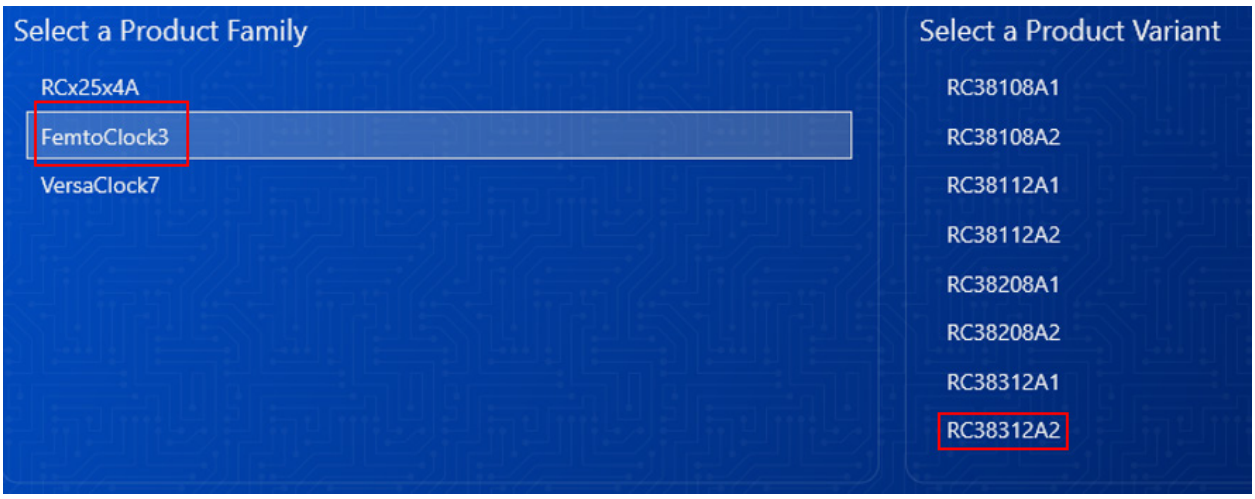


Figure 26. Selecting RC3832A Device GUI in RICBox

5. Follow the on-screen wizard (see Figure 27) to configure the device for general evaluation starting from “Inputs”, then “DPLL”, and finally ”Outputs”.

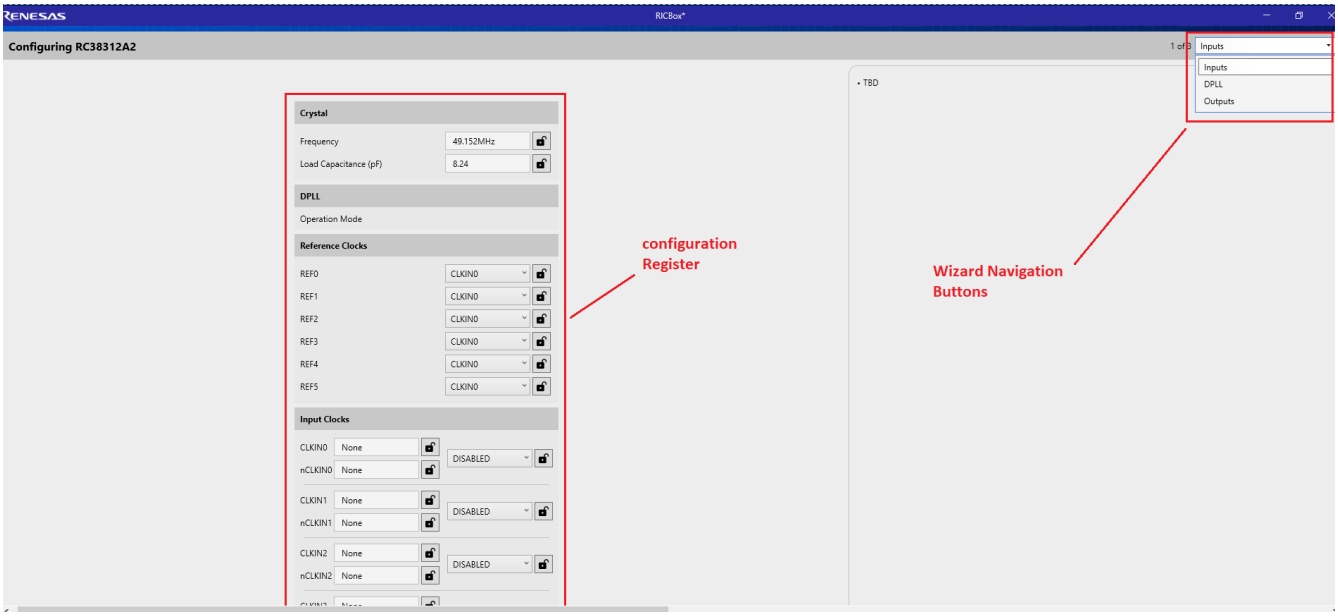


Figure 27. RICBox Wizard Navigation

6. Click on the *Finish* button after the settings are decided and to review the control panel page.
7. Use the side panel menu buttons (see Figure 28) to navigate through the GUI for all five separate pages.

Figure 28. RICBox GUI Menu Buttons

2.1.3. Configure the Evaluation Board

1. To establish communication between the EVB and the GUI, click the *Not Connected* button (1) in the lower right corner, then click *Connect* (2).

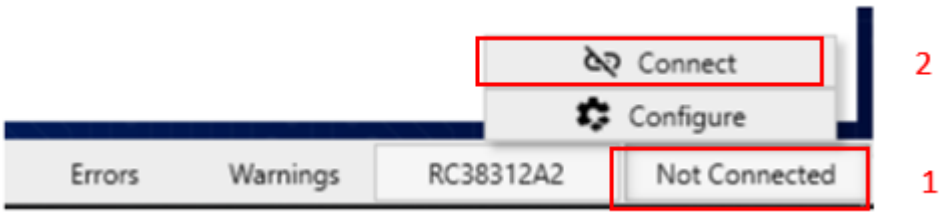


Figure 29. Connect to the Device in RICBox

2. Once the RICBox connection is established to the EVB, the *Not Connected* button will change to *Connected*.

Figure 30. Connected Button

3. Click the *Program* button to write all the changed registers from the GUI to the on-board device. Any register changes made after clicking the *Program* button will occur in real-time and the device will update.

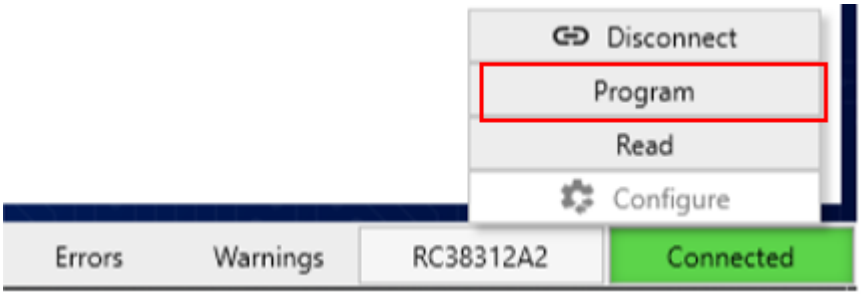


Figure 31. Program Button

3. Board Design

The RC38312A EVB schematic and BOM is available upon request.

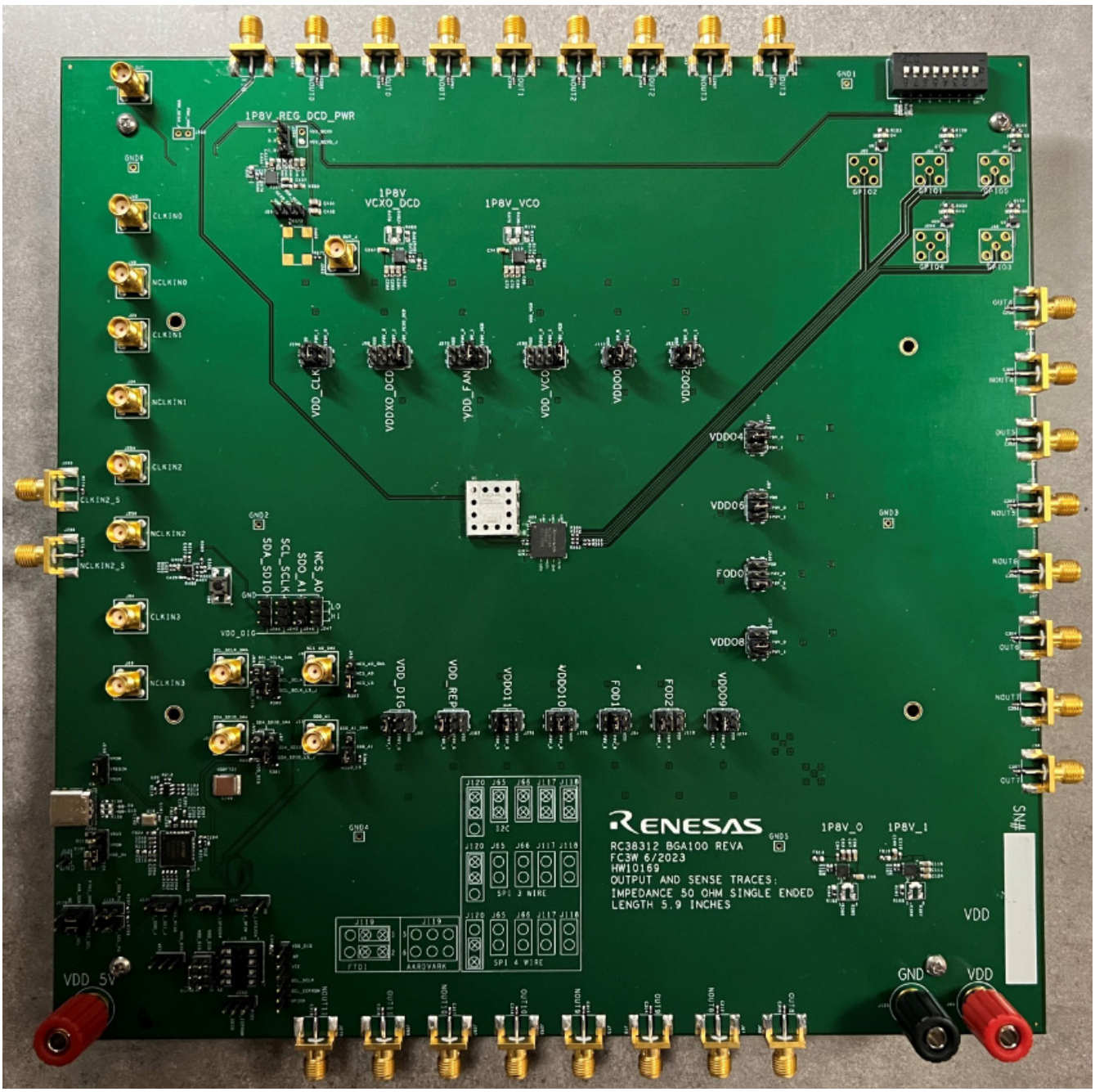


Figure 32. RC38312A Evaluation Board (top)

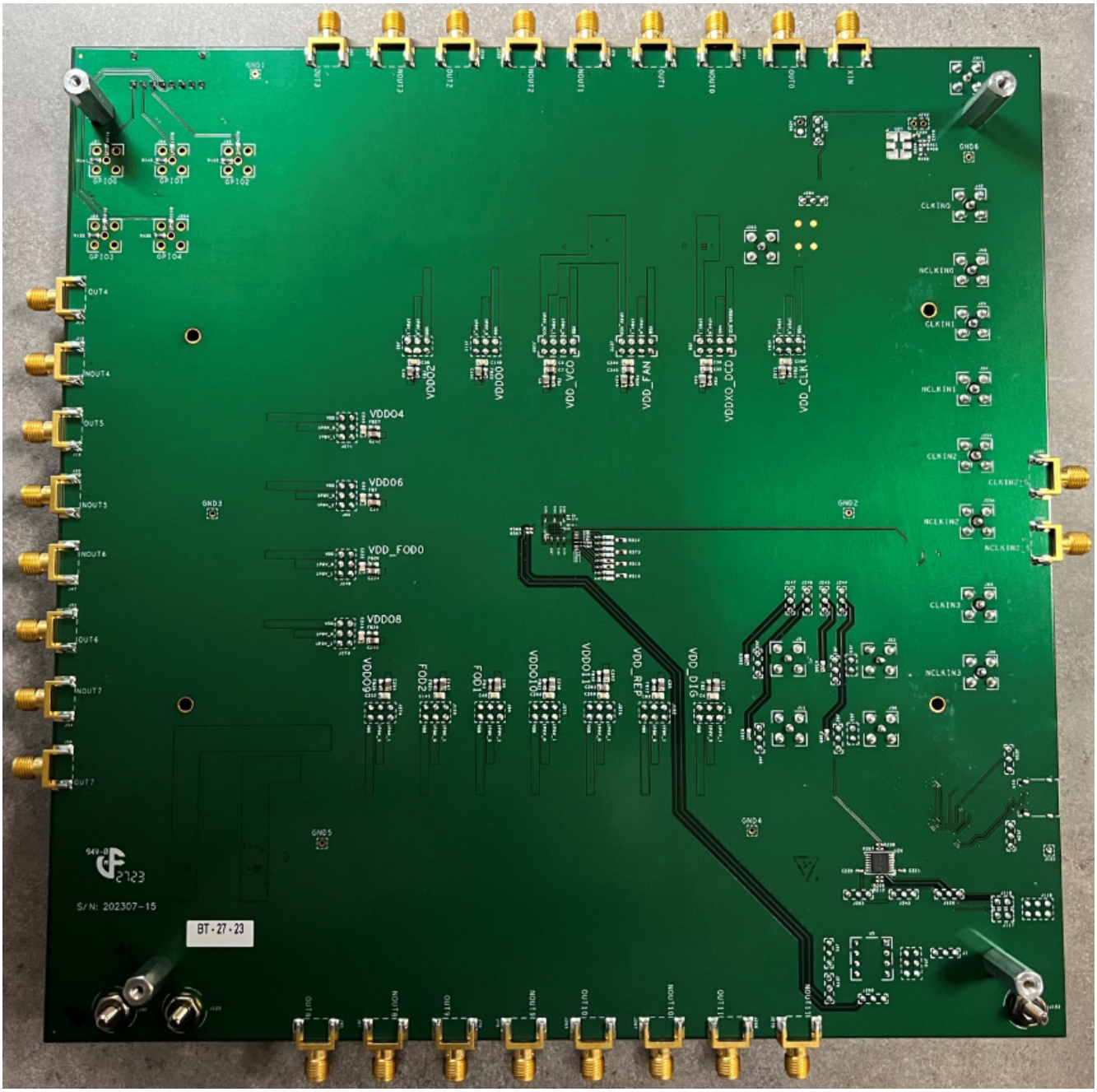
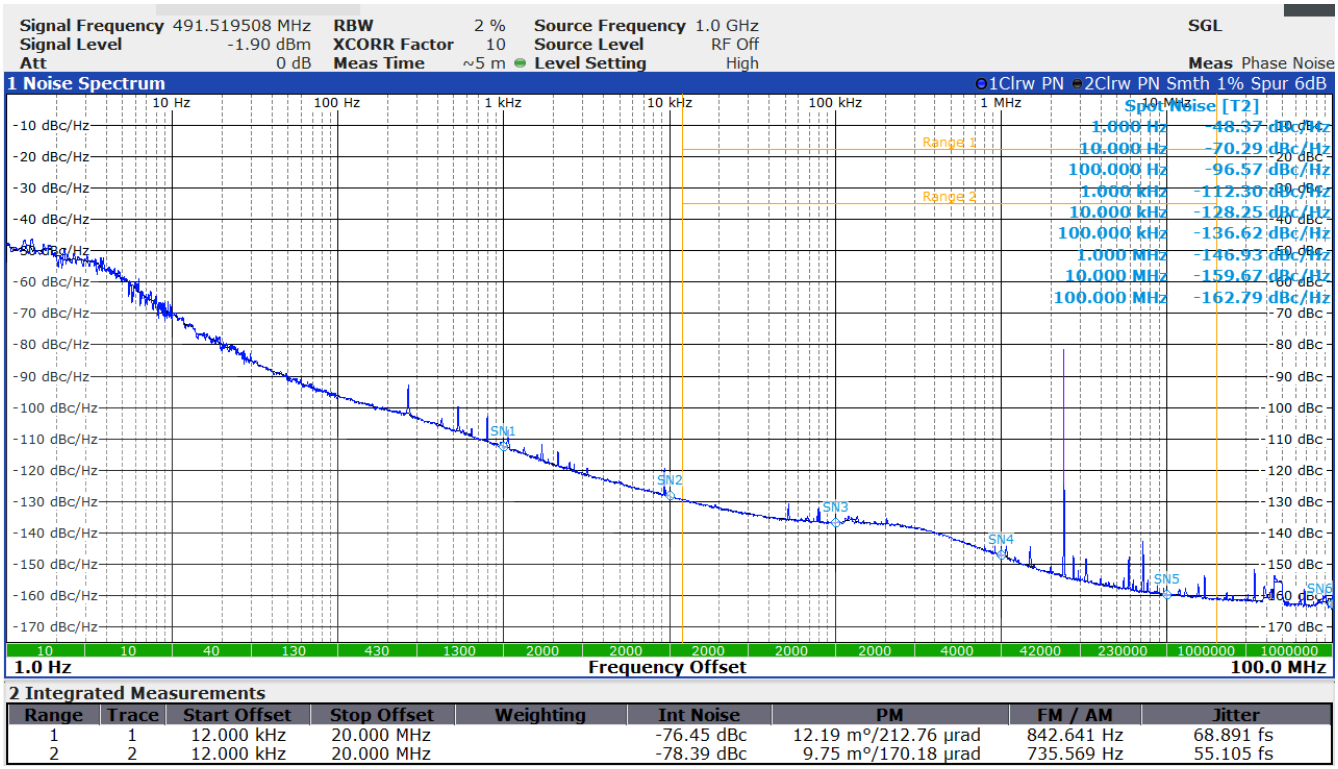


Figure 33. RC38312A Evaluation Board (bottom)

4. Typical Performance Graphs



Range	Trace	Start Offset	Stop Offset	Weighting	Int Noise	PM	FM / AM	Jitter
1	1	12.000 kHz	20.000 MHz		-76.45 dBc	12.19 m°/212.76 µrad	842.641 Hz	68.891 fs
2	2	12.000 kHz	20.000 MHz		-78.39 dBc	9.75 m°/170.18 µrad	735.569 Hz	55.105 fs

Figure 34. Phase Noise 491.52MHz Output Synthesizer Mode

5. Ordering Information

Part Number	Description
RC38312A-EVK	RC38312A Evaluation Board

6. Revision History

Revision	Date	Description
1.01	Mar 3, 2025	Updated bullet text in section 1.2.1.2 to “Set jumper on **J250** between pins 2 and 3” from “Set jumper on **J259** between pins 2 and 3”.
1.00	Sep 12, 2023	Initial release.

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