RA6W2 Hardware Design Guide

This document provides hardware design considerations for RA6W2.

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Tables

1. Terms and Definitions

BPF	Band Pass Filters
DK	Development Kit
ESR	Equivalent Series Resistance
ESD	Electrostatic Discharge
GPIO	General Purpose Input Output (pin)
GND	Ground
IC	Integrated Circuit
JTAG	Joint Test Action Group
MCU	Microcontroller
NP	Not Populated
OTP	One-Time Programmable Memory
PCB	Printed Circuit Board
PCBA	Printed Circuit Board Assembled
POR	Power-On Reset
RF	Radio Frequency
SDIO	Secure Digital Input Output
SWD	Serial Wire Debug
UART	Universal Asynchronous Receiver Transmitter

2. Introduction

RA6W2 is a highly integrated microcontroller (MCU), with integrated dual band IEEE 802.11 b/g/n/ax and Bluetooth V5.1. Wi-Fi subsystem and Bluetooth LE subsystem are independent to each other.
The ultra-low-power Wi-Fi subsystem integrates an Arm® Cortex®-M33 system processor with a dual band 802.11 a/b/g/n/ax radio, on-chip memory, flexible peripheral interfaces, and power management features.
The Bluetooth LE subsystem, is ultra-low power, integrating a 2.4 GHz transceiver and an Arm® Cortex®-M0+ microcontroller with a RAM of 48 kB and a One-Time Programmable (OTP) memory of 32 kB. The radio transceiver, the baseband processor, and the qualified Bluetooth® low energy stack are fully compliant with the Bluetooth® Low Energy 5.1 standard.
The RA6W2 is a synthesis of breakthrough ultra-low-power technologies, which enables an extremely low power operation in the system. The Wi-Fi and Bluetooth® LE shut down every micro element of the chip that is not in use, which creates a power consumption that is near zero when not actively transmitting or receiving data. Such low-power operation can extend the battery life up to a year or more depending on the application. The Wi-Fi also enables ultra-low-power transmission and reception modes when the MCU needs to be awake to exchange information with other devices. Advanced algorithms enable Sleep mode until the exact moment when wake-up is required to transmit or receive data.

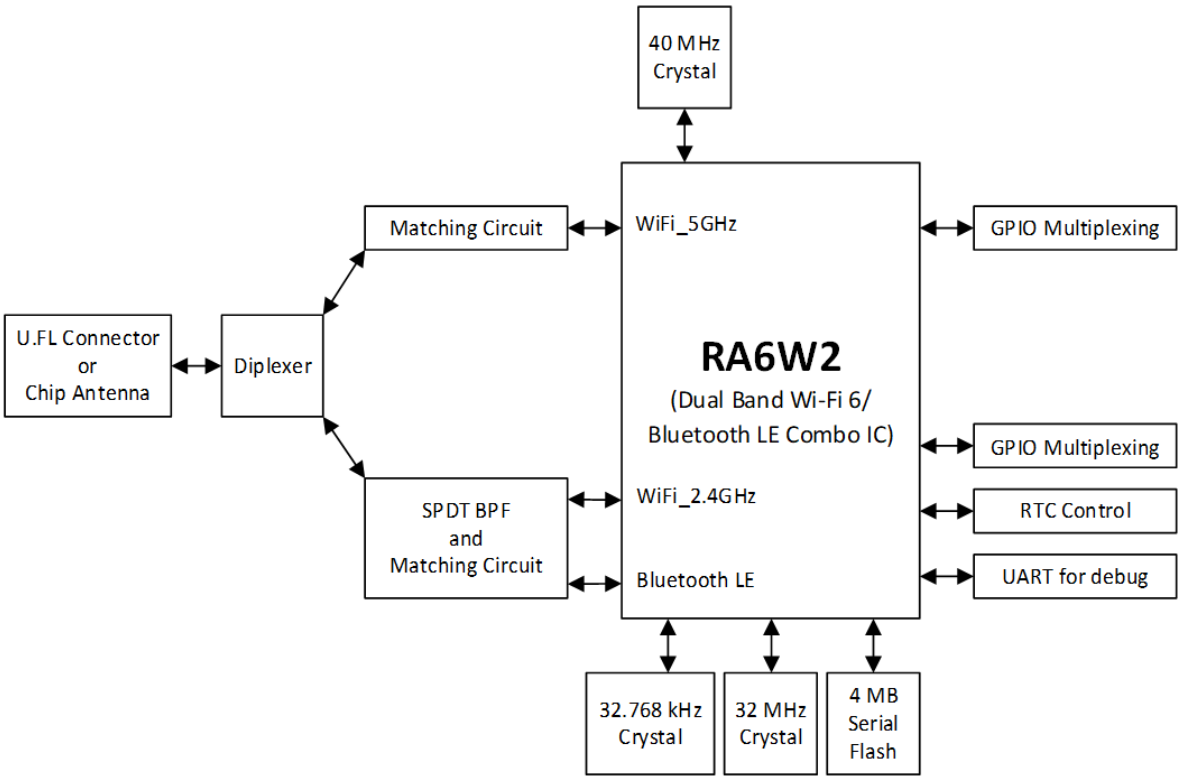

Figure 1. RA6W2 system block diagram

Built from the ground up for the Internet of Things (IoT), the RA6W2 is ideal for door locks, thermostats, sensors, pet trackers, asset trackers, sprinkler systems, connected lighting, video cameras, video doorbells, wearables, and other IoT devices. Figure 1 shows the block diagram of RA6W2 system.
VFBGA93 is the only available package for the RA6W2.

Figure 2 shows the ball and pin assignments and Table 1 shows the differences in features for both versions.

Table 1. RA6W2, VFBGA93 package characteristics

Features	RA6W2
Package (the package dimensions are accessible through the Renesas website – VFBGA93)	VFBGA93, 3.9 mm × 6.4 mm
Number of balls	93
Number of GPIOs, Wi-Fi subsection	28
Number of GPIOs, Bluetooth® LE subsection	5

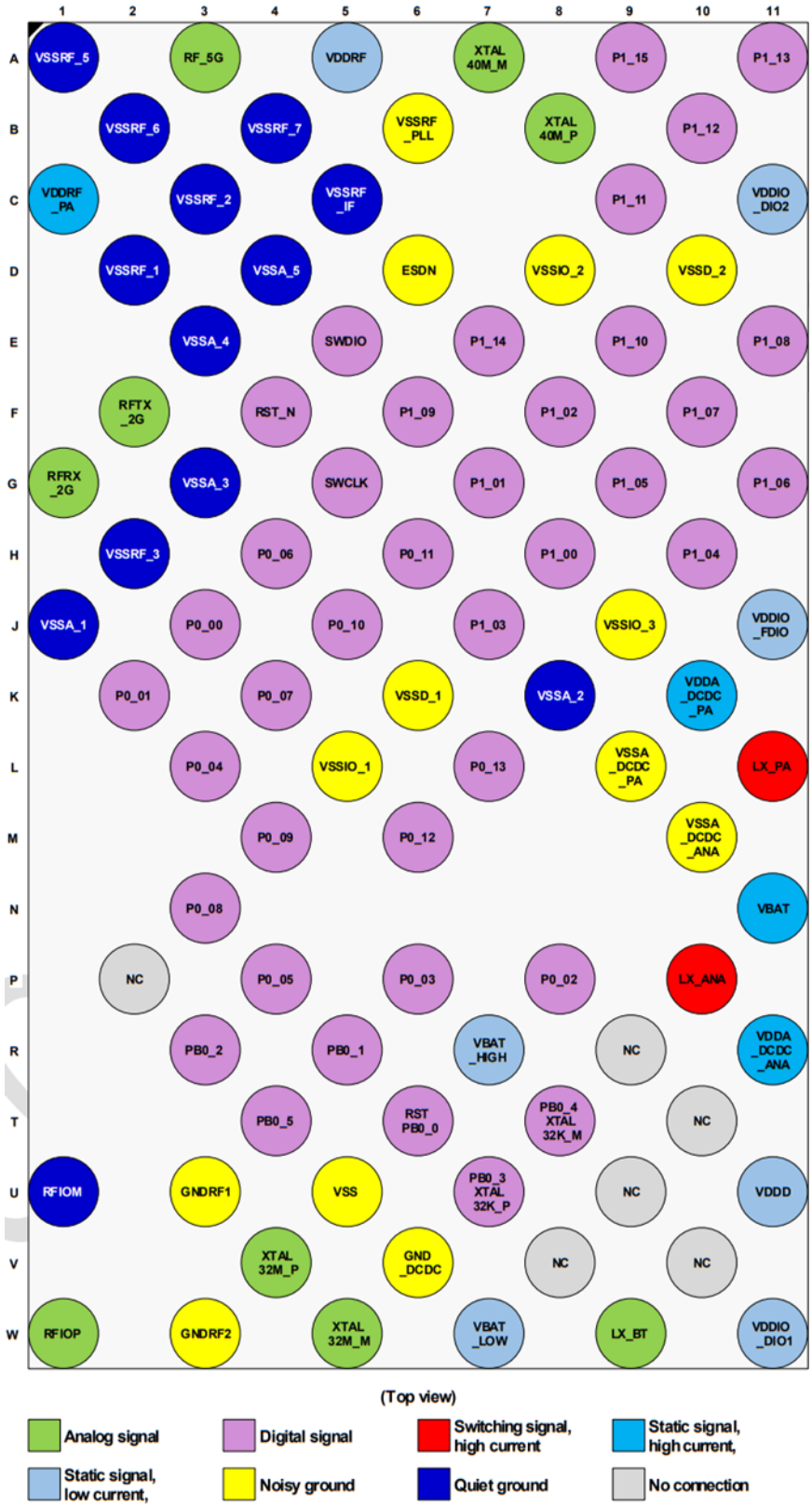

Figure 2. RA6W2, VFBGA93 ball assignment

3. Device Revision Numbering and Marking

The revision number of the chip can be read from the device by reading the Arm Cortex registers in Table 2 and Table 3. Note that the registers are accessed from the Wi-Fi subsystem.

Table 2. CHIP_REVISION_REG (0x40070214)

Bit	Mode	Symbol		Reset
7:0	R	CHIP_REVISION	Chip version, corresponds with type number in ASCII 0x41 = 'A', 0x42 = 'B'.	

Table 3. CHIP_TEST1_REG (0x400702f8)

Bit	Mode	Symbol/Description	Reset
7:0	R	CHIP_LAYOUT_REVISION Chip layout revision corresponds to type number in ASCII. 0x41 = A, 0x43 = C, and so forth for the WLCSP package 0x42 = B, 0x44 = D, and so forth for the VFBGA package	

4. Minimal Design for RA6W2 MCU

The RA6W2 MCU requires a minimum number of external components for proper operation. The necessary sections required for the minimal system operation are:

- Power section
- Crystals and Clocks
- Radio section
- JTAG
- UART
- Memory
- Reset
- Proper PCB routing

Figure 3 shows the required external components, like crystals, decoupling capacitors, power inductors, and radio components.

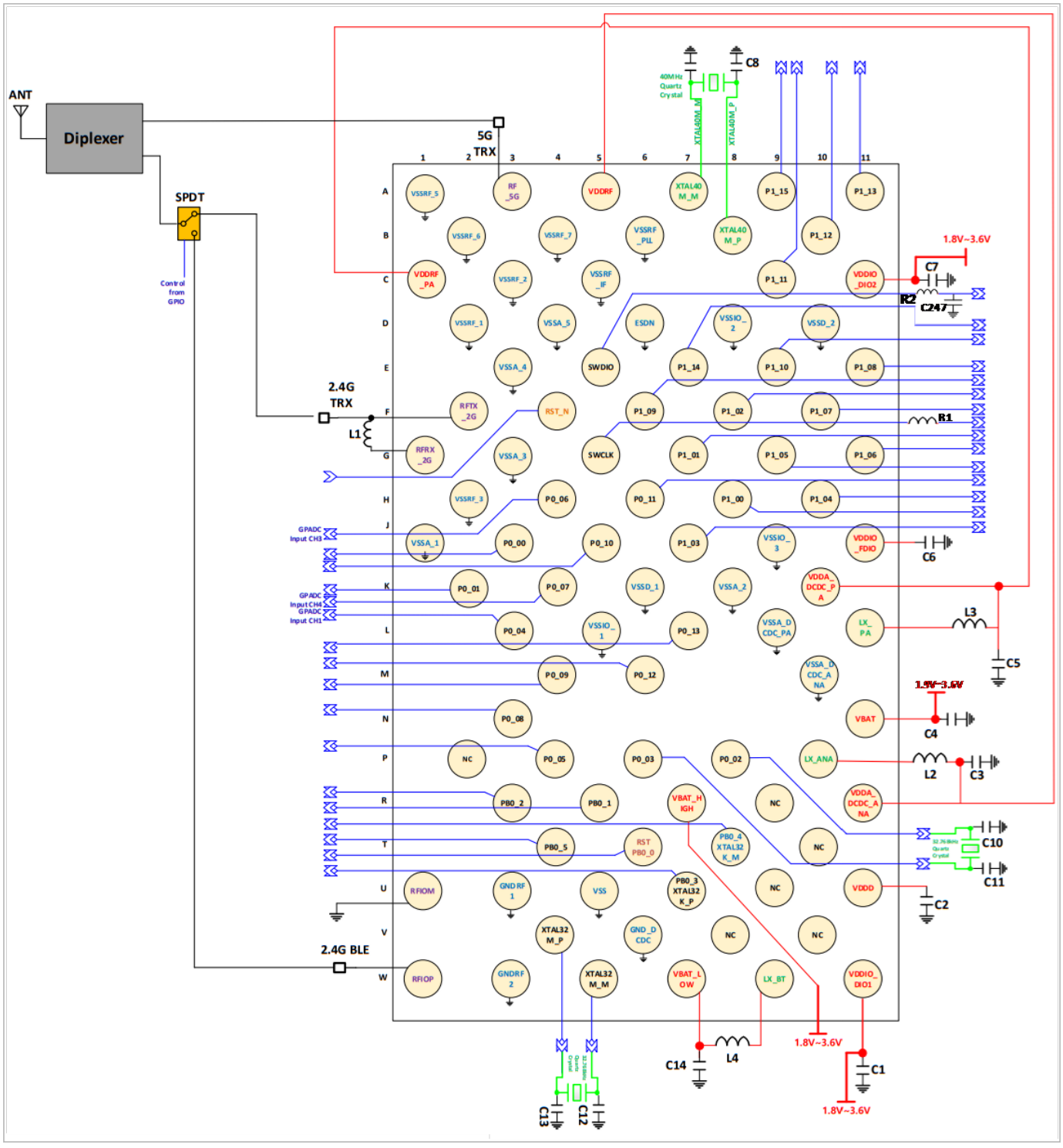

Figure 3. Typical application of Wi-Fi/Bluetooth LE combo application with diplexer

4.1 Power Section

The RA6W2 MCU contains internally all power management for proper and safe system operation.
Stresses beyond listed under Absolute Maximum Ratings (see *RA6W2 Datasheet*) may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
There are four main power inputs, as shown in Table 4, VBAT, VDDIO_DIO1, and VDDIO_DIO2 for the Wi-Fi subsystem and VBAT_BLE for the Bluetooth LE.

Table 4. RA6W2 recommended input power supply operating conditions

Parameter	VFBGA93, Ball No	Min	Typ	Max	Units
VBAT	N11	1.9	3.3	3.6	V
VDDIO_DIO1	W11	1.62	3.3	3.6	V
VDDIO_DIO2	C11	1.62	3.3	3.6	V
VBAT_BLE	R7	1.8	3.3	3.6	V

Figure 4 shows the input voltage signals as well the other power rails of RA6W2 MCU.

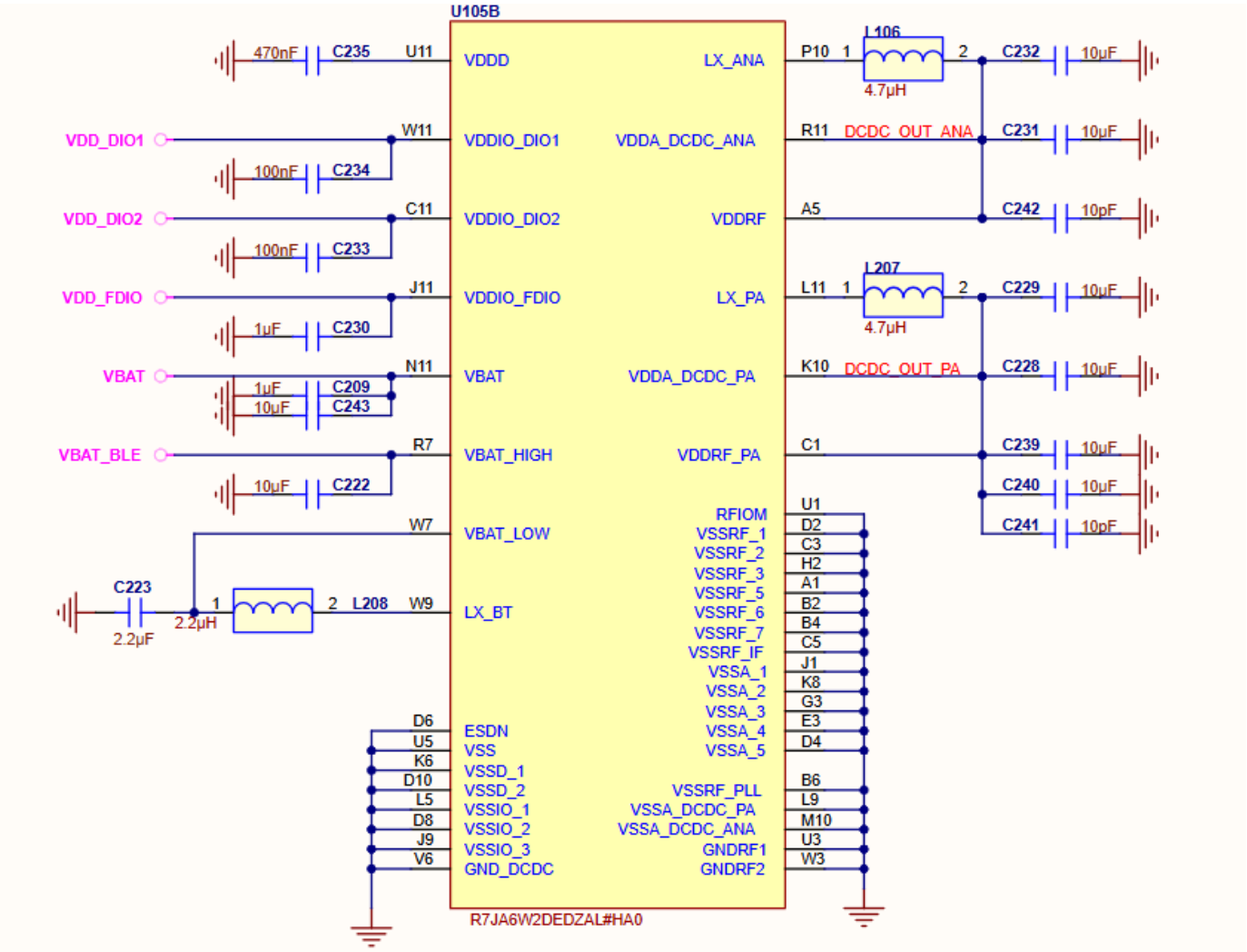

Figure 4. RA6W2 power section schematic

VBAT: this input and it is the main supply of Wi-Fi subsystem. It supplies the two DC-DC converters, the Reset pin and the pins P0_00 to P0_03. The voltage range for VBAT is 1.9 V to 3.6 V. A 10 µF decoupling capacitor is required to be placed close to the pin.

VDDIO_DIO1: this is the input supply pin for P0_04 to P0_13 Digital IO power for the Wi-Fi subsystem. The VDDIO_DIO1 rail needs to be decoupled with a 0.1 µF ceramic capacitor and typical voltage is 3.3 V.
VDDIO_DIO2: this is the input supply pin for P1_10 to P1_17 Digital IO power for the Wi-Fi subsystem. The VDDIO_DIO2 rail needs to be decoupled with a 0.1 µF ceramic capacitors and typical voltage is 3.3 V.
DCDC_PA and VDDRF_PA: no external load to be connected to this rail. These two pins are used for the RF PA of the Wi-Fi subsystem.
The DCDC_OUT_PA output and the VDDRF_PA input must be connected externally. The DCDC_OUT_PA rail output 1.35 V to VDDRF_PA, the inductor (4.7 µH inductor, recommend: MPH201214S4R7MT or LQM21PN4R7MGH) having a low DC resistance, is connected to the LX_PA pins. One 22 µF or two 10 µF capacitors per pin (DCDC_PA and VDDRF_PA) must be allocated. GRM155R61A106ME11 can be used for the ceramic capacitor of 10 µF, 0402. Due to cost, the approach of 2 x10 µF instead of a 22 µF is suggested.
DCDC_ANA and VDDRF: no external load to be connected to this rail. These two pins are for the RF and analog section for Wi-Fi subsection.
The DCDC_OUT_ANA output and the VDDRF input must be connected externally. The DCDC_OUT_ANA rail output 1.375 V to VDDRF, the inductor (4.7 µH inductor, recommend: MPH201214S4R7MT or LQM21PN4R7MGH) having a low DC resistance, is connected to the LX_ANA pins. Two ceramic capacitors of 10 µF, one per pin (DCDC_ANA and VDDRF) must be allocated. GRM155R61A106ME11 can be used for the ceramic capacitor of 10 µF, 0402. Due to cost, the approach of 2x10 µF instead of a 22 µF is suggested.
VDDIO_FDIO: this power rail supplies P1_00 to P1_09 and the external Flash memory. It is connected by default to the internal FDIO_LDO with voltage equal to 1.8 V. An 1 µF-capacitor is used for decoupling.
By connecting a 3.3 V external voltage rail, VDD_FDIO can operate to 3.3 V. In this case, a 3.3 V QSPI Flash must be used.

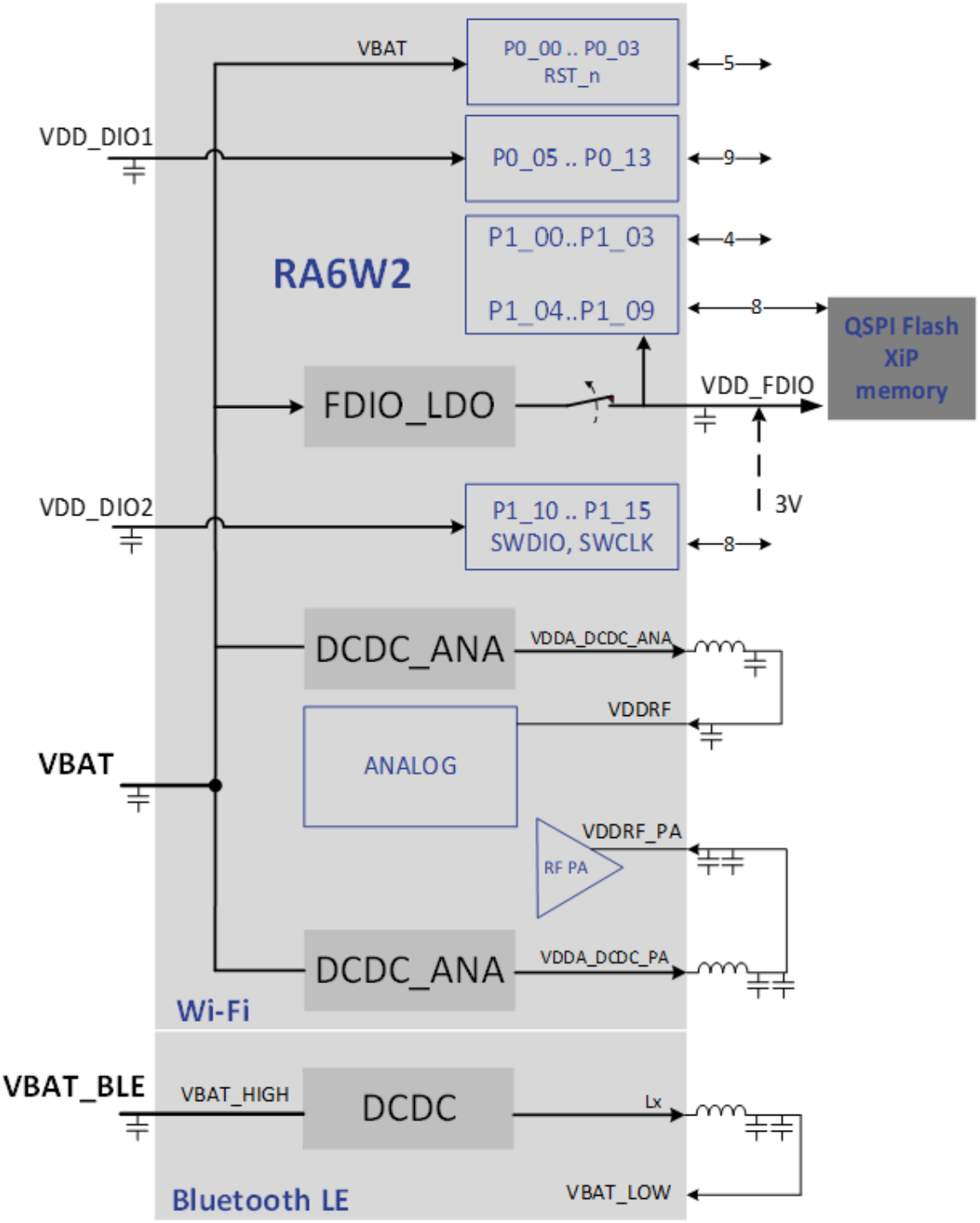

Figure 5. RA6W2 power configuration

VBAT_BLE: It is the main input for the Bluetooth LE subsystem. This voltage rail is connected to the pin R7, VBAT_HIGH configuring the internal DC-DC in Buck mode.
In Buck mode, VBAT_BLE, is in the range of 1.8 V – 3.6V. GPIOs and OTP are supplied from VBAT_HIGH. The lowest voltage for OTP reading is 1.62 V whereas to write OTP this is 2.25 V.
VBAT_HIGH is protected by the power-on-reset circuit POR_HIGH, which generates Power On Reset when the voltage drops below 1.66 V (V_IL) for more than 50 µs and releases the reset at typically 1.75 V.
A 10 µF and a 2.2 µF are connected to VBAT_HIGH and VBAT_LOW respectively.

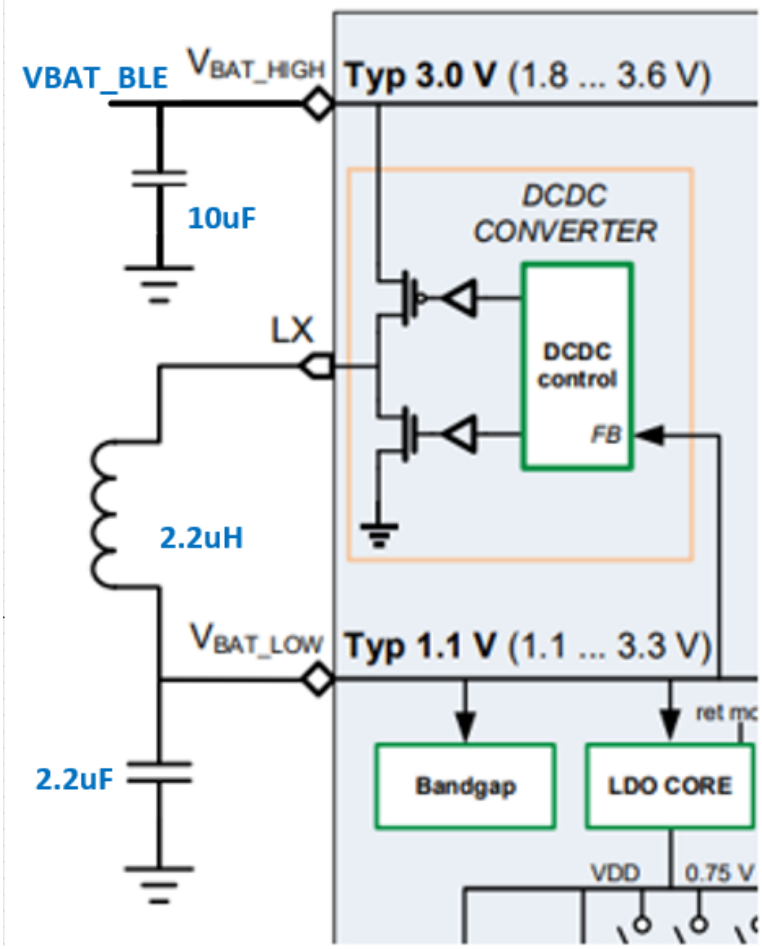

Figure 6. VBAT_BLE connection for Buck Configuration

Table 5. Suggested decoupling capacitors for the power section

Power pins	Value	Description	Part number
VBAT	10 µF	CAP. CER. ±20% 10 V X5R, 0402 (1005M)	GRM155R61A106ME11
	1 µF	CAP. CER. ±20% 10 V X5R, 0402 (1005M)	GRM153R61A105ME95D
VDD_DIO1	0.1 µF	CAP. CER. ±10% 50 V X5R, 0402 (1005M)	GRM155R61H104KE14D
	15 pF	CAP. CER. ±5% 25 V C0G, 0201 (0603M)	GJM0335C1E150JB01D
VDD_DIO2	0.1 µF	CAP. CER. ±10% 50 V X5R, 0402 (1005M)	GRM155R61H104KE14D
	15 pF	CAP. CER. ±5% 25 V C0G, 0201 (0603M)	GJM0335C1E150JB01D
VDD_FDIO	1 µF	CAP. CER. ±20% 10 V X5R 0402 (1005M)	GRM153R61A105ME95D
VDDA_DCDC_PA	2x10 µF	CAP. CER. ±20% 10 V X5R, 0402 (1005M)	GRM155R61A106ME11
VDDRF_PA	2x10 µF	CAP. CER. ±20% 10 V X5R, 0402 (1005M)	GRM155R61A106ME11
	10 pF	CAP. CER. ±5% 50 V COG, 0201 (0603M)	GRM0335C1H100JA01D
VDDA_DCDC_ANA	10 µF	CAP. CER. ±20% 10 V X5R, 0402 (1005M)	GRM155R61A106ME11
VDD_RF	10 µF	CAP. CER. ±20% 10 V X5R, 0402 (1005M)	GRM155R61A106ME11
VDDD	470 nF	CAP. CER. ±10% 25 V X5R, 0402 (1005M)	GRT155R61E474KE01D
VBAT_HIGH	10 µF	BUCK Mode. CAP. CER. ±20% 10 V X5R, 0402 (1005M)	GRM155R61A106ME11
VBAT_LOW	2.2 µF	BUCK Mode. CAP. CER. ±20% 10 V X5R, 0402 (1005M)	GRM155R61A225ME01

The ceramic capacitors must be placed as close as possible to the pins of the chip to reduce the parasitic inductance and to improve performance. Capacitors with the smallest possible package, which meets the voltage range and effective capacitance, can be used.
The selected capacitor values are higher than the required ones because of the capacitance derating phenomenon when a DC bias voltage is applied to the ceramic capacitor. For example, VDCDC_ANA requires effective capacitance of 10 µF. On the circuit, two capacitors of 10 µF are used.
The capacitance de-rating is highly dependent on the dielectric type (for example, X5R versus X7R) and the size of the multi-layer ceramic capacitor. Figure 7 shows the capacitance de-rating for two different packages, 0402 and 0603, of a 10 µF/10 V /X5R muRata ceramic capacitor. To compensate or reduce the negative effect of this DC-bias de-rating, it is advised to apply either a capacitor having a larger size (0603 instead of 0402), or a different type of capacitor.

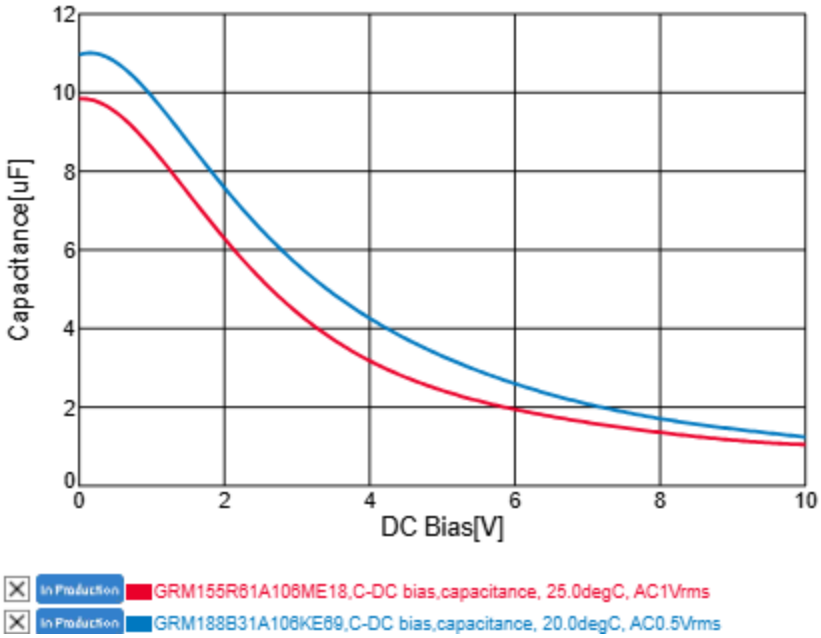

Figure 7. Effective capacitance for 10 µF, 0402 (GRM155R61A106ME11) and 0603 (GRM188B31A106KE69)

To achieve an effective capacitance value of at least 10 µF on 1.8 V, the chosen capacitance needs to be of a much higher nominal value, for example, 22 µF/6.3 V (Figure 7).
Finally, the choice of inductor impacts the DC-DC converter efficiency. Generally, larger inductors with alloy/metal composite cores, low DC resistance and high resonance frequency gives better efficiency. Shielded inductors are preferred over unshielded types.
For Wi-Fi subsystem, same inductor can be used for both DC-DC converters.

Table 6. Wi-Fi subsystem – DC-DC Inductor Examples and Characteristics

Manufacturer	Description	Value	Package	Part number
Murata	Shielded, 0.8 A, RDC 230 mΩ max	4.7 µH	2015	LQM21PN4R7MGH
SunLord	Shielded, 0.75 A, RDC 500 mΩ max	4.7 µH	2015	MPH201214S4R7MT

On Bluetooth LE subsystem, for optimal operation of the DC-DC converter, use the general criteriato select a suitable part:

- 40 MHz self resonance or higher
- 500 mΩ ESR or lower (the lower the better)
- 2.2 µH with 20% or lower tolerance.

Table 7. Bluetooth LE subsystem – DC-DC Inductors and Characteristics

Manufacturer	Description	Value	Package	Part number
Murata	Shielded, 1.7 A, RDC 140 mΩ max	2.2 µH	2015	DFE2016E-2R2M
Tayo Yuden	Shielded, 1.5 A, RDC 160 mΩ max	2.2 µH	2015	MAKK2016T2R2M

Finally, RA6W2 presents emissions on the 5 GHz band, close to the FCC radiated limits. For meeting FCC certification requirements, careful PCB design must be applied (as described in Section 5 PCB Routing Guidelines). Also add passive components on SWDIO and SWCLK lines, pins E5 and G5 respectively, as they are shows in Figure 3 and Figure 8.
The components must be placed as close as possible to the pads of theRA6W2 MCU.

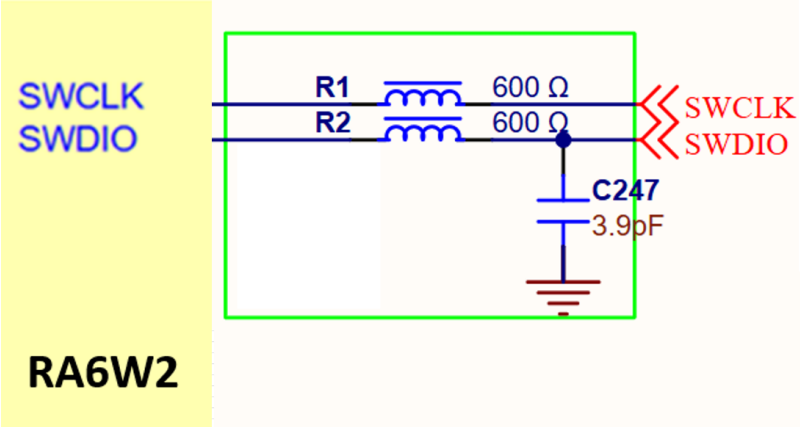

Figure 8. Components on SWDIO and SWCLK

Table 8. Suggested components for SWDIO and SWCLK

Description	Component	Part number
SWDIO Capacitor	C247	GJM1555C1H3R9CB01
SWDIO Ferrite bead	R2	BLM15AG601SN1D
SWCLK Ferrite bead	R11	BLM15AG601SN1D

4.2 Crystals and Clocks

The RA6W2 MCU is equipped with three Crystal Oscillators, two for Wi-Fi subsystem, at 40 MHz (XTAL40M) and 32.768 kHz (XTAL32K) and one for Bluetooth LE subsystem, at 32 MHz (XTAL32M). XTAL32K has no trimming capabilities and is used as the low power clock for low power sleep mode. XTAL40M and XTAL32M can be trimmed by using the internal capacitor bank.

4.2.1 40 MHz Clock

The RA6W2 needs an accurate 40 MHz clock for proper operation. The clock can be generated either by an external 40 MHz crystal or by applying an external 40 MHz clock signal.
The C_{LOAD} value (CL) of the used 40 MHz crystal preferably would be 8 pF typical. Also, crystal's ESR must not exceed 50 Ω, see Table 9.
For the specification of 40 MHz crystals, see the *Crystal Oscillator 40 MHz - Recommended Operating Conditions* section in *RA6W2 Datasheet*.

Table 9. XTAL40M recommended operating conditions

Parameter	Description	Min	Typ	Max	Unit
Frequency	Crystal oscillator frequency		40		MHz
ΔfXTAL(40M)	Crystal frequency tolerance	-20		20	ppm
ESR(40M)	Equivalent series resistance			50	Ω
CL(40M)	Load capacitance	6	8	10	pF

Table 10 lists examples of suitable 40 MHz crystals.

Table 10. 40 MHz crystal example and characteristics

40 MHz crystals	TAI-SAW	KYOCERA AVX	EPSON
Part number	TZ1269D	CX2016SA40000D0FLJG1	FA-20H 40.0000MF10Z-K0
Frequency	40 MHz	40 MHz	40 MHz
Frequency tolerance	+/-10 ppm at 25 °C	+/-10 ppm at 25 °C	+/-10 ppm at 25 °C
Temperature frequency drift	+/-15 ppm	+/-15 ppm	+/-10 ppm
Load capacitance	9 pF	8 pF	6 pF
Drive level	50 µW typical (100 µW max)	10 µW typical	10 µW typical
Temperature range	-40 °C ~ +85 °C	-30 °C ~ +85 °C	-40 °C ~ +85 °C
Size L x W x H (mm)	2.0 x 1.6 x 0.4	2.0 x 1.6 x 0.45	2.5 x 2.0 x 0.55

The 40 MHz crystal oscillator frequency is trimmed by two on-board capacitors of 4.7 pF and the settings of XTAL40M_CCTRL. XTAL40M_CCTRL is a field on register XTAL40M_CTRL_REG (0x400C0204). The valid range of values of the XTAL40M_CCTRL is 0x00 ~ 0x7F which corresponds to a range of 80 ppm. The implementation of TZ1269DA is shows in Figure 9.

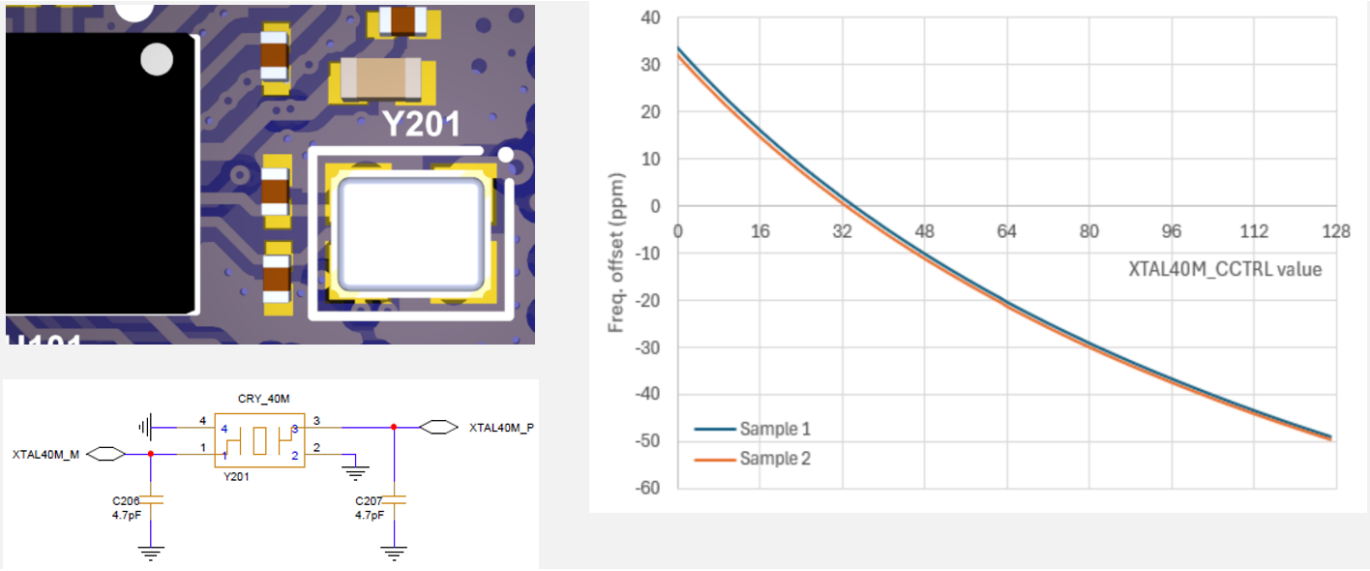

Figure 9. TZ1269DA, 40 MHz crystal implementation (left), crystal oscillator frequency range for the complete XTAL40M_CCTRL range of values

4.2.2 32.768 kHz Clock

For supporting ultra-low power Wi-Fi connected operation like DPM and TWT, an external 32.768 kHz XTAL must be connected to the RA6W2 pins P0_02 and P0_03. The better accuracy of the crystal the tighter timing is achieved. Recommended crystal specification in Table 11. Example of a 32.768 kHz crystal in Table 12.

Table 11. XTAL32K – recommended specification

Parameter	Description	Value
Frequency	Crystal frequency	32.768 kHz
Frequency tolerance	Crystal frequency tolerance	±20 ppm
ESR	Equivalent series resistance	100 kΩ
CL	Load capacitor	10 pF

Table 12. Example of suitable 32.768 kHz crystals

32.768 kHz crystals	Abracon Corp.	Epson
Part number	ABS06	FC-12M32.7680KA-A5
Frequency	32.768 kHz	32.768 kHz
Frequency tolerance	+/-20 ppm at 25 °C	+/-20 ppm at 25 °C
Load capacitance	12.5 pF	12.5 pF
ESR	90 kΩ max	90 kΩ max
Drive level	0.1 µW typ, 0.5 µW max.	0.5 µW max
Temperature range	-40 °C ~ +85 °C	-40 °C ~ +85 °C
Size L x W x H (mm)	2.0 x 1.2 x 0.6	2.0 x 1.2 x 0.6

Two shunt capacitors to GND, 15 pF each, are required for ensuring proper operation of the crystal.

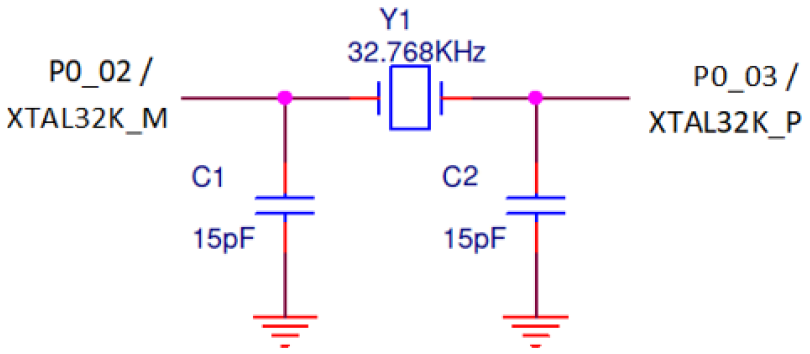

Figure 10. 32.768 kHz crystal configuration

External clock can also be connected to the RA6W2, by connecting the signal to P0_02. In this case, for utilizing the clock direct input mode, the internal XTAL circuit must be disabled by setting CLK_XTAL32K_REG register to 0x18. P0_03 can be used as GPIO.

4.2.3 32 MHz Clock

The main clock of the Bluetooth LE subsystem is 16 MHz, which is generated from a 32 MHz crystal oscillator. The crystal oscillator consists of an external 32 MHz XTAL and the internal clock oscillator. The recommended operating conditions are given in Table 13.

Table 13. XTAL32 MHz oscillator - recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fXTAL_32M	Crystal oscillator frequency			32		MHz
ΔfXTAL	Crystal frequency tolerance	After optional trimming; including aging and temperature drift. Note 1	-20		20	ppm
ΔfXTAL_UNT	Crystal frequency tolerance	Untrimmed; including aging and temperature drift. Note 2	-40		40	ppm
$ESR_{\_1pF}$	Equivalent series resistance	C_0<1pF			200	Ω
$ESR_{\_3pF}$	Equivalent series resistance	C_0<3pF			80	Ω
$ESR_{\_5pF}$	Equivalent series resistance	C_0<5pF			50	Ω
C_L	Load capacitance	No external capacitors are required	4	6	8	pF

Note 1 Using of the internal varicaps a wide range of crystals can be trimmed to the required tolerance.

Note 2 Maximum allowed frequency tolerance for compensation by the internal varicap trimming mechanism.

If the specification of the crystal meets the requirements of the Bluetooth LE oscillator, the crystal package does not affect the operation of the system. Several crystals are tested successfully. A short list can be found in Table 14.

Table 14. Successfully tested crystals

Part number	Provider	Package
XRCGB32M000F1H00R0	Murata	2.0 mm x 1.6 mm
8Q32070005	TXC	1.6 mm x 1.2 mm
TZ3484B	Taisaw	1.6 mm x 1.2 mm
TZ3375C	Taisaw	2.0 mm x 1.6 mm
8J32070002	TXC	1.2 mm x 1.0 mm

The selected crystal for the RA6W2 Evaluation board is the TZ3375C of Taisaw. The XTAL specification is presented in Table 15.

Table 15. TZ3375C specification

Parameter	Description	Min	Typ	Max	Unit
Frequency	Fo		32		MHz
Operating Temperature Range	Top	-40		85	°C
Load Capacitance	CL		6		pF
Drive Level	DL		100	200	µW
Equivalent Series Resistance	ESR			50	Ω
Frequency Tolerance	dF/Fo	-15		15	ppm
Aging	dF/F25	-2		2	ppm
Package	2.0x1.6 mm				mm × mm

4.2.3.1 32 MHz XTAL Trimming

The 32 MHz (XTAL32M) crystal oscillator has trimming capability. The frequency is trimmed by two on-chip variable capacitor banks, see Figure 11. Both capacitor banks are controlled by the same 8-bit register, CLK_FREQ_TRIM_REG.

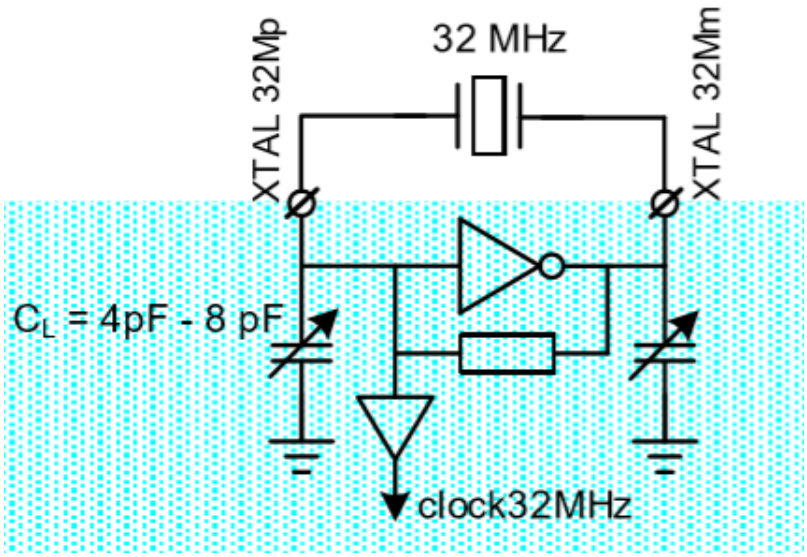

Figure 11. Circuit of 32 MHz crystal oscillator

With CLK_FREQ_TRIM_REG[XTAL32M_TRIM] = 0x00, the minimum capacitance and thus the maximum frequency is selected.

With CLK_FREQ_TRIM_REG[XTAL32M_TRIM] = 0xFF, the maximum capacitance and thus the minimum frequency is selected.

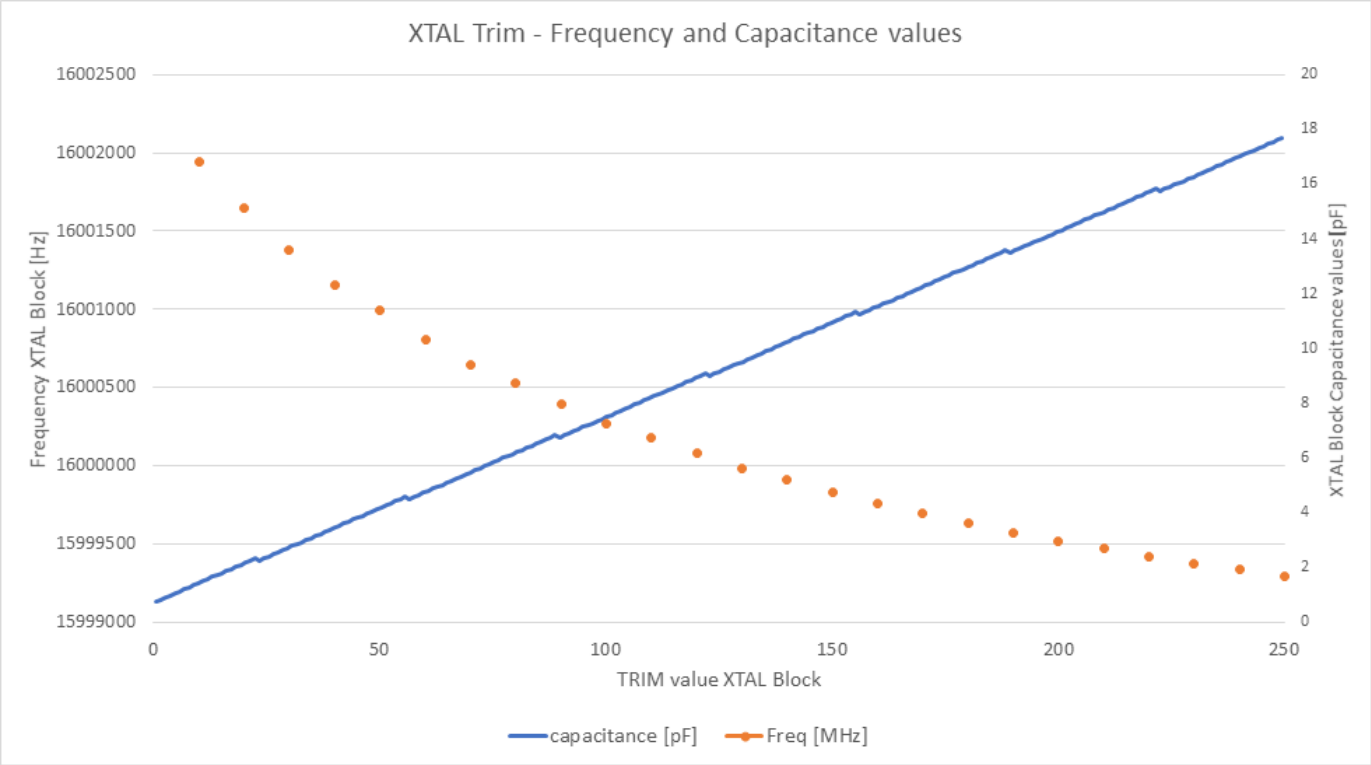

Figure 12. 32 MHz XTAL oscillator capacitance value versus frequency

The advice is to trim the crystal (XTAL) to achieve optimal RF performance and power consumption.
Not trimming the crystal might lead to out of spec RF, when taking frequency drift into account due to temperature and aging.

4.3 GPIOs

RA6W2 provides 28 GPIOs for Wi-Fi subsection and 5 GPIOs for Bluetooth LE. The functions assigned to the GPIO pins are fully configurable and are controlled by the Programmable Pin Assignment (PPA). PPA provides a multiplexing function for the I/O pins of the on-chip peripherals. Any of the peripheral input or output signals can be freely mapped to any available GPIO port, except ADC, QSPI, SDIO, eMMC, and SWD which have fixed assignment. Information for the peripherals can be found in the RA6W2 Datasheet.
When a pin is configured to function as a GPIO, it has the following configurable features:

- Direction (input/output)
- Push pull/Open drain
- Pull-up/Pull-down
- Selectable 25 kΩ pull-up/pull-down resistors per pin up to selected voltage rail
- Drive strength (2 mA, 4 mA, 8 mA, 14 mA), default drive strength for each GPIO is 8 mA
- Slew rate (Fast/Slow)
- Input selection (CMOS/Schmitt Trigger).
- Pin state is maintained when the system enters low-power sleep 4 and 5 modes.

After a power on reset (POR), the default state of the pins of RA6W2, is shown in Table 16.
Other characteristics of GPIOs are:

- Wi-Fi subsystem:
  - RST_n and P0_00 to P0_03 are referred to VBAT.
  - P1_00 to P1_09 are referred to VDD_FDIO, which is by default equal to 1.8 V.
  - Quad SPI Controller is assigned only to P0_08 to P0_13.
  - There is only one SDIO interface which can be assigned to either P0_08 to P0_13 or P1_10 to P1_15.
  - Not all pins can be used for waking up the MCU. The wake-up signals are digital signals, and they are activated by logic state change. On the other hand, analog wake-up signals are activated when a programmable voltage level is crossed.

- ADCs can be assigned only to P0_04 to P0_07.
- P0_00 and P0_01 are assigned to Booting UART.
- P0_16 and P0_17 are assigned to SWD.
- P_02 and P0_03 can be either XTAL32KHz or GPIO pins.

- Bluetooth LE subsystem:
  - Default drive strength for each GPIO is 3.5 mA.
  - PB0_x (Bluetooth LE subsystem) high level is equal to VBAT_BLE.
  - During booting from UART, PB0_0 is assigned to UTX.
  - Between booting steps and after booting, PB0_0 is assigned to Reset pin.
  - Reset is an active high pin.
  - In case that GPIOs of Bluetooth LE and Wi-Fi subsections are connected together, it is critical to apply same voltage range on the GPIOs of both subsystems. This eliminates the possibility of current leakage.

Table 16. Pin configuration

Pin	Support wake-up	Power domain	Alternate function 0	Alternate function 1	Alternate function 2	POR default
PB0_0		VBAT_BLE	UTX (Bluetooth LE)			RST
PB0_1		VBAT_BLE	URX (Bluetooth LE)			
PB0_2		VBAT_BLE	SWCLK			SWCLK
PB0_3		VBAT_BLE				
PB0_4		VBAT_BLE				
PB0_5		VBAT_BLE	SWDIO	RxTx		SWDIO
RST_N		VBAT	RST_N			RST_N
P0_00	yes	VBAT	RTC_WAKE_UP			GPIO
P0_01		VBAT	sen_out			sen_out
P0_02		VBAT	xtal32k_m			xtal32k_m
P0_03		VBAT	xtal32k_p			xtal32k_p
P0_04	ana wake	VDDIO_DIO1	ADC0		eMMC_DIO4	GPIO
P0_05	ana wake	VDDIO_DIO1	ADC1		eMMC_DIO5	GPIO
P0_06	ana wake	VDDIO_DIO1	ADC2		eMMC_DIO6	GPIO
P0_07	ana wake	VDDIO_DIO1	ADC3	MCLK	eMMC_DIO7	GPIO
P0_08	yes	VDDIO_DIO1	QSPIR_CLK	SDIO0_CLK	eMMC_CLK	GPIO
P0_09	yes	VDDIO_DIO1	QSPIR_CS	SDIO0_CMD	eMMC_CMD	GPIO
P0_10	yes	VDDIO_DIO1	QSPIR_D0	SDIO0_D0	eMMC_DIO0	GPIO
P0_11	yes	VDDIO_DIO1	QSPIR_D1	SDIO0_D1	eMMC_DIO1	GPIO
P0_12	yes	VDDIO_DIO1	QSPIR_D2	SDIO0_D2	eMMC_DIO2	GPIO
P0_13	yes	VDDIO_DIO1	QSPIR_D3	SDIO0_D3	eMMC_DIO3	GPIO
P1_00		VDD_FDIO	OQSPI_D4	eMMC_DIO4		GPIO
P1_01		VDD_FDIO	OQSPI_D5	eMMC_DIO5		GPIO
P1_02		VDD_FDIO	OQSPI_D6	eMMC_DIO6		GPIO
P1_03		VDD_FDIO	OQSPI_D7	eMMC_DIO7		GPIO
P1_04		VDD_FDIO	OQSPI_D0			
P1_05		VDD_FDIO	OQSPI_D1			
P1_06		VDD_FDIO	OQSPI_D2			
P1_07		VDD_FDIO	OQSPI_D3			
P1_08		VDD_FDIO	OQSPI_CLK			
P1_09		VDD_FDIO	OQSPI_CS			

Pin	Support wake-up	Power domain	Alternate function 0	Alternate function 1	Alternate function 2	POR default
P1_10	yes	VDDIO_DIO2	eMMC_CMD	SDIO1_CMD		GPIO
P1_11	yes	VDDIO_DIO2	eMMC_CLK	SDIO1_CLK		GPIO
P1_12	yes	VDDIO_DIO2	eMMC_DIO0	SDIO1_D0		GPIO
P1_13	yes	VDDIO_DIO2	eMMC_DIO1	SDIO1_D1		GPIO
P1_14		VDDIO_DIO2	eMMC_DIO2	SDIO1_D2		GPIO
P1_15		VDDIO_DIO2	eMMC_DIO3	SDIO1_D3		GPIO
P1_16		VDDIO_DIO2	SWCLK			SWCLK
P1_17		VDDIO_DIO2	SWDIO			SWDIO

4.4 Reset Pins

4.4.1 RST_n for Wi-F Subsystem

The RA6W2 has an active-low reset pin (RST_N pad) dedicated to Wi-Fi subsystem and it is referred to as VBAT power domain. There is no pull-up internally to RA6W2 MCU. An external pull-up resistor from 10 kΩ to 30 kΩ must be added.

4.4.2 Reset of Bluetooth LE Subsystem

During power on and before booting, the reset pin is active high, and it is assigned on PB0_0. This is the hardware reset. After boot, reset pin assignment and operation is handled by software.
At boot, PB0_0 is also assigned as output to UART and SPI for the time required from each booting step. At the end of each boot step, PB0_0 is assigned again to Reset.

Table 17. PB0_0 assignment during boot

Pin	Booting sequence	State	Comments
PB0_0	Before boot	RST	Input with pull-down.
	During boot	MISO, (Boot Step 1) UTX, (Boot Step 4) MOSI. (Boot Step 5) RST	P0_0 is handled from Booting sequence. At the end of each step, and before next booting step, P0_0 is assigned to Reset.
	After boot	GPIO	Handled by the software.

The RST functionality on PB0_0 can be disabled by setting the HWR_CTRL_REG[DISABLE_HWR] bit.

4.5 UART

The UART interface of Wi-Fi subsystem provides an industry compliant serial interface for communicating with other devices. Three independently configurable UARTs are available which support the RS-232 and RS-485 protocols. There are two different UART configurations possible:

- 2-wire UART (URX and UTX)
- 4-wire UART (URX, UTX, RTS, and CTS).

The UART pins can be assigned to any of the unused GPIO pins through the Programmable Pin Assignment (PPA) function. The assignment can be done by setting the proper field on the mode register of the correspondent GPIO, example for P0_00 is shown in Figure 15.

Table 244: P0_00_MODE_REG (0x400B0024)

Bit	Mode	Symbol/Description	Reset
6:0	R/W	PID 0: GPIO (I/O) 1: UART_RX (IA) 2: UART_TX (OA) 3: UART_CTSN (IA) 4: UART_RTSN (OA) 5: UART_TXDOE (OA) 6: UART1_RX (IA) 7: UART1_TX (OA) 8: UART1_CTSN (IA) 9: UART1_RTSN (OA) 10: UART1_TXDOE (OA) 11: UART2_RX (IA) 12: UART2_TX (OA) 13: UART2_CTSN (IA) 14: UART2_RTSN (OA) 15: UART2_TXDOE (OA)	0x0

Figure 13. PID field on P0_00_Mode register for enabling UART pins

During booting GPIOs P0_00 and P0_01 are assigned as URX and UTX respectively, providing the capability to download a software image. The baud rate during boot is 115.2 kbits/s.

4.6 SWD(JTAG)

A standard Serial Wire Debug (SWD) allows debugging of user applications during the development phase of a product. When development is complete, and the device is set to secure mode and the SWD interface is disabled to protect the device from being tampered with.
For the Wi-Fi subsystem of RA6W2, SWD consists of two pins: P1_16 (SWCLK) and P1_17 (SWDIO).
For Bluetooth LE subsystem, PB0_2 (SWCLK) and PB0_5 (SWDIO) are used for SWD bus.

4.7 Octa/Quad SPI Flash

There is an Octa/Quad SPI Controller (OQSPIC) on Wi-Fi subsystem, which provides a low pin count interface to standard Serial Peripheral Interface (SPI) and a high-performance Dual/Quad/Octa SPI Interface. Purpose of this interface is to connect XiP Flash memory, from where the software of the system runs.
The Quad SPI Controller supports the following SPI modes:

- Single: data transfer through two unidirectional pins.
- Dual: data transfer through two bidirectional pins.
- Quad: data transfer through four bidirectional pins.
- Octa: data transfer using eight bidirectional pins.

Table 18 shows the pin configurations for the OQSPI interface.

Table 18. OQSPI pin configuration

Function	GPIO	Description	Ball No
OQSPI_CLK	P1_08	Output serial clock	E11
OQSPI_CS	P1_09	Active Low output Chip select	F6
OQSPI_D0	P1_04	MOSI (output) in single SPI mode D0 (bidirectional) in Quad/Octa SPI mode	H10
OQSPI_D1	P1_05	MISO (input) in single SPI mode D1 (bidirectional) in Quad/Octa SPI mode	G9
OQSPI_D2	P1_06	WPn Write Protect output in single SPI mode D2 (bidirectional) in Quad/Octa SPI mode	G11
OQSPI_D3	P1_07	HOLDn/Resetn output in Single SPI mode D3 (bidirectional) at Quad/Octa SPI mode	F10
OQSPI_D4	P1_00	D4 (bidirectional) at Octa SPI mode	H8
OQSPI_D5	P1_01	D5 (bidirectional) at Octa SPI mode	G7
OQSPI_D6	P1_02	D6 (bidirectional) at Octa SPI mode	F8
OQSPI_D7	P1_03	D7(bidirectional) at Octa SPI mode	J7

The maximum operating frequency of the QSPI interface in the RA6W2 is 80 MHz. Table 19 shows successfully tested and supported flashes.

Table 19. Examples of suitable QSPI flash

Part number	Capacity	Provider
AT25SL0641C	64 Mbit	Renesas Electronics

To avoid signal integrity issues, keep the distance between the processor and the QSPI Flash memory as short as possible, try to have the length of the traces as equal as possible, and route with enough spacing to avoid crosstalk. The QSPI device must be supplied by the VDD_FDIO rail. VDD_FDIO by default is 1.8 V.

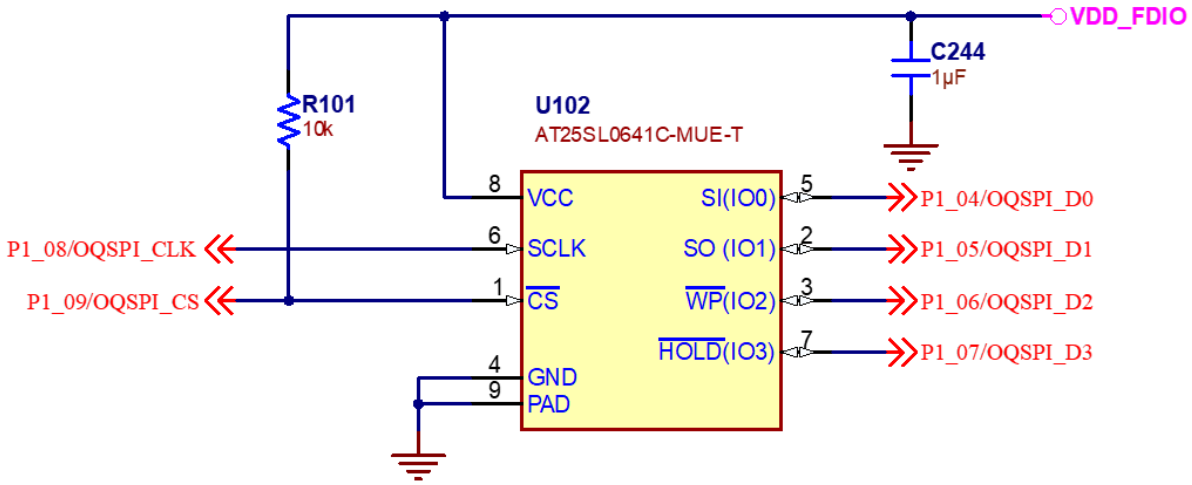

Figure 14. QSPI Flash memory used in RA6W2 daughterboard

4.8 SPI Functions

In RA6W2, Wi-Fi subsystem provides two SPI interfaces (SPI/SPI2), with master and slave capability for connection to SPI devices in master mode or being connected to a host MCU in slave mode. They have separate RX/TX FIFOs (32 bytes) and support SPI clock rates up to 48 MHz for 3.3 V, and 40 MHz for 1.8 V.

The SPI interface supports all four modes of operation and the corresponding polarity (CPOL) and phase (CPHA) of the SPI clock (SPI_CLK).

All available GPIOs can be used as SPI signals, by setting the proper PID field on the correspondent GPIO mode register, example for P0_00 is shown in Figure 15.

Table 244: P0_00_MODE_REG (0x400B0024)

Bit	Mode	Symbol/Description	Reset
6:0	R/W	PID 16: SPI_DI (IA) 17: SPI_DO (OA) 18: SPI_CLK (I/O) 19: SPI_CSN0 (I/O) 20: SPI_CSN1 (OA) 21: SPI2_DI (IA) 22: SPI2_DO (OA) 23: SPI2_CLK (I/O) 24: SPI2_CSN0 (I/O) 25: SPI2_CSN1 (OA)	0x0

Figure 15. PID field on P0_00_Mode register for enabling SPI signals

For operating SPI bus in high frequency and ensuring signal integrity, you should have a provision for termination in-series resistors. Resistors can be from 10 to 33 Ω and they must be placed close to transmission port.

4.9 Interface of QSPI Controller

RA6W2 MCU provides an additional QSPI Controller (QSPIC). QSPIC can interface with an external non secure Flash or PSRAM with capability of up to 64 MB. The QSPIC supports the standard SPI and a high-performance Dual/Quad SPI Interface, in Master only mode.
QSPIC interface is assigned on specific pins of RA6W2, Table 20.

Table 20. Pin assignment of QSPIC interface

Pin name	Pin assignment	SPI	QSPI
QSPI_CLK	P0_08	Output serial clock	Output serial clock
QSPI_CS	P0_09	Active low output Chip select	Active low output Chip select
QSPI_D0	P0_10	MOSI (output)	D0 (bidirectional)
QSPI _D1	P0_11	MISO (input)	D1 (bidirectional)
QSPI _D2	P0_12	WPn Write Protect output	D2 (bidirectional)
QSPI _D3	P0_13	HOLDn/Resetn output	D3 (bidirectional)

As the voltage range of the interface is defined by VDD_DIO1, memory must be supplied from same rail or another rail with equal voltage.
For avoiding signal integrity issues, keep distance between RA6W2 MCU and memory short to avoid stubs and cross talk between the traces. There should be a provision for termination in-series resistors. Resistors values can be from 10 to 33 Ω. Example of PSRAM connectivity is shown in Figure 16.

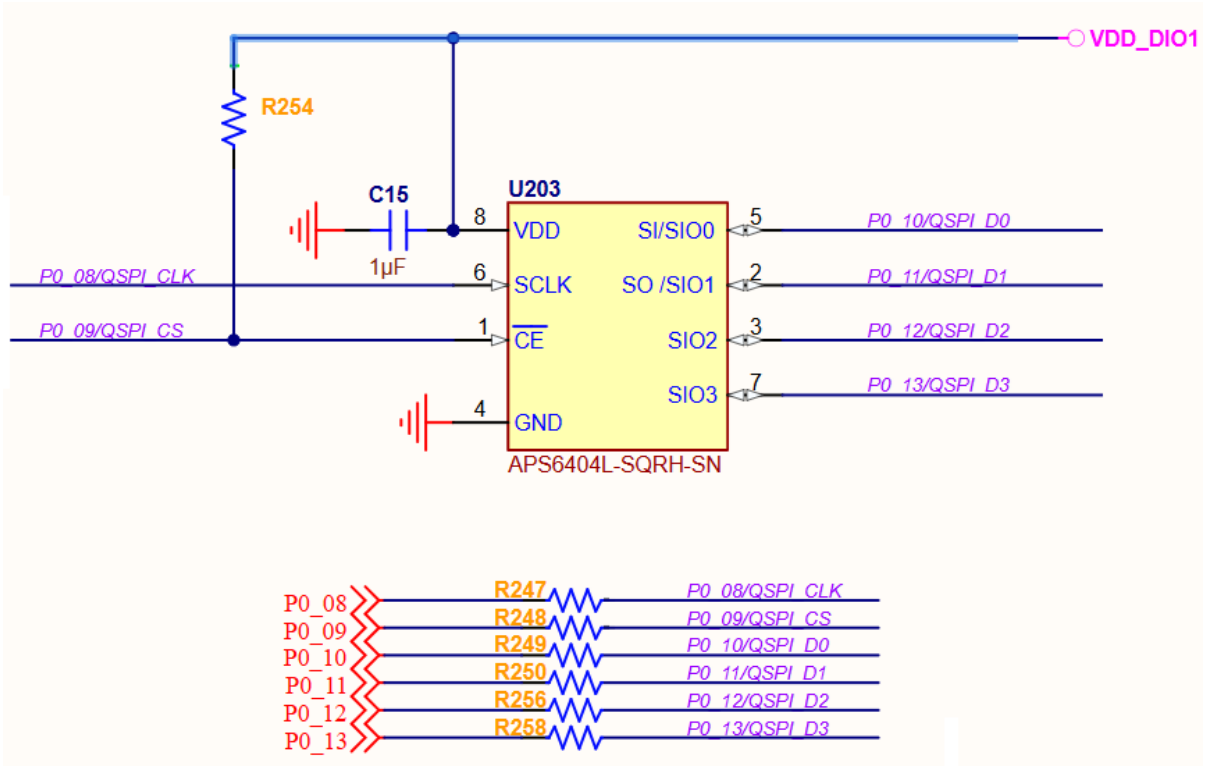

Figure 16. QSPIC interface connectivity to PSRAM

4.10 SDIO Function

RA6W2 supports an SDIO 3.0 card interface suitable for memory card and I/O card applications with low-power consumption. The SDIO interface supports SPI, 1-bit SD, and 4-bit SD transfer modes at the full clock range of 0 to 80 MHz.

The SDIO interface requires pull-up resistors to be connected between the signal lines and the supply to enable communication. Pull-up resistor values may vary based on the board layout. Do not apply a pull-up on SDIO_CLK.

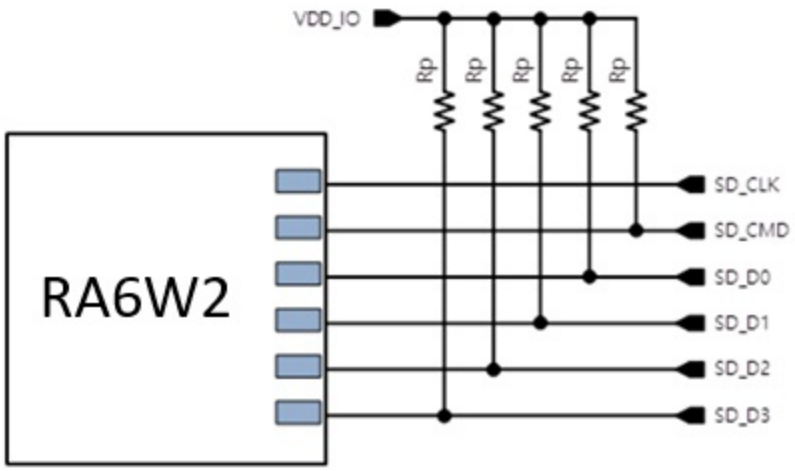

Figure 17. SDIO pull-up resistor

Table 21. SDIO pin configuration

Pin name	Pin assignment (Alt 1/Alt 2)	I/O	Description
SDIO_CMD	P1_10/P0_08	I/O	Command line
SDIO_CLK	P1_11/P0_09	I	Input serial clock
SDIO_D0	P1_12/P0_10	I/O	Bi-directional data line
SDIO_D1	P1_13/P0_11	I/O	Bi-directional data line
SDIO_D2	P1_14/P0_12	I/O	Bi-directional data line
SDIO_D3	P1_15/P0_13	I/O	Bi-directional data line

4.11 RF Section

There are three RF ports, one for 2.4 GHz band and one for 5 GHz band, both for Wi-Fi subsystem and one 2.4 GHz band for Bluetooth LE subsystem.
Wi-Fi subsystem, 2.4 GHz port, consists of two pins, RFTX_2G and RFRX_2G which are combined through an LC circuit, where L=3.9 nH and C=1 pF, both 0201. LC circuit must be placed close to the chip. Figure 18 shows the RF output circuitry with an external diplexer to combine the 2.4 GHz and 5 GHz transmit/receive paths and a band pass filter (BPF) to ensure the rejection of out-of-band emissions on 5 GHz.

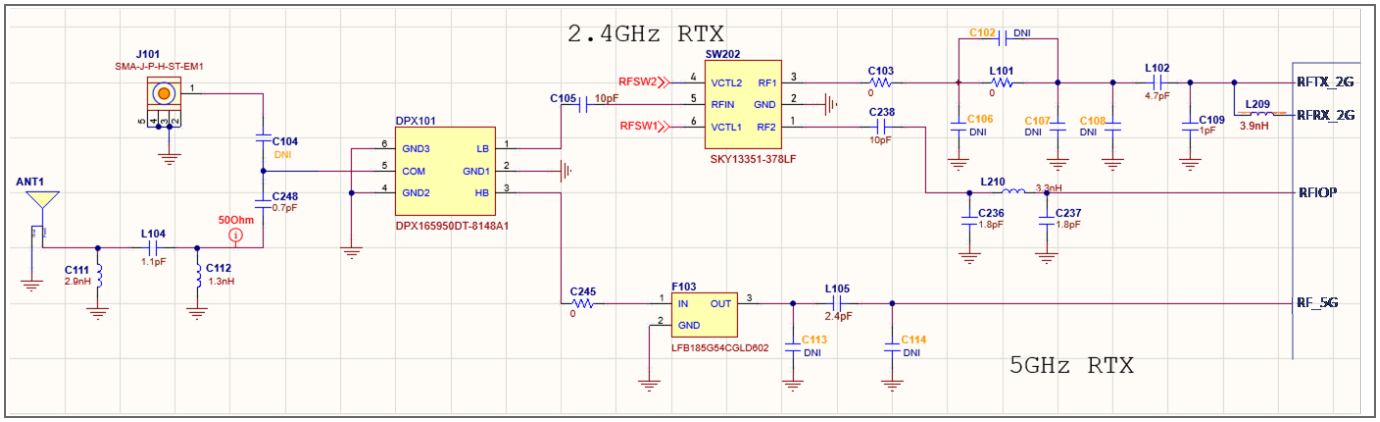

Figure 18. RFIO port and RF circuitry as applied on RA6W2 evaluation board

Table 22. Recommended RF front-end components

Part number	Component	Provider
LFB185G54CGLD602	Band pass filter	Murata Electronics
DPX165950DT-8060C1	Diplexer	TDK
SKY13351-378LF	2.4 GHz RF Switch	Skyworks

The RF section of Bluetooth LE subsection consists of a discrete Low pass filter in pi-configuration, 3.3 nH and two 1.8 pF capacitors, 0201. Bluetooth LE RF section is connected to 2.4 GHz Wi-Fi subsystem 2.4 GHz RF section through RF switch, SKY13351-378LF.
SKY13351-378LF is RF switch with two control pins, RFSW1 and RFSW2. GPIOs P0_07 and P0_06 from Wi-Fi subsystem are connected to RFSW1 and RFSW2 and they are used for controlling which radio is connected to the antenna.

Table 23. SKY13351 RF SPDT truth table

P0_06 (connected to RFSW1)	P0_07 (connected to RFSW2)	2.4 GHz RF band connected to antenna
Low	High	Wi-Fi
High	Low	Bluetooth LE

4.12 ESD Protection

If a GPIO or an antenna can be touched by users, provide an ESD protection device for them. For the RF input an ultra-low capacitance device must be used.
The ESD protected signal lines should be routed directly to the transient-voltage-suppression diode. Ground connections should be made directly to the ground plane to minimize parasitic inductance.
For connectors, the transient-voltage-suppression devices should be placed as close to the connector as possible to reduce transient coupling into nearby traces.
The secondary effects of radiated emissions can cause upset to other areas of the board, even if there is no direct path to the connector.
Apply Uni-Directional ESD protection devices on signals having only positive polarity. Such devices have a lower forward bias voltage to clamp negative ESD voltages.

5. PCB Routing Guidelines

Figure 19 shows the PCB layout applied on the RA6W2 evaluation board. Main target of Evaluation board was the performance, the noise minimization, and the improvement of EMI. In addition, due to the package, the number of pins (VFBGA-93) and the pitch, the use of microvias is necessary. Consequently, an 8-layer PCB with microvias on pad, buried vias, and careful routing was applied. PCB stack-up and PCB routing strategy per layer are described further in the document. The PCB layout is based on the schematic shows in Appendix A RA6W2 Application Circuit.

	Top Overlay		Overlay		
	Top Solder	Solder Resist	Solder Mask		0.01016mm
1	TOP		Signal	1/3oz	0.012mm
	Dielectric 1	FR-4	Prepreg		0.063mm
2	L2		Signal	1/3oz	0.012mm
	Dielectric2	FR-4	Prepreg		0.064mm
3	L3		Signal	1/3oz	0.012mm
	Dielectric 3	FR-4	Prepreg		0.063mm
4	L4		Signal	1/3oz	0.012mm
	Dielectric4	Core-043	Core		1.1mm
5	L5		Signal	1/3oz	0.012mm
	Dielectric 2	FR-4	Prepreg		0.063mm
6	L6		Signal	1/3oz	0.012mm
	Dielectric 4	FR-4	Prepreg		0.064mm
7	L7		Signal	1/3oz	0.012mm
	Dielectric 5	FR-4	Prepreg		0.063mm
8	Bottom Layer		Signal	1/3oz	0.012mm
	Board Layer Sta...	Solder Resist	Solder Mask		0.01016mm
	Board Layer Sta...		Overlay		

Figure 19. RA6W2 evaluation board PCB stack-up

- L1 Top layer is used for component placement and routing the pins located on the periphery of the chip. Components placement must follow the guidelines for power, crystal, and RF sections. Routing of the RF traces are applied on this layer. Digital signals are routed into internal layers.

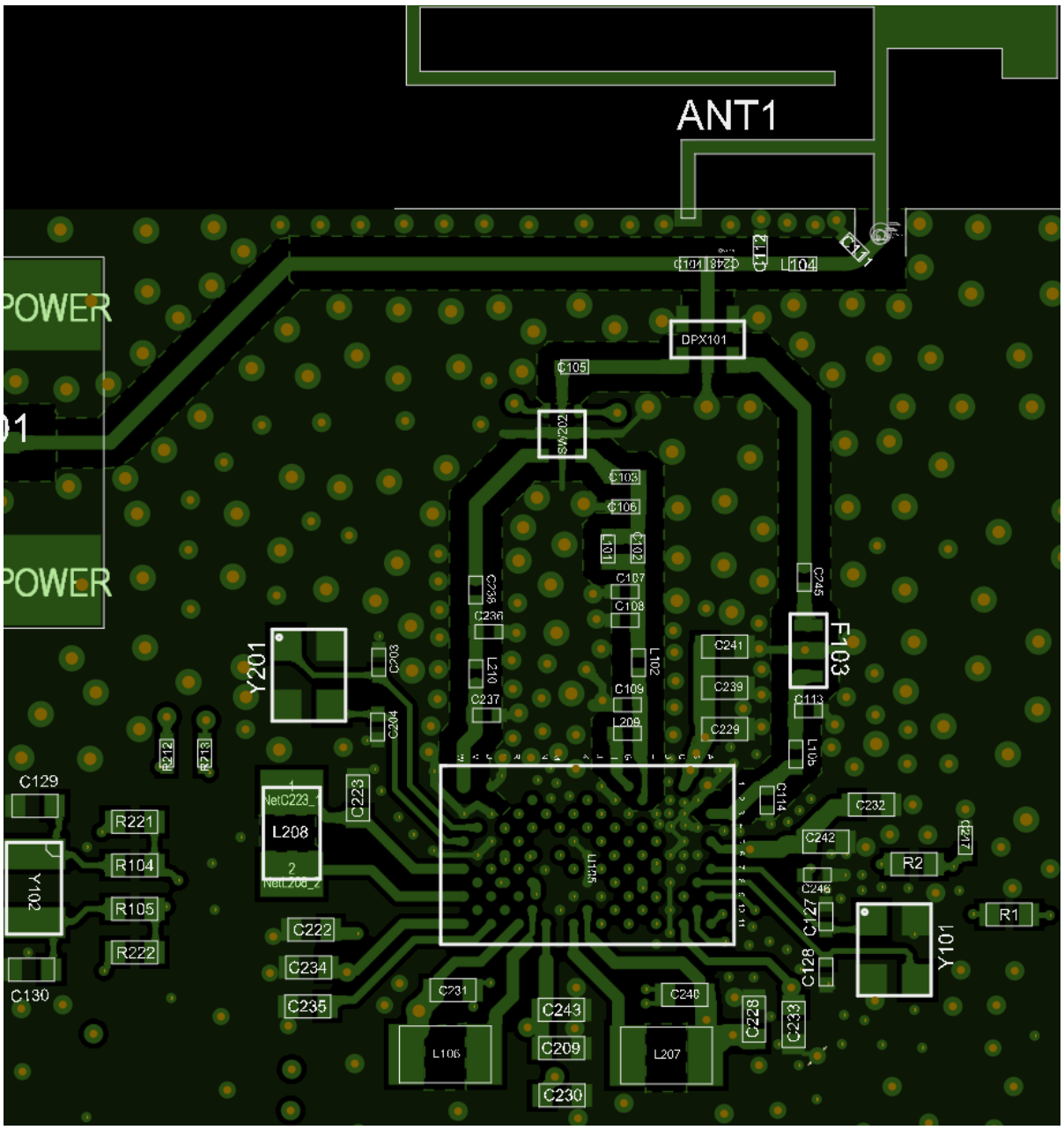

Figure 20. L1 Top layer, RA6W2 – VFBGA93

- L2 internal layer, is considered the reference GND plane for the RF of the chip. It is free of traces under the Chip and RF front-end area. This is important so there are no GND islands, which increase the distance of the grounding current. This is the layer where the RF traces impedance is referred to. GND Vias from the chip are connected to this layer. For achieving impedance equal to 50 Ω, the GND under RF traces has been removed.

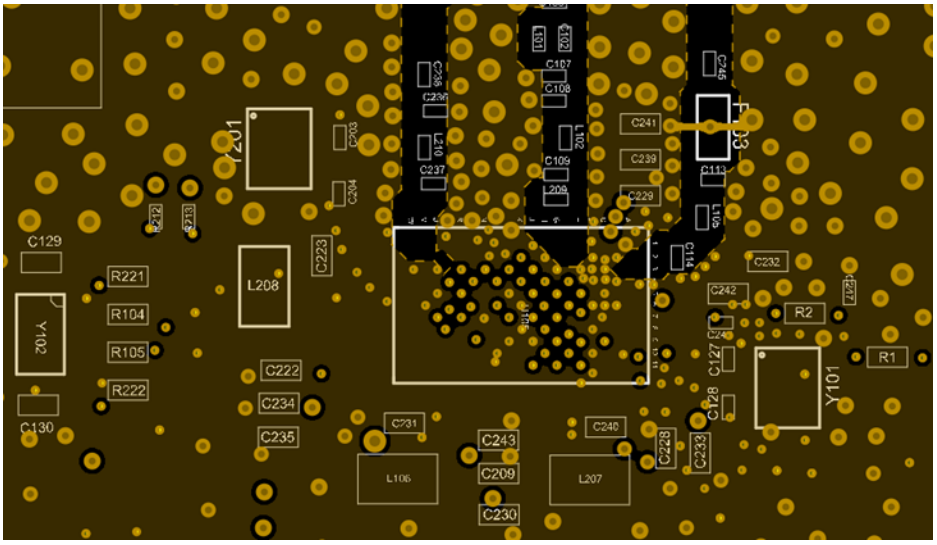

Figure 21. L2 internal layer is solid GND

- L3 and L5 internal layers are used for routing digital signals. Note that for L3, under the RF traces, solid ground is applied. Based on distance between this GND and the RF traces, the impedance is calculated.

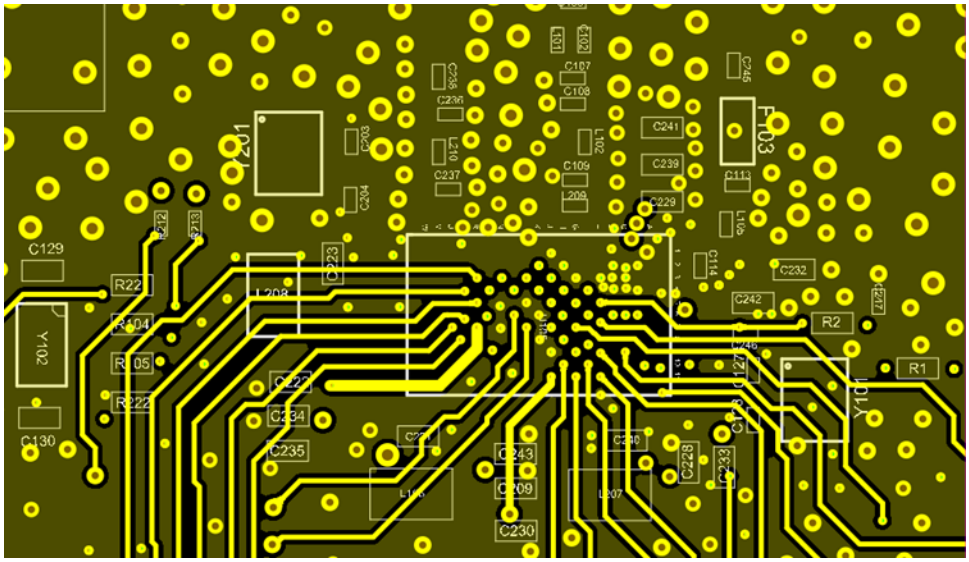

Figure 22. L3 internal layer, digital signals routed

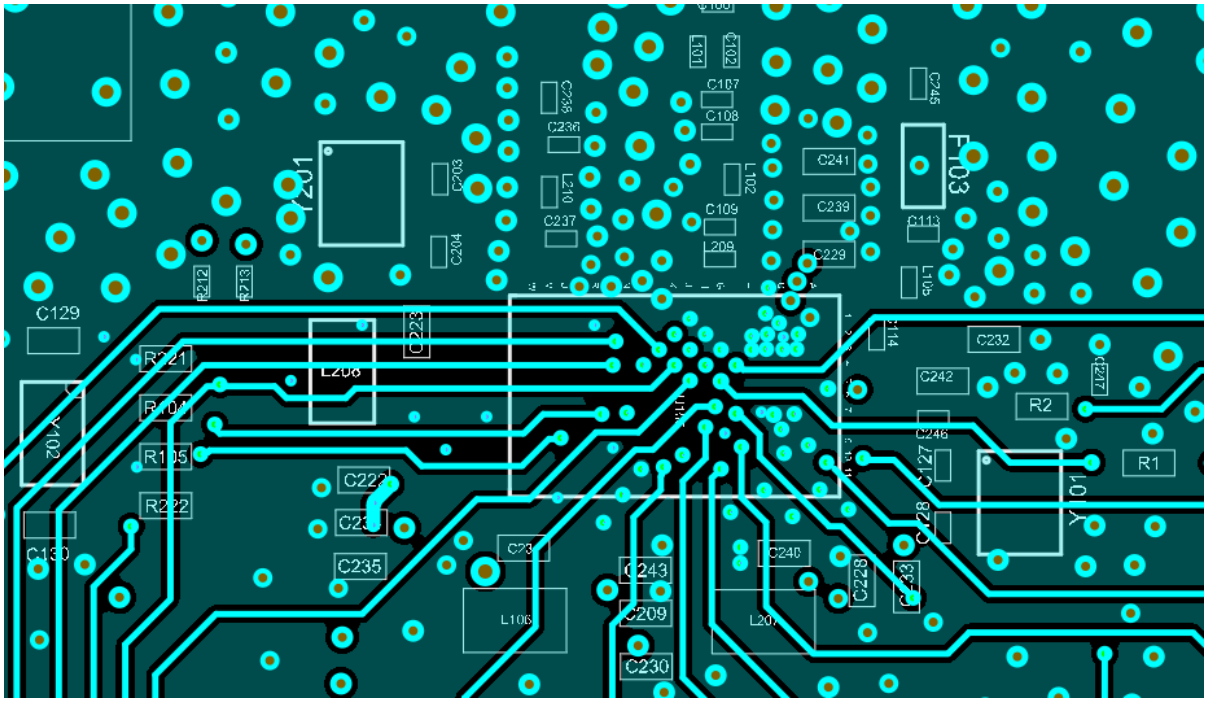

Figure 23. L5 internal Layer, digital signals routed

- Layer L7 is used for routing mainly the power supplies traces. Note the traces for supplying the RF section (yellow color). They are as short as possible and wide (0.8 mm for VDD_RF_PA and 0.5 mm for VDD_RF).

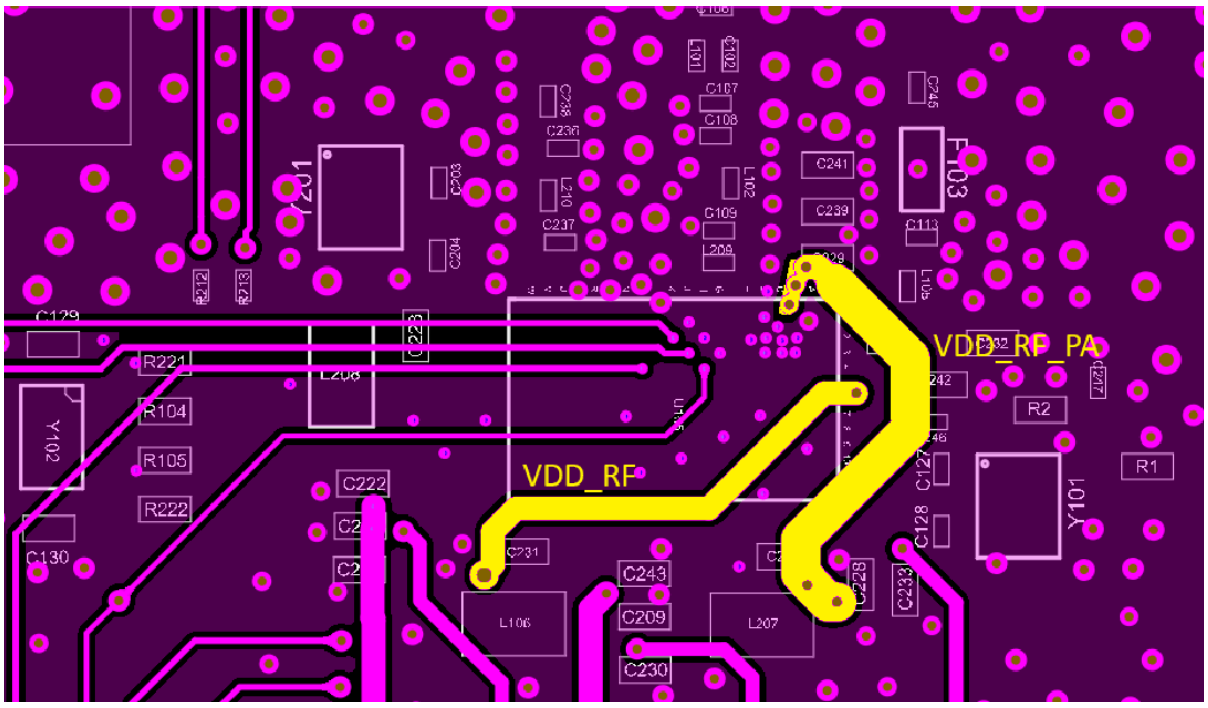

Figure 24. L7 internal layer is used for routing the power traces of RA6W2

- Finally, L4, L6, and Bottom Layers are assigned to GND, providing by this way an EMI shield to RF and signal layers.

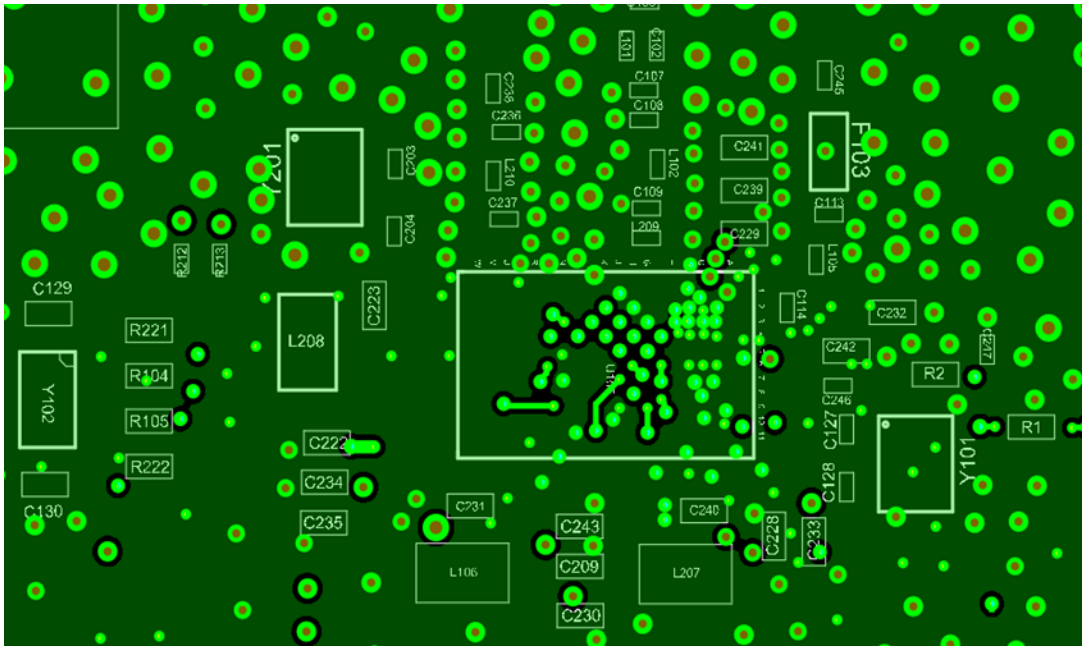

Figure 25. Layer L4 is solid GND

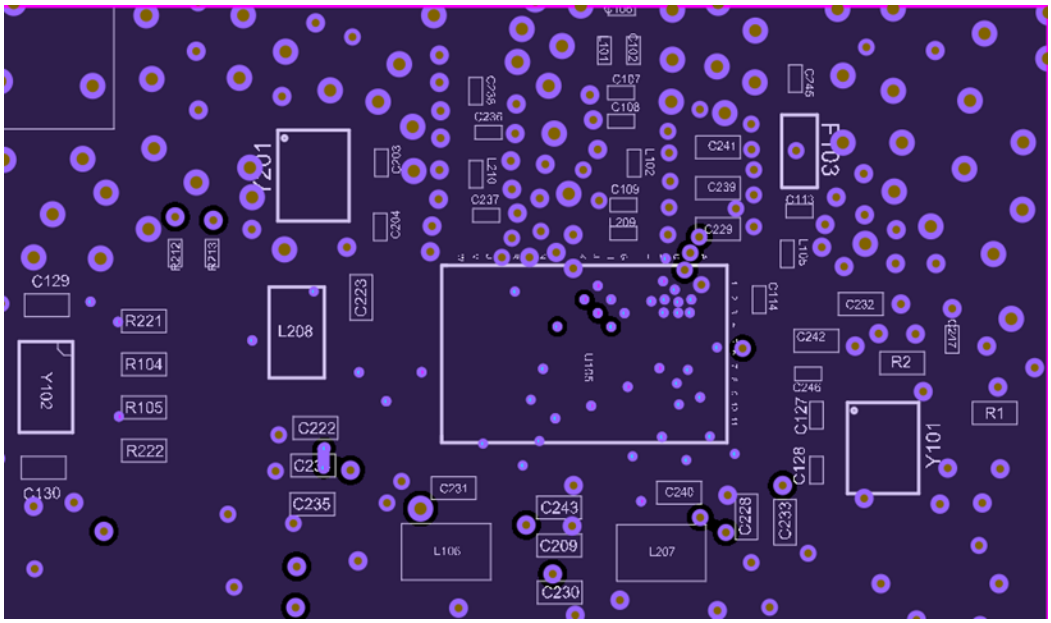

Figure 26. Layer L6 is solid GND

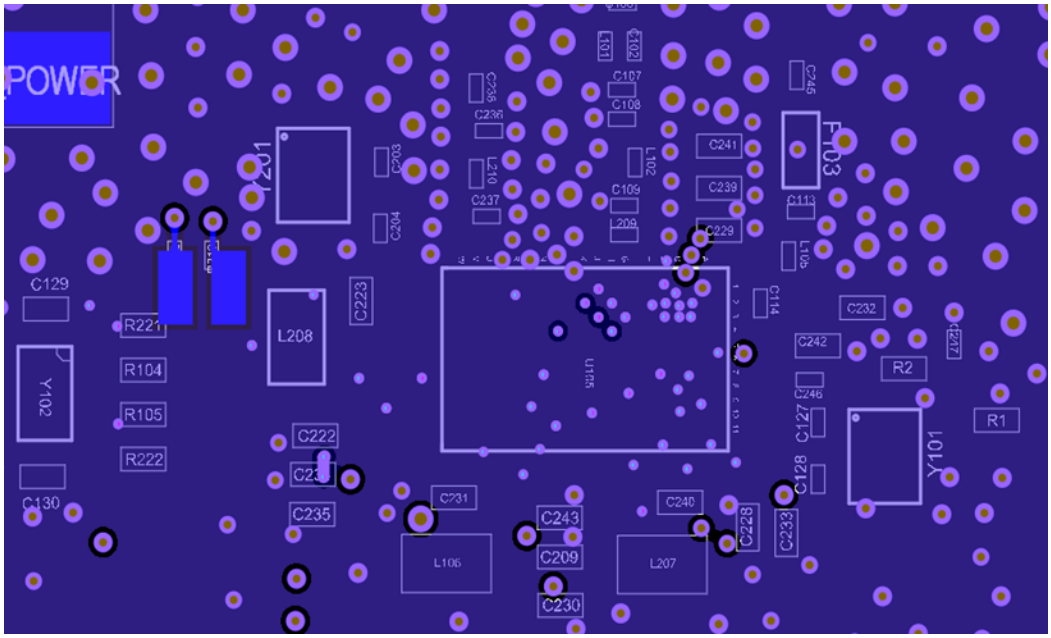

Figure 27. Bottom layer is solid GND

GND vias are placed on the periphery of placement area, for producing a shield for reducing EMI.
Active components operating at high frequency should have a layout as compact as possible to prevent the cross-coupling between lines and to minimize the parasitic effects which have negative impacts on the operating parameters. Use as many vias as possible to create a solid GND under the IC itself and connect the IC to the inner GND layer. It is beneficial to system performance to provide more than one via from GND pins to the reference GND plane.

5.1 PCB Layout for Power Section

The PCB layout guidelines for power supply:

- Place DC-DC converters capacitors close to the chip with their GND pads oriented to chip. By this way, the noisy signals current loops are reduced, resulting to better performance.
- Put the power inductor as close as possible to the chip. Remove grounding under the inductor to minimize any possible coupling from reference ground.

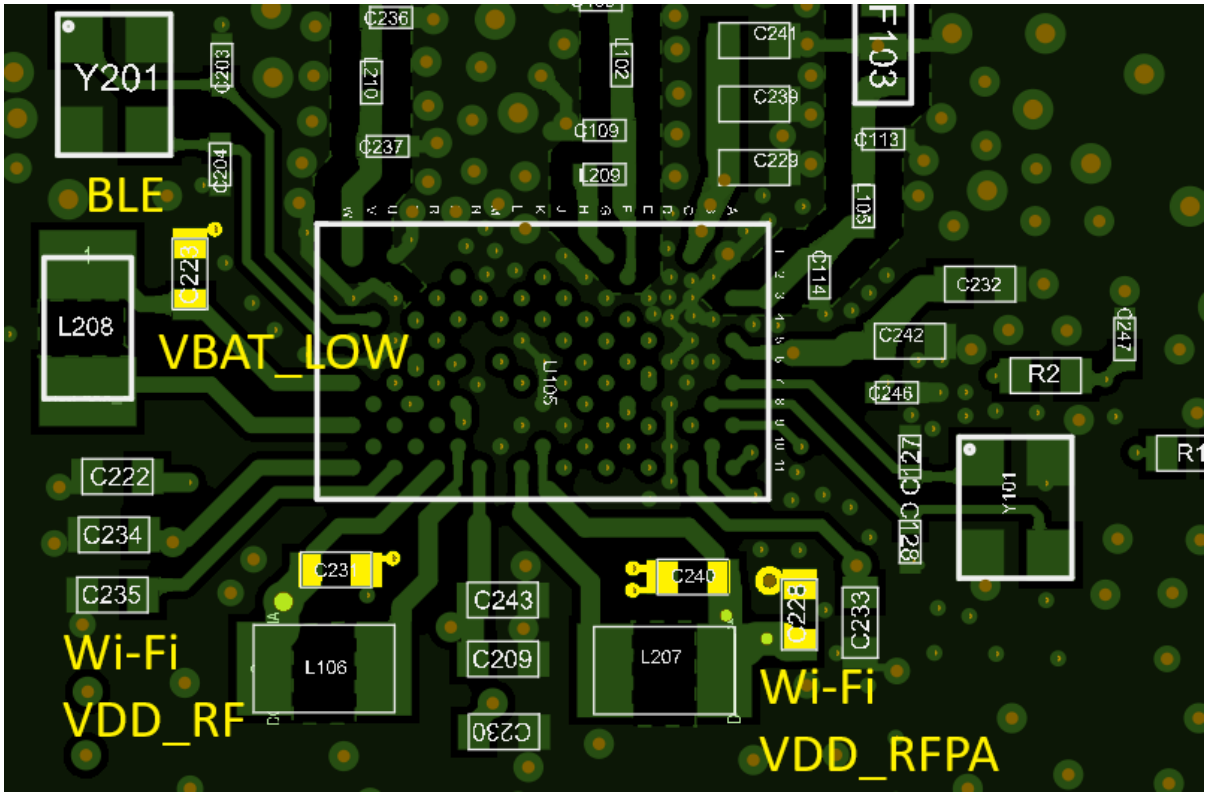

Figure 28. DC-DC capacitors placement

- Capacitors for Wi-Fi, VDD_RFPA, and VDD_RF, as well as VBAT_LOW for Bluetooth LE subsystem, must be placed as close as possible to the pins.
- Use more than one via on both sides of the power traces. Especially for VDD_RFPA, more than two vias is good practice, because the current for RF PA is of the order of several hundreds of milliamperes.
- Use widest and shortest possible traces for connecting DC-DC outputs with VDD_RFPA and VDD_RF. For VDD_RFPA, a 500 µm or internal layers and 400 µm wide traces is suggested. For VDD_RF a 400 µm or internal layers and 300 µm wide traces are suggested . Note that internal layers, most of the times use thinner copper than external copper layers.

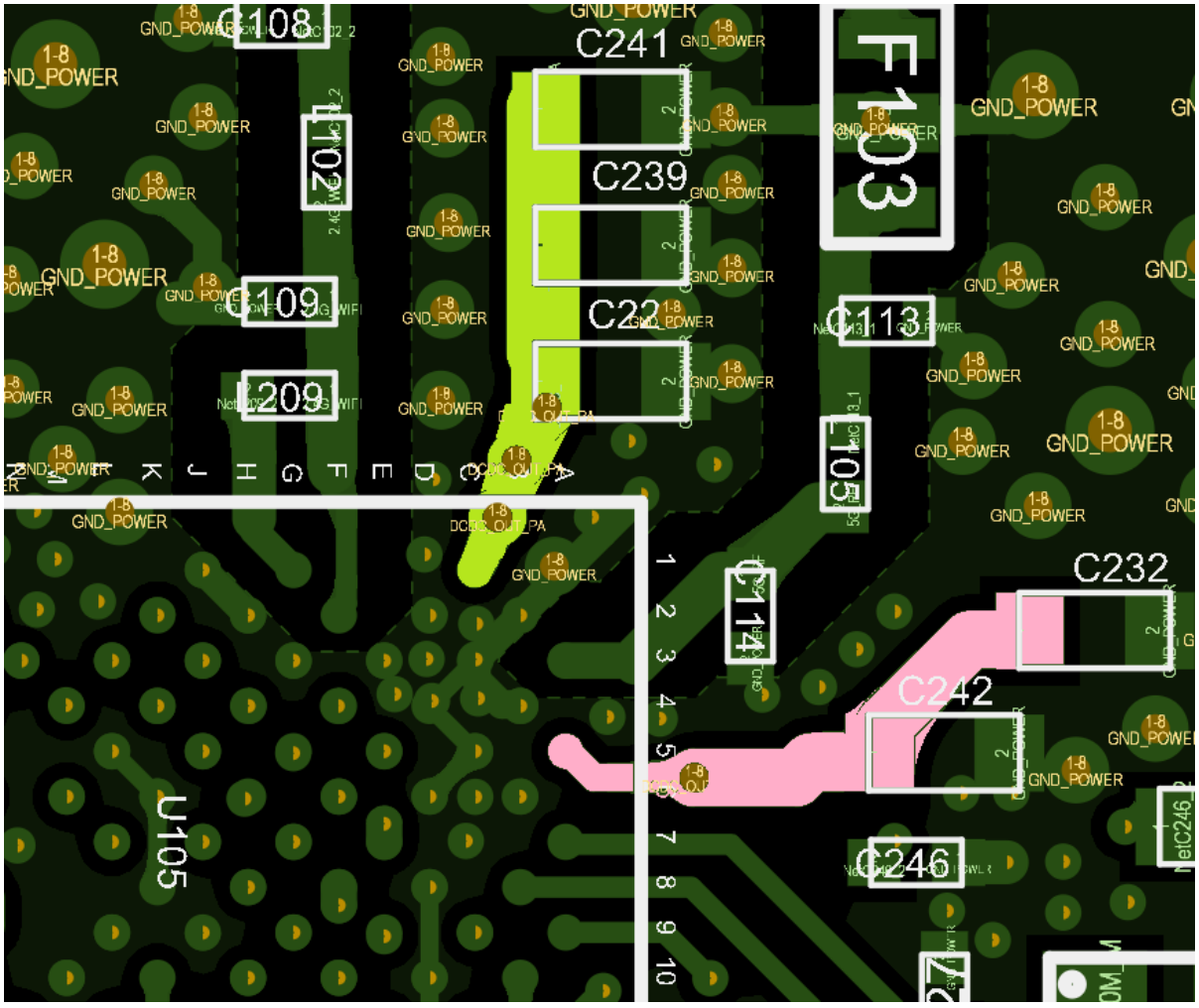

Figure 29. Components placement, vias, and traces for VDD_RFPA (green) and VDD_RF (purple)

- For VDD_DIO1 and VDD_DIO2, use traces with 200 µm width.
- Place the power vias and ground vias as close as possible to the decoupling capacitors.

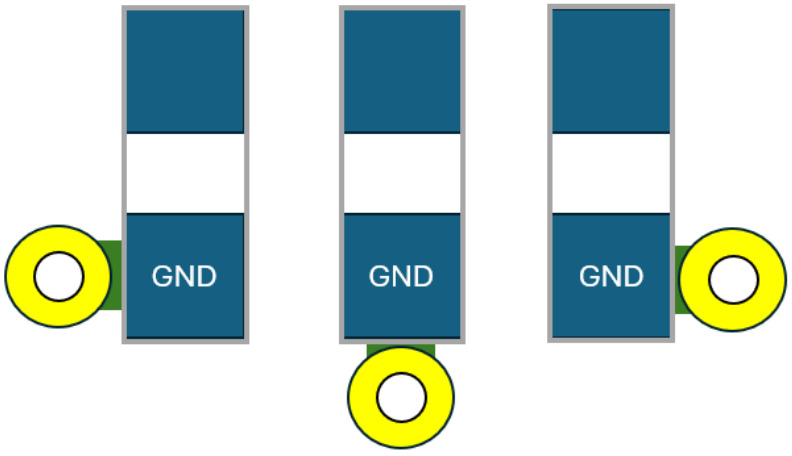

Figure 30. Recommended ground vias layout for the capacitance

5.2 PCB Layout Guidelines for Crystal

PCB layout guidelines for crystal:

- Place XTAL as close as possible to the IC to minimize PCB parasitic capacitance on the input pins and to reduce the chance of crosstalk and interference with other signals on the board. Note that the signals of the XTAL are not differential. Consequently, it is not necessary to be routed differentially.
- Do not route any lines under the XTAL area – risk of coupling and interference.
- Place the ground guard with ground stitching vias around the XTAL_IN and XTAL_OUT traces.
- Place the crystal close to the device and keep it as far away as possible from the RF side of the device and high frequency digital signal traces such as SDIO or QSPI.

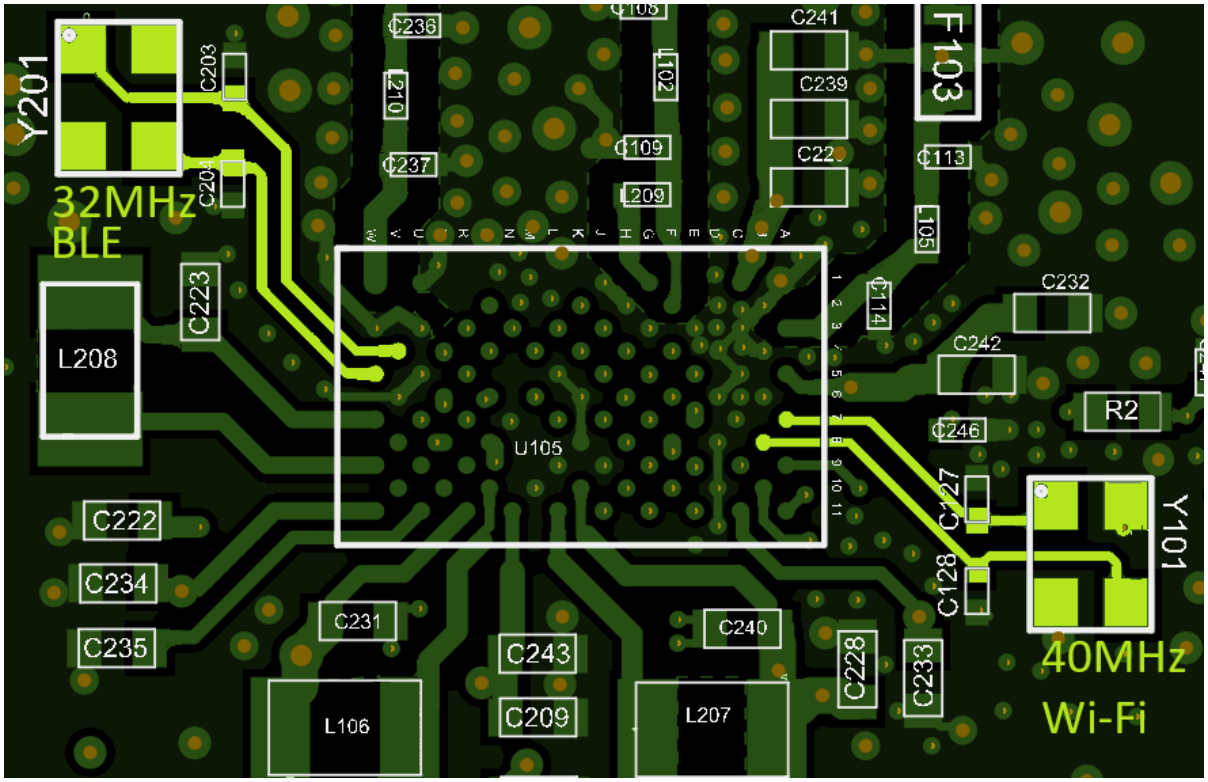

Figure 31. PCB placement and routing of 32 MHz XTAL for Bluetooth LE and 40 MHz XTAL for Wi-Fi

5.3 RF Specific Guidelines

The PCB layout guidelines for RF interface:

- For Wi-Fi subsystem and 2.4 GHz band, the inductor connected to RFTX_2G and RFRX_2G pins is a part of the RF circuit and it must be placed closest possible to the chip.

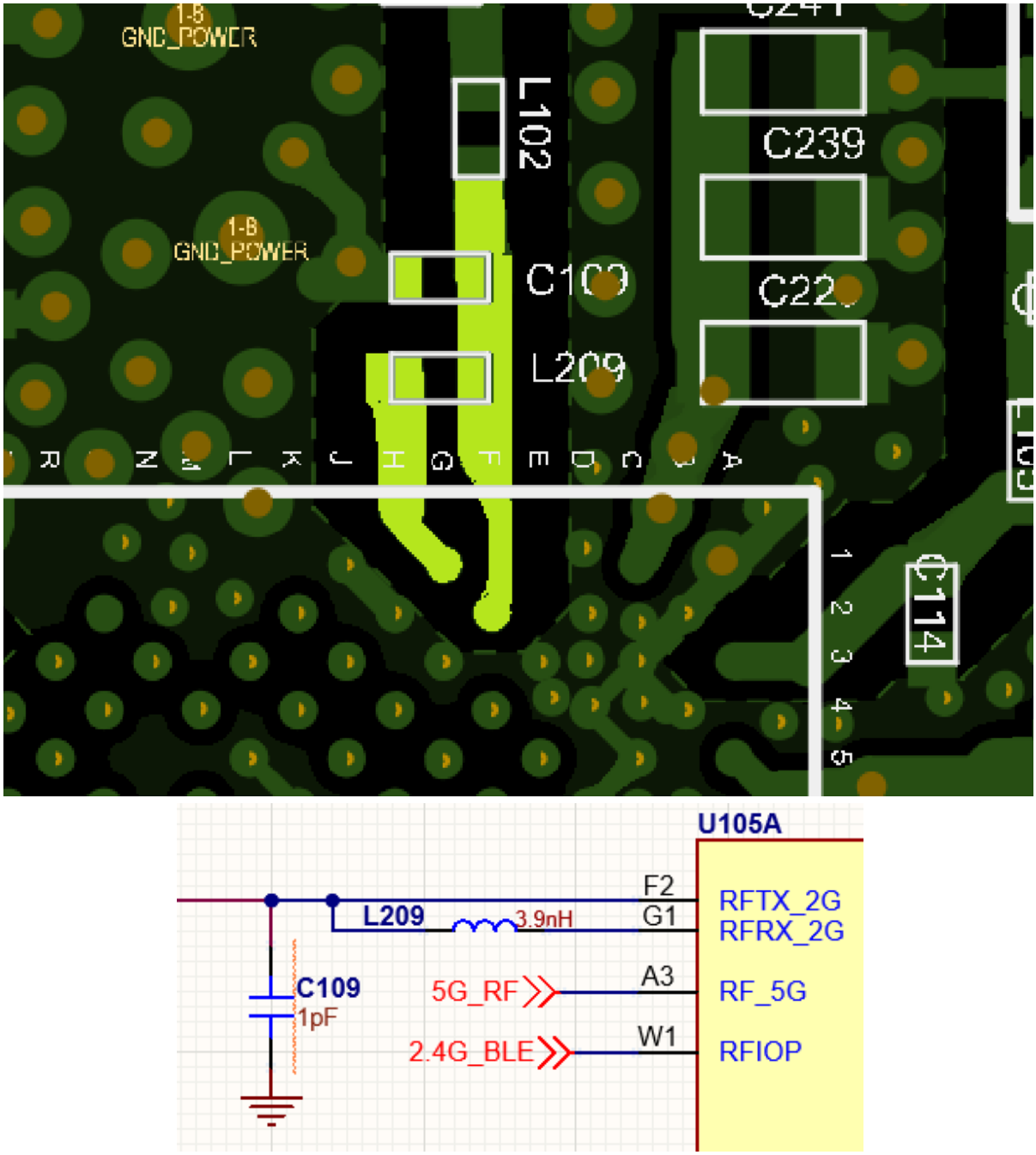

Figure 32. Placement of LC circuit close to RF pins

- Route the RF signals on the top layer with 50 Ω impedance. A good PCB design practice is to have controlled impedance of the routed traces. It is important to properly route the RF strip line to the antenna.
- Place all RF components on the same layer. This way you avoid using vias for transferring the RF signal from one layer to the other.
- Reference the RF signals to a solid ground plane. Apply multiple vias and add GND stitching vias to increase the performance of the system, as shown in Figure 33.
- Keep the high-speed control signal traces as far away as possible from the RF traces.
- Add ground vias close to the RF front-end components pins for a good return path.
- The RF trace must present impedance equal to 50 Ω. Impedance depends on:
  - the physical dimension of the RF trace
  - the distance between RF Trace and GND planes located under and along the track.

- Dielectric constant of the PCB material.

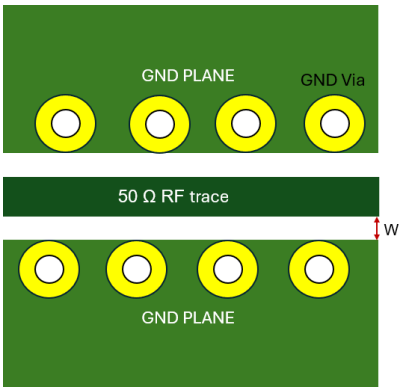

Figure 33. Ground with stitching vias

- The RF bend trace routing should be smooth with a large radius rather than 90 degrees with a sharp edge, as shown in RF Specific Guidelines.

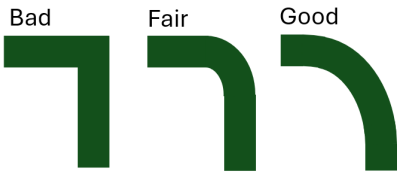

Figure 34. Example of RF trace routing

- Minimize the stubs routing of the configuration straps to the chip lines. Where branched routing is used, minimize the length of the stub. Place the configuration strap resistor in the path or the routed trace where possible (close to the chip). See Figure 35.

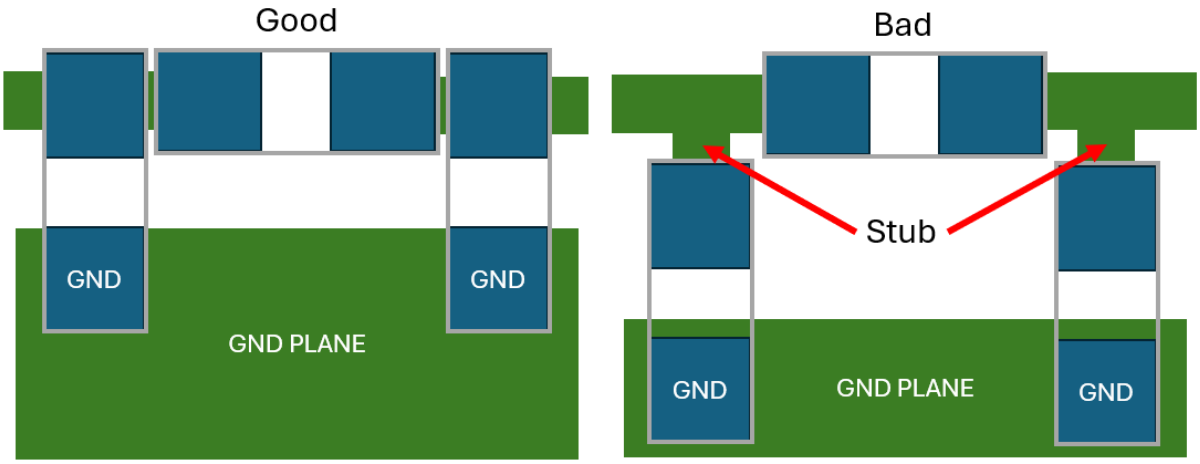

Figure 35. Recommended layout for minimizing the length of the stub

- RF trace to RF connector pad transition must be tapered to avoid discontinuity and high insertion loss, especially at 5 GHz band.

5.4 Antenna Considerations

Antennas general characteristics are as follows, whereas an SMA antenna is shown in Figure 36:

- Frequency range: which is the range of frequencies over which the antenna operates efficiently and maintains its desired characteristics. A Wi-Fi antenna covers Bluetooth LE frequency band.
- Polarization: the orientation of the electric field of the radio wave (for example, vertical, horizontal, circular, or elliptical)
- Impedance: the antenna's resistance to the flow of electrical current at its feed point, crucial for matching with the transmission line.
- Antenna VSWR (Voltage Standing Wave Ratio) measures impedance matching.
- Gain: indicates the antenna's ability to increase radiated power, often expressed in decibels relative to an isotropic source (dBi). It is defined either as peak or average gain.

These characteristics refer to a specific setup (size of PCB, no enclosures, no obstacles and so on) of the antenna. The setup is critical for printed antennas and ceramic antennas. For example, the size of the reference board where antenna characteristics are measured, are different to final product. Consequently, provisions for antenna matching must be added on the final design whereas the antenna performance must be verified.
For certification purposes and specifically radiated measurements, the peak antenna gain is significant because it is added on transmitted RF power. Often conducted RF TX power must be reduced to meet the certification requirements.

RFA-27-H60-GB70-G020

Specifications

Frequency	2400-2500 MHz	4900-5975 MHz	6000-7125 MHz
Peak gain	3.3 dBi	4.4 dBi	4.1 dBi
Average gain	1.7 dBi	1.9 dBi	1.6 dBi
VSWR	2.0 : 1 Max.	2.5 : 1 Max.	2.5 : 1 Max.
Polarization	Linear, vertical		
Impedance	50 Ω		
Connector	SMA PLUG		

Environment & Mechanical Characteristics

Temperature	- 10℃ to +55℃
Humidity	95% @ 25℃

Figure 36. Example of a SMA Wi-Fi6/Bluetooth LE antenna

For adding an antenna (external or PCB printed antenna) apply following considerations:

- Antenna must present impedance of 50 Ω.
- Do not place metal layers in the antenna area. The antenna footprint must be kept free of metal.
- Do not place metal screws, heatsink, any metal, and so on. Validate the antenna radiation pattern if any metal close to antenna.
- Do not use metal enclosures for products with antennas. Metal enclosures prevent the antenna from radiating and performing as intended.
- Use a pi-network, closest possible to the antenna, for matching purposes.

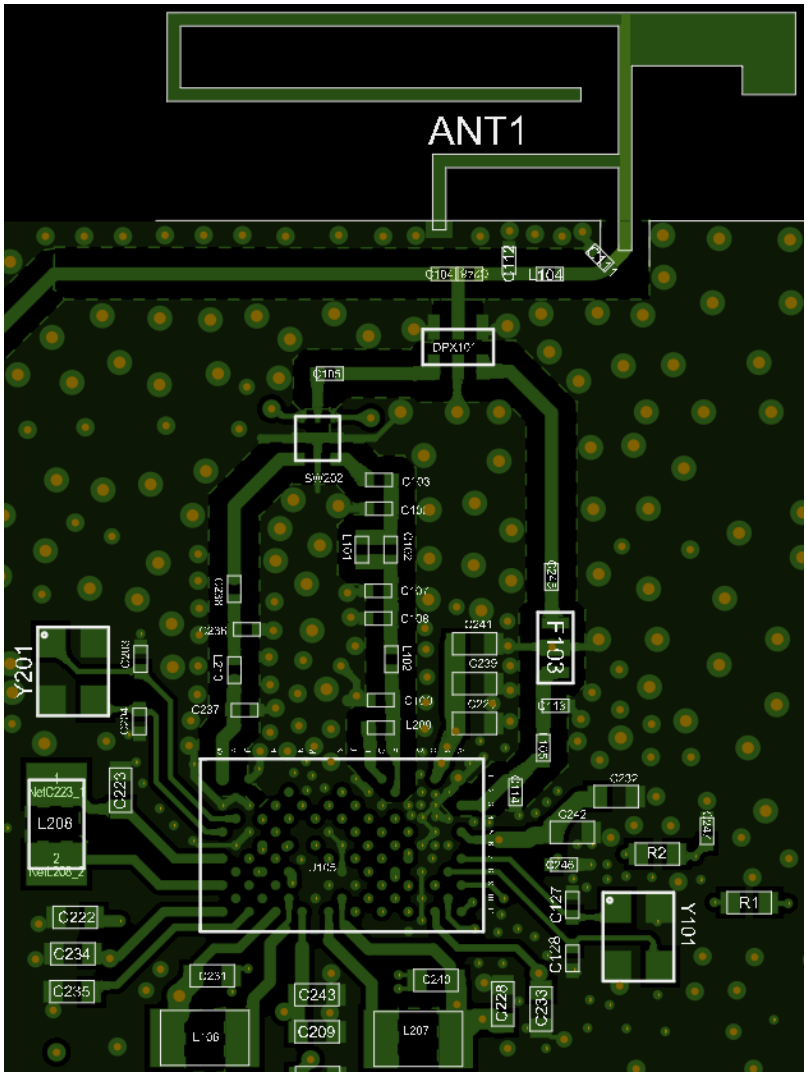

Figure 37. RF Front end and antenna for RA6W2

5.5 PCB Layout Guidelines for SDIO Interface

The PCB layout guidelines for SDIO:

- SDIO signals are routed with 50 Ω impedance.
- Keep the same trace length for all SDIO signals and as short as possible.
- The SDIO signals as far away as possible from the high-speed trace.

Appendix A RA6W2 Application Circuit

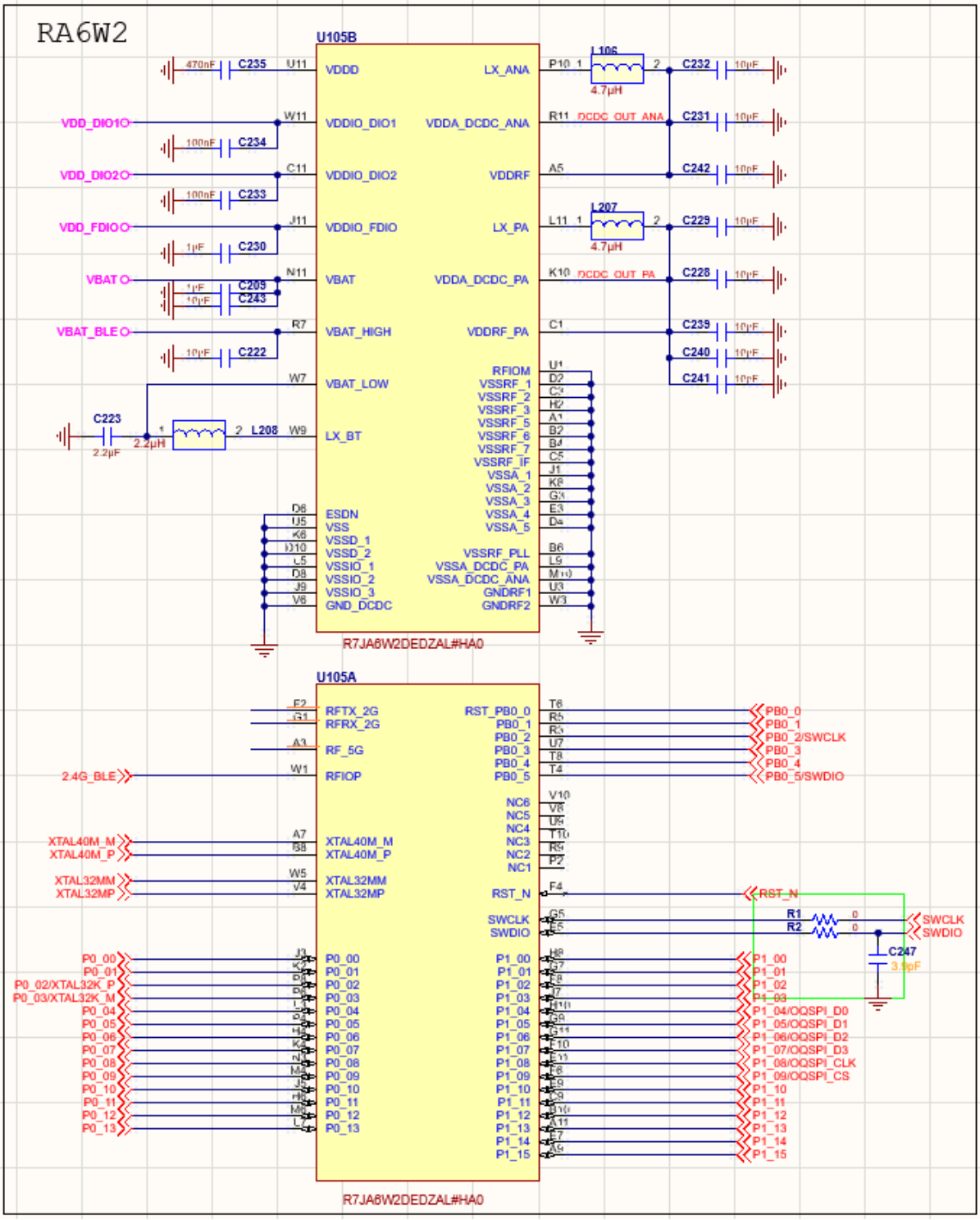

Figure 38. Schematic of the RA6W2 circuit

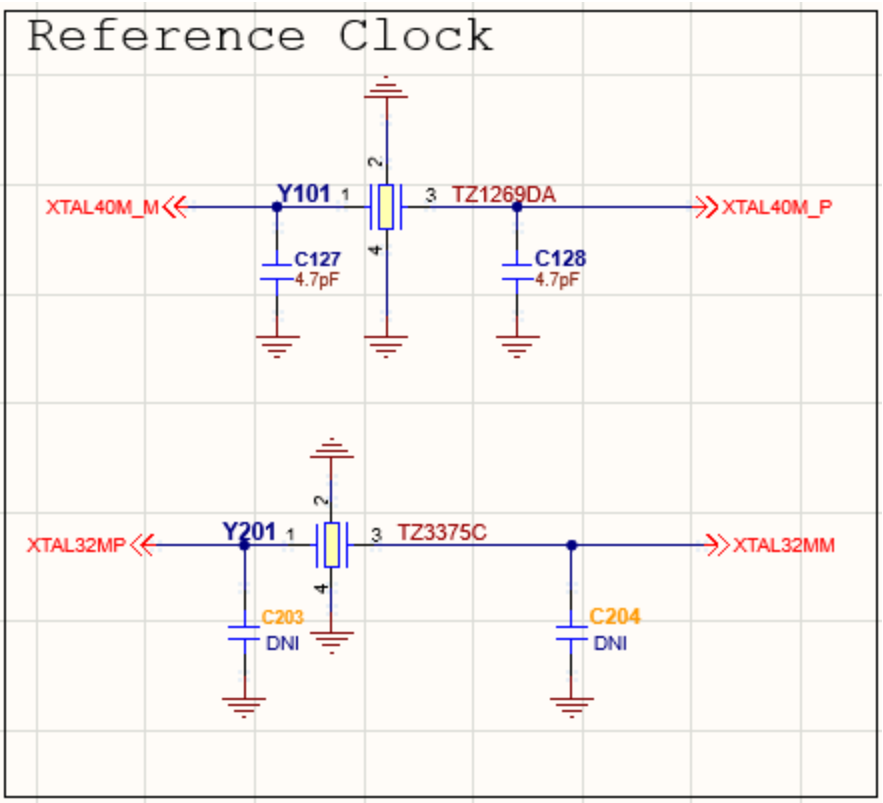

Figure 39. Schematic of the XTAL circuit

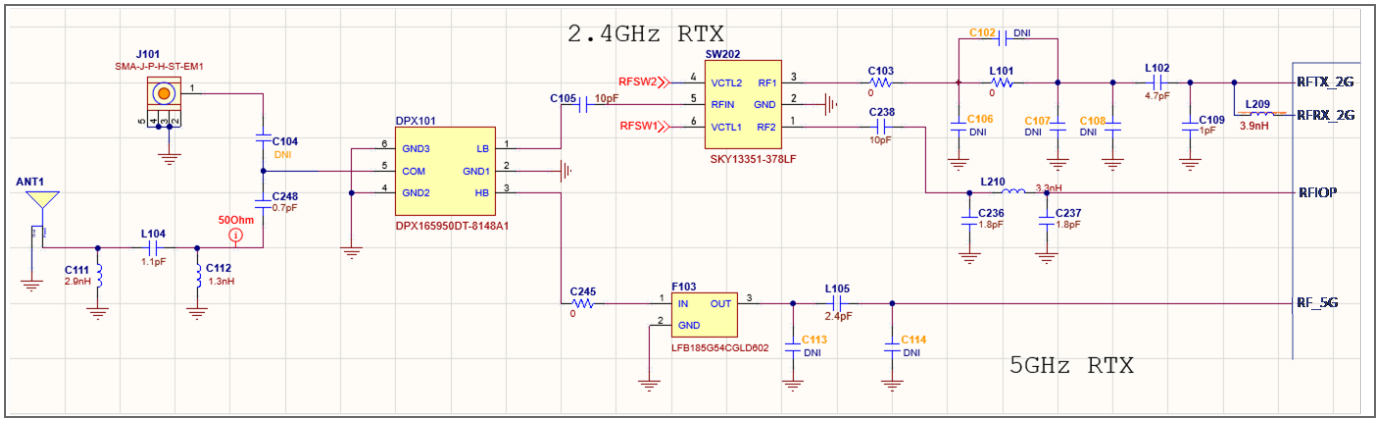

Figure 40. Schematic of RF section

6. Revision History

Revision	Date	Description
1.00	June 9, 2026	First version.

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