User's Manual

R9A06G062GNP
Sub-GHz Transceiver

User's Manual: Hardware

RF Transceiver

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

CONTENTS

Section 1 Overview

1.1 Features

- This fully integrated radio transceiver covers 863 to 928 MHz, which includes the following bands:
  - European bands: 863 to 870, and 870 to 876 MHz
  - North American band: 902 to 928 MHz
  - Brazilian band: 902 to 907.5, and 915 to 928 MHz
  - Japanese band: 920 to 928 MHz

- Supported types of PHY layer
  - SUN FSK
    - Symbol rates: 10, 20, 50, 100, 150, 200 kbps
    - Forward error correction (FEC)
    - Modulation methods: 2FSK, GFSK
  - SUN OFDM
    - Option 1: 100, 200, 400, 800, 1200, 1600, 2400 kbps
    - Option 2: 50, 100, 200, 400, 600, 800, 1200 kbps
    - Option 3: 25, 50, 100, 200, 300, 400, 600 kbps
    - Option 4: 12.5, 25, 50, 100, 150, 200, 300 kbps

- MAC
  - 32-bit timer
  - Transmission RAM, reception RAM: 2 Kbytes each
  - Interrupt
  - 16- or 32-bit auto CRC
  - Address filtering with automatic acknowledgement reply
  - Antenna diversity
  - Auto CSMA-CA

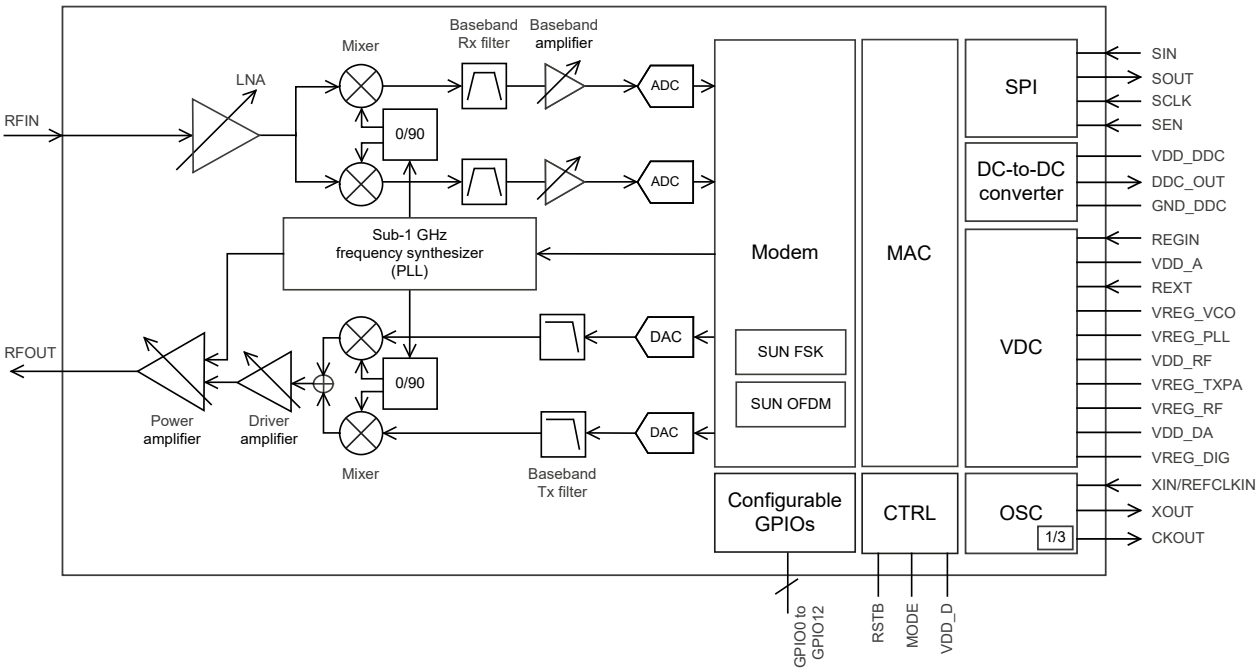
- Transceiver control interface: Serial peripheral interface (SPI)

- Radio transceiver features
  - Programmable Tx output power up to +15 dBm in SUN FSK
  - Programmable Tx output power up to +11 dBm in SUN OFDM
  - Receiver sensitive down to -109 dBm in 50-kbps SUN-FSK reception
  - Receiver sensitive down to -119 dBm in option-4 MCS0 SUN OFDM
  - Received signal strength indicator, energy detection
  - Internal voltage regulators
  - Operating voltage: 2.7 to 3.6 V
  - Low power consumption (incl. for baseband processing)
    - Standby: 0.5 µA
    - Rx active: 16.7 mA for SUN FSK (2GFSK) at 100 kbps
    - Rx active: 21.5 mA for SUN OFDM, option 1, MCS6
    - Tx active: 62.0 mA for SUN-FSK +15-dBm output power
    - Tx active: 68.0 mA for SUN-OFDM +10-dBm output power
  - Operating ambient temperature: -40 to +85°C
  - Package: 40-pin HVQFN (6 × 6, 0.5-mm pitch)

1.2 Applications

- Smart meter (electricity, gas, tap water) supporting products
  IEEE 802.15.4, Wi-SUN™
- HEMS controller
- Security and building automation
- Industrial monitoring and control
- Wireless sensor networks
- Energy-harvesting applications, and others

1.3 Block Diagram



- Receiver path

The reception architecture applies low intermediate frequency conversion. The received RF signal is amplified by the low-noise amplifier (LNA), and down-converted to the IF range by using orthogonally modulated data I and Q. The reception path has high linearity, wide dynamic range with programmable gain, and high-level on-chip channel filtering that guarantees robust operation in the sub-GHz frequency band. The auto gain control (AGC) algorithm is realized by using feedback control from the digital circuit that is optimized for high-speed response. The power detector connected to the outputs of the LNA and baseband amplifiers (BBAs) adjusts the LNA and BBA gains to optimize IM3, frequency channel selectability, and receiver sensitivity.

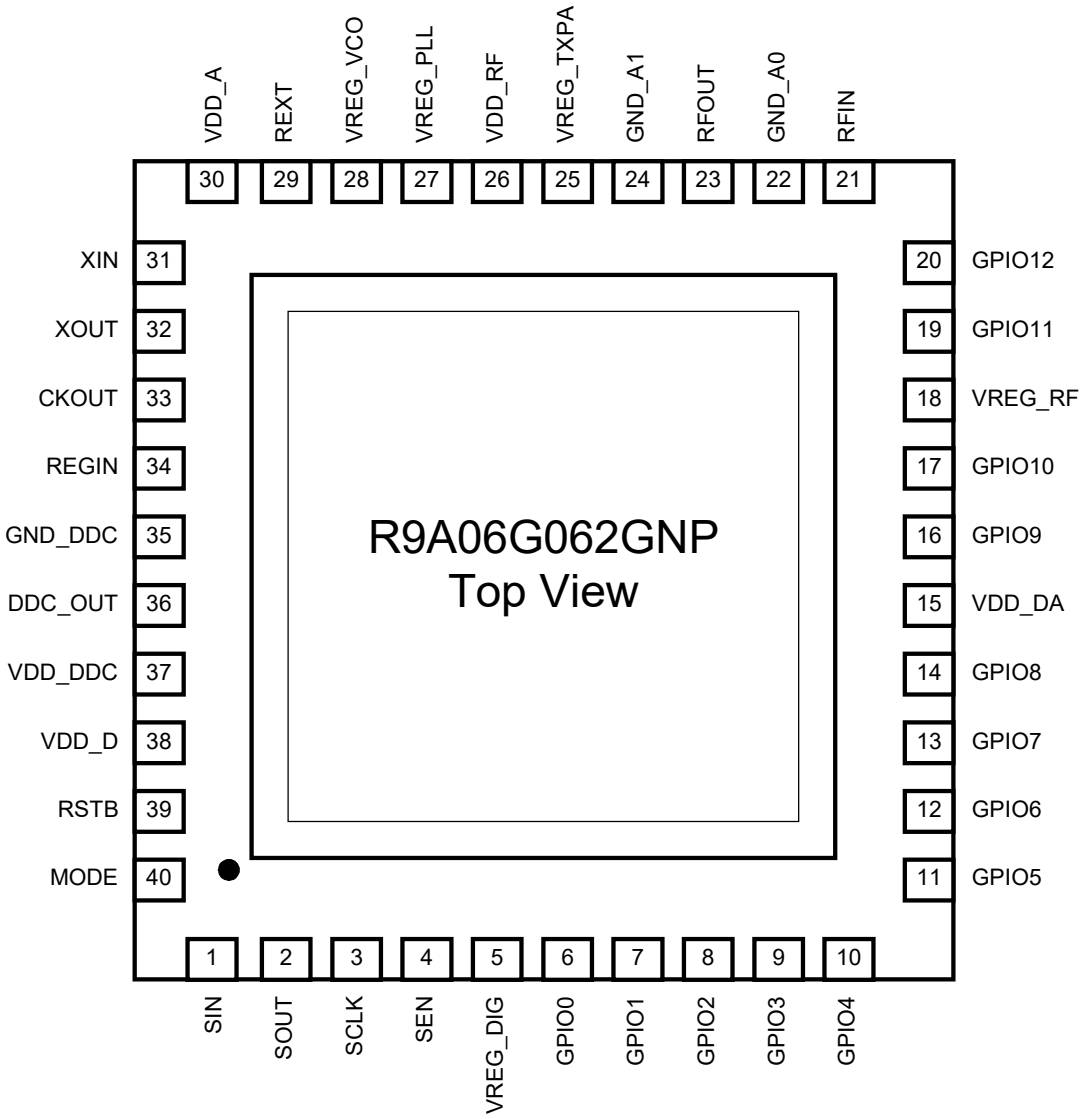
- Transmitter path

The FSK modulation transmitter modulates and synthesizes the RF synthesizer frequency. The RF synthesizer generates the local signal for input to the power amplifier (PA), and the output level is specifiable in 1-dB steps so that the antenna level is within the range from -15 dBm to +15 dBm.
The OFDM modulation transmitter is a zero-IF transmitter in which all circuits required for OFDM modulation transmission are integrated, including a modem and DAC in the digital circuit transmission analog circuit, and a power amplifier. The baseband data for transmission are digitally modulated in the modem block, and up-converted to the sub-GHz frequency band along the transmitter path. The transmitter path handles signal filtering, I/Q up-conversion, high-output power amplification, and RF filtering. The output power level of the result of OFDM modulation is specifiable within the range from -19 dBm to +11 dBm. The maximum output power depends on the modulation and coding scheme (MCS).

- Peripheral circuits
  - A DC-to-DC converter (DDC) that realizes power conversion efficiency of 87% is incorporated.
  - A crystal resonator must be connected between XIN and XOUT for supplying a clock signal to this device. An external clock can also be used to input a suitable signal level to XIN or XOUT.
  - Communications with an external MCU are handled through a standard 4-pin SPI bus.
  - Thirteen GPIO port pins (GPIO0 to GPIO12) are available for use by setting the respective registers.

1.4 Diagram of the Package and Pin Layout

- 40-pin plastic HVQFN (6 × 6 mm, 0.5-mm pitch, NiPdAu substrate)



Caution Connect the exposed pad to ground.

1.5 Pin Functions

No.	Pin Name	I/O	A/D	Description
1	SIN	I	D	Serial input
2	SOUT	O	D	Serial output
3	SCLK	I	D	Serial clock
4	SEN	I	D	Serial enable
5	VREG_DIG	O	A	Internally regulated analog 1.1-V supply output voltage for digital circuits
6	GPIO0	I/O	D	General-purpose digital I/O 0
7	GPIO1	I/O	D	General-purpose digital I/O 1
8	GPIO2	I/O	D	General-purpose digital I/O 2
9	GPIO3	I/O	D	General-purpose digital I/O 3
10	GPIO4	I/O	D	General-purpose digital I/O 4
11	GPIO5	I/O	D	General-purpose digital I/O 5
12	GPIO6	I/O	D	General-purpose digital I/O 6
13	GPIO7	I/O	D	General-purpose digital I/O 7
14	GPIO8	I/O	D	General-purpose digital I/O 8
15	VDD_DA	I	A	3.3-V power supply voltage for the digital and analog circuits
16	GPIO9	I/O	D	General-purpose digital I/O 9
17	GPIO10	I/O	D	General-purpose digital I/O 10
18	VREG_RF	O	A	Internally regulated analog 1.1-V supply output voltage for RF section
19	GPIO11	I/O	D	General-purpose digital I/O 11
20	GPIO12	I/O	D	General-purpose digital I/O 12
21	RFIN	I	A	Rx input
22	GND_A0	I	A	Analog ground
23	RFOUT	O	A	Tx output
24	GND_A1	I	A	Analog ground
25	VREG_TXPA	O	A	Internally regulated analog 1.1-V supply output voltage for the power amplifier (PA)
26	VDD_RF	I	A	3.3-V RF power supply voltage
27	VREG_PLL	O	A	Internally regulated analog 1.1-V supply output voltage for PLL
28	VREG_VCO	O	A	Internally regulated analog 1.1-V supply output voltage for VCO
29	REXT	I	A	External reference resistor connection port
30	VDD_A	I	A	3.3-V power supply voltage for the analog circuits
31	XIN	I	A	Crystal oscillator input
32	XOUT	I/O	A	Crystal oscillator output
33	CKOUT	O	A	Clock output (16 MHz)
34	REGIN	I	A	1.4- to 1.8-V DDC_OUT voltage input
35	GND_DDC	I	A	DC-to-DC converter ground
36	DDC_OUT	O	A	1.4- to 1.8-V DC-to-DC converter output voltage
37	VDD_DDC	I	A	3.3-V DC-to-DC converter power supply voltage
38	VDD_D	I	A	3.3-V power supply voltage for the digital circuits
39	RSTB	I	D	Reset-bar input (active-low)
40	MODE	I	D	Mode switch (always low)
	EPAD			Exposed Pad. Connect the exposed pad to the ground.

1.6 Ordering Information

Table 1-1 shows the ordering part number of the R9A06G062.

Table 1-1 Ordering Part Number

Ordering Part Number	Packaging Specification	Fields of application
R9A06G062GNP#AC1	Tray	Industrial applications

Section 2 Pin Functions

2.1 Pin Functions

2.1.1 Digital Pins

1. RSTB
   This is the active-low system reset pin. Driving this pin low resets the system and driving it high releases the system from the reset state.

2. SIN, SCLK, SEN
   These pins are for the inputs of the data (SIN), clock (SCLK), and slave enable (SEN) signals to the serial peripheral interface (SPI). Driving SEN low allows serial communications. Setting the corresponding bits of pull-up pull-down selection register 3 (PULLSEL3) selects the use of the on-chip pull-up or pull-down resistor for each of the pins.

3. SOUT
   This pin is for the output of data from the serial peripheral interface (SPI).

4. GPIO0 to GPIO12
   These are input and output port pins. These pins can also be used as outputs for the INTOUT0 interrupt, CTX, CPS, and CSD signals. Setting the corresponding bits of pull-up pull-down selection registers 0 to 3 (PULLSEL0 to PULLSEL3) selects the use of the on-chip pull-up or pull-down resistor for each of the pins. Port output driving capability switching registers 0 and 1 (GPIODRV0 and GPIODRV 1) can be used to switch of the driving capability per pin.

   (a) Input/output port mode
   Setting the corresponding bits of port direction registers 0 and 1 (GPIODIR0 and GPIODIR1) specifies input or output for the individual port pins. When a pin is set as an output, the value specified by the corresponding bit in port data register 0 or 1 (GPIODATA0 or GPIODATA1) is output.

   (b) Port functions
   The GPIO function selection registers (BBGPIOFUNCSEL0 to BBGPIOFUNCSEL6) can be used to select the pin functions for each of the GPIO port pins.

5. MODE
   This is the input pin for mode switching. Leave it open-circuit or fix it to the low level by connecting it to the ground on the board.

6. XIN, XOUT
   These are reference clock pins.

   - When a crystal resonator is to be connected to XIN and XOUT
     Connect a 48-MHz crystal resonator between the XIN and XOUT pins. We recommend using a crystal resonator that satisfies the characteristics specified in 9.3, Specifications of the Crystal Resonator.

   - When an external clock is to be connected to XIN
     Input a 48-MHz external clock to the XIN pin via a DC-cutting capacitor. The input signal should be a clipped sine wave clock with amplitude of at least 0.8 Vpp. If you use this connection, connect the XOUT pin to the ground on the board via a 1-nF decoupling capacitor.

7. CKOUT
   This pin is for the output of a 16-MHz clock signal.

2.1.2 Analog Pins

1. RFIN
   This is the RF-reception input pin of this device.

2. RFOUT
   This is the RF-transmission output pin of this device.

2.1.3 Power Supply Pins

For handling of the power supply pins, see section 8, Connections of the Peripheral Circuits.

1. VDD_DA, VDD_RF, VDD_A, VDD_D, VDD_DDC
   These are the positive power supply pins.

2. GND_A0, GND_A1, GND_DDC
   These are the ground level pins.

3. VREG_DIG, VREG_RF, VREG_TXPA, VREG_PLL, VREG_VCO
   These are output pins for internally regulated analog power supply voltages. Connect these pins to the ground on the board via bypass capacitors.

4. REGIN, DDC_OUT
   The REGIN and DDC_OUT pins are the RF power supply input and output, respectively The power supply converted by the internal DC-to-DC converter is output to the DDC_OUT pin. The voltage is smoothed and lowered by an inductor and capacitor, and the result is input to the REGIN pin.

5. REXT
   This is an external reference resistor connection pin.

Remark For protection against noise and latch-up, connect a bypass capacitor between VDD and the ground line. The wiring should be as short as possible, and relatively thick.

2.2 Handling of Unused Pins

Table 2-1 describes how to handle unused pins.

Table 2-1 Handling of Unused Pins

Pin Name	Input/Output	Recommended Handling of Unused Pins
GPIO0 to GPIO12	Input/output	As inputs: Leave them open-circuit, or individually connect each pin to VDD_DDC via a resistor. As outputs: Leave them open-circuit.
CKOUT	Output	Leave it open-circuit.

Section 3 Baseband Section

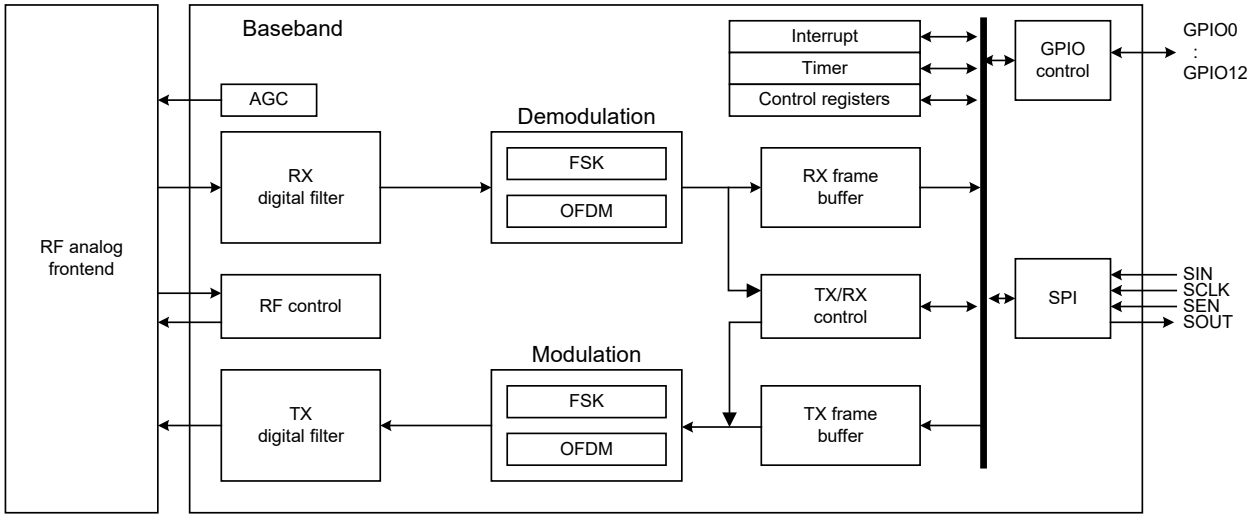
This device incorporates a baseband section that includes the following blocks.

- 32-bit timer
- Transmission RAM
- Reception RAM
- Frame configuration
- Filters
- Interrupt control
- CRC calculation circuit
- Automatic ACK reply
- Automatic ACK reception
- Automatic switching to reception
- Automatic CSMA-CA
- Port control

3.1 Block Diagram of the Baseband Section

Figure 3 - 1 is a block diagram of the baseband section.

Figure 3 - 1 Block Diagram of the Baseband Section

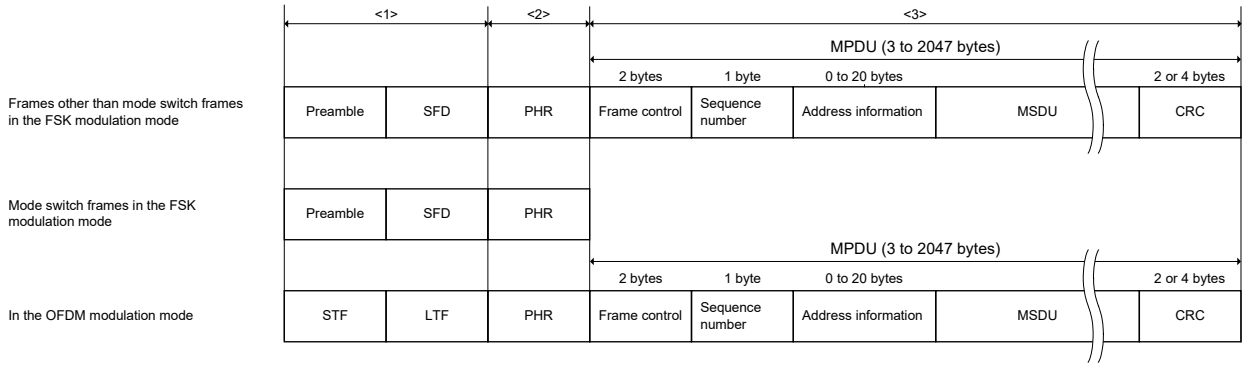


3.2 Configuration of Frames

3.2.1 Configuration of frames for transmission

This device automatically generates and outputs frames for transmission. Figure 3 - 2 shows the configuration of frames for transmission. In the FSK modulation mode, the frame configuration after a PHR depends on whether the frame is a mode switch frame or not.

Figure 3 - 2 Configuration of Frames for Transmission



SFD: Start of Frame Delimiter PHR: PHY header

STF: Short Training Field LTF: Long Training Field

MSDU: MAC Service Data Unit CRC: Cyclic Redundancy Check

MPDU: MAC Protocol Data Unit

<1> In the FSK modulation mode, a frame starts with a preamble, which is followed by an SFD.
In the OFDM modulation mode, a frame starts with an STF, which is followed by an LTF.

<2> The PHR bit configuration depends on whether the mode is FSK modulation or the OFDM modulation. For details, see 3.2.2 Configuration of a PHR.

<3> An MPDU is a data unit from 3 bytes to 2047 bytes in length. The data written in the transmission RAM are output sequentially. The CRC data generated in the CRC calculation circuit are automatically appended as the last 2 or 4 bytes following an MPDU when the setting of the NOCRC bit in the transmission and reception mode register 2 is 0.

- A frame control field is a 2-byte data unit.
  - — Bits 2 to 0 indicate the Frame Type field.
    000B: A beacon frame
    001B: A data frame
    010B: An ACK frame
    011B: A MAC command frame
    100B to 111B: Reserved
  - — Bit 3 indicates the Security Enabled field.
    Bit 4 indicates the Frame Pending field.
  - — Bit 5 indicates the AR field.
    Bit 6 indicates the PAN ID Compression field.

— Bits 10 and 11 indicate the Destination Addressing Mode field.
Bits 14 and 15 indicate the Source Addressing Mode field.
— Bits 12 and 13 indicate the Frame Version field.

- A sequence number field is a 1-byte data unit.
- An address information field indicates the PAN ID and address of the source and destination in transmission.
- An MSDU, also called a MAC payload, is the payload of a frame.
- A CRC is a 2- or 4-byte frame CRC checking sequence.

3.2.2 Configuration of a PHR

(1) For frames other than mode switch frames in the FSK modulation mode

Figure 3 - 3 shows the PHR bit configuration for frames other than mode switch frames in the FSK modulation mode.

Figure 3 - 3 PHR Bit Configuration for Frames Other Than Mode Switch Frames in the FSK Modulation Mode

Bit array	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Bit configuration	MS	R1	R0	FCS	DW	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0

MS: Mode switch

This bit holds the value of the mode switch enable bit (bit 0) in the mode switch frame transmission register. The following values are automatically transmitted when the setting of this bit is 0.

R1, R0: Reserved

The value of these bits is fixed to 00B.

FCS: FCS type

This bit holds the value of the number-of-FSKCRC-bit switching bit (bit 2) in FSK control register 1.

DW: Data whitening

This bit holds the value of the FSKDW enable bit (bit 3) in FSK control register 1.

L10 to L0: Frame length

These bits hold the value of the frame length from bits 10 to 0 in the transmitted frame length register.

(2) For mode switch frames in the FSK modulation mode

Figure 3 - 4 shows the PHR bit configuration for mode switch frames in the FSK modulation mode. Before such a frame is transmitted, calculate the values of the checksum and parity checking, and then write them to the mode switch frame transmission register.

Figure 3 - 4 PHR Bit Configuration for Mode Switch Frames in the FSK Modulation Mode

Bit array	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Bit configuration	MS	M1	M0	FEC	NEWMODE							B3	B2	B1	B0	PC

MS: Mode switch

This bit holds the value of the mode switch enable bit (bit 0) in the mode switch frame transmission register. The following values are automatically transmitted when the setting of this bit is 1.

M1, M0: Mode switch parameter entry

These bits hold the value of bits 1 and 2 in the mode switch frame transmission register.

FEC: NEWMODE FEC

This bit holds the value of bit 3 in the mode switch frame transmission register.

NEWMODE: NEWMODE

These bits hold the value of bits 4 to 10 in the mode switch frame transmission register.

B3 to B0: Checksum

These bits hold the value of bits 11 to 14 in the mode switch frame transmission register.

PC: Parity checking

This bit holds the value of bit 15 in the mode switch frame transmission register.

(3) In the OFDM modulation mode

Figure 3 - 5 shows the PHR bit configuration in the OFDM modulation mode.

Figure 3 - 5 PHR Bit Configuration in the OFDM Modulation Mode

Bit array	0	1	2	3	4	5	6	7
Bit configuration	RATE4	RATE3	RATE2	RATE1	RATE0	R0	L10	L9

Bit array	8	9	10	11	12	13	14	15
Bit configuration	L8	L7	L6	L5	L4	L3	L2	L1

Bit array	16	17	18	19	20	21	22	23
Bit configuration	L0	R1	R2	SCBR1	SCBR0	R3	HCS7	HCS6

Bit array	24	25	26	27	28	29	30	31
Bit configuration	HCS5	HCS4	HCS3	HCS2	HCS1	HCS0	TAIL5	TAIL4

Bit array	32	33	34	35
Bit configuration	TAIL3	TAIL2	TAIL1	TAIL0

RATE4 to RATE0: Rate

The value of the RATE4 and RATE3 bits is fixed to 00B.

The value of the RATE2 to RATE0 bits is the setting of bits 2 to 0 in OFDMPHR transmission register 0.

R0: Reserved

The value of this bit is fixed to 0B.

L10 to L0: Frame length

These bits hold the value of the frame length from bits 10 to 0 in the transmitted frame length register.

R2, R1: Reserved

The value of these bits is fixed to 00B.

SCBR1, SCRB0: Scrambler

These bits hold the value of bits 4 and 3 in OFDMPHR transmission register 0.

R3: Reserved

The value of this bit is fixed to 0B.

HCS7 to HCS0: HCS

The value of these bits is automatically calculated and transmitted.

TAIL5 to TAIL0: Tail

The value of these bits is fixed to 000000B.

3.3 Baseband Interrupts

Table 3 – 1 shows the interrupt sources. When the setting of at least one of the interrupt source flags corresponding to the interrupt sources listed in Table 3 – 1 is 1, and output of the corresponding interrupt signal is enabled by the setting in the INTOUT0 interrupt enable registers 0 to 7, the output on the GPIO port pin selected as the INTOUT0 output pin goes to the high level. When the settings of all the interrupt source flags are 0, the output on the pin is at the low level. Any among the port pins GPIO0 to GPIO12 can be selected as required to operate as the INTOUT0 output pin. Generation of interrupt requests due to the respective interrupt sources can be enabled or disabled by setting the corresponding interrupt source enable bits. The active sense (high or low) of the INTOUT0 output can be switched by setting the INTOUT0SEL bit. The following interrupt source flags are automatically cleared upon completion of reception if the setting of the reception completion synchronized clearing bit is 1.

- Frame length
- Address filtering
- Start reception
- AGC completion
- Preamble detection
- Carrier sense

Interrupt operations:
Upon the generation of an interrupt request due to a given interrupt source condition being satisfied while the corresponding interrupt request is enabled, the corresponding interrupt source flag is set to 1 to indicate generation of the interrupt request. Reading this bit only clears it to 0 after it has been read as 1. Dummy-read the bit to clear it because it is not writable. When an interrupt source flag is set to 1 while the setting of the corresponding interrupt enable bit is 1, the output on the GPIO port pin selected as the INTOUT0 output pin goes to the high level if the setting of the INTOUT0 output sense switching bit is 0. Generation of interrupt request signals due to each of the interrupt sources can be enabled or disabled by setting the corresponding interrupt source enable bits. While the setting of an interrupt source enable bit is 0, the setting of the corresponding interrupt source flag remains 0 upon the generation of an interrupt request even if the corresponding interrupt source condition is satisfied.

Reception canceled interrupts:
Reception is suspended upon the generation of a reception canceled interrupt. After the suspension, this device is automatically placed back in the reception waiting state after a transition through the IDLE state. As reception is suspended during frame reception in this case, no reception completion interrupt is generated. Reception canceled interrupts are generated in the following cases.

- Reception is abandoned due to address filtering.
- Reception is abandoned due to an illegal frame length.
- Reception is abandoned due to reception level filtering.
- Reception is abandoned due to overwriting of received data.
- Reception is abandoned due to the detection of a reception level error, that is, a communications error such as no signal being received during frame reception.
- Reception is abandoned due to the occurrence of an HCS error in the OFDM modulation mode.

- Reception is abandoned due to the cancellation of reception because reception is disabled.
- Reception is abandoned due to MS frame cancellation.

Upon the generation of a reception canceled interrupt due to the detection of a reception level error, that is, a communications error such as no signal being received during frame reception, a reception level interrupt is also generated simultaneously. Reception restarts from the reception RAM bank that was operating when reception was canceled. The reception RAM bank n status bit that had been set to 1 in response to the frame being received when a reception canceled interrupt was generated, meaning that data had been received in bank n, is cleared to 0, meaning that reception is again enabled.

The following interrupt source flags are automatically cleared upon cancellation of reception if the setting of the reception canceling synchronized clearing bit is 1.

- Bank 0 reception completion
- Bank 1 reception completion
- Frame length
- Address filtering
- Start reception
- Number of received bytes
- AGC completion
- Preamble detection
- Carrier sense

Table 3 - 1 Interrupt Sources (1/2)

Number	Interrupt Source	Interrupt Generation Condition
1	Timer comparison 0	The value of the 32-bit timer matches the value of the timer comparison registers 0 and 1 (BBTCOMP0REG0 and BBTCOMP0REG1).
2	Timer comparison 1	The value of the 32-bit timer matches the value of the timer comparison registers 0 and 1 (BBTCOMP1REG0 and BBTCOMP1REG1).
3	Timer comparison 2	The value of the 32-bit timer matches the value of the timer comparison registers 0 and 1 (BBTCOMP2REG0 and BBTCOMP2REG1).
4	Calibration completion	Calibration is completed.
5	Bank 0 transmission completion	The data in transmission RAM bank 0 have been transmitted.
6	Bank 1 transmission completion	The data in transmission RAM bank 1 have been transmitted.
7	Frame synchronization transmission completion	A frame synchronization part such as SFD has been transmitted.
8	CSMA-CA completion	A CSMA-CA sequence is completed.
9	Bank 0 reception completion	The reception RAM bank 0 becomes full.
10	Bank 1 reception completion	The reception RAM bank 1 becomes full.
11	Frame length	A frame length has been received.
12	Address filtering[Note]	Address matching is detected.
13	Reception overrun	In the following cases: • Reception by reception RAM bank 0 is restarted while the setting of the reception RAM bank 0 status bit is 1. • Reception by reception RAM bank 1 is restarted while the setting of the reception RAM bank 1 status bit is 1.
14	Mode switch reception completion	A mode switch frame is received.
15	Reception level	A communications error such as no signal reception occurs during frame reception.
16	Frame transmission completion	In cases other than that described below: • Frame transmission is completed. For each frame for transmission including an ACK request while the automatic ACK reception mode is enabled: • The ACK reception is completed or ACK reception timeout occurs. In this case, an interrupt request is not generated when frame transmission is completed.
17	Number of transmitted bytes	The specified number of bytes has been transferred to the transmitter.
18	Transmission start	A transmission trigger is set via the SPI.
19	Reception start	Frame synchronization such as SFD is detected.
20	Frame reception completion	In cases other than that described below: • Frame reception is completed. For each frame for reception including an ACK request while the automatic ACK reply mode is enabled: • The ACK reply is completed. In this case, an interrupt request is not generated when frame reception is completed.
21	Number of received bytes	The specified number of bytes has been received.
22	AGC completion	AGC is completed.
23	CCA completion	A CCA sequence is completed.

Table 3 - 1 Interrupt Sources (2/2)

Number	Interrupt Source	Interrupt Generation Condition
24	Preamble detection	A preamble is detected.
25	Carrier sense	Carrier sense is detected.
26	CCA limitation	The number of times of consecutive CCAs reaches the specified number of times while the setting of the CCA continuous mode bit is 1.
27	CCA clearance	A frequency channel is cleared in accordance with the CCA result.
28	Automatic reception timeout	Timeout occurs with no received frames while automatic reception timeout is enabled.
29	Transmission underrun	Transmission to the transmitter proceeds before writing to the transmission RAM.
30	Reception canceling	Reception is canceled.

Note: In the case of frames with short lengths, or frames having no address information or only incomplete address information, an address filtering interrupt may not be generated, and only a frame reception completion interrupt may be generated.

3.4 Registers for Controlling the Baseband Section

The following registers are used to control the baseband section.

- RF start register (BBRFCON)
- Transmission and reception reset register (BBTXRXRST)
- Transmission and reception mode register 0 (BBTXRXMODE0)
- Transmission and reception mode register 1 (BBTXRXMODE1)
- RXIDLE mode register (BBRXIDLE)
- High-speed reception switching mode register (BBRXMODE)
- Enhanced ACK mode register (BBEACKMODE)
- Transmission and reception status register 0 (BBTXRXST0)
- Transmission and reception mode register 2 (BBTXRXMODE2)
- Transmission and reception mode register 3 (BBTXRXMODE3)
- Transmission and reception status register 1 (BBTXRXST1)
- Transmission and reception control register (BBTXRXCON)
- CSMA control register 0 (BBCSMACON0)
- Transmission and reception status register 2 (BBTXRXST2)
- Transmission and reception mode register 4 (BBTXRXMODE4)
- CSMA control register 1 (BBCSMACON1)
- CSMA control register 2 (BBCSMACON2)
- PAN identifier register 0 (BBPANID0)
- Short address register 0 (BBSHORTAD0)
- Extended address registers 0 (BBEXTENDAD00 to BBEXTENDAD03)
- Timer read registers 0 and 1 (BBTIMEREAD0 and BBTIMEREAD1)
- Timer comparison registers 0 and 1 (BBTCOMP0REG0 to BBTCOMP2REG0 and BBTCOMP0REG1 to BBTCOMP2REG1)
- Timestamp registers 0 and 1 (BBTSTAMP0 and BBTSTAMP1)
- Timer control register (BBTIMECON)
- Backoff period register (BBBOFFPROD)
- Timing parameter data rate setting register (BBPARAMRATE)
- Extended data rate setting register (BBEXTRATE)
- CSMA control register 3 (BBCSMACON3)
- Calibration register (BBCAL)
- ACK reply time setting register (ACKRTNTIM)
- Automatic switching to reception comparison register (AUTORCVCNT)
- Backoff cycle register (BOFFPERIOD)

- CSMA-CA end count register (CSMAENDCOUNT)
- CSMA-CA start count register (CSMASTACOUNT)
- Communication status register 1 (COMSTATE1)
- Communication status register 2 (COMSTATE2)
- Evaluation control register (BBEVAREG)
- Backoff period register 2 (BBBOFFPROD2)
- Communication status register 3 (COMSTATE3)
- ACK reception wait time setting register (ACKRCVWIT)
- Retransmission start comparison register (RETRNWUP)
- Received frame length register (BBRXFLEN)
- Received data counter register (BBRXCOUNT)
- Transmitted frame length register (BBTXFLEN)
- Frequency setting register (BBFREQ)
- IF frequency setting register (BBIFSET)
- IF frequency offset setting register 0 (BBIFOFST0)
- IF frequency offset setting register 1 (BBIFOFST1)
- SX shift frequency setting register (BBSXSFTFREQ)
- CCA time register (CCATIME)
- Transmitted data counter register (BBTXCOUNT)
- External device control register 0 (BBEXTCON0)
- External device control register 1 (BBEXTCON1)
- CTX set timing register (BBCTXSET)
- CTX clear timing register (BBCTXCLR)
- CPS set timing register (BBCPSSET)
- CPS clear timing register (BBCPSCLR)
- CSD set timing register (BBCSDSET)
- CSD clear timing register (BBCSDCLR)
- Number-of-received-byte interrupt comparison register (BBRCVINTCOMP)
- Backoff period total number register (BBBOPTOTAL)
- CCA total number register (BBCCATOTAL)
- Address filter extension address control register (BBADFCON)
- PAN identifier register 1 (BBPANID1)
- Short address register 1 (BBSHORTAD1)
- Extended address registers 1 (BBEXTENDAD10 to BBEXTENDAD13)
- Reception timeout register (BBTIMEOUT)
- INTOUT mode register (BBINTOUTMODE)

- INTOUT0 interrupt source register 0 (BBINT0REQ0)
- INTOUT0 interrupt source register 1 (BBINT0REQ1)
- INTOUT0 interrupt source register 2 (BBINT0REQ2)
- INTOUT0 interrupt source register 3 (BBINT0REQ3)
- INTOUT0 interrupt source register 4 (BBINT0REQ4)
- INTOUT0 interrupt source register 5 (BBINT0REQ5)
- IINTOUT0 interrupt source register 6 (BBINT0REQ6)
- INTOUT0 interrupt source register 7 (BBINT0REQ7)
- INTOUT0 interrupt enable register 0 (BBINT0EN0)
- INTOUT0 interrupt enable register 1 (BBINT0EN1)
- INTOUT0 interrupt enable register 2 (BBINT0EN2)
- INTOUT0 interrupt enable register 3 (BBINT0EN3)
- INTOUT0 interrupt enable register 4 (BBINT0EN4)
- INTOUT0 interrupt enable register 5 (BBINT0EN5)
- INTOUT0 interrupt enable register 6 (BBINT0EN6)
- INTOUT0 interrupt enable register 7 (BBINT0EN7)
- INTOUT0 interrupt source enable register 0 (BBINT0REQEN0)
- INTOUT0 interrupt source enable register 1 (BBINT0REQEN1)
- INTOUT0 interrupt source enable register 2 (BBINT0REQEN2)
- INTOUT0 interrupt source enable register 3 (BBINT0REQEN3)
- INTOUT0 interrupt source enable register 4 (BBINT0REQEN4)
- INTOUT0 interrupt source enable register 5 (BBINT0REQEN5)
- INTOUT0 interrupt source enable register 6 (BBINT0REQEN6)
- INTOUT0 interrupt source enable register 7 (BBINT0REQEN7)
- Number-of-transmitted-byte interrupt comparison register (BBTRNINTCOMP)
- CCA mode register (BBCCAMODE)
- Receive mode register (BBRCVMODE)
- Frame cancellation minimum length register (BBFLCNCLMIN)
- Frame cancellation maximum length register (BBFLCNCLMAX)
- Number-of-byte interrupt mode register (BBBYTEINTMODE)
- RSSI result register (BBRSSIRSLT)
- RCPI result register (BBRCPIRSLT)
- RSSI result 2 register (BBRSSIRSLT2)
- RCPI result 2 register (BBRCPIRSLT2)
- ED1 result register (BBED1RSLT)
- ED2 result register (BBED2RSLT)

- ED1 result 2 register (BBED1RSLT2)
- ED2 result 2 register (BBED2RSLT2)
- CCA clearance count register (BBCCACLRCOUNT)
- CCA limit setting register (BBCCALIMIT)
- Comparison 0 setting excess time registers (BBPASSTIME0 and BBPASSTIME1)
- Frame synchronization power value read register (BBFSYNCPOWRD)
- Frame synchronization power value 2 read register (BBFSYNCPOWRD2)
- RSSI read register (BBRSSIRD)
- RCPI read register (BBRCPIRD)
- RSSI read 2 register (BBRSSIRD2)
- RCPI read 2 register (BBRCPIRD2)
- Transmission and reception method selection register (BBTRXSEL)
- Reception method check register (BBRXMODEMONI)
- Reception prohibition register (BBRXPROHIBIT)
- Received frame counter control register (BBRCVCOUNTCNT)
- Total reception counter (BBRCVCOUNT)
- PHR error counter (BBPHRERRCOUNT)
- Number-of-successful-receptions counter (BBRCVOKCOUNT)
- Number-of-unsuccessful-receptions counter (BBRCVNGCOUNT)
- Frame synchronization power value result register (BBFSYNCPOWRSLT)
- Frame synchronization power value result 2 register (BBFSYNCPOWRSLT2)
- CCA data rate control register (BBCCARATECON)
- FSK control register 0 (BBFSKCON0)
- FSK control register 1 (BBFSKCON1)
- FSK control register 2 (BBFSKCON2)
- FSKFEC control register (BBFSKFECCON)
- Preamble length setting register (BBPAMBL)
- Preamble setting register (BBPABL)
- TXSFD setting register (BBTXSFD)
- TXSFD setting register 2 (BBTXSFD2)
- TXSFD setting register 3 (BBTXSFD3)
- TXSFD setting register 4 (BBTXSFD4)
- SHR control register (BBSHRCON)
- RXSFD setting register (BBRXSFD)
- RXSFD setting register 2 (BBRXSFD2)
- RXSFD setting register 3 (BBRXSFD3)

- RXSFD setting register 4 (BBRXSFD4)
- Mode switch frame transmission register (BBTXMODESW)
- Mode switch frame reception register (BBRXMODESW)
- Mode switch status register (BBMSSTATE)
- Mode switch frame control register (BBMSCON)
- FSKCCA level threshold setting register (BBFSKCCAVTH)
- FSK reception level threshold setting register (BBFSKLVLVTH)
- FSKPHR reception register (BBFSKPHRRX)
- OFDM control register (BBOFDMCON)
- OFDMPHR transmission register 0 (BBOFDMPHRTX0)
- OFDMPHR transmission register 1 (BBOFDMPHRTX1)
- OFDMPHRACK reply register 0 (BBOFDMPHRACK0)
- OFDMPHRACK reply register 1 (BBOFDMPHRACK1)
- OFDMPHR reception register 0 (BBOFDMPHRRX0)
- OFDMPHR reception register 1 (BBOFDMPHRRX1)
- OFDMPHR reception register 2 (BBOFDMPHRRX2)
- OFDMCCA level threshold setting register (BBOFDMCCAVTH)
- OFDM reception level threshold setting register (BBOFDMLVLVTH)
- Port direction register 0 (GPIODIR0)
- Port direction register 1 (GPIODIR1)
- Port data register 0 (GPIODATA0)
- Port data register 1 (GPIODATA1)
- Port output driving capability switching register 0 (GPIODRV0)
- Port output driving capability switching register 1 (GPIODRV1)
- Pull-up/pull-down selection register 0 (PULLSEL0)
- Pull-up/pull-down selection register 1 (PULLSEL1)
- Pull-up/pull-down selection register 2 (PULLSEL2)
- Pull-up/pull-down selection register 3 (PULLSEL3)
- GPIO function selection register 0 (BBGPIOFUNCSEL0)
- GPIO function selection register 1 (BBGPIOFUNCSEL1)
- GPIO function selection register 2 (BBGPIOFUNCSEL2)
- GPIO function selection register 3 (BBGPIOFUNCSEL3)
- GPIO function selection register 4 (BBGPIOFUNCSEL4)
- GPIO function selection register 5 (BBGPIOFUNCSEL5)
- GPIO function selection register 6 (BBGPIOFUNCSEL6)
- RX-state OSC setting register (BBRXOSC)

- NEWMODE transmission control register (BBNMTXCON)
- NEWMODE Transmission SX shift frequency setting register (BBNMTXSXSFTFREQ)
- NEWMODE transmission frequency setting register (BBNMTXFREQ)
- NEWMODE transmission FSK control register 0 (BBNMTXFSKCON0)
- NEWMODE transmission FSK control register 1 (BBNMTXFSKCON1)
- NEWMODE transmission FSK preamble length setting register (BBMSPAMBL)
- NEWMODE reception control register 0 (BBNMRXCON0)
- NEWMODE reception control register 1 (BBNMRXCON1)
- NEWMODE reception control register 2 (BBNMRXCON2)
- NEWMODE reception frequency setting register (BBNMRXBBFREQ)
- NEWMODE reception FSK control register 0 (BBNMRXFSKCON0)
- NEWMODE reception FSK control register 1 (BBNMRXFSKCON1)
- NEWMODE reception OFDM control register (BBNMRXOFDMCON)
- Version code read control register (VERCNT)
- Version registers (VERR0 to VERR7)

3.4.1 RF start register (BBRFCON)

The RF function is enabled by setting the RF function enable bit to 1. Calibration is enabled by setting the calibration control bit to 1. Clear this bit to 0 after calibration is completed. The register access area switch bit switches the area to be allocated to addresses 0600H to 0FFFH as shown in Figure 3 - 7. Transition to the STANDBY state is allowed by the STANDBY transition enable bit. Set this bit to 1 to make a transition from the IDLE state to the STANDBY state. The value of this register following a reset is 01H.

Figure 3 - 6 Format of RF Start Register (BBRFCON)

Address: 0000H After reset: 01H R/W

Symbol	7	6	5	4	3	2	1	0
BBRFCON	0	0	STANDBY EN	0	REG ACCESS	CSONSET	0	RFSTART

STANDBY EN	STANDBY transition enable
0	Transition to the STANDBY state is allowed. Set this bit to 1 to move from the IDLE state to the STANDBY state.
1	

REG ACCESS	Register access area switch
0	The area allocated to addresses 0600H to 0FFFH is switched.
1	

CSONSET	Calibration control
0	Calibration is disabled.
1	Calibration is enabled.

RFSTART	RF function enable
0	RF function is disabled.
1	RF function is enabled.

Caution When writing to this register, set bits 7, 6, 4, and 1 to the value 0.

Figure 3 - 7 Areas Switched by the Register Access Area Switch Bit

<table>
<tr><th colspan="9">Address</th><th>Register access area switch bit = 0</th><th>Register access area switch bit = 1</th></tr>
<tr><td>0 0 0 0</td><td>to</td><td>0 0 F F</td><td colspan="2" rowspan="6">Register area (no bank)</td></tr>
<tr><td>0 1 0 0</td><td>to</td><td>0 1 F F</td></tr>
<tr><td>0 2 0 0</td><td>to</td><td>0 2 F F</td></tr>
<tr><td>0 3 0 0</td><td>to</td><td>0 3 F F</td></tr>
<tr><td>0 4 0 0</td><td>to</td><td>0 4 F F</td></tr>
<tr><td>0 5 0 0</td><td>to</td><td>0 5 F F</td></tr>
<tr><td>0 6 0 0</td><td>to</td><td>0 6 F F</td><td rowspan="12">Register area (bank 0)</td><td>Register area (bank 1)</td></tr>
<tr><td>0 7 0 0</td><td>to</td><td>0 7 F F</td></tr>
<tr><td>0 8 0 0</td><td>to</td><td>0 8 F F</td><td rowspan="11">Transmission/reception RAM (2 Kbytes)

Write access = Transmission RAM values
Read access = Reception RAM values</td></tr>
<tr><td>0 9 0 0</td><td>to</td><td>0 9 F F</td></tr>
<tr><td>0 A 0 0</td><td>to</td><td>0 A F F</td></tr>
<tr><td>0 B 0 0</td><td>to</td><td>0 B F F</td></tr>
<tr><td>0 C 0 0</td><td>to</td><td>0 C F F</td></tr>
<tr><td>0 D 0 0</td><td>to</td><td>0 D F F</td></tr>
<tr><td>0 E 0 0</td><td>to</td><td>0 E F F</td></tr>
<tr><td>0 F 0 0</td><td>to</td><td>0 F F F</td></tr>
</table>

3.4.2 Transmission and reception reset register (BBTXRXRST)

This register is used to stop the RF communications. The processes of transmission, reception, CCA, and calibration can be stopped by setting the RF communication stop bit to 1. This device enters the IDLE state after the stop. The processes of automatic ACK reply and the automatic receive switch mode function are also canceled. Note that 0 is always read from this bit. However, the values of the other registers are retained. The value of this register following a reset is 00H.

Figure 3 - 8 Format of Transmission and Reception Reset Register (BBTXRXRST)

Address: 0001H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBTXRXRST	0	0	0	0	0	0	0	RFSTOP

RFSTOP	RF communication stop
0	Even though the RF communications are enabled, nothing proceeds.
1	The RF communications are stopped. This device enters the IDLE state after the stop.

Caution When writing to this register, set bits 7 to 1 to the value 0.

3.4.3 Transmission and reception mode register 0 (BBTXRXMODE0)

This register is used to set various modes of the RF transmission and reception. The automatic ACK mode enable bit selects whether to proceed the automatic ACK reply operation after the completion of reception. The automatic receive switch mode 0 enable bit enables the automatic transition to the receive state after the completion of transition. The automatic receive switch mode 1 enable bit enables the automatic transition to the receive state after the completion of reception. Note that the ACK reply operation takes precedence over the receive operation if the automatic ACK mode enable bit is set to 1 (enabled) and the conditions for returning ACK are satisfied. The battery life extension mode, which is a condition for branching in the CSMA-CA processing, can be enabled by the battery life extension mode bit. The beacon mode bit is used to switch between the non-beacon mode and beacon mode. The intraPAN enable bit enables or disables the intraPAN bit in the received frame when the address filter is enabled. The value of this register following a reset is 00H.

Figure 3 - 9 Format of Transmission and Reception Mode Register 0 (BBTXRXMODE0)

Address: 0002H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBTXRXMODE0	INTRAPANEN	BEACON	BATLIFEEXT	AUTORCV1	AUTORCV0	AUTOACKEN	0	0

INTRAPANEN	intraPAN enable
0	intraPAN is disabled.
1	intraPAN is enabled.

BEACON	Beacon mode
0	Non-beacon mode
1	Beacon mode

BATLIFEEXT	Battery life extension mode
0	Battery life extension mode is disabled.
1	Battery life extension mode is enabled.

AUTORCV1	Automatic receive switch mode 1 enable (reception → reception)
0	Automatic switch to reception is disabled.
1	Automatic switch to reception is enabled.

AUTORCV0	Automatic receive switch mode 0 enable (transmission → reception)
0	Automatic switch to reception is disabled.
1	Automatic switch to reception is enabled.

AUTOACKEN	Automatic ACK mode enable
0	Automatic ACK reply is disabled.
1	Automatic ACK reply is enabled.

Caution When writing to this register, set bits 1 and 0 to the value 0.

3.4.4 Transmission and reception mode register 1 (BBTXRXMODE1)

This register is used to set various modes of the RF transmission and reception. The ACK reply frame version setting enable bit switches the value of the frame version for automatic ACK reply between the version of the received frame and the value of the ACK reply frame version setting bits 0 and 1. The ACK reply frame version setting bits 0 and 1 are respectively used to set the values of bits 12 and 13 of the frame version for automatic ACK reply when the ACK reply frame version setting enable bit is set to 1. The sequence number suppress enable bit enables or disables the sequence number suppress in the received frame. While sequence number suppression is enabled by this bit, the sequence number is omitted from the ACK frame in automatic ACK reply when no sequence number is present in the received frame. The ACK receive point setting bit is used to select whether ACK reception in the ACK receive wait time is detected upon completion of the reception or upon reception of the PHR. The value of this register following a reset is C0H.

Figure 3 - 10 Format of Transmission and Reception Mode Register 1 (BBTXRXMODE1)

Address: 0003H After reset: C0H R/W

Symbol	7	6	5	4	3	2	1	0
BBTXRX MODE1	ACKRCV POINT	SQCNUM SUPEN	ACKFV1	ACKFV0	ACKFVEN	0	0	0

ACKRCV POINT	ACK receive point setting
0	ACK reception is recognized upon completion of the reception.
1	ACK reception is recognized upon reception of the PHR.

SQCNUM SUPEN	Sequence number suppress enable
0	Sequence number suppression is enabled.
1	Sequence number suppression is disabled.

ACKFV1	ACK reply frame version setting 1
0	Frame version bit 13 = 0
1	Frame version bit 13 = 1

ACKFV0	ACK reply frame version setting 0
0	Frame version bit 12 = 0
1	Frame version bit 12 = 1

ACKFVEN	ACK reply frame version setting enable
0	Value of the Frame Version field in the received frame
1	Value of the ACK reply frame version setting bits 0 and 1

Caution When writing to this register, set bits 2 to 0 to the value 0.

3.4.5 RXIDLE mode register (BBRXIDLE)

The RXIDLE mode bit is used to place this device in the RX_IDLE state. Set this bit to 1 while the device is in the RX state. To move from the RX_IDLE state to the RX state, clear this bit to 0. Do not make a transition from the RX_IDLE state to the TX state or CCA state. The RF communication stop bit must not be set to 1 in the RX_IDLE state. The value of this register following a reset is 00H.

Figure 3 - 11 Format of RXIDLE Mode Register (BBRXIDLE)

Address: 0004H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBRXIDLE	0	0	0	0	0	0	0	RXIDLE MODE

RXIDLE MODE	RXIDLE mode
0	Normal operation
1	RX_IDLE state

Caution When writing to this register, set bits 7 to 1 to the value 0.

3.4.6 High-speed reception switching mode register (BBRXMODE)

The HISPRX mode bit is used to place this device directly in the receive wait state without going through the IDLE state when reception is stopped and then the receive wait state is automatically entered.

0: RX state → Stop trigger → IDLE state → RX state

1: RX state → Stop trigger → RX state

The high-speed reception switch is effective in any of the following cases.

- Transition to the receive wait state after a frame is discarded by the address filter function
- Transition to the receive wait state after a frame is discarded due to the illegal frame length
- Transition to the receive wait state after a frame is discarded by the receive level filter function
- Transition to the receive wait state after a frame is discarded by the reception overwriting function
- Transition to the receive wait state after reception is abandoned due to the detection of a reception level error, that is, a communications error such as no signal being received during frame reception.
- Transition to the receive wait state after an HCS error (for OFDM modulation)
- Transition to the receive wait state after reception is canceled while reception is prohibited
- Transition to the receive wait state after a mode switch frame is discarded (for FSK modulation)
- Transition to the receive wait state when automatic switch to reception is enabled by automatic receive switch mode bit 1

The value of this register following a reset is 00H.

Figure 3 - 12 Format of High-Speed Reception Switching Mode Register (BBRXMODE)

Address: 0005H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBRX MODE	0	0	0	0	0	0	0	HISPRX MODE

HISPRX MODE	HISPRX mode
0	Receive state is entered via the IDLE state.
1	Receive state is directly entered without going through the IDLE state.

Caution When writing to this register, set bits 7 to 1 to the value 0.

3.4.7 Enhanced ACK mode register (BBEACKMODE)

This register is used to set the enhanced ACK mode. The value of this register following a reset is 01H.

Figure 3 - 13 Format of Enhanced ACK Mode Register (BBEACKMODE)

Address: 0006H After reset: 01H R/W

Symbol	7	6	5	4	3	2	1	0
BBEACK MODE	0	0	0	0	0	0	0	ENHACK MODE

ENHACK MODE	Enhanced ACK mode
0	Enhanced ACK mode is disabled.
1	Enhanced ACK mode is enabled.

Caution When writing to this register, set bits 7 to 1 to the value 0.

3.4.8 Transmission and reception status register 0 (BBTXRXST0)

This register holds various information on the states of the RF transmission and reception. The CCA judge result is stored in bit 0. The CRC judge result is stored in bit 1. The CRC result corresponding to the save bank specified by the receive data save bank select bit is read from this bit. The CSMA-CA judge result is stored in bit 2. Only 0 can be written to this bit. The result of transmission and reception sequence (CSMA-CA → transmission → ACK reception → retransmission → ACK reception, and so on) is stored in the transmission and reception completion judge result bit when the sequence is completed. This device reports "Not completed" when ACK is not received even after the sequence from the transmission to the ACK reception is repeated the specified number of times. Only 0 can be written to this bit. The reception RAM bank 0 status bit and reception RAM bank 1 status bit can be used as flags of data capturing in the respective reception RAM banks 0 and 1. Each flag is automatically set to 1 upon completion of data reception in the respective RAM. After reading data from the reception RAM, clear the flag to 0 by software. Only 0 can be written to clear these flags; set to 1 when writing to the other bits of this register. A receive overrun interrupt occurs when a frame is received again and written to a reception RAM bank while the flag for the respective RAM is set to 1. The reception pending bit holds the data of the pending bit in the received ACK data upon completion of the reception of ACK data only. The reception RAM bank pointer bit is used to check which reception RAM bank has completed data reception. The bit is set to 1 after a reset. The value of the bit changes when a reception RAM bank becomes full or when frame reception is completed. The value of this register following a reset is 80H.

Figure 3 - 14 Format of Transmission and Reception Status Register 0 (BBTXRXST0)

Address: 0007H After reset: 80H R/W[Note]

Symbol	7	6	5	4	3	2	1	0
BBTXRXST0	RCVRAMST	RCVPEND	RCVBANK1	RCVBANK0	TRNRCVSQC	CSMACA	CRC	CCA

RCVRAMST	Reception RAM bank pointer
0	Reception RAM bank 0
1	Reception RAM bank 1

RCVPEND	Reception pending
0	Pending bit is not set.
1	Pending bit is set.

RCVBANK1	Reception RAM bank 1 status
0	Reception is enabled.
1	Data have been stored in the RAM.

RCVBANK0	Reception RAM bank 0 status
0	Reception is enabled.
1	Data have been stored in the RAM.

TRNRCVSQC	Transmission and reception completion judge result
0	Completed
1	Not completed

CSMACA	CSMA-CA judge result
0	Passed
1	Failed

CRC	CRC judge result
0	Successful reception
1	Unsuccessful reception

CCA	CCA judge result
0	The frequency channel is cleared.
1	The frequency channel is busy.

Note: Bits 7, 6, 1, and 0 are read-only.

3.4.9 Transmission and reception mode register 2 (BBTXRXMODE2)

This register is used to set various modes of the RF transmission and reception. The automatic CRC disable bit selects whether to add the result of automatic CRC calculation to the transmit data or send RAM data only. The frame pending setting bit sets the value of the frame pending bit in the ACK data to be returned when the first address match is detected. The information selected by this bit is included in the ACK data in automatic ACK reply. The frame pending status bit indicates whether the ACK has been returned with frame pending enabled in automatic ACK reply. This value is updated at the same time as the occurrence of an interrupt request upon completion of transmission. As the results of automatic ACK reply are retained for individual receive data save banks, the information on the frame pending in ACK reply for the save bank selected by the receive data save bank select bit is read from this bit. The enhanced ACK enable bit enables or disables the enhanced ACK reply function. The retransmission count bits are used to set the maximum number or retransmissions until ACK is received when the automatic ACK receive mode is enabled. Set a value from 0000B to 1000B. The value of this register following a reset is 30H.

Figure 3 - 15 Format of Transmission and Reception Mode Register 2 (BBTXRXMODE2)

Address: 0009H After reset: 30H R/W[Note]

Symbol	7	6	5	4	3	2	1	0
BBTXRXMODE2	RETRN3	RETRN2	RETRN1	RETRN0	ENHACKEN	FLMPENDST	FLMPEND	NOCRC

RETRN3 to RETRN0	Retransmission count (A value from 0000B to 1000B is specifiable.)

ENHACKEN	Enhanced ACK enable
0	Enhanced ACK reply is disabled.
1	Enhanced ACK reply is enabled.

FLMPENDST	Frame pending status
0	Frame pending bit is cleared.
1	Frame pending bit is set.

FLMPEND	Frame pending setting
0	Frame pending bit = 0
1	Frame pending bit = 1

NOCRC	Automatic CRC disable
0	Enabled, i.e., the result of CRC calculation is transmitted.
1	Disabled, i.e., data on the RAM are transmitted.

Note: Bit 2 is read-only.

3.4.10 Transmission and reception mode register 3 (BBTXRXMODE3)

This register is used to set various modes of the RF transmission and reception. The address filter enable bit enables the address filter function for reception. Setting this bit to 1 enables the address filter for the first address. The PAN coordinator bit selects whether the received address matches the PAN coordinator address as an address filter condition for the first address. The receive level filter enable bit enables reception of only the input level equal to or higher than the threshold specified in the FSK reception level threshold setting register or OFDM reception level threshold setting register. The receive data save bank select bit specifies the save bank from which the data related to reception are read (except for the reception RAM data). The reception RAM overwrite enable bit controls overwriting to the reception RAM. If write access to a reception RAM is attempted while this bit is 0 and the respective reception RAM bank n status bit is 1, the reception RAM is not overwritten by the received data. If write access to a reception RAM is attempted while this enable bit is 1, the reception RAM is overwritten by the received data even when the reception RAM bank n status bit is 1. The address filter address extension bit is used to specify whether the second address is used as a condition of the address filter in addition to the first address. The address filter general mode bit selects the general mode for the address filter operation. The value of this register following a reset is 00H.

Figure 3 - 16 Format of Transmission and Reception Mode Register 3 (BBTXRXMODE3)

Address: 000AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBTXRX MODE3	ADFGEN MODE	ADFEXTEN	RCVOVERW REN	RCVBANK SEL	0	LVLFILEN	PANCORD	ADRSFILEN

ADFGEN MODE	Address filter general mode
0	WiSUN mode
1	General mode

ADFEXTEN	Address filter address extension
0	PAN ID and address extension are disabled.
1	PAN ID and address extension are enabled.

RCVOVERW REN	Reception RAM overwrite enable
0	Overwriting is disabled.
1	Overwriting is enabled.

RCVBANK SEL	Receive data save bank select
0	Receive data save bank 0 is selected.
1	Receive data save bank 1 is selected.

LVLFILEN	Receive level filter enable
0	Filter is disabled.
1	Filter is enabled.

PANCORD	PAN coordinator
0	The address is not for the PAN coordinator.
1	The address is for the PAN coordinator.

ADRSFILEN	Address filter enable
0	Address filter is disabled.
1	Address filter is enabled.

Caution When writing to this register, set bit 3 to the value 0.

3.4.11 Transmission and reception status register 1 (BBTXRXST1)

The receive data save bank pointer bit indicates the bank that holds the data related to the received frame such as the frame length. The value of this register following a reset is 02H.

Figure 3 - 17 Format of Transmission and Reception Status Register 1 (BBTXRXST1)

Address: 000BH After reset: 0000001XB R

Symbol	7	6	5	4	3	2	1	0
BBTXRXST1	0	0	0	0	0	0	RCVSTORE ST	X

RCVSTORE ST	Receive data save bank pointer
0	Receive data save bank 0
1	Receive data save bank 1

Caution An undefined value (X) is read from bit 0.

3.4.12 Transmission and reception control register (BBTXRXCON)

This register is used to control the RF transmission and reception. Setting the receive trigger bit to 1 starts warm-up of the RF circuit. Reception becomes ready in 185 µs. Setting the transmit trigger bit to 1 starts warm-up of the RF circuit. Transmission begins in 335 µs. Setting the CCA trigger bit to 1 starts warm-up of the RF circuit. The CCA operation begins in 185 µs. To proceed CCA, specify a value other than 0H in the BEMIN bits. Be sure to set these bits in the IDLE state. Note that each bit is automatically cleared to 0 upon completion of the respective operation (transmission, reception, or CCA). To stop reception while it is in progress, use the RF communication stop bit. Do not stop transmission before it is completed. The automatic ACK receive mode bit selects whether to proceed the automatic ACK receive operation. The value of this register following a reset is 00H.

Figure 3 - 18 Format of Transmission and Reception Control Register (BBTXRXCON)

Address: 000CH After reset: 00H R/W[Note]

Symbol	7	6	5	4	3	2	1	0
BBTXRXCON	0	0	0	0	ACKRCVEN	CCATRG	TRNTRG	RCVTRG

ACKRCVEN	Automatic ACK receive mode
0	Automatic ACK receive operation is disabled.
1	Automatic ACK receive operation is enabled.

CCATRG	CCA trigger
0	Nothing proceeds.
1	CCA is started.

TRNTRG	Transmit trigger
0	Nothing proceeds.
1	Transmission is started.

RCVTRG	Receive trigger
0	Nothing proceeds.
1	Reception is started.

Note: Bits 2 to 0 are write-only.

Caution When writing to this register, set bits 7 to 4 to the value 0.

3.4.13 CSMA control register 0 (BBCSMACON0)

This register is used to control the CSMA-CA operation. Setting the automatic CSMA-CA start bit to 1 starts the CSMA-CA operation. Be sure to set this bit in the IDLE state. Note that this bit is automatically cleared to 0 upon completion of the CSMA-CA operation. This bit cannot be cleared by writing 0 to it. To stop the CSMA-CA operation while it is in progress, use the RF communication stop bit. Setting the transmission-after-automatic-CSMA-CA bit to 1 automatically starts transmission when the frequency channel is cleared in accordance with the CCA judge result after the completion of the CSMA-CA operation. Setting the reception-during-CSMA-CA enable bit to 1 enables reception during the wait time in the CCA operation in the CSMA-CA operation. Counting of the backoff period stops while a frame is being received. The unicast frame bit is used to set the unicast frame value. The function of this bit is enabled by setting the unicast frame enable bit to 1. The wait time until transmission after CCA can be minimized by setting the transmission-after-automatic-CSMA-CA mode bit to 1. The value of this register following a reset is 00H.

Figure 3 - 19 Format of CSMA Control Register 0 (BBCSMACON0)

Address: 000DH After reset: 00H R/W[Note]

Symbol	7	6	5	4	3	2	1	0
BBCSMACON0	0	0	CSMATRNMODE	UNICASTFRM	0	CSMARCVEN	CSMATRNST	CSMAST

CSMATRNMODE	Transmission-after-automatic-CSMA-CA mode
0	Wait timer is inserted (normal operation).
1	Wait time is minimized.

UNICASTFRM	Unicast frame
0	Unicast frame value = 0
1	Unicast frame value = 1

CSMARCVEN	Reception-during-CSMA-CA enable
0	Reception is disabled.
1	Reception is enabled.

CSMATRNST	Transmission-after-automatic-CSMA-CA
0	Nothing proceeds.
1	Transmission proceeds after CSMA-CA.

CSMAST	Automatic CSMA-CA start
0	Nothing proceeds.
1	CSMA-CA is automatically started.

Note: Bit 0 is write-only.

Caution When writing to this register, set bits 7, 6, and 3 to the value 0.

3.4.14 Transmission and reception status register 2 (BBTXRXST2)

This register holds various information on the states of the RF transmission and reception. The reception RAM bank flag indicates the reception RAM bank used at the start of the reception. The receive data save bank flag indicates the receive data save bank at the start of the reception. The value of this register following a reset is 03H.

Figure 3 - 20 Format of Transmission and Reception Status Register 2 (BBTXRXST2)

Address: 0010H After reset: 03H R

Symbol	7	6	5	4	3	2	1	0
BBTXRXST2	0	0	0	0	0	0	RCVSTOREFLG	RCVBANKFLG

RCVSTOREFLG	Receive data save bank flag
0	Receive data save bank 0
1	Receive data save bank 1

RCVBANKFLG	Reception RAM bank flag
0	Reception RAM bank 0
1	Reception RAM bank 1

3.4.15 Transmission and reception mode register 4 (BBTXRXMODE4)

The automatic-receive-with-timeout-after-transmission enable bit is used to specify whether to use the timeout function in the automatic receive operation after transmission when the automatic receive operation is enabled by the automatic receive switch mode 0 enable bit. The value of this register following a reset is 00H.

Figure 3 - 21 Format of Transmission and Reception Mode Register 4 (BBTXRXMODE4)

Address: 0011H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBTXRX MODE4	0	0	0	0	0	0	0	TIMEOUT RCV

TIMEOUT RCV	Automatic-receive-with-timeout-after-transmission enable
0	Normal automatic receive mode
1	Automatic receive mode with timeout function

Caution When writing to this register, set bits 7 to 1 to the value 0.

3.4.16 CSMA control register 1 (BBCSMACON1)

This register is used to control the CSMA-CA operation. The macMaxCSMABackoff value is specified in the NB bits. Set a value from 0H to 5H. The CW value is specified in the CW bits. Set a value from 1H to 3H. The value of this register following a reset is 20H.

Figure 3 - 22 Format of CSMA Control Register 1 (BBCSMACON1)

Address: 0012H After reset: 20H R/W

Symbol	7	6	5	4	3	2	1	0
BBCSMACON1	0	0	CW1	CW0	0	NB2	NB1	NB0

CW1, CW0	CW value

NB2 to NB0	macMaxCSMABackoff value

Caution When writing to this register, set bits 7, 6, and 3 to the value 0.

3.4.17 CSMA control register 2 (BBCSMACON2)

This register is used to control the CSMA-CA operation. The macMaxBE value is specified in the BEMAX bits. Set the BEMAX bits to a greater value than that of the BEMIN bits. The maximum value is EH. The MacMinBE control bit selects whether to proceed the CCA operation when macMinBE is set to 000b, which is a parameter of automatic CSMA-CA. The unicast frame enable bit enables the operation specified by the unicast frame bit. The value of this register following a reset is 05H.

Figure 3 - 23 Format of CSMA Control Register 2 (BBCSMACON2)

Address: 0013H After reset: 05H R/W

Symbol	7	6	5	4	3	2	1	0
BBCSMACON2	0	0	UNICASTFRMEN	MACMINBECON	BEMAX3	BEMAX2	BEMAX1	BEMAX0

UNICASTFRMEN	Unicast frame enable
0	Unicast frame is disabled.
1	Unicast frame is enabled.

MACMINBECON	MacMinBE control
0	CCA operation does not proceed.
1	CCA operation proceeds.

BEMAX3 to BEMAX0	MacMaxBE value

Caution When writing to this register, set bits 7 and 6 to the value 0.

3.4.18 PAN identifier register 0 (BBPANID0)

This register is used to set the PAN identifier as a condition for filtering of the first address. It consists of 16 bits and the specified value is compared with the received PAN identifier to detect an address match. Set a value from 0000H to FFFFH in this register. The value of this register following a reset is FFFFH.

Figure 3 - 24 Format of PAN Identifier Register 0 (BBPANID0)

Address: 0015H, 0014H After reset: FFFFH R/W

Symbol	15	14	13	12	11	10	9	8
BBPANID0 (0015H)	PANID015	PANID014	PANID013	PANID012	PANID011	PANID010	PANID09	PANID08
	7	6	5	4	3	2	1	0
(0014H)	PANID07	PANID06	PANID05	PANID04	PANID03	PANID02	PANID01	PANID00

PANID015 to PANID00	PAN identifier

3.4.19 Short address register 0 (BBSHORTAD0)

This register is used to set the short address as a condition for filtering of the first address. It consists of 16 bits and the specified value is compared with the received short address to detect an address match. Set a value from 0000H to FFFFH in this register. The value of this register following a reset is FFFFH.

Figure 3 - 25 Format of Short Address Register 0 (BBSHORTAD0)

Address: 0017H, 0016H After reset: FFFFH R/W

Symbol	15	14	13	12	11	10	9	8
BBSHORTAD0 (0017H)	SHORTAD015	SHORTAD014	SHORTAD013	SHORTAD012	SHORTAD011	SHORTAD010	SHORTAD09	SHORTAD08
	7	6	5	4	3	2	1	0
(0016H)	SHORTAD07	SHORTAD06	SHORTAD05	SHORTAD04	SHORTAD03	SHORTAD02	SHORTAD01	SHORTAD00

SHORTAD015 to SHORTAD00	Short address

3.4.20 Extended address registers 0 (BBEXTENDAD00 to BBEXTENDAD03)

These registers are used to set the extended address as a condition for filtering of the first address. Four 16-bit registers are provided to specify a 64-bit address and the specified value is compared with the received extended address to detect an address match. Set a value from 0000H to FFFFH in these registers. The value of these registers following a reset is 0000H.

Figure 3 - 26 Format of Extended Address Registers 0 (BBEXTENDAD00 to BBEXTENDAD03) (1/2)

Address: 001FH, 001EH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBEXTENDAD03 (001FH)	EXTENDAD0315	EXTENDAD0314	EXTENDAD0313	EXTENDAD0312	EXTENDAD0311	EXTENDAD0310	EXTENDAD039	EXTENDAD038
	7	6	5	4	3	2	1	0
(001EH)	EXTENDAD037	EXTENDAD036	EXTENDAD035	EXTENDAD034	EXTENDAD033	EXTENDAD032	EXTENDAD031	EXTENDAD030

EXTENDAD0315 to EXTENDAD030	Bits 63 to 48 of extended address

Address: 001DH, 001CH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBEXTENDAD02 (001DH)	EXTENDAD0215	EXTENDAD0214	EXTENDAD0213	EXTENDAD0212	EXTENDAD0211	EXTENDAD0210	EXTENDAD029	EXTENDAD028
	7	6	5	4	3	2	1	0
(001CH)	EXTENDAD027	EXTENDAD026	EXTENDAD025	EXTENDAD024	EXTENDAD023	EXTENDAD022	EXTENDAD021	EXTENDAD020

EXTENDAD0215 to EXTENDAD020	Bits 47 to 32 of extended address

Figure 3 - 26 Format of Extended Address Registers 0 (BBEXTENDAD00 to BBEXTENDAD03) (2/2)

Address: 001BH, 001AH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBEXTENDAD01 (001BH)	EXTENDAD0115	EXTENDAD0114	EXTENDAD0113	EXTENDAD0112	EXTENDAD0111	EXTENDAD0110	EXTENDAD019	EXTENDAD018
	7	6	5	4	3	2	1	0
(001AH)	EXTENDAD017	EXTENDAD016	EXTENDAD015	EXTENDAD014	EXTENDAD013	EXTENDAD012	EXTENDAD011	EXTENDAD010

EXTENDAD0115 to EXTENDAD010	Bits 31 to 16 of extended address

Address: 0019H, 0018H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBEXTENDAD00 (0019H)	EXTENDAD0015	EXTENDAD0014	EXTENDAD0013	EXTENDAD0012	EXTENDAD0011	EXTENDAD0010	EXTENDAD009	EXTENDAD008
	7	6	5	4	3	2	1	0
(0018H)	EXTENDAD007	EXTENDAD006	EXTENDAD005	EXTENDAD004	EXTENDAD003	EXTENDAD002	EXTENDAD001	EXTENDAD000

EXTENDAD0015 to EXTENDAD000	Bits 15 to 0 of extended address

3.4.21 Timer read registers 0 and 1 (BBTIMEREAD0 and BBTIMEREAD1)

These registers are used to read the current value of the 32-bit timer. Be sure to start reading from the lowest-order byte. The counted value is latched when the lowest-order byte at address 0020H is read, so continue by reading the higher-order bytes. When the value read from the lowest-order byte at address 0020H is 00H, re-read from the lowest-order byte at the given address. Note that re-reading from the lowest-order byte should be done before the counter has counted to 256 so that the value of the lowest-order byte becomes 00H. The value of these registers following a reset is 0000H.

Figure 3 - 27 Format of Timer Read Register 0 (BBTIMEREAD0)

Address: 0021H, 0020H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8
BBTIMEREAD0 (0021H)	TIMEREAD015	TIMEREAD014	TIMEREAD013	TIMEREAD012	TIMEREAD011	TIMEREAD010	TIMEREAD09	TIMEREAD08
	7	6	5	4	3	2	1	0
(0020H)	TIMEREAD07	TIMEREAD06	TIMEREAD05	TIMEREAD04	TIMEREAD03	TIMEREAD02	TIMEREAD01	TIMEREAD00

TIMEREAD015 to TIMEREAD00	Lower-order bits of 32-bit timer value (bits 15 to 0)

Figure 3 - 28 Format of Timer Read Register 1 (BBTIMEREAD1)

Address: 0023H, 0022H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8
BBTIMEREAD1 (0023H)	TIMEREAD115	TIMEREAD114	TIMEREAD113	TIMEREAD112	TIMEREAD111	TIMEREAD110	TIMEREAD19	TIMEREAD18
	7	6	5	4	3	2	1	0
(0022H)	TIMEREAD17	TIMEREAD16	TIMEREAD15	TIMEREAD14	TIMEREAD13	TIMEREAD12	TIMEREAD11	TIMEREAD10

TIMEREAD115 to TIMEREAD10	Higher-order bits of 32-bit timer value (bits 31 to 16)

3.4.22 Timer comparison registers 0 and 1 (BBTCOMP0REG0 to BBTCOMP2REG0 and BBTCOMP0REG1 to BBTCOMP2REG1)

These registers are used to specify the values to be compared with the 32-bit timer. There are three channels of registers. All channels are individually compared with the 32-bit timer. The value of these registers following a reset is 0000H.

Figure 3 - 29 Format of Timer Comparison Registers 0 (BBTCOMPnREG0)

Address: 002DH, 002CH (BBTCOMP2REG0), 0029H, 0028H (BBTCOMP1REG0), 0025H, 0024H (BBTCOMP0REG0)

After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBTCOMPnREG0 (002DH) (0029H) (0025H)	TCOMPn REG015	TCOMPn REG014	TCOMPn REG013	TCOMPn REG012	TCOMPn REG011	TCOMPn REG010	TCOMPn REG09	TCOMPn REG08
	7	6	5	4	3	2	1	0
(002CH) (0028H) (0024H)	TCOMPn REG07	TCOMPn REG06	TCOMPn REG05	TCOMPn REG04	TCOMPn REG03	TCOMPn REG02	TCOMPn REG01	TCOMPn REG00

TCOMPnREG015 to TCOMPnREG00	Lower-order bits of 32-bit comparison value (bits 15 to 0)

Caution n = 0 to 2

Figure 3 - 30 Format of Timer Comparison Registers 1 (BBTCOMPnREG1)

Address: 002FH, 002EH (BBTCOMP2REG1), 002BH, 002AH (BBTCOMP1REG1), 0027H, 0026H (BBTCOMP0REG1)

After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBTCOMPnREG1 (002FH) (002BH) (0027H)	TCOMPn REG115	TCOMPn REG114	TCOMPn REG113	TCOMPn REG112	TCOMPn REG111	TCOMPn REG110	TCOMPn REG19	TCOMPn REG18
	7	6	5	4	3	2	1	0
(002EH) (002AH) (0026H)	TCOMPn REG17	TCOMPn REG16	TCOMPn REG15	TCOMPn REG14	TCOMPn REG13	TCOMPn REG12	TCOMPn REG11	TCOMPn REG10

TCOMPnREG115 to TCOMPnREG10	Higher-order bits of 32-bit comparison value (bits 31 to 16)

Caution n = 0 to 2

3.4.23 Timestamp registers 0 and 1 (BBTSTAMP0 and BBTSTAMP1)

These registers hold the timer count value that is stored when reception of packet data is started or completed or when transmission of packet data is completed. The timestamps of reception and transmission are separately stored, and the stamp value read switch bits are used to select the value to be read from these registers from among the reception start stamp, reception completion stamp, and transmission stamp. The timer value upon starting of the reception is automatically stored as a timestamp and it is retained until the reception of the next packet is started. The timer value upon completion of the reception is automatically stored as a timestamp and it is retained until the reception of the next packet is completed. The timestamp value corresponding to the save bank specified by the receive data save bank select bit is read from these registers. The timer value upon completion of the transmission is automatically stored as another timestamp and it is retained until the transmission of the next packet is completed. However, the transmission timestamp value is not updated during automatic ACK reply. The value of these registers following a reset is 0000H.

Figure 3 - 31 Format of Timestamp Register 0 (BBTSTAMP0)

Address: 0031H, 0030H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8
BBTSTAMP 0 (0031H)	TSTAMP015	TSTAMP014	TSTAMP013	TSTAMP012	TSTAMP011	TSTAMP010	TSTAMP09	TSTAMP08
	7	6	5	4	3	2	1	0
(0030H)	TSTAMP07	TSTAMP06	TSTAMP05	TSTAMP04	TSTAMP03	TSTAMP02	TSTAMP01	TSTAMP00

TSTAMP015 to TSTAMP00	Lower-order bits of 32-bit timer value (bits 15 to 0)

Figure 3 - 32 Format of Timestamp Register 1 (BBTSTAMP1)

Address: 0033H, 0032H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8
BBTSTAMP 1 (0033H)	TSTAMP115	TSTAMP114	TSTAMP113	TSTAMP112	TSTAMP111	TSTAMP110	TSTAMP19	TSTAMP18
	7	6	5	4	3	2	1	0
(0032H)	TSTAMP17	TSTAMP16	TSTAMP15	TSTAMP14	TSTAMP13	TSTAMP12	TSTAMP11	TSTAMP10

TSTAMP115 to TSTAMP10	Higher-order bits of 32-bit timer value (bits 31 to 16)

3.4.24 Timer control register (BBTIMECON)

This register is used to control the timer in this device. The timer count enable bit controls the count operation of the 32-bit timer. Setting this bit to 1 enables the count operation. Clearing it to 0 stops the timer and initializes the timer count value to 00000000H. The COMP0 transmit trigger enable bit enables the start of RF transmission when the timer count value matches the value of the timer comparison registers 0 and 1 (BBTCOMP1REG0 and BBTCOMP1REG1). Transmission starts in 335 µs after the match. Be sure to set this bit in the IDLE state. The stamp timing switch bit selects the timing of getting the stamp of the timer count value. The value is updated upon the start of reception regardless of the address filter function when the start of reception is selected as the stamp timing. The COMP0 trigger select bit selects CSMA-CA as the function to be started when the COMP0 transmit trigger enable bit is enabled. The stamp value read switch bits select the value to be read from the time stamp registers from among the reception start stamp value, reception completion stamp value, and the transmission completion stamp value. The count source switch bit switches the count source for the timer between the prescaler output and the data rate specified in the timing parameter data rate setting register. The COMP0-excess transmission enable bit is used to immediately place this device in the transmission start state if the timer count has already exceeded the comp 0 value when the value is specified in timer comparison registers 0 and 1 (BBTCOMP1REG0 and BBTCOMP1REG1) while the COMP0 transmit trigger enable bit is set (enabled). The value of this register following a reset is 00H.

Figure 3 - 33 Format of Timer Control Register (BBTIMECON)

Address: 0034H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBTIMECON	PASSSTARTEN	CNTSRCSEL	STAMPRDSEL1	STAMPRDSEL0	COMP0TRGSEL	STAMPTIMSEL	COMP0TRG	TIMEEN

PASSSTARTEN	COMP0-excess transmission enable
0	Transmission is disabled.
1	Transmission is enabled.

CNTSRCSEL	Count source switch
0	Prescaler output (1 μs)
1	Data rate specified in the timing parameter data rate setting register

STAMPRDSEL1	STAMPRDSEL0	Stamp value read switch
0	0	Reception start stamp value
0	1	Reception completion stamp value
1	0	Transmission completion stamp value
1	1	

COMP0TRGSEL	COMP0 trigger select
0	Transmit trigger
1	CSMA-CA trigger

STAMPTIMSEL	Stamp timing switch
0	Start of reception
1	Generation of frame length interrupt

COMP0TRG	COMP0 transmit trigger enable
0	Transmit trigger is disabled.
1	Transmit trigger is enabled.

TIMEEN	Timer count enable
0	Counting by the timer is stopped.
1	Counting by the timer is enabled.

3.4.25 Backoff period register (BBBOFFPROD)

This register is used to control the backoff period. The automatic random backoff period enable bit is used to automatically generate random values by using the value specified in the backoff period register 2 as the initial value to set the backoff period value in the CSMA-CA circuit. Set a random value in backoff period register 2 and then set the automatic random backoff period enable bit in the backoff period register to 1. The value of this register following a reset is 00H.

Figure 3 - 34 Format of Backoff Period Register (BBBOFFPROD)

Address: 0035H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBBOFFPROD	0	0	0	0	0	0	0	BOFFPRODEN

BOFFPRODEN	Automatic random backoff period enable
0	Automatic generation of random values is disabled.
1	Automatic generation of random values is enabled.

Caution When writing to this register, set bits 7 to 1 to the value 0.

3.4.26 Timing parameter data rate setting register (BBPARAMRATE)

This register is used to set the data rate for timing parameters such as the count sources of the timer and backoff period. Specify the value corresponding to the desired data rate shown in Table 3 - 2. The extended data rate enable bit enables the setting of the data rate in the extended data rate setting register. The value of this register following a reset is 00H.

Figure 3 - 35 Format of Timing Parameter Data Rate Setting Register (BBPARAMRATE)

Address: 0036H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBPARAMRATE	0	0	0	0	EXTRATEEN	PARAMRATE2	PARAMRATE1	PARAMRATE0

EXTRATEEN	Extended data rate enable
0	Extended data rate is disabled.
1	Extended data rate is enabled.

PARAMRATE2 to PARAMRATE0	Timing parameter data rate setting
—	These bits set the data rate for timing parameters.

Caution When writing to this register, set bits 7 to 4 to the value 0.

Table 3 - 2 Data Rate Setting

Value			Data Rate	Cycle
PARAMRATE2	PARAMRATE1	PARAMRATE0		
0	0	0	1000 kbps	1 µs
0	0	1	100 kchip/s	320 µs
0	1	0	10 kbps	100 µs
0	1	1	20 kbps	50 µs
1	0	0	50 kbps	20 µs
1	0	1	100 kbps	10 µs
1	1	0	150 kbps	6.667 µs
1	1	1	200 kbps	5 µs

3.4.27 Extended data rate setting register (BBEXTRATE)

This register is used to set the value other than those set by the PARAMRATE2 to PARAMRATE0 bits in the timing parameter data rate setting register (BBPARAMRATE). The extended data rate enable bit enables the setting of this register.

Data rate [bps] = (48 MHz / 2) / the extended data rate

The value of this register following a reset is 00F0H.

Figure 3 - 36 Format of Extended Data Rate Setting Register (BBEXTRATE)

Address: 0039H, 0038H After reset: 00F0H R/W

Symbol	15	14	13	12	11	10	9	8
BBEXTRATE (0039H)	EXTRATE 15	EXTRATE 14	EXTRATE 13	EXTRATE 12	EXTRATE 11	EXTRATE 10	EXTRATE 9	EXTRATE 8
	7	6	5	4	3	2	1	0
(0038H)	EXTRATE 7	EXTRATE 6	EXTRATE 5	EXTRATE 4	EXTRATE 3	EXTRATE 2	EXTRATE 1	EXTRATE 0

EXTRATE15 to EXTRATE0	Bits 15 to 0 of the extended data rate

3.4.28 CSMA control register 3 (BBCSMACON3)

This register is used to control the CSMA-CA operation. The macMinBE value is specified in the BEMIN bits. Set the BEMIN bits to a smaller value than that of the BEMAX bits. The minimum value is 0H. To proceed CCA, specify a value other than 0H. The value of this register following a reset is 03H.

Figure 3 - 37 Format of CSMA Control Register 3 (BBCSMACON3)

Address: 003EH After reset: 03H R/W

Symbol	7	6	5	4	3	2	1	0
BBCSMACON3	0	0	0	0	BEMIN3	BEMIN2	BEMIN1	BEMIN0

BEMIN3 to BEMIN0	BEMIN (macMinBE value)

Caution When writing to this register, set bits 7 to 4 to the value 0.

3.4.29 Calibration register (BBCAL)

This register is used to control calibration. Set the calibration start bit to start calibration. The value of this register following a reset is 00H.

Figure 3 - 38 Format of Calibration Register (BBCAL)

Address: 003FH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBCAL	0	0	0	0	0	0	0	CALSTART

CALSTART	Calibration start
0	Nothing proceeds.
1	Calibration is started.

Caution When writing to this register, set bits 7 to 1 to the value 0.

3.4.30 ACK reply time setting register (ACKRTNTIM)

This register is used to set the ACK reply time in the non-beacon mode. Set a value from 0001H to FFFFH in this register. The value of this register following a reset is 0002H.

Figure 3 - 39 Format of ACK Reply Time Setting Register (ACKRTNTIM)

Address: 0047H, 0046H After reset: 0002H R/W

Symbol	15	14	13	12	11	10	9	8
ACKRTNTIM (0047H)	ACKRTNTIM15	ACKRTNTIM14	ACKRTNTIM13	ACKRTNTIM12	ACKRTNTIM11	ACKRTNTIM10	ACKRTNTIM9	ACKRTNTIM8
	7	6	5	4	3	2	1	0
(0046H)	ACKRTNTIM7	ACKRTNTIM6	ACKRTNTIM5	ACKRTNTIM4	ACKRTNTIM3	ACKRTNTIM2	ACKRTNTIM1	ACKRTNTIM0

ACKRTNTIM15 to ACKRTNTIM0	ACK reply time in the non-beacon mode

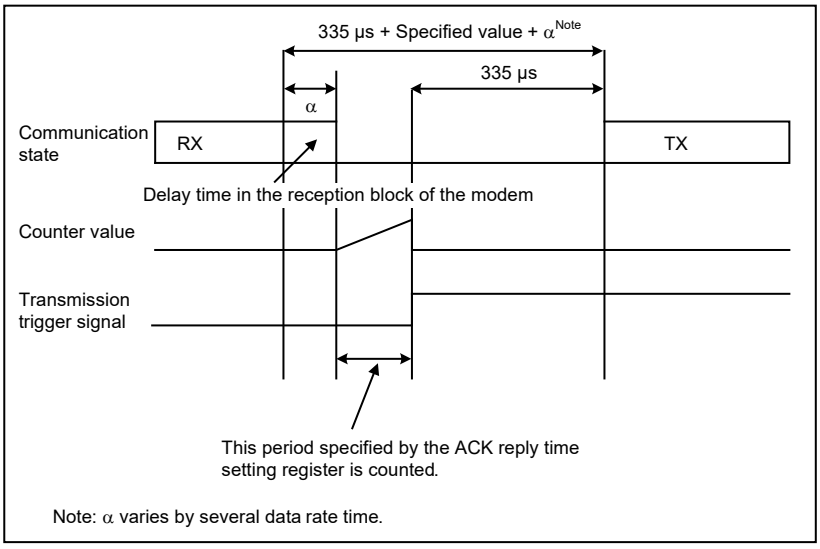
Example of setting: Non-beacon mode

Only use the ACK reply time setting register to set the time from the completion of packet reception to the assertion of the transmission trigger signal. The initial value is 0002H, that is, 2 data rate time[Note]. The setting is possible in 1 data rate time[Note] units (1H = 1 data rate time[Note]).

Note: The rate time depends on the value specified in the timing parameter data rate setting register.

In the non-beacon mode, the 10-bit timer counter for ACK reply mode starts counting from 000H when reception is completed, and the counter stops and the transmission trigger signal is asserted when the timer count reaches the value specified in the ACK reply time setting register.

Figure 3 - 40 Count Operation in the Non-Beacon Mode



3.4.31 Automatic switching to reception comparison register (AUTORCVCNT)

This register is used to set the time until the reception trigger signal is asserted for automatic switching to reception after the completion of transmission or reception when the automatic receive switch mode is specified. The initial value is 000AH, that is, 10 data rate time[Note]. The setting is possible in 1 data rate time[Note] units (1H = 1 data rate time[Note]).

Note: The rate time depends on the value specified in the timing parameter data rate setting register.

Set a value from 0001H to FFFFH in this register. The value of this register following a reset is 000AH.

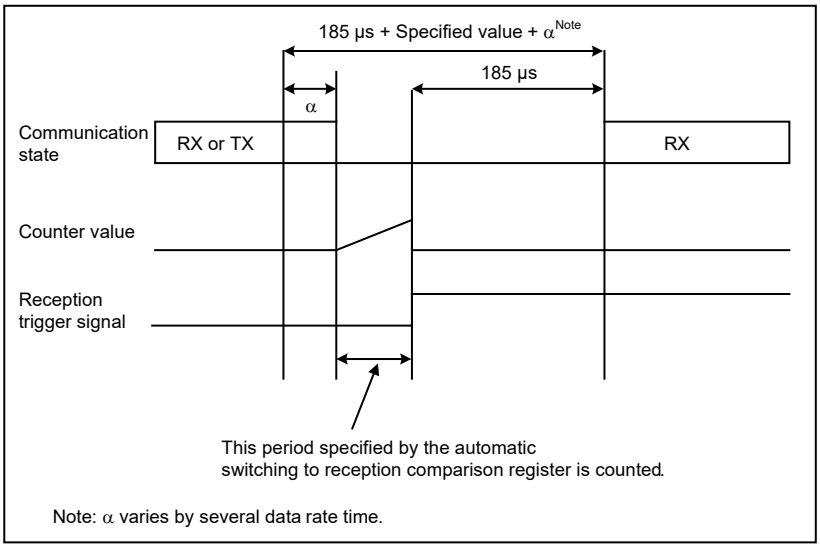
Figure 3 - 41 Format of Automatic Switching to Reception Comparison Register (AUTORCVCNT)

Address: 0049H, 0048H After reset: 000AH R/W

Symbol	15	14	13	12	11	10	9	8
AUTORCV CNT (0049H)	AUTORCV CNT15	AUTORCV CNT14	AUTORCV CNT13	AUTORCV CNT12	AUTORCV CNT11	AUTORCV CNT10	AUTORCV CNT9	AUTORCV CNT8
	7	6	5	4	3	2	1	0
(0048H)	AUTORCV CNT7	AUTORCV CNT6	AUTORCV CNT5	AUTORCV CNT4	AUTORCV CNT3	AUTORCV CNT2	AUTORCV CNT1	AUTORCV CNT0

AUTORCVCNT15 to AUTORCVCNT0	Time until the transmission trigger signal is asserted

Figure 3 - 42 Count Operation Specified by the Automatic Switching to Reception Comparison Register



3.4.32 Backoff cycle register (BOFFPERIOD)

This register is used to set the backoff cycle. The initial value is 0071H, that is, 113 data rate time[Note]. The setting is possible in 1 data rate time[Note] units (1H = 1 data rate time[Note]).

Note: The rate time depends on the value specified in the timing parameter data rate setting register.

Set a value from 000FH to FFFFH in this register. The value of this register following a reset is 0071H.

Figure 3 - 43 Format of Backoff Cycle Register (BOFFPERIOD)

Address: 004BH, 004AH After reset: 0071H R/W

Symbol	15	14	13	12	11	10	9	8
BOFFPERIOD (004BH)	BOFF PERIOD15	BOFF PERIOD14	BOFF PERIOD13	BOFF PERIOD12	BOFF PERIOD11	BOFF PERIOD10	BOFF PERIOD9	BOFF PERIOD8
	7	6	5	4	3	2	1	0
(004AH)	BOFF PERIOD7	BOFF PERIOD6	BOFF PERIOD5	BOFF PERIOD4	BOFF PERIOD3	BOFF PERIOD2	BOFF PERIOD1	BOFF PERIOD0

BOFFPERIOD15 to BOFFPERIOD0	Backoff cycle value

3.4.33 CSMA-CA end count register (CSMAENDCOUNT)

This register is used to set the time between the completion of CCA and the transition to the idle state when the automatic CSMACA sequence is used. The initial value is 0080H, that is, 128 μs. The setting is possible in 1-μs units (1H = 1 μs). Set a value from 0002H to FFFFH in this register. The value of this register following a reset is 0080H.

Figure 3 - 44 Format of CSMA-CA End Count Register (CSMAENDCOUNT)

Address: 004DH, 004CH After reset: 0080H R/W

Symbol	15	14	13	12	11	10	9	8
CSMAENDCOUNT (004DH)	CSMAEND COUNT15	CSMAEND COUNT14	CSMAEND COUNT13	CSMAEND COUNT12	CSMAEND COUNT11	CSMAEND COUNT10	CSMAEND COUNT9	CSMAEND COUNT8
	7	6	5	4	3	2	1	0
(004CH)	CSMAEND COUNT7	CSMAEND COUNT6	CSMAEND COUNT5	CSMAEND COUNT4	CSMAEND COUNT3	CSMAEND COUNT2	CSMAEND COUNT1	CSMAEND COUNT0

CSMAENDCOUNT15 to CSMAENDCOUNT0	Time between the completion of CCA and the transition to the idle state

3.4.34 CSMA-CA start count register (CSMASTACOUNT)

This register is used to adjust the timing of starting CCA when the automatic CSMA-CA sequence is in use. The initial value is 000EH, that is, 14 data rate time[Note]. The setting is possible in 1 data rate time[Note] units (1H = 1 data rate time[Note]).

Note: The rate time depends on the value specified in the timing parameter data rate setting register.

Set a value from 0002H to FFFFH in this register. The value of this register following a reset is 000EH.

Figure 3 - 45 Format of CSMA-CA Start Count Register (CSMASTACOUNT)

Address: 004FH, 004EH After reset: 000EH R/W

Symbol	15	14	13	12	11	10	9	8
CSMASTACOUNT (004FH)	CSMASTACOUNT15	CSMASTACOUNT14	CSMASTACOUNT13	CSMASTACOUNT12	CSMASTACOUNT11	CSMASTACOUNT10	CSMASTACOUNT9	CSMASTACOUNT8
	7	6	5	4	3	2	1	0
(004EH)	CSMASTACOUNT7	CSMASTACOUNT6	CSMASTACOUNT5	CSMASTACOUNT4	CSMASTACOUNT3	CSMASTACOUNT2	CSMASTACOUNT1	CSMASTACOUNT0

CSMASTACOUNT15 to CSMASTACOUNT0	Warm-up time before CCA is started

3.4.35 Communication status register 1 (COMSTATE1)

This register is used to check various information on communication states. The transmission status, CCA status, and frame reception status bits indicate whether this device is in the transmission, CCA, and frame reception states, respectively.

Figure 3 - 46 Format of Communication Status Register 1 (COMSTATE1)

Address: 0066H After reset: XXXX000XB R

Symbol	7	6	5	4	3	2	1	0
COMSTATE1	X	X	X	X	FRCVSTATE	CCASTATE	TRNSTATE	X

FRCVSTATE	Frame reception status
0	Reception has not started.
1	Reception is in progress.

CCASTATE	CCA status
0	CCA has not started.
1	CCA is in progress.

TRNSTATE	Transmission status
0	Transmission has not started.
1	Transmission is in progress.

Caution An undefined value (X) is read from bits 0 and 7 to 4.

3.4.36 Communication status register 2 (COMSTATE2)

This register is used to check various information on communication states. The ACK reply status bit indicates whether this device is in the ACK reply operation state.

Figure 3 - 47 Format of Communication Status Register 2 (COMSTATE2)

Address: 0067H After reset: XXXXXXX0B R

Symbol	7	6	5	4	3	2	1	0
COMSTATE2	X	X	X	X	X	X	X	ACKSTATE

ACKSTATE	ACK reply status
0	ACK reply has not started.
1	ACK reply is in progress.

Caution An undefined value (X) is read from bits 7 to 1.

3.4.37 Evaluation control register (BBEVAREG)

This register is used to set the evaluation mode required to obtain the certification of conformance to technical standards. Setting both the continuous transmit mode bit and transmit trigger bit to 1 places this device in the continuous transmit mode. In this mode, data transmission is repeated for the number of data bytes specified in the transmitted frame length register minus the number of CRC bytes. Note that the data written to the transmission RAM are transmitted. The non-modulation switch bit can select the modulation signal or non-modulation signal. When using this bit, be sure to set the transmission method to FSK by the transmission method selection bit. Setting both the continuous receive mode bit and receive trigger bit to 1 places the device in the continuous receive mode. In this mode, the device does not enter the IDLE state but remains in the receive state after completing data reception. The value of this register following a reset is 00H.

Figure 3 - 48 Format of Evaluation Control Register (BBEVAREG)

Address: 0068H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBEVAREG	0	0	0	0	0	CONTRX	NOMOD	CONTTX

CONTRX	Continuous receive mode
0	Normal operation
1	Continuous receive operation

NOMOD	Non-modulation switch
0	Modulation signal
1	Non-modulation signal

CONTTX	Continuous transmit mode
0	Normal operation
1	Continuous transmit operation

Caution When writing to this register, set bits 7 to 3 to the value 0.

3.4.38 Backoff period register 2 (BBBOFFPROD2)

This register is used to set a random value for the backoff period of CSMA-CA. Set a random value in backoff period bits 0 to 7, and then set the automatic random backoff period enable bit of the backoff period register to 1. Set a value from 01H to FFH in this register. The value of this register following a reset is 00H.

Figure 3 - 49 Format of Backoff Period Register 2 (BBBOFFPROD2)

Address: 0069H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBBOFFPROD2	BOFFPROD7	BOFFPROD6	BOFFPROD5	BOFFPROD4	BOFFPROD3	BOFFPROD2	BOFFPROD1	BOFFPROD0

BOFFPROD7 to BOFFPROD0	Backoff period value

3.4.39 Communication status register 3 (COMSTATE3)

This register indicates the communication state. The number of retransmissions can be read from the RETRNRD3 to RETRNRD0 bits when the automatic ACK receive mode is enabled. The number of times the last CCA was handled can be read from the CCARD2 to CCARD0 bits. The value of this register following a reset is 00H.

Figure 3 - 50 Format of Communication Status Register 3 (COMSTATE3)

Address: 006FH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
COMSTATE3	0	CCARD2	CCARD1	CCARD0	RETRNRD3	RETRNRD2	RETRNRD1	RETRNRD0

CCARD2 to CCARD0	Number of times the last CCA proceeds (3 bits).

RETRNRD3 to RETRNRD0	Number of retransmissions when the automatic ACK receive mode is enabled (4 bits).

3.4.40 ACK reception wait time setting register (ACKRCVWIT)

This register is used to set the ACK receive wait time after the data transmission. Data are retransmitted when there is no ACK reply even after a wait for the specified time. The initial value is 0300H, that is, 768 data rate time[Note]. The setting is possible in 1 data rate time[Note] units (1H = 1 data rate time[Note]).

Note: The rate time depends on the value specified in the timing parameter data rate setting register.

The timing to detect ACK reception is switched by the ACK receive point setting bit. Set a value from 0001H to FFFFH in this register. The value of this register following a reset is 0300H.

Figure 3 - 51 Format of ACK Reception Wait Time Setting Register (ACKRCVWIT)

Address: 0071H, 0070H After reset: 0300H R/W

Symbol	15	14	13	12	11	10	9	8
ACKRCVWIT (0071H)	ACKRCVWIT15	ACKRCVWIT14	ACKRCVWIT13	ACKRCVWIT12	ACKRCVWIT11	ACKRCVWIT10	ACKRCVWIT9	ACKRCVWIT8
	7	6	5	4	3	2	1	0
(0070H)	ACKRCVWIT7	ACKRCVWIT6	ACKRCVWIT5	ACKRCVWIT4	ACKRCVWIT3	ACKRCVWIT2	ACKRCVWIT1	ACKRCVWIT0

ACKRCVWIT15 to ACKRCVWIT0	ACK receive wait time

3.4.41 Retransmission start comparison register (RETRNWUP)

This register is used to set the wait time until a trigger for retransmission is generated. The initial value is 0004H, that is, 4 data rate time[Note]. The setting is possible in 1 data rate time[Note] units (1H = 1 data rate time[Note]).

Note: The rate time depends on the value specified in the timing parameter data rate setting register.

Set a value from 0001H to FFFFH in this register. The value of this register following a reset is 0004H.

Figure 3 - 52 Format of Retransmission Start Comparison Register (RETRNWUP)

Address: 0073H, 0072H After reset: 0004H R/W

Symbol	15	14	13	12	11	10	9	8
RETRNWUP (0073H)	RETRNWUP15	RETRNWUP14	RETRNWUP13	RETRNWUP12	RETRNWUP11	RETRNWUP10	RETRNWUP9	RETRNWUP8
	7	6	5	4	3	2	1	0
(0072H)	RETRNWUP7	RETRNWUP6	RETRNWUP5	RETRNWUP4	RETRNWUP3	RETRNWUP2	RETRNWUP1	RETRNWUP0

RETRNWUP15 to RETRNWUP0	Wait time until a trigger for retransmission is generated

3.4.42 Received frame length register (BBRXFLEN)

This register holds the received frame length value. The value is stored once the packet data reception is started. The value is retained until the start of the next packet data reception. However, the register is updated when the address match is detected if the address filter is enabled. The value corresponding to the save bank specified by the receive data save bank select bit is read from this register. The value of this register following a reset is 0000H.

Figure 3 - 53 Format of Received Frame Length Register (BBRXFLEN)

Address: 00A1H, 00A0H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8
BBRXFLEN (00A1H)	0	0	0	0	0	RCVFLEN10	RCVFLEN9	RCVFLEN8
	7	6	5	4	3	2	1	0
(00A0H)	RCVFLEN7	RCVFLEN6	RCVFLEN5	RCVFLEN4	RCVFLEN3	RCVFLEN2	RCVFLEN1	RCVFLEN0

RCVFLEN10 to RCVFLEN0	Received frame length value

3.4.43 Received data counter register (BBRXCOUNT)

This register indicates the received data counter value. The number of received data bytes that have been stored in the reception RAM can be read from this register. The value is cleared to 0 when packet reception ends. When the value read from the lower-order byte at address 00A2H is 00H, re-read from the lower-order byte at the given address. Note that re-reading from the lower-order byte should be done before the counter has counted to 256 so that the value of the lower-order byte becomes 00H. The value of this register following a reset is 0000H.

Figure 3 - 54 Format of Received Data Counter Register (BBRXCOUNT)

Address: 00A3H, 00A2H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8
BBRXCOUNT (00A3H)	0	0	0	0	0	RXCOUNT 10	RXCOUNT 9	RXCOUNT 8
	7	6	5	4	3	2	1	0
(00A2H)	RXCOUNT 7	RXCOUNT 6	RXCOUNT 5	RXCOUNT 4	RXCOUNT 3	RXCOUNT 2	RXCOUNT 1	RXCOUNT 0

RXCOUNT10 to RXCOUNT0	Received data counter value

3.4.44 Transmitted frame length register (BBTXFLEN)

This register is used to set the frame length for transmission. Set the sum of the payload data length and CRC length (2 bytes or 4 bytes). When the automatic ACK reply function is enabled, ACK is automatically transmitted regardless of the frame length. Set a value from 0003H to 07FFH in this register. The value of this register following a reset is 0000H.

Figure 3 - 55 Format of Transmitted Frame Length Register (BBTXFLEN)

Address: 00A5H, 00A4H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBTXFLEN (00A5H)	0	0	0	0	0	TRNFLEN10	TRNFLEN9	TRNFLEN8
	7	6	5	4	3	2	1	0
(00A4H)	TRNFLEN7	TRNFLEN6	TRNFLEN5	TRNFLEN4	TRNFLEN3	TRNFLEN2	TRNFLEN1	TRNFLEN0

TRNFLEN10 to TRNFLEN0	Frame length for transmission

Caution When writing to this register, set bits 15 to 11 to the value 0.

3.4.45 Frequency setting register (BBFREQ)

This register is used to set a frequency. This register consists of 30 bits. The frequency ranged from 100 MHz to 1000 MHz can be set in 1-Hz steps. The initial value is 36FC3BA0H, that is, 922.5 MHz. Set a value from 337055C0H (863 MHz) to 37502800H (928 MHz) in this register. All four bytes should be specified in the order from the lowest to the highest address. The value of this register following a reset is 36FC3BA0H.

Figure 3 - 56 Format of Frequency Setting Register (BBFREQ)

Address: 00ABH to 00A8H After reset: 36FC3BA0H R/W

Symbol	31	30	29	28	27	26	25	24
BBFREQ (00ABH)	0	0	FREQ29	FREQ28	FREQ27	FREQ26	FREQ25	FREQ24
	23	22	21	20	19	18	17	16
(00AAH)	FREQ23	FREQ22	FREQ21	FREQ20	FREQ19	FREQ18	FREQ17	FREQ16
	15	14	13	12	11	10	9	8
(00A9H)	FREQ15	FREQ14	FREQ13	FREQ12	FREQ11	FREQ10	FREQ9	FREQ8
	7	6	5	4	3	2	1	0
(00A8H)	FREQ7	FREQ6	FREQ5	FREQ4	FREQ3	FREQ2	FREQ1	FREQ0

FREQ29 to FREQ0	Frequency value

Caution When writing to this register, set bits 31 and 30 to the value 0.

3.4.46 IF frequency setting register (BBIFSET)

The IF frequency setting bit is used to set the IF frequency. The frequency offset enable bit enables the function of the SX shift frequency setting register. The IF frequency offset enable bit enables or disables the setting of the offset value for the IF frequency. The offset value is set according to the setting in IF frequency offset setting register 0 or 1. The IF frequency offset selection bit is used to select whether the value in IF frequency offset setting register 0 or 1 is to be used. The value of this register following a reset is 00H.

Figure 3 - 57 Format of IF Frequency Setting Register (BBIFSET)

Address: 00ACH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBIFSET	0	0	0	0	IFOFSTSEL	IFOFSTEN	SFOFSET EN	IFSET

IFOFSTSEL	IF frequency offset selection
0	The value in IF frequency offset setting register 0 is to be used.
1	The value in IF frequency offset setting register 1 is to be used.

IFOFSTEN	IF frequency offset enable
0	IF frequency offset value setting is disabled.
1	IF frequency offset value setting is enabled.

SFOFSET EN	Frequency offset enable
0	Frequency shift setting is disabled.
1	Frequency shift setting is enabled.

IFSET	IF frequency setting
0	550 kHz
1	750 kHz

Caution When writing to this register, set bits 7 to 4 to the value 0.

3.4.47 IF frequency offset setting register 0 (BBIFOFST0)

The IF frequency offset 0 setting bits are used to set the offset value for the IF frequency. Specify a value in 2's complement representation. For example, 1H indicates 1 Hz. The specified value must be within the applicable range below.

- If the setting of the IF frequency setting bit is 0, that is, selecting 550 kHz: From -550 kHz to 1 MHz
- If the setting of the IF frequency setting bit is 1, that is, selecting 750 kHz: From -750 kHz to 1 MHz

The value of this register following a reset is 000000H.

Figure 3 - 58 Format of IF Frequency Offset Setting Register 0 (BBIFOFST0)

Address: 00B6H to 00B4H After reset: 000000H R/W

Symbol	23	22	21	20	19	18	17	16
BBIFOFST0 (00B6H)	0	0	0	IFOFST0 SET20	IFOFST0 SET19	IFOFST0 SET18	IFOFST0 SET17	IFOFST0 SET16
	15	14	13	12	11	10	9	8
(00B5H)	IFOFST0 SET15	IFOFST0 SET14	IFOFST0 SET13	IFOFST0 SET12	IFOFST0 SET11	IFOFST0 SET10	IFOFST0 SET9	IFOFST0 SET8
	7	6	5	4	3	2	1	0
(00B4H)	IFOFST0 SET7	IFOFST0 SET6	IFOFST0 SET5	IFOFST0 SET4	IFOFST0 SET3	IFOFST0 SET2	IFOFST0 SET1	IFOFST0 SET0

IFOFST0SET20 to IFOFST0SET0	IF frequency offset 0 setting
—	The offset value for the IF frequency

Caution When writing to this register, set bits 23 to 21 to the value 0.

3.4.48 IF frequency offset setting register 1 (BBIFOFST1)

The IF frequency offset 1 setting bits are used to set the offset value for the IF frequency. Specify a value in 2's complement representation. For example, 1H indicates 1 Hz. The specified value must be within the applicable range below.

- If the setting of the IF frequency setting bit is 0, that is, selecting 550 kHz: From -550 kHz to 1 MHz
- If the setting of the IF frequency setting bit is 1, that is, selecting 750 kHz: From -750 kHz to 1 MHz

The value of this register following a reset is 000000H.

Figure 3 - 59 Format of IF Frequency Offset Setting Register 1 (BBIFOFST1)

Address: 00BAH to 00B8H After reset: 000000H R/W

Symbol	23	22	21	20	19	18	17	16
BBIFOFST1 (00BAH)	0	0	0	IFOFST1 SET20	IFOFST1 SET19	IFOFST1 SET18	IFOFST1 SET17	IFOFST1 SET16
	15	14	13	12	11	10	9	8
(00B9H)	IFOFST1 SET15	IFOFST1 SET14	IFOFST1 SET13	IFOFST1 SET12	IFOFST1 SET11	IFOFST1 SET10	IFOFST1 SET9	IFOFST1 SET8
	7	6	5	4	3	2	1	0
(00B8H)	IFOFST1 SET7	IFOFST1 SET6	IFOFST1 SET5	IFOFST1 SET4	IFOFST1 SET3	IFOFST1 SET2	IFOFST1 SET1	IFOFST1 SET0

IFOFST1SET20 to IFOFST1SET0	IF frequency offset 1 setting
—	The offset value for the IF frequency

Caution When writing to this register, set bits 23 to 21 to the value 0.

3.4.49 SX shift frequency setting register (BBSXSFTFREQ)

The SX shift frequency setting bits are used to set the amount of SX frequency shifting (1H = 1 kHz). The frequency offset enable bit enables the setting of this register.

000H: 0 kHz

001H: 1 kHz

002H: 2 kHz

:

0C8H: 200 kHz

:

7FFH: 2047 kHz

800H: 0 kHz

801H: -1 kHz

802H: -2 kHz

:

8C8H: -200 kHz

:

FFFH: -2047 kHz

The value of this register following a reset is 0000H.

Figure 3 - 60 Format of SX Shift Frequency Setting Register (BBSXSFTFREQ)

Address: 00AEH, 00ADH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBSXSFTFREQ (00AEH)	0	0	0	0	SXSFTFREQ11	SXSFTFREQ10	SXSFTFREQ9	SXSFTFREQ8
	7	6	5	4	3	2	1	0
(00ADH)	SXSFTFREQ7	SXSFTFREQ6	SXSFTFREQ5	SXSFTFREQ4	SXSFTFREQ3	SXSFTFREQ2	SXSFTFREQ1	SXSFTFREQ0

SXSFTFREQ11 to SXSFTFREQ0	SX shift frequency setting
—	These bits set the amount of SX frequency shifting.

Caution When writing to this register, set bits 15 to 12 to the value 0.

3.4.50 CCA time register (CCATIME)

This register is used to set the time taken for the CCA processing. The initial value is 000DH, that is, 13 data rate time[Note]. The setting is possible in 1 data rate time[Note] units (1H = 1 data rate time[Note]).

Note: The rate time depends on the value specified in the timing parameter data rate setting register.

Control applied by the setting of this register includes the time for auto gain control (AGC) processing. Up to 2000 data rate time can be specified. The value of this register following a reset is 000DH.

Figure 3 - 61 Format of CCA Time Register (CCATIME)

Address: 00B3H, 00B2H After reset: 000DH R/W

Symbol	15	14	13	12	11	10	9	8
CCATIME (00B3H)	CCATIME15	CCATIME14	CCATIME13	CCATIME12	CCATIME11	CCATIME10	CCATIME9	CCATIME8
	7	6	5	4	3	2	1	0
(00B2H)	CCATIME7	CCATIME6	CCATIME5	CCATIME4	CCATIME3	CCATIME2	CCATIME1	CCATIME0

CCATIME15 to CCATIME0	CCA time

Caution The minimum value that can be specified in this register depends on the data rate. See the latest application note which specifies the recommended register settings for use with this product.

3.4.51 Transmitted data counter register (BBTXCOUNT)

This register indicates the transmitted data counter value. The number of transmit data bytes that have been transferred from the transmission RAM to the transmitter can be read from this register. The value is cleared to 0 when packet transmission ends. Be sure to read data in the order from the lower-order byte to the higher-order byte because the higher-order three bits are stored in this register at the timing when the lower eight bits are read. When the value read from the lower-order byte at address 00BCH is 00H, re-read from the lower-order byte at the given address. Note that re-reading from the lower-order byte should be done before the counter has counted to 256 so that the value of the lower-order byte becomes 00H. The value of this register following a reset is 0000H.

Figure 3 - 62 Format of Transmitted Data Counter Register (BBTXCOUNT)

Address: 00BDH, 00BCH After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8
BBTX COUNT (00BDH)	0	0	0	0	0	TRNCOUNT 10	TRNCOUNT 9	TRNCOUNT 8
	7	6	5	4	3	2	1	0
(00BCH)	TRNCOUNT 7	TRNCOUNT 6	TRNCOUNT 5	TRNCOUNT 4	TRNCOUNT 3	TRNCOUNT 2	TRNCOUNT 1	TRNCOUNT 0

TRNCOUNT10 to TRNCOUNT0	Transmitted data counter value

3.4.52 External device control register 0 (BBEXTCON0)

The CTX, CPS, and CSD signals can be output through GPIO port pins to control an external device such as a power amplifier. Output of the CTX, CPS, and CSD signals is enabled by the following bits in this register.

- Transmit CTX enable bit: CTX signal for transmission
- Receive CTX enable bit: CTX signal for reception
- Transmit CPS enable bit: CPS signal for transmission
- Receive CPS enable bit: CPS signal for reception
- Transmit CSD enable bit: CSD signal for transmission
- Receive CSD enable bit: CSD signal for reception

The output pins can be selected from among GPIO0 to GPIO12 by GPIO function selection registers 0 to 7.

The value of this register following a reset is 00H.

(1) CTX signal

Setting the transmit CTX enable bit to 1 drives the CTX signal high once the time specified in the CTX set timing register has elapsed since a transmission trigger is set. The signal is driven low once the time specified in the CTX clear timing register has elapsed since the completion of transmission. Setting the receive CTX enable bit to 1 drives the signal high once a receive trigger is set, and it is driven low upon completion of the reception.

(2) CPS signal

Setting the transmit CPS enable bit to 1 drives the CPS signal high once the time specified in the CPS set timing register has elapsed since a transmission trigger is set. The signal is driven low once the time specified in the CPS clear timing register has elapsed since the completion of transmission. Setting the receive CPS enable bit to 1 drives the signal high once a receive trigger is set, and it is driven low upon completion of the reception.

(3) CSD signal

Setting the transmit CSD enable bit to 1 drives the CSD signal high once the time specified in the CSD set timing register has elapsed since a transmission trigger is set. The signal is driven low once the time specified in the CSD clear timing register has elapsed since the completion of transmission. Setting the receive CSD enable bit to 1 drives the signal high once a receive trigger is set, and it is driven low upon completion of the reception.

Figure 3 - 63 Format of External Device Control Register 0 (BBEXTCON0)

Address: 00BEH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBEXTCON0	0	0	RXCSDEN	TXCSDEN	RXCPSEN	TXCPSEN	RXCTXEN	TXCTXEN

RXCSDEN	Receive CSD enable
0	Signal is disabled.
1	Signal is enabled.

TXCSDEN	Transmit CSD enable
0	Signal is disabled.
1	Signal is enabled.

RXCPSEN	Receive CPS enable
0	Signal is disabled.
1	Signal is enabled.

TXCPSEN	Transmit CPS enable
0	Signal is disabled.
1	Signal is enabled.

RXCTXEN	Receive CTX enable
0	Signal is disabled.
1	Signal is enabled.

TXCTXEN	Transmit CTX enable
0	Signal is disabled.
1	Signal is enabled.

Caution When writing to this register, set bits 7 and 6 to the value 0.

3.4.53 External device control register 1 (BBEXTCON1)

The CTX, CPS, and CSD inversion bits are used to invert the CTX, CPS, and CSD signals, respectively. The value of this register following a reset is 00H.

Figure 3 - 64 Format of External Device Control Register 1 (BBEXTCON1)

Address: 00BFH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBEXTCON1	0	0	0	0	0	CSDRVS	CPSRVS	CTXRVS

CSDRVS	CSD inversion
0	Normal operation.
1	Signal is inverted.

CPSRVS	CPS inversion
0	Normal operation.
1	Signal is inverted.

CTXRVS	CTX inversion
0	Normal operation.
1	Signal is inverted.

Caution When writing to this register, set bits 7 to 3 to the value 0.

3.4.54 CTX set timing register (BBCTXSET)

This register is used to set the timing to drive the CTX signal for transmission to the high level when the transmit CTX enable bit is set (signal is enabled). The setting is possible in 1-µs units (1H = 1 µs). The value of this register following a reset is 0001H.

Figure 3 - 65 Format of CTX Set Timing Register (BBCTXSET)

Address: 00C1H, 00C0H After reset: 0001H R/W

Symbol	15	14	13	12	11	10	9	8
BBCTXSET (00C1H)	CTXSET15	CTXSET14	CTXSET13	CTXSET12	CTXSET11	CTXSET10	CTXSET9	CTXSET8
	7	6	5	4	3	2	1	0
(00C0H)	CTXSET7	CTXSET6	CTXSET5	CTXSET4	CTXSET3	CTXSET2	CTXSET1	CTXSET0

CTXSET15 to CTXSET0	CTX set timing
—	Time for driving CTX for transmission to the high level

3.4.55 CTX clear timing register (BBCTXCLR)

This register is used to set the timing to drive the CTX signal for transmission to the low level when the transmit CTX enable bit is set (signal is enabled). The setting is possible in 1-µs units (1H = 1 µs). The value of this register following a reset is 0001H.

Figure 3 - 66 Format of CTX Clear Timing Register (BBCTXCLR)

Address: 00C3H, 00C2H After reset: 0001H R/W

Symbol	15	14	13	12	11	10	9	8
BBCTXCLR (00C3H)	CTXCLR15	CTXCLR14	CTXCLR13	CTXCLR12	CTXCLR11	CTXCLR10	CTXCLR9	CTXCLR8
	7	6	5	4	3	2	1	0
(00C2H)	CTXCLR7	CTXCLR6	CTXCLR5	CTXCLR4	CTXCLR3	CTXCLR2	CTXCLR1	CTXCLR0

CTXCLR15 to CTXCLR0	CTX clear timing
—	Time for driving CTX for transmission to the low level

3.4.56 CPS set timing register (BBCPSSET)

This register is used to set the timing to drive the CPS signal for transmission to the high level when the transmit CPS enable bit is set (signal is enabled). The setting is possible in 1-µs units (1H = 1 µs). The value of this register following a reset is 0001H.

Figure 3 - 67 Format of CPS Set Timing Register (BBCPSSET)

Address: 00C5H, 00C4H After reset: 0001H R/W

Symbol	15	14	13	12	11	10	9	8
BBCPSSET (00C5H)	CPSSET15	CPSSET14	CPSSET13	CPSSET12	CPSSET11	CPSSET10	CPSSET9	CPSSET8
	7	6	5	4	3	2	1	0
(00C4H)	CPSSET7	CPSSET6	CPSSET5	CPSSET4	CPSSET3	CPSSET2	CPSSET1	CPSSET0

CPSSET15 to CPSSET0	CPS set timing
—	These bits set the timing to drive the CPS signal for transmission to the high level.

3.4.57 CPS clear timing register (BBCPSCLR)

This register is used to set the timing to drive the CPS signal for transmission to the low level when the transmit CPS enable bit is set (signal is enabled). The setting is possible in 1-µs units (1H = 1 µs). The value of this register following a reset is 0001H.

Figure 3 - 68 Format of CPS Clear Timing Register (BBCPSCLR)

Address: 00C7H, 00C6H After reset: 0001H R/W

Symbol	15	14	13	12	11	10	9	8
BBCPSCLR (00C7H)	CPSCLR15	CPSCLR14	CPSCLR13	CPSCLR12	CPSCLR11	CPSCLR10	CPSCLR9	CPSCLR8
	7	6	5	4	3	2	1	0
(00C6H)	CPSCLR7	CPSCLR6	CPSCLR5	CPSCLR4	CPSCLR3	CPSCLR2	CPSCLR1	CPSCLR0

CPSCLR15 to CPSCLR0	CPS clear timing
—	These bits set the timing to drive the CPS signal for transmission to the low level.

3.4.58 CSD set timing register (BBCSDSET)

This register is used to set the timing to drive the CSD signal for transmission to the high level when the transmit CSD enable bit is set (signal is enabled). The setting is possible in 1-µs units (1H = 1 µs). The value of this register following a reset is 0001H.

Figure 3 - 69 Format of CSD Set Timing Register (BBCSDSET)

Address: 00C9H, 00C8H After reset: 0001H R/W

Symbol	15	14	13	12	11	10	9	8
BBCSDSET (00C9H)	CSDSET15	CSDSET14	CSDSET13	CSDSET12	CSDSET11	CSDSET10	CSDSET9	CSDSET8
	7	6	5	4	3	2	1	0
(00C8H)	CSDSET7	CSDSET6	CSDSET5	CSDSET4	CSDSET3	CSDSET2	CSDSET1	CSDSET0

CSDSET15 to CSDSET0	CSD set timing
—	These bits set the timing to drive the CSD signal for transmission to the high level.

3.4.59 CSD clear timing register (BBCSDCLR)

This register is used to set the timing to drive the CSD signal for transmission to the low level when the transmit CSD enable bit is set (signal is enabled). The setting is possible in 1-µs units (1H = 1 µs). The value of this register following a reset is 0001H.

Figure 3 - 70 Format of CSD Clear Timing Register (BBCSDCLR)

Address: 00CBH, 00CAH After reset: 0001H R/W

Symbol	15	14	13	12	11	10	9	8
BBCSDCLR (00CBH)	CSDCLR15	CSDCLR14	CSDCLR13	CSDCLR12	CSDCLR11	CSDCLR10	CSDCLR9	CSDCLR8
	7	6	5	4	3	2	1	0
(00CAH)	CSDCLR7	CSDCLR6	CSDCLR5	CSDCLR4	CSDCLR3	CSDCLR2	CSDCLR1	CSDCLR0

CSDCLR15 to CSDCLR0	CSD clear timing
—	These bits set the timing to drive the CSD signal for transmission to the low level.

3.4.60 Number-of-received-byte interrupt comparison register (BBRCVINTCOMP)

This register is used to generate interrupts depending on the number of received bytes. An interrupt request is generated when the number of received bytes stored in the reception RAM reaches the specified number. When a number-of-receive-byte interrupt is generated while the address filter is enabled, the received data are not stored in the reception RAM until an address filter interrupt is generated. Set a value from 0001H to 07FFH in this register. The value of this register following a reset is 0010H.

Figure 3 - 71 Format of Number-of-Received-Byte Interrupt Comparison Register (BBRCVINTCOMP)

Address: 00D3H, 00D2H After reset: 0010H R/W

Symbol	15	14	13	12	11	10	9	8
BBRCVINTCOMP (00D3H)	0	0	0	0	0	RCVINTCOMP10	RCVINTCOMP9	RCVINTCOMP8
	7	6	5	4	3	2	1	0
(00D2H)	RCVINTCOMP7	RCVINTCOMP6	RCVINTCOMP5	RCVINTCOMP4	RCVINTCOMP3	RCVINTCOMP2	RCVINTCOMP1	RCVINTCOMP0

RCVINTCOMP10 to RCVINTCOMP0	Number of bytes that generates a number-of-receive-byte interrupt

Caution When writing to this register, set bits 15 to 11 to the value 0.

3.4.61 Backoff period total number register (BBBOPTOTAL)

This register indicates the total number of backoff periods in CSMA-CA. The maximum value to be counted is FFFFH.

The value of this register following a reset is 0000H.

Figure 3 - 72 Format of Backoff Period Total Number Register (BBBOPTOTAL)

Address: 00D5H, 00D4H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8
BBBOPTOTAL (00D5H)	BOPTOTAL15	BOPTOTAL14	BOPTOTAL13	BOPTOTAL12	BOPTOTAL11	BOPTOTAL10	BOPTOTAL9	BOPTOTAL8
	7	6	5	4	3	2	1	0
(00D4H)	BOPTOTAL7	BOPTOTAL6	BOPTOTAL5	BOPTOTAL4	BOPTOTAL3	BOPTOTAL2	BOPTOTAL1	BOPTOTAL0

BOPTOTAL15 to BOPTOTAL0	Total number of backoff periods

3.4.62 CCA total number register (BBCCATOTAL)

This register indicates the total number of CCA operations in CSMA-CA. The maximum value to be counted is FFH.

The value of this register following a reset is 00H.

Figure 3 - 73 Format of CCA Total Number Register (BBCCATOTAL)

Address: 00D6H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
BBCCATOTAL	CCATOTAL7	CCATOTAL6	CCATOTAL5	CCATOTAL4	CCATOTAL3	CCATOTAL2	CCATOTAL1	CCATOTAL0

CCATOTAL7 to CCATOTAL0	Total number of CCA operations

3.4.63 Address filter extension address control register (BBADFCON)

The PAN coordinator 2 bit selects whether the received address matches the PAN coordinator address as an address filter condition for the second address. The frame pending 2 setting bit sets the value of the frame pending bit in the ACK data to be returned for the second address. The first address filter match monitor bit and second address filter match monitor bit are used to monitor the first address match and second address match, respectively. The values corresponding to the save bank specified by the receive data save bank select bit is read from these registers. When address extension is disabled by the address filter address extension bit, the values in the first and second address filter match monitor bits are invalid. When address extension is enabled by the address filter address extension bit, the values in the first and second address filter match monitor bits are invalid under the following conditions.

- Frame version: 00 or 01
- Frame type: Beacon frame
- No destination PAN ID or destination address
- The source PAN ID matches the value of either of the PAN identifier register 0 or 1, or either of the value of the PAN identifier register 0 or 1 is FFFFH.
- PANCORD bit = 0

The value of this register following a reset is 00H.

Figure 3 - 74 Format of Address Filter Extension Address Control Register (BBADFCON)

Address: 00DFH After reset: 00H R/W[Note]

Symbol	7	6	5	4	3	2	1	0
BBADFCON	0	0	0	0	ADFMONI2	ADFMONI1	FLMPEND2	PANCORD2

ADFMONI2	Second address filter match monitor
0	Second address mismatch
1	Second address match

ADFMONI1	First address filter match monitor
0	First address mismatch
1	First address match

FLMPEND2	Frame pending 2 setting
0	Frame pending bit = 0
1	Frame pending bit = 1

PANCORD2	PAN coordinator 2
0	The address is not for the PAN coordinator.
1	The address is for the PAN coordinator.

Note: Bits 3 and 2 are read-only.

Caution When writing to this register, set bits 7 to 4 to the value 0.

3.4.64 PAN identifier register 1 (BBPANID1)

This register is used to set the PAN identifier as a condition for filtering of the second address. It consists of 16 bits and the specified value is compared with the received PAN identifier to detect an address match. Set a value from 0000H to FFFFH in this register. The value of this register following a reset is FFFFH.

Figure 3 - 75 Format of PAN Identifier Register 1 (BBPANID1)

Address: 00E1H, 00E0H After reset: FFFFH R/W

Symbol	15	14	13	12	11	10	9	8
BBPANID1 (00E1H)	PANID115	PANID114	PANID113	PANID112	PANID111	PANID110	PANID19	PANID18
	7	6	5	4	3	2	1	0
(00E0H)	PANID17	PANID16	PANID15	PANID14	PANID13	PANID12	PANID11	PANID10

PANID115 to PANID10	PAN identifier

3.4.65 Short address register 1 (BBSHORTAD1)

This register is used to set the short address as a condition for filtering of the second address. It consists of 16 bits and the specified value is compared with the received short address to detect an address match. Set a value from 0000H to FFFFH in this register. The value of this register following a reset is FFFFH.

Figure 3 - 76 Format of Short Address Register 1 (BBSHORTAD1)

Address: 00E3H, 00E2H After reset: FFFFH R/W

Symbol	15	14	13	12	11	10	9	8
BBSHORTAD1 (00E3H)	SHORTAD115	SHORTAD114	SHORTAD113	SHORTAD112	SHORTAD111	SHORTAD110	SHORTAD19	SHORTAD18
	7	6	5	4	3	2	1	0
(00E2H)	SHORTAD17	SHORTAD16	SHORTAD15	SHORTAD14	SHORTAD13	SHORTAD12	SHORTAD11	SHORTAD10

SHORTAD115 to SHORTAD10	Short address

3.4.66 Extended address registers 1 (BBEXTENDAD10 to BBEXTENDAD13)

These registers are used to set the extended address as a condition for filtering of the second address. Four 16-bit registers are provided to specify a 64-bit address and the specified value is compared with the received extended address to detect an address match. Set a value from 0000H to FFFFH in these registers. The value of these registers following a reset is 0000H.

Figure 3 - 77 Format of Extended Address Registers 1 (BBEXTENDAD10 to BBEXTENDAD13) (1/2)

Address: 00EBH, 00EAH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBEXTENDAD13 (00EBH)	EXTENDAD1315	EXTENDAD1314	EXTENDAD1313	EXTENDAD1312	EXTENDAD1311	EXTENDAD1310	EXTENDAD139	EXTENDAD138
	7	6	5	4	3	2	1	0
(00EAH)	EXTENDAD137	EXTENDAD136	EXTENDAD135	EXTENDAD134	EXTENDAD133	EXTENDAD132	EXTENDAD131	EXTENDAD130

EXTENDAD1315 to EXTENDAD130	Bits 63 to 48 of extended address

Address: 00E9H, 00E8H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBEXTENDAD12 (00E9H)	EXTENDAD1215	EXTENDAD1214	EXTENDAD1213	EXTENDAD1212	EXTENDAD1211	EXTENDAD1210	EXTENDAD129	EXTENDAD128
	7	6	5	4	3	2	1	0
(00E8H)	EXTENDAD127	EXTENDAD126	EXTENDAD125	EXTENDAD124	EXTENDAD123	EXTENDAD122	EXTENDAD121	EXTENDAD120

EXTENDAD1215 to EXTENDAD120	Bits 47 to 32 of extended address

Figure 3 - 77 Format of Extended Address Registers 1 (BBEXTENDAD10 to BBEXTENDAD13) (2/2)

Address: 00E7H, 00E6H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBEXTENDAD11 (00E7H)	EXTENDAD1115	EXTENDAD1114	EXTENDAD1113	EXTENDAD1112	EXTENDAD1111	EXTENDAD1110	EXTENDAD119	EXTENDAD118
	7	6	5	4	3	2	1	0
(00E6H)	EXTENDAD117	EXTENDAD116	EXTENDAD115	EXTENDAD114	EXTENDAD113	EXTENDAD112	EXTENDAD111	EXTENDAD110

EXTENDAD1115 to EXTENDAD110	Bits 31 to 16 of extended address

Address: 00E5H, 00E4H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBEXTENDAD10 (00E5H)	EXTENDAD1015	EXTENDAD1014	EXTENDAD1013	EXTENDAD1012	EXTENDAD1011	EXTENDAD1010	EXTENDAD109	EXTENDAD108
	7	6	5	4	3	2	1	0
(00E4H)	EXTENDAD107	EXTENDAD106	EXTENDAD105	EXTENDAD104	EXTENDAD103	EXTENDAD102	EXTENDAD101	EXTENDAD100

EXTENDAD1015 to EXTENDAD100	Bits 15 to 0 of extended address

3.4.67 Reception timeout register (BBTIMEOUT)

This register is used to set the time until a timeout occurs when ACK is not returned (PHR reception is not started) while the automatic receive mode with the timeout function is enabled. This register consists of 12 bits. Set a value from 0001H to 0FFFH in this register. The setting is possible in 1-μs units (1H = 1 μs). The value of this register following a reset is 07D0H, that is, 2 ms.

Figure 3 - 78 Format of Reception Timeout Register (BBTIMEOUT)

Address: 00EDH, 00ECH After reset: 07D0H R/W

Symbol	15	14	13	12	11	10	9	8
BBTIMEOUT (00EDH)	0	0	0	0	TIMEOUT11	TIMEOUT10	TIMEOUT9	TIMEOUT8
	7	6	5	4	3	2	1	0
(00ECH)	TIMEOUT7	TIMEOUT6	TIMEOUT5	TIMEOUT4	TIMEOUT3	TIMEOUT2	TIMEOUT1	TIMEOUT0

TIMEOUT11 to TIMEOUT0	Time until a timeout

Caution When writing to this register, set bits 15 to 12 to the value 0.

3.4.68 INTOUT mode register (BBINTOUTMODE)

The INTOUT0 output sense switching bit can select the interrupt sense (high or low level) of the interrupt output from the port pin selected as the INTOUT0 output pin. The following interrupt source flags are automatically cleared upon completion of reception by setting the reception completion synchronized clearing bit.

- Frame length
- Address filtering
- Start reception
- AGC completion
- Preamble detection
- Carrier sense

The INTREQ0 selection bit can select whether the CSMA-CA completion interrupt or the CCA completion interrupt is the interrupt source assigned to the following bits.

- Respective bits 4 in the registers at 00F8H, 0100H, and 0108H

The INTREQ1 selection bit can select the frame length interrupt or the address filtering interrupt as the interrupt source assigned to the following bits.

- Respective bits 4 in the registers at 00F9H, 0101H, and 0109H
- Respective bits 5 in the registers at 00FAH, 0102H, and 010AH
- Respective bits 5 in the registers at 00FBH, 0103H, and 010BH

The INTREQ2 selection bit can select the CCA clearance interrupt or the reception canceled interrupt as the interrupt source assigned to the following bits.

- Respective bits 2 in the registers at 00FAH, 0102H, and 010AH

The following interrupt source flags are automatically cleared upon cancellation of reception if the setting of the reception canceling synchronized clearing bit is 1.

- Bank 0 reception completion
- Bank 1 reception completion
- Frame length
- Address filtering
- Start reception
- Number of received bytes
- AGC completion
- Preamble detection
- Carrier sense

The value of this register following a reset is 00H.

Figure 3 - 79 Format of INTOUT Mode Register (BBINTOUTMODE)

Address: 00F2H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBINTOUTMODE	RCVCANCELCLR	INTREQ2SEL	INTREQ1SEL	INTREQ0SEL	RCVFINCLR	0	0	INTOUT0SEL

RCVCANCELCLR	Reception canceling synchronized clearing
0	Interrupt source flags are not automatically cleared upon cancellation of reception.
1	Interrupt source flags are automatically cleared upon cancellation of reception.

INTREQ2SEL	INTREQ2 selection
0	The CCA clearance interrupt is selected.
1	The reception canceled interrupt is selected.

INTREQ1SEL	INTREQ1 selection
0	The frame length interrupt is selected.
1	The address filtering interrupt is selected.

INTREQ0SEL	INTREQ0 selection
0	The CSMA-CA completion interrupt is selected.
1	The CCA completion interrupt is selected.

RCVFINCLR	Reception completion synchronized clearing
0	Interrupt source flags are not automatically cleared upon completion of reception.
1	Interrupt source flags are automatically cleared upon completion of reception.

INTOUT0SEL	INTOUT0 output sense switching
0	High level is an interrupt request.
1	Low level is an interrupt request.

Caution When writing to this register, set bits 2 and 1 to the value 0.

3.4.69 INTOUT0 interrupt source register 0 (BBINT0REQ0)

Upon the generation of an interrupt request due to a given interrupt source condition being satisfied while the corresponding interrupt request is enabled, the corresponding interrupt source flag is set to 1 to indicate generation of the interrupt request. Reading this bit only clears it to 0 after it has been read as 1. Dummy-read the bit to clear it because it is not writable. When the setting of at least one of the interrupt source flags in the INTOUT0 interrupt source registers 0 to 7 is 1, and the generation of the corresponding interrupt request is enabled, the 8 bytes of the INTOUT0 interrupt source registers 0 to 7 must be read consecutively with the SEN pin remaining at the low level. The values of these registers following a reset are undefined.

Figure 3 - 80 Format of INTOUT0 Interrupt Source Register 0 (BBINT0REQ0) (1/2)

Address: 00F4H After reset: XXH R

Symbol	7	6	5	4	3	2	1	0
BBINT0 REQ0	CSMA INTREQ	FSYNC INTREQ	TRN1 INTREQ	TRN0 INTREQ	CAL INTREQ	TIM2 INTREQ	TIM1 INTREQ	TIM0 INTREQ

CSMA INTREQ	CSMA-CA completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

FSYNC INTREQ	Frame synchronization transmission completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

TRN1 INTREQ	Bank 1 transmission completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

TRN0 INTREQ	Bank 0 transmission completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

CAL INTREQ	Calibration completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

Figure 3 - 80 Format of INTOUT0 Interrupt Source Register 0 (BBINT0REQ0) (2/2)

TIM2 INTREQ	Timer comparison 2 interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

TIM1 INTREQ	Timer comparison 1 interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

TIM0 INTREQ	Timer comparison 0 interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

3.4.70 INTOUT0 interrupt source register 1 (BBINT0REQ1)

Upon the generation of an interrupt request due to a given interrupt source condition being satisfied while the corresponding interrupt request is enabled, the corresponding interrupt source flag is set to 1 to indicate generation of the interrupt request. Reading this bit only clears it to 0 after it has been read as 1. Dummy-read the bit to clear it because it is not writable. When the setting of at least one of the interrupt source flags in the INTOUT0 interrupt source registers 0 to 7 is 1, and the generation of the corresponding interrupt request is enabled, the 8 bytes of the INTOUT0 interrupt source registers 0 to 7 must be read consecutively with the SEN pin remaining at the low level. The values of these registers following a reset are undefined.

Figure 3 - 81 Format of INTOUT0 Interrupt Source Register 1 (BBINT0REQ1) (1/2)

Address: 00F5H After reset: XXH R

Symbol	7	6	5	4	3	2	1	0
BBINT0 REQ1	TRNFIN INTREQ	RCVLVL INTREQ	MODESW INTREQ	ROVR INTREQ	ADRS INTREQ	FL INTREQ	RCV1 INTREQ	RCV0 INTREQ

TRNFIN INTREQ	Frame transmission completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

RCVLVL INTREQ	Reception level interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

MODESW INTREQ	Mode switch reception completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

ROVR INTREQ	Reception overrun interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

ADRS INTREQ	Address filtering interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

Figure 3 - 81 Format of INTOUT0 Interrupt Source Register 1 (BBINT0REQ1) (2/2)

FL INTREQ	Frame length interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

RCV1 INTREQ	Bank 1 reception completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

RCV0 INTREQ	Bank 0 reception completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

3.4.71 INTOUT0 interrupt source register 2 (BBINT0REQ2)

Upon the generation of an interrupt request due to a given interrupt source condition being satisfied while the corresponding interrupt request is enabled, the corresponding interrupt source flag is set to 1 to indicate generation of the interrupt request. Reading this bit only clears it to 0 after it has been read as 1. Dummy-read the bit to clear it because it is not writable. When the setting of at least one of the interrupt source flags in the INTOUT0 interrupt source registers 0 to 7 is 1, and the generation of the corresponding interrupt request is enabled, the 8 bytes of the INTOUT0 interrupt source registers 0 to 7 must be read consecutively with the SEN pin remaining at the low level. The values of these registers following a reset are undefined.

Figure 3 - 82 Format of INTOUT0 Interrupt Source Register 2 (BBINT0REQ2) (1/2)

Address: 00F6H After reset: XXH R

Symbol	7	6	5	4	3	2	1	0
BBINT0 REQ2	PREAMBL INTREQ	CCA INTREQ	AGC INTREQ	RCVBYTE INTREQ	RCVFIN INTREQ	RCVSTA INTREQ	TRNSTART INTREQ	TRNBYTE INTREQ

PREAMBL INTREQ	Preamble detection interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

CCA INTREQ	CCA completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

AGC INTREQ	AGC completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

RCVBYTE INTREQ	Number of received bytes interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

RCVFIN INTREQ	Frame reception completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

Figure 3 - 82 Format of INTOUT0 Interrupt Source Register 2 (BBINT0REQ2) (2/2)

RCVSTA INTREQ	Reception start interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

TRNSTAR TINTREQ	Transmission start interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

TRNBYTE INTREQ	Number of transmitted bytes interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

3.4.72 INTOUT0 interrupt source register 3 (BBINT0REQ3)

Upon the generation of an interrupt request due to a given interrupt source condition being satisfied while the corresponding interrupt request is enabled, the corresponding interrupt source flag is set to 1 to indicate generation of the interrupt request. Reading this bit only clears it to 0 after it has been read as 1. Dummy-read the bit to clear it because it is not writable. When the setting of at least one of the interrupt source flags in the INTOUT0 interrupt source registers 0 to 7 is 1, and the generation of the corresponding interrupt request is enabled, the 8 bytes of the INTOUT0 interrupt source registers 0 to 7 must be read consecutively with the SEN pin remaining at the low level. The values of these registers following a reset are undefined.

Figure 3 - 83 Format of INTOUT0 Interrupt Source Register 3 (BBINT0REQ3) (1/2)

Address: 00F7H After reset: XXH R

Symbol	7	6	5	4	3	2	1	0
BBINT0 REQ3	CANCEL INTREQ	X	X	TRNUNDRR UNINTREQ	RCVTOUT INTREQ	CCACLR INTREQ	CCALIMIT INTREQ	CS INTREQ

CANCEL INTREQ	Reception canceled interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

TRNUNDRR UNINTREQ	Transmission underrun interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

RCVTOUT INTREQ	Automatic reception timeout interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

CCACLR INTREQ	CCA clearance interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

CCALIMIT INTREQ	CCA limitation interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

Figure 3 - 83 Format of INTOUT0 Interrupt Source Register 3 (BBINT0REQ3) (2/2)

CS INTREQ	Carrier sense interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

3.4.73 INTOUT0 interrupt source register 4 (BBINT0REQ4)

Upon the generation of an interrupt request due to a given interrupt source condition being satisfied while the corresponding interrupt request is enabled, the corresponding interrupt source flag is set to 1 to indicate generation of the interrupt request. Reading this bit only clears it to 0 after it has been read as 1. Dummy-read the bit to clear it because it is not writable. When the setting of at least one of the interrupt source flags in the INTOUT0 interrupt source registers 0 to 7 is 1, and the generation of the corresponding interrupt request is enabled, the 8 bytes of the INTOUT0 interrupt source registers 0 to 7 must be read consecutively with the SEN pin remaining at the low level. The values of these registers following a reset are undefined.

Figure 3 - 84 Format of INTOUT0 Interrupt Source Register 4 (BBINT0REQ4) (1/2)

Address: 00F8H After reset: XXH R

Symbol	7	6	5	4	3	2	1	0
BBINT0REQ4	TRNFIN INTREQ	TRNFSYNC INTREQ	TRNSTART INTREQ	CSMA INTREQ	TRNUNDRR UNINTREQ	TRNBYTE INTREQ	TRN1 INTREQ	TRN0 INTREQ

TRNFIN INTREQ	Frame transmission completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

TRNFSYNC INTREQ	Frame synchronization transmission completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

TRNSTART INTREQ	Transmission start interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

CSMA INTREQ	CSMA-CA completion or CCA completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

TRNUNDRR UNINTREQ	Transmission underrun interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

Figure 3 - 84 Format of INTOUT0 Interrupt Source Register 4 (BBINT0REQ4) (2/2)

TRNBYTE INTREQ	Number of transmitted bytes interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

TRN1 INTREQ	Bank 1 transmission completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

TRN0 INTREQ	Bank 0 transmission completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

3.4.74 INTOUT0 interrupt source register 5 (BBINT0REQ5)

Upon the generation of an interrupt request due to a given interrupt source condition being satisfied while the corresponding interrupt request is enabled, the corresponding interrupt source flag is set to 1 to indicate generation of the interrupt request. Reading this bit only clears it to 0 after it has been read as 1. Dummy-read the bit to clear it because it is not writable. When the setting of at least one of the interrupt source flags in the INTOUT0 interrupt source registers 0 to 7 is 1, and the generation of the corresponding interrupt request is enabled, the 8 bytes of the INTOUT0 interrupt source registers 0 to 7 must be read consecutively with the SEN pin remaining at the low level. The values of these registers following a reset are undefined.

Figure 3 - 85 Format of INTOUT0 Interrupt Source Register 5 (BBINT0REQ5) (1/2)

Address: 00F9H After reset: XXH R

Symbol	7	6	5	4	3	2	1	0
BBINT0 REQ5	RCVTOUT INTREQ	RCVLVL INTREQ	RCVFIN INTREQ	FL INTREQ	RCVSTART INTREQ	PREAMBL INTREQ	CS INTREQ	AGC INTREQ

RCVTOUT INTREQ	Automatic reception timeout interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

RCVLVL INTREQ	Reception level interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

RCVFIN INTREQ	Frame reception completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

FL INTREQ	Frame length or address filtering interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

RCVSTART INTREQ	Reception start interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

Figure 3 - 85 Format of INTOUT0 Interrupt Source Register 5 (BBINT0REQ5) (2/2)

PREAMBL INTREQ	Preamble detection interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

CS INTREQ	Carrier sense interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

AGC INTREQ	AGC completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

3.4.75 INTOUT0 interrupt source register 6 (BBINT0REQ6)

Upon the generation of an interrupt request due to a given interrupt source condition being satisfied while the corresponding interrupt request is enabled, the corresponding interrupt source flag is set to 1 to indicate generation of the interrupt request. Reading this bit only clears it to 0 after it has been read as 1. Dummy-read the bit to clear it because it is not writable. When the setting of at least one of the interrupt source flags in the INTOUT0 interrupt source registers 0 to 7 is 1, and the generation of the corresponding interrupt request is enabled, the 8 bytes of the INTOUT0 interrupt source registers 0 to 7 must be read consecutively with the SEN pin remaining at the low level. The values of these registers following a reset are undefined.

Figure 3 - 86 Format of INTOUT0 Interrupt Source Register 6 (BBINT0REQ6) (1/2)

Address: 00FAH After reset: XXH R

Symbol	7	6	5	4	3	2	1	0
BBINT0REQ6	RCVLVL INTREQ	RCVFIN INTREQ	FL INTREQ	RCVSTART INTREQ	CCALIMIT INTREQ	CCACLR INTREQ	CCA INTREQ	CSMA INTREQ

RCVLVL INTREQ	Reception level interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

RCVFIN INTREQ	Frame reception completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

FL INTREQ	Frame length or address filtering interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

RCVSTART INTREQ	Reception start interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

CCALIMIT INTREQ	CCA limitation interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

Figure 3 - 86 Format of INTOUT0 Interrupt Source Register 6 (BBINT0REQ6) (2/2)

CCACLR INTREQ	CCA clearance or reception canceled interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

CCA INTREQ	CCA completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

CSMA INTREQ	CSMA-CA completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

3.4.76 INTOUT0 interrupt source register 7 (BBINT0REQ7)

Upon the generation of an interrupt request due to a given interrupt source condition being satisfied while the corresponding interrupt request is enabled, the corresponding interrupt source flag is set to 1 to indicate generation of the interrupt request. Reading this bit only clears it to 0 after it has been read as 1. Dummy-read the bit to clear it because it is not writable. When the setting of at least one of the interrupt source flags in the INTOUT0 interrupt source registers 0 to 7 is 1, and the generation of the corresponding interrupt request is enabled, the 8 bytes of the INTOUT0 interrupt source registers 0 to 7 must be read consecutively with the SEN pin remaining at the low level. The values of these registers following a reset are undefined.

Figure 3 - 87 Format of INTOUT0 Interrupt Source Register 7 (BBINT0REQ7) (1/2)

Address: 00FBH After reset: XXH R

Symbol	7	6	5	4	3	2	1	0
BBINT0REQ7	RCVLVL INTREQ	RCVFI NINTREQ	FL INTREQ	RCVSTART INTREQ	ROVR INTREQ	RCVBYTE INTREQ	RCV1 INTREQ	RCV0 INTREQ

RCVLVL INTREQ	Reception level interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

RCVFIN INTREQ	Frame reception completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

FL INTREQ	Frame length or address filtering interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

RCVSTART INTREQ	Reception start interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

ROVR INTREQ	Reception overrun interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

Figure 3 - 87 Format of INTOUT0 Interrupt Source Register 7 (BBINT0REQ7) (2/2)

RCVBYTE INTREQ	Number of received bytes interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

RCV1 INTREQ	Bank 1 reception completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

RCV0 INTREQ	Bank 0 reception completion interrupt source flag
0	No interrupt request has been generated.
1	An interrupt request has been generated.

3.4.77 INTOUT0 interrupt enable register 0 (BBINT0EN0)

An interrupt enable bit enables the output of an interrupt signal on the GPIO port pin selected as the INTOUT0 output pin upon the generation of the corresponding interrupt request. To enable the output of an interrupt signal, set the corresponding interrupt enable bit. The value of this register following a reset is 00H.

Figure 3 - 88 Format of INTOUT0 Interrupt Enable Register 0 (BBINT0EN0) (1/2)

Address: 00FCH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBINT0EN0	CSMAINTEN	FSYNCINTEN	TRN1INTEN	TRN0INTEN	CALINTEN	TIM2INTEN	TIM1INTEN	TIM0INTEN

CSMAINTEN	CSMA-CA completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

FSYNCINTEN	Frame synchronization transmission completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

TRN1INTEN	Bank 1 transmission completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

TRN0INTEN	Bank 0 transmission completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

CALINTEN	Calibration completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

TIM2INTEN	Timer comparison 2 interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

Figure 3 - 88 Format of INTOUT0 Interrupt Enable Register 0 (BBINT0EN0) (2/2)

TIM1 INTEN	Timer comparison 1 interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

TIM0 INTEN	Timer comparison 0 interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

3.4.78 INTOUT0 interrupt enable register 1 (BBINT0EN1)

An interrupt enable bit enables the output of an interrupt signal on the GPIO port pin selected as the INTOUT0 output pin upon the generation of the corresponding interrupt request. To enable the output of an interrupt signal, set the corresponding interrupt enable bit. The value of this register following a reset is 00H.

Figure 3 - 89 Format of INTOUT0 Interrupt Enable Register 1 (BBINT0EN1) (1/2)

Address: 00FDH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBINT0EN1	TRNFININTEN	RCVLVLINTEN	MODESWINTEN	ROVRINTEN	ADRSINTEN	FLINTEN	RCV1INTEN	RCV0INTEN

TRNFININTEN	Frame transmission completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

RCVLVLINTEN	Reception level interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

MODESWINTEN	Mode switch reception completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

ROVRINTEN	Reception overrun interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

ADRSINTEN	Address filtering interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

FLINTEN	Frame length interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

Figure 3 - 89 Format of INTOUT0 Interrupt Enable Register 1 (BBINT0EN1) (2/2)

RCV1 INTEN	Bank 1 reception completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

RCV0 INTEN	Bank 0 reception completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

3.4.79 INTOUT0 interrupt enable register 2 (BBINT0EN2)

An interrupt enable bit enables the output of an interrupt signal on the GPIO port pin selected as the INTOUT0 output pin upon the generation of the corresponding interrupt request. To enable the output of an interrupt signal, set the corresponding interrupt enable bit. The value of this register following a reset is 00H.

Figure 3 - 90 Format of INTOUT0 Interrupt Enable Register 2 (BBINT0EN2) (1/2)

Address: 00FEH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBINT0EN2	PREAMBLINTEN	CCAINTEN	AGCINTEN	RCVBYTEINTEN	RCVFININTEN	RCVSTAINTEN	TRNSTARTINTEN	TRNBYTEINTEN

PREAMBLINTEN	Preamble detection interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

CCAINTEN	CCA completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

AGCINTEN	AGC completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

RCVBYTEINTEN	Number of received bytes interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

RCVFININTEN	Frame reception completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

RCVSTAINTEN	Reception start interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

Figure 3 - 90 Format of INTOUT0 Interrupt Enable Register 2 (BBINT0EN2) (2/2)

TRNSTART INTEN	Transmission start interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

TRNBYTE INTEN	Number of transmitted bytes interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

3.4.80 INTOUT0 interrupt enable register 3 (BBINT0EN3)

An interrupt enable bit enables the output of an interrupt signal on the GPIO port pin selected as the INTOUT0 output pin upon the generation of the corresponding interrupt request. To enable the output of an interrupt signal, set the corresponding interrupt enable bit. The value of this register following a reset is 00H.

Figure 3 - 91 Format of INTOUT0 Interrupt Enable Register 3 (BBINT0EN3)

Address: 00FFH After reset: 00H R/W[Note]

Symbol	7	6	5	4	3	2	1	0
BBINT0EN3	CANCELINTEN	0	0	TRNUNDRRUNINTEN	RCVTOUTINTEN	CCACLRINTEN	CCALIMITINTEN	CSINTEN

CANCELINTEN	Reception canceled interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

TRNUNDRRUNINTEN	Transmission underrun interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

RCVTOUTINTEN	Automatic reception timeout interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

CCACLRINTEN	CCA clearance interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

CCALIMITINTEN	CCA limitation interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

CSINTEN	Carrier sense interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

Caution When writing to this register, set bits 6 and 5 to the value 0.

3.4.81 INTOUT0 interrupt enable register 4 (BBINT0EN4)

An interrupt enable bit enables the output of an interrupt signal on the GPIO port pin selected as the INTOUT0 output pin upon the generation of the corresponding interrupt request. To enable the output of an interrupt signal, set the corresponding interrupt enable bit. The value of this register following a reset is 00H.

Figure 3 - 92 Format of INTOUT0 Interrupt Enable Register 4 (BBINT0EN4) (1/2)

Address: 0100H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBINT0EN4	TRNFININTEN	TRNFSYNCINTEN	TRNSTARTINTEN	CSMAINTEN	TRNUNDRRUNINTEN	TRNBYTEINTEN	TRN1INTEN	TRN0INTEN

TRNFININTEN	Frame transmission completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

TRNFSYNCINTEN	Frame synchronization transmission completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

TRNSTARTINTEN	Transmission start interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

CSMAINTEN	CSMA-CA completion or CCA completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

TRNUNDRRUNINTEN	Transmission underrun interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

TRNBYTEINTEN	Number of transmitted bytes interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

Figure 3 - 92 Format of INTOUT0 Interrupt Enable Register 4 (BBINT0EN4) (2/2)

TRN1 INTEN	Bank 1 transmission completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

TRN0 INTEN	Bank 0 transmission completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

3.4.82 INTOUT0 interrupt enable register 5 (BBINT0EN5)

An interrupt enable bit enables the output of an interrupt signal on the GPIO port pin selected as the INTOUT0 output pin upon the generation of the corresponding interrupt request. To enable the output of an interrupt signal, set the corresponding interrupt enable bit. The value of this register following a reset is 00H.

Figure 3 - 93 Format of INTOUT0 Interrupt Enable Register 5 (BBINT0EN5) (1/2)

Address: 0101H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBINT0EN5	RCVTOUTINTEN	RCVLVLINTEN	RCVFININTEN	FLINTEN	RCVSTARTINTEN	PREAMBLINTEN	CSINTEN	AGCINTEN

RCVTOUTINTEN	Automatic reception timeout interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

RCVLVLINTEN	Reception level interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

RCVFININTEN	Frame reception completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

FLINTEN	Frame length or address filtering interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

RCVSTARTINTEN	Reception start interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

PREAMBLINTEN	Preamble detection interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

Figure 3 - 93 Format of INTOUT0 Interrupt Enable Register 5 (BBINT0EN5) (2/2)

CS INTEN	Carrier sense interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

AGC INTEN	AGC completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

3.4.83 INTOUT0 interrupt enable register 6 (BBINT0EN6)

An interrupt enable bit enables the output of an interrupt signal on the GPIO port pin selected as the INTOUT0 output pin upon the generation of the corresponding interrupt request. To enable the output of an interrupt signal, set the corresponding interrupt enable bit. The value of this register following a reset is 00H.

Figure 3 - 94 Format of INTOUT0 Interrupt Enable Register 6 (BBINT0EN6) (1/2)

Address: 0102H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBINT0EN6	RCVLVLINTEN	RCVFININTEN	FLINTEN	RCVSTARTINTEN	CCALIMITINTEN	CCACLRINTEN	CCAINTEN	CSMAINTEN

RCVLVLINTEN	Reception level interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

RCVFININTEN	Frame reception completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

FLINTEN	Frame length or address filtering interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

RCVSTARTINTEN	Reception start interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

CCALIMITINTEN	CCA limitation interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

CCACLRINTEN	CCA clearance or reception canceled interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

Figure 3 - 94 Format of INTOUT0 Interrupt Enable Register 6 (BBINT0EN6) (2/2)

CCA INTEN	CCA completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

CSMA INTEN	CSMA-CA completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

3.4.84 INTOUT0 interrupt enable register 7 (BBINT0EN7)

An interrupt enable bit enables the output of an interrupt signal on the GPIO port pin selected as the INTOUT0 output pin upon the generation of the corresponding interrupt request. To enable the output of an interrupt signal, set the corresponding interrupt enable bit. The value of this register following a reset is 00H.

Figure 3 - 95 Format of INTOUT0 Interrupt Enable Register 7 (BBINT0EN7) (1/2)

Address: 0103H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBINT0EN7	RCVLVLINTEN	RCVFININTEN	FLINTEN	RCVSTARTINTEN	ROVRINTEN	RCVBYTEINTEN	RCV1INTEN	RCV0INTEN

RCVLVLINTEN	Reception level interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

RCVFININTEN	Frame reception completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

FLINTEN	Frame length or address filtering interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

RCVSTARTINTEN	Reception start interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

ROVRINTEN	Reception overrun interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

RCVBYTEINTEN	Number of received bytes interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

Figure 3 - 95 Format of INTOUT0 Interrupt Enable Register 7 (BBINT0EN7) (2/2)

RCV1 INTEN	Bank 1 reception completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

RCV0 INTEN	Bank 0 reception completion interrupt enable
0	Interrupt signal output is disabled.
1	Interrupt signal output is enabled.

3.4.85 INTOUT0 interrupt source enable register 0 (BBINT0REQEN0)

An interrupt source enable bit enables the generation of interrupt requests in response to the corresponding sources. Upon the generation of an interrupt request while the setting of the corresponding interrupt source enable bit is 1, the corresponding interrupt source flag is set to 1. The value of this register following a reset is 00H.

Figure 3 - 96 Format of INTOUT0 Interrupt Source Enable Register 0 (BBINT0REQEN0) (1/2)

Address: 0104H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBINT0 REQEN0	CSMA INTREQEN	FSYNC INTREQEN	TRN1 INTREQEN	TRN0 INTREQEN	CAL INTREQEN	TIM2 INTREQEN	TIM1 INTREQEN	TIM0 INTREQEN

CSMA INTREQEN	CSMA-CA completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

FSYNC INTREQEN	Frame synchronization transmission completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

TRN1 INTREQEN	Bank 1 transmission completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

TRN0 INTREQEN	Bank 0 transmission completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

CAL INTREQEN	Calibration completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

TIM2 INTREQEN	Timer comparison 2 interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

Figure 3 - 96 Format of INTOUT0 Interrupt Source Enable Register 0 (BBINT0REQEN0) (2/2)

TIM1 INTREQEN	Timer comparison 1 interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

TIM0 INTREQEN	Timer comparison 0 interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

3.4.86 INTOUT0 interrupt source enable register 1 (BBINT0REQEN1)

An interrupt source enable bit enables the generation of interrupt requests in response to the corresponding sources. Upon the generation of an interrupt request while the setting of the corresponding interrupt source enable bit is 1, the corresponding interrupt source flag is set to 1. The value of this register following a reset is 00H.

Figure 3 - 97 Format of INTOUT0 Interrupt Source Enable Register 1 (BBINT0REQEN1) (1/2)

Address: 0105H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBINT0 REQEN1	TRNFININT REQEN	RCVLVL INTREQEN	MODESW INTREQEN	ROVR INTREQEN	ADRS INTREQEN	FL INTREQEN	RCV1 INTREQEN	RCV0 INTREQEN

TRNFININT REQEN	Frame transmission completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

RCVLVL INTREQEN	Reception level interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

MODESW INTREQEN	Mode switch reception completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

ROVR INTREQEN	Reception overrun interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

ADRS INTREQEN	Address filtering interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

FL INTREQEN	Frame length interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

Figure 3 - 97 Format of INTOUT0 Interrupt Source Enable Register 1 (BBINT0REQEN1) (2/2)

RCV1 INTREQEN	Bank 1 reception completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

RCV0 INTREQEN	Bank 0 reception completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

3.4.87 INTOUT0 interrupt source enable register 2 (BBINT0REQEN2)

An interrupt source enable bit enables the generation of interrupt requests in response to the corresponding sources. Upon the generation of an interrupt request while the setting of the corresponding interrupt source enable bit is 1, the corresponding interrupt source flag is set to 1. The value of this register following a reset is 00H.

Figure 3 - 98 Format of INTOUT0 Interrupt Source Enable Register 2 (BBINT0REQEN2) (1/2)

Address: 0106H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBINT0 REQEN2	PREAMBL INTREQEN	CCA INTREQEN	AGC INTREQEN	RCVBYTE INTREQEN	RCVFIN INTREQEN	RCVSTA INTREQEN	TRNSTART INTREQEN	TRNBYTE INTREQEN

PREAMBL INTREQEN	Preamble detection interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

CCA INTREQEN	CCA completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

AGC INTREQEN	AGC completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

RCVBYTE INTREQEN	Number of received bytes interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

RCVFIN INTREQEN	Frame reception completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

RCVSTA INTREQEN	Reception start interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

Figure 3 - 98 Format of INTOUT0 Interrupt Source Enable Register 2 (BBINT0REQEN2) (2/2)

TRNSTART INTREQEN	Transmission start interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

TRNBYTE INTREQEN	Number of transmitted bytes interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

3.4.88 INTOUT0 interrupt source enable register 3 (BBINT0REQEN3)

An interrupt source enable bit enables the generation of interrupt requests in response to the corresponding sources. Upon the generation of an interrupt request while the setting of the corresponding interrupt source enable bit is 1, the corresponding interrupt source flag is set to 1. The value of this register following a reset is 00H.

Figure 3 - 99 Format of INTOUT0 Interrupt Source Enable Register 3 (BBINT0REQEN3) (1/2)

Address: 0107H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBINT0 REQEN3	CANCEL INTREQEN	0	0	TRNUNDRRUN INTREQEN	RCVTOUT INTREQEN	CCACLR INTREQEN	CCALIMIT INTREQEN	CS INTREQEN

CANCEL INTREQEN	Reception canceled interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

TRNUNDRRUN INTREQEN	Transmission underrun interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

RCVTOUT INTREQEN	Automatic reception timeout interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

CCACLR INTREQEN	CCA clearance interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

CCALIMIT INTREQEN	CCA limitation interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

Figure 3 - 99 Format of INTOUT0 Interrupt Source Enable Register 3 (BBINT0REQEN3) (2/2)

CS INTREQEN	Carrier sense interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

Caution When writing to this register, set bits 6 and 5 to the value 0.

3.4.89 INTOUT0 interrupt source enable register 4 (BBINT0REQEN4)

An interrupt source enable bit enables the generation of interrupt requests in response to the corresponding sources. Upon the generation of an interrupt request while the setting of the corresponding interrupt source enable bit is 1, the corresponding interrupt source flag is set to 1. The value of this register following a reset is 00H.

Figure 3 - 100 Format of INTOUT0 Interrupt Source Enable Register 4 (BBINT0REQEN4) (1/2)

Address: 0108H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBINT0 REQEN4	TRNFIN INTREQEN	TRNFSYNC INTREQEN	TRNSTART INTREQEN	CSMA INTREQEN	TRNUNDRR UN INTREQEN	TRNBYTE INTREQEN	TRN1 INTREQEN	TRN0 INTREQEN

TRNFIN INTREQEN	Frame transmission completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

TRNFSYNC INTREQEN	Frame synchronization transmission completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

TRNSTART INTREQEN	Transmission start interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

CSMA INTREQEN	CSMA-CA completion or CCA completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

TRNUNDRR UN INTREQEN	Transmission underrun interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

Figure 3 - 100 Format of INTOUT0 Interrupt Source Enable Register 4 (BBINT0REQEN4) (2/2)

TRNBYTE INTREQEN	Number of transmitted bytes interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

TRN1 INTREQEN	Bank 1 transmission completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

TRN0 INTREQEN	Bank 0 transmission completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

3.4.90 INTOUT0 interrupt source enable register 5 (BBINT0REQEN5)

An interrupt source enable bit enables the generation of interrupt requests in response to the corresponding sources. Upon the generation of an interrupt request while the setting of the corresponding interrupt source enable bit is 1, the corresponding interrupt source flag is set to 1. The value of this register following a reset is 00H.

Figure 3 - 101 Format of INTOUT0 Interrupt Source Enable Register 5 (BBINT0REQEN5) (1/2)

Address: 0109H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBINT0 REQEN5	RCVTOUT INTREQEN	RCVLVL INTREQEN	RCVFIN INTREQEN	FL INTREQEN	RCVSTART INTREQEN	PREAMBL INTREQEN	CS INTREQEN	AGC INTREQEN

RCVTOUT INTREQEN	Automatic reception timeout interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

RCVLVL INTREQEN	Reception level interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

RCVFIN INTREQEN	Frame reception completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

FL INTREQEN	Frame length or address filtering interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

RCVSTART INTREQEN	Reception start interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

Figure 3 - 101 Format of INTOUT0 Interrupt Source Enable Register 5 (BBINT0REQEN5) (2/2)

PREAMBL INTREQEN	Preamble detection interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

CS INTREQEN	Carrier sense interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

AGC INTREQEN	AGC completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

3.4.91 INTOUT0 interrupt source enable register 6 (BBINT0REQEN6)

An interrupt source enable bit enables the generation of interrupt requests in response to the corresponding sources. Upon the generation of an interrupt request while the setting of the corresponding interrupt source enable bit is 1, the corresponding interrupt source flag is set to 1. The value of this register following a reset is 00H.

Figure 3 - 102 Format of INTOUT0 Interrupt Source Enable Register 6 (BBINT0REQEN6) (1/2)

Address: 010AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBINT0 REQEN6	RCVLVL INTREQEN	RCVFIN INTREQEN	FL INTREQEN	RCVSTART INTREQEN	CCALIMIT INTREQEN	CCACLR INTREQEN	CCA INTREQEN	CSMA INTREQEN

RCVLVL INTREQEN	Reception level interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

RCVFIN INTREQEN	Frame reception completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

FL INTREQEN	Frame length or address filtering interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

RCVSTART INTREQEN	Reception start interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

CCALIMIT INTREQEN	CCA limitation interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

Figure 3 - 102 Format of INTOUT0 Interrupt Source Enable Register 6 (BBINT0REQEN6) (2/2)

CCACLR INTREQEN	CCA clearance or reception canceled interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

CCA INTREQEN	CCA completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

CSMA INTREQEN	CSMA-CA completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

3.4.92 INTOUT0 interrupt source enable register 7 (BBINT0REQEN7)

An interrupt source enable bit enables the generation of interrupt requests in response to the corresponding sources. Upon the generation of an interrupt request while the setting of the corresponding interrupt source enable bit is 1, the corresponding interrupt source flag is set to 1. The value of this register following a reset is 00H.

Figure 3 - 103 Format of INTOUT0 Interrupt Source Enable Register 7 (BBINT0REQEN7) (1/2)

Address: 010BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBINT0 REQEN7	RCVLVL INTREQEN	RCVFIN INTREQEN	FL INTREQEN	RCVSTART INTREQEN	ROVR INTREQEN	RCVBYTE INTREQEN	RCV1 INTREQEN	RCV0 INTREQEN

RCVLVL INTREQEN	Reception level interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

RCVFIN INTREQEN	Frame reception completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

FL INTREQEN	Frame length or address filtering interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

RCVSTART INTREQEN	Reception start interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

ROVR INTREQEN	Reception overrun interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

Figure 3 - 103 Format of INTOUT0 Interrupt Source Enable Register 7 (BBINT0REQEN7) (2/2)

RCVBYTE INTREQEN	Number of received bytes interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

RCV1 INTREQEN	Bank 1 reception completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

RCV0 INTREQEN	Bank 0 reception completion interrupt source enable
0	Interrupt request generation is disabled.
1	Interrupt request generation is enabled.

3.4.93 Number-of-transmitted-byte interrupt comparison register (BBTRNINTCOMP)

This register is used to generate interrupts depending on the number of transmitted bytes. An interrupt request is generated when the specified number of bytes are transferred from the transmission RAM to the transmitter. The value specified in this register can be modified even while transmission is in progress. In this case, the new value takes effect after an interrupt is generated based on the old value. The value of this register following a reset is 0010H.

Figure 3 - 104 Format of Number-of-Transmitted-Byte Interrupt Comparison Register (BBTRNINTCOMP)

Address: 0117H, 0116H After reset: 0010H R/W

Symbol	15	14	13	12	11	10	9	8
BBTRNINT COMP (0117H)	0	0	0	0	TRNINT COMP11	TRNINT COMP10	TRNINT COMP9	TRNINT COMP8
	7	6	5	4	3	2	1	0
(0116H)	TRNINT COMP7	TRNINT COMP6	TRNINT COMP5	TRNINT COMP4	TRNINT COMP3	TRNINT COMP2	TRNINT COMP1	TRNINT COMP0

TRNINTCOMP11 to TRNINTCOMP0	Number-of-transmit-byte interrupt compare
—	These bits set the number of bytes that generates a number-of-transmit-byte interrupt.

Caution When writing to this register, set bits 15 to 12 to the value 0.

3.4.94 CCA mode register (BBCCAMODE)

The CCA mode can be specified by the CCA mode bits.

1. CCA mode bits = 00B: CCA proceeds by comparing the detected power value with the CCAVTH value.
2. CCA mode bits = 01B: CCA proceeds by checking whether the sensed carrier signal is detected.
3. CCA mode bits = 10B: CCA proceeds by the logical OR of the results of (1) and (2).
4. CCA mode bits = 11B: CCA proceeds by the logical AND of the results of (1) and (2).

The CCA continuation enable bit is used to continue CCA until the frequency channel is found to be cleared, instead of terminating the operation after CCA. When CCA is proceeds in this continuation enabled mode, this device updates the values in the CCA judge result bit, and ED1 result register and ED2 result register on detection of power value and continues CCA until the frequency channel is found to be cleared. To stop CCA, use the RF communication stop bit. CCA also stops after the frequency channel is found to be cleared (including the case when the frequency channel is cleared at the start of CCA). Be sure to use the continuation mode only while the CCA mode bits are set to 00B. Note that, when the setting of the CCA mode bit is 1, do not set the mid-CCA reception enable bit or the automatic CSMA-CA start bit to 1. This mode cannot be used together with the mid-CCA reception enable mode or the automatic CSMA-CA mode. The CCA continuation mode bit switches the operating mode when CCA continuation is enabled. While this bit is set to 1, CCA stops when the number of CCA repetitions reaches the value specified in the CCA limit setting register. While this bit is set to 0, CCA stops after the frequency channel is found to be cleared. The mid-CCA reception enable bit is used to stop CCA and proceed to frame reception when signal reception is detected during CCA. This mode cannot be used together with the automatic CSMA-CA mode. In addition, the automatic receive switch mode or high-speed receive switch function cannot be used. Once the reception start operation begins, a CCA completion interrupt is generated. As the receive operation is triggered by the reception start signal, the hardware may cancel the reception — for example, if an illegal frame length is detected. In this case, a reception cancellation interrupt is generated. If reception is canceled in this mode, this device does not return to the receive wait state. The value of this register following a reset is 00H.

Figure 3 - 105 Format of CCA Mode Register (BBCCAMODE) (1/2)

Address: 0118H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBCCA MODE	0	0	0	CCA RCVEN	CCACONT INUESEL	CCACONT INUEEN	CCA MODE1	CCA MODE0

CCA RCVEN	Mid-CCA reception enable
0	Normal operation.
1	Reception is enabled during CCA.

CCACON TINUESEL	CCA continuation mode
0	CCA continues until the frequency channel is found to be cleared.
1	CCA continues until the specified count is reached.

Figure 3 - 105 Format of CCA Mode Register (BBCCAMODE) (2/2)

CCACONTINUEEN	CCA continuation enable
0	Normal operation (CCA stops after execution).
1	CCA is continued.

CCA MODE1	CCA MODE0	CCA mode
0	0	Power value is compared with CCAVTH.
0	1	Whether the sensed carrier signal is detected is checked.
1	0	Logical OR of the results of the above checks.
1	1	Logical AND of the results of the above checks.

Caution When writing to this register, set bits 7 to 5 to the value 0.

3.4.95 Receive mode register (BBRCVMODE)

The MS frame discard bit is used to discard the mode switch frame received. When a mode switch frame is received while this bit is set to 1, this device automatically enters the IDLE state and then returns to the receive wait state again. Note that a mode switch reception completion interrupt does not occur even if a mode switch frame is received. In this case, the mode switch frame reception register is not updated. The value of this register following a reset is 00H.

Figure 3 - 106 Format of Receive Mode Register (BBRCVMODE)

Address: 0119H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBRCV MODE	0	0	0	0	0	0	0	MSCANCEL EN

MSCANCEL EN	MS frame discard
0	Mode switch frame is not discarded.
1	Mode switch frame is discarded.

Caution When writing to this register, set bits 7 to 1 to the value 0.

3.4.96 Frame cancellation minimum length register (BBFLCNCLMIN)

This register is used to set the length of the received frame to be discarded. When the length of the received frame is equal to or smaller than the value specified in this register, this device discards the frame. Set a value from 0002H to 07FFH. Note that the received frame is always discarded regardless of this setting if its length is 4 bytes or smaller for a frame with the 32-bit CRC or 2 bytes or smaller for a frame with the 16-bit CRC. The value of this register following a reset is 0002H.

Figure 3 - 107 Format of Frame Cancellation Minimum Length Register (BBFLCNCLMIN)

Address: 011BH, 011AH After reset: 0002H R/W

Symbol	15	14	13	12	11	10	9	8
BBFLCNCLMIN (011BH)	0	0	0	0	0	FLCNCLMIN10	FLCNCLMIN9	FLCNCLMIN8
	7	6	5	4	3	2	1	0
(011AH)	FLCNCLMIN7	FLCNCLMIN6	FLCNCLMIN5	FLCNCLMIN4	FLCNCLMIN3	FLCNCLMIN2	FLCNCLMIN1	FLCNCLMIN0

FLCNCLMIN10 to FLCNCLMIN0	Minimum frame length for comparison
—	These bits set the length of the received frame to be discarded.

Caution When writing to this register, set bits 15 to 11 to the value 0.

3.4.97 Frame cancellation maximum length register (BBFLCNCLMAX)

This register is used to set the length of the received frame to be discarded. When the length of the received frame is equal to or greater than the value specified in this register, this device discards the frame. Set a value from 0008H to 0800H. To stop discarding a frame, specify 0800H. The value of this register following a reset is 0800H.

Figure 3 - 108 Format of Frame Cancellation Maximum Length Register (BBFLCNCLMAX)

Address: 011DH, 011CH After reset: 0800H R/W

Symbol	15	14	13	12	11	10	9	8
BBFLCNCLMAX (011DH)	0	0	0	0	FLCNCLMAX11	FLCNCLMAX10	FLCNCLMAX9	FLCNCLMAX8
	7	6	5	4	3	2	1	0
(011CH)	FLCNCLMAX7	FLCNCLMAX6	FLCNCLMAX5	FLCNCLMAX4	FLCNCLMAX3	FLCNCLMAX2	FLCNCLMAX1	FLCNCLMAX0

FLCNCLMAX11 to FLCNCLMAX0	Frame cancellation maximum length for comparison
—	These bits set the length of the received frame to be discarded.

Caution When writing to this register, set bits 15 to 11 to the value 0.

3.4.98 Number-of-byte interrupt mode register (BBBYTEINTMODE)

The number-of-transmit-byte interrupt mode bit and number-of-receive-byte interrupt mode bit are used to specify the conditions for generating number-of-transmit-byte interrupts and number-of-receive-byte interrupts, respectively. The ADF link bit for the number-of-receive-byte interrupt is used to link the address match detected by the address filter (when enabled) to the condition for the number-of-receive-byte interrupt when the number-of-receive-byte interrupt mode bit is set to 1. When this link is enabled, a number-of-receive-byte interrupt is generated only after the reception of a byte following the detection of an address match. The value of this register following a reset is 07H.

Figure 3 - 109 Format of Number-of-Byte Interrupt Mode Register (BBBYTEINTMODE)

Address: 011EH After reset: 07H R/W

Symbol	7	6	5	4	3	2	1	0
BBBYTE INTMODE	0	0	0	0	0	RXCOUNT INTADF	RXCOUNT INTSEL	TXCOUNT INTSEL

RXCOUNT INTADF	ADF link with the number-of-receive-byte interrupt
0	Interrupt generation is independent of the address match detected by the address filter.
1	Interrupt generation is linked with the address match detected by the address filter.

RXCOUNT INTSEL	Number-of-receive-byte interrupt mode
0	An interrupt is generated only one time after the number of bytes is specified.
1	An interrupt is generated every time the specified number of bytes is reached.

TXCOUNT INTSEL	Number-of-transmit-byte interrupt mode
0	An interrupt is generated only one time after the number of bytes is specified.
1	An interrupt is generated every time the specified number of bytes is reached.

Caution When writing to this register, set bits 7 to 3 to the value 0.

3.4.99 RSSI result register (BBRSSIRSLT)

This register holds the RSSI result value. The 10-bit power value at the start of reception is stored in the RSSIRSLT bits. The RSSI result corresponding to the save bank specified by the receive data save bank select bit is read from this register. The read value is a 2's complement indicating a value from -256.0 dBm to +255.5 dBm in steps of 0.5 dBm. The unit of indication is dBm. For example, 33DH indicates -97.5 dBm. The value of this register following a reset is 0200H.

Figure 3 - 110 Format of RSSI Result Register (BBRSSIRSLT)

Address: 0121H, 0120H After reset: 0200H R

Symbol	15	14	13	12	11	10	9	8
BBRSSIRSLT (0121H)	0	0	0	0	0	0	RSSIRSLT9	RSSIRSLT8
	7	6	5	4	3	2	1	0
(0120H)	RSSIRSLT7	RSSIRSLT6	RSSIRSLT5	RSSIRSLT4	RSSIRSLT3	RSSIRSLT2	RSSIRSLT1	RSSIRSLT0

RSSIRSLT9 to RSSIRSLT0	RSSI result value
—	10-bit RSSI result value

3.4.100 RCPI result register (BBRCPIRSLT)

This register holds the RCPI result value. The 10-bit average of the received power values is stored in the RCPIRSLT bits. The RCPI result corresponding to the save bank specified by the receive data save bank select bit is read from this register. The read value is a 2's complement indicating a value from -256.0 dBm to +255.5 dBm in steps of 0.5 dBm. The unit of indication is dBm. For example, 33DH indicates -97.5 dBm. The value of this register following a reset is 0200H.

Figure 3 - 111 Format of RCPI Result Register (BBRCPIRSLT)

Address: 0123H, 0122H After reset: 0200H R

Symbol	15	14	13	12	11	10	9	8
BBRCPIRSLT (0123H)	0	0	0	0	0	0	RCPIRSLT9	RCPIRSLT8
	7	6	5	4	3	2	1	0
(0122H)	RCPIRSLT7	RCPIRSLT6	RCPIRSLT5	RCPIRSLT4	RCPIRSLT3	RCPIRSLT2	RCPIRSLT1	RCPIRSLT0

RCPIRSLT9 to RCPIRSLT0	RCPI result value
—	10-bit RCPI result value

3.4.101 RSSI result 2 register (BBRSSIRSLT2)

This register holds the RSSI result value. The 8-bit power value at the start of reception is stored in the RSSIRSLT2 bits. The RSSI result corresponding to the save bank specified by the receive data save bank select bit is read from this register. The read value is a 2's complement indicating a value from -128 dBm to +127 dBm in steps of 1 dBm. The unit of indication is dBm. For example, 9EH indicates -98 dBm. The value of this register following a reset is 80H.

Figure 3 - 112 Format of RSSI Result 2 Register (BBRSSIRSLT2)

Address: 0124H After reset: 80H R

Symbol	7	6	5	4	3	2	1	0
BBRSSIRSLT2	RSSIRSLT27	RSSIRSLT26	RSSIRSLT25	RSSIRSLT24	RSSIRSLT23	RSSIRSLT22	RSSIRSLT21	RSSIRSLT20

RSSIRSLT27 to RSSIRSLT20	RSSI result value 2
—	8-bit RSSI result value

3.4.102 RCPI result 2 register (BBRCPIRSLT2)

This register holds the RCPI result value. The 8-bit average of the received power values is stored in the RCPIRSLT2 bits. The RCPI result corresponding to the save bank specified by the receive data save bank select bit is read from this register. The read value is a 2's complement indicating a value from -128 dBm to +127 dBm in steps of 1 dBm. The unit of indication is dBm. For example, 9EH indicates -98 dBm. The value of this register following a reset is 80H.

Figure 3 - 113 Format of RCPI Result 2 Register (BBRCPIRSLT2)

Address: 0125H After reset: 80H R

Symbol	7	6	5	4	3	2	1	0
BBRCPIRSLT2	RCPIRSLT27	RCPIRSLT26	RCPIRSLT25	RCPIRSLT24	RCPIRSLT23	RCPIRSLT22	RCPIRSLT21	RCPIRSLT20

RCPIRSLT27 to RCPIRSLT20	RCPI result value 2
—	8-bit RCPI result value

3.4.103 ED1 result register (BBED1RSLT)

This register holds the ED result value in FSK modulation. The value is retained until the next CCA operation begins. A 10-bit power value is stored in the ED1RSLT bits. The read value is a 2's complement indicating a value from -256.0 dBm to +255.5 dBm in steps of 0.5 dBm. The unit of indication is dBm. For example, 33DH indicates -97.5 dBm. The value of this register following a reset is 0200H.

Figure 3 - 114 Format of ED1 Result Register (BBED1RSLT)

Address: 0127H, 0126H After reset: 0200H R

Symbol	15	14	13	12	11	10	9	8
BBED1RSLT (0127H)	0	0	0	0	0	0	ED1RSLT9	ED1RSLT8
	7	6	5	4	3	2	1	0
(0126H)	ED1RSLT7	ED1RSLT6	ED1RSLT5	ED1RSLT4	ED1RSLT3	ED1RSLT2	ED1RSLT1	ED1RSLT0

ED1RSLT9 to ED1RSLT0	ED result value
—	10-bit ED result value

3.4.104 ED2 result register (BBED2RSLT)

This register holds the ED result value in OFDM modulation. The value is retained until the next CCA operation begins. A 10-bit power value is stored in the ED2RSLT bits. The read value is a 2's complement indicating a value from -256.0 dBm to +255.5 dBm in steps of 0.5 dBm. The unit of indication is dBm. For example, 33DH indicates -97.5 dBm. The value of this register following a reset is 0200H.

Figure 3 - 115 Format of ED2 Result Register (BBED2RSLT)

Address: 0129H, 0128H After reset: 0200H R

Symbol	15	14	13	12	11	10	9	8
BBED2RSLT (0129H)	0	0	0	0	0	0	ED2RSLT9	ED2RSLT8
	7	6	5	4	3	2	1	0
(0128H)	ED2RSLT7	ED2RSLT6	ED2RSLT5	ED2RSLT4	ED2RSLT3	ED2RSLT2	ED2RSLT1	ED2RSLT0

ED2RSLT9 to ED2RSLT0	ED result value
—	10-bit ED result value

3.4.105 ED1 result 2 register (BBED1RSLT2)

This register holds the ED result value in FSK modulation. The value is retained until the next CCA operation begins. An 8-bit power value is stored in the ED1RSLT2 bits. The read value is a 2's complement indicating a value from -128 dBm to +127 dBm in steps of 1 dBm. The unit of indication is dBm. For example, 9EH indicates -98 dBm. The value of this register following a reset is 80H.

Figure 3 - 116 Format of ED1 Result 2 Register (BBED1RSLT2)

Address: 012AH After reset: 80H R

Symbol	7	6	5	4	3	2	1	0
BBED1RSLT2	ED1RSLT27	ED1RSLT26	ED1RSLT25	ED1RSLT24	ED1RSLT23	ED1RSLT22	ED1RSLT21	ED1RSLT20

ED1RSLT27 to ED1RSLT20	ED result value 2
—	8-bit ED result value

3.4.106 ED2 result 2 register (BBED2RSLT2)

This register holds the ED result value in OFDM modulation. The value is retained until the next CCA operation begins. An 8-bit power value is stored in the ED2RSLT2 bits. The read value is a 2's complement indicating a value from -128 dBm to +127 dBm in steps of 1 dBm. The unit of indication is dBm. For example, 9EH indicates -98 dBm. The value of this register following a reset is 80H.

Figure 3 - 117 Format of ED2 Result 2 Register (BBED2RSLT2)

Address: 012BH After reset: 80H R

Symbol	7	6	5	4	3	2	1	0
BBED1RSLT2	ED2RSLT27	ED2RSLT26	ED2RSLT25	ED2RSLT24	ED2RSLT23	ED2RSLT22	ED2RSLT21	ED2RSLT20

ED2RSLT27 to ED2RSLT20	ED result value 2
—	8-bit ED result value

3.4.107 CCA clearance count register (BBCCACLRCOUNT)

This register is used to set the maximum number of clear operations while the CCA continuation enable bit is set to 1. When the number of clear operations reaches the value specified in this register, a CCA clearance interrupt is generated and the CCA operation is stopped. Set a value from 01H to 03H. The value of this register following a reset is 01H.

Figure 3 - 118 Format of CCA Clearance Count Register (BBCCACLRCOUNT)

Address: 012DH After reset: 01H R/W

Symbol	7	6	5	4	3	2	1	0
BBCCACLRCOUNT	0	0	0	0	0	0	CCACLRCOUNT1	CCACLRCOUNT0

CCACLRCOUNT1, 0	Number of CCA clear operations
—	Maximum number of CCA clear operations

Caution When writing to this register, set bits 7 to 2 to the value 0.

3.4.108 CCA limit setting register (BBCCALIMIT)

This register is used to set the limit on the number of CCA repetitions when the CCA continuation mode bit is set to 1. This device stops the continuation of CCA operation when the number of CCA repetitions reaches the value specified in this register. In this case, a CCA limit interrupt is generated. The value of this register following a reset is 0100H.

Figure 3 - 119 Format of CCA Limit Setting Register (BBCCALIMIT)

Address: 012FH, 012EH After reset: 0100H R/W

Symbol	15	14	13	12	11	10	9	8
BBCCALIMIT (012FH)	CCALIMIT15	CCALIMIT14	CCALIMIT13	CCALIMIT12	CCALIMIT11	CCALIMIT10	CCALIMIT9	CCALIMIT8
	7	6	5	4	3	2	1	0
(012EH)	CCALIMIT7	CCALIMIT6	CCALIMIT5	CCALIMIT4	CCALIMIT3	CCALIMIT2	CCALIMIT1	CCALIMIT0

CCALIMIT15 to CCALIMIT0	CCA repetition limit
—	Maximum number of CCA repetitions until the frequency channel is found to be cleared

3.4.109 Comparison 0 setting excess time registers (BBPASSTIME0 and BBPASSTIME1)

These registers are used to set the maximum elapsed time after the time specified in timer comparison register 0 is reached while both the COMP0 transmit trigger enable bit and the COMP0-excess transmission enable bit are set enabled. This device transmits data when the difference between the timer count value and the value specified in the timer comparison registers 0 and 1 (BBTCOMP0REG0 and BBTCOMP0REG1) is equal to or smaller than the time specified in these registers. The value of these registers following a reset is 80000000H.

Figure 3 - 120 Format of Comparison 0 Setting Excess Time Registers (BBPASSTIME0 and BBPASSTIME1)

Address: 0131H, 0130H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBPASSTIME0 (0131H)	PASSTIME015	PASSTIME014	PASSTIME013	PASSTIME012	PASSTIME011	PASSTIME010	PASSTIME09	PASSTIME08
	7	6	5	4	3	2	1	0
(0130H)	PASSTIME07	PASSTIME06	PASSTIME05	PASSTIME04	PASSTIME03	PASSTIME02	PASSTIME01	PASSTIME00

PASSTIME015 to PASSTIME00	Comparison 0 setting excess time register 0

Address: 0133H, 0132H After reset: 8000H R/W

Symbol	15	14	13	12	11	10	9	8
BBPASSTIME1 (0133H)	PASSTIME115	PASSTIME114	PASSTIME113	PASSTIME112	PASSTIME111	PASSTIME110	PASSTIME19	PASSTIME18
	7	6	5	4	3	2	1	0
(0132H)	PASSTIME17	PASSTIME16	PASSTIME15	PASSTIME14	PASSTIME13	PASSTIME12	PASSTIME11	PASSTIME10

PASSTIME115 to PASSTIME10	Comparison 0 setting excess time register 1

3.4.110 Frame synchronization power value read register (BBFSYNCPOWRD)

This register holds the power value of the frame synchronization section of the frame being received. The 10-bit power value of the frame synchronization section is stored in the FSYNCPOWRD bits. The receive level filter function uses this power value. The read value is a 2's complement indicating a value from -256.0 dBm to +255.5 dBm in steps of 0.5 dBm. The unit of indication is dBm. For example, 33DH indicates -97.5 dBm. The value of this register following a reset is 0200H.

Figure 3 - 121 Format of Frame Synchronization Power Value Read Register (BBFSYNCPOWRD)

Address: 0135H, 0134H After reset: 0200H R

Symbol	15	14	13	12	11	10	9	8
BBFSYNCPOWRD (0135H)	0	0	0	0	0	0	FSYNCPOWRD9	FSYNCPOWRD8
	7	6	5	4	3	2	1	0
(0134H)	FSYNCPOWRD7	FSYNCPOWRD6	FSYNCPOWRD5	FSYNCPOWRD4	FSYNCPOWRD3	FSYNCPOWRD2	FSYNCPOWRD1	FSYNCPOWRD0

FSYNCPOWRD9 to FSYNCPOWRD0	Frame synchronization power value read
—	10-bit power value of the frame synchronization section in the frame being received

3.4.111 Frame synchronization power value 2 read register (BBFSYNCPOWRD2)

This register holds the power value of the frame synchronization section of the frame being received. The 8-bit power value at the start of reception is stored in the FSYNCPOWRD2 bits. The read value is a 2's complement indicating a value from -128 dBm to +127 dBm in steps of 1 dBm. The unit of indication is dBm. For example, 9EH indicates -98 dBm. The value of this register following a reset is 80H.

Figure 3 - 122 Format of Frame Synchronization Power Value 2 Read Register (BBFSYNCPOWRD2)

Address: 0136H After reset: 80H R

Symbol	7	6	5	4	3	2	1	0
BBFSYNCPOWRD2	FSYNCPOWRD27	FSYNCPOWRD26	FSYNCPOWRD25	FSYNCPOWRD24	FSYNCPOWRD23	FSYNCPOWRD22	FSYNCPOWRD21	FSYNCPOWRD20

FSYNCPOWRD27 to FSYNCPOWRD20	Frame synchronization power value read
—	8-bit power value of the frame synchronization section in the frame being received

3.4.112 RSSI read register (BBRSSIRD)

This register holds the RSSI value of the frame being received. The 10-bit power value at the start of reception is stored in the RSSIRD bits. The read value is a 2's complement indicating a value from -256.0 dBm to +255.5 dBm in steps of 0.5 dBm. The unit of indication is dBm. For example, 33DH indicates -97.5 dBm. The value of this register following a reset is 0200H.

Figure 3 - 123 Format of RSSI Read Register (BBRSSIRD)

Address: 0139H, 0138H After reset: 0200H R

Symbol	15	14	13	12	11	10	9	8
BBRSSIRD (0139H)	0	0	0	0	0	0	RSSIRD9	RSSIRD8
	7	6	5	4	3	2	1	0
(0138H)	RSSIRD7	RSSIRD6	RSSIRD5	RSSIRD4	RSSIRD3	RSSIRD2	RSSIRD1	RSSIRD0

RSSIRD9 to RSSIRD0	RSSI read value
—	10-bit RSSI value of the frame being received

3.4.113 RCPI read register (BBRCPIRD)

This register holds the RCPI value of the frame being received. The 10-bit average of the received power values is stored in the RCPIRD bits. The read value is a 2's complement indicating a value from -256.0 dBm to +255.5 dBm in steps of 0.5 dBm. The unit of indication is dBm. For example, 33DH indicates -97.5 dBm. The value of this register following a reset is 0200H.

Figure 3 - 124 Format of RCPI Read Register (BBRCPIRD)

Address: 013BH, 013AH After reset: 0200H R

Symbol	15	14	13	12	11	10	9	8
BBRCPIRD (013BH)	0	0	0	0	0	0	RCPIRD9	RCPIRD8
	7	6	5	4	3	2	1	0
(013AH)	RCPIRD7	RCPIRD6	RCPIRD5	RCPIRD4	RCPIRD3	RCPIRD2	RCPIRD1	RCPIRD0

RCPIRD9 to RCPIRD0	RCPI read value
—	10-bit RCPI value of the frame being received

3.4.114 RSSI read 2 register (BBRSSIRD2)

This register holds the RSSI value of the frame being received. The 8-bit power value at the start of reception is stored in the RSSIRD2 bits. The read value is a 2's complement indicating a value from -128 dBm to +127 dBm in steps of 1 dBm. The unit of indication is dBm. For example, 9EH indicates -98 dBm. The value of this register following a reset is 80H.

Figure 3 - 125 Format of RSSI Read 2 Register (BBRSSIRD2)

Address: 013CH After reset: 80H R

Symbol	7	6	5	4	3	2	1	0
BBRSSIRD2	RSSIRD27	RSSIRD26	RSSIRD25	RSSIRD24	RSSIRD23	RSSIRD22	RSSIRD21	RSSIRD20

RSSIRD27 to RSSIRD20	RSSI read value
—	8-bit RSSI value of the frame being received

3.4.115 RCPI read 2 register (BBRCPIRD2)

This register holds the RCPI value of the frame being received. The 8-bit average of the received power values is stored in the RCPIRD2 bits. The read value is a 2's complement indicating a value from -128 dBm to +127 dBm in steps of 1 dBm. The unit of indication is dBm. For example, 9EH indicates -98 dBm. The value of this register following a reset is 80H.

Figure 3 - 126 Format of RCPI Read 2 Register (BBRCPIRD2)

Address: 013DH After reset: 80H R

Symbol	7	6	5	4	3	2	1	0
BBRCPIRD2	RCPIRD27	RCPIRD26	RCPIRD25	RCPIRD24	RCPIRD23	RCPIRD22	RCPIRD21	RCPIRD20

RCPIRD27 to RCPIRD20	RCPI read value
—	8-bit RCPI value of the frame being received

3.4.116 Transmission and reception method selection register (BBTRXSEL)

The transmission method selection bit and reception method selection bit are used to select the transmission and reception methods, respectively. The CCA method selection bits select the CCA method. The value of this register following a reset is 00H.

Figure 3 - 127 Format of Transmission and Reception Method Selection Register (BBTRXSEL)

Address: 0140H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBTRXSEL	0	0	CCAMODE1	CCAMODE0	RXMODE1	RXMODE0	0	TXMODE

CCAMODE1	CCAMODE0	CCA method selection
0	0	FSK
0	1	OFDM
1	0	Setting prohibited
1	1	FSK and OFDM

RXMODE1	RXMODE0	Reception method selection
0	0	FSK
0	1	OFDM
1	0	Setting prohibited
1	1	FSK and OFDM

TXMODE	Transmission method selection
0	FSK
1	OFDM

Caution When writing to this register, set bits 7, 6, and 1 to the value 0.

3.4.117 Reception method check register (BBRXMODEMONI)

This register is used to check the current reception method. The reception method is stored in this register at the same time as the frame length value is stored. The reception method value corresponding to the save bank specified by the receive data save bank select bit is read from this register. The value of this register following a reset is 00H.

Figure 3 - 128 Format of Reception Method Check Register (BBRXMODEMONI)

Address: 0141H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
BBRXMODEMONI	0	0	0	0	0	0	0	RXMODEMONI

RXMODEMONI	Reception method check
0	FSK
1	OFDM

3.4.118 Reception prohibition register (BBRXPROHIBIT)

The reception prohibition bit is used to prohibit reception. The reception prohibition bit is set to 1 upon reception of every frame while the reception prohibition enable bit is set to 1. In this state, this device does not receive but discards the next frame and the MODEM circuit block is reset. To receive the next frame, clear the prohibition bit to 0. This bit can also be set to 1 by writing 1 to the bit. The reception prohibition enable bit enables the function of the reception prohibition bit. While the enable bit is set to 1, the prohibition bit can be used to prohibit reception. The value of this register following a reset is 00H.

Figure 3 - 129 Format of Reception Prohibition Register (BBRXPROHIBIT)

Address: 0142H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBRXPROHIBIT	0	0	0	0	0	0	RXPROHIBITEN	RXPROHIBIT

RXPROHIBITEN	Reception prohibition bit enable
0	Reception prohibition bit is disabled.
1	Reception prohibition bit is enabled.

RXPROHIBIT	Reception prohibition
0	Reception is allowed.
1	Reception is prohibited.

Caution When writing to this register, set bits 7 to 2 to the value 0.

3.4.119 Received frame counter control register (BBRCVCOUNTCNT)

The receive frame counter reset bit is used to reset the total reception counter, PHR error count register, number-of-successful-receptions counter, and number-of-unsuccessful-receptions counter to 00000000H together. After 1 is written, this bit is automatically cleared to 0. The counting of discarded frames by the PHR error counter can be enabled or disabled by the respective bits as follows.

MS discard count enable bit: Counting of discarded mode switch frames

Minimum value FL cancellation count enable bit: Counting of received frames discarded due to the frame length equal to or smaller than the value specified in the frame cancellation minimum length register

Maximum value FL cancellation count enable bit: Counting of received frames discarded due to the frame length equal to or greater than the value specified in the frame cancellation maximum length register

MS error count enable bit: Counting of received mode switch frames including a PC error

HCS error count enable bit: Counting of received frames including an HCS check error in the PHR, which is detected by the MODEM block

The value of this register following a reset is 00H.

Figure 3 - 130 Format of Received Frame Counter Control Register (BBRCVCOUNTCNT) (1/2)

Address: 0143H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBRCVCOUNTCNT	0	0	HCSERRCOUNTEN	MSERRCOUNTEN	FLMAXCOUNTEN	FLMINCOUNTEN	MSCOUNTEN	RCVCOUNTRST

HCSERRCOUNTEN	HCS error count enable
0	Counting is disabled.
1	Counting is enabled.

MSERRCOUNTEN	MS error count enable
0	Counting is disabled.
1	Counting is enabled.

FLMAXCOUNTEN	Maximum value FL cancellation count enable
0	Counting is disabled.
1	Counting is enabled.

Figure 3 - 130 Format of Received Frame Counter Control Register (BBRCVCOUNTCNT) (2/2)

FLMIN COUNTEN	Minimum value FL cancellation count enable
0	Counting is disabled.
1	Counting is enabled.

MS COUNTEN	MS discard count enable
0	Counting is disabled.
1	Counting is enabled.

RCV COUNTRST	Receive frame counter reset
0	No operation
1	Counters are reset.

Caution When writing to this register, set bits 7 and 6 to the value 0.

3.4.120 Total reception counter (BBRCVCOUNT)

This counter indicates the total number of received frames from which frame synchronization is detected. When the value read from the lowest-order byte at address 0144H is 00H in a state other than IDLE, re-read from the lowest-order byte at the given address. Note that re-reading from the lowest-order byte should be done before the counter has counted to 256 so that the value of the lowest-order byte becomes 00H. This counter can be reset by setting the receive frame counter reset bit. The value of this register following a reset is 00000000H.

Figure 3 - 131 Format of Total Reception Counter (BBRCVCOUNT)

Address: 0147H to 0144H After reset: 00000000H R

Symbol	31	30	29	28	27	26	25	24
BBRCV COUNT (0147H)	RCVCOUNT 31	RCVCOUNT 30	RCVCOUNT 29	RCVCOUNT 28	RCVCOUNT 27	RCVCOUNT 26	RCVCOUNT 25	RCVCOUNT 24
	23	22	21	20	19	18	17	16
(0146H)	RCVCOUNT 23	RCVCOUNT 22	RCVCOUNT 21	RCVCOUNT 20	RCVCOUNT 19	RCVCOUNT 18	RCVCOUNT 17	RCVCOUNT 16
	15	14	13	12	11	10	9	8
(0145H)	RCVCOUNT 15	RCVCOUNT 14	RCVCOUNT 13	RCVCOUNT 12	RCVCOUNT 11	RCVCOUNT 10	RCVCOUNT 9	RCVCOUNT 8
	7	6	5	4	3	2	1	0
(0144H)	RCVCOUNT 7	RCVCOUNT 6	RCVCOUNT 5	RCVCOUNT 4	RCVCOUNT 3	RCVCOUNT 2	RCVCOUNT 1	RCVCOUNT 0

RCVCOUNT31 to RCVCOUNT0	Total number of received frames
—	These bits indicate the total number of received frames.

3.4.121 PHR error counter (BBPHRERRCOUNT)

This counter indicates the number of the received frames that are discarded as a result of the PHR validation. The frames that match the following check conditions are counted. Each check can be enabled or disabled individually.

- Received frames whose MS bit is set to 1 when the MS frame discard bit is set to 1 (frame is discarded).
- Received frames that are discarded because the frame length value is equal to or smaller than the value specified in the frame cancellation minimum length register
- Received frames that are discarded because the frame length value is equal to or greater than the value specified in the frame cancellation maximum length register
- Received mode switch frames that include a PC error
- Received frames that include an HCS check error in the PHR, which is detected in the MODEM block.

When the value read from the lowest-order byte at address 0148H is 00H in a state other than IDLE, re-read from the lowest-order byte at the given address. Note that re-reading from the lowest-order byte should be done before the counter has counted to 256 so that the value of the lowest-order byte becomes 00H. The value of this register following a reset is 00000000H.

Figure 3 - 132 Format of PHR Error Counter (BBPHRERRCOUNT)

Address: 014BH to 0148H After reset: 00000000H R

Symbol	31	30	29	28	27	26	25	24
BBPHRERRCOUNT (014BH)	PHRERRCOUNT31	PHRERRCOUNT30	PHRERRCOUNT29	PHRERRCOUNT28	PHRERRCOUNT27	PHRERRCOUNT26	PHRERRCOUNT25	PHRERRCOUNT24
	23	22	21	20	19	18	17	16
(014AH)	PHRERRCOUNT23	PHRERRCOUNT22	PHRERRCOUNT21	PHRERRCOUNT20	PHRERRCOUNT19	PHRERRCOUNT18	PHRERRCOUNT17	PHRERRCOUNT16
	15	14	13	12	11	10	9	8
(0149H)	PHRERRCOUNT15	PHRERRCOUNT14	PHRERRCOUNT13	PHRERRCOUNT12	PHRERRCOUNT11	PHRERRCOUNT10	PHRERRCOUNT9	PHRERRCOUNT8
	7	6	5	4	3	2	1	0
(0148H)	PHRERRCOUNT7	PHRERRCOUNT6	PHRERRCOUNT5	PHRERRCOUNT4	PHRERRCOUNT3	PHRERRCOUNT2	PHRERRCOUNT1	PHRERRCOUNT0

PHRERRCOUNT31 to PHRERRCOUNT0	Number of PHR errors
—	These bits indicate the number of the received frames that are discarded as a result of the PHR validation.

3.4.122 Number-of-successful-receptions counter (BBRCVOKCOUNT)

This register is used to count the number of frames that have been successfully received after having passed the PHR and CRC validations. When the value read from the lowest-order byte at address 014CH is 00H in a state other than IDLE, re-read from the lowest-order byte at the given address. Note that re-reading from the lowest-order byte should be done before the counter has counted to 256 so that the value of the lowest-order byte becomes 00H. The value of this register following a reset is 00000000H.

Figure 3 - 133 Format of Number-of-Successful-Receptions Counter (BBRCVOKCOUNT)

Address: 014FH to 014CH After reset: 00000000H R

Symbol	31	30	29	28	27	26	25	24
BBRCVOKCOUNT (014FH)	RCVOKCOUNT31	RCVOKCOUNT30	RCVOKCOUNT29	RCVOKCOUNT28	RCVOKCOUNT27	RCVOKCOUNT26	RCVOKCOUNT25	RCVOKCOUNT24
	23	22	21	20	19	18	17	16
(014EH)	RCVOKCOUNT23	RCVOKCOUNT22	RCVOKCOUNT21	RCVOKCOUNT20	RCVOKCOUNT19	RCVOKCOUNT18	RCVOKCOUNT17	RCVOKCOUNT16
	15	14	13	12	11	10	9	8
(014DH)	RCVOKCOUNT15	RCVOKCOUNT14	RCVOKCOUNT13	RCVOKCOUNT12	RCVOKCOUNT11	RCVOKCOUNT10	RCVOKCOUNT9	RCVOKCOUNT8
	7	6	5	4	3	2	1	0
(014CH)	RCVOKCOUNT7	RCVOKCOUNT6	RCVOKCOUNT5	RCVOKCOUNT4	RCVOKCOUNT3	RCVOKCOUNT2	RCVOKCOUNT1	RCVOKCOUNT0

RCVOKCOUNT31 to RCVOKCOUNT0	Number-of-successful-receptions counter value
—	These bits indicate the number of frames that have been successfully received by this device.

3.4.123 Number-of-unsuccessful-receptions counter (BBRCVNGCOUNT)

This register is used to count the number of frames that have been unsuccessfully received after having passed the PHR validation but failed the CRC validation. When the value read from the lowest-order byte at address 0150H is 00H in a state other than IDLE, re-read from the lowest-order byte at the given address. Note that re-reading from the lowest-order byte should be done before the counter has counted to 256 so that the value of the lowest-order byte becomes 00H. The value of this register following a reset is 00000000H.

Figure 3 - 134 Format of Number-of-Unsuccessful-Receptions Counter (BBRCVNGCOUNT)

Address: 0153H to 0150H After reset: 00000000H R

Symbol	31	30	29	28	27	26	25	24
BBRCVNG COUNT (0153H)	RCVNG COUNT31	RCVNG COUNT30	RCVNG COUNT29	RCVNG COUNT28	RCVNG COUNT27	RCVNG COUNT26	RCVNG COUNT25	RCVNG COUNT24
	23	22	21	20	19	18	17	16
(0152H)	RCVNG COUNT23	RCVNG COUNT22	RCVNG COUNT21	RCVNG COUNT20	RCVNG COUNT19	RCVNG COUNT18	RCVNG COUNT17	RCVNG COUNT16
	15	14	13	12	11	10	9	8
(0151H)	RCVNG COUNT15	RCVNG COUNT14	RCVNG COUNT13	RCVNG COUNT12	RCVNG COUNT11	RCVNG COUNT10	RCVNG COUNT9	RCVNG COUNT8
	7	6	5	4	3	2	1	0
(0150H)	RCVNG COUNT7	RCVNG COUNT6	RCVNG COUNT5	RCVNG COUNT4	RCVNG COUNT3	RCVNG COUNT2	RCVNG COUNT1	RCVNG COUNT0

RCVNGCOUNT31 to RCVNGCOUNT0	Number-of-unsuccessful-receptions counter value
—	These bits indicate the number of frames that have been unsuccessfully received by this device.

3.4.124 Frame synchronization power value result register (BBFSYNCPOWRSLT)

This register holds the power value of the frame synchronization section. The 10-bit power value of the frame synchronization section is stored in the FSYNCPOWRSLT bits. The receive level filter function uses this power value. The power value of the frame synchronization section corresponding to the save bank specified by the receive data save bank select bit is read from this register. The read value is a 2's complement indicating a value from -256.0 dBm to +255.5 dBm in steps of 0.5 dBm. The unit of indication is dBm. For example, 33DH indicates -97.5 dBm. The value of this register following a reset is 0200H.

Figure 3 - 135 Format of Frame Synchronization Power Value Result Register (BBFSYNCPOWRSLT)

Address: 0159H, 0158H After reset: 0200H R

Symbol	15	14	13	12	11	10	9	8
BBFSYNCPOWRSLT (0159H)	0	0	0	0	0	0	FSYNCPOWRSLT9	FSYNCPOWRSLT8
	7	6	5	4	3	2	1	0
(0158H)	FSYNCPOWRSLT7	FSYNCPOWRSLT6	FSYNCPOWRSLT5	FSYNCPOWRSLT4	FSYNCPOWRSLT3	FSYNCPOWRSLT2	FSYNCPOWRSLT1	FSYNCPOWRSLT0

FSYNCPOWRSLT9 to FSYNCPOWRSLT0	Frame synchronization power value
—	10-bit power value of the frame synchronization section

3.4.125 Frame synchronization power value result 2 register (BBFSYNCPOWRSLT2)

This register holds the power value of the frame synchronization section. The 8-bit power value of the frame synchronization section is stored in the FSYNCPOWRSLT2 bits. The power value of the frame synchronization section corresponding to the save bank specified by the receive data save bank select bit is read from this register. The read value is a 2's complement indicating a value from -128 dBm to +127 dBm in steps of 1 dBm. The unit of indication is dBm. For example, 9EH indicates -98 dBm. The value of this register following a reset is 80H.

Figure 3 - 136 Format of Frame Synchronization Power Value Result 2 Register (BBFSYNCPOWRSLT2)

Address: 015AH After reset: 80H R

Symbol	7	6	5	4	3	2	1	0
BBFSYNCPOWRSLT2	FSYNCPOWRSLT27	FSYNCPOWRSLT26	FSYNCPOWRSLT25	FSYNCPOWRSLT24	FSYNCPOWRSLT23	FSYNCPOWRSLT22	FSYNCPOWRSLT21	FSYNCPOWRSLT20

FSYNCPOWRSLT27 to FSYNCPOWRSLT20	Frame synchronization power value
—	8-bit power value of the frame synchronization section

3.4.126 CCA data rate control register (BBCCARATECON)

The data rate for CCA can be set independently of that for transmission and reception by setting the CCA data rate switching bit. While the setting of this bit is 1, the following settings are effective.

- The CCAFSK modulation index setting bit is used to specify the modulation index for CCA in the FSK modulation mode.
- The data rate for CCA in the FSK modulation mode can be selected by the CCAFSK data rate selection bits.
- The CCAOFDMOPTION setting bits are used to set the option value for CCA in the OFDM modulation mode.

The value of this register following a reset is 00H.

Figure 3 - 137 Format of CCA Data Rate Control Register (BBCCARATECON) (1/2)

Address: 015EH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBCCA RATECON	CCAOFDM OPTION1	CCAOFDM OPTION0	CCAFSK RATE3	CCAFSK RATE2	CCAFSK RATE1	CCAFSK RATE0	CCAFSK INDEX	CCADATA RATESEL

CCAOFDM OPTION1	CCAOFDM OPTION0	CCAOFDMOPTION setting
0	0	Option 1
0	1	Option 2
1	0	Option 3
1	1	Option 4

CCAFSK RATE3	CCAFSK RATE2	CCAFSK RATE1	CCAFSK RATE0	CCAFSK data rate selection
0	0	0	0	50 kbps
0	0	0	1	100 kbps
0	0	1	0	150 kbps
0	0	1	1	200 kbps
0	1	0	0	10 kbps
0	1	0	1	20 kbps
0	1	1	0	Setting prohibited
0	1	1	1	Setting prohibited
1	0	0	0	9.6 kbps
1	0	0	1	19.2 kbps
1	0	1	0	38.4 kbps
1	0	1	1	115.2 kbps
1	1	0	0	Setting prohibited
1	1	0	1	Setting prohibited
1	1	1	0	Setting prohibited
1	1	1	1	Setting prohibited

Figure 3 - 137 Format of CCA Data Rate Control Register (BBCCARATECON) (2/2)

CCAFS KINDEX	CCAFSK modulation index setting
0	0.5
1	1.0

CCADATA RATESEL	CCA data rate switching
0	The data rate for CCA is same as that for transmission and reception.
1	The data rate for CCA can be set independently of that for transmission and reception.

3.4.127 FSK control register 0 (BBFSKCON0)

The FSK modulation index setting bit is used to specify the modulation index for FSK transmission and reception. The rate of FSK data transmission and reception can be selected by the FSK data rate selection bits. The value of this register following a reset is 00H.

Figure 3 - 138 Format of FSK Control Register 0 (BBFSKCON0)

Address: 0160H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBFSKCON0	0	0	0	FSKRATE3	FSKRATE2	FSKRATE1	FSKRATE0	FSKINDEX

FSKRATE3	FSKRATE2	FSKRATE1	FSKRATE0	FSK data rate selection
0	0	0	0	50 kbps
0	0	0	1	100 kbps
0	0	1	0	150 kbps
0	0	1	1	200 kbps
0	1	0	0	10 kbps
0	1	0	1	20 kbps
0	1	1	0	Setting prohibited
0	1	1	1	Setting prohibited
1	0	0	0	9.6 kbps
1	0	0	1	19.2 kbps
1	0	1	0	38.4 kbps
1	0	1	1	115.2 kbps
1	1	0	0	Setting prohibited
1	1	0	1	Setting prohibited
1	1	1	0	Setting prohibited
1	1	1	1	Setting prohibited

FSKINDEX	FSK modulation index setting
0	0.5
1	1.0

Caution When writing to this register, set bits 7 to 5 to the value 0.

3.4.128 FSK control register 1 (BBFSKCON1)

The FSK reception FEC enable bit enables FEC for reception. The FSKFEC mode switch bit is used to switch the mode of FEC encoding. The FSKCRC bit count switch bit selects the number of CRC calculation bits for FSK transmission. For auto ACK reply, the number of CRC bits in the received frame is used. The FSKDW enable bit enables data whitening for transmission. The FSKPHR transmission 1 and 2 bits are used to specify the values of bits 1 and 2 of the PHR for FSK transmission, respectively. The FSK interleaving enable bit enables interleaving. Be sure to set this bit to 1 when using the NRNSC encoder. When using the RSC encoder, interleaving can be enabled or disabled as desired. The reception MS bit forcible clear bit is used to forcibly clear the received MS bit to 0. The value of this register following a reset is 8CH.

Figure 3 - 139 Format of FSK Control Register 1 (BBFSKCON1) (1/2)

Address: 0161H After reset: 8CH R/W

Symbol	7	6	5	4	3	2	1	0
BBFSKCON1	RXFORCEMS	FSKINTLVEN	FSKPHRTX2	FSKPHRTX1	FSKDWEN	FSKCRCBIT	FSKFECMODE	FSKFECENRX

RXFORCEMS	Reception MS bit forcible clear
0	The MS bit is not forcibly cleared to 0.
1	The MS bit is forcibly cleared to 0.

FSKINTLVEN	FSK interleaving enable
0	Interleaving is disabled.
1	Interleaving is enabled.

FSKPHRTX2	FSKPHR transmission 2
—	Value to be transmitted.

FSKPHRTX1	FSKPHR transmission 1
—	Value to be transmitted.

Figure 3 - 139 Format of FSK Control Register 1 (BBFSKCON1) (2/2)

FSKDW EN	FSKDW enable
0	Data whitening is disabled.
1	Data whitening is enabled.

FSKCRC BIT	FSKCRC bit count switch
0	32-bit CRC
1	16-bit CRC

FSKFEC MODE	FSKFEC mode switch
0	NRNSC encoder
1	RSC encoder

FSKFEC ENRX	FSK reception FEC enable
0	FEC is disabled.
1	FEC is enabled.

3.4.129 FSK control register 2 (BBFSKCON2)

The GFSK/FSK switch bits for transmission and reception are used to switch between GFSK modulation and FSK modulation for transmission and reception, respectively. The value of this register following a reset is 00H.

Figure 3 - 140 Format of FSK Control Register 2 (BBFSKCON2)

Address: 0162H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBFSKCON2	0	0	0	0	0	0	RXFSKSEL	TXFSKSEL

RXFSKSEL	GFSK/FSK switch for reception
0	GFSK
1	FSK

TXFSKSEL	GFSK/FSK switch for transmission
0	GFSK
1	FSK

Caution When writing to this register, set bits 7 to 2 to the value 0.

3.4.130 FSKFEC control register (BBFSKFECCON)

The automatic FEC detection enable bit is used to detect whether FEC is enabled in reception. The transmission FEC enable bit enables or disables FEC for transmission. The auto ACK reply FEC control bit selects whether the enabling of FEC in auto ACK reply depends on the FEC state (enabled or disabled) in reception or the setting of the auto ACK reply FEC enable bit. When the auto ACK reply FEC control bit is set to 1, FEC in auto ACK reply can be enabled or disabled by the auto ACK reply FEC enable bit. The auto ACK receive FEC control bit selects whether the enabling of FEC in auto ACK reception depends on the setting of the auto ACK receive FEC enable bit. When the auto ACK receive FEC control bit is set to 1, FEC in auto ACK reception can be enabled or disabled by the auto ACK receive FEC enable bit. The MRFSKSFD selection bit is used to specify the phyMRFSKSFD value. The reception FEC monitor bit is used to monitor whether FEC is enabled in the received frame. The value of this register following a reset is 00H.

Figure 3 - 141 Format of FSKFEC Control Register (BBFSKFECCON) (1/2)

Address: 0163H After reset: 00H R/W[Note]

Symbol	7	6	5	4	3	2	1	0
BBFSKFECCON	FECMONI	MRFSKSFD	FECEN ACKRCV	FECCON ACKRCV	FECEN ACKRTN	FECCON ACKRTN	FEC ENTX	FEC AUTOEN

FECMONI	Reception FEC monitor
0	Reception without FEC
1	Reception with FEC

MRFSKSFD	MRFSKSFD selection
0	phyMRFSKSFD = 0
1	phyMRFSKSFD = 1

FECEN ACKRCV	Auto ACK receive FEC enable
0	FEC is disabled.
1	FEC is enabled.

FECCON ACKRCV	Auto ACK receive FEC control
0	FEC does not depend on the setting of the auto ACK receive FEC enable bit.
1	FEC depends on the setting of the auto ACK receive FEC enable bit.

Figure 3 - 141 Format of FSKFEC Control Register (BBFSKFECCON) (2/2)

FECEN ACKRTN	Auto ACK reply FEC enable
0	FEC is disabled.
1	FEC is enabled.

FECCON ACKRTN	Auto ACK reply FEC control
0	FEC depends on the FEC enabled or disabled state in reception.
1	FEC depends on the setting of the auto ACK reply FEC enable bit.

FEC ENTX	Transmission FEC enable
0	FEC is disabled.
1	FEC is enabled.

FEC AUTOEN	Automatic FEC detection enable
0	Automatic detection is disabled.
1	Automatic detection is enabled.

Caution Writing to bit 7 has no effect.

3.4.131 Preamble length setting register (BBPAMBL)

This register is used to set the preamble length for transmission. Set a value from 0004H to 03E8H as the number of preamble bytes. The value of this register following a reset is 0004H.

Figure 3 - 142 Format of Preamble Length Setting Register (BBPAMBL)

Address: 0446H, 0445H After reset: 0004H R/W

Symbol	15	14	13	12	11	10	9	8
BBPAMBL (0446H)	0	0	0	0	0	0	PAMBLLEN9	PAMBLLEN8
	7	6	5	4	3	2	1	0
(0445H)	PAMBLLEN7	PAMBLLEN6	PAMBLLEN5	PAMBLLEN4	PAMBLLEN3	PAMBLLEN2	PAMBLLEN1	PAMBLLEN0

PAMBLLEN9 to PAMBLLEN0	Preamble length

Caution When writing to this register, set bits 15 to 10 to the value 0.

3.4.132 Preamble setting register (BBPABL)

This register is used to set the preamble value (LSB first). This register consists of 8 bits. The value of this register following a reset is AAH.

Figure 3 - 143 Format of Preamble Setting Register (BBPABL)

Address: 0447H After reset: AAH R/W

Symbol	7	6	5	4	3	2	1	0
BBPABL	PABL7	PABL6	PABL5	PABL4	PABL3	PABL2	PABL1	PABL0

PABL7 to PABL0	Preamble value

3.4.133 TXSFD setting register (BBTXSFD)

This register is used to set the SFD value for transmission of an FEC disabled frame when the MRFSKSFD bit is 0.

This register consists of 32 bits. Set this register to 904E0000H. The value of this register following a reset is 904E0000H.

Figure 3 - 144 Format of TXSFD Setting Register (BBTXSFD)

Address: 044BH to 0448H After reset: 904E0000H R/W

Symbol	31	30	29	28	27	26	25	24
BBTXSFD (044BH)	TSFD31	TSFD30	TSFD29	TSFD28	TSFD27	TSFD26	TSFD25	TSFD24
	23	22	21	20	19	18	17	16
(044AH)	TSFD23	TSFD22	TSFD21	TSFD20	TSFD19	TSFD18	TSFD17	TSFD16
	15	14	13	12	11	10	9	8
(0449H)	TSFD15	TSFD14	TSFD13	TSFD12	TSFD11	TSFD10	TSFD9	TSFD8
	7	6	5	4	3	2	1	0
(0448H)	TSFD7	TSFD6	TSFD5	TSFD4	TSFD3	TSFD2	TSFD1	TSFD0

TSFD31 to TSFD0	SFD value for transmission

3.4.134 TXSFD setting register 2 (BBTXSFD2)

This register is used to set the SFD value for transmission of an FEC enabled frame when the MRFSKSFD bit is 0.

This register consists of 32 bits. Set this register to 6F4E0000H. The value of this register following a reset is 6F4E0000H.

Figure 3 - 145 Format of TXSFD Setting Register 2 (BBTXSFD2)

Address: 044FH to 044CH After reset: 6F4E0000H R/W

Symbol	31	30	29	28	27	26	25	24
BBTXSFD2 (044FH)	TSFD231	TSFD230	TSFD229	TSFD228	TSFD227	TSFD226	TSFD225	TSFD224
	23	22	21	20	19	18	17	16
(044EH)	TSFD223	TSFD222	TSFD221	TSFD220	TSFD219	TSFD218	TSFD217	TSFD216
	15	14	13	12	11	10	9	8
(044DH)	TSFD215	TSFD214	TSFD213	TSFD212	TSFD211	TSFD210	TSFD209	TSFD208
	7	6	5	4	3	2	1	0
(044CH)	TSFD207	TSFD206	TSFD205	TSFD204	TSFD203	TSFD202	TSFD201	TSFD200

TSFD231 to TSFD200	SFD2 value for transmission

3.4.135 TXSFD setting register 3 (BBTXSFD3)

This register is used to set the SFD value for transmission of an FEC disabled frame when the MRFSKSFD bit is 1.

This register consists of 32 bits. Set this register to 7A0E0000H. The value of this register following a reset is 7A0E0000H.

Figure 3 - 146 Format of TXSFD Setting Register 3 (BBTXSFD3)

Address: 0453H to 0450H After reset: 7A0E0000H R/W

Symbol	31	30	29	28	27	26	25	24
BBTXSFD3 (0453H)	TSFD331	TSFD330	TSFD329	TSFD328	TSFD327	TSFD326	TSFD325	TSFD324
	23	22	21	20	19	18	17	16
(0452H)	TSFD323	TSFD322	TSFD321	TSFD320	TSFD319	TSFD318	TSFD317	TSFD316
	15	14	13	12	11	10	9	8
(0451H)	TSFD315	TSFD314	TSFD313	TSFD312	TSFD311	TSFD310	TSFD309	TSFD308
	7	6	5	4	3	2	1	0
(0450H)	TSFD307	TSFD306	TSFD305	TSFD304	TSFD303	TSFD302	TSFD301	TSFD300

TSFD331 to TSFD300	SFD3 value for transmission

3.4.136 TXSFD setting register 4 (BBTXSFD4)

This register is used to set the SFD value for transmission of an FEC enabled frame when the MRFSKSFD bit is 1.

This register consists of 32 bits. Set this register to 632D0000H. The value of this register following a reset is 632D0000H.

Figure 3 - 147 Format of TXSFD Setting Register 4 (BBTXSFD4)

Address: 0460H to 045EH, 0454H After reset: 632D0000H R/W

Symbol	31	30	29	28	27	26	25	24
BBTXSFD4 (0460H)	TSFD431	TSFD430	TSFD429	TSFD428	TSFD427	TSFD426	TSFD425	TSFD424
	23	22	21	20	19	18	17	16
(045FH)	TSFD423	TSFD422	TSFD421	TSFD420	TSFD419	TSFD418	TSFD417	TSFD416
	15	14	13	12	11	10	9	8
(045EH)	TSFD415	TSFD414	TSFD413	TSFD412	TSFD411	TSFD410	TSFD409	TSFD408
	7	6	5	4	3	2	1	0
(0454H)	TSFD407	TSFD406	TSFD405	TSFD404	TSFD403	TSFD402	TSFD401	TSFD400

TSFD431 to TSFD400	SFD4 value for transmission

3.4.137 SHR control register (BBSHRCON)

The number-of-SFD-byte setting bits are used to set the number of bytes in the SFD setting[Note 1] to be output as the SFD pattern.

00: 1 byte (bits 31 to 24 of the SFD setting[Note 1])

01: 2 bytes (bits 31 to 16 of the SFD setting[Note 1])

10: 3 bytes (bits 31 to 8 of the SFD setting[Note 1])

11: 4 bytes (bits 31 to 0 of the SFD setting[Note 1])

The value of this register following a reset is 01H.

Note 1. TXSFD setting register, and TXSFD setting registers 2 to 4

Figure 3 - 148 Format of SHR Control Register (BBSHRCON)

Address: 0461H After reset: 01H R/W

Symbol	7	6	5	4	3	2	1	0
BBSHRCON	0	0	0	0	0	0	SFDBYTE1	SFDBYTE0

SFDBYTE1	SFDBYTE0	Number-of-SFD-byte setting
0	0	1 byte
0	1	2 bytes
1	0	3 bytes
1	1	4 bytes

Caution When writing to this register, set bits 7 to 2 to the value 0.

3.4.138 RXSFD setting register (BBRXSFD)

This register is used to set the SFD value for reception of an FEC disabled frame when the MRFSKSFD bit is 0. This register consists of 32 bits. Set this register to 5555904EH. When using a 16-bit value as the SFD, specify the preamble value (5555H) in the higher-order 16 bits (SFD31 to SFD16). When using a 17-bit to 32-bit value as the SFD, specify the preamble value in the higher-order unused bits.

Examples:

17-bit SFD: Specify 5555H in the RSFD31 to RSFD17 bits.

25-bit SFD: Specify 55H in the RSFD31 to RSFD25 bits

Specify an SFD pattern that differs in at least six bits from the SFD value for FEC enabled frames when the MRFSKSFD bit is 0. The value of this register following a reset is 5555904EH.

Figure 3 - 149 Format of RXSFD Setting Register (BBRXSFD)

Bank number: 0 Address: 08F4H to 08F7H After reset: 5555904EH R/W

Symbol	31	30	29	28	27	26	25	24
BBRXSFD (08F4H)	RSFD31	RSFD30	RSFD29	RSFD28	RSFD27	RSFD26	RSFD25	RSFD24
	23	22	21	20	19	18	17	16
(08F5H)	RSFD23	RSFD22	RSFD21	RSFD20	RSFD19	RSFD18	RSFD17	RSFD16
	15	14	13	12	11	10	9	8
(08F6H)	RSFD15	RSFD14	RSFD13	RSFD12	RSFD11	RSFD10	RSFD9	RSFD8
	7	6	5	4	3	2	1	0
(08F7H)	RSFD7	RSFD6	RSFD5	RSFD4	RSFD3	RSFD2	RSFD1	RSFD0

RSFD31 to RSFD0	SFD value for reception

3.4.139 RXSFD setting register 2 (BBRXSFD2)

This register is used to set the SFD value for reception of an FEC enabled frame when the MRFSKSFD bit is 0. This register consists of 32 bits. Set this register to 55556F4EH. When using a 16-bit value as the SFD, specify the preamble value (5555H) in the higher-order 16 bits (RSFD231 to RSFD216). When using a 17-bit to 32-bit value as the SFD, specify the preamble value in the higher-order unused bits.

Examples:

17-bit SFD: Specify 5555H in the RSFD231 to RSFD217 bits.

25-bit SFD: Specify 55H in the RSFD231 to RSFD225 bits

Specify an SFD pattern that differs in at least six bits from the SFD value for FEC disabled frames when the MRFSKSFD bit is 0. The value of this register following a reset is 55556F4EH.

Figure 3 - 150 Format of RXSFD Setting Register 2 (BBRXSFD2)

Bank number: 0 Address: 08F0H to 08F3H After reset: 55556F4EH R/W

Symbol	31	30	29	28	27	26	25	24
BBRXSFD2 (08F0H)	RSFD231	RSFD230	RSFD229	RSFD228	RSFD227	RSFD226	RSFD225	RSFD224
	23	22	21	20	19	18	17	16
(08F1H)	RSFD223	RSFD222	RSFD221	RSFD220	RSFD219	RSFD218	RSFD217	RSFD216
	15	14	13	12	11	10	9	8
(08F2H)	RSFD215	RSFD214	RSFD213	RSFD212	RSFD211	RSFD210	RSFD209	RSFD208
	7	6	5	4	3	2	1	0
(08F3H)	RSFD207	RSFD206	RSFD205	RSFD204	RSFD203	RSFD202	RSFD201	RSFD200

RSFD231 to RSFD200	SFD2 value for reception

3.4.140 RXSFD setting register 3 (BBRXSFD3)

This register is used to set the SFD value for reception of an FEC disabled frame when the MRFSKSFD bit is 1. This register consists of 32 bits. Set this register to 55557A0EH. When using a 16-bit value as the SFD, specify the preamble value (5555H) in the higher-order 16 bits (RSFD331 to RSFD316). When using a 17-bit to 32-bit value as the SFD, specify the preamble value in the higher-order unused bits.

Examples:

17-bit SFD: Specify 5555H in the RSFD331 to RSFD317 bits.

25-bit SFD: Specify 55H in the RSFD331 to RSFD325 bits

Specify an SFD pattern that differs in at least six bits from the SFD value for FEC enabled frames when the MRFSKSFD bit is 1. The value of this register following a reset is 55557A0EH.

Figure 3 - 151 Format of RXSFD Setting Register 3 (BBRXSFD3)

Bank number: 0 Address: 08FCH to 08FFH After reset: 55557A0EH R/W

Symbol	31	30	29	28	27	26	25	24
BBRXSFD3 (08FCH)	RSFD331	RSFD330	RSFD329	RSFD328	RSFD327	RSFD326	RSFD325	RSFD324
	23	22	21	20	19	18	17	16
(08FDH)	RSFD323	RSFD322	RSFD321	RSFD320	RSFD319	RSFD318	RSFD317	RSFD316
	15	14	13	12	11	10	9	8
(08FEH)	RSFD315	RSFD314	RSFD313	RSFD312	RSFD311	RSFD310	RSFD309	RSFD308
	7	6	5	4	3	2	1	0
(08FFH)	RSFD307	RSFD306	RSFD305	RSFD304	RSFD303	RSFD302	RSFD301	RSFD300

RSFD331 to RSFD300	SFD3 value for reception

3.4.141 RXSFD setting register 4 (BBRXSFD4)

This register is used to set the SFD value for reception of an FEC enabled frame when the MRFSKSFD bit is 1. This register consists of 32 bits. Set this register to 5555632DH. When using a 16-bit value as the SFD, specify the preamble value (5555H) in the higher-order 16 bits (RSFD431 to RSFD416). When using a 17-bit to 32-bit value as the SFD, specify the preamble value in the higher-order unused bits.

Examples:

17-bit SFD: Specify 5555H in the RSFD431 to RSFD417 bits.

25-bit SFD: Specify 55H in the RSFD431 to RSFD425 bits

Specify an SFD pattern that differs in at least six bits from the SFD value for FEC disabled frames when the MRFSKSFD bit is 1. The value of this register following a reset is 5555632DH.

Figure 3 - 152 Format of RXSFD Setting Register 4 (BBRXSFD4)

Bank number: 0 Address: 08F8H to 08FBH After reset: 5555632DH R/W

Symbol	31	30	29	28	27	26	25	24
BBRXSFD4 (08F8H)	RSFD431	RSFD430	RSFD429	RSFD428	RSFD427	RSFD426	RSFD425	RSFD424
	23	22	21	20	19	18	17	16
(08F9H)	RSFD423	RSFD422	RSFD421	RSFD420	RSFD419	RSFD418	RSFD417	RSFD416
	15	14	13	12	11	10	9	8
(08FAH)	RSFD415	RSFD414	RSFD413	RSFD412	RSFD411	RSFD410	RSFD409	RSFD408
	7	6	5	4	3	2	1	0
(08FBH)	RSFD407	RSFD406	RSFD405	RSFD404	RSFD403	RSFD402	RSFD401	RSFD400

RSFD431 to RSFD400	SFD4 value for reception

3.4.142 Mode switch frame transmission register (BBTXMODESW)

The mode switch enable bit enables the transmission of the mode switch frame. Setting this bit to 1 and then setting the transmit trigger to 1 transmits the mode switch frame. Only set this bit to 1 for FSK modulation; do not set to 1 for OFDM modulation. Also set the FSKCRC bit count switch bit (FSKCRCBIT) in the FSK control register 1 (BBFSKCON1) to 1. TXMODESW1 to TXMODESW15 bits are used to specify PHR bits 1 to 15 of the mode switch frame to be transmitted. The value of this register following a reset is 0000H.

Figure 3 - 153 Format of Mode Switch Frame Transmission Register (BBTXMODESW)

Address: 0165H, 0164H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBTXMODESW (0165H)	TXMODESW15	TXMODESW14	TXMODESW13	TXMODESW12	TXMODESW11	TXMODESW10	TXMODESW9	TXMODESW8
	7	6	5	4	3	2	1	0
(0164H)	TXMODESW7	TXMODESW6	TXMODESW5	TXMODESW4	TXMODESW3	TXMODESW2	TXMODESW1	MODESW

TXMODESW15 to 1	TXMODESW
—	Value of PHR bits 1 to 15 of the mode switch frame to be transmitted

MODESW	Mode switch enable
0	Disabled, i.e., frames other than mode switch frames are transmitted.
1	Enabled, i.e., the mode switch frame is transmitted.

3.4.143 Mode switch frame reception register (BBRXMODESW)

This register holds the PHY header data (PHR) when a mode switch frame is received. The stored data is retained until the start of the next reception of a mode switch frame. The value of this register following a reset is 0000H.

Figure 3 - 154 Format of Mode Switch Frame Reception Register (BBRXMODESW)

Address: 0167H, 0166H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8
BBRXMODESW (0167H)	RXMODESW15	RXMODESW14	RXMODESW13	RXMODESW12	RXMODESW11	RXMODESW10	RXMODESW9	RXMODESW8
	7	6	5	4	3	2	1	0
(0166H)	RXMODESW7	RXMODESW6	RXMODESW5	RXMODESW4	RXMODESW3	RXMODESW2	RXMODESW1	RXMODESW0

RXMODESW15 to RXMODESW0	RXMODESW
—	Value of PHR bits 0 to 15 of the received mode switch frame

3.4.144 Mode switch status register (BBMSSTATE)

The BCH syndrome calculation result bit is used to check the result of BCH syndrome calculation for the received mode switch frame. The PC error flag is used to check whether a PC error has been found in the received mode switch frame. The received mode switch bit is used to check the value of the mode switch in the received mode switch frame. The value of this register following a reset is 00000X00B.

Figure 3 - 155 Format of Mode Switch Status Register (BBMSSTATE)

Address: 0168H After reset: 00000X00B R

Symbol	7	6	5	4	3	2	1	0
BBMS STATE	0	0	0	0	0	MSFLD	PCERRFLG	BCHSYND

MSFLD	Received mode switch
—	Value of the mode switch in the received mode switch frame

PCERRFLG	PC error flag
0	No PC error has been found.
1	A PC error has been found.

BCHSYND	BCH syndrome calculation result
0	Result of BCH syndrome calculation = 0
1	Result of BCH syndrome calculation = 1

3.4.145 Mode switch frame control register (BBMSCON)

The parity check target bits setting bit is used to set the range of bits in received mode switch frames to be parity checked. The value of this register following a reset is 00H.

Figure 3 - 156 Format of Mode Switch Frame Control Register (BBMSCON)

Address: 0169H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBMSCON	0	0	0	0	0	0	0	PCSEL

PCSEL	Parity check target bits setting
0	Bits 0 to 10 are to be parity checked.
1	Bits 0 to 14 are to be parity checked.

Caution When writing to this register, set bits 7 to 1 to the value 0.

3.4.146 FSKCCA level threshold setting register (BBFSKCCAVTH)

This register is used to set the threshold level for CCA in FSK modulation. The frequency channel is judged to be busy when the CCA value is equal to or greater than the setting in this register. This device compares the receive level with the threshold in 10 bits; bits 9 to 0 of this register are used and bit 9 is the sign bit. Specify a value in 2's complement representation. The unit of setting is dBm. For example, 33DH indicates -97.5 dBm. The value of this register following a reset is 0200H.

Figure 3 - 157 Format of FSKCCA Level Threshold Setting Register (BBFSKCCAVTH)

Address: 016BH, 016AH After reset: 0200H R/W

Symbol	15	14	13	12	11	10	9	8
BBFSKCCAVTH (016BH)	0	0	0	0	0	0	FSKCCAVTH9	FSKCCAVTH8
	7	6	5	4	3	2	1	0
(016AH)	FSKCCAVTH7	FSKCCAVTH6	FSKCCAVTH5	FSKCCAVTH4	FSKCCAVTH3	FSKCCAVTH2	FSKCCAVTH1	FSKCCAVTH0

FSKCCAVTH9 to FSKCCAVTH0	FSKCCA threshold
—	Threshold level for CCA in FSK modulation

Caution When writing to this register, set bits 15 to 10 to the value 0.

3.4.147 FSK reception level threshold setting register (BBFSKLVLVTH)

This register is used to set the threshold value for the receive level filter function in FSK modulation. Reception is done for the level higher than the specified value. This device compares the receive level with the threshold in 10 bits; bits 9 to 0 of this register are used and bit 9 is the sign bit. Specify a value in 2's complement representation. The unit of setting is dBm. For example, 33DH indicates -97.5 dBm. The value of this register following a reset is 0200H.

Figure 3 - 158 Format of FSK Reception Level Threshold Setting Register (BBFSKLVLVTH)

Address: 016DH, 016CH After reset: 0200H R/W

Symbol	15	14	13	12	11	10	9	8
BBFSKLVLVTH (016DH)	0	0	0	0	0	0	FSKLVLVTHT9	FSKLVLVTHT8
	7	6	5	4	3	2	1	0
(016CH)	FSKLVLVTHT7	FSKLVLVTHT6	FSKLVLVTHT5	FSKLVLVTHT4	FSKLVLVTHT3	FSKLVLVTHT2	FSKLVLVTHT1	FSKLVLVTHT0

FSKLVLVTHT9 to FSKLVLVTHT0	FSK receive level threshold
—	Threshold value for the receive level filter function in FSK modulation

Caution When writing to this register, set bits 15 to 10 to the value 0.

3.4.148 FSKPHR reception register (BBFSKPHRRX)

This register holds the values of bits 0 to 4 of the PHY header data when a non-mode switch frame is received. The timing of the storage in this register is the same as the timing when the frame length value is stored. The values corresponding to the save bank specified by the receive data save bank select bit is read from this register. The value of this register following a reset is 0200H.

Figure 3 - 159 Format of FSKPHR Reception Register (BBFSKPHRRX)

Address: 016EH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
BBFSKPHRRX	0	0	0	FSKPHRRX4	FSKPHRRX3	FSKPHRRX2	FSKPHRRX1	FSKPHRRX0

FSKPHRRX4	FSKPHR reception 4
—	Received value (DW)

FSKPHRRX3	FSKPHR reception 3
—	Received value (FCS)

FSKPHRRX2	FSKPHR reception 2
—	Received value (Reserved)

FSKPHRRX1	FSKPHR reception 1
—	Received value (Reserved)

FSKPHRRX0	FSKPHR reception 0
—	Received value (MS)

3.4.149 OFDM control register (BBOFDMCON)

The number-of-OFDMCRC-bit switch bit selects the number of bits for the CRC calculation process in OFDM transmission or reception. The OFDMOPTION setting bits are used to set the option value for OFDM transmission or reception. The OFDM interleaving setting bit is used to set the interleaving value for OFDM transmission or reception. The OFDM extended mode bit is used to select an internal setting for OFDM modulation. When any of option-3 MCS0, option-4 MCS0, or option-4 MCS1 is selected, set this bit to 1. Otherwise, set this bit to 0. The value of this register following a reset is 00H.

Figure 3 - 160 Format of OFDM Control Register (BBOFDMCON)

Address: 0170H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBOFDMCON	0	0	0	OFDMEXT	OFDMINTERLEAVING	OFDMOPTION1	OFDMOPTION0	OFDMCRCBIT

OFDMEXT	OFDM extended mode
0	For other cases than those described below
1	For option-3 MCS0, option-4 MCS0, and option-4 MCS1

OFDMINTERLEAVING	OFDM interleaving setting
—	Interleaving value

OFDMOPTION1	OFDMOPTION0	OFDMOPTION setting
0	0	Option 1
0	1	Option 2
1	0	Option 3
1	1	Option 4

OFDMCRCBIT	Number-of-OFDMCRC-bit switch
0	32-bit CRC
1	16-bit CRC

Caution When writing to this register, set bits 7 to 5 to the value 0.

3.4.150 OFDMPHR transmission register 0 (BBOFDMPHRTX0)

The OFDMMCSTX setting bits are used to specify the MCS value for OFDM transmission. Specify the values of bits 4 to 2 of the PHR for OFDM transmission in the OFDMMCSTX0 to OFDMMCSTX2 bits, respectively. The OFDMSCBTX setting bits are used to specify the scrambler value for OFDM transmission. Specify the values of bits 20 and 19 of the PHR for OFDM transmission in the OFDMSCBTX0 and OFDMSCBTX1 bits, respectively. Note the correspondence of bit positions between the PHR and this register. The value of this register following a reset is 00H.

Figure 3 - 161 Format of OFDMPHR Transmission Register 0 (BBOFDMPHRTX0)

Address: 0172H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBOFDM PHRTX0	0	0	0	OFDM SCBTX1	OFDM SCBTX0	OFDM MCSTX2	OFDM MCSTX1	OFDM MCSTX0

OFDMSCBTX1, OFDMSCBTX0	OFDMSCBTX setting
—	Scrambler value

OFDMMCSTX2 to OFDMMCSTX0	OFDMMCSTX setting
—	MCS value

Caution When writing to this register, set bits 7 to 5 to the value 0.

3.4.151 OFDMPHR transmission register 1 (BBOFDMPHRTX1)

Specify the values of bits 5, 17, 18, and 21 of the PHR for OFDM transmission in the OFDMPHRTX5, OFDMPHRTX17, OFDMPHRTX18, and OFDMPHRTX21 bits, respectively. The value of this register following a reset is 00H.

Figure 3 - 162 Format of OFDMPHR Transmission Register 1 (BBOFDMPHRTX1)

Address: 0173H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBOFDM PHRTX1	0	0	OFDM PHRTX21	OFDM PHRTX18	OFDM PHRTX17	OFDM PHRTX5	0	0

OFDM PHRTX21	OFDMPHR transmission 21
—	Value to be transmitted

OFDM PHRTX18	OFDMPHR transmission 18
—	Value to be transmitted

OFDM PHRTX17	OFDMPHR transmission 17
—	Value to be transmitted

OFDM PHRTX5	OFDMPHR transmission 5
—	Value to be transmitted

Caution When writing to this register, set bits 7, 6, 1, and 0 to the value 0.

3.4.152 OFDMPHRACK reply register 0 (BBOFDMPHRACK0)

The OFDMMCSACK setting bits are used to specify the MCS value in the PHR for OFDM auto ACK reply. Specify the values of bits 4 to 2 of the PHR for OFDM auto ACK reply in the OFDMMCSACK0 to OFDMMCSACK2 bits, respectively. The OFDMSCBACK setting bits are used to specify the scrambler value in the PHR for OFDM auto ACK reply. Specify the values of bits 20 and 19 of the PHR for OFDM auto ACK reply in the OFDMSCBACK0 and OFDMSCBACK1 bits, respectively. Note the correspondence of bit positions between the PHR and this register. The value of this register following a reset is 00H.

Figure 3 - 163 Format of OFDMPHRACK Reply Register 0 (BBOFDMPHRACK0)

Address: 0174H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBOFDM PHRACK0	0	0	0	OFDM SCBACK1	OFDM SCBACK0	OFDM MCSACK2	OFDM MCSACK1	OFDM MCSACK0

OFDMSCBACK1, OFDMSCBACK0	OFDMSCBACK setting
—	Scrambler value

OFDMMCSACK2 to OFDMMCSACK0	OFDMMCSACK setting
—	MCS value

Caution When writing to this register, set bits 7 to 5 to the value 0.

3.4.153 OFDMPHRACK reply register 1 (BBOFDMPHRACK1)

Specify the values of bits 5, 17, 18, and 21 of the PHR for OFDM auto ACK reply in the OFDMPHRACK5, OFDMPHRACK17, OFDMPHRACK18, and OFDMPHRACK21 bits, respectively. The value of this register following a reset is 00H.

Figure 3 - 164 Format of OFDMPHRACK Reply Register 1 (BBOFDMPHRACK1)

Address: 0175H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBOFDM PHRACK1	0	0	OFDM PHRACK21	OFDM PHRACK18	OFDM PHRACK17	OFDM PHRACK5	0	0

OFDM PHRACK21	OFDMPHRACK reply 21
—	Value to be transmitted

OFDM PHRACK18	OFDMPHRACK reply 18
—	Value to be transmitted

OFDM PHRACK17	OFDMPHRACK reply 17
—	Value to be transmitted

OFDM PHRACK5	OFDMPHRACK reply 5
—	Value to be transmitted

Caution When writing to this register, set bits 7, 6, 1, and 0 to the value 0.

3.4.154 OFDMPHR reception register 0 (BBOFDMPHRRX0)

This register holds the values of bits 2 to 5 of the PHY header data when an OFDM frame is received. The timing of the storage in this register is the same as the timing when the frame length value is stored. The values corresponding to the save bank specified by the receive data save bank select bit is read from this register. The value of this register following a reset is 00H.

Figure 3 - 165 Format of OFDMPHR Reception Register 0 (BBOFDMPHRRX0)

Address: 0176H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
BBOFDM PHRRX0	0	0	OFDM PHRRX5	OFDM PHRRX4	OFDM PHRRX3	OFDM PHRRX2	0	0

OFDM PHRRX5	OFDMPHR reception 5
—	Received value (Reserved)

OFDM PHRRX4	OFDMPHR reception 4
—	Received value (RATE0)

OFDM PHRRX3	OFDMPHR reception 3
—	Received value (RATE1)

OFDM PHRRX2	OFDMPHR reception 2
—	Received value (RATE2)

3.4.155 OFDMPHR reception register 1 (BBOFDMPHRRX1)

This register holds the values of bits 17 to 21 of the PHY header data when an OFDM frame is received. The timing of the storage in this register is the same as the timing when the frame length value is stored. The values corresponding to the save bank specified by the receive data save bank select bit is read from this register. The value of this register following a reset is 00H.

Figure 3 - 166 Format of OFDMPHR Reception Register 1 (BBOFDMPHRRX1)

Address: 0177H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
BBOFDM PHRRX1	0	0	0	OFDM PHRRX21	OFDM PHRRX20	OFDM PHRRX19	OFDM PHRRX18	OFDM PHRRX17

OFDM PHRRX21	OFDMPHR reception 21
—	Received value (Reserved)

OFDM PHRRX20	OFDMPHR reception 20
—	Received value (SCBR0)

OFDM PHRRX19	OFDMPHR reception 19
—	Received value (SCBR1)

OFDM PHRRX18	OFDMPHR reception 18
—	Received value (Reserved)

OFDM PHRRX17	OFDMPHR reception 17
—	Received value (Reserved)

3.4.156 OFDMPHR reception register 2 (BBOFDMPHRRX2)

This register holds the values of bits 22 to 29 of the PHY header data when an OFDM frame is received. The timing of the storage in this register is the same as the timing when the frame length value is stored. The values corresponding to the save bank specified by the receive data save bank select bit is read from this register. The value of this register following a reset is 00H.

Figure 3 - 167 Format of OFDMPHR Reception Register 2 (BBOFDMPHRRX2) (1/2)

Address: 0178H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
BBOFDM PHRRX2	OFDM PHRRX29	OFDM PHRRX28	OFDM PHRRX27	OFDM PHRRX26	OFDM PHRRX25	OFDM PHRRX24	OFDM PHRRX23	OFDM PHRRX22

OFDM PHRRX29	OFDMPHR reception 29
—	Received value HCS0

OFDM PHRRX28	OFDMPHR reception 28
—	Received value HCS1

OFDM PHRRX27	OFDMPHR reception 27
—	Received value HCS2

OFDM PHRRX26	OFDMPHR reception 26
—	Received value HCS3

OFDM PHRRX25	OFDMPHR reception 25
—	Received value HCS4

OFDM PHRRX24	OFDMPHR reception 24
—	Received value HCS5

Figure 3 - 167 Format of OFDMPHR Reception Register 2 (BBOFDMPHRRX2) (2/2)

OFDM PHRRX23	OFDMPHR reception 23
—	Received value HCS6

OFDM PHRRX22	OFDMPHR reception 22
—	Received value HCS7

3.4.157 OFDMCCA level threshold setting register (BBOFDMCCAVTH)

This register is used to set the threshold level for CCA in OFDM modulation. The frequency channel is judged to be busy when the CCA value is equal to or greater than the setting in this register. This device compares the receive level with the threshold in 10 bits; bits 9 to 0 of this register are used and bit 9 is the sign bit. Specify a value in 2's complement representation. The unit of setting is dBm. For example, 33DH indicates -97.5 dBm. The value of this register following a reset is 0200H.

Figure 3 - 168 Format of OFDMCCA Level Threshold Setting Register (BBOFDMCCAVTH)

Address: 017BH, 017AH After reset: 0200H R/W

Symbol	15	14	13	12	11	10	9	8
BBOFDMCCAVTH (017BH)	0	0	0	0	0	0	OFDMCCAVTH9	OFDMCCAVTH8
	7	6	5	4	3	2	1	0
(017AH)	OFDMCCAVTH7	OFDMCCAVTH6	OFDMCCAVTH5	OFDMCCAVTH4	OFDMCCAVTH3	OFDMCCAVTH2	OFDMCCAVTH1	OFDMCCAVTH0

OFDMCCAVTH9 to OFDMCCAVTH0	OFDMCCA threshold
—	Threshold level for CCA in OFDM modulation

Caution When writing to this register, set bits 15 to 10 to the value 0.

3.4.158 OFDM reception level threshold setting register (BBOFDMLVLVTH)

This register is used to set the threshold value for the receive level filter function in OFDM modulation. Reception is done for the level higher than the specified value. This device compares the receive level with the threshold in 10 bits; bits 9 to 0 of this register are used and bit 9 is the sign bit. Specify a value in 2's complement representation. The unit of setting is dBm. For example, 33DH indicates -97.5 dBm. The value of this register following a reset is 0200H.

Figure 3 - 169 Format of OFDM Reception Level Threshold Setting Register (BBOFDMLVLVTH)

Address: 017DH, 017CH After reset: 0200H R/W

Symbol	15	14	13	12	11	10	9	8
BBOFDMLVLVTH (017DH)	0	0	0	0	0	0	OFDMLVLVTHT9	OFDMLVLVTHT8
	7	6	5	4	3	2	1	0
(017CH)	OFDMLVLVTHT7	OFDMLVLVTHT6	OFDMLVLVTHT5	OFDMLVLVTHT4	OFDMLVLVTHT3	OFDMLVLVTHT2	OFDMLVLVTHT1	OFDMLVLVTHT0

OFDMLVLVTHT9 to OFDMLVLVTHT0	OFDM receive level threshold
—	Threshold value for the receive level filter function in OFDM modulation

Caution When writing to this register, set bits 15 to 10 to the value 0.

3.4.159 Port direction register 0 (GPIODIR0)

This register is used to set the I/O direction of the individual ports of GPIO0 to GPIO7. The value of this register following a reset is 00H.

Figure 3 - 170 Format of Port Direction Register 0 (GPIODIR0)

Address: 0190H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
GPIODIR0	GPIO7DIR	GPIO6DIR	GPIO5DIR	GPIO4DIR	GPIO3DIR	GPIO2DIR	GPIO1DIR	GPIO0DIR

GPIO7DIR	GPIO7 direction
0	Input port
1	Output port

GPIO6DIR	GPIO6 direction
0	Input port
1	Output port

GPIO5DIR	GPIO5 direction
0	Input port
1	Output port

GPIO4DIR	GPIO4 direction
0	Input port
1	Output port

GPIO3DIR	GPIO3 direction
0	Input port
1	Output port

GPIO2DIR	GPIO2 direction
0	Input port
1	Output port

GPIO1DIR	GPIO1 direction
0	Input port
1	Output port

GPIO0DIR	GPIO0 direction
0	Input port
1	Output port

3.4.160 Port direction register 1 (GPIODIR1)

This register is used to set the I/O direction of the individual ports of GPIO8 to GPIO12. The value of this register following a reset is 00H.

Figure 3 - 171 Format of Port Direction Register 1 (GPIODIR1)

Address: 0191H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
GPIODIR1	0	0	0	GPIO12DIR	GPIO11DIR	GPIO10DIR	GPIO9DIR	GPIO8DIR

GPIO12DIR	GPIO12 direction
0	Input port
1	Output port

GPIO11DIR	GPIO11 direction
0	Input port
1	Output port

GPIO10DIR	GPIO10 direction
0	Input port
1	Output port

GPIO9DIR	GPIO9 direction
0	Input port
1	Output port

GPIO8DIR	GPIO8 direction
0	Input port
1	Output port

Caution When writing to this register, set bits 7 to 5 to the value 0.

3.4.161 Port data register 0 (GPIODATA0)

This register is used to set the values to be output from the individual ports of GPIO0 to GPIO7 when they are set to output. When a GPIO port is set to input, the pin state (high or low) can be read from this register. The value of this register following a reset is 00H.

Figure 3 - 172 Format of Port Data Register 0 (GPIODATA0) (1/2)

Address: 0192H After reset: 00H (when the port is set to output) R/W

Symbol	7	6	5	4	3	2	1	0
GPIODATA0	GPIO7DATA	GPIO6DATA	GPIO5DATA	GPIO4DATA	GPIO3DATA	GPIO2DATA	GPIO1DATA	GPIO0DATA

GPIO7DATA	GPIO7 data
—	When the respective port pin is set to input, this bit indicates the value of the port pin. When the respective port pin is set to output, this bit sets the value to be output from the port pin. Set 0 or 1 to respectively output 0 or 1.

GPIO6DATA	GPIO6 data
—	When the respective port pin is set to input, this bit indicates the value of the port pin. When the respective port pin is set to output, this bit sets the value to be output from the port pin. Set 0 or 1 to respectively output 0 or 1.

GPIO5DATA	GPIO5 data
—	When the respective port pin is set to input, this bit indicates the value of the port pin. When the respective port pin is set to output, this bit sets the value to be output from the port pin. Set 0 or 1 to respectively output 0 or 1.

GPIO4DATA	GPIO4 data
—	When the respective port pin is set to input, this bit indicates the value of the port pin. When the respective port pin is set to output, this bit sets the value to be output from the port pin. Set 0 or 1 to respectively output 0 or 1.

GPIO3DATA	GPIO3 data
—	When the respective port pin is set to input, this bit indicates the value of the port pin. When the respective port pin is set to output, this bit sets the value to be output from the port pin. Set 0 or 1 to respectively output 0 or 1.

Figure 3 - 172 Format of Port Data Register 0 (GPIODATA0) (2/2)

GPIO2DATA	GPIO2 data
—	When the respective port pin is set to input, this bit indicates the value of the port pin. When the respective port pin is set to output, this bit sets the value to be output from the port pin. Set 0 or 1 to respectively output 0 or 1.

GPIO1DATA	GPIO1 data
—	When the respective port pin is set to input, this bit indicates the value of the port pin. When the respective port pin is set to output, this bit sets the value to be output from the port pin. Set 0 or 1 to respectively output 0 or 1.

GPIO0DATA	GPIO0 data
—	When the respective port pin is set to input, this bit indicates the value of the port pin. When the respective port pin is set to output, this bit sets the value to be output from the port pin. Set 0 or 1 to respectively output 0 or 1.

3.4.162 Port data register 1 (GPIODATA1)

This register is used to set the values to be output from the individual ports of GPIO8 to GPIO12 when they are set to output. When a GPIO port is set to input, the pin state (high or low) can be read from this register. The value of this register following a reset is 00H.

Figure 3 - 173 Format of Port Data Register 1 (GPIODATA1)

Address: 0193H After reset: 00H (when the port is set to output) R/W

Symbol	7	6	5	4	3	2	1	0
GPIODATA1	0	0	0	GPIO12 DATA	GPIO11 DATA	GPIO10 DATA	GPIO9 DATA	GPIO8 DATA

GPIO12 DATA	GPIO12 data
—	When the respective port pin is set to input, this bit indicates the value of the port pin. When the respective port pin is set to output, this bit sets the value to be output from the port pin. Set 0 or 1 to respectively output 0 or 1.

GPIO11 DATA	GPIO11 data
—	When the respective port pin is set to input, this bit indicates the value of the port pin. When the respective port pin is set to output, this bit sets the value to be output from the port pin. Set 0 or 1 to respectively output 0 or 1.

GPIO10 DATA	GPIO10 data
—	When the respective port pin is set to input, this bit indicates the value of the port pin. When the respective port pin is set to output, this bit sets the value to be output from the port pin. Set 0 or 1 to respectively output 0 or 1.

GPIO9 DATA	GPIO9 data
—	When the respective port pin is set to input, this bit indicates the value of the port pin. When the respective port pin is set to output, this bit sets the value to be output from the port pin. Set 0 or 1 to respectively output 0 or 1.

GPIO8 DATA	GPIO8 data
—	When the respective port pin is set to input, this bit indicates the value of the port pin. When the respective port pin is set to output, this bit sets the value to be output from the port pin. Set 0 or 1 to respectively output 0 or 1.

Caution When writing to this register, set bits 7 to 5 to the value 0.

3.4.163 Port output driving capability switching register 0 (GPIODRV0)

This register is used to switch the output driving capability of the individual ports of GPIO0 to GPIO7 when they are set to output. The value of this register following a reset is 00H.

Figure 3 - 174 Format of Port Output Driving Capability Switching Register 0 (GPIODRV0)

Address: 0194H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
GPIODRV0	GPIO7DRV	GPIO6DRV	GPIO5DRV	GPIO4DRV	GPIO3DRV	GPIO2DRV	GPIO1DRV	GPIO0DRV

GPIO7DRV	GPIO7 driving capability
0	Low driving capability
1	High driving capability

GPIO6DRV	GPIO6 driving capability
0	Low driving capability
1	High driving capability

GPIO5DRV	GPIO5 driving capability
0	Low driving capability
1	High driving capability

GPIO4DRV	GPIO4 driving capability
0	Low driving capability
1	High driving capability

GPIO3DRV	GPIO3 driving capability
0	Low driving capability
1	High driving capability

GPIO2DRV	GPIO2 driving capability
0	Low driving capability
1	High driving capability

GPIO1DRV	GPIO1 driving capability
0	Low driving capability
1	High driving capability

GPIO0DRV	GPIO0 driving capability
0	Low driving capability
1	High driving capability

3.4.164 Port output driving capability switching register 1 (GPIODRV1)

This register is used to switch the output driving capability of the individual ports of GPIO8 to GPIO12 and SOUT when they are set to output. The value of this register following a reset is 00H.

Figure 3 - 175 Format of Port Output Driving Capability Switching Register 1 (GPIODRV1)

Address: 0195H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
GPIODRV1	0	0	SOUTDRV	GPIO12DRV	GPIO11DRV	GPIO10DRV	GPIO9DRV	GPIO8DRV

SOUTDRV	SOUT driving capability
0	Low driving capability
1	High driving capability

GPIO12DRV	GPIO12 driving capability
0	Low driving capability
1	High driving capability

GPIO11DRV	GPIO11 driving capability
0	Low driving capability
1	High driving capability

GPIO10DRV	GPIO10 driving capability
0	Low driving capability
1	High driving capability

GPIO9DRV	GPIO9 driving capability
0	Low driving capability
1	High driving capability

GPIO8DRV	GPIO8 driving capability
0	Low driving capability
1	High driving capability

Caution When writing to this register, set bits 7 and 6 to the value 0.

3.4.165 Pull-up/pull-down selection register 0 (PULLSEL0)

This register is used to enable or disable the pull-up and pull-down of the individual ports of GPIO0 to GPIO3. When the pull-up and pull-down of a port is enabled, the selection of pull-up or pull-down takes effect. Note that the pull-up or pull-down is disabled when a port is set to output. The value of this register following a reset is FFH.

Figure 3 - 176 Format of Pull-Up/Pull-Down Selection Register 0 (PULLSEL0) (1/2)

Address: 0198H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PULLSEL0	PULL3SEL	PULL3EN	PULL2SEL	PULL2EN	PULL1SEL	PULL1EN	PULL0SEL	PULL0EN

PULL3SEL	PULL3 selection
0	GPIO3 = Pulled down
1	GPIO3 = Pulled up

PULL3EN	PULL3 enable
0	GPIO3 = Pull-up and pull-down are disabled.
1	GPIO3 = Pull-up and pull-down are enabled.

PULL2SEL	PULL2 selection
0	GPIO2 = Pulled down
1	GPIO2 = Pulled up

PULL2EN	PULL2 enable
0	GPIO2 = Pull-up and pull-down are disabled.
1	GPIO2 = Pull-up and pull-down are enabled.

PULL1SEL	PULL1 selection
0	GPIO1 = Pulled down
1	GPIO1 = Pulled up

PULL1EN	PULL1 enable
0	GPIO1 = Pull-up and pull-down are disabled.
1	GPIO1 = Pull-up and pull-down are enabled.

Figure 3 - 176 Format of Pull-Up/Pull-Down Selection Register 0 (PULLSEL0) (2/2)

PULL0SEL	PULL0 selection
0	GPIO0 = Pulled down
1	GPIO0 = Pulled up

PULL0EN	PULL0 enable
0	GPIO0 = Pull-up and pull-down are disabled.
1	GPIO0 = Pull-up and pull-down are enabled.

3.4.166 Pull-up/pull-down selection register 1 (PULLSEL1)

This register is used to enable or disable the pull-up and pull-down of the individual ports of GPIO4 to GPIO7. When the pull-up and pull-down of a port is enabled, the selection of pull-up or pull-down takes effect. Note that the pull-up or pull-down is disabled when a port is set to output. The value of this register following a reset is FFH.

Figure 3 - 177 Format of Pull-Up/Pull-Down Selection Register 1 (PULLSEL1) (1/2)

Address: 0199H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PULLSEL1	PULL7SEL	PULL7EN	PULL6SEL	PULL6EN	PULL5SEL	PULL5EN	PULL4SEL	PULL4EN

PULL7SEL	PULL7 selection
0	GPIO7 = Pulled down
1	GPIO7 = Pulled up

PULL7EN	PULL7 enable
0	GPIO7 = Pull-up and pull-down are disabled.
1	GPIO7 = Pull-up and pull-down are enabled.

PULL6SEL	PULL6 selection
0	GPIO6 = Pulled down
1	GPIO6 = Pulled up

PULL6EN	PULL6 enable
0	GPIO6 = Pull-up and pull-down are disabled.
1	GPIO6 = Pull-up and pull-down are enabled.

PULL5SEL	PULL5 selection
0	GPIO5 = Pulled down
1	GPIO5 = Pulled up

PULL5EN	PULL5 enable
0	GPIO5 = Pull-up and pull-down are disabled.
1	GPIO5 = Pull-up and pull-down are enabled.

Figure 3 - 177 Format of Pull-Up/Pull-Down Selection Register 1 (PULLSEL1) (2/2)

PULL4SEL	PULL4 selection
0	GPIO4 = Pulled down
1	GPIO4 = Pulled up

PULL4EN	PULL4 enable
0	GPIO4 = Pull-up and pull-down are disabled.
1	GPIO4 = Pull-up and pull-down are enabled.

3.4.167 Pull-up/pull-down selection register 2 (PULLSEL2)

This register is used to enable or disable the pull-up and pull-down of the individual ports of GPIO8 to GPIO11. When the pull-up and pull-down of a port is enabled, the selection of pull-up or pull-down takes effect. Note that the pull-up or pull-down is disabled when a port is set to output. The value of this register following a reset is FFH.

Figure 3 - 178 Format of Pull-Up/Pull-Down Selection Register 2 (PULLSEL2) (1/2)

Address: 019AH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PULLSEL2	PULL11SEL	PULL11EN	PULL10SEL	PULL10EN	PULL9SEL	PULL9EN	PULL8SEL	PULL8EN

PULL11SEL	PULL11 selection
0	GPIO11 = Pulled down
1	GPIO11 = Pulled up

PULL11EN	PULL11 enable
0	GPIO11 = Pull-up and pull-down are disabled.
1	GPIO11 = Pull-up and pull-down are enabled.

PULL10SEL	PULL10 selection
0	GPIO10 = Pulled down
1	GPIO10 = Pulled up

PULL10EN	PULL10 enable
0	GPIO10 = Pull-up and pull-down are disabled.
1	GPIO10 = Pull-up and pull-down are enabled.

PULL9SEL	PULL9 selection
0	GPIO9 = Pulled down
1	GPIO9 = Pulled up

PULL9EN	PULL9 enable
0	GPIO9 = Pull-up and pull-down are disabled.
1	GPIO9 = Pull-up and pull-down are enabled.

Figure 3 - 178 Format of Pull-Up/Pull-Down Selection Register 2 (PULLSEL2) (2/2)

PULL8SEL	PULL8 selection
0	GPIO8 = Pulled down
1	GPIO8 = Pulled up

PULL8EN	PULL8 enable
0	GPIO8 = Pull-up and pull-down are disabled.
1	GPIO8 = Pull-up and pull-down are enabled.

3.4.168 Pull-up/pull-down selection register 3 (PULLSEL3)

This register is used to enable or disable the pull-up and pull-down of the individual ports of GPIO12, SEN, SIN, and SCLK. When the pull-up and pull-down of a port is enabled, the selection of pull-up or pull-down takes effect. Note that the pull-up or pull-down is disabled when a port is set to output. The value of this register following a reset is FFH.

Figure 3 - 179 Format of Pull-Up/Pull-Down Selection Register 3 (PULLSEL3) (1/2)

Address: 019BH After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PULLSEL3	PULLSCLK SEL	PULLSCLK EN	PULLSIN SEL	PULLSIN EN	PULLSEN SEL	PULLSEN EN	PULL12 SEL	PULL12 EN

PULLSCLK SEL	PULLSCLK selection
0	SCLK = Pulled down
1	SCLK = Pulled up

PULLSCLK EN	PULLSCLK enable
0	SCLK = Pull-up and pull-down are disabled.
1	SCLK = Pull-up and pull-down are enabled.

PULLSIN SEL	PULLSIN selection
0	SIN = Pulled down
1	SIN = Pulled up

PULLSIN EN	PULLSIN enable
0	SIN = Pull-up and pull-down are disabled.
1	SIN = Pull-up and pull-down are enabled.

PULLSEN SEL	PULLSEN selection
0	SEN = Pulled down
1	SEN = Pulled up

Figure 3 - 179 Format of Pull-Up/Pull-Down Selection Register 3 (PULLSEL3) (2/2)

PULLSEN EN	PULLSEN enable
0	SEN = Pull-up and pull-down are disabled.
1	SEN = Pull-up and pull-down are enabled.

PULL12 SEL	PULL12 selection
0	GPIO12 = Pulled down
1	GPIO12 = Pulled up

PULL12 EN	PULL12 enable
0	GPIO12 = Pull-up and pull-down are disabled.
1	GPIO12 = Pull-up and pull-down are enabled.

3.4.169 GPIO function selection register 0 (BBGPIOFUNCSEL0)

The pin functions of the port pins GPIO0 and GPIO1 can be selected by setting the GPIO0 and GPIO1 function selection bits, respectively. The value of this register following a reset is 00H.

Figure 3 - 180 Format of GPIO Function Selection Register 0 (BBGPIOFUNCSEL0)

Address: 01A0H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBGPIO FUNCSEL0	GPIO1SEL3	GPIO1SEL2	GPIO1SEL1	GPIO1SEL0	GPIO0SEL3	GPIO0SEL2	GPIO0SEL1	GPIO0SEL0

GPIO1SEL3	GPIO1SEL2	GPIO1SEL1	GPIO1SEL0	GPIO1 function selection
0	0	0	0	GPIO
0	0	0	1	INTOUT0
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	CTX
0	1	0	1	CPS
0	1	1	0	CSD
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
Other than above				Setting prohibited

GPIO0SEL3	GPIO0SEL2	GPIO0SEL1	GPIO0SEL0	GPIO0 function selection
0	0	0	0	GPIO
0	0	0	1	INTOUT0
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	CTX
0	1	0	1	CPS
0	1	1	0	CSD
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
Other than above				Setting prohibited

3.4.170 GPIO function selection register 1 (BBGPIOFUNCSEL1)

The pin functions of the port pins GPIO2 and GPIO3 can be selected by setting the GPIO2 and GPIO3 function selection bits, respectively. The value of this register following a reset is 00H.

Figure 3 - 181 Format of GPIO Function Selection Register 1 (BBGPIOFUNCSEL1)

Address: 01A1H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBGPIO FUNCSEL1	GPIO3SEL3	GPIO3SEL2	GPIO3SEL1	GPIO3SEL0	GPIO2SEL3	GPIO2SEL2	GPIO2SEL1	GPIO2SEL0

GPIO3SEL3	GPIO3SEL2	GPIO3SEL1	GPIO3SEL0	GPIO3 function selection
0	0	0	0	GPIO
0	0	0	1	INTOUT0
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	CTX
0	1	0	1	CPS
0	1	1	0	CSD
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
Other than above				Setting prohibited

GPIO2SEL3	GPIO2SEL2	GPIO2SEL1	GPIO2SEL0	GPIO2 function selection
0	0	0	0	GPIO
0	0	0	1	INTOUT0
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	CTX
0	1	0	1	CPS
0	1	1	0	CSD
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
Other than above				Setting prohibited

3.4.171 GPIO function selection register 2 (BBGPIOFUNCSEL2)

The pin functions of the port pins GPIO4 and GPIO5 can be selected by setting the GPIO4 and GPIO5 function selection bits, respectively. The value of this register following a reset is 00H.

Figure 3 - 182 Format of GPIO Function Selection Register 2 (BBGPIOFUNCSEL2)

Address: 01A2H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBGPIO FUNCSEL2	GPIO5SEL3	GPIO5SEL2	GPIO5SEL1	GPIO5SEL0	GPIO4SEL3	GPIO4SEL2	GPIO4SEL1	GPIO4SEL0

GPIO5SEL3	GPIO5SEL2	GPIO5SEL1	GPIO5SEL0	GPIO5 function selection
0	0	0	0	GPIO
0	0	0	1	INTOUT0
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	CTX
0	1	0	1	CPS
0	1	1	0	CSD
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
Other than above				Setting prohibited

GPIO4SEL3	GPIO4SEL2	GPIO4SEL1	GPIO4SEL0	GPIO4 function selection
0	0	0	0	GPIO
0	0	0	1	INTOUT0
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	CTX
0	1	0	1	CPS
0	1	1	0	CSD
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
Other than above				Setting prohibited

3.4.172 GPIO function selection register 3 (BBGPIOFUNCSEL3)

The pin functions of the port pins GPIO6 and GPIO7 can be selected by setting the GPIO6 and GPIO7 function selection bits, respectively. The value of this register following a reset is 00H.

Figure 3 - 183 Format of GPIO Function Selection Register 3 (BBGPIOFUNCSEL3)

Address: 01A3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBGPIOFUNCSEL3	GPIO7SEL3	GPIO7SEL2	GPIO7SEL1	GPIO7SEL0	GPIO6SEL3	GPIO6SEL2	GPIO6SEL1	GPIO6SEL0

GPIO7SEL3	GPIO7SEL2	GPIO7SEL1	GPIO7SEL0	GPIO7 function selection
0	0	0	0	GPIO
0	0	0	1	INTOUT0
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	CTX
0	1	0	1	CPS
0	1	1	0	CSD
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
Other than above				Setting prohibited

GPIO6SEL3	GPIO6SEL2	GPIO6SEL1	GPIO6SEL0	GPIO6 function selection
0	0	0	0	GPIO
0	0	0	1	INTOUT0
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	CTX
0	1	0	1	CPS
0	1	1	0	CSD
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
Other than above				Setting prohibited

3.4.173 GPIO function selection register 4 (BBGPIOFUNCSEL4)

The pin functions of the port pins GPIO8 and GPIO9 can be selected by setting the GPIO8 and GPIO9 function selection bits, respectively. The value of this register following a reset is 00H.

Figure 3 - 184 Format of GPIO Function Selection Register 4 (BBGPIOFUNCSEL4)

Address: 01A4H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBGPIO FUNCSEL4	GPIO9SEL3	GPIO9SEL2	GPIO9SEL1	GPIO9SEL0	GPIO8SEL3	GPIO8SEL2	GPIO8SEL1	GPIO8SEL0

GPIO9SEL3	GPIO9SEL2	GPIO9SEL1	GPIO9SEL0	GPIO9 function selection
0	0	0	0	GPIO
0	0	0	1	INTOUT0
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	CTX
0	1	0	1	CPS
0	1	1	0	CSD
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
Other than above				Setting prohibited

GPIO8SEL3	GPIO8SEL2	GPIO8SEL1	GPIO8SEL0	GPIO8 function selection
0	0	0	0	GPIO
0	0	0	1	INTOUT0
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	CTX
0	1	0	1	CPS
0	1	1	0	CSD
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
Other than above				Setting prohibited

3.4.174 GPIO function selection register 5 (BBGPIOFUNCSEL5)

The pin functions of the port pins GPIO10 and GPIO11 can be selected by setting the GPIO10 and GPIO11 function selection bits, respectively. The value of this register following a reset is 00H.

Figure 3 - 185 Format of GPIO Function Selection Register 5 (BBGPIOFUNCSEL5)

Address: 01A5H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBGPIO FUNCSEL5	GPIO11SEL 3	GPIO11SEL 2	GPIO11SEL 1	GPIO11SEL 0	GPIO10SEL 3	GPIO10SEL 2	GPIO10SEL 1	GPIO10SEL 0

GPIO11SEL 3	GPIO11SEL 2	GPIO11SEL 1	GPIO11SEL 0	GPIO11 function selection
0	0	0	0	GPIO
0	0	0	1	INTOUT0
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	CTX
0	1	0	1	CPS
0	1	1	0	CSD
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
Other than above				Setting prohibited

GPIO10SEL 3	GPIO10SEL 2	GPIO10SEL 1	GPIO10SEL 0	GPIO10 function selection
0	0	0	0	GPIO
0	0	0	1	INTOUT0
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	CTX
0	1	0	1	CPS
0	1	1	0	CSD
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
Other than above				Setting prohibited

3.4.175 GPIO function selection register 6 (BBGPIOFUNCSEL6)

The pin function of the port pin GPIO12 can be selected by setting the GPIO12 function selection bit. The value of this register following a reset is 00H.

Figure 3 - 186 Format of GPIO Function Selection Register 6 (BBGPIOFUNCSEL6)

Address: 01A6H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBGPIO FUNCSEL6	0	0	0	0	GPIO12SEL 3	GPIO12SEL 2	GPIO12SEL 1	GPIO12SEL 0

GPIO12SEL 3	GPIO12SEL 2	GPIO12SEL 1	GPIO12SEL 0	GPIO12 function selection
0	0	0	0	GPIO
0	0	0	1	INTOUT0
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	CTX
0	1	0	1	CPS
0	1	1	0	CSD
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
Other than above				Setting prohibited

Caution When writing to this register, set bits 7 to 4 to the value 0.

3.4.176 RX-state OSC setting register (BBRXOSC)

The RXDDC clock division ratio control bit is used to select the division ratio of the clock for the DDC for reception. The value of this register following a reset is 00H. See the latest application note which specifies the recommended register settings for use with this product.

Figure 3 - 187 Format of RX-State OSC Setting Register (BBRXOSC)

Address: 01C8H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBRXOSC	0	0	0	0	0	RXOSCBFD DCDIVSEL2	RXOSCBFD DCDIVSEL1	RXOSCBFD DCDIVSEL0

RXOSCBFD DCDIVSEL2	RXOSCBFD DCDIVSEL1	RXOSCBFD DCDIVSEL0	RXDDC clock division ratio control
0	0	0	Division ratio is 12.
0	0	1	Division ratio is 13.
0	1	0	Division ratio is 14.
0	1	1	Division ratio is 11.
1	0	0	Division ratio is 10.
1	0	1	Division ratio is 9.
1	1	0	Setting prohibited
1	1	1	Setting prohibited

Caution When writing to this register, set bits 7 to 3 to the value 0.

3.4.177 NEWMODE transmission control register (BBNMTXCON)

The automatic NEWMODE transmission enable 0 to 2 bits are used to automatically transmit a NEWMODE frame. Setting all bits to 1 transmits a NEWMODE frame after the transmission of a mode switch frame. Be sure to set all bits to the same value. The method of automatic NEWMODE frame transmission can be selected by the NEWMODE transmission method selection bit.

0: FSK transmission

The settings in the NEWMODE transmission frequency setting register and NEWMODE transmission FSK control registers 0 and 1 are used for transmission.

1: OFDM transmission

The settings in the NEWMODE transmission frequency setting register, OFDM control register, and OFDMPHR transmission registers 0 and 1 are used for transmission.

The NEWMODE transmission sequence switch 0 and 1 bits select the operation sequence. Be sure to set both bits to the same value. The NEWMODE transmission enable bit enables or disables the transmission of a NEWMODE frame. While this bit is 0, transmission is not enabled even when the timing of enabling transmission comes in the MODEM block. The NEWMODE transmission completion interrupt selection bit is used to set the number of generation times of frame transmission completion interrupts in automatic NEWMODE transmission.

- When the setting of the NEWMODE transmission completion interrupt selection bit is 0:
  Frame transmission completion interrupts are generated twice, that is, upon completions of the transmission of the mode switch frame and of the transmission of a NEWMODE frame.
- When the setting of the NEWMODE transmission completion interrupt selection bit is 1:
  A frame transmission completion interrupt is only generated once, that is, upon completion of the transmission of a NEWMODE frame. The interrupt is not generated upon completion of the transmission of a mode switch frame.

The value of this register following a reset is 80H.

Table 3 - 3 Settings of NEWMODE Transmit Registers

Register	Address	Bit	Normal Sequence	Shortest Sequence	Remark
Address 057H		b7 to b0	65H	15H	For FSK and OFDM
Address 058H		b7 to b0	8DH	3DH	For FSK and OFDM
Automatic NEWMODE transmission enable 0 bit	01E8H	b0	1 (automatic transmission is enabled)		For FSK and OFDM
NEWMODE transmission method selection bit	01E8H	b1	0 (FSK) or 1 (OFDM)	0 (FSK) or 1 (OFDM)	For FSK and OFDM
Automatic NEWMODE transmission enable 1 bit	01E8H	b2	1 (automatic transmission is enabled)		For FSK and OFDM
Automatic NEWMODE transmission enable 2 bit	01E8H	b3	1 (automatic transmission is enabled)		For FSK and OFDM
NEWMODE transmission sequence switch 0 bit	01E8H	b4	0	1	For FSK and OFDM
NEWMODE transmission enable bit	01E8H	b5	1 (enabled)	1 (enabled)	For FSK and OFDM
NEWMODE transmission sequence switch 1 bit	01E8H	b6	0	1	For FSK and OFDM
NEWMODE transmission SX shift frequency setting bits	01EBH, 01EAH	b11 to b0	0 (±0)	Value set for the SX shift frequency	For FSK and OFDM
NEWMODE transmission frequency setting bits	01EFH to 01ECH	b29 to b0	Frequency of NEWMODE frame transmission	Setting is ignored.	For FSK and OFDM
NEWMODE transmission FSK control registers 0 and 1	01F1H, 01F0H	—	Desired setting		For FSK
OFDM control register	0170H	—	Desired setting		For OFDM
OFDMPHR transmission registers 0 and 1	0173H, 0172H	—	Desired setting		For OFDM

Figure 3 - 188 Format of NEWMODE Transmission Control Register (BBNMTXCON)

Address: 01E8H After reset: 80H R/W

Symbol	7	6	5	4	3	2	1	0
BBNMTXCON	NMTX INTSEL	NMTX SQC1	NMTX EN	NMTX SQC0	NMTX ON2	NMTX ON1	NMTX MODE	NMTX ON0

NMTX INTSEL	NEWMODE transmission completion interrupt selection
0	An interrupt is generated upon completion of the transmission of the mode switch frame.
1	No interrupt is generated upon completion of the transmission of the mode switch frame.

NMTX SQC1	NEWMODE transmission sequence switch 1
0	Normal sequence
1	Shortest sequence

NMTXEN	NEWMODE transmission enable
0	NEWMODE transmission is disabled.
1	NEWMODE transmission is enabled.

NMTXSQC0	NEWMODE transmission sequence switch 0
0	Normal sequence
1	Shortest sequence

NMTXON2	Automatic NEWMODE transmission enable 2
0	Automatic transmission is disabled.
1	Automatic transmission is enabled

NMTXON1	Automatic NEWMODE transmission enable 1
0	Automatic transmission is disabled.
1	Automatic transmission is enabled

NMTXMODE	NEWMODE transmission method selection
0	FSK transmission
1	OFDM transmission

NMTXON0	Automatic NEWMODE transmission enable 0
0	Automatic transmission is disabled.
1	Automatic transmission is enabled.

3.4.178 NEWMODE Transmission SX shift frequency setting register (BBNMTXSXSFTFREQ)

The NEWMODE transmission SX shift frequency setting bits are used to set the amount of SX frequency shifting in NEWMODE transmission. The setting is possible in 1-kHz units (1H = 1 kHz).

000H: 0 kHz

001H: 1 kHz

002H: 2 kHz

:

0C8H: 200 kHz

:

7FFH: 2047 kHz

800H: 0 kHz

801H: -1 kHz

802H: -2 kHz

:

8C8H: -200 kHz

:

FFFH: -2047 kHz

This device uses this setting to shift the SX frequency when the NEWMODE transmission sequence switch 0 and 1 bits are set to 1. The device ignores this setting when the switch bits are 0. The value of this register following a reset is 0000H.

Figure 3 - 189 Format of NEWMODE Transmission SX Shift Frequency Setting Register (BBNMTXSXSFTFREQ)

Address: 01EBH, 01EAH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8
BBNMTXSXSFTFREQ (01EBH)	0	0	0	0	NMTXSXSFTFREQ11	NMTXSXSFTFREQ10	NMTXSXSFTFREQ9	NMTXSXSFTFREQ8
	7	6	5	4	3	2	1	0
(01EAH)	NMTXSXSFTFREQ7	NMTXSXSFTFREQ6	NMTXSXSFTFREQ5	NMTXSXSFTFREQ4	NMTXSXSFTFREQ3	NMTXSXSFTFREQ2	NMTXSXSFTFREQ1	NMTXSXSFTFREQ0

NMTXSXSFTFREQ11 to NMTXSXSFTFREQ0	NEWMODE transmission SX shift frequency setting
—	These bits set the amount of SX frequency shifting.

Caution When writing to this register, set bits 15 to 12 to the value 0.

3.4.179 NEWMODE transmission frequency setting register (BBNMTXFREQ)

This register is used to set the frequency of NEWMODE transmission after the transmission of a mode switch frame. This register consists of 30 bits. The frequency can be set in 1-Hz steps. The initial value is 36FC3BA0H, that is, 922.5 MHz. Set a value from 337055C0H (863 MHz) to 37502800H (928 MHz). All four bytes should be specified starting from the lowest-order address. The frequency of NEWMODE transmission is switched to the value specified in this register when the NEWMODE transmission sequence switch 0 and 1 bits are 0. When the switch bits are set to 1, this device ignores the setting in this register and uses the value specified in the frequency setting register. The value of this register following a reset is 36FC3BA0H.

Figure 3 - 190 Format of NEWMODE Transmission Frequency Setting Register (BBNMTXFREQ)

Address: 01EFH to 01ECH After reset: 36FC3BA0H R/W

Symbol	31	30	29	28	27	26	25	24
BBNMTXFREQ (01EFH)	0	0	NMTXFREQ29	NMTXFREQ28	NMTXFREQ27	NMTXFREQ26	NMTXFREQ25	NMTXFREQ24
	23	22	21	20	19	18	17	16
(01EEH)	NMTXFREQ23	NMTXFREQ22	NMTXFREQ21	NMTXFREQ20	NMTXFREQ19	NMTXFREQ18	NMTXFREQ17	NMTXFREQ16
	15	14	13	12	11	10	9	8
(01EDH)	NMTXFREQ15	NMTXFREQ14	NMTXFREQ13	NMTXFREQ12	NMTXFREQ11	NMTXFREQ10	NMTXFREQ9	NMTXFREQ8
	7	6	5	4	3	2	1	0
(01ECH)	NMTXFREQ7	NMTXFREQ6	NMTXFREQ5	NMTXFREQ4	NMTXFREQ3	NMTXFREQ2	NMTXFREQ1	NMTXFREQ0

NMTXFREQ29 to NMTXFREQ0	NEWMODE transmission frequency setting
—	Frequency of NEWMODE transmission

Caution When writing to this register, set bits 31 and 30 to the value 0.

3.4.180 NEWMODE transmission FSK control register 0 (BBNMTXFSKCON0)

The NEWMODE transmission FSK modulation index setting bit is used to specify the modulation index for FSK transmission. The rate of FSK data transmission can be selected by the NEWMODE transmission FSK data rate selection bits. The value of this register following a reset is 00H.

Figure 3 - 191 Format of NEWMODE Transmission FSK Control Register 0 (BBNMTXFSKCON0)

Address: 01F0H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBNMTXFSKCON0	0	0	0	NMTXFSKRATE3	NMTXFSKRATE2	NMTXFSKRATE1	NMTXFSKRATE0	NMTXFSKINDEX

NMTXFSKRATE3	NMTXFSKRATE2	NMTXFSKRATE1	NMTXFSKRATE0	NEWMODE transmission FSK data rate selection
0	0	0	0	50 kbps
0	0	0	1	100 kbps
0	0	1	0	150 kbps
0	0	1	1	200 kbps
0	1	0	0	10 kbps
0	1	0	1	20 kbps
0	1	1	0	Setting prohibited
0	1	1	1	Setting prohibited
1	0	0	0	9.6 kbps
1	0	0	1	19.2 kbps
1	0	1	0	38.4 kbps
1	0	1	1	115.2 kbps
1	1	0	0	Setting prohibited
1	1	0	1	Setting prohibited
1	1	1	0	Setting prohibited
1	1	1	1	Setting prohibited

NMTXFSKINDEX	NEWMODE transmission FSK modulation index setting
0	0.5
1	1.0

Caution When writing to this register, set bits 7 to 5 to the value 0.

3.4.181 NEWMODE transmission FSK control register 1 (BBNMTXFSKCON1)

The NEWMODE transmission FEC enable bit enables FEC for NEWMODE transmission. The NEWMODE transmission FSKFEC mode switch bit is used to switch the mode of FEC encoding for NEWMODE transmission. The NEWMODE transmission FSKCRC bit count switch bit selects the number of CRC calculation bits for NEWMODE transmission. The NEWMODE transmission FSKDW enable bit enables data whitening for NEWMODE transmission. The NEWMODE transmission FSKPHR transmission 1 and 2 bits are used to specify the values of bits 1 and 2 of the PHR for NEWMODE transmission, respectively. The NEWMODE transmission FSK interleaving enable bit enables interleaving for NEWMODE transmission. Set this bit to 1 when using the NRNSC encoder. When using the RSC encoder, interleaving can be enabled or disabled as desired. The value of this register following a reset is 0CH.

Figure 3 - 192 Format of NEWMODE Transmission FSK Control Register 1 (BBNMTXFSKCON1) (1/2)

Address: 01F1H After reset: 0CH R/W

Symbol	7	6	5	4	3	2	1	0
BBNMTXFSKCON1	NMTXMRFSKSFD	NMTXFSKINTLVEN	NMTXFSKPHRTX2	NMTXFSKPHRTX1	NMTXFSKDWEN	NMTXFSKCRCBIT	NMTXFSKFECMODE	NMFECENTX

NMTXMRFSKSFD	NEWMODE transmission MRFSKSFD selection
0	phyMRFSKSFD = 0
1	phyMRFSKSFD = 1

NMTXFSKINTLVEN	NEWMODE transmission FSK interleaving enable
0	Interleaving is disabled.
1	Interleaving is enabled.

NMTXFSKPHRTX2	NEWMODE transmission FSKPHR transmission 2
—	Value to be transmitted.

NMTXFSKPHRTX1	NEWMODE transmission FSKPHR transmission 1
—	Value to be transmitted.

Figure 3 - 192 Format of NEWMODE Transmission FSK Control Register 1 (BBNMTXFSKCON1) (2/2)

NMTXFSK DWEN	NEWMODE transmission FSKDW enable
0	Data whitening is disabled.
1	Data whitening is enabled.

NMTXFSK CRCBIT	NEWMODE transmission FSKCRC bit count switch
0	32-bit CRC
1	16-bit CRC

NMTXFSK FECMODE	NEWMODE transmission FSKFEC mode switch
0	NRNSC encoder
1	RSC encoder

NMFEC ENTX	NEWMODE transmission FEC enable
0	FEC is disabled.
1	FEC is enabled.

3.4.182 NEWMODE transmission FSK preamble length setting register (BBMSPAMBL)

This register is used to set the preamble length for NEWMODE frame transmission after the transmission of a mode switch frame. Set a value from 0004H to 03E8H as the number of preamble bytes. The value of this register following a reset is 0010H.

Figure 3 - 193 Format of NEWMODE Transmission FSK Preamble Length Setting Register (BBMSPAMBL)

Address: 0475H, 0474H After reset: 0010H R/W

Symbol	15	14	13	12	11	10	9	8
BBMSPAMBL (0475H)	0	0	0	0	0	0	MSPAMBLLEN9	MSPAMBLLEN8
	7	6	5	4	3	2	1	0
(0474H)	MSPAMBLLEN7	MSPAMBLLEN6	MSPAMBLLEN5	MSPAMBLLEN4	MSPAMBLLEN3	MSPAMBLLEN2	MSPAMBLLEN1	MSPAMBLLEN0

MSPAMBLLEN9 to MSPAMBLLEN0	Preamble length for NEWMODE frame transmission

Caution When writing to this register, set bits 15 to 10 to the value 0.

3.4.183 NEWMODE reception control register 0 (BBNMRXCON0)

The NEWMODE reception setting 0 bit is used to switch the reception settings to those in the registers for NEWMODE reception after the reception of a mode switch frame. After a mode switch frame is received while this bit is set to 1, the settings in the following registers for NEWMODE reception take effect when the next receive trigger is set.

Registers for NEWMODE reception:

NEWMODE reception control registers 0 and 1, NEWMODE reception frequency setting register, NEWMODE reception FSK control registers 0 and 1, and NEWMODE reception OFDM control register

Be sure to set the NEWMODE reception setting 1 bit to the same value as the NEWMODE reception setting 0 bit. The NEWMODE reception enable bit enables or disables the reception of a NEWMODE frame. While this bit is 0, reception is not enabled even when the timing of enabling reception comes in the MODEM block. The value of this register following a reset is 00H.

Figure 3 - 194 Format of NEWMODE Reception Control Register 0 (BBNMRXCON0)

Address: 01F2H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBNMRXCON0	0	0	0	0	0	NMRXEN	NMRXMODEON1	NMRXMODEON0

NMRXEN	NEWMODE reception enable
0	NEWMODE reception is disabled.
1	NEWMODE reception is enabled.

NMRXMODEON1	NEWMODE reception setting 1
0	NEWMODE reception is disabled.
1	NEWMODE reception is enabled.

NMRXMODEON0	NEWMODE reception setting 0
0	NEWMODE reception is disabled.
1	NEWMODE reception is enabled.

Caution When writing to this register, set bits 7 to 3 to the value 0.

3.4.184 NEWMODE reception control register 1 (BBNMRXCON1)

The NEWMODE reception setting switch bits are used to select the bank of the NEWMODE reception control register 2, NEWMODE reception frequency setting register, NEWMODE reception FSK control registers 0 and 1, and NEWMODE reception OFDM control register to be used for settings. There are 12 banks for settings. The bank selected by this register is used to make read or write access to registers or make settings of NEWMODE reception. The value of this register following a reset is 00H.

Figure 3 - 195 Format of NEWMODE Reception Control Register 1 (BBNMRXCON1)

Address: 01F3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBNMRXCON1	0	0	0	0	NMRXBANK3	NMRXBANK2	NMRXBANK1	NMRXBANK0

NMRXBANK3	NMRXBANK2	NMRXBANK1	NMRXBANK0	NEWMODE reception setting switch
0	0	0	0	Bank 0 for settings
0	0	0	1	Bank 1 for settings
0	0	1	0	Bank 2 for settings
0	0	1	1	Bank 3 for settings
0	1	0	0	Bank 4 for settings
0	1	0	1	Bank 5 for settings
0	1	1	0	Bank 6 for settings
0	1	1	1	Bank 7 for settings
1	0	0	0	Bank 8 for settings
1	0	0	1	Bank 9 for settings
1	0	1	0	Bank 10 for settings
1	0	1	1	Bank 11 for settings
Other than above				Setting prohibited

Caution When writing to this register, set bits 7 to 4 to the value 0.

3.4.185 NEWMODE reception control register 2 (BBNMRXCON2)

The NEWMODE reception method selection bits are used to select the method of NEWMODE frame reception.

0: FSK reception

The settings in the NEWMODE reception control register 1, NEWMODE reception frequency setting register, and NEWMODE reception FSK control registers 0 and 1 are used for reception.

1: OFDM reception

The settings in the NEWMODE reception control register 1, NEWMODE reception frequency setting register, and NEWMODE reception OFDM control register are used for reception.

The IF frequency of NEWMODE reception can be specified by the NEWMODE reception IF frequency setting bits. The NEWMODE reception IF frequency offset enable bit enables or disables the setting of the offset value for the IF frequency in NEWMODE reception. The offset value is set according to the setting in IF frequency offset setting register 0 or 1. The NEWMODE reception IF frequency offset selection bit is used to select whether the value in IF frequency offset setting register 0 or 1 is to be used in NEWMODE reception. The NEWMODE reception DDC clock division ratio selection bits are used to select the division ratio of the clock for the DDC for use in NEWMODE reception. See the latest application note which specifies the recommended register settings for use with this product. The value of this register following a reset is 00H.

Figure 3 - 196 Format of NEWMODE Reception Control Register 2 (BBNMRXCON2) (1/2)

Address: 01F4H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBNMRXCON2	0	NMRXOSCBFDDCDIVSEL2	NMRXOSCBFDDCDIVSEL1	NMRXOSCBFDDCDIVSEL0	NMIFOFSTSEL	NMIFOFSTEN	NMRXIFSET	NMRXMODE

NMRXOSCBFDDCDIVSEL2	NMRXOSCBFDDCDIVSEL1	NMRXOSCBFDDCDIVSEL0	NEWMODE reception DDC clock division ratio selection
0	0	0	Division ratio is 12.
0	0	1	Division ratio is 13.
0	1	0	Division ratio is 14.
0	1	1	Division ratio is 11.
1	0	0	Division ratio is 10.
1	0	1	Division ratio is 9.
1	1	0	Setting prohibited
1	1	1	Setting prohibited

Figure 3 - 196 Format of NEWMODE Reception Control Register 2 (BBNMRXCON2) (2/2)

NMIF OFSTSEL	NEWMODE reception IF frequency offset selection
0	The value in IF frequency offset setting register 0 is to be used.
1	The value in IF frequency offset setting register 1 is to be used.

NMIF OFSTEN	NEWMODE reception IF frequency offset enable
0	IF frequency offset value setting is disabled.
1	IF frequency offset value setting is enabled.

NMRX IFSET	NEWMODE reception IF frequency setting
0	550 kHz
1	750 kHz

NMRX MODE	NEWMODE reception method selection
0	FSK reception
1	OFDM reception

Caution When writing to this register, set bit 7 to the value 0.

3.4.186 NEWMODE reception frequency setting register (BBNMRXBBFREQ)

This register is used to set the frequency of NEWMODE reception after the reception of a mode switch frame. This register consists of 30 bits. The frequency can be set in 1-Hz steps. The initial value is 36FC3BA0H = 922.5 MHz. Set a value from 337055C0H (863 MHz) to 37502800H (928 MHz). All four bytes should be specified starting from the lowest-order address. The value of this register following a reset is 36FC3BA0H.

Figure 3 - 197 Format of NEWMODE Reception Frequency Setting Register (BBNMRXBBFREQ)

Address: 01F8H to 01F5H After reset: 36FC3BA0H R/W

Symbol	31	30	29	28	27	26	25	24
BBNMRXBBFREQ (01F8H)	0	0	NMRXFREQ29	NMRXFREQ28	NMRXFREQ27	NMRXFREQ26	NMRXFREQ25	NMRXFREQ24
	23	22	21	20	19	18	17	16
(01F7H)	NMRXFREQ23	NMRXFREQ22	NMRXFREQ21	NMRXFREQ20	NMRXFREQ19	NMRXFREQ18	NMRXFREQ17	NMRXFREQ16
	15	14	13	12	11	10	9	8
(01F6H)	NMRXFREQ15	NMRXFREQ14	NMRXFREQ13	NMRXFREQ12	NMRXFREQ11	NMRXFREQ10	NMRXFREQ9	NMRXFREQ8
	7	6	5	4	3	2	1	0
(01F5H)	NMRXFREQ7	NMRXFREQ6	NMRXFREQ5	NMRXFREQ4	NMRXFREQ3	NMRXFREQ2	NMRXFREQ1	NMRXFREQ0

NMRXFREQ29 to NMRXFREQ0	NEWMODE reception frequency setting
—	Frequency of NEWMODE reception

Caution When writing to this register, set bits 31 and 30 to the value 0.

3.4.187 NEWMODE reception FSK control register 0 (BBNMRXFSKCON0)

The NEWMODE reception FSK modulation index setting bit is used to specify the modulation index for NEWMODE FSK reception. The rate of NEWMODE FSK data reception can be selected by the NEWMODE reception FSK data rate selection bits. The value of this register following a reset is 00H.

Figure 3 - 198 Format of NEWMODE Reception FSK Control Register 0 (BBNMRXFSKCON0)

Address: 01F9H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBNMRXFSKCON0	0	0	0	NMRXFSKRATE3	NMRXFSKRATE2	NMRXFSKRATE1	NMRXFSKRATE0	NMRXFSKINDEX

NMRXFSKRATE3	NMRXFSKRATE2	NMRXFSKRATE1	NMRXFSKRATE0	NEWMODE reception FSK data rate selection
0	0	0	0	50 kbps
0	0	0	1	100 kbps
0	0	1	0	150 kbps
0	0	1	1	200 kbps
0	1	0	0	10 kbps
0	1	0	1	20 kbps
0	1	1	0	Setting prohibited
0	1	1	1	Setting prohibited
1	0	0	0	9.6 kbps
1	0	0	1	19.2 kbps
1	0	1	0	38.4 kbps
1	0	1	1	115.2 kbps
1	1	0	0	Setting prohibited
1	1	0	1	Setting prohibited
1	1	1	0	Setting prohibited
1	1	1	1	Setting prohibited

NMRXFSKINDEX	NEWMODE reception FSK modulation index setting
0	0.5
0	1.0

Caution When writing to this register, set bits 7 to 5 to the value 0.

3.4.188 NEWMODE reception FSK control register 1 (BBNMRXFSKCON1)

The NEWMODE reception FSK reception FEC enable bit enables FEC (CODE) for NEWMODE FSK reception. The NEWMODE reception FSKFEC mode switch bit is used to switch the mode of FEC encoding for NEWMODE FSK reception. The NEWMODE reception FSK interleaving enable bit enables interleaving for NEWMODE FSK reception. The NEWMODE reception automatic FEC detection enable bit is used to detect whether FEC is enabled in NEWMODE FSK reception. The NEWMODE reception MRFSKSFD selection bit specifies the phyMRFSKSFD value for NEWMODE FSK reception. The NEWMODE reception MS bit forcible clear bit is used to forcibly clear the received MS bit to 0. The value of this register following a reset is 20H.

Figure 3 - 199 Format of NEWMODE Reception FSK Control Register 1 (BBNMRXFSKCON1) (1/2)

Address: 01FAH After reset: 20H R/W

Symbol	7	6	5	4	3	2	1	0
BBNMRX FSKCON1	0	0	NMRX FORCEMS	NMRX MRFSKSFD	NMRXFEC AUTOEN	NMRXFSK INTLVEN	NMRXFSK FECMODE	NMFSK FECENRX

NMRX FORCEMS	NEWMODE reception MS bit forcible clear
0	The MS bit is not forcibly cleared to 0.
1	The MS bit is forcibly cleared to 0.

NMRX MRFSKSFD	NEWMODE reception MRFSKSFD selection
0	phyMRFSKSFD = 0
1	phyMRFSKSFD = 1

NMRXFEC AUTOEN	NEWMODE reception automatic FEC detection enable
0	Detection is disabled.
1	Detection is enabled.

Figure 3 - 199 Format of NEWMODE Reception FSK Control Register 1 (BBNMRXFSKCON1) (2/2)

NMRXFSKINTLVEN	NEWMODE reception FSK interleaving enable
0	Interleaving is disabled.
1	Interleaving is enabled.

NMRXFSKFECMODE	NEWMODE reception FSKFEC mode switch
0	NRNSC encoder
1	RSC encoder

NMFSKFECENRX	NEWMODE reception FSK reception FEC enable
0	FEC is disabled.
1	FEC is enabled.

Caution When writing to this register, set bits 7 and 6 to the value 0.

3.4.189 NEWMODE reception OFDM control register (BBNMRXOFDMCON)

The NEWMODE reception number-of-OFDMCRC-bit switch bit selects the number of bits for the CRC calculation process in OFDM reception. The NEWMODE reception OFDMOPTION setting bits are used to set the option value for OFDM reception as follows.

b1 b0

0 0: Option 1

0 1: Option 2

1 0: Option 3

1 1: Option 4

The NEWMODE reception OFDM interleaving setting bit is used to set the interleaving value for OFDM reception.

The NEWMODE reception OFDM extended mode bit is used to select an internal setting for OFDM modulation in NEWMODE reception. When any of option-3 MCS0, option-4 MCS0, or option-4 MCS1 is selected, set this bit to 1. Otherwise, set this bit to 0. The value of this register following a reset is 00H.

Figure 3 - 200 Format of NEWMODE Reception OFDM Control Register (BBNMRXOFDMCON) (1/2)

Address: 01FBH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
BBNMRXOFDMCON	0	0	0	NMRXOFDMEXT	NMRXOFDMINTERLEAVING	NMRXOFDMOPTION1	NMRXOFDMOPTION0	NMRXOFDMCRCBIT

NMRXOFDMEXT	NEWMODE reception OFDM extended mode
0	For other cases than those described below
1	For option-3 MCS0, option-4 MCS0, and option-4 MCS1

NMRXOFDMINTERLEAVING	NEWMODE reception OFDM interleaving setting
—	Interleaving value

NMRXOFDMOPTION1	NMRXOFDMOPTION0	NEWMODE reception OFDMOPTION setting
0	0	Option 1
0	1	Option 2
1	0	Option 3
1	1	Option 4

Figure 3 - 200 Format of NEWMODE Reception OFDM Control Register (BBNMRXOFDMCON) (2/2)

NMRXOFDM CRCBIT	NEWMODE reception number-of-OFDMCRC-bit switch
0	32-bit CRC
1	16-bit CRC

Caution When writing to this register, set bits 7 to 5 to the value 0.

3.4.190 Version code read control register (VERCNT)

This register is used to control the operation of reading the 8-byte version code prepared for identification of the LSI chip through the SPI. The value of this register following a reset is 00H.

Figure 3 - 201 Format of Version Code Read Control Register (VERCNT)

Address: 04DEH After reset: 00H R/W[Note]

Symbol	7	6	5	4	3	2	1	0
VERCNT	0	0	0	CGCEN	0	0	ENDSEQ	STARTSEQ

CGCEN	Version code read enable
0	Reading is disabled.
1	Reading is enabled.

ENDSEQ	Version code read end flag
0	Reading has not been started or is in progress.
1	Reading has been completed.

STARTSEQ	Version code read operation start
0	Reading is stopped.
1	Reading is started.

Note: Bit 1 is read-only.

Caution When writing to this register, set bits 7 to 5, 3, and 2 to the value 0.

3.4.191 Version registers (VERR0 to VERR7)

An 8-byte version code is stored in these registers. The user cannot modify the register values. The following shows the procedure for reading the version registers. After a command for reading is issued, the values of the version registers are retained until this device is reset.

Figure 3 - 202 Procedure for Reading the Version Registers (VERR0 to VERR7)

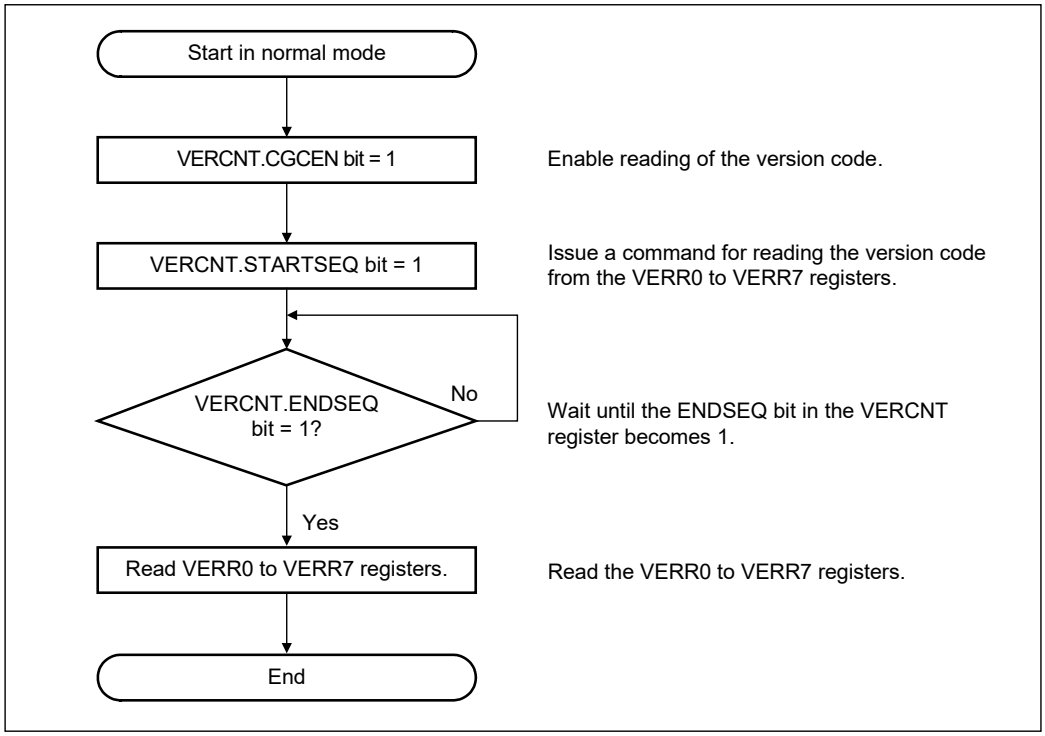


Figure 3 - 203 Format of Version Registers (VERR0 to VERR7)

Address: 04E0H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
VERR0	VERR07	VERR06	VERR05	VERR04	VERR03	VERR02	VERR01	VERR00

VERR07 to VERR00	VERR0 value

Address: 04E1H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
VERR1	VERR17	VERR16	VERR15	VERR14	VERR13	VERR12	VERR11	VERR10

VERR17 to VERR10	VERR1 value

Address: 04E2H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
VERR2	VERR27	VERR26	VERR25	VERR24	VERR23	VERR22	VERR21	VERR20

VERR27 to VERR20	VERR2 value

Address: 04E3H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
VERR3	VERR37	VERR36	VERR35	VERR34	VERR33	VERR32	VERR31	VERR30

VERR37 to VERR30	VERR3 value

Address: 04E4H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
VERR4	VERR47	VERR46	VERR45	VERR44	VERR43	VERR42	VERR41	VERR40

VERR47 to VERR40	VERR4 value

Address: 04E5H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
VERR5	VERR57	VERR56	VERR55	VERR54	VERR53	VERR52	VERR51	VERR50

VERR57 to VERR50	VERR5 value

Address: 04E6H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
VERR6	VERR67	VERR66	VERR65	VERR64	VERR63	VERR62	VERR61	VERR60

VERR67 to VERR60	VERR6 value

Address: 04E7H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
VERR7	VERR77	VERR76	VERR75	VERR74	VERR73	VERR72	VERR71	VERR70

VERR77 to VERR70	VERR7 value

Section 4 Serial Peripheral Interface (SPI)

4.1 Communications Format

The serial interface handles 8-bit serial communications. Figures 4-1 and 4-2 are the respective timing charts for reading and writing when SCLK is set to 24 MHz.

- Address: 12 bits (AD11 to AD0)
- R/W: 1 bit (values are 1 for reading and 0 for writing)
- INCB: 1 bit (address incrementation mode for burst transfer; 0 for incrementation, 1 for non-incrementation)
- Fixed to 0: 2 bits
- Data: 8 bits (DB7 to DB0)

Figure 4 - 1 Overall Timing of Communications through the Serial Peripheral Interface in the Case of Reading

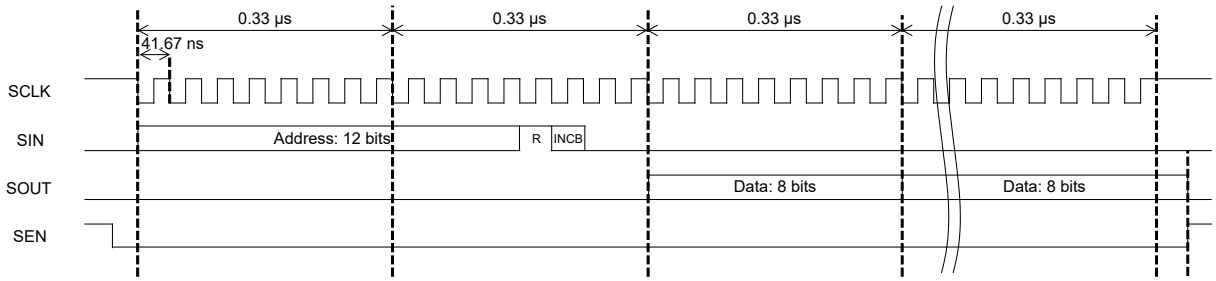
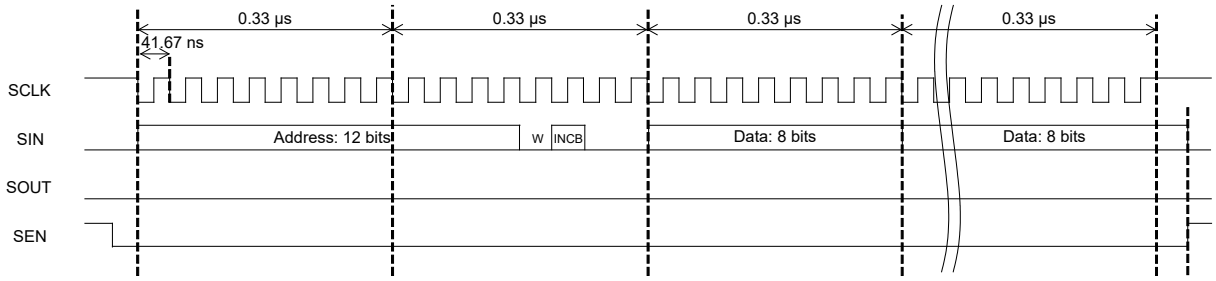


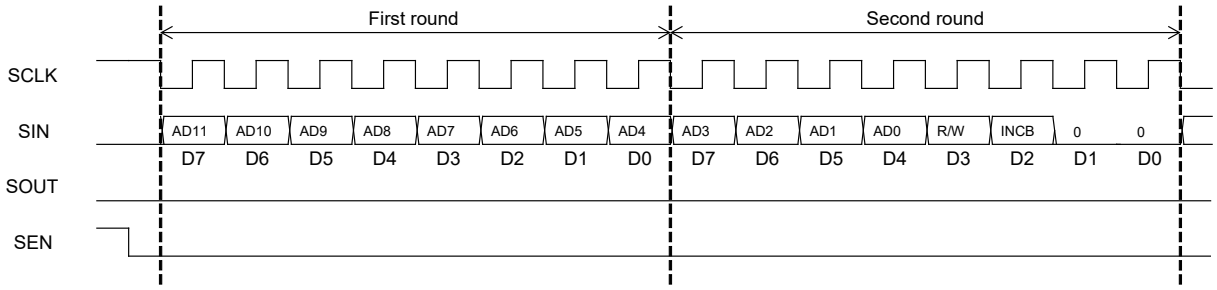
Figure 4 - 2 Overall Timing of Communications through the Serial Peripheral Interface in the Case of Writing



4.1.1 Address, R/W, and INCB Bits

Figure 4-3 shows the timing of the first and second rounds of communications after the SEN pin is driven low. The first round of 8-bit serial communications is handled with the eight higher-order address bits (AD11 to AD4). The following round of 8-bit serial communications is handled with the four lower-order address bits, R/W bit, and INCB bit. Be sure to set the two bits after the INCB bit to 0.

Figure 4 - 3 Timing of Handling of the Address, R/W, and INCB Bits in Communications through the Serial Peripheral Interface



4.1.2 Data Bits

Figures 4-4 and 4-5 respectively show the timing of the third and subsequent rounds of communications for reading and writing after the SEN pin is driven low. The R/W bit being 0 leads to the writing of 8 bits of data input through the SIN pin to the specified address. The R/W bit being 1 leads to the reading of data from the specified address and output of that data through the SOUT pin. The INCB bit being 0 leads to the automatic incrementation of addresses for reading and writing of data in the fourth and subsequent rounds of serial communications with the SEN pin remaining at the low level. The INCB bit being 1 leads to the sequential reading or writing of data from or to the same address in the fourth and subsequent rounds of serial communications, that is, the address is not incremented. In this case too, the SEN pin remains at the low level.

Figure 4 - 4 Timing of Communications through the Serial Peripheral Interface for Reading the Data Bits

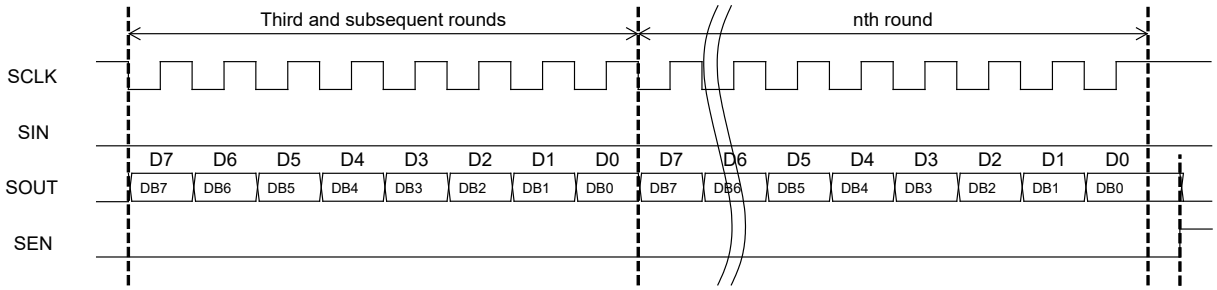
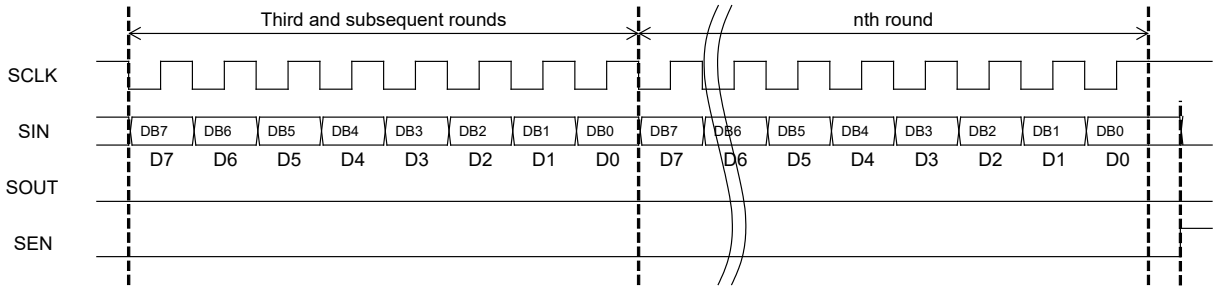


Figure 4 - 5 Timing of Communications through the Serial Peripheral Interface for Writing the Data Bits



Section 5 State Transitions

Figure 5-1 shows the state transitions of this device. It can be placed in the following states by making the respective register settings: SLEEP, STANDBY, IDLE, TX, RX, CAL, CCA, or RX_IDLE.
This device is automatically returned to the IDLE state once data transmission, data reception, or a CCA sequence is completed. This device has the following functionality for transmission and reception.

- Auto ACK to reception: Once data have been transmitted, ACK is issued and this device is automatically placed in the IDLE state and then in the RX state.
- Auto ACK to transmission: Once data have been received, ACK is issued and this device is automatically placed in the IDLE state and then in the TX state.

Figure 5-1 State Transitions

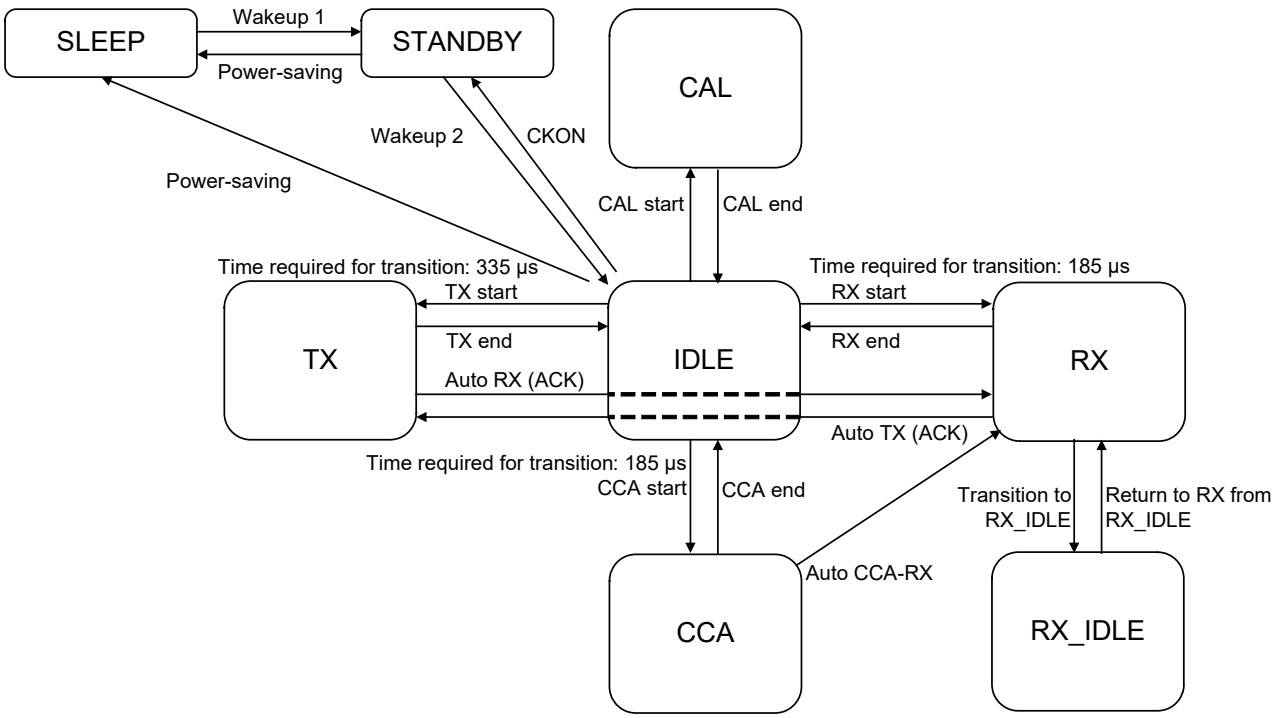


Table 5-1 Descriptions of the States

State	Descriptions
SLEEP	The internal circuits of this device are all off in this state. The CKOUT output is also stopped. The control registers are all reset to their initial values and cannot be set. To place this device in the STANDBY state, follow the procedure in 5.1.1 Wakeup 1: Transition from the SLEEP State to the STANDBY State.
STANDBY	Only the RF reference clock generation circuit and RF start control circuit are active in this state. If the CKOUT output is enabled by the wakeup 1 or CKON operation, a 16-MHz clock signal is output from the CKOUT pin. Other internal circuits are all disabled, and the control registers are all reset to their initial values and cannot be set. To place this device in the IDLE state, follow the procedure in 5.1.2 Wakeup 2: Transition from the STANDBY State to the IDLE State.
IDLE	The power supply circuits (DDC and LDO) are active in this state. The settings and data in the control registers of this device are retained. • In the case of transmission, this device is returned to the IDLE state once transmission is completed, or by setting the RFSTOP bit to 1. • In the case of reception, this device is returned to the IDLE state once reception is completed, or by setting the RFSTOP bit to 1. • In the case of a CGA sequence, this device is returned to the IDLE state once the CCA sequence is completed, or by setting the RFSTOP bit to 1.
TX	This device is transmitting the data written to the data RAM from the RFOUT pin in the specified format.
RX	This device is ready for reception of data input to the RFIN pin.
CCA	This device is handling the CCA sequence for the signal input to the RFIN pin.
CAL	This device is being calibrated.
RX_IDLE	The power supply settings for the analog circuits are retained for reception while those for the digital circuits are all initialized in this state.

5.1 Wakeup: Transition from the SLEEP State to the IDLE State

Wakeup is a part of the startup sequence of this device. The following settings for wakeup are required, and are made by executing dedicated commands through the SEN, SIN, and SCLK pins.

- Setting of the RF reference clock generation circuit
  This setting selects the clock to start this device; a crystal resonator or an external clock (including TCXO).
- Setting of the CKOUT output
  This setting enables or disables output of the 16-MHz clock from the CKOUT pin.
- Setting of the power supply
  This setting selects the internal DDC or external power supply.

This device has two wakeup modes: wakeup 1 and wakeup 2.

5.1.1 Wakeup 1: Transition from the SLEEP State to the STANDBY State

In wakeup 1, transition from the SLEEP state to the STANDBY state is obtained by setting of the RF reference clock generation circuit and CKOUT output. Four startup sequences shown in Table 5-2 are available. The sequence to be used depends on the settings of the RF reference clock generation circuit and CKOUT output.

Table 5-2 Types of Wakeup 1

Case	Setting of the RF reference clock generation circuit	Setting of the CKOUT output
1-1	Crystal resonator	Disabled
1-2	External clock (such as TCXO)	Disabled
1-3	Crystal resonator	Enabled
1-4	External clock (such as TCXO)	Enabled

Operations in cases 1-1 to 1-4 are respectively shown in Figures 5-2 to 5-5. Input commands C1 to C3 through the SEN, SIN, and SCLK pins with the timing shown in the corresponding figure. Figure 5-8 and Table 5-3 respectively show the timing of the command input and the settings of the SIN pin for each of the commands. The setting should be made so that the periods of states 1 to 4 are at least the times shown in the figures. Tables 5-4 and 5-5 respectively show the operation in each state and the states of the pins in each state.

If a transition to the STANDBY state is made with the CKOUT output disabled (case 1-1 or 1-2), the CKON operation can be used to enable the CKOUT output. For the procedure, see section 5.2 CKON Operation: Transition from the IDLE State to the STANDBY State. If disabling of the CKOUT output is required once a transition to the STANDBY state with the CKOUT output enabled is made (case 1-3 or 1-4), the power-saving operation is required. For the procedure, see section 5.4 Power-Saving Operation: Transition from the IDLE State to the SLEEP State.

Figure 5-2 Case 1-1 of Wakeup 1: the Crystal Resonator is Selected and CKOUT Output is Disabled

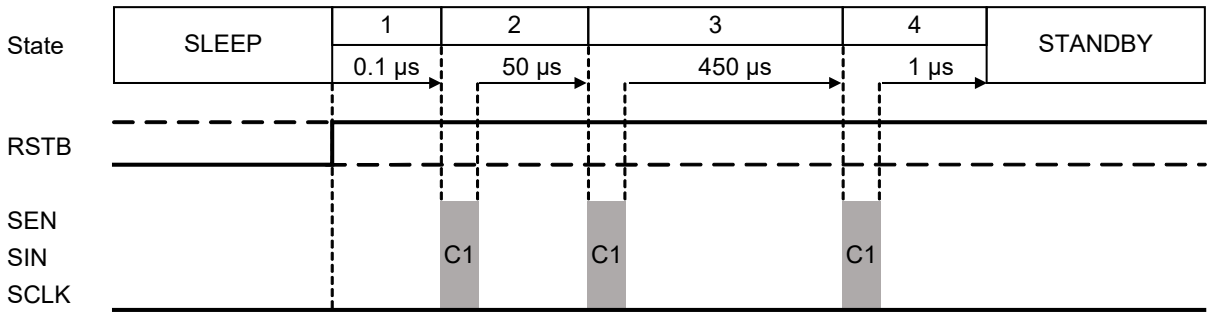


Figure 5-3 Case 1-2 of Wakeup 1: the External Clock is Selected and CKOUT Output is Disabled

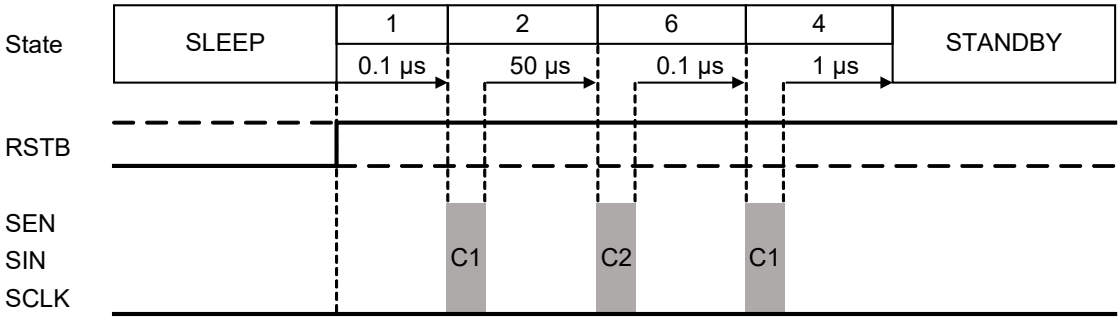


Figure 5-4 Case 1-3 of Wakeup 1: the Crystal Resonator is Selected and CKOUT Output is Enabled

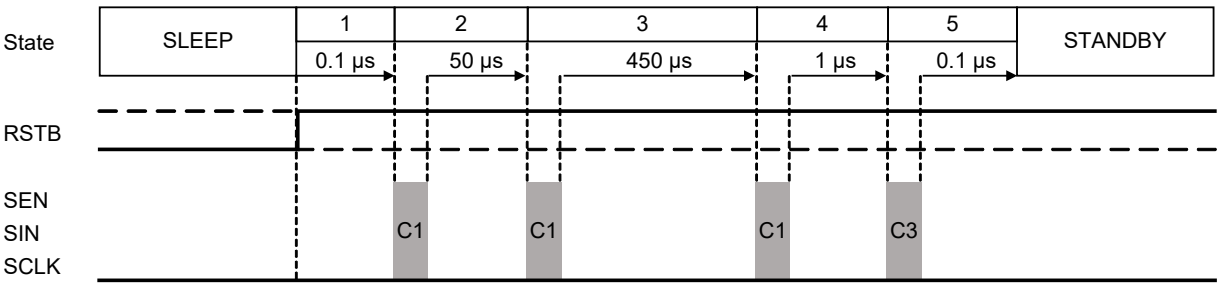
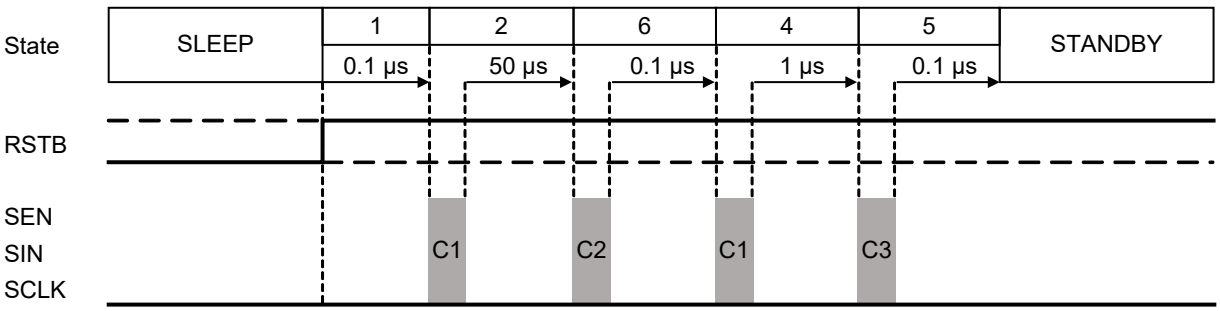


Figure 5-5 Case 1-4 in Wakeup 1: the External Clock is Selected and CKOUT Output is Enabled



5.1.2 Wakeup 2: Transition from the STANDBY State to the IDLE State

Wakeup 2 requires a power supply setting before the transition from the STANDBY state to the IDLE state. Two types of startup sequence are possible in wakeup 2; one with the use of the DDC (case 2-1) and the other with the external power supply (case 2-2). Operations in cases 2-1 and 2-2 are respectively shown in Figures 5-6 and 5-7. Input commands C1 to C5 through the SEN, SIN, and SCLK pins with the timing shown in the corresponding figure. Figure 5-8 and Table 5-3 respectively show the timing of the command input and the settings of the SIN pin for each of the commands. The setting should be made so that the periods of states 7 and 8 are at least the times shown in the figures. Tables 5-4 and 5-5 respectively show the operation in each state and the states of the pins in each state.

Figure 5-6 Case 2-1 of Wakeup 2: when the DDC is to be Used

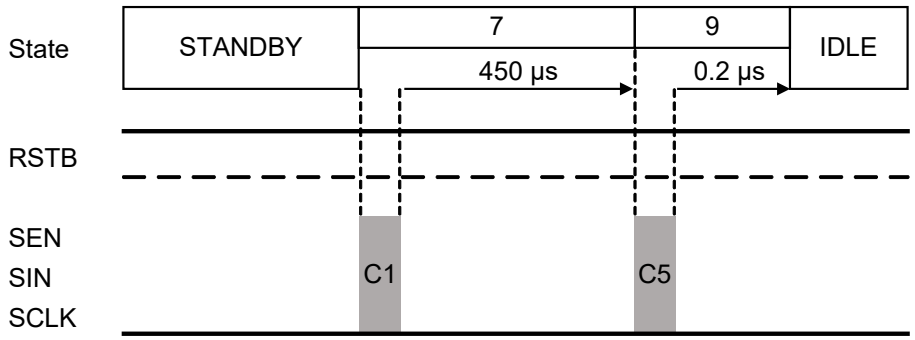


Figure 5-7 Case 2-2 of Wakeup 2: when the External Power Supply is to be Used

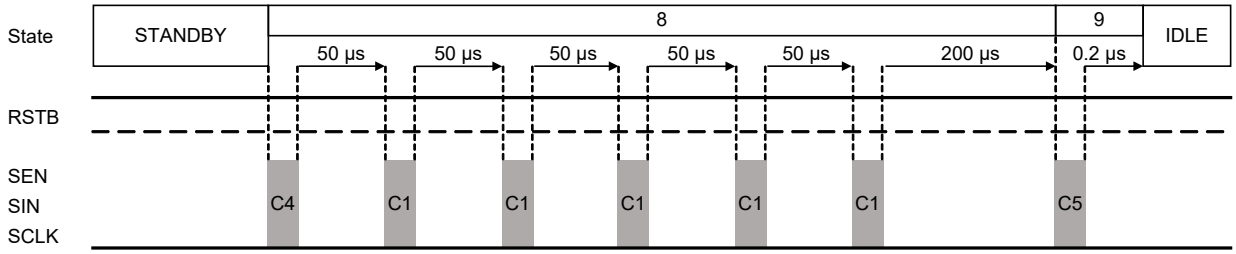


Figure 5-8 Timing of Inputs of SEN, SIN, and SCLK in the Startup Sequence when SCLK is 24 MHz

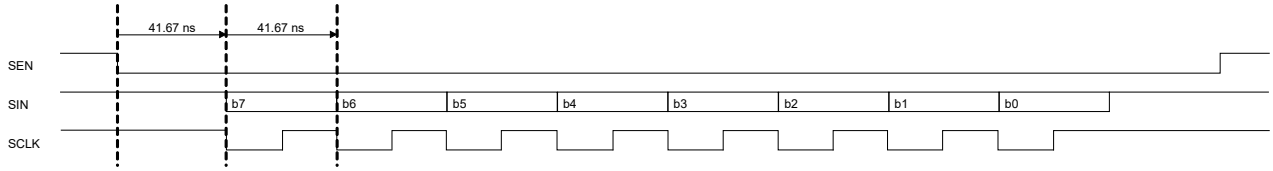


Table 5-3 Settings of the SIN Pin for Commands

Symbol	b7	b6	b5	b4	b3	b2	b1	b0
C1	1	1	1	1	1	1	1	1
C2	0	1	1	1	1	1	1	1
C3	0	0	0	0	0	0	0	0
C4	1	1	0	0	0	0	0	0
C5	1	0	0	0	0	0	0	0
C6	1	0	1	0	0	0	0	0

Table 5-4 Operations in each State of the Startup Sequence

State	Operation
1	The RF startup control circuit is released from the reset state.
2	Time until the power supply to the crystal oscillation circuit becomes stable following the power to the crystal oscillation circuit being turned on.
3	Time until oscillation by the crystal oscillator circuit becomes stable.
4	The driving capability of the crystal oscillator circuit is switched.
5	Output of the 16-MHz clock signal from CKOUT is enabled.
6	Startup by the external clock is selected.
7	Time until the voltage output from the DDC becomes stable following starting up of the DDC circuit. This period includes the time until output of the crystal oscillation circuit becomes stable when the crystal resonator is selected.
8	Time until the voltage output from the internal regulator becomes stable following selection of the external power supply to start up the internal regulator. This period includes the time until output of the crystal oscillation circuit becomes stable when the crystal resonator is selected.
9	The internal circuits are released from the reset state.

Table 5-5 States of the Pins in each State of Operation

Pin	SLEEP	STANDBY	1 to 9	IDLE
RSTB	Driven low	Driven high	Driven high	Driven high
SEN	Pulled up	Input	Input	Input
SCLK	Pulled up	Input	Input	Input
SIN	Pulled up	Input	Input	Input
SOUT	Pulled up	Pulled up	Pulled up	Output
GPIO0 to GPIO12	Pulled up	Pulled up	Pulled up	Depend on the settings of the respective registers

5.2 CKON Operation: Transition from the IDLE State to the STANDBY State

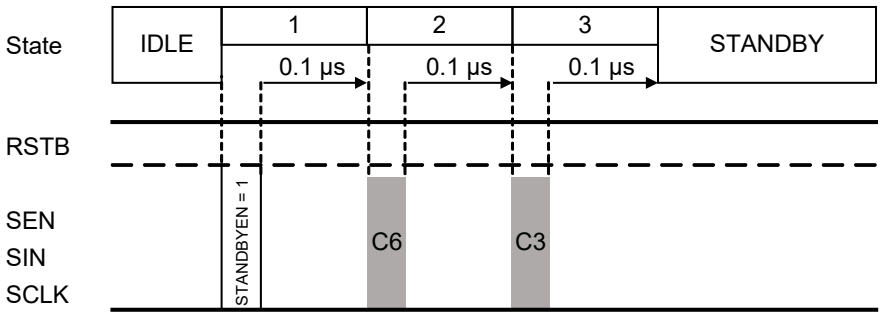
The CKON operation allows the transition of this device from the IDLE state to the STANDBY state, and enabling of the CKOUT output. Setting of the registers through the serial interface and execution of the commands used in wakeup allows the transition.

Follow the procedure below for this operation.

1. Set the STANDBYEN bit in the RF start register (BBRFCON) to 1.
2. Execute command C6 in Table 5-3 with the timing shown in Figure 5-8.
3. Execute command C3 in Table 5-3 with the timing shown in Figure 5-8.

Figure 5-9 shows the timing of executing steps 1 to 3. Numbers 1 to 3 in Figure 5-9 corresponds to steps 1 to 3 of the procedure above. The setting should be made so that the periods of states 1 to 3 are at least the times shown in the figure.

Figure 5-9 CKON Operation



To place this device back in the IDLE state after having executed CKON, follow the procedure for wakeup 2.

Caution When this device is to be returned to the IDLE state, executing a sequence that differs from the one used in the previous wakeup 2 is prohibited. That is, if the previous wakeup 2 was obtained as case 2-1, use the procedure for case 2-1 when returning this device to the IDLE state. The same is applicable if the previous wakeup 2 was obtained as case 2-2.

5.3 Procedure after the Transition to the IDLE State

Start the following procedure after the transition to the IDLE state described in 5.1.2 Wakeup 2: Transition from the STANDBY State to the IDLE State.

1. Setting of the registers through the serial interface
   The procedure depends on the setting of the CKOUT output.
   - If CKOUT output is enabled.
     Set 40H in address 01B1H.
   - If CKOUT output is disabled.
     Set 40H in address 01B1H.
     Set 10H in address 01B4H.

2. Setting of the registers that require initial settings
   Set the initial values of the registers that require initial settings. For the values, see the latest application note which specifies the recommended register settings for use with this product.

3. Calibration
   Proceed with calibration by following the procedure shown in 5.5.5 Example of Calibration Procedure.

5.4 Power-Saving Operation: Transition from the IDLE State to the SLEEP State

Driving the RSTB pin low places this device in the SLEEP state.

5.5 Other Transitions

Transitions between IDLE and TX, IDLE and RX, and TX and RX proceed after the respective register settings have been made through the serial interface. Sections 5.5.1 and 5.5.2 respectively describe examples of the procedures for transmission and reception.

5.5.1 Example of Procedure for Transmission

1. Proceed with the operation described in 5.1 Wakeup: Transition from the SLEEP State to the IDLE State.
2. Proceed with the operation described in 5.3 Procedure after the Transition to the IDLE State.
3. Set the frequency setting register (BBFREQ) to specify the transmission frequency.
4. Set the transmission output power. For details, see section 6.1 Example of Setting the Transmission Output Power.
5. If the auto reception switching mode is to be used, set the AUTORCV0 bit in transmission and reception mode register 0 (BBTXRXMODE0) to 1.
6. Set the REGACCESS bit in the RF start register (BBRFCON) to 1 to write the data for transmission to the transmission RAM.
   Bank 0 (addresses 0800H to 0BFFH), bank 1 (addresses 0C00H to 0FFFH)
7. Set the frame length for use in transmission in the transmission frame length register (BBTXFLEN).
8. Set the TRNTRG bit in the transmission and reception control register (BBTXRXCON) to 1 to start transmission.

A transmission completion interrupt is generated when any of the following conditions is met after the start of transmission.

- Transmission is completed.
- When transmission with the appending of ACK requests with ACK reception enabled has proceeded, ACK reception is then completed.
- Reception of a further ACK is not possible for a specified period of time after transmission with the appending of ACK requests with ACK reception enabled.
- The result for CCA is that the channel was busy after the completion of transmission with the auto CSMA-CA enabled.

5.5.2 Example of Procedure for Reception

1. Proceed with the operation described in 5.1 Wakeup: Transition from the SLEEP State to the IDLE State.
2. Proceed with the operation described in 5.3 Procedure after the Transition to the IDLE State.
3. Set the frequency setting register (BBFREQ) to specify the transmission frequency.
4. If the auto ACK mode is to be used, set the AUTOACKEN, AUTORCV0, and BEACON bits in transmission and reception mode register 0 (BBTXRXMODE0).
5. Set PAN identifier registers 0 and 1 (BBPANID0 and BBPANID1) to specify the PAN identifier.
6. Set short address registers 0 and 1 (BBSHORTAD0 and BBSHORTAD1) or extended address registers 0 and 1 (BBEXTENDAD00 to BBEXTENDAD03 and BBEXTENDAD10 to BBEXTENDAD13).
7. Set the RCVTRG bit in the transmission and reception control register (BBTXRXCON) to start transmission.
8. Wait for a reception completion interrupt.
9. Set the RCVBANKSEL bit in transmission and reception mode register 3 (RCVBANKSEL) to select the received data saving bank.
10. Read the reception frame length register (BBRXFLEN).
11. Read the CRC bit in the transmission and reception status register 0 (BBTXRXST0) to check the result of the CRC check.
12. Set the REGACCESS bit in the RF start register (BBRFCON) to 1 to read the data in the reception RAM. Bank 0 at addresses 0800H to 0BFFH, bank 1 at addresses 0C00H to 0FFFH

5.5.3 Example of Procedure for CCA

1. Make settings for the operation described in 5.1 Wakeup: Transition from the SLEEP State to the IDLE State.
2. Proceed with the procedure described in 5.3 Procedure after the Transition to the IDLE State.
3. Set the frequency setting register (BBFREQ) to specify the reception frequency.
4. Set the CCATRG bit in the transmission and reception control register (BBTXRXCON) to 1 to start CCA.
5. Wait for a CCA completion interrupt.
6. Read the CRC bit in transmission and reception status register 0 (BBTXRXST0) to check the result of the CRC check.

5.5.4 Example of CSMA-CA Procedure

1. Make settings for the operation described in 5.1 Wakeup: Transition from the SLEEP State to the IDLE State.
2. Proceed with the procedure described in 5.3 Procedure after the Transition to the IDLE State.
3. Set the frequency setting register (BBFREQ) to specify the reception frequency.
4. Set the BEACON bit in transmission and reception mode register 0 (BBTXRXMODE0) to 1 to select the beacon mode.
5. Set the BOFFPROD7 to BOFFPROD0 bits in backoff period register 2 (BBBOFFPROD2) to their initial values. After that, set the BOFFPRODEN bit in the backoff period register (BBBOFFPROD) to 1 to enable the automatic generation of random values.
6. Set the CSMAST bit in CSMA control register 0 (BBCSMACON0) to 1 to select automatic starting of CSMA-CA. If transmission following CSMA-CA will be required, also set the CSMATRNST bit in CSMA control register 0 (BBCSMACON0) to 1 so that transmission proceeds following CSMA-CA.
7. Wait for a CSMA-CA completion interrupt.
8. Read the CSMACA bit in the transmission and reception status register 0 (BBTXRXST0) to check the CSMA-CA result.

5.5.5 Example of Procedure for Calibration

1. Set the RF start register (BBRFCON) to 05H.
2. Set the calibration register (BBCAL) to 01H to start calibration.
3. Wait for a calibration completion interrupt.
4. Set the RF start register (BBRFCON) to 01H.
5. Set the transmission and reception reset register (BBTXRXRST) to 01H.

Section 6 Examples of Settings for the Function

6.1 Example of Setting the Transmission Output Power

The following details the setting of the transmission output power mentioned as step 4 of 5.5.1 Example of Procedure for Transmission.

6.1.1 Tx-FSK mode

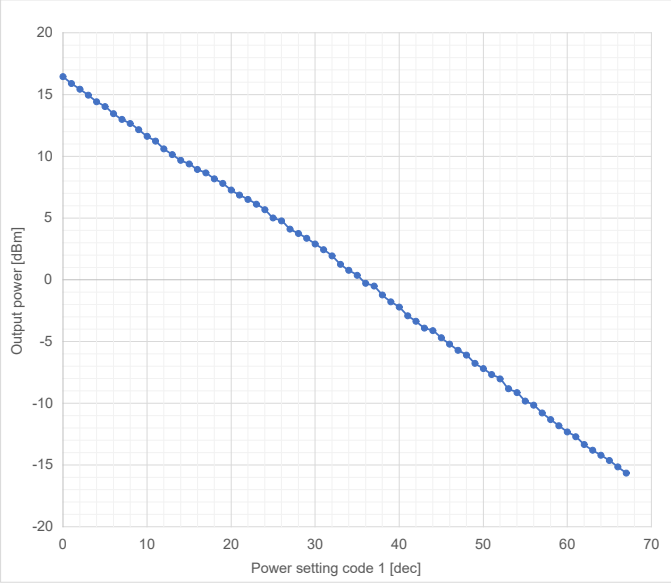
The output power setting must be made before the start of transmission. Do not change the setting during transmission.

1. Set the register at address 0C38H. Set bits 7 to 2 to 000000B.
2. Set the register at address 0C37H. Set bits 7 and 6 to 00B.

Figure 6-1 shows the typical characteristic of the transmission output power and power setting code 1. The actual characteristic of the transmission output power depends on the load conditions including the matching circuit for the RFPOUT pin and the board pattern, and the particular sample of the device that is in use. The combination of coarse and fine tuning of the amplifier can realize precise levels of transmission output power within the wide range from +15 dBm to -15 dBm.

Caution For the details on the setting values, see the latest application note which specifies the recommended register settings for use with this product.

Figure 6 - 1 Characteristic of the Transmission Power vs. Power Setting Code 1 for FSK



Caution This characteristic of the output power was obtained with the use of our recommended circuits and the output frequency set to 920.6 MHz.

6.1.2 Tx-OFDM mode

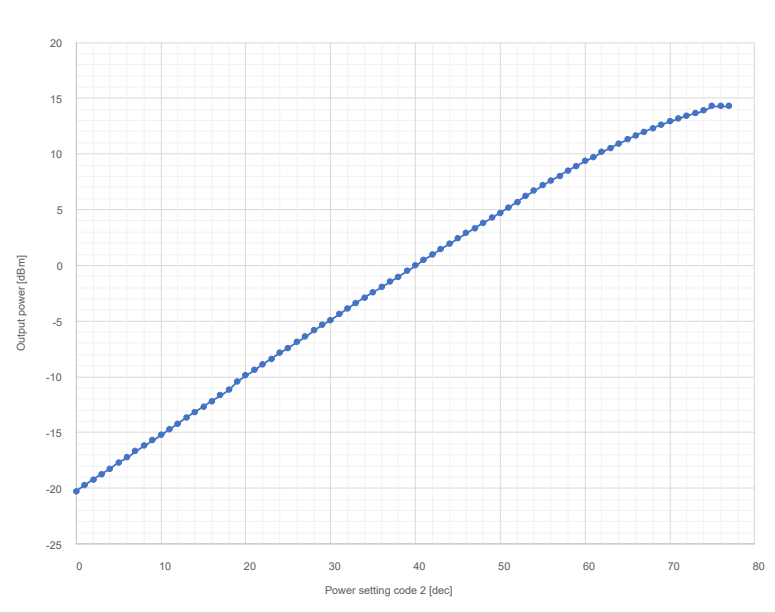
The output power setting must be made before the start of transmission. Do not change the setting during transmission. The transmission output power is specifiable within the range approximately from -19 dBm to +14 dBm.

1. Set the register at address 0468H. Set bits 7 and 6 to 00B. This setting specify the transmission output power for OFDM. Set the given register to 00H to specify the maximum output power. Set it to 3EH to specify the minimum output power. Setting of 3FH is prohibited.
2. To realize a resolution with 0.5 dB per 1 LSB, setting of the registers at addresses 0C1CH, 0C1DH, 0C1EH, and 0C1FH is required.
3. Ensuring the linearity of power control requires setting of the registers at addresses 0ECBH and 0EC1H in accord with the output power.

Settings 1 to 3 above ensure the typical characteristic of the transmission power versus the power setting code 2 shown in Figure 6-2. The actual characteristic of the transmission output power depends on the load conditions including the matching circuit for the RFPOUT pin and the board pattern, and the particular sample of the device that is in use. Note that the gain step becomes smaller than 0.5 dB in the maximum output range of the power amplifier due to the effect of saturation. Specifically, the output power reaches saturation at around +14 to +15 dBm.

Caution For the details on the setting values, see the latest application note which specifies the recommended register settings for use with this product.

Figure 6 - 2 Characteristic of the Transmission Power vs. Power Setting Code 2 for OFDM



Caution This characteristic of the output power was obtained with the use of our recommended circuits and the output frequency set to 920.6 MHz.

6.2 Setting the RF Frequency for Transmission

The following details the setting of the transmission frequency mentioned as step 3 in 5.5.1 Example of Procedure for Transmission. Set the frequency setting register (BBFREQ) to specify the desired frequency. Set the central frequency for the channel in this register.

6.3 Setting the RF Frequency for Reception

The following details the setting of the reception frequency mentioned as step 3 in 5.5.2 Example of Procedure for Reception. Use the frequency setting register (BBFREQ) to specify the reception channel's intermediate frequency. The reception section has an intermediate frequency (IF) circuit, so IF settings by setting the BBIFSET register is also required. Set bit 0 in the BBIFSET register to specify the intermediate frequency (550 kHz or 750 kHz). To add an offset to the intermediate frequency specified in bit 0 in the BBIFSET register, set bits 3 and 2 in the BBIFSET register, the BBIFOFST0 register, and the BBIFOFST1 register.

Example of the basic setting:

1. Set the frequency setting register (BBFREQ) to specify the frequency that matches the central RF frequency for the reception channel.
2. Set the IF frequency setting register (BBIFSET) in accord with the reception modulation method and data rate. Table 6-1 lists examples of the typical settings of the IF frequency in FSK and OFDM reception.

Table 6-1 Typical Settings of the IF Frequency in FSK and OFDM Reception

Modulation Method	Data Rate/Mode	IF Frequency	Setting of the IFSET bit (bit 0) in the BBIFSET register
2-FSK	10 to 200 kbps	550 kHz	0
OFDM	Option 1	750 kHz	1
OFDM	Options 2 to 4	550 kHz	0

Caution Changing the setting of the IF frequency in the settings for the modulation method, data rate, and mode may improve the reception characteristics. For the details on the setting values, see the latest application note which specifies the recommended register settings for use with this product.

Section 7 Point to Note on Using the Baseband Section

7.1 Note on Reading from Specified Registers

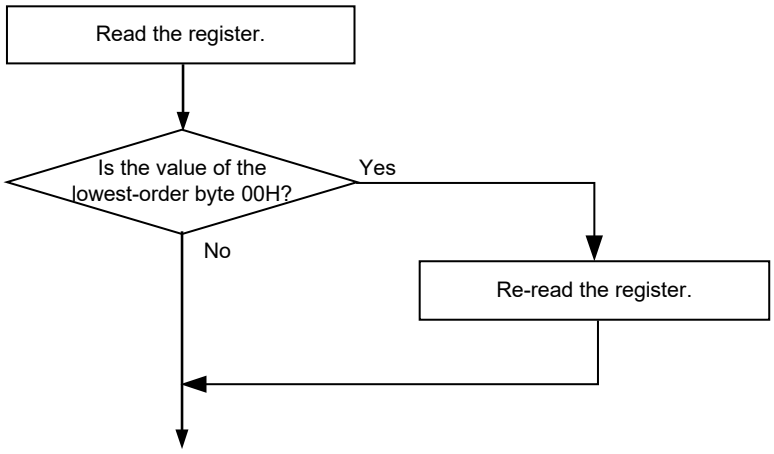
When the value read from the lowest-order byte of the registers listed in Table 7-1 is 00H[Note], re-read the lowest-order byte. Note that re-reading from the lowest-order byte should be done before the counter has counted to 256 so that the value of the lowest-order byte becomes 00H.

Note: This is only applicable to the registers listed as No. 4 to No. 7 in Table 7-1 when this device is not in the IDLE state.

Table 7-1 List of the Specified Registers

No.	Register	Address
1	Timer read registers 0 and 1	0023H to 0020H
2	Received data counter register	00A3H, 00A2H
3	Transmitted data counter register	00BDH, 00BCH
4	Total reception counter	0147H to 0144H
5	PHR error counter	014BH to 0148H
6	Number-of-successful-receptions counter	014FH to 014CH
7	Number-of-unsuccessful-receptions counter	0153H to 0150H

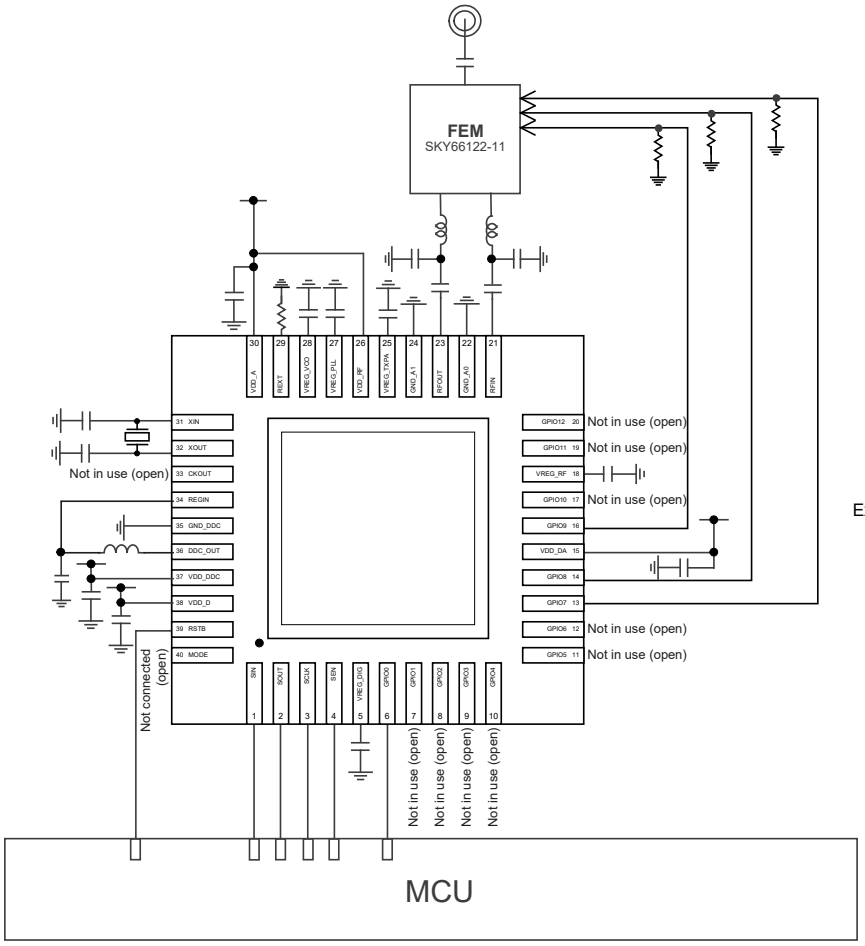
Figure 7 - 1 Flow of Reading from the Specified Registers



Section 8 Connections of the Peripheral Circuits

Figure 8-1 shows the connections of the peripheral circuits, including a front-end module (FEM).

Figure 8 - 1 Connections of the Peripheral Circuits, including a Front-end Module (FEM).



Example of the GPIO settings
GPIO0: Output to indicate the interrupt state
GPIO1: Not in use
GPIO2: Not in use
GPIO3: Not in use
GPIO4: Not in use
GPIO5: Not in use
GPIO6: Not in use
GPIO7: Output for the CSD signal to control the FEM
GPIO8: Output for the CTX signal to control the FEM
GPIO9: Output for the CPX signal to control the FEM
GPIO10: Not in use
GPIO11: Not in use
GPIO12: Not in use

Section 9 Electrical Characteristics

9.1 Absolute Maximum Ratings

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Power supply voltage	VDD	-0.5		3.8	V	VDD_A, VDD_D, VDD_AD, VDD_RF, VDD_DDC
Analog input voltage	V_{REGIN}	-0.3		2.8	V	REGIN
Analog output voltage	V_{DDCOUT}	-0.3		3.8	V	DDCOUT
	V_{REGOUT}	-0.3		1.25	V	VREG_DIG, VREG_RF, VREG_PLL, VREG_VCO
	V_{REGRFO}	-0.3		3.8	V	VREG_TXPA
RF input level	Rfin			16	dBm	RFIN
Voltage on the digital pins	Vd	-0.3		3.8	V	
Voltage on the analog pins	Va	-0.3		1.25	V	
Operating ambient temperature	Ta	-40	25	85	°C	
Storage temperature	Tstg	-65	25	+150	°C	
Characteristics of electro-static discharge (ESD)	Human-body model (HBM)	-2000		2000	V	
	Charged device model (CDM)	-500		500	V	

The listed values are AC ratings. Applying a DC voltage on the RFIN or RFOUT pin is prohibited.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

9.2 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	Vdd		2.7	3.3	3.6	V
Crystal resonator/oscillator oscillation frequency	Frefclk			48		MHz
Operating frequency	Frf		863		928	MHz
RFIN pin (input impedance)	Zin			50		Ω
RFOUT pin (output impedance)	Zout			50		Ω

9.3 Specifications of the Crystal Resonator

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency	F_xtal			48		MHz
Equivalent series resistance (ESR)	ESR_xtal			20	80	Ω
Load capacitance (CL)	CL_xtal		5		9	pF

9.4 DC Characteristics

9.4.1 Digital input/output pins

VDD = 3.3 V, 25°C

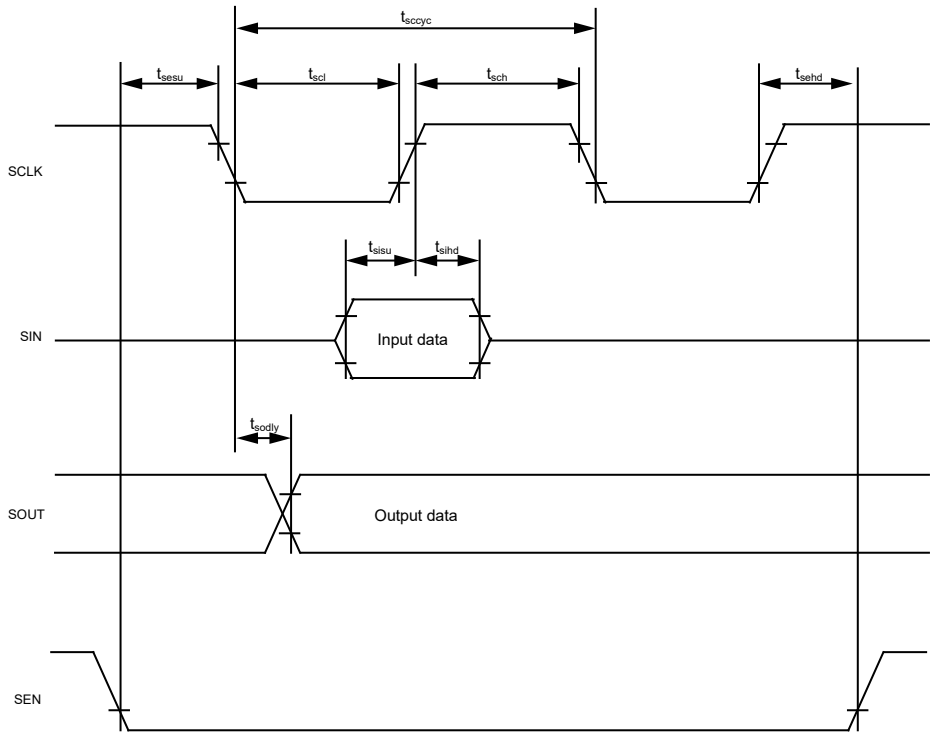
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High-level input voltage	V_{IHRF}	RSTB, SIN, SCLK, SEN, GPIO0 to GPIO12	2.4		VDD	V
Low-level input voltage	V_{ILRF}	RSTB, MODE, SIN, SCLK, SEN, GPIO0 to GPIO12	0		0.1 × VDD	V
High-level output voltage	V_{OHRF}	Ioh = 0 mA, SOUT, GPIO0 to GPIO12	VDD - 0.1		VDD	V
Low-level output voltage	V_{OLRF}	Iol = 0 mA, SOUT, GPIO0 to GPIO12	0		0.1	V
High-level output current	I_{OHRF}	V_{OHRF} = VDD - 0.4 V, SOUT, GPIO0 to GPIO12			-4	mA
Low-level output current	I_{OLRF}	V_{OLRF} = 0.4 V, SOUT, GPIO0 to GPIO12			+4	mA
High-level input leakage current	I_{LIHRF1}	Vin = VDD, SIN, SCLK, SEN, GPIO0 to GPIO12, RSTB			200	µA
Low-level input leakage current 1	I_{LILRF1}	Vin = GND, SIN, SCLK, SEN, GPIO0 to GPIO12			-200	µA
High-level input leakage current 2 (with no pulling-up)	I_{LIHRF2}	Vin = VDD, SIN, SCLK, SEN, GPIO0 to GPIO12			10	µA
Low-level input leakage current 2 (with no pulling-up)	I_{LILRF2}	Vin = GND, SIN, SCLK, SEN, GPIO0 to GPIO12			-10	µA

9.5 AC Characteristics

9.5.1 Serial peripheral interface (SPI)

VDD = 3.3 V, 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK cycle time	t_{sccyc}		41.67			ns
SCLK high-level width	t_{sch}		18.5			ns
SCLK low-level width	t_{scl}		18.5			ns
SIN setup time	t_{sisu}		15			ns
SIN hold time	t_{sihd}		15			ns
SOUT output delay time	t_{sodly}				14.8	ns
SEN setup time	t_{sesu}		33.3			ns
SEN hold time	t_{sehd}		200			ns



9.6 Characteristics of the Power Supply Current

Data rate = 100 kbps, 2-FSK, modulation index = 1.0, frequency = 920.6 MHz, VDD = 3.3 V, 25°C

Item	Condition	Min.	Typ.	Max.	Unit
SUN-FSK transmission supply current	+15.0 dBm		62		mA
	+10.0 dBm		41		
	+8.0 dBm		36		
	+0.0 dBm		23		

Data rate = 100 kbps (MCS2), band width = 400 kHz (option 3), frequency = 920.6 MHz, VDD = 3.3 V, 25°C

Item	Condition	Min.	Typ.	Max.	Unit
SUN-OFDM transmission supply current	+10.0 dBm		68.0		mA

Data rate = 100 kbps, 2-FSK, modulation index = 1.0, frequency = 920.6 MHz, VDD = 3.3 V, 25°C

Item	Condition	Min.	Typ.	Max.	Unit
SUN-FSK reception supply current	RF input at reception: -95 dBm		16.7		mA
	No RF input while waiting for reception		16.8		

Data rate = 100 kbps (MCS2), band width = 400 kHz (option 3), frequency = 920.6 MHz, VDD = 3.3 V, 25°C

Item	Condition	Min.	Typ.	Max.	Unit
SUN-OFDM reception supply current	RF input at reception: -95 dBm		21.5		mA
	No RF input while waiting for reception		21.7		

VDD = 3.3 V, 25°C

Item	Condition	Min.	Typ.	Max.	Unit
SLEEP			0.5		µA
IDLE			5.5		mA

9.7 Characteristics of the Transceiver Reception

9.7.1 Reception sensitivity for SUN FSK

Packet length = 250 bytes, packet error rate (PER) = 10%, with no forward error correction (FEC), VDD = 3.3 V, 25°C

- North America (Frequency: 920.6 MHz)

Modulation Parameter	Channel Spacing [kHz]	Data Rate [kbps]	Modulation Index	Modulation Method	Min.	Typ.	Max.	Unit
Operating mode #1a	50	10	1	2-GFSK		-116		dBm
Operating mode #1b	100	20	1	2-GFSK		-113		dBm
Operating mode #1	200	50	1	2-GFSK		-109		dBm
Operating mode #2	400	150	0.5	2-GFSK		-105		dBm
Operating mode #3	400	200	0.5	2-GFSK		-104		dBm

- Europe (Frequency: 870.6 MHz)

Modulation Parameter	Channel Spacing [kHz]	Data Rate [kbps]	Modulation Index	Modulation Method	Min.	Typ.	Max.	Unit
Operating mode #1a	50	10	1	2-GFSK		-115		dBm
Operating mode #1b	100	20	1	2-GFSK		-112		dBm
Operating mode #1	100	50	0.5	2-GFSK		-109		dBm
Operating mode #2	200	100	0.5	2-GFSK		-106		dBm
Operating mode #3	200	150	0.5	2-GFSK		-104		dBm

- Japan (Frequency: 920.6 MHz)

Modulation Parameter	Channel Spacing [kHz]	Data Rate [kbps]	Modulation Index	Modulation Method	Min.	Typ.	Max.	Unit
Operating mode #1a	50	10	1	2-GFSK		-116		dBm
Operating mode #1b	100	20	1	2-GFSK		-113		dBm
Operating mode #1	200	50	1	2-GFSK		-109		dBm
Operating mode #2	400	100	1	2-GFSK		-105		dBm
Operating mode #3	600	200	1	2-GFSK		-102		dBm

9.7.2 Adjacent channel rejection ratio for SUN FSK

Packet length = 250 bytes, packet error rate (PER) = 10%, with no forward error correction (FEC), VDD = 3.3 V, 25°C, desired wave input level: sensitivity specified in the standard[1] + 3 dB

- North America (Frequency: 920.6 MHz)

Modulation Parameter	Channel Spacing [kHz]	Data Rate [kbps]	Modulation Index	Modulation Method	Min. (-1ch/+1ch)	Typ. (-1ch/+1ch)	Max. (-1ch/+1ch)	Unit
Operating mode #1a	50	10	1	2-GFSK		47/47		dB
Operating mode #1b	100	20	1	2-GFSK		44/44		dB
Operating mode #1	200	50	1	2-GFSK		44/44		dB
Operating mode #2	400	150	0.5	2-GFSK		48/48		dB
Operating mode #3	400	200	0.5	2-GFSK		41/42		dB

- Europe (Frequency: 863.1 MHz)

Modulation Parameter	Channel Spacing [kHz]	Data Rate [kbps]	Modulation Index	Modulation Method	Min. (-1ch/+1ch)	Typ. (-1ch/+1ch)	Max. (-1ch/+1ch)	Unit
Operating mode #1a	50	10	1	2-GFSK		45/45		dB
Operating mode #1b	100	20	1	2-GFSK		42/42		dB
Operating mode #1	100	50	0.5	2-GFSK		38/38		dB
Operating mode #2	200	100	0.5	2-GFSK		41/40		dB
Operating mode #3	200	150	0.5	2-GFSK		34/34		dB

- Japan (Frequency: 920.6 MHz)

Modulation Parameter	Channel Spacing [kHz]	Data Rate [kbps]	Modulation Index	Modulation Method	Min. (-1ch/+1ch)	Typ. (-1ch/+1ch)	Max. (-1ch/+1ch)	Unit
Operating mode #1a	50	10	1	2-GFSK		47/47		dB
Operating mode #1b	100	20	1	2-GFSK		44/44		dB
Operating mode #1	200	50	1	2-GFSK		44/45		dB
Operating mode #2	400	100	1	2-GFSK		49/49		dB
Operating mode #3	600	200	1	2-GFSK		48/49		dB

9.7.3 Alternate channel rejection ratio for SUN FSK

Packet length = 250 bytes, packet error rate (PER) = 10%, with no forward error correction (FEC), VDD = 3.3 V, 25°C, desired wave input level: sensitivity specified in the standard[1] + 3 dB

- North America (Frequency: 920.6 MHz)

Modulation Parameter	Channel Spacing [kHz]	Data Rate [kbps]	Modulation Index	Modulation Method	Min. (-2ch/+2ch)	Typ. (-2ch/+2ch)	Max. (-2ch/+2ch)	Unit
Operating mode #1a	50	10	1	2-GFSK		48/48		dB
Operating mode #1b	100	20	1	2-GFSK		49/49		dB
Operating mode #1	200	50	1	2-GFSK		53/53		dB
Operating mode #2	400	150	0.5	2-GFSK		57/58		dB
Operating mode #3	400	200	0.5	2-GFSK		55/55		dB

- Europe (Frequency: 863.1 MHz)

Modulation Parameter	Channel Spacing [kHz]	Data Rate [kbps]	Modulation Index	Modulation Method	Min. (-2ch/+2ch)	Typ. (-2ch/+2ch)	Max. (-2ch/+2ch)	Unit
Operating mode #1a	50	10	1	2-GFSK		45/45		dB
Operating mode #1b	100	20	1	2-GFSK		45/46		dB
Operating mode #1	100	50	0.5	2-GFSK		44/44		dB
Operating mode #2	200	100	0.5	2-GFSK		51/51		dB
Operating mode #3	200	150	0.5	2-GFSK		46/38		dB

- Japan (Frequency: 920.6 MHz)

Modulation Parameter	Channel Spacing [kHz]	Data Rate [kbps]	Modulation Index	Modulation Method	Min. (-2ch/+2ch)	Typ. (-2ch/+2ch)	Max. (-2ch/+2ch)	Unit
Operating mode #1a	50	10	1	2-GFSK		48/48		dB
Operating mode #1b	100	20	1	2-GFSK		49/49		dB
Operating mode #1	200	50	1	2-GFSK		53/53		dB
Operating mode #2	400	100	1	2-GFSK		59/60		dB
Operating mode #3	600	200	1	2-GFSK		47/58		dB

9.7.4 Characteristics of the SUN-FSK reception

Frequency = 920.6 MHz, 2-GFSK, 50 kbps, modulation index = 1.0, VDD = 3.3 V, 25°C

Item	Condition	Min.	Typ.	Max.	Unit
Maximum RF input voltage	Packet length = 250 bytes Packet error rate (PER) = 10%			+10	dBm
RSSI range		-108		-5	dBm
RSSI resolution			1		dB
RSSI precision		-5		5	dB
Frequency deviation tolerance	Sensitivity degradation: 1 dB	-10		10	ppm
Modulation quality tolerance (fdev_error)	Sensitivity degradation: 3 dB	-20		20	%

9.7.5 Reception sensitivity for SUN OFDM

- North America and Japan

Frequency = 920.6 MHz, packet length = 250 bytes, packet error rate (PER) = 10%, VDD = 3.3 V, 25°C,
typical values

Modulation Parameter	Option 1	Option 2	Option 3	Option 4	Unit
MCS0 (BPSK 1/2 w/ 4xfreq.rep)	-113	-116	-118	-119	dBm
MCS1 (BPSK 1/2 w/ 2xfreq.rep)	-110	-114	-117	-118	
MCS2 (QPSK 1/2 w/ 2xfreq.rep)	-107	-110	-114	-112	
MCS3 (QPSK 1/2)	-104	-107	-111	-111	
MCS4 (QPSK 3/4)	-102	-104	-108	-109	
MCS5 (16QAM 1/2)	-99	-101	-105	-106	
MCS6 (16QAM 3/4)	-95	-98	-101	-103	

9.7.6 Adjacent channel rejection ratio for SUN OFDM

- North America and Japan

Frequency = 920.6 MHz, packet length = 250 bytes, packet error rate (PER) = 10%, VDD = 3.3 V, 25°C,
typical values, desired wave input level: sensitivity specified in the standard[1] + 3 dB

Parameter	Option 1	Option 2	Option 3	Option 4	Unit
	-1.2/+1.2 MHz	-0.8/+0.8 MHz	-0.4/+0.4 MHz	-0.2/+0.2 MHz	
MCS0 (BPSK 1/2 w/ 4xfreq.rep)	33/31	44/48	49/45	34/31	dB
MCS1 (BPSK 1/2 w/ 2xfreq.rep)	33/31	43/53	46/44	34/31	
MCS2 (QPSK 1/2 w/ 2xfreq.rep)	34/31	40/52	47/45	33/31	
MCS3 (QPSK 1/2)	33/31	37/49	42/45	33/31	
MCS4 (QPSK 3/4)	31/30	33/46	46/45	33/31	
MCS5 (16QAM 1/2)	28/28	31/44	44/42	32/31	
MCS6 (16QAM 3/4)	23/23	28/41	41/39	31/30	

9.7.7 Alternate channel rejection ratio for SUN OFDM

- North America and Japan

Frequency = 920.6 MHz, packet length = 250 bytes, packet error rate (PER) = 10%, VDD = 3.3 V, 25°C,

typical values, desired wave input level: sensitivity specified in the standard[1] + 3 dB

Parameter	Option 1	Option 2	Option 3	Option 4	Unit
	-2.4/+2.4 MHz	-1.6/+1.6 MHz	-0.8/+0.8 MHz	-0.4/+0.4 MHz	
MCS0 (BPSK 1/2 w/ 4xfreq.rep)	50/48	54/58	60/63	49/49	dB
MCS1 (BPSK 1/2 w/ 2xfreq.rep)	47/46	52/62	60/63	50/50	
MCS2 (QPSK 1/2 w/ 2xfreq.rep)	54/55	54/58	59/59	48/48	
MCS3 (QPSK 1/2)	52/53	52/52	56/56	47/48	
MCS4 (QPSK 3/4)	47/51	51/51	53/53	47/48	
MCS5 (16QAM 1/2)	46/48	48/50	50/50	47/48	
MCS6 (16QAM 3/4)	42/44	45/47	47/47	46/46	

9.7.8 Co-channel rejection ratio for SUN OFDM

- North America and Japan

Frequency = 920.6 MHz, packet length = 250 bytes, packet error rate (PER) = 10%, VDD = 3.3 V, 25°C,

typical values, desired wave input level: sensitivity specified in the standard[1] + 3 dB

Parameter	Option 1	Option 2	Option 3	Option 4	Unit
	±0 kHz	±0 kHz	±0 kHz	±0 kHz	
MCS0 (BPSK 1/2 w/ 4xfreq.rep)	4	3	2	-1	dB
MCS1 (BPSK 1/2 w/ 2xfreq.rep)	2	2	1	-1	
MCS2 (QPSK 1/2 w/ 2xfreq.rep)	-2	-2	-3	-9	
MCS3 (QPSK 1/2)	-5	-5	-4	-7	
MCS4 (QPSK 3/4)	-7	-7	-7	-8	
MCS5 (16QAM 1/2)	-10	-12	-10	-11	
MCS6 (16QAM 3/4)	-13	-13	-13	-13	

9.7.9 Characteristics of the SUN-OFDM reception

Frequency = 920.6 MHz, option 1, MCS6, VDD = 3.3 V, 25°C

Item	Condition	Min.	Typ.	Max.	Unit
Maximum RF input power	Packet length = 250 bytes Packet error rate (PER): 10%		+5		dBm
RSSI range		-97		-5	dBm
RSSI resolution			1		dB
RSSI accuracy		-5		5	dB
Frequency deviation tolerance	Sensibility degradation: 1 dB	-20		20	ppm
Modulation quality tolerance (degradation of sensitivity)	Error vector magnitude (EVM): IEEE802.15.4-2020[1]		2		dB

9.8 Characteristics of Transceiver Transmission

9.8.1 Characteristics of the SUN-FSK transmission

Frequency = 920.6 MHz, VDD = 3.3 V, 25°C

Item		Condition		Min.	Typ.	Max.	Unit
Maximum transmission output power		CW			+15.0		dBm
Minimum transmission output power		CW			-15.0		dBm
Adjustable step size for transmission output power		CW			1.0		dB
Deviation of the output power depending on the temperature		Ta: -40°C to +85°C				2	dB
Harmonics	Second	Output power level = +15 dBm			-41.3		dBm
	Third				-41.3		dBm
	Fourth to seventh				-41.3		dBm
Frequency deviation error		Output power level = +15 dBm				30	%
Maximum zero crossing offset		Output power level = +15 dBm		-12.5		12.5	%
Transmission frequency deviation		Output power level = +15 dBm		-20		20	ppm
Adjacent channel leakage ratio		Output power level = +15 dBm	50 kbps, MI = 0.5		-49		dB
			50 kbps, MI = 1.0		-50		
			100 kbps, MI = 0.5		-50		
			100 kbps, MI = 1.0		-47		

9.8.2 Characteristics of the SUN-OFDM transmission

Frequency = 920.6 MHz, option 1, VDD = 3.3 V, 25°C

Item		Condition	Min.	Typ.	Max.	Unit
Maximum transmission output power		BPSK, R = 1/2, (MCS0,1), EVM = -10 dB		11		dBm
		QPSK, R = 1/2, (MCS2,3), EVM = -13 dB		10		
		QPSK, R = 3/4, (MCS4), EVM = -13 dB		10		
		16QAM, R = 1/2, (MCS5), EVM = -19 dB		9		
		16QAM, R = 3/4, (MCS6), EVM = -19 dB		9		
Minimum transmission output power		BPSK, R = 1/2, (MCS0,1), EVM = -10 dB		-19		dBm
		QPSK, R = 1/2, (MCS2,3), EVM = -13 dB		-19		
		QPSK, R = 3/4, (MCS4), EVM = -13 dB		-19		
		16QAM, R = 1/2, (MCS5), EVM = -19 dB		-19		
		16QAM, R = 3/4, (MCS6), EVM = -19 dB		-19		
Adjustable step size for transmission output power				1.0		dB
Deviation of the output power depending on the temperature		Ta: -40°C to +85°C		2		dB
Harmonic	Second harmonic	The transmission output power is at its maximum.		-41.3		dBm
	Third harmonic			-41.3		dBm
	Fourth to seventh harmonic			-41.3		dBm
Adjacent channel leakage ratio		BPSK, R = 1/2 (MCS0,1), +11 dBm output		-29		dB
		QPSK, R = 1/2 (MCS2,3), +10 dBm output		-31		
		QPSK, R = 3/4 (MCS4), +10 dBm output		-31		
		16QAM, R = 1/2 (MCS5), +9 dBm output		-33		
		16QAM, R = 3/4 (MCS6), +9 dBm output		-33		

9.9 Specifications of the Data Rate

- SUN FSK

Data Rate [kbps]	Modulation Method	Modulation Index	Descriptions
10	2-GFSK	1.0	
20	2-GFSK	1.0	
50	2-GFSK	0.5	
50	2-GFSK	1.0	
100	2-GFSK	0.5	
100	2-GFSK	1.0	
150	2-GFSK	0.5	
200	2-GFSK	0.5	
200	2-GFSK	1.0	

- SUN OFDM

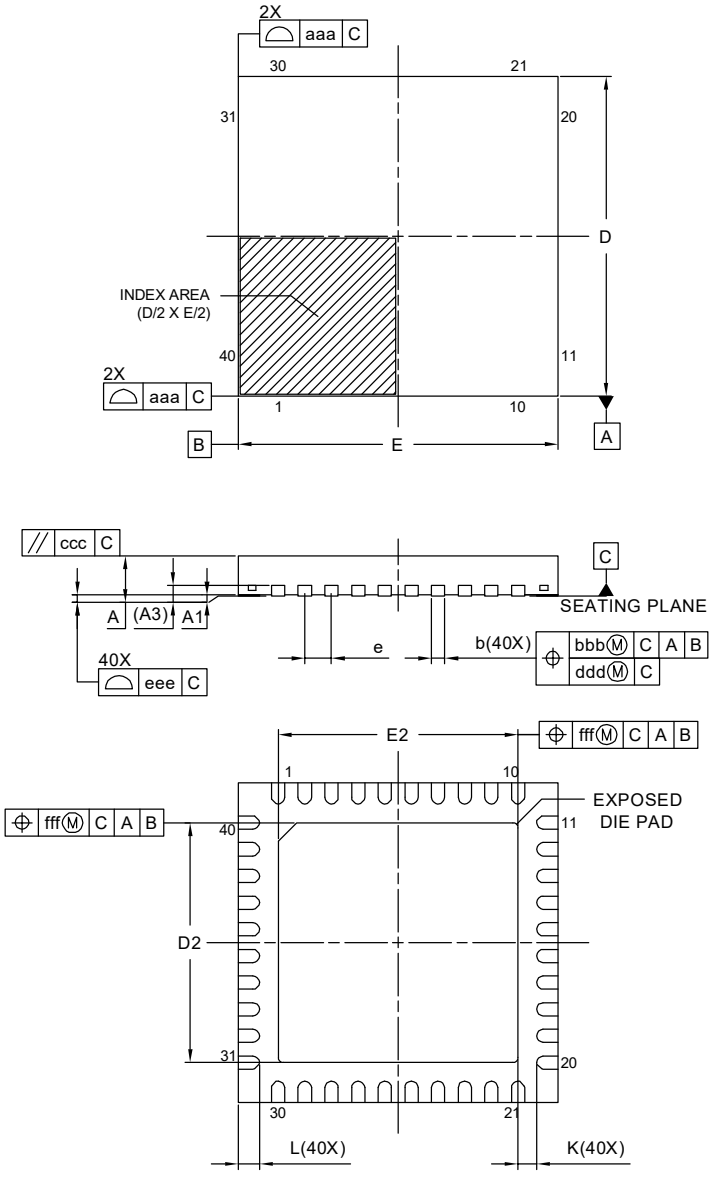
Parameter	Option 1 Band Width: 1200 kHz	Option 2 Band Width: 800 kHz	Option 3 Band Width: 400 kHz	Option 4 Band Width: 200 kHz	Unit	Descriptions
MCS0	100	50	25	12.5	kbps	BPSK CR = 1/2 with 4xFreq. repetition
MCS1	200	100	50	25		BPSK CR = 1/2 with 2xFreq. repetition
MCS2	400	200	100	50		QPSK CR = 1/2 with 2xFreq. repetition
MCS3	800	400	200	100		QPSK CR = 1/2
MCS4	1200	600	300	150		QPSK CR = 3/4
MCS5	1600	800	400	200		16-QAM CR = 1/2
MCS6	2400	1200	600	300		16-QAM CR = 3/4

9.10 Compliant Standard

[1] IEEE Std 802.15.4™ -2020: IEEE Standard for Low-Rate Wireless Networks

Section 10 Package Drawings

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN040-6x6-0.50	PWQN0040KD-A	0.08



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		6.00 BSC	
E		6.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	4.45	4.50	4.55
E_2	4.45	4.50	4.55
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Appendix A Revision History

A.1 Major Revisions in This Edition

Rev.	Date	Description	
		Pages	Summary
1.00	Jan. 31, 2022	—	First edition issued
1.10	Jun. 30, 2022	Section 1 Overview	
		7	Table 1-1 List of the Ordering Part Numbers was changed.
		Section 3 Baseband Section: Some descriptions were added in the following subsections.	
		55	3.4.21 Timer read registers 0 and 1 (BBTIMEREAD0 and BBTIMEREAD1)
		74	3.4.43 Received data counter register (BBRXCOUNT)
		82	3.4.51 Transmitted data counter register (BBTXCOUNT)
		175	3.4.120 Total reception counter (BBRCVCOUNT)
		176	3.4.121 PHR error counter (BBPHRERRCOUNT)
		177	3.4.122 Number-of-successful-receptions counter (BBRCVOKCOUNT)
		178	3.4.123 Number-of-unsuccessful-receptions counter (BBRCVNGCOUNT)
		Section 7 Point to Note on Using the Baseband Section	
		278	This section was newly added.
1.20	Apr. 28, 2023	Section 1 Overview	
		3	1.3 Block Diagram was changed.
		Section 2 Pin Functions	
		8	2.1.1 Digital Pins, 6. XIN, XOUT: The sub-section number in the description was changed.
		9	2.1.3 Power Supply Pins: The section number in the description was changed.

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