User's Manual

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R8C/54E Group, R8C/54F Group, R8C/54G Group, R8C/54H Group

User's Manual: Hardware

RENESAS MCU

R8C Family / R8C/5x Series

Renesas Electronics
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.
The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. For details, refer to the text of the manual.

The following documents apply to the R8C/54E Group, R8C/54F Group, R8C/54G Group, R8C/54H Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Datasheet	Hardware overview characteristic	R8C/54E Group, R8C/54F Group, R8C/54G Group, R8C/54H Group Datasheet	R01DS0043EJ
User's manual: Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	R8C/54E Group, R8C/54F Group, R8C/54G Group, R8C/54H Group User's Manual: Hardware	This User's manual
User's manual: Software	Description of CPU instruction set	R8C/5x Series User's manual: Software	R01US0007EJ
Application note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas technical update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names
Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.
Examples the SRST bit in the PM0 register
P3_5 pin, VCC pin

(2) Peripheral Function Names, Register Names, and Pin Names
The number after the underscore (_) in peripheral function names, register names, and pin names indicates the corresponding number of on-chip modules.
Examples
- Peripheral function names
  Timer RC: Timer RC_0, Timer RC_1
  Timer RJ: Timer RJ_0, Timer RJ_1, Timer RJ_2, Timer RJ_3
- Pin names
  Timer RC: TRCCLK_0, TRCCLK_1
  UART0: RXD_0, RXD_1, RXD_2, RXD_3

(3) Notation of Numbers
The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.
Examples Binary: 11b
Hexadecimal: EFA0h
Decimal: 1234

3. Register Notation

The symbols and terms used in register diagrams are described below.

x.x.x XXX Register (Symbol)

Address XXXXXh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	XXX7	XXX6	XXX5	—	—	—	XXX1	XXX0
After Reset	0	0	0	0	0	0	0	0

*1

Bit	Symbol	Bit Name	Function	R/W
b0	XXX0	XXX bit	b1 b0 0 0: XXX 0 1: XXX 1 0: Do not set. 1 1: XXX	R/W
b1	XXX1			R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is undefined.		—
b3	—	Reserved	Set to 0.	W
b4	—			
b5	XXX5	XXX bits	Function varies depending on the operating mode.	R/W
b6	XXX6			R/W
b7	XXX7	XXX bit	0: XXX 1: XXX	R

*2 *3

*1
R/W: Read and write.
R: Read only.
W: Write only.
—: Nothing is assigned.

*2
• Reserved
Reserved bits. Set to the specified value. For R/W bits, the written value is read unless otherwise noted.

*3
• Nothing is assigned.
Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.
• Do not set.
Operation is not guaranteed when a value is set.
• Function varies depending on the operating mode.
The function of the bit varies with the peripheral function mode. For information on the individual modes, refer to the register diagram.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Table of Contents

SFR Page Reference

Address	Register Name	Symbol	Page
00000h			
00001h			
00002h			
00003h			
00004h	Processor Mode Register 0	PM0	55, 66
00005h	Processor Mode Register 1	PM1	56
00006h			
00007h	Protect Register	PRCR	57
00008h	System Clock Control Register 0	CM0	109, 131
00009h	System Clock Control Register 1	CM1	110, 132
0000Ah	Oscillation Stop Detection Register	OCD	111
0000Bh	System Clock Control Register 3	CM3	112, 133
0000Ch	System Clock Control Register 4	CM4	113, 134
0000Dh			
0000Eh			
0000Fh	Peripheral Clock Select Register 1	PCLKR1	114
00010h			
00011h			
00012h	High-Speed On-Chip Oscillator Control Register 0	FRA0	114, 135
00013h			
00014h	High-Speed On-Chip Oscillator Control Register 2	FRA2	115
00015h			
00016h			
00017h			
00018h			
00019h			
0001Ah			
0001Bh			
0001Ch	PLL Control Register 0	PLC0	116
0001Dh			
0001Eh			
0001Fh			
00020h	Reset Interrupt Select Register	RISR	97
00021h	Watchdog Timer Reset Register	WDTR	97
00022h	Watchdog Timer Start Register	WDTS	98
00023h	Watchdog Timer Control Register	WDTC	98
00024h	Count Source Protection Mode Register	CSPR	99
00025h			
00026h			
00027h			
00028h	Reset Source Determination Register	RSTFR	67
00029h			
0002Ah			
0002Bh			
0002Ch	STBY VDC Power Control Register	SVDC	135
0002Dh			
0002Eh			
0002Fh			
00030h	Voltage Monitor Circuit Control Register	CMPA	81
00031h	Voltage Monitor Circuit Edge Select Register	VCAC	82
00032h	On-Chip Reference Voltage Control Register	OCVREFCR	645
00033h			
00034h	Voltage Detection Register 2	VCA2	82, 117
00035h			
00036h	Voltage Detection 1 Level Select Register	VD1LS	83
00037h			
00038h	Voltage Monitor 0 Circuit Control Register	VW0C	84
00039h	Voltage Monitor 1 Circuit Control Register	VW1C	85

Note:
1. Do not access the reserved areas.

Address	Register Name	Symbol	Page
0003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	86
0003Bh			
0003Ch			
0003Dh			
0003Eh			
0003Fh			
00040h			
00041h	Interrupt Control Register	FMRDYIC	156
00042h	Interrupt Control Register	TRJIC_1	156
00043h			
00044h			
00045h			
00046h	Interrupt Control Register	INT4IC	156
00047h	Interrupt Control Register	TRCIC_0	156
00048h	Interrupt Control Register	TRD0IC_0	156
00049h	Interrupt Control Register	TRD1IC_0	156
0004Ah	Interrupt Control Register	TRE2IC	156
0004Bh	Interrupt Control Register	U2TIC	156
0004Ch	Interrupt Control Register	U2RIC	156
0004Dh	Interrupt Control Register	KUPIC	156
0004Eh	Interrupt Control Register	ADIC	156
0004Fh	Interrupt Control Register	SSUIC_0/IICIC_0	156
00050h			
00051h	Interrupt Control Register	U0TIC_0	156
00052h	Interrupt Control Register	U0RIC_0	156
00053h	Interrupt Control Register	U0TIC_1	156
00054h	Interrupt Control Register	U0RIC_1	156
00055h	Interrupt Control Register	INT2IC	156
00056h	Interrupt Control Register	TRJIC_0	156
00057h			
00058h	Interrupt Control Register	TRB2IC_0	156
00059h	Interrupt Control Register	INT1IC	156
0005Ah	Interrupt Control Register	INT3IC	156
0005Bh			
0005Ch			
0005Dh	Interrupt Control Register	INT0IC	156
0005Eh	Interrupt Control Register	U2BCNIC	156
0005Fh			
00060h			
00061h			
00062h			
00063h			
00064h			
00065h			
00066h			
00067h			
00068h			
00069h			
0006Ah			
0006Bh			
0006Ch	Interrupt Control Register	CANRXIC_0	156
0006Dh	Interrupt Control Register	CANTXIC_0	156
0006Eh	Interrupt Control Register	CANERIC_0	156
0006Fh			
00070h			
00071h			
00072h	Interrupt Control Register	VCMP1IC	156
00073h	Interrupt Control Register	VCMP2IC	156
00074h			
00075h			
00076h			
00077h			
00078h			
00079h	Interrupt Control Register	SSUIC_1/IICIC_1	156

Address	Register Name	Symbol	Page
0007Ah			
0007Bh			
0007Ch			
0007Dh			
0007Eh			
0007Fh			
00080h	UART0_0 Transmit/Receive Mode Register	U0MR_0	437
00081h	UART0_0 Bit Rate Register	U0BRG_0	438
00082h	UART0_0 Transmit Buffer Register	U0TB_0	438
00083h			
00084h	UART0_0 Transmit/Receive Control Register 0	U0C0_0	439
00085h	UART0_0 Transmit/Receive Control Register 1	U0C1_0	440
00086h	UART0_0 Receive Buffer Register	U0RB_0	441
00087h			
00088h	UART0_0 Interrupt Flag and Enable Register	U0IR_0	442
00089h			
0008Ah			
0008Bh			
0008Ch	LIN_0 Special Function Register	LINCR2_0	565
0008Dh			
0008Eh	LIN_0 Control Register	LINCT_0	565
0008Fh	LIN_0 Status Register	LINST_0	566
00090h	UART0_1 Transmit/Receive Mode Register	U0MR_1	437
00091h	UART0_1 Bit Rate Register	U0BRG_1	438
00092h	UART0_1 Transmit Buffer Register	U0TB_1	438
00093h			
00094h	UART0_1 Transmit/Receive Control Register 0	U0C0_1	439
00095h	UART0_1 Transmit/Receive Control Register 1	U0C1_1	440
00096h	UART0_1 Receive Buffer Register	U0RB_1	441
00097h			
00098h	UART0_1 Interrupt Flag and Enable Register	U0IR_1	442
00099h			
0009Ah			
0009Bh			
0009Ch	LIN_1 Special Function Register	LINCR2_1	565
0009Dh			
0009Eh	LIN_1 Control Register	LINCT_1	565
0009Fh	LIN_1 Status Register	LINST_1	566
000A0h			
000A1h			
000A2h			
000A3h			
000A4h			
000A5h			
000A6h			
000A7h			
000A8h			
000A9h			
000AAh			
000ABh			
000ACh			
000ADh			
000AEh			
000AFh			
000B0h			
000B1h			
000B2h			
000B3h			
000B4h			
000B5h			
000B6h			
000B7h			
000B8h			
000B9h			

Address	Register Name	Symbol	Page
000BAh			
000BBh			
000BCh			
000BDh			
000BEh			
000BFh			
000C0h	UART2 Transmit/Receive Mode Register	U2MR	462
000C1h	UART2 Bit Rate Register	U2BRG	462
000C2h	UART2 Transmit Buffer Register	U2TB	463
000C3h			
000C4h	UART2 Transmit/Receive Control Register 0	U2C0	464
000C5h	UART2 Transmit/Receive Control Register 1	U2C1	465
000C6h	UART2 Receive Buffer Register	U2RB	466
000C7h			
000C8h	UART2 Digital Filter Function Select Register	U2RXDF	467
000C9h			
000CAh			
000CBh			
000CCh			
000CDh			
000CEh			
000CFh			
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000D1h			
000D2h			
000D3h			
000D4h			
000D5h	UART2 Special Mode Register 3	U2SMR3	468
000D6h			
000D7h	UART2 Special Mode Register	U2SMR	469
000D8h			
000D9h			
000DAh			
000DBh			
000DCh			
000DDh			
000DEh			
000DFh			
000E0h	I^2C_0 Control Register	IICCR_0	500
000E1h	SS_0 Bit Counter Register	SSBR_0	501
000E2h	SI_0 Transmit Data Register	SITDR_0	502
000E3h			
000E4h	SI_0 Receive Data Register	SIRDR_0	502
000E5h			
000E6h	SI_0 Control Register 1	SICR1_0	503
000E7h	SI_0 Control Register 2	SICR2_0	505
000E8h	SI_0 Mode Register 1	SIMR1_0	507
000E9h	SI_0 Interrupt Enable Register	SIER_0	509
000EAh	SI_0 Status Register	SISR_0	511
000EBh	SI_0 Mode Register 2	SIMR2_0	513
000ECh			
000EDh			
000EEh			
000EFh			
000F0h	I^2C_1 Control Register	IICCR_1	500
000F1h	SS_1 Bit Counter Register	SSBR_1	501
000F2h	SI_1 Transmit Data Register	SITDR_1	502
000F3h			
000F4h	SI_1 Receive Data Register	SIRDR_1	502
000F5h			
000F6h	SI_1 Control Register 1	SICR1_1	503
000F7h	SI_1 Control Register 2	SICR2_1	505
000F8h	SI_1 Mode Register 1	SIMR1_1	507
000F9h	SI_1 Interrupt Enable Register	SIER_1	509

Note:
1. Do not access the reserved areas.

Address	Register Name	Symbol	Page
000FAh	SI_1 Status Register	SISR_1	511
000FBh	SI_1 Mode Register 2	SIMR2_1	513
000FCh			
000FDh			
000FEh			
000FFh			
00100h			
00101h			
00102h			
00103h			
00104h			
00105h			
00106h			
00107h			
00108h			
00109h			
0010Ah			
0010Bh			
0010Ch			
0010Dh			
0010Eh			
0010Fh			
00110h	Timer RJ_0 Counter Register	TRJ_0	252
00111h			
00112h	Timer RJ_0 Control Register	TRJCR_0	253
00113h	Timer RJ_0 I/O Control Register	TRJIOC_0	254
00114h	Timer RJ_0 Mode Register	TRJMR_0	256
00115h	Timer RJ_0 Event Pin Select Register	TRJISR_0	257
00116h			
00117h			
00118h	Timer RJ_1 Counter Register	TRJ_1	252
00119h			
0011Ah	Timer RJ_1 Control Register	TRJCR_1	253
0011Bh	Timer RJ_1 I/O Control Register	TRJIOC_1	254
0011Ch	Timer RJ_1 Mode Register	TRJMR_1	256
0011Dh	Timer RJ_1 Event Pin Select Register	TRJISR_1	257
0011Eh			
0011Fh			
00120h			
00121h			
00122h			
00123h			
00124h			
00125h			
00126h			
00127h			
00128h			
00129h			
0012Ah			
0012Bh			
0012Ch			
0012Dh			
0012Eh			
0012Fh			
00130h	Timer RB2_0 Control Register	TRBCR_0	271
00131h	Timer RB2_0 One-Shot Control Register	TRBOCR_0	272
00132h	Timer RB2_0 I/O Control Register	TRBIOC_0	273
00133h	Timer RB2_0 Mode Register	TRBMR_0	274
00134h	Timer RB2_0 Prescaler Register Timer RB2_0 Primary/Secondary Register(Lower 8 Bits)	TRBPRE_0 / TRBPRSC_0	275
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00136h	Timer RB2_0 Secondary Register Timer RB2_0 Secondary Register (Higher 8 Bits)	TRBSC_0	277
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00139h			

Address	Register Name	Symbol	Page
0013Ah	Timer RC_0 General Register A	TRCGRA_0	305
0013Bh			
0013Ch	Timer RC_0 General Register B	TRCGRB_0	305
0013Dh			
0013Eh	Timer RC_0 General Register C	TRCGRC_0	305
0013Fh			
00140h	Timer RC_0 General Register D	TRCGRD_0	305
00141h			
00142h	Timer RC_0 Mode Register	TRCMR_0	307
00143h	Timer RC_0 Control Register 1	TRCCR1_0	309
00144h	Timer RC_0 Interrupt Enable Register	TRCIER_0	310
00145h	Timer RC_0 Status Register	TRCSR_0	311
00146h	Timer RC_0 I/O Control Register 0	TRCIOR0_0	312
00147h	Timer RC_0 I/O Control Register 1	TRCIOR1_0	313
00148h	Timer RC_0 Control Register 2	TRCCR2_0	314
00149h	Timer RC_0 Digital Filter Function Select Register	TRCDF_0	315
0014Ah	Timer RC_0 Output Enable Register	TRCOER_0	316
0014Bh	Timer RC_0 A/D Conversion Trigger Control Register	TRCADCR_0	317
0014Ch	Timer RC_0 Output Waveform Manipulation Register	TRCOPR_0	318
0014Dh	Timer RC_0 ELC Cooperation Control Register	TRCELCCR_0	319
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0014Fh			
00150h			
00151h			
00152h			
00153h			
00154h			
00155h			
00156h			
00157h			
00158h			
00159h			
0015Ah			
0015Bh			
0015Ch			
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00160h			
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00165h			
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00167h			
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00169h			
0016Ah			
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0016Dh			
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0016Fh			
00170h	Timer RE2 Counter Data Register	TRESEC	424
00171h	Timer RE2 Compare Data Register	TREMIN	424
00172h			
00173h			
00174h			
00175h			
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00177h	Timer RE2 Control Register	TRECR	425
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00179h			

Note:
1. Do not access the reserved areas.

Address	Register Name	Symbol	Page
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0017Dh			
0017Eh			
0017Fh	Timer RE2 Protect Register	TREPRC	429
00180h	Timer RD_0 ELC Cooperation Control Register	TRDELCCR_0	355
00181h			
00182h	Timer RD_0 Trigger Control Register	TRDADCR_0	356
00183h	Timer RD_0 Start Register	TRDSTR_0	357
00184h	Timer RD_0 Mode Register	TRDMR_0	358
00185h	Timer RD_0 PWM Mode Register	TRDPMR_0	358
00186h	Timer RD_0 Function Control Register	TRDFCR_0	359
00187h	Timer RD_0 Output Master Enable Register 1	TRDOER1_0	361
00188h	Timer RD_0 Output Master Enable Register 2	TRDOER2_0	362
00189h	Timer RD_0 Output Control Register	TRDOCR_0	362
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00190h	Timer RD_0 Control Register 0	TRDCR0_0	365
00191h	Timer RD_0 I/O Control Register A0	TRDIORA0_0	368
00192h	Timer RD_0 I/O Control Register C0	TRDIORC0_0	370
00193h	Timer RD_0 Status Register 0	TRDSR0_0	372
00194h	Timer RD_0 Interrupt Enable Register 0	TRDIER0_0	374
00195h	Timer RD_0 PWM Mode Output Level Control Register 0	TRDPOCR0_0	374
00196h	Timer RD_0 Counter 0	TRD0_0	375
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00198h	Timer RD_0 General Register A0	TRDGRA0_0	376
00199h			
0019Ah	Timer RD_0 General Register B0	TRDGRB0_0	376
0019Bh			
0019Ch	Timer RD_0 General Register C0	TRDGRC0_0	376
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0019Eh	Timer RD_0 General Register D0	TRDGRD0_0	376
0019Fh			
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001A1h	Timer RD_0 I/O Control Register A1	TRDIORA1_0	368
001A2h	Timer RD_0 I/O Control Register C1	TRDIORC1_0	370
001A3h	Timer RD_0 Status Register 1	TRDSR1_0	372
001A4h	Timer RD_0 Interrupt Enable Register 1	TRDIER1_0	374
001A5h	Timer RD_0 PWM Mode Output Level Control Register 1	TRDPOCR1_0	374
001A6h	Timer RD_0 Counter 1	TRD1_0	375
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001A8h	Timer RD_0 General Register A1	TRDGRA1_0	376
001A9h			
001AAh	Timer RD_0 General Register B1	TRDGRB1_0	376
001ABh			
001ACh	Timer RD_0 General Register C1	TRDGRC1_0	376
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001AEh	Timer RD_0 General Register D1	TRDGRD1_0	376
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Note:
1. Do not access the reserved areas.

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00202h	A/D Register 1	AD1	646
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00204h	A/D Register 2	AD2	646
00205h			
00206h	A/D Register 3	AD3	646
00207h			
00208h	A/D Register 4	AD4	646
00209h			
0020Ah	A/D Register 5	AD5	646
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00210h			
00211h			
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00214h	A/D Mode Register	ADMOD	647
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00216h	A/D Control Register 0	ADCON0	649
00217h	A/D Control Register 1	ADCON1	650
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00219h			
0021Ah			
0021Bh			
0021Ch			
0021Dh			
0021Eh			
0021Fh			
00220h			
00221h			
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00223h			
00224h			
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00227h			
00228h	Comparator B Control Register 0	INTCMP	669
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00230h	External Input Enable Register 0	INTEN	157
00231h	External Input Enable Register 1	INTEN1	158
00232h	INT Input Filter Select Register 0	INTF	159
00233h	INT Input Filter Select Register 1	INTF1	159
00234h	INT Input Polarity Switch Register	INTPOL	160
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00236h	Key Input Interrupt Enable Register	KIEN	160
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00252h	Flash Memory Status Register	FST	677
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00254h	Flash Memory Control Register 0	FMR0	680
00255h	Flash Memory Control Register 1	FMR1	683
00256h	Flash Memory Control Register 2	FMR2	685
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00259h			
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00262h	Address Match Interrupt Address 0H Register	AIADR0H	161
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00264h	Address Match Interrupt Address 1L Register	AIADR1L	161
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00266h	Address Match Interrupt Address 1H Register	AIADR1H	161
00267h	Address Match Interrupt Enable 1 Register	AIEN1	161
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0026Ah			
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00271h			
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00273h			
00274h			
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00276h			
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0027Bh			
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0027Eh			
0027Fh			

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0028Ah	DTC Activation Enable Register 2	DTCEN2	194
0028Bh	DTC Activation Enable Register 3	DTCEN3	194
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0028Dh	DTC Activation Enable Register 5	DTCEN5	194
0028Eh	DTC Activation Enable Register 6	DTCEN6	194
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00291h			
00292h	CRC Control Register	CRCMR	716
00293h			
00294h	CRC Data Register	CRCD	717
00295h			
00296h	CRC Input Register	CRCIN	717
00297h			
00298h			
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002A1h	Timer RJ_1 Pin Select Register	TRJ_1SR	222
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002A4h	Timer RB2 Pin Select Register	TRBSR	223
002A5h	Timer RCCLK Pin Select Register	TRCCLKSR	224
002A6h	Timer RC_0 Pin Select Register 0	TRC_0SR0	225
002A7h	Timer RC_0 Pin Select Register 1	TRC_0SR1	226
002A8h			
002A9h	Timer RD_0 Pin Select Register 0	TRD_0SR0	227
002AAh	Timer RD_0 Pin Select Register 1	TRD_0SR1	228
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002ADh	Timer Pin Select Register	TIMSR	229
002AEh	UART0_0 Pin Select Register	U_0SR	230
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002B3h	UART2 Pin Select Register 1	U2SR1	233
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Note:
1. Do not access the reserved areas.

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002C8h	Port P1 Drive Capacity Control Register	P1DRR	238
002C9h	Port P2 Drive Capacity Control Register	P2DRR	239
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002CCh	Drive Capacity Control Register 0	DRR0	240
002CDh	Drive Capacity Control Register 1	DRR1	241
002CEh	Drive Capacity Control Register 2	DRR2	242
002CFh			
002D0h	Input Threshold Control Register 0	VLT0	243
002D1h	Input Threshold Control Register 1	VLT1	244
002D2h	Input Threshold Control Register 2	VLT2	245
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002DBh			
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002DEh			
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002E1h	Port P1 Register	PORT1	246
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002E3h	Port P1 Direction Register	PD1	247
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002E5h	Port P3 Register	PORT3	246
002E6h	Port P2 Direction Register	PD2	247
002E7h	Port P3 Direction Register	PD3	247
002E8h	Port P4 Register	PORT4	246
002E9h			
002EAh	Port P4 Direction Register	PD4	247
002EBh			
002ECh	Port P6 Register	PORT6	246
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002EEh	Port P6 Direction Register	PD6	247
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002F1h	Port P9 Register	PORT9	246
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06A03h	Event Output Destination Select Register 3	ELSELR3	184
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06A05h			
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06A09h	Event Output Destination Select Register 9	ELSELR9	184
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06C03h	Area for storing DTC transfer vector 3		198
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Note:
1. Do not access the reserved areas.

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06C41h	DTC Block Size Register 0	DTBLS0	195
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Note:

1. Do not access the reserved areas.

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06C4Ch	DTC Source Address Register 1	DTSAR1	196
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06C50h	DTC Control Register 2	DTCCR2	195
06C51h	DTC Block Size Register 2	DTBLS2	195
06C52h	DTC Transfer Count Register 2	DTCCT2	195
06C53h	DTC Transfer Count Reload Register 2	DTRLD2	196
06C54h	DTC Source Address Register 2	DTSAR2	196
06C55h			
06C56h	DTC Destination Address Register 2	DTDAR2	196
06C57h			
06C58h	DTC Control Register 3	DTCCR3	195
06C59h	DTC Block Size Register 3	DTBLS3	195
06C5Ah	DTC Transfer Count Register 3	DTCCT3	195
06C5Bh	DTC Transfer Count Reload Register 3	DTRLD3	196
06C5Ch	DTC Source Address Register 3	DTSAR3	196
06C5Dh			
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06C5Fh			
06C60h	DTC Control Register 4	DTCCR4	195
06C61h	DTC Block Size Register 4	DTBLS4	195
06C62h	DTC Transfer Count Register 4	DTCCT4	195
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06C68h	DTC Control Register 5	DTCCR5	195
06C69h	DTC Block Size Register 5	DTBLS5	195
06C6Ah	DTC Transfer Count Register 5	DTCCT5	195
06C6Bh	DTC Transfer Count Reload Register 5	DTRLD5	196
06C6Ch	DTC Source Address Register 5	DTSAR5	196
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06C6Eh	DTC Destination Address Register 5	DTDAR5	196
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06C70h	DTC Control Register 6	DTCCR6	195
06C71h	DTC Block Size Register 6	DTBLS6	195
06C72h	DTC Transfer Count Register 6	DTCCT6	195
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06C78h	DTC Control Register 7	DTCCR7	195
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06C7Bh	DTC Transfer Count Reload Register 7	DTRLD7	196
06C7Ch	DTC Source Address Register 7	DTSAR7	196
06C7Dh			
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06C80h	DTC Control Register 8	DTCCR8	195
06C81h	DTC Block Size Register 8	DTBLS8	195
06C82h	DTC Transfer Count Register 8	DTCCT8	195
06C83h	DTC Transfer Count Reload Register 8	DTRLD8	196
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06C86h	DTC Destination Address Register 8	DTDAR8	196
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06C88h	DTC Control Register 9	DTCCR9	195
06C89h	DTC Block Size Register 9	DTBLS9	195
06C8Ah	DTC Transfer Count Register 9	DTCCT9	195
06C8Bh	DTC Transfer Count Reload Register 9	DTRLD9	196
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06C93h	DTC Transfer Count Reload Register 10	DTRLD10	196
06C94h	DTC Source Address Register 10	DTSAR10	196
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06C96h	DTC Destination Address Register 10	DTDAR10	196
06C97h			
06C98h	DTC Control Register 11	DTCCR11	195
06C99h	DTC Block Size Register 11	DTBLS11	195
06C9Ah	DTC Transfer Count Register 11	DTCCT11	195
06C9Bh	DTC Transfer Count Reload Register 11	DTRLD11	196
06C9Ch	DTC Source Address Register 11	DTSAR11	196
06C9Dh			
06C9Eh	DTC Destination Address Register 11	DTDAR11	196
06C9Fh			
06CA0h	DTC Control Register 12	DTCCR12	195
06CA1h	DTC Block Size Register 12	DTBLS12	195
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06CA3h	DTC Transfer Count Reload Register 12	DTRLD12	196
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06CA8h	DTC Control Register 13	DTCCR13	195
06CA9h	DTC Block Size Register 13	DTBLS13	195
06CAAh	DTC Transfer Count Register 13	DTCCT13	195
06CABh	DTC Transfer Count Reload Register 13	DTRLD13	196
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06CAEh	DTC Destination Address Register 13	DTDAR13	196
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06CB3h	DTC Transfer Count Reload Register 14	DTRLD14	196
06CB4h	DTC Source Address Register 14	DTSAR14	196
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06CB8h	DTC Control Register 15	DTCCR15	195
06CB9h	DTC Block Size Register 15	DTBLS15	195
06CBAh	DTC Transfer Count Register 15	DTCCT15	195
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06CC8h	DTC Control Register 17	DTCCR17	195
06CC9h	DTC Block Size Register 17	DTBLS17	195
06CCAh	DTC Transfer Count Register 17	DTCCT17	195
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Note:
1. Do not access the reserved areas.

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06CD3h	DTC Transfer Count Reload Register 18	DTRLD18	196
06CD4h	DTC Source Address Register 18	DTSAR18	196
06CD5h			
06CD6h	DTC Destination Address Register 18	DTDAR18	196
06CD7h			
06CD8h	DTC Control Register 19	DTCCR19	195
06CD9h	DTC Block Size Register 19	DTBLS19	195
06CDAh	DTC Transfer Count Register 19	DTCCT19	195
06CDBh	DTC Transfer Count Reload Register 19	DTRLD19	196
06CDCh	DTC Source Address Register 19	DTSAR19	196
06CDDh			
06CDEh	DTC Destination Address Register 19	DTDAR19	196
06CDFh			
06CE0h	DTC Control Register 20	DTCCR20	195
06CE1h	DTC Block Size Register 20	DTBLS20	195
06CE2h	DTC Transfer Count Register 20	DTCCT20	195
06CE3h	DTC Transfer Count Reload Register 20	DTRLD20	196
06CE4h	DTC Source Address Register 20	DTSAR20	196
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06CE6h	DTC Destination Address Register 20	DTDAR20	196
06CE7h			
06CE8h	DTC Control Register 21	DTCCR21	195
06CE9h	DTC Block Size Register 21	DTBLS21	195
06CEAh	DTC Transfer Count Register 21	DTCCT21	195
06CEBh	DTC Transfer Count Reload Register 21	DTRLD21	196
06CECh	DTC Source Address Register 21	DTSAR21	196
06CEDh			
06CEEh	DTC Destination Address Register 21	DTDAR21	196
06CEFh			
06CF0h	DTC Control Register 22	DTCCR22	195
06CF1h	DTC Block Size Register 22	DTBLS22	195
06CF2h	DTC Transfer Count Register 22	DTCCT22	195
06CF3h	DTC Transfer Count Reload Register 22	DTRLD22	196
06CF4h	DTC Source Address Register 22	DTSAR22	196
06CF5h			
06CF6h	DTC Destination Address Register 22	DTDAR22	196
06CF7h			
06CF8h	DTC Control Register 23	DTCCR23	195
06CF9h	DTC Block Size Register 23	DTBLS23	195
06CFAh	DTC Transfer Count Register 23	DTCCT23	195
06CFBh	DTC Transfer Count Reload Register 23	DTRLD23	196
06CFCh	DTC Source Address Register 23	DTSAR23	196
06CFDh			
06CFEh	DTC Destination Address Register 23	DTDAR23	196
06CFFh			
06D00h to 06DFFh			
06E00h	CAN_0 Mailbox 0	CMB0_0	583
06E01h			
06E02h			
06E03h			
06E04h			
06E05h			
06E06h			
06E07h			
06E08h			
06E09h			
06E0Ah			
06E0Bh			
06E0Ch			
06E0Dh			
06E0Eh			
06E0Fh			

Address	Register Name	Symbol	Page
06E10h	CAN_0 Mailbox 1	CMB1_0	583
06E11h			
06E12h			
06E13h			
06E14h			
06E15h			
06E16h			
06E17h			
06E18h			
06E19h			
06E1Ah			
06E1Bh			
06E1Ch			
06E1Dh			
06E1Eh			
06E1Fh			
06E20h	CAN_0 Mailbox 2	CMB2_0	583
06E21h			
06E22h			
06E23h			
06E24h			
06E25h			
06E26h			
06E27h			
06E28h			
06E29h			
06E2Ah			
06E2Bh			
06E2Ch			
06E2Dh			
06E2Eh			
06E2Fh			
06E30h	CAN_0 Mailbox 3	CMB3_0	583
06E31h			
06E32h			
06E33h			
06E34h			
06E35h			
06E36h			
06E37h			
06E38h			
06E39h			
06E3Ah			
06E3Bh			
06E3Ch			
06E3Dh			
06E3Eh			
06E3Fh			
06E40h	CAN_0 Mailbox 4	CMB4_0	583
06E41h			
06E42h			
06E43h			
06E44h			
06E45h			
06E46h			
06E47h			
06E48h			
06E49h			
06E4Ah			
06E4Bh			
06E4Ch			
06E4Dh			
06E4Eh			
06E4Fh			

Address	Register Name	Symbol	Page
06E50h	CAN_0 Mailbox 5	CMB5_0	583
06E51h			
06E52h			
06E53h			
06E54h			
06E55h			
06E56h			
06E57h			
06E58h			
06E59h			
06E5Ah			
06E5Bh			
06E5Ch			
06E5Dh			
06E5Eh			
06E5Fh			
06E60h	CAN_0 Mailbox 6	CMB6_0	583
06E61h			
06E62h			
06E63h			
06E64h			
06E65h			
06E66h			
06E67h			
06E68h			
06E69h			
06E6Ah			
06E6Bh			
06E6Ch			
06E6Dh			
06E6Eh			
06E6Fh			
06E70h	CAN_0 Mailbox 7	CMB7_0	583
06E71h			
06E72h			
06E73h			
06E74h			
06E75h			
06E76h			
06E77h			
06E78h			
06E79h			
06E7Ah			
06E7Bh			
06E7Ch			
06E7Dh			
06E7Eh			
06E7Fh			
06E80h	CAN_0 Mailbox 8	CMB8_0	583
06E81h			
06E82h			
06E83h			
06E84h			
06E85h			
06E86h			
06E87h			
06E88h			
06E89h			
06E8Ah			
06E8Bh			
06E8Ch			
06E8Dh			
06E8Eh			
06E8Fh			

Note:
1. Do not access the reserved areas.

Address	Register Name	Symbol	Page
06E90h	CAN_0 Mailbox 9	CMB9_0	583
06E91h			
06E92h			
06E93h			
06E94h			
06E95h			
06E96h			
06E97h			
06E98h			
06E99h			
06E9Ah			
06E9Bh			
06E9Ch			
06E9Dh			
06E9Eh			
06E9Fh			
06EA0h	CAN_0 Mailbox 10	CMB10_0	583
06EA1h			
06EA2h			
06EA3h			
06EA4h			
06EA5h			
06EA6h			
06EA7h			
06EA8h			
06EA9h			
06EAAh			
06EABh			
06EACh			
06EADh			
06EAEh			
06EAFh			
06EB0h	CAN_0 Mailbox 11	CMB11_0	583
06EB1h			
06EB2h			
06EB3h			
06EB4h			
06EB5h			
06EB6h			
06EB7h			
06EB8h			
06EB9h			
06EBAh			
06EBBh			
06EBCh			
06EBDh			
06EBEh			
06EBFh			
06EC0h	CAN_0 Mailbox 12	CMB12_0	583
06EC1h			
06EC2h			
06EC3h			
06EC4h			
06EC5h			
06EC6h			
06EC7h			
06EC8h			
06EC9h			
06ECAh			
06ECBh			
06ECCh			
06ECDh			
06ECEh			
06ECFh			

Address	Register Name	Symbol	Page
06ED0h	CAN_0 Mailbox 13	CMB13_0	583
06ED1h			
06ED2h			
06ED3h			
06ED4h			
06ED5h			
06ED6h			
06ED7h			
06ED8h			
06ED9h			
06EDAh			
06EDBh			
06EDCh			
06EDDh			
06EDEh			
06EDFh			
06EE0h	CAN_0 Mailbox 14	CMB14_0	583
06EE1h			
06EE2h			
06EE3h			
06EE4h			
06EE5h			
06EE6h			
06EE7h			
06EE8h			
06EE9h			
06EEAh			
06EEBh			
06EECh			
06EEDh			
06EEEh			
06EEFh			
06EF0h	CAN_0 Mailbox 15	CMB15_0	583
06EF1h			
06EF2h			
06EF3h			
06EF4h			
06EF5h			
06EF6h			
06EF7h			
06EF8h			
06EF9h			
06EFAh			
06EFBh			
06EFCh			
06EFDh			
06EFEh			
06EFFh			
06F00h			
06F01h			
06F02h			
06F03h			
06F04h			
06F05h			
06F06h			
06F07h			
06F08h			
06F09h			
06F0Ah			
06F0Bh			
06F0Ch			
06F0Dh			
06F0Eh			
06F0Fh			

Note:
1. Do not access the reserved areas.

Address	Register Name	Symbol	Page
06F10h	CAN_0 Mask Register 0	CMKR0_0	587
06F11h			
06F12h			
06F13h			
06F14h	CAN_0 Mask Register 1	CMKR1_0	587
06F15h			
06F16h			
06F17h			
06F18h	CAN_0 Mask Register 2	CMKR2_0	587
06F19h			
06F1Ah			
06F1Bh			
06F1Ch	CAN_0 Mask Register 3	CMKR3_0	587
06F1Dh			
06F1Eh			
06F1Fh			
06F20h	CAN_0 FIFO Received ID Compare Register 0	CFIDCR0_0	588
06F21h			
06F22h			
06F23h			
06F24h	CAN_0 FIFO Received ID Compare Register 1	CFIDCR1_0	588
06F25h			
06F26h			
06F27h			
06F28h			
06F29h			
06F2Ah	CAN_0 Mask Invalid Register	CMKIVLR_0	589
06F2Bh			
06F2Ch			
06F2Dh			
06F2Eh	CAN_0 Mailbox Interrupt Enable Register	CMIER_0	590
06F2Fh			
06F30h	CAN_0 Message Control Register 0	CMCTL0_0	591
06F31h	CAN_0 Message Control Register 1	CMCTL1_0	591
06F32h	CAN_0 Message Control Register 2	CMCTL2_0	591
06F33h	CAN_0 Message Control Register 3	CMCTL3_0	591
06F34h	CAN_0 Message Control Register 4	CMCTL4_0	591
06F35h	CAN_0 Message Control Register 5	CMCTL5_0	591
06F36h	CAN_0 Message Control Register 6	CMCTL6_0	591
06F37h	CAN_0 Message Control Register 7	CMCTL7_0	591
06F38h	CAN_0 Message Control Register 8	CMCTL8_0	591
06F39h	CAN_0 Message Control Register 9	CMCTL9_0	591
06F3Ah	CAN_0 Message Control Register 10	CMCTL10_0	591
06F3Bh	CAN_0 Message Control Register 11	CMCTL11_0	591
06F3Ch	CAN_0 Message Control Register 12	CMCTL12_0	591
06F3Dh	CAN_0 Message Control Register 13	CMCTL13_0	591
06F3Eh	CAN_0 Message Control Register 14	CMCTL14_0	591
06F3Fh	CAN_0 Message Control Register 15	CMCTL15_0	591
06F40h	CAN_0 Control Register	CCTLR_0	595
06F41h			
06F42h	CAN_0 Status Register	CSTR_0	600
06F43h			
06F44h	CAN_0 Bit Configuration Register	CBCR_0	603
06F45h			
06F46h			
06F47h	CAN_0 Clock Select Register	CCLKR_0	604
06F48h	CAN_0 Receive FIFO Control Register	CRFCR_0	605
06F49h	CAN_0 Receive FIFO Pointer Control Register	CRFPCR_0	607
06F4Ah	CAN_0 Transmit FIFO Control Register	CTFCR_0	608
06F4Bh	CAN_0 Transmit FIFO Pointer Control Register	CTFPCR_0	609
06F4Ch	CAN_0 Error Interrupt Enable Register	CEIER_0	610
06F4Dh	CAN_0 Error Interrupt Factor Judge Register	CEIFR_0	612
06F4Eh	CAN_0 Receive Error Count Register	CRECR_0	614
06F4Fh	CAN_0 Transmit Error Count Register	CTECR_0	614

Note:
1. Do not access the reserved areas.

Address	Register Name	Symbol	Page
06F50h	CAN_0 Error Code Store Register	CECSR_0	615
06F51h	CAN_0 Channel Search Support Register	CCSSR_0	616
06F52h	CAN_0 Mailbox Search Status Register	CMSSR_0	617
06F53h	CAN_0 Mailbox Search Mode Register	CMSMR_0	618
06F54h	CAN_0 Time Stamp Register	CTSR_0	619
06F55h			
06F56h	CAN_0 Acceptance Filter Support Register	CAFSR_0	620
06F57h			
06F58h	CAN_0 Test Control Register	CTCR_0	621
06F59h			
06F5Ah			
06F5Bh			
06F5Ch			
06F5Dh			
06F5Eh			
06F5Fh			
06F60h			
06F61h			
06F62h			
06F63h			
06F64h			
06F65h			
06F66h			
06F67h			
06F68h			
06F69h			
06F6Ah			
06F6Bh			
06F6Ch			
06F6Dh			
06F6Eh			
06F6Fh			
06F70h			
06F71h			
06F72h			
06F73h			
06F74h			
06F75h			
06F76h			
06F77h			
06F78h			
06F79h			
06F7Ah			
06F7Bh			
06F7Ch			
06F7Dh			
06F7Eh	CAN_0 Interrupt Status Register	CANISR_0	623
06F7Fh	CAN_0 Interrupt Control Register	CANIE_0	623
06F80h to 06FFFh			

:

0FFDBh	Option Function Select Register 2	OFS2	58, 68, 100

:

0FFFFh	Option Function Select Register	OFS	59, 69, 87, 101, 687

1. Overview

1.1 Features

The R8C/54E Group, R8C/54F Group, R8C/54G Group, R8C/54H Group of single-chip microcontrollers (MCUs) incorporate the R8C CPU core, which provides sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, the CPU core is capable of executing instructions at high speed. In addition, it features a multiplier for high-speed arithmetic processing.
Power consumption is low, and additional power control is possible by selecting the operating mode. The R8C/54E Group, R8C/54F Group, R8C/54G Group, R8C/54H Group are also designed to maximize EMI/EMS performance. Integration of many peripheral functions, including multifunction timer and serial interface on the same chip, reduces the number of system components.
The R8C/54E Group and R8C/54F Group incorporate one channel of CAN module, ideal for the LAN systems of automotive and factory automation applications.
The R8C/54G Group and R8C/54H Group do not incorporate the CAN module.
The R8C/54E Group and R8C/54G Group also have on-chip data flash (1 KB × 4 blocks) with background operation (BGO) function.

1.1.1 Applications

Automotive, etc.

1.1.2 Specifications

Tables 1.1 and 1.2 outline the R8C/54E Group Specifications. Tables 1.3 and 1.4 outline the R8C/54F Group Specifications. Tables 1.5 and 1.6 outline the R8C/54G Group Specifications. Tables 1.7 and 1.8 outline the R8C/54H Group Specifications.

Table 1.1 R8C/54E Group Specifications (1)

Item	Function	Description
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 31.25 ns (CPU clock = 32 MHz, VCC = 2.7 V to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, data flash	Refer to **Table 1.9 R8C/54E Group Product List**.
Voltage detection	Voltage detection circuit	• Power-on reset • Voltage detection with three check points (the detection levels for voltage detection 0 and voltage detection 1 can be selected.)
I/O ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 43, selectable pull-up resistor • Peripheral mapping controller (PMC) allows communication function priority pin assignment selection.
Clock	Clock generation circuits	• 4 circuits: XIN clock oscillation circuit, high-speed on-chip oscillator (with frequency adjustment function), low-speed on-chip oscillator, PLL frequency synthesizer (up to 32 MHz), multiplied by 2, 4, 6, or 8 • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Divided by 1, 2, 4, 8, or 16 can be selected • Low-power mode: Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator, PLL operating), wait mode, stop mode
Interrupts		• Number of interrupt vectors: 69 • External interrupt inputs: 9 (INT × 5, key input × 4) • Priority levels: 7
Event link controller (ELC)		• Events output from peripheral functions can be linked to events input to different peripheral functions. (22 sources × 7 types of event link operations) • Events can be handled independently from interrupt requests.
Watchdog timer		• 14 bits × 1 (with prescaler) • Selectable reset start function • Selectable low-speed on-chip oscillator for the watchdog timer
DTC (data transfer controller)		• 1 channel • Activation sources: 36 • Transfer modes: 2 (normal mode, repeat mode)

Table 1.2 R8C/54E Group Specifications (2)

Item	Function	Description
Timer	Timers RJ_0 and RJ_1	16 bits × 1: 2 circuits integrated on-chip Timer mode (periodic timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timers RB2_0	16 bits × 1: 1 circuit integrated on-chip Timer mode (periodic timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timers RC_0	16 bits (with 4 capture/compare registers) × 1: 1 circuit integrated on-chip Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin)
	Timers RD_0	16 bits (with 4 capture/compare registers) × 2: 1 circuit integrated on-chip Timer mode (input capture function, output compare function), PWM mode (output: 6 pins), reset synchronous PWM mode (three-phase waveform output (6 pins), sawtooth wave modulation), complementary PWM mode (three-phase waveform output (6 pins), triangular wave modulation), PWM3 mode (PWM output with fixed period: 2 pins)
	Timer RE2	8 bits × 1 Compare match timer mode
Serial interface	UART0_0 and UART0_1	2 channels Clock synchronous serial I/O mode, clock asynchronous serial I/O mode
	UART2	1 channel Clock synchronous serial I/O mode, clock asynchronous serial I/O mode, special mode 3 (IE mode), multiprocessor communication mode
Clock Synchronous serial interface	(SSU) SSU_0 and SSU_1	2 channels (also used for the I^2C bus) (2 channels can be used only for communication function priority pin assignment (only 1 channel for others))
	(I^2C bus) I^2C_0 and I^2C_1	2 channels (also used for the SSU) (2 channels can be used only for communication function priority pin assignment (only 1 channel for others))
LIN module	HW-LIN_0 and HW-LIN_1	Hardware LIN 2 channels (timer RJ_0, RJ_1, UART0_0, or UART0_1 used)
CAN module	CAN_0	1 channel: 16 mailboxes (ISO11898-1 standard compliant)
A/D converter		Resolution: 10 bits × 12 channels, sample and hold function, sweep mode
Comparator B		2 circuits
CRC calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash memory		• Program/erase voltage: VCC = 2.7 V to 5.5 V • Read voltage: VCC = 2.7 V to 5.5 V • Program/erase endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • BGO (background operation) function (data flash)
Debug functions		• 1-wire debug interface provided (dedicated hardware provided) • Hot plug connection is supported, allowing the debugger interface to be connected during user mode operation.
Operating frequency/ Power supply voltage		CPU clock = 32 MHz (VCC = 2.7 V to 5.5 V)
Current consumption		Typ. 14 mA (VCC = 5.0 V, f(CPU) = 32 MHz)
Operating ambient temperature		-40°C to 85°C (J version) -40°C to 125°C (K version) (1)
Package		48-pin LQFP Package code: PLQP0048KB-A (previous code: 48P6Q-A)

Note:
1. Specify the K version if it is to be used.

Table 1.3 R8C/54F Group Specifications (1)

Item	Function	Description
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 31.25 ns (CPU clock = 32 MHz, VCC = 2.7 V to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM	Refer to **Table 1.10 R8C/54F Group Product List**.
Voltage detection	Voltage detection circuit	• Power-on reset • Voltage detection with three check points (the detection levels for voltage detection 0 and voltage detection 1 can be selected.)
I/O ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 43, selectable pull-up resistor • Peripheral mapping controller (PMC) allows communication function priority pin assignment selection.
Clock	Clock generation circuits	• 4 circuits: XIN clock oscillation circuit, high-speed on-chip oscillator (with frequency adjustment function), low-speed on-chip oscillator, PLL frequency synthesizer (up to 32 MHz), multiplied by 2, 4, 6, or 8 • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Divided by 1, 2, 4, 8, or 16 can be selected • Low-power mode: Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator, PLL operating), wait mode, stop mode
Interrupts		• Number of interrupt vectors: 69 • External interrupt inputs: 9 (INT × 5, key input × 4) • Priority levels: 7
Event link controller (ELC)		• Events output from peripheral functions can be linked to events input to different peripheral functions. (22 sources × 7 types of event link operations) • Events can be handled independently from interrupt requests.
Watchdog timer		• 14 bits × 1 (with prescaler) • Selectable reset start function • Selectable low-speed on-chip oscillator for the watchdog timer
DTC (data transfer controller)		• 1 channel • Activation sources: 36 • Transfer modes: 2 (normal mode, repeat mode)

Table 1.4 R8C/54F Group Specifications (2)

Item	Function	Description
Timer	Timers RJ_0 and RJ_1	16 bits × 1: 2 circuits integrated on-chip Timer mode (periodic timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timers RB2_0	16 bits × 1: 1 circuit integrated on-chip Timer mode (periodic timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timers RC_0	16 bits (with 4 capture/compare registers) × 1: 1 circuit integrated on-chip Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin)
	Timers RD_0	16 bits (with 4 capture/compare registers) × 2: 1 circuit integrated on-chip Timer mode (input capture function, output compare function), PWM mode (output: 6 pins), reset synchronous PWM mode (three-phase waveform output (6 pins), sawtooth wave modulation), complementary PWM mode (three-phase waveform output (6 pins), triangular wave modulation), PWM3 mode (PWM output with fixed period: 2 pins)
	Timer RE2	8 bits × 1 Compare match timer mode
Serial interface	UART0_0 and UART0_1	2 channels Clock synchronous serial I/O mode, clock asynchronous serial I/O mode
	UART2	1 channel Clock synchronous serial I/O mode, clock asynchronous serial I/O mode, special mode 3 (IE mode), multiprocessor communication mode
Clock Synchronous serial interface	(SSU) SSU_0 and SSU_1	2 channels (also used for the I^2C bus) (2 channels can be used only for communication function priority pin assignment (only 1 channel for others))
	(I^2C bus) I^2C_0 and I^2C_1	2 channels (also used for the SSU) (2 channels can be used only for communication function priority pin assignment (only 1 channel for others))
LIN module	HW-LIN_0 and HW-LIN_1	Hardware LIN 2 channels (timer RJ_0, RJ_1, UART0_0, or UART0_1 used)
CAN module	CAN_0	1 channel: 16 mailboxes (ISO11898-1 standard compliant)
A/D converter		Resolution: 10 bits × 12 channels, sample and hold function, sweep mode
Comparator B		2 circuits
CRC calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash memory		• Program/erase voltage: VCC = 2.7 V to 5.5 V • Read voltage: VCC = 2.7 V to 5.5 V • Program/erase endurance: 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Debug functions		• 1-wire debug interface provided (dedicated hardware provided) • Hot plug connection is supported, allowing the debugger interface to be connected during user mode operation.
Operating frequency/ Power supply voltage		CPU clock = 32 MHz (VCC = 2.7 V to 5.5 V)
Current consumption		Typ. 14 mA (VCC = 5.0 V, f(CPU) = 32 MHz)
Operating ambient temperature		-40°C to 85°C (J version) -40°C to 125°C (K version) (1)
Package		48-pin LQFP Package code: PLQP0048KB-A (previous code: 48P6Q-A)

Note:
1. Specify the K version if it is to be used.

Table 1.5 R8C/54G Group Specifications (1)

Item	Function	Description
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 31.25 ns (CPU clock = 32 MHz, VCC = 2.7 V to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, data flash	Refer to **Table 1.11 R8C/54G Group Product List**.
Voltage detection	Voltage detection circuit	• Power-on reset • Voltage detection with three check points (the detection levels for voltage detection 0 and voltage detection 1 can be selected.)
I/O ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 43, selectable pull-up resistor • Peripheral mapping controller (PMC) allows communication function priority pin assignment selection.
Clock	Clock generation circuits	• 4 circuits: XIN clock oscillation circuit, high-speed on-chip oscillator (with frequency adjustment function), low-speed on-chip oscillator, PLL frequency synthesizer (up to 32 MHz), multiplied by 2, 4, 6, or 8 • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Divided by 1, 2, 4, 8, or 16 can be selected • Low-power mode: Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator, PLL operating), wait mode, stop mode
Interrupts		• Number of interrupt vectors: 69 • External interrupt inputs: 9 (INT × 5, key input × 4) • Priority levels: 7
Event link controller (ELC)		• Events output from peripheral functions can be linked to events input to different peripheral functions. (22 sources × 7 types of event link operations) • Events can be handled independently from interrupt requests.
Watchdog timer		• 14 bits × 1 (with prescaler) • Selectable reset start function • Selectable low-speed on-chip oscillator for the watchdog timer
DTC (data transfer controller)		• 1 channel • Activation sources: 36 • Transfer modes: 2 (normal mode, repeat mode)

Table 1.6 R8C/54G Group Specifications (2)

Item	Function	Description
Timer	Timers RJ_0 and RJ_1	16 bits × 1: 2 circuits integrated on-chip Timer mode (periodic timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timers RB2_0	16 bits × 1: 1 circuit integrated on-chip Timer mode (periodic timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timers RC_0	16 bits (with 4 capture/compare registers) × 1: 1 circuit integrated on-chip Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin)
	Timers RD_0	16 bits (with 4 capture/compare registers) × 2: 1 circuit integrated on-chip Timer mode (input capture function, output compare function), PWM mode (output: 6 pins), reset synchronous PWM mode (three-phase waveform output (6 pins), sawtooth wave modulation), complementary PWM mode (three-phase waveform output (6 pins), triangular wave modulation), PWM3 mode (PWM output with fixed period: 2 pins)
	Timer RE2	8 bits × 1 Compare match timer mode
Serial interface	UART0_0 and UART0_1	2 channels Clock synchronous serial I/O mode, clock asynchronous serial I/O mode
	UART2	1 channel Clock synchronous serial I/O mode, clock asynchronous serial I/O mode, special mode 3 (IE mode), multiprocessor communication mode
Clock Synchronous serial interface	(SSU) SSU_0 and SSU_1	2 channels (also used for the I^2C bus) (2 channels can be used only for communication function priority pin assignment (only 1 channel for others))
	(I^2C bus) I^2C_0 and I^2C_1	2 channels (also used for the SSU) (2 channels can be used only for communication function priority pin assignment (only 1 channel for others))
LIN module	HW-LIN_0 and HW-LIN_1	Hardware LIN 2 channels (timer RJ_0, RJ_1, UART0_0, or UART0_1 used)
A/D converter		Resolution: 10 bits × 12 channels, sample and hold function, sweep mode
Comparator B		2 circuits
CRC calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash memory		• Program/erase voltage: VCC = 2.7 V to 5.5 V • Read voltage: VCC = 2.7 V to 5.5 V • Program/erase endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • BGO (background operation) function (data flash)
Debug functions		• 1-wire debug interface provided (dedicated hardware provided) • Hot plug connection is supported, allowing the debugger interface to be connected during user mode operation.
Operating frequency/ Power supply voltage		CPU clock = 32 MHz (VCC = 2.7 V to 5.5 V)
Current consumption		Typ. 14 mA (VCC = 5.0 V, f(CPU) = 32 MHz)
Operating ambient temperature		-40°C to 85°C (J version) -40°C to 125°C (K version) (1)
Package		48-pin LQFP Package code: PLQP0048KB-A (previous code: 48P6Q-A)

Note:
1. Specify the K version if it is to be used.

Table 1.7 R8C/54H Group Specifications (1)

Item	Function	Description
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 31.25 ns (CPU clock = 32 MHz, VCC = 2.7 V to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM	Refer to **Table 1.12 R8C/54H Group Product List**.
Voltage detection	Voltage detection circuit	• Power-on reset • Voltage detection with three check points (the detection levels for voltage detection 0 and voltage detection 1 can be selected.)
I/O ports	Programmable I/O ports	• Input only: 1 • CMOS I/O: 43, selectable pull-up resistor • Peripheral mapping controller (PMC) allows communication function priority pin assignment selection.
Clock	Clock generation circuits	• 4 circuits: XIN clock oscillation circuit, high-speed on-chip oscillator (with frequency adjustment function), low-speed on-chip oscillator, PLL frequency synthesizer (up to 32 MHz), multiplied by 2, 4, 6, or 8 • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Divided by 1, 2, 4, 8, or 16 can be selected • Low-power mode: Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator, PLL operating), wait mode, stop mode
Interrupts		• Number of interrupt vectors: 69 • External interrupt inputs: 9 (INT × 5, key input × 4) • Priority levels: 7
Event link controller (ELC)		• Events output from peripheral functions can be linked to events input to different peripheral functions. (22 sources × 7 types of event link operations) • Events can be handled independently from interrupt requests.
Watchdog timer		• 14 bits × 1 (with prescaler) • Selectable reset start function • Selectable low-speed on-chip oscillator for the watchdog timer
DTC (data transfer controller)		• 1 channel • Activation sources: 36 • Transfer modes: 2 (normal mode, repeat mode)

Table 1.8 R8C/54H Group Specifications (2)

Item	Function	Description
Timer	Timers RJ_0 and RJ_1	16 bits × 1: 2 circuits integrated on-chip Timer mode (periodic timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timers RB2_0	16 bits × 1: 1 circuit integrated on-chip Timer mode (periodic timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timers RC_0	16 bits (with 4 capture/compare registers) × 1: 1 circuit integrated on-chip Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin)
	Timers RD_0	16 bits (with 4 capture/compare registers) × 2: 1 circuit integrated on-chip Timer mode (input capture function, output compare function), PWM mode (output: 6 pins), reset synchronous PWM mode (three-phase waveform output (6 pins), sawtooth wave modulation), complementary PWM mode (three-phase waveform output (6 pins), triangular wave modulation), PWM3 mode (PWM output with fixed period: 2 pins)
	Timer RE2	8 bits × 1 Compare match timer mode
Serial interface	UART0_0 and UART0_1	2 channels Clock synchronous serial I/O mode, clock asynchronous serial I/O mode
	UART2	1 channel Clock synchronous serial I/O mode, clock asynchronous serial I/O mode, special mode 3 (IE mode), multiprocessor communication mode
Clock Synchronous serial interface	(SSU) SSU_0 and SSU_1	2 channels (also used for the I^2C bus) (2 channels can be used only for communication function priority pin assignment (only 1 channel for others))
	(I^2C bus) I^2C_0 and I^2C_1	2 channels (also used for the SSU) (2 channels can be used only for communication function priority pin assignment (only 1 channel for others))
LIN module	HW-LIN_0 and HW-LIN_1	Hardware LIN 2 channels (timer RJ_0, RJ_1, UART0_0, or UART0_1 used)
A/D converter		Resolution: 10 bits × 12 channels, sample and hold function, sweep mode
Comparator B		2 circuits
CRC calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash memory		• Program/erase voltage: VCC = 2.7 V to 5.5 V • Read voltage: VCC = 2.7 V to 5.5 V • Program/erase endurance: 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Debug functions		• 1-wire debug interface provided (dedicated hardware provided) • Hot plug connection is supported, allowing the debugger interface to be connected during user mode operation.
Operating frequency/ Power supply voltage		CPU clock = 32 MHz (VCC = 2.7 V to 5.5 V)
Current consumption		Typ. 14 mA (VCC = 5.0 V, f(CPU) = 32 MHz)
Operating ambient temperature		-40°C to 85°C (J version) -40°C to 125°C (K version) (1)
Package		48-pin LQFP Package code: PLQP0048KB-A (previous code: 48P6Q-A)

Note:
1. Specify the K version if it is to be used.

1.2 Product List

Table 1.9 shows the R8C/54E Group Product List. Figure 1.1 shows the R8C/54E Group Product Part Number Structure. Table 1.10 shows the R8C/54F Group Product List. Figure 1.2 shows the R8C/54F Group Product Part Number Structure. Table 1.11 shows the R8C/54G Group Product List. Figure 1.3 shows the R8C/54G Group Product Part Number Structure. Table 1.12 shows the R8C/54H Group Product List. Figure 1.4 shows the R8C/54H Group Product Part Number Structure.

Table 1.9 R8C/54E Group Product List **Current of Sep 2014**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F21546EJFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0048KB-A	J version
R5F21547EJFP	48 Kbytes		4 Kbytes		
R5F21548EJFP	64 Kbytes		6 Kbytes		
R5F2154AEJFP	96 Kbytes		8 Kbytes		
R5F2154CEJFP	128 Kbytes		10 Kbytes		
R5F21546EKFP	32 Kbytes		2.5 Kbytes		K version
R5F21547EKFP	48 Kbytes		4 Kbytes		
R5F21548EKFP	64 Kbytes		6 Kbytes		
R5F2154AEKFP	96 Kbytes		8 Kbytes		
R5F2154CEKFP	128 Kbytes		10 Kbytes		

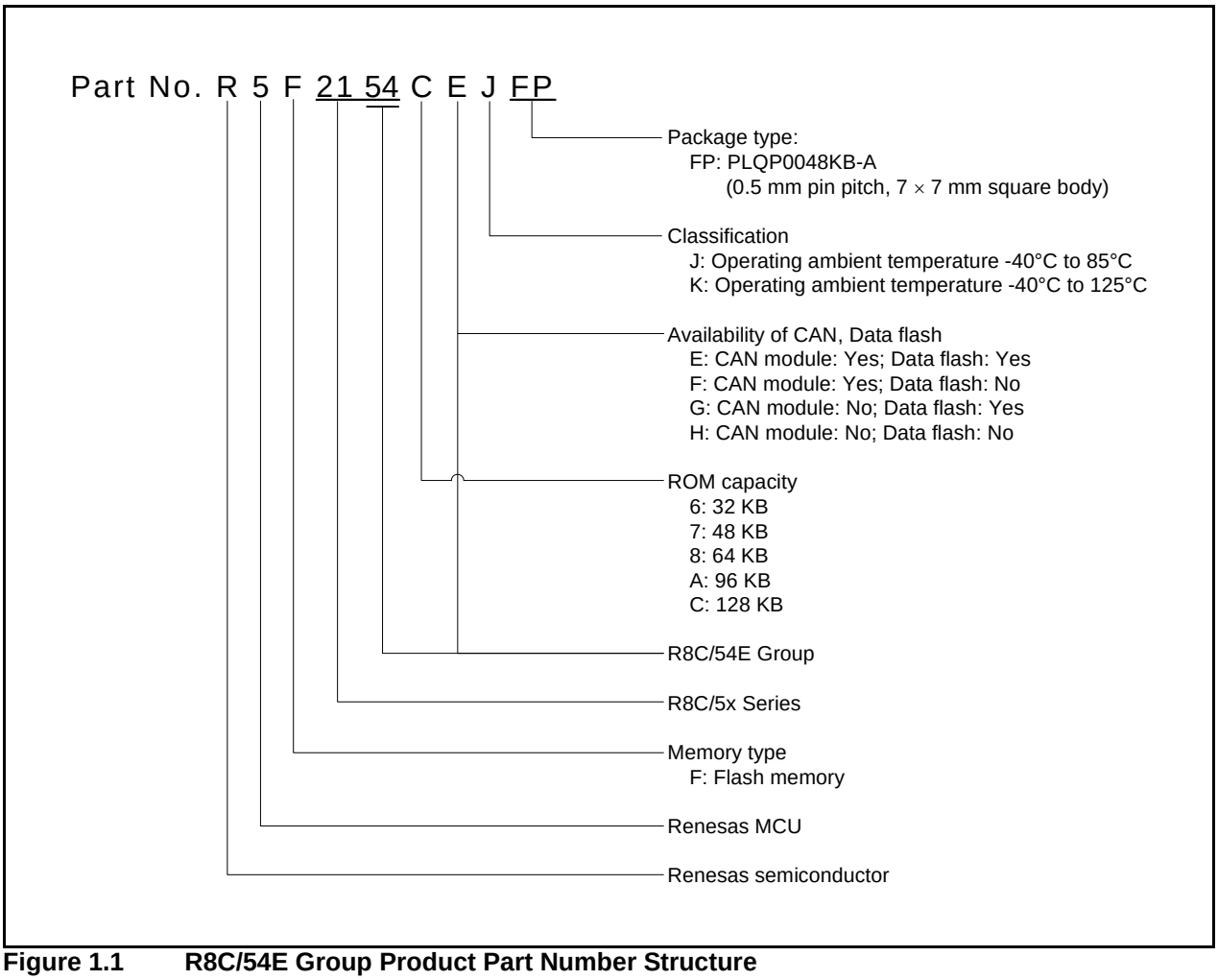


Figure 1.1 R8C/54E Group Product Part Number Structure

Table 1.10 R8C/54F Group Product List **Current of Sep 2014**

Part No.	Internal ROM Capacity Program ROM	Internal RAM Capacity	Package Type	Remarks
R5F21546FJFP	32 Kbytes	2.5 Kbytes	PLQP0048KB-A	J version
R5F21547FJFP	48 Kbytes	4 Kbytes		
R5F21548FJFP	64 Kbytes	6 Kbytes		
R5F2154AFJFP	96 Kbytes	8 Kbytes		
R5F2154CFJFP	128 Kbytes	10 Kbytes		
R5F21546FKFP	32 Kbytes	2.5 Kbytes		K version
R5F21547FKFP	48 Kbytes	4 Kbytes		
R5F21548FKFP	64 Kbytes	6 Kbytes		
R5F2154AFKFP	96 Kbytes	8 Kbytes		
R5F2154CFKFP	128 Kbytes	10 Kbytes		

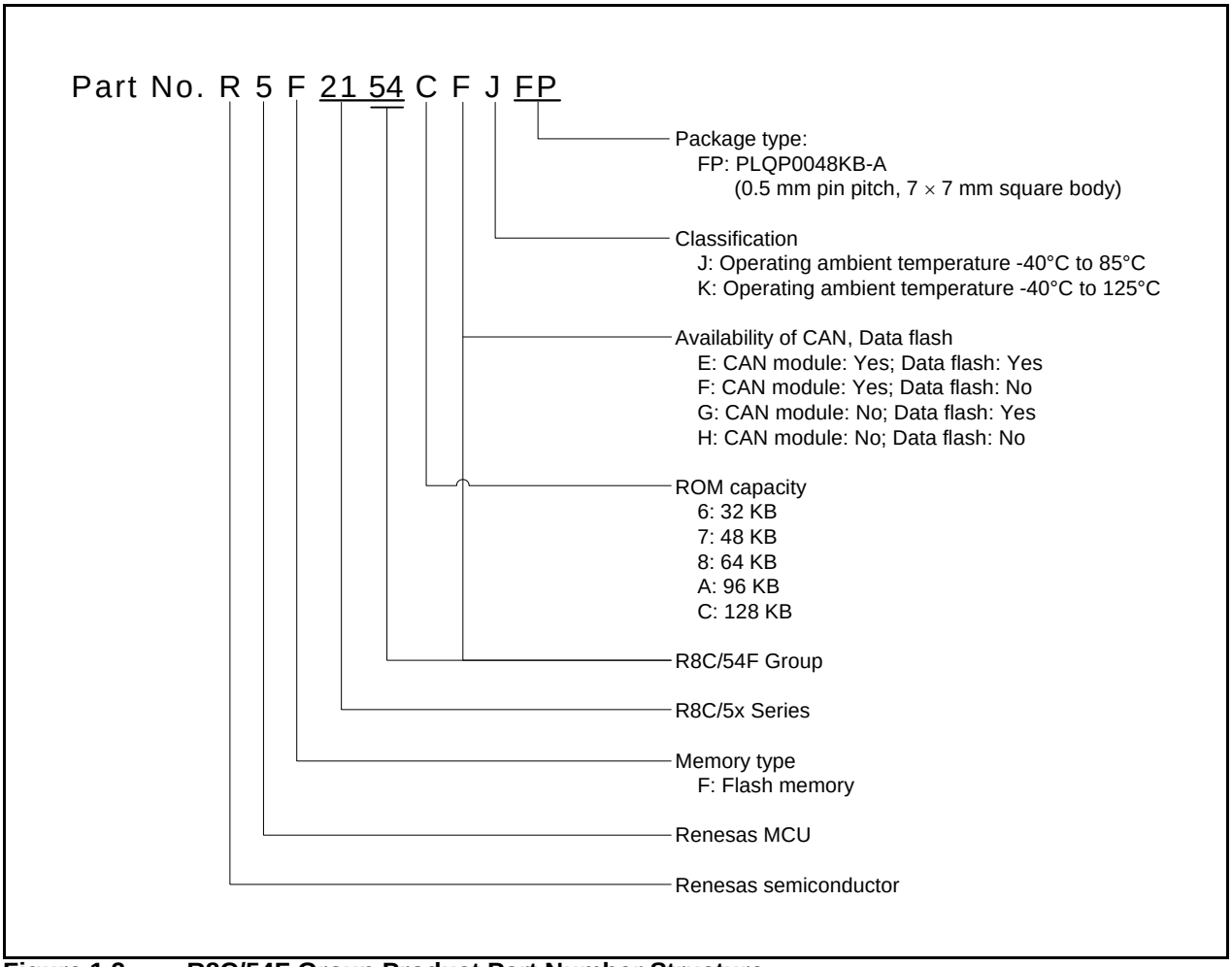


Figure 1.2 R8C/54F Group Product Part Number Structure

Table 1.11 R8C/54G Group Product List **Current of Sep 2014**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F21546GJFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0048KB-A	J version
R5F21547GJFP	48 Kbytes		4 Kbytes		
R5F21548GJFP	64 Kbytes		6 Kbytes		
R5F2154AGJFP	96 Kbytes		8 Kbytes		
R5F2154CGJFP	128 Kbytes		10 Kbytes		
R5F21546GKFP	32 Kbytes		2.5 Kbytes		K version
R5F21547GKFP	48 Kbytes		4 Kbytes		
R5F21548GKFP	64 Kbytes		6 Kbytes		
R5F2154AGKFP	96 Kbytes		8 Kbytes		
R5F2154CGKFP	128 Kbytes		10 Kbytes		

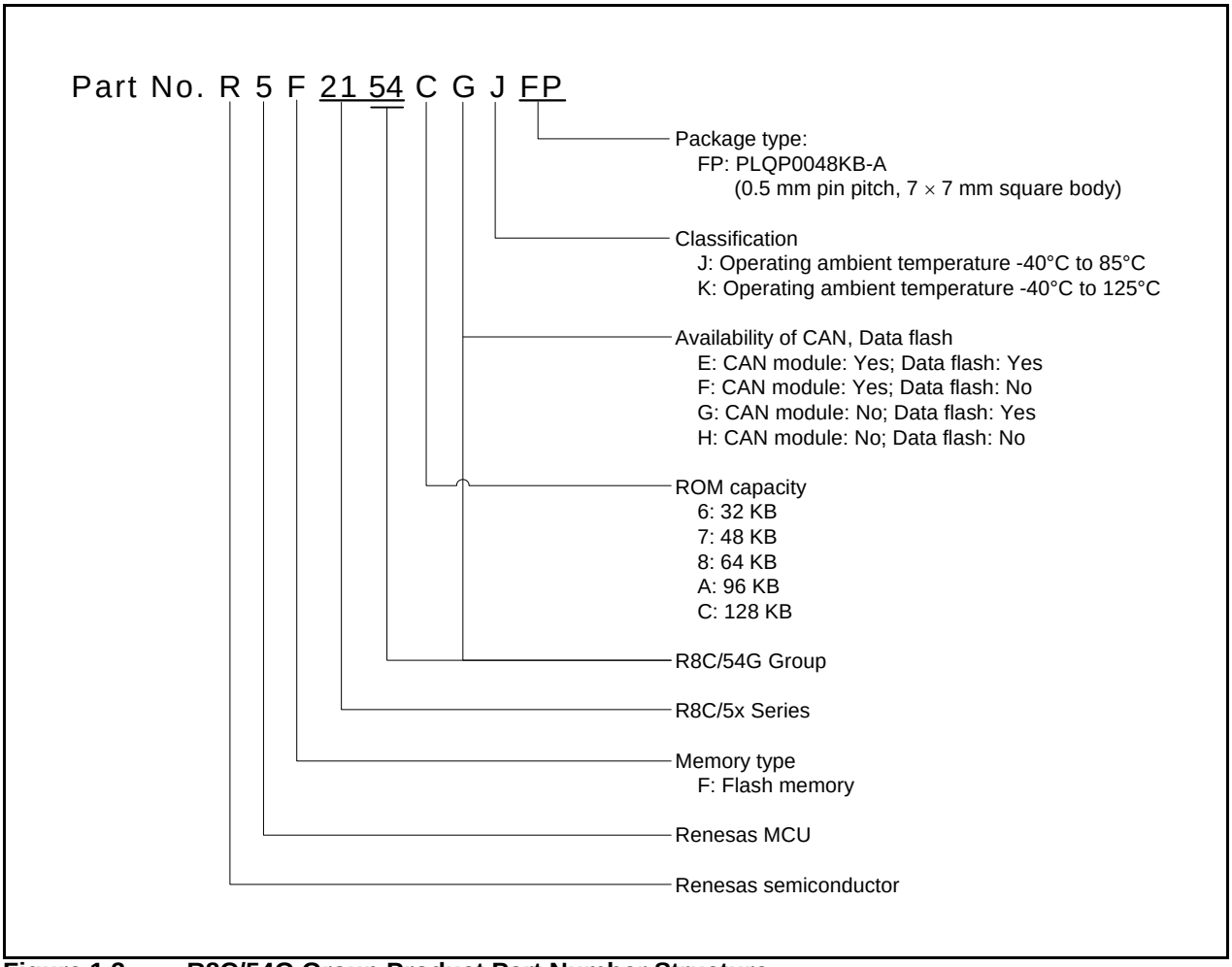


Figure 1.3 R8C/54G Group Product Part Number Structure

Table 1.12 R8C/54H Group Product List **Current of Sep 2014**

Part No.	Internal ROM Capacity Program ROM	Internal RAM Capacity	Package Type	Remarks
R5F21546HJFP	32 Kbytes	2.5 Kbytes	PLQP0048KB-A	J version
R5F21547HJFP	48 Kbytes	4 Kbytes		
R5F21548HJFP	64 Kbytes	6 Kbytes		
R5F2154AHJFP	96 Kbytes	8 Kbytes		
R5F2154CHJFP	128 Kbytes	10 Kbytes		
R5F21546HKFP	32 Kbytes	2.5 Kbytes		K version
R5F21547HKFP	48 Kbytes	4 Kbytes		
R5F21548HKFP	64 Kbytes	6 Kbytes		
R5F2154AHKFP	96 Kbytes	8 Kbytes		
R5F2154CHKFP	128 Kbytes	10 Kbytes		

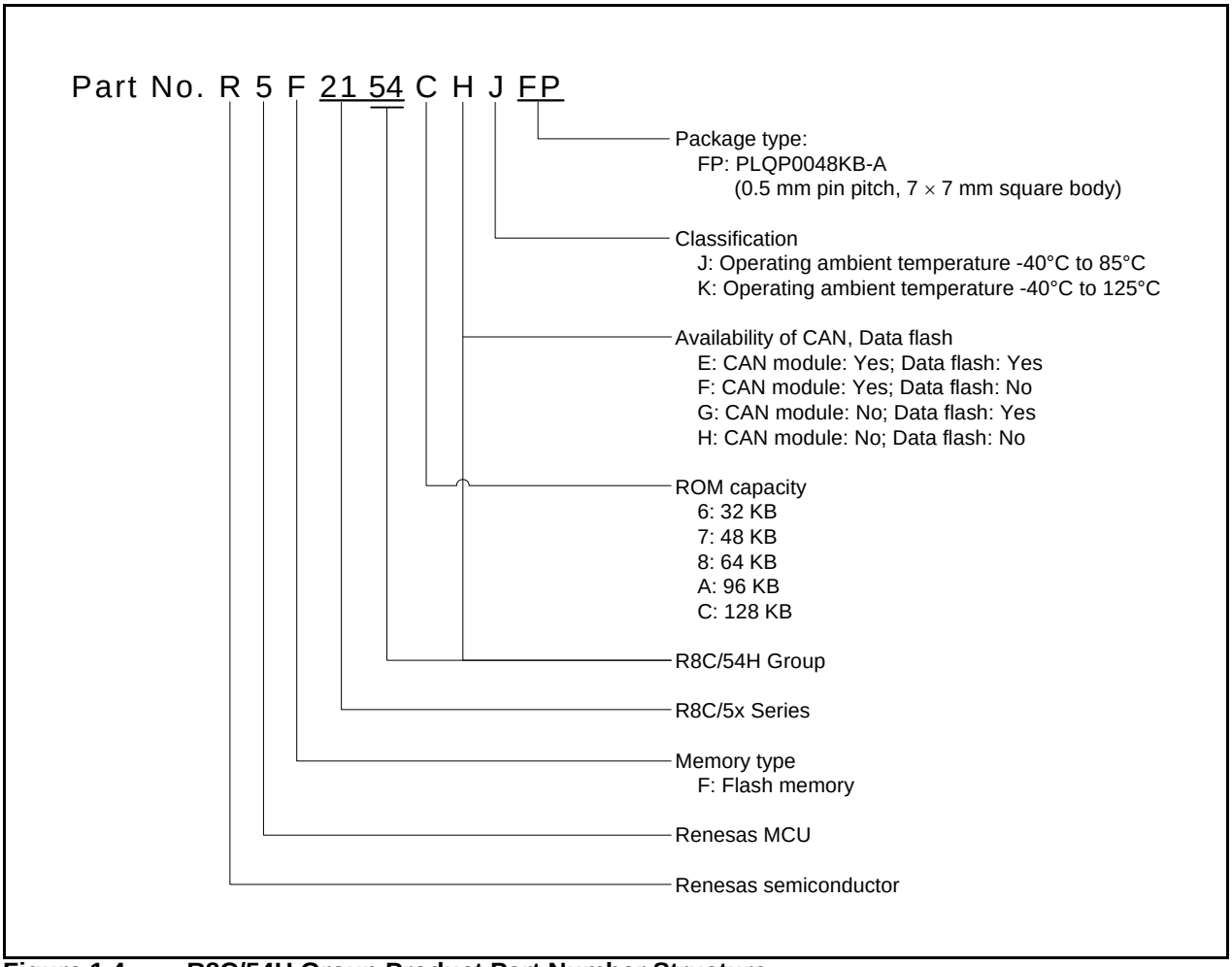
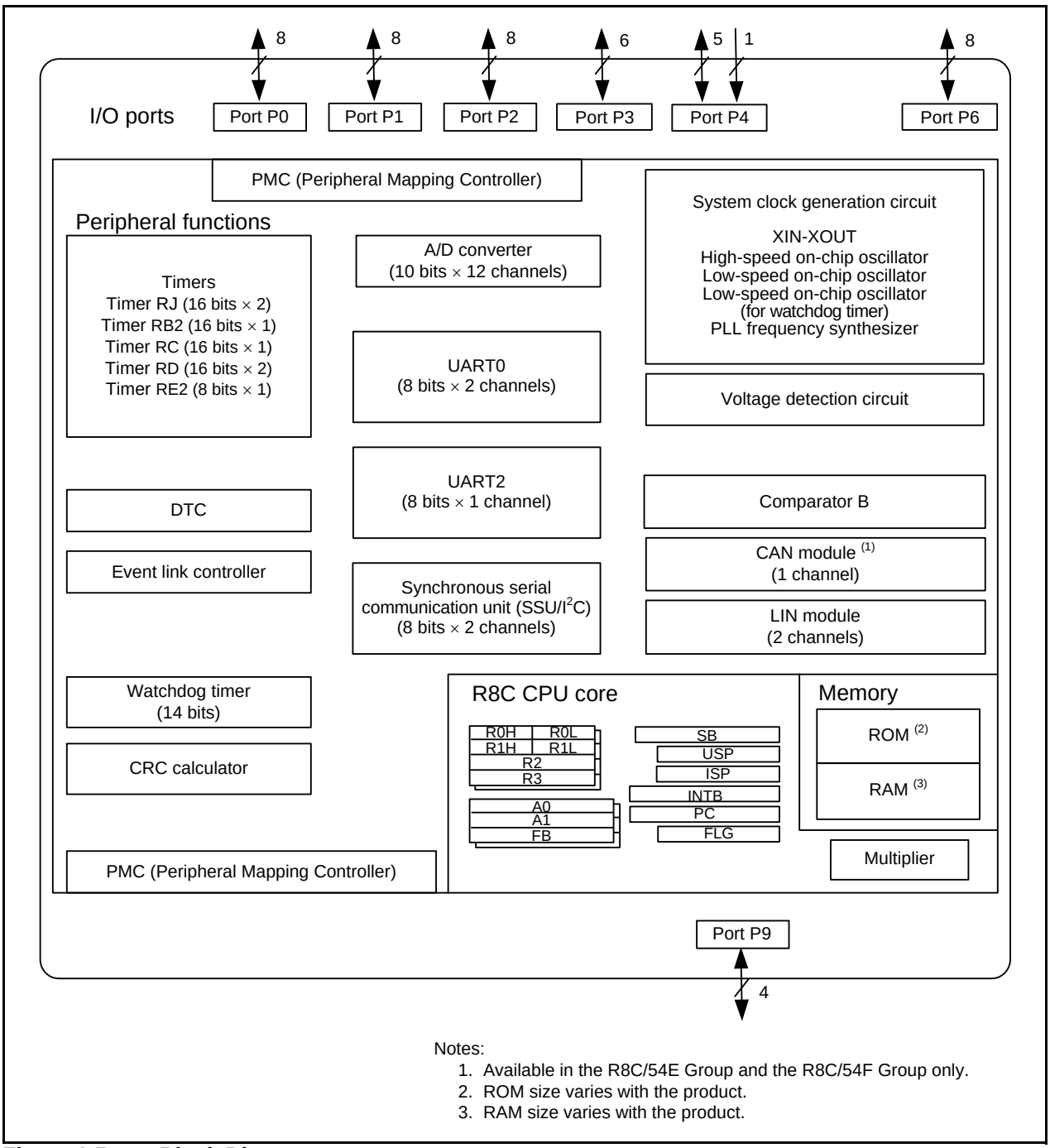


Figure 1.4 R8C/54H Group Product Part Number Structure

1.3 Block Diagram

Figure 1.5 shows the Block Diagram.

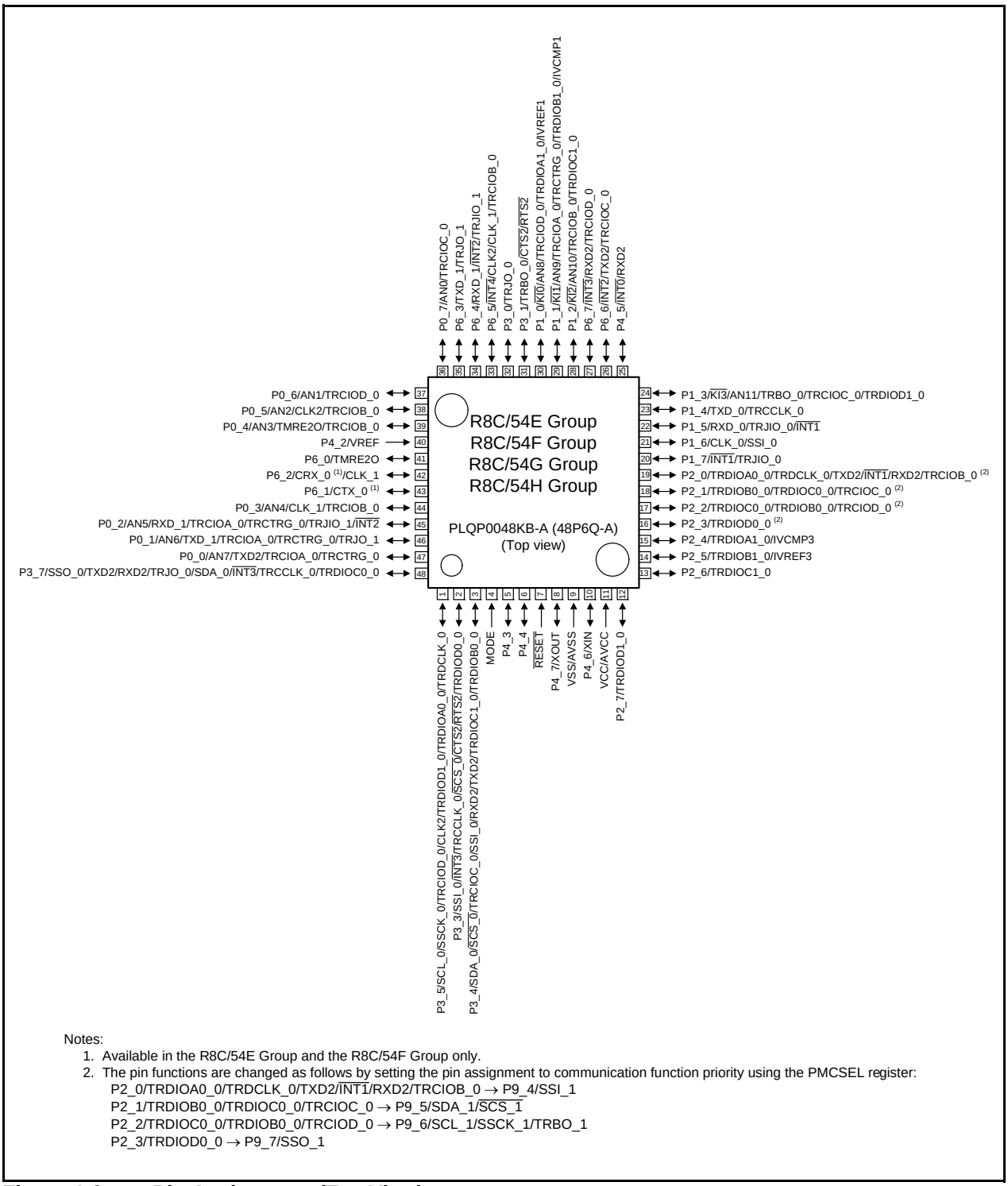


Notes:
1. Available in the R8C/54E Group and the R8C/54F Group only.
2. ROM size varies with the product.
3. RAM size varies with the product.

Figure 1.5 Block Diagram

1.4 Pin Assignment

Figure 1.6 shows Pin Assignment (Top View). Tables 1.13 to 1.17 list the Pin Name Information by Pin Number.



Notes:
1. Available in the R8C/54E Group and the R8C/54F Group only.
2. The pin functions are changed as follows by setting the pin assignment to communication function priority using the PMCSEL register:
   P2_0/TRDIOA0_0/TRDCLK_0/TXD2/INT1/RXD2/TRCIOB_0 → P9_4/SSI_1
   P2_1/TRDIOB0_0/TRDIOC0_0/TRCIOC_0 → P9_5/SDA_1/SCS_1
   P2_2/TRDIOC0_0/TRDIOB0_0/TRCIOD_0 → P9_6/SCL_1/SSCK_1/TRBO_1
   P2_3/TRDIOD0_0 → P9_7/SSO_1

Figure 1.6 Pin Assignment (Top View)

Table 1.13 Pin Name Information by Pin Number (INT, URAT0, and UART2)

Port	Pin No.	INT					UART0						UART2				
		$\overline{INT0}$	$\overline{INT1}$	$\overline{INT2}$	$\overline{INT3}$	$\overline{INT4}$	TXD_0	TXD_1	RXD_0	RXD_1	CLK_0	CLK_1	TXD2	RXD2	$\overline{CTS2}$	$\overline{RTS2}$	CLK2
P0_0	47												TXD2				
P0_1	46							TXD_1									
P0_2	45			$\overline{INT2}$						RXD_1							
P0_3	44											CLK_1					
P0_4	39																
P0_5	38																CLK2
P0_6	37																
P0_7	36																
P1_0	30																
P1_1	29																
P1_2	28																
P1_3	24																
P1_4	23						TXD_0										
P1_5	22		$\overline{INT1}$						RXD_0								
P1_6	21										CLK_0						
P1_7	20		$\overline{INT1}$														
P2_0	19 (1)		$\overline{INT1}$										TXD2	RXD2			
P2_1	18 (1)																
P2_2	17 (1)																
P2_3	16 (1)																
P2_4	15																
P2_5	14																
P2_6	13																
P2_7	12																
P3_0	32																
P3_1	31														$\overline{CTS2}$	$\overline{RTS2}$	
P3_3	2				$\overline{INT3}$										$\overline{CTS2}$	$\overline{RTS2}$	
P3_4	3												TXD2	RXD2			
P3_5	1																CLK2
P3_7	48				$\overline{INT3}$								TXD2	RXD2			
P4_2	40																
P4_3	5																
P4_4	6																
P4_5	25	$\overline{INT0}$												RXD2			
P4_6	10																
P4_7	8																
P6_0	41																
P6_1	43																
P6_2	42											CLK_1					
P6_3	35							TXD_1									
P6_4	34			$\overline{INT2}$						RXD_1							
P6_5	33					$\overline{INT4}$						CLK_1					CLK2
P6_6	26			$\overline{INT2}$									TXD2				
P6_7	27				$\overline{INT3}$									RXD2			
P9_4	19 (1)																
P9_5	18 (1)																
P9_6	17 (1)																
P9_7	16 (1)																

Note:
1. Pin assignments change depending on the PMC function.

Table 1.14 Pin Name Information by Pin Number (CAN and SSU/I²C)

Port	Pin No.	CAN (1)		SSU/I²C											
		CTX_0	CRX_0	SCL_0	SCL_1	SDA_0	SDA_1	SSI_0	SSI_1	$\overline{SCS\_0}$	$\overline{SCS\_1}$	SSCK_0	SSCK_1	SSO_0	SSO_1
P0_0	47														
P0_1	46														
P0_2	45														
P0_3	44														
P0_4	39														
P0_5	38														
P0_6	37														
P0_7	36														
P1_0	30														
P1_1	29														
P1_2	28														
P1_3	24														
P1_4	23														
P1_5	22														
P1_6	21							SSI_0							
P1_7	20														
P2_0	19 (2)														
P2_1	18 (2)														
P2_2	17 (2)														
P2_3	16 (2)														
P2_4	15														
P2_5	14														
P2_6	13														
P2_7	12														
P3_0	32														
P3_1	31														
P3_3	2							SSI_0		$\overline{SCS\_0}$					
P3_4	3					SDA_0		SSI_0		$\overline{SCS\_0}$					
P3_5	1			SCL_0								SSCK_0			
P3_7	48					SDA_0								SSO_0	
P4_2	40														
P4_3	5														
P4_4	6														
P4_5	25														
P4_6	10														
P4_7	8														
P6_0	41														
P6_1	43	CTX_0													
P6_2	42		CRX_0												
P6_3	35														
P6_4	34														
P6_5	33														
P6_6	26														
P6_7	27														
P9_4	19 (2)								SSI_1						
P9_5	18 (2)						SDA_1				$\overline{SCS\_1}$				
P9_6	17 (2)				SCL_1								SSCK_1		
P9_7	16 (2)														SSO_1

Notes:
1. Available in the R8C/54E Group and the R8C/54F Group only.
2. Pin assignments change depending on the PMC function.

Table 1.15 Pin Name Information by Pin Number (Timer RJ, Timer RB2, and Timer RC)

Port	Pin No.	Timer RJ				Timer RB2	Timer RC					
		TRJO_0	TRJO_1	TRJIO_0	TRJIO_1	TRBO_0	TRCCLK_0	TRCIOA_0	TRCIOB_0	TRCIOC_0	TRCIOD_0	TRCTRG_0
P0_0	47							TRCIOA_0				TRCTRG_0
P0_1	46		TRJO_1					TRCIOA_0				TRCTRG_0
P0_2	45				TRJIO_1			TRCIOA_0				TRCTRG_0
P0_3	44								TRCIOB_0			
P0_4	39								TRCIOB_0			
P0_5	38								TRCIOB_0			
P0_6	37										TRCIOD_0	
P0_7	36									TRCIOC_0		
P1_0	30										TRCIOD_0	
P1_1	29							TRCIOA_0				TRCTRG_0
P1_2	28								TRCIOB_0			
P1_3	24					TRBO_0				TRCIOC_0		
P1_4	23						TRCCLK_0					
P1_5	22			TRJIO_0								
P1_6	21											
P1_7	20			TRJIO_0								
P2_0	19 (1)								TRCIOB_0			
P2_1	18 (1)									TRCIOC_0		
P2_2	17 (1)										TRCIOD_0	
P2_3	16 (1)											
P2_4	15											
P2_5	14											
P2_6	13											
P2_7	12											
P3_0	32	TRJO_0										
P3_1	31					TRBO_0						
P3_3	2						TRCCLK_0					
P3_4	3									TRCIOC_0		
P3_5	1										TRCIOD_0	
P3_7	48	TRJO_0					TRCCLK_0					
P4_2	40											
P4_3	5											
P4_4	6											
P4_5	25											
P4_6	10											
P4_7	8											
P6_0	41											
P6_1	43											
P6_2	42											
P6_3	35		TRJO_1									
P6_4	34				TRJIO_1							
P6_5	33								TRCIOB_0			
P6_6	26									TRCIOC_0		
P6_7	27										TRCIOD_0	
P9_4	19 (1)											
P9_5	18 (1)											
P9_6	17 (1)											
P9_7	16 (1)											

Note:
1. Pin assignments change depending on the PMC function.

Table 1.16 Pin Name Information by Pin Number (Timer RD and Timer RE2)

Port	Pin No.	Timer RD									Timer RE2
		TRDCLK_0	TRDIOA0_0	TRDIOB0_0	TRDIOC0_0	TRDIOD0_0	TRDIOA1_0	TRDIOB1_0	TRDIOC1_0	TRDIOD1_0	TMRE2O
P0_0	47										
P0_1	46										
P0_2	45										
P0_3	44										
P0_4	39										TMRE2O
P0_5	38										
P0_6	37										
P0_7	36										
P1_0	30						TRDIOA1_0				
P1_1	29							TRDIOB1_0			
P1_2	28								TRDIOC1_0		
P1_3	24									TRDIOD1_0	
P1_4	23										
P1_5	22										
P1_6	21										
P1_7	20										
P2_0	19 (1)	TRDCLK_0	TRDIOA0_0								
P2_1	18 (1)			TRDIOB0_0	TRDIOC0_0						
P2_2	17 (1)			TRDIOB0_0	TRDIOC0_0						
P2_3	16 (1)					TRDIOD0_0					
P2_4	15						TRDIOA1_0				
P2_5	14							TRDIOB1_0			
P2_6	13								TRDIOC1_0		
P2_7	12									TRDIOD1_0	
P3_0	32										
P3_1	31										
P3_3	2					TRDIOD0_0					
P3_4	3			TRDIOB0_0					TRDIOC1_0		
P3_5	1	TRDCLK_0	TRDIOA0_0							TRDIOD1_0	
P3_7	48				TRDIOC0_0						
P4_2	40										
P4_3	5										
P4_4	6										
P4_5	25										
P4_6	10										
P4_7	8										
P6_0	41										TMRE2O
P6_1	43										
P6_2	42										
P6_3	35										
P6_4	34										
P6_5	33										
P6_6	26										
P6_7	27										
P9_4	19 (1)										
P9_5	18 (1)										
P9_6	17 (1)										
P9_7	16 (1)										

Note:
1. Pin assignments change depending on the PMC function.

Table 1.17 Pin Name Information by Pin Number (Others)

Port	Pin No.	Others		
P0_0	47	AN7		
P0_1	46	AN6		
P0_2	45	AN5		
P0_3	44	AN4		
P0_4	39	AN3		
P0_5	38	AN2		
P0_6	37	AN1		
P0_7	36	AN0		
P1_0	30	$\overline{KI0}$	AN8	IVREF1
P1_1	29	$\overline{KI1}$	AN9	IVCMP1
P1_2	28	$\overline{KI2}$	AN10	
P1_3	24	$\overline{KI3}$	AN11	
P1_4	23			
P1_5	22			
P1_6	21			
P1_7	20			
P2_0	19 (1)			
P2_1	18 (1)			
P2_2	17 (1)			
P2_3	16 (1)			
P2_4	15	IVCMP3		
P2_5	14	IVREF3		
P2_6	13			
P2_7	12			
P3_0	32			
P3_1	31			
P3_3	2			
P3_4	3			
P3_5	1			
P3_7	48			
P4_2	40	VREF		
P4_3	5			
P4_4	6			
P4_5	25			
P4_6	10	XIN		
P4_7	8	XOUT		
P6_0	41			
P6_1	43			
P6_2	42			
P6_3	35			
P6_4	34			
P6_5	33			
P6_6	26			
P6_7	27			
P9_4	19 (1)			
P9_5	18 (1)			
P9_6	17 (1)			
P9_7	16 (1)			

Note:
1. Pin assignments change depending on the PMC function.

1.5 Pin Functions

Tables 1.18 and 1.19 list Pin Functions.

Table 1.18 Pin Functions (1)

Item	Pin Name	I/O	Description
Power supply input	VCC, VSS	—	Apply 2.7 V through 5.5 V to the VCC pin when the CPU clock = 32 MHz. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	—	Power supply input for the A/D converter. Connect a capacitor between pins AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Applying a low level to this pin resets the MCU.
MODE	MODE	I	Connect this pin to the VCC pin via a resistor.
XIN clock input	XIN	I	I/O for the XIN clock generation circuit. Connect a ceramic resonator or a crystal oscillator between pins XIN and XOUT. (1) To use an external clock, input it to the XIN pin and leave the XOUT pin open.
XIN clock output	XOUT	I/O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT4}}$	I	$\overline{\text{INT}}$ interrupt input.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input.
Timers RJ_0 and RJ_1	TRJIO_0, TRJIO_1	I/O	Input/output for timer RJ.
	TRJO_0, TRJO_1	O	Output for timer RJ.
Timers RB2_0	TRBO_0	O	Output for timer RB2.
Timers RC_0	TRCCLK_0	I	External clock input.
	TRCTRG_0	I	External trigger input.
	TRCIOA_0, TRCIOB_0, TRCIOC_0, TRCIOD_0	I/O	Input/output for timer RC.
Timers RD_0	TRDIOA0_0, TRDIOA1_0, TRDIOB0_0, TRDIOB1_0, TRDIOC0_0, TRDIOC1_0, TRDIOD0_0, TRDIOD1_0	I/O	Input/output for timer RD.
	TRDCLK_0	I	External clock input.
Timer RE2	TMRE2O	O	Divided clock output.
Serial interface (UART0)	CLK_0, CLK_1	I/O	Transfer clock input/output.
	RXD_0, RXD_1	I	Serial data input.
	TXD_0, TXD_1	O	Serial data output.
Serial interface (UART2)	$\overline{\text{CTS2}}$	I	Input for transmission control.
	$\overline{\text{RTS2}}$	O	Output for reception control.
	RXD2	I	Serial data input.
	TXD2	O	Serial data output.
	CLK2	I/O	Transfer clock input/output.

Note:
1. Contact the oscillator manufacturer for oscillation characteristics.

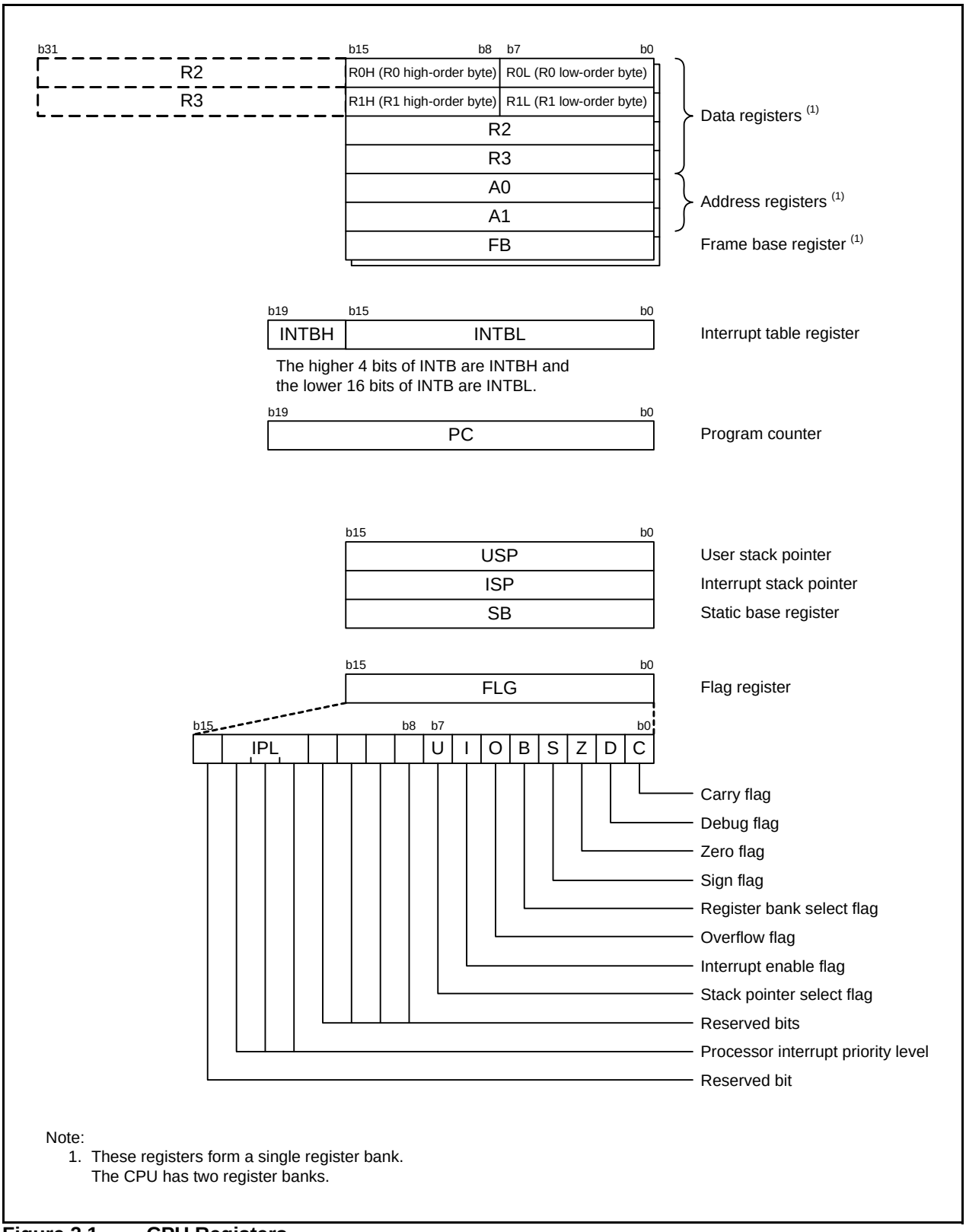
Table 1.19 Pin Functions (2)

Item	Pin Name	I/O	Description
Synchronous serial communication unit (SSU_0, SSU_1)	SSI_0, SSI_1	I/O	Data input/output.
	$\overline{SCS\_0}$, $\overline{SCS\_1}$	I/O	Chip-select input/output.
	SSCK_0, SSCK_1	I/O	Clock input/output.
	SSO_0, SSO_1	I/O	Data input/output.
I^2C bus (I^2C_0 and I^2C_1)	SCL_0, SCL_1	I/O	Clock input/output.
	SDA_0, SDA_1	I/O	Data input/output.
CAN module (CAN_0) (1)	CRX_0	I	Data input for CAN.
	CTX_0	O	Data output for CAN.
Reference voltage input	VREF	I	Reference voltage input for the A/D converter.
A/D converter	AN0 to AN11	I	Analog input for the A/D converter.
Comparator B	IVCMP1, IVCMP3	I	Analog voltage input for comparator B.
	IVREF1, IVREF3	I	Reference voltage input for comparator B.
I/O ports	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 and P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_7, P6_0 to P6_7, P9_4 to P9_7	I/O	8-bit CMOS input/output ports. Each port has an I/O select direction register, enabling switching input and output for each pin. For input ports, the presence or absence of a pull-up resistor can be selected by a program. All ports can be used as LED drive (high drive) ports.
Input port	P4_2	I	Input-only port.

Note:
1. Available in the R8C/54E Group and the R8C/54F Group only.

2. Central Processing Unit (CPU)

Figure 2.1 shows the 13 CPU Registers. The registers R0, R1, R2, R3, A0, A1, and FB form a single register bank. The CPU has two register banks.



Note:
1. These registers form a single register bank.
The CPU has two register banks.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 through R3.
R0 can be split into high-order (R0H) and low-order (R0L) registers to be used separately as 8-bit data registers. The same applies to R1H and R1L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). Similarly, R3 and R1 can be used as a 32-bit data register.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 functions in the same manner as A0. A1 can be combined with A0 and used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

PC is a 20-bit register that indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of the FLG register is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register used for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register that indicates the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated in the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. It must only be set to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0. Otherwise it is set to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value. Otherwise it is set to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow. Otherwise it is set to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts. Interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is 0. USP is selected when the U flag is 1. The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction for a software interrupt numbered from 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns eight processor interrupt priority levels from 0 to 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled.

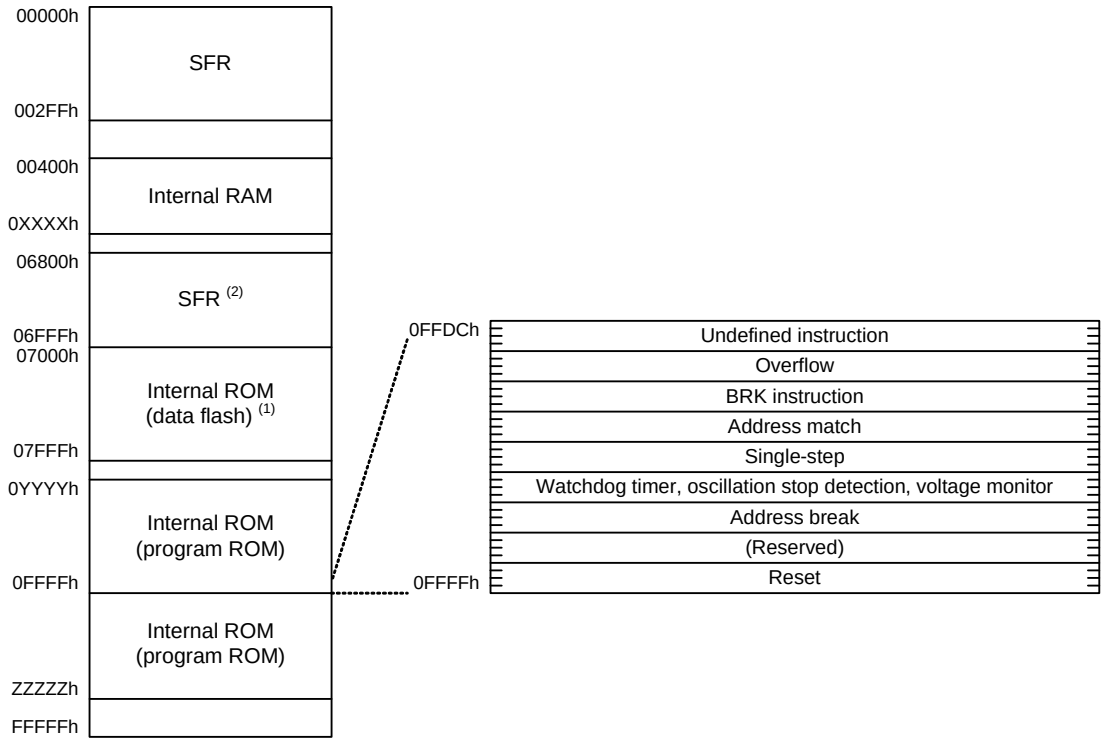
2.8.10 Reserved Bit

The write value must be 0. The read value is undefined.

3. Address Space

3.1 R8C/54E Group Memory Map

Figure 3.1 shows the R8C/54E Group Memory Map. The R8C/54E Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. Up to 32 Kbytes of the internal ROM (program ROM) is allocated at lower addresses, beginning with address 0FFFFh. The area in excess of 32 Kbytes is allocated at higher addresses, beginning with address 10000h.
For example, a 64-Kbyte internal ROM is allocated at addresses 08000h to 17FFFh.
The fixed interrupt vector table is allocated at addresses 0FFDCh to 0FFFFh. The start address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated at addresses 07000h to 07FFFh.
The internal RAM is allocated at higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM is allocated at addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated at addresses 00000h to 02FFFh and addresses 06800h to 06FFFh. Peripheral function control registers are allocated here. All unallocated locations within the SFRs are reserved and cannot be accessed by users.



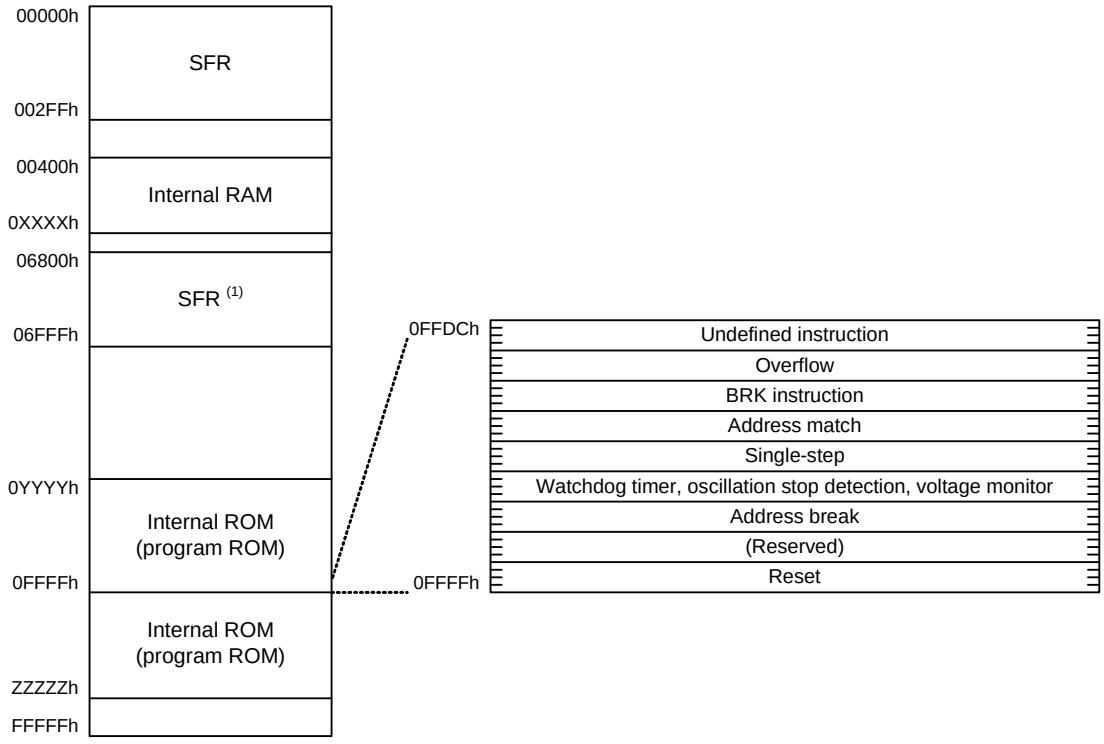
Notes:
1. Data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
2. Addresses 06800h to 06FFFh are used for the CAN, DTC, and other SFR areas.
3. The blank areas are reserved. No access is allowed.

Part Number	Internal ROM			Internal RAM	
	Capacity	Address 0YYYYh	Address ZZZZZh	Capacity	Address 0XXXXh
R5F21546EJFP, R5F21546EKFP	32 Kbytes	08000h	0FFFFh	2.5 Kbytes	00DFFh
R5F21547EJFP, R5F21547EKFP	48 Kbytes	08000h	13FFFh	4 Kbytes	013FFh
R5F21548EJFP, R5F21548EKFP	64 Kbytes	08000h	17FFFh	6 Kbytes	01BFFh
R5F2154AEJFP, R5F2154AEKFP	96 Kbytes	08000h	1FFFFh	8 Kbytes	023FFh
R5F2154CEJFP, R5F2154CEKFP	128 Kbytes	08000h	27FFFh	10 Kbytes	02BFFh

Figure 3.1 R8C/54E Group Memory Map

3.2 R8C/54F Group Memory Map

Figure 3.2 shows the R8C/54F Group Memory Map. The R8C/54F Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. Up to 32 Kbytes of the internal ROM (program ROM) is allocated at lower addresses, beginning with address 0FFFFh. The area in excess of 32 Kbytes is allocated at higher addresses, beginning with address 10000h.
For example, a 64-Kbyte internal ROM is allocated at addresses 08000h to 17FFFh.
The fixed interrupt vector table is allocated at addresses 0FFDCh to 0FFFFh. The start address of each interrupt routine is stored here.
The internal RAM is allocated at higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM is allocated at addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated at addresses 00000h to 02FFFh and addresses 06800h to 06FFFh. Peripheral function control registers are allocated here. All unallocated locations within the SFRs are reserved and cannot be accessed by users.



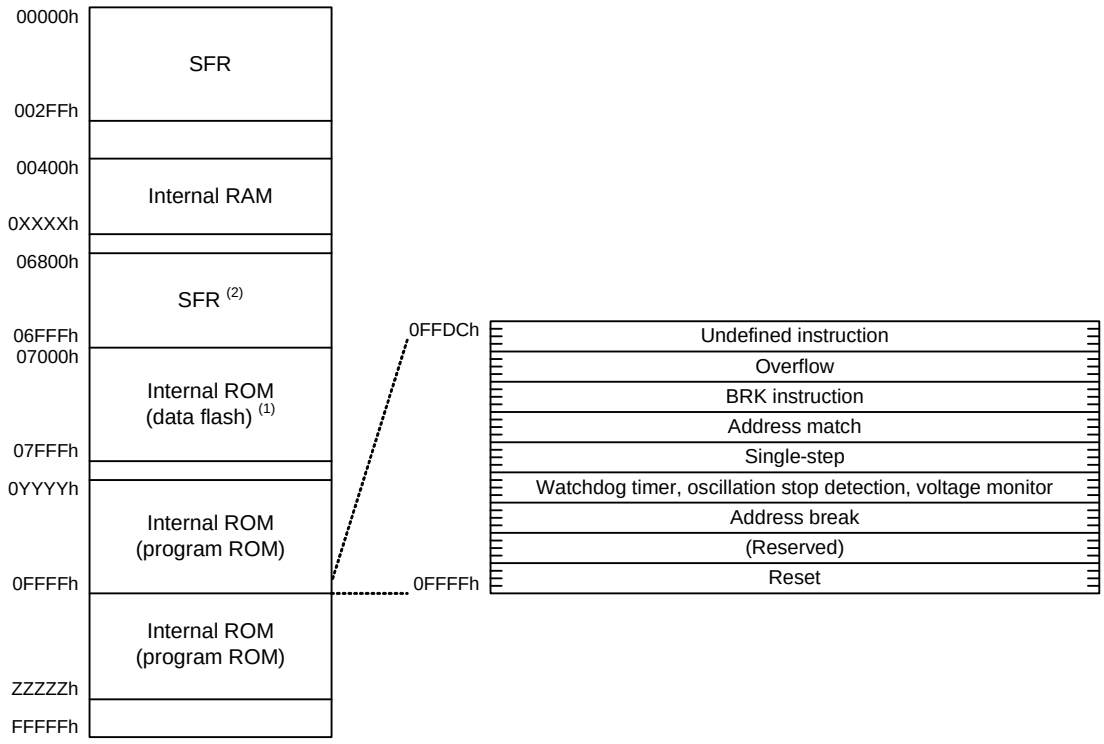
Notes:
1. Addresses 06800h to 06FFFh are used for the CAN, DTC, and other SFR areas.
2. The blank areas are reserved. No access is allowed.

Part Number	Internal ROM			Internal RAM	
	Capacity	Address 0YYYYh	Address ZZZZZh	Capacity	Address 0XXXXh
R5F21546FJFP, R5F21546FKFP	32 Kbytes	08000h	0FFFFh	2.5 Kbytes	00DFFh
R5F21547FJFP, R5F21547FKFP	48 Kbytes	08000h	13FFFh	4 Kbytes	013FFh
R5F21548FJFP, R5F21548FKFP	64 Kbytes	08000h	17FFFh	6 Kbytes	01BFFh
R5F2154AFJFP, R5F2154AFKFP	96 Kbytes	08000h	1FFFFh	8 Kbytes	023FFh
R5F2154CFJFP, R5F2154CFKFP	128 Kbytes	08000h	27FFFh	10 Kbytes	02BFFh

Figure 3.2 R8C/54F Group Memory Map

3.3 R8C/54G Group Memory Map

Figure 3.3 shows the R8C/54G Group Memory Map. The R8C/54G Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. Up to 32 Kbytes of the internal ROM (program ROM) is allocated at lower addresses, beginning with address 0FFFFh. The area in excess of 32 Kbytes is allocated at higher addresses, beginning with address 10000h.
For example, a 64-Kbyte internal ROM is allocated at addresses 08000h to 17FFFh.
The fixed interrupt vector table is allocated at addresses 0FFDCh to 0FFFFh. The start address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated at addresses 07000h to 07FFFh.
The internal RAM is allocated at higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM is allocated at addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated at addresses 00000h to 02FFFh and addresses 06800h to 06FFFh. Peripheral function control registers are allocated here. All unallocated locations within the SFRs are reserved and cannot be accessed by users.



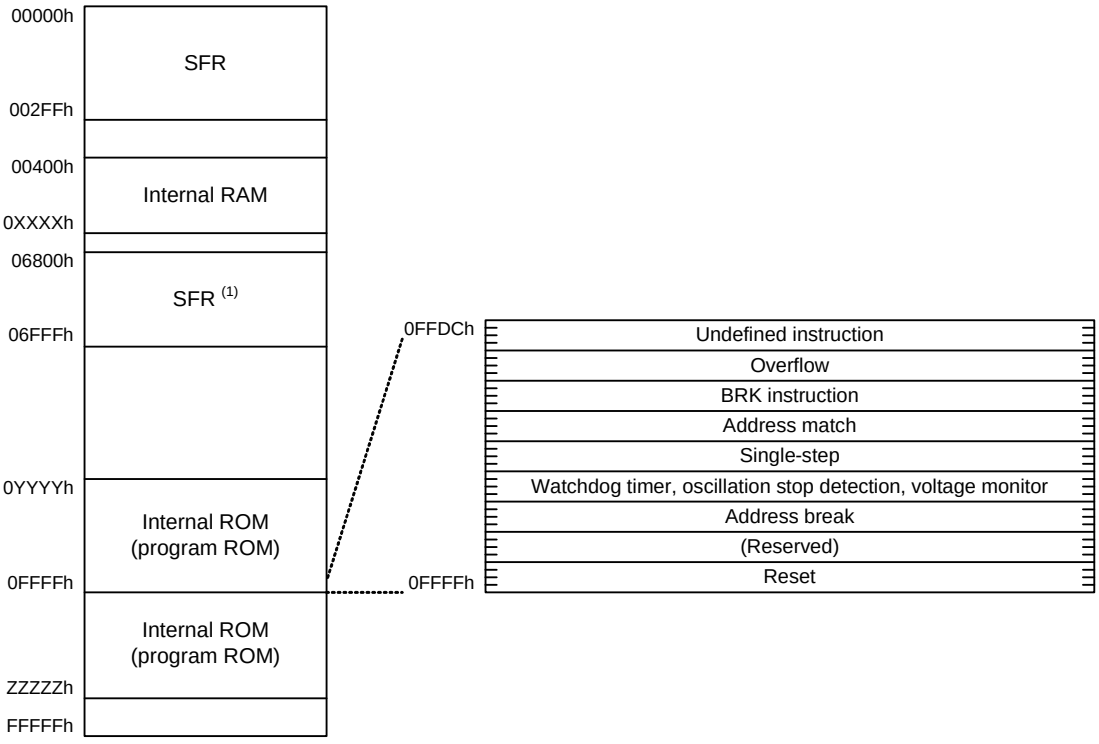
Notes:
1. Data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
2. Addresses 06800h to 06FFFh are used for the DTC and other SFR areas.
3. The blank areas are reserved. No access is allowed.

Part Number	Internal ROM			Internal RAM	
	Capacity	Address 0YYYYh	Address ZZZZZh	Capacity	Address 0XXXXh
R5F21546GJFP, R5F21546GKFP	32 Kbytes	08000h	0FFFFh	2.5 Kbytes	00DFFh
R5F21547GJFP, R5F21547GKFP	48 Kbytes	08000h	13FFFh	4 Kbytes	013FFh
R5F21548GJFP, R5F21548GKFP	64 Kbytes	08000h	17FFFh	6 Kbytes	01BFFh
R5F2154AGJFP, R5F2154AGKFP	96 Kbytes	08000h	1FFFFh	8 Kbytes	023FFh
R5F2154CGJFP, R5F2154CGKFP	128 Kbytes	08000h	27FFFh	10 Kbytes	02BFFh

Figure 3.3 R8C/54G Group Memory Map

3.4 R8C/54H Group Memory Map

Figure 3.4 shows the R8C/54H Group Memory Map. The R8C/54H Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. Up to 32 Kbytes of the internal ROM (program ROM) is allocated at lower addresses, beginning with address 0FFFFh. The area in excess of 32 Kbytes is allocated at higher addresses, beginning with address 10000h.
For example, a 64-Kbyte internal ROM is allocated at addresses 08000h to 17FFFh.
The fixed interrupt vector table is allocated at addresses 0FFDCh to 0FFFFh. The start address of each interrupt routine is stored here.
The internal RAM is allocated at higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM is allocated at addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated at addresses 00000h to 02FFFh and addresses 06800h to 06FFFh. Peripheral function control registers are allocated here. All unallocated locations within the SFRs are reserved and cannot be accessed by users.



Notes:
1. Addresses 06800h to 06FFFh are used for the DTC and other SFR areas.
2. The blank areas are reserved. No access is allowed.

Part Number	Internal ROM			Internal RAM	
	Capacity	Address 0YYYYh	Address ZZZZZh	Capacity	Address 0XXXXh
R5F21546HJFP, R5F21546HKFP	32 Kbytes	08000h	0FFFFh	2.5 Kbytes	00DFFh
R5F21547HJFP, R5F21547HKFP	48 Kbytes	08000h	13FFFh	4 Kbytes	013FFh
R5F21548HJFP, R5F21548HKFP	64 Kbytes	08000h	17FFFh	6 Kbytes	01BFFh
R5F2154AHJFP, R5F2154AHKFP	96 Kbytes	08000h	1FFFFh	8 Kbytes	023FFh
R5F2154CHJFP, R5F2154CHKFP	128 Kbytes	08000h	27FFFh	10 Kbytes	02BFFh

Figure 3.4 R8C/54H Group Memory Map

3.5 Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 3.1 to 3.22 list the SFR Information. Table 3.23 lists the ID Code Area, Option Function Select Area.

Table 3.1 SFR Information (1) (1)

Address	Symbol	Register Name	After Reset	Remarks
00000h				
00001h				
00002h				
00003h				
00004h	PM0	Processor Mode Register 0	00h	
00005h	PM1	Processor Mode Register 1	10000000b	
00006h				
00007h	PRCR	Protect Register	00h	
00008h	CM0	System Clock Control Register 0	00101000b	
00009h	CM1	System Clock Control Register 1	00100000b	
0000Ah	OCD	Oscillation Stop Detection Register	00h	
0000Bh	CM3	System Clock Control Register 3	00h	
0000Ch	CM4	System Clock Control Register 4	00000001b	
0000Dh				
0000Eh				
0000Fh	PCLKR1	Peripheral Clock Select Register 1	00h	
00010h				
00011h				
00012h	FRA0	High-Speed On-Chip Oscillator Control Register 0	00h	
00013h				
00014h	FRA2	High-Speed On-Chip Oscillator Control Register 2	00h	
00015h				
00016h				
00017h				
00018h				
00019h				
0001Ah				
0001Bh				
0001Ch	PLC0	PLL Control Register 0	00010010b	
0001Dh				
0001Eh				
0001Fh				
00020h	RISR	Reset Interrupt Select Register	10000000b or 00000000b	(Note 2)
00021h	WDTR	Watchdog Timer Reset Register	FFh	
00022h	WDTS	Watchdog Timer Start Register	FFh	
00023h	WDTC	Watchdog Timer Control Register	01111111b	
00024h	CSPR	Count Source Protection Mode Register	10000000b or 00000000b	(Note 2)
00025h				
00026h				
00027h				
00028h	RSTFR	Reset Source Determination Register	00XXXXXXb	
00029h				
0002Ah				
0002Bh				
0002Ch	SVDC	STBY VDC Power Control Register	00h	
0002Dh				
0002Eh				
0002Fh				
00030h	CMPA	Voltage Monitor Circuit Control Register	00h	
00031h	VCAC	Voltage Monitor Circuit Edge Select Register	00h	
00032h	OCVREFCR	On-Chip Reference Voltage Control Register	00h	
00033h				
00034h	VCA2	Voltage Detection Register 2	00000000b or 00100000b	(Note 3)
00035h				
00036h	VD1LS	Voltage Detection 1 Level Select Register	00000111b	
00037h				
00038h	VW0C	Voltage Monitor 0 Circuit Control Register	1100XX10b or 1100XX11b	(Note 3)
00039h	VW1C	Voltage Monitor 1 Circuit Control Register	10001010b	

X: Undefined

Notes:

1. The blank areas are reserved. No access is allowed.
2. Depends on the CSPROINI bit in the OFS register.
3. Depends on the LVDASI bit in the OFS register.

Table 3.2 SFR Information (2) (1)

Address	Symbol	Register Name	After Reset	Remarks
0003Ah	VW2C	Voltage Monitor 2 Circuit Control Register	10001010b	
0003Bh				
0003Ch				
0003Dh				
0003Eh				
0003Fh				
00040h				
00041h	FMRDYIC	Interrupt Control Register	00h	
00042h	TRJIC_1	Interrupt Control Register	00h	
00043h				
00044h				
00045h				
00046h	INT4IC	Interrupt Control Register	00h	
00047h	TRCIC_0	Interrupt Control Register	00h	
00048h	TRD0IC_0	Interrupt Control Register	00h	
00049h	TRD1IC_0	Interrupt Control Register	00h	
0004Ah	TRE2IC	Interrupt Control Register	00h	
0004Bh	U2TIC	Interrupt Control Register	00h	
0004Ch	U2RIC	Interrupt Control Register	00h	
0004Dh	KUPIC	Interrupt Control Register	00h	
0004Eh	ADIC	Interrupt Control Register	00h	
0004Fh	SSUIC_0/IICIC_0	Interrupt Control Register	00h	
00050h				
00051h	U0TIC_0	Interrupt Control Register	00h	
00052h	U0RIC_0	Interrupt Control Register	00h	
00053h	U0TIC_1	Interrupt Control Register	00h	
00054h	U0RIC_1	Interrupt Control Register	00h	
00055h	INT2IC	Interrupt Control Register	00h	
00056h	TRJIC_0	Interrupt Control Register	00h	
00057h				
00058h	TRB2IC_0	Interrupt Control Register	00h	
00059h	INT1IC	Interrupt Control Register	00h	
0005Ah	INT3IC	Interrupt Control Register	00h	
0005Bh				
0005Ch				
0005Dh	INT0IC	Interrupt Control Register	00h	
0005Eh	U2BCNIC	Interrupt Control Register	00h	
0005Fh				
00060h				
00061h				
00062h				
00063h				
00064h				
00065h				
00066h				
00067h				
00068h				
00069h				
0006Ah				
0006Bh				
0006Ch	CANRXIC_0	Interrupt Control Register	00h	
0006Dh	CANTXIC_0	Interrupt Control Register	00h	
0006Eh	CANERIC_0	Interrupt Control Register	00h	
0006Fh				
00070h				
00071h				
00072h	VCMP1IC	Interrupt Control Register	00h	
00073h	VCMP2IC	Interrupt Control Register	00h	
00074h				
00075h				
00076h				
00077h				
00078h				
00079h	SSUIC_1/IICIC_1	Interrupt Control Register	00h	

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.3 SFR Information (3) (1)

Address	Symbol	Register Name	After Reset	Remarks
0007Ah				
0007Bh				
0007Ch				
0007Dh				
0007Eh				
0007Fh				
00080h	U0MR_0	UART0_0 Transmit/Receive Mode Register	00h	
00081h	U0BRG_0	UART0_0 Bit Rate Register	XXh	
00082h	U0TB_0	UART0_0 Transmit Buffer Register	XXh	
00083h			XXh	
00084h	U0C0_0	UART0_0 Transmit/Receive Control Register 0	00001000b	
00085h	U0C1_0	UART0_0 Transmit/Receive Control Register 1	00000010b	
00086h	U0RB_0	UART0_0 Receive Buffer Register	XXXXh	
00087h				
00088h	U0IR_0	UART0_0 Interrupt Flag and Enable Register	00h	
00089h				
0008Ah				
0008Bh				
0008Ch	LINCR2_0	LIN_0 Special Function Register	00h	
0008Dh				
0008Eh	LINCT_0	LIN_0 Control Register	00h	
0008Fh	LINST_0	LIN_0 Status Register	00h	
00090h	U0MR_1	UART0_1 Transmit/Receive Mode Register	00h	
00091h	U0BRG_1	UART0_1 Bit Rate Register	XXh	
00092h	U0TB_1	UART0_1 Transmit Buffer Register	XXh	
00093h			XXh	
00094h	U0C0_1	UART0_1 Transmit/Receive Control Register 0	00001000b	
00095h	U0C1_1	UART0_1 Transmit/Receive Control Register 1	00000010b	
00096h	U0RB_1	UART0_1 Receive Buffer Register	XXXXh	
00097h				
00098h	U0IR_1	UART0_1 Interrupt Flag and Enable Register	00h	
00099h				
0009Ah				
0009Bh				
0009Ch	LINCR2_1	LIN_1 Special Function Register	00h	
0009Dh				
0009Eh	LINCT_1	LIN_1 Control Register	00h	
0009Fh	LINST_1	LIN_1 Status Register	00h	
000A0h				
000A1h				
000A2h				
000A3h				
000A4h				
000A5h				
000A6h				
000A7h				
000A8h				
000A9h				
000AAh				
000ABh				
000ACh				
000ADh				
000AEh				
000AFh				
000B0h				
000B1h				
000B2h				
000B3h				
000B4h				
000B5h				
000B6h				
000B7h				
000B8h				
000B9h				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.4 SFR Information (4) (1)

Address	Symbol	Register Name	After Reset	Remarks
000BAh				
000BBh				
000BCh				
000BDh				
000BEh				
000BFh				
000C0h	U2MR	UART2 Transmit/Receive Mode Register	00h	
000C1h	U2BRG	UART2 Bit Rate Register	00h	
000C2h	U2TB	UART2 Transmit Buffer Register	00h	
000C3h			00h	
000C4h	U2C0	UART2 Transmit/Receive Control Register 0	00001000b	
000C5h	U2C1	UART2 Transmit/Receive Control Register 1	00000010b	
000C6h	U2RB	UART2 Receive Buffer Register	0000h	
000C7h				
000C8h	U2RXDF	UART2 Digital Filter Function Select Register	00h	
000C9h				
000CAh				
000CBh				
000CCh				
000CDh				
000CEh				
000CFh				
000D0h	U2SMR5	UART2 Special Mode Register 5	00h	
000D1h				
000D2h				
000D3h				
000D4h				
000D5h	U2SMR3	UART2 Special Mode Register 3	00h	
000D6h				
000D7h	U2SMR	UART2 Special Mode Register	00h	
000D8h				
000D9h				
000DAh				
000DBh				
000DCh				
000DDh				
000DEh				
000DFh				
000E0h	IICCR_0	I²C_0 Control Register	00001110b	
000E1h	SSBR_0	SS_0 Bit Counter Register	11111000b	
000E2h	SITDR_0	SI_0 Transmit Data Register	FFh	
000E3h			FFh	
000E4h	SIRDR_0	SI_0 Receive Data Register	FFh	
000E5h			FFh	
000E6h	SICR1_0	SI_0 Control Register 1	00h	
000E7h	SICR2_0	SI_0 Control Register 2	01111101b	
000E8h	SIMR1_0	SI_0 Mode Register 1	00010000b	
000E9h	SIER_0	SI_0 Interrupt Enable Register	00h	
000EAh	SISR_0	SI_0 Status Register	00h	
000EBh	SIMR2_0	SI_0 Mode Register 2	00h	
000ECh				
000EDh				
000EEh				
000EFh				
000F0h	IICCR_1	I²C_1 Control Register	00001110b	
000F1h	SSBR_1	SS_1 Bit Counter Register	11111000b	
000F2h	SITDR_1	SI_1 Transmit Data Register	FFh	
000F3h			FFh	
000F4h	SIRDR_1	SI_1 Receive Data Register	FFh	
000F5h			FFh	
000F6h	SICR1_1	SI_1 Control Register 1	00h	
000F7h	SICR2_1	SI_1 Control Register 2	01111101b	
000F8h	SIMR1_1	SI_1 Mode Register 1	00010000b	
000F9h	SIER_1	SI_1 Interrupt Enable Register	00h	

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.5 SFR Information (5) (1)

Address	Symbol		Register Name	After Reset	Remarks
000FAh	SISR_1		SI_1 Status Register	00h	
000FBh	SIMR2_1		SI_1 Mode Register 2	00h	
000FCh					
000FDh					
000FEh					
000FFh					
00100h					
00101h					
00102h					
00103h					
00104h					
00105h					
00106h					
00107h					
00108h					
00109h					
0010Ah					
0010Bh					
0010Ch					
0010Dh					
0010Eh					
0010Fh					
00110h	TRJ_0		Timer RJ_0 Counter Register	FFFFh	
00111h					
00112h	TRJCR_0		Timer RJ_0 Control Register	00h	
00113h	TRJIOC_0		Timer RJ_0 I/O Control Register	00h	
00114h	TRJMR_0		Timer RJ_0 Mode Register	00h	
00115h	TRJISR_0		Timer RJ_0 Event Pin Select Register	00h	
00116h					
00117h					
00118h	TRJ_1		Timer RJ_1 Counter Register	FFFFh	
00119h					
0011Ah	TRJCR_1		Timer RJ_1 Control Register	00h	
0011Bh	TRJIOC_1		Timer RJ_1 I/O Control Register	00h	
0011Ch	TRJMR_1		Timer RJ_1 Mode Register	00h	
0011Dh	TRJISR_1		Timer RJ_1 Event Pin Select Register	00h	
0011Eh					
0011Fh					
00120h					
00121h					
00122h					
00123h					
00124h					
00125h					
00126h					
00127h					
00128h					
00129h					
0012Ah					
0012Bh					
0012Ch					
0012Dh					
0012Eh					
0012Fh					
00130h	TRBCR_0		Timer RB2_0 Control Register	00h	
00131h	TRBOCR_0		Timer RB2_0 One-Shot Control Register	00h	
00132h	TRBIOC_0		Timer RB2_0 I/O Control Register	00h	
00133h	TRBMR_0		Timer RB2_0 Mode Register	00h	
00134h	TRBPRE_0	TRBPRSC_0	Timer RB2_0 Prescaler Register Timer RB2_0 Primary/Secondary Register (Lower 8 Bits)	FFh	
00135h	TRBPR_0		Timer RB2_0 Primary Register Timer RB2_0 Primary Register (Higher 8 Bits)	FFh	
00136h	TRBSC_0		Timer RB2_0 Secondary Register Timer RB2_0 Secondary Register (Higher 8 Bits)	FFh	
00137h	TRBIR_0		Timer RB2_0 Interrupt Request Register	00h	
00138h	TRCCNT_0		Timer RC_0 Counter	0000h	
00139h					

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.6 SFR Information (6) (1)

Address	Symbol	Register Name	After Reset	Remarks
0013Ah	TRCGRA_0	Timer RC_0 General Register A	FFFFh	
0013Bh				
0013Ch	TRCGRB_0	Timer RC_0 General Register B	FFFFh	
0013Dh				
0013Eh	TRCGRC_0	Timer RC_0 General Register C	FFFFh	
0013Fh				
00140h	TRCGRD_0	Timer RC_0 General Register D	FFFFh	
00141h				
00142h	TRCMR_0	Timer RC_0 Mode Register	01001000b	
00143h	TRCCR1_0	Timer RC_0 Control Register 1	00h	
00144h	TRCIER_0	Timer RC_0 Interrupt Enable Register	01110000b	
00145h	TRCSR_0	Timer RC_0 Status Register	01110000b	
00146h	TRCIOR0_0	Timer RC_0 I/O Control Register 0	10001000b	
00147h	TRCIOR1_0	Timer RC_0 I/O Control Register 1	10001000b	
00148h	TRCCR2_0	Timer RC_0 Control Register 2	00011000b	
00149h	TRCDF_0	Timer RC_0 Digital Filter Function Select Register	00h	
0014Ah	TRCOER_0	Timer RC_0 Output Enable Register	01111111b	
0014Bh	TRCADCR_0	Timer RC_0 A/D Conversion Trigger Control Register	11110000b	
0014Ch	TRCOPR_0	Timer RC_0 Output Waveform Manipulation Register	00h	
0014Dh	TRCELCCR_0	Timer RC_0 ELC Cooperation Control Register	00h	
0014Eh				
0014Fh				
00150h				
00151h				
00152h				
00153h				
00154h				
00155h				
00156h				
00157h				
00158h				
00159h				
0015Ah				
0015Bh				
0015Ch				
0015Dh				
0015Eh				
0015Fh				
00160h				
00161h				
00162h				
00163h				
00164h				
00165h				
00166h				
00167h				
00168h				
00169h				
0016Ah				
0016Bh				
0016Ch				
0016Dh				
0016Eh				
0016Fh				
00170h	TRESEC	Timer RE2 Counter Data Register	00h	
00171h	TREMIN	Timer RE2 Compare Data Register	00h	
00172h				
00173h				
00174h				
00175h				
00176h				
00177h	TRECR	Timer RE2 Control Register	00000100b	
00178h	TRECSR	Timer RE2 Count Source Select Register	00001000b	
00179h				

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.7 SFR Information (7) (1)

Address	Symbol	Register Name	After Reset	Remarks
0017Ah	TREIFR	Timer RE2 Interrupt Flag Register	00h	
0017Bh	TREIER	Timer RE2 Interrupt Enable Register	00h	
0017Ch				
0017Dh				
0017Eh				
0017Fh	TREPRC	Timer RE2 Protect Register	00h	
00180h	TRDELCCR_0	Timer RD_0 ELC Cooperation Control Register	00h	
00181h				
00182h	TRDADCR_0	Timer RD_0 Trigger Control Register	00h	
00183h	TRDSTR_0	Timer RD_0 Start Register	11111100b	
00184h	TRDMR_0	Timer RD_0 Mode Register	00001110b	
00185h	TRDPMR_0	Timer RD_0 PWM Mode Register	10001000b	
00186h	TRDFCR_0	Timer RD_0 Function Control Register	10000000b	
00187h	TRDOER1_0	Timer RD_0 Output Master Enable Register 1	FFh	
00188h	TRDOER2_0	Timer RD_0 Output Master Enable Register 2	01111111b	
00189h	TRDOCR_0	Timer RD_0 Output Control Register	00h	
0018Ah	TRDDF0_0	Timer RD_0 Digital Filter Function Select Register 0	00h	
0018Bh	TRDDF1_0	Timer RD_0 Digital Filter Function Select Register 1	00h	
0018Ch				
0018Dh				
0018Eh				
0018Fh				
00190h	TRDCR0_0	Timer RD_0 Control Register 0	00h	
00191h	TRDIORA0_0	Timer RD_0 I/O Control Register A0	10001000b	
00192h	TRDIORC0_0	Timer RD_0 I/O Control Register C0	10001000b	
00193h	TRDSR0_0	Timer RD_0 Status Register 0	11100000b	
00194h	TRDIER0_0	Timer RD_0 Interrupt Enable Register 0	11100000b	
00195h	TRDPOCR0_0	Timer RD_0 PWM Mode Output Level Control Register 0	11111000b	
00196h	TRD0_0	Timer RD_0 Counter 0	0000h	
00197h				
00198h	TRDGRA0_0	Timer RD_0 General Register A0	FFFFh	
00199h				
0019Ah	TRDGRB0_0	Timer RD_0 General Register B0	FFFFh	
0019Bh				
0019Ch	TRDGRC0_0	Timer RD_0 General Register C0	FFFFh	
0019Dh				
0019Eh	TRDGRD0_0	Timer RD_0 General Register D0	FFFFh	
0019Fh				
001A0h	TRDCR1_0	Timer RD_0 Control Register 1	00h	
001A1h	TRDIORA1_0	Timer RD_0 I/O Control Register A1	10001000b	
001A2h	TRDIORC1_0	Timer RD_0 I/O Control Register C1	10001000b	
001A3h	TRDSR1_0	Timer RD_0 Status Register 1	11000000b	
001A4h	TRDIER1_0	Timer RD_0 Interrupt Enable Register 1	11100000b	
001A5h	TRDPOCR1_0	Timer RD_0 PWM Mode Output Level Control Register 1	11111000b	
001A6h	TRD1_0	Timer RD_0 Counter 1	0000h	
001A7h				
001A8h	TRDGRA1_0	Timer RD_0 General Register A1	FFFFh	
001A9h				
001AAh	TRDGRB1_0	Timer RD_0 General Register B1	FFFFh	
001ABh				
001ACh	TRDGRC1_0	Timer RD_0 General Register C1	FFFFh	
001ADh				
001AEh	TRDGRD1_0	Timer RD_0 General Register D1	FFFFh	
001AFh				
001B0h to 001FFh				

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.8 SFR Information (8) (1)

Address	Symbol	Register Name	After Reset	Remarks
00200h	AD0	A/D Register 0	00h	
00201h			00h	
00202h	AD1	A/D Register 1	00h	
00203h			00h	
00204h	AD2	A/D Register 2	00h	
00205h			00h	
00206h	AD3	A/D Register 3	00h	
00207h			00h	
00208h	AD4	A/D Register 4	00h	
00209h			00h	
0020Ah	AD5	A/D Register 5	00h	
0020Bh			00h	
0020Ch	AD6	A/D Register 6	00h	
0020Dh			00h	
0020Eh	AD7	A/D Register 7	00h	
0020Fh			00h	
00210h				
00211h				
00212h				
00213h				
00214h	ADMOD	A/D Mode Register	00h	
00215h	ADINSEL	A/D Input Select Register	11000000b	
00216h	ADCON0	A/D Control Register 0	00h	
00217h	ADCON1	A/D Control Register 1	00h	
00218h				
00219h				
0021Ah				
0021Bh				
0021Ch				
0021Dh				
0021Eh				
0021Fh				
00220h				
00221h				
00222h				
00223h				
00224h				
00225h				
00226h				
00227h				
00228h	INTCMP	Comparator B Control Register 0	00h	
00229h				
0022Ah				
0022Bh				
0022Ch				
0022Dh				
0022Eh				
0022Fh				
00230h	INTEN	External Input Enable Register 0	00h	
00231h	INTEN1	External Input Enable Register 1	00h	
00232h	INTF	INT Input Filter Select Register 0	00h	
00233h	INTF1	INT Input Filter Select Register 1	00h	
00234h	INTPOL	INT Input Polarity Switch Register	00h	
00235h				
00236h	KIEN	Key Input Interrupt Enable Register	00h	
00237h				
00238h	MSTCR0	Module Standby Control Register 0	00h	
00239h	MSTCR1	Module Standby Control Register 1	00h	
0023Ah	MSTCR2	Module Standby Control Register 2	00h	
0023Bh	MSTCR3	Module Standby Control Register 3	00h	
0023Ch				
0023Dh				
0023Eh				
0023Fh				

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.9 SFR Information (9) (1)

Address	Symbol	Register Name	After Reset	Remarks
00240h				
00241h				
00242h				
00243h				
00244h				
00245h				
00246h				
00247h				
00248h				
00249h				
0024Ah				
0024Bh				
0024Ch				
0024Dh				
0024Eh				
0024Fh				
00250h				
00251h				
00252h	FST	Flash Memory Status Register	10000X00b	
00253h				
00254h	FMR0	Flash Memory Control Register 0	00h	
00255h	FMR1	Flash Memory Control Register 1	00h	
00256h	FMR2	Flash Memory Control Register 2	00h	
00257h				
00258h				
00259h				
0025Ah				
0025Bh				
0025Ch				
0025Dh				
0025Eh				
0025Fh				
00260h	AIADR0L	Address Match Interrupt Address 0L Register	XXXXh	
00261h				
00262h	AIADR0H	Address Match Interrupt Address 0H Register	0000XXXXb	
00263h	AIEN0	Address Match Interrupt Enable 0 Register	00h	
00264h	AIADR1L	Address Match Interrupt Address 1L Register	XXXXh	
00265h				
00266h	AIADR1H	Address Match Interrupt Address 1H Register	0000XXXXb	
00267h	AIEN1	Address Match Interrupt Enable 1 Register	00h	
00268h				
00269h				
0026Ah				
0026Bh				
0026Ch				
0026Dh				
0026Eh				
0026Fh				
00270h				
00271h				
00272h				
00273h				
00274h				
00275h				
00276h				
00277h				
00278h				
00279h				
0027Ah				
0027Bh				
0027Ch				
0027Dh				
0027Eh				
0027Fh				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.10 SFR Information (10) (1)

Address	Symbol	Register Name	After Reset	Remarks
00280h	DTCTL	DTC Activation Control Register	00h	
00281h				
00282h				
00283h				
00284h				
00285h				
00286h				
00287h				
00288h	DTCEN0	DTC Activation Enable Register 0	00h	
00289h	DTCEN1	DTC Activation Enable Register 1	00h	
0028Ah	DTCEN2	DTC Activation Enable Register 2	00h	
0028Bh	DTCEN3	DTC Activation Enable Register 3	00h	
0028Ch	DTCEN4	DTC Activation Enable Register 4	00h	
0028Dh	DTCEN5	DTC Activation Enable Register 5	00h	
0028Eh	DTCEN6	DTC Activation Enable Register 6	00h	
0028Fh				
00290h	CRCSAR	SFR Snoop Address Register	0000h	
00291h				
00292h	CRCMR	CRC Control Register	00h	
00293h				
00294h	CRCD	CRC Data Register	0000h	
00295h				
00296h	CRCIN	CRC Input Register	00h	
00297h				
00298h				
00299h				
0029Ah				
0029Bh				
0029Ch				
0029Dh				
0029Eh				
0029Fh				
002A0h	TRJ_0SR	Timer RJ_0 Pin Select Register	00h	
002A1h	TRJ_1SR	Timer RJ_1 Pin Select Register	00h	
002A2h				
002A3h				
002A4h	TRBSR	Timer RB2 Pin Select Register	00h	
002A5h	TRCCLKSR	Timer RCCLK Pin Select Register	00h	
002A6h	TRC_0SR0	Timer RC_0 Pin Select Register 0	00h	
002A7h	TRC_0SR1	Timer RC_0 Pin Select Register 1	00h	
002A8h				
002A9h	TRD_0SR0	Timer RD_0 Pin Select Register 0	00h	
002AAh	TRD_0SR1	Timer RD_0 Pin Select Register 1	00h	
002ABh				
002ACh				
002ADh	TIMSR	Timer Pin Select Register	00h	
002AEh	U_0SR	UART0_0 Pin Select Register	00h	
002AFh	U_1SR	UART0_1 Pin Select Register	00h	
002B0h				
002B1h				
002B2h	U2SR0	UART2 Pin Select Register 0	00h	
002B3h	U2SR1	UART2 Pin Select Register 1	00h	
002B4h	SSUIIC_0SR	SSU/IIC_0 Pin Select Register	00h	
002B5h				
002B6h	INTSR0	INT Interrupt Input Pin Select Register 0	00h	
002B7h				
002B8h				
002B9h	PINSR	I/O Function Pin Select Register	00h	
002BAh				
002BBh				
002BCh				
002BDh				
002BEh	PMCSEL	Pin Assignment Select Register	00h	
002BFh				

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.11 SFR Information (11) (1)

Address	Symbol	Register Name	After Reset	Remarks
002C0h	PUR0	Pull-Up Control Register 0	00h	
002C1h	PUR1	Pull-Up Control Register 1	00h	
002C2h	PUR2	Pull-Up Control Register 2	00h	
002C3h				
002C4h				
002C5h				
002C6h				
002C7h				
002C8h	P1DRR	Port P1 Drive Capacity Control Register	00h	
002C9h	P2DRR	Port P2 Drive Capacity Control Register	00h	
002CAh				
002CBh				
002CCh	DRR0	Drive Capacity Control Register 0	00h	
002CDh	DRR1	Drive Capacity Control Register 1	00h	
002CEh	DRR2	Drive Capacity Control Register 2	00h	
002CFh				
002D0h	VLT0	Input Threshold Control Register 0	00h	
002D1h	VLT1	Input Threshold Control Register 1	00h	
002D2h	VLT2	Input Threshold Control Register 2	00h	
002D3h				
002D4h				
002D5h				
002D6h				
002D7h				
002D8h				
002D9h				
002DAh				
002DBh				
002DCh				
002DDh				
002DEh				
002DFh				
002E0h	PORT0	Port P0 Register	XXh	
002E1h	PORT1	Port P1 Register	XXh	
002E2h	PD0	Port P0 Direction Register	00h	
002E3h	PD1	Port P1 Direction Register	00h	
002E4h	PORT2	Port P2 Register	XXh	
002E5h	PORT3	Port P3 Register	XXh	
002E6h	PD2	Port P2 Direction Register	00h	
002E7h	PD3	Port P3 Direction Register	00h	
002E8h	PORT4	Port P4 Register	XXh	
002E9h				
002EAh	PD4	Port P4 Direction Register	00h	
002EBh				
002ECh	PORT6	Port P6 Register	XXh	
002EDh				
002EEh	PD6	Port P6 Direction Register	00h	
002EFh				
002F0h				
002F1h	PORT9	Port P9 Register	XXh	
002F2h				
002F3h	PD9	Port P9 Direction Register	00h	
002F4h				
002F5h				
002F6h				
002F7h				
002F8h				
002F9h				
002FAh				
002FBh				
002FCh				
002FDh				
002FEh				
002FFh				
00300h to 003FFh				

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.12 SFR Information (12) (1)

Address	Symbol	Register Name	After Reset	Remarks
00400h to 02BFFh	On-chip RAM	On-chip RAM		
02C00h to 069FFh				
06A00h	ELSELR0	Event Output Destination Select Register 0	00h	
06A01h	ELSELR1	Event Output Destination Select Register 1	00h	
06A02h	ELSELR2	Event Output Destination Select Register 2	00h	
06A03h	ELSELR3	Event Output Destination Select Register 3	00h	
06A04h	ELSELR4	Event Output Destination Select Register 4	00h	
06A05h				
06A06h				
06A07h				
06A08h	ELSELR8	Event Output Destination Select Register 8	00h	
06A09h	ELSELR9	Event Output Destination Select Register 9	00h	
06A0Ah	ELSELR10	Event Output Destination Select Register 10	00h	
06A0Bh	ELSELR11	Event Output Destination Select Register 11	00h	
06A0Ch	ELSELR12	Event Output Destination Select Register 12	00h	
06A0Dh	ELSELR13	Event Output Destination Select Register 13	00h	
06A0Eh	ELSELR14	Event Output Destination Select Register 14	00h	
06A0Fh	ELSELR15	Event Output Destination Select Register 15	00h	
06A10h	ELSELR16	Event Output Destination Select Register 16	00h	
06A11h	ELSELR17	Event Output Destination Select Register 17	00h	
06A12h	ELSELR18	Event Output Destination Select Register 18	00h	
06A13h	ELSELR19	Event Output Destination Select Register 19	00h	
06A14h	ELSELR20	Event Output Destination Select Register 20	00h	
06A15h	ELSELR21	Event Output Destination Select Register 21	00h	
06A16h	ELSELR22	Event Output Destination Select Register 22	00h	
06A17h	ELSELR23	Event Output Destination Select Register 23	00h	
06A18h	ELSELR24	Event Output Destination Select Register 24	00h	
06A19h				
06A1Ah				
06A1Bh				
06A1Ch				
06A1Dh				
06A1Eh				
06A1Fh				
06A20h				
06A21h				
06A22h				
06A23h				
06A24h				
06A25h				
06A26h				
06A27h				
06A28h				
06A29h				
06A2Ah				
06A2Bh				
06A2Ch				
06A2Dh				
06A2Eh				
06A2Fh				
06A30h				
06A31h to 06BFFh				
06C00h		Area for storing DTC transfer vector 0	XXh	
06C01h		Area for storing DTC transfer vector 1	XXh	
06C02h		Area for storing DTC transfer vector 2	XXh	
06C03h		Area for storing DTC transfer vector 3	XXh	
06C04h		Area for storing DTC transfer vector 4	XXh	
06C05h				
06C06h				
06C07h				
06C08h		Area for storing DTC transfer vector 8	XXh	
06C09h		Area for storing DTC transfer vector 9	XXh	

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.13 SFR Information (13) (1)

Address	Symbol	Register Name	After Reset	Remarks
06C0Ah		Area for storing DTC transfer vector 10	XXh	
06C0Bh		Area for storing DTC transfer vector 11	XXh	
06C0Ch		Area for storing DTC transfer vector 12	XXh	
06C0Dh		Area for storing DTC transfer vector 13	XXh	
06C0Eh		Area for storing DTC transfer vector 14	XXh	
06C0Fh		Area for storing DTC transfer vector 15	XXh	
06C10h		Area for storing DTC transfer vector 16	XXh	
06C11h		Area for storing DTC transfer vector 17	XXh	
06C12h		Area for storing DTC transfer vector 18	XXh	
06C13h		Area for storing DTC transfer vector 19	XXh	
06C14h				
06C15h				
06C16h		Area for storing DTC transfer vector 22	XXh	
06C17h		Area for storing DTC transfer vector 23	XXh	
06C18h		Area for storing DTC transfer vector 24	XXh	
06C19h		Area for storing DTC transfer vector 25	XXh	
06C1Ah		Area for storing DTC transfer vector 26	XXh	
06C1Bh		Area for storing DTC transfer vector 27	XXh	
06C1Ch		Area for storing DTC transfer vector 28	XXh	
06C1Dh		Area for storing DTC transfer vector 29	XXh	
06C1Eh		Area for storing DTC transfer vector 30	XXh	
06C1Fh		Area for storing DTC transfer vector 31	XXh	
06C20h		Area for storing DTC transfer vector 32	XXh	
06C21h		Area for storing DTC transfer vector 33	XXh	
06C22h				
06C23h				
06C24h				
06C25h				
06C26h		Area for storing DTC transfer vector 38	XXh	
06C27h		Area for storing DTC transfer vector 39	XXh	
06C28h				
06C29h				
06C2Ah		Area for storing DTC transfer vector 42	XXh	
06C2Bh				
06C2Ch				
06C2Dh				
06C2Eh				
06C2Fh				
06C30h				
06C31h		Area for storing DTC transfer vector 49	XXh	
06C32h		Area for storing DTC transfer vector 50	XXh	
06C33h		Area for storing DTC transfer vector 51	XXh	
06C34h		Area for storing DTC transfer vector 52	XXh	
06C35h				
06C36h				
06C37h				
06C38h				
06C39h				
06C3Ah				
06C3Bh				
06C3Ch				
06C3Dh				
06C3Eh				
06C3Fh				
06C40h	DTCCR0	DTC Control Register 0	XXh	
06C41h	DTBLS0	DTC Block Size Register 0	XXh	
06C42h	DTCCT0	DTC Transfer Count Register 0	XXh	
06C43h	DTRLD0	DTC Transfer Count Reload Register 0	XXh	
06C44h	DTSAR0	DTC Source Address Register 0	XXXXh	
06C45h				
06C46h	DTDAR0	DTC Destination Address Register 0	XXXXh	
06C47h				
06C48h	DTCCR1	DTC Control Register 1	XXh	
06C49h	DTBLS1	DTC Block Size Register 1	XXh	

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.14 SFR Information (14) (1)

Address	Symbol	Register Name	After Reset	Remarks
06C4Ah	DTCCT1	DTC Transfer Count Register 1	XXh	
06C4Bh	DTRLD1	DTC Transfer Count Reload Register 1	XXh	
06C4Ch	DTSAR1	DTC Source Address Register 1	XXXXh	
06C4Dh				
06C4Eh	DTDAR1	DTC Destination Address Register 1	XXXXh	
06C4Fh				
06C50h	DTCCR2	DTC Control Register 2	XXh	
06C51h	DTBLS2	DTC Block Size Register 2	XXh	
06C52h	DTCCT2	DTC Transfer Count Register 2	XXh	
06C53h	DTRLD2	DTC Transfer Count Reload Register 2	XXh	
06C54h	DTSAR2	DTC Source Address Register 2	XXXXh	
06C55h				
06C56h	DTDAR2	DTC Destination Address Register 2	XXXXh	
06C57h				
06C58h	DTCCR3	DTC Control Register 3	XXh	
06C59h	DTBLS3	DTC Block Size Register 3	XXh	
06C5Ah	DTCCT3	DTC Transfer Count Register 3	XXh	
06C5Bh	DTRLD3	DTC Transfer Count Reload Register 3	XXh	
06C5Ch	DTSAR3	DTC Source Address Register 3	XXXXh	
06C5Dh				
06C5Eh	DTDAR3	DTC Destination Address Register 3	XXXXh	
06C5Fh				
06C60h	DTCCR4	DTC Control Register 4	XXh	
06C61h	DTBLS4	DTC Block Size Register 4	XXh	
06C62h	DTCCT4	DTC Transfer Count Register 4	XXh	
06C63h	DTRLD4	DTC Transfer Count Reload Register 4	XXh	
06C64h	DTSAR4	DTC Source Address Register 4	XXXXh	
06C65h				
06C66h	DTDAR4	DTC Destination Address Register 4	XXXXh	
06C67h				
06C68h	DTCCR5	DTC Control Register 5	XXh	
06C69h	DTBLS5	DTC Block Size Register 5	XXh	
06C6Ah	DTCCT5	DTC Transfer Count Register 5	XXh	
06C6Bh	DTRLD5	DTC Transfer Count Reload Register 5	XXh	
06C6Ch	DTSAR5	DTC Source Address Register 5	XXXXh	
06C6Dh				
06C6Eh	DTDAR5	DTC Destination Address Register 5	XXXXh	
06C6Fh				
06C70h	DTCCR6	DTC Control Register 6	XXh	
06C71h	DTBLS6	DTC Block Size Register 6	XXh	
06C72h	DTCCT6	DTC Transfer Count Register 6	XXh	
06C73h	DTRLD6	DTC Transfer Count Reload Register 6	XXh	
06C74h	DTSAR6	DTC Source Address Register 6	XXXXh	
06C75h				
06C76h	DTDAR6	DTC Destination Address Register 6	XXXXh	
06C77h				
06C78h	DTCCR7	DTC Control Register 7	XXh	
06C79h	DTBLS7	DTC Block Size Register 7	XXh	
06C7Ah	DTCCT7	DTC Transfer Count Register 7	XXh	
06C7Bh	DTRLD7	DTC Transfer Count Reload Register 7	XXh	
06C7Ch	DTSAR7	DTC Source Address Register 7	XXXXh	
06C7Dh				
06C7Eh	DTDAR7	DTC Destination Address Register 7	XXXXh	
06C7Fh				
06C80h	DTCCR8	DTC Control Register 8	XXh	
06C81h	DTBLS8	DTC Block Size Register 8	XXh	
06C82h	DTCCT8	DTC Transfer Count Register 8	XXh	
06C83h	DTRLD8	DTC Transfer Count Reload Register 8	XXh	
06C84h	DTSAR8	DTC Source Address Register 8	XXXXh	
06C85h				
06C86h	DTDAR8	DTC Destination Address Register 8	XXXXh	
06C87h				
06C88h	DTCCR9	DTC Control Register 9	XXh	
06C89h	DTBLS9	DTC Block Size Register 9	XXh	
06C8Ah	DTCCT9	DTC Transfer Count Register 9	XXh	
06C8Bh	DTRLD9	DTC Transfer Count Reload Register 9	XXh	
06C8Ch	DTSAR9	DTC Source Address Register 9	XXXXh	
06C8Dh				
06C8Eh	DTDAR9	DTC Destination Address Register 9	XXXXh	
06C8Fh				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.15 SFR Information (15) (1)

Address	Symbol	Register Name	After Reset	Remarks
06C90h	DTCCR10	DTC Control Register 10	XXh	
06C91h	DTBLS10	DTC Block Size Register 10	XXh	
06C92h	DTCCT10	DTC Transfer Count Register 10	XXh	
06C93h	DTRLD10	DTC Transfer Count Reload Register 10	XXh	
06C94h	DTSAR10	DTC Source Address Register 10	XXXXh	
06C95h				
06C96h	DTDAR10	DTC Destination Address Register 10	XXXXh	
06C97h				
06C98h	DTCCR11	DTC Control Register 11	XXh	
06C99h	DTBLS11	DTC Block Size Register 11	XXh	
06C9Ah	DTCCT11	DTC Transfer Count Register 11	XXh	
06C9Bh	DTRLD11	DTC Transfer Count Reload Register 11	XXh	
06C9Ch	DTSAR11	DTC Source Address Register 11	XXXXh	
06C9Dh				
06C9Eh	DTDAR11	DTC Destination Address Register 11	XXXXh	
06C9Fh				
06CA0h	DTCCR12	DTC Control Register 12	XXh	
06CA1h	DTBLS12	DTC Block Size Register 12	XXh	
06CA2h	DTCCT12	DTC Transfer Count Register 12	XXh	
06CA3h	DTRLD12	DTC Transfer Count Reload Register 12	XXh	
06CA4h	DTSAR12	DTC Source Address Register 12	XXXXh	
06CA5h				
06CA6h	DTDAR12	DTC Destination Address Register 12	XXXXh	
06CA7h				
06CA8h	DTCCR13	DTC Control Register 13	XXh	
06CA9h	DTBLS13	DTC Block Size Register 13	XXh	
06CAAh	DTCCT13	DTC Transfer Count Register 13	XXh	
06CABh	DTRLD13	DTC Transfer Count Reload Register 13	XXh	
06CACh	DTSAR13	DTC Source Address Register 13	XXXXh	
06CADh				
06CAEh	DTDAR13	DTC Destination Address Register 13	XXXXh	
06CAFh				
06CB0h	DTCCR14	DTC Control Register 14	XXh	
06CB1h	DTBLS14	DTC Block Size Register 14	XXh	
06CB2h	DTCCT14	DTC Transfer Count Register 14	XXh	
06CB3h	DTRLD14	DTC Transfer Count Reload Register 14	XXh	
06CB4h	DTSAR14	DTC Source Address Register 14	XXXXh	
06CB5h				
06CB6h	DTDAR14	DTC Destination Address Register 14	XXXXh	
06CB7h				
06CB8h	DTCCR15	DTC Control Register 15	XXh	
06CB9h	DTBLS15	DTC Block Size Register 15	XXh	
06CBAh	DTCCT15	DTC Transfer Count Register 15	XXh	
06CBBh	DTRLD15	DTC Transfer Count Reload Register 15	XXh	
06CBCh	DTSAR15	DTC Source Address Register 15	XXXXh	
06CBDh				
06CBEh	DTDAR15	DTC Destination Address Register 15	XXXXh	
06CBFh				
06CC0h	DTCCR16	DTC Control Register 16	XXh	
06CC1h	DTBLS16	DTC Block Size Register 16	XXh	
06CC2h	DTCCT16	DTC Transfer Count Register 16	XXh	
06CC3h	DTRLD16	DTC Transfer Count Reload Register 16	XXh	
06CC4h	DTSAR16	DTC Source Address Register 16	XXXXh	
06CC5h				
06CC6h	DTDAR16	DTC Destination Address Register 16	XXXXh	
06CC7h				
06CC8h	DTCCR17	DTC Control Register 17	XXh	
06CC9h	DTBLS17	DTC Block Size Register 17	XXh	
06CCAh	DTCCT17	DTC Transfer Count Register 17	XXh	
06CCBh	DTRLD17	DTC Transfer Count Reload Register 17	XXh	
06CCCh	DTSAR17	DTC Source Address Register 17	XXXXh	
06CCDh				
06CCEh	DTDAR17	DTC Destination Address Register 17	XXXXh	
06CCFh				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.16 SFR Information (16) (1)

Address	Symbol	Register Name	After Reset	Remarks
06CD0h	DTCCR18	DTC Control Register 18	XXh	
06CD1h	DTBLS18	DTC Block Size Register 18	XXh	
06CD2h	DTCCT18	DTC Transfer Count Register 18	XXh	
06CD3h	DTRLD18	DTC Transfer Count Reload Register 18	XXh	
06CD4h	DTSAR18	DTC Source Address Register 18	XXXXh	
06CD5h				
06CD6h	DTDAR18	DTC Destination Address Register 18	XXXXh	
06CD7h				
06CD8h	DTCCR19	DTC Control Register 19	XXh	
06CD9h	DTBLS19	DTC Block Size Register 19	XXh	
06CDAh	DTCCT19	DTC Transfer Count Register 19	XXh	
06CDBh	DTRLD19	DTC Transfer Count Reload Register 19	XXh	
06CDCh	DTSAR19	DTC Source Address Register 19	XXXXh	
06CDDh				
06CDEh	DTDAR19	DTC Destination Address Register 19	XXXXh	
06CDFh				
06CE0h	DTCCR20	DTC Control Register 20	XXh	
06CE1h	DTBLS20	DTC Block Size Register 20	XXh	
06CE2h	DTCCT20	DTC Transfer Count Register 20	XXh	
06CE3h	DTRLD20	DTC Transfer Count Reload Register 20	XXh	
06CE4h	DTSAR20	DTC Source Address Register 20	XXXXh	
06CE5h				
06CE6h	DTDAR20	DTC Destination Address Register 20	XXXXh	
06CE7h				
06CE8h	DTCCR21	DTC Control Register 21	XXh	
06CE9h	DTBLS21	DTC Block Size Register 21	XXh	
06CEAh	DTCCT21	DTC Transfer Count Register 21	XXh	
06CEBh	DTRLD21	DTC Transfer Count Reload Register 21	XXh	
06CECh	DTSAR21	DTC Source Address Register 21	XXXXh	
06CEDh				
06CEEh	DTDAR21	DTC Destination Address Register 21	XXXXh	
06CEFh				
06CF0h	DTCCR22	DTC Control Register 22	XXh	
06CF1h	DTBLS22	DTC Block Size Register 22	XXh	
06CF2h	DTCCT22	DTC Transfer Count Register 22	XXh	
06CF3h	DTRLD22	DTC Transfer Count Reload Register 22	XXh	
06CF4h	DTSAR22	DTC Source Address Register 22	XXXXh	
06CF5h				
06CF6h	DTDAR22	DTC Destination Address Register 22	XXXXh	
06CF7h				
06CF8h	DTCCR23	DTC Control Register 23	XXh	
06CF9h	DTBLS23	DTC Block Size Register 23	XXh	
06CFAh	DTCCT23	DTC Transfer Count Register 23	XXh	
06CFBh	DTRLD23	DTC Transfer Count Reload Register 23	XXh	
06CFCh	DTSAR23	DTC Source Address Register 23	XXXXh	
06CFDh				
06CFEh	DTDAR23	DTC Destination Address Register 23	XXXXh	
06CFFh				
06D00h to 06DFFh				
06E00h	CMB0_0	CAN_0 Mailbox 0	XXh	
06E01h			XXh	
06E02h			XXh	
06E03h			XXh	
06E04h			XXh	
06E05h			XXh	
06E06h			XXh	
06E07h			XXh	
06E08h			XXh	
06E09h			XXh	
06E0Ah			XXh	
06E0Bh			XXh	
06E0Ch			XXh	
06E0Dh			XXh	
06E0Eh			XXh	
06E0Fh			XXh	

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.17 SFR Information (17) (1)

Address	Symbol	Register Name	After Reset	Remarks
06E10h	CMB1_0	CAN_0 Mailbox 1	XXh	
06E11h			XXh	
06E12h			XXh	
06E13h			XXh	
06E14h			XXh	
06E15h			XXh	
06E16h			XXh	
06E17h			XXh	
06E18h			XXh	
06E19h			XXh	
06E1Ah			XXh	
06E1Bh			XXh	
06E1Ch			XXh	
06E1Dh			XXh	
06E1Eh			XXh	
06E1Fh			XXh	
06E20h	CMB2_0	CAN_0 Mailbox 2	XXh	
06E21h			XXh	
06E22h			XXh	
06E23h			XXh	
06E24h			XXh	
06E25h			XXh	
06E26h			XXh	
06E27h			XXh	
06E28h			XXh	
06E29h			XXh	
06E2Ah			XXh	
06E2Bh			XXh	
06E2Ch			XXh	
06E2Dh			XXh	
06E2Eh			XXh	
06E2Fh			XXh	
06E30h	CMB3_0	CAN_0 Mailbox 3	XXh	
06E31h			XXh	
06E32h			XXh	
06E33h			XXh	
06E34h			XXh	
06E35h			XXh	
06E36h			XXh	
06E37h			XXh	
06E38h			XXh	
06E39h			XXh	
06E3Ah			XXh	
06E3Bh			XXh	
06E3Ch			XXh	
06E3Dh			XXh	
06E3Eh			XXh	
06E3Fh			XXh	
06E40h	CMB4_0	CAN_0 Mailbox 4	XXh	
06E41h			XXh	
06E42h			XXh	
06E43h			XXh	
06E44h			XXh	
06E45h			XXh	
06E46h			XXh	
06E47h			XXh	
06E48h			XXh	
06E49h			XXh	
06E4Ah			XXh	
06E4Bh			XXh	
06E4Ch			XXh	
06E4Dh			XXh	
06E4Eh			XXh	
06E4Fh			XXh	

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.18 SFR Information (18) (1)

Address	Symbol	Register Name	After Reset	Remarks
06E50h	CMB5_0	CAN_0 Mailbox 5	XXh	
06E51h			XXh	
06E52h			XXh	
06E53h			XXh	
06E54h			XXh	
06E55h			XXh	
06E56h			XXh	
06E57h			XXh	
06E58h			XXh	
06E59h			XXh	
06E5Ah			XXh	
06E5Bh			XXh	
06E5Ch			XXh	
06E5Dh			XXh	
06E5Eh			XXh	
06E5Fh			XXh	
06E60h	CMB6_0	CAN_0 Mailbox 6	XXh	
06E61h			XXh	
06E62h			XXh	
06E63h			XXh	
06E64h			XXh	
06E65h			XXh	
06E66h			XXh	
06E67h			XXh	
06E68h			XXh	
06E69h			XXh	
06E6Ah			XXh	
06E6Bh			XXh	
06E6Ch			XXh	
06E6Dh			XXh	
06E6Eh			XXh	
06E6Fh			XXh	
06E70h	CMB7_0	CAN_0 Mailbox 7	XXh	
06E71h			XXh	
06E72h			XXh	
06E73h			XXh	
06E74h			XXh	
06E75h			XXh	
06E76h			XXh	
06E77h			XXh	
06E78h			XXh	
06E79h			XXh	
06E7Ah			XXh	
06E7Bh			XXh	
06E7Ch			XXh	
06E7Dh			XXh	
06E7Eh			XXh	
06E7Fh			XXh	
06E80h	CMB8_0	CAN_0 Mailbox 8	XXh	
06E81h			XXh	
06E82h			XXh	
06E83h			XXh	
06E84h			XXh	
06E85h			XXh	
06E86h			XXh	
06E87h			XXh	
06E88h			XXh	
06E89h			XXh	
06E8Ah			XXh	
06E8Bh			XXh	
06E8Ch			XXh	
06E8Dh			XXh	
06E8Eh			XXh	
06E8Fh			XXh	

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.19 SFR Information (19) (1)

Address	Symbol	Register Name	After Reset	Remarks
06E90h	CMB9_0	CAN_0 Mailbox 9	XXh	
06E91h			XXh	
06E92h			XXh	
06E93h			XXh	
06E94h			XXh	
06E95h			XXh	
06E96h			XXh	
06E97h			XXh	
06E98h			XXh	
06E99h			XXh	
06E9Ah			XXh	
06E9Bh			XXh	
06E9Ch			XXh	
06E9Dh			XXh	
06E9Eh			XXh	
06E9Fh			XXh	
06EA0h	CMB10_0	CAN_0 Mailbox 10	XXh	
06EA1h			XXh	
06EA2h			XXh	
06EA3h			XXh	
06EA4h			XXh	
06EA5h			XXh	
06EA6h			XXh	
06EA7h			XXh	
06EA8h			XXh	
06EA9h			XXh	
06EAAh			XXh	
06EABh			XXh	
06EACh			XXh	
06EADh			XXh	
06EAEh			XXh	
06EAFh			XXh	
06EB0h	CMB11_0	CAN_0 Mailbox 11	XXh	
06EB1h			XXh	
06EB2h			XXh	
06EB3h			XXh	
06EB4h			XXh	
06EB5h			XXh	
06EB6h			XXh	
06EB7h			XXh	
06EB8h			XXh	
06EB9h			XXh	
06EBAh			XXh	
06EBBh			XXh	
06EBCh			XXh	
06EBDh			XXh	
06EBEh			XXh	
06EBFh			XXh	
06EC0h	CMB12_0	CAN_0 Mailbox 12	XXh	
06EC1h			XXh	
06EC2h			XXh	
06EC3h			XXh	
06EC4h			XXh	
06EC5h			XXh	
06EC6h			XXh	
06EC7h			XXh	
06EC8h			XXh	
06EC9h			XXh	
06ECAh			XXh	
06ECBh			XXh	
06ECCh			XXh	
06ECDh			XXh	
06ECEh			XXh	
06ECFh			XXh	

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.20 SFR Information (20) (1)

Address	Symbol	Register Name	After Reset	Remarks
06ED0h	CMB13_0	CAN_0 Mailbox 13	XXh	
06ED1h			XXh	
06ED2h			XXh	
06ED3h			XXh	
06ED4h			XXh	
06ED5h			XXh	
06ED6h			XXh	
06ED7h			XXh	
06ED8h			XXh	
06ED9h			XXh	
06EDAh			XXh	
06EDBh			XXh	
06EDCh			XXh	
06EDDh			XXh	
06EDEh			XXh	
06EDFh			XXh	
06EE0h	CMB14_0	CAN_0 Mailbox 14	XXh	
06EE1h			XXh	
06EE2h			XXh	
06EE3h			XXh	
06EE4h			XXh	
06EE5h			XXh	
06EE6h			XXh	
06EE7h			XXh	
06EE8h			XXh	
06EE9h			XXh	
06EEAh			XXh	
06EEBh			XXh	
06EECh			XXh	
06EEDh			XXh	
06EEEh			XXh	
06EEFh			XXh	
06EF0h	CMB15_0	CAN_0 Mailbox 15	XXh	
06EF1h			XXh	
06EF2h			XXh	
06EF3h			XXh	
06EF4h			XXh	
06EF5h			XXh	
06EF6h			XXh	
06EF7h			XXh	
06EF8h			XXh	
06EF9h			XXh	
06EFAh			XXh	
06EFBh			XXh	
06EFCh			XXh	
06EFDh			XXh	
06EFEh			XXh	
06EFFh			XXh	
06F00h				
06F01h				
06F02h				
06F03h				
06F04h				
06F05h				
06F06h				
06F07h				
06F08h				
06F09h				
06F0Ah				
06F0Bh				
06F0Ch				
06F0Dh				
06F0Eh				
06F0Fh				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.21 SFR Information (21) (1)

Address	Symbol	Register Name	After Reset	Remarks
06F10h	CMKR0_0	CAN_0 Mask Register 0	XXh	
06F11h			XXh	
06F12h			XXh	
06F13h			XXh	
06F14h	CMKR1_0	CAN_0 Mask Register 1	XXh	
06F15h			XXh	
06F16h			XXh	
06F17h			XXh	
06F18h	CMKR2_0	CAN_0 Mask Register 2	XXh	
06F19h			XXh	
06F1Ah			XXh	
06F1Bh			XXh	
06F1Ch	CMKR3_0	CAN_0 Mask Register 3	XXh	
06F1Dh			XXh	
06F1Eh			XXh	
06F1Fh			XXh	
06F20h	CFIDCR0_0	CAN_0 FIFO Received ID Compare Register 0	XXh	
06F21h			XXh	
06F22h			XXh	
06F23h			XXh	
06F24h	CFIDCR1_0	CAN_0 FIFO Received ID Compare Register 1	XXh	
06F25h			XXh	
06F26h			XXh	
06F27h			XXh	
06F28h				
06F29h				
06F2Ah	CMKIVLR_0	CAN_0 Mask Invalid Register	XXh	
06F2Bh			XXh	
06F2Ch				
06F2Dh				
06F2Eh	CMIER_0	CAN_0 Mailbox Interrupt Enable Register	XXh	
06F2Fh			XXh	
06F30h	CMCTL0_0	CAN_0 Message Control Register 0	00h	
06F31h	CMCTL1_0	CAN_0 Message Control Register 1	00h	
06F32h	CMCTL2_0	CAN_0 Message Control Register 2	00h	
06F33h	CMCTL3_0	CAN_0 Message Control Register 3	00h	
06F34h	CMCTL4_0	CAN_0 Message Control Register 4	00h	
06F35h	CMCTL5_0	CAN_0 Message Control Register 5	00h	
06F36h	CMCTL6_0	CAN_0 Message Control Register 6	00h	
06F37h	CMCTL7_0	CAN_0 Message Control Register 7	00h	
06F38h	CMCTL8_0	CAN_0 Message Control Register 8	00h	
06F39h	CMCTL9_0	CAN_0 Message Control Register 9	00h	
06F3Ah	CMCTL10_0	CAN_0 Message Control Register 10	00h	
06F3Bh	CMCTL11_0	CAN_0 Message Control Register 11	00h	
06F3Ch	CMCTL12_0	CAN_0 Message Control Register 12	00h	
06F3Dh	CMCTL13_0	CAN_0 Message Control Register 13	00h	
06F3Eh	CMCTL14_0	CAN_0 Message Control Register 14	00h	
06F3Fh	CMCTL15_0	CAN_0 Message Control Register 15	00h	
06F40h	CCTLR_0	CAN_0 Control Register	00000101b	
06F41h			00h	
06F42h	CSTR_0	CAN_0 Status Register	00000101b	
06F43h			00h	
06F44h	CBCR_0	CAN_0 Bit Configuration Register	00h	
06F45h			00h	
06F46h			00h	
06F47h	CCLKR_0	CAN_0 Clock Select Register	00h	
06F48h	CRFCR_0	CAN_0 Receive FIFO Control Register	10000000b	
06F49h	CRFPCR_0	CAN_0 Receive FIFO Pointer Control Register	XXh	
06F4Ah	CTFCR_0	CAN_0 Transmit FIFO Control Register	10000000b	
06F4Bh	CTFPCR_0	CAN_0 Transmit FIFO Pointer Control Register	XXh	
06F4Ch	CEIER_0	CAN_0 Error Interrupt Enable Register	00h	
06F4Dh	CEIFR_0	CAN_0 Error Interrupt Factor Judge Register	00h	
06F4Eh	CRECR_0	CAN_0 Receive Error Count Register	00h	
06F4Fh	CTECR_0	CAN_0 Transmit Error Count Register	00h	

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.22 SFR Information (22) (1)

Address	Symbol	Register Name	After Reset	Remarks
06F50h	CECSR_0	CAN_0 Error Code Store Register	00h	
06F51h	CCSSR_0	CAN_0 Channel Search Support Register	XXh	
06F52h	CMSSR_0	CAN_0 Mailbox Search Status Register	10000000b	
06F53h	CMSMR_0	CAN_0 Mailbox Search Mode Register	00h	
06F54h	CTSR_0	CAN_0 Time Stamp Register	0000h	
06F55h				
06F56h	CAFSR_0	CAN_0 Acceptance Filter Support Register	XXh	
06F57h			XXh	
06F58h	CTCR_0	CAN_0 Test Control Register	00h	
06F59h				
06F5Ah				
06F5Bh				
06F5Ch				
06F5Dh				
06F5Eh				
06F5Fh				
06F60h				
06F61h				
06F62h				
06F63h				
06F64h				
06F65h				
06F66h				
06F67h				
06F68h				
06F69h				
06F6Ah				
06F6Bh				
06F6Ch				
06F6Dh				
06F6Eh				
06F6Fh				
06F70h				
06F71h				
06F72h				
06F73h				
06F74h				
06F75h				
06F76h				
06F77h				
06F78h				
06F79h				
06F7Ah				
06F7Bh				
06F7Ch				
06F7Dh				
06F7Eh	CANISR_0	CAN_0 Interrupt Status Register	00h	
06F7Fh	CANIE_0	CAN_0 Interrupt Control Register	00h	
06F80h to 06FFFh				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.23 ID Code Area, Option Function Select Area

Address	Symbol	Area Name	After Reset	Address size
:				
0FFDBh	OFS2	Option Function Select Register 2	(Note 1)	
:				
0FFDFh	ID1		(Note 2)	
:				
0FFE3h	ID2		(Note 2)	
:				
0FFEBh	ID3		(Note 2)	
:				
0FFEFh	ID4		(Note 2)	
:				
0FFF3h	ID5		(Note 2)	
:				
0FFF7h	ID6		(Note 2)	
:				
0FFFBh	ID7		(Note 2)	
:				
0FFFFh	OFS	Option Function Select Register	(Note 1)	

Notes:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not perform any additional writes to the option function select area. Erasing the block including the option function select area sets the option function select area to FFh.
2. The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not perform any additional writes to the ID code area. Erasing the block including the ID code area sets the ID code area to FFh.

4. Bus Access

4.1 Bus Access

The number of bus cycles differs depending on the area accessed: ROM, RAM, DTC vector area, DTC control data, and SFR. For ROM and SFR, the restrictions on the number of access cycles differ depending on the CPU clock frequency. Thus the number must be set with the control registers (processor mode register (PM1) and flash control register (FMR2)).
Tables 4.1 and 4.2 list the Data Bus Widths and Bus Cycles for Accessing Different Areas for the R8C/54E Group, R8C/54F Group, R8C/54G Group, R8C/54H Group (with data flash).
Table 4.3 lists the settings for number of access cycles using control registers. Set the settings listed in this table according to the CPU clock frequency.
A part of SFR and data flash are connected to the CPU via an 8-bit bus. When these areas are accessed as word (16-bit) units, they are accessed twice in 8-bit units.

Table 4.1 Data Bus Widths and Bus Cycles for Accessing Different Areas (CPU Clock ≤ 20 MHz)

Access Target	Bus Width (bit)	Number of Wait Cycles	Number of Access Cycles		
			Byte Access	Word Access (even address)	Word Access (odd address)
SFR (00002h to 0003Fh)	8	1 wait state	2	4	4
SFR (1) (other than 00002h to 0003Fh)	16	1 wait state	2	2	4
RAM	16	0 wait state	1	1	2
Data flash	8	1 wait state	2	4	4
Program ROM	16	0 wait state	1	1	2

Note:
1. The number of cycles to write to the following registers is three wait states.
   • SSU/IIC: SISR
   • Timer RC: TRCSR
   • Timer RD: TRDSR0, TRDSR1

   The number of cycles to write to the SITDR register for the SSU/IIC is three wait states.
   However, the number of cycles to write to the SITDR register by DTC access is one wait state.

Table 4.2 Data Bus Widths and Bus Cycles for Accessing Different Areas (CPU Clock > 20 MHz)

Access Target (1)	Bus Width (bit)	Number of Wait Cycles	Number of Access Cycles		
			Byte Access	Word Access (even address)	Word Access (odd address)
SFR read (00002h to 0003Fh)	8	2 wait states	3	6	6
SFR write (00002h to 0003Fh)	8	1 wait state	2	4	4
SFR read (2) (other than 00002h to 0003Fh)	16	2 wait states	3	3	6
SFR write (2) (other than 00002h to 0003Fh)	16	1 wait state	2	2	4
RAM	16	0 wait state	1	1	2
Data flash	8	1 wait state	2	4	4
Program ROM (random access)	16	0 wait state	1	1	2
Program ROM (page access)	16	0 wait state	1	1	2

Notes:
1. When accessing the page space (for 16-byte address), page access is used. Otherwise, random access is used. Even when there are multiple accesses to areas other than program ROM, if the area accessed last and program ROM are in the same page space, page access is used.
2. The number of cycles to write to the following registers is three wait states.
   • SSU/IIC: SISR
   • Timer RC: TRCSR
   • Timer RD: TRDSR0, TRDSR1
   The number of cycles to write to the SITDR register for the SSU/IIC is three wait states.
   However, the number of cycles to write to the SITDR register by DTC access is one wait state.

Table 4.3 Settings for Wait Cycles for Accessing Different Areas

Access Target for Register Control Specification	Processor Mode Register 1 (PM1: Address 00005h)		Flash Control Register 2 (FMR2: Address 00256h)	
	PM17 = 1 (peripheral wait cycle is added)	PM17 = 0 (peripheral wait cycle is set to 1 wait state)	FMR24 = 1 (flash high-speed read disabled)	FMR24 = 0 (flash high-speed read enabled)
SFR read	2 wait states	1 wait state	No effect	No effect
SFR write	1 wait state	1 wait state	No effect	No effect
Data flash	No effect	No effect	1 wait state	3 wait states
Program ROM (random access)	No effect	No effect	0 wait state	1 wait state
Program ROM (page access)	No effect	No effect	0 wait state	0 wait state

5. System Control

5.1 Overview

This chapter describes system control functions, such as ID code checking, register access protection, and option functions.

5.2 Registers

Table 5.1 lists the Register Configuration for System Control.

Table 5.1 Register Configuration for System Control

Register Name	Symbol	After Reset	Address	Access Size
Processor Mode Register 0	PM0	00h	00004h	8
Processor Mode Register 1	PM1	10000000b	00005h	8
Protect Register	PRCR	00h	00007h	8
Option Function Select Register 2	OFS2	(Note 1)	0FFDBh	8
Option Function Select Register	OFS	(Note 2)	0FFFFh	8

Notes:
1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform any additional writes to the OFS2 register. Erasing the block including the OFS2 register sets the OFS2 register to FFh.
2. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform any additional writes to the OFS register. Erasing the block including the OFS register sets the OFS register to FFh.

5.2.1 Processor Mode Register 0 (PM0)

Address 00004h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PM03	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			
b2	—			
b3	PM03	Software reset bit	0: State is retained 1: Reset is generated	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM0 register.

PM03 Bit (Software reset bit)

When the PM03 bit is set to 1, the entire MCU is reset. The read value is 0.

5.2.2 Processor Mode Register 1 (PM1)

Address 00005h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PM17	—	—	—	—	—	—	—
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	PM17	Bus cycle wait bit (1)	0: Peripheral wait cycle is set to 1 wait state 1: Peripheral wait cycle is added	R/W

Note:

1. Refer to **Table 4.3 Settings for Wait Cycles for Accessing Different Areas**.
   - Set PM17 = 0 or 1 when the CPU clock ≤ 20 MHz.
   - Maintain PM17 = 1 when the CPU clock > 20 MHz.

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM0 register.

5.2.3 Protect Register (PRCR)

Address 00007h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PRC3	PRC2	PRC1	PRC0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	0: Disabled 1: Enabled (1)	R/W
b1	PRC1	Protect bit 1		R/W
b2	PRC2	Protect bit 2	0: Disabled 1: Enabled (2)	R/W
b3	PRC3	Protect bit 3	0: Disabled 1: Enabled (1)	R/W
b4	—	Reserved	Set to 0.	R/W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	—			
b7	—			

Notes:
1. Once this bit is set to 1, writing remains enabled until it is set to 0 by a program.
2. The PRC2 bit is set to 0 after setting it to 1 (write enabled) and writing to the SFR area. The registers protected by the PRC2 bit must be changed by the instruction after that used to set the PRC2 bit to 1. Interrupts and DTC activation must be disabled between the instruction to set to the PRC2 bit to 1 and the next instruction.

PRC0 Bit (Protect bit 0)

This bit enables/disables writing to registers CM0, CM1, CM3, CM4, OCD, FRA0, FRA2, PLC0, and PCLKR1.

PRC1 Bit (Protect bit 1)

This bit enables/disables writing to registers PM0, PM1, and RISR.

PRC2 Bit (Protect bit 2)

This bit enables/disables writing to the PD0 register.

PRC3 Bit (Protect bit 3)

This bit enables/disables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, VW2C, and SVDC.

5.2.4 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bits	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acceptance period set bits	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not perform any additional writes to the OFS2 register. Erasing the block including the OFS2 register sets the OFS2 register to FFh. The value of the OFS2 register is FFh at shipment of blank products. After programming, the value is the same as that programmed by the user. At shipment of factory-programmed products, the value of the OFS2 register is the same as that set in a program by the user.

   For an example of the OFS2 register settings, refer to **5.6.1 Option Function Select Area Setting Examples**.

Bits WDTRCS0 and WDTRCS1 (Watchdog timer refresh acceptance period set bits)

These bits are used to select the refresh acceptance period as a percentage. Note that the period from the start of counting to underflow is 100%.
For details, refer to **8.3.1.1 Refresh Acceptance Period**.

5.2.5 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bits (2)	b5 b4 0 0: 3.80 V (typ.) selected (Vdet0_3) 0 1: 2.85 V (typ.) selected (Vdet0_2) Other than the above: Do not set.	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not perform any additional writes to the OFS register. Erasing the block including the OFS register sets the OFS register to FFh. The value of the OFS register is FFh at shipment of blank products. After programming, the value is the same as that programmed by the user. At shipment of factory-programmed products, the value of the OFS register is the same as that set in a program by the user.
2. The same voltage detection 0 level selected by bits VDSEL0 and VDSEL1 is set in both the voltage monitor 0 reset and power-on reset functions.
3. Set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset) to use the power-on reset or voltage monitor 0 reset.

For an example of the OFS register settings, refer to **5.6.1 Option Function Select Area Setting Examples**.

LVDAS Bit (Voltage detection 0 circuit start bit)

The Vdet0 voltage monitored in the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

5.3 ID Code Area

5.3.1 Overview

The ID code area is assigned to certain of the highest addresses for each vector in the fixed vector table, 0FFDFh, 0FFE3h, 0FFEBh, 0FFEFh, 0FFF3h, 0FFF7h, and 0FFFBh.
Figure 5.1 shows the ID Code Area.

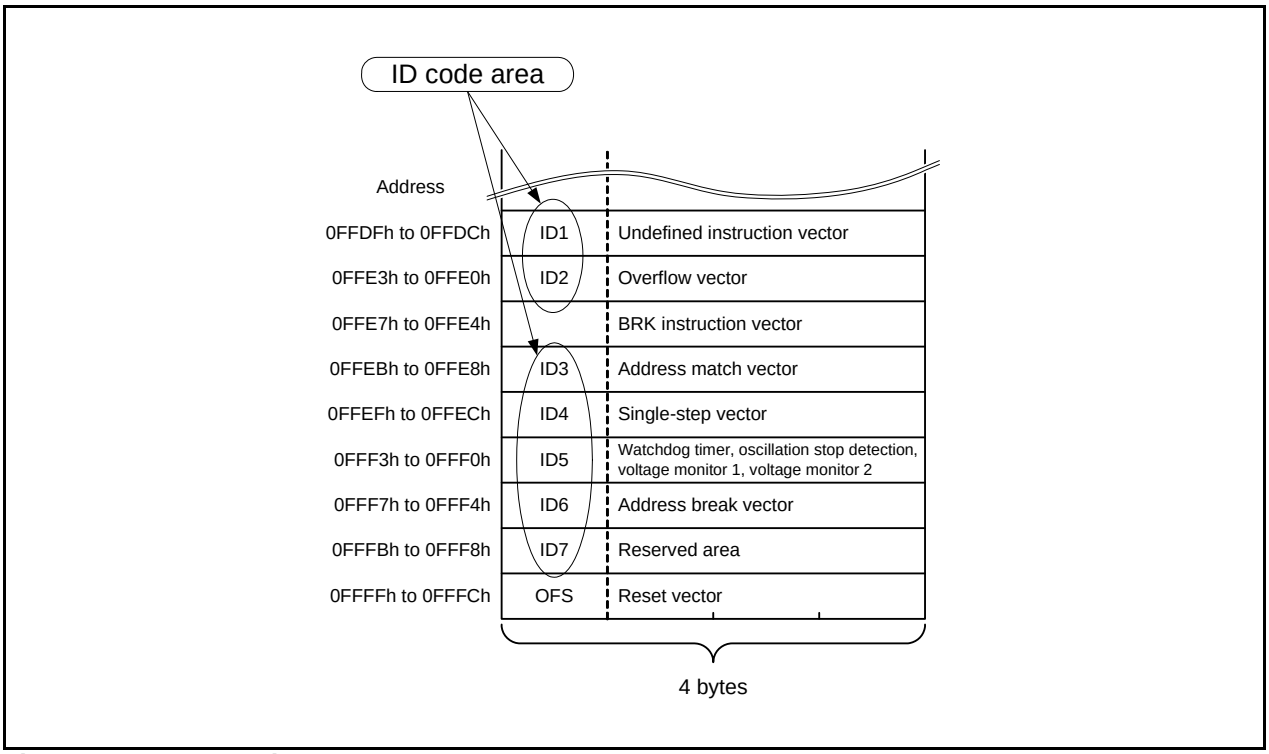


Figure 5.1 ID Code Area

5.3.2 Function

The ID code area is used in standard serial I/O mode. Its operation differs depending on whether the 3 bytes in the reset vector at addresses 0FFFCh to 0FFFEh are FFFFFFh or not.
If the value is not FFFFFFh in standard serial I/O mode, the ID code stored in the ID code area (stored ID code) and that sent from the serial programmer or the on-chip debugging emulator are examined to see whether they match. If they match, the commands are accepted. Otherwise, the commands are not accepted. To use the serial programmer or the on-chip debugging emulator, write predetermined ID codes, in advance, to the ID code area. If the value is FFFFFFh, the ID codes are not examined and all commands are accepted.
The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
The ID code with the character combination expressed “ALeRASE” in ASCII is the reserved word for the forced erase function. The ID code “Protect” is the reserved word for the standard serial I/O mode disabled function.
Table 5.2 lists the ID Code Reserved Word. When the combination of ID codes and addresses match those listed in Table 5.2 respectively, the ID codes form the corresponding reserved word. When the forced erase function or standard serial I/O mode disabled function is not used, use another combination of ID codes.

Table 5.2 ID Code Reserved Word

ID Code Storage Address		ID Code Reserved Word (ASCII) (1)	
		ALeRASE (Forced Erase Function)	Protect (Standard Serial I/O Mode Disabled Function)
0FFDFh	ID1	41h (upper-case “A”)	50h (upper-case “P”)
0FFE3h	ID2	4Ch (upper-case “L”)	72h (lower-case “r”)
0FFEBh	ID3	65h (lower-case “e”)	6Fh (lower-case “o”)
0FFEFh	ID4	52h (upper-case “R”)	74h (lower-case “t”)
0FFF3h	ID5	41h (upper-case “A”)	65h (lower-case “e”)
0FFF7h	ID6	53h (upper-case “S”)	63h (lower-case “c”)
0FFFBh	ID7	45h (upper-case “E”)	74h (lower-case “t”)

Note:
1. When the combination of ID codes and addresses match those listed in Table 5.2 respectively, the ID codes form the corresponding reserved word.

5.3.3 Forced Erase Function

The forced erase function is used in standard serial I/O mode. When the ID code sent from the serial programmer or the on-chip debugging emulator is the ASCII code “ALeRASE”, the entire data in the user ROM area will be erased. However, if the stored ID codes are any value other than “ALeRASE” (refer to **Table 5.2 ID Code Reserved Word**) and when the ROMCR bit is 1 and the ROMCP1 bit is 0 (ROM code protect enabled) in the OFS register, a forced erase is not performed and the ID codes are examined with the ID code check function. Table 5.3 lists the Conditions and Operations of Forced Erase Function.

Also, when the stored ID codes are set to “ALeRASE” in ASCII, if the ID codes sent from the serial programmer or the on-chip debugging emulator are “ALeRASE”, the data in the user ROM area will be erased. For ID codes other than “ALeRASE”, the ID codes do not match and no command is accepted, and thus the user ROM area remains protected.

Table 5.3 Conditions and Operations of Forced Erase Function

Condition			Operation
ID code from serial programmer or on-chip debugging emulator	ID code in ID code storage address	Bits ROMCP1 and ROMCR in OFS register	
ALeRASE	ALeRASE	—	Erasure of whole user ROM area (forced erase function)
	Other than ALeRASE (1)	Other than 01b (ROM code protect disabled)	
		01b (ROM code protect enabled)	ID code check (ID code check function)
Other than ALeRASE	ALeRASE	—	ID code check (ID code check function. No ID code match.)
	Other than ALeRASE (1)	—	ID code check (ID code check function)

Note:
1. Refer to **5.3.4 Standard Serial I/O Mode Disabled Function** for the case where the ID code is “Protect”.

5.3.4 Standard Serial I/O Mode Disabled Function

The standard serial I/O mode disabled function is used in standard serial I/O mode. When an ID code is “Protect” in ASCII (refer to **Table 5.2 ID Code Reserved Word**), no communication with the serial programmer or the on-chip debugging emulator is performed. This prevents the flash memory from being read, written, or erased using the serial programmer or the on-chip debugging emulator.
If the ID code is set to “Protect” in ASCII when the ROMCR bit is 1 and the ROMCP1 bit is 0 (ROM code protect enabled) in the OFS register, ROM code protection cannot be disabled using the serial programmer or the on-chip debugging emulator. This prevents the flash memory from being read, written, or erased using the serial programmer, the on-chip debugging emulator, or the parallel programmer.

5.3.5 Notes on ID Code Area (Setting Example)

The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

• To set 55h in all of the ID code area

```
.org 00FFDCH
.lword dummy | (55000000h)      ; UND
.lword dummy | (55000000h)      ; INTO
.lword dummy                    ; BREAK
.lword dummy | (55000000h)      ; ADDRESS MATCH
.lword dummy | (55000000h)      ; SET SINGLE STEP
.lword dummy | (55000000h)      ; WDT
.lword dummy | (55000000h)      ; ADDRESS BREAK
.lword dummy | (55000000h)      ; RESERVE
```

Programming formats vary depending on the compiler. Check the compiler manual.

5.4 Protection

The protection function protects important registers from being easily rewritten if a program runs out of control. The following registers are protected by the PRCR register.

Table 5.4 PRCR Register Bits and Registers Protected

Bit	Register Protected
PRC0	Registers CM0, CM1, CM3, CM4, OCD, FRA0, FRA2, PLC0, and PCLKR1
PRC1	Registers PM0, PM1, and RISR
PRC2	PD0 register
PRC3	Registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, VW2C, and SVDC

5.5 Option Function Select Area

5.5.1 Overview

The option function select area allows the user to select the MCU state after a reset and to disable rewriting in parallel I/O mode.
This area is allocated at addresses 0FFFFh (highest of the reset vector in the fixed vector table) and address 0FFDBh.
Figure 5.2 shows the Option Function Select Area.

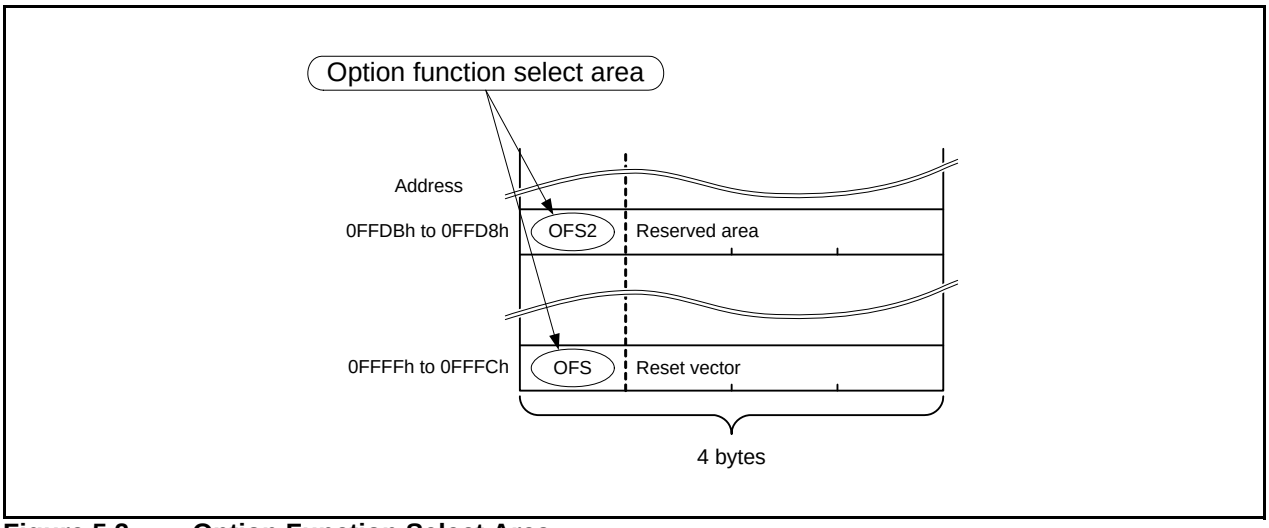


Figure 5.2 Option Function Select Area

5.6 Notes on System Control

5.6.1 Option Function Select Area Setting Examples

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows setting examples.

• To set FFh in the OFS2 register

```
.org 00FFDBH
.byte 0FFh
```

Programming formats vary depending on the compiler. Check the compiler manual.

• To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h)          ; RESET
```

Programming formats vary depending on the compiler. Check the compiler manual.

6. Resets

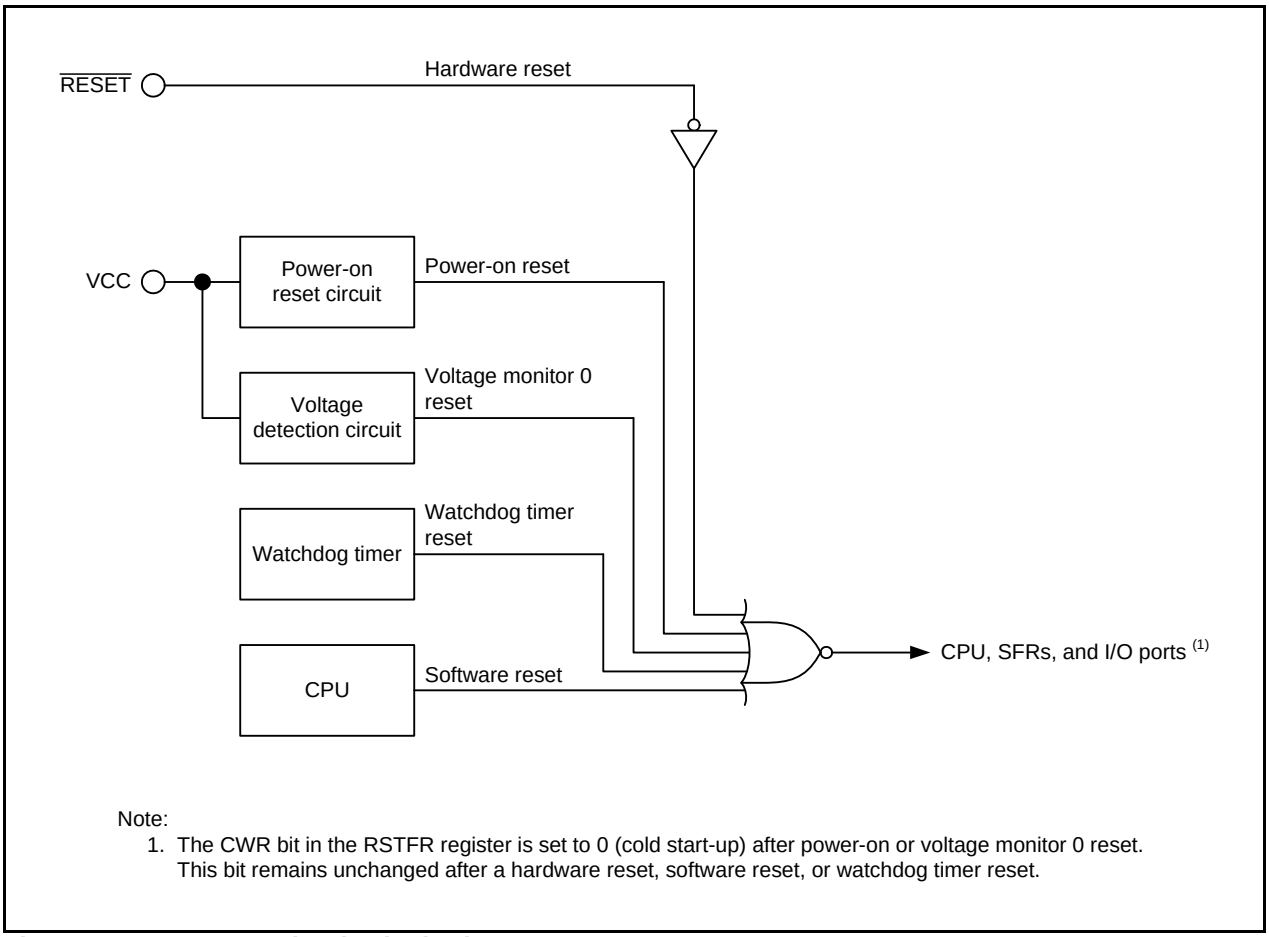
The following resets are provided: hardware reset, power-on reset, voltage monitor 0 reset triggered by the voltage detection circuit, watchdog timer reset, and software reset.

6.1 Overview

Table 6.1 lists the Reset Names and Sources and Figure 6.1 shows the Reset Circuit Block Diagram.

Table 6.1 Reset Names and Sources

Reset Name	Source
Hardware reset	When a low level is applied to the $\overline{\text{RESET}}$ pin.
Power-on reset	When VCC is turned on.
Voltage monitor 0 reset	When VCC falls below Vdet0, which is detected by voltage detection circuit 0.
Watchdog timer reset	When the watchdog timer underflows.
Software reset	When 1 is written to the PM03 bit in the PM0 register by a program.



Note:
1. The CWR bit in the RSTFR register is set to 0 (cold start-up) after power-on or voltage monitor 0 reset. This bit remains unchanged after a hardware reset, software reset, or watchdog timer reset.

Figure 6.1 Reset Circuit Block Diagram

6.2 Registers

Table 6.2 lists the Register Configuration for Reset.

Table 6.2 Register Configuration for Reset

Register Name	Symbol	After Reset	Address	Access Size
Processor Mode Register 0	PM0	00h	00004h	8
Reset Source Determination Register	RSTFR	00XXXXXXb	00028h	8
Option Function Select Register 2	OFS2	(Note 1)	0FFDBh	8
Option Function Select Register	OFS	(Note 2)	0FFFFh	8

Notes:
1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform any additional writes to the OFS2 register. Erasing the block including the OFS2 register sets the OFS2 register to FFh.
2. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform any additional writes to the OFS register. Erasing the block including the OFS register sets the OFS register to FFh.

6.2.1 Processor Mode Register 0 (PM0)

Address 00004h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PM03	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			
b2	—			
b3	PM03	Software reset bit	0: State is retained 1: Reset is generated	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM0 register.

PM03 Bit (Software reset bit)

When the PM03 bit is set to 1, the entire MCU is reset. The read value is 0.

6.2.2 Reset Source Determination Register (RSTFR)

Address 00028h

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	WDR	SWR	HWR	CWR	
After Reset	0	0	X	X	X	X	X	X	(Note 1)

Bit	Symbol	Bit Name	Function	R/W
b0	CWR	Cold start-up/warm start-up determine flag (2, 3)	0: Cold start-up 1: Warm start-up	R/W
b1	HWR	Hardware reset detect flag	0: Not detected 1: Detected	R
b2	SWR	Software reset detect flag		R
b3	WDR	Watchdog timer reset detect flag		R
b4	—	Reserved	The read value is undefined.	R
b5	—			
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

Notes:
1. The CWR bit is set to 0 (cold start-up) after power-on or voltage monitor 0 reset. This bit remains unchanged after a hardware reset, software reset, or watchdog timer reset.
2. The CWR bit is set to 1 by writing 1 by a program. (Writing 0 to this bit has no effect.)
3. When the VW0C0 bit in the VW0C register is 0 (voltage monitor 0 reset disabled), the CWR bit is undefined.

6.2.3 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bits	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acceptance period set bits	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not perform any additional writes to the OFS2 register. Erasing the block including the OFS2 register sets the OFS2 register to FFh. The value of the OFS2 register is FFh at shipment of blank products. After programming, the value is the same as that programmed by the user. At shipment of factory-programmed products, the value of the OFS2 register is the same as that set in a program by the user.

   For an example of the OFS2 register settings, refer to **5.6.1 Option Function Select Area Setting Examples**.

Bits WDTRCS0 and WDTRCS1 (Watchdog timer refresh acceptance period set bits)

These bits are used to select the refresh acceptance period as a percentage. Note that the period from the start of counting to underflow is 100%.
For details, refer to **8.3.1.1 Refresh Acceptance Period**.

6.2.4 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bits (2)	b5 b4 0 0: 3.80 V (typ.) selected (Vdet0_3) 0 1: 2.85 V (typ.) selected (Vdet0_2) Other than the above: Do not set.	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not perform any additional writes to the OFS register. Erasing the block including the OFS register sets the OFS register to FFh. The value of the OFS register is FFh at shipment of blank products. After programming, the value is the same as that programmed by the user. At shipment of factory-programmed products, the value of the OFS register is the same as that set in a program by the user.
2. The same voltage detection 0 level selected by bits VDSEL0 and VDSEL1 is set in both the voltage monitor 0 reset and power-on reset functions.
3. Set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset) to use the power-on reset or voltage monitor 0 reset.

For an example of the OFS register settings, refer to **5.6.1 Option Function Select Area Setting Examples**.

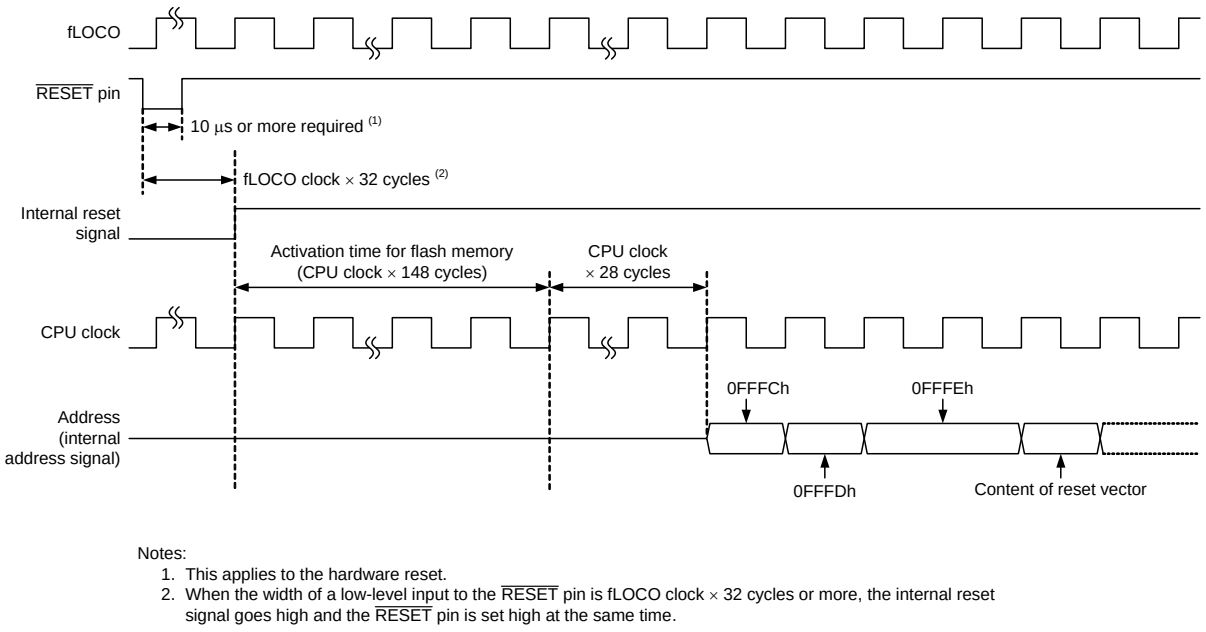
LVDAS Bit (Voltage detection 0 circuit start bit)

The Vdet0 voltage monitored in the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

6.3 Operation

6.3.1 Reset Sequence

Figure 6.2 shows the Reset Sequence using a hardware reset as an example. When the internal reset signal is cleared, the CPU starts operation from the reset vector (addresses 0FFFCh to 0FFFEh) after a predetermined time has elapsed.



Notes:
1. This applies to the hardware reset.
2. When the width of a low-level input to the RESET pin is fLOCO clock × 32 cycles or more, the internal reset signal goes high and the RESET pin is set high at the same time.

Figure 6.2 Reset Sequence

6.3.2 Hardware Reset

The hardware reset is the reset that is caused by the $\overline{\text{RESET}}$ pin. When a low level is applied to the $\overline{\text{RESET}}$ pin under the condition that the supply voltage meets the recommended operating conditions, the CPU, SFRs, and I/O ports are initialized (refer to **Table 6.3 Pin States while $\overline{\text{RESET}}$ Pin Level is Low**, **Figure 6.8 CPU Register States after Reset**, and **Tables 3.1** to **3.22 SFR Information**).
When the $\overline{\text{RESET}}$ pin is changed from low to high, a program is executed starting at the address indicated by the reset vector. The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after a reset.
For the states of the SFRs after a reset, refer to **3.5 Special Function Registers (SFRs)**.
The internal RAM is not initialized. If the $\overline{\text{RESET}}$ pin is set to low while writing to the internal RAM, the RAM values will be undefined.

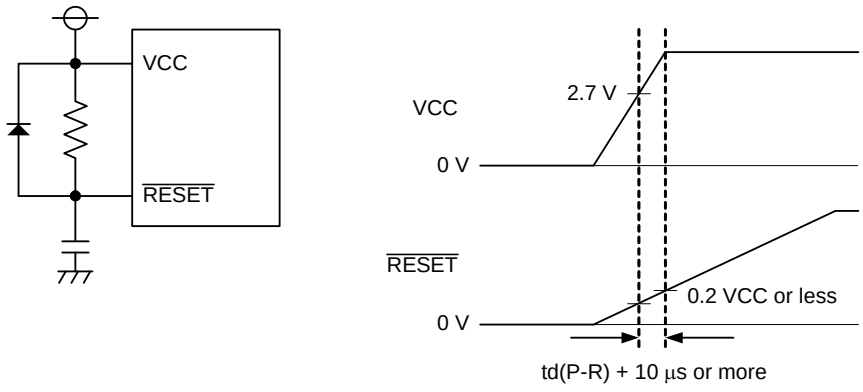
Figure 6.3 shows the Hardware Reset Circuit Example and Operation. Figure 6.4 shows the Hardware Reset Circuit Example (Using External Supply Voltage Detection Circuit) and Operation.

6.3.2.1 When Power Supply is Stable

(1) Apply a low level to the $\overline{\text{RESET}}$ pin.
(2) Wait for 10 µs.
(3) Apply a high level to the $\overline{\text{RESET}}$ pin.

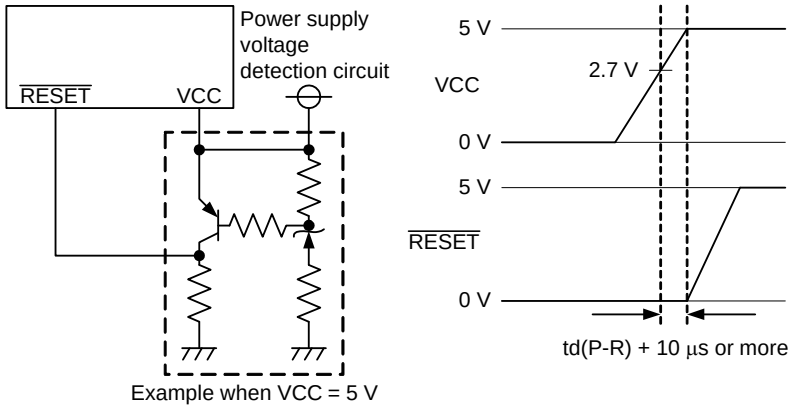
6.3.2.2 When Power Supply is Turned on

(1) Apply a low level to the $\overline{\text{RESET}}$ pin.
(2) Let the supply voltage increase until it meets the recommended operating conditions.
(3) Wait for td(P-R) until the internal power supply is stabilized (refer to **30. Electrical Characteristics**).
(4) Wait for 10 µs.
(5) Apply a high level to the $\overline{\text{RESET}}$ pin.



Note:
1. Refer to the **Electrical Characteristics** chapter.

Figure 6.3 Hardware Reset Circuit Example and Operation



Note:
1. Refer to the **Electrical Characteristics** chapter.

Figure 6.4 Hardware Reset Circuit Example (Using External Supply Voltage Detection Circuit) and Operation

6.3.3 Power-On Reset

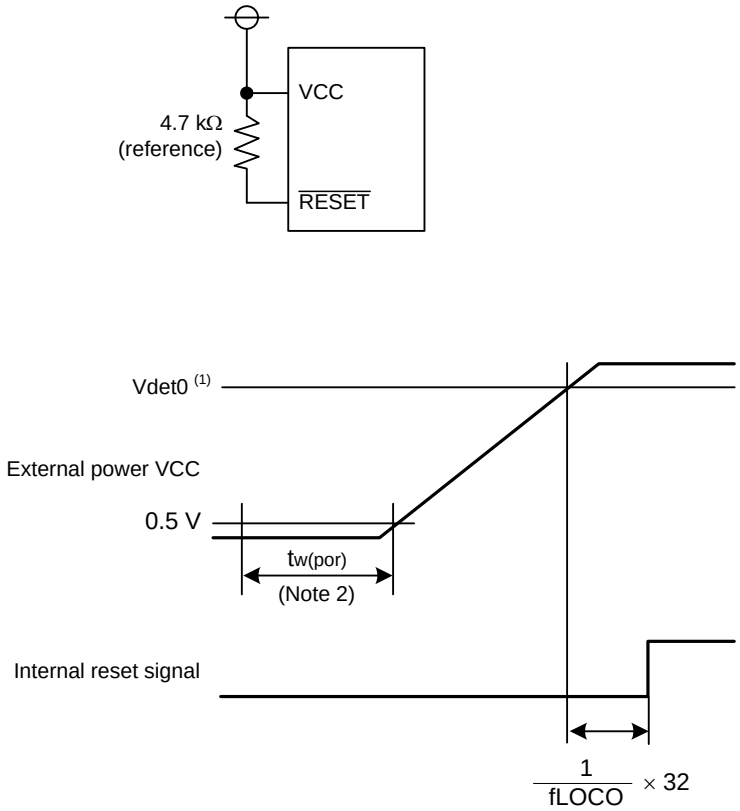
When the $\overline{\text{RESET}}$ pin is connected to the VCC pin via a resistor and the VCC pin voltage level rises, the power-on reset is activated and the CPU, SFRs, and I/O ports are initialized. The internal RAM values will be undefined. In addition, when a capacitor is connected to the $\overline{\text{RESET}}$ pin, ensure that the voltage applied to the $\overline{\text{RESET}}$ pin is always 0.8 VCC or more.

When the voltage applied to the VCC pin reaches Vdet0 or above, the low-speed on-chip oscillator clock count starts. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal goes high and the MCU proceeds to the reset sequence (refer to Figure 6.2). The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after a reset.

For the states of the SFRs after a reset, refer to **3.5 Special Function Registers (SFRs)**.

To use the power-on reset, set the LVDAS bit in the OFS register to 0 (voltage monitor 0 reset enabled) and enable the voltage monitor 0 reset.

Figure 6.5 shows the Power-On Reset Circuit Example and Operation.



Notes:
1. Vdet0 indicates the voltage detection level of the voltage detection 0 circuit. Refer to the **Voltage Detection Circuit** chapter for details.
2. tw(por) is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (0.5 V).
   When VCC falls with voltage monitor 0 reset disabled and then turns on, maintain tw(por) for 1 ms or more.
3. To use the power-on reset, enable the voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Figure 6.5 Power-On Reset Circuit Example and Operation

6.3.4 Voltage Monitor 0 Reset

The voltage monitor 0 reset is due to the on-chip voltage detection 0 circuit. The voltage detection 0 circuit monitors the voltage applied to the VCC pin. Vdet0 is the detection level. To use the voltage monitoring 0 reset, set the LVDAS bit in the OFS register to 0 (voltage monitoring 0 reset enabled after reset). The Vdet0 detection level can be changed by setting bits VDSEL0 and VDSEL1 in the OFS register.

When the input voltage to the VCC pin falls to the Vdet0 level or lower, the CPU, SFRs and I/O ports are initialized.

When the voltage applied to the VCC pin next rises to the Vdet0 level or higher, the low-speed on-chip oscillator clock count starts. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal goes high and the MCU proceeds to the reset sequence (refer to Figure 6.2). The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after a reset.

To use the power-on reset, set the LVDAS bit and enable the voltage monitor 0 reset.

Bits VDSEL0, VDSEL1, and LVDAS cannot be changed by a program. To set these bits, write values to b4 to b6 at address 0FFFFh using a flash programmer.

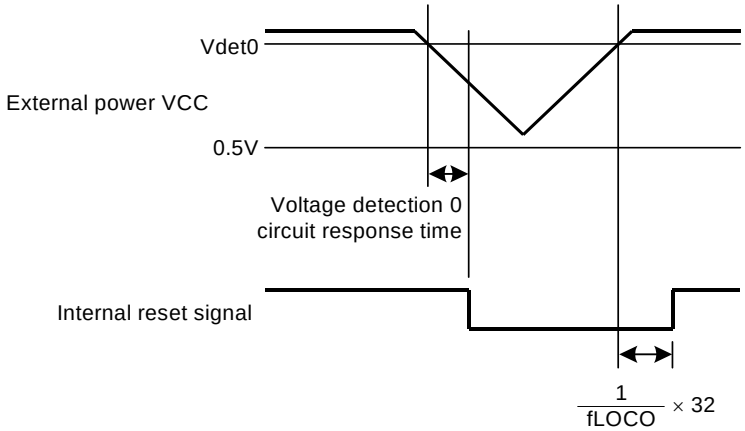
For details on the OFS register, refer to **6.2.4 Option Function Select Register (OFS)**.

For details on the states of the SFRs after a voltage monitor 0 reset, refer to **3.5 Special Function Registers (SFRs)**.

The internal RAM is not initialized. If the voltage applied to the VCC pin falls to Vdet0 or lower while writing to the internal RAM, the RAM values will be undefined.

For details on the voltage monitor 0 reset, refer to **7. Voltage Detection Circuit**.

Figure 6.6 shows the Voltage Monitor 0 Reset Circuit Example and Operation.



Notes:
1. Vdet0 indicates the voltage detection level of the voltage detection 0 circuit. For details, refer to the **Voltage Detection Circuit** chapter.
2. To use the power-on reset, enable the voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Figure 6.6 Voltage Monitor 0 Reset Circuit Example and Operation

6.3.5 Watchdog Timer Reset

When the RIS bit in the RISR register is 1 (watchdog timer reset enabled), if the watchdog timer underflows, the CPU, SFRs, and I/O ports are initialized. Next, the program located at the address indicated by the reset vector is executed. The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after a reset.
For the states of the SFR after a watchdog timer reset, refer to **3.5 Special Function Registers (SFRs)**.
The internal RAM is not initialized. When the watchdog timer underflows while writing to the internal RAM, the RAM values will be undefined.
The underflow period and refresh acceptance period for the watchdog timer are set by bits WDTUFS0 and WDTUFS1 and bits WDTRCS0 and WDTRCS1 in the OFS2 register, respectively.
For details on the watchdog timer, refer to **8. Watchdog Timer**.

6.3.6 Software Reset

When the PM03 bit in the PM0 register is 1 (MCU reset), the CPU, SFRs, and I/O ports are initialized. Next, the program located at the address indicated by the reset vector is executed. The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after a reset.
For the states of the SFRs after a software reset, refer to **3.5 Special Function Registers (SFRs)**.
The internal RAM is not initialized.

6.3.7 Cold Start-Up/Warm Start-Up Determination Function

The CWR bit in the RSTFR register is used to determine whether a cold start-up reset process was initiated at power-on, or whether a warm start-up reset process was initiated during operation.
The CWR bit is set to 0 (cold start-up) at power-on and also set to 0 by a voltage monitor 0 reset. If 1 is written to the CWR bit by a program, it is set to 1. This bit remains unchanged after a hardware reset, software reset, or watchdog timer reset.
The cold start-up/warm stat-up determination function uses the voltage monitor 0 reset.
Figure 6.7 shows an Example of Cold Start-Up/Warm Start-Up Function Operation.

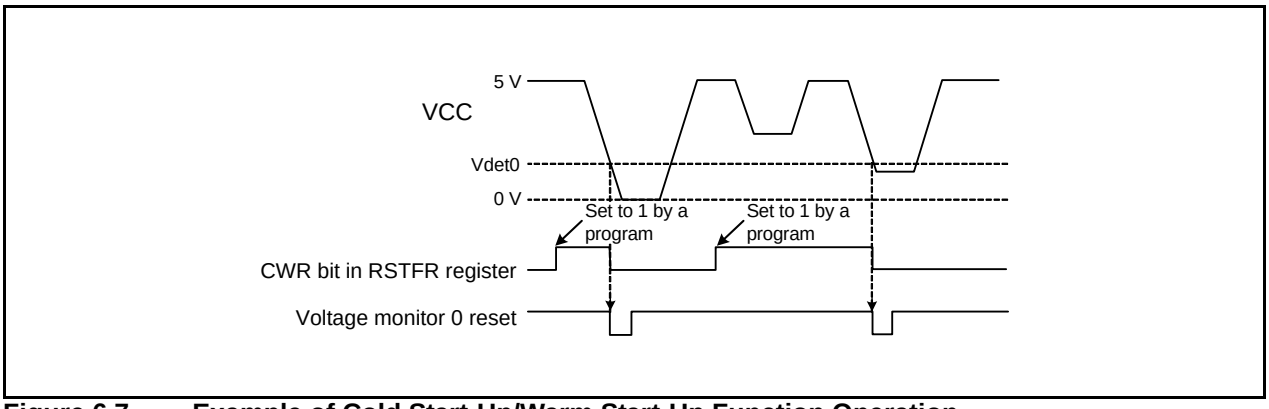


Figure 6.7 Example of Cold Start-Up/Warm Start-Up Function Operation

6.3.8 Reset Source Determination Function

The RSTFR register can be used to detect whether a hardware reset, software reset, or watchdog timer reset has occurred.
If a hardware reset occurs, the HWR bit in the RSTFR register is set to 1 (detected). If a software reset occurs, the SWR bit in the RSTFR register is set to 1 (detected). If a watchdog timer reset occurs, the WDR bit in the RSTFR register is set to 1 (detected).

6.4 States during Reset

6.4.1 Pin States while $\overline{\text{RESET}}$ Pin Level is Low

Table 6.3 lists the Pin States while $\overline{\text{RESET}}$ Pin Level is Low.

Table 6.3 Pin States while $\overline{\text{RESET}}$ Pin Level is Low

Pin Name	Pin Function
P0, P1, P2, P3_0, P3_1, P3_3 to P3_5, P3_7, P6, P9_4 to P9_7	Input port
P4_3 to P4_7	Input port

6.4.2 CPU Register States after Reset

Figure 6.8 shows the CPU Register States after Reset.

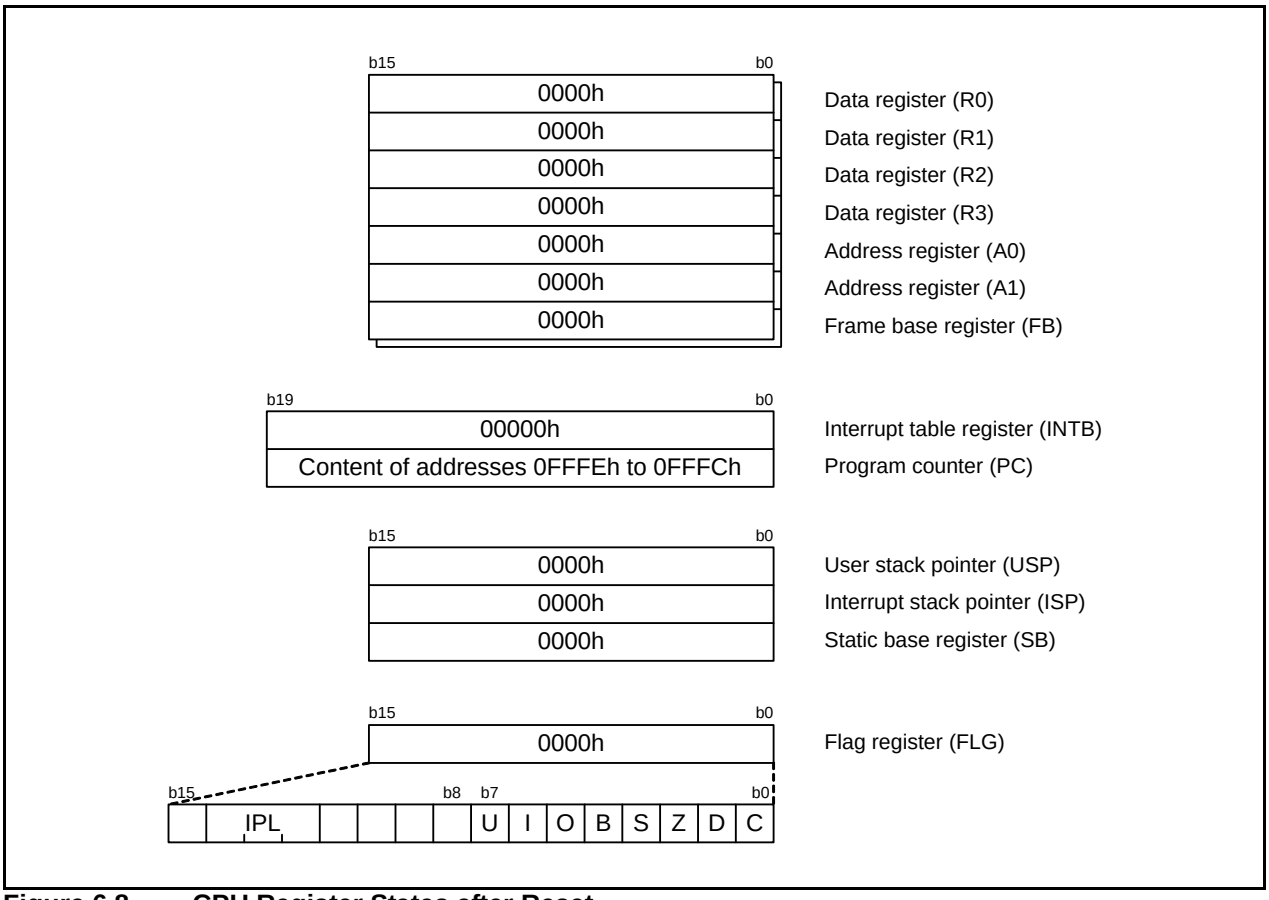


Figure 6.8 CPU Register States after Reset

6.5 Notes on Resets

6.5.1 RSTFR Register

When reading the RSTFR register successively twice or more, write 00h immediately before reading this register.

Program Example

```
MOV.B   #00H, 0028H     ; Write 00h to the RSTFR register (1)
MOV.B   0028H, A0       ; Store the read value of the RSTFR register into A0
```

Note:

1. The value of the CWR bit in the RSTFR register is not changed by writing 0.
   Also, the values of the other bits in this register are not affected because these bits are all read-only.

7. Voltage Detection Circuit

The voltage detection circuit is used to monitor the voltage applied to the VCC pin. The VCC input voltage can be monitored by a program.

7.1 Overview

The detection voltage for voltage detection 0 can be selected from two levels with the OFS register.
The detection voltage for voltage detection 1 can be selected from nine levels with the VD1LS register.
The voltage monitor 0 reset and voltage monitor 1 and 2 interrupts can be used.
Table 7.1 lists the Voltage Detection Circuit Specifications. Figure 7.1 shows the Voltage Detection Circuit Block Diagram. Figure 7.2 shows the Voltage Monitor 0 Reset Generation Circuit Block Diagram. Figure 7.3 shows the Voltage Monitor 1 Interrupt Generation Circuit Block Diagram. Figure 7.4 shows the Voltage Monitor 2 Interrupt Generation Circuit Block Diagram.

Table 7.1 Voltage Detection Circuit Specifications

Item		Voltage Monitor 0	Voltage Monitor 1	Voltage Monitor 2
VCC monitor	Voltage to be monitored	Vdet0	Vdet1	Vdet2
	Detection target	Whether passing through Vdet0 by falling	Whether passing through Vdet1 by rising or falling	Whether passing through Vdet2 by rising or falling
	Detection voltage	Selectable from 2 levels with the OFS register	Selectable from 9 levels with the VD1LS register	Fixed level
	Monitor	None	The VW1C3 bit in the VW1C register	The VW2C3 bit in the VW2C register
			Higher or lower than Vdet1	Higher or lower than Vdet2
Process at voltage detection	Reset	Voltage monitor 0 reset	None	None
		Reset at Vdet0 > VCC, CPU operation is restarted at VCC > Vdet0		
	Interrupts	None	Voltage monitor 1 interrupt	Voltage monitor 2 interrupt
			Non-maskable or maskable selectable	Non-maskable or maskable selectable
			Interrupt request at Vdet1 > VCC and/or VCC > Vdet1	Interrupt request at Vdet2 > VCC and/or VCC > Vdet2
Digital filter	Switching enabled/disabled	No digital filter function	Available	Available
	Sampling time	—	(fLOCO divided by n) × 2 n: 1, 2, 4, or 8	(fLOCO divided by n) × 2 n: 1, 2, 4, or 8

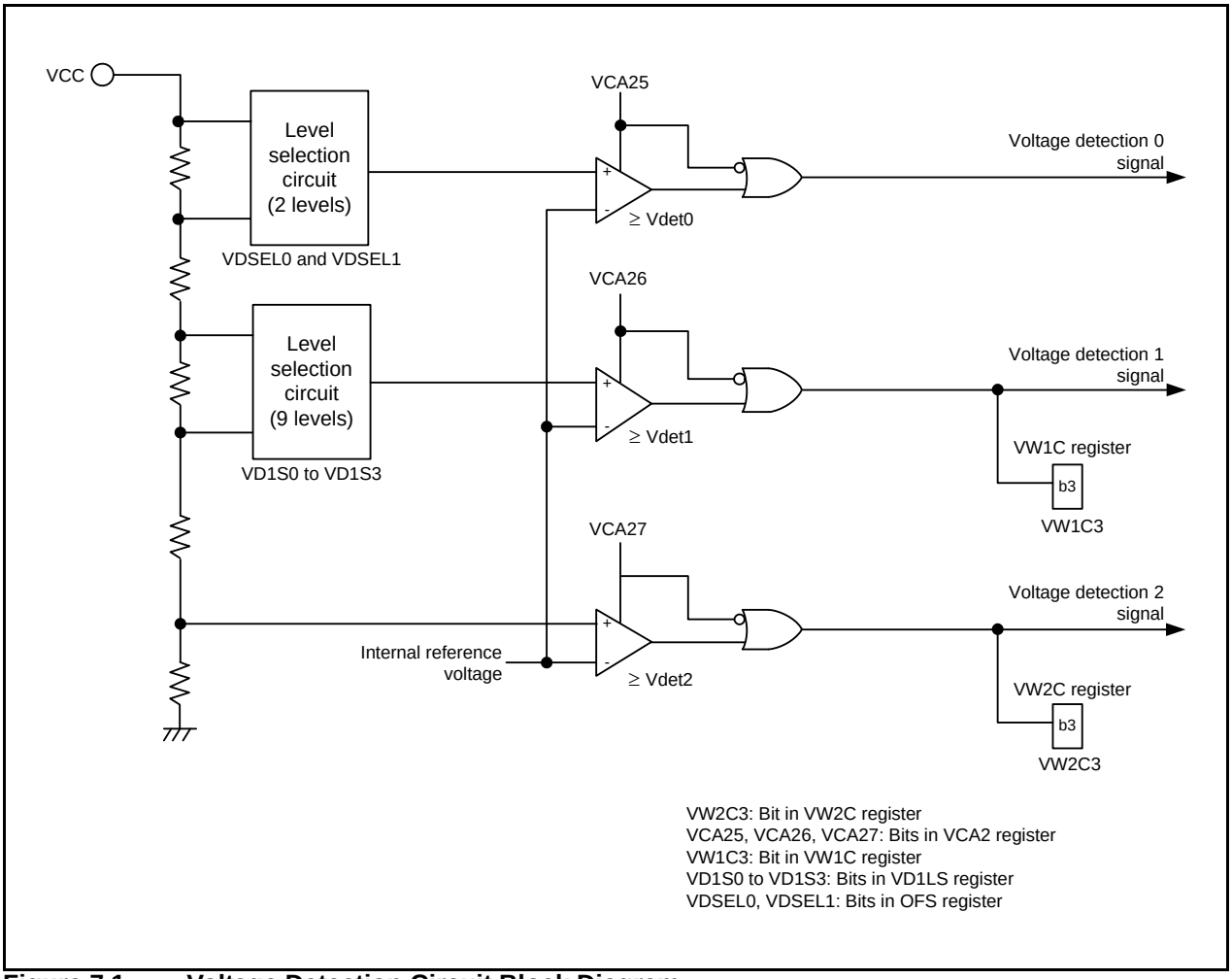


Figure 7.1 Voltage Detection Circuit Block Diagram

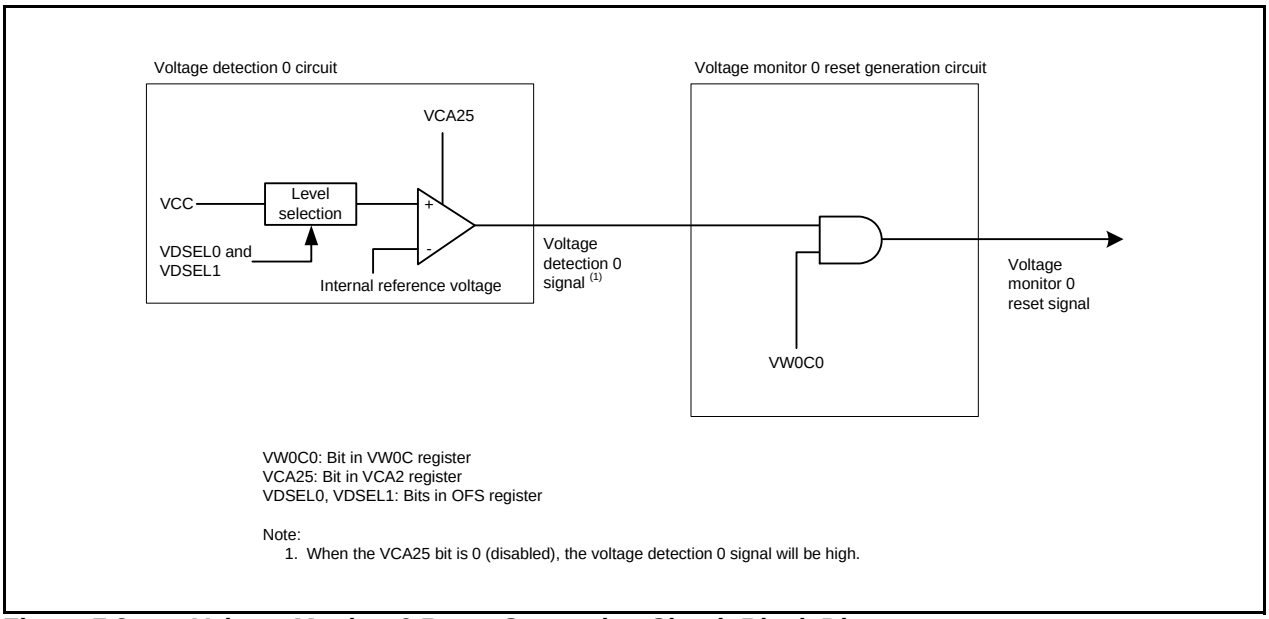
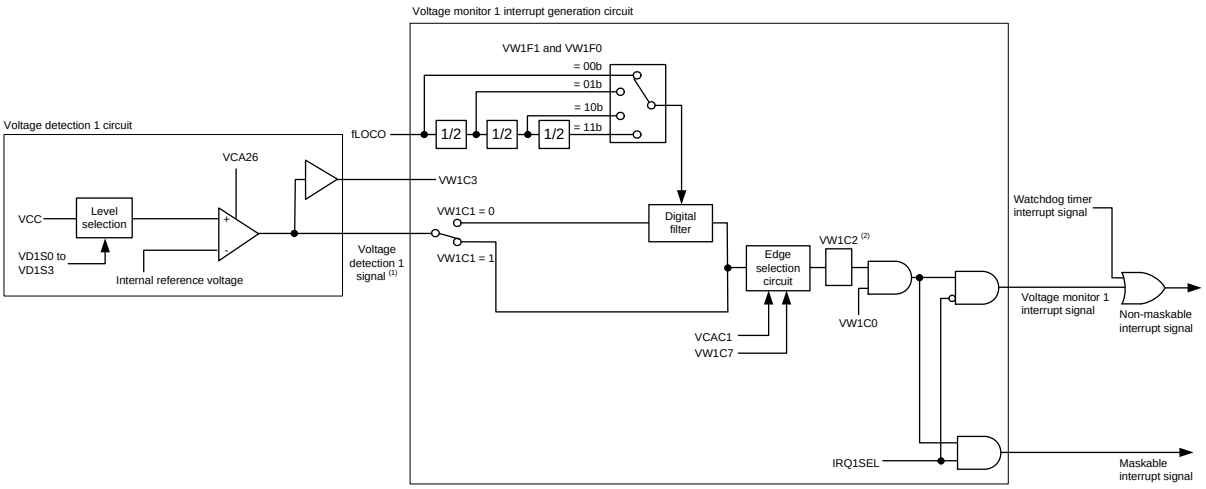


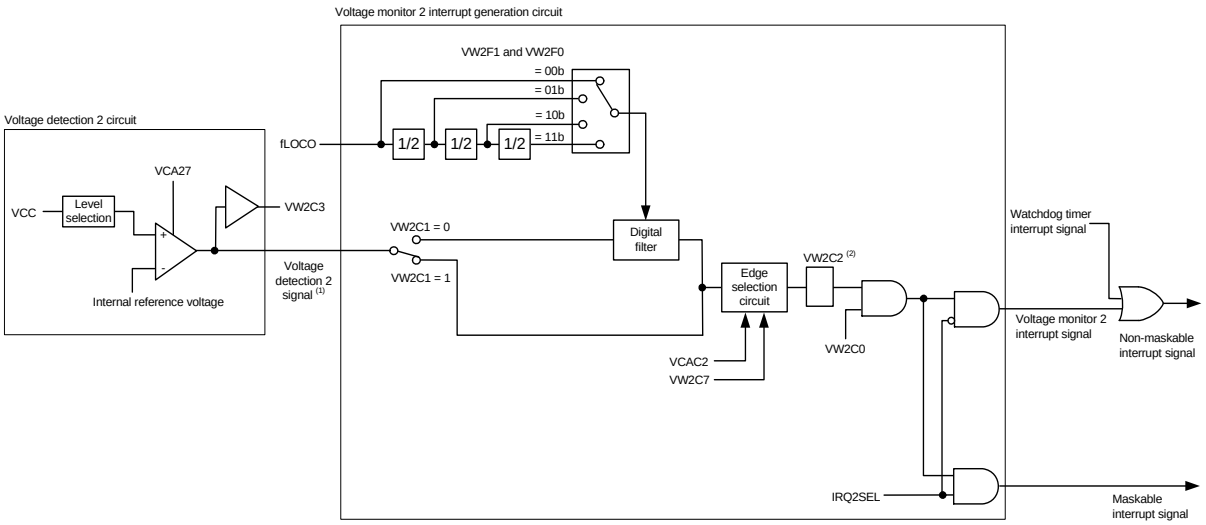
Figure 7.2 Voltage Monitor 0 Reset Generation Circuit Block Diagram



VW1C0 to VW1C3, VW1F0 to VW1F1, VW1C7: Bits in VW1C register
VCA26: Bit in VCA2 register
VD1S1 to VD1S3: Bits in VD1LS register
IRQ1SEL: Bit in COMPA register
VCAC1: Bit in VCAC register

Notes:
1. When the VCA26 bit is 0 (disabled), the voltage detection 1 signal will be high.
2. The VW1C2 bit is set to 0 by writing 0 (not detected) by a program. When the VCA26 bit is 0 (voltage detection 1 circuit disabled), the VW1C2 bit will be 0.

Figure 7.3 Voltage Monitor 1 Interrupt Generation Circuit Block Diagram



VW2C0 to VW2C3, VW2F0, VW2F1, VW2C7: Bits in VW2C register
VCA27: Bit in VCA2 register
IRQ2SEL: Bit in CMPA register
VCAC2: Bit in VCAC register

Notes:
1. When the VCA27 bit is 0 (disabled), the voltage detection 2 signal will be high.
2. The VW2C2 bit is set to 0 by Writing 0 (not detected) by a program. When the VCA27 bit is 0 (voltage detection 2 circuit disabled), the VW2C2 bit will be 0.

Figure 7.4 Voltage Monitor 2 Interrupt Generation Circuit Block Diagram

7.2 Registers

Table 7.2 lists the Voltage Detection Circuit Register Configuration.

Table 7.2 Voltage Detection Circuit Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Voltage Monitor Circuit Control Register	CMPA	00h	00030h	8
Voltage Monitor Circuit Edge Select Register	VCAC	00h	00031h	8
Voltage Detection Register 2	VCA2	00000000b or 00100000b (1)	00034h	8
Voltage Detection 1 Level Select Register	VD1LS	00000111b	00036h	8
Voltage Monitor 0 Circuit Control Register	VW0C	1100XX10b or 1100XX11b (1)	00038h	8
Voltage Monitor 1 Circuit Control Register	VW1C	10001010b	00039h	8
Voltage Monitor 2 Circuit Control Register	VW2C	10001010b	0003Ah	8
Option Function Select Register	OFS	(Note 2)	0FFFFh	8

Notes:
1. The value after reset differs depending on the LVDAS bit in the OFS register.
2. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform any additional writes to the OFS register. Erasing the block including the OFS register sets the OFS register to FFh.

7.2.1 Voltage Monitor Circuit Control Register (CMPA)

Address 00030h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	IRQ2SEL	IRQ1SEL	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	IRQ1SEL	Voltage monitor 1 interrupt type select bit	0: Non-maskable interrupt 1: Maskable interrupt	R/W
b5	IRQ2SEL	Voltage monitor 2 interrupt type select bit		R/W
b6	—	Reserved	Set to 0.	R/W
b7	—			

7.2.2 Voltage Monitor Circuit Edge Select Register (VCAC)

Address 00031h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	VCAC2	VCAC1	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	VCAC1	Voltage monitor 1 circuit edge select bit	0: One edge 1: Both edges	R/W
b2	VCAC2	Voltage monitor 2 circuit edge select bit		R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

7.2.3 Voltage Detection Register 2 (VCA2)

Address 00034h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VCA27	VCA26	VCA25	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is 1.

After Reset	0	0	1	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is 0.

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	—			
b5	VCA25	Voltage detection 0 enable bit (1)	0: Voltage detection 0 circuit disabled 1: Voltage detection 0 circuit enabled	R/W
b6	VCA26	Voltage detection 1 enable bit (2)	0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W
b7	VCA27	Voltage detection 2 enable bit (3)	0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled	R/W

Notes:
1. To use the voltage monitor 0 reset, set the VCA25 bit to 1.
2. To use the voltage detection 1 interrupt or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1. After the VCA26 bit is set from 0 to 1 and td(E-A) has elapsed, the voltage detection 1 circuit operates.
3. To use the voltage detection 2 interrupt or the VW2C3 bit in the VW2C register, set the VCA27 bit to 1. After the VCA27 bit is set from 0 to 1 and td(E-A) has elapsed, the voltage detection 2 circuit operates.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCA2 register.

7.2.4 Voltage Detection 1 Level Select Register (VD1LS)

Address 00036h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VD1S3	VD1S2	VD1S1	VD1S0
After Reset	0	0	0	0	0	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	VD1S0	Voltage detection 1 level select bits (Typical voltage when the voltage falls)	b3 b2 b1 b0 0 1 1 1: 3.25 V (Vdet1_7) 1 0 0 0: 3.40 V (Vdet1_8) 1 0 0 1: 3.55 V (Vdet1_9) 1 0 1 0: 3.70 V (Vdet1_A) 1 0 1 1: 3.85 V (Vdet1_B) 1 1 0 0: 4.00 V (Vdet1_C) 1 1 0 1: 4.15 V (Vdet1_D) 1 1 1 0: 4.30 V (Vdet1_E) 1 1 1 1: 4.45 V (Vdet1_F) Other than the above: Do not set.	R/W
b1	VD1S1			R/W
b2	VD1S2			R/W
b3	VD1S3			R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VD1LS register.

7.2.5 Voltage Monitor 0 Circuit Control Register (VW0C)

Address 00038h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	VW0C0
After Reset	1	1	0	0	X	X	1	0

The above applies when the LVDAS bit in the OFS register is 1.

After Reset	1	1	0	0	X	X	1	1

The above applies when the LVDAS bit in the OFS register is 0.

Bit	Symbol	Bit Name	Function	R/W
b0	VW0C0	Voltage monitor 0 reset enable bit (1)	0: Disabled 1: Enabled	R/W
b1	—	Reserved	Set to 1.	R/W
b2	—	Reserved	The read value is undefined.	R
b3	—			
b4	—	Reserved	Set to 0.	R/W
b5	—			
b6	—	Reserved	Set to 1.	R/W
b7	—			

Note:

1. The VW0C0 bit is enabled when the VCA25 bit in the VCA2 register is 1 (voltage detection 0 circuit enabled). The value written to the VW0C0 bit must be the value after reset.
   To set the VW0C0 bit to 1, follow the procedure below:
   (1) Set the VCA25 bit to 1
   (2) Wait for td(E-A) until the detection circuit operates.
   (3) Set the VW0C0 bit to 1.

   Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW0C register.

7.2.6 Voltage Monitor 1 Circuit Control Register (VW1C)

Address 00039h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VW1C7	—	VW1F1	VW1F0	VW1C3	VW1C2	VW1C1	VW1C0
After Reset	1	0	0	0	1	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	VW1C0	Voltage monitor 1 interrupt enable bit (1)	0: Disabled 1: Enabled	R/W
b1	VW1C1	Voltage monitor 1 digital filter mode select bit (2, 3)	0: Digital filter enabled mode (digital filter circuit enabled) 1: Digital filter disabled mode (digital filter circuit disabled)	R/W
b2	VW1C2	Voltage change detection flag (4, 5)	0: Not detected 1: Detected by passing through Vdet1	R/W
b3	VW1C3	Voltage detection 1 signal monitor flag (4)	0: VCC < Vdet1 1: VCC ≥ Vdet1 or voltage detection 1 circuit disabled	R
b4	VW1F0	Sampling clock select bits (3)	b5 b4 0 0: fLOCO divided by 1 0 1: fLOCO divided by 2 1 0: fLOCO divided by 4 1 1: fLOCO divided by 8	R/W
b5	VW1F1			R/W
b6	—	Reserved	Set to 0.	R/W
b7	VW1C7	Voltage monitor 1 interrupt generation condition select bit	0: VCC reaches Vdet1 or above 1: VCC reaches Vdet1 or below	R/W

Notes:
1. The VW1C0 bit is enabled when the VCA26 bit in the VCA2 register is 1 (voltage detection 1 circuit enabled). When the VCA26 bit is 0 (voltage detection 1 circuit disabled), set the VW1C0 bit to 0 (disabled). To set the VW1C0 bit to 1 (enabled), refer to **Table 7.3 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt**.
2. When the digital filter is used (the VW1C1 bit is 0), set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).
   When the voltage monitor 1 interrupt is used to exit stop mode, set the VW1C1 bit in the VW1C register to 1 (digital filter disabled mode).
3. When the VW1C0 bit is 1 (enabled), do not set bits VW1C1 and VW1F0 to VW1F1 at the same time (with one instruction).
4. Bits VW1C2 and VW1C3 are enabled when the VCA26 bit is 1 (voltage detection 1 circuit enabled).
5. Set to 0 by a program. This bit is set to 0 by writing 0 by a program, but writing 1 has no effect.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW1C register. Rewriting the VW1C register may set the VW1C2 bit to 1. Rewrite this register before setting the VW1C2 bit to 0.

7.2.7 Voltage Monitor 2 Circuit Control Register (VW2C)

Address 0003Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VW2C7	—	VW2F1	VW2F0	VW2C3	VW2C2	VW2C1	VW2C0
After Reset	1	0	0	0	1	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	VW2C0	Voltage monitor 2 interrupt enable bit (1)	0: Disabled 1: Enabled	R/W
b1	VW2C1	Voltage monitor 2 digital filter mode select bit (2, 3)	0: Digital filter enabled mode (digital filter circuit enabled) 1: Digital filter disabled mode (digital filter circuit disabled)	R/W
b2	VW2C2	Voltage change detection flag (4, 5)	0: Not detected 1: Detected by passing through Vdet2	R/W
b3	VW2C3	Voltage detection 2 signal monitor flag (5)	0: VCC < Vdet2 1: VCC ≥ Vdet2 or voltage detection 2 circuit disabled	R
b4	VW2F0	Sampling clock select bits (3)	b5 b4 0 0: fLOCO divided by 1 0 1: fLOCO divided by 2 1 0: fLOCO divided by 4 1 1: fLOCO divided by 8	R/W
b5	VW2F1			R/W
b6	—	Reserved	Set to 0.	R/W
b7	VW2C7	Voltage monitor 2 interrupt generation condition select bit	0: VCC reaches Vdet2 or above 1: VCC reaches Vdet2 or below	R/W

Notes:
1. The VW2C0 bit is enabled when the VCA27 bit in the VCA2 register is 1 (voltage detection 2 circuit enabled). When the VCA27 bit is 0 (voltage detection 2 circuit disabled), set the VW2C0 bit to 0 (disabled). To set the VW2C0 bit to 1 (enabled), refer to **Table 7.4 Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt**.
2. When the digital filter is used (the VW2C1 bit is 0), set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).
   When the voltage monitor 2 interrupt is used to exit stop mode, set the VW2C1 bit to 1 (digital filter disabled mode).
3. When the VW2C0 bit is 1 (enabled), do not set bits VW2C1 and VW2F0 to VW2F1 at the same time (with one instruction).
4. The VW2C2 bit is enabled when the VC27 bit is 1 (voltage detection 2 circuit enabled).
5. Set to 0 by a program. This bit is set to 0 by writing 0 by a program, but writing 1 has no effect.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW2C register. Rewriting the VW2C register may set the VW2C2 bit to 1. Rewrite this register before setting the VW2C2 bit to 0.

7.2.8 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bits (2)	b5 b4 0 0: 3.80 V (typ.) selected (Vdet0_3) 0 1: 2.85 V (typ.) selected (Vdet0_2) Other than the above: Do not set.	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not perform any additional writes to the OFS register. Erasing the block including the OFS register sets the OFS register to FFh. The value of the OFS register is FFh at shipment of blank products. After programming, the value is the same as that programmed by the user. At shipment of factory-programmed products, the value of the OFS register is the same as that set in a program by the user.
2. The same voltage detection 0 level selected by bits VDSEL0 and VDSEL1 is set in both the voltage monitor 0 reset and power-on reset functions.
3. Set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset) to use the power-on reset or voltage monitor 0 reset.

For an example of the OFS register settings, refer to **5.6.1 Option Function Select Area Setting Examples**.

LVDAS Bit (Voltage detection 0 circuit start bit)

The Vdet0 voltage monitored in the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

7.3 Monitoring VCC Input Voltage

7.3.1 Monitoring Vdet0

Vdet0 cannot be monitored.

7.3.2 Monitoring Vdet1

Make the following settings and wait for td(E-A) (refer to **30. Electrical Characteristics**). After that, the comparison result from voltage monitor 1 can be monitored with the VW1C3 bit in the VW1C register.

(1) Set bits VD1S0 to VD1S3 in the VD1LS register to select the detection voltage for voltage detection 1.
(2) Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).

7.3.3 Monitoring Vdet2

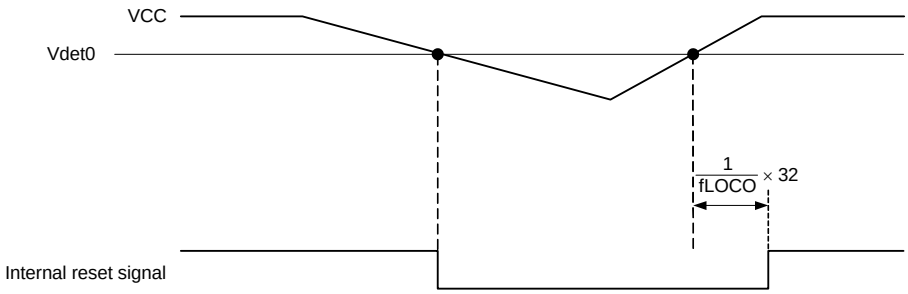
Make the following settings and wait for td(E-A) (refer to **30. Electrical Characteristics**). After that, the comparison result from voltage monitor 2 can be monitored with the VW2C3 bit in the VW2C register.

(1) Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled).

7.4 Voltage Monitor 0 Reset

To use the voltage monitoring 0 reset, set the LVDAS bit in the OFS register to 0 (voltage monitoring 0 reset enabled after reset).

Figure 7.5 shows an Example of Voltage Monitor 0 Reset Operation.



When the internal reset signal goes low, the CPU, SFRs, and I/O ports are initialized.
When the internal reset signal changes from low to high, program execution starts from the address indicated by the reset vector.
For the states of the SFRs, refer to the **Special Function Registers (SFRs)** section shown in the **Address Space** chapter.

Figure 7.5 Example of Voltage Monitor 0 Reset Operation

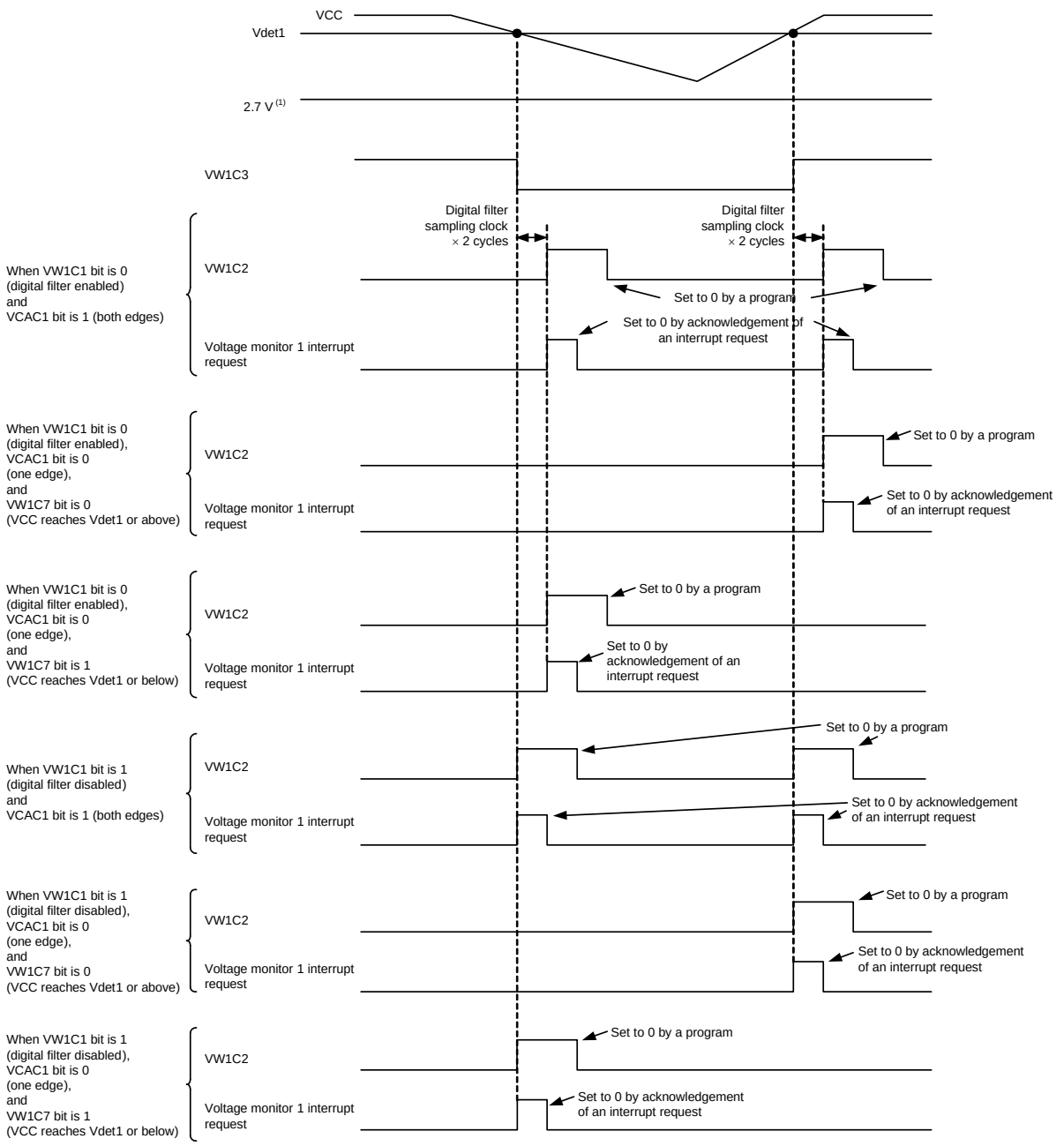
7.5 Voltage Monitor 1 Interrupt

Table 7.3 lists the Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt and Figure 7.6 shows an Example of Voltage Monitor 1 Interrupt Operation.
Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled mode) to use the voltage monitor 1 interrupt to exit stop mode.

Table 7.3 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt

Step	When Digital Filter is Used	When Digital Filter is Not Used
1	Set bits VD1S0 to VD1S3 in the VD1LS register to select the detection voltage for voltage detection 1.	
2	Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).	
3	Wait for td(E-A).	
4	Set the IRQ1SEL bit in the CMPA register to select the interrupt type.	
5 (1)	Set bits VW1F0 and VW1F1 in the VW1C register to select the sampling clock for the digital filter.	Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).
6 (1)	Set the VW1C1 bit in the VW1C register to 0 (digital filter enabled).	—
7 (1)	Set the VW1C7 bit in the VW1C register to select the timing for interrupt detection.	
8	Set the VCAC1 bit in the VCAC register to select the timing for interrupt detection.	
9	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).	—
10	Wait for 4 cycles of the sampling clock (2 cycles of the low-speed on-chip oscillator clock) of the digital filter.	— (No wait time)
11	Set the VW1C2 bit in the VW1C register to 0.	
12 (2)	Set the VW1C0 bit in the VW1C register to 1 (voltage monitor 1 interrupt enabled).	

Notes:
1. When the VW1C0 bit is 0, steps 5 to 7 can be performed at the same time (with one instruction).
2. When this setting is made with the voltage monitor 1 interrupt disabled (the VW1C0 bit is 0, the VCA26 bit is 0), if VCC < Vdet1 (or VCC > Vdet1) is detected, no interrupt is generated until the voltage monitor 1 interrupt in step 12 is enabled. If VCC < Vdet1 (or VCC > Vdet1) is detected between steps 11 and 12, the VW1C2 bit is set to 1. Read the VW1C2 bit after step 12, and perform the processing required for detection if the read value is 1.



VW1C1 to VW1C3, VW1C7: Bits in VW1C register
VCAC1: Bit in VCAC register

The above diagram applies under the following conditions:
- VCA26 bit in VCA2 register = 1 (voltage detection 1 circuit enabled)
- VW1C0 bit in VW1C register = 1 (voltage detection 1 interrupt enabled)

Note:
1. If voltage monitor 0 reset is not used, VCC must be at least 2.7 V.

Figure 7.6 Example of Voltage Monitor 1 Interrupt Operation

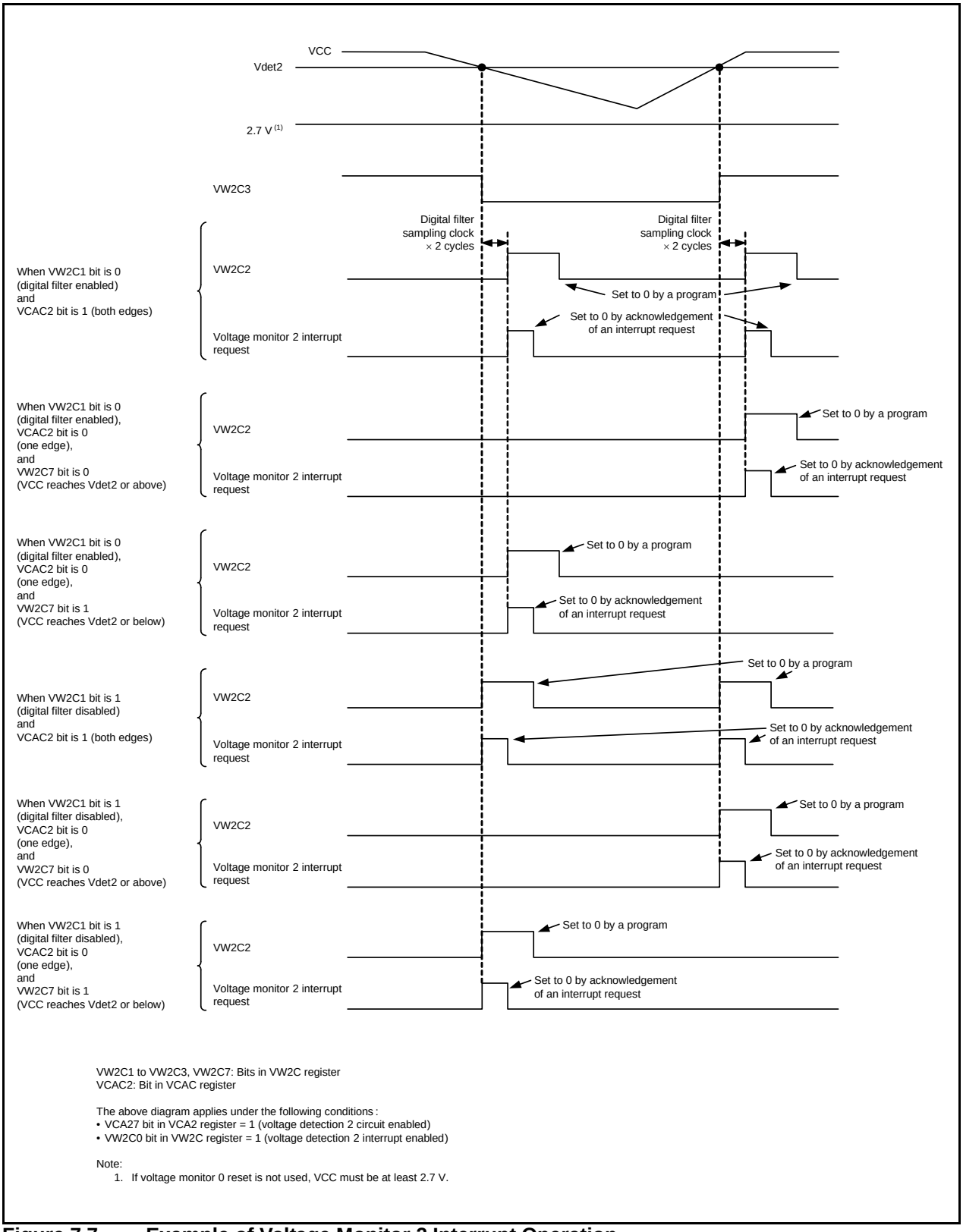
7.6 Voltage Monitor 2 Interrupt

Table 7.4 lists the Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt and Figure 7.7 shows an Example of Voltage Monitor 2 Interrupt Operation. When the voltage monitor 2 interrupt is used to exit stop mode, set the VW2C1 bit in the VW2C register to 1 (digital filter disabled mode).

Table 7.4 Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt

Step	When Digital Filter is Used	When Digital Filter is Not Used
1	Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled).	
2	Wait for td(E-A).	
3	Set the IRQ2SEL bit in the CMPA register to select the interrupt type.	
4 (1)	Set bits VW2F0 and VW2F1 in the VW2C register to select the sampling clock for the digital filter.	Set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).
5 (1)	Set the VW2C1 bit in the VW2C register to 0 (digital filter enabled).	—
6 (1)	Set the VW2C7 bit in the VW2C register to select the timing for interrupt detection.	
7	Set the VCAC2 bit in the VCAC register to select the timing for interrupt detection.	
8	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).	—
9	Wait for 4 cycles of the sampling clock (2 cycles of the low-speed on-chip oscillator clock) of the digital filter.	— (No wait time)
10	Set the VW2C2 bit in the VW2C register to 0.	
11 (2)	Set the VW2C0 bit in the VW2C register to 1 (voltage monitor 2 interrupt enabled).	

Notes:
1. When the VW2C0 bit is 0, steps 4 to 6 can be performed at the same time (with one instruction).
2. When this setting is made with the voltage monitor 2 interrupt disabled (the VW2C0 bit is 0, the VCA27 bit is 0), if VCC < Vdet2 (or VCC > Vdet2) is detected, no interrupt is generated until the voltage monitor 2 interrupt in step 11 is enabled. If VCC < Vdet2 (or VCC > Vdet2) is detected between steps 10 and 11, the VW2C2 bit is set to 1. Read the VW2C2 bit after step 11, and perform the processing required for detection if the read value is 1.



VW2C1 to VW2C3, VW2C7: Bits in VW2C register
VCAC2: Bit in VCAC register

The above diagram applies under the following conditions :
- VCA27 bit in VCA2 register = 1 (voltage detection 2 circuit enabled)
- VW2C0 bit in VW2C register = 1 (voltage detection 2 interrupt enabled)

Note:
1. If voltage monitor 0 reset is not used, VCC must be at least 2.7 V.

Figure 7.7 Example of Voltage Monitor 2 Interrupt Operation

8. Watchdog Timer

The watchdog timer is a function for detecting software malfunctions. Using this function is recommended, since it can improve system reliability.

8.1 Overview

The watchdog timer has a 14-bit down counter and count source protection mode can be enabled or disabled.
Table 8.1 lists the Watchdog Timer Specifications.
For details on the watchdog timer reset, refer to **6.3.5 Watchdog Timer Reset**.
Figure 8.1 shows the Watchdog Timer Block Diagram.

Table 8.1 Watchdog Timer Specifications

Item	Count Source Protection Mode Disabled	Count Source Protection Mode Enabled
Count source	CPU clock or low-speed on-chip oscillator clock for the watchdog timer (1/16)	Low-speed on-chip oscillator clock for the watchdog timer
Count operation	Decrement	
Count start condition	Either of the following can be selected: • The count is automatically started after a reset. • The count is started by writing to the WDTS register.	
Count stop conditions	• When the count source is the CPU clock divided by 2, 16, or 128, if the MCU enters wait mode or stop mode, the count is stopped. • When the count source is the watchdog timer low-speed on-chip oscillator clock divided by 16, even if the MCU enters wait mode or stop mode, the count is not stopped.	None
Watchdog timer initialization conditions	• Reset • 00h and then FFh are written to the WDTR register during the acceptance period (1) (when an acceptance period is set.) • Underflow	
Operation at underflow	Watchdog timer interrupt or watchdog timer reset	Watchdog timer reset
Selectable functions	• Prescaler division ratio Selected by bits WDTC6 and WDTC7 in the WDTC register. • Count source protection mode - Whether count source protection mode is enabled or disabled after a reset can be selected by the CSPROINI bit in the OFS register (flash memory). - If count source protection mode is disabled, whether count source protection mode is enabled or disabled is selected by the CSPRO bit in the CSPR register (program). • Start or stop of the watchdog timer after a reset Selected by the WDTON bit in the OFS register (flash memory). • Initial value of the watchdog timer Selected by bits WDTUFS0 and WDTUFS1 in the OFS2 register. • Refresh acceptance period for the watchdog timer Selected by bits WDTRCS0 and WDTRCS1 in the OFS2 register.	

Note:
1. Only write to the WDTR register during the refresh period when the watchdog timer is counting.

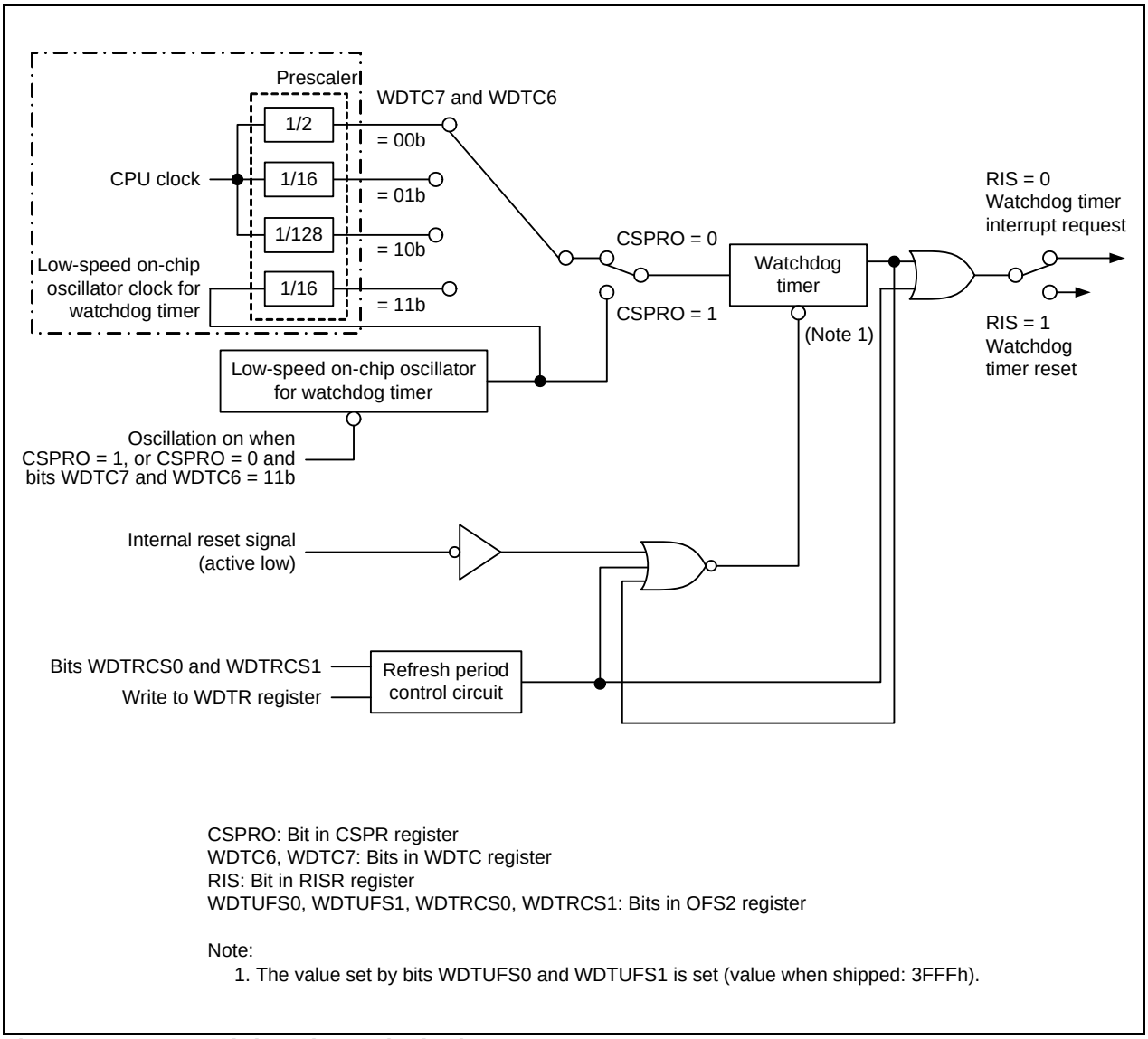


Figure 8.1 Watchdog Timer Block Diagram

8.2 Registers

Table 8.2 lists the Watchdog Timer Register Configuration.

Table 8.2 Watchdog Timer Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Reset Interrupt Select Register	RISR	10000000b or 00000000b (1)	00020h	8
Watchdog Timer Reset Register	WDTR	FFh	00021h	8
Watchdog Timer Start Register	WDTS	FFh	00022h	8
Watchdog Timer Control Register	WDTC	01111111b	00023h	8
Count Source Protection Mode Register	CSPR	10000000b or 00000000b (1)	00024h	8
Option Function Select Register 2	OFS2	(Note 2)	0FFDBh	8
Option Function Select Register	OFS	(Note 3)	0FFFFh	8

Notes:
1. The value after reset differs depending on the CSPROINI bit in the OFS register.
2. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform any additional writes to the OFS2 register. Erasing the block including the OFS2 register sets the OFS2 register to FFh.
3. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform any additional writes to the OFS register. Erasing the block including the OFS register sets the OFS register to FFh.

8.2.1 Reset Interrupt Select Register (RISR)

Address 00020h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RIS	UFIF	—	—	—	—	—	—
After Reset	1	0	0	0	0	0	0	0

The above applies when the CSPROINI bit in the OFS register is 0.

After Reset	0	0	0	0	0	0	0	0

The above applies when the CSPROINI bit in the OFS register is 1.

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	UFIF	WDT underflow detection flag	0: No watchdog timer underflow 1: Watchdog timer underflow (1)	R/W
b7	RIS	WDT interrupt/reset switch bit	0: Watchdog timer interrupt 1: Watchdog timer reset (2)	R/W

Notes:
1. After reading this bit as 1, wait for at least one cycle of the count source before writing 0 to it.
2. The RIS bit is set to 1 by writing 1 by a program, but writing 0 to this bit has no effect.
   When the CSPRO bit in the CSPR register is 1 (count source protection mode enabled), the RIS bit is automatically set to 1.

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the RISR register.

UFIF Bit (WDT underflow detection flag)

[Condition for setting to 0]
- When 0 is written to this bit.

[Conditions for setting to 1]
- When the watchdog timer underflows while the RIS bit is 0 (watchdog timer interrupt).
- When a refresh is executed during a period other than the acceptance period (illegal refresh) while the RIS bit is 0 (watchdog timer interrupt).

8.2.2 Watchdog Timer Reset Register (WDTR)

Address 00021h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b7 to b0	The watchdog timer is initialized by writing 00h and then FFh during the acceptance period. The initial value of the watchdog timer is specified by bits WDTUFS0 and WDTUFS1 in the OFS2 register. (1)	W

Note:
1. Only write to the WDTR register while the watchdog timer is counting.

8.2.3 Watchdog Timer Start Register (WDTS)

Address 00022h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b7 to b0	The watchdog timer is started by executing a write instruction to this register.	W

8.2.4 Watchdog Timer Control Register (WDTC)

Address 00023h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WDTC7	WDTC6	WDTC5	WDTC4	WDTC3	WDTC2	WDTC1	WDTC0
After Reset	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	WDTC0	Watchdog timer monitor bits	The watchdog timer bits listed in Table 8.3 can be read, depending on the set value of bits WDTUFS1 to WDTUFS0 in the OFS2 register.	R
b1	WDTC1			
b2	WDTC2			
b3	WDTC3			
b4	WDTC4			
b5	WDTC5			
b6	WDTC6	Watchdog timer count source select bits	b7 b6 0 0: CPU clock divided by 2 0 1: CPU clock divided by 16 1 0: CPU clock divided by 128 1 1: Watchdog timer low-speed on-chip oscillator clock divided by 16	R/W
b7	WDTC7			R/W

Table 8.3 Watchdog Timer Bits Indicated by Bits WDTC5 to WDTC0

OFS2 Register	WDTC Register
Set value of bits WDTUFS1 to WDTUFS0	Corresponding watchdog timer bits indicated by WDTC5 to WDTC0
00b (03FFh)	Content of watchdog timer b5 to b0
01b (0FFFh)	Content of watchdog timer b7 to b2
10b (1FFFh)	Content of watchdog timer b8 to b3
11b (3FFFh)	Content of watchdog timer b9 to b4

8.2.5 Count Source Protection Mode Register (CSPR)

Address 00024h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPRO	—	—	—	—	—	—	—
After Reset	1	0	0	0	0	0	0	0
	The above applies when the CSPROINI bit in the OFS register is 0.							
After Reset	0	0	0	0	0	0	0	0
	The above applies when the CSPROINI bit in the OFS register is 1.							

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	CSPRO	Count source protection mode select bit (1)	0: Count source protection mode disabled 1: Count source protection mode enabled	R/W

Note:
1. To set the CSPRO bit to 1, first write 0 and then write 1. This bit cannot be set to 0 by a program. Interrupts and DTC activation must be disabled between writing 0 and writing 1.

8.2.6 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bits	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acceptance period set bits	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not perform any additional writes to the OFS2 register. Erasing the block including the OFS2 register sets the OFS2 register to FFh. The value of the OFS2 register is FFh at shipment of blank products. After programming, the value is the same as that programmed by the user. At shipment of factory-programmed products, the value of the OFS2 register is the same as that set in a program by the user.

   For an example of the OFS2 register settings, refer to **5.6.1 Option Function Select Area Setting Examples**.

Bits WDTRCS0 and WDTRCS1 (Watchdog timer refresh acceptance period set bits)

These bits are used to select the refresh acceptance period as a percentage. Note that the period from the start of counting to underflow is 100%.
For details, refer to **8.3.1.1 Refresh Acceptance Period**.

8.2.7 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bits (2)	b5 b4 0 0: 3.80 V (typ.) selected (Vdet0_3) 0 1: 2.85 V (typ.) selected (Vdet0_2) Other than the above: Do not set.	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not perform any additional writes to the OFS register. Erasing the block including the OFS register sets the OFS register to FFh. The value of the OFS register is FFh at shipment of blank products. After programming, the value is the same as that programmed by the user. At shipment of factory-programmed products, the value of the OFS register is the same as that set in a program by the user.
2. The same voltage detection 0 level selected by bits VDSEL0 and VDSEL1 is set in both the voltage monitor 0 reset and power-on reset functions.
3. Set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset) to use the power-on reset or voltage monitor 0 reset.

For an example of the OFS register settings, refer to **5.6.1 Option Function Select Area Setting Examples**.

LVDAS Bit (Voltage detection 0 circuit start bit)

The Vdet0 voltage monitored in the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

8.3 Operation

8.3.1 Items Common to Multiple Modes

8.3.1.1 Refresh Acceptance Period

The period for accepting a refresh operation to the watchdog timer (a write to the WDTR register) can be selected by bits WDTRCS0 and WDTRCS1 in the OFS2 register. Figure 8.2 shows the Watchdog Timer Refresh Acceptance Period.

When the period from the start of counting to underflow is 100%, a refresh operation executed during the acceptance period is accepted as shown below. A refresh operation executed during a period other than the acceptance period is processed as an illegal write, generating a watchdog timer interrupt or watchdog timer reset (selected by the RIS bit in the RISR register).

Do not perform a refresh operation when the watchdog timer is stopped.

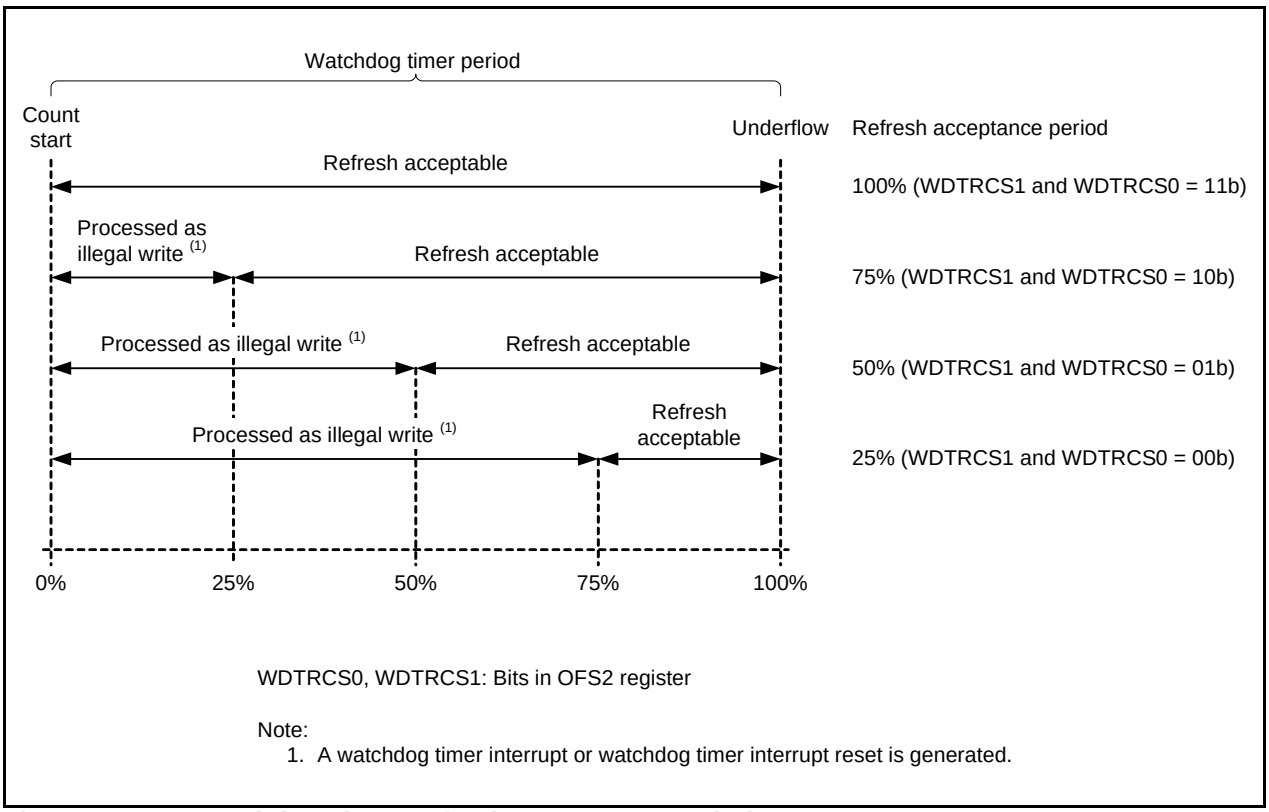


Figure 8.2 Watchdog Timer Refresh Acceptance Period

8.3.2 When Count Source Protection Mode is Disabled

When count source protection mode is disabled, the count source for the watchdog timer is the CPU clock or the low-speed on-chip oscillator clock for the watchdog timer.
Table 8.4 lists the Watchdog Timer Specifications when Count Source Protection Mode is Disabled.

Table 8.4 Watchdog Timer Specifications when Count Source Protection Mode is Disabled

Item	Specification
Count source	CPU clock or low-speed on-chip oscillator clock for the watchdog timer (1/16)
Count operation	Decrement
Period	$\frac{\text{Prescaler division ratio (n)} \times \text{Count value of the watchdog timer (m)}\ ^{(1)}}{\text{Count source}}$ n: 2, 16, or 128 (selected by bits WDTC6 and WDTC7 in the WDTC register) However, when bits WDTC7 and WDTC6 are 11b (the count source is the low-speed on-chip oscillator for the watchdog timer), n is 16. m: Value set by bits WDTUFS0 and WDTUFS1 in the OFS2 register Ex.: When the prescaler divides a CPU clock of 20 MHz by 16, and bits WDTUFS1 and WDTUFS0 are 11b (3FFFh), the period is approx. 13.1 ms.
Watchdog timer initialization conditions	• Reset • 00h and then FFh are written to the WDTR register (2) • Underflow
Count start conditions	The operation of the watchdog timer after a reset is selected by the WDTON bit (3) in the OFS register (address 0FFFFh). • When the WDTON bit is 1 (watchdog timer is stopped after reset) The watchdog timer and the prescaler are stopped after a reset, and only start counting when the WDTS register is written. • When the WDTON bit is 0 (watchdog timer automatically starts after reset) The watchdog timer and the prescaler automatically start counting after a reset.
Count stop conditions	• When the count source is obtained by dividing the CPU clock by 2, 16, or 128, if the MCU enters wait mode or stop mode, count stops. • When the count source is obtained by dividing the watchdog timer low-speed on-chip oscillator clock by 16, even if the MCU enters wait mode or stop mode, count does not stop.
Operation at underflow	• When the RIS bit in the RISR register is 0 Watchdog timer interrupt • When the RIS bit in the RISR register is 1 Watchdog timer reset (refer to **6.3.5 Watchdog Timer Reset**.)

Notes:
1. The watchdog timer is initialized by writing 00h and then FFh to the WDTR register. The prescaler is initialized after a reset. This results in discrepancies in the watchdog timer period due to the prescaler.
2. Only write to the WDTR register while the watchdog timer is counting.
3. The WDTON bit cannot be changed by a program. To set this bit, write 0 to bit 0 at address 0FFFFh with a flash programmer.

8.3.3 When Count Source Protection Mode is Enabled

When count source protection mode is enabled, the count source for the watchdog timer is the low-speed on-chip oscillator clock for the watchdog timer. If the CPU clock is stopped when a program runs out of control, a clock will still be supplied to the watchdog timer.
Table 8.5 lists the Watchdog Timer Specifications when Count Source Protection Mode is Enabled.

Table 8.5 Watchdog Timer Specifications when Count Source Protection Mode is Enabled

Item	Specification
Count source	Low-speed on-chip oscillator clock for the watchdog timer
Count operation	Decrement
Period	$\frac{\text{Count value of the watchdog timer (m)}}{\text{Low-speed on-chip oscillator clock for the watchdog timer}}$ m: Value set by bits WDTUFS0 and WDTUFS1 in the OFS2 register Ex.: When the low-speed on-chip oscillator clock for the watchdog timer is 125 kHz and bits WDTUFS1 and WDTUFS0 are 00b (03FFh), the period is approx. 8.2 ms.
Watchdog timer initialization conditions	• Reset • 00h and then FFh are written to the WDTR register (1) • Underflow
Count start conditions	The operation of the watchdog timer after a reset is selected by the WDTON bit (2) in the OFS register (address 0FFFFh). • When the WDTON bit is 1 (watchdog timer is stopped after reset) The watchdog timer and the prescaler are stopped after a reset, and only start counting when the WDTS register is written. • When the WDTON bit is 0 (watchdog timer automatically starts after reset) The watchdog timer and the prescaler automatically start counting after a reset.
Count stop condition	None (Once count has started, it will not stop even in wait mode or stop mode.)
Operation at underflow	Watchdog timer reset (refer to **6.3.5 Watchdog Timer Reset**.)
Registers, bits	When the CSPRO bit in the CSPR register is set to 1 (count source protection mode enabled) (3), the following are automatically set: • The low-speed on-chip oscillator for the watchdog timer oscillates. • The RIS bit in the RISR register is set to 1 (watchdog timer reset).

Notes:
1. Only write to the WDTR register while the watchdog timer is counting.
2. The WDTON bit cannot be changed by a program. To set this bit, write 0 to bit 0 at address 0FFFFh with a flash programmer.
3. The CSPRO bit is set to 1 even if 0 is written to the CSPROINI bit in the OFS register. The CSPROINI bit cannot be changed by a program. To set this bit, write 0 to bit 7 at address 0FFFFh with a flash programmer.

9. Clock Generation Circuit

9.1 Overview

The following five circuits are included in the clock generation circuit:
- XIN clock oscillation circuit
- Low-speed on-chip oscillator
- High-speed on-chip oscillator
- Low-speed on-chip oscillator for the watchdog timer
- PLL frequency synthesizer

Table 9.1 lists the Clock Generation Circuit Specifications, Figure 9.1 shows the Clock Generation Circuit Block Diagram. Figure 9.2 shows the Supply of Peripheral Function Clocks, and Table 9.2 lists the Clock Generation Circuit Pin Configuration.

Table 9.1 Clock Generation Circuit Specifications

Item	XIN Clock Oscillation Circuit	Oscillators		Low-Speed On-Chip Oscillator for Watchdog Timer	PLL Frequency Synthesizer
		High-Speed On-Chip Oscillator	Low-Speed On-Chip Oscillator		
Applications	• CPU clock source • Peripheral function clock source	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock sources when the XIN clock oscillation stops.		• Watchdog timer clock source	• CPU clock source • Peripheral function clock source
Clock frequency	0 to 20 MHz	Approx. 40 MHz (3)	Approx.125 kHz	Approx.125 kHz	10 MHz to 32 MHz
Connectable oscillator	• Ceramic resonator • Crystal oscillator	—		—	— (6)
Oscillator connect pins	XIN, XOUT (1)	— (1)		—	— (6)
Oscillation start and stop	Usable	Usable		Usable	Usable
State after reset	Stopped	Stopped	Oscillates	Stopped (4) Oscillates (5)	Stopped
Others	• An externally generated clock can be input. (2)	—		—	— (6)

Notes:
1. When the on-chip oscillator clock is used as the CPU clock without using the XIN clock oscillation circuit, these pins can be used as P4_6 and P4_7.
2. When inputting an external clock, set the CM05 bit in the CM0 register to 0 (oscillates), the CM07 bit in the CM0 register to 1 (XIN clock is supplied by external clock input to XOUT pin), and the CM13 bit in the CM1 register to 1 (XIN-XOUT pin).
3. When the high-speed on-chip oscillator is used as the CPU clock source, the frequency will be a maximum of 20 MHz by setting the divider.
4. This applies when the CSPROINI bit in the OFS register is 1 (count source protection mode disabled after reset).
5. This applies when the CSPROINI bit is 0 (count source protection mode enabled after reset).
6. The PLL frequency synthesizer uses the XIN clock oscillation circuit as a reference clock source.

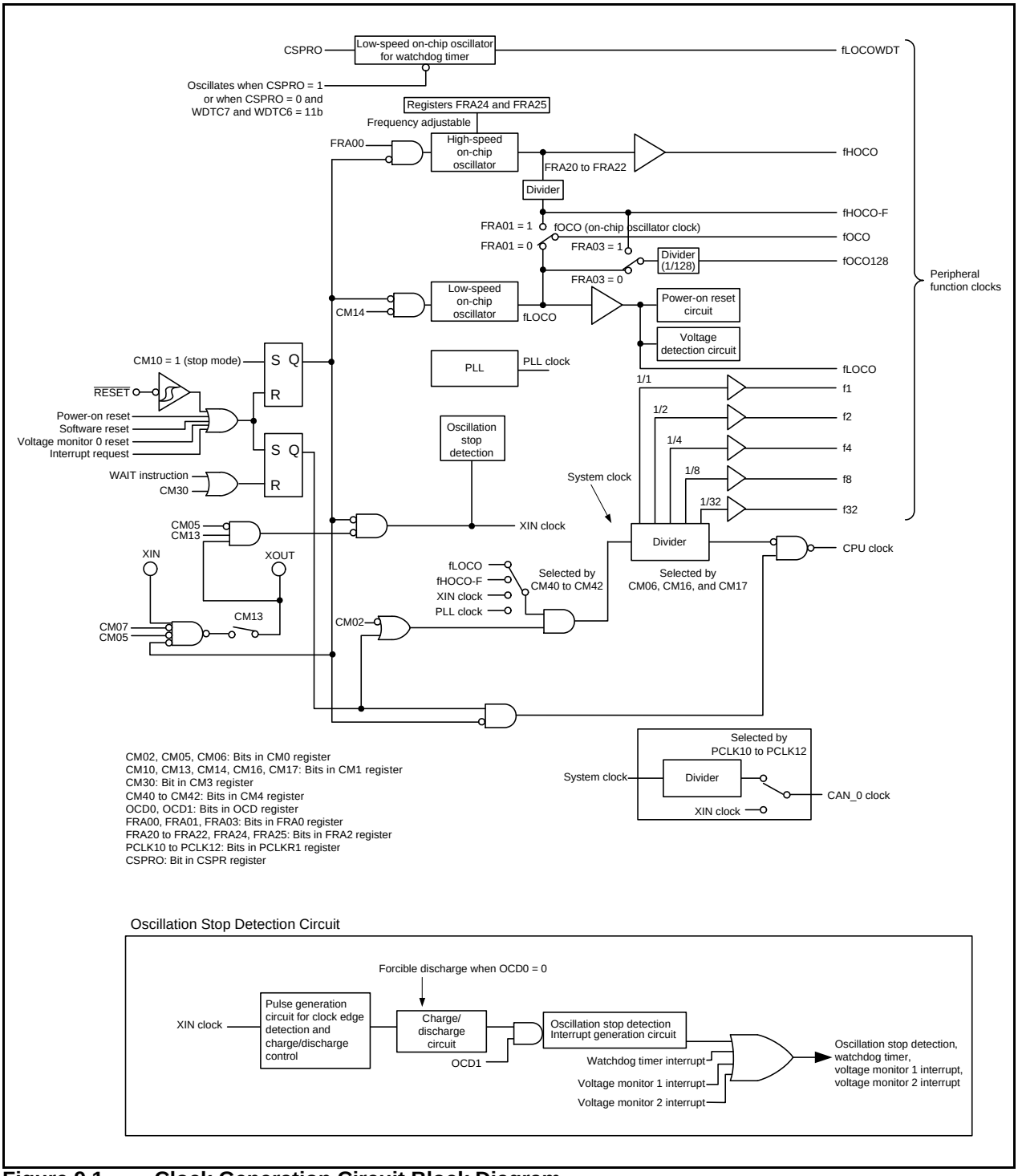


Figure 9.1 Clock Generation Circuit Block Diagram

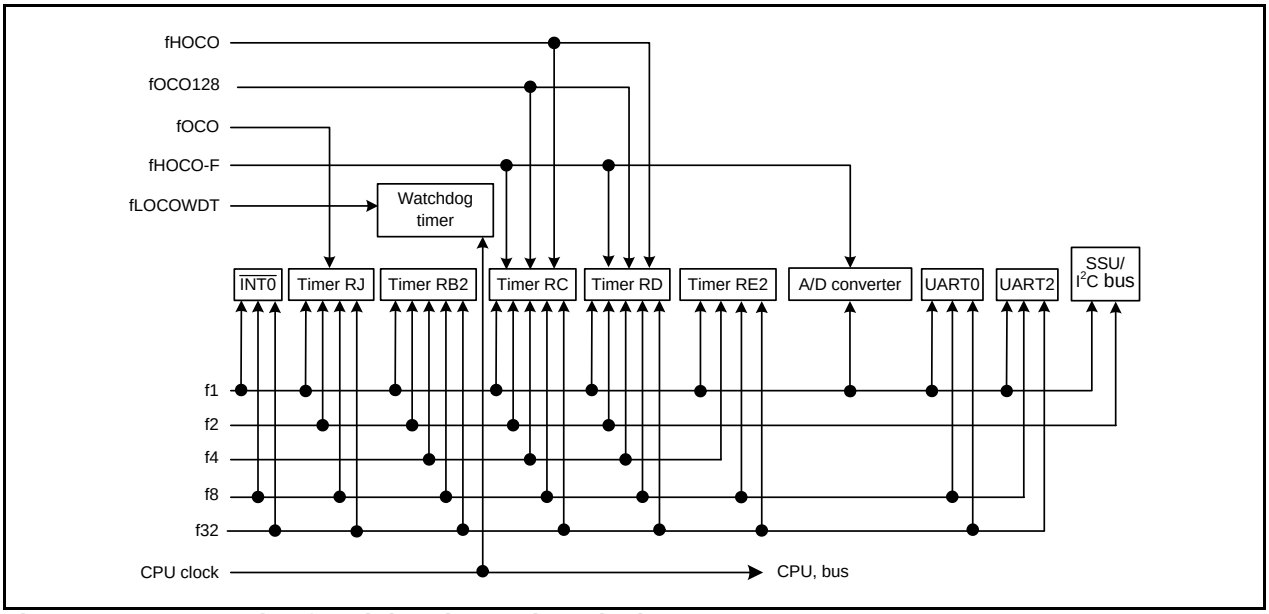


Figure 9.2 Supply of Peripheral Function Clocks

Table 9.2 Clock Generation Circuit Pin Configuration

Pin Name	I/O	Function
XIN	Input	XIN clock oscillation circuit input
XOUT	Input/Output	XIN clock oscillation circuit input/external clock input

9.2 Registers

Table 9.3 lists the Clock Generation Circuit Register Configuration.

Table 9.3 Clock Generation Circuit Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
System Clock Control Register 0	CM0	00101000b	00008h	8
System Clock Control Register 1	CM1	00100000b	00009h	8
Oscillation Stop Detection Register	OCD	00h	0000Ah	8
System Clock Control Register 3	CM3	00h	0000Bh	8
System Clock Control Register 4	CM4	00000001b	0000Ch	8
Peripheral Clock Select Register 1	PCLKR1	00h	0000Fh	8
High-Speed On-Chip Oscillator Control Register 0	FRA0	00h	00012h	8
High-Speed On-Chip Oscillator Control Register 2	FRA2	00h	00014h	8
PLL Control Register 0	PLC0	00010010b	0001Ch	8
Voltage Detection Register 2	VCA2	00000000b or 00100000b (1)	00034h	8
I/O Function Pin Select Register	PINSR	00h	002B9h	8

Note:
1. The value after reset differs depending on the LVDAS bit in the OFS register.

9.2.1 System Clock Control Register 0 (CM0)

Address 00008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM07	CM06	CM05	—	—	CM02	—	—
After Reset	0	0	1	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			R/W
b2	CM02	Peripheral function clock stop bit in wait mode	0: Peripheral function clock does not stop in wait mode 1: Peripheral function clock stops in wait mode	R/W
b3	—	Reserved	Set to 1.	R/W
b4	—	Reserved	Set to 0.	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit (1, 2)	0: Oscillates 1: Stops (3)	R/W
b6	CM06	CPU clock division ratio select bit 0 (4)	0: Bits CM16 and CM17 in CM1 register enabled 1: Divide-by-8 mode	R/W
b7	CM07	XIN clock supply set bit (5)	0: XIN clock is supplied by oscillator (external ceramic resonator, etc.) 1: XIN clock is supplied by external clock input to XOUT pin	R/W

Notes:
1. The CM05 bit is used to stop the XIN clock. This bit cannot be used to detect whether the XIN clock has stopped. To stop the XIN clock, make the following settings:
   (1) Set bits OCD1 and OCD0 in the OCD register to 00b (oscillation stop detection function disabled).
   (2) Set bits CM42 to CM40 in the CM4 register to 001b (fLOCO clock) or 101b (fHOCO-F clock).
2. P4_6 and P4_7 can be used as I/O ports only when the CM05 bit is 1 (XIN clock stops) and the CM13 bit in the CM1 register is 0 (P4_6 and P4_7).
3. When an external clock is input, the clock input itself is not accepted.
4. When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode).
5. When the MCU exits stop mode or wait mode, do not set the CM05 bit to 1 (XIN clock stops) if switching to the XIN clock.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM0 register.

9.2.2 System Clock Control Register 1 (CM1)

Address 00009h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM17	CM16	—	CM14	CM13	—	CM11	CM10
After Reset	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM10	All clock stop control bit (1, 2)	0: Clocks oscillate 1: All clocks stop (stop mode)	R/W
b1	CM11	XIN-XOUT on-chip feedback resistor select bit	0: On-chip feedback resistor enabled 1: On-chip feedback resistor disabled	R/W
b2	—	Reserved	Set to 0.	R/W
b3	CM13	Port/XIN-XOUT switch bit (3)	0: I/O ports P4_6 and P4_7 1: XIN-XOUT pin	R/W
b4	CM14	Low-speed on-chip oscillator oscillation stop bit (4, 5)	0: Low-speed on-chip oscillator on 1: Low-speed on-chip oscillator off	R/W
b5	—	Reserved	Set to 1.	R/W
b6	CM16	CPU clock division select bits 1 (6)	b7 b6 0 0: Divide-by-1 mode 0 1: Divide-by-2 mode 1 0: Divide-by-4 mode 1 1: Divide-by-16 mode	R/W
b7	CM17			R/W

Notes:

1. If the CM10 bit is 1 (stop mode), the on-chip feedback register is disabled. If the CM10 bit is 1 (stop mode), when the CM13 bit is 1 (XIN-XOUT pin), pins XIN (P4_6) and XOUT (P4_7) are set to high impedance.
2. When the SVC0 bit in the SVDC register is 1 (transition to low-power-consumption mode enabled), do not set the CM10 bit to 1 (stop mode).
3. Once the CM13 bit is set to 1 by a program, it cannot be set to 0. Set the CM13 bit to 1 to use P4_6 and P4_7 as the XIN-XOUT pin.
4. The CM14 bit can be set to 1 (low-speed on-chip oscillator off) when bits CM42 to CM40 in the CM4 register are 000b (XIN clock). When bits CM42 to CM40 are set to 001b (fLOCO clock), the CM14 bit is set to 0 (low-speed on-chip oscillator on). Writing 1 to this bit has no effect.
5. To use a voltage monitor 1 interrupt or a voltage monitor 2 interrupt (when the digital filter is used), set the CM14 bit to 0 (low-speed on-chip oscillator on).
6. When the CM06 bit in the CM0 register is 0 (bits CM16 and CM17 enabled), bits CM16 and CM17 are enabled.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM1 register.

9.2.3 Oscillation Stop Detection Register (OCD)

Address 0000Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	OCD6	—	—	OCD3	OCD2	OCD1	OCD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	OCD0	Oscillation stop detection enable bit (1)	0: Oscillation stop detection function disabled (2) 1: Oscillation stop detection function enabled	R/W
b1	OCD1	Oscillation stop detection interrupt enable bit	0: Disabled (2) 1: Enabled	R/W
b2	OCD2	Oscillation stop detection flag (3)	0: Oscillating 1: Oscillation stop is detected	R
b3	OCD3	Oscillation stop monitor bit (4)	0: Oscillation frequency > Approx. 2 MHz 1: Oscillation frequency ≤ Approx. 2 MHz	R/W
b4	—	Reserved	Set to 0.	R/W
b5	—			
b6	OCD6	Switching clock select bit when oscillation stop is detected (5)	0: fLOCO 1: fHOCO-F	R/W
b7	—	Reserved	Set to 0.	R/W

Notes:

1. Refer to **Figure 9.6 Procedure for Switching from Low-Speed On-Chip Oscillator to XIN Clock** for the switching procedure when the XIN clock reoscillates after the oscillation stop is detected.
2. Set bits OCD1 and OCD0 to 00b before entering stop mode, high-speed on-chip oscillator mode, or low-speed on-chip oscillator mode (XIN clock stops).
3. The OCD2 bit is set to 1 if oscillation stop is detected when the OCD0 bit is 1 (oscillation stop detection function enabled) and the OCD1 bit is 1 (oscillation stop interrupt enabled).
   The OCD2 bit remains 1 until the OCD1 bit to set to 0 (oscillation stop interrupt disabled).
4. The OCD3 bit is enabled when the OCD0 bit is 1 (oscillation stop detection function enabled). Since the OCD3 bit can be used to monitor the oscillation state continuously, determine the state of the selected clock by reading this bit several times.
5. When selecting a clock after oscillation is stopped, set the OCD6 bit first and then set bits OCD1 and OCD0 to 11b.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the OCD register.

9.2.4 System Clock Control Register 3 (CM3)

Address 0000Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM37	CM36	CM35	—	—	—	—	CM30
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM30	Wait control bit (1)	0: Not in wait mode 1: MCU enters wait mode	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	—			
b5	CM35	CPU clock division ratio select bit when exiting wait mode (2)	0: Settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled 1: No division	R/W
b6	CM36	System clock select bits when exiting wait mode or stop mode (3)	b7 b6 0 0: MCU exits using the CPU clock used immediately before entering wait mode or stop mode 0 1: Do not set. 1 0: High-speed on-chip oscillator clock selected (4) 1 1: XIN clock selected (5)	R/W
b7	CM37			R/W

Notes:
1. When the MCU exits wait mode by a peripheral function interrupt, the CM30 bit is set to 0 (not in wait mode).
2. Set the CM35 bit to 0 in stop mode. When the MCU enters wait mode, if the CM35 bit is 1 (no division), the CM06 bit in the CM0 register is set to 0 (bits CM16 and CM17 in CM1 register enabled) and bits CM17 and CM16 are set to 00b (divide-by-1 mode).
3. To enter wait mode or stop mode while the FMR27 bit in the FMR2 register is 1 (flash memory low-current-consumption read mode enabled), set bits CM37 and CM36 to 00b (MCU exits using the CPU clock used immediately before entering wait mode or stop mode) and set the CM35 bit to 0 (settings of CM06 bit in CM0 register and bits CM16b and CM17 in CM1 register enabled). During low-current-consumption read mode, do not set the FMSTP bit in the FMR0 register to 1 (flash memory stops).
4. When bits CM37 and CM36 are set to 10b (high-speed on-chip oscillator clock selected), the following will be set when the MCU exits wait mode or stop mode.
   • Bits CM42 to CM40 in CM4 register = 001b (fLOCO clock)
   • FRA00 bit in FRA0 register (high-speed on-chip oscillator on)
   • Bits CM42 to CM40 in CM4 register = 101b (fHOCO-F clock)
5. When bits CM37 and CM36 are set to 11b (XIN clock selected), the following will be set when the MCU exits wait mode or stop mode.
   • CM05 bit in CM0 register = 1 (XIN clock oscillates)
   • CM13 bit in CM1 register = 1 (XIN-XOUT pin)
   • Bits CM42 to CM40 in CM4 register = 000b (XIN clock selected)
   When entering wait mode while the CM05 bit in the CM0 register is 1 (XIN clock stops), if the XIN clock is selected as the CPU clock used to exit wait mode, set the CM06 bit to 1 (divide-by-8 mode) and the CM35 bit to 0.
   However, if an externally generated clock is used as the XIN clock, do not set bits CM37 and CM36 to 11b (XIN clock selected).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM3 register.

CM30 Bit (Wait control bit)

When the CM30 bit is set to 1 (MCU enters wait mode), the CPU clock stops (wait mode). Since the XIN, low-speed on-chip oscillator, high-speed on-chip oscillator, and watchdog timer low-speed on-chip oscillator clocks do not stop, the peripheral functions that use these clocks continue operating. When setting the CM30 bit to 1, set the I flag to 0 (maskable interrupt disabled).

A reset or a peripheral function interrupt is used to exit wait mode. When a peripheral function interrupt is used to exit wait mode, the MCU resumes executing the instruction immediately after the instruction to set the CM30 bit to 1.

However, when using the WAIT mode to enter wait mode, set the I flag to 1 (maskable interrupt enabled). With this setting, interrupt handling is performed by the CPU when the MCU exits wait mode.

9.2.5 System Clock Control Register 4 (CM4)

Address 0000Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	CM42	CM41	CM40
After Reset	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	CM40	CPU clock select bits (1)	b2 b1 b0 0 0 0: XIN clock 0 0 1: fLOCO clock 0 1 0: Do not set. 0 1 1: Do not set. 1 0 0: PLL clock 1 0 1: fHOCO-F clock Other than the above: Do not set.	R/W
b1	CM41			R/W
b2	CM42			R/W
b3	—	Reserved	Set to 0.	R/W
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. For details, refer to **Figure 10.1 State Transitions in Power Control Mode**.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before setting the CM4 register.

9.2.6 Peripheral Clock Select Register 1 (PCLKR1)

Address 0000Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	PCLK12	PCLK11	PCLK10
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PCLK10	CAN_0 clock select bits (1)	b2 b1 b0 0 0 0: System clock divided by 1 0 0 1: System clock divided by 2 0 1 0: System clock divided by 4 0 1 1: System clock divided by 8 1 0 0: XIN clock Other than the above: Do not set.	R/W
b1	PCLK11			R/W
b2	PCLK12			R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—	Reserved	Set to 0.	R/W
b5	—			
b6	—			
b7	—	Nothing is assigned. The write value must be 0. The read value is 0.		—

Note:
1. These bits are used to select the CAN clock source.
   The CAN clock can be selected as the CAN system clock (fCAN) using the CCLKS bit in the CCLKR register.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the PCLKR1 register.

9.2.7 High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Address 00012h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	FRA03	—	FRA01	FRA00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	0: High-speed on-chip oscillator off 1: High-speed on-chip oscillator on	R/W
b1	FRA01	fOCO clock source select bit (1)	0: Low-speed on-chip oscillator selected (2) 1: High-speed on-chip oscillator selected	R/W
b2	—	Reserved	Set to 0.	R/W
b3	FRA03	fOCO128 clock select bit	0: fLOCO divided by 128 selected 1: fHOCO-F divided by 128 selected	R/W
b4	—	Reserved	Set to 0.	R/W
b5	—			
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

Notes:
1. Set the FRA01 bit under the following conditions:
   • FRA00 bit = 1 (high-speed on-chip oscillator on)
   • CM14 bit in the CM1 register = 0 (low-speed on-chip oscillator on)
   • Bits FRA22 to FRA20 in the FRA2 register:
   All division modes can be set when VCC = 2.7 to 5.5 V: 000b to 111b
2. When writing 0 (low-speed on-chip oscillator selected) to the FRA01 bit, do not write 0 (high-speed on-chip oscillator off) to the FRA00 bit at the same time. After the FRA01 bit is set to 0, set the FRA00 bit to 0.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA0 register.

9.2.8 High-Speed On-Chip Oscillator Control Register 2 (FRA2)

Address 00014h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	FRA25	FRA24	—	FRA22	FRA21	FRA20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA20	High-speed on-chip oscillator division ratio select bits	b2 b1 b0 0 0 0: Divide-by-2 mode 0 0 1: Divide-by-3 mode 0 1 0: Divide-by-4 mode 0 1 1: Divide-by-5 mode 1 0 0: Divide-by-6 mode 1 0 1: Divide-by-7 mode 1 1 0: Divide-by-8 mode 1 1 1: Divide-by-9 mode	R/W
b1	FRA21			R/W
b2	FRA22			R/W
b3	—	Reserved	Set to 0.	R/W
b4	FRA24	High-speed on-chip oscillator frequency switch bits	b5 b4 0 0: 40 MHz 0 1: 36.864 MHz 1 0: 32 MHz 1 1: The same applies as with the setting of 00b	R/W
b5	FRA25			
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

When rewriting the FRA2 register, set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting while the high-speed on-chip oscillator is stopped.

9.2.9 PLL Control Register 0 (PLC0)

Address 0001Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PLC07	—	PLC05	PLC04	—	PLC02	PLC01	PLC00
After Reset	0	0	0	1	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	PLC00	PLL multiplying rate select bits (1)	b2 b1 b0 0 0 0: Do not set. 0 0 1: Multiply-by-2 0 1 0: Multiply-by-4 0 1 1: Multiply-by-6 1 0 0: Multiply-by-8 Other than the above: Do not set.	R/W
b1	PLC01			R/W
b2	PLC02			R/W
b3	—	Reserved	The read value is undefined.	R
b4	PLC04	Reference frequency counter set bits (1)	b5 b4 0 0: No division 0 1: Divide-by-2 1 0: Divide-by-4 1 1: Divide-by-8	R/W
b5	PLC05			R/W
b6	—	Reserved	Set to 0.	R/W
b7	PLC07	PLL operation enable bit (2)	0: PLL stops 1: PLL operates	R/W

Notes:
1. These bits can be written when the PLC07 bit is 0 (PLL stops). Once a value has been written, it must not be changed.
2. After setting the PLC07 bit to 1 (PLL operates), set bits CM42 to CM40 in the CM4 register to 100b (PLL clock).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the PLC0 register.

9.2.10 Voltage Detection Register 2 (VCA2)

Address 00034h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VCA27	VCA26	VCA25	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is 1.

After Reset	0	0	1	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is 0.

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	—			
b5	VCA25	Voltage detection 0 enable bit (1)	0: Voltage detection 0 circuit disabled 1: Voltage detection 0 circuit enabled	R/W
b6	VCA26	Voltage detection 1 enable bit (2)	0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W
b7	VCA27	Voltage detection 2 enable bit (3)	0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled	R/W

Notes:
1. To use the voltage monitor 0 reset, set the VCA25 bit to 1.
2. To use the voltage detection 1 interrupt or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1. After the VCA26 bit is set from 0 to 1 and td(E-A) has elapsed, the voltage detection 1 circuit operates.
3. To use the voltage detection 2 interrupt or the VW2C3 bit in the VW2C register, set the VCA27 bit to 1. After the VCA27 bit is set from 0 to 1 and td(E-A) has elapsed, the voltage detection 2 circuit operates.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCA2 register.

9.2.11 I/O Function Pin Select Register (PINSR)

Address 002B9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IOINSEL	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	IOINSEL	I/O port input function select bit	0: The I/O port input function depends on the PDi (i = 0 to 4, 6, or 9) register. When the PDi_j (j = 0 to 7) bit in the PDi register is set to 0 (input mode), the pin input level can be read. When the PDi_j bit in the PDi register is set to 1 (output mode), the value of the port latch can be read. 1: The I/O port input function can read the pin input level regardless of the PDi register	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

IOINSEL Bit (I/O port input function select bit)

When the PDi_j bit in the PDi register is 1 (output mode), the IOINSEL bit is used to select whether the value read from the PORTi register is the port latch or the pin input level of the I/O port. If set to 0, the value of the port latch is read. If set to 1, the pin input level of the I/O port is read.

Table 9.4 lists I/O Port Values Read by Using IOINSEL Bit. The IOINSEL bit can be used to change the input function of all I/O ports.

Table 9.4 I/O Port Values Read by Using IOINSEL Bit

PDi_j Bit in PDi Register	0 (Input Mode)		1 (Output Mode)	
IOINSEL bit	0	1	0	1
I/O port values read	Pin input level		Port latch value	Pin input level

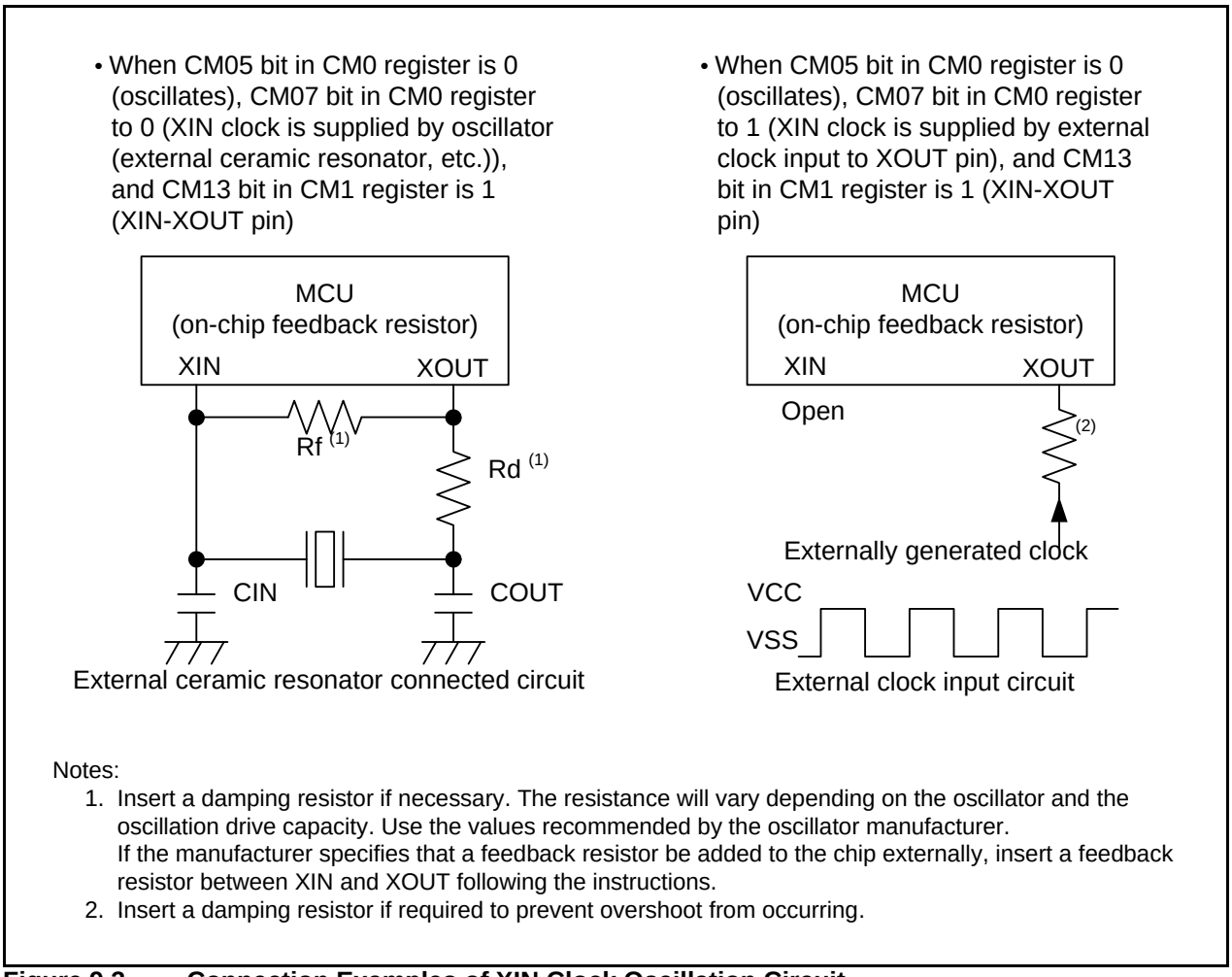
i = 0 to 4, 6, or 9, j = 0 to 7

9.3 XIN Clock

The XIN clock is supplied by the XIN clock oscillation circuit. This clock is used as the clock source for the CPU clock and the peripheral function clock. The XIN clock oscillation circuit is configured by connecting an oscillator between pins XIN and XOUT. The XIN clock oscillation circuit includes an on-chip feedback resistor, which is disconnected from the oscillation circuit in stop mode to reduce power consumption. The XIN clock oscillation circuit also allows an externally generated clock to be input to the XOUT pin.
Figure 9.3 shows Connection Examples of XIN Clock Oscillation Circuit.
The XIN clock is stopped during and after a reset.
After setting the CM13 bit in the CM1 register to 1 (XIN-XOUT pin), when the CM05 bit in the CM0 register is set to 0 (XIN clock oscillates), the XIN clock starts oscillating. After the XIN clock oscillation stabilizes, when bits CM42 to CM40 in the CM4 register are set to 000b (XIN clock selected), the XIN clock is used as the clock source for the CPU.
In stop mode, all clocks including the XIN clock are stopped. For details, refer to **10. Power Control**.
The settings listed in Table 9.5 are necessary to set the XIN clock, corresponding to the external oscillator or external clock input.

Table 9.5 CM0 and CM1 Register Settings

CM0 Register		CM1 Register	XIN Clock
CM05 Bit	CM07 Bit	CM13 Bit	
1	0	1	Oscillation stops
0	0	1	Oscillation enabled
1	1	1	External clock stops
0	1	1	External clock input enabled



Notes:
1. Insert a damping resistor if necessary. The resistance will vary depending on the oscillator and the oscillation drive capacity. Use the values recommended by the oscillator manufacturer.
   If the manufacturer specifies that a feedback resistor be added to the chip externally, insert a feedback resistor between XIN and XOUT following the instructions.
2. Insert a damping resistor if required to prevent overshoot from occurring.

Figure 9.3 Connection Examples of XIN Clock Oscillation Circuit

9.4 On-Chip Oscillator Clocks

These clocks are supplied by the on-chip oscillators. There are high-speed and low-speed on-chip oscillators as on-chip oscillators. The clock for the on-chip oscillator selected by the FRA01 bit in the FRA0 register will be the on-chip oscillator clock.

9.4.1 Low-Speed On-Chip Oscillator Clock

The clock generated by the low-speed on-chip oscillator is used as the clock source for the CPU clock, peripheral function clock, fOCO, fLOCO, and fOCO128.
After a reset, the on-chip oscillator clock with no division generated by the low-speed oscillator will be the CPU clock.
While bits OCD1 and OCD0 in the OCD register are 11b, when the XIN clock is stopped, the low-speed on-chip oscillator automatically starts operating and supplies the clock.
The frequency of the on-chip oscillator clock will vary greatly depending on the supply voltage and operating ambient temperature. Application products must be designed with sufficient margin to allow for these variations in frequency.

9.4.2 High-Speed On-Chip Oscillator Clock

The clock generated by the high-speed on-chip oscillator is used as the clock source for the CPU clock, peripheral function clock, fOCO, fHOCO-F, fHOCO, and fOCO128.
The on-chip oscillator clock generated by the high-speed on-chip oscillator is stopped after a reset. When the FRA00 bit in the FRA0 register is set to 1 (on-chip oscillator on), the clock starts oscillating.

To adjust the frequency of the high-speed on-chip oscillator clock to 36.864 MHz, set bits FRA25 and FRA24 in the FRA2 register to 01b. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.
To adjust the frequency of the high-speed on-chip oscillator clock to 32 MHz, set bits FRA25 and FRA24 to 10b.

9.5 PLL Clock

The PLL clock is generated by the PLL frequency synthesizer. This clock is used as the clock source for the CPU clock and the peripheral function clock. After a reset, the PLL frequency synthesizer is stopped. When the PLC07 bit in the PLC0 register is set to 1 (PLL operates), the PLL frequency synthesizer operates. To use the PLL clock as the clock source for the CPU clock, wait for tsu(PLL) until the PLL clock stabilizes and set bits CM42 to CM40 in the CM4 register to 100b.

Figure 9.4 shows the Procedure for Setting PLL Clock as CPU Clock Source. The PLL clock is obtained by dividing the XIN clock by the selected values of bits PLC04 and PLC05 in the PLC0 register, and then multiplied by the selected values of bits PLC00 to PLC02 in the PLC0 register. Set bits PLC04 and PLC05 so that the clock frequency after division will be between 2 MHz to 6 MHz. Figure 9.5 shows the Relation between XIN Clock and PLL Clock.

PLL operating mode cannot be used to transit to wait mode or stop mode.

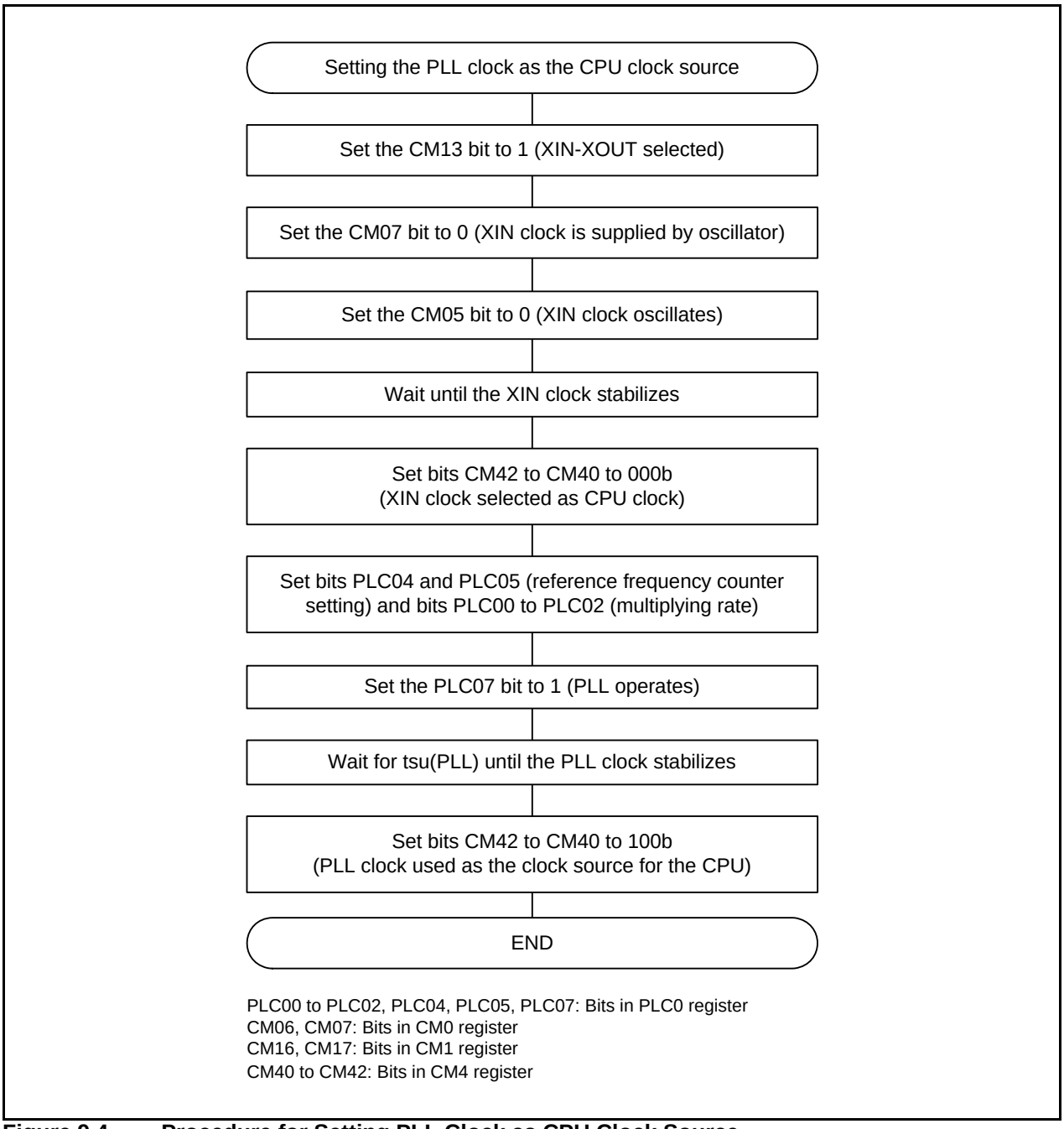


Figure 9.4 Procedure for Setting PLL Clock as CPU Clock Source

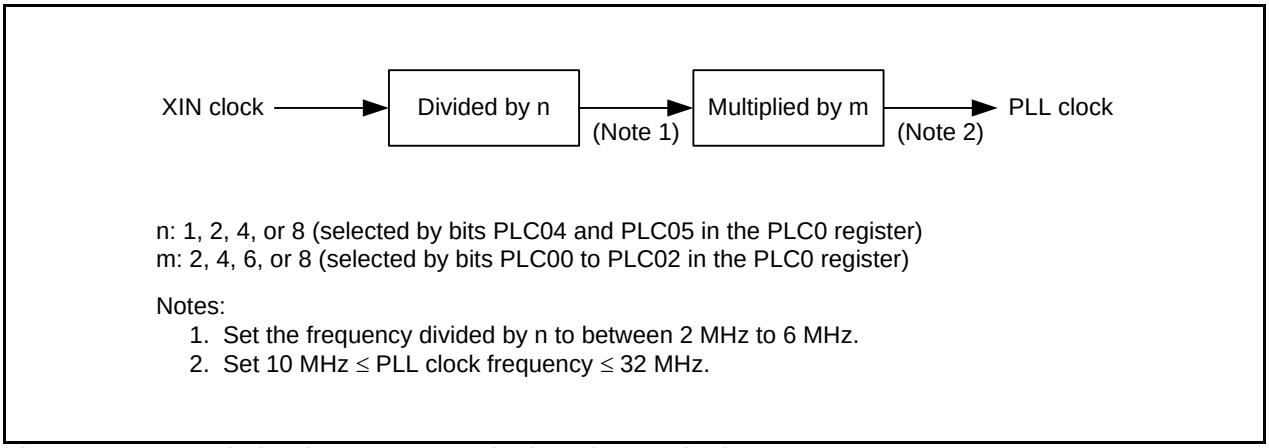


Figure 9.5 Relation between XIN Clock and PLL Clock

Bits PLC00 to PLC02, PLC04, and PLC05 in the PLC0 register can be set only once after a reset. Table 9.6 lists an Example of PLL Clock Frequency Settings.

Table 9.6 Example of PLL Clock Frequency Settings

XIN Clock	Setting Values		PLL Clock
	Bits PLC05 and PLC04	Bits PLC02 to PLC00	
10 MHz	01b (divide-by-2)	010b (multiply-by-4)	20 MHz
5 MHz	00b (no division)	010b (multiply-by-4)	
12 MHz	10b (divide-by-4)	100b (multiply-by-8)	24 MHz
6 MHz	01b (divide-by-2)	100b (multiply-by-8)	
16 MHz	10b (divide-by-4)	100b (multiply-by-8)	32 MHz
8 MHz	01b (divide-by-2)	100b (multiply-by-8)	

9.6 CPU Clock and Peripheral Functional Clock

There are a CPU clock to operate the CPU and a peripheral function clock to operate the peripheral functions (refer to **Figure 9.1 Clock Generation Circuit Block Diagram**).

9.6.1 System Clock

This clock is used as the clock source for the CPU clock and the peripheral function clock. The XIN clock, on-chip oscillator clock, or PLL clock can be selected.

9.6.2 CPU Clock

This is an operating clock for the CPU and the watchdog timer.
The CPU clock can be obtained by dividing the system clock by 1 (no division), 2, 4, 8, or 16. The frequency division ratio can be selected by the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register.
After a reset, the low-speed on-chip oscillator clock with no division will be the CPU clock.
When entering stop mode, the CM06 bit is set to 1 (divide-by-8 mode). To enter stop mode, set the CM35 bit in the CM3 register to 0 (settings of CM06 bit and bits CM16 and CM17 enabled).

9.6.3 Peripheral Function Clocks (f1, f2, f4, f8, and f32)

These clocks are operating clocks for the peripheral functions.
fi (i = 1, 2, 4, 8, or 32) is obtained by dividing the system clock by i. fi is used for timer RJ, timer RB2, timer RC, timer RD, timer RE2, the serial interface, and the A/D converter.
When the MCU enters wait mode after the CM02 bit in the CM0 register are set to 1 (peripheral function clock stops in wait mode), fi is stopped.

9.6.4 fOCO

This clock is an operating clock for the peripheral functions.
This clock runs at the same frequency as the on-chip oscillator clock and can be used for timer RJ.
In wait mode, fOCO is not stopped.

9.6.5 fHOCO

This clock is used as the count source for timer RC and timer RD.
fHOCO is generated by the high-speed on-chip oscillator and supplied by setting the FRA00 bit in the FRA0 register to 1.
In wait mode, fHOCO is not stopped.

9.6.6 fHOCO-F

This clock is used as the count source for timer RC, timer RD, and the A/D converter.
fHOCO-F is a clock generated by the high-speed on-chip oscillator and divided by i (i = 2, 3, 4, 5, 6, 7, 8, or 9; division ratio selected by the FRA2 register), and it is supplied by setting the FRA00 bit to 1.
In wait mode, fHOCO-F is not stopped.

9.6.7 fLOCO

This clock is an operating clock for the voltage detecting circuit.
fLOCO is generated by the low-speed on-chip oscillator and supplied by setting the CM14 bit in the CM1 register o 0 (low-speed on-chip oscillator on).
In wait mode, fLOCO is not stopped.

9.6.8 fOCO128

This clock is generated by dividing fLOCO or fHOCO-F by 128. When the FRA03 bit in the FRA0 register is set to 0, fLOCO divided by 128 is selected. When this bit is set to 1, fHOCO-F divided by 128 is selected. fOCO128 is configured as the capture signal used in timer RC_0 for timer RC and timer RD_0 for timer RD.

9.6.9 fLOCOWDT

This is an operating clock for the watchdog timer.
fLOCOWDT is generated by the low-speed on-chip oscillator for the watchdog timer. This clock is supplied when CSPRO = 1 (count source protection mode enabled) or when CSPRO = 0 (count source protection mode disabled) and WDTC7 and WDTC6 = 11b (watchdog timer low-speed on-chip oscillator clock divided by 16). In count source protection mode for the watchdog timer, fLOCOWDT is not stopped.

9.6.10 CAN Clock

This is a communication clock for the CAN.
For details on the CAN clock, refer to **24.4.1 CAN Clock Configuration**.

9.7 Oscillation Stop Detection Function

The oscillation stop detection function is used to detect whether the XIN clock oscillation is stopped.
The oscillation stop detection function can be enabled or disabled with the OCD0 bit in the OCD register.
Table 9.7 lists the Oscillation Stop Detection Function Specifications.

When the XIN clock is the CPU clock source and bits OCD1 and OCD0 are 11b, if the XIN clock is stopped, the states will change as follows:
• Bits CM42 to CM40 in CM4 register = 001b (fLOCO)
• CM14 bit in CM1 register = 0 (low-speed on-chip oscillator on).
• An oscillation stop detection interrupt is generated

Table 9.7 Oscillation Stop Detection Function Specifications

Item	Specification
Clock frequency range for oscillation stop detection	f(XIN) ≥ 2 MHz
Condition for enabling the oscillation stop detection function	Set bits OCD1 and OCD0 in the OCD register to 11b.
Operation at oscillation stop detection	An oscillation stop detection interrupt is generated.

9.7.1 How to Use Oscillation Stop Detection Function

- The oscillation stop detection interrupt shares a vector with the watchdog timer, voltage monitor 1, and voltage monitor 2 interrupts. To use both the oscillation stop detection and watchdog timer interrupts, the interrupt source needs to be determined.
  Table 9.8 lists How to Determine Interrupt Source for Oscillation Stop Detection Interrupt, Watchdog Timer Interrupt, Voltage Monitor 1 Interrupt, or Voltage Monitor 2 Interrupt. Figure 9.7 shows an Example of How to Determine Interrupt Sources for Oscillation Stop Detection Interrupt, Watchdog Timer Interrupt, Voltage Monitor 1 Interrupt, or Voltage Monitor 2 Interrupt.
- When the XIN clock reoscillates after oscillation is stopped, switch the XIN clock to the clock source for the CPU clock and the peripheral functions by a program.
  Figure 9.6 shows the Procedure for Switching from Low-Speed On-Chip Oscillator to XIN Clock.
- When entering wait mode while using the oscillation stop detection function, set the CM02 bit in the CM0 register to 0 (peripheral function clock does not stop in wait mode).
- Since the oscillation stop detection function is a function for cases where the XIN clock is stopped by an external cause, set bits OCD1 and OCD0 to 00b to stop or oscillate the XIN clock by a program (to select stop mode or change the CM05 bit in the CM05 register).
- This function cannot be used when the XIN clock frequency is below 2 MHz. In this case, set bits OCD1 and OCD0 to 00b.
- To use the low-speed on-chip oscillator clock for the clock source for the CPU clock and the peripheral functions after oscillation stop is detected, set the OCD6 bit in the OCD register to 0 (low-speed on-chip oscillator selected) before setting bits OCD1 and OCD0 to 11b.
  To use the high-speed on-chip oscillator clock for the clock source for the CPU clock and the peripheral functions after oscillation stop is detected, set the FRA00 bit in the FRA0 register to 1 (high-speed on-chip oscillator on) and the OCD6 bit to 1 (high-speed on-chip oscillator selected) before setting bits OCD1 and OCD0 to 11b.

Table 9.8 How to Determine Interrupt Source for Oscillation Stop Detection Interrupt, Watchdog Timer Interrupt, Voltage Monitor 1 Interrupt, or Voltage Monitor 2 Interrupt

Item	Specification
Oscillation stop detection	OCD2 bit in OCD register = 1
Watchdog timer	UFIF bit in RISR register = 1
Voltage monitor 1	VW1C2 bit in VW1C register = 1
Voltage monitor 2	VW2C2 bit in VW2C register = 1

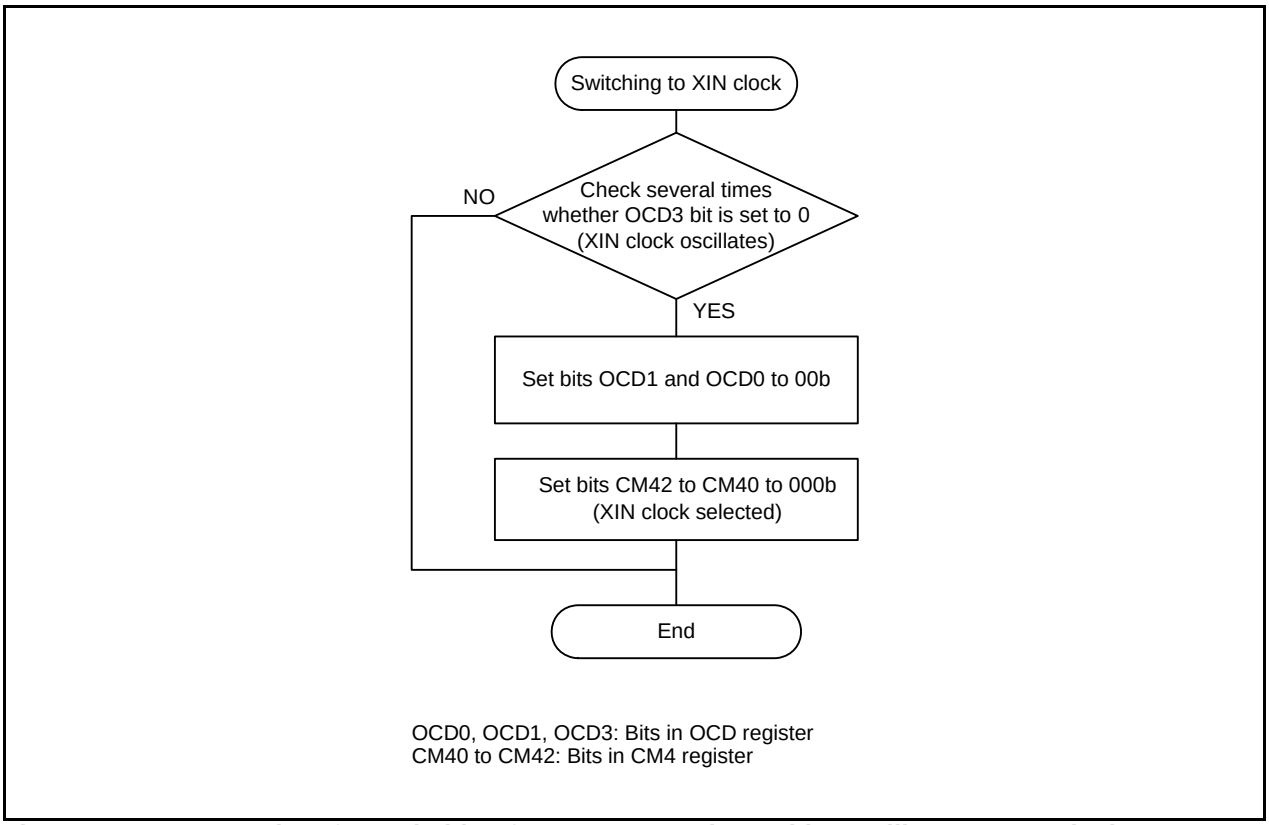
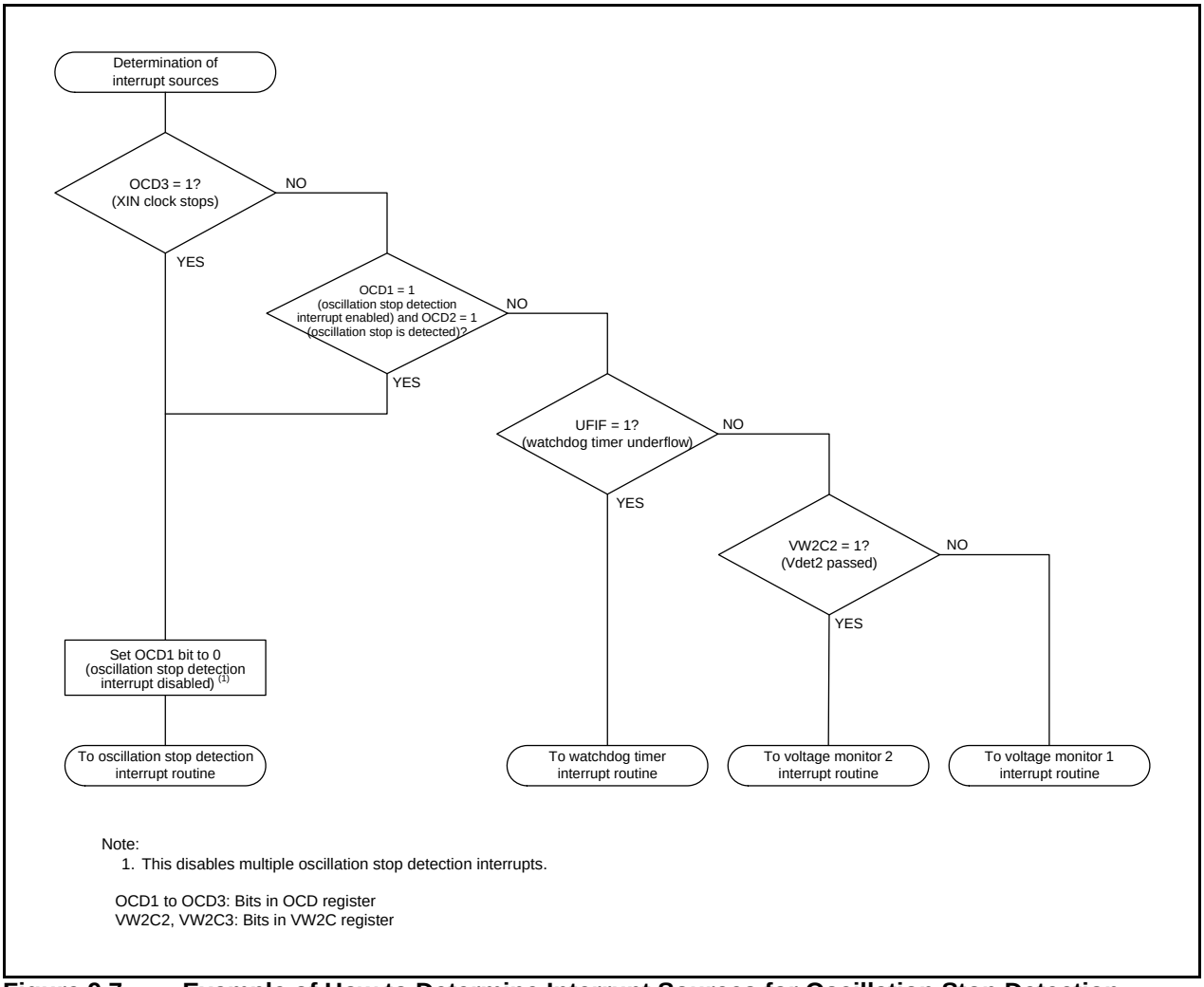


Figure 9.6 Procedure for Switching from Low-Speed On-Chip Oscillator to XIN Clock



Note:
1. This disables multiple oscillation stop detection interrupts.

OCD1 to OCD3: Bits in OCD register
VW2C2, VW2C3: Bits in VW2C register

Figure 9.7 Example of How to Determine Interrupt Sources for Oscillation Stop Detection Interrupt, Watchdog Timer Interrupt, Voltage Monitor 1 Interrupt, or Voltage Monitor 2 Interrupt

9.8 Notes on Clock Generation Circuit

9.8.1 Oscillation Stop Detection Function

The oscillation stop detection function cannot be used when the XIN clock frequency is below 2 MHz. In this case, set bits OCD1 and OCD0 in the OCD register to 00b (applicable: bits OCD2 and OCD3).

9.8.2 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system.

10. Power Control

Power control refers to the control of power consumption by selecting or stopping the CPU clock and the peripheral function clocks.

10.1 Overview

There are three power control modes. All modes other than wait mode and stop mode will be referred to here as standard operating mode.
Figure 10.1 shows the State Transitions in Power Control Mode.

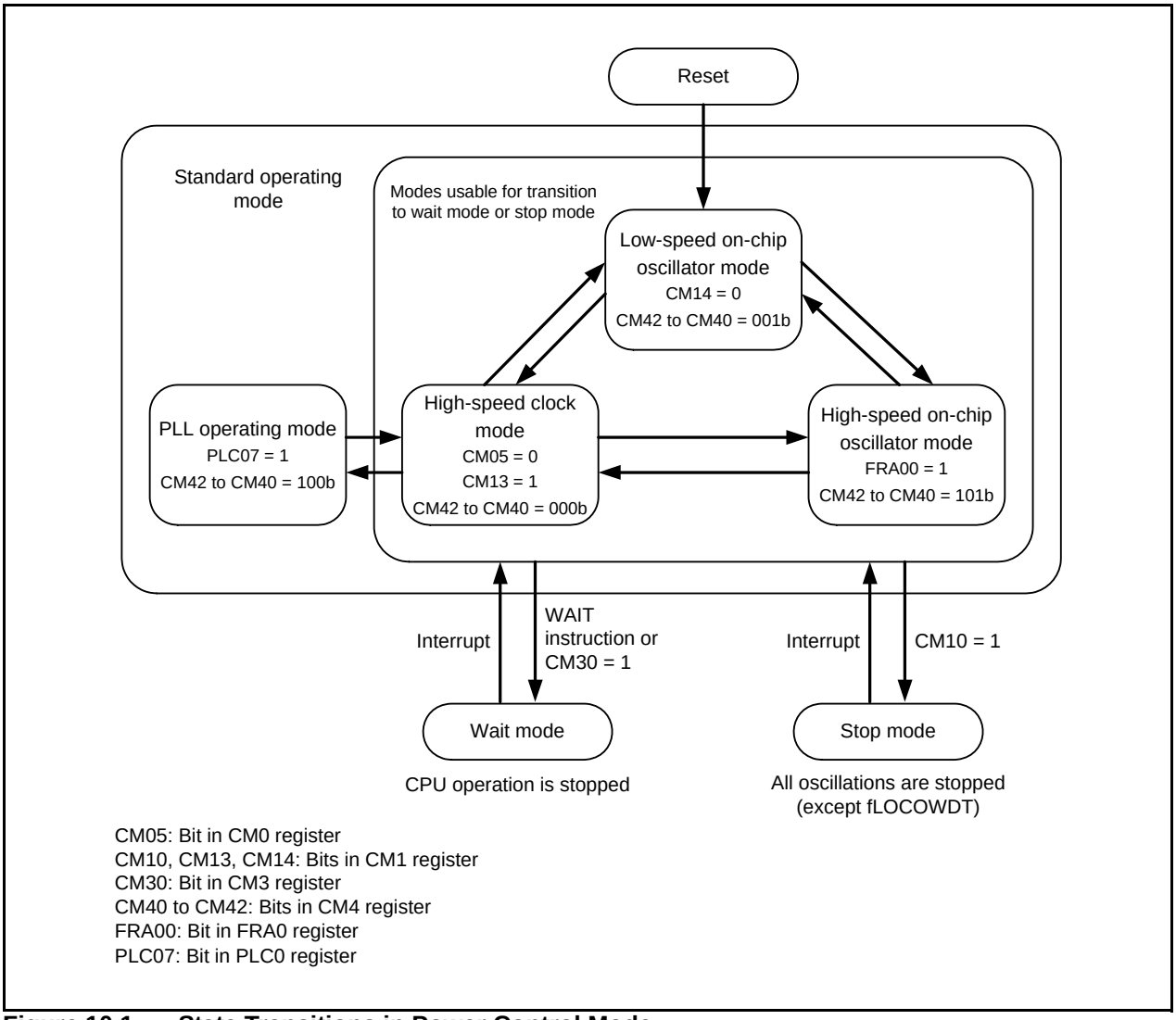


Figure 10.1 State Transitions in Power Control Mode

10.2 Registers

Table 10.1 lists the Register Configuration for Power Control.

Table 10.1 Register Configuration for Power Control

Register Name	Symbol	After Reset	Address	Access Size
System Clock Control Register 0	CM0	00101000b	00008h	8
System Clock Control Register 1	CM1	00100000b	00009h	8
System Clock Control Register 3	CM3	00h	0000Bh	8
System Clock Control Register 4	CM4	00000001b	0000Ch	8
High-Speed On-Chip Oscillator Control Register 0	FRA0	00h	00012h	8
STBY VDC Power Control Register	SVDC	00h	0002Ch	8
Module Standby Control Register 0	MSTCR0	00h	00238h	8
Module Standby Control Register 1	MSTCR1	00h	00239h	8
Module Standby Control Register 2	MSTCR2	00h	0023Ah	8
Module Standby Control Register 3	MSTCR3	00h	0023Bh	8

10.2.1 System Clock Control Register 0 (CM0)

Address 00008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM07	CM06	CM05	—	—	CM02	—	—
After Reset	0	0	1	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			R/W
b2	CM02	Peripheral function clock stop bit in wait mode	0: Peripheral function clock does not stop in wait mode 1: Peripheral function clock stops in wait mode	R/W
b3	—	Reserved	Set to 1.	R/W
b4	—	Reserved	Set to 0.	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit (1, 2)	0: Oscillates 1: Stops (3)	R/W
b6	CM06	CPU clock division ratio select bit 0 (4)	0: Bits CM16 and CM17 in CM1 register enabled 1: Divide-by-8 mode	R/W
b7	CM07	XIN clock supply set bit (5)	0: XIN clock is supplied by oscillator (external ceramic resonator, etc.) 1: XIN clock is supplied by external clock input to XOUT pin	R/W

Notes:
1. The CM05 bit is used to stop the XIN clock. This bit cannot be used to detect whether the XIN clock has stopped. To stop the XIN clock, make the following settings:
   (1) Set bits OCD1 and OCD0 in the OCD register to 00b (oscillation stop detection function disabled).
   (2) Set bits CM42 to CM40 in the CM4 register to 001b (fLOCO clock) or 101b (fHOCO-F clock).
2. P4_6 and P4_7 can be used as I/O ports only when the CM05 bit is 1 (XIN clock stops) and the CM13 bit in the CM1 register is 0 (P4_6 and P4_7).
3. When an external clock is input, the clock input itself is not accepted.
4. When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode).
5. When the MCU exits stop mode or wait mode, do not set the CM05 bit to 1 (XIN clock stops) if switching to the XIN clock.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM0 register.

10.2.2 System Clock Control Register 1 (CM1)

Address 00009h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM17	CM16	—	CM14	CM13	—	CM11	CM10
After Reset	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM10	All clock stop control bit (1, 2)	0: Clocks oscillate 1: All clocks stop (stop mode)	R/W
b1	CM11	XIN-XOUT on-chip feedback resistor select bit	0: On-chip feedback resistor enabled 1: On-chip feedback resistor disabled	R/W
b2	—	Reserved	Set to 0.	R/W
b3	CM13	Port/XIN-XOUT switch bit (3)	0: I/O ports P4_6 and P4_7 1: XIN-XOUT pin	R/W
b4	CM14	Low-speed on-chip oscillator oscillation stop bit (4, 5)	0: Low-speed on-chip oscillator on 1: Low-speed on-chip oscillator off	R/W
b5	—	Reserved	Set to 1.	R/W
b6	CM16	CPU clock division select bits 1 (6)	b7 b6 0 0: Divide-by-1 mode 0 1: Divide-by-2 mode 1 0: Divide-by-4 mode 1 1: Divide-by-16 mode	R/W
b7	CM17			R/W

Notes:

1. If the CM10 bit is 1 (stop mode), the on-chip feedback register is disabled. If the CM10 bit is 1 (stop mode), when the CM13 bit is 1 (XIN-XOUT pin), pins XIN (P4_6) and XOUT (P4_7) are set to high impedance.
2. When the SVC0 bit in the SVDC register is 1 (transition to low-power-consumption mode enabled), do not set the CM10 bit to 1 (stop mode).
3. Once the CM13 bit is set to 1 by a program, it cannot be set to 0. Set the CM13 bit to 1 to use P4_6 and P4_7 as the XIN-XOUT pin.
4. The CM14 bit can be set to 1 (low-speed on-chip oscillator off) when bits CM42 to CM40 in the CM4 register are 000b (XIN clock). When bits CM42 to CM40 are set to 001b (fLOCO clock), the CM14 bit is set to 0 (low-speed on-chip oscillator on). Writing 1 to this bit has no effect.
5. To use a voltage monitor 1 interrupt or a voltage monitor 2 interrupt (when the digital filter is used), set the CM14 bit to 0 (low-speed on-chip oscillator on).
6. When the CM06 bit in the CM0 register is 0 (bits CM16 and CM17 enabled), bits CM16 and CM17 are enabled.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM1 register.

10.2.3 System Clock Control Register 3 (CM3)

Address 0000Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM37	CM36	CM35	—	—	—	—	CM30
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM30	Wait control bit (1)	0: Not in wait mode 1: MCU enters wait mode	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	—			
b5	CM35	CPU clock division ratio select bit when exiting wait mode (2)	0: Settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled 1: No division	R/W
b6	CM36	System clock select bits when exiting wait mode or stop mode (3)	b7 b6 0 0: MCU exits using the CPU clock used immediately before entering wait mode or stop mode 0 1: Do not set. 1 0: High-speed on-chip oscillator clock selected (4) 1 1: XIN clock selected (5)	R/W
b7	CM37			R/W

Notes:

1. When the MCU exits wait mode by a peripheral function interrupt, the CM30 bit is set to 0 (not in wait mode).
2. Set the CM35 bit to 0 in stop mode. When the MCU enters wait mode, if the CM35 bit is 1 (no division), the CM06 bit in the CM0 register is set to 0 (bits CM16 and CM17 in CM1 register enabled) and bits CM17 and CM16 are set to 00b (divide-by-1 mode).
3. To enter wait mode or stop mode while the FMR27 bit in the FMR2 register is 1 (flash memory low-current-consumption read mode enabled), set bits CM37 and CM36 to 00b (MCU exits using the CPU clock used immediately before entering wait mode or stop mode) and set the CM35 bit to 0 (settings of CM06 bit in CM0 register and bits CM16b and CM17 in CM1 register enabled). During low-current-consumption read mode, do not set the FMSTP bit in the FMR0 register to 1 (flash memory stops).
4. When bits CM37 and CM36 are set to 10b (high-speed on-chip oscillator clock selected), the following will be set when the MCU exits wait mode or stop mode.
   • Bits CM42 to CM40 in CM4 register = 001b (fLOCO clock)
   • FRA00 bit in FRA0 register (high-speed on-chip oscillator on)
   • Bits CM42 to CM40 in CM4 register = 101b (fHOCO-F clock)
5. When bits CM37 and CM36 are set to 11b (XIN clock selected), the following will be set when the MCU exits wait mode or stop mode.
   • CM05 bit in CM0 register = 1 (XIN clock oscillates)
   • CM13 bit in CM1 register = 1 (XIN-XOUT pin)
   • Bits CM42 to CM40 in CM4 register = 000b (XIN clock selected)
   When entering wait mode while the CM05 bit in the CM0 register is 1 (XIN clock stops), if the XIN clock is selected as the CPU clock used to exit wait mode, set the CM06 bit to 1 (divide-by-8 mode) and the CM35 bit to 0.
   However, if an externally generated clock is used as the XIN clock, do not set bits CM37 and CM36 to 11b (XIN clock selected).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM3 register.

CM30 Bit (Wait control bit)

When the CM30 bit is set to 1 (MCU enters wait mode), the CPU clock stops (wait mode). Since the XIN, low-speed on-chip oscillator, high-speed on-chip oscillator, and watchdog timer low-speed on-chip oscillator clocks do not stop, the peripheral functions that use these clocks continue operating. When setting the CM30 bit to 1, set the I flag to 0 (maskable interrupt disabled).

A reset or a peripheral function interrupt is used to exit wait mode. When a peripheral function interrupt is used to exit wait mode, the MCU resumes executing the instruction immediately after the instruction to set the CM30 bit to 1.

However, when using the WAIT mode to enter wait mode, set the I flag to 1 (maskable interrupt enabled). With this setting, interrupt handling is performed by the CPU when the MCU exits wait mode.

10.2.4 System Clock Control Register 4 (CM4)

Address 0000Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	CM42	CM41	CM40
After Reset	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	CM40	CPU clock select bits (1)	b2 b1 b0 0 0 0: XIN clock 0 0 1: fLOCO clock 0 1 0: Do not set. 0 1 1: Do not set. 1 0 0: PLL clock 1 0 1: fHOCO-F clock Other than the above: Do not set.	R/W
b1	CM41			R/W
b2	CM42			R/W
b3	—	Reserved	Set to 0.	R/W
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. For details, refer to **Figure 10.1 State Transitions in Power Control Mode**.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before setting the CM4 register.

10.2.5 High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Address 00012h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	FRA03	—	FRA01	FRA00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	0: High-speed on-chip oscillator off 1: High-speed on-chip oscillator on	R/W
b1	FRA01	fOCO clock source select bit (1)	0: Low-speed on-chip oscillator selected (2) 1: High-speed on-chip oscillator selected	R/W
b2	—	Reserved	Set to 0.	R/W
b3	FRA03	fOCO128 clock select bit	0: fLOCO divided by 128 selected 1: fHOCO-F divided by 128 selected	R/W
b4	—	Reserved	Set to 0.	R/W
b5	—			
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

Notes:
1. Set the FRA01 bit under the following conditions:
   - FRA00 bit = 1 (high-speed on-chip oscillator on)
   - CM14 bit in the CM1 register = 0 (low-speed on-chip oscillator on)
   - Bits FRA22 to FRA20 in the FRA2 register:
     All division modes can be set when VCC = 2.7 to 5.5 V: 000b to 111b
2. When writing 0 (low-speed on-chip oscillator selected) to the FRA01 bit, do not write 0 (high-speed on-chip oscillator off) to the FRA00 bit at the same time. After the FRA01 bit is set to 0, set the FRA00 bit to 0.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA0 register.

10.2.6 STBY VDC Power Control Register (SVDC)

Address 0002Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	SVC0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SVC0	Low-power-consumption mode transition enabled bit	0: Transition to low-power-consumption mode disabled 1: Transition to low-power-consumption mode enabled	R/W
b1	—	Reserved	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the SVDC register.

10.2.7 Module Standby Control Register 0 (MSTCR0)

Address 00238h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	MSTURT2	—	—	MSTURT_1	MSTURT_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MSTURT_0	UART0_0 module standby bit	0: UART0_0 normal operation 1: UART0_0 standby	R/W
b1	MSTURT_1	UART0_1 module standby bit	0: UART0_1 normal operation 1: UART0_1 standby	R/W
b2	—	Reserved	Set to 0.	R/W
b3	—			
b4	MSTURT2	UART2 module standby bit	0: UART2 normal operation 1: UART2 standby	R/W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	—			
b7	—			

10.2.8 Module Standby Control Register 1 (MSTCR1)

Address 00239h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	MSTIIC_1	MSTIIC_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MSTIIC_0	IICSSU_0 module standby bit	0: IICSSU_0 normal operation 1: IICSSU_0 standby	R/W
b1	MSTIIC_1	IICSSU_1 module standby bit	0: IICSSU_1 normal operation 1: IICSSU_1 standby	R/W
b2	—	Reserved	Set to 0.	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

10.2.9 Module Standby Control Register 2 (MSTCR2)

Address 0023Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	MSTTRC_0	—	MSTTRB_0	—	—	MSTTRJ_1	MSTTRJ_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MSTTRJ_0	Timer RJ_0 module standby bit	0: Timer RJ_0 normal operation 1: Timer RJ_0 standby	R/W
b1	MSTTRJ_1	Timer RJ_1 module standby bit	0: Timer RJ_1 normal operation 1: Timer RJ_1 standby	R/W
b2	—	Reserved	Set to 0.	R/W
b3	—			
b4	MSTTRB_0	Timer RB2_0 module standby bit	0: Timer RB2_0 normal operation 1: Timer RB2_0 standby	R/W
b5	—	Reserved	Set to 0.	R/W
b6	MSTTRC_0	Timer RC_0 module standby bit	0: Timer RC_0 normal operation 1: Timer RC_0 standby	R/W
b7	—	Reserved	Set to 1.	R/W

10.2.10 Module Standby Control Register 3 (MSTCR3)

Address 0023Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	MSTTRE	—	MSTTRD_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MSTTRD_0	Timer RD_0 module standby bit	0: Timer RD_0 normal operation 1: Timer RD_0 standby	R/W
b1	—	Reserved	Set to 0.	R/W
b2	MSTTRE	Timer RE2 module standby bit	0: Timer RE2 normal operation 1: Timer RE2 standby	R/W
b3	—	Reserved	Set to 1.	R/W
b4	—			
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	—			
b7	—			

10.3 Standard Operating Mode

Standard operating mode is further divided into four modes.
In standard operating mode, the CPU clock and the peripheral function clock are supplied to operate the CPU and the peripheral functions. Power consumption control is implemented by controlling the frequency of the CPU clock. To operate the peripheral functions using a clock other than the peripheral clocks (f1, f2, f4, f8, and f32), the oscillation of the target clock needs to be stable. The higher the CPU clock frequency, the higher processing power. The lower the CPU clock frequency, the lower the power consumption. Stopping unnecessary oscillation circuits will further reduce power consumption.
When the clock sources for the CPU clock are switched, the new clock needs to be oscillating and stable. Allow the new clock oscillation to stabilize in a program before switching the clocks.

Table 10.2 Settings and Modes of Clock Associated Bits

Mode		CM4 Register	CM1 Register			CM0 Register	FRA0 Register	PLC0 Register
		Bits CM42 to CM40	Bits CM17 and CM16	CM14 Bit	CM13 Bit	CM06 Bit	FRA00 Bit	PLC07 Bit
High-speed clock mode	No division	000b	00b	—	1	0	—	—
	Divide-by-2	000b	01b	—	1	0	—	—
	Divide-by-4	000b	10b	—	1	0	—	—
	Divide-by-8	000b	—	—	1	1	—	—
	Divide-by-16	000b	11b	—	1	0	—	—
High-speed on-chip oscillator mode	No division	101b	00b	—	—	0	1	—
	Divide-by-2	101b	01b	—	—	0	1	—
	Divide-by-4	101b	10b	—	—	0	1	—
	Divide-by-8	101b	—	—	—	1	1	—
	Divide-by-16	101b	11b	—	—	0	1	—
Low-speed on-chip oscillator mode	No division	001b	00b	0	—	0	—	—
	Divide-by-2	001b	01b	0	—	0	—	—
	Divide-by-4	001b	10b	0	—	0	—	—
	Divide-by-8	001b	—	0	—	1	—	—
	Divide-by-16	001b	11b	0	—	0	—	—
PLL operating mode	No division	100b	00b	—	1	0	—	1
	Divide-by-2	100b	01b	—	1	0	—	1
	Divide-by-4	100b	10b	—	1	0	—	1
	Divide-by-8	100b	—	—	1	1	—	1
	Divide-by-16	100b	11b	—	1	0	—	1

—: Indicates that either 0 or 1 can be set

10.3.1 High-Speed Clock Mode

When the CM13 bit in the CM1 register is 1 (XIN-XOUT pin) and bits CM42 to CM40 in the CM4 register are 000b, the XIN clock is used as the system clock, and the CPU clock is obtained by dividing the system clock by 1 (no division), 2, 4, 8, or 16.

10.3.2 High-Speed On-Chip Oscillator Mode

When the FRA00 bit is 1 (high-speed on-chip oscillator on) and bits CM42 to CM40 in the CM4 register are 101b, the high-speed on-chip oscillator is used as the system clock. At this time, the CPU clock is obtained by dividing the system clock by 1 (no division), 2, 4, 8, or 16.

10.3.3 Low-Speed On-Chip Oscillator Mode

When the CM14 bit is 0 (low-speed on-chip oscillator on) and bits CM42 to CM40 are 001b, the low-speed on-chip oscillator is used as the system clock. At this time, the CPU clock is obtained by dividing the system clock by 1 (no division), 2, 4, 8, or 16.

In this mode, low-power operation can be enabled by stopping the XIN clock and the high-speed on-chip oscillator and setting the FMR27 bit to 1 (low-current-consumption read mode enabled). Low-power-consumption mode can be used when the CPU clock is the low-speed on-chip oscillator divided by 4, 8 or 16. When the CPU clock is the low-speed on-chip oscillator divided by 1 (no division) or 2, do not use low-power-consumption mode. Set the FMR27 bit to 1 after setting the division ratio for the CPU clock.

Furthermore, if the MCU enters wait mode from this mode, current consumption in wait mode can be reduced even further by setting the SVD0 bit to 1 (transition to low-power-consumption mode enabled).

For details on how to reduce power consumption, refer to **10.6 Reducing Power Consumption**.

10.3.4 PLL Operating Mode

When the PLC07 bit in the PLC0 register is 1 (PLL operates) and bits CM42 to CM40 in the CM4 register are 100b, the PLL is used as the system clock, and the CPU clock is obtained by dividing the system clock by 1 (no division), 2, 4, 8, or 16.

10.4 Wait Mode

The CPU clock is stopped in wait mode. Thus the CPU, which operates using the CPU clock, and the watchdog timer with the CPU clock selected as the count source are stopped. The oscillations of the XIN clock, high-speed on-chip oscillator, low-speed on-chip oscillator, and watchdog timer low-speed on-chip oscillator are not stopped, so the peripheral functions that use these clocks continue operating.

10.4.1 Peripheral Function Clock Stop Function

When the CM02 bit in the CM0 register is 1 (peripheral function clock stops in wait mode), power consumption is reduced because f1, f2, f4, f8, and f32 are stopped in wait mode.

10.4.2 Entering Wait Mode

The MCU enters wait mode when the WAIT instruction is executed or the CM30 bit in the CM3 register is set to 1 (MCU enters wait mode).

When bits CM42 to CM40 bit in the CM4 register are set to 001b (fLOCO selected as CPU clock) or 101b (fHOCO-F clock selected as CPU clock), set the OCD1 bit in the OCD register to 0 (oscillation stop detection disabled) before executing the WAIT instruction or set the CM30 bit to 1 (MCU enters wait mode).

If the MCU enters wait mode while the OCD1 bit is 1 (oscillation stop detection enabled), power consumption is not reduced because the CPU is not stopped.

To enter wait mode or stop mode while the FMR27 bit in the FMR2 register is 1 (low-current-consumption read mode enabled), set bits CM37 and CM36 in the CM3 register to 00b (MUC exits using the CPU clock used immediately before entering wait mode or stop mode) and the CM35 bit in the CM3 register to 0 (settings of CM06 bit in CM0 register and bits CM16b and CM17 in CM1 register enabled).

10.4.3 Pin States in Wait Mode

The I/O ports retain the states immediately before the MCU enters wait mode.

10.4.4 Exiting Wait Mode

A reset or a peripheral function interrupt is used to exit wait mode.

Peripheral function interrupts are affected by the CM02 bit in the CM0 register. When the CM02 bit is 0 (peripheral function clock does not stop in wait mode), peripheral function interrupts other the A/D conversion interrupt can be used to exit wait mode. When the CM02 bit is 1 (peripheral function clock stops in wait mode), the peripheral functions that use the peripheral function clock are stopped. Only the peripheral function interrupts that operate using external signals or the fHOCO, fOCO128, fOCO, fHOCO-F, and fLOCOWDT clocks can be used to exit wait mode.

Table 10.3 lists the Interrupts Used to Exit Wait Mode and Usage Conditions.

Table 10.3 Interrupts Used to Exit Wait Mode and Usage Conditions

Interrupt	When CM02 = 0	When CM02 = 1
Serial interface interrupt	Usable with an internal clock or external clock supplied.	Usable with an external clock supplied.
Synchronous serial communication unit/I^2C bus interface	Usable in all modes.	— (Do not use.)
Key input interrupt	Usable	Usable
A/D interrupt	— (Do not use.)	— (Do not use.)
Timer RJ interrupt	Usable in all modes.	Usable without a filter in event counter mode. Usable when fOCO is selected as the count source.
Timer RB2 interrupt	Usable in all modes.	— (Do not use.)
Timer RC interrupt	Usable in all modes.	Usable when fHOCO or fHOCO-F is selected as the count source.
Timer RD interrupt	Usable in all modes.	Usable when fHOCO or fHOCO-F is selected as the count source.
Timer RE2 interrupt	Usable in all modes.	— (Do not use.)
$\overline{INT}$ interrupt	Usable	Usable (usable when $\overline{INT0}$ to $\overline{INT4}$ are used without a filter.)
Voltage monitor 1 interrupt	Usable	Usable
Voltage monitor 2 interrupt	Usable	Usable
Oscillation stop detection interrupt	Usable	— (Do not use.)
CAN wake-up interrupt	Usable	Usable

Figure 10.2 shows the Time from Wait Mode to First Instruction Execution after Exit after CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode).
To use a peripheral function interrupt to exit wait mode, the following items must be set before setting the CM30 bit to 1:

(1) Set the I flag in the FLG register to 0 (maskable interrupts disabled).
(2) Set the interrupt priority level in bits ILVL0 to ILVL2 in the interrupt priority level registers for the peripheral function interrupts that are used to exit wait mode. Also, set 000b (interrupt disabled) in bits ILVL2 to ILVL0 in the interrupt priority level registers for the peripheral function interrupts that are not to be used to exit wait mode.
(3) Operate the peripheral functions to be used to exit wait mode.

When a peripheral function interrupt is used to exit, the time (number of cycles) from interrupt request generation to the next instruction execution is as shown in Figure 10.2, depending on the settings of the FMSTP bit in the FMR0 register and the SVC0 bit in the SVDC register.
The CPU clock when a peripheral function interrupt is used to exit wait mode is the clock set by bits CM35, CM36, and CM37 in the CM3 register. At this time, the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register are automatically changed.

FMR0 Register FMSTP Bit	SVDC Register SVC0 Bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T1)	Time until CPU Clock Supply (T2)	Remarks
0 (flash memory operates)	0 (transition to low-power consumption mode disabled)	0 μs	Period of system clock × 1 cycle + 60 μs (max.)	Period of CPU clock × 2 cycles	The total on the left amounts to the time from wait mode until the first instruction is executed after exiting.
	1 (transition to low-power consumption mode enabled)	100 μs (max.)			
1 (flash memory stops)	0 (transition to low-power consumption mode disabled)	0 μs	Period of system clock × 1 cycle	Same as above	
	1 (transition to low-power consumption mode enabled)	100 μs (max.)			

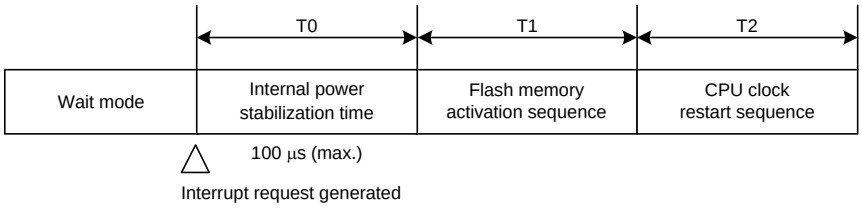


Figure 10.2 Time from Wait Mode to First Instruction Execution after Exit after CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode)

Figure 10.3 shows the Time from Wait Mode after WAIT Instruction Execution to Interrupt Routine Execution. To use a peripheral function interrupt to exit wait mode, the following items must be set before executing the WAIT instruction:

(1) Set the interrupt priority level in bits ILVL0 to ILVL2 in the interrupt priority level registers for the peripheral function interrupts that are used to exit wait mode. Also, set 000b (interrupt disabled) in bits ILVL2 to ILVL0 for the peripheral function interrupts that are not to be used to exit wait mode.
(2) Operate the peripheral functions to be used to exit wait mode.
(3) Set the I flag in the FLG register to 1.

When a peripheral function interrupt is used to exit, the time (number of cycles) from interrupt request generation to the next instruction execution is as shown in Figure 10.3, depending on the settings of the FMSTP bit in the FMR0 register and the SVC0 bit in the SVDC register.
The CPU clock when a peripheral function interrupt is used to exit wait mode is the clock set by bits CM35, CM36, and CM37 in the CM3 register. At this time, the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register are automatically changed.

FMR0 Register FMSTP Bit	SVDC Register SVC0 Bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T1)	Time until CPU Clock Supply (T2)	Time for Interrupt Sequence (T3)	Remarks
0 (flash memory operates)	0 (transition to low-power consumption mode disabled)	0 μs	Period of system clock × 1 cycle + 60 μs (max.)	Period of CPU clock × 2 cycles	Period of CPU clock × 20 cycles	The total on the left amounts to the time from wait mode to interrupt routine execution.
	1 (transition to low-power consumption mode enabled)	100 μs (max.)				
1 (flash memory stops)	0 (transition to low-power consumption mode disabled)	0μs	Period of system clock × 1 cycle	Same as above	Same as above	
	1 (transition to low-power consumption mode enabled)	100 μs (max.)				

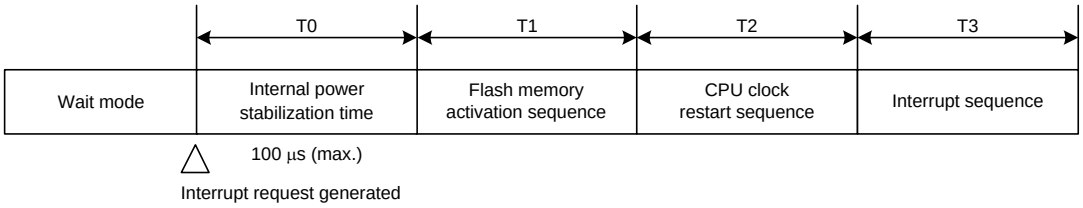


Figure 10.3 Time from Wait Mode after WAIT Instruction Execution to Interrupt Routine Execution

10.5 Stop Mode

All oscillators except fLOCOWDT are stopped in stop mode. Thus, the CPU clock and the peripheral function clock are stopped and the CPU and the peripheral functions that operate using these clocks are stopped. Power consumption is lowest compared to other modes. When the voltage applied to the VCC pin is VRAM or above, the content of the internal RAM is retained.
The peripheral functions clocked by external signals continue operating.
Table 10.4 lists the Interrupts Used to Exit Stop Mode and Usage Conditions.

Table 10.4 Interrupts Used to Exit Stop Mode and Usage Conditions

Interrupt	Usage Condition
Key input interrupt	Usable
$\overline{\text{INT0}}$ to $\overline{\text{INT4}}$ interrupts	Usable without a filter.
Timer RJ interrupt	Usable when an external pulse is counted without a filter in event counter mode.
Serial interface interrupt	When an external clock is selected.
Voltage monitor 1 interrupt	Usable in digital filter disabled mode (when the VW1C1 bit in the VW1C register is 1).
Voltage monitor 2 interrupt	Usable in digital filter disabled mode (when the VW2C1 bit in the VW2C register is 1).
CAN wake-up interrupt	Usable without a filter.

10.5.1 Entering Stop Mode

The MCU enters stop mode when the CM10 bit in the CM1 register is set to 1 (all clocks stop). At the same time, the CM06 bit in the CM0 register is set to 1 (divide-by-8 mode).
To use stop mode, set bits OCD1 and OCD0 in the OCD register to 00b and the CM35 bit in the CM3 register to 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled) before entering the mode.
To enter wait mode or stop mode while the FMR27 bit in the FMR2 register is 1 (low-current-consumption read mode enabled), set bits CM37 and CM36 to 00b (MCU exits using the CPU clock used immediately before entering wait mode or stop mode) and the CM35 bit to 0.

10.5.2 Pin States in Stop Mode

The I/O ports retain the states immediately before the MCU enters stop mode.
However, when the CM13 bit in the CM1 register is set to 1 (XIN-XOUT pin), pins XIN (P4_6) and XOUT (P4_7) are set to high impedance.

10.5.3 Exiting Stop Mode

A reset or a peripheral function interrupt is used to exit stop mode.
Figure 10.4 shows the Time from Stop Mode to Interrupt Routine Execution.
To use a peripheral function interrupt to exit stop mode, the following items must be set before setting the CM10 bit in the CM1 register to 1:

(1) Set the interrupt priority level in bits ILVL0 to ILVL2 in the interrupt priority level registers for the peripheral function interrupts that are used to exit stop mode.
Also, set 000b (interrupt disabled) in bits ILVL0 to ILVL2 in the interrupt priority level registers for the peripheral function interrupts that are not to be used to exit stop mode.
(2) Operate the peripheral functions to be used to exit stop mode.
(3) Set the I flag in the FLG register to 1.

When a peripheral function interrupt is used to exit stop mode, the interrupt sequence is executed after the interrupt request is generated and the supply of the CPU clock starts.
The CPU clock when a peripheral function interrupt is used to exit stop mode is a divide-by-8 of the clock used immediately before entering stop mode. When entering stop mode, set the CM35 bit in the CM3 register to 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled).

FMR0 Register FMSTP Bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T2)	Time until CPU Clock Supply (T3)	Time for Interrupt Sequence (T4)	Remarks
0 (flash memory operates)	100 μs (max.)	Period of system clock × 1 cycle + 60 μs (max.)	Period of CPU clock × 2 cycles	Period of CPU clock × 20 cycles	The total of T0 to T4 amounts to the time from stop mode to interrupt routine execution.
1 (flash memory stops)	100 μs (max.)	Period of system clock × 1 cycle	Same as above	Same as above	

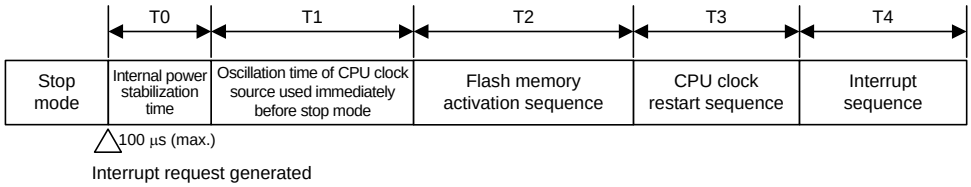


Figure 10.4 Time from Stop Mode to Interrupt Routine Execution

10.6 Reducing Power Consumption

The following describes key points and processing methods for reducing power consumption.

10.6.1 Voltage Detection Circuit

If voltage monitor 1 is not used, set the VCA26 bit in the VCA2 register to 0 (voltage detection 1 circuit disabled). If voltage monitor 2 is not used, set the VCA27 bit in the VCA2 register to 0 (voltage detection 2 circuit disabled).
If the power-on reset and voltage monitor 0 reset are not used, set the VCA25 bit in the VCA2 register to 0 (voltage detection 0 circuit disabled).

10.6.2 Ports

Even after the MCU enters wait mode or stop mode, the states of the I/O ports are retained. Current flows into the output ports in the active state. Shoot-through current flows into the input ports in the high-impedance state. Unnecessary ports should be set to input and fixed to a stable electric potential before the MCU enters wait mode or stop mode.

10.6.3 Clocks

Power consumption generally depends on the number of the operating clocks and their frequencies. The fewer the number of operating clocks or the lower their frequencies, the more power consumption decreases.
For that reason, unnecessary clocks should be stopped.

Stopping low-speed on-chip oscillator oscillation: CM14 bit in CM1 register
Stopping high-speed on-chip oscillator oscillation: FRA00 bit in FRA0 register
Stopping PLL: PLC07 bit in PLC0 register

10.6.4 Wait Mode, Stop Mode

Power consumption can be reduced in wait mode and stop mode. For details, refer to **10.4 Wait Mode** and **10.5 Stop Mode**.

10.6.5 Stopping Peripheral Function Clocks

If the peripheral function f1, f2, f4, f8, and f32 clocks are not necessary in wait mode, set the CM02 bit in the CM0 register to 1 (peripheral function clock stops in wait mode). This will stop the f1, f2, f4, f8, and f32 clocks in wait mode.

10.6.6 Timers

When timer RJ_i (i = 0 or 1) is not used, set the corresponding MSTTRJ_i bit in the MSTCR2 register for the unused timer RJ to 1 (standby).
When timer RB2 is not used, set the corresponding MSTTRB_0 bit in the MSTCR2 register for the unused timer RB2 to 1 (standby).
When timer RC is not used, set the corresponding MSTTRC_0 bit in the MSTCR2 register for the unused timer RC to 1 (standby).
Set the corresponding MSTTRC_0 bit in the MSTCR2 register for the unused timer RC to 1 (standby). Also, set bit 7 in the MSTCR2 register to 1.
When timer RD is not used, set the corresponding MSTTRD_0 bit in the MSTCR3 register for the unused timer RD to 1 (standby).
When timer RE2 is not used, set the MSTTRE bit in the MSTCR3 register to 1 (standby).

Set bit 3 and bit 4 in the MSTCR3 register to 1.

10.6.7 A/D Converter

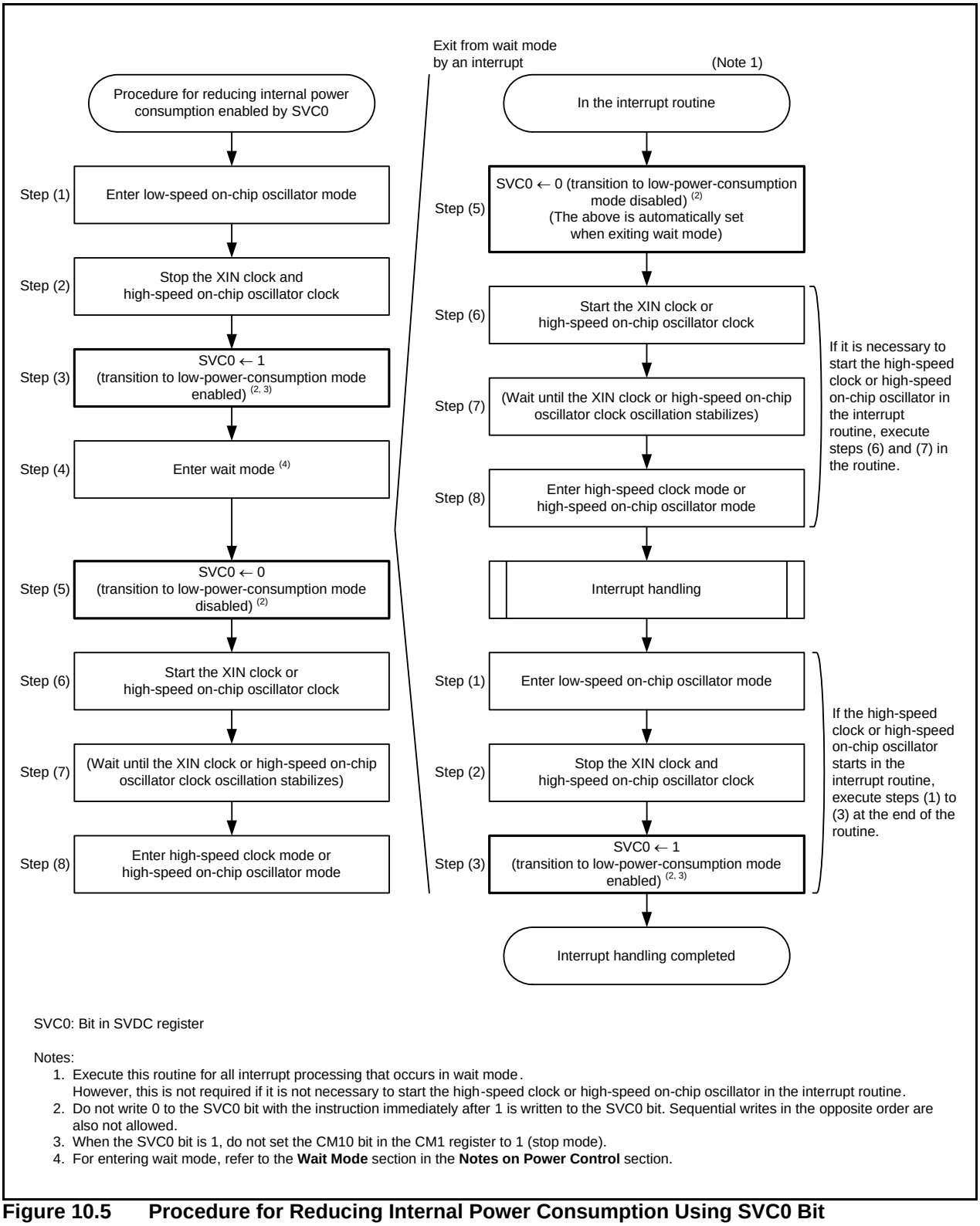
When the A/D converter is not used, power consumption can be reduced by setting the ADSTBY bit in the ADCON1 register to 0 (A/D operation stops (standby)) to shut off any analog circuit current flow.

10.6.8 Clock Synchronous Serial Interface and Serial Interfaces

When both the SSU and I^2C bus functions are not used, set the corresponding MSTIIC_i (i = 0 or 1) bit in the MSTCR1 register for the unused SSU function or the I^2C bus function to 1 (standby).
When UART0 is not used, set the corresponding MSTURT_i bit in the MSTCR0 register for the unused UART0 to 1 (standby).
When UART2 is not used, set the MSTURT2 bit in the MSTCR0 register to 1 (standby).

10.6.9 Reducing Internal Power Consumption (Low-Power-Consumption Mode)

When entering wait mode using low-speed on-chip oscillator mode (the oscillations of the XIN clock and the high-speed on-chip oscillator are stopped), internal power consumption can be reduced using the SVC0 bit in the SVDC register. Figure 10.5 shows the Procedure for Reducing Internal Power Consumption Using SVC0 Bit. To enable the transition to low-power-consumption mode using the SVC0 bit, follow this procedure.



SVC0: Bit in SVDC register

Notes:
1. Execute this routine for all interrupt processing that occurs in wait mode.
   However, this is not required if it is not necessary to start the high-speed clock or high-speed on-chip oscillator in the interrupt routine.
2. Do not write 0 to the SVC0 bit with the instruction immediately after 1 is written to the SVC0 bit. Sequential writes in the opposite order are also not allowed.
3. When the SVC0 bit is 1, do not set the CM10 bit in the CM1 register to 1 (stop mode).
4. For entering wait mode, refer to the **Wait Mode** section in the **Notes on Power Control** section.

Figure 10.5 Procedure for Reducing Internal Power Consumption Using SVC0 Bit

10.6.10 Stopping Flash Memory

In low-speed on-chip oscillator mode, the flash memory can be stopped using the FMSTP bit in the FMR0 register to further reduce the power consumption.

When the FMSTP bit is set to 1 (flash memory stops), the flash memory cannot be accessed. The FMSTP bit must be written by a program that has been transferred to the RAM.

When entering stop mode or wait mode with CPU rewrite mode disabled, the power supply for the flash memory is automatically turned off. It is turned on again when the MCU exits stop mode or wait mode. This eliminates the need to set the FMR0 register.

Figure 10.6 shows the Procedure for Reducing Power Consumption Using FMSTP Bit.

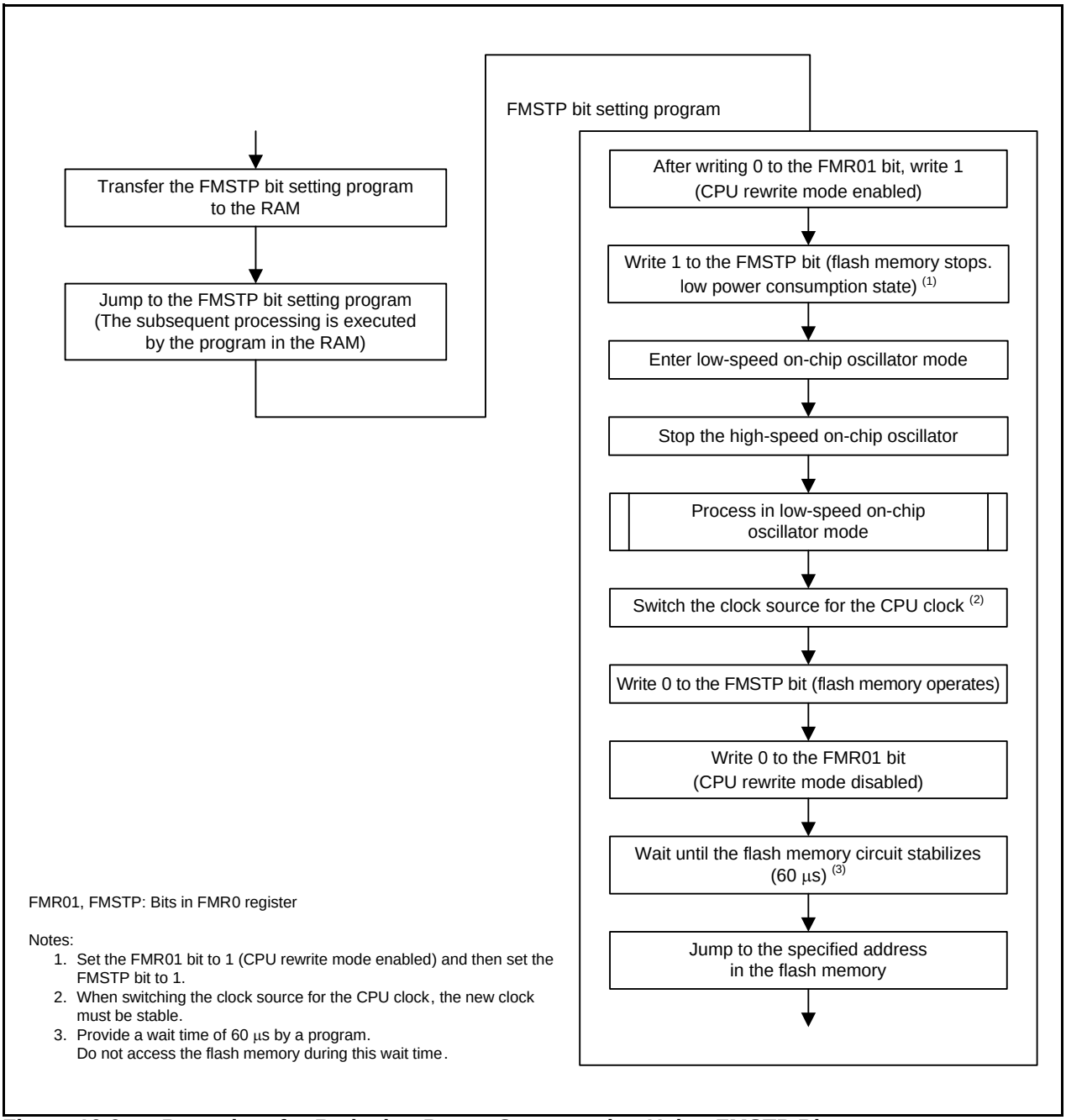
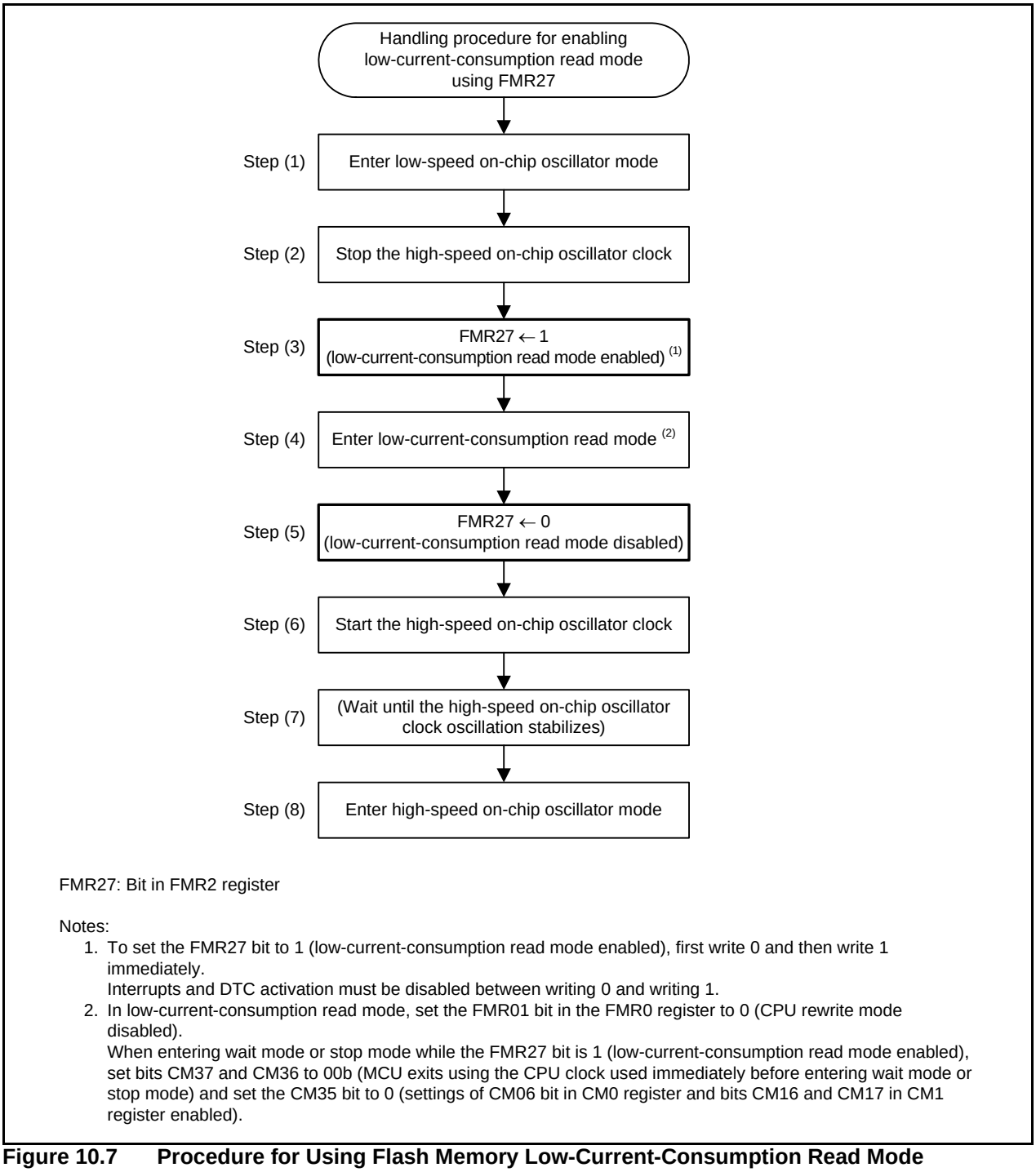


Figure 10.6 Procedure for Reducing Power Consumption Using FMSTP Bit

10.6.11 Low-Current-Consumption Read Mode

In low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).
Low-current-consumption read mode can be used when the CPU clock is set to the following:
• The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
After setting the division ratio of the CPU clock, set the FMR27 bit to 1.
When entering wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled), set bits CM37 and CM36 to 00b (MCU exits using the CPU clock used immediately before entering wait mode or stop mode) and set the CM35 bit to 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled).
Figure 10.7 shows the Procedure for Using Flash Memory Low-Current-Consumption Read Mode.



FMR27: Bit in FMR2 register

Notes:
1. To set the FMR27 bit to 1 (low-current-consumption read mode enabled), first write 0 and then write 1 immediately.
   Interrupts and DTC activation must be disabled between writing 0 and writing 1.
2. In low-current-consumption read mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled).
   When entering wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled), set bits CM37 and CM36 to 00b (MCU exits using the CPU clock used immediately before entering wait mode or stop mode) and set the CM35 bit to 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled).

Figure 10.7 Procedure for Using Flash Memory Low-Current-Consumption Read Mode

10.7 Notes on Power Control

10.7.1 Stop Mode

To enter stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before setting the CM10 bit in the CM1 register to 1 (stop mode). The 4 bytes of instruction data following the instruction that sets the CM10 bit to 1 (stop mode) are prefetched from the instruction queue and then the program stops.
Insert at least four NOP instructions following the JMP.B instruction immediately after the instruction that sets the CM10 bit to 1.

• Program example for entering stop mode

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        BSET    0, PRCR         ; Protection disabled
        FSET    I               ; Interrupt enabled
        BSET    0, CM1          ; Stop mode
        JMP.B   LABEL_001
LABEL_001:
        NOP
        NOP
        NOP
        NOP
```

10.7.2 Wait Mode

To enter wait mode by setting the CM30 bit in the CM3 register to 1, set the FMR01 bit to 0 (CPU rewrite mode disabled) before setting the CM30 bit to 1.
To enter wait mode with the WAIT instruction, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before executing the WAIT instruction. The 4 bytes of instruction data following the instruction that sets the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction are prefetched from the instruction queue and then the program stops. Insert at least four NOP instructions after the instruction that sets the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction.

• Program example for executing the WAIT instruction

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        FSET    I               ; Interrupt enabled
        WAIT                    ; Wait mode
        NOP
        NOP
        NOP
        NOP
```

• Program example for executing the instruction that sets the CM30 bit to 1

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        BSET    0, PRCR         ; Writing to CM3 register enabled
        FCLR    I               ; Interrupt enabled
        BSET    0, CM3          ; Wait mode
        NOP
        NOP
        NOP
        NOP
        BCLR    0, PRCR         ; Writing to CM3 register disabled
        FSET    I               ; Interrupt enabled
```

11. Interrupts

11.1 Overview

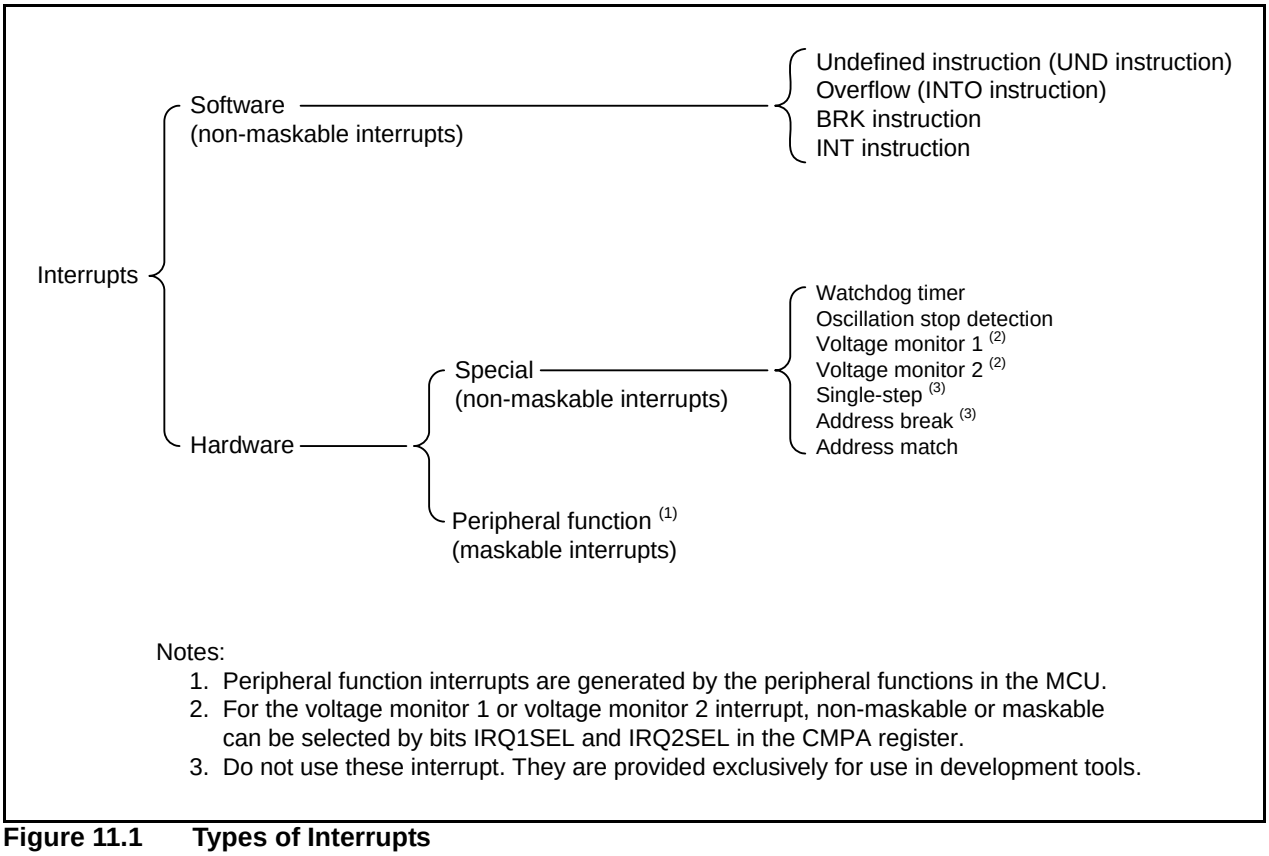
Interrupts are classified as either non-maskable or maskable interrupts. These differ in whether or not the interrupt can be enabled or disabled by the interrupt enable flag (I flag) in the FLG register and in whether or not the interrupt priority level can be changed as listed in Table 11.1.

Table 11.1 Maskable/Non-Maskable Interrupts

	Enabling or Disabling Interrupts by Interrupt Enable Flag (I Flag)	Changing Priority by Setting Interrupt Priority Level
Non-maskable interrupts	Not possible	Not possible
Maskable interrupts	Possible	Possible

11.1.1 Types of Interrupts

Figure 11.1 shows the Types of Interrupts.



Notes:
1. Peripheral function interrupts are generated by the peripheral functions in the MCU.
2. For the voltage monitor 1 or voltage monitor 2 interrupt, non-maskable or maskable can be selected by bits IRQ1SEL and IRQ2SEL in the CMPA register.
3. Do not use these interrupt. They are provided exclusively for use in development tools.

Figure 11.1 Types of Interrupts

11.1.2 Software Interrupts

A software interrupt is generated when an instruction is executed. Software interrupts are non-maskable.

11.1.2.1 Undefined Instruction Interrupt

An unidentified instruction interrupt is generated when the UND instruction is executed.

11.1.2.2 Overflow Interrupt

An overflow interrupt is generated when the O flag is 1 (arithmetic operation overflow) and the INTO instruction is executed. Instructions that change the O flag are as follows:
ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, and SUB.

11.1.2.3 BRK Interrupt

A BRK interrupt is generated when the BRK instruction is executed.

11.1.2.4 INT Instruction Interrupt

An INT instruction interrupt is generated when the INT instruction is executed. Software interrupt numbers the INT instruction can specify are 0 to 63. The number is assigned to each peripheral function interrupt. When the INT instruction is executed specifying the number, the peripheral function interrupt with the same number can be executed.
For software interrupt numbers 0 to 31, the U flag in the FLG register is saved on the stack during instruction execution, and the U flag is set to 0 (ISP selected) before the interrupt sequence is executed. The U flag is restored from the stack when the MCU returns from the interrupt routine. For software interrupt numbers 32 to 63, the U flag does not change state during instruction execution, and the selected SP is used.

11.1.3 Special Interrupts

Special interrupts are non-maskable.

11.1.3.1 Watchdog Timer Interrupt

This interrupt is generated by the watchdog timer.
For details on the watchdog timer, refer to **8. Watchdog Timer**.

11.1.3.2 Oscillation Stop Detection Interrupt

This interrupt is generated by the oscillation stop detection function.
For details on the oscillation stop detection function, refer to **9. Clock Generation Circuit**.

11.1.3.3 Voltage Monitor 1 Interrupt

This interrupt is generated by the voltage detection circuit. A non-maskable or maskable interrupt can be selected by IRQ1SEL bit in the CMPA register.
For details on the voltage detection circuit, refer to **7. Voltage Detection Circuit**.

11.1.3.4 Voltage Monitor 2 Interrupt

This interrupt is generated by the voltage detection circuit. A non-maskable or maskable interrupt can be selected by IRQ2SEL bit in the CMPA register.
For details on the voltage detection circuit, refer to **7. Voltage Detection Circuit**.

11.1.3.5 Single-Step Interrupt, Address Break Interrupt

Do not use these interrupts. They are provided exclusively for use in development tools.

11.1.3.6 Address Match Interrupt

When either the AIEN00 bit in the AIEN0 register or the AIEN10 bit in the AIEN1 register is 1 (address match interrupt enabled), an address match interrupt is generated immediately before executing the instruction that is stored at an address indicated by the corresponding AIADR0j or AIADR1j register (j = L or H).
For details on the address match interrupt, refer to **11.7 Address Match Interrupt**.

11.1.3.7 Peripheral Function Interrupts

A peripheral function interrupt is generated by a peripheral function in the MCU. Peripheral function interrupts are maskable. For the interrupt sources for the corresponding peripheral function interrupt, refer to the interrupts and the vector table addresses listed in **Tables 11.4** and **11.5 Relocatable Vector Table**. For details on the peripheral functions, refer to the descriptions of individual peripheral functions.

11.2 Registers

Table 11.2 lists the Register Configuration for Interrupts.

Table 11.2 Register Configuration for Interrupts

Register Name	Symbol	After Reset	Address	Access Size
Interrupt Control Register	FMRDYIC	00h	00041h	8
Interrupt Control Register	TRJIC_1	00h	00042h	8
Interrupt Control Register	INT4IC	00h	00046h	8
Interrupt Control Register	TRCIC_0	00h	00047h	8
Interrupt Control Register	TRD0IC_0	00h	00048h	8
Interrupt Control Register	TRD1IC_0	00h	00049h	8
Interrupt Control Register	TRE2IC	00h	0004Ah	8
Interrupt Control Register	U2TIC	00h	0004Bh	8
Interrupt Control Register	U2RIC	00h	0004Ch	8
Interrupt Control Register	KUPIC	00h	0004Dh	8
Interrupt Control Register	ADIC	00h	0004Eh	8
Interrupt Control Register	SSUIC_0/IICIC_0	00h	0004Fh	8
Interrupt Control Register	U0TIC_0	00h	00051h	8
Interrupt Control Register	U0RIC_0	00h	00052h	8
Interrupt Control Register	U0TIC_1	00h	00053h	8
Interrupt Control Register	U0RIC_1	00h	00054h	8
Interrupt Control Register	INT2IC	00h	00055h	8
Interrupt Control Register	TRJIC_0	00h	00056h	8
Interrupt Control Register	TRB2IC_0	00h	00058h	8
Interrupt Control Register	INT1IC	00h	00059h	8
Interrupt Control Register	INT3IC	00h	0005Ah	8
Interrupt Control Register	INT0IC	00h	0005Dh	8
Interrupt Control Register	U2BCNIC	00h	0005Eh	8
Interrupt Control Register	CANRXIC_0	00h	0006Ch	8
Interrupt Control Register	CANTXIC_0	00h	0006Dh	8
Interrupt Control Register	CANERIC_0	00h	0006Eh	8
Interrupt Control Register	VCMP1IC	00h	00072h	8
Interrupt Control Register	VCMP2IC	00h	00073h	8
Interrupt Control Register	SSUIC_1/IICIC_1	00h	00079h	8
External Input Enable Register 0	INTEN	00h	00230h	8
External Input Enable Register 1	INTEN1	00h	00231h	8
INT Input Filter Select Register 0	INTF	00h	00232h	8
INT Input Filter Select Register 1	INTF1	00h	00233h	8
INT Input Polarity Switch Register	INTPOL	00h	00234h	8
Key Input Interrupt Enable Register	KIEN	00h	00236h	8
Address Match Interrupt Address 0L Register	AIADR0L	XXXXh	00260h	16
Address Match Interrupt Address 0H Register	AIADR0H	0000XXXXb	00262h	8
Address Match Interrupt Enable 0 Register	AIEN0	00h	00263h	8
Address Match Interrupt Address 1L Register	AIADR1L	XXXXh	00264h	16
Address Match Interrupt Address 1H Register	AIADR1H	0000XXXXb	00266h	8
Address Match Interrupt Enable 1 Register	AIEN1	00h	00267h	8
INT Interrupt Input Pin Select Register 0	INTSR0	00h	002B6h	8

11.2.1 Interrupt Control Register (FMRDYIC, TRJIC_1, INT4IC, TRCIC_0,TRD0IC_0, TRD1IC_0, TRE2IC, U2TIC, U2RIC, KUPIC, ADIC, SSUIC_0/IICIC_0, U0TIC_0, U0RIC_0, U0TIC_1, U0RIC_1, INT2IC, TRJIC_0, TRB2IC_0, INT1IC, INT3IC, INT0IC, U2BCNIC, CANRXIC_0, CANTXIC_0, CANERIC_0, VCMP1IC, VCMP2IC, SSUIC_1/IICIC_1)

Address 00041h (FMRDYIC), 00042h (TRJIC_1), 00046h (INT4IC), 00047h (TRCIC_0), 00048h (TRD0IC_0), 00049h (TRD1IC_0), 0004Ah (TRE2IC), 0004Bh (U2TIC), 0004Ch (U2RIC), 0004Dh (KUPIC), 0004Eh (ADIC), 0004Fh (SSUIC_0/IICIC_0), 00051h (U0TIC_0), 00052h (U0RIC_0), 00053h (U0TIC_1), 00054h (U0RIC_1), 00055h (INT2IC), 00056h (TRJIC_0), 00058h (TRB2IC_0), 00059h (INT1IC), 0005Ah (INT3IC), 0005Dh (INT0IC), 0005Eh (U2BCNIC), 0006Ch (CANRXIC_0), 0006Dh (CANTXIC_0), 0006Eh (CANERIC_0), 00072h (VCMP1IC), 00073h (VCMP2IC), 00079h (SSUIC_1/IICIC_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IR	ILVL2	ILVL1	ILVL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bits	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R/W (1)
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. Only 0 can be written to the IR bit. (Do not write 1 to this bit.)

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **11.9.5 Rewriting Interrupt Control Register**.

11.2.2 External Input Enable Register 0 (INTEN)

Address 00230h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3PL	INT3EN	INT2PL	INT2EN	INT1PL	INT1EN	INT0PL	INT0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0EN	$\overline{\text{INT0}}$ input enable bit	0: Disabled 1: Enabled	R/W
b1	INT0PL	$\overline{\text{INT0}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b2	INT1EN	$\overline{\text{INT1}}$ input enable bit	0: Disabled 1: Enabled	R/W
b3	INT1PL	$\overline{\text{INT1}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b4	INT2EN	$\overline{\text{INT2}}$ input enable bit	0: Disabled 1: Enabled	R/W
b5	INT2PL	$\overline{\text{INT2}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b6	INT3EN	$\overline{\text{INT3}}$ input enable bit	0: Disabled 1: Enabled	R/W
b7	INT3PL	$\overline{\text{INT3}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W

Notes:
1. To set the INTiPL bit (i = 0 to 3) to 1 (both edges), set the INTiPOL bit in the INTPOL register to 0 (falling edge selected).
2. The IR bit in the INTiIC register may be set to 1 (interrupt requested) if the INTEN register is rewritten. Refer to **11.9.4 Changing Interrupt Sources**.

11.2.3 External Input Enable Register 1 (INTEN1)

Address 00231h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	INT4PL	INT4EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT4EN	$\overline{\text{INT4}}$ input enable bit	0: Disabled 1: Enabled	R/W
b1	INT4PL	$\overline{\text{INT4}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b2	—	Reserved	Set to 0.	R/W
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. To set the INT4PL bit to 1 (both edges), set the INT4POL bit in the INTPOL register to 0 (falling edge selected).
2. The IR bit in the INT4IC register may be set to 1 (interrupt requested) if the INTEN1 register is rewritten. Refer to **11.9.4 Changing Interrupt Sources**.

11.2.4 INT Input Filter Select Register 0 (INTF)

Address 00232h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3F1	INT3F0	INT2F1	INT2F0	INT1F1	INT1F0	INT0F1	INT0F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0F0	$\overline{\text{INT0}}$ input filter select bits	b1 b0 0 0: No filter 0 1: Filter enabled, sampling at f1 1 0: Filter enabled, sampling at f8 1 1: Filter enabled, sampling at f32	R/W
b1	INT0F1			R/W
b2	INT1F0	$\overline{\text{INT1}}$ input filter select bits	b3 b2 0 0: No filter 0 1: Filter enabled, sampling at f1 1 0: Filter enabled, sampling at f8 1 1: Filter enabled, sampling at f32	R/W
b3	INT1F1			R/W
b4	INT2F0	$\overline{\text{INT2}}$ input filter select bits	b5 b4 0 0: No filter 0 1: Filter enabled, sampling at f1 1 0: Filter enabled, sampling at f8 1 1: Filter enabled, sampling at f32	R/W
b5	INT2F1			R/W
b6	INT3F0	$\overline{\text{INT3}}$ input filter select bits	b7 b6 0 0: No filter 0 1: Filter enabled, sampling at f1 1 0: Filter enabled, sampling at f8 1 1: Filter enabled, sampling at f32	R/W
b7	INT3F1			R/W

11.2.5 INT Input Filter Select Register 1 (INTF1)

Address 00233h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	INT4F1	INT4F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT4F0	$\overline{\text{INT4}}$ input filter select bits	b1 b0 0 0: No filter 0 1: Filter enabled, sampling at f1 1 0: Filter enabled, sampling at f8 1 1: Filter enabled, sampling at f32	R/W
b1	INT4F1			R/W
b2	—	Reserved	Set to 0.	R/W
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

11.2.6 INT Input Polarity Switch Register (INTPOL)

Address 00234h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	INT4POL	INT3POL	INT2POL	INT1POL	INT0POL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0POL	$\overline{\text{INT0}}$ polarity switch bit	0: Falling edge 1: Rising edge (2)	R/W
b1	INT1POL	$\overline{\text{INT1}}$ polarity switch bit		R/W
b2	INT2POL	$\overline{\text{INT2}}$ polarity switch bit		R/W
b3	INT3POL	$\overline{\text{INT3}}$ polarity switch bit		R/W
b4	INT4POL	$\overline{\text{INT4}}$ polarity switch bit		R/W
b5	—	Reserved	Set to 0.	R/W
b6	—			
b7	—			

Notes:
1. Changing the INTiPOL bit (i = 0 to 4) may set the IRKI bit in the INTiIC register to 1 (interrupt requested). Refer to **11.9.4 Changing Interrupt Sources**.
2. If the INTiPL bit in registers INTEN and INTEN1 is set to 1 (both edges), set the INTiPOL bit to 0 (falling edge selected).

11.2.7 Key Input Interrupt Enable Register (KIEN)

Address 00236h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	KI3PL	KI3EN	KI2PL	KI2EN	KI1PL	KI1EN	KI0PL	KI0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	KI0EN	$\overline{\text{KI0}}$ input enable bit	0: Disabled 1: Enabled	R/W
b1	KI0PL	$\overline{\text{KI0}}$ input polarity select bit	0: Falling edge 1: Rising edge	R/W
b2	KI1EN	$\overline{\text{KI1}}$ input enable bit	0: Disabled 1: Enabled	R/W
b3	KI1PL	$\overline{\text{KI1}}$ input polarity select bit	0: Falling edge 1: Rising edge	R/W
b4	KI2EN	$\overline{\text{KI2}}$ input enable bit	0: Disabled 1: Enabled	R/W
b5	KI2PL	$\overline{\text{KI2}}$ input polarity select bit	0: Falling edge 1: Rising edge	R/W
b6	KI3EN	$\overline{\text{KI3}}$ input enable bit	0: Disabled 1: Enabled	R/W
b7	KI3PL	$\overline{\text{KI3}}$ input polarity select bit	0: Falling edge 1: Rising edge	R/W

The IR bit in the KUPIC register may be set to 1 (interrupt requested) if the KIEN register is rewritten. Refer to **11.9.4 Changing Interrupt Sources**.

11.2.8 Address Match Interrupt Address ij Register (AIADRij) (i = 0 or 1, j = L or H)

Address 00260h (AIADR0L), 00262h (AIADR0H), 00264h (AIADR1L), 00266h (AIADR1H)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b23	b22	b21	b20	b19	b18	b17	b16
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	X	X	X	X

Bit	Symbol	Function	Settable Value	R/W
b19 to b0	—	Target PC value: 20 bits	00000h to FFFFFh	R/W
b20	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b21	—			
b22	—			
b23	—			

11.2.9 Address Match Interrupt Enable i Register (AIENi) (i = 0 or 1)

Address 00263h (AIEN0), 00267h (AIEN1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	AIENi0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	AIENi0	Address match interrupt enable bit	0: Disabled 1: Enabled	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

11.2.10 INT Interrupt Input Pin Select Register 0 (INTSR0)

Address 002B6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3SEL1	INT3SEL0	INT2SEL1	INT2SEL0	INT1SEL2	INT1SEL1	INT1SEL0	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	INT1SEL0	$\overline{\text{INT1}}$ pin select bits	b3 b2 b1 0 0 0: P1_7 assigned 0 0 1: P1_5 assigned 0 1 0: P2_0 assigned Other than the above: Do not set.	R/W
b2	INT1SEL1			R/W
b3	INT1SEL2			R/W
b4	INT2SEL0	$\overline{\text{INT2}}$ pin select bits	b5 b4 0 0: P6_6 assigned 0 1: Do not set. 1 0: P6_4 assigned 1 1: P0_2 assigned	R/W
b5	INT2SEL1			R/W
b6	INT3SEL0	$\overline{\text{INT3}}$ pin select bits	b7 b6 0 0: P3_3 assigned 0 1: P3_7 assigned 1 0: P6_7 assigned 1 1: Do not set.	R/W
b7	INT3SEL1			R/W

The INTSR0 register is used to select which pin is assigned to $\overline{\text{INTi}}$ (i = 1 to 3) input. To use $\overline{\text{INTi}}$, set this register.
Set the INTSR0 register before setting the registers associated with $\overline{\text{INTi}}$. Also, do not change the set value of this register during $\overline{\text{INTi}}$ operation.
$\overline{\text{INT0}}$ and $\overline{\text{INT4}}$ are assigned to P4_5 and P6_5, respectively, regardless of the INTSR0 register.

11.3 Interrupts and Interrupt Vectors

There are 4 bytes in each vector. Store the start address of an interrupt routine in each interrupt vector. When an interrupt request is acknowledged, the CPU branches to the address set in the corresponding interrupt vector. Figure 11.2 shows an Interrupt Vector.

Figure 11.2 Interrupt Vector

11.3.1 Fixed Vector Table

The fixed vector table is allocated at addresses 0FFDCh to 0FFFFh.
Table 11.3 lists the Fixed Vector Table. The vector addresses (H) of the fixed vectors are used by the ID code check function. Refer to **27.4 Functions to Prevent Flash Memory from being Rewritten** for details.

Table 11.3 Fixed Vector Table

Interrupt Source	Vector Addresses Address (L) to (H)	Remarks	Reference
Undefined instruction	0FFDCh to 0FFDFh	Interrupt with UND instruction	R8C/5x Series User's manual: Software
Overflow	0FFE0h to 0FFE3h	Interrupt with INTO instruction	
BRK instruction	0FFE4h to 0FFE7h	If the content of address 0FFE6h is FFh, program execution starts from the address shown by the vector in the relocatable vector table.	
Address match	0FFE8h to 0FFEBh		11.7 Address Match Interrupt
Single step (1)	0FFECh to 0FFEFh		
Watchdog timer, Oscillation stop detection, Voltage monitor 1 (2), Voltage monitor 2 (2)	0FFF0h to 0FFF3h		8. Watchdog Timer, 9. Clock Generation Circuit, 7. Voltage Detection Circuit
Address break (1)	0FFF4h to 0FFF7h		
(Reserved)	0FFF8h to 0FFFBh		
Reset	0FFFCh to 0FFFFh		6. Resets

Notes:
1. Do not use this interrupt. It is provided exclusively for use in development tools.
2. For the voltage monitor 1 or voltage monitor 2 interrupt, non-maskable or maskable can be selected by the IRQ1SEL or IRQ2SEL bit in the CMPA register.

11.3.2 Relocatable Vector Table

The relocatable vector table occupies 256 bytes beginning from the start address set in the INTB register. Tables 11.4 and 11.5 list the Relocatable Vector Table.

Table 11.4 Relocatable Vector Table (1)

Interrupt Source	Vector Addresses (1) Address (L) to Address (H)	Software Interrupt Number	Interrupt Control Register	Reference
BRK instruction (2)	+0 to +3 (00000h to 00003h)	0	—	R8C/5x Series User's manual: Software
Flash memory	+4 to +7 (00004h to 00007h)	1	FMRDYIC	27. Flash Memory
Timer RJ_1	+8 to +11 (00008h to 0000Bh)	2	TRJIC_1	15. Timer RJ
— (Reserved)	+12 to +15 (0000Ch to 0000Fh)	3	—	—
— (Reserved)	+16 to +19 (00010h to 00013h)	4	—	
— (Reserved)	+20 to +23 (00014h to 00017h)	5	—	
$\overline{\text{INT4}}$	+24 to +27 (00018h to 0001Bh)	6	INT4IC	11.5 $\overline{\text{INT}}$ Interrupt
Timer RC_0	+28 to +31 (0001Ch to 0001Fh)	7	TRCIC_0	17. Timer RC
Timer RD0_0	+32 to +35 (00020h to 00023h)	8	TRD0IC_0	18. Timer RD
Timer RD1_0	+36 to +39 (00024h to 00027h)	9	TRD1IC_0	
Timer RE2	+40 to +43 (00028h to 0002Bh)	10	TRE2IC	19. Timer RE2
UART2 transmit/NACK2	+44 to +47 (0002Ch to 0002Fh)	11	U2TIC	21. Serial Interface (UART2)
UART2 receive/ACK2	+48 to +51 (00030h to 00033h)	12	U2RIC	
Key input	+52 to +55 (00034h to 00037h)	13	KUPIC	11.6 Key Input Interrupt
A/D conversion	+56 to +59 (00038h to 0003Bh)	14	ADIC	25. A/D Converter
Synchronous serial communication unit/ I^2C bus interface	+60 to +63 (0003Ch to 0003Fh)	15	SSUIC_0/ IICIC_0	22. Clock Synchronous Serial Interface
— (Reserved)	+64 to +67 (00040h to 00043h)	16	—	—
UART0_0 transmit	+68 to +71 (00044h to 00047h)	17	U0TIC_0	20. Serial Interface (UART0)
UART0_0 receive	+72 to +75 (00048h to 0004Bh)	18	U0RIC_0	
UART0_1 transmit	+76 to +79 (0004Ch to 0004Fh)	19	U0TIC_1	
UART0_1 receive	+80 to +83 (00050h to 00053h)	20	U0RIC_1	
$\overline{\text{INT2}}$	+84 to +87 (00054h to 00057h)	21	INT2IC	11.5 $\overline{\text{INT}}$ Interrupt
Timer RJ_0	+88 to +91 (00058h to 0005Bh)	22	TRJIC_0	15. Timer RJ
— (Reserved)	+92 to +95 (0005Ch to 0005Fh)	23	—	—
Timer RB2_0	+96 to +99 (00060h to 00063h)	24	TRB2IC_0	16. Timer RB2
$\overline{\text{INT1}}$ (multiplexed with comparator B)	+100 to +103 (00064h to 00067h)	25	INT1IC	11.5 $\overline{\text{INT}}$ Interrupt
$\overline{\text{INT3}}$ (multiplexed with comparator B)	+104 to +107 (00068h to 0006Bh)	26	INT3IC	
— (Reserved)	+108 to +111 (0006Ch to 0006Fh)	27	—	—
— (Reserved)	+112 to +115 (00070h to 00073h)	28	—	
$\overline{\text{INT0}}$	+116 to +119 (00074h to 00077h)	29	INT0IC	11.5 $\overline{\text{INT}}$ Interrupt
UART2 bus collision detection	+120 to +123 (00078h to 0007Bh)	30	U2BCNIC	21. Serial Interface (UART2)
— (Reserved)	+124 to +127 (0007Ch to 0007Fh)	31	—	—

Notes:
1. These addresses are relative to that indicated by the INTB register.
2. These interrupts are not disabled by the I flag.

Table 11.5 Relocatable Vector Table (2)

Interrupt Source	Vector Addresses (1) Address (L) to Address (H)	Software Interrupt Number	Interrupt Control Register	Reference
Software (2)	+128 to +131 (00080h to 00083h) to +164 to +167 (000A4h to 000A7h)	32 to 41	—	R8C/5x Series User's manual: Software
— (Reserved)	+168 to +171 (000A8h to 000ABh)	42	—	—
— (Reserved)	+172 to +175 (000ACh to 000AFh)	43	—	—
CAN_0 receive	+176 to +179 (000B0h to 000B3h)	44	CANRXIC_0	24. CAN Module
CAN_0 transmit	+180 to +183 (000B4h to 000B7h)	45	CANTXIC_0	
CAN_0 error	+184 to +187 (000B8h to 000BBh)	46	CANERIC_0	
— (Reserved)	+188 to +191 (000BCh to 000BFh)	47	—	—
— (Reserved)	+192 to +195 (000C0h to 000C3h)	48	—	
— (Reserved)	+196 to +199 (000C4h to 000C7h)	49	—	
Voltage monitor 1 (3)	+200 to +203 (000C8h to 000CBh)	50	VCMP1IC	7. Voltage Detection Circuit
Voltage monitor 2 (3)	+204 to +207 (000CCh to 000CFh)	51	VCMP2IC	
— (Reserved)	+208 to +211 (000D0h to 000D3h) to +224 to +227 (000E0h to 000E3h)	52 to 56	—	—
Synchronous serial communication unit/I^2C bus interface	+228 to +231 (000E4h to 000E7h)	57	SSUIC_1/ IICIC_1	22. Clock Synchronous Serial Interface
— (Reserved)	+232 to +235 (000E8h to 000EBh)	58	—	—
— (Reserved)	+236 to +239 (000ECh to 000EFh)	59	—	—
— (Reserved)	+240 to +243 (000F0h to 000F3h)	60	—	
— (Reserved)	+244 to +247 (000F4h to 000F7h)	61	—	
— (Reserved)	+248 to +251 (000F8h to 000FBh)	62	—	

Notes:
1. These addresses are relative to that indicated by the INTB register.
2. These interrupts are not disabled by the I flag.
3. For the voltage monitor 1 or voltage monitor 2 interrupt, non-maskable or maskable can be selected by the IRQ1SEL or IRQ2SEL bit in the CMPA register.

11.4 Interrupt Control

The following describes enabling and disabling maskable interrupts and setting the priority for acknowledgement. This description does not apply to non-maskable interrupts.
Use the I flag in the FLG register, IPL, and bits ILVL2 to ILVL0 in the corresponding interrupt control register to enable or disable a maskable interrupt. Whether an interrupt is requested or not is indicated by the IR bit in the corresponding interrupt control register.

11.4.1 I Flag

The I flag enables or disables maskable interrupts. Setting the I flag to 1 (enabled) enables maskable interrupts. Setting the I flag to 0 (disabled) disables all maskable interrupts.

11.4.2 IR Bit

The IR bit is set to 1 (interrupt requested) when an interrupt request is generated. After the interrupt request is acknowledged and the CPU branches to the corresponding interrupt vector, the IR bit is set to 0 (no interrupt requested).
The IR bit can be set to 0 by a program. Do not write 1 to this bit.
However, the IR bit operations of the timer RC interrupt, the timer RD interrupt, the timer RE2 interrupt, the synchronous serial communication unit/I^2C bus interface interrupt, the CAN transmit interrupt, the CAN receive interrupt, the CAN error interrupt, and the flash memory interrupt are different. Refer to **11.8 Timer RC Interrupt, Timer RD Interrupt, Timer RE2 Interrupt, Synchronous Serial Communication Unit/I^2C bus Interface, CAN Transmit Interrupt, CAN Receive Interrupt, CAN Error Interrupt, and Flash Memory Interrupt (Interrupts with Multiple Interrupt Request Sources)**.

11.4.3 Bits ILVL2 to ILVL0, IPL

Interrupt priority levels can be set using bits ILVL2 to ILVL0.
Table 11.6 lists the Interrupt Priority Level Settings. Table 11.7 lists the Interrupt Priority Levels Enabled by IPL.
The following are the conditions when an interrupt is acknowledged:
- I flag = 1
- IR bit = 1
- Interrupt priority level > IPL

The I flag, IR bit, bits ILVL2 to ILVL0, and IPL are independent of each other. They do not affect one another.

Table 11.6 Interrupt Priority Level Settings

Bits ILVL2 to ILVL0	Interrupt Priority Level	Priority
000b	Level 0 (interrupt disabled)	—
001b	Level 1	Low
010b	Level 2	
011b	Level 3	
100b	Level 4	
101b	Level 5	
110b	Level 6	
111b	Level 7	High

Table 11.7 Interrupt Priority Levels Enabled by IPL

IPL	Enabled Interrupt Priority Level
000b	Interrupt level 1 and above
001b	Interrupt level 2 and above
010b	Interrupt level 3 and above
011b	Interrupt level 4 and above
100b	Interrupt level 5 and above
101b	Interrupt level 6 and above
110b	Interrupt level 7 and above
111b	All maskable interrupts are disabled

11.4.4 Interrupt Sequence

The following describes the interrupt sequence performed from when an interrupt request is acknowledged until the interrupt routine is executed.
When an interrupt request is generated while an instruction is being executed, the CPU determines its interrupt priority level after the instruction has completed. The CPU starts the interrupt sequence from the following cycle. However, for the SMOVB, SMOVF, SSTR, and RMPA instructions, if an interrupt request is generated while the instruction is being executed, the MCU suspends the instruction to start the interrupt sequence.
The interrupt sequence is performed as described below.
Figure 11.3 shows the Time Required for Executing Interrupt Sequence.

(1) The CPU obtains interrupt information (interrupt number and interrupt request level) by reading address 00000h. Then, the corresponding bit for the interrupt is set to 0 (no interrupt requested).(1)
(2) The FLG register is saved to a temporary register (2) in the CPU immediately before the interrupt sequence is entered.
(3) The I, D, and U flags in the FLG register are set as follows:
The I flag is 0 (interrupt disabled)
The D flag is 0 (single-step interrupt disabled)
The U flag is set to 0 (ISP selected).
However, the U flag does not change if an INT instruction for software interrupts numbered 32 to 63 is executed.
(4) The CPU internal temporary register (2) is saved on the stack.
(5) The PC is saved on the stack.
(6) The interrupt priority level of the acknowledged interrupt is set in the IPL.
(7) The start address of the interrupt routine set in the interrupt vector is stored in the PC.

After the interrupt sequence is completed, instructions are executed from the start address of the interrupt routine.

Notes:
1. Refer to **11.8 Timer RC Interrupt, Timer RD Interrupt, Timer RE2 Interrupt, Synchronous Serial Communication Unit/I²C bus Interface, CAN Transmit Interrupt, CAN Receive Interrupt, CAN Error Interrupt, and Flash Memory Interrupt (Interrupts with Multiple Interrupt Request Sources)** for the IR bit operations of the timer RC interrupt, timer RD interrupt, timer RE2 interrupt, synchronous serial communication unit/I²C bus interface interrupt, CAN transmit interrupt, CAN receive interrupt, CAN error interrupt, and flash memory interrupt.
2. Temporary registers cannot be used by the user.

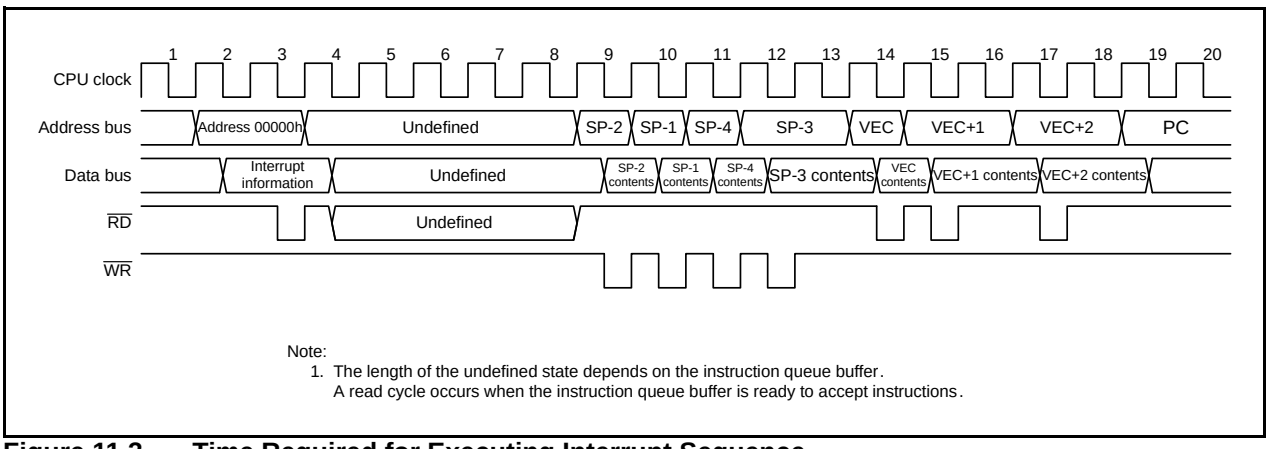
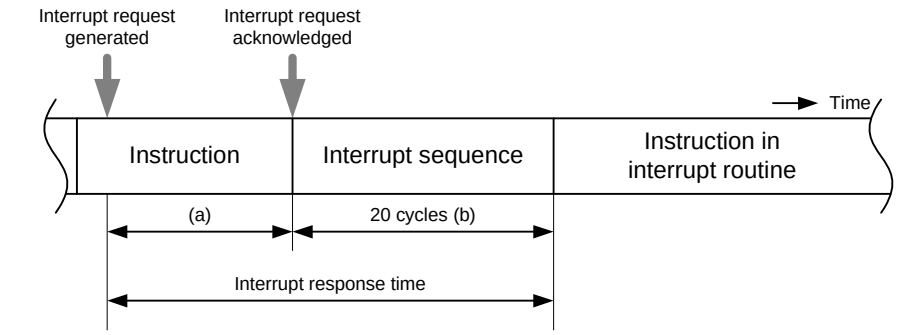


Figure 11.3 Time Required for Executing Interrupt Sequence

11.4.5 Interrupt Response Time

Figure 11.4 shows the Interrupt Response Time. The interrupt response time is the period from when an interrupt request is generated until the first instruction in the interrupt routine is executed. This time consists of two periods: the first period ranges from when an interrupt request is generated until the currently executing instruction is completed ((a) in Figure 11.4) and the second from when an interrupt request is acknowledged until the interrupt sequence is executed (20 cycles (b)).



(a) The period from when an interrupt request is generated until the currently executing instruction is completed. The length of this time varies with the instruction being executed. The DIVX instruction requires the longest time, 30 cycles (no wait states, and the divisor is a register).
(b) 21 cycles for address match and single-step interrupts.

Figure 11.4 Interrupt Response Time

11.4.6 IPL Change when Interrupt Request is Acknowledged

When a maskable interrupt request is acknowledged, the interrupt priority level of the acknowledged interrupt is set in the IPL.
For a software interrupt or special interrupt request, the level listed in Table 11.8 is set in the IPL.
Table 11.8 lists the IPL Value when Software or Special Interrupt is Acknowledged.

Table 11.8 IPL Value when Software or Special Interrupt is Acknowledged

Interrupt Source without Interrupt Priority Level	Value Set in IPL
Watchdog timer, oscillation stop detection, voltage monitor 1, voltage monitor 2, address break	7
Software, address match, single-step	Not changed

11.4.7 Saving Registers

In the interrupt sequence, the FLG register and PC are saved on the stack.
After a total of 16 bits: higher 4 bits in the PC, higher 4 (IPL) and lower 8 bits in the FLG register, are saved on the stack, the lower 16 bits in the PC are saved.
Figure 11.5 shows the Stack State Before and After Interrupt Request is Acknowledged.
Any other necessary registers should be saved at the beginning of the interrupt routine. The PUSHM instruction can save all registers (1) other than the SP with a single instruction.

Note:
1. Selected from registers R0, R1, R2, R3, A0, A1, SB, and FB.

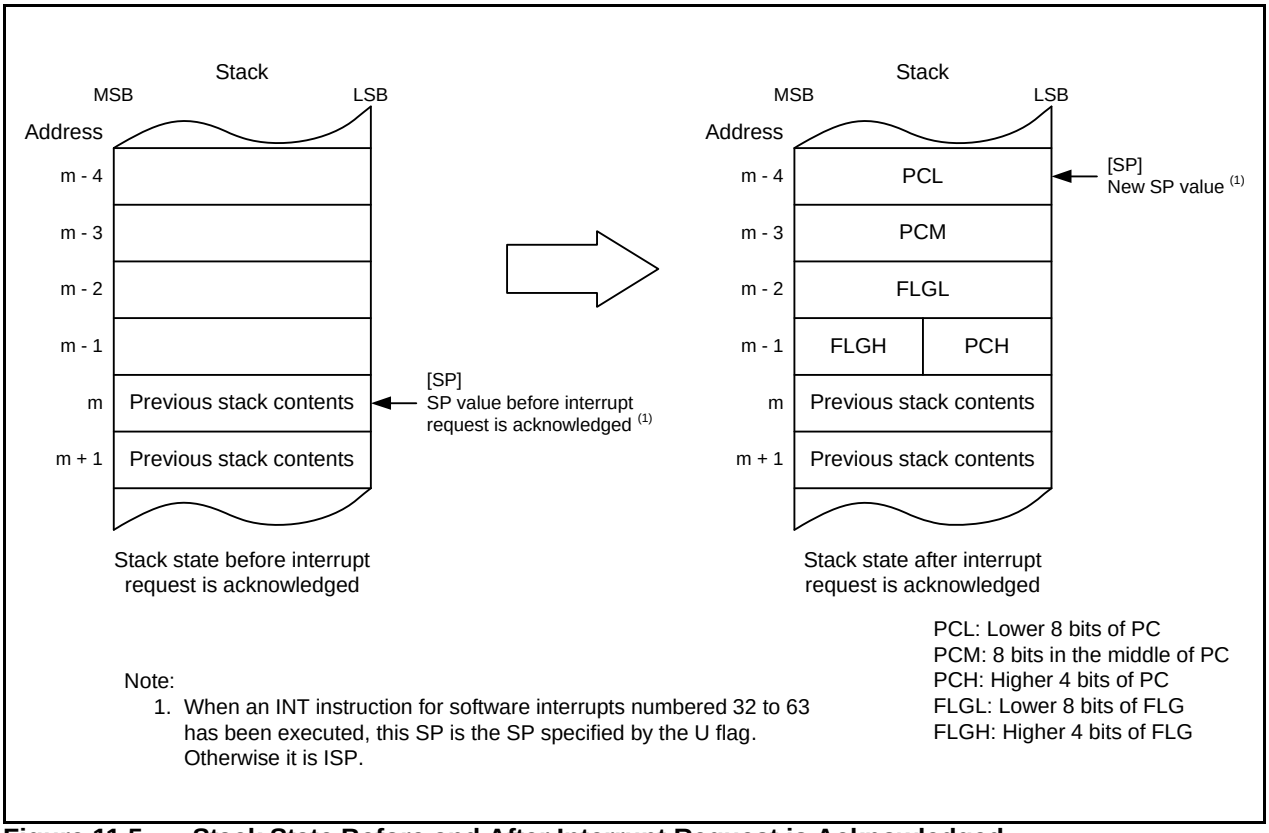
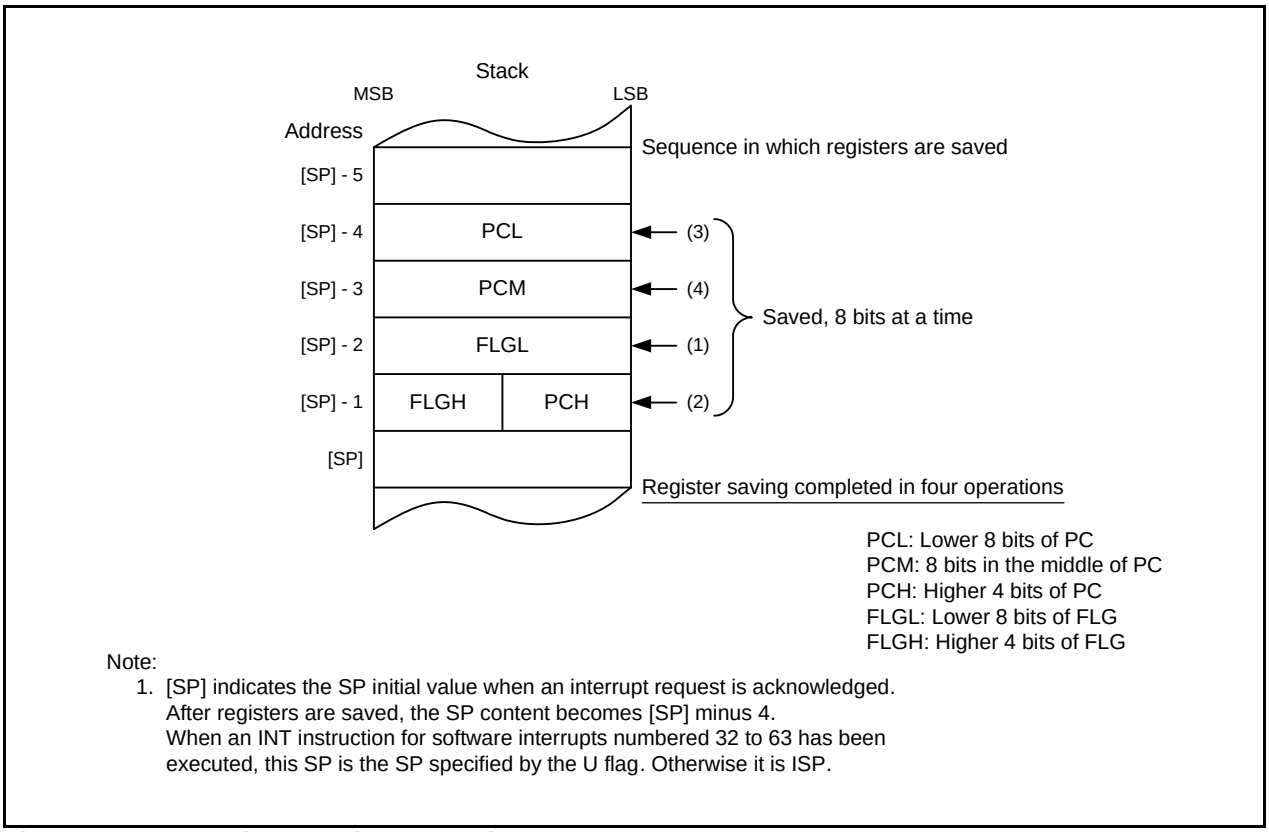


Figure 11.5 Stack State Before and After Interrupt Request is Acknowledged

The register saving operation in the interrupt sequence uses four operations, each one of which saves 8 bits. Figure 11.6 shows the Register Saving Operation.



Note:
1. [SP] indicates the SP initial value when an interrupt request is acknowledged. After registers are saved, the SP content becomes [SP] minus 4. When an INT instruction for software interrupts numbered 32 to 63 has been executed, this SP is the SP specified by the U flag. Otherwise it is ISP.

Figure 11.6 Register Saving Operation

11.4.8 Returning from Interrupt Routine

When the REIT instruction is executed at the end of an interrupt routine, the FLG register and PC, which have been saved on the stack, are restored. Then, the processing before acknowledgement of the interrupt request starts again.

The registers saved by a program in the interrupt routine should be restored using the POPM or similar instruction before executing the REIT instruction.

11.4.9 Interrupt Priority

If two or more interrupt requests are generated while a single instruction is being executed, the interrupt with the higher priority is acknowledged.

Any maskable interrupt (peripheral function) priority level can be selected by bits ILVL0 to ILVL2. However, if two or more maskable interrupts have the same priority level, the interrupt with higher priority given by hardware is acknowledged.

The priority of special interrupts such as the watchdog timer interrupt is set by hardware.

Figure 11.7 shows the Hardware Interrupt Priority.

Software interrupts are not affected by the interrupt priority. If a software interrupt instruction is executed, the MCU will execute the corresponding interrupt routine.

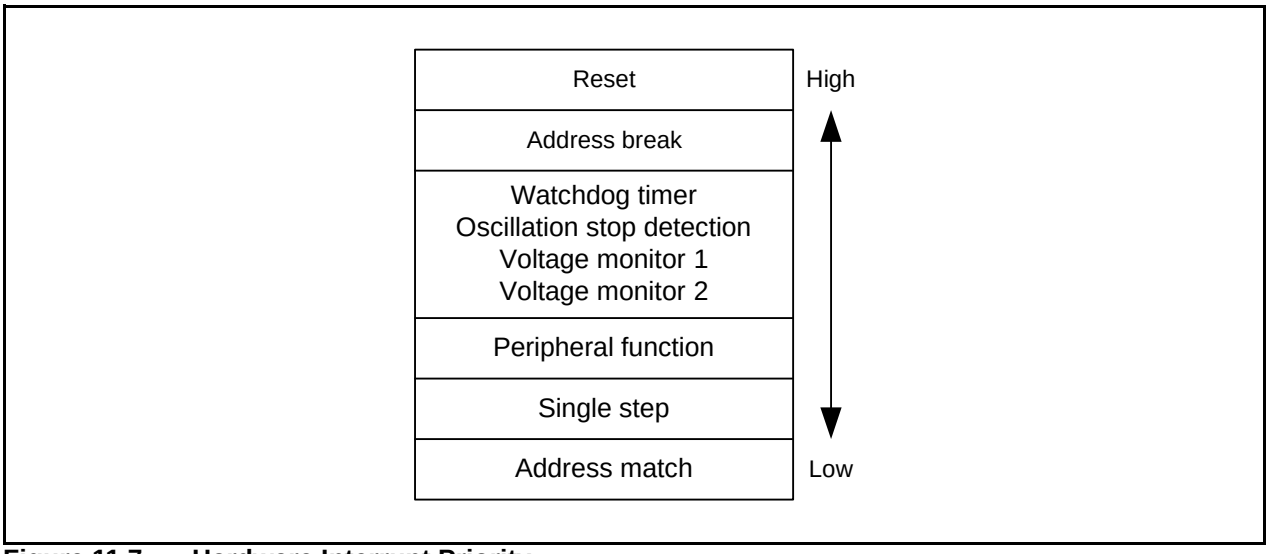


Figure 11.7 Hardware Interrupt Priority

11.4.10 Interrupt Priority Level Selection Circuit

The interrupt priority level selection circuit is used to select the highest priority interrupt.
Figure 11.8 shows the Interrupt Priority Level Selection Circuit.

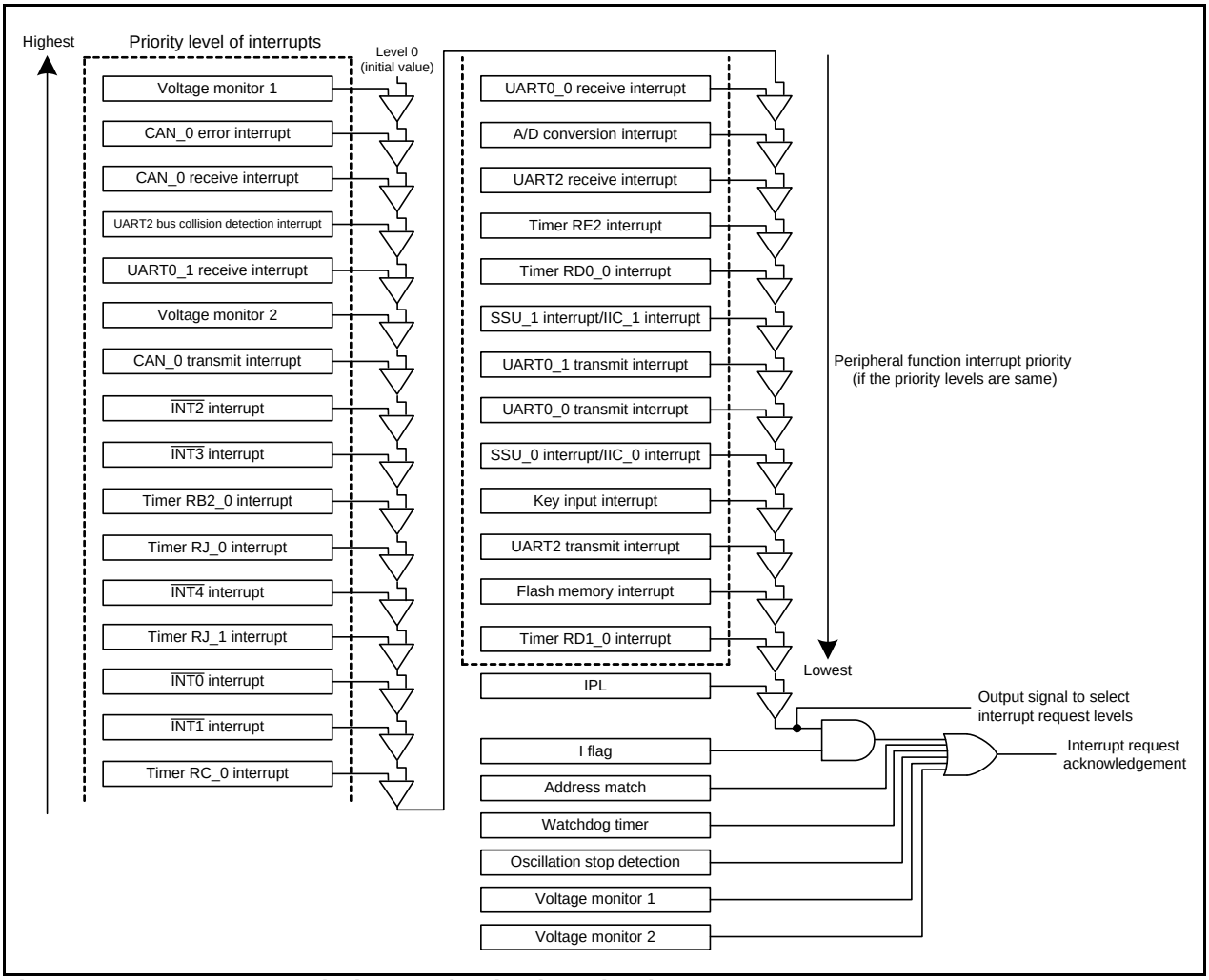


Figure 11.8 Interrupt Priority Level Selection Circuit

11.5 $\overline{\text{INT}}$ Interrupt

11.5.1 $\overline{\text{INTi}}$ Interrupt (i = 0 to 4)

The $\overline{\text{INTi}}$ interrupt is generated by an $\overline{\text{INTi}}$ input. To use the $\overline{\text{INTi}}$ interrupt, set the INTiEN bit in the INTEN or INTEN1 register to 1 (enabled). The edge polarity can be selected by the INTiPL bit in the INTEN or INTEN1 register and the INTiPOL bit in the INTPOL register. The input pins used as the $\overline{\text{INT1}}$ to $\overline{\text{INT4}}$ input can be selected.

Inputs can be passed through a digital filter with three different sampling clocks. The $\overline{\text{INT0}}$ pin is multiplexed with the pulse output forced cutoff input for timer RC and timer RD, and the external trigger input for timer RB2. The $\overline{\text{INT2}}$ pin is multiplexed with the event input enabled for timer RJ.

Table 11.9 lists the Pin Configuration for $\overline{\text{INTi}}$ Interrupts (i = 0 to 4).

Table 11.9 Pin Configuration for $\overline{\text{INTi}}$ Interrupts (i = 0 to 4)

Pin Name	I/O	Function
$\overline{\text{INT0}}$	Input	$\overline{\text{INT0}}$ interrupt input
$\overline{\text{INT1}}$	Input	$\overline{\text{INT1}}$ interrupt input
$\overline{\text{INT2}}$	Input	$\overline{\text{INT2}}$ interrupt input
$\overline{\text{INT3}}$	Input	$\overline{\text{INT3}}$ interrupt input
$\overline{\text{INT4}}$	Input	$\overline{\text{INT4}}$ interrupt input

11.5.2 $\overline{\text{INTi}}$ Input Filter (i = 0 to 4)

The $\overline{\text{INTi}}$ input includes a digital filter. The sampling clock can be selected by bits INTiF0 and INTiF1 in registers INTF and INTF1. The $\overline{\text{INTi}}$ level is sampled every sampling clock cycle, and the corresponding IR bit in the INTiIC register is set to 1 (interrupt requested) when the sampled input level matches three times.
Figure 11.9 shows the $\overline{\text{INTi}}$ Input Filter Configuration (i = 0 to 4) and Figure 11.10 shows an Example of $\overline{\text{INTi}}$ Input Filter Operation (i = 0 to 4).

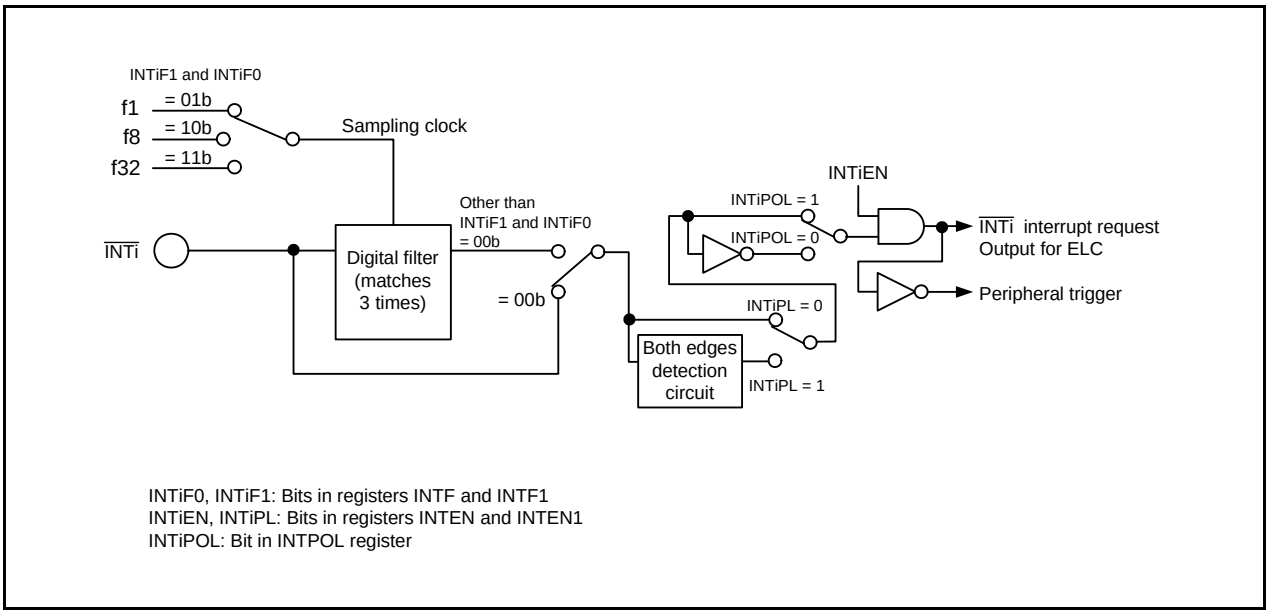


Figure 11.9 $\overline{\text{INTi}}$ Input Filter Configuration (i = 0 to 4)

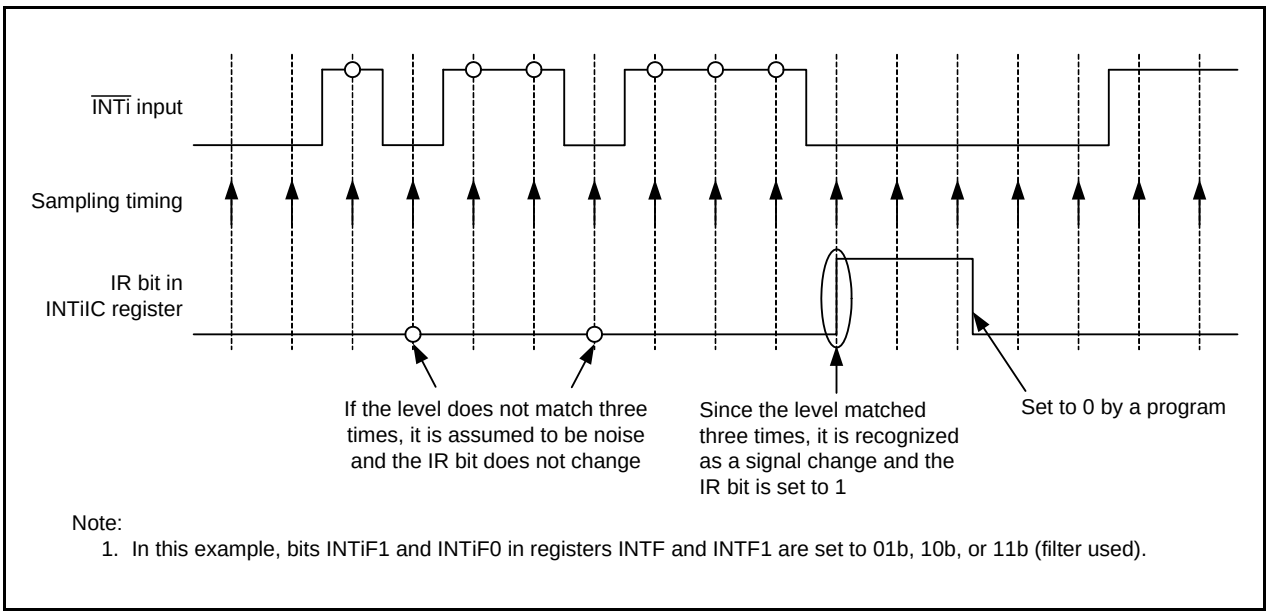


Figure 11.10 Example of $\overline{\text{INTi}}$ Input Filter Operation (i = 0 to 4)

11.6 Key Input Interrupt

A key input interrupt request is generated by one of the input edges on pins $\overline{KI0}$ to $\overline{KI3}$. The key input interrupt is used as a key-on wake-up function to cancel wait mode or stop mode.

The KIiEN bit (i = 0 to 3) in the KIEN register is used to select whether the pins are used as the $\overline{KIi}$ input. The KIiPL bit in the KIEN register can be used to select the input polarity.

When a low level is input to the $\overline{KIi}$ pin, which sets the KIiPL bit to 0 (falling edge), inputs to the other pins $\overline{KI0}$ to $\overline{KI3}$ are not detected as interrupts. Likewise, when a high level is input to the $\overline{KIi}$ pin, which sets the KIiPL bit to 1 (rising edge), inputs to the other pins $\overline{KI0}$ to $\overline{KI3}$ are not detected as interrupts.

Figure 11.11 shows the Key Input Interrupt Block Diagram (i = 0 to 3). Table 11.10 lists the Key Input Interrupt Pin Configuration.

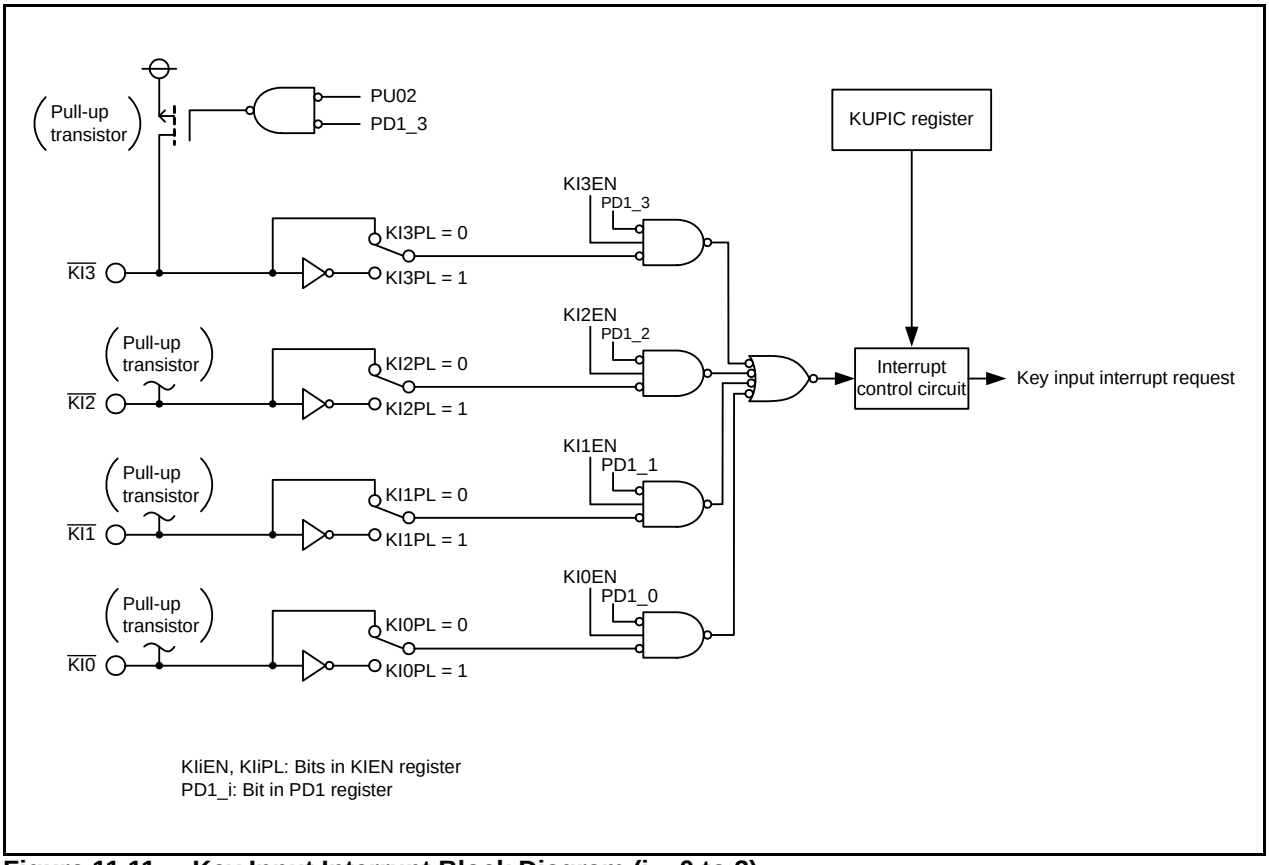


Figure 11.11 Key Input Interrupt Block Diagram (i = 0 to 3)

Table 11.10 Key Input Interrupt Pin Configuration

Pin Name	I/O	Function
$\overline{KI0}$	Input	$\overline{KI0}$ interrupt input
$\overline{KI1}$	Input	$\overline{KI1}$ interrupt input
$\overline{KI2}$	Input	$\overline{KI2}$ interrupt input
$\overline{KI3}$	Input	$\overline{KI3}$ interrupt input

11.7 Address Match Interrupt

An address match interrupt request is generated immediately before execution of the instruction at the address indicated by the AIADRij register (i = 0 or 1, j = L or H). This interrupt is used as a break function for the debugger. When the on-chip debugger is used, do not set an address match interrupt (registers AIENi, AIADRij, and fixed vector table) in the user system.

Set the start address of any instruction in the AIADRij register. The AIENi0 bit in the AIENi register can be used to enable or disable the interrupt. The address match interrupt is not affected by the I flag in the FLG register and IPL. The PC value (refer to **11.4.7 Saving Registers**), which is saved on the stack when an address match interrupt request is acknowledged, will differ depending on the instruction at the address indicated by the AIADRij register. (The appropriate return address is not saved on the stack.) Therefore, when returning from the address match interrupt, use one of the following methods:

- Rewrite the contents of the stack and use the REIT instruction to return.
- Use an instruction such as POP to restore the stack to its previous state where the interrupt request was acknowledged. Then use a jump instruction to return.

Table 11.11 lists the PC Value Saved when Address Match Interrupt Request is Acknowledged. Table 11.12 lists the Correspondence between Address Match Interrupt Sources and Associated Registers.

Table 11.11 PC Value Saved when Address Match Interrupt Request is Acknowledged

Instruction at Address Indicated by AIADRij Register (i = 0 or 1, j = L or H)	PC Value Saved (1)
• Instruction with 2-byte operation code (2) • Instruction with 1-byte operation code (2) ADD.B:S #IMM8, dest SUB.B:S #IMM8, dest AND.B:S #IMM8,dest OR.B:S #IMM8, dest MOV.B:S #IMM8, dest STZ #IMM8,dest STNZ #IMM8, dest STZX #IMM81, #IMM82,dest CMP.B:S #IMM8, dest PUSHM src POPM dest JMPS #IMM8 JSRS #IMM8 MOV.B:S #IMM, dest (however, dest = A0 or A1)	Address indicated by AIADRij register + 2
Instructions other than above	Address indicated by AIADRij register + 1

Notes:
1. PC value saved: Refer to **11.4.7 Saving Registers**.
2. Operation code: Refer to the **R8C/5x Series User's manual: Software (R01US0007EJ)**. **Chapter 4. Instruction Code/Number of Cycles** contains diagrams showing operation code below each syntax. Operation code is shown in the bold frame in the diagrams.

Table 11.12 Correspondence between Address Match Interrupt Sources and Associated Registers

Address Match Interrupt Source	Address Match Interrupt Enable Bit	Address Match Interrupt Register
Address match interrupt 0	AIEN00	AIADR0j
Address match interrupt 1	AIEN10	AIADR1j

11.8 Timer RC Interrupt, Timer RD Interrupt, Timer RE2 Interrupt, Synchronous Serial Communication Unit/I2C bus Interface, CAN Transmit Interrupt, CAN Receive Interrupt, CAN Error Interrupt, and Flash Memory Interrupt (Interrupts with Multiple Interrupt Request Sources)

The timer RC, timer RD, timer RE2, synchronous serial communication unit/I2C bus interface, CAN transmit, CAN receive, CAN error, and flash memory interrupts each have multiple interrupt request sources. An interrupt request is generated by the logical OR of several interrupt request sources and is reflected in the IR bit in the corresponding interrupt control register. Therefore, each of these peripheral functions has its own interrupt request source status register (status register) and interrupt request source enable register (enable register) to control the generation of interrupt requests (change of the IR bit in the interrupt control register). Table 11.13 lists the Registers Associated with Timer RC, Timer RD, Timer RE2, Synchronous Serial Communication Unit/I2C bus Interface, CAN Transmit, CAN Receive, CAN Error and Flash Memory Interrupts.Figure 11.12 shows the Timer RD Interrupt Block Diagram (i = 0 or 1).

Table 11.13 Registers Associated with Timer RC, Timer RD, Timer RE2, Synchronous Serial Communication Unit/I2C bus Interface, CAN Transmit, CAN Receive, CAN Error and Flash Memory Interrupts

Peripheral Function Name		Status Register of Interrupt Request Source	Enable Register of Interrupt Request Source	Interrupt Control Register
Timer RC		TRCSR	TRCIER	TRCIC
Timer RD_0	Timer RD0_0	TRDSR0_0	TRDIER0_0	TRD0IC_0
	Timer RD1_0	TRDSR1_0	TRDIER1_0	TRD1IC_0
Timer RE2		TREIFR	TREIER	TRE2IC
Synchronous serial communication unit/I2C bus interface		SISR_0	SIER_0	SSUIC_0/IICIC_0
		SISR_1	SIER_1	SSUIC_1/IICIC_1
CAN_0	CAN_0 transmit	CANISR_0	CANIE_0	CANRXIC_0
	CAN_0 receive			CANTXIC_0
	CAN_0 error			CANERIC_0
Flash memory		RDYSTI	RDYSTIE	FMRDYIC
		BSYAEI	BSYAEIE	
			CMDERIE	

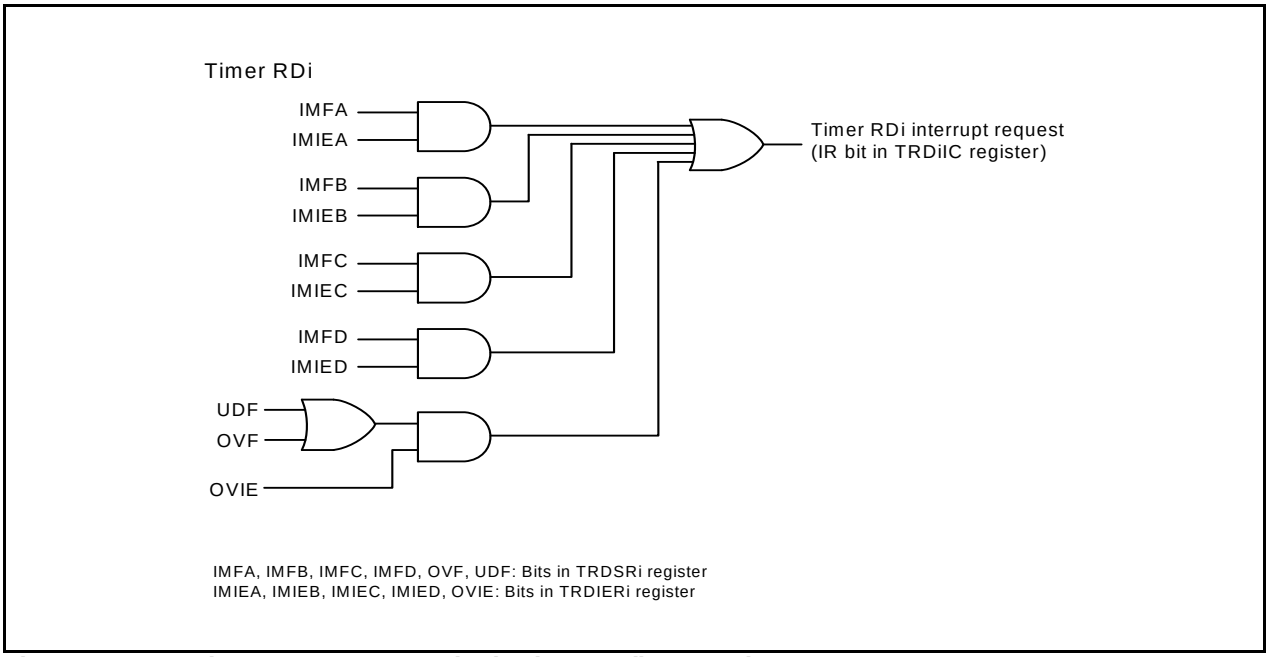


Figure 11.12 Timer RD Interrupt Block Diagram (i = 0 or 1)

As with other maskable interrupts, the timer RC, timer RD, timer RE2, synchronous serial communication unit/I^{2}C bus interface, CAN transmit, CAN receive, CAN error, and flash memory interrupts are controlled by the combination of the IR bit, bits ILVL0 to ILVL2, and IPL. However, since each interrupt source is generated by a combination of multiple interrupt request sources, the following differences from other maskable interrupts apply:

- When bits in the enable register are set to 1 and the corresponding bits in the status register are set to 1 (interrupt enabled), the IR bit in the interrupt control register is set to 1 (interrupt requested).
- When either bits in the status register or the corresponding bits in the enable register, or both are set to 0, the IR bit is set to 0 (no interrupt requested).
  That is, even if the interrupt is not acknowledged after the IR bit is set to 1, the interrupt request will not be retained.
  Also, if 0 is written to the IR bit, this bit is temporarily set to 0 (for five cycles of the CPU clock) and then set back to 1.
- Individual bits in the status register are not automatically set to 0 even if the interrupt is acknowledged.
  The IR bit is also not automatically set to 0 when the interrupt is acknowledged.
  Set individual bits in the status register to 0 in the interrupt routine. Refer to the status register figure for how to set individual bits in the status register to 0.
- When multiple bits in the enable register are set to 1 and other request sources are generated after the IR bit is set to 1, the IR bit remains 1.
- When multiple bits in the enable register are set to 1, use the status register to determine which request source causes an interrupt.
  When interrupt source bits and enable bits are cleared by software, the IR bit is cleared after a maximum of two cycles of the CPU clock.

Refer to the chapters of the individual peripheral functions (**17. Timer RC**, **18. Timer RD**, **19. Timer RE2**, **22. Clock Synchronous Serial Interface**, **24. CAN Module** and **27. Flash Memory**) for the status register and enable register.
For the interrupt control register, refer to **11.4 Interrupt Control**.

11.9 Notes on Interrupts

11.9.1 Reading Address 00000h

Do not read address 00000h by a program. When an external interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from address 00000h in the interrupt sequence. At this time, the corresponding IR bit in the interrupt control register for the acknowledged interrupt is set to 0.

If a program is used to read address 00000h, the corresponding IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

11.9.2 SP Setting

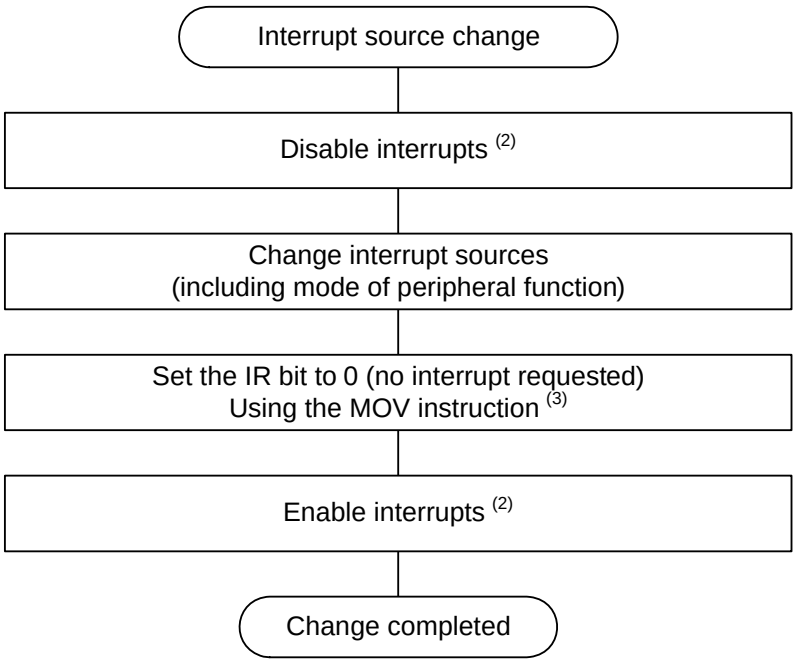
Set a value in the SP before any interrupt is acknowledged. The SP is 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

11.9.3 External Interrupt, Key Input Interrupt

Signal input to pins $\overline{\text{INT0}}$ to $\overline{\text{INT4}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ must meet either the low-level width or the high-level width requirements shown in External Interrupt $\overline{\text{INT0}}$ to $\overline{\text{INT4}}$ Input in the Electrical Characteristics, regardless of the CPU operating clock.

11.9.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source is changed. To use an interrupt, set the IR bit to 0 (no interrupt requested) after changing interrupt sources.
Changing interrupt sources as referred to here includes all factors that change the source, polarity, or timing of the interrupt assigned to a software interrupt number. Therefore, if a mode change of a peripheral function involves the source, polarity, or timing of an interrupt, set the IR bit to 0 (no interrupt requested) after making these changes. Refer to the descriptions of the individual peripheral functions for related interrupts.
Figure 11.13 shows a Procedure Example for Changing Interrupt Sources.



IR bit: Corresponding interrupt control register bit for the interrupt whose source is to be changed

Notes:
1. The above settings must be executed individually. Do not execute two or more settings simultaneously (using one instruction).
2. To prevent interrupt requests from being generated, disable the peripheral function before changing the interrupt source. In this case, use the I flag if all maskable interrupts can be disabled.
   If all maskable interrupts cannot be disabled, use bits ILVL0 to ILVL2 for the interrupt whose source is to be changed.
3. To change the interrupt source to an input with the digital filter used, wait for at least three cycles of the digital filter sampling clock + two cycles of the CPU clock before setting the IR bit to 0 (no interrupt requested).
   Refer to **11.9.5 Rewriting Interrupt Control Registers** for the instructions to use and related notes.

Figure 11.13 Procedure Example for Changing Interrupt Sources

11.9.5 Rewriting Interrupt Control Register

(a) The contents of the interrupt control register can be rewritten only while no interrupt requests corresponding to that register are generated. If an interrupt request may be generated, disable the interrupt before rewriting the contents of the interrupt control register.

(b) When rewriting the contents of the interrupt control register after disabling the interrupt, be careful to choose appropriate instructions

Changing any bit other than the IR bit

If an interrupt request corresponding to the register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt may be ignored. If this causes a problem, use one of the following instructions to rewrite the contents of the register:

Applicable instructions..... AND, OR, BCLR, and BSET

Changing the IR bit

Depending on the instruction used, the IR bit may not be set to 0 (no interrupt requested). Use the MOV instruction to set the IR bit to 0.

(c) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below. (Refer to (b) regarding rewriting the contents of interrupt control registers using the sample programs.)

Examples 1 to 3 show how to prevent the I flag from being set to 1 (interrupt enabled) before the contents of the interrupt control register are rewritten due to effects of the internal bus and the instruction queue buffer.

Example 1: Use the NOP instructions to pause the program until the interrupt control register is rewritten

```
INT_SWITCH1:
  FCLR    I              ; Interrupt disabled
  MOV.B   #00H, 0056H    ; Set the TRJIC_0 register to 00h
  NOP                    ;
  NOP
  FSET    I              ; Interrupt enabled
```

Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
  FCLR    I              ; Interrupt disabled
  MOV.B   #00H, 0056H    ; Set the TRJIC_0 register to 00h
  MOV.W   MEM, R0        ; Dummy read
  FSET    I              ; Interrupt enabled
```

Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
  PUSHC   FLG
  FCLR    I              ; Interrupt disabled
  MOV.B   #00H, 0056H    ; Set the TRJIC_0 register to 00h
  POPC    FLG            ; Interrupt enabled
```

12. Event Link Controller (ELC)

The event link controller (ELC) mutually connects (links) events output from each peripheral function. By linking events, it becomes possible to coordinate operation between peripheral functions directly without going through the CPU.

12.1 Overview

The ELC has the following functions.

- Capable of directly linking 22 types of event signals output from peripheral functions to specified peripheral functions
- Event signals can be used as activation sources for operating any one of 7 peripheral functions

Figure 12.1 shows the Event Link Controller Block Diagram (n = 0 to 4, 8 to 24).

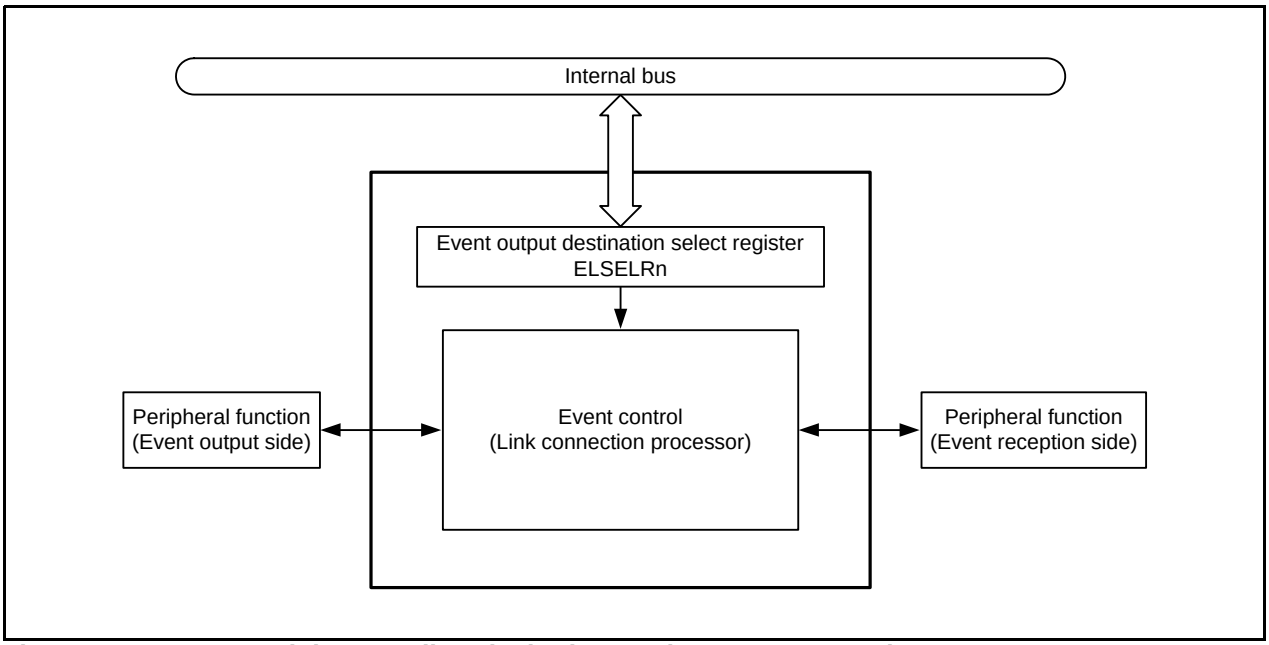


Figure 12.1 Event Link Controller Block Diagram (n = 0 to 4, 8 to 24)

12.2 Registers

Table 12.1 lists the ELC Register Configuration.

Table 12.1 ELC Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Event Output Destination Select Register 0	ELSELR0	00h	06A00h	8
Event Output Destination Select Register 1	ELSELR1	00h	06A01h	8
Event Output Destination Select Register 2	ELSELR2	00h	06A02h	8
Event Output Destination Select Register 3	ELSELR3	00h	06A03h	8
Event Output Destination Select Register 4	ELSELR4	00h	06A04h	8
Event Output Destination Select Register 8	ELSELR8	00h	06A08h	8
Event Output Destination Select Register 9	ELSELR9	00h	06A09h	8
Event Output Destination Select Register 10	ELSELR10	00h	06A0Ah	8
Event Output Destination Select Register 11	ELSELR11	00h	06A0Bh	8
Event Output Destination Select Register 12	ELSELR12	00h	06A0Ch	8
Event Output Destination Select Register 13	ELSELR13	00h	06A0Dh	8
Event Output Destination Select Register 14	ELSELR14	00h	06A0Eh	8
Event Output Destination Select Register 15	ELSELR15	00h	06A0Fh	8
Event Output Destination Select Register 16	ELSELR16	00h	06A10h	8
Event Output Destination Select Register 17	ELSELR17	00h	06A11h	8
Event Output Destination Select Register 18	ELSELR18	00h	06A12h	8
Event Output Destination Select Register 19	ELSELR19	00h	06A13h	8
Event Output Destination Select Register 20	ELSELR20	00h	06A14h	8
Event Output Destination Select Register 21	ELSELR21	00h	06A15h	8
Event Output Destination Select Register 22	ELSELR22	00h	06A16h	8
Event Output Destination Select Register 23	ELSELR23	00h	06A17h	8
Event Output Destination Select Register 24	ELSELR24	00h	06A18h	8

12.2.1 Event Output Destination Select Register n (ELSELRn) (n = 0 to 4, 8 to 24)

Address 06A00h (ELSELR0) to 06A04h (ELSELR4), 06A08h (ELSELR8) to 06A18h (ELSELR24)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	ELSEL3	ELSEL2	ELSEL1	ELSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ELSEL0	Event link select 0 bit	b3 b2 b1 b0 0 0 0 0: Event link disabled 0001 to 1111: Select operation of peripheral function to link (1)	R/W
b1	ELSEL1	Event link select 1 bit		R/W
b2	ELSEL2	Event link select 2 bit		R/W
b3	ELSEL3	Event link select 3 bit		R/W
b4	—	Reserved	The read value is 0.	R
b5	—			
b6	—			
b7	—			

Note:
1. Refer to **Table 12.3 Correspondence between Values Set to ELSELRn (n = 0 to 4, 8 to 24) Registers and Operation of Link Destination Peripheral Functions at Reception**.

An ELSELRn register links each event signal to an operation of an event-receiving peripheral function (link destination peripheral function) at reception.
Do not set multiple event inputs to the same event output destination (event reception side). The operation of the event-receiving peripheral function will become undefined, and event signals may not be received correctly. Set an ELSELRn register during a period when no event output peripheral functions are generating event signals.
Tables 12.2 lists the Correspondence between ELSELRn (n = 0 to 4, 8 to 24) Registers and Peripheral Functions, and Table 12.3 lists the Correspondence between Values Set to ELSELRn (n = 0 to 4, 8 to 24) Registers and Operation of Link Destination Peripheral Functions at Reception.

Table 12.2 Correspondence between ELSELRn (n = 0 to 4, 8 to 24) Registers and Peripheral Functions

Register Name	Event Generator (Output Origin of Event Input n)	Event Description
ELSELR0	External interrupt	$\overline{\text{INT0}}$ input level
ELSELR1	External interrupt	$\overline{\text{INT1}}$ input level/comparison result change
ELSELR2	External interrupt	$\overline{\text{INT2}}$ input level
ELSELR3	External interrupt	$\overline{\text{INT3}}$ input level/comparison result change
ELSELR4	External interrupt	$\overline{\text{INT4}}$ input level
ELSELR8	External interrupt	Key input event
ELSELR9	Timer RJ_0	Timer RJ_0 underflow
ELSELR10	Timer RJ_1	Timer RJ_1 underflow
ELSELR11	Timer RE2	Timer RE2 compare match
ELSELR12	Timer RB2_0	Timer RB2_0 underflow
ELSELR13	Timer RC_0	Timer RC_0 compare match A
ELSELR14	Timer RC_0	Timer RC_0 compare match B
ELSELR15	Timer RC_0	Timer RC_0 compare match C
ELSELR16	Timer RC_0	Timer RC_0 compare match D
ELSELR17	Timer RD0_0	Timer RD0_0 compare match A
ELSELR18	Timer RD0_0	Timer RD0_0 compare match B
ELSELR19	Timer RD0_0	Timer RD0_0 compare match C
ELSELR20	Timer RD0_0	Timer RD0_0 compare match D
ELSELR21	Timer RD1_0	Timer RD1_0 compare match A
ELSELR22	Timer RD1_0	Timer RD1_0 compare match B
ELSELR23	Timer RD1_0	Timer RD1_0 compare match C
ELSELR24	Timer RD1_0	Timer RD1_0 compare match D

Table 12.3 Correspondence between Values Set to ELSELRn (n = 0 to 4, 8 to 24) Registers and Operation of Link Destination Peripheral Functions at Reception

Bits ELSEL3 to ELSEL0 in ELSELRn Register	Link Destination Peripheral Function	Operation when Receiving Event
0001b	10-bit A/D converter	A/D conversion start trigger
0010b	Timer RJ_0	Event count operation
0011b	Timer RJ_1	Event count operation
0100b (1)	—	—
0101b (1)	—	—
0110b	Timer RB2_0	Count start trigger of programmable one-shot generation mode, count start trigger of programmable wait one-shot generation mode
0111b (1)	—	—
1000b	Timer RC_0	Input capture, external trigger of PWM2 mode
1001b (1)	—	—
1010b	Timer RD0_0	Input capture, pulse output forced cutoff
1011b	Timer RD1_0	Input capture, pulse output forced cutoff
1100b (1)	—	—
1101b (1)	—	—
1110b (1)	—	—
1111b (1)	—	—

Note:
1. Do not set any value.

12.3 Operation

The path for using an event signal generated by a peripheral function as an interrupt request to the interrupt control circuit is independent from the path for using it as an ELC event. Therefore, each event signal can be used as an event signal for operation of an event-receiving peripheral function, regardless of interrupt control.
In addition, event link operation can be performed without being influenced by the presence or absence of a CPU clock supply. However, the operating clock of a peripheral function needs to be supplied and be in an operational state.
Figure 12.2 shows the Relationship between Interrupt Handling and ELC. This figure shows the configuration when a peripheral function such as timer RC, which has status flags and a register that controls enabling of interrupts, is set to the ELC event output. By supplying an interrupt request (event signal) separately to the ELC and the interrupt control circuit, the ELC and interrupt control can be operated independently. The ELC and interrupt control do not affect each other.
An event signal applied to the ELC is input each time an event is generated. This event signal allows the event receiving peripheral function to perform operations at event reception. Thus, it is unnecessary to clear the status flag or the interrupt request bit (IR bit) by software.
Table 12.4 lists the Responses of Event Receiving Peripheral Functions.
A peripheral function which receives an event from the ELC will perform the operation corresponding to the event-receiving peripheral function after reception of an event (Refer to **Table 12.3 Correspondence between Values Set to ELSELRn (n = 0 to 4, 8 to 24) Registers and Operation of Link Destination Peripheral Functions at Reception**).

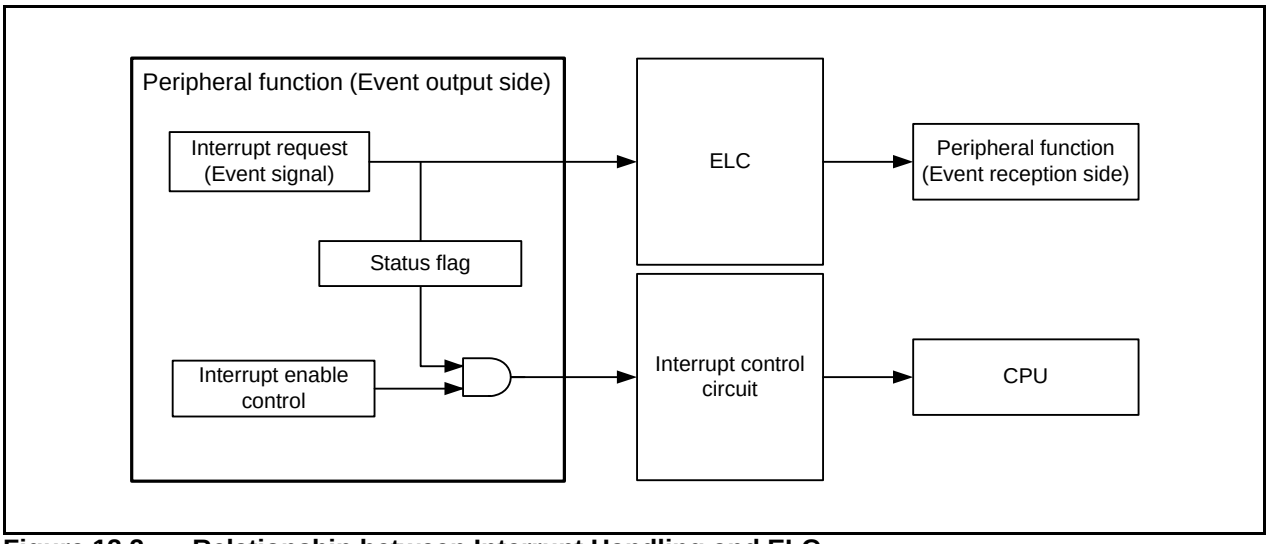


Figure 12.2 Relationship between Interrupt Handling and ELC

Table 12.4 Responses of Event Receiving Peripheral Functions

Event Reception Side No. (Event Trigger No.)	Link Destination Module	Operation after Event Reception	Real-Timeliness of Operation after Event Reception
1	A/D Converter	A/D conversion start trigger	A conversion start trigger is generated 2 or 3 cycles of the A/D converter operating clock (1) after ELC event generation.
2	Timer RJ_0	Event count operation	An event from the ELC is used directly as the count clock. (No time lag in sampling at the internal clock, etc.)
3	Timer RJ_1		
6	Timer RB2_0	Count start trigger of one-shot generation mode/count start trigger of delayed one-shot generation mode	A conversion start trigger is generated 2 or 3 cycles of the timer RB2 operating clock after ELC event generation.
8	Timer RC_0	Input capture/external trigger of PWM2 mode	Input capture, PWM2 mode: A count start trigger is generated 2 or 3 cycles of the timer RC operating clock (1) after ELC event generation.
a	Timer RD0_0	Input capture/pulse output forced cutoff	Input capture: A count start trigger is generated 2 or 3 cycles of the timer RD operating clock (1) after ELC event generation. Pulse output forced cutoff: The pulse output is forcibly cut off 2 or 3 cycles of the timer RD operating clock (1) after ELC event generation.
b	Timer RD1_0	Input capture/pulse output forced cutoff	

Note:
1. Refer to the chapter of each peripheral function for details on the operating clock.

13. DTC

The DTC (data transfer controller) is a function that transfers data between the SFR and on-chip memory without using the CPU. The DTC is activated by a peripheral function interrupt to perform data transfers. The DTC and CPU use the same bus, and the DTC takes priority over the CPU in using the bus.
To control DTC data transfers, control data comprised of a transfer source address, a transfer destination address, and operating modes are allocated in the DTC control data area. Each time the DTC is activated, the DTC reads control data to perform data transfers.

13.1 Overview

Table 13.1 lists the DTC Specifications.

Table 13.1 DTC Specifications

Item		Specification
Activation sources		36 sources
Allocatable control data		24 sets
Address space which can be transferred		64 Kbytes (00000h to 0FFFFh)
Maximum number of transfers	Normal mode	256 times
	Repeat mode	255 times
Maximum size of block to be transferred	Normal mode	256 bytes
	Repeat mode	255 bytes
Unit of transfers		Byte, word
Transfer mode	Normal mode	Transfers end on completion of the transfer causing the DTCCTj register value to change from 1 to 0.
	Repeat mode	On completion of the transfer causing the DTCCTj register value to change from 1 to 0, the repeat area address is initialized and the DTRLDj register value is reloaded to the DTCCTj register to continue transfers.
Address control	Normal mode	Fixed or incremented
	Repeat mode	Addresses of the area not selected as the repeat area are fixed or incremented.
Priority of activation sources		Refer to **Table 13.8 DTC Activation Sources and DTC Vector Addresses**.
Interrupt request	Normal mode	When the data transfer causing the DTCCTj register value to change from 1 to 0 is performed, the activation source interrupt request is generated for the CPU, and interrupt handling is performed on completion of the data transfer.
	Repeat mode	When the data transfer causing the DTCCTj register value to change from 1 to 0 is performed while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled), the activation source interrupt request is generated for the CPU, and interrupt handling is performed on completion of the transfer.
Transfer start		When bits DTCENi0 to DTCENi7 in the DTCENi registers are set to 1 (activation enabled), data transfer is started each time the corresponding DTC activation sources are generated.
Transfer stop	Normal mode	• When bits DTCENi0 to DTCENi7 are set to 0 (activation disabled). • When the data transfer causing the DTCCTj register value to change from 1 to 0 is completed.
	Repeat mode	• When bits DTCENi0 to DTCENi7 are set to 0 (activation disabled). • When the data transfer causing the DTCCTj register value to change from 1 to 0 is completed while the RPTINT bit is 1 (interrupt generation enabled).

i = 0 to 6, j = 0 to 23

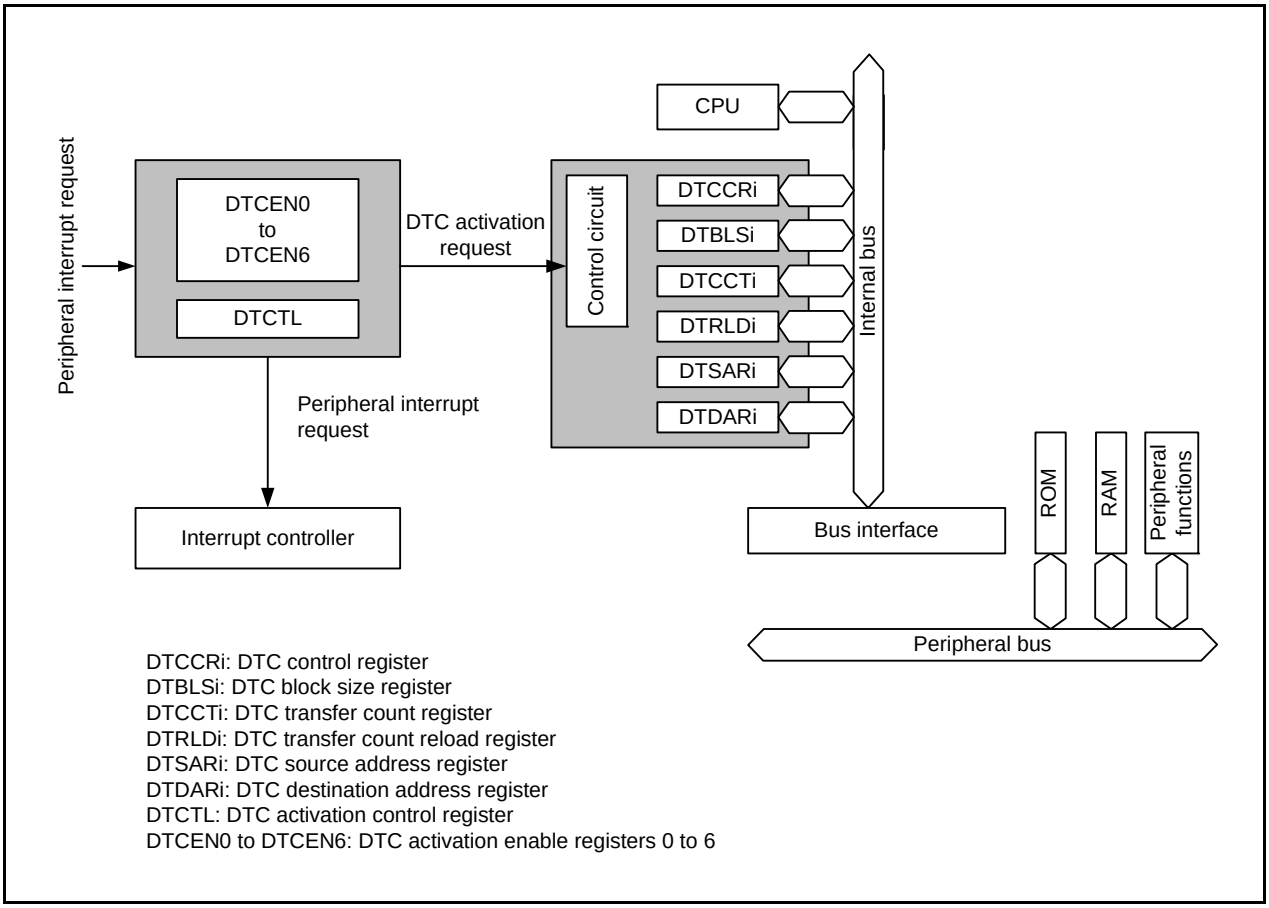


Figure 13.1 DTC Block Diagram (i = 0 to 23)

13.2 Registers

When the DTC is activated, control data (DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj, j = 0 to 23) allocated in the RAM control data area is read, and then transferred to the control registers (DTCCR, DTBLS, DTCCT, DTRLD, DTSAR, and DTDAR) in the DTC. On completion of the DTC data transfer, the contents of the DTC control registers are written back to the control data area.

The DTCCR, DTBLS, DTCCT, DTRLD, DTSAR, and DTDAR registers cannot be accessed directly. DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj can be directly accessed by the system bus. Also, registers DTCTL and DTCENi (i = 0 to 6) can be accessed via the peripheral bus.
Tables 13.2 to 13.5 list the DTC Register Configuration.

Table 13.2 DTC Register Configuration (1)

Register Name	Symbol	After Reset	Address	Access Size
DTC Activation Control Register	DTCTL	00h	00280h	8
DTC Activation Enable Register 0	DTCEN0	00h	00288h	8
DTC Activation Enable Register 1	DTCEN1	00h	00289h	8
DTC Activation Enable Register 2	DTCEN2	00h	0028Ah	8
DTC Activation Enable Register 3	DTCEN3	00h	0028Bh	8
DTC Activation Enable Register 4	DTCEN4	00h	0028Ch	8
DTC Activation Enable Register 5	DTCEN5	00h	0028Dh	8
DTC Activation Enable Register 6	DTCEN6	00h	0028Eh	8
DTC Control Register 0	DTCCR0	XXh	06C40h	8
DTC Block Size Register 0	DTBLS0	XXh	06C41h	8
DTC Transfer Count Register 0	DTCCT0	XXh	06C42h	8
DTC Transfer Count Reload Register 0	DTRLD0	XXh	06C43h	8
DTC Source Address Register 0	DTSAR0	XXXXh	06C44h	16
DTC Destination Address Register 0	DTDAR0	XXXXh	06C46h	16
DTC Control Register 1	DTCCR1	XXh	06C48h	8
DTC Block Size Register 1	DTBLS1	XXh	06C49h	8
DTC Transfer Count Register 1	DTCCT1	XXh	06C4Ah	8
DTC Transfer Count Reload Register 1	DTRLD1	XXh	06C4Bh	8
DTC Source Address Register 1	DTSAR1	XXXXh	06C4Ch	16
DTC Destination Address Register 1	DTDAR1	XXXXh	06C4Eh	16
DTC Control Register 2	DTCCR2	XXh	06C50h	8
DTC Block Size Register 2	DTBLS2	XXh	06C51h	8
DTC Transfer Count Register 2	DTCCT2	XXh	06C52h	8
DTC Transfer Count Reload Register 2	DTRLD2	XXh	06C53h	8
DTC Source Address Register 2	DTSAR2	XXXXh	06C54h	16
DTC Destination Address Register 2	DTDAR2	XXXXh	06C56h	16
DTC Control Register 3	DTCCR3	XXh	06C58h	8
DTC Block Size Register 3	DTBLS3	XXh	06C59h	8
DTC Transfer Count Register 3	DTCCT3	XXh	06C5Ah	8
DTC Transfer Count Reload Register 3	DTRLD3	XXh	06C5Bh	8
DTC Source Address Register 3	DTSAR3	XXXXh	06C5Ch	16
DTC Destination Address Register 3	DTDAR3	XXXXh	06C5Eh	16
DTC Control Register 4	DTCCR4	XXh	06C60h	8
DTC Block Size Register 4	DTBLS4	XXh	06C61h	8
DTC Transfer Count Register 4	DTCCT4	XXh	06C62h	8
DTC Transfer Count Reload Register 4	DTRLD4	XXh	06C63h	8

Table 13.3 DTC Register Configuration (2)

Register Name	Symbol	After Reset	Address	Access Size
DTC Source Address Register 4	DTSAR4	XXXXh	06C64h	16
DTC Destination Address Register 4	DTDAR4	XXXXh	06C66h	16
DTC Control Register 5	DTCCR5	XXh	06C68h	8
DTC Block Size Register 5	DTBLS5	XXh	06C69h	8
DTC Transfer Count Register 5	DTCCT5	XXh	06C6Ah	8
DTC Transfer Count Reload Register 5	DTRLD5	XXh	06C6Bh	8
DTC Source Address Register 5	DTSAR5	XXXXh	06C6Ch	16
DTC Destination Address Register 5	DTDAR5	XXXXh	06C6Eh	16
DTC Control Register 6	DTCCR6	XXh	06C70h	8
DTC Block Size Register 6	DTBLS6	XXh	06C71h	8
DTC Transfer Count Register 6	DTCCT6	XXh	06C72h	8
DTC Transfer Count Reload Register 6	DTRLD6	XXh	06C73h	8
DTC Source Address Register 6	DTSAR6	XXXXh	06C74h	16
DTC Destination Address Register 6	DTDAR6	XXXXh	06C76h	16
DTC Control Register 7	DTCCR7	XXh	06C78h	8
DTC Block Size Register 7	DTBLS7	XXh	06C79h	8
DTC Transfer Count Register 7	DTCCT7	XXh	06C7Ah	8
DTC Transfer Count Reload Register 7	DTRLD7	XXh	06C7Bh	8
DTC Source Address Register 7	DTSAR7	XXXXh	06C7Ch	16
DTC Destination Address Register 7	DTDAR7	XXXXh	06C7Eh	16
DTC Control Register 8	DTCCR8	XXh	06C80h	8
DTC Block Size Register 8	DTBLS8	XXh	06C81h	8
DTC Transfer Count Register 8	DTCCT8	XXh	06C82h	8
DTC Transfer Count Reload Register 8	DTRLD8	XXh	06C83h	8
DTC Source Address Register 8	DTSAR8	XXXXh	06C84h	16
DTC Destination Address Register 8	DTDAR8	XXXXh	06C86h	16
DTC Control Register 9	DTCCR9	XXh	06C88h	8
DTC Block Size Register 9	DTBLS9	XXh	06C89h	8
DTC Transfer Count Register 9	DTCCT9	XXh	06C8Ah	8
DTC Transfer Count Reload Register 9	DTRLD9	XXh	06C8Bh	8
DTC Source Address Register 9	DTSAR9	XXXXh	06C8Ch	16
DTC Destination Address Register 9	DTDAR9	XXXXh	06C8Eh	16
DTC Control Register 10	DTCCR10	XXh	06C90h	8
DTC Block Size Register 10	DTBLS10	XXh	06C91h	8
DTC Transfer Count Register 10	DTCCT10	XXh	06C92h	8
DTC Transfer Count Reload Register 10	DTRLD10	XXh	06C93h	8
DTC Source Address Register 10	DTSAR10	XXXXh	06C94h	16
DTC Destination Address Register 10	DTDAR10	XXXXh	06C96h	16
DTC Control Register 11	DTCCR11	XXh	06C98h	8
DTC Block Size Register 11	DTBLS11	XXh	06C99h	8
DTC Transfer Count Register 11	DTCCT11	XXh	06C9Ah	8
DTC Transfer Count Reload Register 11	DTRLD11	XXh	06C9Bh	8
DTC Source Address Register 11	DTSAR11	XXXXh	06C9Ch	16
DTC Destination Address Register 11	DTDAR11	XXXXh	06C9Eh	16
DTC Control Register 12	DTCCR12	XXh	06CA0h	8
DTC Block Size Register 12	DTBLS12	XXh	06CA1h	8
DTC Transfer Count Register 12	DTCCT12	XXh	06CA2h	8

Table 13.4 DTC Register Configuration (3)

Register Name	Symbol	After Reset	Address	Access Size
DTC Transfer Count Reload Register 12	DTRLD12	XXh	06CA3h	8
DTC Source Address Register 12	DTSAR12	XXXXh	06CA4h	16
DTC Destination Address Register 12	DTDAR12	XXXXh	06CA6h	16
DTC Control Register 13	DTCCR13	XXh	06CA8h	8
DTC Block Size Register 13	DTBLS13	XXh	06CA9h	8
DTC Transfer Count Register 13	DTCCT13	XXh	06CAAh	8
DTC Transfer Count Reload Register 13	DTRLD13	XXh	06CABh	8
DTC Source Address Register 13	DTSAR13	XXXXh	06CACh	16
DTC Destination Address Register 13	DTDAR13	XXXXh	06CAEh	16
DTC Control Register 14	DTCCR14	XXh	06CB0h	8
DTC Block Size Register 14	DTBLS14	XXh	06CB1h	8
DTC Transfer Count Register 14	DTCCT14	XXh	06CB2h	8
DTC Transfer Count Reload Register 14	DTRLD14	XXh	06CB3h	8
DTC Source Address Register 14	DTSAR14	XXXXh	06CB4h	16
DTC Destination Address Register 14	DTDAR14	XXXXh	06CB6h	16
DTC Control Register 15	DTCCR15	XXh	06CB8h	8
DTC Block Size Register 15	DTBLS15	XXh	06CB9h	8
DTC Transfer Count Register 15	DTCCT15	XXh	06CBAh	8
DTC Transfer Count Reload Register 15	DTRLD15	XXh	06CBBh	8
DTC Source Address Register 15	DTSAR15	XXXXh	06CBCh	16
DTC Destination Address Register 15	DTDAR15	XXXXh	06CBEh	16
DTC Control Register 16	DTCCR16	XXh	06CC0h	8
DTC Block Size Register 16	DTBLS16	XXh	06CC1h	8
DTC Transfer Count Register 16	DTCCT16	XXh	06CC2h	8
DTC Transfer Count Reload Register 16	DTRLD16	XXh	06CC3h	8
DTC Source Address Register 16	DTSAR16	XXXXh	06CC4h	16
DTC Destination Address Register 16	DTDAR16	XXXXh	06CC6h	16
DTC Control Register 17	DTCCR17	XXh	06CC8h	8
DTC Block Size Register 17	DTBLS17	XXh	06CC9h	8
DTC Transfer Count Register 17	DTCCT17	XXh	06CCAh	8
DTC Transfer Count Reload Register 17	DTRLD17	XXh	06CCBh	8
DTC Source Address Register 17	DTSAR17	XXXXh	06CCCh	16
DTC Destination Address Register 17	DTDAR17	XXXXh	06CCEh	16
DTC Control Register 18	DTCCR18	XXh	06CD0h	8
DTC Block Size Register 18	DTBLS18	XXh	06CD1h	8
DTC Transfer Count Register 18	DTCCT18	XXh	06CD2h	8
DTC Transfer Count Reload Register 18	DTRLD18	XXh	06CD3h	8
DTC Source Address Register 18	DTSAR18	XXXXh	06CD4h	16
DTC Destination Address Register 18	DTDAR18	XXXXh	06CD6h	16
DTC Control Register 19	DTCCR19	XXh	06CD8h	8
DTC Block Size Register 19	DTBLS19	XXh	06CD9h	8
DTC Transfer Count Register 19	DTCCT19	XXh	06CDAh	8
DTC Transfer Count Reload Register 19	DTRLD19	XXh	06CDBh	8
DTC Source Address Register 19	DTSAR19	XXXXh	06CDCh	16
DTC Destination Address Register 19	DTDAR19	XXXXh	06CDEh	16
DTC Control Register 20	DTCCR20	XXh	06CE0h	8
DTC Block Size Register 20	DTBLS20	XXh	06CE1h	8

Table 13.5 DTC Register Configuration (4)

Register Name	Symbol	After Reset	Address	Access Size
DTC Transfer Count Register 20	DTCCT20	XXh	06CE2h	8
DTC Transfer Count Reload Register 20	DTRLD20	XXh	06CE3h	8
DTC Source Address Register 20	DTSAR20	XXXXh	06CE4h	16
DTC Destination Address Register 20	DTDAR20	XXXXh	06CE6h	16
DTC Control Register 21	DTCCR21	XXh	06CE8h	8
DTC Block Size Register 21	DTBLS21	XXh	06CE9h	8
DTC Transfer Count Register 21	DTCCT21	XXh	06CEAh	8
DTC Transfer Count Reload Register 21	DTRLD21	XXh	06CEBh	8
DTC Source Address Register 21	DTSAR21	XXXXh	06CECh	16
DTC Destination Address Register 21	DTDAR21	XXXXh	06CEEh	16
DTC Control Register 22	DTCCR22	XXh	06CF0h	8
DTC Block Size Register 22	DTBLS22	XXh	06CF1h	8
DTC Transfer Count Register 22	DTCCT22	XXh	06CF2h	8
DTC Transfer Count Reload Register 22	DTRLD22	XXh	06CF3h	8
DTC Source Address Register 22	DTSAR22	XXXXh	06CF4h	16
DTC Destination Address Register 22	DTDAR22	XXXXh	06CF6h	16
DTC Control Register 23	DTCCR23	XXh	06CF8h	8
DTC Block Size Register 23	DTBLS23	XXh	06CF9h	8
DTC Transfer Count Register 23	DTCCT23	XXh	06CFAh	8
DTC Transfer Count Reload Register 23	DTRLD23	XXh	06CFBh	8
DTC Source Address Register 23	DTSAR23	XXXXh	06CFCh	16
DTC Destination Address Register 23	DTDAR23	XXXXh	06CFEh	16

13.2.1 DTC Activation Control Register (DTCTL)

Address 00280h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	NMIF	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	NMIF	Non-maskable interrupt generation bit (1)	0: Non-maskable interrupts not generated 1: Non-maskable interrupts generated	R/W
b2	—	Nothing is assigned. The read value is 0.		R
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. This bit is set to 0 when the read result is 1 and then 0 is written to the same bit. This bit remains unchanged even if the read result is 0 and then 0 is written to the same bit. This bit remains unchanged if 1 is written to it.

NMIF Bit (Non-maskable interrupt generation bit)

The NMIF bit is set to 1 when a watchdog timer interrupt, an oscillation stop detection interrupt, a voltage monitor 1 interrupt, or a voltage monitor 2 interrupt is generated.
When the NMIF bit is 1, the DTC is not activated even if an interrupt which enables DTC activation is generated. If the NMIF bit is changed to 1 during a DTC transfer, the transfer continues until it has completed.

13.2.2 DTC Activation Enable Register i (DTCENi) (i = 0 to 6)

Address 00288h (DTCEN0), 00289h (DTCEN1), 0028Ah (DTCEN2), 0028Bh (DTCEN3), 0028Ch (DTCEN4), 0028Dh (DTCEN5), 0028Eh (DTCEN6)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DTCENi7	DTCENi6	DTCENi5	DTCENi4	DTCENi3	DTCENi2	DTCENi1	DTCENi0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DTCENi0	DTC activation enable bits	0: Activation disabled 1: Activation enabled	R/W
b1	DTCENi1			R/W
b2	DTCENi2			R/W
b3	DTCENi3			R/W
b4	DTCENi4			R/W
b5	DTCENi5			R/W
b6	DTCENi6			R/W
b7	DTCENi7			R/W

The DTCENi registers enable or disable DTC activation by interrupt sources. Table 13.6 lists the Correspondences between Bits DTCENi0 to DTCENi7 (i = 0 to 6) and Interrupt Sources.

Table 13.6 Correspondences between Bits DTCENi0 to DTCENi7 (i = 0 to 6) and Interrupt Sources

Register	DTCENi7 Bit	DTCENi6 Bit	DTCENi5 Bit	DTCENi4 Bit	DTCENi3 Bit	DTCENi2 Bit	DTCENi1 Bit	DTCENi0 Bit
DTCEN0	$\overline{\text{INT0}}$	$\overline{\text{INT1}}$	$\overline{\text{INT2}}$	$\overline{\text{INT3}}$	$\overline{\text{INT4}}$	—	—	—
DTCEN1	Key input	A/D conversion	UART0_0 reception	UART0_0 transmission	UART0_1 reception	UART0_1 transmission	UART2 reception	UART2 transmission
DTCEN2	SSU_0/I²C_0 receive data full	SSU_0/I²C_0 transmit data empty	Voltage monitor 2	Voltage monitor 1	—	—	Timer RC_0 input-capture/ compare-match A	Timer RC_0 input-capture/ compare-match B
DTCEN3	Timer RC_0 input-capture/ compare-match C	Timer RC_0 input-capture/ compare-match D	Timer RD0_0 input-capture/ compare-match A	Timer RD0_0 input-capture/ compare-match B	Timer RD0_0 input-capture/ compare-match C	Timer RD0_0 input-capture/ compare-match D	Timer RD1_0 input-capture/ compare-match A	Timer RD1_0 input-capture/ compare-match B
DTCEN4	Timer RD1_0 input-capture/ compare-match C	Timer RD1_0 input-capture/ compare-match D	—	—	—	—	SSU_1/I²C_1 receive data full	SSU_1/I²C_1 transmit data empty
DTCEN5	—	—	Timer RE2	—	—	—	—	—
DTCEN6	—	Timer RJ_0	Timer RJ_1	Timer RB2	Flash ready status	—	—	—

13.2.3 DTC Control Register j (DTCCRj) (j = 0 to 23)

Address Refer to **Table 13.7 Control Data Allocation Addresses**

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	RPTINT	CHNE	DAMOD	SAMOD	RPTSEL	MODE
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	MODE	Transfer mode select bit	0: Normal mode 1: Repeat mode	R/W
b1	RPTSEL	Repeat area select bit (1)	0: Transfer destination is the repeat area 1: Transfer source is the repeat area	R/W
b2	SAMOD	Source address control bit (2)	0: Fixed 1: Incremented	R/W
b3	DAMOD	Destination address control bit (2)		R/W
b4	CHNE	Chain transfer enable bit (3)	0: Chain transfers disabled 1: Chain transfers enabled	R/W
b5	RPTINT	Repeat mode interrupt enable bit (1)	0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b6	—	Reserved	Set to 0. The read value is undefined.	R/W
b7	—			

Notes:
1. Enabled when the MODE bit is 1 (repeat mode).
2. Settings of bits SAMOD and DAMOD are invalid for the repeat area.
3. Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).

13.2.4 DTC Block Size Register j (DTBLSj) (j = 0 to 23)

Address Refer to **Table 13.7 Control Data Allocation Addresses**

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	These bits specify the size of the data block to be transferred by one activation.	00h to FFh (1)	R/W

Note:
1. When the DTBLS register is set to 00h, the block size is 256 bytes.
   The value that can be specified in repeat mode is between 01h to FFh (1 to 255 bytes).

13.2.5 DTC Transfer Count Register j (DTCCTj) (j = 0 to 23)

Address Refer to **Table 13.7 Control Data Allocation Addresses**

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	These bits specify the number of times of DTC data transfers.	00h to FFh (1)	R/W

Note:
1. When the DTCCT register is set to 00h, the number of transfer times is 256. The number is decremented by 1 each time the DTC is activated.
   The value that can be specified in repeat mode is between 01h to FFh (1 to 255 times).

13.2.6 DTC Transfer Count Reload Register j (DTRLDj) (j = 0 to 23)

Address Refer to **Table 13.7 Control Data Allocation Addresses**

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	This register value is reloaded to the DTCCT register in repeat mode.	00h to FFh (1)	R/W

Note:
1. Set the initial value of the DTCCT register.
   The value that can be specified in repeat mode is between 01h to FFh (1 to 255 times).

13.2.7 DTC Source Address Register j (DTSARj) (j = 0 to 23)

Address Refer to **Table 13.7 Control Data Allocation Addresses**

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b15 to b0	These bits specify a transfer source address for data transfer.	0000h to FFFFh	R/W

13.2.8 DTC Destination Address Register j (DTDARj) (j = 0 to 23)

Address Refer to **Table 13.7 Control Data Allocation Addresses**

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b15 to b0	These bits specify a transfer destination address for data transfer.	0000h to FFFFh	R/W

13.3 Operation

13.3.1 Overview

When the DTC is activated, control data (1) is read from the DTC control data area to perform data transfers and control data after data transfer is written back to the DTC control data area. Twenty-four sets of control data can be stored in the DTC control data area, which allows 24 types of data transfers to be performed.
There are two transfer modes: normal mode and repeat mode. When the CHNE bit in the DTCCRj (j = 0 to 23) register is set to 1 (chain transfers enabled), multiple control data is read and data transfers are continuously performed by one activation source (chain transfers).
A transfer source address is specified by the 16-bit register DTSARj, and a transfer destination address is specified by the 16-bit register DTDARj. The values in the registers DTSARj and DTDARj are separately fixed or incremented according to the control data on completion of the data transfer.
Note:

1. For details on control data, refer to **13.2.3 DTC Control Register j (DTCCRj) (j = 0 to 23)** to **13.2.8 DTC Destination Address Register j (DTDARj) (j = 0 to 23)**, and **Table 13.7 Control Data Allocation Addresses**.

13.3.2 Activation Sources

The DTC is activated by an interrupt source. Figure 13.2 is a Block Diagram Showing Control of DTC Activation Sources (i = 0 to 6).
The interrupt sources to activate the DTC are selected with the DTCENi (i = 0 to 6) registers.
The DTC sets 0 (activation disabled) to the corresponding bit among bits DTCENi0 to DTCENi7 in the DTCENi register during operation when the setting of data transfer (the first transfer in chain transfers) is either of the following:

- Transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 in normal mode
- Transfer causing the DTCCTj register value to change to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode

If the data transfer setting is not either of the above, the DTC sets 0 to the interrupt source flag corresponding to the activation source during operation.
If multiple activation sources are simultaneously generated, the DTC activation will be performed according to the DTC activation source priority.
If multiple activation sources are simultaneously generated on completion of DTC operation, the next transfer will be performed according to the priority.
DTC activation is not affected by the I flag or interrupt control register, unlike with interrupt request operation. Therefore, even if interrupt requests cannot be acknowledged because interrupts are disabled, DTC activation requests can be acknowledged. The IR bit in the interrupt control register does not change even when an interrupt source to enable DTC activation is generated.

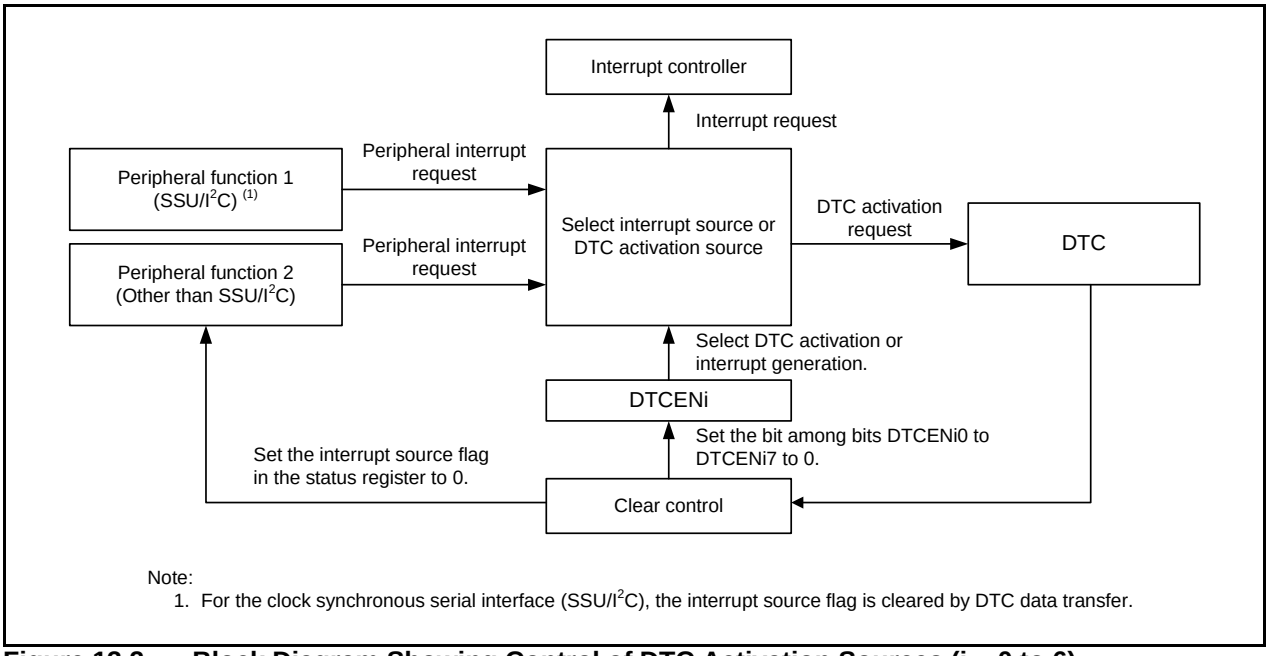


Figure 13.2 Block Diagram Showing Control of DTC Activation Sources (i = 0 to 6)

13.3.3 Control Data Allocation and DTC Vector Table

Control data is allocated in the order: Registers DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj (j = 0 to 23). Table 13.7 lists the Control Data Allocation Addresses.

Table 13.7 Control Data Allocation Addresses

Control Data No.	Address	DTCCRj Register	DTBLSj Register	DTCCTj Register	DTRLDj Register	DTSARj Register (Lower 8 Bits)	DTSARj Register (Higher 8 Bits)	DTDARj Register (Lower 8 Bits)	DTDARj Register (Higher 8 Bits)
Control data 0	06C40h to 06C47h	06C40h	06C41h	06C42h	06C43h	06C44h	06C45h	06C46h	06C47h
Control data 1	06C48h to 06C4Fh	06C48h	06C49h	06C4Ah	06C4Bh	06C4Ch	06C4Dh	06C4Eh	06C4Fh
Control data 2	06C50h to 06C57h	06C50h	06C51h	06C52h	06C53h	06C54h	06C55h	06C56h	06C57h
Control data 3	06C58h to 06C5Fh	06C58h	06C59h	06C5Ah	06C5Bh	06C5Ch	06C5Dh	06C5Eh	06C5Fh
Control data 4	06C60h to 06C67h	06C60h	06C61h	06C62h	06C63h	06C64h	06C65h	06C66h	06C67h
Control data 5	06C68h to 06C6Fh	06C68h	06C69h	06C6Ah	06C6Bh	06C6Ch	06C6Dh	06C6Eh	06C6Fh
Control data 6	06C70h to 06C77h	06C70h	06C71h	06C72h	06C73h	06C74h	06C75h	06C76h	06C77h
Control data 7	06C78h to 06C7Fh	06C78h	06C79h	06C7Ah	06C7Bh	06C7Ch	06C7Dh	06C7Eh	06C7Fh
Control data 8	06C80h to 06C87h	06C80h	06C81h	06C82h	06C83h	06C84h	06C85h	06C86h	06C87h
Control data 9	06C88h to 06C8Fh	06C88h	06C89h	06C8Ah	06C8Bh	06C8Ch	06C8Dh	06C8Eh	06C8Fh
Control data 10	06C90h to 06C97h	06C90h	06C91h	06C92h	06C93h	06C94h	06C95h	06C96h	06C97h
Control data 11	06C98h to 06C9Fh	06C98h	06C99h	06C9Ah	06C9Bh	06C9Ch	06C9Dh	06C9Eh	06C9Fh
Control data 12	06CA0h to 06CA7h	06CA0h	06CA1h	06CA2h	06CA3h	06CA4h	06CA5h	06CA6h	06CA7h
Control data 13	06CA8h to 06CAFh	06CA8h	06CA9h	06CAAh	06CABh	06CACh	06CADh	06CAEh	06CAFh
Control data 14	06CB0h to 06CB7h	06CB0h	06CB1h	06CB2h	06CB3h	06CB4h	06CB5h	06CB6h	06CB7h
Control data 15	06CB8h to 06CBFh	06CB8h	06CB9h	06CBAh	06CBBh	06CBCh	06CBDh	06CBEh	06CBFh
Control data 16	06CC0h to 06CC7h	06CC0h	06CC1h	06CC2h	06CC3h	06CC4h	06CC5h	06CC6h	06CC7h
Control data 17	06CC8h to 06CCFh	06CC8h	06CC9h	06CCAh	06CCBh	06CCCh	06CCDh	06CCEh	06CCFh
Control data 18	06CD0h to 06CD7h	06CD0h	06CD1h	06CD2h	06CD3h	06CD4h	06CD5h	06CD6h	06CD7h
Control data 19	06CD8h to 06CDFh	06CD8h	06CD9h	06CDAh	06CDBh	06CDCh	06CDDh	06CDEh	06CDFh
Control data 20	06CE0h to 06CE7h	06CE0h	06CE1h	06CE2h	06CE3h	06CE4h	06CE5h	06CE6h	06CE7h
Control data 21	06CE8h to 06CEFh	06CE8h	06CE9h	06CEAh	06CEBh	06CECh	06CEDh	06CEEh	06CEFh
Control data 22	06CF0h to 06CF7h	06CF0h	06CF1h	06CF2h	06CF3h	06CF4h	06CF5h	06CF6h	06CF7h
Control data 23	06CF8h to 06CFFh	06CF8h	06CF9h	06CFAh	06CFBh	06CFCh	06CFDh	06CFEh	06CFFh

j = 0 to 23

When the DTC is activated, one control data is selected according to the data read from the vector table which has been assigned to each activation source, and the selected control data is read from the DTC control data area.
Tables 13.8 lists the DTC Activation Sources and DTC Vector AddressesDTC Activation Sources and DTC Vector Addresses. One-byte vector table area is assigned to each activation source and one value from 00000000b to 00010111b (control data numbers in Table 13.7) is stored in each area to select one of the 24 control data sets.
Figures 13.3 to 13.7 show the DTC Internal Operation Flowchart.

Table 13.8 DTC Activation Sources and DTC Vector Addresses

Interrupt Request Source	Interrupt Name	Source No.	DTC Vector Address	Priority
External input	$\overline{\text{INT0}}$	0	06C00h	High
	$\overline{\text{INT1}}$	1	06C01h	
	$\overline{\text{INT2}}$	2	06C02h	
	$\overline{\text{INT3}}$	3	06C03h	
	$\overline{\text{INT4}}$	4	06C04h	
Key input	Key input	8	06C08h	
A/D	A/D conversion	9	06C09h	
UART0_0	UART0_0 reception	10	06C0Ah	
	UART0_0 transmission	11	06C0Bh	
UART0_1	UART0_1 reception	12	06C0Ch	
	UART0_1 transmission	13	06C0Dh	
UART2	UART2 reception	14	06C0Eh	
	UART2 transmission	15	06C0Fh	
SSU_0/I^2C_0	SSU_0/I^2C_0 receive data full	16	06C10h	
	SSU_0/I^2C_0 transmit data empty	17	06C11h	
Voltage detection circuit	Voltage monitor 2	18	06C12h	
	Voltage monitor 1	19	06C13h	
Timer RC_0	Input-capture/compare-match A	22	06C16h	
	Input-capture/compare-match B	23	06C17h	
	Input-capture/compare-match C	24	06C18h	
	Input-capture/compare-match D	25	06C19h	
Timer RD0_0	Input-capture/compare-match A	26	06C1Ah	
	Input-capture/compare-match B	27	06C1Bh	
	Input-capture/compare-match C	28	06C1Ch	
	Input-capture/compare-match D	29	06C1Dh	
Timer RD1_0	Input-capture/compare-match A	30	06C1Eh	
	Input-capture/compare-match B	31	06C1Fh	
	Input-capture/compare-match C	32	06C20h	
	Input-capture/compare-match D	33	06C21h	
SSU_1/I^2C_1	SSU_1/I^2C_1 receive data full	38	06C26h	
	SSU_1/I^2C_1 transmit data empty	39	06C27h	
Timer RE2	Timer RE2	42	06C2Ah	
Timer RJ_0	Timer RJ_0	49	06C31h	
Timer RJ_1	Timer RJ_1	50	06C32h	
Timer RB2_0	Timer RB2_0	51	06C33h	
Flash memory	Flash ready status	52	06C34h	Low

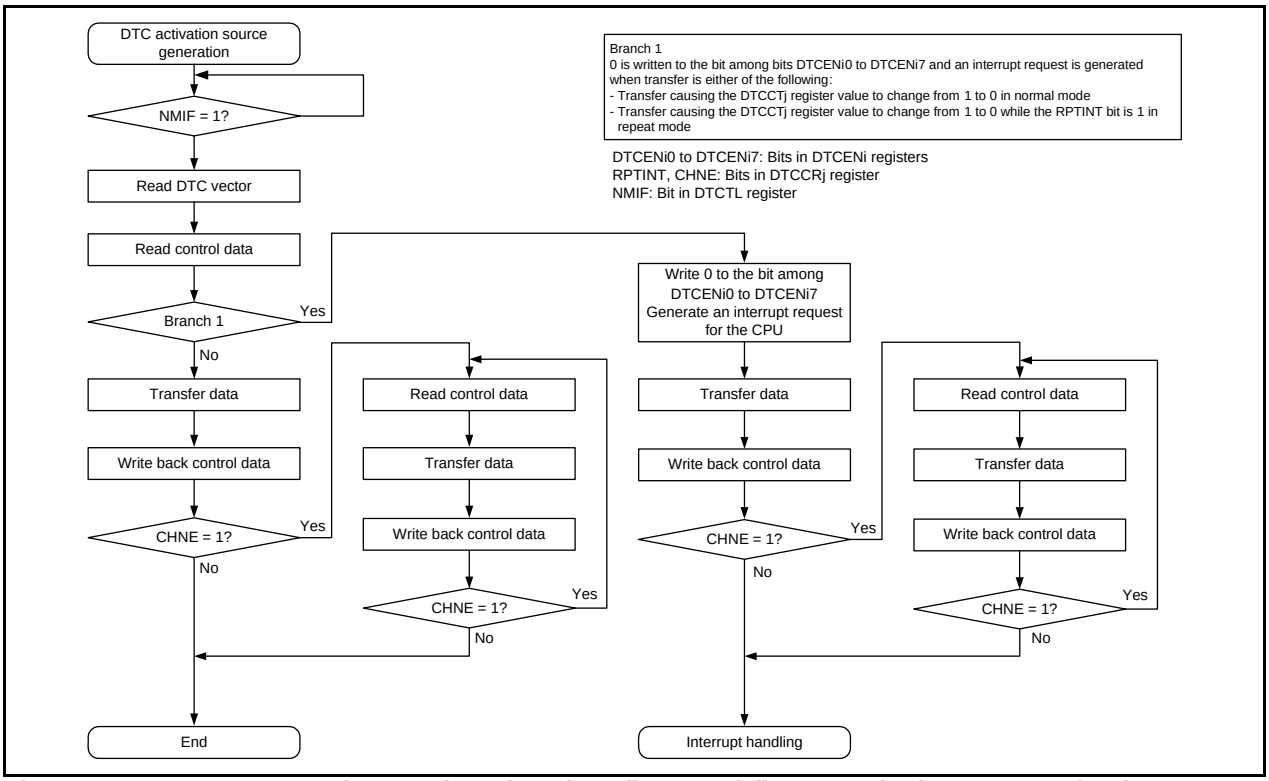


Figure 13.3 DTC Internal Operation Flowchart (i = 0 to 6) (j = 0 to 23) when DTC Activation Source is not Timer RC, Timer RD, Timer RE2, SSU/I²C bus, or Flash Memory Interrupt Source

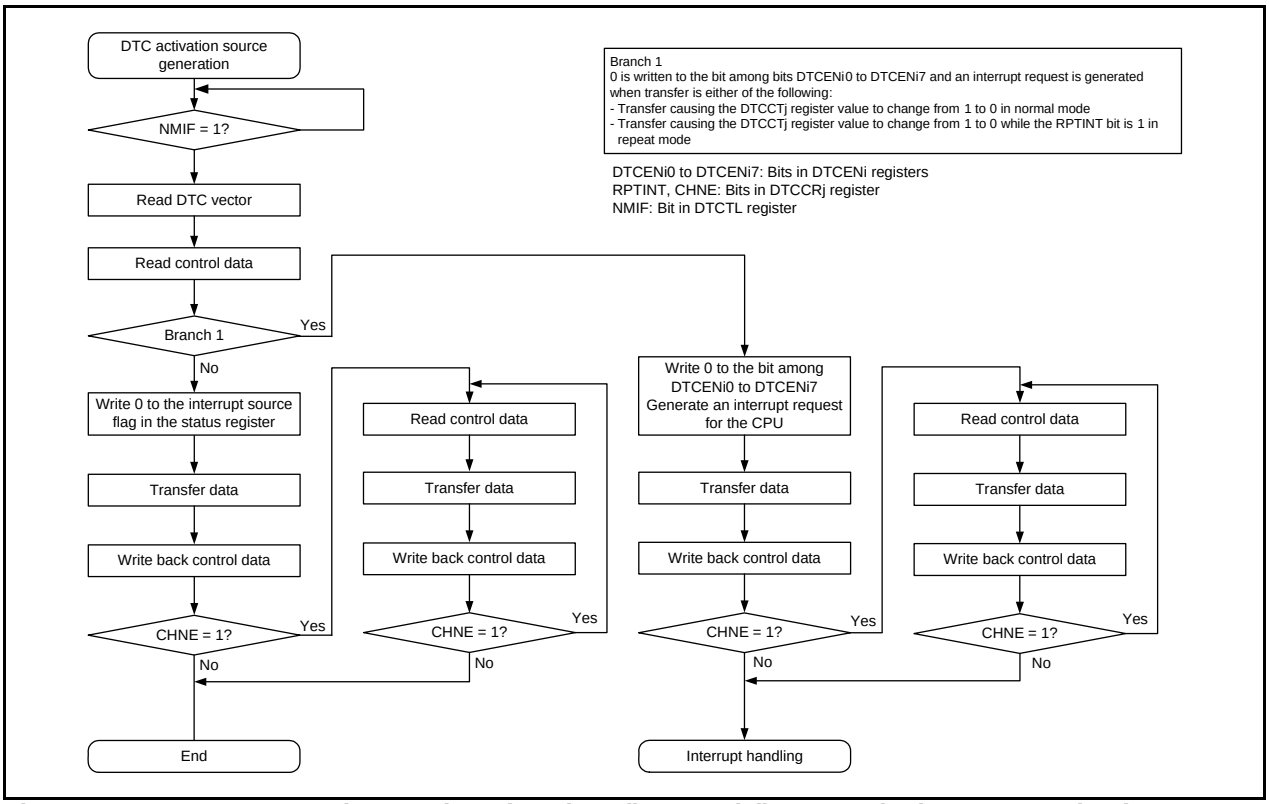
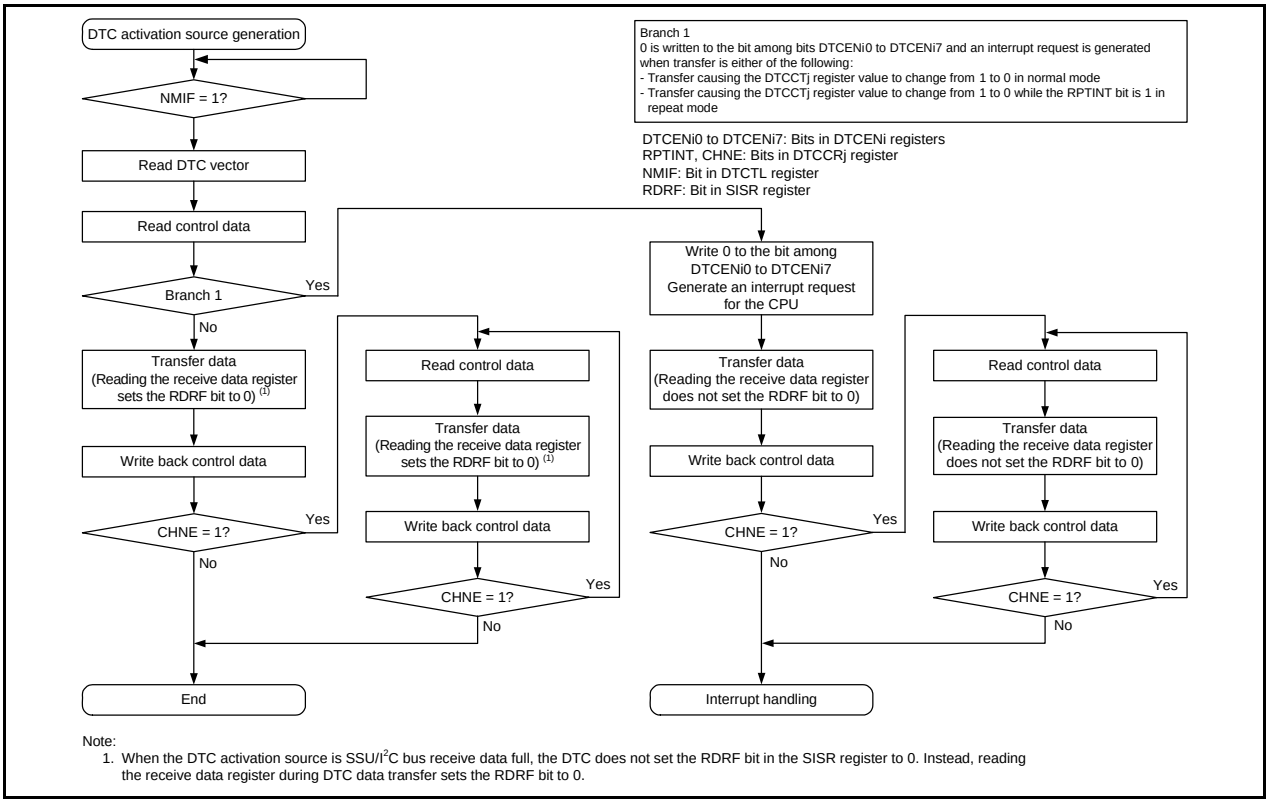
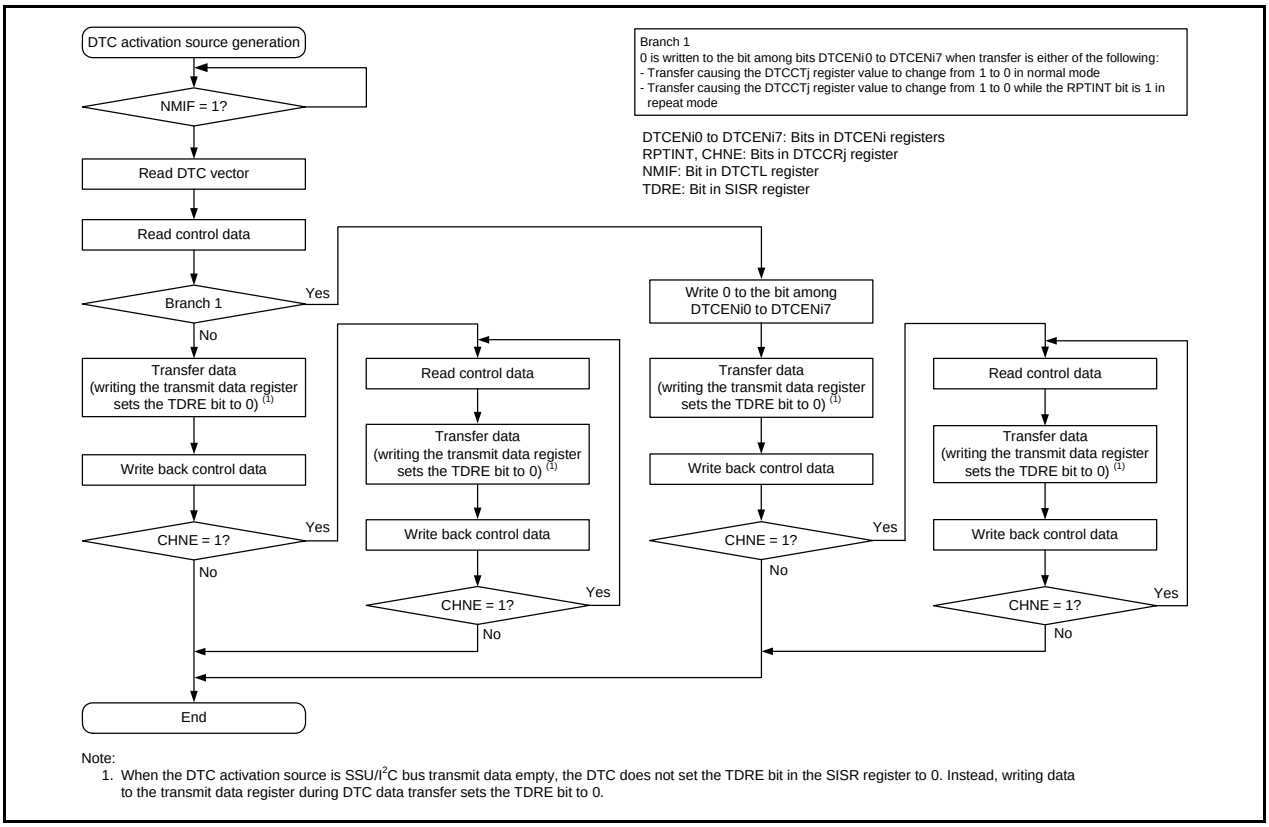


Figure 13.4 DTC Internal Operation Flowchart (i = 0 to 6) (j = 0 to 23) when DTC Activation Source is Timer RC, Timer RD, or Timer RE2 Interrupt Source



Note:
1. When the DTC activation source is SSU/I^{2}C bus receive data full, the DTC does not set the RDRF bit in the SISR register to 0. Instead, reading the receive data register during DTC data transfer sets the RDRF bit to 0.

Figure 13.5 DTC Internal Operation Flowchart when DTC Activation Source is SSU/I^{2}C bus Receive Data Full (i = 0 to 6) (j = 0 to 23)



Note:
1. When the DTC activation source is SSU/I^{2}C bus transmit data empty, the DTC does not set the TDRE bit in the SISR register to 0. Instead, writing data to the transmit data register during DTC data transfer sets the TDRE bit to 0.

Figure 13.6 DTC Internal Operation Flowchart when DTC Activation Source is SSU/I^{2}C bus Transmit Data Empty (i = 0 to 6) (j = 0 to 23)

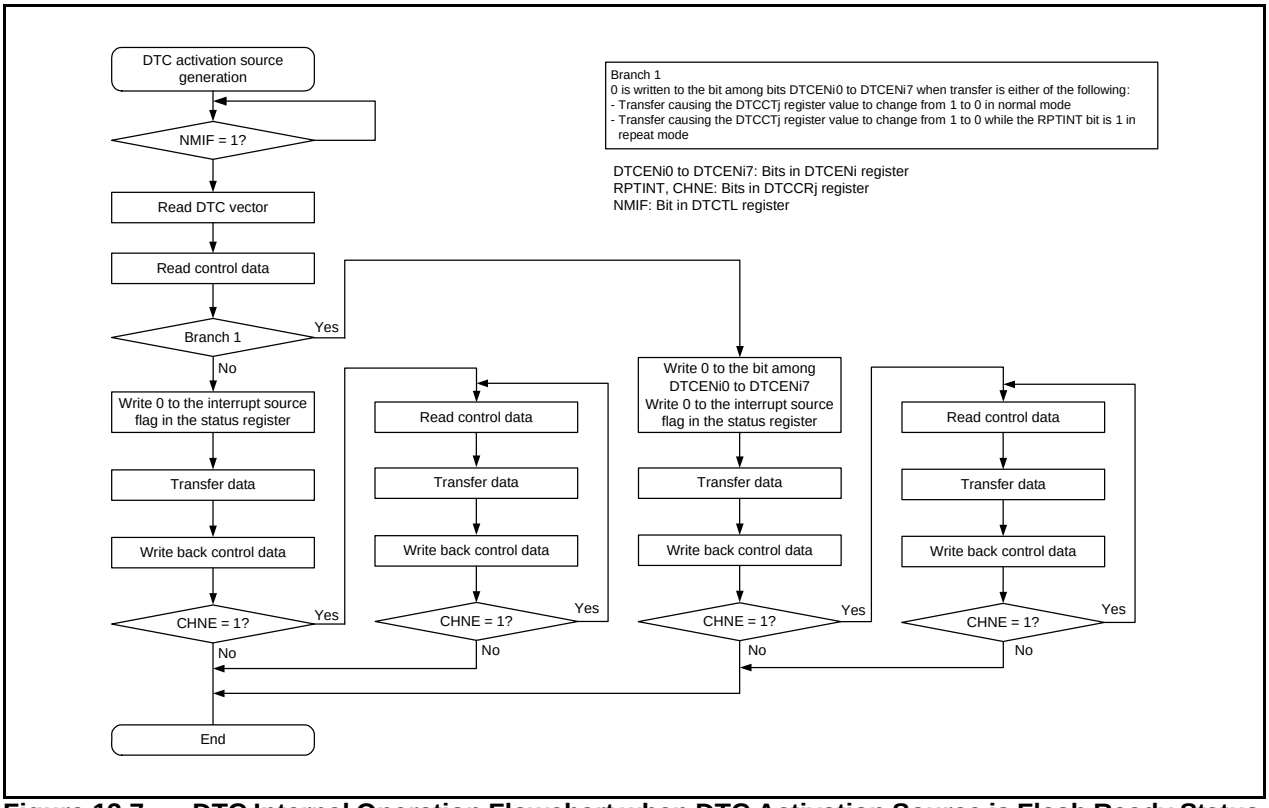


Figure 13.7 DTC Internal Operation Flowchart when DTC Activation Source is Flash Ready Status (i = 0 to 6) (j = 0 to 23)

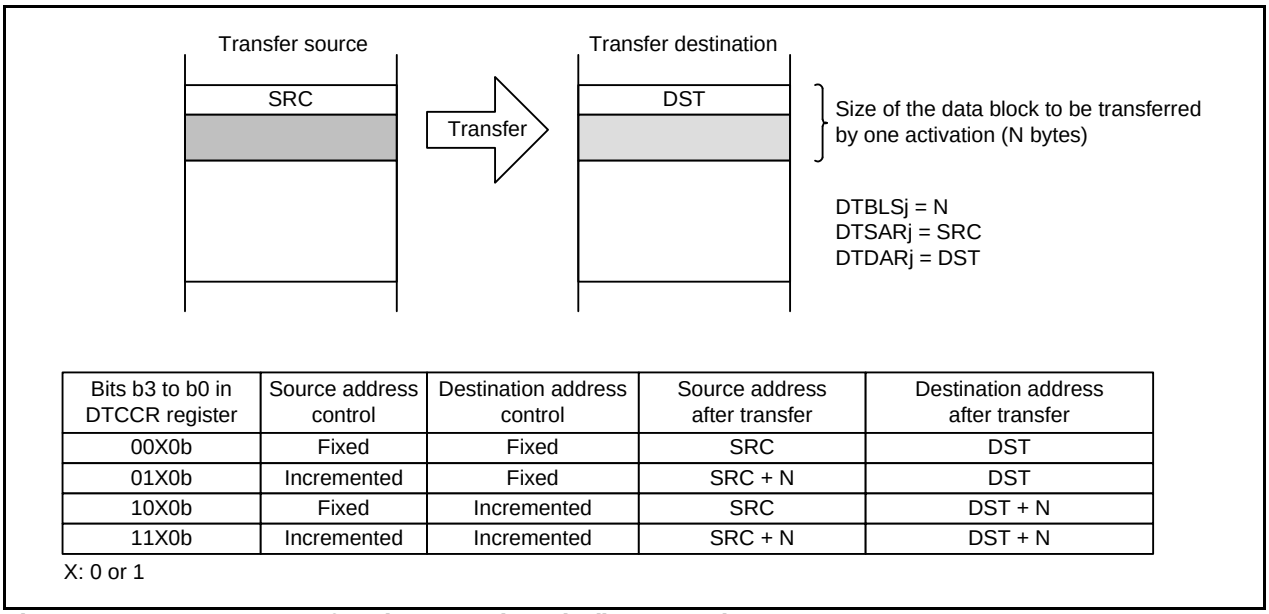
13.3.4 Normal Mode

One to 256 bytes of data are transferred by one activation. The number of transfer times can be 1 to 256. When the data transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 is performed, an interrupt request for the CPU is generated during DTC operation.
Table 13.9 lists Register Functions in Normal Mode.
Figure 13.8 shows Data Transfers in Normal Mode (j = 0 to 23).

Table 13.9 Register Functions in Normal Mode

Register	Symbol	Function
DTC block size register j	DTBLSj	Size of the data block to be transferred by one activation
DTC transfer count register j	DTCCTj	Number of times of data transfers
DTC transfer count reload register j	DTRLDj	Not used
DTC source address register j	DTSARj	Data transfer source address
DTC destination address register j	DTDARj	Data transfer destination address

j = 0 to 23



Bits b3 to b0 in DTCCR register	Source address control	Destination address control	Source address after transfer	Destination address after transfer
00X0b	Fixed	Fixed	SRC	DST
01X0b	Incremented	Fixed	SRC + N	DST
10X0b	Fixed	Incremented	SRC	DST + N
11X0b	Incremented	Incremented	SRC + N	DST + N

X: 0 or 1

Figure 13.8 Data Transfers in Normal Mode (j = 0 to 23)

13.3.5 Repeat Mode

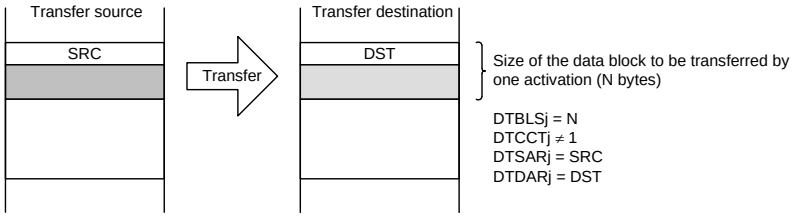
One to 255 bytes of data are transferred by one activation. Either the transfer source or destination should be specified as the repeat area. The number of transfer times can be 1 to 255. On completion of the specified number of transfer times, the DTCCTj (i =0 to 23) register and the address specified for the repeat area are initialized to continue transfers. When the data transfer causing the DTCCTj register value to change to 0 is performed while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled), an interrupt request for the CPU is generated during DTC operation.
The lower 8 bits of the initial value for the repeat area address must be 00h. The size of data to be transferred must be set to 255 bytes or less before the specified number of transfer times is completed.
Table 13.10 lists Register Functions in Repeat Mode. Figure 13.9 shows Data Transfers in Repeat Mode (j = 0 to 23).

Table 13.10 Register Functions in Repeat Mode

Register	Symbol	Function
DTC block size register j	DTBLSj	Size of the data block to be transferred by one activation
DTC transfer count register j	DTCCTj	Number of times of data transfers
DTC transfer count reload register j	DTRLDj	This register value is reloaded to the DTCCT register (Data transfer count is initialized)
DTC source address register j	DTSARj	Data transfer source address
DTC destination address register j	DTDARj	Data transfer destination address

j = 0 to 23

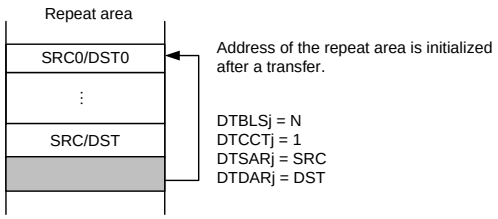
DTCCTj register ≠ 1



Bits b3 to b0 in DTCCR register	Source address control	Destination address control	Source address after transfer	Destination address after transfer
0X11b	Repeat area	Fixed	SRC + N	DST
1X11b	Repeat area	Incremented	SRC + N	DST + N
X001b	Fixed	Repeat area	SRC	DST + N
X101b	Incremented	Repeat area	SRC + N	DST + N

X: 0 or 1

DTCCTj register = 1



Bits b3 to b0 in DTCCR register	Source address control	Destination address control	Source address after transfer	Destination address after transfer
0X11b	Repeat area	Fixed	SRC0	DST
1X11b	Repeat area	Incremented	SRC0	DST + N
X001b	Fixed	Repeat area	SRC	DST0
X101b	Incremented	Repeat area	SRC + N	DST0

SRC0: Initial source address value
DST0: Initial destination address value
X: 0 or 1

Figure 13.9 Data Transfers in Repeat Mode (j = 0 to 23)

13.3.6 Chain Transfers

When the CHNE bit in registers DTCCR0 to DTCCR22 are 1 (chain transfers enabled), multiple data transfers can be continuously performed by one activation source. Figure 13.10 shows a Flow of Chain Transfers.
When the DTC is activated, one control data is selected according to the data read from the DTC vector address corresponding to the activation source, and the selected control data is read from the DTC control data area. When the CHNE bit for the control data is 1, the next control data immediately following the current control data is read and transferred after the current transfer is completed. This operation is repeated until the data transfer with the control data for which the CHNE bit is 0 (chain transfers disabled) is completed.
Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).
Data transfers corresponding to each activation source can be set to either normal mode or repeat mode. For details on data transfer operations, refer to **13.3.4 Normal Mode** and **13.3.5 Repeat Mode**.

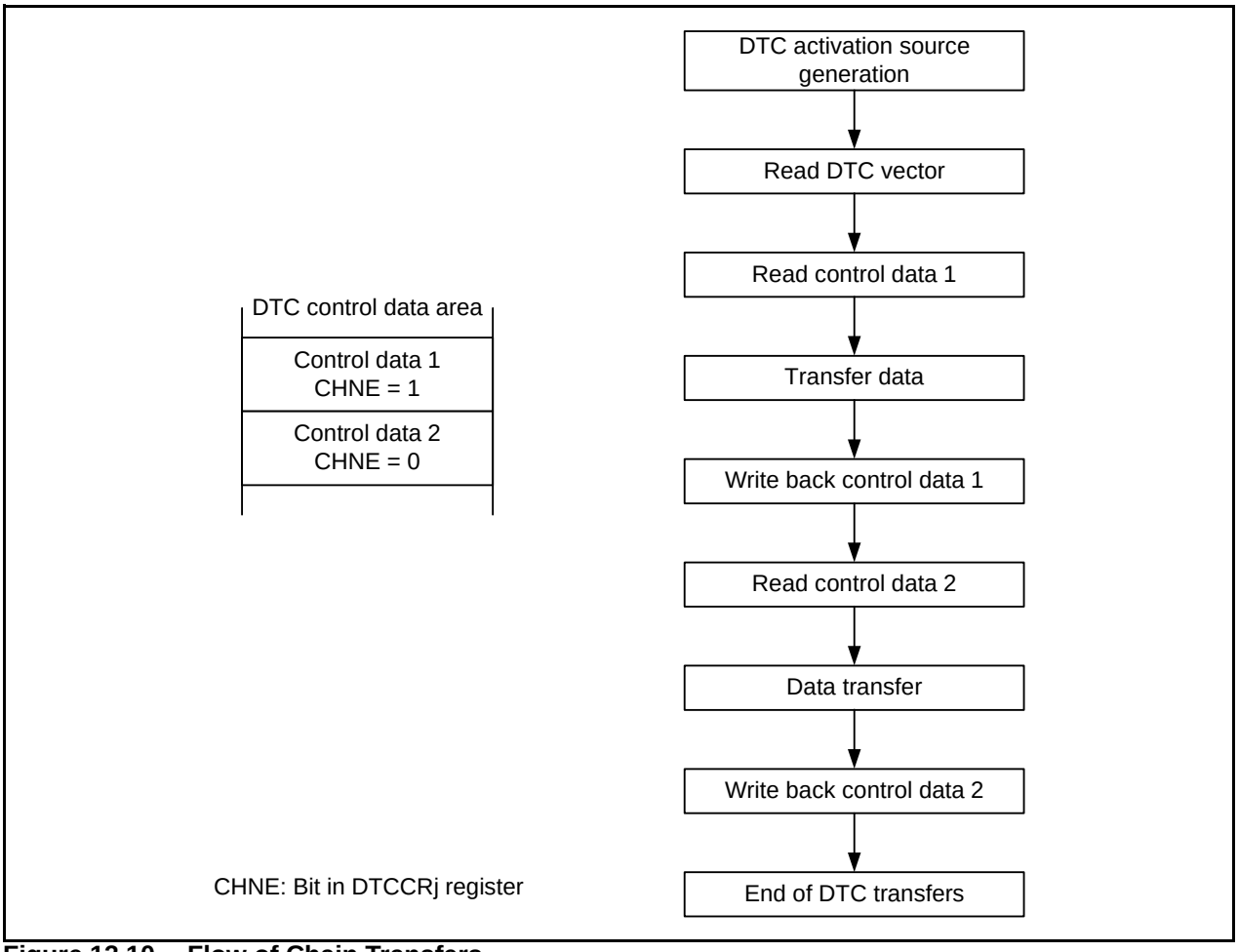


Figure 13.10 Flow of Chain Transfers

13.3.7 Interrupt Sources

When the data transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 is performed in normal mode, and when the data transfer causing the DTCCTj register value to change to 0 is performed while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode, the interrupt request corresponding to the activation source is generated for the CPU during DTC operation. However, no interrupt request is generated for the CPU when the activation source is SSU/I^2C bus transmit data empty or flash ready status.
Interrupt requests for the CPU are affected by the I flag or interrupt control register. In chain transfers, whether the interrupt request is generated or not is determined either by the number of transfer times specified for the first type of the transfer or the RPTINT bit. When an interrupt request is generated for the CPU, the bit among bits DTCENi0 to DTCENi7 in the DTCENi (i = 0 to 6) registers corresponding to the activation source is set to 0 (activation disabled).

13.3.8 Operation Timings

The DTC requires five clock cycles to read control data allocated in the DTC control data area. The number of clock cycles required to write back control data differs depending on the control data settings.
Figure 13.11 shows an Example of DTC Operation Timings and Figure 13.12 shows Example of DTC Operation Timings in Chain Transfers.
Table 13.11 lists the Specifications of Control Data Write-Back Operation.

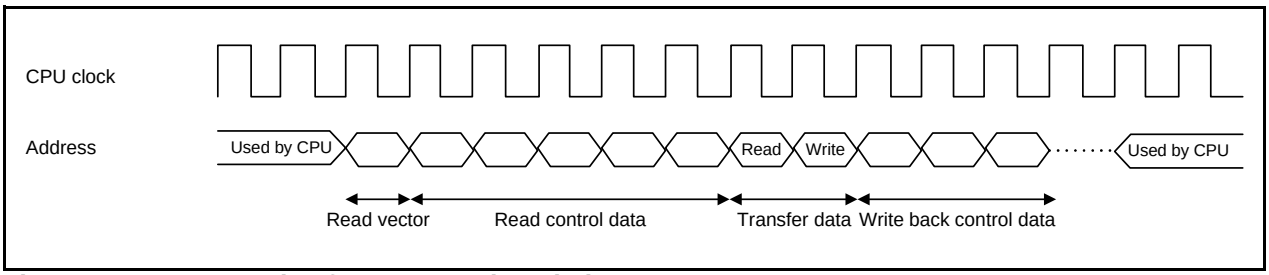


Figure 13.11 Example of DTC Operation Timings

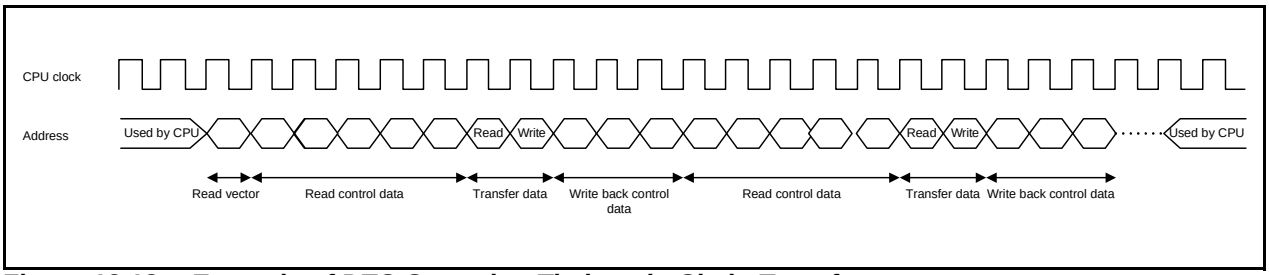


Figure 13.12 Example of DTC Operation Timings in Chain Transfers

Table 13.11 Specifications of Control Data Write-Back Operation

Bits b3 to b0 in DTCCR Register	Operating Mode	Address Control		Control Data to be Written Back				Number of Clock Cycles
		Source	Destination	DTCCTj Register	DTRLDj Register	DTSARj Register	DTDARj Register	
00X0b	Normal mode	Fixed	Fixed	Written back	Written back	Not written back	Not written back	1
01X0b		Incremented	Fixed	Written back	Written back	Written back	Not written back	2
10X0b		Fixed	Incremented	Written back	Written back	Not written back	Written back	2
11X0b		Incremented	Incremented	Written back	Written back	Written back	Written back	3
0X11b	Repeat mode	Repeat area	Fixed	Written back	Written back	Written back	Not written back	2
1X11b			Incremented	Written back	Written back	Written back	Written back	3
X001b		Fixed	Repeat area	Written back	Written back	Not written back	Written back	2
X101b		Incremented		Written back	Written back	Written back	Written back	3

j = 0 to 23
X: 0 or 1

The specifications for writing back control data in chained transfer operations depend on either normal mode or repeat mode as listed in Table 13.2 for each activation source, according to the operating mode set for each activation source.

13.3.9 Number of DTC Execution Cycles

Table 13.12 lists the Operations Following DTC Activation and Required Number of Cycles for each operation.
Table 13.13 lists the Number of Clock Cycles Required for Data Transfers.

Table 13.12 Operations Following DTC Activation and Required Number of Cycles

Vector Read	Control Data		Data Read	Data Write	Internal Operation
	Read	Write-back			
1	5	(Note 1)	(Note 2)	(Note 2)	1

Notes:
1. For the number of clock cycles required for control data write-back, refer to **Table 13.11 Specifications of Control Data Write-Back Operation**.
2. For the number of clock cycles required for data read/write, refer to **Table 13.13 Number of Clock Cycles Required for Data Transfers**.

Data is transferred as described below, when the DTBLSj (j = 0 to 23) register = N,
(1) When N = 2n (even), two-byte transfers are performed n times.
(2) When N = 2n + 1 (odd), two-byte transfers are performed n times followed by one time of one-byte transfer.

Table 13.13 Number of Clock Cycles Required for Data Transfers

Operation	Unit of Transfers	Internal RAM (During DTC Transfers)		Internal ROM (Program ROM)	Internal ROM (Data flash)	SFR (Word Access)		SFR (Byte Access)	SFR (DTC Control Data Area)	
		Even Address	Odd Address			Even Address	Odd Address		Even Address	Odd Address
Data read	1-byte	1		1 (1)	4	3		3	1	
	2-byte	1	2	1 (1)	8	3	6	6	1	2
Data write	1-byte	1		—	—	2		2	1	
	2-byte	1	2	—	—	2	4	4	1	2

Note:
1. This value applies when using page access.
Two cycles are required for 2 bytes and an odd address.
An additional cycle is required when accessing across a page boundary. An additional cycle is also required when using any access other than page access.

The total number of required execution cycles can be obtained by the following formula:

Number of required execution cycles = 1 + Σ [formula A] + 2
Σ: Sum of the cycles for the number of transfer times performed by one activation source ([the number of transfer times for which the CHNE bit is set to 1] + 1)
(1) For N = 2n (even)
Formula A = J + n • SK2 + n • SL2
(2) For N = 2n + 1 (odd)
Formula A = J + n • SK2 + 1 • SK1 + n • SL2 + 1 • SL1
J: Number of cycles required to read control data (5 cycles) + number of cycles required to write back control data

To read data from or write data to the register that to be accessed in 16-bit units, set an even value of 2 or greater to the DTBLSj (j = 0 to 23) register.
The DTC performs accesses in 16-bit units.

13.3.10 DTC Activation Source Acknowledgement and Interrupt Source Flags

13.3.10.1 Interrupt Sources Except for Clock Synchronous Serial Interface (SSU/I2C) and Flash Memory

When the DTC activation source is an interrupt source except for the SSU/I2C or the flash memory, after transfer is started by the interrupt source, the same DTC activation source cannot be acknowledged for 8 to 12 cycles of the CPU clock. If a DTC activation source is generated during DTC operation and acknowledged, the same DTC activation source cannot be acknowledged for 8 to 12 cycles of the CPU clock on completion of the DTC transfer immediately before the DTC is activated by the source.
When a software command is executed on completion of the DTC transfer immediately before the DTC is activated, the same DTC activation source cannot be acknowledged for 16 cycles of the CPU clock.

13.3.10.2 Flash Memory

When the DTC activation source is flash ready status, even if a flash ready status interrupt request is generated, it is not acknowledged as the DTC activation source after the RDYSTI bit in the FST register is set to 1 (flash ready status interrupt requested) and before the DTC sets the RDYSTI bit to 0 (no flash ready status interrupt requested). If a flash ready status interrupt request is generated after the DTC sets the RDYSTI bit to 0, the DTC acknowledges it as the activation source. 8 to 12 cycles of the CPU clock are required after the DTC starts transfer when the RDYSTI bit is set to 1 and before the DTC sets the interrupt request flag to 0.
When a software command is executed on completion of the DTC transfer immediately before the DTC is activated, the RDYSTI bit is set to 0 after 16 cycles of the CPU clock.

13.3.10.3 SSU/I2C bus Receive Data Full

When the DTC activation source is SSU/I2C bus receive data full, read the SIRDR register using a data transfer. The RDRF bit in the SISR register is set to 0 (no data in SIRDR register) by reading the SIRDR register. If an interrupt source for receive data full is subsequently generated, the DTC acknowledges it as the activation source.

13.3.10.4 SSU/I2C bus Transmit Data Empty

When the DTC activation source is SSU/I2C bus transmit data empty, write to the SITDR register using a data transfer. The TDRE bit in the SISR register is set to 0 (data is not transferred from registers SITDR to SIDR) by writing to the SITDR register. If an interrupt source for transmit data empty is subsequently generated, the DTC acknowledges it as the activation source.

13.4 Notes on DTC

13.4.1 DTC Activation Source

- When entering wait mode, complete DTC transfer before the cycle to execute wait mode.
- When entering stop mode, complete DTC transfer before the cycle to execute stop mode.

13.4.2 DTCENi Registers (i = 0 to 6)

- Modify bits DTCENi0 to DTCENi7 only while an interrupt request corresponding to the register is not generated.
- When the interrupt source flag in the status register for the peripheral function is 1, do not modify the corresponding activation source bit among bits DTCENi0 to DTCENi7.
- Do not access the DTCENi registers using DTC transfers.

13.4.3 Peripheral Modules

- Do not set the status register bit for the peripheral function to 0 using a DTC transfer.
- When the DTC activation source is SSU/I^2C receive data full, read the SIRDR register using a DTC transfer. The RDRF bit in the SISR register is set to 0 (no data in the SIRDR register) by reading the SIRDR register. However, the RDRF bit is not set to 0 by reading the SIRDR register when the DTC data transfer setting is either of the following:
  - Transfer causing the DTCCTj (j = 0 to 23) register value to change from 1 to 0 in normal mode
  - Transfer causing the DTCCTj register value to change from 1 to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode.
- When the DTC activation source is SSU/I^2C transmit data empty, write to the SITDR register using a DTC transfer. The TDRE bit in the SISR register is set to 0 (data is not transferred from registers SITDR to SISDR) by writing to the SITDR register.

13.4.4 Interrupt Requests

- When the DTC activation source is either SSU/I^2C transmit data empty or flash ready status, no interrupt request is generated for the CPU in either of the following cases:
  - When the DTC performs a data transfer that causes the DTCCTj register value to change to 0 in normal mode.
  - When the DTC performs a data transfer that causes the DTCCRj register value to change to 0 while the RPTINT bit in the DTCCRj register is 1 in repeat mode.

13.4.5 DTC Activation

- When the DTC is activated, operation may be shifted for one cycle before reading a vector.

14. I/O Ports

Note

Set the assignment of pins using the PMCSEL register before operating the peripheral functions.

14.1 Overview

There are 48 I/O ports P0 to P2, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_7, P6, and P9_4 to P9_7. (The number of the I/O ports that can be used simultaneously is 44. P4_6 and P4_7 can be used as I/O ports if the XIN clock oscillation circuit is not used.)
If the A/D converter is not used, P4_2 can be used as an input-only port.
Table 14.1 lists the I/O Port Overview.

Table 14.1 I/O Port Overview

Ports	I/O	Output Type	I/O Setting	Internal Pull-Up Resister	Drive Capacity Switch	Input Level Switch
P0, P3_0, P3_1, P3_3 to P3_5, P3_7, P6, P9_4 to P9_7 (7)	I/O	CMOS3 state	Set in 1-bit units	Set in 4-bit units (1)	Set in 4-bit units (2)	Set in 8-bit units (3)
P1, P2_0 to P2_3 (7), P2_4 to P2_7	I/O	CMOS3 state	Set in 1-bit units	Set in 4-bit units (1)	Set in 1-bit units (4)	Set in 8-bit units (3)
P4_3	I/O	CMOS3 state	Set in 1-bit units	Set in 1-bit units (1)	Set in 1-bit units (2)	Set in 6-bit units (3)
P4_4, P4_5, P4_6 (5), P4_7 (5)	I/O	CMOS3 state	Set in 1-bit units	Set in 4-bit units (1)	Set in 4-bit units (2)	
P4_2 (6)	I	(No output function)	None	None	None	

Notes:
1. In input mode, whether an internal pull-up resistor is connected or not can be selected by registers PUR0 to PUR2.
2. Whether the drive capacity of the output transistor is set to low or high can be selected by registers DRR0 to DRR2.
3. The input threshold value can be selected from three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC) using registers VLT0 to VLT2.
4. Whether the drive capacity of the output transistor is set to low or high can be selected by registers P1DRR and P2DRR.
5. When the XIN clock oscillation circuit is not used, these ports can be used as I/O ports.
6. When the A/D converter is not used, this port can be used as an input-only port.
7. When the pin assignment is set to communication function priority using the PMCSEL register, the functions of P2_0 to P2_3 are changed to those of P9_4 to P9_7.
8. For details on the PMCSEL register, refer to **29.3.1 Pin Assignment Select Register (PMCSEL)**.

14.2 I/O Port Functions

The PDi_j (i = 0 to 4, 6, or 9, j = 0 to 7) bit in the PDi register controls the I/O of ports P0 to P2, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_7, P6, and P9_4 to P9_7. The PORTi register consists of a port latch to hold output data and a circuit to read the pin states.
Figures 14.1 to 14.7 show the I/O Port Configuration and Table 14.2 lists the I/O Port Functions.

Table 14.2 I/O Port Functions

Operation when Accessing PORTi Register	Value of PDi_j Bit in PDi Register	
	When PDi_j Bit is Set to 0 (Input Mode)	When PDi_j Bit is Set to 1 (Output Mode)
Read	Read the pin input level.	Read the port latch.
Write	Write to the port latch.	Write to the port latch. The value written to the port latch is output from the pin.

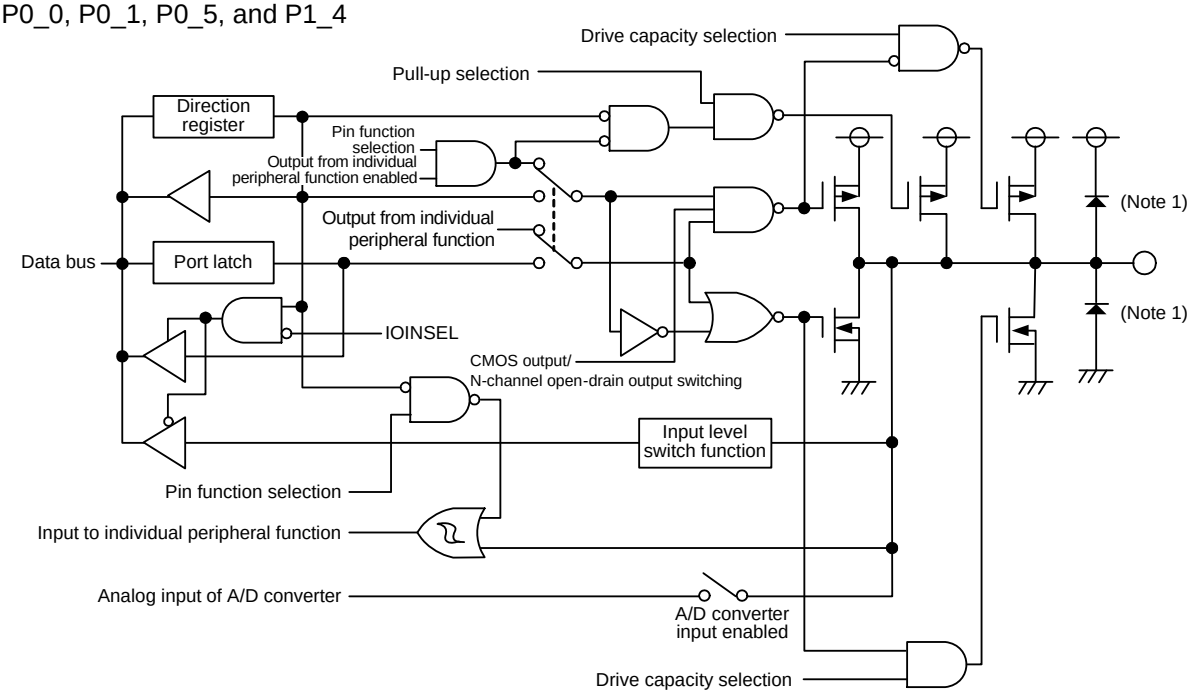
i = 0 to 4, 6, 9, j = 0 to 7

1. Nothing is assigned to bits PD4_0 to PD4_2. Bits PD3_2, PD3_6, and PD9_0 to PD9_3 are reserved.
2. Nothing is assigned to bits P4_0 and P4_1. Bits P3_2, P3_6, and P9_0 to P9_3 are reserved.
3. When the PORT3 register is read, bits P3_2 and P3_6 are set to 0.
4. When the PORT4 register is read, bits P4_0 and P4_1 are set to 0.
5. When the PORT9 register is read, bits P9_0 to P9_3 are set to 0.
6. When using bits P4_6 and P4_7 with XIN and XOUT, the pin input levels cannot be read by reading the PORT4 register. Bits P4_6 and P4_7 are set to 1. Similarly, the values of bits P4_6 and P4_7 will not be output from the pins even if bits PD4_6 and PD4_7 are set to 1 (output mode).

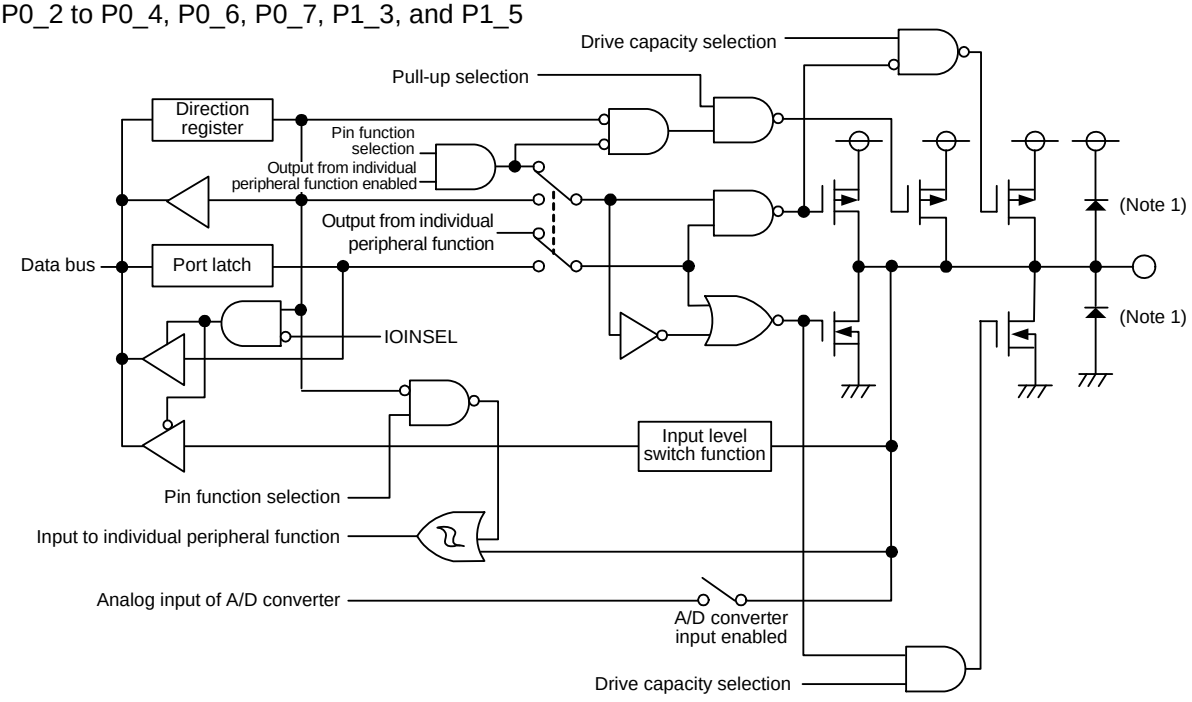
14.3 Pins Other than I/O Ports

Figure 14.8 shows the Pin Configuration.

P0_0, P0_1, P0_5, and P1_4



P0_2 to P0_4, P0_6, P0_7, P1_3, and P1_5



Note:
1. ⟵ symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

IOINSEL: Bit in PINSR register

Figure 14.1 I/O Port Configuration (1)

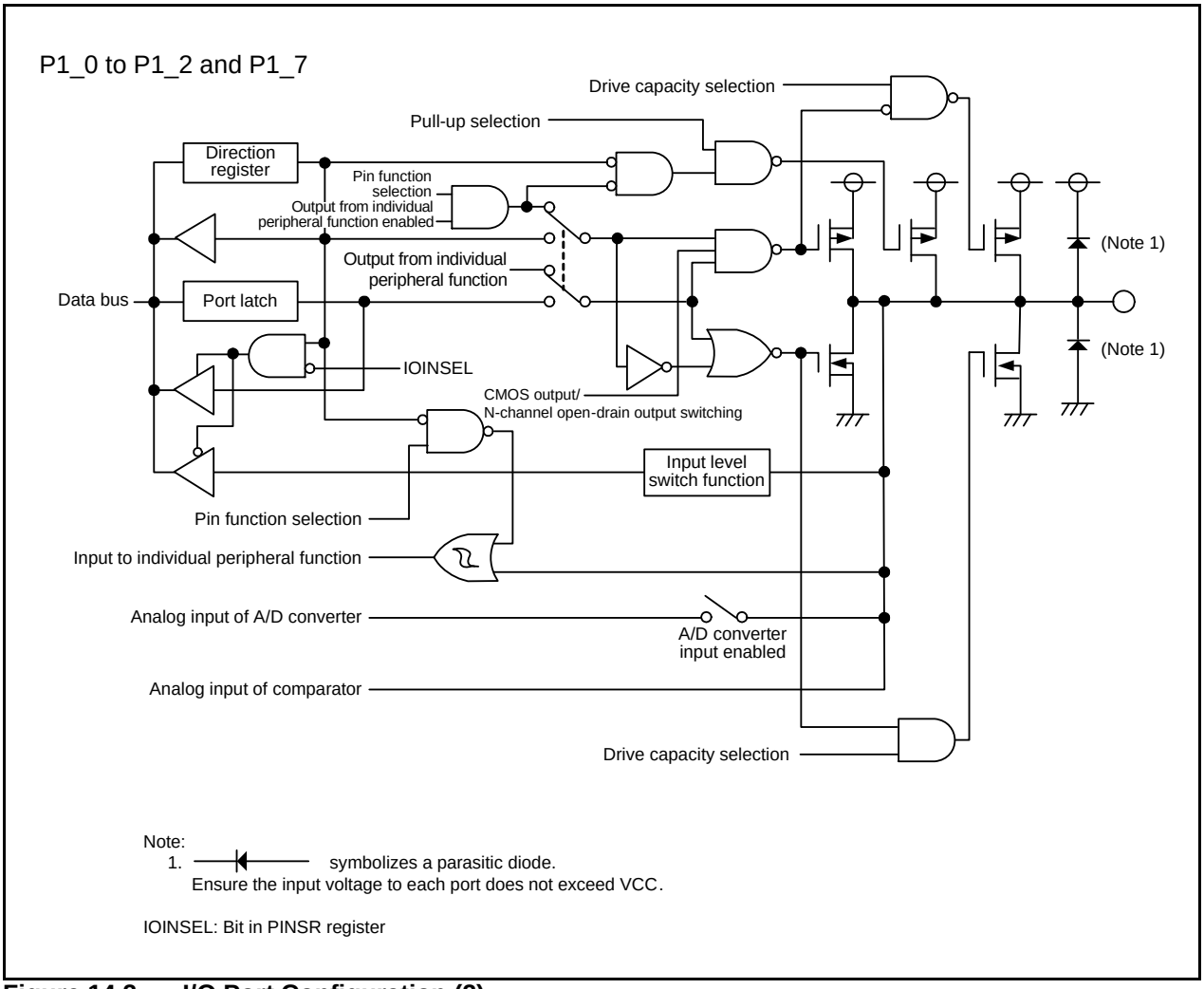


Figure 14.2 I/O Port Configuration (2)

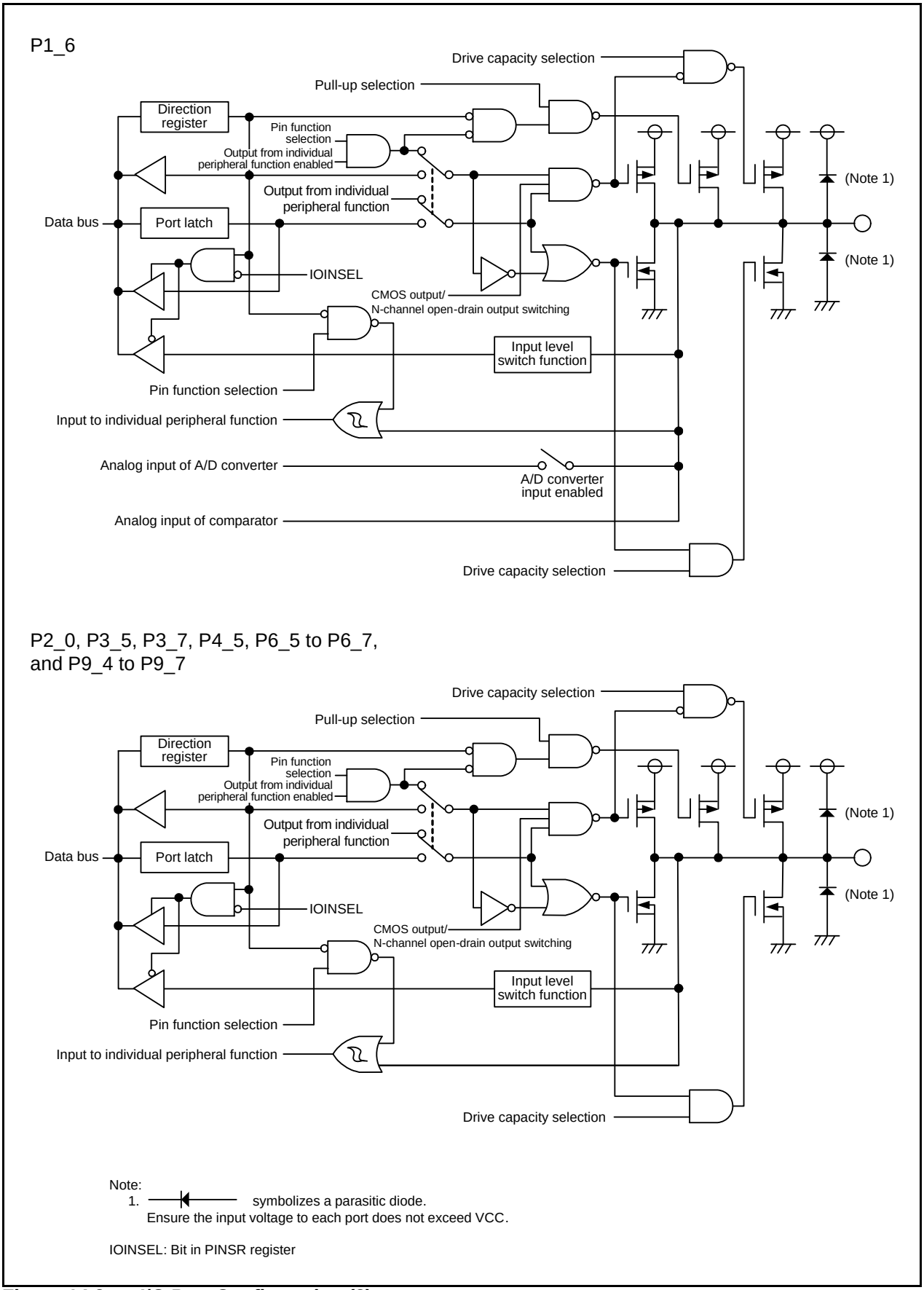
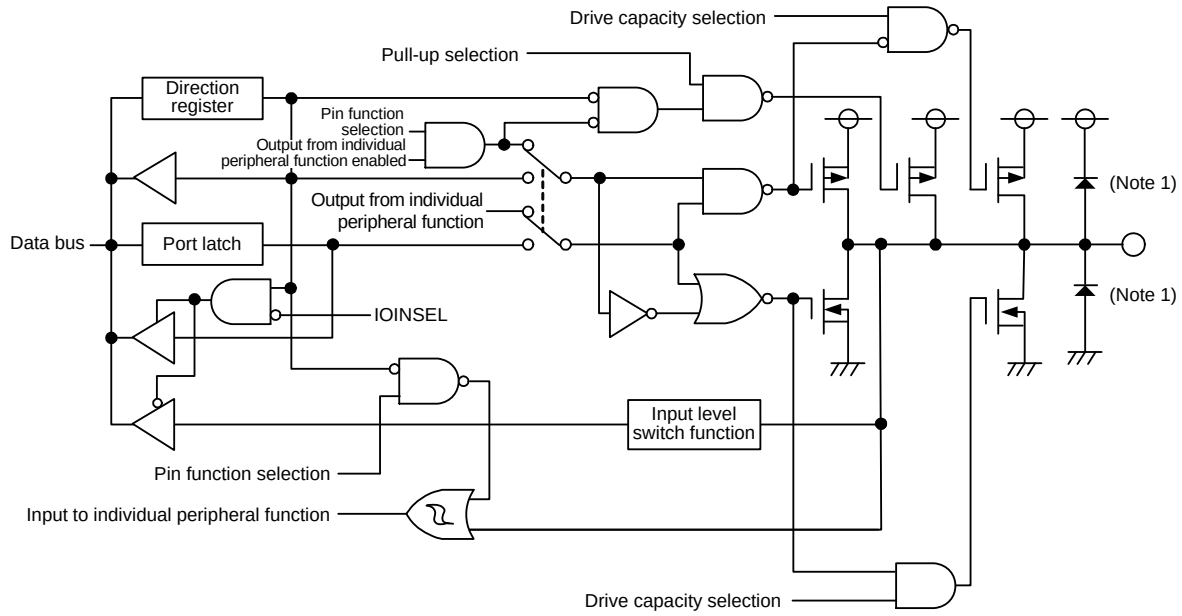
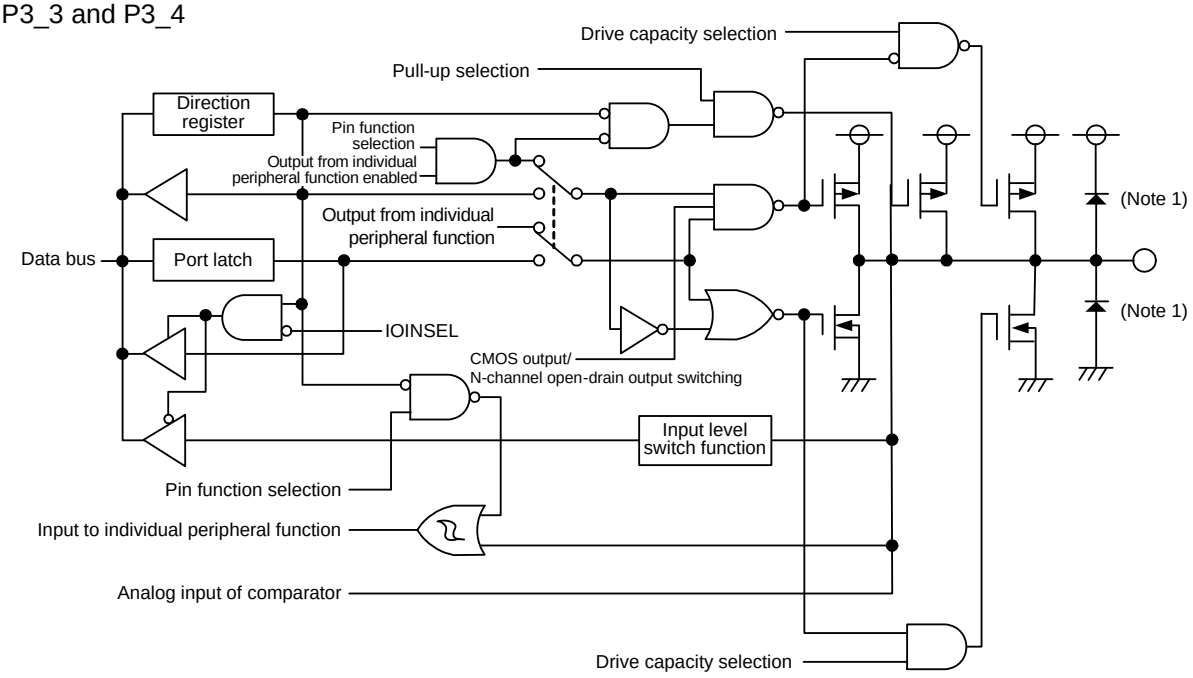


Figure 14.3 I/O Port Configuration (3)

P2_1 to P2_7, P3_0, P3_1, P6_2, and P6_4



P3_3 and P3_4



Note:
1. ⟵ symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

IOINSEL: Bit in PINSR register

Figure 14.4 I/O Port Configuration (4)

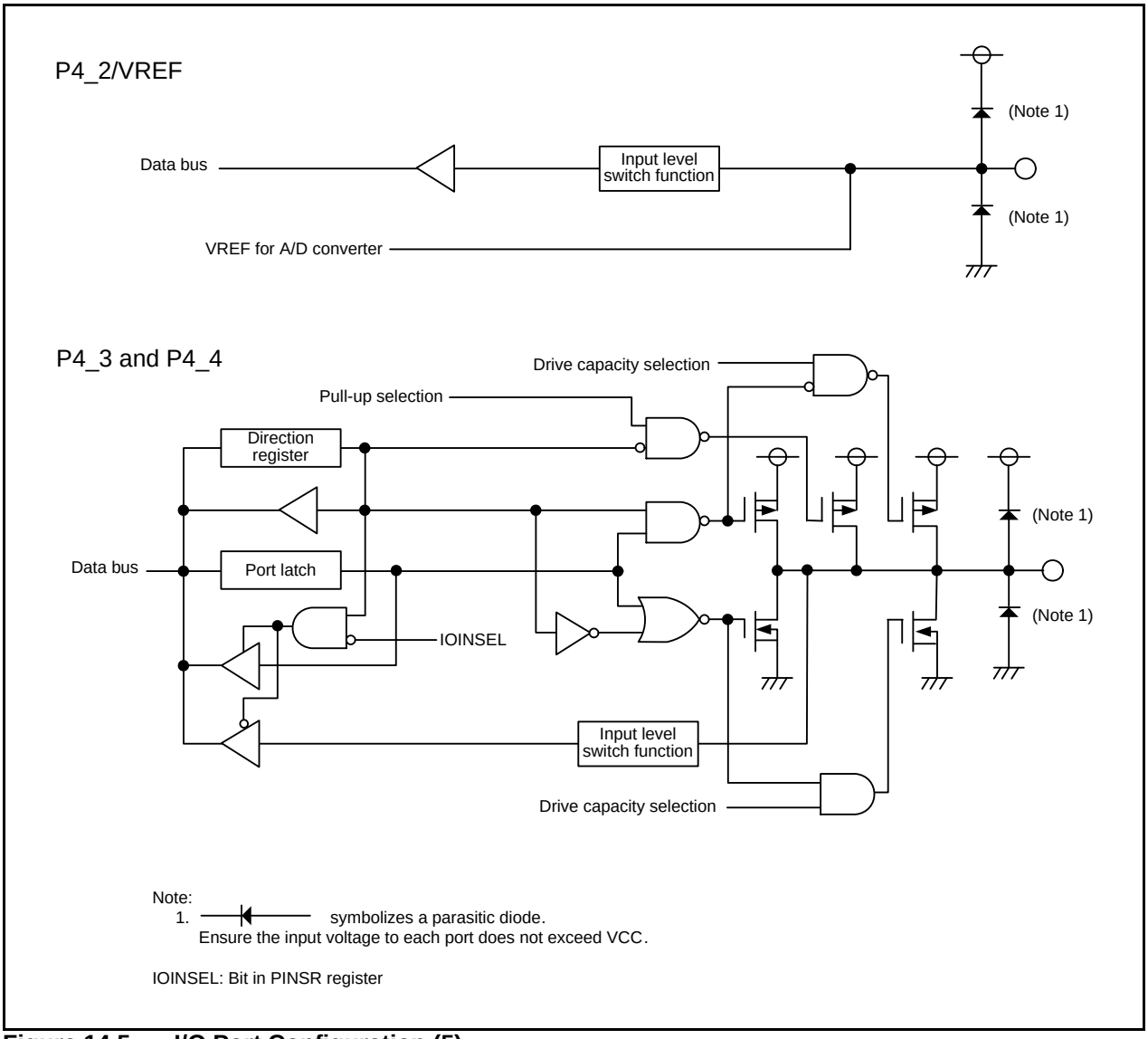
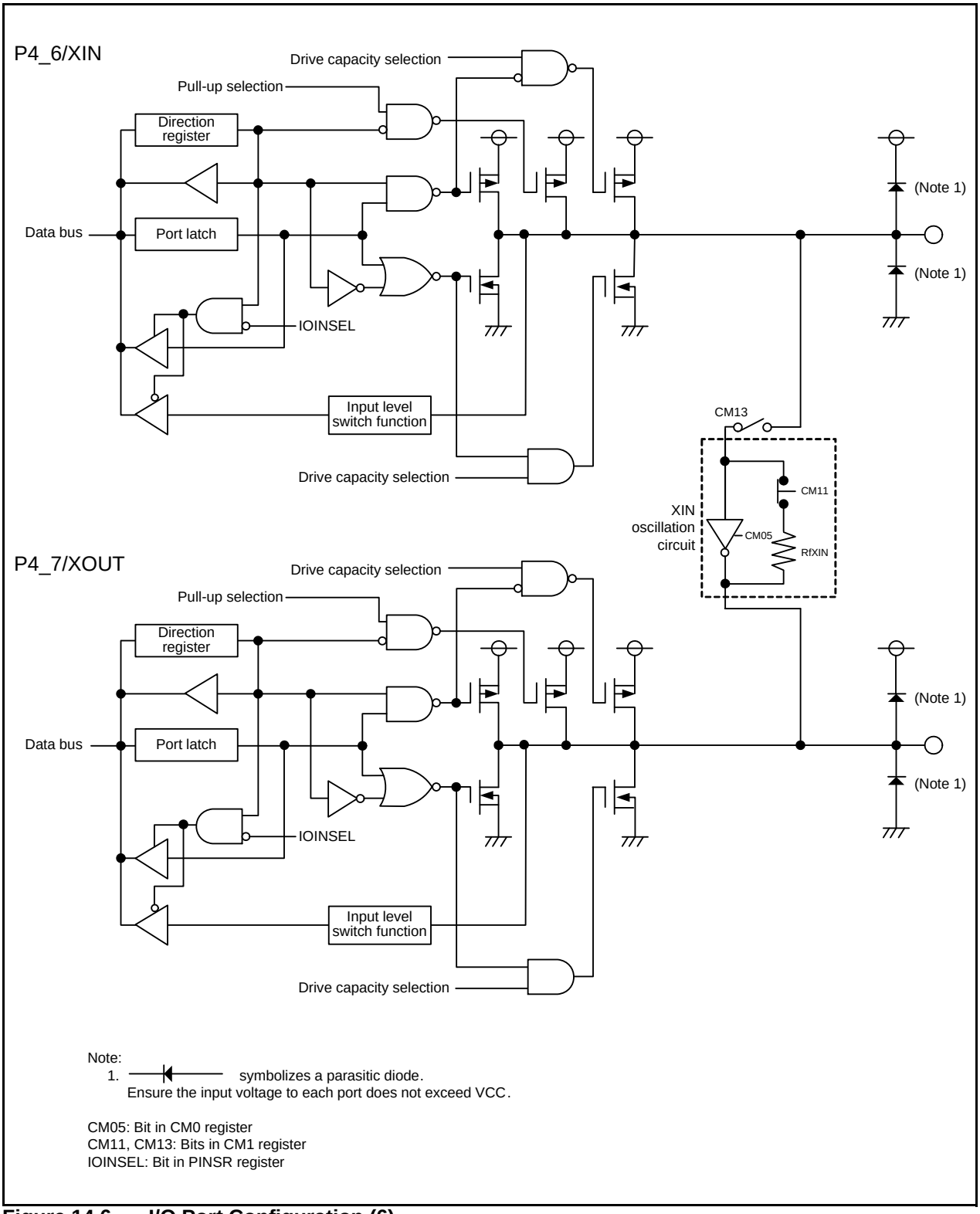


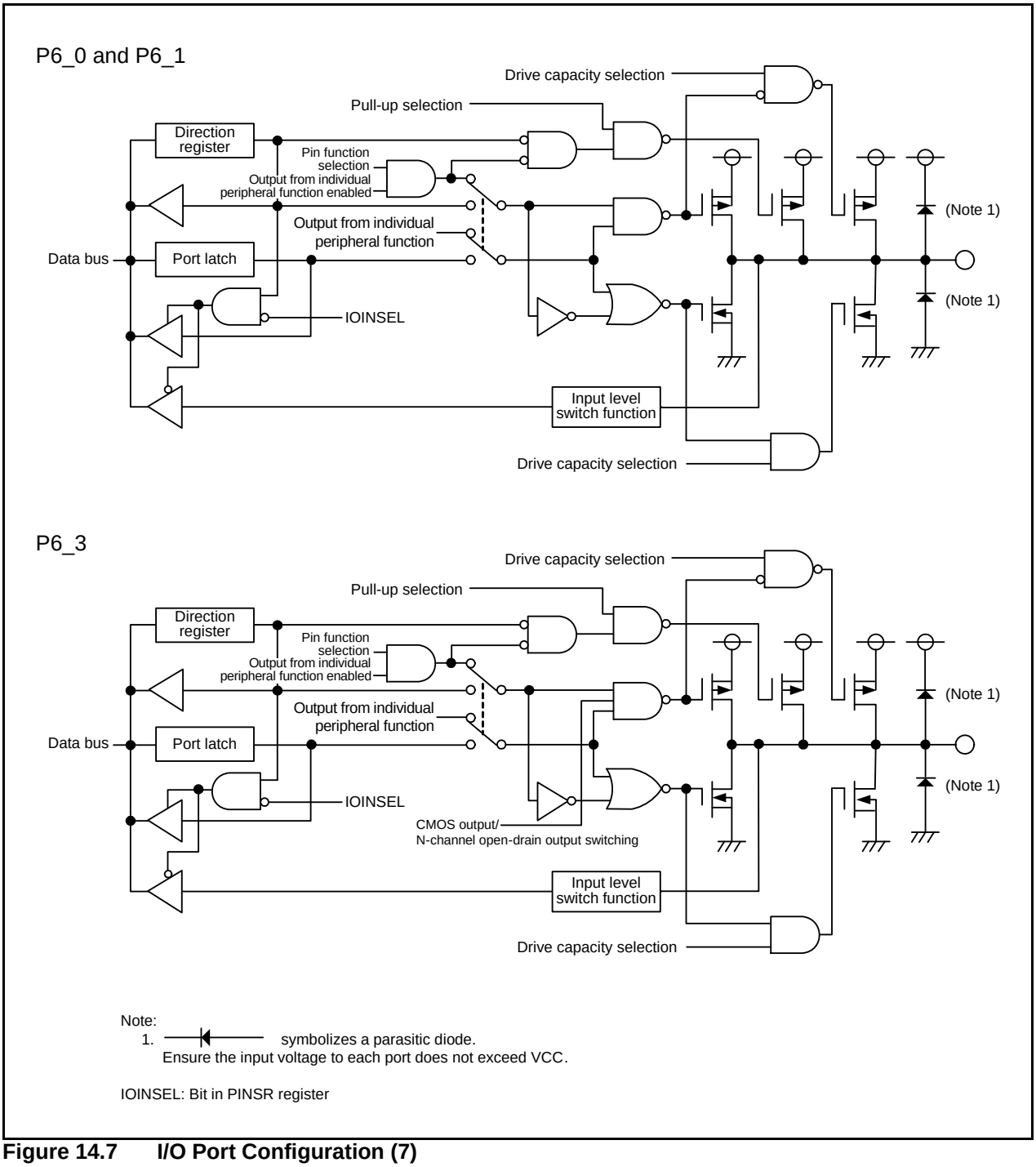
Figure 14.5 I/O Port Configuration (5)



Note:
1. ⟵| symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

CM05: Bit in CM0 register
CM11, CM13: Bits in CM1 register
IOINSEL: Bit in PINSR register

Figure 14.6 I/O Port Configuration (6)



Note:
1. ⟵ symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

IOINSEL: Bit in PINSR register

Figure 14.7 I/O Port Configuration (7)

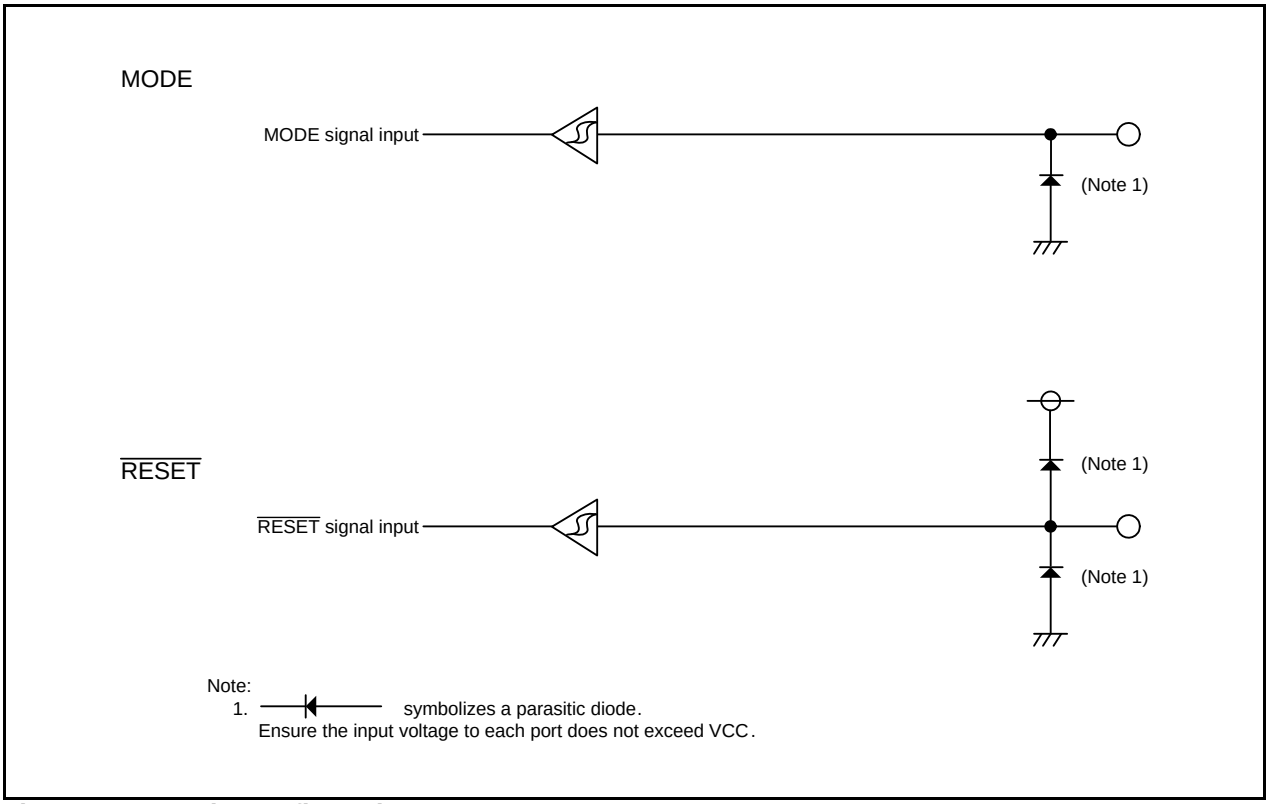


Figure 14.8 Pin Configuration

14.4 I/O of Peripheral Functions

14.4.1 Peripheral Function I/O and PDi Bit (i = 0 to 4, 6, or 9)

The I/O ports function as I/O for the peripheral functions. Peripheral function I/O may be affected by the PDi bit of the I/O port sharing the pins. Table 14.3 lists the PDi_j Bit (i = 0 to 4, 6, or 9, j = 0 to 7) Settings when Functioning as Peripheral Function I/O. Refer to the description of each function for information on how to set up the peripheral functions.

Table 14.3 PDi_j Bit (i = 0 to 4, 6, or 9, j = 0 to 7) Settings when Functioning as Peripheral Function I/O

Peripheral Function I/O		PDi_j Bit Settings for Ports Sharing Pin
Input		Set to 0 (input mode).
Output	D/A converter	Set to 0 (input mode).
	Other	Can be set to either 0 or 1 (output regardless of the port setting).

14.5 Registers

Table 14.4 lists the Register Configuration for I/O Ports.

Table 14.4 Register Configuration for I/O Ports

Register Name	Symbol	After Reset	Address	Access Size
Timer RJ_0 Pin Select Register	TRJ_0SR	00h	002A0h	8
Timer RJ_1 Pin Select Register	TRJ_1SR	00h	002A1h	8
Timer RB2 Pin Select Register	TRBSR	00h	002A4h	8
Timer RCCLK Pin Select Register	TRCCLKSR	00h	002A5h	8
Timer RC_0 Pin Select Register 0	TRC_0SR0	00h	002A6h	8
Timer RC_0 Pin Select Register 1	TRC_0SR1	00h	002A7h	8
Timer RD_0 Pin Select Register 0	TRD_0SR0	00h	002A9h	8
Timer RD_0 Pin Select Register 1	TRD_0SR1	00h	002AAh	8
Timer Pin Select Register	TIMSR	00h	002ADh	8
UART0_0 Pin Select Register	U_0SR	00h	002AEh	8
UART0_1 Pin Select Register	U_1SR	00h	002AFh	8
UART2 Pin Select Register 0	U2SR0	00h	002B2h	8
UART2 Pin Select Register 1	U2SR1	00h	002B3h	8
SSU/IIC_0 Pin Select Register	SSUIIC_0SR	00h	002B4h	8
INT Interrupt Input Pin Select Register 0	INTSR0	00h	002B6h	8
I/O Function Pin Select Register	PINSR	00h	002B9h	8
Pull-Up Control Register 0	PUR0	00h	002C0h	8
Pull-Up Control Register 1	PUR1	00h	002C1h	8
Pull-Up Control Register 2	PUR2	00h	002C2h	8
Port P1 Drive Capacity Control Register	P1DRR	00h	002C8h	8
Port P2 Drive Capacity Control Register	P2DRR	00h	002C9h	8
Drive Capacity Control Register 0	DRR0	00h	002CCh	8
Drive Capacity Control Register 1	DRR1	00h	002CDh	8
Drive Capacity Control Register 2	DRR2	00h	002CEh	8
Input Threshold Control Register 0	VLT0	00h	002D0h	8
Input Threshold Control Register 1	VLT1	00h	002D1h	8
Input Threshold Control Register 2	VLT2	00h	002D2h	8
Port P0 Register	PORT0	XXh	002E0h	8
Port P1 Register	PORT1	XXh	002E1h	8
Port P0 Direction Register	PD0	00h	002E2h	8
Port P1 Direction Register	PD1	00h	002E3h	8
Port P2 Register	PORT2	XXh	002E4h	8
Port P3 Register	PORT3	XXh	002E5h	8
Port P2 Direction Register	PD2	00h	002E6h	8
Port P3 Direction Register	PD3	00h	002E7h	8
Port P4 Register	PORT4	XXh	002E8h	8
Port P4 Direction Register	PD4	00h	002EAh	8
Port P6 Register	PORT6	XXh	002ECh	8
Port P6 Direction Register	PD6	00h	002EEh	8
Port P9 Register	PORT9	XXh	002F1h	8
Port P9 Direction Register	PD9	00h	002F3h	8

14.5.1 Timer RJ_0 Pin Select Register (TRJ_0SR)

Address 002A0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	TRJO_0SEL1	TRJO_0SEL0	—	TRJIO_0SEL1	TRJIO_0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRJIO_0SEL0	TRJIO_0 pin select bits	b1 b0 0 0: TRJIO_0 pin not used 0 1: P1_7 assigned 1 0: P1_5 assigned 1 1: Do not set.	R/W
b1	TRJIO_0SEL1			R/W
b2	—	Reserved	Set to 0.	R/W
b3	TRJO_0SEL0	TRJO_0 pin select bits	b4 b3 0 0: P3_7 assigned 0 1: P3_0 assigned Other than the above: Do not set.	R/W
b4	TRJO_0SEL1			R/W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	—			
b7	—			

The TRJ_0SR register is used to select which pin is assigned to timer RJ_0 I/O. To use the I/O pin for timer RJ_0, set this register.
Set the TRJ_0SR register before setting the registers associated with timer RJ_0. Also, do not change the set value of this register during timer RJ_0 operation.

14.5.2 Timer RJ_1 Pin Select Register (TRJ_1SR)

Address 002A1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	TRJO_1SEL	—	TRJIO_1SEL1	TRJIO_1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRJIO_1SEL0	TRJIO_1 pin select bits	b1 b0 0 0: TRJIO_1 pin not used 0 1: P6_4 assigned 1 0: P0_2 assigned 1 1: Do not set.	R/W
b1	TRJIO_1SEL1			R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	TRJO_1SEL	TRJO_1 pin select bit	0: P6_3 assigned 1: P0_1 assigned	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

The TRJ_1SR register is used to select which pin is assigned to timer RJ_1 I/O. To use the I/O pin for timer RJ_1, set this register.
Set the TRJ_1SR register before setting the registers associated with timer RJ_1. Also, do not change the set value of this register during timer RJ_1 operation.

14.5.3 Timer RB2 Pin Select Register (TRBSR)

Address 002A4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	TRBO_0SEL1	TRBO_0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRBO_0SEL0	TRBO_0 pin select bits	b1 b0 0 0: P1_3 assigned 0 1: P3_1 assigned 1 0: Do not set. 1 1: TRBO pin not used	R/W
b1	TRBO_0SEL1			R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

The TRBSR register is used to select which pin is assigned to timer RB2_0 I/O. To use the I/O pin for timer RB2_0, set this register.

Set bits TRBO_0SEL0 and TRBO_0SEL1 before setting timer RB2 associated registers (1). Also, do not change the set values of bits TRBO_0SEL0 and TRBO_0SEL1 during timer RB2_0 operation.

Note:

1. Registers associated with timer RB2: TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBSC, and TRBPR

14.5.4 Timer RCCLK Pin Select Register (TRCCLKSR)

Address 002A5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TRCCLK_0SEL2	TRCCLK_0SEL1	TRCCLK_0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCCLK_0SEL0	TRCCLK_0 pin select bits	b2 b1 b0 0 0 0: TRCCLK_0 pin not used 0 0 1: P1_4 assigned 0 1 0: P3_3 assigned 0 1 1: P3_7 assigned Other than the above: Do not set.	R/W
b1	TRCCLK_0SEL1			R/W
b2	TRCCLK_0SEL2			R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—	Reserved	Set to 0.	R/W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	—			
b7	—			

The TRCCLKSR register is used to select which pin is assigned to timer RC_0 I/O. To use the I/O pin for timer RC_0, set this register.
Set bits TRCCLK_0SEL0 to TRCCLK_0SEL2 before setting the registers associated with timer RC_0. Also, do not change the set values of bits TRCCLK_0SEL0 to TRCCLK_0SEL2 during timer RC_0 operation.

14.5.5 Timer RC_0 Pin Select Register 0 (TRC_0SR0)

Address 002A6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRCIOB_0SEL2	TRCIOB_0SEL1	TRCIOB_0SEL0	—	TRCIOA_0SEL2	TRCIOA_0SEL1	TRCIOA_0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOA_0SEL0	TRCIOA_0/TRCTRG_0 pin select bits	b2 b1 b0 0 0 0: TRCIOA_0/TRCTRG_0 pin not used 0 0 1: P1_1 assigned 0 1 0: P0_0 assigned 0 1 1: P0_1 assigned 1 0 0: P0_2 assigned Other than the above: Do not set.	R/W
b1	TRCIOA_0SEL1			R/W
b2	TRCIOA_0SEL2			R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	TRCIOB_0SEL0	TRCIOB_0 pin select bits	b6 b5 b4 0 0 0: TRCIOB_0 pin not used 0 0 1: P1_2 assigned 0 1 0: P0_3 assigned 0 1 1: P0_4 assigned 1 0 0: P0_5 assigned 1 0 1: P2_0 assigned 1 1 0: P6_5 assigned 1 1 1: Do not set.	R/W
b5	TRCIOB_0SEL1			R/W
b6	TRCIOB_0SEL2			R/W
b7	—	Nothing is assigned. The write value must be 0. The read value is 0.		—

The TRC_0SR0 register is used to select which pin is assigned to timer RC_0 I/O. To use the I/O pin for timer RC_0, set this register.
Set the TRC_0SR0 register before setting the registers associated with timer RC_0. Also, do not change the set value of this register during timer RC_0 operation.

14.5.6 Timer RC_0 Pin Select Register 1 (TRC_0SR1)

Address 002A7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRCIOD_0SEL2	TRCIOD_0SEL1	TRCIOD_0SEL0	—	TRCIOC_0SEL2	TRCIOC_0SEL1	TRCIOC_0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOC_0SEL0	TRCIOC_0 pin select bits	b2 b1 b0 0 0 0: TRCIOC_0 pin not used 0 0 1: P1_3 assigned 0 1 0: P3_4 assigned 0 1 1: P0_7 assigned 1 0 0: P2_1 assigned 1 0 1: P6_6 assigned Other than the above: Do not set.	R/W
b1	TRCIOC_0SEL1			R/W
b2	TRCIOC_0SEL2			R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	TRCIOD_0SEL0	TRCIOD_0 pin select bits	b6 b5 b4 0 0 0: TRCIOD_0 pin not used 0 0 1: P1_0 assigned 0 1 0: P3_5 assigned 0 1 1: P0_6 assigned 1 0 0: P2_2 assigned 1 0 1: P6_7 assigned Other than the above: Do not set.	R/W
b5	TRCIOD_0SEL1			R/W
b6	TRCIOD_0SEL2			R/W
b7	—	Nothing is assigned. The write value must be 0. The read value is 0.		—

The TRC_0SR1 register is used to select which pin is assigned to timer RC_0 I/O. To use the I/O pin for timer RC_0, set this register.

Set the TRC_0SR1 register before setting the registers associated with timer RC_0. Also, do not change the set value of this register during timer RC_0 operation.

14.5.7 Timer RD_0 Pin Select Register 0 (TRD_0SR0)

Address 002A9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRDIOD0_0SEL1	TRDIOD0_0SEL0	TRDIOC0_0SEL1	TRDIOC0_0SEL0	TRDIOB0_0SEL1	TRDIOB0_0SEL0	TRDIOA0_0SEL1	TRDIOA0_0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA0_0SEL0	TRDIOA0_0/TRDCLK_0 pin select bits	b1 b0 0 0: TRDIOA0_0/TRDCLK_0 pin not used 0 1: P2_0 assigned 1 0: P3_5 assigned 1 1: Do not set.	R/W
b1	TRDIOA0_0SEL1			R/W
b2	TRDIOB0_0SEL0	TRDIOB0_0 pin select bits	b3 b2 0 0: TRDIOB0_0 pin not used 0 1: P2_1 assigned 1 0: P2_2 assigned 1 1: P3_4 assigned	R/W
b3	TRDIOB0_0SEL1			R/W
b4	TRDIOC0_0SEL0	TRDIOC0_0 pin select bits	b5 b4 0 0: TRDIOC0_0 pin not used 0 1: P2_2 assigned 1 0: P2_1 assigned 1 1: P3_7 assigned	R/W
b5	TRDIOC0_0SEL1			R/W
b6	TRDIOD0_0SEL0	TRDIOD0_0 pin select bits	b7 b6 0 0: TRDIOD0_0 pin not used 0 1: P2_3 assigned 1 0: P3_3 assigned 1 1: Do not set.	R/W
b7	TRDIOD0_0SEL1			R/W

The TRD_0SR0 register is used to select which pin is assigned to timer RD_0 I/O. To use the I/O pin for timer RD_0, set this register.
Set the TRD_0SR0 register before setting the registers associated with timer RD_0. Also, do not change the set value of this register during timer RD_0 operation.

14.5.8 Timer RD_0 Pin Select Register 1 (TRD_0SR1)

Address 002AAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRDIOD1_0SEL1	TRDIOD1_0SEL0	TRDIOC1_0SEL1	TRDIOC1_0SEL0	TRDIOB1_0SEL1	TRDIOB1_0SEL0	TRDIOA1_0SEL1	TRDIOA1_0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA1_0SEL0	TRDIOA1_0 pin select bits	b1 b0 0 0: TRDIOA1_0 pin not used 0 1: P2_4 assigned 1 0: P1_0 assigned 1 1: Do not set.	R/W
b1	TRDIOA1_0SEL1			R/W
b2	TRDIOB1_0SEL0	TRDIOB1_0 pin select bits	b3 b2 0 0: TRDIOB1_0 pin not used 0 1: P2_5 assigned 1 0: P1_1 assigned 1 1: Do not set.	R/W
b3	TRDIOB1_0SEL1			R/W
b4	TRDIOC1_0SEL0	TRDIOC1_0 pin select bits	b5 b4 0 0: TRDIOC1_0 pin not used 0 1: P2_6 assigned 1 0: P3_4 assigned 1 1: P1_2 assigned	R/W
b5	TRDIOC1_0SEL1			R/W
b6	TRDIOD1_0SEL0	TRDIOD1_0 pin select bits	b7 b6 0 0: TRDIOD1_0 pin not used 0 1: P2_7 assigned 1 0: P3_5 assigned 1 1: P1_3 assigned	R/W
b7	TRDIOD1_0SEL1			R/W

The TRD_0SR1 register is used to select which pin is assigned to timer RD_0 I/O. To use the I/O pin for timer RD_0, set this register.
Set the TRD_0SR1 register before setting the registers associated with timer RD_0. Also, do not change the set value of this register during timer RD_0 operation.

14.5.9 Timer Pin Select Register (TIMSR)

Address 002ADh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	TRE2OSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRE2OSEL0	TMRE2O pin select bit	0: P0_4 assigned 1: P6_0 assigned	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—	Reserved	Set to 0.	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—	Reserved	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

The TIMSR register is used to select which pin is assigned as timer RE2 I/O. To use the I/O pin for timer RE2, set this register.
Set the TIMSR register before setting the registers associated with timer RE2. Also, do not change the set value of this register during the operation of timer RE2.

14.5.10 UART0_0 Pin Select Register (U_0SR)

Address 002AEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	CLK_0SEL	—	RXD_0SEL	—	TXD_0SEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD_0SEL	TXD_0 pin select bit	0: TXD_0 pin not used 1: P1_4 assigned	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	RXD_0SEL	RXD_0 pin select bit	0: RXD_0 pin not used 1: P1_5 assigned	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	CLK_0SEL	CLK_0 pin select bit	0: CLK_0 pin not used 1: P1_6 assigned	R/W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	—			
b7	—			

The U_0SR register is used to select which pin is assigned to UART0_0 I/O. To use the I/O pin for UART0_0, set this register.
Set the U_0SR register before setting the registers associated with UART0_0. Also, do not change the set value of this register during UART0_0 operation.

14.5.11 UART0_1 Pin Select Register (U_1SR)

Address 002AFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	CLK_1SEL1	CLK_1SEL0	RXD_1SEL1	RXD_1SEL0	TXD_1SEL1	TXD_1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD_1SEL0	TXD_1 pin select bits	b1 b0 0 0: TXD_1 pin not used 0 1: P0_1 assigned 1 0: P6_3 assigned 1 1: Do not set.	R/W
b1	TXD_1SEL1			R/W
b2	RXD_1SEL0	RXD_1 pin select bits	b3 b2 0 0: RXD_1 pin not used 0 1: P0_2 assigned 1 0: P6_4 assigned 1 1: Do not set.	R/W
b3	RXD_1SEL1			R/W
b4	CLK_1SEL0	CLK_1 pin select bits	b5 b4 0 0: CLK_1 pin not used 0 1: P0_3 assigned 1 0: P6_2 assigned 1 1: P6_5 assigned	R/W
b5	CLK_1SEL1			R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

The U_1SR register is used to select which pin is assigned to UART0_1 I/O. To use the I/O pin for UART0_1, set this register.
Set the U_1SR register before setting the registers associated with UART0_1. Also, do not change the set value of this register during UART0_1 operation.

14.5.12 UART2 Pin Select Register 0 (U2SR0)

Address 002B2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	RXD2SEL2	RXD2SEL1	RXD2SEL0	—	TXD2SEL2	TXD2SEL1	TXD2SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD2SEL0	TXD2 pin select bits	b2 b1 b0 0 0 0: TXD2 pin not used 0 0 1: P3_7 assigned 0 1 0: P3_4 assigned 0 1 1: P0_0 assigned 1 0 0: P2_0 assigned 1 0 1: P6_6 assigned Other than the above: Do not set.	R/W
b1	TXD2SEL1			R/W
b2	TXD2SEL2			R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	RXD2SEL0	RXD2 pin select bits	b6 b5 b4 0 0 0: RXD2 pin not used 0 0 1: P3_4 assigned 0 1 0: P3_7 assigned 0 1 1: P4_5 assigned 1 0 0: P2_0 assigned 1 0 1: P6_7 assigned Other than the above: Do not set.	R/W
b5	RXD2SEL1			R/W
b6	RXD2SEL2			R/W
b7	—	Nothing is assigned. The write value must be 0. The read value is 0.		—

The U2SR0 register is used to select which pin is assigned to UART2 I/O. To use the I/O pin for UART2, set this register.
Set the U2SR0 register before setting the registers associated with UART2. Also, do not change the set value of this register during UART2 operation.

14.5.13 UART2 Pin Select Register 1 (U2SR1)

Address 002B3h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	CTS2SEL1	CTS2SEL0	—	CLK2SEL2	CLK2SEL1	CLK2SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK2SEL0	CLK2 pin select bits	b2 b1 b0 0 0 0: CLK2 pin not used 0 0 1: P3_5 assigned 0 1 0: P0_5 assigned 0 1 1: P6_5 assigned Other than the above: Do not set.	R/W
b1	CLK2SEL1			R/W
b2	CLK2SEL2			R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	CTS2SEL0	$\overline{CTS2}$/$\overline{RTS2}$ pin select bits	b5 b4 0 0: $\overline{CTS2}$/$\overline{RTS2}$ pin not used 0 1: P3_3 assigned 1 0: P3_1 assigned 1 1: Do not set.	R/W
b5	CTS2SEL1			R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

The U2SR1 register is used to select which pin is assigned to UART2 I/O. To use the I/O pin for UART2, set this register.
Set the U2SR1 register before setting the registers associated with UART2. Also, do not change the set value of this register during UART2 operation.

14.5.14 SSU/IIC_0 Pin Select Register (SSUIIC_0SR)

Address 002B4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	SCS_0SEL	SSI_0SEL1	SSI_0SEL0	—	—	SDA_0SEL	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	SDA_0SEL	SDA_0 pin select bit	0: P3_7 assigned 1: P3_4 assigned	R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	—			
b4	SSI_0SEL0	SSI_0 pin select bits	b1 b0 0 0: P3_4 assigned 0 1: P3_3 assigned 1 0: P1_6 assigned 1 1: Do not set.	R/W
b5	SSI_0SEL1			R/W
b6	SCS_0SEL	$\overline{\text{SCS\_0}}$ pin select bit	0: P3_3 assigned 1: P3_4 assigned	R/W
b7	—	Nothing is assigned. The write value must be 0. The read value is 0.		—

The SSUIIC_0SR register is used to select which pin is assigned to synchronous serial communication unit (SSU_0)/I^{2}C bus interface (I^{2}C_0) I/O. To use the I/O pin for SSU_0/I^{2}C_0, set this register.
Set the SSUIIC_0SR register before setting the registers associated with SSU_0/I^{2}C_0. Also, do not change the set value of this register during SSU_0/I^{2}C_0 operation.

14.5.15 INT Interrupt Input Pin Select Register 0 (INTSR0)

Address 002B6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3SEL1	INT3SEL0	INT2SEL1	INT2SEL0	INT1SEL2	INT1SEL1	INT1SEL0	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	INT1SEL0	$\overline{\text{INT1}}$ pin select bits	b3 b2 b1 0 0 0: P1_7 assigned 0 0 1: P1_5 assigned 0 1 0: P2_0 assigned Other than the above: Do not set.	R/W
b2	INT1SEL1			R/W
b3	INT1SEL2			R/W
b4	INT2SEL0	$\overline{\text{INT2}}$ pin select bits	b5 b4 0 0: P6_6 assigned 0 1: Do not set. 1 0: P6_4 assigned 1 1: P0_2 assigned	R/W
b5	INT2SEL1			R/W
b6	INT3SEL0	$\overline{\text{INT3}}$ pin select bits	b7 b6 0 0: P3_3 assigned 0 1: P3_7 assigned 1 0: P6_7 assigned 1 1: Do not set.	R/W
b7	INT3SEL1			R/W

The INTSR0 register is used to select which pin is assigned to $\overline{\text{INTi}}$ (i = 1 to 3) input. To use $\overline{\text{INTi}}$, set this register.
Set the INTSR0 register before setting the registers associated with $\overline{\text{INTi}}$. Also, do not change the set value of this register during $\overline{\text{INTi}}$ operation.
$\overline{\text{INT0}}$ and $\overline{\text{INT4}}$ are assigned to P4_5 and P6_5, respectively, regardless of the INTSR0 register.

14.5.16 I/O Function Pin Select Register (PINSR)

Address 002B9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IOINSEL	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	IOINSEL	I/O port input function select bit	0: The I/O port input function depends on the PDi (i = 0 to 4, 6, or 9) register. When the PDi_j (j = 0 to 7) bit in the PDi register is set to 0 (input mode), the pin input level can be read. When the PDi_j bit in the PDi register is set to 1 (output mode), the value of the port latch can be read. 1: The I/O port input function can read the pin input level regardless of the PDi register	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

IOINSEL Bit (I/O port input function select bit)

When the PDi_j bit in the PDi register is 1 (output mode), the IOINSEL bit is used to select whether the value read from the PORTi register is the port latch or the pin input level of the I/O port. If set to 0, the value of the port latch is read. If set to 1, the pin input level of the I/O port is read.

Table 14.5 lists I/O Port Values Read by Using IOINSEL Bit. The IOINSEL bit can be used to change the input function of all I/O ports.

Table 14.5 I/O Port Values Read by Using IOINSEL Bit

PDi_j Bit in PDi Register	0 (Input Mode)		1 (Output Mode)	
IOINSEL bit	0	1	0	1
I/O port values read	Pin input level		Port latch value	Pin input level

i = 0 to 4, 6, or 9, j = 0 to 7

14.5.17 Pull-Up Control Register 0 (PUR0)

Address 002C0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PUR07	PUR06	PUR05	PUR04	PUR03	PUR02	PUR01	PUR00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PUR00	P0_0 to P0_3 pull-up	0: Not pulled up 1: Pulled up (1)	R/W
b1	PUR01	P0_4 to P0_7 pull-up		R/W
b2	PUR02	P1_0 to P1_3 pull-up		R/W
b3	PUR03	P1_4 to P1_7 pull-up		R/W
b4	PUR04	P2_0 to P2_3 pull-up		R/W
b5	PUR05	P2_4 to P2_7 pull-up		R/W
b6	PUR06	P3_0, P3_1, or P3_3 pull-up		R/W
b7	PUR07	P3_4, P3_5, or P3_7 pull-up		R/W

Note:
1. When this bit is set to 1 (pulled up), the pin whose port direction bit is set to 0 (input mode) is pulled up.

The set values in the PUR0 register are valid for pins used as input.

14.5.18 Pull-Up Control Register 1 (PUR1)

Address 002C1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	PUR15	PUR14	—	—	PUR11	PUR10
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PUR10	P4_3 pull-up	0: Not pulled up 1: Pulled up (1)	R/W
b1	PUR11	P4_4 to P4_7 pull-up		R/W
b2	—	Reserved	Set to 0.	R/W
b3	—			
b4	PUR14	P6_0 to P6_3 pull-up	0: Not pulled up 1: Pulled up (1)	R/W
b5	PUR15	P6_4 to P6_7 pull-up		R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

Note:
1. When this bit is set to 1 (pulled up), the pin whose port direction bit is set to 0 (input mode) is pulled up.

The set values in the PUR1 register are valid for pins used as input.

14.5.19 Pull-Up Control Register 2 (PUR2)

Address 002C2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PUR23	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			
b2	—			
b3	PUR23	P9_4 to P9_7 pull-up	0: Not pulled up 1: Pulled up (1)	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. When this bit is set to 1 (pulled up), the pin whose port direction bit is set to 0 (input mode) is pulled up.

The set values in the PUR2 register are valid for pins used as input.

14.5.20 Port P1 Drive Capacity Control Register (P1DRR)

Address 002C8h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P1DRR7	P1DRR6	P1DRR5	P1DRR4	P1DRR3	P1DRR2	P1DRR1	P1DRR0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P1DRR0	P1_0 drive capacity	0: Low 1: High (1)	R/W
b1	P1DRR1	P1_1 drive capacity		R/W
b2	P1DRR2	P1_2 drive capacity		R/W
b3	P1DRR3	P1_3 drive capacity		R/W
b4	P1DRR4	P1_4 drive capacity		R/W
b5	P1DRR5	P1_5 drive capacity		R/W
b6	P1DRR6	P1_6 drive capacity		R/W
b7	P1DRR7	P1_7 drive capacity		R/W

Note:
1. Both high and low output are set to high drive capacity.

The P1DRR register is used to select whether the drive capacity of the P1 output transistor is set to low or high. The P1DRRj bit (j = 0 to 7) is used to select whether the drive capacity of the output transistor is set to low or high for each pin.
The set values in the P1DRR register are valid for pins used as output.

14.5.21 Port P2 Drive Capacity Control Register (P2DRR)

Address 002C9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P2DRR7	P2DRR6	P2DRR5	P2DRR4	P2DRR3	P2DRR2	P2DRR1	P2DRR0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P2DRR0	P2_0 drive capacity	0: Low 1: High (1)	R/W
b1	P2DRR1	P2_1 drive capacity		R/W
b2	P2DRR2	P2_2 drive capacity		R/W
b3	P2DRR3	P2_3 drive capacity		R/W
b4	P2DRR4	P2_4 drive capacity		R/W
b5	P2DRR5	P2_5 drive capacity		R/W
b6	P2DRR6	P2_6 drive capacity		R/W
b7	P2DRR7	P2_7 drive capacity		R/W

Note:
1. Both high and low output are set to high drive capacity.

The P2DRR register is used to select whether the drive capacity of the P2 output transistor is set to low or high. The P2DRRj bit (j = 0 to 7) is used to select whether the drive capacity of the output transistor is set to low or high for each pin.
The set values in the P2DRR register are valid for pins used as output.

14.5.22 Drive Capacity Control Register 0 (DRR0)

Address 002CCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DRR07	DRR06	—	—	—	—	DRR01	DRR00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DRR00	P0_0 to P0_3 drive capacity	0: Low 1: High (1)	R/W
b1	DRR01	P0_4 to P0_7 drive capacity		R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	—			
b4	—			
b5	—			
b6	DRR06	P3_0, P3_1, or P3_3 drive capacity	0: Low 1: High (1)	R/W
b7	DRR07	P3_4, P3_5, or P3_7 drive capacity		R/W

Note:
1. Both high and low output are set to high drive capacity.

The set values in the DRR0 register are valid for pins used as output.

DRR00 Bit (P0_0 to P0_3 drive capacity)

The DRR00 bit is used to select whether the drive capacity of the P0_0 to P0_3 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for four pins.

DRR01 Bit (P0_4 to P0_7 drive capacity)

The DRR01 bit is used to select whether the drive capacity of the P0_4 to P0_7 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for four pins.

DRR06 Bit (P3_0, P3_1, or P3_3 drive capacity)

The DRR06 bit is used to select whether the drive capacity of the P3_0, P3_1, or P3_3 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for three pins.

DRR07 Bit (P3_4, P3_5, or P3_7 drive capacity)

The DRR07 bit is used to select whether the drive capacity of the P3_4, P3_5, or P3_7 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for three pins.

14.5.23 Drive Capacity Control Register 1 (DRR1)

Address 002CDh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	DRR15	DRR14	—	—	DRR11	DRR10
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DRR10	P4_3 drive capacity	0: Low 1: High (1)	R/W
b1	DRR11	P4_4 to P4_7 drive capacity		R/W
b2	—	Reserved	Set to 0.	R/W
b3	—			
b4	DRR14	P6_0 to P6_3 drive capacity	0: Low 1: High (1)	R/W
b5	DRR15	P6_4 to P6_7 drive capacity		R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

Note:
1. Both high and low output are set to high drive capacity.

The set values in the DRR1 register are valid for pins used as output.

DRR10 Bit (P4_3 drive capacity)

The DRR10 bit is used to select whether the drive capacity of the P4_3 output transistor is set to low or high. This bit is used to select whether the drive capacity of the output transistor is set to low or high for one pin.

DRR11 Bit (P4_4 to P4_7 drive capacity)

The DRR11 bit is used to select whether the drive capacity of the P4_4 to P4_7 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for four pins.

DRR14 Bit (P6_0 to P6_3 drive capacity)

The DRR14 bit is used to select whether the drive capacity of the P6_0 to P6_3 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for four pins.

DRR15 Bit (P6_4 to P6_7 drive capacity)

The DRR15 bit is used to select whether the drive capacity of the P6_4 to P6_7 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for four pins.

14.5.24 Drive Capacity Control Register 2 (DRR2)

Address 002CEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	DRR23	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			
b2	—			
b3	DRR23	P9_4 to P9_7 drive capacity	0: Low 1: High (1)	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. Both high and low output are set to high drive capacity.

The set values in the DRR2 register are valid for pins used as output.

DRR23 Bit (P9_4 to P9_7 drive capacity)

The DRR23 bit is used to select whether the drive capacity of the P9_4 to P9_7 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for four pins.

14.5.25 Input Threshold Control Register 0 (VLT0)

Address 002D0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VLT07	VLT06	VLT05	VLT04	VLT03	VLT02	VLT01	VLT00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VLT00	P0 input level select bits	b1 b0 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b1	VLT01			R/W
b2	VLT02	P1 input level select bits	b3 b2 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b3	VLT03			R/W
b4	VLT04	P2 input level select bits	b5 b4 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b5	VLT05			R/W
b6	VLT06	P3_0, P3_1, P3_3 to P3_5, P3_7 input level select bits	b7 b6 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b7	VLT07			R/W

The VLT0 register is used to select the voltage level of the input threshold values for ports P0 to P2, P3_0, P3_1, P3_3 to P3_5, or P3_7. Bits VLT00 to VLT07 are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC) for every eight pins.

14.5.26 Input Threshold Control Register 1 (VLT1)

Address 002D1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	VLT15	VLT14	—	—	VLT11	VLT10
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VLT10	P4_2 to P4_7 input level select bits	b1 b0 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b1	VLT11			R/W
b2	—	Reserved	Set to 0.	R/W
b3	—			
b4	VLT14	P6 input level select bits	b5 b4 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b5	VLT15			R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

The VLT1 register is used to select the voltage level of the input threshold values for ports P4_2 to P4_7, and P6. Bits VLT10, VLT11, VLT14, and VLT15 are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC).

14.5.27 Input Threshold Control Register 2 (VLT2)

Address 002D2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VLT23	VLT22	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			
b2	VLT22	P9_4 to P9_7 input level select bits	b3 b2 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b3	VLT23			R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

The VLT2 register is used to select the voltage level of the input threshold values for ports P9_4 to P9_7. Bits VLT22 and VLT23 are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC).

14.5.28 Port Pi Register (PORTi) (i = 0 to 4, 6, or 9)

Address 002E0h (PORT0), 002E1h (PORT1), 002E4h (PORT2), 002E5h (PORT3 (1)), 002E8h (PORT4 (2)), 002ECh (PORT6), 002F1h (PORT9 (3))

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	Pi_7	Pi_6	Pi_5	Pi_4	Pi_3	Pi_2	Pi_1	Pi_0
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	Pi_0	Port Pi_0 bit	0: Low level 1: High level	R/W
b1	Pi_1	Port Pi_1 bit		R/W
b2	Pi_2	Port Pi_2 bit		R/W
b3	Pi_3	Port Pi_3 bit		R/W
b4	Pi_4	Port Pi_4 bit		R/W
b5	Pi_5	Port Pi_5 bit		R/W
b6	Pi_6	Port Pi_6 bit		R/W
b7	Pi_7	Port Pi_7 bit		R/W

Notes:
1. Bits P3_2 and P3_6 are reserved.
   The write value must be 0 for bits P3_2 and P3_6. The read value is 0.
2. Nothing is assigned to bits P4_0 and P4_1 in the PORT4 register.
   The write value must be 0 for bits P4_0 and P4_1 in the P4 register. The read value is 0.
3. Bits P9_0 to P9_3 are reserved.
   The write value must be 0 for bits P9_0 to P9_3. The read value is 0.

Data input to and output from external devices are accomplished by reading and writing to the PORTi register. The PORTi register consists of a port latch to retain output data and a circuit to read the pin state. The value written in the port latch is output from the pin. Each bit in the PORTi register corresponds to one port.

Pi_j Bit (j = 0 to 7) (Port Pi_j bit)

The pin level of any I/O port which is set to input mode can be read by reading the corresponding bit in this register. The pin level of any I/O port which is set to output mode can be controlled by writing to the corresponding bit in this register.

14.5.29 Port Pi Direction Register (PDi) (i = 0 to 4, 6, or 9)

Address 002E2h (PD0 (1)), 002E3h (PD1), 002E6h (PD2), 002E7h (PD3 (2)), 002EAh (PD4 (3)), 002EEh (PD6), 002F3h (PD9 (4))

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PDi_7	PDi_6	PDi_5	PDi_4	PDi_3	PDi_2	PDi_1	PDi_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PDi_0	Port Pi_0 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b1	PDi_1	Port Pi_1 direction bit		R/W
b2	PDi_2	Port Pi_2 direction bit		R/W
b3	PDi_3	Port Pi_3 direction bit		R/W
b4	PDi_4	Port Pi_4 direction bit		R/W
b5	PDi_5	Port Pi_5 direction bit		R/W
b6	PDi_6	Port Pi_6 direction bit		R/W
b7	PDi_7	Port Pi_7 direction bit		R/W

Notes:
1. Write to the PD0 register with the next instruction after that used to set the PRC2 bit in the PRCR register to 1 (write enabled).
2. Bits PD3_2 and PD3_6 are reserved.
   The write value must be 0 for bits PD3_2 and PD3_6. The read value is 0.
3. Nothing is assigned to bits PD4_0 to PD4_2 in the PD4 register.
   The write value must be 0 for bits PD4_0 to PD4_2 in the PD4 register. The read value is 0.
4. Bits PD9_0 to P9_3 are reserved.
   The write value must be 0 for bits PD9_0 to PD9_3. The read value is 0.

The PDi register is used to select whether I/O ports are used for input or output. Each bit in the PDi register corresponds to one port.

14.5.30 I/O Pins Not Controlled by Pin Select Registers

I/O pins that are not controlled by the pin select registers are shown below.

(1) Clock synchronous serial interface (SSU_1/IIC_1) I/O pins
SCL_1: P9_6
SDA_1: P9_5
SSI_1: P9_4
SCS_1: P9_5
SSCK_1: P9_6
SSO_1: P9_7

(2) Key input interrupt input pins
KI0: P1_0
KI1: P1_1
KI2: P1_2
KI3: P1_3

(3) CAN I/O pins
CTX_0: P6_1
CRX_0: P6_2

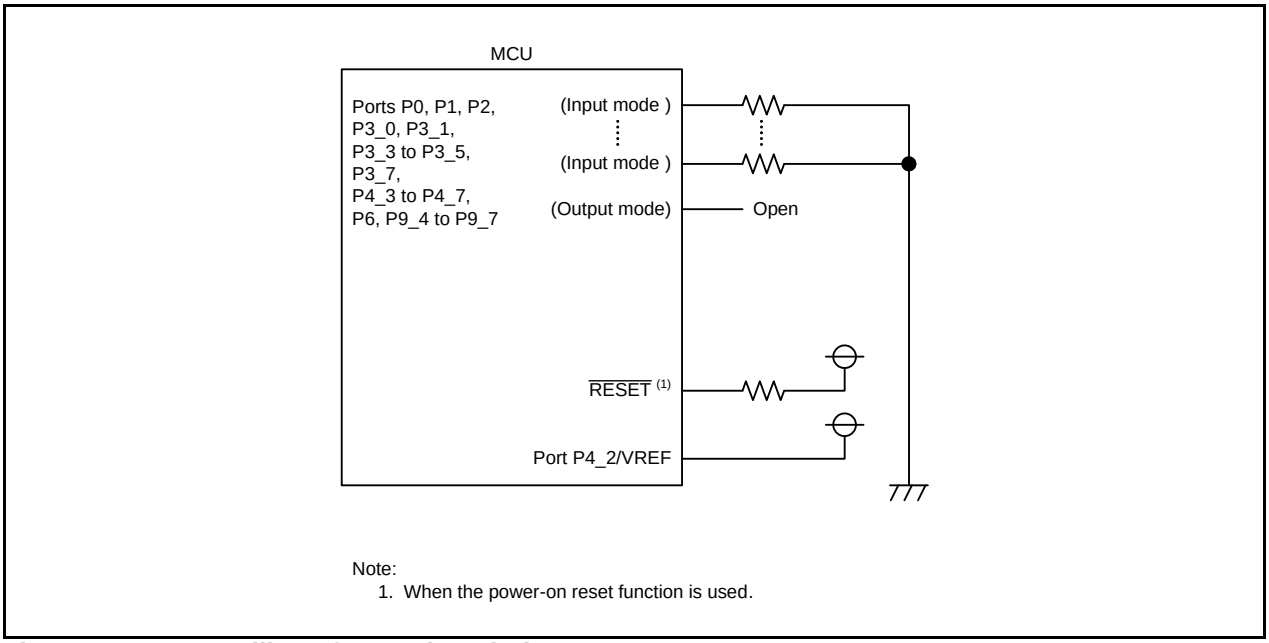
14.6 Handling of Unassigned Pins

Table 14.6 lists the Handling of Unassigned Pins and Figure 14.9 shows the Handling of Unassigned Pins.

Table 14.6 Handling of Unassigned Pins

Pin Name	Connection
Ports P0, P1, P2, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_7, P6, P9_4 to P9_7	For each of these pins either: • Set the pin to input mode and either connect it to VSS through a resistor (pull-down) or connect it to VCC through a resistor (pull-up) (1) Or: • Set each of these pins to output mode and leave it open (1, 2)
Port P4_2/VREF	Connect to VCC
$\overline{\text{RESET}}$ (3)	Connect to VCC through a resistor (pull-up) (1)

Notes:
1. Connect these unused pins to the MCU using the shortest wire length (2 cm or less) possible.
2. If these ports are set to output mode and left open, they remain in input mode until they are switched to output mode by a program. The voltage level of these pins may be unstable and the power current may increase while the ports remain in input mode. The content of the direction registers may change due to noise or program runaway caused by noise. The program should periodically reconfigure the content for enhanced reliability.
3. When the power-on reset is used.



Note:
1. When the power-on reset function is used.

Figure 14.9 Handling of Unassigned Pins

15. Timer RJ

Timer RJ is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting an internal source or external pulse.
Timer RJ contains two units, timer RJ_0 and timer RJ_1, which have the same function. This chapter describes these units as timer RJ unless there are differences between them. This timer consists of a reload register and a counter which are allocated to the same address.

15.1 Overview

Table 15.1 lists the Timer RJ Specifications and Figure 15.1 shows the Timer RJ Block Diagram (i = 1 or 2).

Table 15.1 Timer RJ Specifications

Item		Description
Operating modes	Timer mode	The internal count source is counted.
	Pulse output mode	The internal count source is counted and the output is inverted at each underflow of the timer.
	Event counter mode	An external pulse is counted.
	Pulse width measurement mode	An external pulse width is measured.
	Pulse period measurement mode	An external pulse period is measured.
Count source		f1, f2, f8, fOCO, event input from the ELC, or external pulse selectable
Interrupt		• When the counter underflows. • When the measurement of the active width of the external input (TRJIO) is completed in pulse width measurement mode. • When the set edge of the external input (TRJIO) is input in pulse period measurement mode.
Selectable functions		• Coordination with the hardware LIN module Input from the hardware LIN module can be used for counter reload operation. • Coordination with the event link controller (ELC) Event input from the ELC is selectable as a count source.

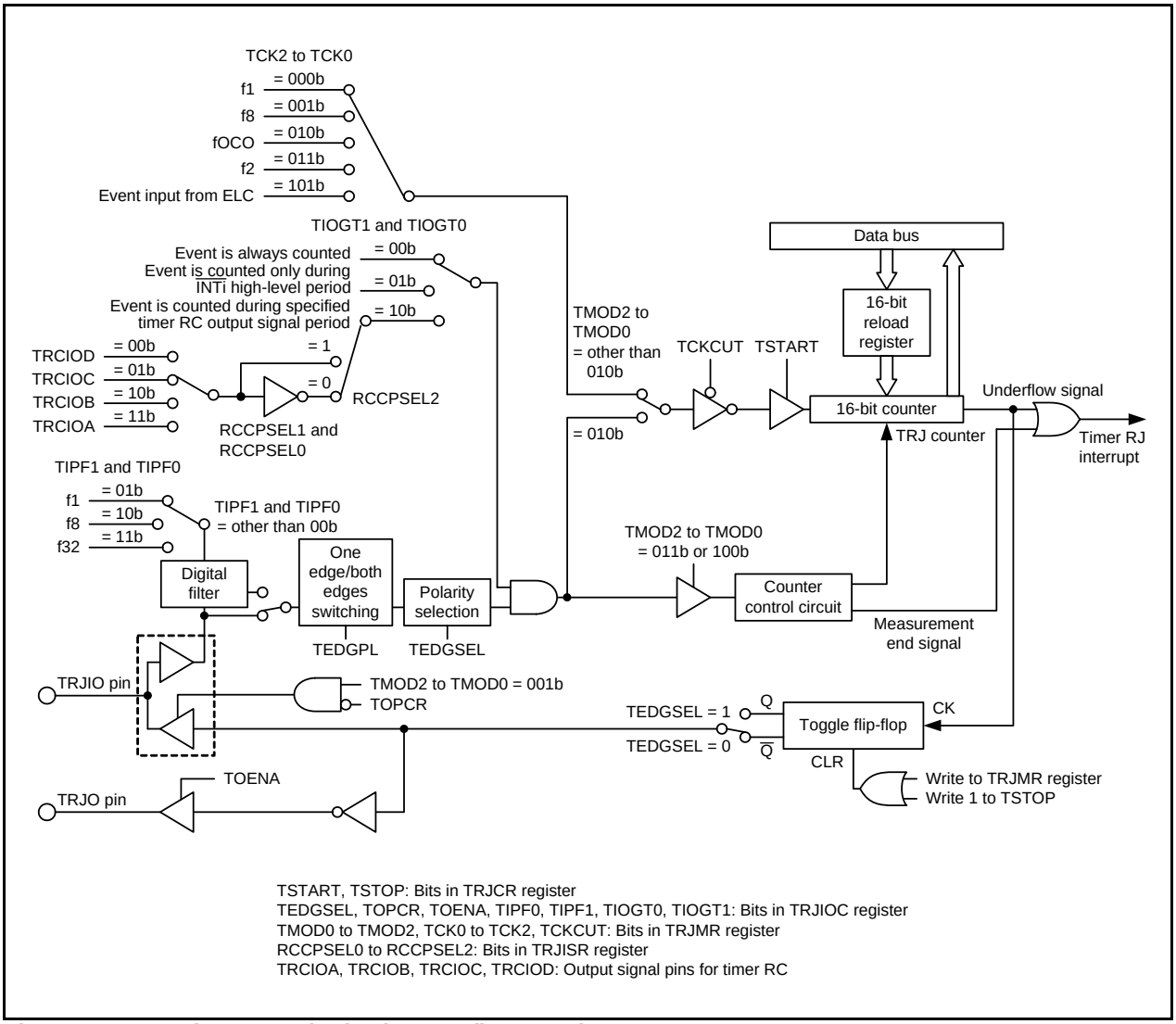


Figure 15.1 Timer RJ Block Diagram (i = 1 or 2)

15.2 I/O Pins

Table 15.2 lists the Timer RJ Pin Configuration.

Table 15.2 Timer RJ Pin Configuration

Pin Name	I/O	Function
$\overline{\text{INT1}}$	Input	Event counter mode control for timer RJ_0
$\overline{\text{INT2}}$	Input	Event counter mode control for timer RJ_1
TRJIO (1)	Input/Output	External pulse input and pulse output for timer RJ
TRJO (1)	Output	Pulse output for timer RJ

Note:
1. When a pulse is output from TRJIO and TRJO simultaneously, TRJIO is set to the inverted output of TRJO.

15.3 Registers

Table 15.3 lists the Timer RJ Register Configuration.

Table 15.3 Timer RJ Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Timer RJ_0 Counter Register	TRJ_0	FFFFh	00110h	16
Timer RJ_0 Control Register	TRJCR_0	00h	00112h	8
Timer RJ_0 I/O Control Register	TRJIOC_0	00h	00113h	8
Timer RJ_0 Mode Register	TRJMR_0	00h	00114h	8
Timer RJ_0 Event Pin Select Register	TRJISR_0	00h	00115h	8
Timer RJ_1 Counter Register	TRJ_1	FFFFh	00118h	16
Timer RJ_1 Control Register	TRJCR_1	00h	0011Ah	8
Timer RJ_1 I/O Control Register	TRJIOC_1	00h	0011Bh	8
Timer RJ_1 Mode Register	TRJMR_1	00h	0011Ch	8
Timer RJ_1 Event Pin Select Register	TRJISR_1	00h	0011Dh	8

15.3.1 Timer RJ Counter Register (TRJ)

Address 00110h (TRJ_0), 00118h (TRJ_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Function	Setting Range	R/W
b15 to b0	—	16-bit counter and reload register (1, 2)	0001h to FFFFh	R/W

Notes:
1. When 1 is written to the TSTOP bit in the TRJCR register, the 16-bit counter is forcibly stopped and set to FFFFh.
2. The TRJ register must be accessed in 16-bit units. Do not access this register in 8-bit units.

TRJ is a 16-bit register. The write value is written to the reload register and the read value is read from the counter.
When a value is written to the TRJ register, the value is reflected to the reload register and the counter differently depending on the value of the TCSTF bit in the TRJCR register. For details, refer to **15.4.1 Reload Register and Counter Rewrite Operation**.

15.3.2 Timer RJ Control Register (TRJCR)

Address 00112h (TRJCR_0), 0011Ah (TRJCR_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RJ count start bit (1)	0: Count stops 1: Count starts	R/W
b1	TCSTF	Timer RJ count status flag (1)	0: Count stops 1: Count in progress	R
b2	TSTOP	Timer RJ count forced stop bit (2)	When 1 is written to this bit, the count is forcibly stopped. The read value is 0.	W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	TEDGF	Active edge judgement flag (3)	0: No active edge received 1: Active edge received	R/W
b5	TUNDF	Timer RJ underflow flag (3)	0: No underflow 1: Underflow	R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

Notes:
1. For notes on using bits TSTART and TCSTF, refer to **15.5 Notes on Timer RJ (2)**.
2. When 1 (count is forcibly stopped) is written to the TSTOP bit, bits TSTART and TCSTF are initialized at the same time. The pulse output level is also initialized.
3. Write to the TRJCR register using the MOV instruction. If the read-modify-write instruction is executed to set the TRJCR register, bits TEDGF and TUNDF may be set to 0 depending on the timing.

TSTART Bit (Timer RJ count start bit)

Count operation is started by writing 1 to the TSTART bit and stopped by writing 0. When the TSTART bit is set to 1 (count starts), the TCSTF bit is set to 1 (count in progress) in synchronization with the count source. Also, after 0 is written to the TSTART bit, the TCSTF bit is set to 0 (count stops) in synchronization with the count source. For details, refer to **15.5 Notes on Timer RJ (2)**.

TCSTF Bit (Timer RJ count status flag)

[Conditions for setting to 0]
- When 0 is written to the TSTART bit (the TCSTF bit is set to 0 in synchronization with the count source).
- When 1 is written to the TSTOP bit.

[Condition for setting to 1]
- When 1 is written to the TSTART bit (the TCSTF bit is set to 1 in synchronization with the count source).

TEDGF Bit (Active edge judgement flag)

[Condition for setting to 0]
- When 0 is written to this bit by a program.

[Conditions for setting to 1]
- When the measurement of the active width of the external input (TRJIO) is completed in pulse width measurement mode.
- The set edge of the external input (TRJIO) is input in pulse period measurement mode.

TUNDF Bit (Timer RJ underflow flag)

[Condition for setting to 0]
- When 0 is written to this bit by a program.

[Condition for setting to 1]
- When the counter underflows.

15.3.3 Timer RJ I/O Control Register (TRJIOC)

Address 00113h (TRJIOC_0), 0011Bh (TRJIOC_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	TIOSEL	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	I/O polarity switch bit	Function varies depending on the operating mode (refer to Tables 15.4 and 15.5).	R/W
b1	TOPCR	TRJIO output control bit (1)	0: TRJIO output enabled (toggle output is started) 1: TRJIO output disabled (toggle output is stopped)	R/W
b2	TOENA	TRJO output enable bit	0: TRJO output disabled (port) 1: TRJO output enabled	R/W
b3	TIOSEL	Event input select bit	0: Input from TRJIO pin 1: Input from hardware LIN	R/W
b4	TIPF0	TRJIO input filter select bits	b5 b4 0 0: No filter 0 1: Filter enabled, sampling at f1 1 0: Filter enabled, sampling at f8 1 1: Filter enabled, sampling at f32	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRJIO count control bits (2, 3)	b7 b6 0 0: Event is counted 0 1: Event is counted only during $\overline{\text{INTi}}$ (i = 1 or 2) high-level period 1 0: Event is counted during timer RC output signal period specified by RCCPSEL bit in TRJISR register 1 1: Do not set.	R/W
b7	TIOGT1			R/W

Notes:
1. The TOPCR bit is enabled only in pulse output mode. In pulse output mode, output is inverted when this bit is set to 0, and output is disabled and the port selected as the TRJIO function is held in the high-impedance state when this bit is set to 1. Set the TOPCR bit after the setting of the TRJMR register is completed.
2. The period to count the event is selected by the RCCPSEL2 bit when the timer RC output signal is used.
3. Bits TIOGT0 and TIOGT1 are enabled only in event counter mode.

TEDGSEL Bit (I/O polarity switch bit)

The TEDGSEL bit is used to switch the TRJO output polarity and the TRJIO I/O edge and polarity. In pulse output mode, only the polarities of the TRJO output and the TRJIO output are controlled. The TRJO output and TRJIO output are initialized when the TRJMR register is written or 1 is written to the TSTOP bit in the TRJCR register.

Table 15.4 TRJIO I/O Edge and Polarity Switching

Operating Mode	Function
Timer mode	Not used (I/O port)
Pulse output mode	0: Output is started at high (initialization level is high) 1: Output is started at low (initialization level is low)
Event counter mode	0: Count at rising edge 1: Count at falling edge
Pulse width measurement mode	0: Low-level width is measured 1: High-level width is measured
Pulse period measurement mode	0: Measure from one rising edge to the next rising edge 1: Measure from one falling edge to the next falling edge

Table 15.5 TRJO Output Polarity Switching

Operating Mode	Function
All modes	0: Output is started at low (initialization level is low) 1: Output is started at high (initialization level is high)

TOPCR Bit (TRJIO output control bit)

The TOPCR bit is enabled only in pulse output mode. When this bit is set to 0, a pulse can be output from the TRJIO pin. When this bit is set to 1, output is disabled and the port selected as the TRJIO function is held in the high-impedance state.

In other operating modes, the functions listed in Table 15.6 are supported regardless of the setting of the TOPCR bit.

Table 15.6 TRJIO Pin Function

Operating Mode	Function
Timer mode	Not used (I/O port)
Event counter mode	Event count input (count source input)
Pulse width measurement mode	Input for pulse width measurement
Pulse period measurement mode	Input for pulse period measurement

TIOSEL Bit (Event input select bit)

When using as hardware LIN, set the TIOSEL bit to 1.

Bits TIPF0 and TIPF1 (TRJIO input filter select bits)

These bits are used to specify the sampling frequency of the filter for the TRJIO input. If the input to the TRJIO pin is sampled and the value matches three successive times, the input is determined.

15.3.4 Timer RJ Mode Register (TRJMR)

Address 00114h (TRJMR_0), 0011Ch (TRJMR_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	TCK2	TCK1	TCK0	TEDGPL	TMOD2	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RJ operating mode select bits	b2 b1 b0 0 0 0: Timer mode 0 0 1: Pulse output mode 0 1 0: Event counter mode 0 1 1: Pulse width measurement mode 1 0 0: Pulse period measurement mode Other than the above: Do not set.	R/W
b1	TMOD1			R/W
b2	TMOD2			R/W
b3	TEDGPL	TRJIO edge polarity select bit (1)	0: One edge 1: Both edges	R/W
b4	TCK0	Timer RJ count source select bits (2, 3)	b6 b5 b4 0 0 0: f1 0 0 1: f8 0 1 0: fOCO 0 1 1: f2 1 0 0: Do not set. 1 0 1: Event input from event link controller (ELC) Other than the above: Do not set.	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	TCKCUT	Timer RJ count source cutoff bit (3)	0: Count source is supplied 1: Count source is cut off	R/W

Notes:
1. The TEDGPL bit is enabled only in event counter mode.
2. When event counter mode is selected, the external input (TRJIO) is selected as the count source regardless of the setting of bits TCK0 to TCK2.
3. Do not switch or cut off the count source during count operation. When switching or cutting off the count source, set the TSTART bit in the TRJCR register to 0 (count is stopped) and the TCSTF bit to 0 (count is stopped) to stop the timer count.

Select the operating mode when the count is stopped (the TSTART bit is 0 and the TCSTF bit is 0).
When a value is written to the TRJMR register, the toggle flip-flop is initialized. For details on the output level at initialization, refer to the description of the TEDGSEL bit shown in **15.3.3 Timer RJ I/O Control Register (TRJIOC)**

15.3.5 Timer RJ Event Pin Select Register (TRJISR)

Address 00115h (TRJISR_0), 0011Dh (TRJISR_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	RCCPSEL2	RCCPSEL1	RCCPSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RCCPSEL0	Timer RC output signal select bits	b1 b0 0 0: TRCIOD 0 1: TRCIOC 1 0: TRCIOB 1 1: TRCIOA	R/W
b1	RCCPSEL1			R/W
b2	RCCPSEL2	Timer RC output signal inversion bit	0: Low-level period of timer RC output signal is counted 1: High-level period of timer RC output signal is counted	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

This register is used in event counter mode. Enabled only when bits TIOGT1 and TIOGT0 in the TRJIOC register are 10b (event is counted during timer RC output signal period specified by bits RCCPSEL0 and RCCPSE1 in TRJISR register).

The connection between event input from timer RC and timer RJ_0 is shown below.

• Timer RC_0 → timer RJ_0

15.4 Operation

15.4.1 Reload Register and Counter Rewrite Operation

Regardless of the operating mode, the timing of the rewrite operation to the reload register and the counter differs depending on the value of the TSTART bit in the TRJCR register. When the TSTART bit is 0 (count stops), the count value is directly written to the reload register, and then to the counter in synchronization with the system clock (f). When the TSTART bit is 1 (count starts), the value is written to the reload register in synchronization with the count source after three cycles, and then to the counter in synchronization with the next count source.

Figure 15.2 shows the Timing of Rewrite Operation with TSTART Bit Value.

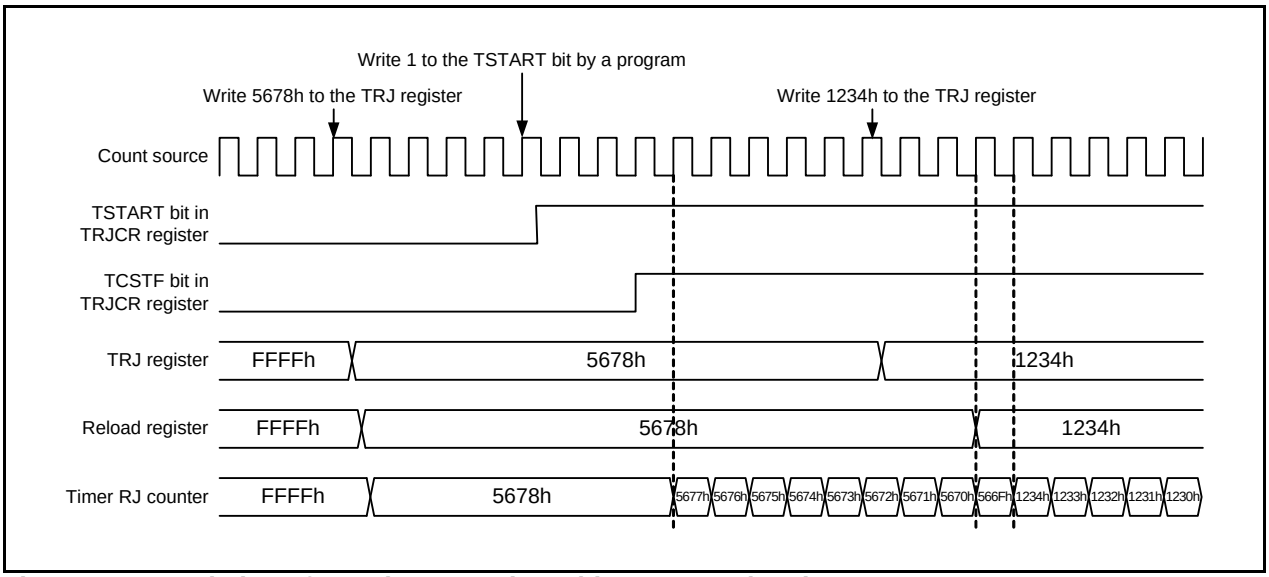


Figure 15.2 Timing of Rewrite Operation with TSTART Bit Value

15.4.2 Timer Mode

In this mode, the counter is decremented by the count source selected by bits TCK0 to TCK2 in the TRJMR register.

In timer mode, the count value is decremented by 1 each time the count source is input. If the next count source is input after the count value reaches 0000h, the set value in the reload register is loaded, and an underflow occurs, generating an interrupt.

Figure 15.3 shows an Operation Timing Example in Timer Mode.

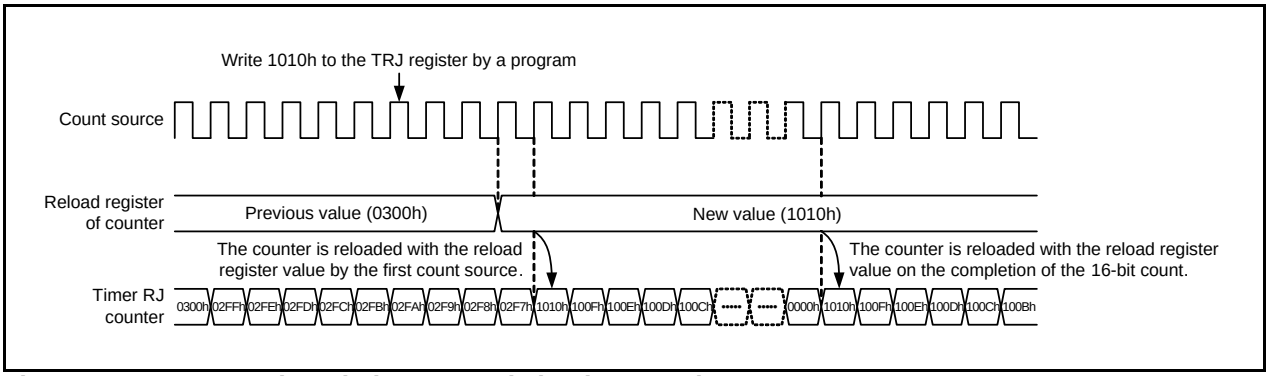


Figure 15.3 Operation Timing Example in Timer Mode

15.4.3 Pulse Output Mode

In this mode, the counter is decremented by the count source selected by bits TCK0 to TCK2 in the TRJMR register and a pulse is output from the TRJIO pin. The output level is inverted when an underflow occurs.
In pulse output mode, the count value is decremented by 1 each time the count source is input. If the next count source is input after the count value reaches 0000h, the set value in the reload register is loaded, and an underflow occurs, generating an interrupt.
In addition, a pulse can be output from pins TRJIO and TRJO. The output level is inverted each time an underflow occurs. The pulse output from the TRJIO pin can be stopped by the TOPCR bit in the TRJIOC register.
Also, the output level can be selected by the TEDGSEL bit in the TRJIOC register.
Figure 15.4 shows an Operation Timing Example in Pulse Output Mode when TEDGSEL Bit is 0.

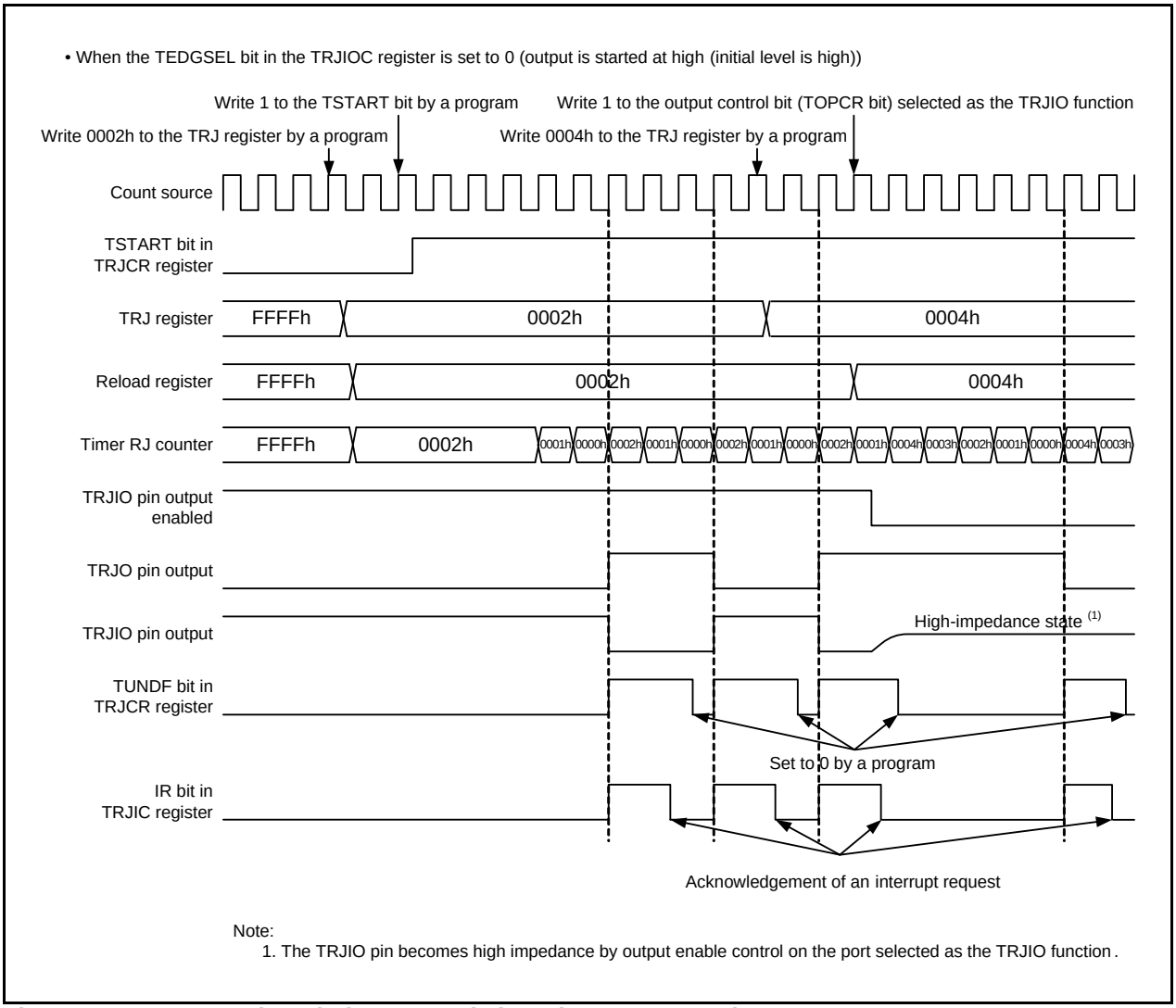


Figure 15.4 Operation Timing Example in Pulse Output Mode

15.4.4 Event Counter Mode

In this mode, the counter is decremented by an external pulse signal input to the TRJIO pin.
Various periods for counting events can be set by bits TIOGT0 and TIOGT1 in the TRJIOC register and the TRJISR register. In addition, the filter function for the TRJIO input can be specified by bits TIPF0 and TIPF1 in the TRJIOC register.
Also, the output from the TRJO pin can be toggled even in event counter mode.
When event counter mode is used, refer to **15.5 Notes on Timer RJ (3)**.
Figure 15.5 shows an Operation Timing Example in Event Counter Mode (1).

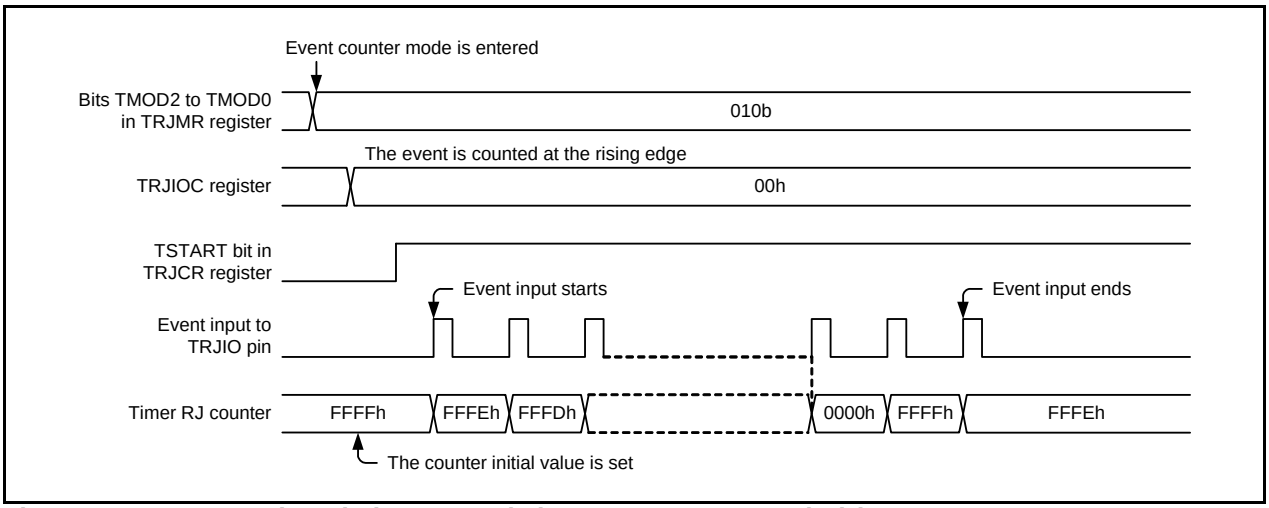


Figure 15.5 Operation Timing Example in Event Counter Mode (1)

Figure 15.6 shows an operation example for counting in event counter mode during the specified period (bits TIOGT1 and TIOGT0 in the TRJIOC register are set to 01b or 10b).

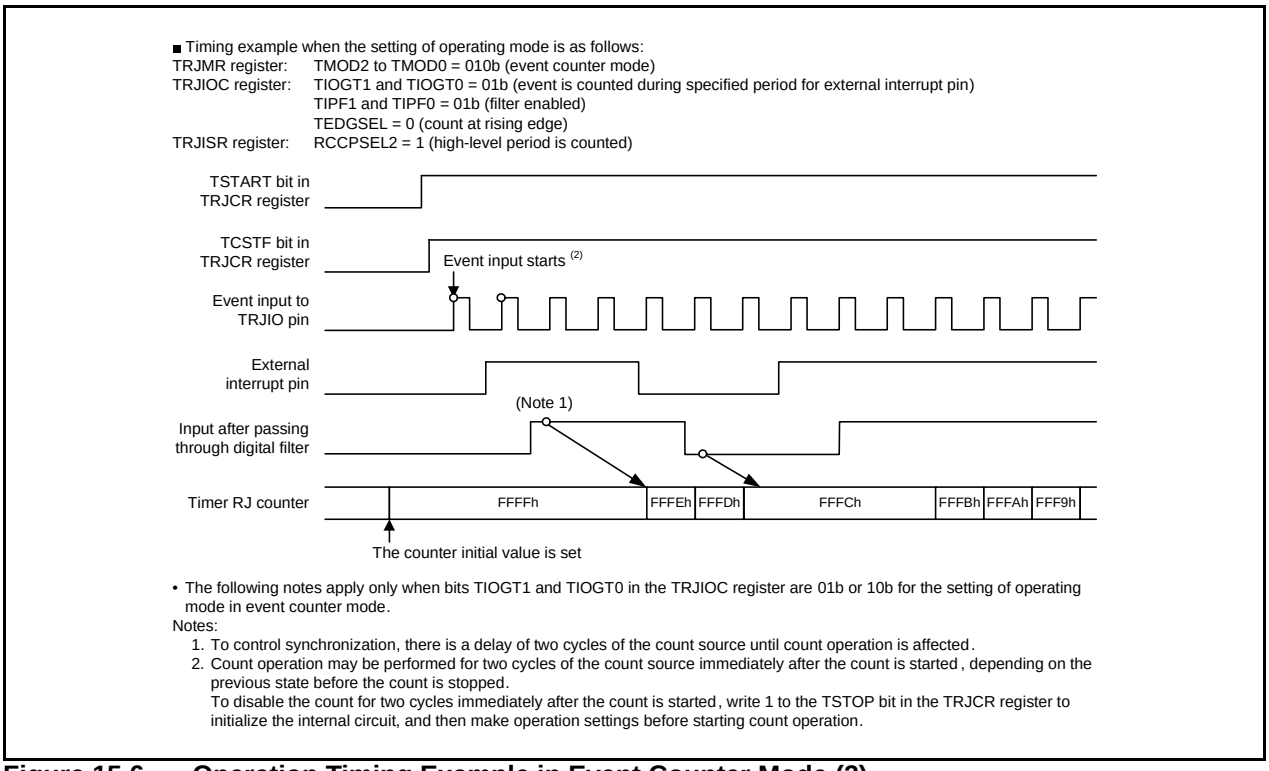


Figure 15.6 Operation Timing Example in Event Counter Mode (2)

Figure 15.6 shows an operation example during the specified period for the external interrupt pin, but the same timing also applies during the specified period for PWM input.

15.4.5 Pulse Width Measurement Mode

In this mode, the pulse width of an external signal input to the TRJIO pin is measured.
In pulse width measurement mode, when the level specified by the TEDGSEL bit in the TRJIOC register is input to the TRJIO pin, the decrement is started with the selected count source. When the specified level on the TRJIO pin ends, the counter is stopped, the TEDGF bit in the TRJCR register is set to 1 (active edge received) and an interrupt is generated. The measurement of pulse width data is performed by reading the count value while the counter is stopped. Also, when the counter underflows during measurement, the TUNDF bit in the TRJCR register is set to 1 (underflow) and an interrupt is generated.
Figure 15.7 shows an Operation Timing Example in Pulse Width Measurement Mode.
When accessing bits TEDGF and TUNDF in the TRJCR register, refer to **15.5 Notes on Timer RJ (4)**.

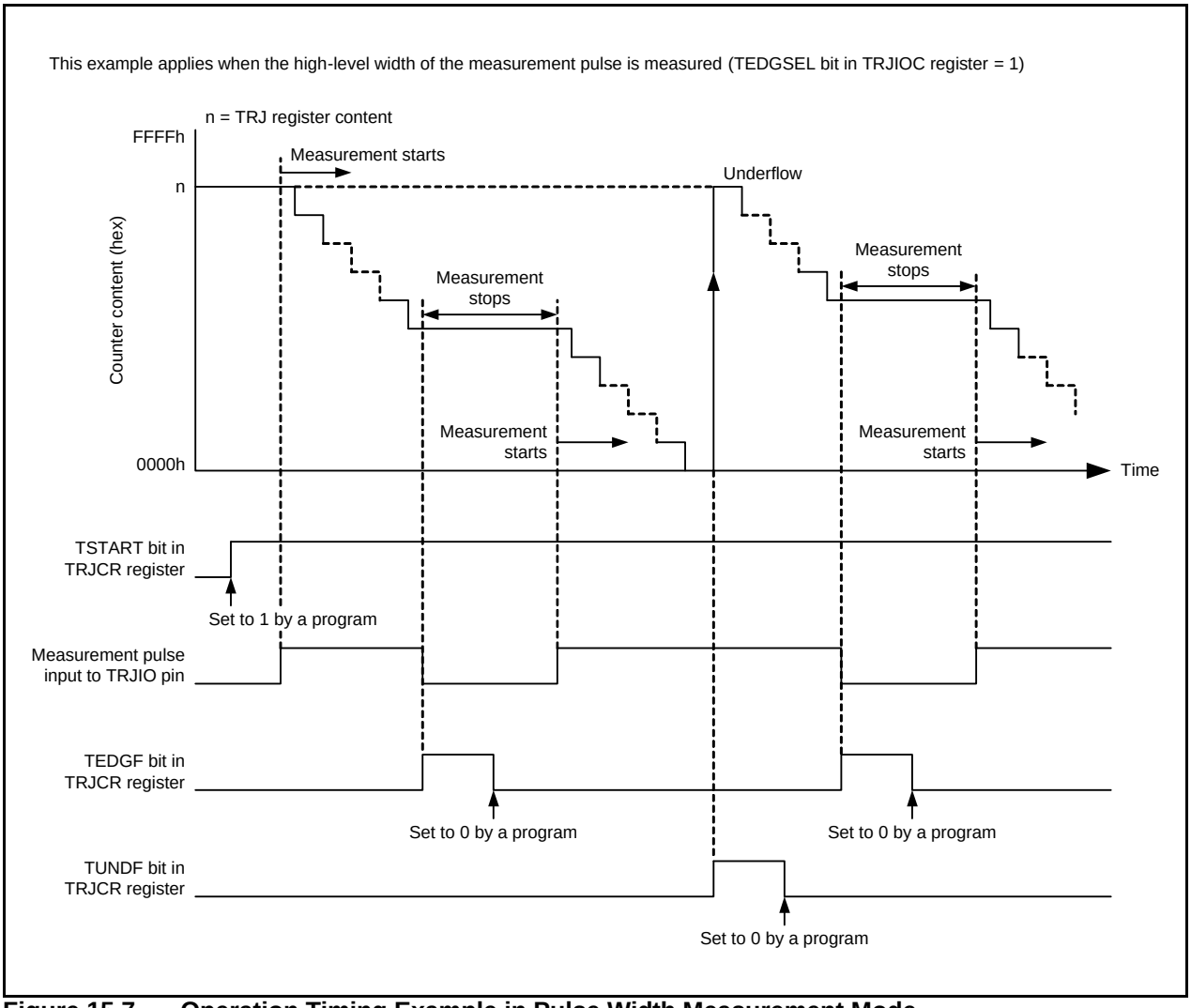
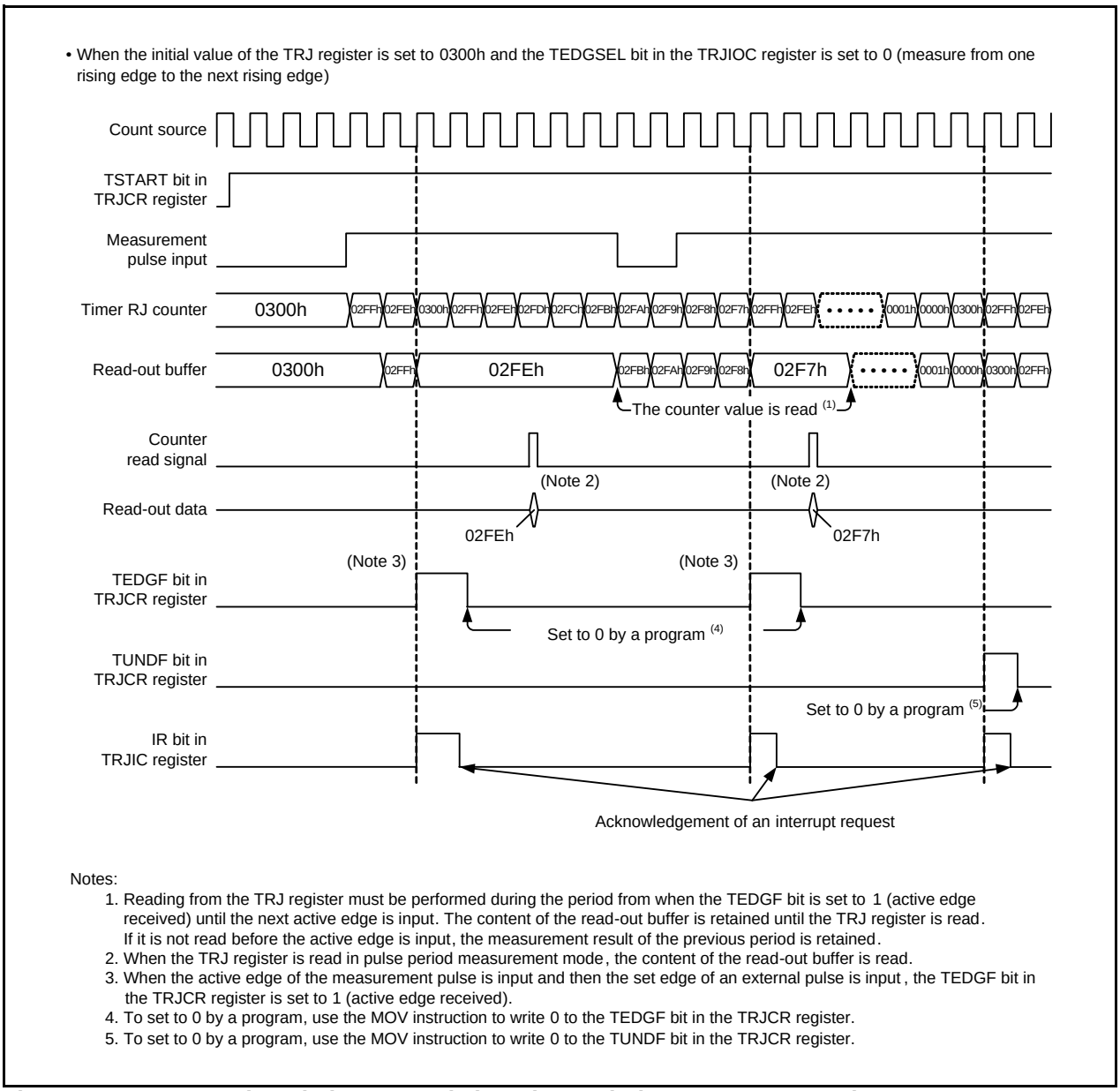


Figure 15.7 Operation Timing Example in Pulse Width Measurement Mode

15.4.6 Pulse Period Measurement Mode

In this mode, the pulse period of an external signal input to the TRJIO pin is measured.
The counter is decremented by the count source selected by bits TCK0 to TCK2 in the TRJMR register. When a pulse with the period specified by the TEDGSEL bit in the TRJIOC register is input to the TRJIO pin, the count value is transferred to the read-out buffer at the rising edge of the count source. The value of the reload register is loaded into the counter at the next rising edge. Simultaneously, the TEDGF bit in the TRJCR register is set to 1 (active edge received) and an interrupt is generated. The read-out buffer (TRJ register) is read at this time and the difference from the reload value is the period data of the input pulse. The period data is retained until the read-out buffer is read. When the counter underflows, the TUNDF bit in the TRJCR register is set to 1 (underflow) and an interrupt is generated.
Figure 15.8 shows an Operation Timing Example in Pulse Period Measurement Mode.
Only input pulses with a period longer than twice the period of the count source. Also, the low-level and high-level widths must both be longer than the period of the count source. If a pulse period shorter than these conditions is input, the input may be ignored.



Notes:
1. Reading from the TRJ register must be performed during the period from when the TEDGF bit is set to 1 (active edge received) until the next active edge is input. The content of the read-out buffer is retained until the TRJ register is read. If it is not read before the active edge is input, the measurement result of the previous period is retained.
2. When the TRJ register is read in pulse period measurement mode, the content of the read-out buffer is read.
3. When the active edge of the measurement pulse is input and then the set edge of an external pulse is input, the TEDGF bit in the TRJCR register is set to 1 (active edge received).
4. To set to 0 by a program, use the MOV instruction to write 0 to the TEDGF bit in the TRJCR register.
5. To set to 0 by a program, use the MOV instruction to write 0 to the TUNDF bit in the TRJCR register.

Figure 15.8 Operation Timing Example in Pulse Period Measurement Mode

15.4.7 Coordination with Event Link Controller (ELC)

Through coordination with the ELC, event input from the ELC can be set to be the counter count source. Bits TCK0 to TCK2 in the TRJMR register are used to count at the rising edge of event input from the ELC.
The ELC setting procedure is shown below:

• Procedure for starting operation

(1) Set the event output destination select register (ELSELRn) for the event link controller (ELC).
(2) Set the operating mode for the event generation source.
(3) Set the mode for timer RJ.
(4) Start the count operation of timer RJ.
(5) Start the operation of the event generation source.

• Procedure for stopping operation

(1) Stop the operation of the event generation source.
(2) Stop the count operation of timer RJ.
(3) Set the event output destination select register (ELSELRn) for the event link controller (ELC) to 0.

Refer to **15.5 Notes on Timer RJ (12)** for coordination with the ELC module.

15.4.8 I/O Settings for Each Mode

Tables 15.7 and 15.8 list the states of pins TRJO and TRJIO in each mode.

Table 15.7 TRJO Pin Setting (when TONEA Bit is Enabled) (1)

Operating Mode	TRJIOC Register		TRJO Pin Output
	TOENA Bit	TEDGSEL Bit	
All modes	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled

Note:
1. When setting TRJO and TRJIO as external pins, it is necessary to set registers TRJ_0SR and TRJ_1SR other than the timer RJ control register (shown above). Refer to **14. I/O Ports** for details.

Table 15.8 TRJIO Pin Setting (1)

Operating Mode	TRJIOC Register		TRJIO Pin I/O
	TOPCR Bit	TEDGSEL Bit	
Timer mode	0 or 1	0 or 1	Input
Pulse output mode	1	0 or 1	Output disabled
	0	1	Normal output
		0	Inverted output
Event counter mode	0 or 1	0 or 1	Input
Pulse width measurement mode			
Pulse period measurement mode			

Note:
1. When setting TRJO and TRJIO as external pins, it is necessary to set registers TRJ_0SR and TRJ_1SR other than the timer RJ control register (shown above). Refer to **14. I/O Ports** for details.

15.5 Notes on Timer RJ

(1) The timer count is stopped after a reset. Start the count only after setting the values of the registers associated timer RJ (1).
Note:
1. Registers associated with timer RJ: TRJCR, TRJIOC, TRJMR, TRJ, and TRJISR

(2) There are the following restrictions on register access while the count is stopped, depending on the timer mode:
• Event counter mode
After 1 (count starts) is written to the TSTART bit in the TRJCR register while the count is stopped, the TCSTF bit in the TRJCR register remains 0 (count stops) for two cycles of the CPU clock. Do not write to the TRJCR register until the TCSTF bit is set to 1. Also, do not access other registers associated with timer RJ (1). After the TCSTF bit is set to 1, the count is started from the first active edge of the count source.
After 0 (count stops) is written to the TSTART bit during a count operation, the TCSTF bit remains 1 for two cycles of the CPU clock. When the TCSTF bit is set to 0, the count is stopped. Do not write to the TRJCR register until the TCSTF bit is set to 0. Also, do not access other registers associated with timer RJ (1). Writing to the TRJ register has no effect until the TRJIO pin is set to the inactive level (low level when the TEDGSEL bit in the TRJIOC register is 0 and high level when this bit is 1). To change the TRJ register in this case, use the following procedure:
1. Write 0 to the TSTART bit to stop the count.
2. Wait until the TCSTF bit is set to 0.
3. Set bits TIPF1 and TIPF0 in the TRJIOC register to 00b (no filter). This setting is not necessary when no digital filter is used.
4. Write 1 and then write 0 to the TEDGSEL bit.
5. Set the TEDGSEL bit to the previous value (value before step 4).
Step 5 is not necessary if the value before step 4 is 0.
6. Set bits TIPF1 and TIPF0 to the previous value (value before step 3).
This step is not necessary when the digital filter is not used.
7. Access the TRJ register.

• Modes other than event counter mode
After 1 (count starts) is written to the TSTART bit while the count is stopped, the TCSTF bit remains 0 (count stops) for three cycles of the count source. Do not write to the TRJCR register until the TCSTF bit is set to 1. Also, do not access other registers associated with timer RJ (1). After the TCSTF bit is set to 1, the count is started at the first active edge of the counter source.
After 0 (count stops) is written to the TSTART bit during a count operation, the TCSTF bit remains 1 for three cycles of the count source. When the TCSTF bit is set to 0, the count is stopped. Do not write to the TRJCR register until the TCSTF bit is set to 0. Also, do not access other registers associated with timer RJ (1).

Note:
1. Registers associated with timer RJ: TRJIOC, TRJMR, TRJ, and TRJISR

(3) In event counter mode, set the TSTART bit in the TRJCR register to 1 (count starts), and then input an external pulse after the TCSTF bit is set to 1.

(4) In pulse width/pulse period measurement modes, bits TEDGF and TUNDF in the TRJCR register used are set to 0 by writing 0 by a program, but remain unchanged even if 1 is written to these bits. If a bit manipulation instruction is used to set the TRJCR register, bits TEDGF and TUNDF may be erroneously set to 0 depending on the timing, even when the TEDGF bit is set to 1 (active edge received) and the TUNDF bit is set to 1 (underflow) during execution of the instruction.
In order to avoid this, set bits TEDGF and TUNDF to 1 using the MOV instruction.

(5) Insert two NOP instructions between writing to and reading from registers associated with timer RJ (1) while the timer RJ count is stopped.

Note:
1. Registers associated with timer RJ: TRJCR, TRJIOC, TRJMR, TRJ, and TRJISR

(6) When the TSTART bit in the TRJCR register is 1 (count starts) and the TCSTF bit is 1 (count in progress), allow at least three cycles of the count source clock between writes when writing to the TRJ register successively.

(7) After changing to pulse width measurement mode or pulse period measurement mode from another mode, the values of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before starting timer RJ count.

(8) To lower current consumption, switch to module standby state when bits TSTART and TCSTF in TRJCR are 0 (count stops). For details on the bits for switching to module standby state, refer to **10.2.9 Module Standby Control Register 2 (MSTCR2)**.

(9) In pulse width measurement mode or pulse period measurement mode, perform settings in the following order:

1. Set the registers associated with timer RJ (1).
2. Set the TSTART bit to 1 (count starts) and then wait until the TCSTF bit is set to 1 (count is in progress).
3. Input an external event.

Note:

1. Registers associated with timer RJ: TRJCR, TRJIOC, TRJMR, TRJ, and TRJISR

(10) In pulse period measurement mode, the processing on completion of the first measurement is invalid (the measured value is valid for the second and subsequent times)

(11) The TRJ register must not be set to 0000h.

(12) In pulse width measurement mode and event counter mode, do not select an event from the event link controller (ELC) as the count source.

(13) In pulse output mode, set the TOPCR bit in the TRJIOC register after setting the TRJMR register.

(14) The registers associated with timer RJ operating mode (TRJIOC, TRJMR, and TRJISR) can be changed only when the count is stopped (both the TSTART and TCSTF bits in the TRJCR register are 0 (count stops)). Do not change these registers during count operation.

• Applicable: All modes of timer RJ

16. Timer RB2

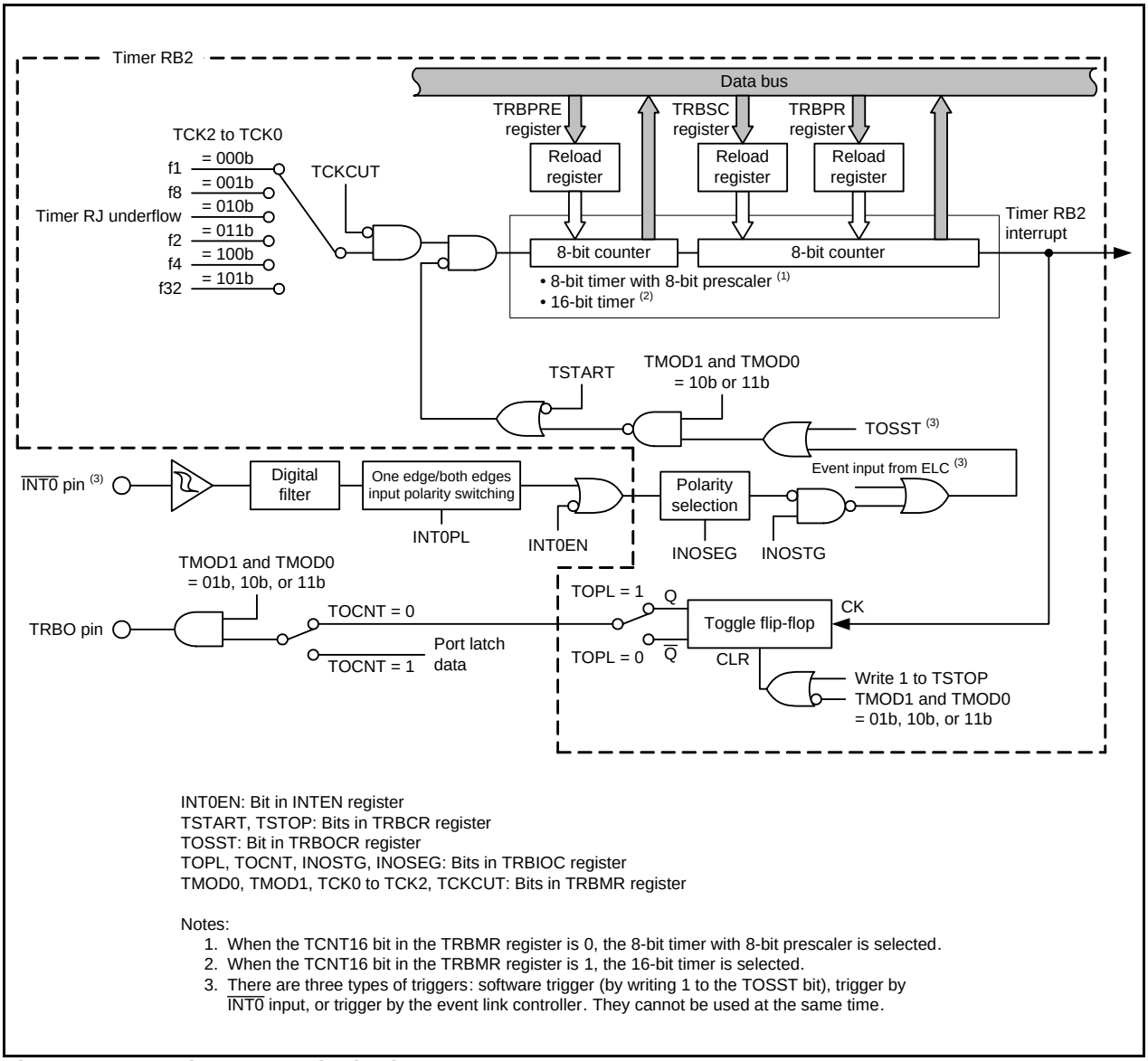
Timer RB2 can be used as an 8-bit timer with an 8-bit prescaler or as a 16-bit timer. The prescaler and timer each consist of a reload register and counter which are allocated to the same address. Timer RB2 has timer RB2 primary and timer RB2 secondary reload registers.

16.1 Overview

Table 16.1 lists the Timer RB2 Specifications and Figure 16.1 shows the Timer RB2 Block Diagram.

Table 16.1 Timer RB2 Specifications

Item		Description
Operating modes	Timer mode	An internal count source or timer RJ underflow is counted.
	Programmable waveform generation mode	An arbitrary pulse width is output successively.
	Programmable one-shot generation mode	A one-shot pulse is output.
	Programmable wait one-shot generation mode	A delayed one-shot pulse is output.
Count source		f1, f2, f4, f8, f32, or timer RJ underflow selectable
Interrupt		Timer RB2 underflow
Selectable function		• Coordination with the event link controller (ELC) Event input from the ELC can be used for timer RB2 one-shot start.



INT0EN: Bit in INTEN register
TSTART, TSTOP: Bits in TRBCR register
TOSST: Bit in TRBOCR register
TOPL, TOCNT, INOSTG, INOSEG: Bits in TRBIOC register
TMOD0, TMOD1, TCK0 to TCK2, TCKCUT: Bits in TRBMR register

Notes:
1. When the TCNT16 bit in the TRBMR register is 0, the 8-bit timer with 8-bit prescaler is selected.
2. When the TCNT16 bit in the TRBMR register is 1, the 16-bit timer is selected.
3. There are three types of triggers: software trigger (by writing 1 to the TOSST bit), trigger by INT0 input, or trigger by the event link controller. They cannot be used at the same time.

Figure 16.1 Timer RB2 Block Diagram

16.2 I/O Pins

Table 16.2 lists the Timer RB2 Pin Configuration.

Table 16.2 Timer RB2 Pin Configuration

Pin Name	I/O	Function
$\overline{\text{INT0}}$	Input	External trigger
TRBO	Output	Continuous pulse output or one-shot pulse output

For details on $\overline{\text{INT0}}$, refer to **11. Interrupts**. After a reset has been cleared, do not use the digital filter immediately after the setting is changed from 'no filter' to 'filter enabled' by setting the INTF register. Wait for four cycles of the sampling clock and then set the INOSTG bit in the TRBIOC register to 1 (one-shot trigger to $\overline{\text{INT0}}$ pin enabled).

16.3 Registers

Table 16.3 lists the Timer RB2 Register Configuration.

Table 16.3 Timer RB2 Register Configuration

Register Name	Symbol		After Reset	Address	Access Size
Timer RB2_0 Control Register	TRBCR_0		00h	00130h	8
Timer RB2_0 One-Shot Control Register	TRBOCR_0		00h	00131h	8
Timer RB2_0 I/O Control Register	TRBIOC_0		00h	00132h	8
Timer RB2_0 Mode Register	TRBMR_0		00h	00133h	8
8-bit timer with 8-bit prescaler: Timer RB2_0 Prescaler Register 16-bit timer: Timer RB2_0 Primary/Secondary Register (Lower 8 Bits)	8-bit timer: TRBPRE_0	16-bit timer: TRBPRSC_0	FFh	00134h	8-bit timer: 8 16-bit timer: 16 (1)
8-bit timer with 8-bit prescaler: Timer RB2_0 Primary Register 16-bit timer: Timer RB2_0 Primary Register (Higher 8 Bits)	8-bit timer: TRBPR_0		FFh	00135h	8-bit timer: 8 16-bit timer: 16 (1)
8-bit timer with 8-bit prescaler: Timer RB2_0 Secondary Register 16-bit timer (1): Timer RB2_0 Secondary Register (Higher 8 Bits)	TRBSC_0		FFh	00136h	8
Timer RB2_0 Interrupt Request Register	TRBIR_0		00h	00137h	8

Note:

1. While using the 16-bit timer, when accessing registers TRBPRE, TRBPR, and TRBSC in 8-bit units (8-bit access), always access TRBPRE, TRBPR, and TRBSC in that order.
   The configuration of the counter is shown below.
   - In timer mode and programmable one-shot generation mode
     The value of the TRBPR register is counted with the higher 8 bits and the value of TRBPRE register is counted with the lower 8 bits. The TRBSC register is not used.
   - In programmable waveform generation mode
     The values of registers TRBPR and TRBSC are counted alternately with the higher 8 bits and the value of the TRBPRE register is counted with the lower 8 bits.
   - In programmable wait one-shot generation mode
     As the wait time, the value of the TRBPR register is counted with the higher 8 bits and the value of the TRBPRE register is counted with the lower 8 bits.
     As the pulse width, the value of the TRBSC register is counted with the higher 8 bits and the value of the TRBPRE register is counted with the lower 8 bits.

16.3.1 Timer RB2 Control Register (TRBCR)

Address 00130h (TRBCR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TSTOP	TCSTF	TSTART
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RB2 count start bit (1)	0: Count stops 1: Count starts	R/W
b1	TCSTF	Timer RB2 count status flag (1)	0: Count stops 1: Count enabled	R
b2	TSTOP	Timer RB2 count forced stop bit (1, 2)	When 1 is written to this bit, the count is forcibly stopped. The read value is 0.	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. For notes on using bits TSTART, TCSTF, and TSTOP, refer to **16.8 Notes on Timer RB2**.
2. When 1 (count is forcibly stopped) is written to the TSTOP bit, the counter, registers TRBPRE, TRBPR, and TRBSC, bits TSTART and TCSTF, and bits TOSST, TOSSP, and TOSSTF in the TRBOCR register are initialized. The TRBO output is also initialized. For details on the initial state of the TRBO output, refer to **16.5.3 TOCNT Bit Setting and Pin States**.

TSTART Bit (Timer RB2 count start bit)

Count operation is started by writing 1 to the TSTART bit and stopped by writing 0. When the TSTART bit is set to 1 (count starts), the TCSTF bit is set to 1 (count in progress) in synchronization with the count source. Also, after 0 is written to the TSTART bit, the TCSTF bit is set to 0 (count stops) in synchronization with the count source. Do not access the registers associated with timer RB2 (1) until the TCSTF bit is set to 1 after the count is started, or until the TCSTF bit is set to 0 after the count is stopped. For details, refer to **16.8 Notes on Timer RB2**.

Note:
1. Registers associated with the timer RB2: TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBSC, and TRBPR

TCSTF Bit (Timer RB2 count status flag)

[Conditions for setting to 0]
- When 0 is written to the TSTART bit (the TCFTF bit is set to 0 in synchronization with the count source).
- When 1 is written to the TSTOP bit.

[Condition for setting to 1]
- When 1 is written to the TSTART bit (the TCFTF bit is set to 1 in synchronization with the count source).

16.3.2 Timer RB2 One-Shot Control Register (TRBOCR)

Address 00131h (TRBOCR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TOSSTF	TOSSP	TOSST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOSST	Timer RB2 one-shot start bit (1, 2)	When 1 is written to this bit, one-shot count starts. The read value is 0.	R/W
b1	TOSSP	Timer RB2 one-shot stop bit (2, 3)	When 1 is written to this bit, one-shot count stops. The read value is 0.	R/W
b2	TOSSTF	Timer RB2 one-shot status flag	0: One-shot is stopped 1: One-shot is operating (including wait period)	R
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. Verify that the TOSSTF bit is 0 (one-shot is stopped) before writing 1 (one-shot count starts) to the TOSST bit.
2. When 0 is written to this bit, the value is invalid.
3. Verify that the TOSSTF bit is 1 (one-shot is operating (including wait period)) before writing 1 (one-shot count stops) to the TOSSP bit.

The TRBOCR register is enabled when bits TMOD1 and TMOD0 in the TRBMR register are 10b (programmable one-shot generation mode) or 11b (programmable wait one-shot generation mode).

TOSSTF Bit (Timer RB2 one-shot status flag)

[Conditions for setting to 0]
- When the TSTOP bit in the TRBCR register is set to 1 (count is forcibly stopped).
- When the count value reaches 00h and is reloaded in programmable one-shot generation mode.
- When the secondary count value reaches 00h and is reloaded in programmable wait one-shot generation mode.
- After two or three cycles of the timer RB2 count source when the TOSSP bit is set to 1 (one-shot count stops).
- After two or three cycles of the timer RB2 count source when the TSTART bit in the TRBCR register is set to 0 (count stops) while timer RB2 is counting (TOSSTF = 1).

[Conditions for setting to 1]
- After three cycles of the timer RB2 count source when the TOSST bit is set to 1 (one-shot count starts) while the TCSTF bit is 1 (count enabled).
- After three cycles of the timer RB2 count source when a trigger is input while the TCSTF bit is 1 (count enabled).

16.3.3 Timer RB2 I/O Control Register (TRBIOC)

Address 00132h (TRBIOC_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB2 output level select bit	Refer to **Table 16.4 Functions of Timer RB2 Output Level Select Bit**.	R/W
b1	TOCNT	Timer RB2 output switch bit	0: Waveform output 1: Fixed-value output	R/W
b2	INOSTG	One-shot trigger control bit	0: One-shot trigger to $\overline{\text{INT0}}$ pin disabled 1: One-shot trigger to INT0 pin enabled	R/W
b3	INOSEG	One-shot trigger polarity select bit	0: Falling edge 1: Rising edge	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

TOCNT Bit (Timer RB2 output switch bit)

The setting of the TOCNT bit is valid only in programmable waveform, programmable one-shot, and programmable wait one-shot generation modes.

For details on the change in the states of the TRBO output in each mode, refer to **16.5.3 TOCNT Bit Setting and Pin States**.

Table 16.4 Functions of Timer RB2 Output Level Select Bit

Operating Mode	Function	
Timer mode	Set to 0 in timer mode.	
Programmable waveform generation mode	0	High output during primary period Low output during secondary period Low output at timer stop
	1	Low output during primary period High output during secondary period High output at timer stop
Programmable one-shot generation mode	0	High one-shot pulse output Low output at timer stop
	1	Low one-shot pulse output High output at timer stop
Programmable wait one-shot generation mode	0	High one-shot pulse output Low output at timer stop and during wait period
	1	Low one-shot pulse output High output at timer stop and during wait period

16.3.4 Timer RB2 Mode Register (TRBMR)

Address 00133h (TRBMR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	TCK2	TCK1	TCK0	TWRC	TCNT16	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RB2 operating mode select bits (1)	b1 b0 0 0: Timer mode 0 1: Programmable waveform generation mode 1 0: Programmable one-shot generation mode 1 1: Programmable wait one-shot generation mode	R/W
b1	TMOD1			R/W
b2	TCNT16	Timer RB2 counter select bit (1)	0: 8-bit timer with 8-bit prescaler 1: 16-bit timer	R/W
b3	TWRC	Timer RB2 write control bit (2)	0: Write to reload register and counter 1: Write to reload register only	R/W
b4	TCK0	Timer RB2 count source select bits (1)	b6 b5 b4 0 0 0: f1 0 0 1: f8 0 1 0: Timer RJ underflow 0 1 1: f2 1 0 0: f4 1 0 1: f32 Other than the above: Do not set.	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	TCKCUT	Timer RB2 count source cutoff bit (1)	0: Count source is supplied 1: Count source is cut off	R/W

Notes:
1. Only change these bits when bits TSTART and TCSTF in TRBCR register are 0 (count stops).
2. For details on writing to the register and counter using the TWRC bit, refer to **16.5.2 Prescaler and Counter Operation Using TWRC Bit**.
   The TWRC bit can be selected as 0 or 1 in timer mode. In programmable waveform, programmable one-shot, and programmable wait one-shot generation modes, set this bit to 1 (write to reload register only).

16.3.5 Timer RB2 Prescaler Register (TRBPRE)

Address 00134h (TRBPRE_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Initial Value	Setting Range	R/W
b7 to b0	Timer mode	An internal count source or the timer RJ underflow is counted.	FFh	00h to FFh	R/W
	Programmable waveform generation mode		FFh	00h to FFh	R/W
	Programmable one-shot generation mode		FFh	00h to FFh	R/W
	Programmable wait one-shot generation mode		FFh	00h to FFh	R/W

In the 8-bit timer with 8-bit prescaler, the 8-bit TRBPRE register is used to set the period of the prescaler. Each time the prescaler decrements and underflows, the value of the TRBPRE register is reloaded. When read, the value is read from the prescaler.

In the 16-bit timer, the TRBPRE register is used to set the lower 8 bits of the 16-bit counter. Each time the counter decrements and underflows, the value of the TRBPRE register is reloaded. When read, the value is read from the lower 8 bits of the counter. When accessing registers TRBPRE, TRBPR, and TRBSC in 8-bit units (8-bit access), always access TRBPRE, TRBPR, and TRBSC in that order.

The TRBPRE register is configured with a master – reload register structure, so the reload register is written simultaneously while the count is stopped. During the counter operation, the timing for updating the reload register differs in each mode. For details, refer to **Table 16.6 Reload Register Update Timing for Registers TRBPR and TRBSC in 8-Bit Timer with 8-Bit Prescaler**, and **Table 16.7 Reload Register Update Timing for Registers TRBPRE, TRBPR, and TRBSC in 16-Bit Timer**. The value is updated in synchronization with the count source.

If 1 (count is forcibly stopped) is written to the TSTOP bit in the TRBCR register, the TRBPRE register is initialized (FFh).

16.3.6 Timer RB2 Primary Register (TRBPR)

Address 00135h (TRBPR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function		Initial Value	Setting Range	R/W
		8-Bit Timer with 8-Bit Prescaler	16-Bit Timer			
b7 to b0	Timer mode	Timer RB2 prescaler underflow is counted.	Timer RB prescaler underflow is counted.	FFh	00h to FFh	R/W
	Programmable waveform generation mode	Timer RB2 prescaler underflow is counted. (1)		FFh	00h to FFh	R/W
	Programmable one-shot generation mode	Timer RB2 prescaler underflow is counted (one-shot width is counted).		FFh	00h to FFh	R/W
	Programmable wait one-shot generation mode	Timer RB2 prescaler underflow is counted (wait period is counted).		FFh	00h to FFh	R/W

Note:
1. The values in registers TRBPR and TRBSC are reloaded and counted alternately.

In the 8-bit timer with 8-bit prescaler, use the following procedure when writing to the TRBSC register.
(1) Write a value to the TRBSC register.
(2) Write a value to TRBPR register (write the same value as the previous one again even if the value is not changed).

In the 16-bit timer, use the following procedure when writing to the TRBSC register.
(1) Write values to registers TRBPRE and TRBSC.
(2) Write a value to TRBPR register (write the same value as the previous one again even if the value is not changed).

In the 8-bit timer with 8-bit prescaler, the 8-bit TRBPR register is used to set the period of the counter and the primary period. When read, the value is read from the 8-bit counter.

In the 16-bit timer, the 8-bit TRBPR register is used to set the period of the higher 8-bit counter and the primary period. When read, the value is read from the higher 8 bits of the 16-bit timer. Access the TRBPRE register and then the TRBPR register.

The TRBPR register is configured with a master – reload register structure, so the reload register is written simultaneously while the count is stopped. During the counter operation, the timing for updating the reload register differs in each mode. For details, refer to **Table 16.6 Reload Register Update Timing for Registers TRBPR and TRBSC in 8-Bit Timer with 8-Bit Prescaler**, and **Table 16.7 Reload Register Update Timing for Registers TRBPRE, TRBPR, and TRBSC in 16-Bit Timer**.

If 1 (count is forcibly stopped) is written to the TSTOP bit in the TRBCR register, the TRBPR register is initialized (FFh).

16.3.7 Timer RB2 Secondary Register (TRBSC)

Address 00136h (TRBSC_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function		Initial Value	Setting Range	R/W
		8-Bit Timer with 8-Bit Prescaler	16-Bit Timer			
b7 to b0	Timer mode	Disabled		FFh	Invalid	—
	Programmable waveform generation mode	Timer RB2 prescaler underflow	Timer RB prescaler underflow is counted. (1)	FFh	00h to FFh	R/W
	Programmable one-shot generation mode	Disabled		FFh	Invalid	—
	Programmable wait one-shot generation mode	Timer RB2 prescaler underflow	Timer RB prescaler underflow is counted. (1)	FFh	00h to FFh	R/W

Note:
1. The values in registers TRBPR and TRBSC are reloaded and counted alternately. The count value can be read from the TRBPR register while the secondary period is counted.

In the 8-bit timer with 8-bit prescaler, the 8-bit TRBSC register is used to set the secondary period used in programmable waveform and programmable wait one-shot generation modes. When read, the value is read from the reload register.

In the 16-bit timer, the 8-bit TRBSC register is used to set the higher 8-bit secondary period used in programmable waveform and programmable wait one-shot generation modes. This setting can be made in timer mode and programmable one-shot generation mode, but it is not used for counter operation. When read, the value is read from the reload register.

The TRBSC register is configured with a master – reload register structure, so the reload register is written simultaneously while the count is stopped. During the counter operation, the timing for updating the reload register differs in each mode. For details, refer to **Table 16.6 Reload Register Update Timing for Registers TRBPR and TRBSC in 8-Bit Timer with 8-Bit Prescaler**, and **Table 16.7 Reload Register Update Timing for Registers TRBPRE, TRBPR, and TRBSC in 16-Bit Timer**.

If 1 (count is forcibly stopped) is written to the TSTOP bit in the TRBCR register, the TRBSC register is initialized (FFh).

16.3.8 Timer RB2 Interrupt Request Register (TRBIR)

Address 00137h (TRBIR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRBIE	TRBIF	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	TRBIF	Timer RB2 interrupt request flag	0: No interrupt requested 1: Interrupt requested	R/W
b7	TRBIE	Timer RB2 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	R/W

TRBIF Bit (Timer RB2 interrupt request flag)

[Conditions for setting to 0]
- When 0 is written to this bit after reading it as 1.
- When an interrupt from the DTC is automatically cleared.
- When a jump is made to the interrupt routine (an interrupt is acknowledged by the CPU).

[Condition for setting to 1]
- Refer to **Table 16.5 Conditions for Setting TRBIF Bit to 1**.

Table 16.5 Conditions for Setting TRBIF Bit to 1

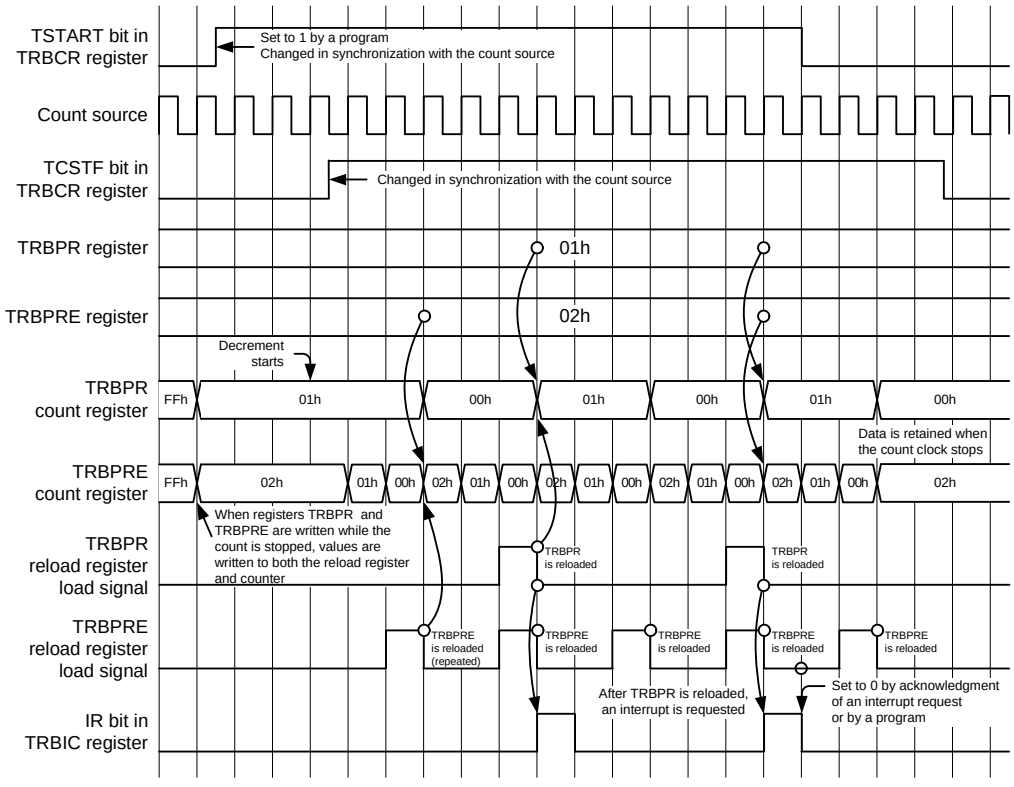
Operating Mode	Condition
Timer mode	When the timer RB2 counter underflows.
Programmable waveform generation mode	When timer RB2 counter underflows during the secondary period.
Programmable one-shot generation mode	When the timer RB2 counter underflows.
Programmable wait one-shot generation mode	When timer RB2 counter underflows during the secondary period.

16.4 Operation

16.4.1 Timer Mode

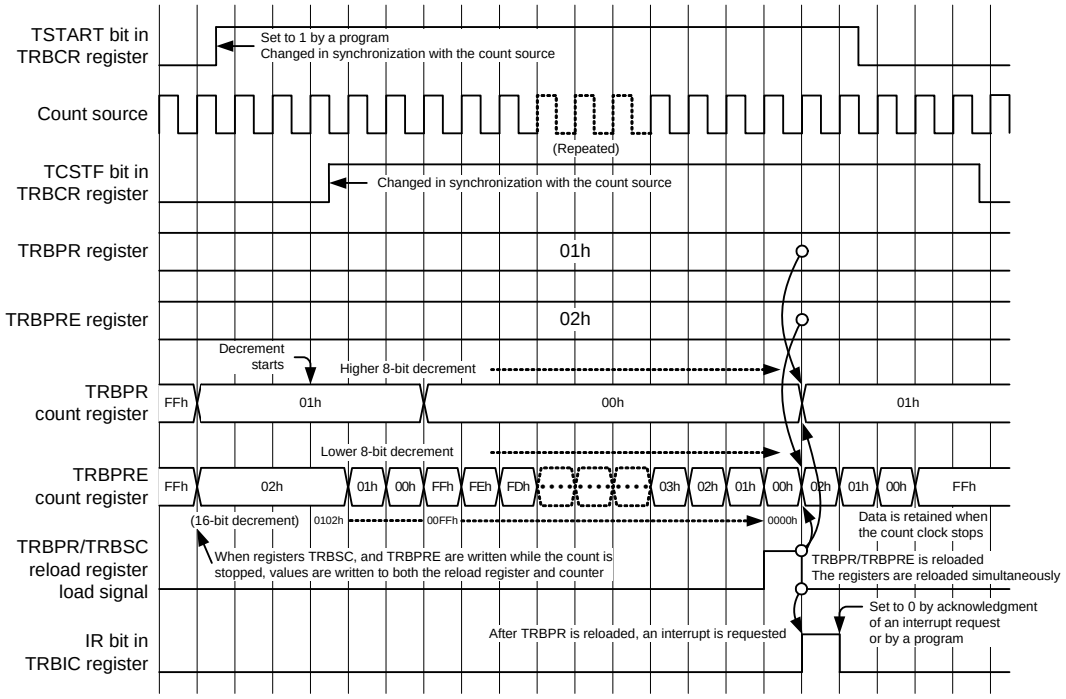
In this mode, an internally generated count source or the timer RJ underflow is counted. Registers TRBOCR and TRBSC are not used.
When 1 (count starts) is written to the TSTART bit in the TRBCR register, the count is started. When 0 (count stops) is written to the TSTART bit, the count is stopped. When 1 (count is forcibly stopped) is written to the TSTOP bit in the TRBCR register, the count is stopped.
An interrupt request is generated when the timer RB2 counter underflows.
When registers TRBPRE and TRBPR are read, each count value can be read. When registers TRBPRE and TRBPR are written while the count is stopped, values are written to both the reload register and counter, respectively. When these registers are written during count operation, the reload register is written. A program can be used to select whether values are transferred to the counter at the next count operation, or written to the reload register only and then transferred to the counter at the next reload operation.
Figures 16.2 and 16.3 show Operation Examples in Timer Mode.

Note:
1. The count is started after three cycles of the count source when the TSTART bit is set to 1 (count starts). The count is stopped after two or three cycles of the count source when the TSTART bit is set to 0 (count stops).
   Monitor the TCSTF bit in the TRBCR register to confirm the operating state of the counter.



The above diagram applies under the following conditions:
- TRBPRE register = 02h, TRBPR register = 01h
- TCNT16 bit in TRBMR register = 0 (8-bit timer with 8-bit prescaler)
- TOCNT bit in TRBIOC register = 0 (waveform output)

Figure 16.2 Operation Example in Timer Mode (8-Bit Timer)



The above diagram applies under the following conditions:
- TRBPRSC register = 0102h
- TCNT16 bit in TRBMR register = 1 (16-bit timer)
- TOCNT bit in TRBIOC register = 0 (waveform output)

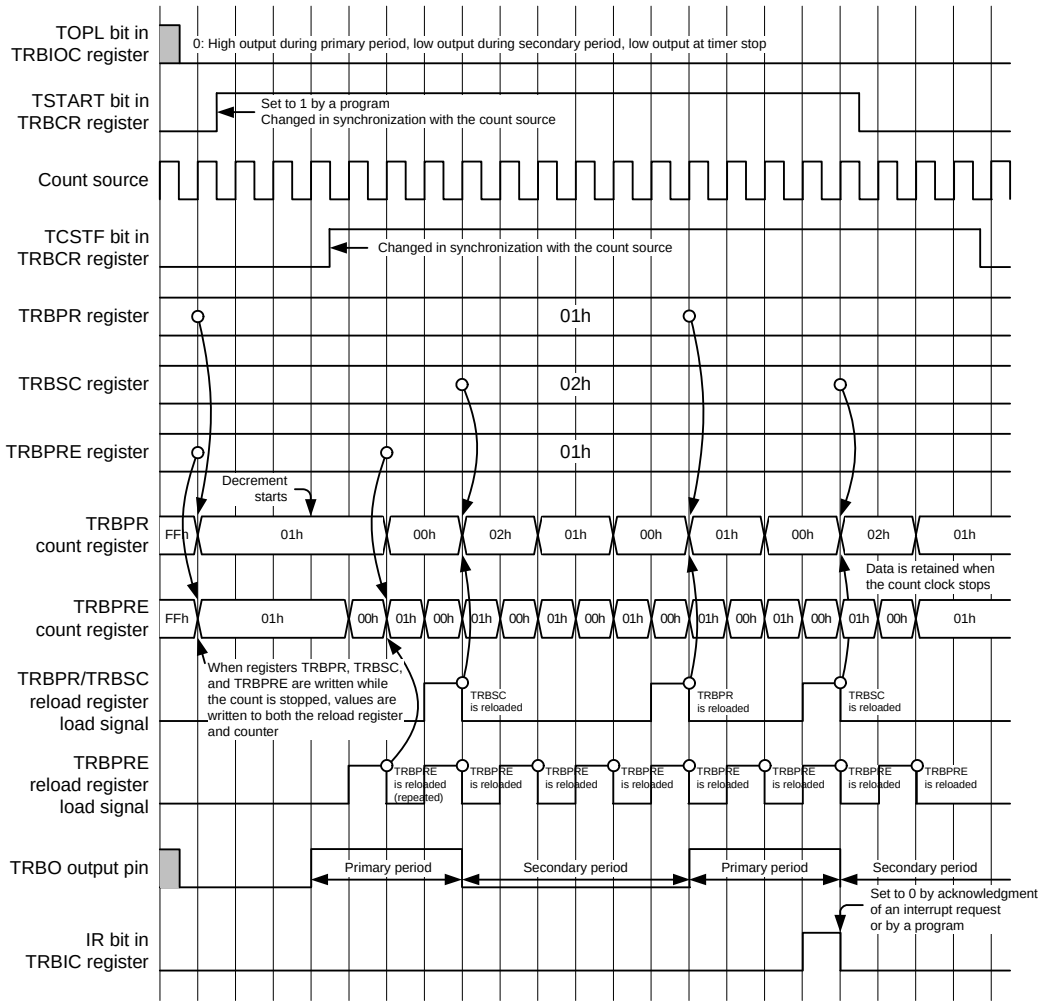
Figure 16.3 Operation Example in Timer Mode (16-Bit Timer)

16.4.2 Programmable Waveform Generation Mode

In the 8-bit timer with 8-bit prescaler, registers TRBPR and TRBSC are switched alternately each time the timer RB2 counter underflows.
In the 16-bit timer, the primary and secondary periods are switched alternately each time the 16-bit counter underflows. The 16-bit counter for the primary period consists of the higher 8 bits in the TRBPR register and the lower 8 bits in the TRBPRE register. The 16-bit counter for the secondary period consists of the higher 8 bits in the TRBSC register and the lower 8 bits in the TRBPRE register.
The TRBO pin outputs an inverted waveform each time the counter underflows. The count is started from the primary period. In programmable waveform generation mode, the TRBOCR register is not used.
When 1 (count starts) is written to the TSTART bit in the TRBCR register, the count is started. When 0 (count stops) is written to the TSTART bit, the count is stopped. When 1 (count is forcibly stopped) is written to the TSTOP bit in the TRBCR register, the count is stopped.
An interrupt request is generated when the timer RB2 counter underflows during the secondary period.
When registers TRBPRE and TRBPR are read, each count value can be read. Read the TRBPR register even while the secondary period is counted. When registers TRBPRE, TRBPR, and TRBSC are written while the count is stopped, values are written to both the reload register and counter, respectively. When these registers are written during count operation, values are written to the reload register and then transferred to the counter at the next reload operation.
Figure 16.4 shows an Example of 8-Bit Timer with 8-Bit Prescaler Operation in Programmable Waveform Generation Mode. Figure 16.5 shows an Example of 16-Bit Timer Operation in Programmable Waveform Generation Mode.

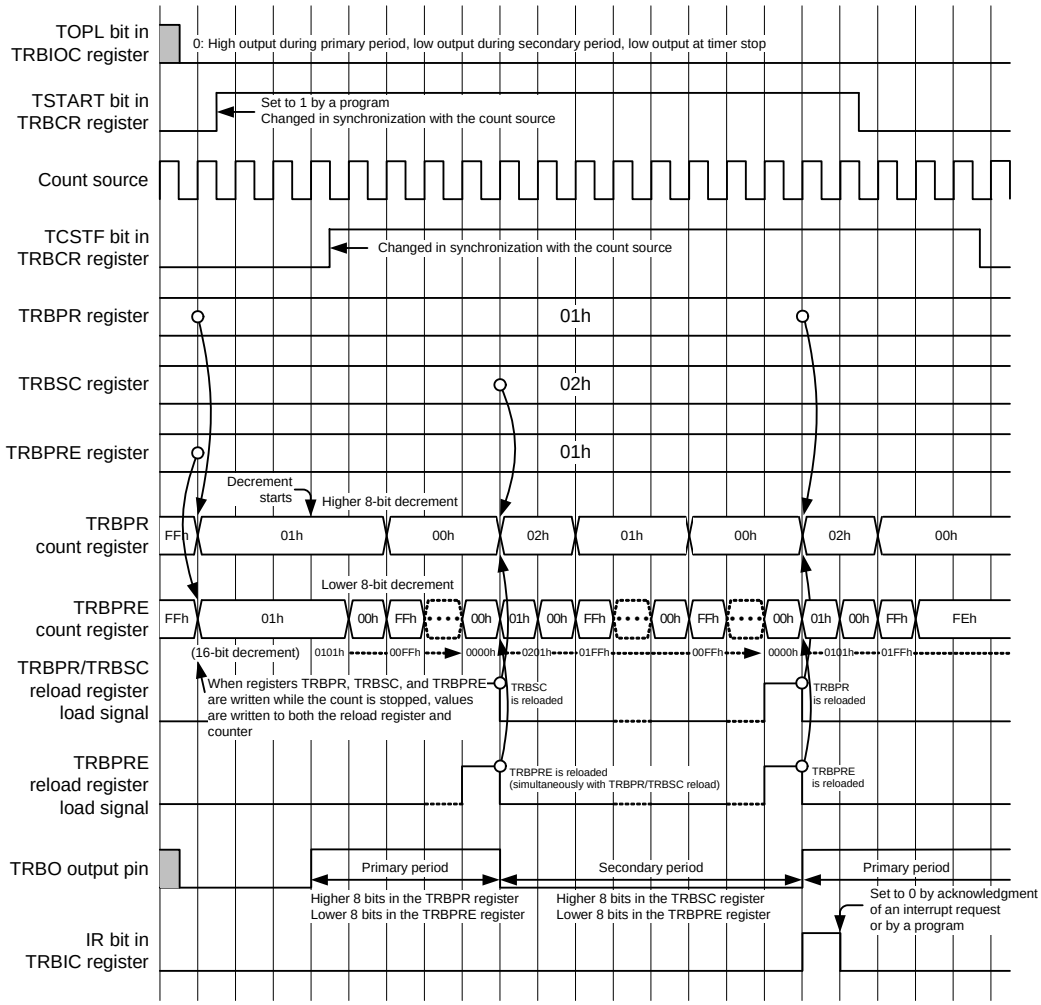
Note:

1. • The count is started after three cycles of the count source when the TSTART bit is set to 1 (count starts). The count is stopped after two or three cycles of the count source when the TSTART bit is set to 0 (count stops).
   Monitor the TCSTF bit in the TRBCR register to confirm the operating state of the counter.
   • Monitor the TCSTF bit in the TRBCR register to confirm the actual state of counter operation.
   • During 16-bit timer operation, the lower 8 bits for both primary and secondary periods are set by the same TRBPRE register, so theses bits are always set to the same value in one cycle. Therefore, even if an attempt is made to change only the pulse width of a PWM waveform without changing the period, PWM control cannot be performed at fine resolution because only the higher 8 bits can be set.



The above diagram applies under the following conditions:
- TRBPRE register = 01h, TRBPR register = 01h, TRBSC register = 02h
- TCNT16 bit in TRBMR register = 0 (8-bit timer with 8-bit prescaler)
- TOPL bit = 0 (high output during primary period, low output during secondary period, low output at timer stop), TOCNT bit = 0 (waveform output) in TRBIOC register
- TRBIE bit in TRBIR register = 1 (timer RB2 interrupt enabled)

Figure 16.4 Example of 8-Bit Timer with 8-Bit Prescaler Operation in Programmable Waveform Generation Mode



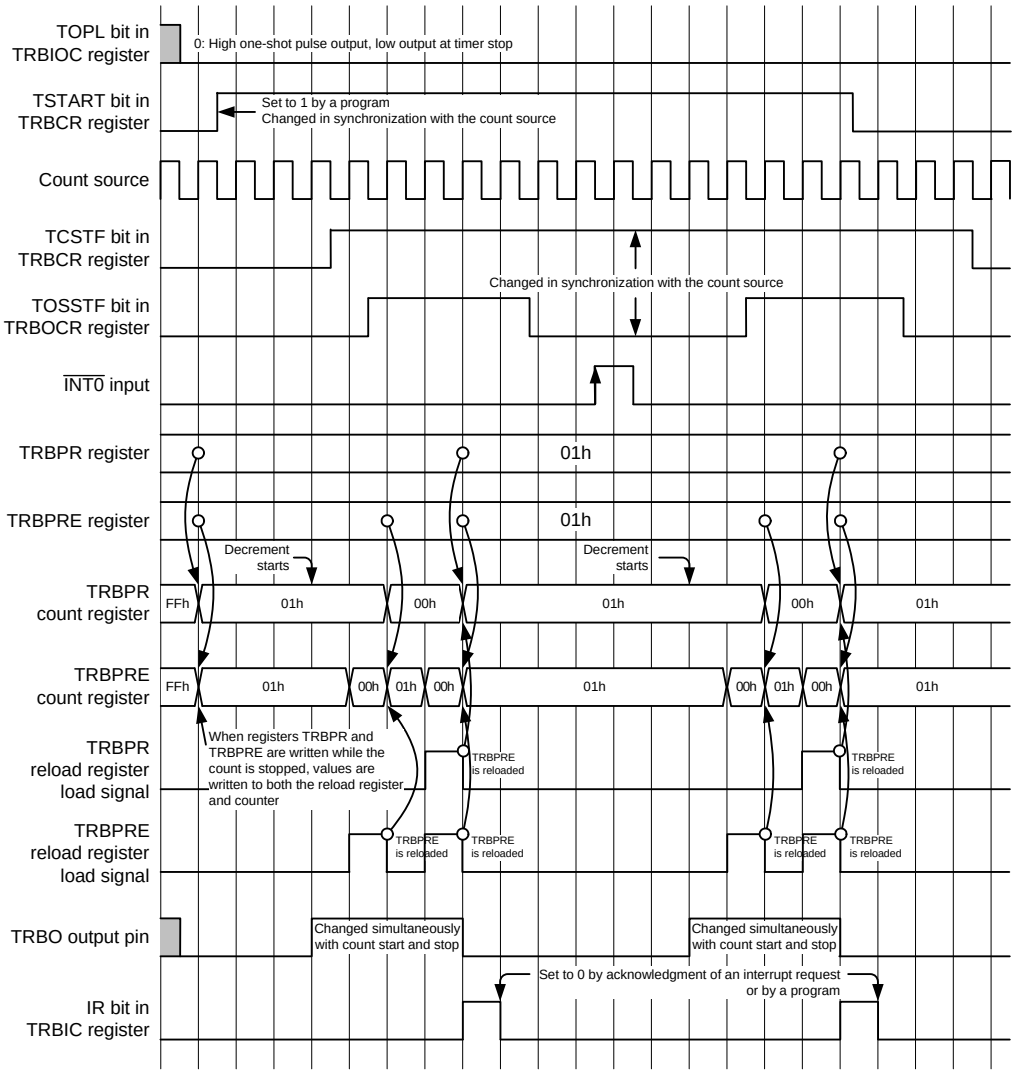
The above diagram applies under the following conditions:
- TRBPRSC register = 0101h, TRBSC register = 02h
- TCNT16 bit in TRBMR register = 1 (16-bit timer)
- TOPL bit = 0 (high output during primary period, low output during secondary period, low output at timer stop), TOCNT bit = 0 (waveform output) in TRBIOC register
- TRBIE bit in TRBIR register = 1 (timer RB2 interrupt enabled)

Figure 16.5 Example of 16-Bit Timer Operation in Programmable Waveform Generation Mode

16.4.3 Programmable One-Shot Generation Mode

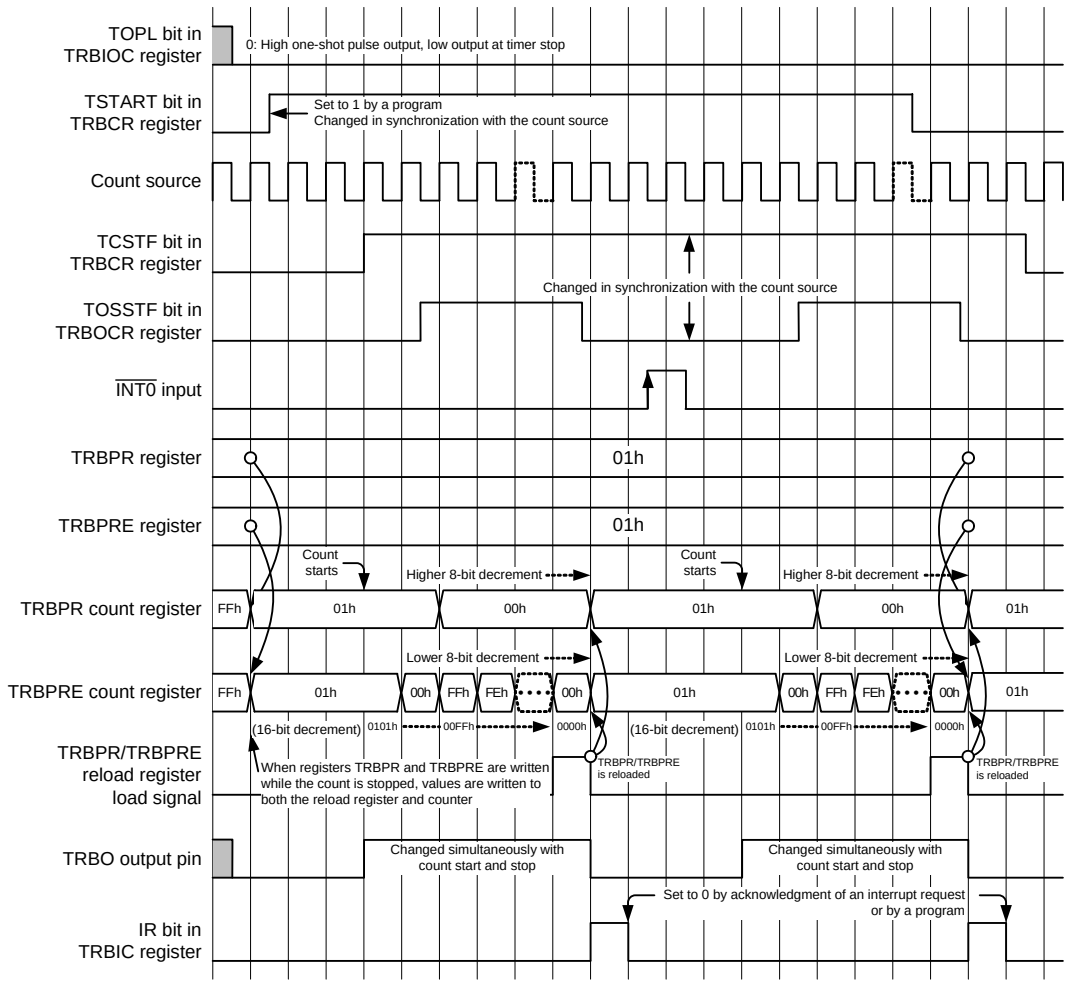
In this mode, a one-shot pulse is output from the TRBO pin by a program, external trigger input ($\overline{\text{INT0}}$), or event input from the event link controller (ELC). When a trigger is generated from that point, the timer operates only once to count a given length of the time equal to the setting value of the TRBPR register.
In the 8-bit timer with 8-bit prescaler, the count value is set in the TRBPR register.
In the 16-bit timer, the count value of the higher 8 bits is set in the TRBPR register and that of the lower 8 bits is set in the TRBPRE register.
In programmable one-shot generation mode, the TRBSC register is not used.
When 1 (one-shot count starts) is written to the TOSST bit in the TRBOCR register while the TCSTF bit in the TRBCR register is 1 (count enabled), the count is started. If a valid trigger is input to the $\overline{\text{INT0}}$ pin while the TCSTF bit is 1, the count is started. The count is also started by event input from the ELC while the TCSTF bit is 1. When the count value underflows and then it is reloaded, the count is stopped. The count is also stopped by any of the following settings:
• When 1 (one-shot count stops) is written to the TOSSP bit in the TRBOCR register, the count is stopped.
• When 0 (count stops) is written to the TSTART bit in the TRBCR register, the count is stopped.
• When 1 (count is forcibly stopped) is written to the TSTOP bit in the TRBCR register, the count is stopped.
An interrupt request is generated when the timer RB2 counter underflows.
When registers TRBPRE and TRBPR are read, each count value can be read. When registers TRBPRE and TRBPR are written while the count is stopped, values are written to both the reload register and counter, respectively. When these registers are written during count operation, values are written to the reload register and then transferred to the counter at the next reload operation.
For the setting of trigger by the $\overline{\text{INT0}}$ input, refer to **16.7 INT0 Input Trigger Selection**.
Operation of timer RB2 is not affected even if a one-shot trigger is generated while the TOSSTF bit is 1, but the IR bit in the INT0IC register is changed.
Figure 16.6 shows an Example of 8-Bit Timer with 8-Bit Prescaler Operation in Programmable One-Shot Generation Mode. Figure 16.7 shows an Example of 16-Bit Timer Operation in Programmable One-Shot Generation Mode.

Note:
1. After 1 is written to bits TOSST and TOSSP, a valid trigger is input to the $\overline{\text{INT0}}$ pin, event input from the event link controller (ELC), or 0 is written to the TSTART bit, settings are reflected in the counter operation after three cycles of the count source.
   Monitor the TOSSTF bit in the TRBOCR register to confirm the operating state of the counter.



The above diagram applies under the following conditions:
- TRBPRE register = 01h, TRBPR register = 01h
- TCNT16 bit in TRBMR register = 0 (8-bit timer with 8-bit prescaler)
- TOPL bit = 0 (high one-shot pulse output, low output at timer stop), TOCNT bit = 0 (waveform output), INOSTG bit = 1 (one-shot trigger to $\overline{\text{INT0}}$ pin enabled), INOSEG bit = 1 (rising edge) in TRBIOC register
- TRBIE bit in TRBIR register = 1 (timer RB2 interrupt enabled)

Figure 16.6 Example of 8-Bit Timer with 8-Bit Prescaler Operation in Programmable One-Shot Generation Mode



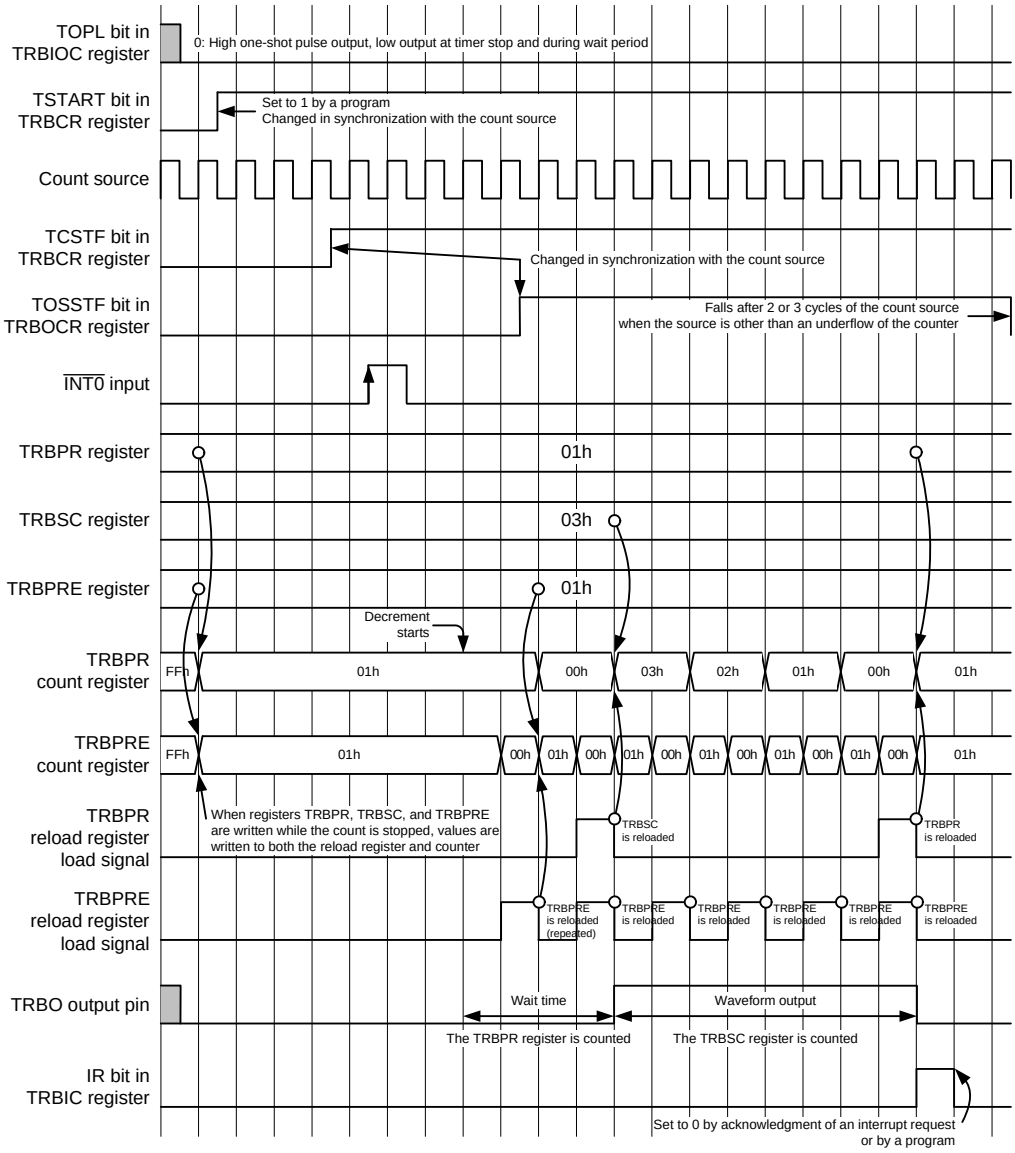
The above diagram applies under the following conditions:
- TRBPRSC register = 0101h
- TCNT16 bit in TRBMR register = 1 (16-bit timer)
- TOPL bit = 0 (high one-shot pulse output, low output at timer stop),
  TOCNT bit = 0 (waveform output), INOSTG bit = 1 (one-shot trigger to $\overline{\text{INT0}}$ pin enabled),
  INOSEG bit = 1 (rising edge) in TRBIOC register
- TRBIE bit in TRBIR register = 1 (timer RB2 interrupt enabled)

Figure 16.7 Example of 16-Bit Timer Operation in Programmable One-Shot Generation Mode

16.4.4 Programmable Wait One-Shot Generation Mode

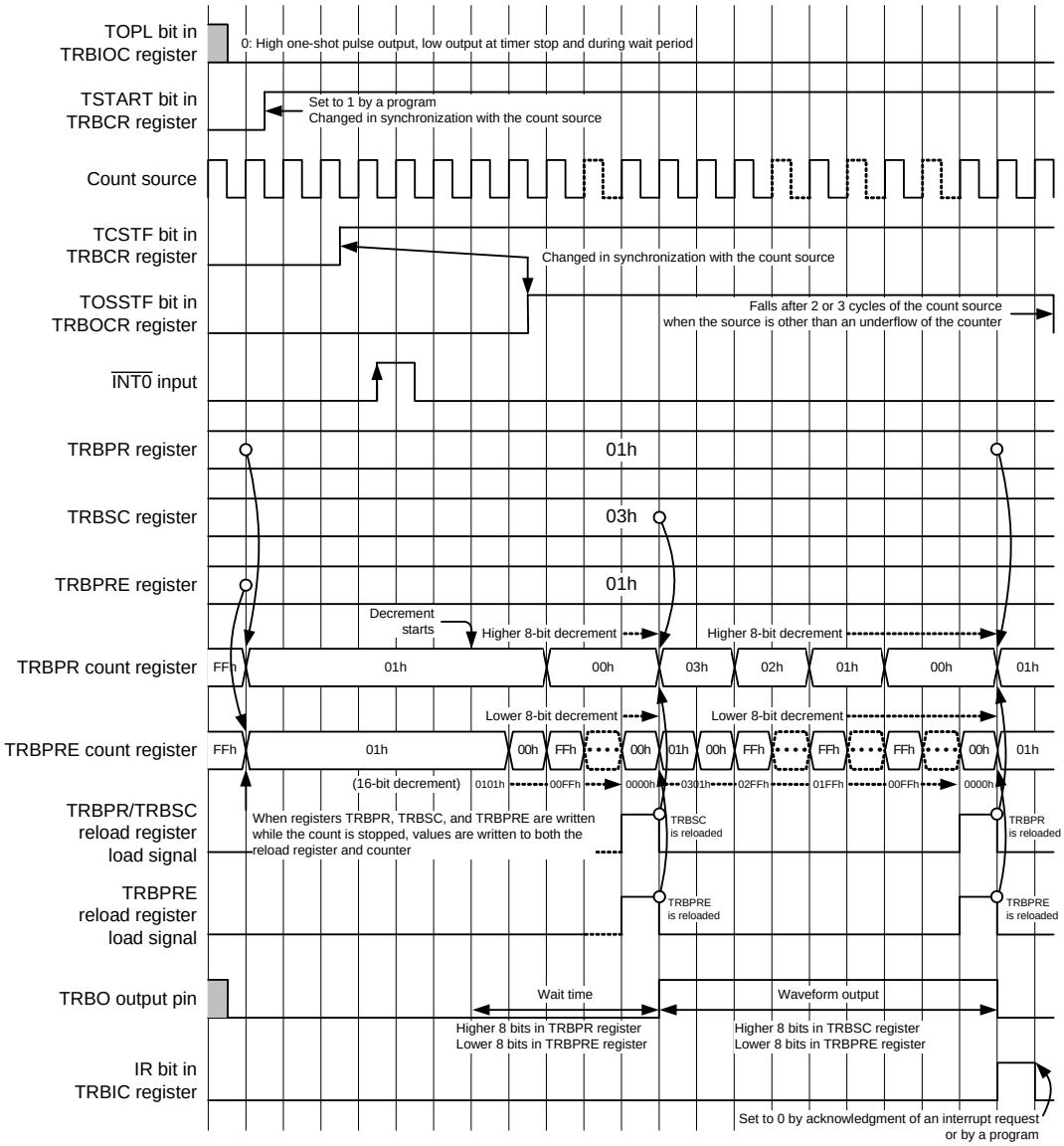
In this mode, a one-shot pulse is output from the TRBO pin by a program, an external trigger ($\overline{\text{INT0}}$ pin input), or event input from the ELC after a specified period.
When a trigger is generated from that point, the timer outputs a pulse only once for a given length of the time equal to the setting value of the TRBSC register after waiting for a given length of time equal to the setting value of the TRBPR register.
In the 8-bit timer with 8-bit prescaler, set the count value of the wait time in the TRBPR register and set the count value of the pulse width in the TRBSC register.
In the 16-bit timer, set the count value of the wait time of the higher 8 bits in the TRBPR register and that of the lower 8 bits in the TRBPRE register. Set the count value of the pulse width of the higher 8 bits in the TRBSC register and that of the lower 8 bits in the TRBPRE register.
When 1 (one-shot count starts) is written to the TOSST bit in the TRBOCR register while the TCSTF bit in the TRBCR register is 1 (count enabled), the count is started. If a valid trigger is input to the $\overline{\text{INT0}}$ pin while the TCSTF bit is 1, the count is started. The count is also started by event input from the ELC while the TCSTF bit is 1. When the count value in the timer RB secondary underflows and then it is reloaded, the count is stopped. The count is also stopped by any of the following settings:
• When 1 (one-shot count stops) is written to the TOSSP bit in the TRBOCR register, the count is stopped.
• When 0 (count stops) is written to the TSTART bit in the TRBCR register, the count is stopped.
• When 1 (count is forcibly stopped) is written to the TSTOP bit in the TRBCR register, the count is stopped.
An interrupt request is generated when the timer RB2 counter underflows during the secondary period.
When registers TRBPRE and TRBPR are read, each count value is read. When registers TRBPRE, TRBPR, and TRBSC are written while the count is stopped, values are written to both the reload register and counter, respectively. When these registers are written during a count operation, values are written to the reload register and then transferred to the counter at the next reload operation.
During 16-bit timer operation, the lower 8 bits for both primary and secondary periods are set by the same TRBPRE register, so theses bits are always set to the same value in one cycle. Therefore, even if an attempt is made to change only the pulse width of a PWM waveform without changing the period, PWM control cannot be performed at fine resolution because only the higher 8 bits can be set.
For the setting of trigger by the $\overline{\text{INT0}}$ input, refer to **16.7 INT0 Input Trigger Selection**.
Figure 16.8 shows an Example of 8-Bit Timer with 8-Bit Prescaler Operation in Programmable Wait One-Shot Generation Mode. Figure 16.9 shows an Example of 16-Bit Timer Operation in Programmable Wait One-Shot Generation Mode.

Note:
1. After 1 is written to bits TOSST and TOSSP, a valid trigger is input to the $\overline{\text{INT0}}$ pin, event input from the event link controller (ELC), or 0 is written to the TSTART bit, settings are reflected in the counter operation after three cycles of the count source.
   Monitor the TOSSTF bit in the TRBOCR register to confirm the operating state of the counter.



The above diagram applies under the following conditions:
- TRBPRE register = 01h, TRBPR register = 01h, TRBSC register = 03h
- TCNT16 bit in TRBMR register = 0 (8-bit timer with 8-bit prescaler)
- TOPL bit = 0 (high one-shot pulse output, low output at timer stop and during wait period), TOCNT bit = 0 (waveform output), INOSTG bit = 1 (one-shot trigger to $\overline{\text{INT0}}$ pin enabled), INOSEG bit = 1 (rising edge) in TRBIOC register
- TRBIE bit in TRBIR register = 1 (timer RB2 interrupt enabled)

Figure 16.8 Example of 8-Bit Timer with 8-Bit Prescaler Operation in Programmable Wait One-Shot Generation Mode



The above diagram applies under the following conditions:
- TRBPRSC register = 0101h, TRBSC register = 03h
- TCNT16 bit in TRBMR register = 1 (16-bit timer)
- TOP bit = 0 (high one-shot pulse output, low output at timer stop and during wait period), TOCNT bit = 0 (waveform output), INOSTG bit = 1 (one-shot trigger to $\overline{\text{INT0}}$ pin enabled), INOSEG bit = 1 (rising edge) in TRBIOC register
- TRBIE bit in TRBIR register = 1 (timer RB2 interrupt enabled)

Figure 16.9 Example of 16-Bit Timer Operation in Programmable Wait One-Shot Generation Mode

16.5 Selectable Functions

16.5.1 Configuration and Update Timing for Registers TRBPRE, TRBPR, and TRBSC

Registers TRBPRE, TRBPR, and TRBSC are configured with a master – reload register structure. Figure 16.10 shows the Configuration of Registers TRBPRE, TRBPR, and TRBSC. When the TSTART bit in the TRBCR register is set to 0 (count stops), values are updated to the reload registers immediately after the registers are written. However, when the TSTART bit is 1 (count starts), the timing for updating the reload registers differs in each mode. In the 8-bit timer with 8-bit prescaler, after the TRBPRE register is written, the TRBPRE register reload register is updated in synchronization with the count source.
When the counter is operating in programmable waveform or programmable wait one-shot generation mode, after the TRBPR register is written, the TRBPRE register reload register is updated at the same time.
In programmable waveform and programmable wait one-shot generation modes, write to the TRBPR register after writing to the TRBSC register.
Table 16.6 lists the Reload Register Update Timing for Registers TRBPR and TRBSC in 8-Bit Timer with 8-Bit Prescaler. Table 16.7 lists the Reload Register Update Timing for Registers TRBPRE, TRBPR, and TRBSC in 16-Bit Timer.

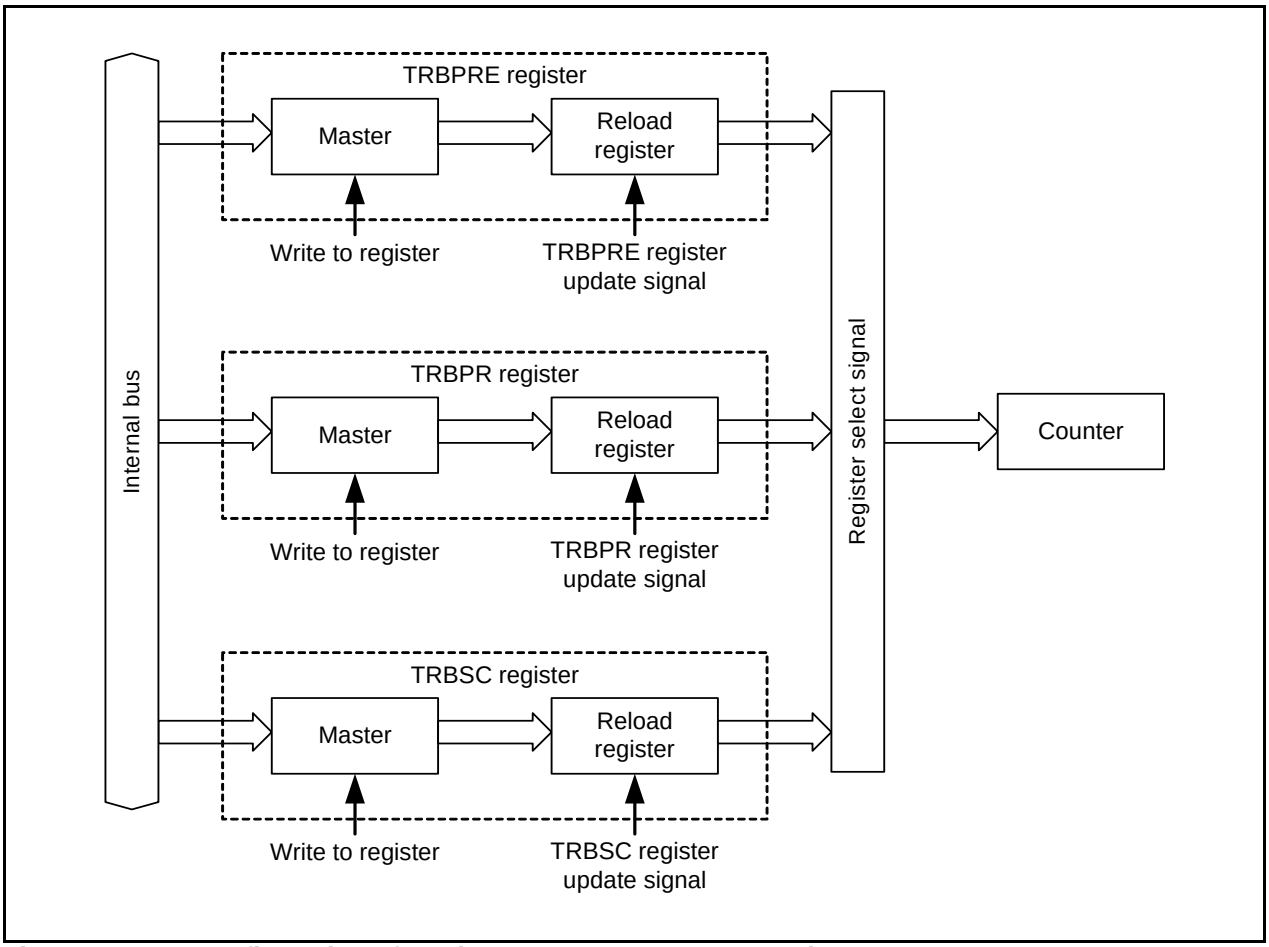


Figure 16.10 Configuration of Registers TRBPRE, TRBPR, and TRBSC

Table 16.6 Reload Register Update Timing for Registers TRBPR and TRBSC in 8-Bit Timer with 8-Bit Prescaler

Operating Mode		Update Timing (1)	
		TRBPR Register	TRBSC Register
Timer mode		Updated in synchronization with the prescaler underflow after the TRBPR register is written.	Not used
Programmable waveform generation mode	TWRC = 1	Updated immediately before the end of the secondary output period after the TRBPR register is written.	
	TWRC = 0	Updated in synchronization with the prescaler underflow after the TRBPR register is written. (2)	
Programmable one-shot generation mode		Updated in synchronization with the prescaler underflow after the TRBPR register is written.	Not used
Programmable wait one-shot generation mode	TWRC = 1	Updated immediately before the end of the secondary output period after the TRBPR register is written.	
	TWRC = 0	Updated in synchronization with the prescaler underflow after the TRBPR register is written. (2)	

TWRC: Bit in TRBMR register

Notes:
1. For details, refer to **16.5.2 Prescaler and Counter Operation Using TWRC Bit**.
2. When the TWRC bit is 0 (write to reload register and counter) in programmable waveform and programmable wait one-shot generation modes, if the data in registers TRBSC and TRBPR is updated during count operation, the waveform is output for the updated period from that time.

Table 16.7 Reload Register Update Timing for Registers TRBPRE, TRBPR, and TRBSC in 16-Bit Timer

Operating Mode		Update Timing (1)	
		Registers TRBPRE and TRBPR	TRBSC Register
Timer mode		Updated in synchronization with the count source after the TRBPR register is written.	Not used
Programmable waveform generation mode	TWRC = 1	Updated immediately before the end of the secondary output period after the TRBPR register is written	
	TWRC = 0	Updated in synchronization with the count source after the TRBPR register is written. (2)	
Programmable one-shot generation mode		Updated in synchronization with the count source after the TRBPR register is written.	Not used
Programmable wait one-shot generation mode	TWRC = 1	Updated immediately before the end of the secondary output period after the TRBPR register is written.	
	TWRC = 0	Updated in synchronization with the count source after the TRBPR register is written. (2)	

TWRC: Bit in TRBMR register

Notes:
1. For details, refer to **16.5.2 Prescaler and Counter Operation Using TWRC Bit**.
2. When the TWRC bit is 0 (write to reload register and counter) in programmable waveform and programmable wait one-shot generation modes, if the data in registers TRBSC and TRBPR is updated during count operation, the waveform is output for the updated period from that time.

16.5.2 Prescaler and Counter Operation Using TWRC Bit

Set the TWRC bit to 1 in any operating mode other than timer mode.

While timer RB2 is used in timer mode, the TWRC bit in the TRBMR register can be used to select whether only registers TRBPRE and TRBPR are written or the reload register, and counter are written. However, when the TCSTF bit in the TRBCR register is 0 (count stops), the reload register, and counter are written regardless of the setting of the TWRC bit in the TRBMR register. When the TWRC bit is set to 1 (write to reload register only) and the value of the prescaler is changed, the period when the value is written is shifted. When only the register is written, periods can be switched smoothly from pre- to post-settings without any irregular periods.

During programmable one-shot and programmable wait one-shot generation modes, when the TCSTF bit in the TRBCR register is 1 (count in progress) and the TOSSTF bit in the TRBOCR register is 0 (one-shot is stopped), the reload register and counter can be written because the setting of the TWRC bit in the TRBMR register is invalid.

Figures 16.11 and 16.12 show Example of Prescaler and Counter Operation in 8-Bit Timer with 8-Bit Prescaler.

Figures 16.13 and 16.14 show Example of Counter Operation in 16-Bit Timer.

When the TCSTF bit is 1 (count in progress), even if the TWRC bit is set to 0 (write to reload register and counter), the count value is not updated immediately after the write instruction is executed because transfer to the prescaler and counter is performed in synchronization with the count source.

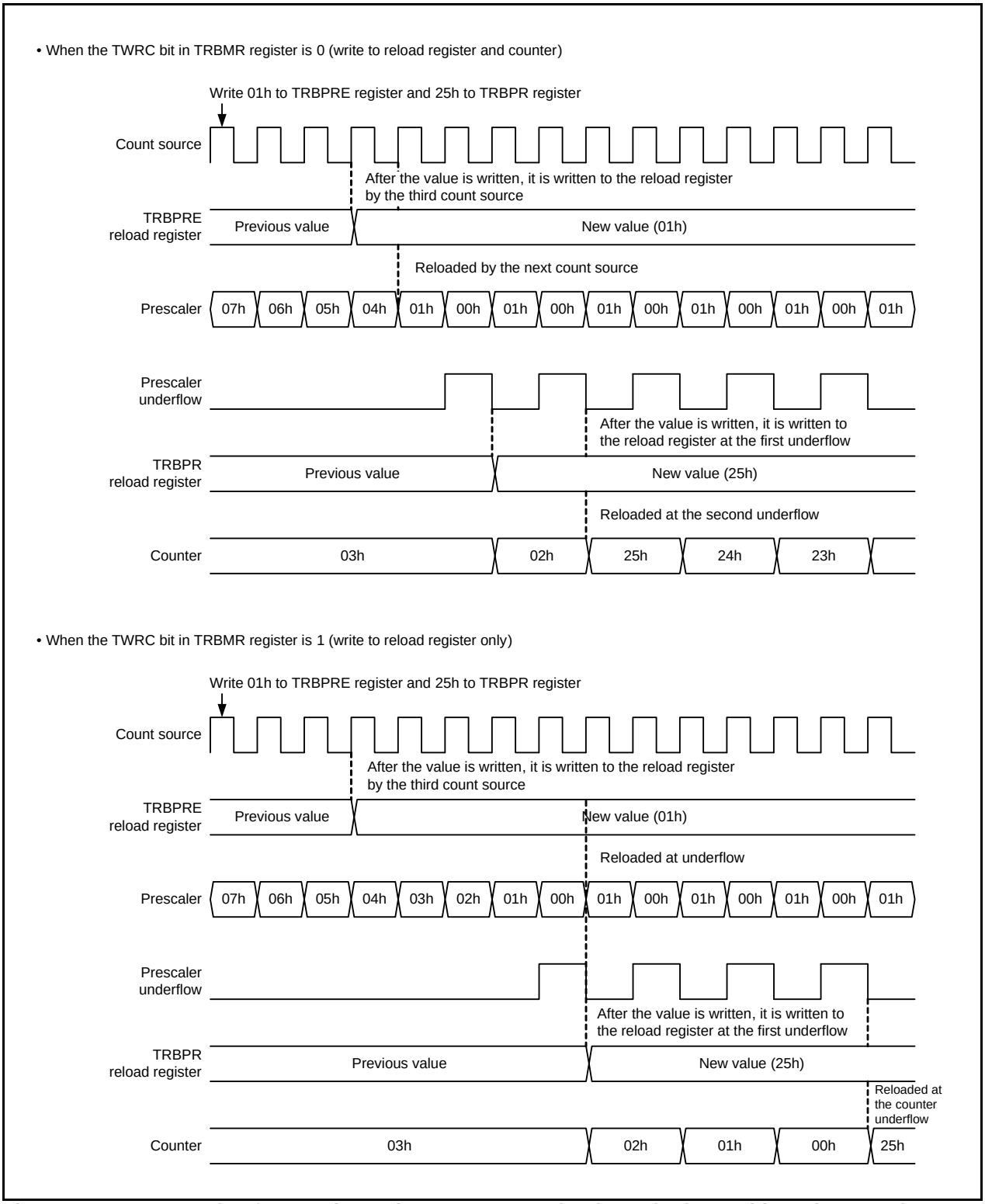


Figure 16.11 Example of Prescaler and Counter Operation in 8-Bit Timer with 8-Bit Prescaler (Timer Mode or Programmable One-Shot Generation Mode)

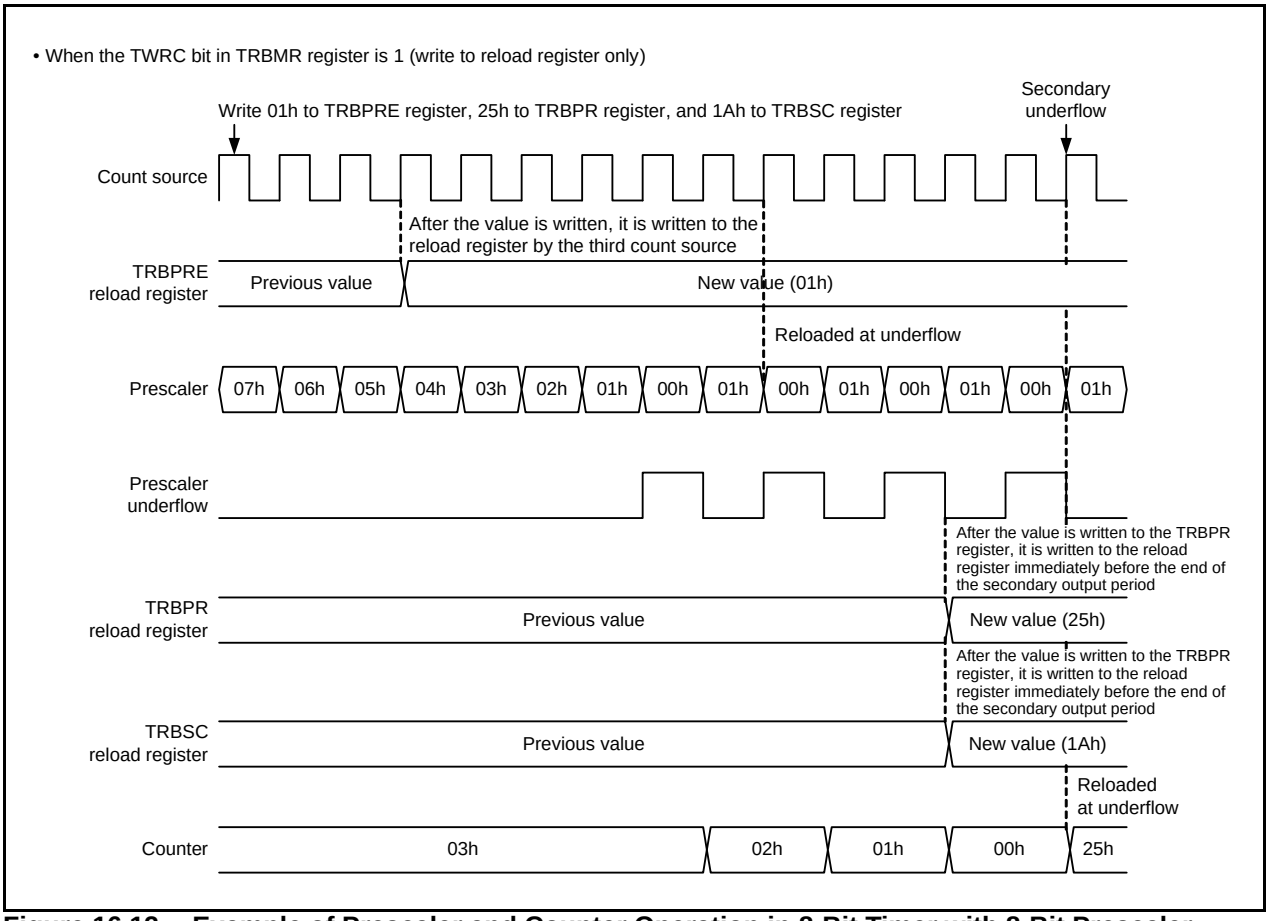


Figure 16.12 Example of Prescaler and Counter Operation in 8-Bit Timer with 8-Bit Prescaler (Programmable Waveform Generation Mode or Programmable Wait One-Shot Generation Mode)

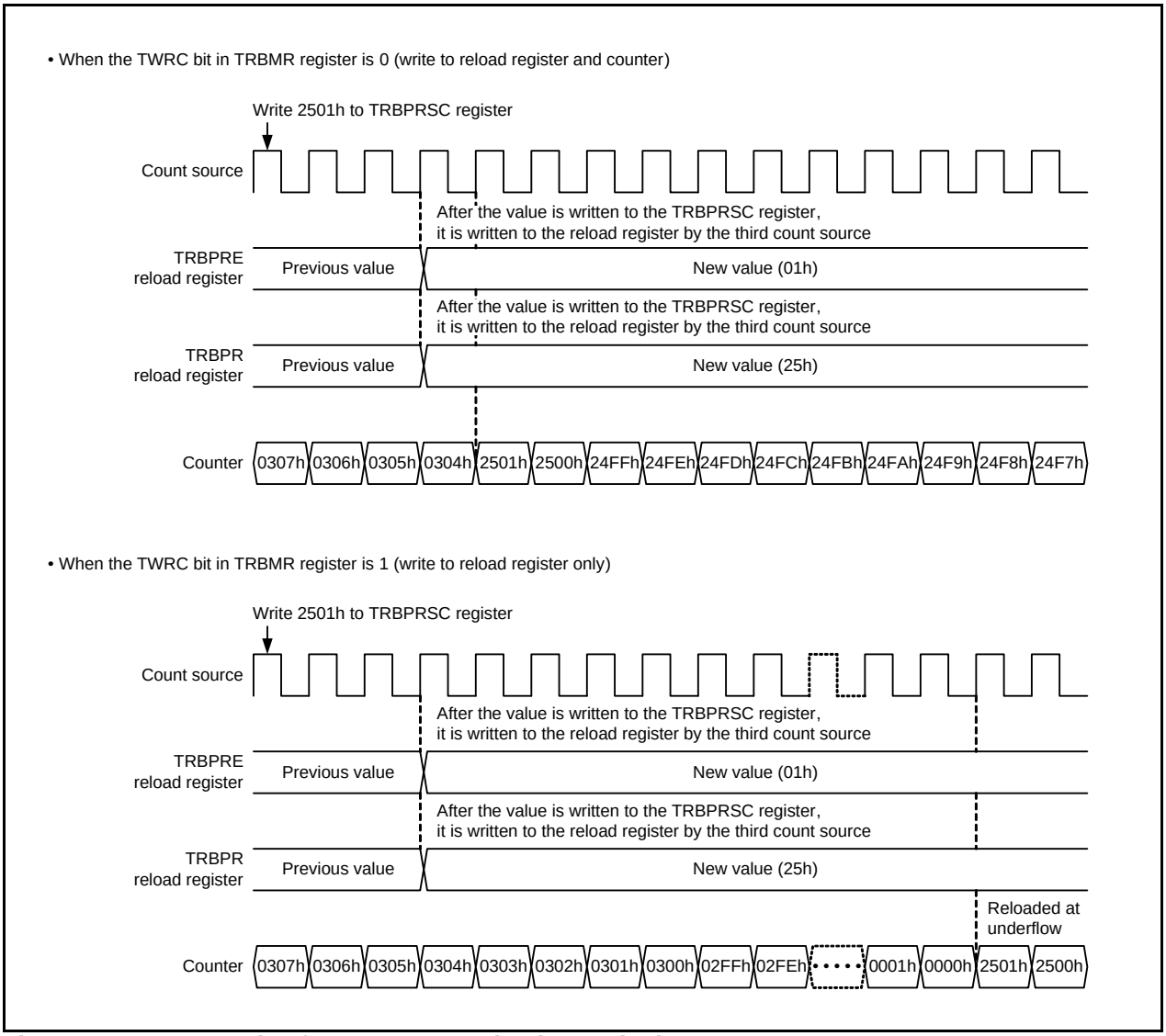


Figure 16.13 Example of Counter Operation in 16-Bit Timer (Timer Mode or Programmable One-Shot Generation Mode)

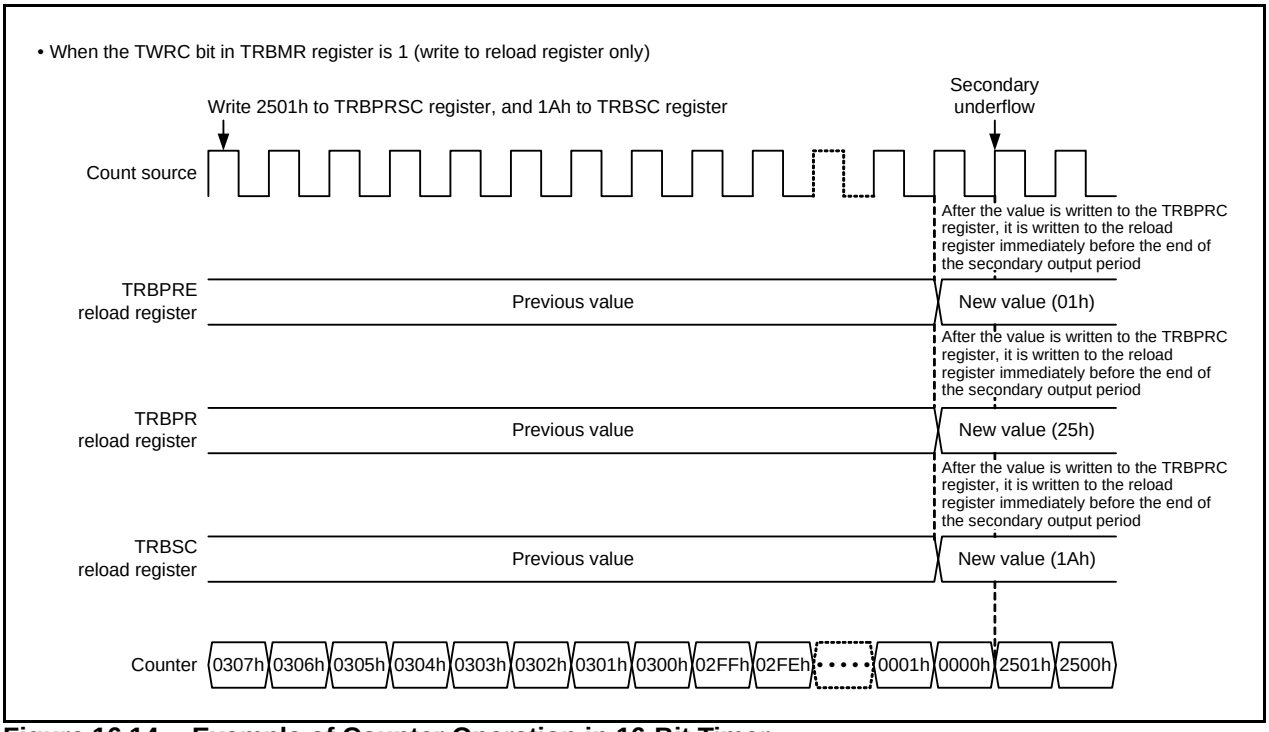


Figure 16.14 Example of Counter Operation in 16-Bit Timer (Programmable Waveform Generation Mode or Programmable Wait One-Shot Generation Mode)

16.5.3 TOCNT Bit Setting and Pin States

The TOCNT bit in the TRBIOC register can be used to select whether a timer waveform or fixed value is output.
Table 16.8 lists the Output Data in Each Mode.

Table 16.8 Output Data in Each Mode

Operating Mode	Enable Signal for TRBO Output		Output Data
Timer mode	Output disabled		High impedance
Programmable waveform generation mode	TOCNT	0	Waveform output
		1	Fixed value (inverted value of TOPL) Refer to Table 16.4 Functions of Timer RB2 Output Level Select Bit.
Programmable one-shot generation mode	Output enabled		Waveform output
Programmable wait one-shot generation mode			

TOPL, TOCNT: Bits in TRBIOC register

For timer mode, programmable one-shot generation mode, and programmable wait one-shot generation mode, regardless of the setting of the TOCNT bit, the state is high impedance in timer mode, and a waveform is output in programmable one-shot generation mode and programmable wait one-shot generation mode.
If the TOCNT bit is rewritten in programmable waveform generation mode, the pin state does not change immediately. The data is reflected in the pin state when one of the following conditions is met. When the TOCNT bit is 1 (fixed-value output), the inverted value of the TOPL bit in the TRBIOC register is output.

[Update conditions for pin states]
• When the TSTART bit in the TRBCR register is changed from 0 (count stops) to 1 (count starts).
• When the TRBPR register is reloaded to the counter.

16.5.4 Coordination with Event Link Controller (ELC)

In programmable one-shot and programmable wait one-shot generation mode, through coordination with the ELC, timer RB2 can start the count at the rising edge of event input from the ELC.

16.6 Interrupt Requests

When the TRBIF bit in the TRBIR register is 1 (interrupt requested) and the TRBIE bit is 1 (interrupt enabled), an interrupt request is generated to the CPU. The timer RB2 interrupt request flag relates to the CPU interrupt enable flag (I flag) in the flag register (FLG), the processor interrupt priority level (IPL), and the ICU control register (bits IR and ILVL0 to ILVL2 in the TRB2IC_0 register) for interrupt control. If the CPU acknowledges an interrupt, the TRBIF bit is set to 0 during the interrupt sequence. The conditions for setting the TRBIF bit to 1 differ depending on the mode. Refer to the descriptions of the TRBIF bit and individual modes.

16.7 $\overline{\text{INT0}}$ Input Trigger Selection

In programmable one-shot and programmable wait one-shot generation modes, when 1 (one-shot count starts) is written to the TOSST bit in the TRBCR register or a trigger is input to the $\overline{\text{INT0}}$ pin with the TCSTF bit in the TRBCR register set to 1 (count enabled), one-shot operation is started.

When using the trigger input from the $\overline{\text{INT0}}$ pin, make the following settings beforehand.

(1) Set the PD4_5 bit in the PD4 register to 0 (input port).
(2) Set bits INT0F0 and INT0F1 in the INTF register to select the digital filter sampling clock for the $\overline{\text{INT0}}$ pin.
(3) Select one edge or both edges using the INT0PL bit in the INTEN register. When one edge is selected, select falling or rising edge using the INOSEG bit in the TRBIOC register.
(4) Set the INT0EN bit in the INTEN register to 1 (enabled) to enable an interrupt.
(5) Set the INOSTG bit in the TRBIOC register to 1 (one-shot trigger to $\overline{\text{INT0}}$ pin enabled).

When an interrupt request is generated by the trigger input from the $\overline{\text{INT0}}$ pin, note the following:

- Select one edge or both edges using the INT0PL bit. When one edge is selected, select falling or rising edge using the INT0POL bit in the INTPOL register (the IN0SEG bit in the TRBIOC register (the one-shot trigger polarity select bit is unrelated to $\overline{\text{INT0}}$ interrupt)).
- While the TOSSTF bit in the TRBOCR register is 1 (one-shot is operating (including wait period)), even if a one-shot trigger is generated the operation of timer RB2 will be unaffected. However, the IR bit in the INT0IC register will change.
- For details on $\overline{\text{INT}}$ interrupt, refer to **11.5 $\overline{\text{INT}}$ Interrupt**.

16.8 Notes on Timer RB2

(1) Timer RB2 stops counting after a reset. Start the count after setting the values in the timer and prescaler.

(2) While using the 16-bit timer, when accessing registers TRBPRE, TRBPR, and TRBSC in 8-bit units (8-bit access), always access TRBPRE, TRBPR, and TRBSC in that order.

(3) In programmable one-shot and programmable wait one-shot generation modes, when the TOSSP bit in the TRBOCR register is set to 1 and the one-shot is stopped, the timer reloads the reload register value and is stopped. The timer count value must be read before the timer is stopped.

(4) After 1 (count starts) is written to the TSTART bit in the TRBCR register while the count is stopped, the TCSTF bit in the TRBCR register remains 0 (count stops) for two or three cycles of the count source. Do not access the registers associated with timer RB2 (1) other than the TCSTF bit until this bit is set to 1 (count in progress).
After 0 (count stops) is written to the TSTART bit during count operation, the TCSTF bit remains 1 for two or three cycles of the count source. When the TCSTF bit is set to 0, the count is stopped. Do not access the registers associated with timer RB2 (1) other than the TCSTF bit until this bit is set to 0.

Note:
1. Registers associated with timer RB2:
TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBPR, and TRBSC

(5) When the TSTART bit is 0 (count stops), wait for at least two cycles of the CPU clock and then set the TSTART bit to 1 (count starts) to change the values of registers TRBPRE, TRBPR, and TRBSC.

(6) When the TSTART bit is 1 (count starts) or the TCSTF bit is 1 (count in progress), do not change the values of registers TRBIOC and TRBMR, and the TRBIE bit in the TRBIR register. The TOCNT bit can be changed during count operation, according to the specifications shown in 16.5.3.

(7) When 1 is written to the TSTOP bit in the TRBCR register during count operation (the TCSTF bit is 1), timer RB2 stops without any wait time (the TSTART bit is 0, the TCSTF bit is 0, the TOSST bit is 0, and the TOSSTF bit is 0).

(8) When 1 (one-shot starts) is written to the TOSST bit in the TRBOCR register, the TOSSTF bit changes after three cycles of the timer RB count source. If 1 (one-shot stops) is written to the TOSSP bit in the TRBOCR register, the TOSSTF bit changes after two or three cycles of the RB count source. If 1 is written to the TOSSP bit during the period after 1 is written to the TOSST bit but before the TOSSTF bit can become 1 (one-shot is operating (including wait period)), depending on the internal state the TOSSTF bit may become 0 (one-shot is stopped) or 1. Similarly, if 1 is written to the TOSST bit during the period after 1 is written to the TOSSP bit but before the TOSSTF bit can become 0, the TOSSTF bit may become 0 or 1.

(9) When the underflow signal from timer RJ is used as the count source for timer RB2, set timer RJ to timer mode, pulse output mode, or event counter mode.

(10) Make sure that the TCSTF bit is 1 (count in progress) before writing 1 (one-shot count starts) to the TOSST bit in the TRBOCR register. When the TCSTF bit is 0 (count stops), writing 1 (one-shot count starts) to the TOSST bit has no effect.

(11) In programmable waveform and programmable wait one-shot generation modes of timer RB2, write to the TRBSC register before writing to the TRBPR register. The value of the TRBPR register is reflected to the counter during the underflow of the secondary period after the TRBPR register is written. If registers TRBSC and TRBPR are written multiple times during the period after the TRBPR register was written but before the secondary period underflow, the data that was written last will be reflected in the counter. However, do not write to the TRBSC register only on its own. Write to both the TRBSC and TRBPR registers.

(12) When writing to and reading from the TRBPRE or TRBPR register successively while the count is stopped, insert NOP instructions between writing and reading.

(13) When writing to registers TRBPRE, TRBPR, and TRBSC during count operation (the TSTART bit is 1 or the TCSTF bit is 1), note the following points:
- When writing to the TRBPRE register successively, allow at least three cycles of the count source between writes.
- When writing to the TRBPR register successively, allow at least three cycles of the prescaler underflow between writes.
- When writing to the TRBSC register successively, allow at least three cycles of the prescaler underflow between writes.

(14) To lower current consumption, switch to standby module state while bits TSTART and TCSTF in the TRBCR register are both 0 (count stops). For details on the bits for switching to module standby state, refer to **10.2.9 Module Standby Control Register 2 (MSTCR2)**

(15) To forcibly stop the count using the TSTOP bit, set as follows:
(1) Set the interrupt priority level of the TRB2IC_0 register to 0 (interrupt disabled).
(2) Set the TSTOP bit to 1 (count is forcibly stopped).
(3) Set the TRBIF bit to 0 (no interrupt requested)

(16) When the TRBPR register is rewritten in programmable waveform generation mode, do not write to the TRBPRE, TRBPR, or TRBSC register at the following timing during the next secondary period after rewriting.
- 8-bit timer with 8-bit prescaler:
  Two cycles of the prescaler underflow before the secondary output period ends.
- 16-bit timer:
  Two cycles of the count source clock before the secondary output period ends.

17. Timer RC

Timer RC is a 16-bit timer that provides output compare and input capture functions and can count external events. It can be used as a multifunction timer with various applications such as generation of pulse output with an arbitrary duty cycle using the compare match between the timer RC counter and four general registers.

17.1 Overview

Table 17.1 lists the Timer RC Specifications, Table 17.2 lists the Timer RC Functions, Figure 17.1 shows the Timer RC Block Diagram, and Table 17.3 lists the Timer RC Pin Configuration.

Table 17.1 Timer RC Specifications

Item			Description
Count sources (counter input clocks)	Operating clock	Internal clock	• f1, f2, f4, f8, or f32: Selected when bits CKS2 to CKS0 in the TRCCR1 register are 000b to 100b. • fHOCO: Selected when bits CKS2 to CKS0 in the TRCCR1 register are 110b. • fHOCO-F: Selected when bits CKS2 to CKS0 in the TRCCR1 register are 111b.
		External clock (external event count)	TRCCLK input: Selected when bits CKS2 to CKS0 in the TRCCR1 register are 101b.
Pulse I/O pins			4
General registers			4 • Can be set as output compare or input capture registers individually. • Can be used as buffer registers for output compare or input capture.
Operating modes		Timer mode	• Output compare function: Low-level, high-level, or toggle output can be performed. • Input capture function: A rising edge, falling edge, or both edges can be detected. • Counter clear function: A count period can be set.
		PWM mode	PWM output with up to three phases.
		PWM2 mode	Pulse output with an arbitrary period and duty.
Interrupt sources			• Compare match/input capture multiplexed interrupt × 4 sources • Overflow interrupt
Others			• The initial value of the timer RC output can be set arbitrarily. • A/D conversions triggered by compare matches in registers TRCGRA, TRCGRB, TRCGRC, and TRCGRD can be set. • Timer RC can cooperate with the event link controller (ELC) or the DTC. • The $\overline{\text{INT0}}$ pin can be used to control disabling of timer output. • The $\overline{\text{INT1}}$ pin can be used to input timer RC_0 output waveform manipulation events. • Input-capture trigger selection fOCO128 can be selected as the input-capture trigger input for the TRCGRA register.

Table 17.2 Timer RC Functions

Item		Counter	I/O Pin			
			TRCIOA	TRCIOB	TRCIOC	TRCIOD
Count sources		Internal clock: f1, f2, f4, f8, f32, fHOCO, or fHOCO-F External clock: TRCCLK				
General registers (output compare/input capture multiplexed registers)		Period setting with the TRCGRA register	TRCGRA register	TRCGRB register	TRCGRC register In buffer operation Buffer register for the TRCGRA register	TRCGRD register In buffer operation Buffer register for the TRCGRB register
Counter clear function		Input capture/ compare match for the TRCGRA register	Input capture/ compare match for the TRCGRA register	—	—	—
		TRCTRG input	—	—	—	—
Setting function for initial output level		—	Available	Available	Available	Available
Buffer operation		—	Available	Available	—	—
Compare match	Low output	—	Available	Available	Available	Available
	High output	—	Available	Available	Available	Available
	Toggle output	—	Available	Available	Available	Available
Input capture function		—	Available	Available	Available	Available
PWM mode		—	—	Available	Available	Available
PWM2 mode		—	—	Available	—	—
Interrupt sources		Overflow	Compare match/ input capture	Compare match/ input capture	Compare match/ input capture	Compare match/ input capture

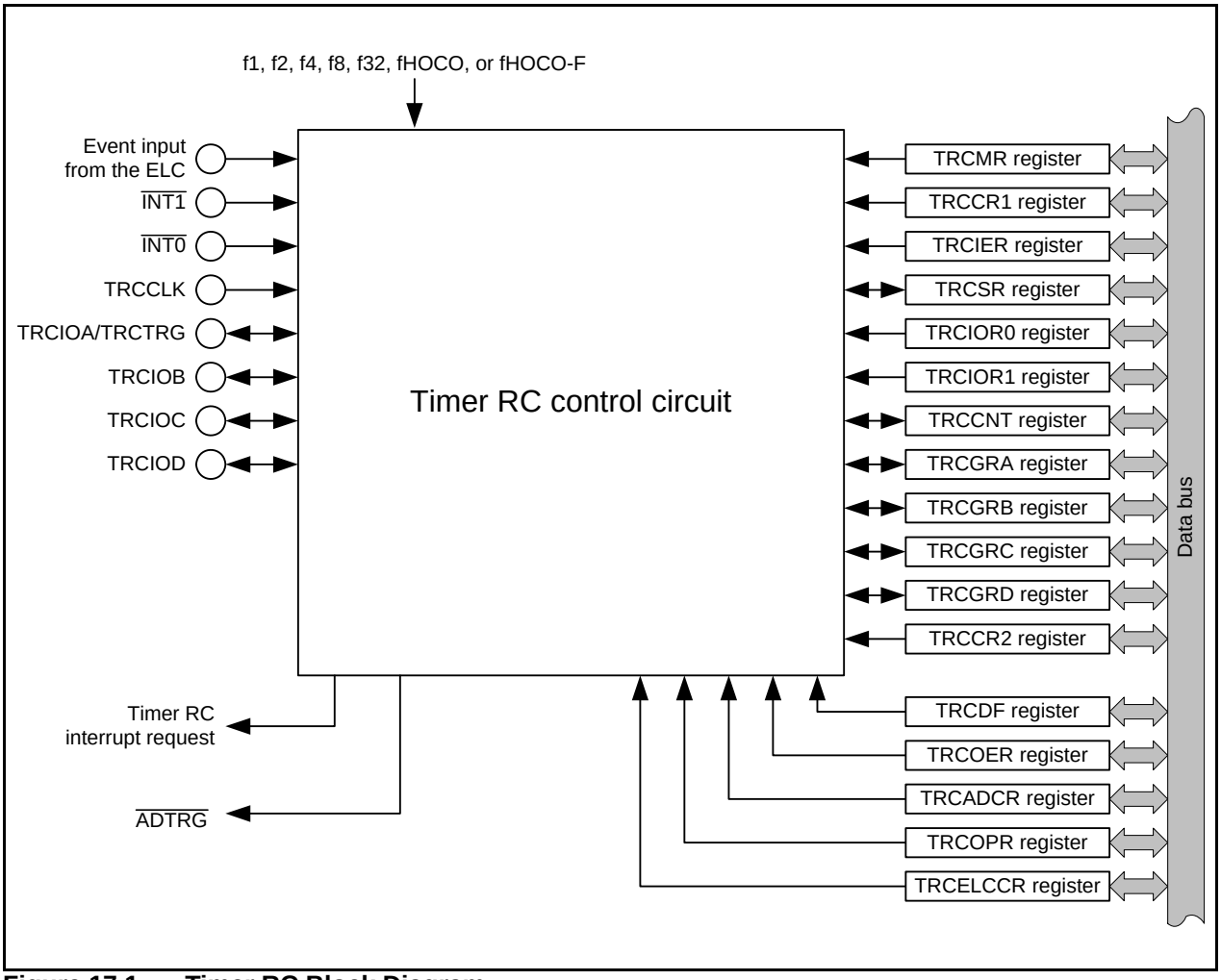


Figure 17.1 Timer RC Block Diagram

Table 17.3 Timer RC Pin Configuration

Pin Name	I/O	Function
TRCCLK	Input	External clock input
TRCIOA/TRCTRG	Input/Output	TRCGRA output-compare output/TRCGRA input-capture input/external trigger input (TRCTRG)
TRCIOB	Input/Output	TRCGRB output-compare output/TRCGRB input-capture input/PWM output (in PWM mode and PWM2 mode)
TRCIOC	Input/Output	TRCGRC output-compare output/TRCGRC input-capture input/PWM output (in PWM mode)
TRCIOD	Input/Output	TRCGRD output-compare output/TRCGRD input-capture input/PWM output (in PWM mode)
$\overline{\text{INT0}}$	Input	Timer output disabling control input
$\overline{\text{INT1}}$	Input	Timer RC_0 output waveform manipulation event input

17.2 Registers

Table 17.4 lists the Timer RC Register Configuration.

Table 17.4 Timer RC Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Timer RC_0 Counter	TRCCNT_0	0000h	00138h	16
Timer RC_0 General Register A	TRCGRA_0	FFFFh	0013Ah	16
Timer RC_0 General Register B	TRCGRB_0	FFFFh	0013Ch	16
Timer RC_0 General Register C	TRCGRC_0	FFFFh	0013Eh	16
Timer RC_0 General Register D	TRCGRD_0	FFFFh	00140h	16
Timer RC_0 Mode Register	TRCMR_0	01001000b	00142h	8
Timer RC_0 Control Register 1	TRCCR1_0	00h	00143h	8
Timer RC_0 Interrupt Enable Register	TRCIER_0	01110000b	00144h	8
Timer RC_0 Status Register	TRCSR_0	01110000b	00145h	8
Timer RC_0 I/O Control Register 0	TRCIOR0_0	10001000b	00146h	8
Timer RC_0 I/O Control Register 1	TRCIOR1_0	10001000b	00147h	8
Timer RC_0 Control Register 2	TRCCR2_0	00011000b	00148h	8
Timer RC_0 Digital Filter Function Select Register	TRCDF_0	00h	00149h	8
Timer RC_0 Output Enable Register	TRCOER_0	01111111b	0014Ah	8
Timer RC_0 A/D Conversion Trigger Control Register	TRCADCR_0	11110000b	0014Bh	8
Timer RC_0 Output Waveform Manipulation Register	TRCOPR_0	00h	0014Ch	8
Timer RC_0 ELC Cooperation Control Register	TRCELCCR_0	00h	0014Dh	8

17.2.1 Timer RC Counter (TRCCNT)

Address 00138h (TRCCNT_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	16-bit readable/writable up counter. When this counter overflows, the OVF bit in the TRCSR register is set to 1. If the OVIE bit in the TRCIER register is set to 1 (interrupt request by OVF bit is enabled) at this time, an interrupt request is generated.	0000h to FFFFh	R/W

The count source for the timer RC counter is selected by bits CKS0 to CKS2 in the TRCCR1 register. By setting the CCLR bit in the TRCCR1 register to 1, the TRCCNT register is set to 0000h at a compare match with the TRCCRA register.

Do not access the TRCCNT register in 8-bit units. This register must be accessed in 16-bit units.

17.2.2 Timer RC General Registers A, B, C, and D (TRCGRA, TRCGRB, TRCGRC, TRCGRD)

Address 0013Ah (TRCGRA_0), 0013Ch (TRCGRB_0), 0013Eh (TRCGRC_0), 00140h (TRCGRD_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Function varies according to the operating mode.	R/W

Do not access registers TRCGRA to TRCGRD in 8-bit units. These registers must be accessed in 16-bit units.

Table 17.5 Functions of TRCGRj Register when Using Input Capture Function

Register	Setting	Register Function	Input Capture Input Pin
TRCGRA	—	General register. Can be used to read the TRC register value at input capture.	TRCIOA
TRCGRB			TRCIOB
TRCGRC	BUFEA = 0	General register. Can be used to read the TRC register value at input capture.	TRCIOC
TRCGRD	BUFEB = 0		TRCIOD
TRCGRC	BUFEA = 1	Buffer registers. Can be used to hold transferred value from the general register. (Refer to **17.5.5 Buffer Operation Timing**.)	TRCIOA
TRCGRD	BUFEB = 1		TRCIOB

j = A, B, C, or D
BUFEA, BUFEB: Bits in TRCMR register

Table 17.6 Functions of TRCGRj Register when Using Output Compare Function

Register	Setting	Register Function	Output Compare Output Pin
TRCGRA	—	General register. Write a compare value to one of these registers.	TRCIOA
TRCGRB			TRCIOB
TRCGRC	BUFEA = 0	General register. Write a compare value to one of these registers.	TRCIOC
TRCGRD	BUFEB = 0		TRCIOD
TRCGRC	BUFEA = 1	Buffer register. Write the next compare value to one of these registers. (Refer to **17.5.5 Buffer Operation Timing**.)	TRCIOA
TRCGRD	BUFEB = 1		TRCIOB

j = A, B, C, or D
BUFEA, BUFEB: Bits in TRCMR register

Table 17.7 Functions of TRCGRh Register in PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRCGRA	—	General register. Set the PWM period.	—
TRCGRB	—	General register. Set the PWM output change point.	TRCIOB
TRCGRC	BUFEA = 0	General register. Set the PWM output change point.	TRCIOC
TRCGRD	BUFEB = 0		TRCIOD
TRCGRC	BUFEA = 1	Buffer register. Set the next PWM period. (Refer to **17.5.5 Buffer Operation Timing**.)	—
TRCGRD	BUFEB = 1	Buffer register. Set the next PWM output change point. (Refer to **17.5.5 Buffer Operation Timing**.)	TRCIOB

h = A, B, C, or D
BUFEA, BUFEB: Bits in TRCMR register
Note:
1. The output level does not change even when a compare match occurs if the TRCGRA register value (PWM period) is the same as the TRCGRB, TRCGRC, or TRCGRD register value.

Table 17.8 Functions of TRCGRj Register in PWM2 Mode

Register	Setting	Register Function	PWM2 Output Pin
TRCGRA	—	General register. Set the PWM period.	TRCIOB pin
TRCGRB (1)	—	General register. Set the PWM output change point.	
TRCGRC (1)	BUFEA = 0	General register. Set the PWM output change point (wait time after trigger).	
TRCGRD	BUFEB = 0	(Not used in PWM2 mode)	—
TRCGRD	BUFEB = 1	Buffer register. Set the next PWM output change point. (Refer to **17.5.5 Buffer Operation Timing**.)	TRCIOB pin

j = A, B, C, or D
BUFEA, BUFEB: Bits in TRCMR register
Note:
1. Do not set the TRCGRB and TRCGRC registers to the same value.

17.2.3 Timer RC Mode Register (TRCMR)

Address 00142h (TRCMR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CTS	—	BUFEB	BUFEA	PWM2	PWMD	PWMC	PWMB
After Reset	0	1	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PWMB	TRCIOB PWM mode select bit (1)	0: Timer mode 1: PWM mode	R/W
b1	PWMC	TRCIOC PWM mode select bit (1)		R/W
b2	PWMD	TRCIOD PWM mode select bit (1)		R/W
b3	PWM2	PWM2 mode select bit	0: PWM2 mode 1: Timer mode or PWM mode	R/W
b4	BUFEA	TRCGRC register function select bit (2)	0: Output compare register or input capture register 1: TRCGRC register is used as a buffer register for TRCRGA register	R/W
b5	BUFEB	TRCGRD register function select bit	0: Output compare register or input capture register 1: TRCGRD register is used as a buffer register for TRCRGB register	R/W
b6	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b7	CTS	TRCCNT count start bit	0: Count stops 1: Count starts	R/W

Notes:
1. These bits are enabled when the PWM2 bit is 1 (timer mode or PWM mode).
2. Set the BUFEA bit to 0 (output compare register or input capture register) in PWM2 mode.

CTS Bit (TRCCNT count start bit)

[Conditions for setting to 0]
- When 0 is written to this bit.
- When a compare match occurs while the CSTP bit in the TRCCR2 register is 1 (count is stopped at compare match with TRCGRA register) in PWM2 mode.

[Condition for setting to 1]
- When 1 is written to this bit.

The following shows the count stop conditions for each mode.

Count stop conditions

[In the input capture function]
- 0 (count stops) is written to the CTS bit in the TRCMR register.
- The TRCCNT register retains the value before the count stops.

[In the output compare function]
When the CSTP bit in the TRCCR2 register is 0 (count continues after compare match with TRCGRA register)
- 0 (count stops) is written to the CTS bit in the TRCMR register.
- The output-compare output pin retains the output level before the count stops. The TRCCNT register retains the value before the count stops.

[In PWM mode]
When the CSTP bit in the TRCCR2 register is 0 (count continues after compare match with TRCGRA register)
- 0 (count stops) is written to the CTS bit in the TRCMR register.
- The PWM output pin retains the output level before the count stops. The TRCCNT register retains the value before the count stops.

[In PWM2 mode]
- 0 (count stops) is written to the CTS bit in the TRCMR register. This applies when the CSTP bit in the TRCCR2 register is 0 and also when this bit is 1.
- The TRCIOB pin outputs the initial level according to the setting of the TOB bit in the TRCCR1 register. The TRCCNT register retains the value before the count stops.

17.2.4 Timer RC Control Register 1 (TRCCR1)

Address 00143h (TRCCR1_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	CKS2	CKS1	CKS0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	Timer output level select A bit (1)	0: Output value is low 1: Output value is high	R/W
b1	TOB	Timer output level select B bit (1)		R/W
b2	TOC	Timer output level select C bit (1)		R/W
b3	TOD	Timer output level select D bit (1)		R/W
b4	CKS0	Count source select bits (3)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: Rising edge of TRCCLK input (5) 1 1 0: fHOCO (2) 1 1 1: fHOCO-F (4)	R/W
b5	CKS1			R/W
b6	CKS2			R/W
b7	CCLR	TRCCNT counter clear select bit	0: Clear disabled (free-running operation) 1: TRCCNT counter is cleared by input capture/compare match A	R/W

Notes:
1. The output values set in bits TOA to TOD are reflected at the timing when the values are written. Set the value when the CTS bit in the TRCMR register is 0 (count stops).
2. When selecting fHOCO, set these bits with the high-speed on-chip oscillator operating.
3. The count source must be switched while the counter is stopped.
4. To select fHOCO-F, set it to the clock frequency higher than the CPU clock frequency.
5. The pulse width of an external clock input to TRCCLK must be three or more cycles of the operating clock.

TOA Bit (Timer output level select A bit)

This bit is used to set the output value from the TRCIOA pin until the first compare match A (match between the values of registers TRCCNT and TRCGRA) occurs. The TRCIOA pin is used in timer mode (for the output compare function). In PWM mode, this pin is not used.

TOB Bit (Timer output level select B bit)

This bit is used to set the output value from the TRCIOB pin until the first compare match B (match between the values of registers TRCCNT and TRCGRB) occurs. In PWM mode and PWM2 mode, this bit is used to control the output level of the TRCIOB pin. For details, refer to **Figure 17.9 Operation Example in PWM Mode**.

TOC Bit (Timer output level select C bit)

This bit is used to set the output value from the TRCIOC pin until the first compare match C (match between the values of registers TRCCNT and TRCGRC) occurs. In PWM mode, this bit is used to control the output level of the TRCIOC pin. For details, refer to **Figure 17.9 Operation Example in PWM Mode**.

TOD Bit (Timer output level select D bit)

This bit is used to set the output value from the TRCIOD pin until the first compare match D (match between the values of registers TRCCNT and TRCGRD) occurs. In PWM mode, this bit is used to control the output level of the TRCIOD pin. For details, refer to **Figure 17.9 Operation Example in PWM Mode**.

17.2.5 Timer RC Interrupt Enable Register (TRCIER)

Address 00144h (TRCIER_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	OVIE	—	—	—	IMIED	IMIEC	IMIEB	IMIEA
After Reset	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input capture/compare match A interrupt enable bit	0: Interrupt request by IMFA bit in TRCSR register is disabled 1: Interrupt request by IMFA bit in TRCSR register is enabled	R/W
b1	IMIEB	Input capture/compare match B interrupt enable bit	0: Interrupt request by IMFB bit in TRCSR register is disabled 1: Interrupt request by IMFB bit in TRCSR register is enabled	R/W
b2	IMIEC	Input capture/compare match C interrupt enable bit	0: Interrupt request by IMFC bit in TRCSR register is disabled 1: Interrupt request by IMFC bit in TRCSR register is enabled	R/W
b3	IMIED	Input capture/compare match D interrupt enable bit	0: Interrupt request by IMFD bit in TRCSR register is disabled 1: Interrupt request by IMFD bit in TRCSR register is enabled	R/W
b4	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b5	—			
b6	—			
b7	OVIE	Timer overflow interrupt enable bit	0: Interrupt request by OVF bit in TRCSR register is disabled 1: Interrupt request by OVF bit in TRCSR register is enabled	R/W

17.2.6 Timer RC Status Register (TRCSR)

Address 00145h (TRCSR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	OVF	—	—	—	IMFD	IMFC	IMFB	IMFA
After Reset	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture/compare match A flag	[Conditions for setting to 0] • When 0 is written to this bit after reading it as 1. (1) • Set to 0 by the DTC acknowledge when the DTC is activated by an IMFi interrupt (i = A to D). [Condition for setting to 1] • Refer to **Table 17.9 Conditions for Setting Each Flag to 1**.	R/W
b1	IMFB	Input capture/compare match B flag		R/W
b2	IMFC	Input capture/compare match C flag		R/W
b3	IMFD	Input capture/compare match D flag		R/W
b4	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b5	—			
b6	—			
b7	OVF	Timer overflow flag	[Condition for setting to 0] • When 0 is written to this bit after reading it as 1. [Condition for setting to 1] • Refer to **Table 17.9 Conditions for Setting Each Flag to 1**.	R/W

Note:
1. The results of writing this bit are as follows.
   - If the result of reading this bit is 1, writing 0 to this bit will set it to 0.
   - If the result of reading this bit is 0, writing 0 to this bit will not change its value. (If this bit changes from 0 to 1 after the read, the bit will remain 1 even if 0 is written.)
   - Writing 1 has no effect.

Table 17.9 Conditions for Setting Each Flag to 1

Symbol	Timer Mode		PWM Mode	PWM2 Mode
	Input Capture Function	Output Compare Function		
IMFA	When the value of the TRCCNT register is transferred to the TRCGRA register at the input edge (1) of the TRCIOA pin.	When the values of registers TRCCNT and TRCGRA match (compare match A)		
IMFB	When the value of the TRCCNT register is transferred to the TRCGRB register at the input edge (1) of the TRCIOB pin.	When the values of registers TRCCNT and TRCGRB match (compare match B).		
IMFC	When the value of the TRCCNT register is transferred to the TRCGRC register at the input edge (1) of the TRCIOC pin.	When the values of registers TRCCNT and TRCGRC match (compare match C). (2)		
IMFD	When the value of the TRCCNT register is transferred to the TRCGRD register at the input edge (1) of the TRCIOD pin.	When the values of registers TRCCNT and TRCGRD match (compare match D). (2)		
OVF	When the TRCCNT register overflows from FFFFh to 0000h.			

Notes:
1. The edge is selected by bits IOi0 to IOi1 (i = A to D) in registers TRCIO0 and TRCIOR1.
2. Includes when bits BUFEA and BUFEB in the TRCMR register are 1 (buffer registers for TRCGRA and TRCGRB).

17.2.7 Timer RC I/O Control Register 0 (TRCIOR0)

Address 00146h (TRCIOR0_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control A0 bit	[IOA2 = 0 (output compare register)]	R/W
b1	IOA1	TRCGRA control A1 bit	b1 b0 0 0: Pin output by compare match A is disabled 0 1: Low output from TRCIOA pin at compare match A 1 0: High output from TRCIOA pin at compare match A 1 1: Toggle output from TRCIOA pin at compare match A [IOA2 = 1 (input capture register)] b1 b0 0 0: Rising edge of TRCIOA pin 0 1: Falling edge of TRCIOA pin 1 0: Both edges of TRCIOA pin 1 1: Do not set.	R/W
b2	IOA2	TRCGRA control A2 bit (1, 2)	0: Output compare function 1: Input capture function	R/W
b3	IOA3	TRCGRA input-capture input switch bit	0: Input capture of fOCO128 1: Input capture of TRCIOA pin input	R/W
b4	IOB0	TRCGRB control B0 bit	[IOB2 = 0 (output compare register)]	R/W
b5	IOB1	TRCGRB control B1 bit	b5 b4 0 0: Pin output by compare match B is disabled 0 1: Low output from TRCIOB pin at compare match B 1 0: High output from TRCIOB pin at compare match B 1 1: Toggle output from TRCIOB pin at compare match B [IOB2 = 1 (input capture register)] b5 b4 0 0: Rising edge of TRCIOB pin 0 1: Falling edge of TRCIOB pin 1 0: Both edges of TRCIOB pin 1 1: Do not set.	R/W
b6	IOB2	TRCGRB control B2 bit (1, 2)	0: Output compare function 1: Input capture function	R/W
b7	—	Nothing is assigned. The write value must be 1. The read value is 1.		—

Notes:
1. When bits BUFEA and BUFEB in the TRCMR register are set to 1, registers TRCGRA and TRCGRC, and registers TRCGRB and TRCGRD are paired. The same values must be set in the IOA2 bit and the IOC2 bit in the TRCIOR1 register, and in the IOB2 bit and the IOD2 bit in the TRCIOR1 register, respectively.
2. When the input capture function is used, do not rewrite the TRCIOR0 register while the timer is counting.

The setting of the TRCIOR0 register is invalid in PWM mode and PWM2 mode. The written value is retained, but not reflected in control.

17.2.8 Timer RC I/O Control Register 1 (TRCIOR1)

Address 00147h (TRCIOR1_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control C0 bit	[IOC3 = 0 (general register for TRCIOA pin)] b1 b0 0 0: Pin output by compare match C is disabled 0 1: Low output from TRCIOA pin at compare match C 1 0: High output from TRCIOA pin at compare match C 1 1: Toggle output from TRCIOA pin at compare match C [IOC2 = 0, IOC3 = 1 (output compare register)] b1 b0 0 0: Pin output by compare match C is disabled 0 1: Low output from TRCIOC pin at compare match C 1 0: High output from TRCIOC pin at compare match C 1 1: Toggle output from TRCIOC pin at compare match C [IOC2 = 1, IOC3 = 1 (input capture register)] b1 b0 0 0: Rising edge of TRCIOC pin 0 1: Falling edge of TRCIOC pin 1 0: Both edges of TRCIOC pin 1 1: Do not set.	R/W
b1	IOC1	TRCGRC control C1 bit		R/W
b2	IOC2	TRCGRC control C2 bit (1, 2)	0: Output compare function 1: Input capture function	R/W
b3	IOC3	TRCGRC control C3 bit	0: Used as a general register for TRCIOA pin 1: Used as a general register for TRCIOC pin	R/W
b4	IOD0	TRCGRD control D0 bit	[IOD3 = 0 (general register for TRCIOB pin)] b5 b4 0 0: Pin output by compare match D is disabled 0 1: Low output from TRCIOB pin at compare match D 1 0: High output from TRCIOB pin at compare match D 1 1: Toggle output from TRCIOB pin at compare match D [IOD2 = 0, IOD3 = 1 ((output compare register)] b5 b4 0 0: Pin output by compare match D is disabled 0 1: Low output from TRCIOD pin at compare match D 1 0: High output from TRCIOD pin at compare match D 1 1: Toggle output from TRCIOD pin at compare match D [IOD2 = 1, IOD3 = 1 (input capture register)] b5 b4 0 0: Rising edge of TRCIOD pin 0 1: Falling edge of TRCIOD pin 1 0: Both edges of TRCIOD pin 1 1: Do not set.	R/W
b5	IOD1	TRCGRD control D1 bit		R/W
b6	IOD2	TRCGRD control D2 bit (1, 2)	0: Output compare function 1: Input capture function	R/W
b7	IOD3	TRCGRD control D3 bit	0: Used as a general register for TRCIOB pin 1: Used as a general register for TRCIOD pin	R/W

Notes:
1. When bits BUFEA and BUFEB in the TRCMR register are set to 1, registers TRCGRA and TRCGRC, and registers TRCGRB and TRCGRD are paired. The same values must be set in the IOC2 bit and the IOA2 bit in the TRCIOR0 register, and in the IOD2 bit and the IOB2 bit in the TRCIOR0 register, respectively.
2. When the input capture function is used, do not rewrite the TRCIOR1 register while the timer is counting.

The setting of the TRCIOR1 register is invalid in PWM mode and PWM2 mode. The written value is retained, but not reflected in control.

17.2.9 Timer RC Control Register 2 (TRCCR2)

Address 00148h (TRCCR2_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSTP	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	TRCIOB PWM mode output level control bit (1)	0: Output level is active low 1: Output level is active high	R/W
b1	POLC	TRCIOC PWM mode output level control bit (1)		R/W
b2	POLD	TRCIOD PWM mode output level control bit (1)		R/W
b3	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b4	—			
b5	CSTP	Count stop bit (2)	0: Count is continued even after compare match with TRCGRA register 1: Count is stopped at compare match with TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bits (3)	b7 b6 0 0: TRCTRG input disabled 0 1: Rising edge 1 0: Falling edge 1 1: Both rising and falling edges	R/W
b7	TCEG1			R/W

Notes:
1. Enabled in PWM mode.
2. Enabled in the output compare function, PWM mode, and PWM2 mode. For notes on PWM2 mode, refer to **17.7.6 TRCMR Register in PWM2 Mode**.
3. Enabled in PWM2 mode.

CSTP Bit (Count stop bit)

The following shows the count stop conditions for each mode.

Count stop conditions

[In the output compare function]
- When the CSTP bit in the TRCCR2 register is 1 (count stops at compare match with TRCGRA register)
- The count stops at a compare match with the TRCGRA register. The output-compare output pin retains the level after the output change due to the compare match.

[In PWM mode]
- When the CSTP bit in the TRCCR2 register is 1 (count stops at compare match with TRCGRA register)
- The count stops at a compare match with the TRCGRA register. The PWM output pin retains the level after the output change due to the compare match.

[In PWM2 mode]
- When the CSTP bit in the TRCCR2 register is 1, the count stops at a compare match with the TRCGRA register)
- The TRCIOB pin outputs the initial level.
- When the CCLR bit in the TRCCR1 register is 0, the TRCCNT register retains the value before the count stops.
- When the CCLR bit in the TRCCR1 register is 1, the TRCCNT register is set to 0000h.

17.2.10 Timer RC Digital Filter Function Select Register (TRCDF)

Address 00149h (TRCDF_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DFCK1	DFCK0	—	DFTRG	DFD	DFC	DFB	DFA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRCIOA digital filter function bit (1)	0: Function is not used. 1: Function is used.	R/W
b1	DFB	TRCIOB digital filter function bit (1)		R/W
b2	DFC	TRCIOC digital filter function bit (1)		R/W
b3	DFD	TRCIOD digital filter function bit (1)		R/W
b4	DFTRG	TRCTRG digital filter function bit (1, 2)		R/W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	DFCK0	Digital filter clock select bits (1, 2)	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits CKS0 to CKS2 in the TRCCR1 register)	R/W
b7	DFCK1			R/W

Notes:
1. Enabled in the input capture function.
2. Enabled when in PWM2 mode and bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger input enabled).

17.2.11 Timer RC Output Enable Register (TRCOER)

Address 0014Ah (TRCOER_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PTO	—	—	—	ED	EC	EB	EA
After Reset	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	EA	TRCIOA output disable bit (1)	[When the OPE bit in the TRCOPR register is 0 (output waveform manipulation disabled)] 0: TRCIOi pin (i = A or B) output enabled according to settings of registers TRCMR and TRCIOR0 1: TRCIOi pin output disabled (TRCIOi pin is used as a programmable I/O port) regardless of settings of registers TRCMR and TRCIOR0 [When the OPE bit in the TRCOPR register is 1 (output waveform manipulation enabled)] 0: TRCIOi pin output enabled according to settings of registers TRCMR and TRCIOR0 1: TRCIOi pin output level is fixed depending on setting of TRCOPR register	R/W
b1	EB	TRCIOB output disable bit (1)		R/W
b2	EC	TRCIOC output disable bit (1)	[When the OPE bit in the TRCOPR register is 0 (output waveform manipulation disabled)] 0: TRCIOk pin (k = C or D) output enabled according to settings of registers TRCMR and TRCIOR1 1: TRCIOk pin output disabled (TRCIOi pin is used as a programmable I/O port) regardless of settings of registers TRCMR and TRCIOR1 [When the OPE bit in the TRCOPR register is 1 (output waveform manipulation enabled)] 0: TRCIOk pin (k = C or D) output enabled according to settings of registers TRCMR and TRCIOR1 1: TRCIOk pin output level is fixed depending on setting of TRCOPR register	R/W
b3	ED	TRCIOD output disable bit (1)		R/W
b4	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b5	—			
b6	—			
b7	PTO	Timer output disable bit	[When the OPE bit in the TRCOPR register is 0 (output waveform manipulation disabled)] 0: Timer output disabled is invalid 1: Timer output disabled is valid (when a low level is input to the INT0 pin, bits EA to ED are set to 1 (output disabled)) For details on INT0, refer to **11. Interrupts**. [When the OPE bit in the TRCOPR register is 1 (output waveform manipulation enabled)] The function of the PTO bit is disabled. This bit can be read or written.	R/W

Note:
1. Disabled when the corresponding pin is used as input capture input.

17.2.12 Timer RC A/D Conversion Trigger Control Register (TRCADCR)

Address 0014Bh (TRCADCR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	ADTRGDE	ADTRGCE	ADTRGBE	ADTRGAE
After Reset	1	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGAE	TRCGRA A/D conversion start trigger enable bit	0: No A/D conversion start trigger generated at compare match A 1: An A/D conversion start trigger generated at compare match A	R/W
b1	ADTRGBE	TRCGRB A/D conversion start trigger enable bit	0: No A/D conversion start trigger generated at compare match B 1: An A/D conversion start trigger generated at compare match B	R/W
b2	ADTRGCE	TRCGRC A/D conversion start trigger enable bit	0: No A/D conversion start trigger generated at compare match C 1: An A/D conversion start trigger generated at compare match C	R/W
b3	ADTRGDE	TRCGRD A/D conversion start trigger enable bit	0: No A/D conversion start trigger generated at compare match D 1: An A/D conversion start trigger generated at compare match D	R/W
b4	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b5	—			
b6	—			
b7	—			

The TRCADCR register is used to select the A/D conversion start trigger source. At the corresponding compare match, an A/D conversion start trigger is generated.

17.2.13 Timer RC Output Waveform Manipulation Register (TRCOPR)

Address 0014Ch (TRCOPR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	OPE	RESTATS	OPOL1	OPOL0	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	OPOL0	Waveform output manipulation period output level select bits (1)	b3 b2 0 0: When pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD are set to be pulled down externally, output level of each pin is fixed to high impedance 0 1: When pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD are set to be pulled up externally, output level of each pin is fixed to high impedance 1 0: Output level of pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD is fixed to low during waveform output manipulation period 1 1: Output level of pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD is fixed to high during waveform output manipulation period	R/W
b3	OPOL1			R/W
b4	RESTATS	Output restart method select bit (1)	0: Output waveform manipulation is stopped by software and output is restarted 1: Automatic output waveform manipulation is stopped and automatic output is restarted	R/W
b5	OPE	Waveform output manipulation enable bit (1)	0: Waveform output manipulation disabled 1: Waveform output manipulation enabled	R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

Note:
1. Do not rewrite the TRCOPR register during count operation.

RESTATS Bit (Output restart method select bit)

When the OPE bit is 1 or the RESTATS bit is 0 (output waveform manipulation is stopped by software, output is restarted), bits EA to ED in the TRCOER register must be set to 0 by software. Even if the waveform output manipulation event is cancelled, bits EA to ED do not automatically change to 0.

When the OPE bit is 1 or the RESTATS bit is 1 (automatic output waveform manipulation is stopped, automatic output is restarted), if the waveform output event is cancelled, bits EA to ED automatically change to 0.

OPE Bit (Waveform output manipulation enable bit)

When the OPE bit is 1 (waveform output manipulation enabled), if a waveform output manipulation event is input, bits EA to ED in the TRCOER register are set to 1 (fixed-level output depending on setting of TRCOPR register).

When the OPE bit is 0 (waveform output manipulation disabled), bits EA to ED in the TRCOER register are not affected by the setting of this bit.

When the OPE bit is 0, the waveform output of timer RC is manipulated by setting the TRCOER register only.

When the OPE bit is 1, the waveform output of timer RC is manipulated by setting the TRCOER register regardless of the setting of the PTO bit in the TRCOER register. Bits EA to ED in the TRCOER register are used as the flags for waveform output manipulation. When a waveform output manipulation event is input, bits EA to ED are set to 1.

17.2.14 Timer RC ELC Cooperation Control Register (TRCELCCR)

Address 0014Dh (TRCELCCR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	ELCICE	ELCP2TE	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	ELCP2TE	Input trigger select bit for PWM2 mode	0: TRCTRG pin input 1: Event input from ELC	R/W
b2	ELCICE	TRCGRD input capture signal select bit	0: TRCIOD pin input 1: Event input from ELC	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

ELCP2TE Bit (Input trigger select bit for PWM2 mode)

- When the ELCP2TE bit is 1
  Event input from the ELC is the input trigger in PWM2 mode, regardless of the settings of bits TCEG0 and TCEG1 in the TRCCR2 register
- When the ELCP2TE bit is 0
  TRCTRG input is the input trigger in PWM2 mode, according to the settings of bits TCEG0 and TCEG1 in the TRCCR2 register

ELCICE Bit (TRCGRD input capture signal select bit)

- When bits IOD3 and IOD2 in the TRCIOR1 register are 1 and the ELCICE bit is 1
  The rising edge of event input from the ELC is captured.
- When the ELCICE bit is 0
  The active edge of the TRCIOD pin input is decided by the settings of the TRCIOR1 register.

17.3 Operation

Table 17.10 lists the Timer RC Operating Modes.

Table 17.10 Timer RC Operating Modes

Item	Description
Timer mode	Timer mode is used by setting the PWM2 bit to 0 and bits PWMB to PWMD to 0 in the TRCMR register. In this case, the output compare function or input capture function is used by setting bits IOA0 to IOA2 and IOB0 to IOB2 in the TRCIOR0 register and bits IOC0 to IOC2 and IOD0 to IOD2 in the TRCIOR1 register.
PWM mode	PWM mode is used by setting the PWM2 bit to 0 and bits PWMB to PWMD to 1 in the TRCMR register.
PWM2 mode	PWM2 mode is used by setting the PWM2 bit in the TRCMR register to 1.

Tables 17.11 to 17.14 list the settings of pins TRCIOA to TRCIOD. For the assignments of pins TRCIOA to TRCIOD, refer to **14. I/O Ports**.

Table 17.11 TRCIOA Pin Settings

Register	TRCOER	TRCMR	TRCIOR0			Function
Bit	EA	PWM2	IOA2	IOA1	IOA0	
Setting value	0	1	0	0	1	Timer mode waveform output (output compare function)
				1	X	
	X	1	1	X	X	Timer mode (input capture function)
	Other than the above					I/O port

X: 0 or 1

Table 17.12 TRCIOB Pin Settings

Register	TRCOER	TRCMR		TRCIOR0			Function
Bit	EB	PWM2	PWMB	IOB2	IOB1	IOB0	
Setting value	0	0	X	X	X	X	PWM2 mode waveform output
	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer mode waveform output (output compare function)
					1	X	
	X	1	0	1	X	X	Timer mode (input capture function)
	Other than the above						I/O port

X: 0 or 1

Table 17.13 TRCIOC Pin Settings

Register	TRCOER	TRCMR		TRCIOR1			Function
Bit	EC	PWM2	PWMC	IOC2	IOC1	IOC0	
Setting value	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer mode waveform output (output compare function)
					1	X	
	X	1	0	1	X	X	Timer mode (input capture function)
	PWM2 = 1 and other than the above						I/O port

X: 0 or 1

Table 17.14 TRCIOD Pin Settings

Register	TRCOER	TRCMR		TRCIOR1			Function
Bit	ED	PWM2	PWMD	IOD2	IOD1	IOD0	
Setting value	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer mode waveform output (output compare function)
					1	X	
	X	1	0	1	X	X	Timer mode (input capture function)
	PWM2 = 1 and other than the above						I/O port

X: 0 or 1

17.3.1 Timer Mode

17.3.1.1 Free-Running Operation

The TRCCNT register performs free-running or period count operations. Immediately after a reset, the TRCCNT register functions as a free-running counter. When the CTS bit in the TRCMR register is set to 1 (count starts), count operation is started. When the TRCCNT register overflows from FFFFh to 0000h, the OVF bit in the TRCSR register is set to 1, and a timer RC interrupt is generated if the OVIE bit in the TRCIER register is 1 (interrupt request by OVF bit is enabled).
Figure 17.2 shows an Example of Free-Running Counter Operation.

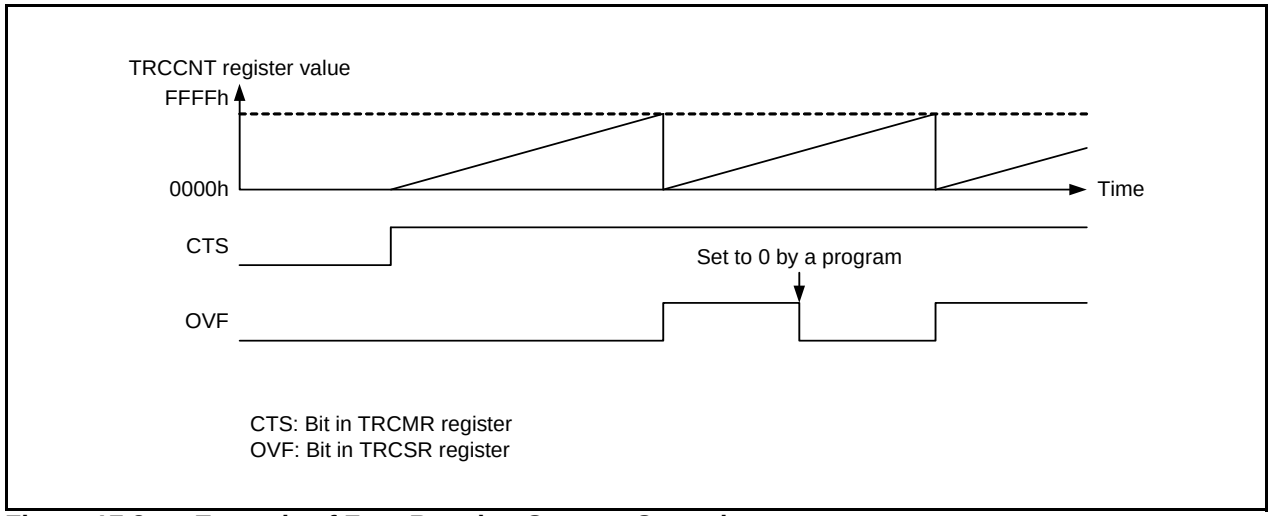


Figure 17.2 Example of Free-Running Counter Operation

17.3.1.2 Period Count Operation

When the TRCGRA register for period setting is set to any value and the CCLR bit in the TRCCR1 register is set to 1, a period count operation is performed. When the count value matches the TRCGRA register, the TRCCNT register is set to 0000h and the IMFA bit in the TRCSR register is set to 1. If the corresponding IMIEA bit in the TRCIER register is 1 (interrupt request by IMFA bit is enabled) at this time, an interrupt request is generated. When the CSTP bit in the TRCCR2 register is 0, the TRCCNT register continues increment operation from 0000h. When the CSTP bit in the TRCCR2 register is 1, the TRCCNT register stops increment operation from 0000h.
Figure 17.3 shows an Example of Period Counter Operation.

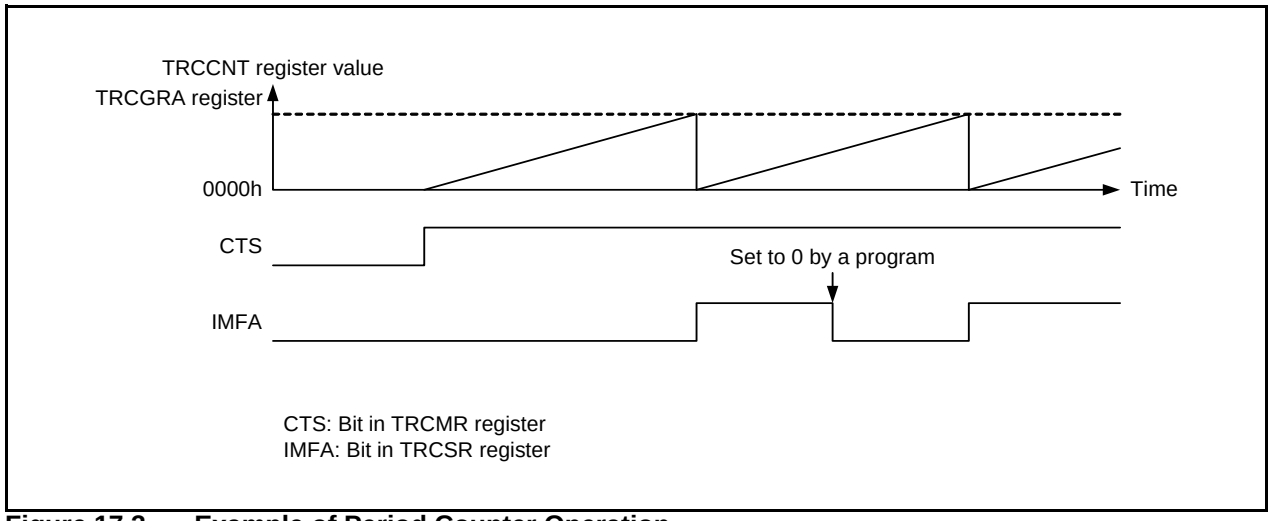


Figure 17.3 Example of Period Counter Operation

17.3.1.3 Output Compare Function

By setting the general register as an output compare register, low-level, high-level, or toggle output is performed at compare matches A to D from pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD.
For the output level of pins TRCIOA to TRCIOD, the initial output level can be set by bits TOA to TOD in the TRCCR1 register, and the active level and toggle output can be set by bits IOA0, IOA1, IOB0, and IOB1 in the TRCIOR0 register and bits IOC0, IOC1, IOD0, and IOD1 in the TRCIOR1 register.
Figure 17.4 shows a Low Output and High Output Operation Example. The TRCCNT register is used for the free-running count operation, a low level is output at compare match B, and a high level is output at compare match A. When the set level and the pin level are the same, the pin level remains unchanged.

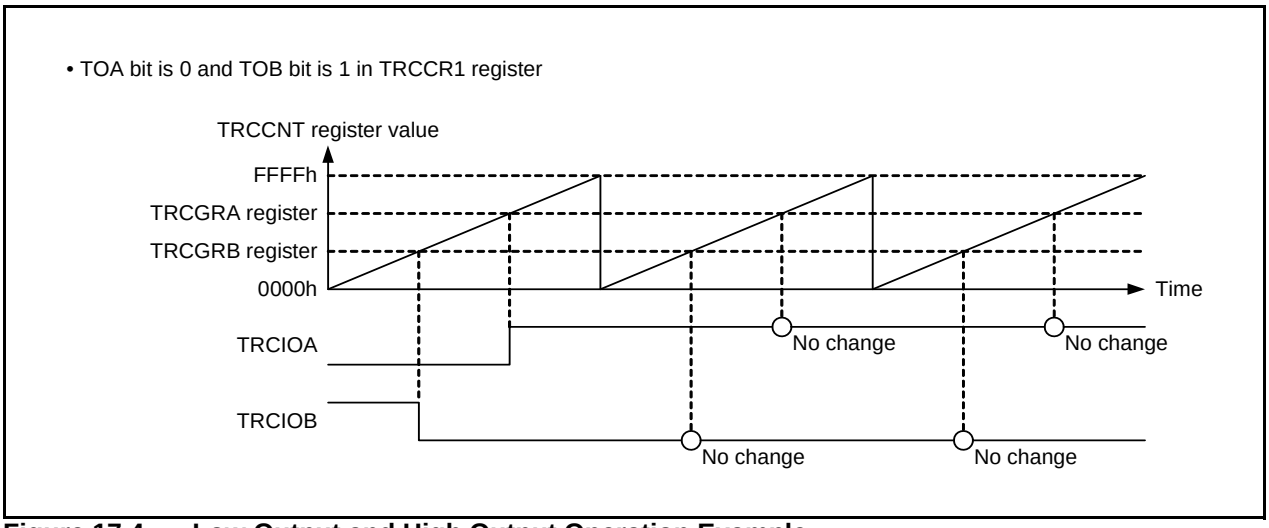


Figure 17.4 Low Output and High Output Operation Example

Figure 17.5 shows an Example of Toggle Output Operation during Free-Running Count. The TRCCNT register is used for the free-running count operation, and toggle output is performed at compare matches A and B.

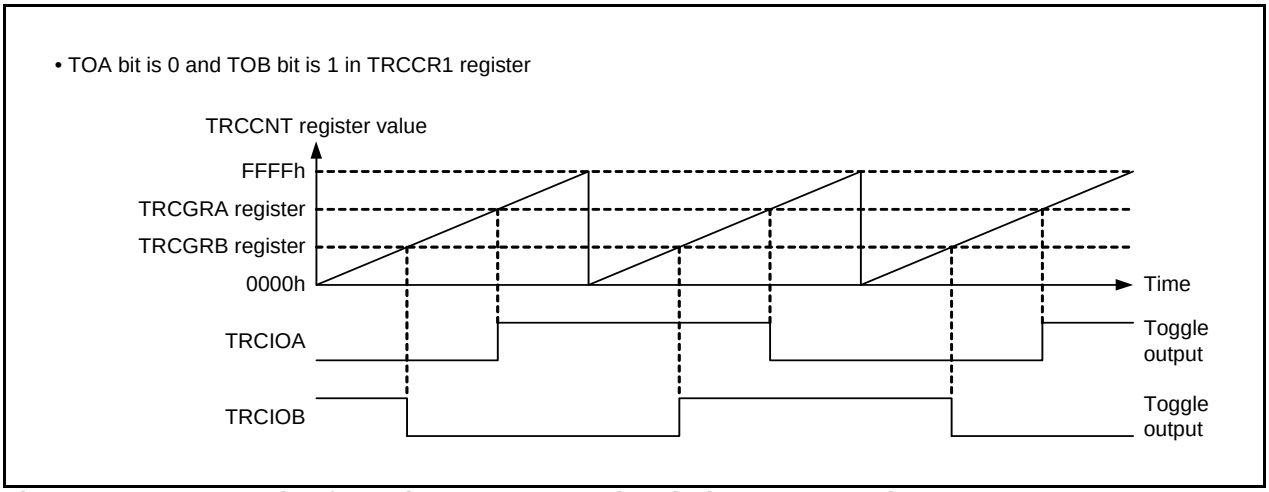


Figure 17.5 Example of Toggle Output Operation during Free-Running Count

Figure 17.6 shows an Example of Toggle Output Operation during Period Count. The TRCCNT register is used for the period count operation, and toggle output is performed at compare matches A and B.

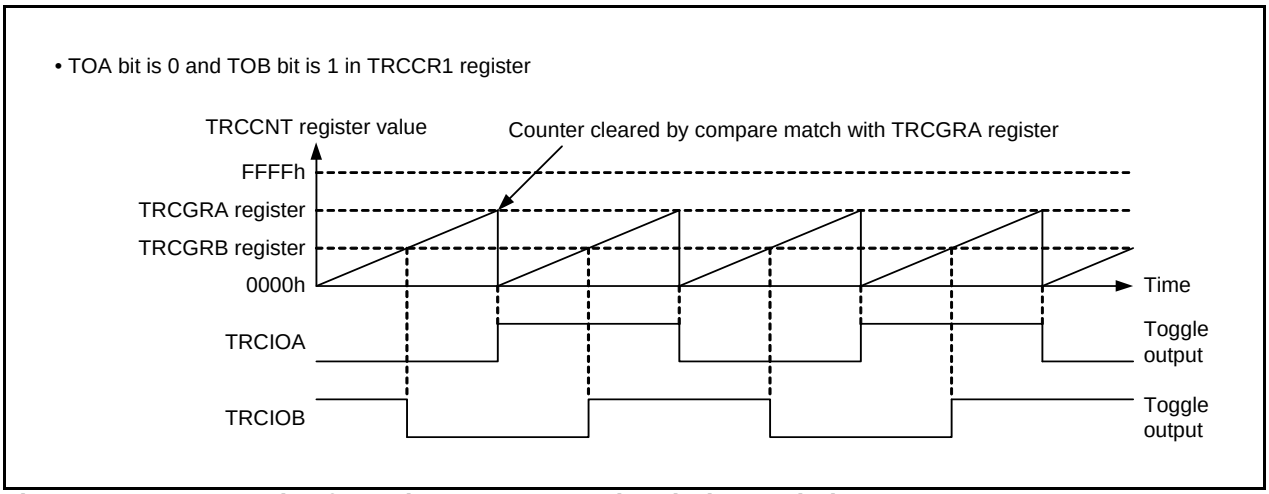


Figure 17.6 Example of Toggle Output Operation during Period Count

17.3.1.4 Input Capture Function

The input capture function can be used to measure the pulse width or period.

By setting the general register to be an input capture register, the value in the TRCCNT register on input edge detection of pins TRCIOA to TRCIOD is transferred to registers TRCGRA to TRCGRD. When the input capture function is used, the input edge of pins TRCIOA to TRCIOD can set to any of rising edge, falling edge, or both edges, using the corresponding bits (bits IOA0, IOA1, IOB0, and IOB1 in the TRCIOR0 register and bits IOC0, IOC1, IOD0, and IOD1 in the TRCIOR1 register).

By using the input capture function, the measurement result of the period or pulse width can be calculated from the value stored in registers TRCGRA to TRCGRD.

Figure 17.7 shows an Input Capture Operation Example. The TRCCNT register is used for the free-running operation, and both edges are selected for the input-capture input to the TRCIOA pin and a falling edge is selected for the input-capture input to the TRCIOB pin.

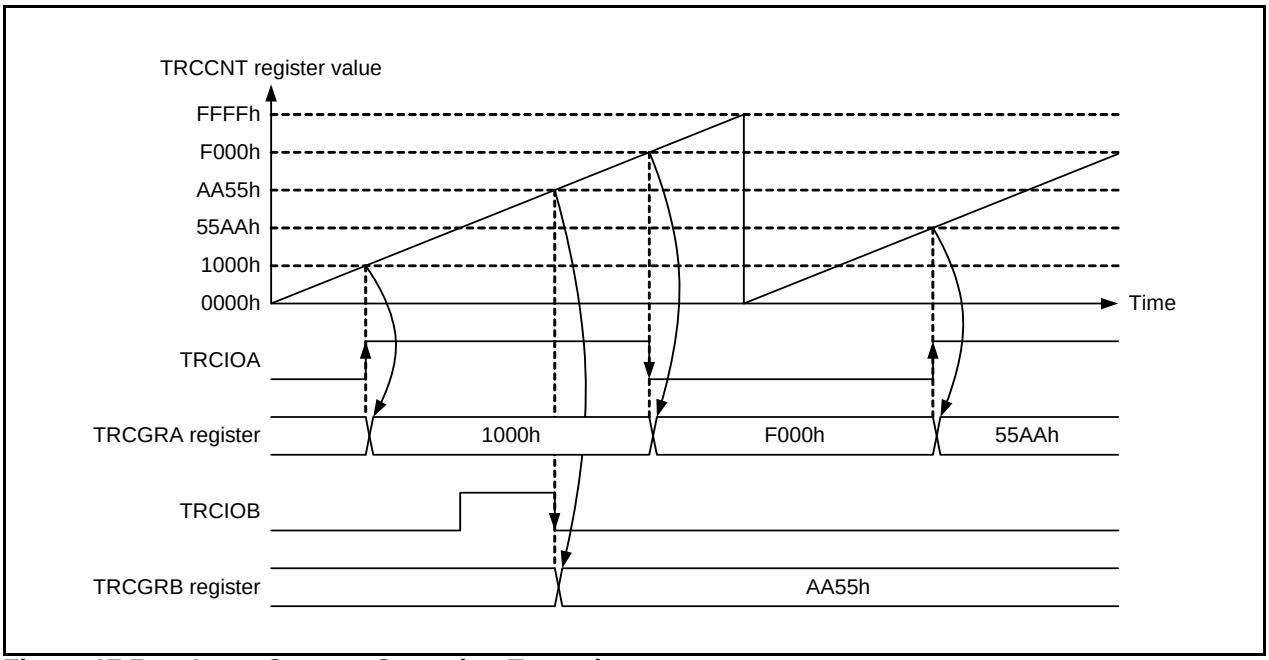


Figure 17.7 Input Capture Operation Example

Figure 17.8 shows an Example of Buffer Operation during Input Capture. This example applies when the TRCGRA register is set as an input capture register and the TRCGRC register is set as a buffer register for the TRCGRA register. In this example, the TRCCNT register is used for the free-running count operation and both rising and falling edges are selected for the input-capture input to the TRCIOA pin. Since buffer operation is set, the value of the TRCCNT register is stored in the TRCGRA register by input capture (upon detecting the input edge of the input capture pin), and the value that has been stored in the TRCGRA register is transferred to the TRCGRC register at the same time.

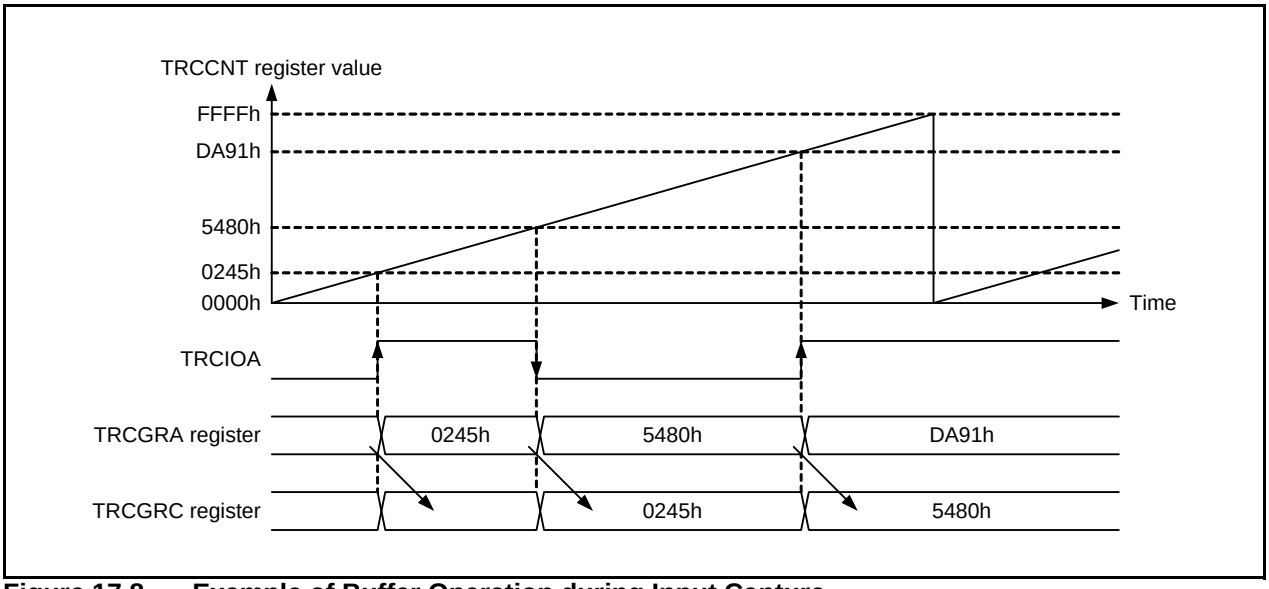


Figure 17.8 Example of Buffer Operation during Input Capture

17.3.2 PWM Mode

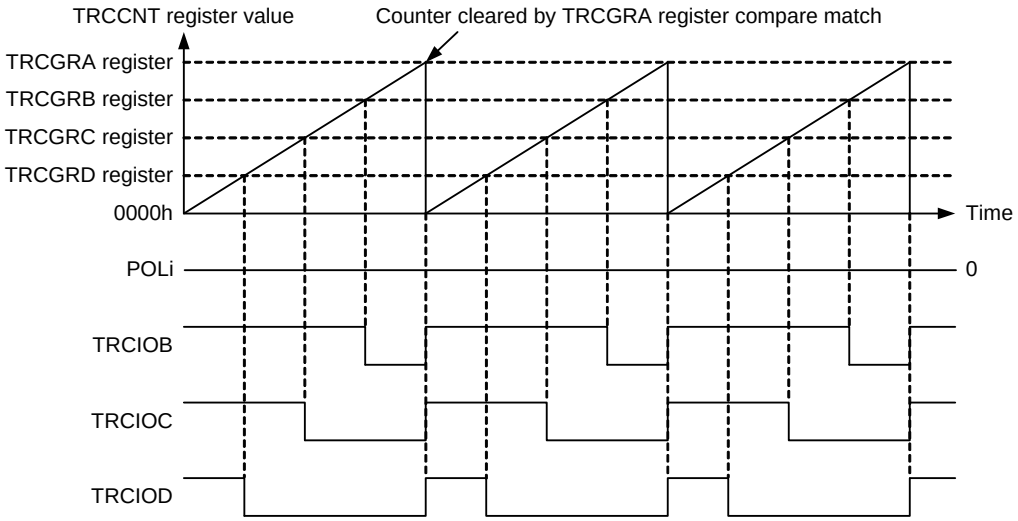
In PWM mode, when the TRCGRA register is set as the period register and registers TRCGRB, TRCGRC, and TRCGRD are set as the duty registers, a PWM waveform is output from pins TRCIOB, TRCIOC, and TRCIOD individually. Up to three PWM outputs can be performed when the buffer function is not used. In this mode, the general register functions as an output compare register. The settings of bits IOB2, IOC2, and IOD2 are invalid. The initial output level of the corresponding pin is set according to the set values of bits TOA to TOD in the TRCCR1 register and bits POLB to POLD in the TRCCR2 register.
For TRCIOB, TRCIOC, and TRCIOD output, if the initial value until compare match is the same as the set value for the active polarity at compare match, the compare match output is actually performed, but because the output value does not change during output it will appear as if the initial value were retained.
Table 17.15 lists the Initial Output Level of TRCIOB Pin. The same applies to the initial output level of pins TRCIOC and TRCIOD.

Table 17.15 Initial Output Level of TRCIOB Pin

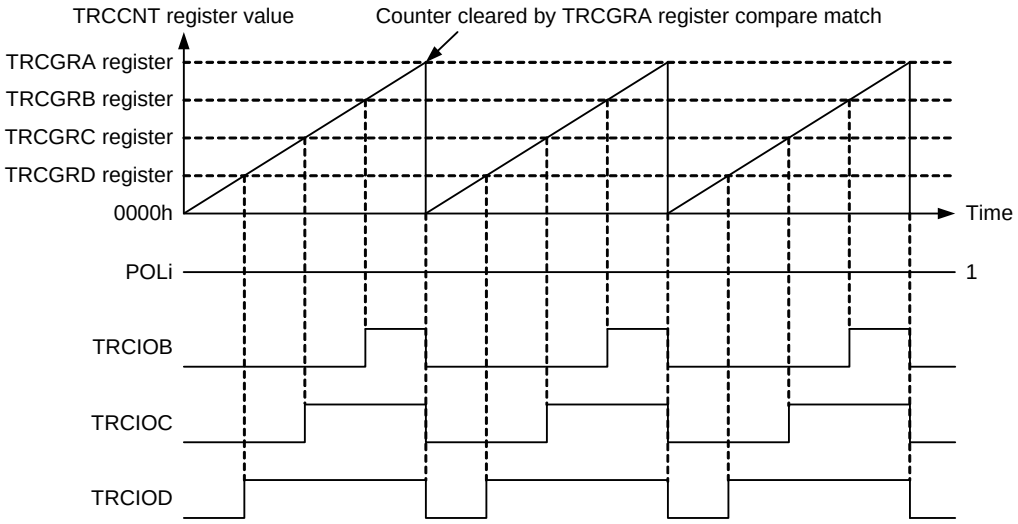
TOB Bit in TRCCR1 Register	POLB Bit in TRCCR2 Register	Initial Output Level
0	0	1
	1	0
1	0	0
	1	1

The output level is determined by bits POLB to POLD. When the POLB bit is 0 (output level is active low), the TRCIOB output pin is set to low at compare match B and high at compare match A. When the POLB bit is 1 (output level is active high), the TRCIOB output pin is set to high at compare match B and low at compare match A.
The setting values of bits PWMD to PWMB in TRCMR take precedence over those in registers TRCIOR0 and TRCIOR1. When the values set in the period and duty registers are the same, the output value remains unchanged even if a compare match occurs.
Figure 17.9 shows an Operation Example in PWM Mode.

• High output when TRCCNT register is cleared at compare match A. Low output at compare matches B, C, and D. (POLB bit = 0, POLC bit = 0, and POLD bit = 0 in TRCCR2 register)



• Low output when TRCCNT register is cleared at compare match A. High output at compare matches B, C, and D. (POLB bit = 1, POLC bit = 1, and POLD bit = 1 in TRCCR2 register)



i = B, C, or D

Figure 17.9 Operation Example in PWM Mode

Figure 17.10 shows an Example of Buffer Operation during Output Compare. In this example, the TRCIOB pin is set to PWM mode and the TRCGRD register is set as the buffer register for the TRCGRB register. The TRCCNT register is cleared by compare match A, and the output is set to low at compare match A and high at compare match B.
Since buffer operation is set, the output is changed when compare match B occurs, and the value in the buffer register TRCGRD is transferred to the TRCGRB register at the same time. This operation is repeated each time compare match B occurs.

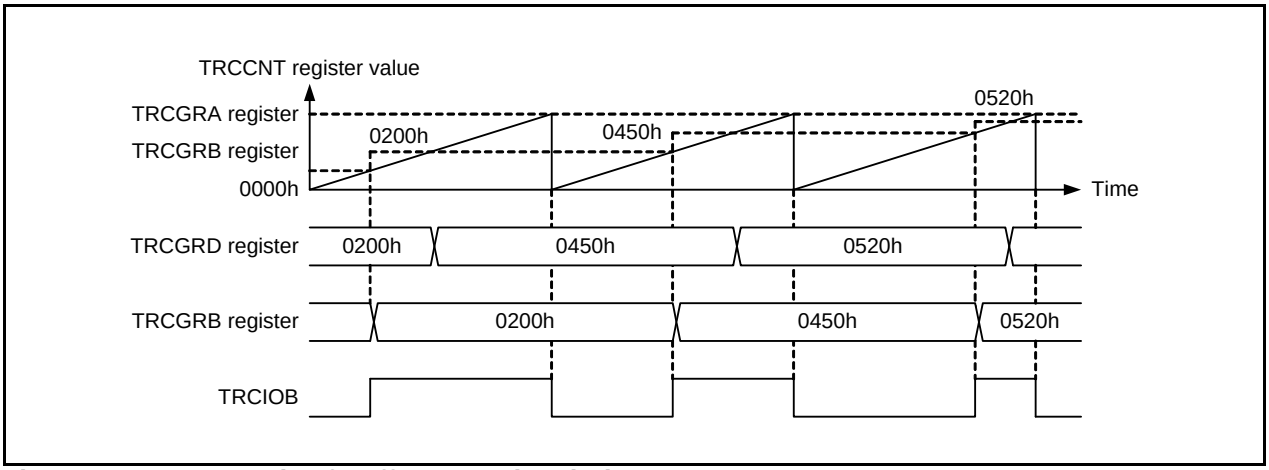
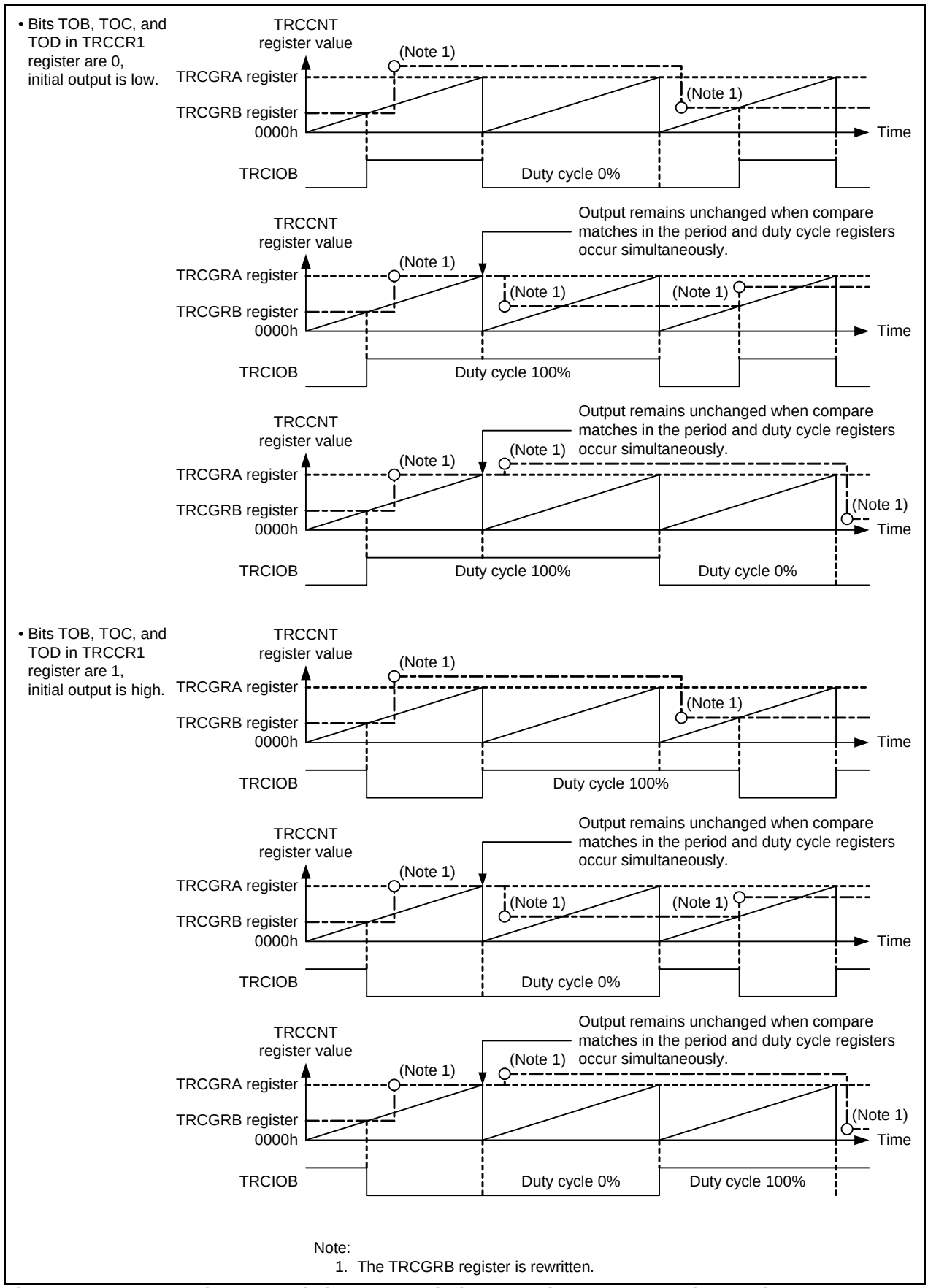


Figure 17.10 Example of Buffer Operation during Output Compare

Figure 17.11 shows an Operation Example in PWM Mode (Duty Cycle 0%, Duty Cycle 100%).



Note:
1. The TRCGRB register is rewritten.

Figure 17.11 Operation Example in PWM Mode (Duty Cycle 0%, Duty Cycle 100%)

17.3.3 PWM2 Mode

Unlike PWM mode, in PWM2 mode, a PWM waveform is output from the TRCIOB pin at a compare match between the count value of the TRCCNT register and registers TRCGRB and TRCGRC. When the BUFEB bit in the TRCMR register is set to 1 (TRCGRD register is used as a buffer register for TRCRGB register), the TRCGRD register functions as a buffer register for the TRCGRB register. The output level is determined by the TOB bit in the TRCCR1 register.

When the TOB bit is 0 (output value is low), a low level is output at a compare match with the TRCGRB register and a high level is output at a compare match with the TRCGRC register. When the TOB bit is 1 (output value is high), a high level is output at a compare match with the TRCGRB register and a low level is output at a compare match with the TRCGRC register.

Table 17.16 lists the Combinations of Pin Functions and General Registers for PWM2 Mode. Figure 17.12 shows the PWM2 Mode Block Diagram. Figure 17.13 shows the Timing of Buffer Operations for Registers TRCGRD and TRCGRB in PWM2 Mode.

The value in the TRCGRD register is transferred to the TRCGRB register and the counter is cleared by a compare match with the TRCGRA register. However, the counter is cleared only when the CCLR bit in the TRCCR1 register is set to 1 (TRCCNT counter is cleared by input capture/compare match A). Also, when trigger input is enabled by bits TCEG0 and TCEG1 in the TRCCR2 register in PWM2 mode, the value in the TRCGRD register is transferred to the TRCGRB register and the counter is cleared by a trigger. The timer I/O pins that are not used in PWM2 mode can be used as I/O ports.

Table 17.16 Combinations of Pin Functions and General Registers for PWM2 Mode

Pin Name	Pin Function	Usable General Register	Function of General Register
TRCIOA	Port function/TRCTRG input	—	—
TRCIOB	Timer RC PWM output	TRCGRA register TRCGRB register TRCGRC register TRCGRD register (arbitrary)	Period setting Duty cycle setting: Change to inactive level Duty cycle setting: Change to active level TRCGRB buffer register (arbitrary)
TRCIOC	Port function	—	—
TRCIOD	Port function	—	—

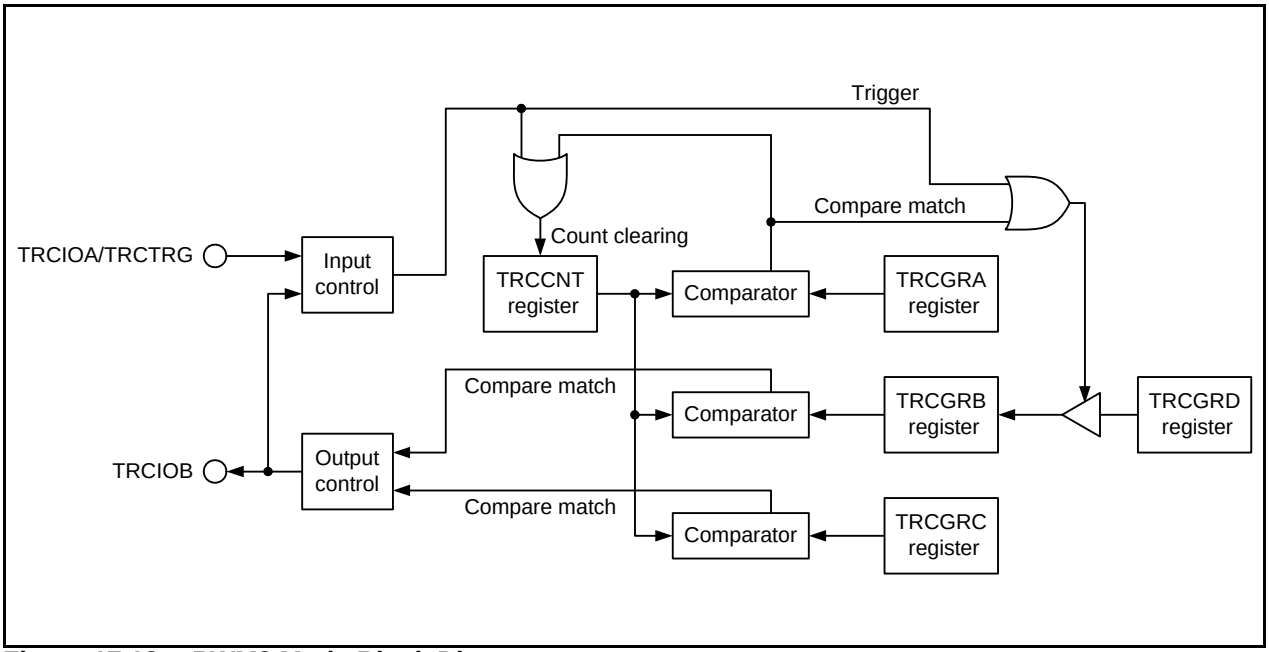


Figure 17.12 PWM2 Mode Block Diagram

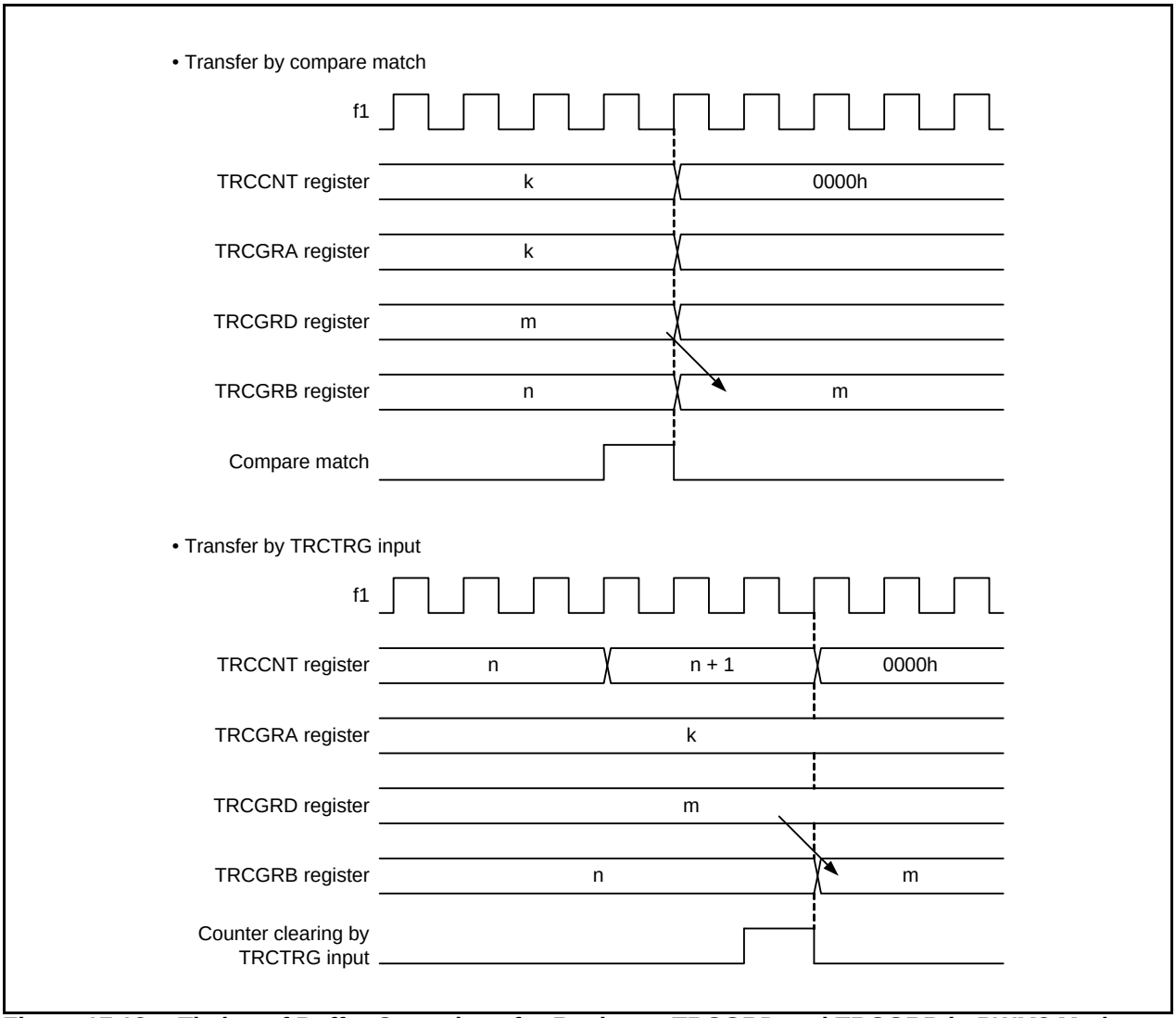


Figure 17.13 Timing of Buffer Operations for Registers TRCGRD and TRCGRB in PWM2 Mode

In PWM2 mode, the TRCTRG input is used to output a pulse with an arbitrary delay time and width from the TRCIOB pin. The active edge for the TRCTRG input is selected to be a rising edge, falling edge, or both edges, using bits TCEG0 and TCEG1 in the TRCCR2 register.

Set bits TCEG1 and TCEG0 in the TRCCR2 register to 10b (falling edge) to set the falling edge for the TRCTRG input. Set the CSTP bit in the TRCCR2 register to 0 (count is continued even after compare match with TRCGRA register) to continue incrementing when compare match A with the TRCGRA register occurs. Set the BUFEB bit in the TRCMR register to 1 (TRCGRD register is used as a buffer register for TRCRGB register) to set the TRCGRD register as the buffer register. Set the TOB bit in the TRCCR1 register to 0 (output value is low) or 1 (output value is high) to set the initial level of the output level to 0 or 1. Next, set the CCLR bit in the TRCCR1 register to 1 (TRCCNT counter is cleared by input capture/compare match A) to clear the TRCCNT register by compare match A.

Figure 17.14 shows an Operation Example in PWM2 Mode when TRCTRG Input is Enabled, and Figure 17.15 shows an Operation Example in PWM2 Mode when TRCTRG Input is Disabled by the above setting. These examples apply when the PWM2 bit in the TRCMR register is set to 0 (PWM2 mode) and a waveform is output from the TRCIOB pin.

In PWM2 mode, when the TOB bit in the TRCCR1 register is 0 (output value is low), the TRCTRG input edge is disabled while a high level is output from the TRCIOB pin. Likewise, when the TOB bit is 1 (output value is high), the TRCTRG input edge is disabled while a low level is output from the TRCIOB pin. In addition, transfer from registers TRCGRD to TRCGRB is performed when a compare match with the TRCGRA register or TRCTRG input occurs. However, if the TRCTRG input is disabled depending on the level of the TRCIOB pin, transfer from registers TRCGRD to TRCGRB is not performed.

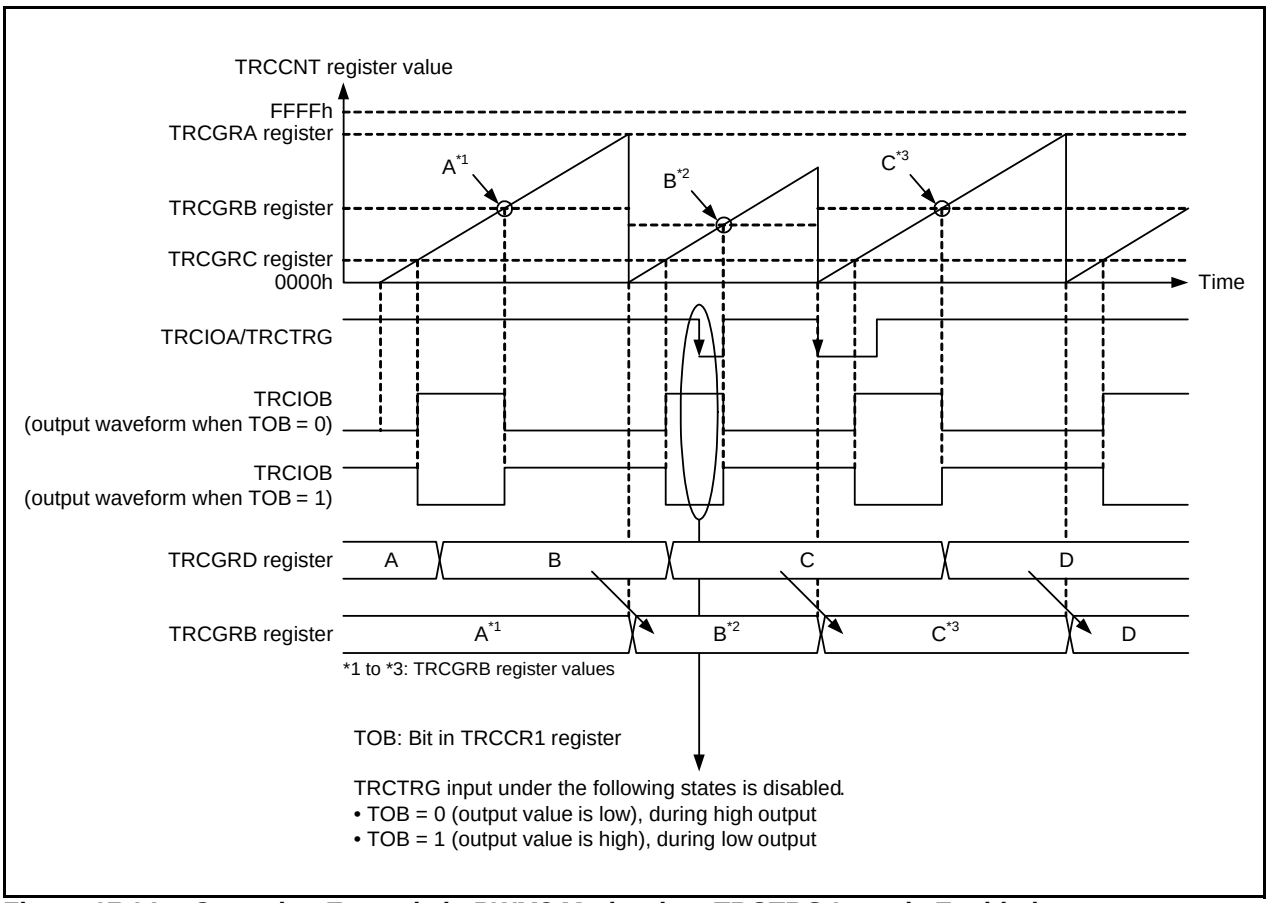


Figure 17.14 Operation Example in PWM2 Mode when TRCTRG Input is Enabled

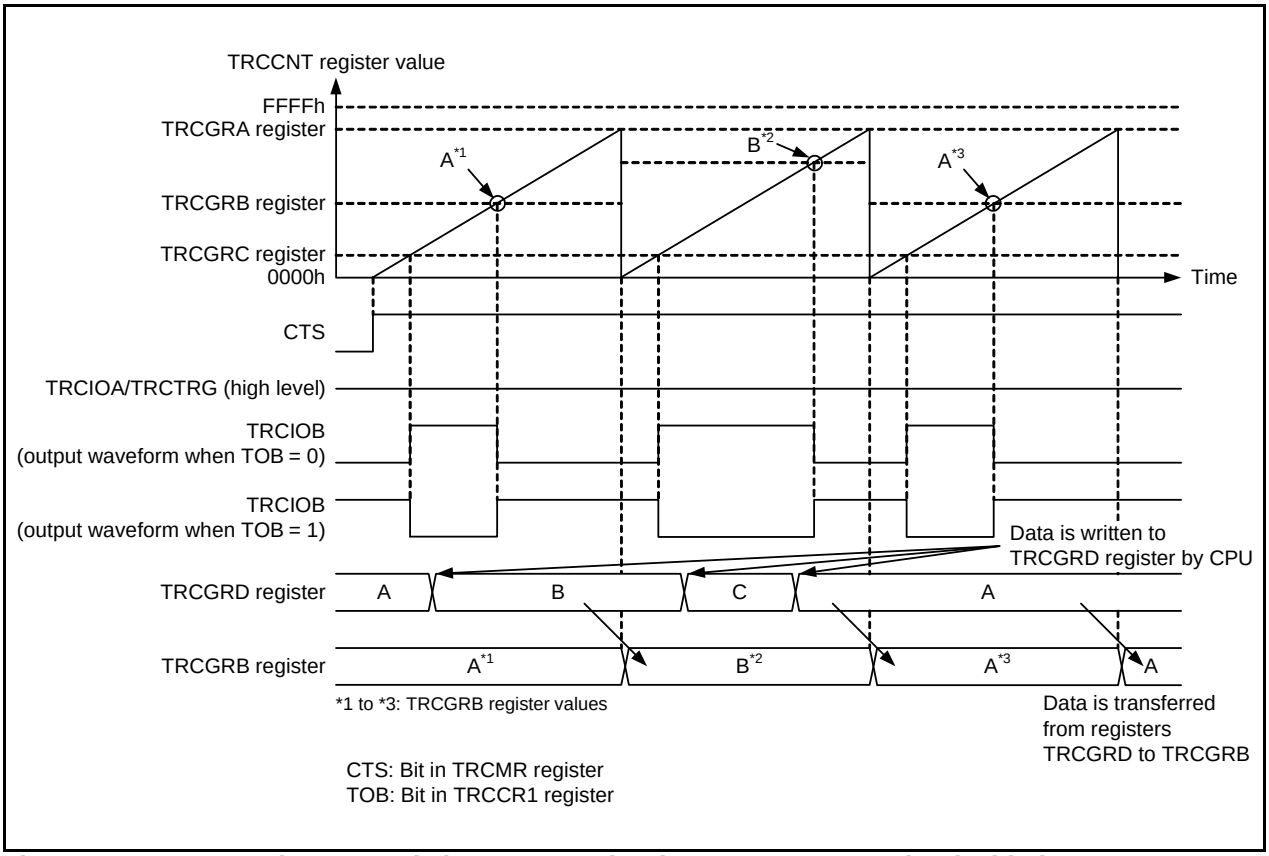


Figure 17.15 Operation Example in PWM2 Mode when TRCTRG Input is Disabled

Figure 17.16 shows an Example of Count Stop Operation in PWM2 Mode. In this example, the TOB bit in the TRCCR1 register is set to 0 (output value is low) and the TOB bit is set to 1 (output value is high).
By setting the CSTP bit in the TRCCR2 register to 1 (count is stopped at compare match with TRCGRA register) and the CCLR bit in the TRCCR1 register to 1 (TRCCNT counter is cleared by input capture/compare match A), the counter is changed to 0000h and stopped by the compare match between registers TRCCNT and TRCGRA. By setting the CTS bit in the TRCMR register to 0 (count stops), the counter is forcibly stopped and the output is set to the initial level.

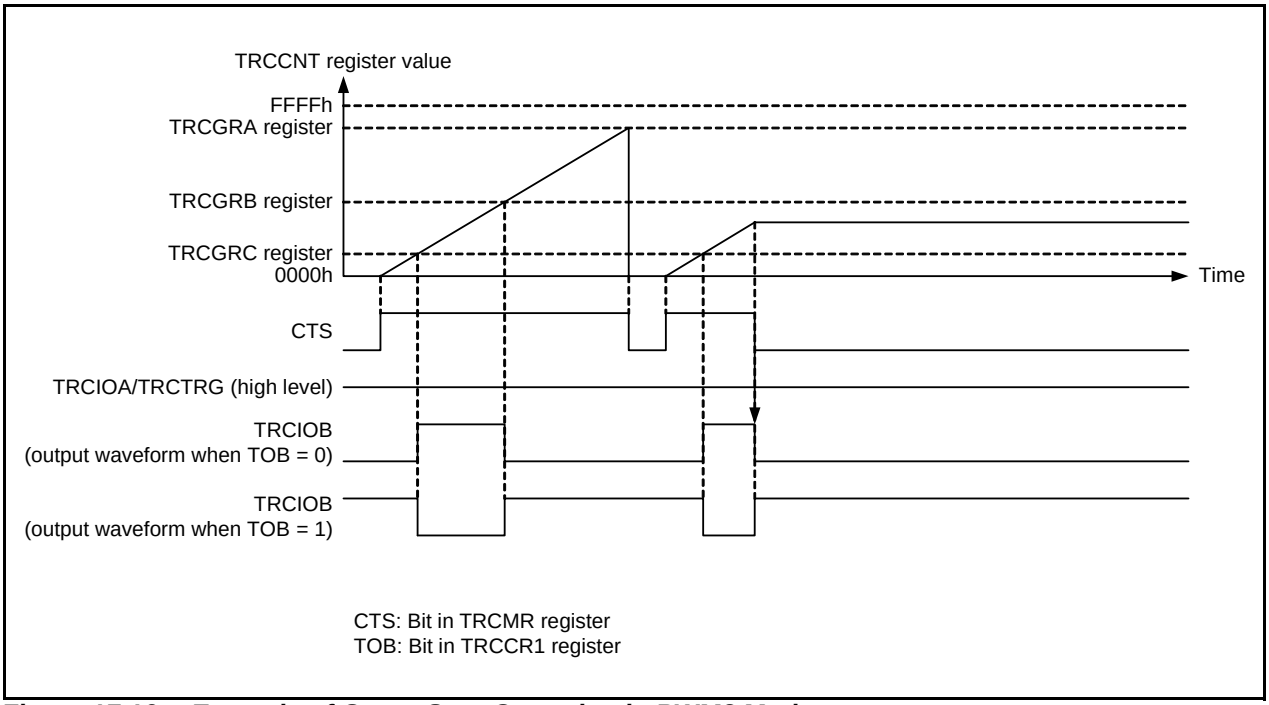


Figure 17.16 Example of Count Stop Operation in PWM2 Mode

Figure 17.17 shows an Example of One-Shot Pulse Waveform Output Operation in PWM2 Mode.
The count is started when the CTS bit in the TRCMR register is set to 1 (count starts) under the following conditions. Then, the counter is changed to 0000h by a compare match with the TRCGRA register, the count operation is stopped, and a one-shot waveform is output.

- Bits TCEG1 and TCEG0 in the TRCCR2 register are set to 00b (TRCTRG input disabled) to disable the TRCTRG input.
- The CSTP bit in the TRCCR2 register is set to 1 (count is stopped at compare match with TRCGRA register) to stop the increment when compare match A with the TRCGRA register occurs.
- The CCLR bit in the TRCCR1 register is set to 1 (TRCCNT counter is cleared by input capture/compare match A) to clear the TRCCNT register by compare match A.
- The TOB bit in the TRCCR1 register is set to 0 (output value is low) to set the initial value of the output level to low.

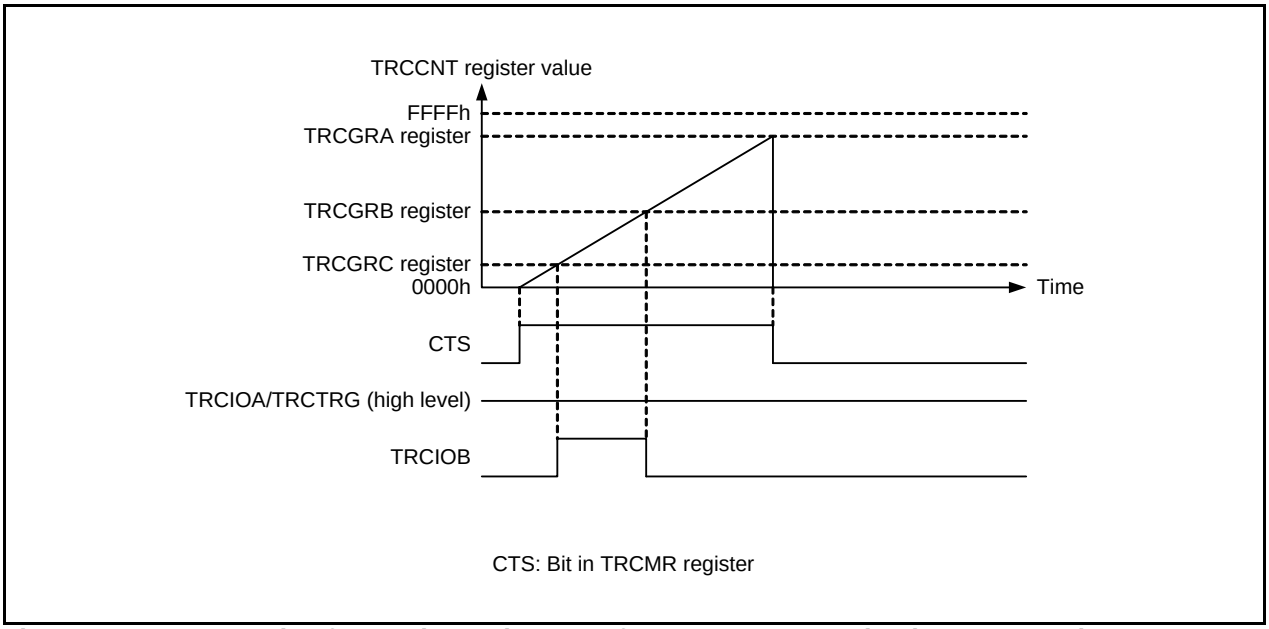


Figure 17.17 Example of One-Shot Pulse Waveform Output Operation in PWM2 Mode

Figure 17.18 shows an Example of One-Shot Waveform Output Operation in PWM2 Mode (Count is Started by TRCTRG Input).

After the CTS bit in the TRCMR register is set to 1 (count starts), the increment is started at the rising edge of TRCIOA/TRCTRG, and the counter is changed to 0000h by a compare match with the TRCGRA register, the count operation is stopped, and a one-shot waveform is output under the following conditions.

- Bits TCEG1 and TCEG0 in the TRCCR2 register are set to 10b (falling edge) to set the falling edge of the TRCTRG input.
- The CSTP bit in the TRCCR2 register is set to 1 (count is stopped at compare match with TRCGRA register) to stop the increment when a compare match with the TRCGRA register occurs.
- The CCLR bit in the TRCCR1 register is set to 1 (TRCCNT counter is cleared by input capture/compare match A) to clear the TRCCNT register by a compare match.
- The TOB bit in the TRCCR1 register is set to 0 (output value is low) to set the initial value of the output level to low.

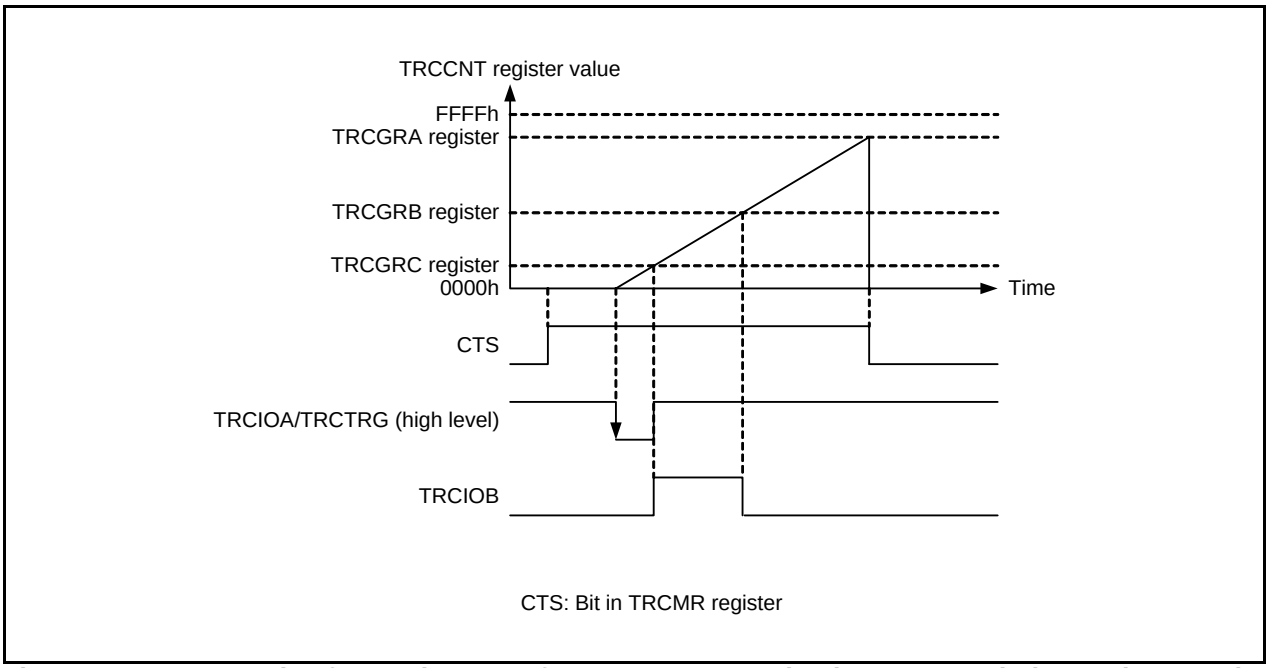


Figure 17.18 Example of One-Shot Waveform Output Operation in PWM2 Mode (Count is Started by TRCTRG Input)

17.4 Selectable Functions

17.4.1 Input Digital Filter for Input Capture

Figure 17.19 shows the Digital Filter Circuit Block Diagram. The TRCIOA to TRCIOD and TRCTRG input can be latched internally through the digital filter circuit. This circuit consists of three cascaded latch circuits and a match detection circuit. When the TRCIOA to TRCIOD and TRCTRG input are sampled on the clock selected by bits DFCK0 and DFCK1 in the TRCDF register and three outputs from the latch circuits match, the level is passed forward to the next circuit. If they do not match, the previous level is retained. That is, the pulse input with a width of three sampling clocks or more is recognized as a signal. If not, the change in the signal is recognized as noise and cancelled.

After a reset has been cleared, use the digital filter when the sampling clock is supplied, the pin state is determined, and at least five clocks have elapsed. Wait for four cycles of the sampling clock and make the setting for input capture before using the input capture function.

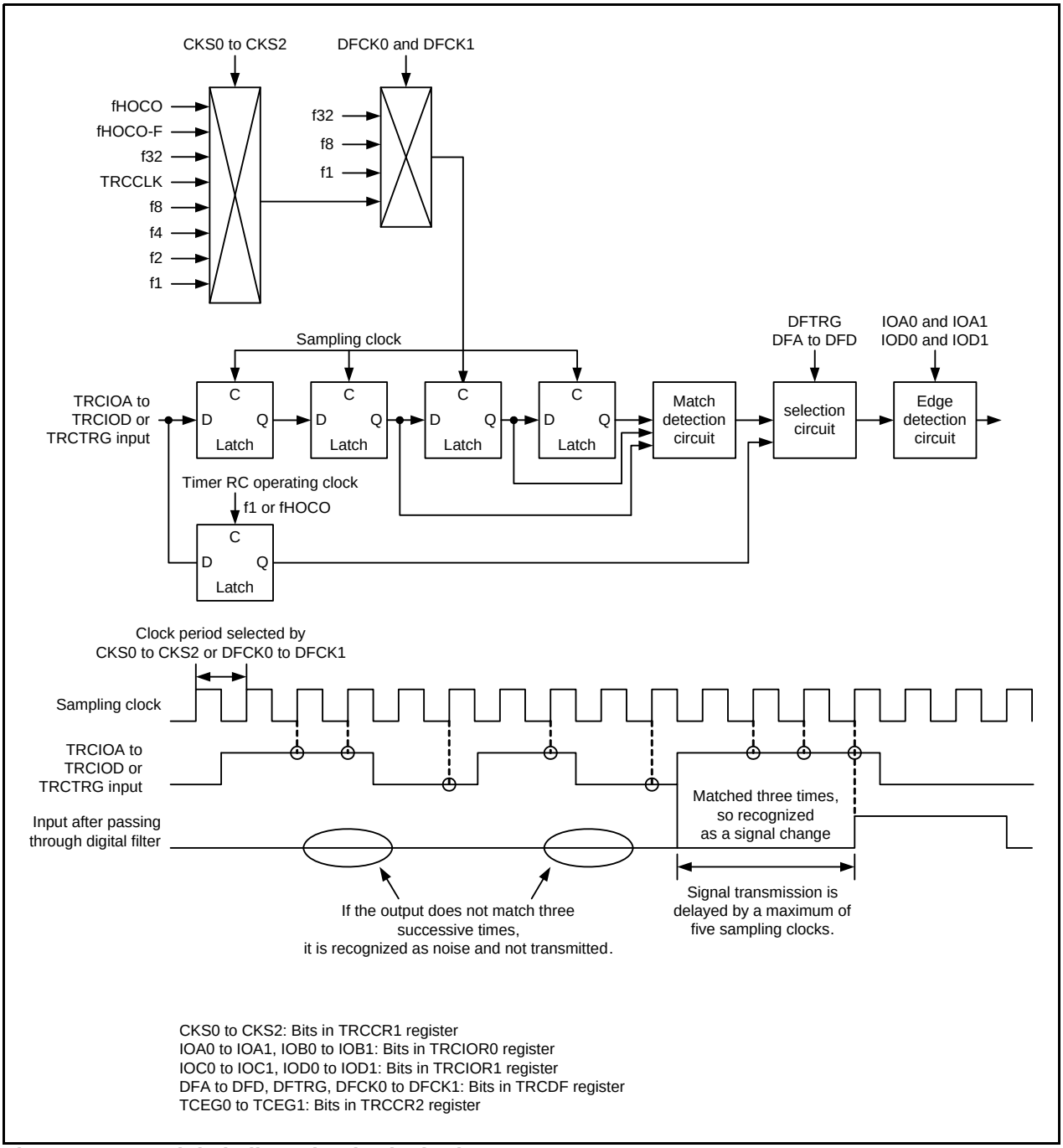


Figure 17.19 Digital Filter Circuit Block Diagram

17.4.2 A/D Conversion Start Trigger

By setting the TRCADCR register, an A/D conversion start trigger can be generated at compare matches A to D.
Figure 17.20 shows the Operation of A/D Conversion Start Trigger by Compare Matches B and C.

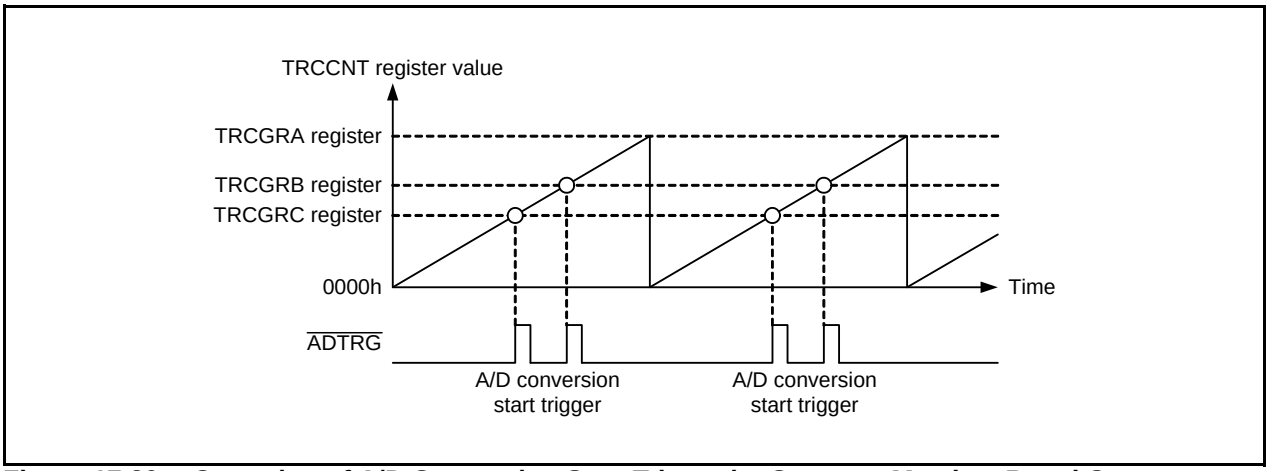


Figure 17.20 Operation of A/D Conversion Start Trigger by Compare Matches B and C

An A/D conversion start trigger is not generated from the buffer register during buffer operation. The TRCGRC register cannot operate as a buffer register for the TRCGRA register in PWM2 mode.
Table 17.17 lists the States Where A/D Conversion Start Trigger Sources are Generated.

Table 17.17 States Where A/D Conversion Start Trigger Sources are Generated

Operating Mode	Buffer Operation	A/D Conversion Start Trigger Source			
		TRCGRA	TRCGRB	TRCGRC	TRCGRD
Input capture	Used	No	No	No	No
	Not used	No	No	No	No
Compare match	Used	Yes	Yes	No	No
	Not used	Yes	Yes	Yes	Yes
PWM mode	Used	Yes	Yes	No	No
	Not used	Yes	Yes	Yes	Yes
PWM2 mode	Used	Yes	Yes	Yes	No
	Not used	Yes	Yes	Yes	Yes

Yes: An A/D conversion start trigger is generated.
No: No A/D conversion start trigger is generated.

17.4.3 Changing Output Pins and General Registers

The settings for bits IOC3 and IOD3 in the TRCIOR1 register can redirect the compare match output with registers TRCGRC and TRCGRD from pins TRCIOC and TRCIOD to pins TRCIOA and TRCIOB, respectively. The TRCIOA pin can output a combination of compare matches A and C and the TRCIOB pin can output a combination of compare matches B and D.
Figure 17.21 shows the Block Diagram for Changing Output Pins and General Registers.

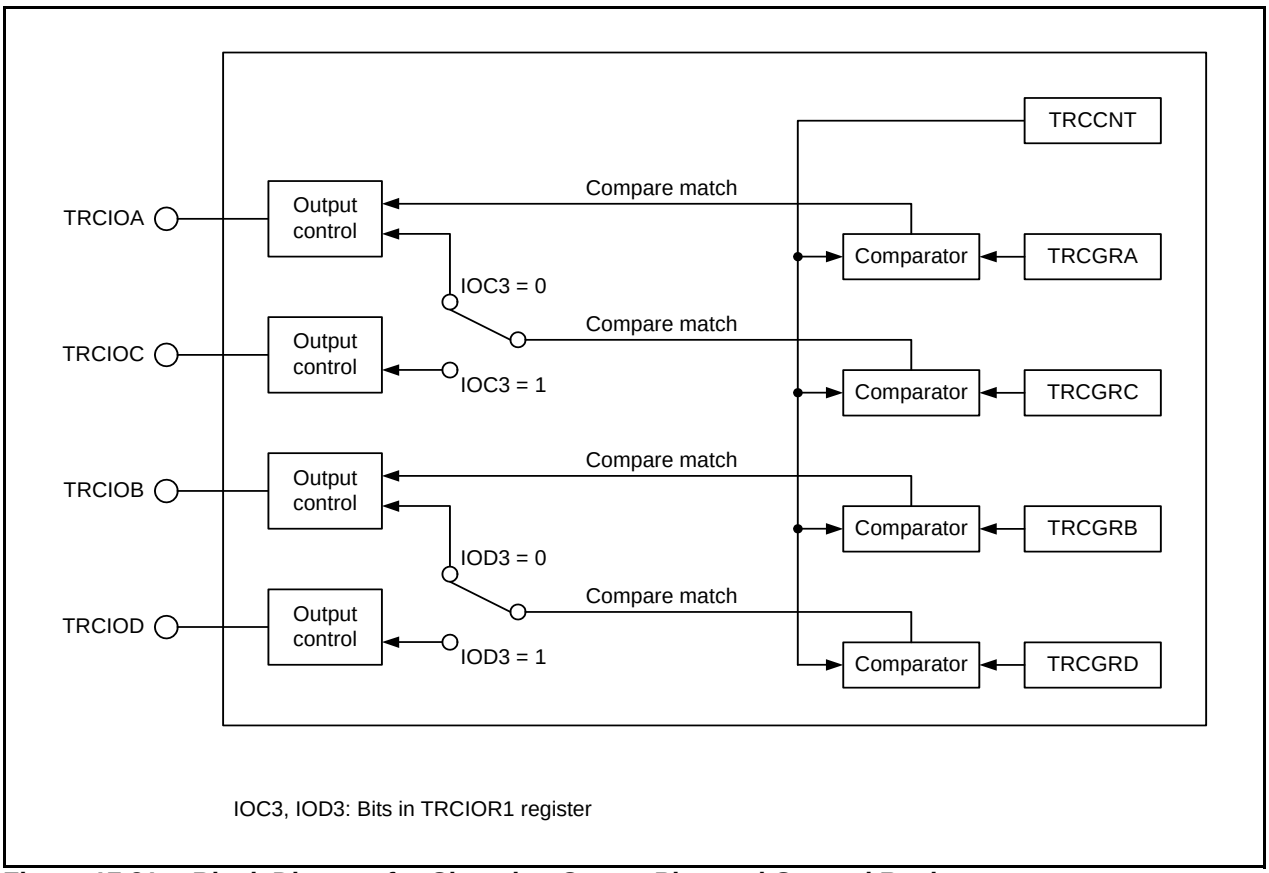


Figure 17.21 Block Diagram for Changing Output Pins and General Registers

Change output pins in registers TRCGRC and TRCGRD as follows:

- Set the IOC3 bit in the TRCIOR1 register to 0 (TRCIOA output register) and the IOD3 bit to 0 (TRCIOB output register).
- Set bits BUFEA and BUFEB in the TRCMR register to 0 (general register).
- Set different values in registers TRCGRA and TRCGRC. Also, set different values in registers TRCGRB and TRCGRD.

Figure 17.22 shows an Operation Example when TRCIOA and TRCIOB Output is not Overlapped. The following items must be set:

- Set the CCLR bit in the TRCCR1 register to 1 (TRCCNT counter is cleared by input capture/compare match A) to clear the counter by a compare match and set the TRCCNT register for period count operation.
- Set bits IOA2 to IOA0 in the TRCIOR0 register to 011b (toggle output from TRCIOA pin at compare match A) for toggle output.
- Set bits IOB2 to IOB0 in the TRCIOR0 register to 011b (toggle output from TRCIOB pin at compare match B) for toggle output.
- Set bits IOC3 to IOC0 in the TRCIOR1 register to 0011b (toggle output from TRCIOA pin at compare match C) for toggle output.
- Set bits IOD3 to IOD0 in the TRCIOR1 register to 0011b (toggle output from TRCIOB pin at compare match D) for toggle output.

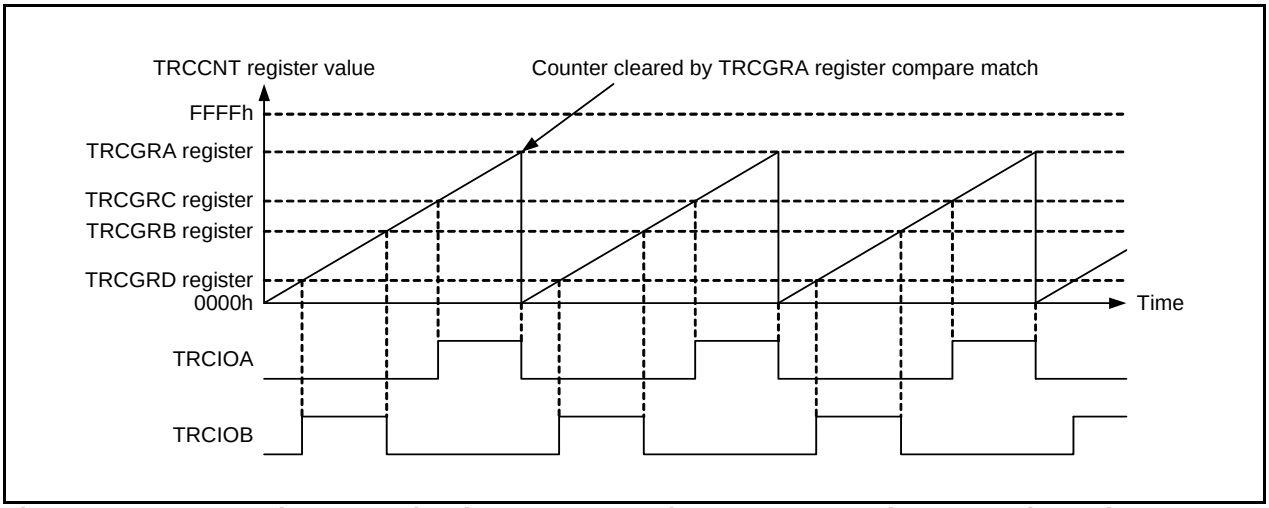


Figure 17.22 Operation Example when TRCIOA and TRCIOB Output is not Overlapped

17.4.4 Output Waveform Manipulation

By setting the TRCOPR register (timer RC output waveform manipulation register), an output waveform from the port can be controlled using $\overline{\text{INT1}}$ input.

When the OPE bit in the TRCOPR register is 0, the output waveform manipulation function is disabled. Even if a request event for output waveform manipulation is input while the output waveform manipulation function is disabled, the event is not accepted. Timer RC pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD output a waveform set by registers TRCIOR0, TRCIOR1, and TRCOER. When the PTO bit in the TRCOER register is 1 (pulse output forced cutoff signal input $\overline{\text{INT0}}$ enabled), if a low level is input to the INT0 pin, bits EA, EB, EC, and ED in the TRCOER register are set to all 1 (timer RC output disabled) and output pins TRCIOA to TRCIOD become high impedance.

When the OPE bit is 1, the output waveform manipulation is enabled. If an output waveform manipulation event ($\overline{\text{INT1}}$ = low for timer RC_0) is input, bits EA to ED in the TRCOER register are automatically set to 1. By setting the timer RC port level using bits OPOL0 and OPOL1 in the TRCOPR register, low, high, or high impedance is forcibly output. When the request event for output waveform manipulation is cancelled, output waveform manipulation from the timer RC port is stopped and output is restarted by setting RESTATS. After output waveform manipulation is stopped, output from the pin is restarted from the next timer count period after the timing when output restart is set.

Figures 17.23 to 17.26 show operation examples of output waveform manipulation.

- When the TRCIOB pin is pulled down externally, the OPE bit in the TRCOPR register is 1 (output waveform manipulation enabled), and bits OPOL1 and OPOL0 are 00b (when pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD are set to be pulled down externally, timer RC output level is fixed to high impedance during output waveform manipulation period), and the RESTATS bit is 0 (output waveform manipulation is stopped by software and output is restarted)

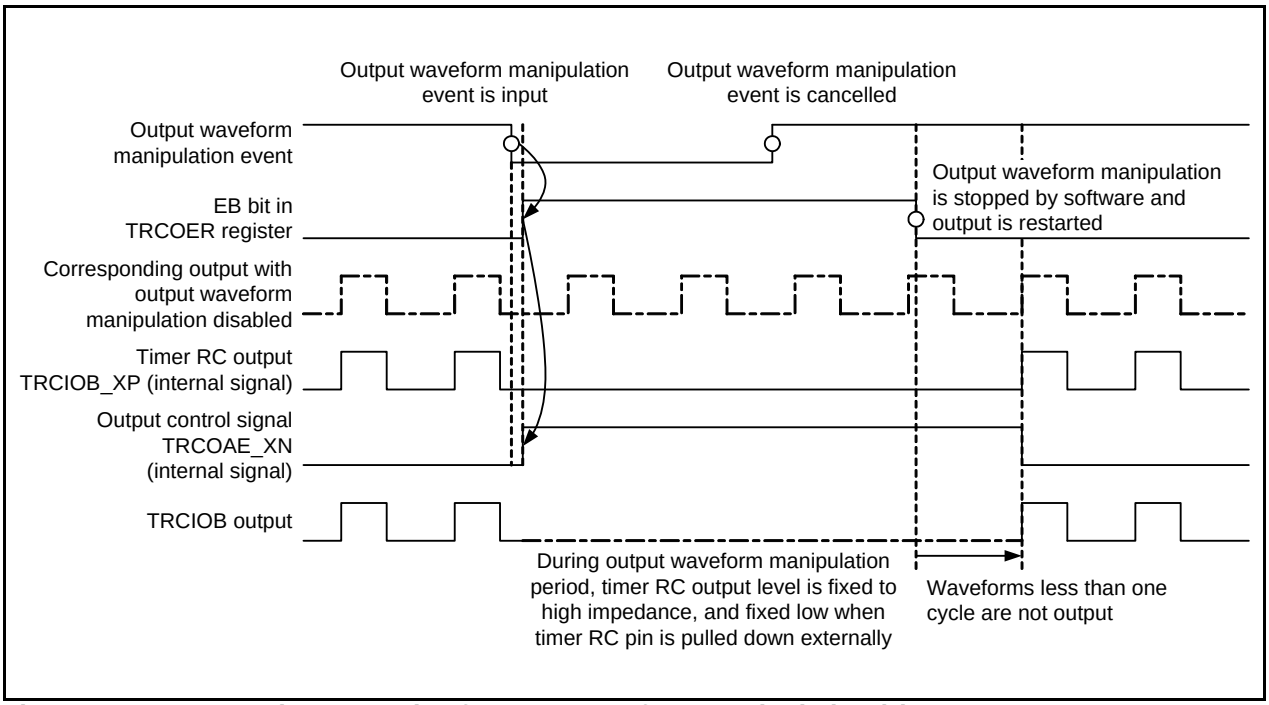


Figure 17.23 Operation Example of Output Waveform Manipulation (1)

• When the TRCIOB pin is pulled up externally, the OPE bit in the TRCOPR register is 1 (output waveform manipulation enabled), bits OPOL1 and OPOL0 are 01b (when pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD are set to be pulled up externally, timer RC output level is fixed to high impedance during output waveform manipulation period), and the RESTATS bit is 0 (output waveform manipulation is stopped by software and output is restarted)

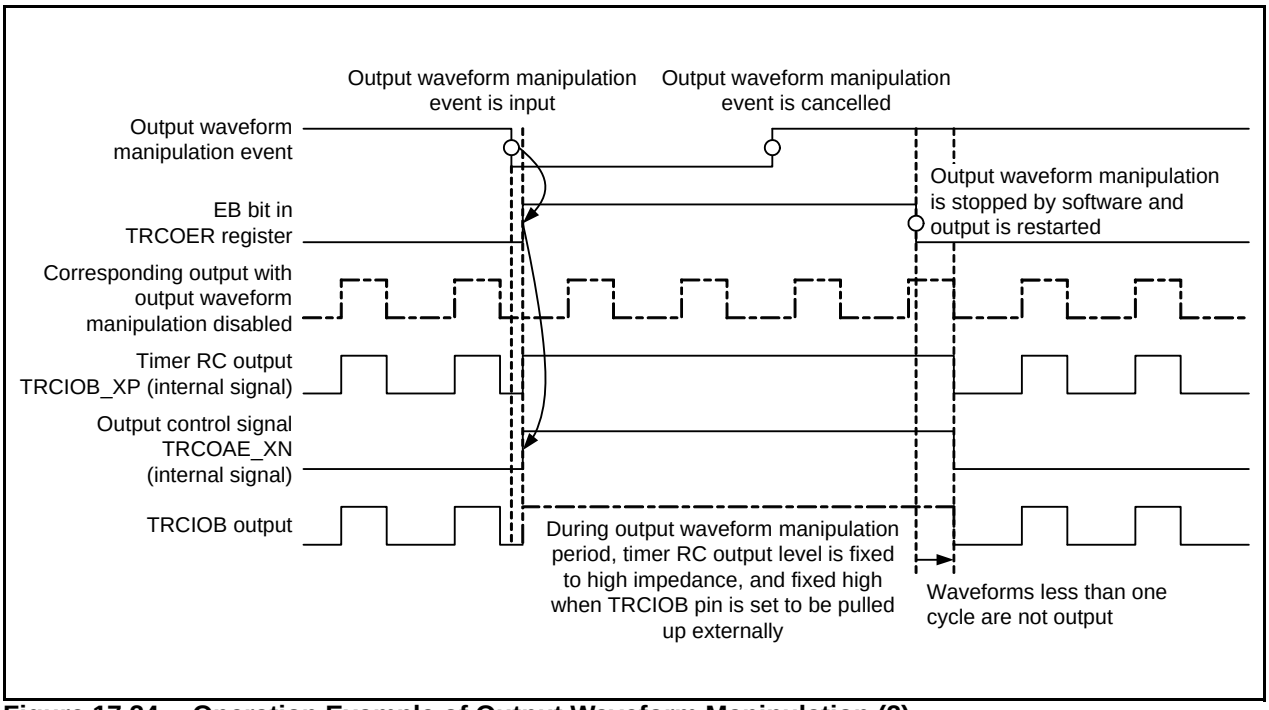


Figure 17.24 Operation Example of Output Waveform Manipulation (2)

• When the OPE bit in the TRCOPR register is 1 (output waveform manipulation enabled), bits OPOL1 and OPOL0 are 10b (timer RC output level is fixed low during output waveform manipulation period), and the RESTATS bit is 1 (automatic output waveform manipulation is stopped by software and automatic output is restarted)

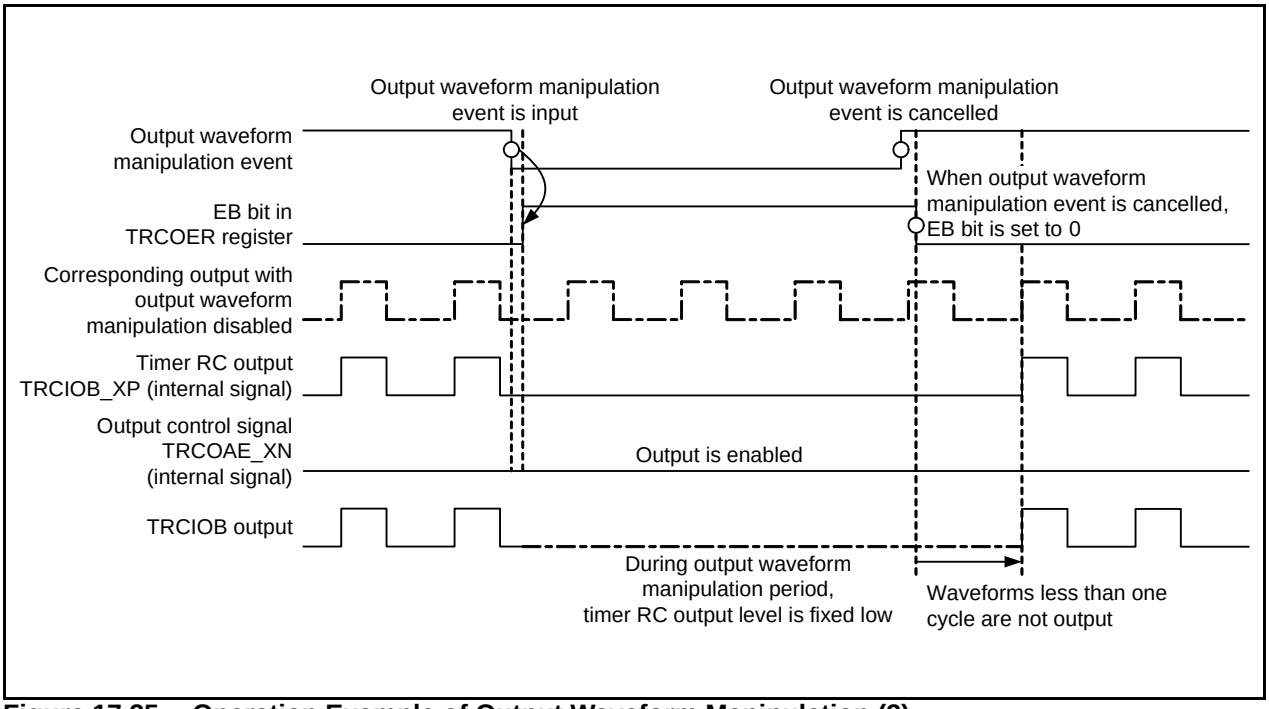


Figure 17.25 Operation Example of Output Waveform Manipulation (3)

• When the OPE bit in the TRCOPR register is 1 (output waveform manipulation enabled), bits OPOL1 and OPOL0 are 11b (timer RC output level is fixed high during output waveform manipulation period), and the RESTATS bit is 1 (automatic output waveform manipulation is stopped by software and automatic output is restarted)

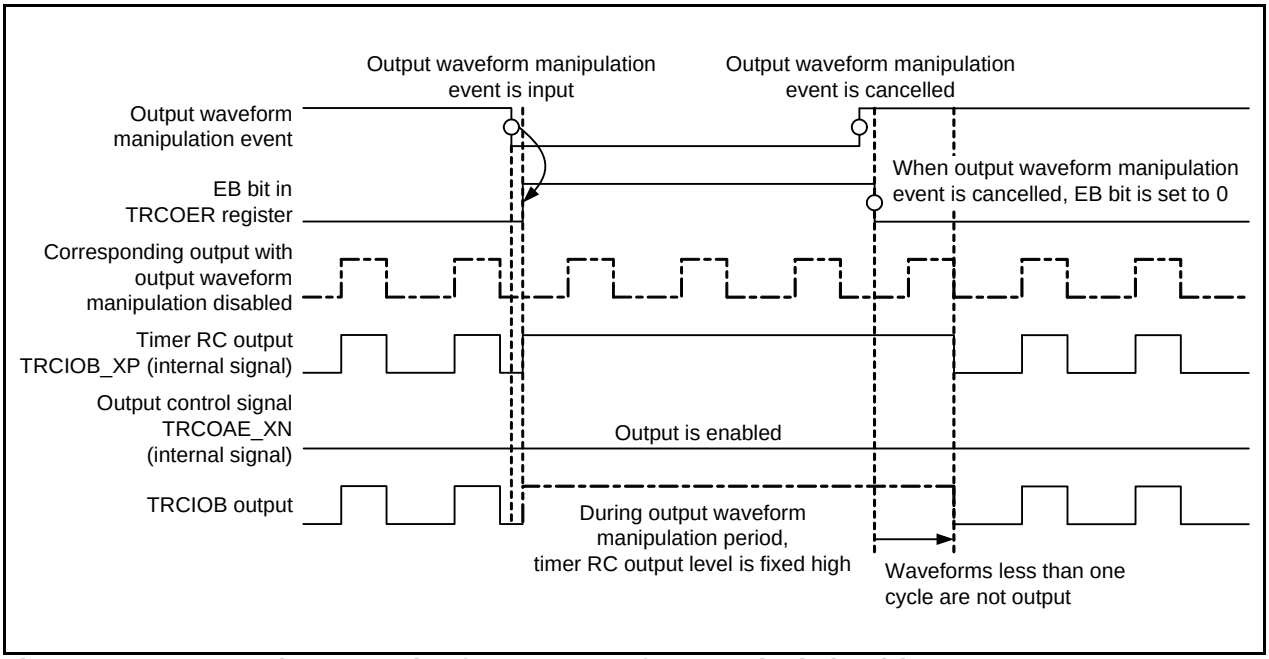


Figure 17.26 Operation Example of Output Waveform Manipulation (4)

17.5 Operation Timing

17.5.1 TRCCNT Register Count Timing

Figure 17.27 shows the Count Operation Timing.

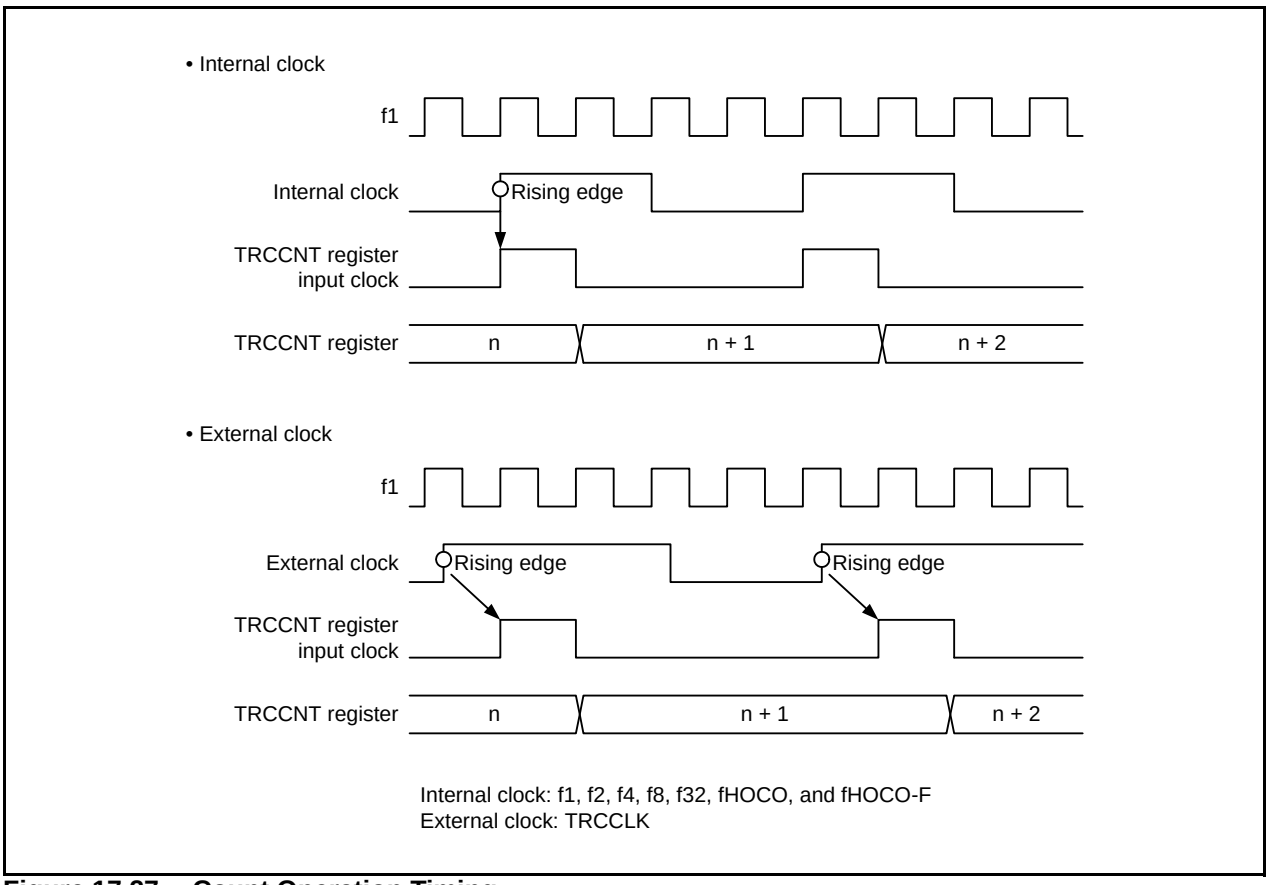


Figure 17.27 Count Operation Timing

17.5.2 Output-Compare Output Timing

A compare match signal occurs at the last state (timing when the TRCCNT register updates a matched value) when the TRCCNT register and the general register match. When the compare match occurs, the output value set by the TRCIOR register is output to the output-compare output pins (TRCIOA, TRCIOB, TRCIOC, and TRCIOD). After the TRCCNT register and the general register match, a compare match signal does not occur until an input clock to the TRCCNT register is generated.
Figure 17.28 shows the Output-Compare Output Timing.

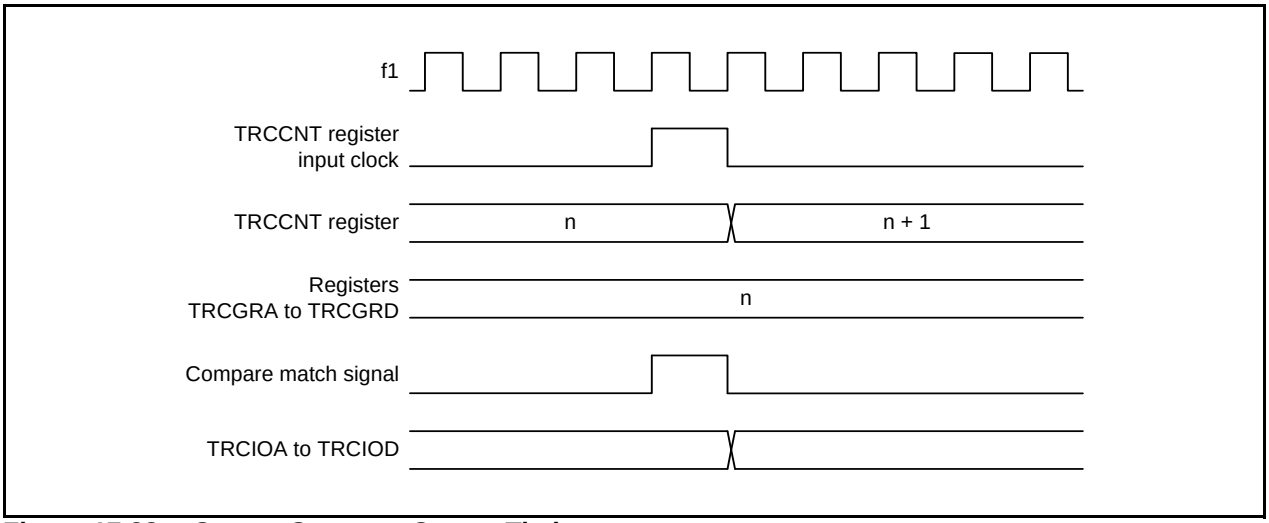


Figure 17.28 Output-Compare Output Timing

17.5.3 Input-Capture Input Timing

A falling edge, rising edge, or both edges can be selected for input-capture input by setting registers TRCIOR0 and TRCIOR1.
Figure 17.29 shows the Input-Capture Input Timing. This applies when a falling edge is selected.

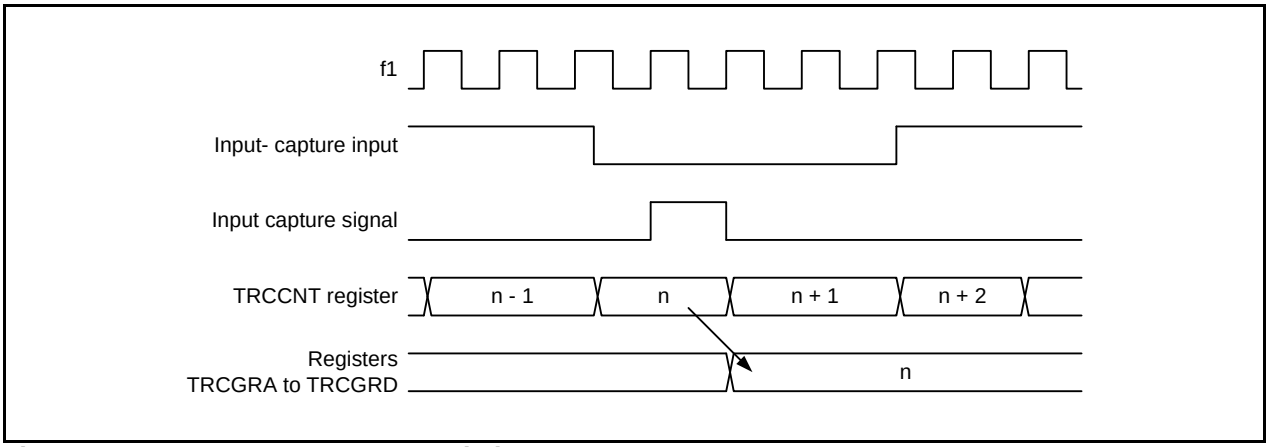


Figure 17.29 Input-Capture Input Timing

17.5.4 Timing for Counter Clearing by Compare Match

Figure 17.30 shows the Timing for Counter Clearing by Compare Match A. If the value in the TRCGRA register is n, the counter counts from 0 to n and the period is thus set to n + 1.

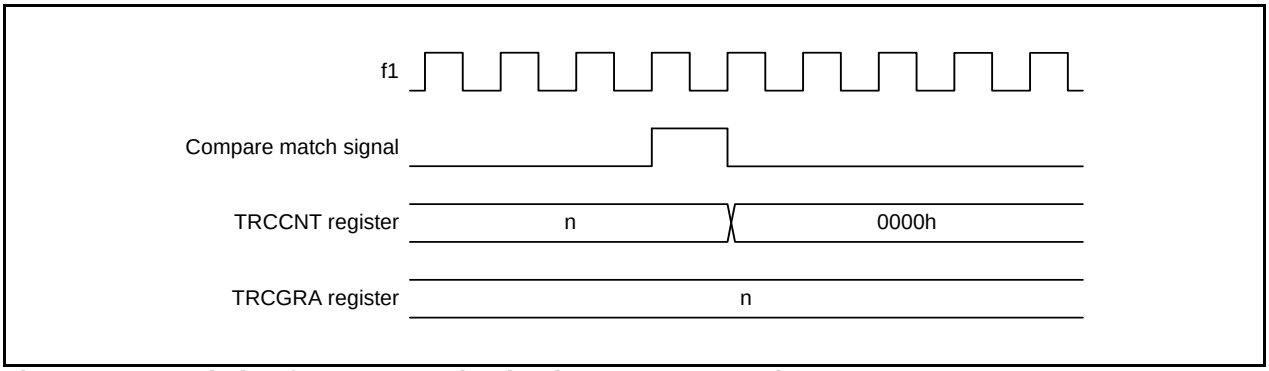


Figure 17.30 Timing for Counter Clearing by Compare Match A

17.5.5 Buffer Operation Timing

Figure 17.31 shows the Buffer Operation Timing.

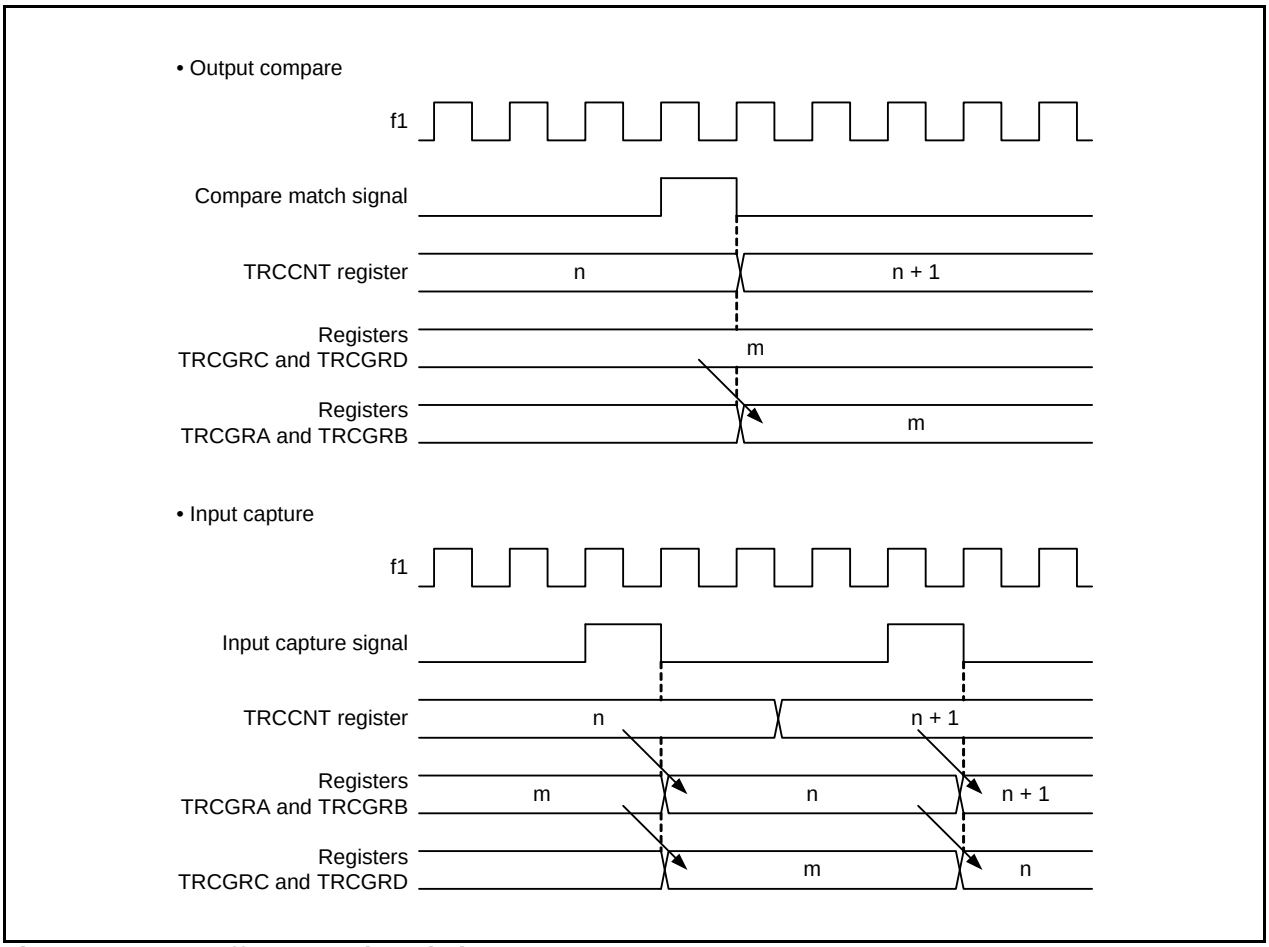


Figure 17.31 Buffer Operation Timing

17.5.6 Bits IMFA to IMFD Timing at Compare Match

While the TRCSR register functions as an output compare register, bits IMFA to IMFD are set to 1 when the TRCCNT register and the general registers (TRCGRA, TRCGRB, TRCGRC, TRCGRD) match.
A compare match signal occurs at the last state (timing when the TRCCNT register updates a matched value). Thus, after the TRCCNT register and the general register match, a compare match signal does not occur until an input clock to the TRCCNT register is generated.
Figure 17.32 shows the Timing at Compare Match.

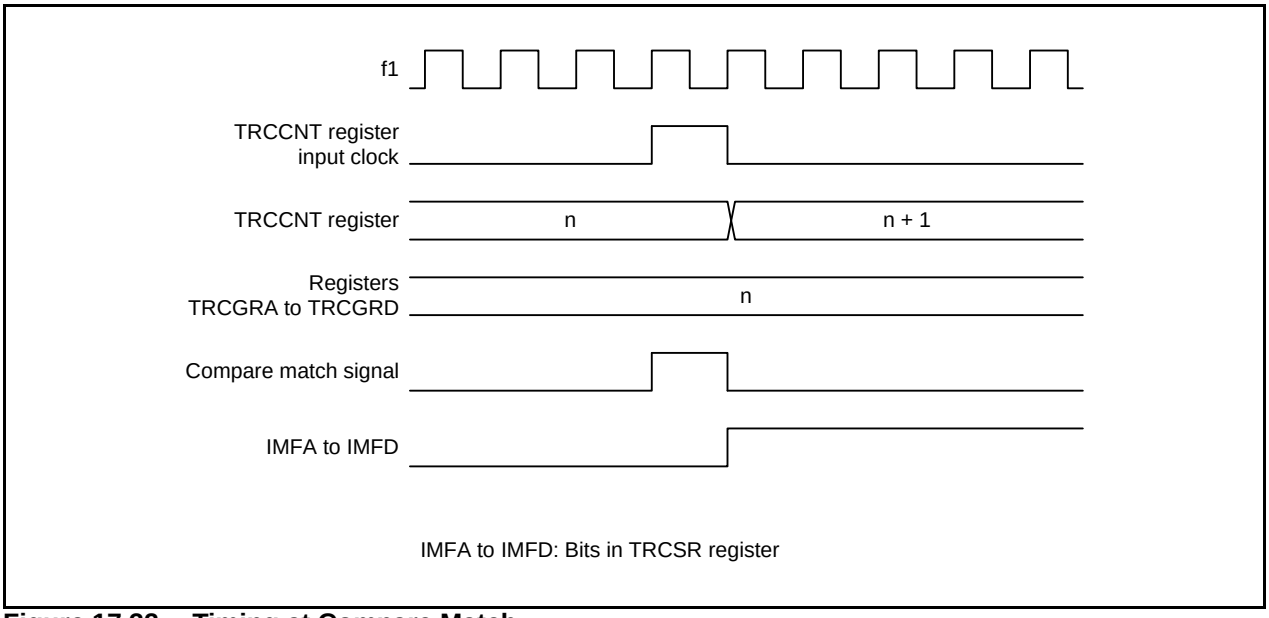


Figure 17.32 Timing at Compare Match

17.5.7 Bits IMFA to IMFD Timing at Input Capture

While the TRCSR register functions as an input capture register, bits IMFA to IMFD are set to 1 when an input capture occurs.
Figure 17.33 shows the Timing at Input Capture.

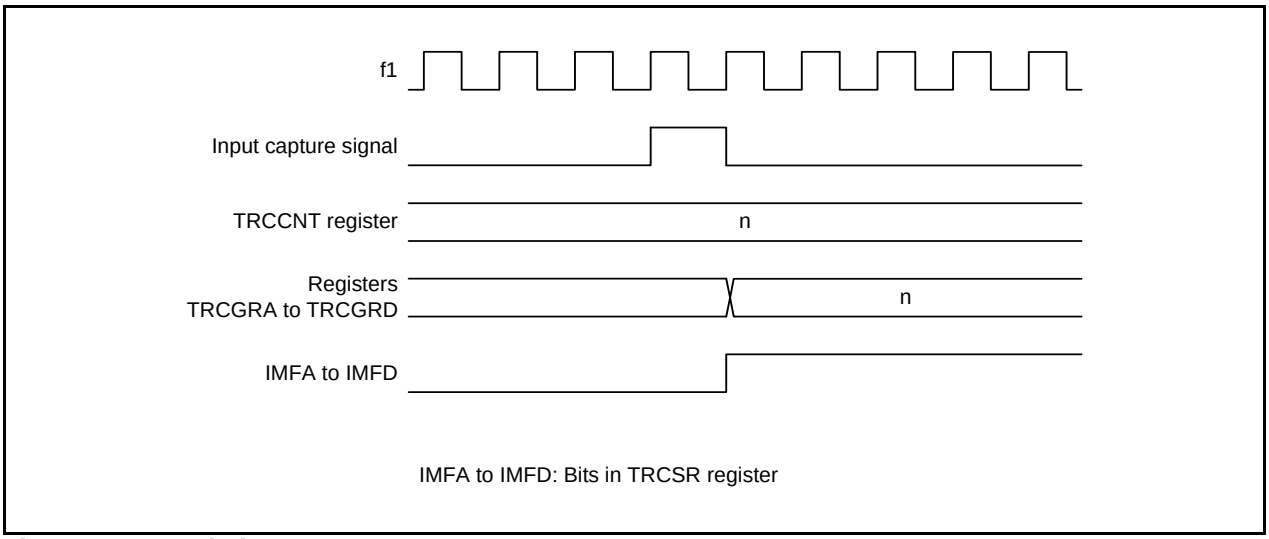


Figure 17.33 Timing at Input Capture

17.5.8 Timing for Setting Bits IMFA to IMFD and OVF to 0

Bits IMFA to IMFD and OVF are set to 0 when 0 is written to a flag after the CPU reads it as 1. Figure 17.34 shows the Timing for Setting Bits IMFA to IMFD and OVF by CPU.

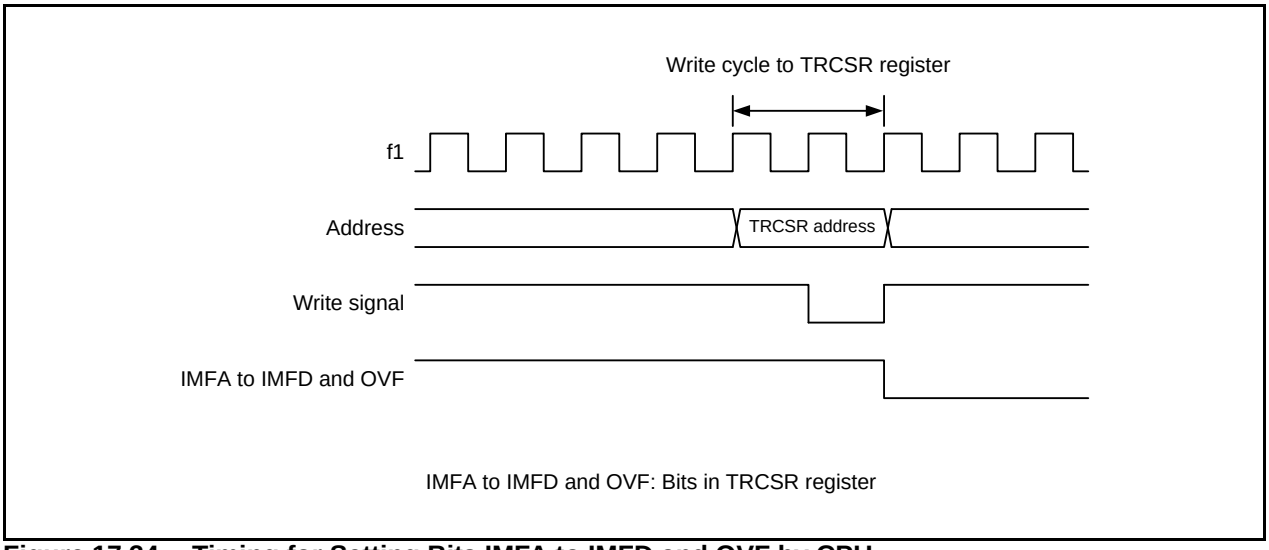


Figure 17.34 Timing for Setting Bits IMFA to IMFD and OVF by CPU

17.5.9 Timing of A/D Conversion Start Trigger due to Compare Match

Figure 17.35 shows the Timing of A/D Conversion Start Trigger due to Compare Match.

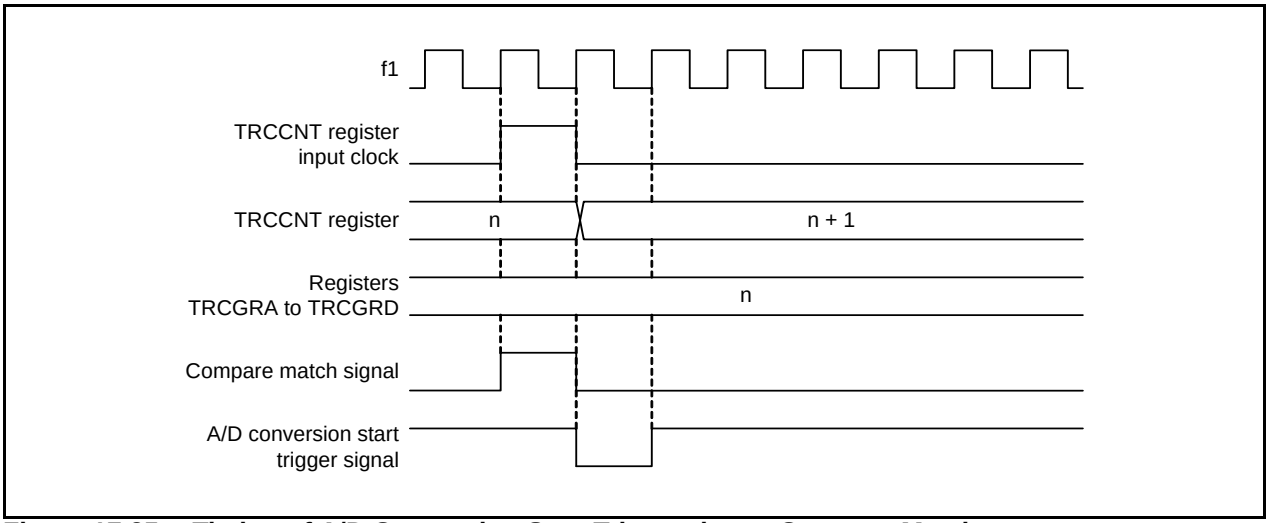


Figure 17.35 Timing of A/D Conversion Start Trigger due to Compare Match

17.6 Timer RC Interrupt

Timer RC generates a timer RC interrupt request from five sources. The timer RC interrupt uses the single TRCIC register (bits IR and ILVL0 to ILVL2) and a single vector.
Table 17.18 lists the Registers Associated with Timer RC Interrupt, and Figure 17.36 shows a Timer RC Interrupt Block Diagram.

Table 17.18 Registers Associated with Timer RC Interrupt

Timer RC Status Register	Timer RC Interrupt Enable Register	Timer RC Interrupt Control Register
TRCSR	TRCIER	TRCIC

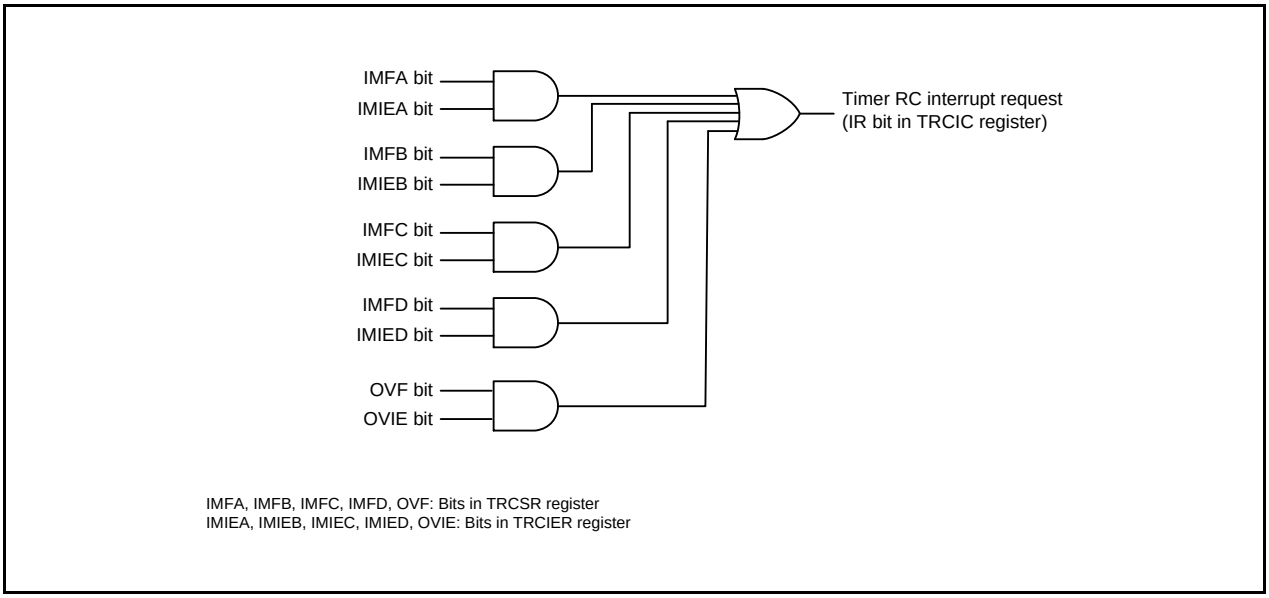


Figure 17.36 Timer RC Interrupt Block Diagram

Like other maskable interrupts, the timer RC interrupt is controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, it differs from other maskable interrupts in the following respects because a single interrupt source (timer RC interrupt) is generated from multiple interrupt request sources.

- The IR bit in the TRCIC register is set to 1 (interrupt requested) when a bit in the TRCSR register is set to 1 and the corresponding bit in the TRCIER register is also set to 1 (interrupt enabled).
- The IR bit is set to 0 (no interrupt requested) when the bit in the TRCSR register or the corresponding bit in the TRCIER register is set to 0, or both are set to 0. In other words, the interrupt request is not maintained if the IR bit is once set to 1 but the interrupt is not acknowledged.
- If another interrupt source is triggered after the IR bit is set to 1, the IR bit remains set to 1 and does not change.
- If multiple bits in the TRCIER register are set to 1, use the TRCSR register to determine the source of the interrupt request.
- The bits in the TRCSR register are not automatically set to 0 when an interrupt is acknowledged. Set them to 0 within the interrupt routine. Refer to **17.2.6 Timer RC Status Register (TRCSR)**, for the procedure for setting these bits to 0.

Refer to **17.2.5 Timer RC Interrupt Enable Register (TRCIER)**, for details of the TRCIER register.
Refer to **11.4 Interrupt Control**, for details of the TRCIC register and **11.3.2 Relocatable Vector Table**, for information on interrupt vectors.

17.7 Notes on Timer RC

17.7.1 TRCCNT Register

The following notes apply when the CCLR bit in the TRCCR1 register is set to 1 (TRCCNT counter is cleared by input capture/compare match A).

- When writing a value to the TRCCNT register by a program while the CTS bit in the TRCMR register is set to 1 (count starts), ensure that the write timing does not coincide with when the TRCCNT register is set to 0000h.
- If the timing when the TRCCNT register is set to 0000h and is written coincide, the value is not written and the TRCCNT register is set to 0000h.

If the TRCCNT register is written and read, the value before this register is written may be read. In this case, execute the JMP.B instruction between the write and read instructions.

- Program Example

```
        MOV.W   #XXXXh, TRCCNT      ; Write
        JMP.B   L1                  ; JMP.B instruction
L1:     MOV.W   TRCCNT, DATA        ; Read
```

17.7.2 TRCCR1 Register

When setting bits CKS2 to CKS0 in the TRCCR1 register to 111b (fHOCO-F), set fHOCO-F to a clock frequency higher than the CPU clock frequency.

17.7.3 TRCSR Register

If the TRCSR register is written and read, the value before this register is written may be read. In this case, execute the JMP.B instruction between the write and read instructions.

- Program Example

```
        MOV.B   #XXh, TRCSR         ; Write
        JMP.B   L1                  ; JMP.B instruction
L1:     MOV.B   TRCSR, DATA         ; Read
```

17.7.4 Count Source Switching

- When switching the count source, stop the count before switching. After switching the count source, wait for at least two cycles of the CPU clock before writing to the registers (at addresses 00138h to 0014Dh) associated with timer RC.

[Changing procedure]

(1) Set the CTS bit in the TRCMR register to 0 (count stops).
(2) Change bits CKS0 to CKS2 in the TRCCR1 register.
(3) Wait for at least two cycles of the CPU clock.
(4) Write to the registers (at addresses 00138h to 0014Dh) associated with timer RC.

- When changing the count source from fHOCO-F to fHOCO and stopping fHOCO-F, wait for at least two cycles of fHOCO-F after changing the clock setting before stopping fHOCO-F.

[Changing procedure]

(1) Set the CTS bit in the TRCMR register to 0 (count stops).
(2) Change bits CKS0 to CKS2 in the TRCCR1 register.
(3) Wait for at least two cycles of fHOCO-F.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

• When changing the count source from fHOCO-F to another source and stopping fHOCO-F, wait for at least one cycle of fHOCO-F + one cycle of fHOCO after changing the clock setting before stopping fHOCO-F.

[Changing procedure]

(1) Set the CTS bit in the TRCMR register to 0 (count stops).
(2) Change bits CKS0 to CKS2 in the TRCCR1 register.
(3) Wait for at least one cycle of fHOCO-F + one cycle of fHOCO.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

Notes:

1. Do not set the FRA00 bit to 0 (high-speed on-chip oscillator off) while fHOCO or fHOCO-F is selected as the count source.
2. Do not change the division ratio of the high-speed on-chip oscillator set by the FRA2 register while fHOCO-F is selected as the count source.

17.7.5 Input Capture Function

Set the pulse width of the input capture signal as follows:
[When the digital filter is not used]
Three or more cycles of the timer RC operation clock (refer to Table 17.1 Timer RC Specifications)
[When the digital filter is used]
Five cycles of the digital filter sampling clock + three cycles of the timer RC operating clock, minimum (refer to **Figure 17.19 Digital Filter Circuit Block Diagram**)

The value of the TRCCNT register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).

17.7.6 TRCMR Register in PWM2 Mode

When the CSTP bit in the TRCCR2 register is 1 (count is stopped at compare match with TRCGRA register), do not set the TRCMR register when a compare match occurs between registers TRCCNT and TRCGRA.

17.7.7 Module Standby

Write to the MSTTRC_0 bit in the MSTCR2 register while the timer RC count is stopped. The timer RC module standby bit exists in the MSTCR2 register.

17.7.8 Mode Switching

- When switching modes during operation, set the CTS bit in the TRCMR register to 0 (count stops) before switching.
- After switching modes, set the flags in the TRCSR register to 0 and set the IR bit in the TRCIC register to 0 before starting operation.
  For details, refer to **11.9.4 Changing Interrupt Sources**.

17.7.9 Input Capture Operation when Count is Stopped

When the input capture function is used, if an input capture signal (edge selected by bits IOj0 and IOj1 (j = A or B) in the TRCIOR0 register or bits IOk0 and IOk1 (k = C or D) in the TRCIOR1 register) is input to the TRCIOi pin (i = A, B, C, or D), the IMFi bit in the TRCSR register is set to 1 even when the CTS bit in the TRCMR register is set to 0 (count stops).

18. Timer RD

Timer RD has two 16-bit timers (timer RD0 and timer RD1).

18.1 Overview

Timer RD has four I/O pins.
The timer RD operating clock is f1, fHOCO or fHOCO-F. Table 18.1 lists the Timer RD Operating Clocks.

Table 18.1 Timer RD Operating Clocks

Condition	Timer RD Operating Clock
The count source is f1, f2, f4, f8, f32, or TRDCLK input (Bits TCK2 to TCK0 in registers TRDCR0 and TRDCR1 are set to 000b to 101b)	f1
The count source is fHOCO (Bits TCK2 to TCK0 in registers TRDCR0 and TRDCR1 are set to 110b)	fHOCO
The count source is fHOCO-F (Bits TCK2 to TCK0 in registers TRDCR0 and TRDCR1 are set to 111b)	fHOCO-F

Figure 18.1 shows the Timer RD Block Diagram (i = 0 or 1) and Table 18.2 lists Timer RD Pin Configuration.
Timer RD supports five modes:

- Timer mode
  - Input capture function — The counter value is transferred to a register with an external signal as the trigger.
  - Output compare function — Register value matches with a counter are detected. (Pin output can be changed at detection.)

The following four modes use the output compare function.

- PWM mode — Pulses of any width are output continuously.
- Reset synchronous PWM mode — Three-phase waveforms (6) without sawtooth wave modulation and dead time are output.
- Complementary PWM mode — Three-phase waveforms (6) with triangular wave modulation and dead time are output.
- PWM3 mode — PWM waveforms (2) with a fixed period are output.

In the input capture function, the output compare function, and PWM mode, timer RD0 and timer RD1 have the equivalent functions, and functions or modes can be selected individually for each pin. Also, a combination of these functions and modes can be used in timer RD0 and timer RD1.
In reset synchronous PWM mode, complementary PWM mode, and PWM3 mode, a waveform is output with a combination of counters and registers in timer RD0 and timer RD1. Pin functions depend on the mode.

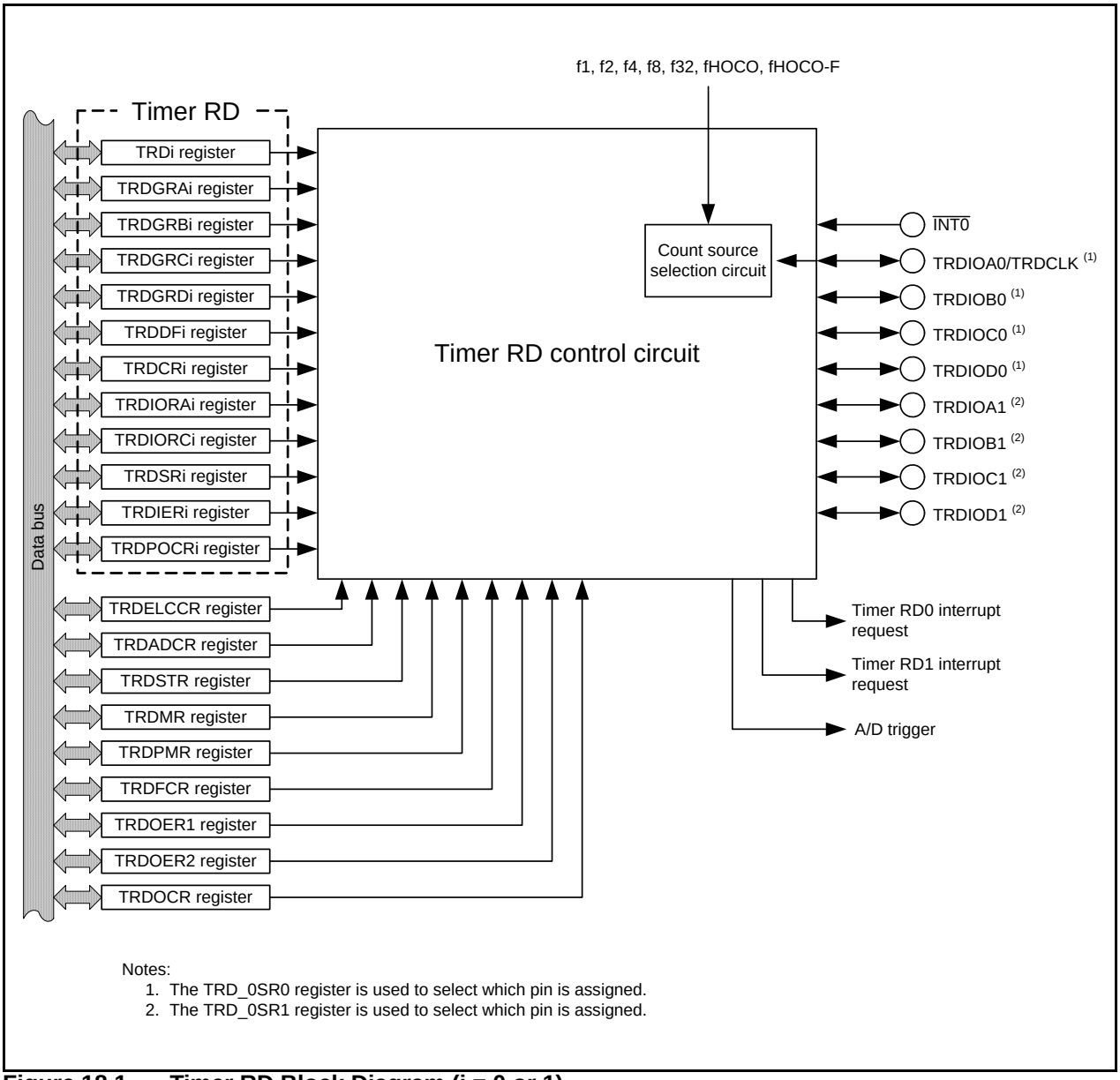


Figure 18.1 Timer RD Block Diagram (i = 0 or 1)

Table 18.2 Timer RD Pin Configuration

Pin Name	I/O	Function
TRDIOA0/TRDCLK	Input/Output	Function varies depending on the mode. Refer to descriptions of individual modes for details.
TRDIOB0	Input/Output	
TRDIOC0	Input/Output	
TRDIOD0	Input/Output	
TRDIOA1	Input/Output	
TRDIOB1	Input/Output	
TRDIOC1	Input/Output	
TRDIOD1	Input/Output	

18.2 Registers

Table 18.3 lists the Timer RD Register Configuration.

Table 18.3 Timer RD Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Timer RD_0 ELC Cooperation Control Register	TRDELCCR_0	00h	00180h	8
Timer RD_0 Trigger Control Register	TRDADCR_0	00h	00182h	8
Timer RD_0 Start Register	TRDSTR_0	11111100b	00183h	8
Timer RD_0 Mode Register	TRDMR_0	00001110b	00184h	8
Timer RD_0 PWM Mode Register	TRDPMR_0	10001000b	00185h	8
Timer RD_0 Function Control Register	TRDFCR_0	10000000b	00186h	8
Timer RD_0 Output Master Enable Register 1	TRDOER1_0	FFh	00187h	8
Timer RD_0 Output Master Enable Register 2	TRDOER2_0	01111111b	00188h	8
Timer RD_0 Output Control Register	TRDOCR_0	00h	00189h	8
Timer RD_0 Digital Filter Function Select Register 0	TRDDF0_0	00h	0018Ah	8
Timer RD_0 Digital Filter Function Select Register 1	TRDDF1_0	00h	0018Bh	8
Timer RD_0 Control Register 0	TRDCR0_0	00h	00190h	8
Timer RD_0 I/O Control Register A0	TRDIORA0_0	10001000b	00191h	8
Timer RD_0 I/O Control Register C0	TRDIORC0_0	10001000b	00192h	8
Timer RD_0 Status Register 0	TRDSR0_0	11100000b	00193h	8
Timer RD_0 Interrupt Enable Register 0	TRDIER0_0	11100000b	00194h	8
Timer RD_0 PWM Mode Output Level Control Register 0	TRDPOCR0_0	11111000b	00195h	8
Timer RD_0 Counter 0	TRD0_0	0000h	00196h	16
Timer RD_0 General Register A0	TRDGRA0_0	FFFFh	00198h	16
Timer RD_0 General Register B0	TRDGRB0_0	FFFFh	0019Ah	16
Timer RD_0 General Register C0	TRDGRC0_0	FFFFh	0019Ch	16
Timer RD_0 General Register D0	TRDGRD0_0	FFFFh	0019Eh	16
Timer RD_0 Control Register 1	TRDCR1_0	00h	001A0h	8
Timer RD_0 I/O Control Register A1	TRDIORA1_0	10001000b	001A1h	8
Timer RD_0 I/O Control Register C1	TRDIORC1_0	10001000b	001A2h	8
Timer RD_0 Status Register 1	TRDSR1_0	11000000b	001A3h	8
Timer RD_0 Interrupt Enable Register 1	TRDIER1_0	11100000b	001A4h	8
Timer RD_0 PWM Mode Output Level Control Register 1	TRDPOCR1_0	11111000b	001A5h	8
Timer RD_0 Counter 1	TRD1_0	0000h	001A6h	16
Timer RD_0 General Register A1	TRDGRA1_0	FFFFh	001A8h	16
Timer RD_0 General Register B1	TRDGRB1_0	FFFFh	001AAh	16
Timer RD_0 General Register C1	TRDGRC1_0	FFFFh	001ACh	16
Timer RD_0 General Register D1	TRDGRD1_0	FFFFh	001AEh	16

18.2.1 Timer RD ELC Cooperation Control Register (TRDELCCR)

Address 00180h (TRDELCCR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	ELCOBE1	ELCICE1	—	—	ELCOBE0	ELCICE0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ELCICE0	Timer RD0 ELC input capture request signal select bit	0: Input capture TRDIOD0 selected 1: Timer RD0 ELC input capture request signal selected	R/W
b1	ELCOBE0	Timer RD0 ELC input capture request signal enable bit for pulse forced cutoff ($\overline{INT0}$)	0: Timer RD0 ELC input capture request signal enable bit disabled 1: Timer RD0 ELC input capture request signal enable bit enabled	R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	—			
b4	ELCICE1	Timer RD1 ELC input capture request signal select bit	0: Input capture TRDIOD1 is selected 1: Timer RD1 ELC input capture request signal selected	R/W
b5	ELCOBE1	Timer RD1 ELC input capture request signal enable bit for pulse forced cutoff ($\overline{INT0}$)	0: Timer RD1 ELC input capture request signal enable bit disabled 1: Timer RD1 ELC input capture request signal enable bit enabled	R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

18.2.2 Timer RD Trigger Control Register (TRDADCR)

18.2.2.1 Output Compare Function, PWM Mode, Reset Synchronous PWM Mode, Complementary PWM Mode, and PWM3 Mode

Address 00182h (TRDADCR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADTRGD1E	ADTRGC1E	ADTRGB1E	ADTRGA1E	ADTRGD0E	ADTRGC0E	ADTRGB0E	ADTRGA0E
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGA0E	A/D trigger A0 enable bit (1)	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRA0	R/W
b1	ADTRGB0E	A/D trigger B0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRB0	R/W
b2	ADTRGC0E	A/D trigger C0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRC0	R/W
b3	ADTRGD0E	A/D trigger D0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRD0	R/W
b4	ADTRGA1E	A/D trigger A1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRA1	R/W
b5	ADTRGB1E	A/D trigger B1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRB1	R/W
b6	ADTRGC1E	A/D trigger C1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRC1	R/W
b7	ADTRGD1E	A/D trigger D1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRD1	R/W

Note:
1. Set to 0 in complementary PWM mode.

18.2.3 Timer RD Start Register (TRDSTR)

Address 00183h (TRDSTR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	CSEL1	CSEL0	TSTART1	TSTART0
After Reset	1	1	1	1	1	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART0	TRD0 count start flag (1, 2)	0: Count stops 1: Count starts	R/W
b1	TSTART1	TRD1 count start flag (3, 4)		R/W
b2	CSEL0	TRD0 count operation select bit	0: Count stops at compare match with TRDGRA0 register 1: Count continues after compare match with TRDGRA0 register (5)	R/W
b3	CSEL1	TRD1 count operation select bit (6)	0: Count stops at compare match with TRDGRA1 register 1: Count continues after compare match with TRDGRA1 register (5)	R/W
b4	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b5	—			
b6	—			
b7	—			

Note:
1. To stop the count operation of timer RD0, write 0 to the TSTART0 bit while the CSEL0 bit is 1.
2. When the CSEL0 bit is 0 and a compare match signal (TRDIOA0) is generated, this flag is set to 0 (count stops).
3. To stop the count operation of timer RD1, write 0 to the TSTART1 bit while the CSEL1 bit is 1.
4. When the CSEL1 bit is 0 and a compare match signal (TRDIOA1) is generated, this flag is set to 0 (count stops).
5. Set to 1 for the input capture function.
6. Do not use in PWM3 mode.

Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **18.4.1.2 TRDSTR Register** in the usage notes on timer RD.

18.2.4 Timer RD Mode Register (TRDMR)

Address 00184h (TRDMR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BFD1	BFC1	BFD0	BFC0	—	—	—	SYNC
After Reset	0	0	0	0	1	1	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	SYNC	Timer RD synchronous bit (1)	0: Registers TRD0 and TRD1 operate independently 1: Registers TRD0 and TRD1 operate synchronously	R/W
b1	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b2	—			
b3	—			
b4	BFC0	TRDGRC0 register function select bit (2, 3)	0: General register 1: Buffer register for TRDGRA0 register	R/W
b5	BFD0	TRDGRD0 register function select bit (3)	0: General register 1: Buffer register for TRDGRB0 register	R/W
b6	BFC1	TRDGRC1 register function select bit (3)	0: General register 1: Buffer register for TRDGRA1 register	R/W
b7	BFD1	TRDGRD1 register function select bit (3)	0: General register 1: Buffer register for TRDGRB1 register	R/W

Notes:
1. Set to 0 (TRD0 and TRD1 operate independently) in reset synchronous PWM mode, complementary PWM mode, and PWM3 mode.
2. Set to 0 (general register) in complementary PWM mode.
3. In the output compare function, if 0 (TRDGRji register output pin is changed) is selected for the IOj3 (j = C or D) bit in the TRDIORCi (i = 0 or 1) register, set the BFji bit in the TRDMR register to 0.

18.2.5 Timer RD PWM Mode Register (TRDPMR)

18.2.5.1 Input Capture Function, Output Compare Function, and PWM Mode

Address 00185h (TRDPMR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	PWMD1	PWMC1	PWMB1	—	PWMD0	PWMC0	PWMB0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PWMB0	PWM mode of TRDIOB0 select bit (1)	0: Timer mode 1: PWM mode	R/W
b1	PWMC0	PWM mode of TRDIOC0 select bit (1)		R/W
b2	PWMD0	PWM mode of TRDIOD0 select bit (1)		R/W
b3	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b4	PWMB1	PWM mode of TRDIOB1 select bit (1)	0: Timer mode 1: PWM mode	R/W
b5	PWMC1	PWM mode of TRDIOC1 select bit (1)		R/W
b6	PWMD1	PWM mode of TRDIOD1 select bit (1)		R/W
b7	—	Nothing is assigned. The write value must be 1. The read value is 1.		—

Note:
1. Set to 0 (timer mode) for the input capture and output compare functions.

18.2.6 Timer RD Function Control Register (TRDFCR)

Address 00186h (TRDFCR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PWM3	STCLK	ADEG	ADTRG	OLS1	OLS0	CMD1	CMD0
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CMD0	Combination mode select bits (1, 2)	• In the input capture function, the output compare function, PWM mode, and PWM3 mode, set to 00b (timer mode, PWM mode, PWM3 mode). • In reset synchronous PWM mode, set to 01b (reset synchronous PWM mode). • In complementary PWM mode, b1 b0 1 0: Complementary PWM mode (transfer from the buffer register to the general register when TRD1 underflows) 1 1: Complementary PWM mode (transfer from the buffer register to the general register at compare match between registers TRD0 and TRDGRA0) Other than the above: Do not set.	R/W
b1	CMD1			R/W
b2	OLS0	Normal-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	• In reset synchronous and complementary PWM modes, 0: High initial output and low active level 1: Low initial output and high active level • Disabled in the input capture function, the output compare function, PWM mode, and PWM3 mode.	R/W
b3	OLS1	Counter-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)		R/W
b4	ADTRG	A/D trigger enable bit (in complementary PWM mode)	• In complementary PWM mode, 0: A/D trigger disabled 1: A/D trigger enabled (3) • Disabled in the input capture function, the output compare function, PWM mode, reset synchronous PWM mode, and PWM3 mode.	R/W
b5	ADEG	A/D trigger generation select bit (in complementary PWM mode)	• In complementary PWM mode, 0: A/D trigger is generated at compare match between registers TRD0 and TRDGRA0 1: A/D trigger is generated when TRD1 underflows • Disabled in the input capture function, the output compare function, PWM mode, reset synchronous PWM mode, and PWM3 mode.	R/W
b6	STCLK	External clock input select bit	• In the input capture function, the output compare function, PWM mode, reset synchronous PWM mode, and complementary PWM mode, 0: External clock input disabled 1: External clock input enabled • In PWM3 mode, set to 0 (external clock input disabled).	R/W
b7	PWM3	PWM3 mode select bit (4)	• In the input capture function, the output compare function, and PWM mode, set to 1 (other than PWM3 mode). • In PWM3 mode, set to 0 (PWM3 mode). • Disabled in reset synchronous and complementary PWM modes.	R/W

Notes:
1. Set bits CMD0 and CMD1 when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).
2. When bits CMD1 and CMD0 are set to 01b, 10b, or 11b, the MCU enters reset synchronous PWM mode or complementary PWM mode regardless of the settings of the TRDPMR register.
3. Set bits ADCAP1 and ADCAP0 in the ADMOD register to 10b (start by timer RD).
4. When bits CMD1 and CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

18.2.7 Timer RD Output Master Enable Register 1 (TRDOER1)

18.2.7.1 Output Compare Function, PWM Mode, Reset Synchronous PWM Mode, Complementary PWM Mode, and PWM3 Mode

Address 00187h (TRDOER1_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ED1	EC1	EB1	EA1	ED0	EC0	EB0	EA0
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	EA0	TRDIOA0 output disable bit (1)	0: Output enabled 1: Output disabled (TRDIOA0 pin functions as a programmable I/O port)	R/W
b1	EB0	TRDIOB0 output disable bit	0: Output enabled 1: Output disabled (TRDIOB0 pin functions as a programmable I/O port)	R/W
b2	EC0	TRDIOC0 output disable bit (2)	0: Output enabled 1: Output disabled (TRDIOC0 pin functions as a programmable I/O port)	R/W
b3	ED0	TRDIOD0 output disable bit (2)	0: Output enabled 1: Output disabled (TRDIOD0 pin functions as a programmable I/O port)	R/W
b4	EA1	TRDIOA1 output disable bit (3)	0: Output enabled 1: Output disabled (TRDIOA1 pin functions as a programmable I/O port)	R/W
b5	EB1	TRDIOB1 output disable bit (2)	0: Output enabled 1: Output disabled (TRDIOB1 pin functions as a programmable I/O port)	R/W
b6	EC1	TRDIOC1 output disable bit (2)	0: Output enabled 1: Output disabled (TRDIOC1 pin functions as a programmable I/O port)	R/W
b7	ED1	TRDIOD1 output disable bit (2)	0: Output enabled 1: Output disabled (TRDIOD1 pin functions as a programmable I/O port)	R/W

Notes:
1. Set to 1 in PWM mode, reset synchronous PWM mode, and complementary PWM mode.
2. Set to 1 in PWM3 mode.
3. Set to 1 in PWM mode and PWM3 mode.

18.2.8 Timer RD Output Master Enable Register 2 (TRDOER2)

18.2.8.1 Output Compare Function, PWM Mode, Reset Synchronous PWM Mode, Complementary PWM Mode, and PWM3 Mode

Address 00188h (TRDOER2_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PTO	—	—	—	—	—	—	—
After Reset	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit (1)	0: Pulse output forced cutoff input disabled 1: Pulse output forced cutoff input enabled (All bits in the TRDOER1 register are set to 1 (output disabled) when a low level is applied to the $\overline{\text{INT0}}$ pin.)	R/W

Note:
1. Refer to **18.3.1.4 Pulse Output Forced Cutoff**.

18.2.9 Timer RD Output Control Register (TRDOCR)

Write to the TRDOCR register when bits TSTART0 and TSTART1 in the TRDSTR register are both 0 (count stops).

Address 00189h (TRDOCR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TOD1	TOC1	TOB1	TOA1	TOD0	TOC0	TOB0	TOA0
After Reset	0	0	0	0	0	0	0	0

18.2.9.1 Output Compare Function

Bit	Symbol	Bit Name	Function	R/W
b0	TOA0	TRDIOA0 output level select bit	0: Low initial output 1: High initial output	R/W
b1	TOB0	TRDIOB0 output level select bit (1)		R/W
b2	TOC0	TRDIOC0 initial output level select bit (1)		R/W
b3	TOD0	TRDIOD0 initial output level select bit (1)		R/W
b4	TOA1	TRDIOA1 initial output level select bit		R/W
b5	TOB1	TRDIOB1 initial output level select bit (1)		R/W
b6	TOC1	TRDIOC1 initial output level select bit (1)		R/W
b7	TOD1	TRDIOD1 initial output level select bit (1)		R/W

Note:
1. If the pin function is set for waveform output, the initial output level is output when the TRDOCR register is set.

18.2.9.2 PWM Mode

Bit	Symbol	Bit Name	Function	R/W
b0	TOA0	TRDIOA0 output level select bit	Set to 0.	R/W
b1	TOB0	TRDIOB0 output level select bit (1)	0: Initial output is inactive level 1: Initial output is active level	R/W
b2	TOC0	TRDIOC0 initial output level select bit (1)	0: Initial output is inactive level 1: Initial output is active level Enabled in reset synchronous and complementary PWM modes.	R/W
b3	TOD0	TRDIOD0 initial output level select bit (1)	0: Initial output is inactive level 1: Initial output is active level	R/W
b4	TOA1	TRDIOA1 initial output level select bit	Set to 0.	R/W
b5	TOB1	TRDIOB1 initial output level select bit (1)	0: Initial output is inactive level 1: Initial output is active level	R/W
b6	TOC1	TRDIOC1 initial output level select bit (1)		R/W
b7	TOD1	TRDIOD1 initial output level select bit (1)		R/W

Note:
1. If the pin function is set for waveform output, the initial output level is output when the TRDOCR register is set.

18.2.9.3 PWM3 Mode

Bit	Symbol	Bit Name	Function	R/W
b0	TOA0	TRDIOA0 output level select bit	0: Low initial output, high active level, high output at TRDGRA1 compare match, and low output at TRDGRA0 compare match 1: High initial output, low active level, low output at TRDGRA1 compare match, and high output at TRDGRA0 compare match	R/W
b1	TOB0	TRDIOB0 output level select bit (1)	0: Low initial output, high active level, high output at TRDGRB1 compare match, and low output at TRDGRB0 compare match 1: High initial output, low active level, low output at TRDGRB1 compare match, and high output at TRDGRB0 compare match	R/W
b2	TOC0	TRDIOC0 initial output level select bit	Disabled in PWM3 mode.	R/W
b3	TOD0	TRDIOD0 initial output level select bit		R/W
b4	TOA1	TRDIOA1 initial output level select bit		R/W
b5	TOB1	TRDIOB1 initial output level select bit		R/W
b6	TOC1	TRDIOC1 initial output level select bit		R/W
b7	TOD1	TRDIOD1 initial output level select bit		R/W

Note:
1. If the pin function is set for waveform output, the initial output level is output when the TRDOCR register is set.

18.2.10 Timer RD Digital Filter Function Select Register i (TRDDFi) (i = 0 or 1)

18.2.10.1 Input Capture Function

Address 0018Ah (TRDDF0_0), 0018Bh (TRDDF1_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DFCK1	DFCK0	—	—	DFD	DFC	DFB	DFA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRDIOA pin digital filter function select bit	0: Function is not used 1: Function is used	R/W
b1	DFB	TRDIOB pin digital filter function select bit		R/W
b2	DFC	TRDIOC pin digital filter function select bit		R/W
b3	DFD	TRDIOD pin digital filter function select bit		R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	DFCK0	Clock select bits for digital filter function (1)	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits TCK0 to TCK2 in the TRDCRi register)	R/W
b7	DFCK1			R/W

Note:
1. Set bits DFCK0 and DFCK1 before starting the count operation.

DFj Bit (TRDIOj pin digital filter function select bit) (j = A, B, C, or D)

If the digital filter is enabled, correct edge detection is performed after five or more cycles of the digital filter sampling clock have elapsed.

18.2.11 Timer RD Control Register i (TRDCRi) (i = 0 or 1)

The TRDCR1 register is not used in reset synchronous PWM mode or PWM3 mode.

Address 00190h (TRDCR0_0), 001A0h (TRDCR1_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
After Reset	0	0	0	0	0	0	0	0

18.2.11.1 Input Capture Function and Output Compare Function

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bits	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRDCLK input (1) 1 1 0: fHOCO 1 1 1: fHOCO-F (2)	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock edge select bits (3)	b4 b3 0 0: Count at the rising edge 0 1: Count at the falling edge 1 0: Count at both edges 1 1: Do not set.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRDi counter clear select bits	b7 b6 b5 0 0 0: Clear disabled (free-running operation) 0 0 1: Clear by input capture/compare match with TRDGRAi 0 1 0: Clear by input capture/compare match with TRDGRBi 0 1 1: Synchronous clear (clear simultaneously with other timer RDi counter) (4) 1 0 0: Do not set. 1 0 1: Clear by input capture/compare match with TRDGRCi 1 1 0: Clear by input capture/compare match with TRDGRDi 1 1 1: Do not set.	R/W
b6	CCLR1			R/W
b7	CCLR2			R/W

Notes:
1. Enabled when the STCLK bit in the TRDFCR register is 1 (external clock input enabled).
2. When selecting fHOCO-F, set it to a higher clock frequency than the CPU clock frequency.
3. Enabled when bits TCK2 to TCK0 are 101b (TRDCLK input), the STCLK bit is 1 (external clock input enabled).
4. Enabled when the SYNC bit in the TRDMR register is 1 (registers TRD0 and TRD1 operate synchronously).

18.2.11.2 PWM Mode

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bits	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRDCLK input (1) 1 1 0: fHOCO 1 1 1: fHOCO-F (2)	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock edge select bits (3)	b4 b3 0 0: Count at the rising edge 0 1: Count at the falling edge 1 0: Count at both edges 1 1: Do not set.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRDi counter clear select bits	Set to 001b (TRDi register is cleared by compare match with TRDGRAi register).	R/W
b6	CCLR1			R/W
b7	CCLR2			R/W

Notes:
1. Enabled when the STCLK bit in the TRDFCR register is 1 (external clock input enabled).
2. When selecting fHOCO-F, set it to a higher clock frequency than the CPU clock frequency.
3. Enabled when bits TCK2 to TCK0 are 101b (TRDCLK input), the STCLK bit is 1 (external clock input enabled).

18.2.11.3 Reset Synchronous PWM Mode

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bits	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRDCLK input (1) 1 1 0: fHOCO 1 1 1: fHOCO-F (2)	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock edge select bits (3)	b4 b3 0 0: Count at the rising edge 0 1: Count at the falling edge 1 0: Count at both edges 1 1: Do not set.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRD0 counter clear select bits	Set to 001b (TRD0 register is cleared by compare match with TRDGRA0 register).	R/W
b6	CCLR1			R/W
b7	CCLR2			R/W

Notes:
1. Enabled when the STCLK bit in the TRDFCR register is 1 (external clock input enabled).
2. When selecting fHOCO-F, set it to a higher clock frequency than the CPU clock frequency.
3. Enabled when bits TCK2 to TCK0 are 101b (TRDCLK input), the STCLK bit is 1 (external clock input enabled).

18.2.11.4 Complementary PWM Mode

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bits (1)	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRDCLK input (2) 1 1 0: fHOCO 1 1 1: fHOCO-F (3)	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock edge select bits (1, 4)	b4 b3 0 0: Count at the rising edge 0 1: Count at the falling edge 1 0: Count at both edges 1 1: Do not set.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRDi counter clear select bits	Set to 000b (clear disabled (free-running operation)).	R/W
b6	CCLR1			R/W
b7	CCLR2			R/W

Notes:
1. Set the same value to bits TCK0 to TCK2, CKEG0, and CKEG1 in registers TRDCR0 and TRDCR1.
2. Enabled when the STCLK bit in the TRDFCR register is 1 (external clock input enabled).
3. When selecting fHOCO-F, set it to a higher clock frequency than the CPU clock frequency.
4. Enabled when bits TCK2 to TCK0 are 101b (TRDCLK input), the STCLK bit is 1 (external clock input enabled).

18.2.11.5 PWM3 Mode

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bits	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: Do not set. 1 1 0: fHOCO 1 1 1: fHOCO-F (1)	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock edge select bits	Disabled in PWM3 mode.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRD0 counter clear select bits	Set to 001b (TRD0 register is cleared by compare match with TRDGRA0 register).	R/W
b6	CCLR1			R/W
b7	CCLR2			R/W

Note:
1. When selecting fHOCO-F, set it to a higher clock frequency than the CPU clock frequency.

18.2.12 Timer RD I/O Control Register Ai (TRDIORAi) (i = 0 or 1)

Address 00191h (TRDIORA0_0), 001A1h (TRDIORA1_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

18.2.12.1 Input Capture Function

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRDGRA control bits (1)	b1 b0 0 0: Input capture to TRDGRAi at the rising edge 0 1: Input capture to TRDGRAi at the falling edge 1 0: Input capture to TRDGRAi at both edges 1 1: Do not set.	R/W
b1	IOA1			R/W
b2	IOA2	TRDGRA mode select bit (2)	Set to 1 (input capture) for the input capture function.	R/W
b3	IOA3	Input-capture input switch bit (3, 4)	0: fOCO128 1: TRDIOA0 pin input	R/W
b4	IOB0	TRDGRB control bits	b5 b4 0 0: Input capture to TRDGRBi at the rising edge 0 1: Input capture to TRDGRBi at the falling edge 1 0: Input capture to TRDGRBi at both edges 1 1: Do not set.	R/W
b5	IOB1			R/W
b6	IOB2	TRDGRB mode select bit (5)	Set to 1 (input capture) for the input capture function.	R/W
b7	—	Nothing is assigned. The write value must be 1. The read value is 1.		—

Notes:
1. When the IOA3 bit is 0 (fOCO128), set bits IOA1 and IOA0 to 00b.
2. If 1 (buffer register for TRDGRAi register) is selected for the BFCi bit in the TRDMR register, set the same value to the IOA2 bit in the TRDIORAi register and the IOC2 bit in the TRDIORCi register.
3. Enabled when the IOA2 bit is 1 (input capture function).
4. The IOA3 bit only exists in the TRDIORA0 register, not the TRDIORA1 register.
   When writing to b3, write 1. The read value is 1.
5. If 1 (buffer register for TRDGRBi register) is selected for the BFDi bit in the TRDMR register, set the same value to the IOB2 bit in the TRDIORAi register and the IOD2 bit in the TRDIORCi register.

18.2.12.2 Output Compare Function

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRDGRA control bits	b1 b0 0 0: Pin output by compare match is disabled (TRDIOAi pin functions as a programmable I/O port) 0 1: Low output at compare match with TRDGRAi 1 0: High output at compare match with TRDGRAi 1 1: Toggle output at compare match with TRDGRAi	R/W
b1	IOA1			R/W
b2	IOA2	TRDGRA mode select bit (1)	Set to 0 (output compare) for the output compare function.	R/W
b3	IOA3	Input-capture input switch bit (2)	Set to 1 (TRDIOA0 pin input) for the output compare function.	R/W
b4	IOB0	TRDGRB control bits	b5 b4 0 0: Pin output by compare match is disabled (TRDIOBi pin functions as a programmable I/O port) 0 1: Low output at compare match with TRDGRBi 1 0: High output at compare match with TRDGRBi 1 1: Toggle output at compare match with TRDGRBi	R/W
b5	IOB1			R/W
b6	IOB2	TRDGRB mode select bit (3)	Set to 0 (output compare) for the output compare function.	R/W
b7	—	Nothing is assigned. The write value must be 1. The read value is 1.		—

Notes:
1. If 1 (buffer register for TRDGRAi register) is selected for the BFCi bit in the TRDMR register, set the same value to the IOA2 bit in the TRDIORAi register and the IOC2 bit in the TRDIORCi register.
2. The IOA3 bit only exists in the TRDIORA0 register, not the TRDIORA1 register.
   When writing to b3, write 1. The read value is 1.
3. If 1 (buffer register for TRDGRBi register) is selected for the BFDi bit in the TRDMR register, set the same value to the IOB2 bit in the TRDIORAi register and the IOD2 bit in the TRDIORCi register.

18.2.13 Timer RD I/O Control Register Ci (TRDIORCi) (i = 0 or 1)

Address 00192h (TRDIORC0_0), 001A2h (TRDIORC1_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

18.2.13.1 Input Capture Function

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRDGRC control bits	b1 b0 0 0: Input capture to TRDGRCi at the rising edge 0 1: Input capture to TRDGRCi at the falling edge 1 0: Input capture to TRDGRCi at both edges 1 1: Do not set.	R/W
b1	IOC1			R/W
b2	IOC2	TRDGRC mode select bit (1)	Set to 1 (input capture) for the input capture function.	R/W
b3	IOC3	TRDGRC register function select bit	Set to 1 (general register or buffer register) for the input capture function.	R/W
b4	IOD0	TRDGRD control bits	b5 b4 0 0: Input capture to TRDGRDi at the rising edge 0 1: Input capture to TRDGRDi at the falling edge 1 0: Input capture to TRDGRDi at both edges 1 1: Do not set.	R/W
b5	IOD1			R/W
b6	IOD2	TRDGRD mode select bit (2)	Set to 1 (input capture) for the input capture function.	R/W
b7	IOD3	TRDGRD register function select bit	Set to 1 (general register or buffer register) for the input capture function.	R/W

Notes:
1. If 1 (buffer register for TRDGRAi register) is selected for the BFCi bit in the TRDMR register, set the same value to the IOA2 bit in the TRDIORAi register and the IOC2 bit in the TRDIORCi register.
2. If 1 (buffer register for TRDGRBi register) is selected for the BFDi bit in the TRDMR register, set the same value to the IOB2 bit in the TRDIORAi register and the IOD2 bit in the TRDIORCi register.

18.2.13.2 Output Compare Function

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRDGRC control bits	b1 b0 0 0: Pin output by compare match is disabled 0 1: Low output at compare match with TRDGRCi 1 0: High output at compare match with TRDGRCi 1 1: Toggle output at compare match with TRDGRCi	R/W
b1	IOC1			R/W
b2	IOC2	TRDGRC mode select bit (1)	Set to 0 (output compare) for the output compare function.	R/W
b3	IOC3	TRDGRC register function select bit	0: TRDIOA output register (refer to **18.3.3.2 Changing Output Pins in Registers TRDGRCi (i = 0 or 1) and TRDGRDi**) 1: General register or buffer register	R/W
b4	IOD0	TRDGRD control bits	b5 b4 0 0: Pin output by compare match is disabled 0 1: Low output at compare match with TRDGRDi 1 0: High output at compare match with TRDGRDi 1 1: Toggle output at compare match with TRDGRDi	R/W
b5	IOD1			R/W
b6	IOD2	TRDGRD mode select bit (2)	Set to 0 (output compare) for the output compare function.	R/W
b7	IOD3	TRDGRD register function select bit	0: TRDIOB output register (refer to **18.3.3.2 Changing Output Pins in Registers TRDGRCi (i = 0 or 1) and TRDGRDi**) 1: General register or buffer register	R/W

Notes:
1. If 1 (buffer register for TRDGRAi register) is selected for the BFCi bit in the TRDMR register, set the same value to the IOA2 bit in the TRDIORAi register and the IOC2 bit in the TRDIORCi register.
2. If 1 (buffer register for TRDGRBi register) is selected for the BFDi bit in the TRDMR register, set the same value to the IOB2 bit in the TRDIORAi register and the IOD2 bit in the TRDIORCi register.

18.2.14 Timer RD Status Register i (TRDSRi) (i = 0 or 1)

Address 00193h (TRDSR0_0), 001A3h (TRDSR1_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	UDF	OVF	IMFD	IMFC	IMFB	IMFA	
After Reset	1	1	1	0	0	0	0	0	TRDSR0 register
After Reset	1	1	0	0	0	0	0	0	TRDSR1 register

18.2.14.1 Input Capture Function

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture/compare match flag A	[Source for setting to 0] Write 0 after reading. (1) [Source for setting to 1] TRDSR0 register: Edge of fOCO128 when the IOA3 bit in the TRDIORA0 register is 0 (fOCO128). Input edge of TRDIOA0 pin when the IOA3 bit in the TRDIORA0 register is 1 (TRDIOA0 input) (2) TRDSR1 register: Input edge of TRDIOA1 pin (2)	R/W
b1	IMFB	Input capture/compare match flag B	[Source for setting to 0] Write 0 after reading. (1) [Source for setting to 1] Input edge of TRDIOBi pin (2)	R/W
b2	IMFC	Input capture/compare match flag C	[Source for setting to 0] Write 0 after reading. (1) [Source for setting to 1] Input edge of TRDIOCi pin (3)	R/W
b3	IMFD	Input capture/compare match flag D	[Source for setting to 0] Write 0 after reading (1) [Source for setting to 1] Input edge of TRDIODi pin (3)	R/W
b4	OVF	Overflow flag (4)	[Source for setting to 0] Write 0 after reading (1) [Source for setting to 1] When the TRDi register overflows	R/W
b5	UDF	Underflow flag (5)	Disabled in the input capture function.	R/W
b6	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b7	—			

Notes:
1. The writing results are as follows:
   - If the read value is 1, writing 0 to the bit sets it to 0.
   - If the read value is 0, the bit remains unchanged even if 0 is written to it. (Even if the bit is changed from 0 to 1 after reading and then 0 is written to it, it remains 1.)
   - Writing 1 has no effect.
2. Edge selected by bits IOj1 and IOj0 (j = A or B) in the TRDIORAi register.
3. Edge selected by bits IOk1 and IOk0 (k = C or D) in the TRDIORCi register.
   Including when the BFki bit in the TRDMR register is 1 (TRDGRki is buffer register).
4. When the counter value of timer RDi changes from FFFFh to 0000h, the overflow flag is set to 1.
   Also, if the counter value of timer RDi changes from FFFFh to 0000h due to an input capture/compare match during operation according to the settings of bits CCLR0 to CCLR2 in the TRDCRi register, the overflow flag is set to 1.
5. Nothing is assigned to b5 in the TRDSR0 register. When writing to b5, write 0. The read value is 1.

18.2.14.2 Functions Other Than Input Capture Function

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture/compare match flag A	[Source for setting to 0] Write 0 after reading. (1) [Source for setting to 1] When the values of TRDi (i = 0 or 1) and TRDGRAi match.	R/W
b1	IMFB	Input capture/compare match flag B	[Source for setting to 0] Write 0 after reading. (1) [Source for setting to 1] When the values of TRDi and TRDGRBi match.	R/W
b2	IMFC	Input capture/compare match flag C	[Source for setting to 0] Write 0 after reading. (1) [Source for setting to 1] When the values of TRDi and TRDGRCi match. (2)	R/W
b3	IMFD	Input capture/compare match flag D	[Source for setting to 0] Write 0 after reading. (1) [Source for setting to 1] When the values of TRDi and TRDGRDi match. (2)	R/W
b4	OVF	Overflow flag (3)	[Source for setting to 0] Write 0 after reading. (1) [Source for setting to 1] When TRDi overflows.	R/W
b5	UDF	Underflow flag (4)	In complementary PWM mode [Source for setting to 0] Write 0 after reading. (1) [Source for setting to 1] When TRDi underflows. Enabled only in complementary PWM mode.	R/W
b6	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b7	—			

Notes:
1. The writing results are as follows:
   - If the read value is 1, writing 0 to the bit sets it to 0.
   - If the read value is 0, the bit remains unchanged even if 0 is written to it. (Even if the bit is changed from 0 to 1 after reading and then 0 is written to it, it remains 1.)
   - Writing 1 has no effect.
2. Including when the BFki bit (k = C or D) in the TRDMR register is set to 1 (TRDGRKi is buffer register).
3. When the counter value of timer RDi changes from FFFFh to 0000h, the overflow flag is set to 1.
   Also, if the counter value of timer RDi changes from FFFFh to 0000h due to an input capture/compare during operation according to the settings of bits CCLR0 to CCLR2 in the TRDCRi register, the overflow flag is set to 1.
4. Nothing is assigned to b5 in the TRDSR0 register. The write value must be 1 for b5. The read value is 1.

18.2.15 Timer RD Interrupt Enable Register i (TRDIERi) (i = 0 or 1)

Address 00194h (TRDIER0_0), 001A4h (TRDIER1_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA
After Reset	1	1	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input capture/compare match interrupt enable bit A	0: Interrupt (IMIA) by the IMFA bit is disabled 1: Interrupt (IMIA) by the IMFA bit is enabled	R/W
b1	IMIEB	Input capture/compare match interrupt enable bit B	0: Interrupt (IMIB) by the IMFB bit is disabled 1: Interrupt (IMIB) by the IMFB bit is enabled	R/W
b2	IMIEC	Input capture/compare match interrupt enable bit C	0: Interrupt (IMIC) by the IMFC bit is disabled 1: Interrupt (IMIC) by the IMFC bit is enabled	R/W
b3	IMIED	Input capture/compare match interrupt enable bit D	0: Interrupt (IMID) by the IMFD bit is disabled 1: Interrupt (IMID) by the IMFD bit is enabled	R/W
b4	OVIE	Overflow/underflow interrupt enable bit	0: Interrupt (OVI) by bits OVF and UDF disabled 1: Interrupt (OVI) by bits OVF and UDF enabled	R/W
b5	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b6	—			
b7	—			

18.2.16 Timer RD PWM Mode Output Level Control Register i (TRDPOCRi) (i = 0 or 1)

Address 00195h (TRDPOCR0_0), 001A5h (TRDPOCR1_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	POLD	POLC	POLB
After Reset	1	1	1	1	1	0	0	0

18.2.16.1 PWM Mode

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B	0: TRDIOBi output level is low active 1: TRDIOBi output level is high active	R/W
b1	POLC	PWM mode output level control bit C	0: TRDIOCi output level is low active 1: TRDIOCi output level is high active	R/W
b2	POLD	PWM mode output level control bit D	0: TRDIODi output level is low active 1: TRDIODi output level is high active	R/W
b3	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b4	—			
b5	—			
b6	—			
b7	—			

Settings to the TRDPOCRi register are enabled only in PWM mode. When not in PWM mode, they are disabled.

18.2.17 Timer RD Counter i (TRDi) (i = 0 or 1)

Address 00196h (TRD0_0), 001A6h (TRD1_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRDi7	TRDi6	TRDi5	TRDi4	TRDi3	TRDi2	TRDi1	TRDi0
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	TRDi15	TRDi14	TRDi13	TRDi12	TRDi11	TRDi10	TRDi9	TRDi8
After Reset	0	0	0	0	0	0	0	0

18.2.17.1 Input Capture Function, Output Compare Function, and PWM Mode

Bit	Function	Setting Range	R/W
b15 to b0	Count the count source. Count operation is increment. When an overflow occurs, the OVF bit in the TRDSRi register is set to 1.	0000h to FFFFh	R/W

Access the TRDi register in 16-bit units. Do not access it in 8-bit units.

18.2.17.2 Reset Synchronous PWM Mode and PWM3 Mode

Bit	Function	Setting Range	R/W
b15 to b0	Count the count source. Count operation is increment. When an overflow occurs, the OVF bit in the TRDSR0 register is set to 1.	0000h to FFFFh	R/W

Access the TRD0 register in 16-bit units. Do not access it in 8-bit units. The TRD1 register is not used in reset synchronous PWM mode and PWM3 mode.

18.2.17.3 Complementary PWM Mode (TRD0)

Bit	Function	Setting Range	R/W
b15 to b0	The dead time must be set. Count the count source. Count operation is increment or decrement. When an overflow occurs, the OVF bit in the TRDSR0 register is set to 1.	0001h to FFFFh	R/W

Access the TRD0 register in 16-bit units. Do not access it in 8-bit units.

18.2.17.4 Complementary PWM Mode (TRD1)

Bit	Function	Setting Range	R/W
b15 to b0	Set to 0000h. Count the count source. Count operation is increment or decrement. When an underflow occurs, the UDF bit in the TRDSR1 register is set to 1.	0000h to FFFFh	R/W

Access the TRD1 register in 16-bit units. Do not access it in 8-bit units.

18.2.18 Timer RD General Registers ji (TRDGRji) (j = A, B, C, or D, i = 0 or 1)

Address 00198h (TRDGRA0_0), 0019Ah (TRDGRB0_0),
0019Ch (TRDGRC0_0), 0019Eh (TRDGRD0_0),
001A8h (TRDGRA1_0), 001AAh (TRDGRB1_0),
001ACh (TRDGRC1_0), 001AEh (TRDGRD1_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRDGRji7	TRDGRji6	TRDGRji5	TRDGRji4	TRDGRji3	TRDGRji2	TRDGRji1	TRDGRji0
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	TRDGRji15	TRDGRji14	TRDGRji13	TRDGRji12	TRDGRji11	TRDGRji10	TRDGRji9	TRDGRji8
After Reset	1	1	1	1	1	1	1	1

18.2.18.1 Input Capture Function

Bit	Function	R/W
b15 to b0	Refer to **Table 18.4 TRDGRji Register Functions in Input Capture Function**.	R/W

Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.

The following registers are disabled in the input capture function:
TRDOER1, TRDOER2, TRDOCR, TRDPOCR0, and TRDPOCR1

Table 18.4 TRDGRji Register Functions in Input Capture Function

Register	Setting	Register Function	Input-Capture Input Pin
TRDGRAi	—	General register. The value of the TRDi register can be read at input capture.	TRDIOAi
TRDGRBi			TRDIOBi
TRDGRCi	BFCi = 0	General register. The value of the TRDi register can be read at input capture.	TRDIOCi
TRDGRDi	BFDi = 0		TRDIODi
TRDGRCi	BFCi = 1	Buffer register. The value of the TRDi register can be read at input capture (refer to **18.3.1.2 Buffer Operation**).	TRDIOAi
TRDGRDi	BFDi = 1		TRDIOBi

i = 0 or 1, j = A, B, C, or D
BFCi, BFDi: Bits in TRDMR register

The pulse width of the input capture signal applied to the TRDIOji pin must be three or more cycles of the timer RD operating clock (refer to **Table 18.1 Timer RD Operating Clocks**) when no digital filter is used (the DFj bit in the TRDDFi register is 0).

18.2.18.2 Output Compare Function

Bit	Function	R/W
b15 to b0	Refer to **Table 18.5 TRDGRji Register Function in Output Compare Function**.	R/W

Access registers TRDGRAi to TRDGRDi (i = 0 or 1) in 16-bit units. Do not access them in 8-bit units.

The following registers are disabled in the output compare function:
TRDDF0, TRDDF1, TRDPOCR0, and TRDPOCR1

Table 18.5 TRDGRji Register Function in Output Compare Function

Register	Setting		Register Function		Output-Compare Output Pin
	BFji	IOj3			
TRDGRAi	—	—	General register. Write the compare value.		TRDIOAi
TRDGRBi					TRDIOBi
TRDGRCi	0	1	General register. Write the compare value.		TRDIOCi
TRDGRDi					TRDIODi
TRDGRCi	1	1	Buffer register. Write the next compare value (refer to **18.3.1.2 Buffer Operation**).		TRDIOAi
TRDGRDi					TRDIOBi
TRDGRCi	0	0	TRDIOAi output control	(refer to **18.3.3.2 Changing Output Pins in Registers TRDGRCi (i = 0 or 1) and TRDGRDi**)	TRDIOAi
TRDGRDi			TRDIOBi output control		TRDIOBi

i = 0 or 1, j = A, B, C, or D
BFji: Bit in TRDMR register, IOj3: Bit in TRDIORCi register

18.2.18.3 PWM Mode

Bit	Function	R/W
b15 to b0	Refer to **Table 18.6 TRDGRji Register Functions in PWM Mode**.	R/W

Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.

The following registers are disabled in PWM mode:
TRDDF0, TRDDF1, TRDIORA0, TRDIORC0, TRDIORA1, and TRDIORC1

Table 18.6 TRDGRji Register Functions in PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRAi	—	General register. Set the PWM period.	—
TRDGRBi	—	General register. Set the changing point of PWM output.	TRDIOBi
TRDGRCi	BFCi = 0	General register. Set the changing point of PWM output.	TRDIOCi
TRDGRDi	BFDi = 0		TRDIODi
TRDGRCi	BFCi = 1	Buffer register. Set the next PWM period (refer to **18.3.1.2 Buffer Operation**).	—
TRDGRDi	BFDi = 1	Buffer register. Set the changing point of the next PWM output (refer to **18.3.1.2 Buffer Operation**).	TRDIOBi

i = 0 or 1, j = A, B, C, or D
BFCi, BFDi: Bits in TRDMR register

18.2.18.4 Reset Synchronous PWM Mode

Bit	Function	R/W
b15 to b0	Refer to **Table 18.7 TRDGRji Register Functions in Reset Synchronous PWM Mode**.	R/W

Access registers TRDGRAi to TRDGRDi (i = 0 or 1) in 16-bit units. Do not access them in 8-bit units.

The following registers are disabled in reset synchronous PWM mode:
TRDPMR, TRDOCR (1), TRDDF0, TRDDF1, TRDIORA0, TRDIORC0, TRDPOCR0, TRDIORA1, TRDIORC1, and TRDPOCR1

Note:
1. The TOC0 bit in the TRDOCR register is enabled as the initial output setting of TRDIOC0 in reset synchronous PWM mode and complementary PWM mode.

Table 18.7 TRDGRji Register Functions in Reset Synchronous PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRA0	—	General register. Set the PWM period.	(TRDIOC0, output inverted every PWM period)
TRDGRB0	—	General register. Set the changing point of PWM1 output.	TRDIOB0 TRDIOD0
TRDGRC0	BFC0 = 0	(Not used in reset synchronous PWM mode.)	—
TRDGRD0	BFD0 = 0		
TRDGRA1	—	General register. Set the changing point of PWM2 output.	TRDIOA1 TRDIOC1
TRDGRB1	—	General register. Set the changing point of PWM3 output.	TRDIOB1 TRDIOD1
TRDGRC1	BFC1 = 0	(Not used in reset synchronous PWM mode.)	—
TRDGRD1	BFD1 = 0		
TRDGRC0	BFC0 = 1	Buffer register. Set the next PWM period (refer to **18.3.1.2 Buffer Operation**).	(TRDIOC0, output inverted every PWM period)
TRDGRD0	BFD0 = 1	Buffer register. Set the changing point of the next PWM1 output (refer to **18.3.1.2 Buffer Operation**).	TRDIOB0 TRDIOD0
TRDGRC1	BFC1 = 1	Buffer register. Set the changing point of the next PWM2 output (refer to **18.3.1.2 Buffer Operation**).	TRDIOA1 TRDIOC1
TRDGRD1	BFD1 = 1	Buffer register. Set the changing point of the next PWM3 output (refer to **18.3.1.2 Buffer Operation**).	TRDIOB1 TRDIOD1

i = 0 or 1, j = A, B, C, or D
BFC0, BFD0, BFC1, BFD1: Bits in TRDMR register

18.2.18.5 Complementary PWM Mode

Bit	Function	R/W
b15 to b0	Refer to **Table 18.8 TRDGRji Register Functions in Complementary PWM Mode**.	R/W

Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.
The TRDGRC0 register is not used in complementary PWM mode.

The following registers are disabled in complementary PWM mode:
TRDPMR, TRDOCR (1), TRDDF0, TRDDF1, TRDIORA0, TRDIORC0, TRDPOCR0, TRDIORA1, TRDIORC1, and TRDPOCR1

Note:
1. The TOC0 bit in the TRDOCR register is enabled as the initial output setting of TRDIOC0 in reset synchronous PWM mode and complementary PWM mode.

Table 18.8 TRDGRji Register Functions in Complementary PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRA0	—	General register. Set the PWM period at initialization. Setting range: ≥ Value set in TRD0 register ≤ FFFFh - value set in TRD0 register Do not write to this register when bits TSTART0 and TSTART1 in the TRDSTR register are set to 1 (count starts).	(TRDIOC0, output inverted every half period)
TRDGRB0	—	General register. Set the changing point of PWM1 output at initialization. Setting range: ≥ Value set in TRD0 register ≤ Value set in TRDGRA0 register - value set in TRD0 register Do not write to this register when bits TSTART0 and TSTART1 in the TRDSTR register are set to 1 (count starts).	TRDIOB0 TRDIOD0
TRDGRA1	—	General register. Set the changing point of PWM2 output at initialization. Setting range: ≥ Value set in TRD0 register ≤ Value set in TRDGRA0 register - value set in TRD0 register Do not write to this register when bits TSTART0 and TSTART1 in the TRDSTR register are set to 1 (count starts).	TRDIOA1 TRDIOC1
TRDGRB1	—	General register. Set the changing point of PWM3 output at initialization. Setting range: ≥ Value set in TRD0 register ≤ Value set in TRDGRA0 register - value set in TRD0 register Do not write to this register when bits TSTART0 and TSTART1 in the TRDSTR register are set to 1 (count starts).	TRDIOB1 TRDIOD1
TRDGRC0	—	(Not used in complementary PWM mode.)	—
TRDGRD0	BFD0 = 1	Buffer register. Set the changing point of next PWM1 output (refer to **18.3.1.2 Buffer Operation**). Setting range: ≥ Value set in TRD0 register ≤ Value set in TRDGRA0 register - value set in TRD0 register Set this register to the same value as the TRDGRB0 register for initialization.	TRDIOB0 TRDIOD0
TRDGRC1	BFC1 = 1	Buffer register. Set the changing point of next PWM2 output (refer to **18.3.1.2 Buffer Operation**). Setting range: ≥ Value set in TRD0 register ≤ Value set in TRDGRA0 register - value set in TRD0 register Set this register to the same value as the TRDGRA1 register for initialization.	TRDIOA1 TRDIOC1
TRDGRD1	BFD1 = 1	Buffer register. Set the changing point of next PWM3 output (refer to **18.3.1.2 Buffer Operation**). Setting range: ≥ Value set in TRD0 register ≤ Value set in TRDGRA0 register - value set in TRD0 register Set this register to the same value as the TRDGRB1 register for initialization.	TRDIOB1 TRDIOD1

i = 0 or 1, j = A, B, C, or D
BFD0, BFC1, BFD1: Bits in TRDMR register

Since values cannot be written to the TRDGRB0, TRDGRA1, or TRDGRB1 register directly after count operation starts (prohibited item), use the TRDGRD0, TRDGRC1, or TRDGRD1 register as a buffer register. However, to write data to the TRDGRD0, TRDGRC1, or TRDGRD1 register, set bits BFD0, BFC1, and BFD1 to 0 (general register). After this, bits BFD0, BFC1, and BFD1 may be set to 1 (buffer register).

18.2.18.6 PWM3 Mode

Bit	Function	R/W
b15 to b0	Refer to **Table 18.9 TRDGRji Register Functions in PWM3 Mode**.	R/W

Access registers TRDGRAi to TRDGRDi (i = 0 or 1) in 16-bit units. Do not access them in 8-bit units.

The following registers are disabled in PWM3 mode:
TRDPMR, TRDDF0, TRDDF1, TRDIORA0, TRDIORC0, TRDPOCR0, TRDIORA1, TRDIORC1, and TRDPOCR1

Table 18.9 TRDGRji Register Functions in PWM3 Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRA0	—	General register. Set the PWM period. Setting range: ≥ Value set in TRDGRA1 register	TRDIOA0
TRDGRA1		General register. Set the changing point (active level timing) of PWM output. Setting range: ≤ Value set in TRDGRA0 register	
TRDGRB0		General register. Set the changing point (the timing for returning to initial output level) of PWM output. Setting range: ≥ Value set in TRDGRB1 register and ≤ value set in TRDGRA0 register	TRDIOB0
TRDGRB1		General register. Set the changing point (active level timing) of PWM output. Setting range: ≤ Value set in TRDGRB0 register	
TRDGRC0	BFC0 = 0	(Not used in PWM3 mode.)	—
TRDGRC1	BFC1 = 0		
TRDGRD0	BFD0 = 0		
TRDGRD1	BFD1 = 0		
TRDGRC0	BFC0 = 1	Buffer register. Set the next PWM period (refer to **18.3.1.2 Buffer Operation**). Setting range: ≥ Value set in TRDGRC1 register	TRDIOA0
TRDGRC1	BFC1 = 1	Buffer register. Set the changing point of next PWM output (refer to **18.3.1.2 Buffer Operation**). Setting range: ≤ Value set in TRDGRC0 register	
TRDGRD0	BFD0 = 1	Buffer register. Set the changing point of next PWM output (refer to **18.3.1.2 Buffer Operation**). Setting range: ≥ Value set in TRDGRD1 register and ≤ value set in TRDGRC0 register	TRDIOB0
TRDGRD1	BFD1 = 1	Buffer register. Set the changing point of next PWM output (refer to **18.3.1.2 Buffer Operation**). Setting range: ≤ Value set in TRDGRD0 register	

i = 0 or 1, j = A, B, C, or D
BFC0, BFD0, BFC1, BFD1: Bits in TRDMR register

Registers TRDGRC0, TRDGRC1, TRDGRD0, and TRDGRD1 are not used in PWM3 mode. To use them as buffer registers, set bits BFC0, BFC1, BFD0, and BFD1 to 0 (general register) and write a value to the TRDGRC0, TRDGRC1, TRDGRD0, or TRDGRD1 register. After this, bits BFC0, BFC1, BFD0, and BFD1 may be set to 1 (buffer register).

18.3 Operation

18.3.1 Items Common to Multiple Modes

18.3.1.1 Count Sources

The count source selection method is the same in all modes. However the external clock cannot be selected in PWM3 mode.

Table 18.10 Count Source Selection

Count Source	Selection
f1, f2, f4, f8, f32	The count source is selected by bits TCK2 to TCK0 in the TRDCRi register.
fHOCO fHOCO-F (1, 2, 3)	The FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator on). Bits TCK2 to TCK0 in the TRDCRi register are set to 110b (fHOCO). Bits TCK2 to TCK0 in the TRDCRi register are set to 111b (fHOCO-F).
External signal input to TRDCLK pin	The STCLK bit in the TRDFCR register is set to 1 (external clock input enabled). Bits TCK2 to TCK0 in the TRDCRi register are set to 101b (count source: external clock). The active edge is selected by bits CKEG1 and CKEG0 in the TRDCRi register. The PD2_0 bit in the PD2 register is set to 0 (input mode).

i = 0 or 1

Notes:
1. The count source fHOCO can be used with VCC = 3.0 V to 5.5 V.
2. Do not set the FRA00 bit to 0 (high-speed on-chip oscillator off) while fHOCO or fHOCO-F is selected as the count source.
3. Do not change the division ratio of the high-speed on-chip oscillator set by the FRA2 register while fHOCO is selected as the count source.

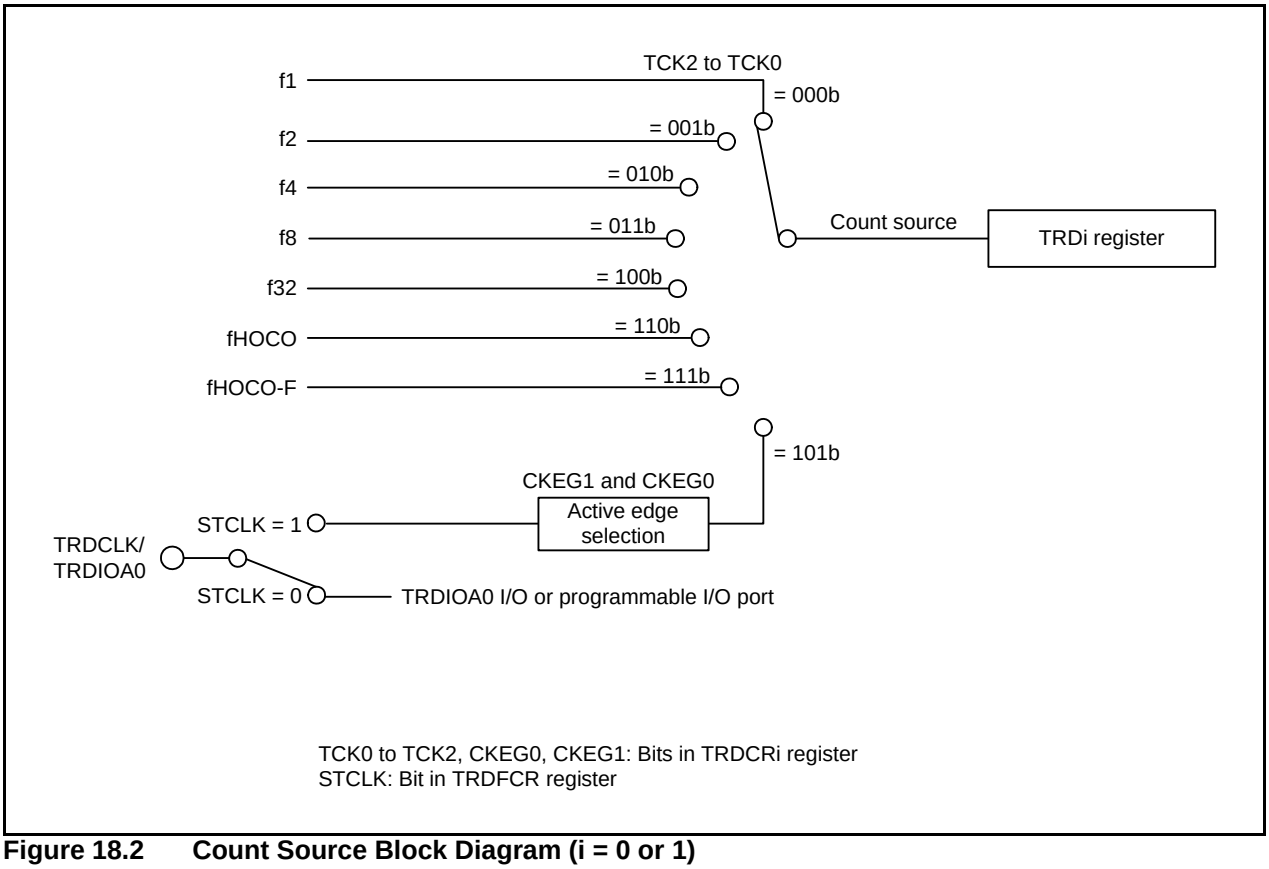


Figure 18.2 Count Source Block Diagram (i = 0 or 1)

The pulse width of the external clock applied to the TRDCLK pin must be three or more cycles of the timer RD operating clock (refer to **Table 18.1 Timer RD Operating Clocks**).

When selecting fHOCO or fHOCO-F as the count source, set the FRA00 bit in the FRA0 register to 1 (high-speed on-chip oscillator on) before setting bits TCK2 to TCK0 in the TRDCRi register (i = 0 or 1) to 110b (fHOCO) or 111b (fHOCO-F).

18.3.1.2 Buffer Operation

The TRDGRCi register can be used as the buffer register for the TRDGRAi register, and the TRDGRDi register can be used as the buffer register for the TRDGRBi register by setting bits BFCi and BFDi in the TRDMR register.

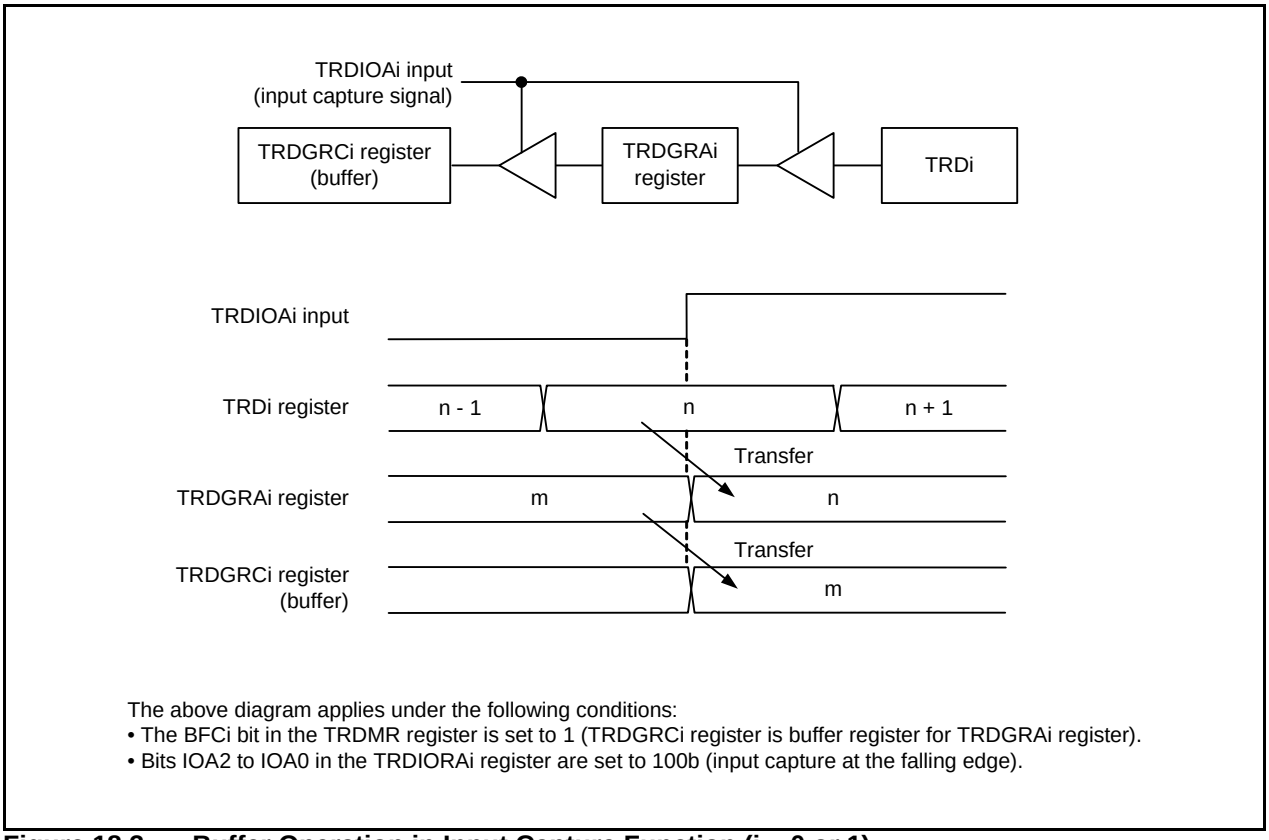
- TRDGRAi buffer register: TRDGRCi register
- TRDGRBi buffer register: TRDGRDi register

Buffer operation depends on the mode. Table 18.11 lists the Buffer Operation in Each Mode.

Table 18.11 Buffer Operation in Each Mode

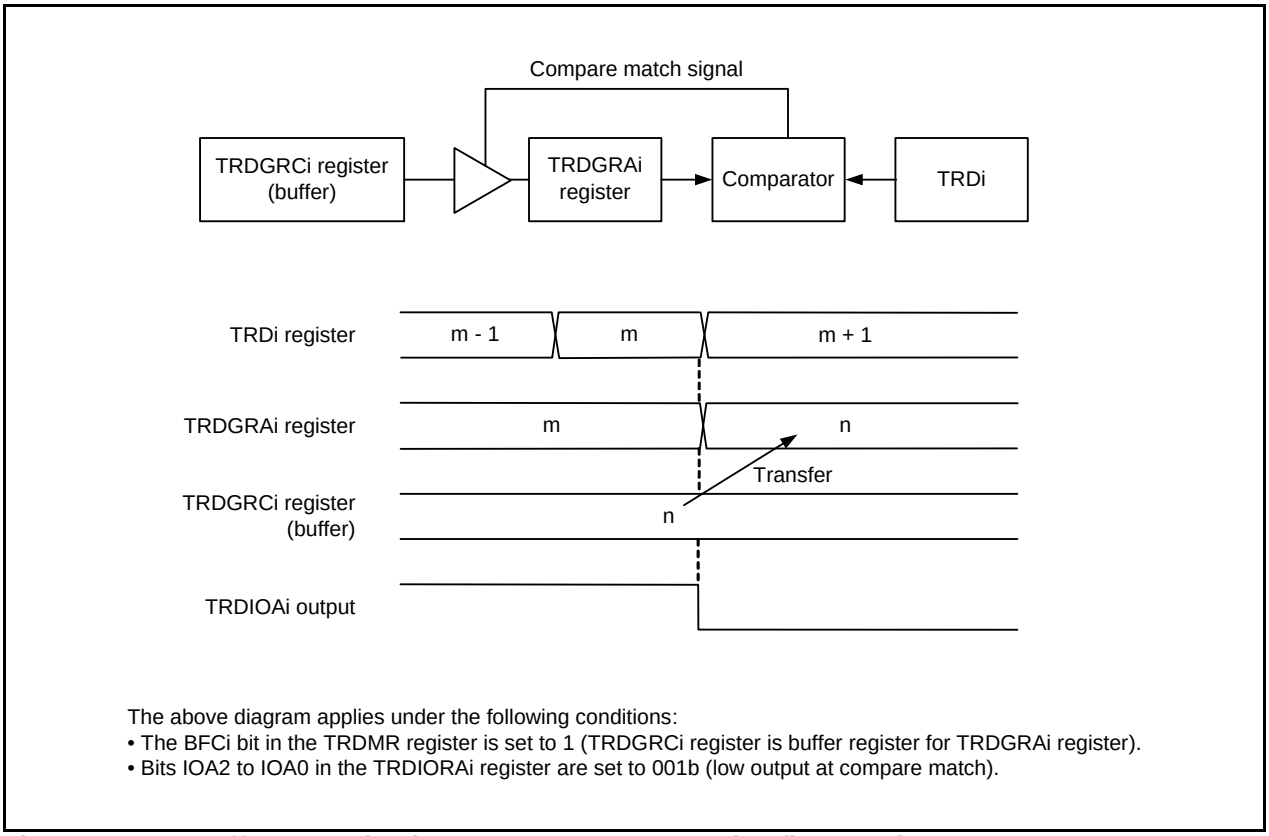
Function and Mode	Transfer Timing	Transfer Register
Input capture function	Input capture signal input	Transfer content of TRDGRAi (TRDGRBi) register to buffer register
Output compare function PWM mode	Compare match with TRDi register and TRDGRAi (TRDGRBi) register	Transfer content of buffer register to TRDGRAi (TRDGRBi) register
Reset synchronous PWM mode	Compare match withTRD0 register and TRDGRA0 register	Transfer content of buffer register to TRDGRAi (TRDGRBi) register
Complementary PWM mode	Compare match with TRD0 register and TRDGRA0 register TRD1 register underflow	Transfer content of buffer register to registers TRDGRB0, TRDGRA1, and TRDGRB1
PWM3 mode	Compare match with TRD0 register and TRDGRA0 register	Transfer content of buffer register to TRDGRAi (TRDGRBi) register

i = 0 or 1



The above diagram applies under the following conditions:
- The BFCi bit in the TRDMR register is set to 1 (TRDGRCi register is buffer register for TRDGRAi register).
- Bits IOA2 to IOA0 in the TRDIORAi register are set to 100b (input capture at the falling edge).

Figure 18.3 Buffer Operation in Input Capture Function (i = 0 or 1)



The above diagram applies under the following conditions:
- The BFCi bit in the TRDMR register is set to 1 (TRDGRCi register is buffer register for TRDGRAi register).
- Bits IOA2 to IOA0 in the TRDIORAi register are set to 001b (low output at compare match).

Figure 18.4 Buffer Operation in Output Compare Function (i = 0 or 1)

Perform the following for the timer mode (input capture and output compare functions).
When using the TRDGRCi (i = 0 or 1) register as the buffer register for the TRDGRAi register
• Set the IOC3 bit in the TRDIORCi register to 1 (general register or buffer register).
• Set the IOC2 bit in the TRDIORCi register to the same value as the IOA2 bit in the TRDIORAi register.

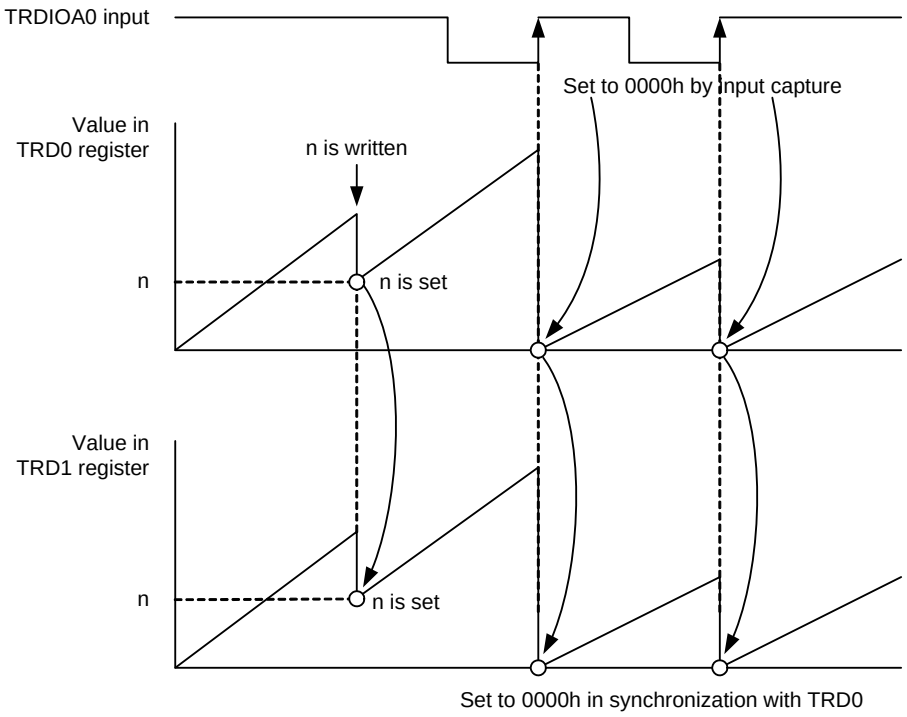
When using the TRDGRDi register as the buffer register for the TRDGRBi register
• Set the IOD3 bit in the TRDIORCi register to 1 (general register or buffer register).
• Set the IOD2 bit in the TRDIORCi register to the same value as the IOB2 bit in the TRDIORAi register.

In the input capture function, when the TRDGRCi register or TRDGRDi register is used as a buffer register, the IMFC bit or IMFD bit in the TRDSRi register is set to 1 at the input edge of the TRDIOCi pin or TRDIODi pin. When also using registers TRDGRCi and TRDGRDi as buffer registers for the output compare function, PWM mode, reset synchronous PWM mode, complementary PWM mode, and PWM3 mode, bits IMFC and IMFD in the TRDSRi register are set to 1 by a compare match with the TRDi register.

18.3.1.3 Synchronous Operation

The TRD1 register is synchronized with the TRD0 register.

- Synchronous preset
  When the SYNC bit in the TRDMR register is set to 1 (synchronous operation), the data is written to both the TRD0 and TRD1 registers after writing to the TRDi register.
- Synchronous clear
  When the SYNC bit is 1 and bits CCLR2 to CCLR0 in the TRDCR0 register are 011b (synchronous clear), the TRD0 register is set to 0000h at the same time as the TRD1 register is set to 0000h.
  Also, when the SYNC bit is 1 and bits CCLR2 to CCLR0 are 011b (synchronous clear), the TRD1 register is set to 0000h at the same time as the TRD0 register is set to 0000h.



The above diagram applies under the following conditions:

- The SYNC bit in the TRDMR register is set to 1 (synchronous operation).
- Bits CCLR2 to CCLR0 in the TRDCR0 register are set to 001b (TRD0 is set to 0000h by input capture).
  Bits CCLR2 to CCLR0 in the TRDCR1 register are set to 011b (TRD1 is set to 0000h in synchronization with TRD0).
- Bits IOA2 to IOA0 in the TRDIORA0 register are set to 100b.
- Bits CMD1 to CMD0 in the TRDFCR register are set to 00b.
  The PWM 3 bit in the TRDFCR register is set to 1.

} (Input capture at the rising edge of TRDIOA0 input)

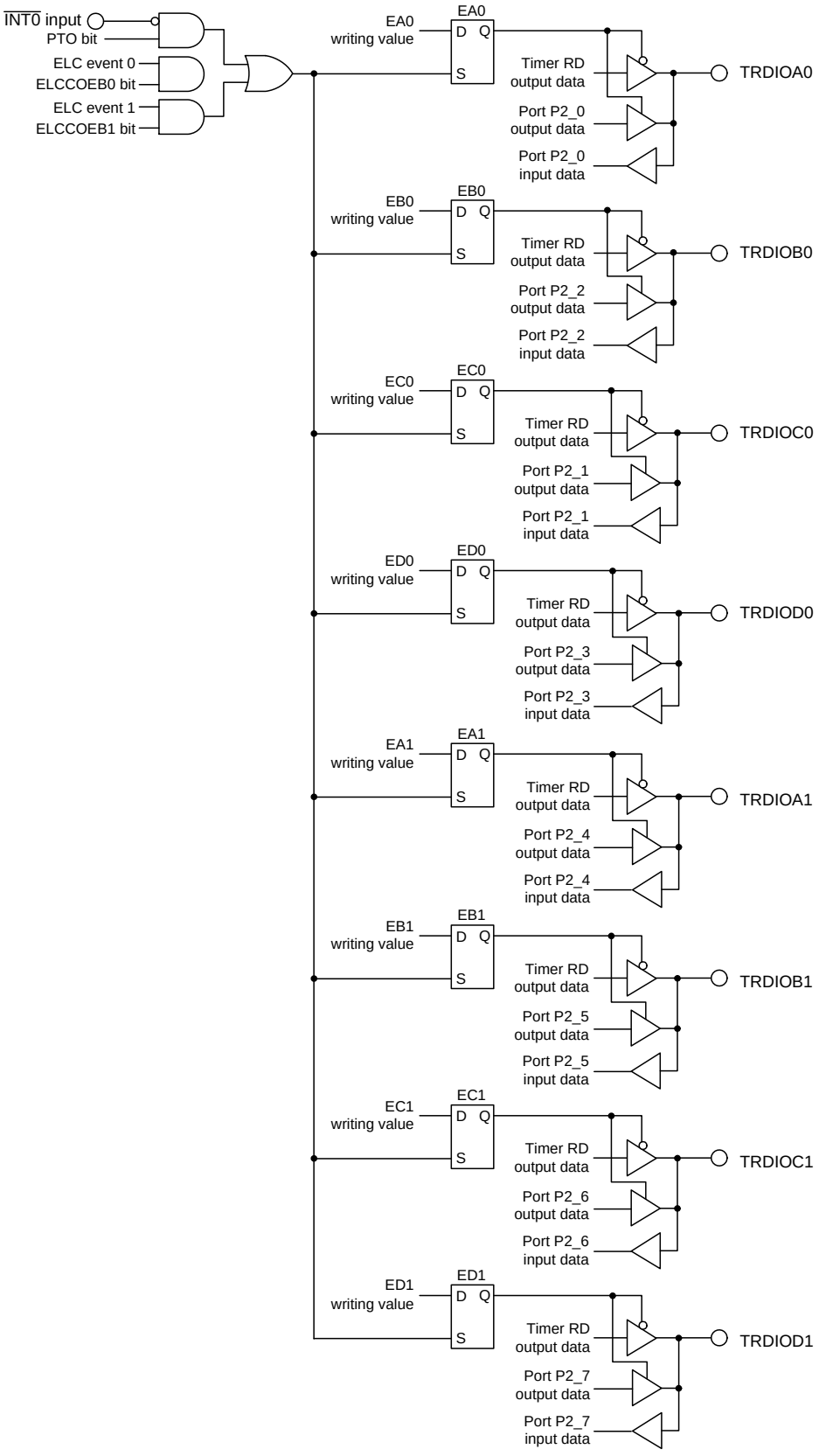
Figure 18.5 Synchronous Operation

18.3.1.4 Pulse Output Forced Cutoff

In the output compare function, PWM mode, reset synchronous PWM mode, complementary PWM mode, and PWM3 mode, the TRDIOji output pin (i = 0 or 1, j = A, B, C, or D) can be forcibly set to a programmable I/O port by the $\overline{\text{INT0}}$ pin input, and pulse output can be cut off.
The pins used for output in these functions or modes can function as the output pin of timer RD when the corresponding bit in the TRDOER1 register is set to 0 (timer RD output disabled). When the PTO bit in the TRDOER2 register to 1 (pulse output forced cutoff signal input $\overline{\text{INT0}}$ enabled), all bits in the TRDOER1 register are set to 1 (timer RD output disabled, TRDIOji output pin functions as a programmable I/O port) after a low level is applied to the $\overline{\text{INT0}}$ pin. The TRDIOji output pin is set to a programmable I/O port after a low level is applied to the $\overline{\text{INT0}}$ pin and waiting for one to two cycles of the timer RD operating clock (refer to **Table 18.1 Timer RD Operating Clocks**).

Make the following settings to use this function:
- Set the pin state (high impedance, low output, or high output) to pulse output forced cutoff using registers PORT2 and PD2.
- Set the INT0EN bit in the INTEN register to 1 ($\overline{\text{INT0}}$ input enabled) and the INT0PL bit to 0 (one edge).
- Set the PD4_5 bit in the PD4 register to 0 (input mode).
- Select the $\overline{\text{INT0}}$ digital filter using bits INT0F0 and INT0F1 in the INTF register.
- Set the PTO bit in the TRDOER2 register to 1 (pulse output forced cutoff signal input $\overline{\text{INT0}}$ enabled).

The IR bit in the INT0IC register is set to 1 (interrupt requested) in accordance with the setting of the INT0PL bit in the INTEN register and a change in the $\overline{\text{INT0}}$ pin input (refer to **11.9 Notes on Interrupts**).
For details on interrupts, refer to **11. Interrupts**.



PTO: Bit in TRDOER2 register
EA0, EB0, EC0, ED0, EA1, EB1, EC1, ED1: Bits in TRDOER1 register

Figure 18.6 Pulse Output Forced Cutoff

18.3.1.5 ELC Event Input

Timer RD performs two operations by ELC event input.

(1) Event input capture operation D0/D1
Input capture operation is performed by ELC event input.
The interrupt status flag (IMFD0/IMFD1) is set to 1 at that time.
To use this function, select the input capture function in timer mode and set the ELCICE0/ELCICE1 bit in the TRDELCCR register to 1.
This function is disabled in any other modes (for the output compare function in timer mode, in PWM mode, reset synchronous PWM mode, complementary PWM mode, and PWM3 mode).

Setting procedure
(1) Set ELC event input for timer RD.
(2) Set bits ELCICE0 to ELCICE0 in the TRDELCCR register for timer RD to 1.

(2) Pulse output forced cutoff operation
The pulse output is forcibly cut off by ELC event input.
This function can be used by setting ELCOBE0/ELCOBE1 = 1 in pulse output modes (for the output compare function in timer mode, in PWM mode, reset synchronous PWM mode, complementary PWM mode, and PWM3 mode).
This function is disabled for the input capture function in timer mode.

Setting procedure
(1) Set ELC event input for timer RD.
(2) Set bits ELCICE0 to ELCICE0 in the TRDELCCR register for timer RD to 1.

18.3.1.6 A/D Trigger Generation

In the output compare function, PWM mode, reset synchronous PWM mode, PWM3 mode, and complementary PWM mode, a conversion start trigger of the A/D conversion can be generated.

- In the output compare function, PWM mode, reset synchronous PWM mode, and PWM3 mode
  A compare match signal between registers TRDi (i = 0 or 1) and TRDGRji (j = A, B, C, or D) can be used as the conversion start trigger for the A/D converter.
  The TRDADCR register is used to select which compare match is used.
- In complementary PWM mode
  A compare match between registers TRD0 and TRDGRA0 or underflow of TRD1 can be used as the conversion start trigger for the A/D converter. This should be set using bits ADEG and ADTRG in the TRDFCR register and the TRDADCR register. Also, set bits ADCAP1 and ADCAP0 in the ADMOD register to 01b (start by timer RD).

18.3.1.7 Setting External Pins

When timer RD is used, make the following settings.

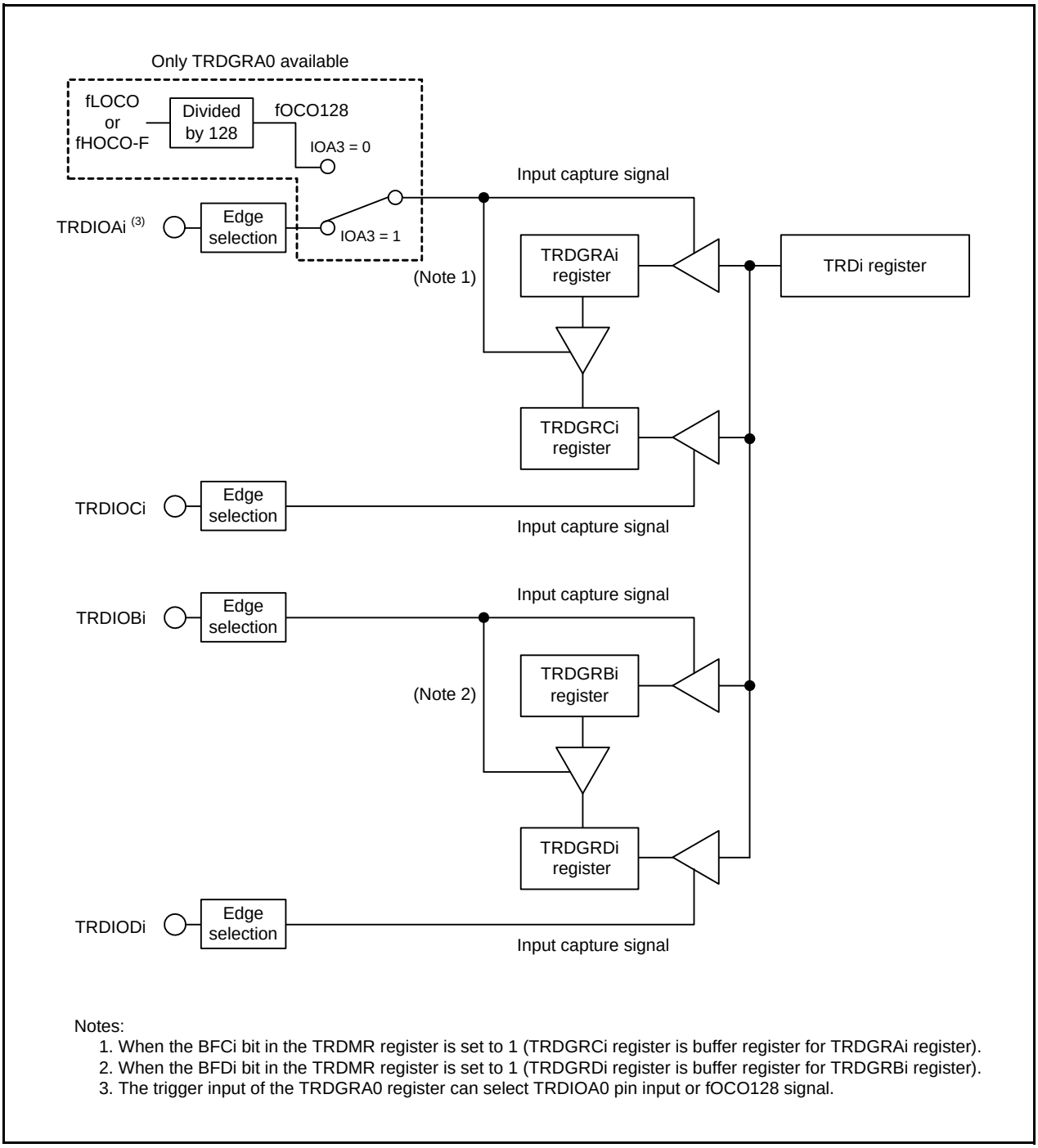
- To use the TRDIOA0 pin: Set bits TRDIOA0_0SEL1 and TRDIOA0_0SEL0 in the TRD_0SR0 register to 01b or 10b.
- To use the TRDIOB0 pin: Set bits TRDIOB0_0SEL1 and TRDIOB0_0SEL0 in the TRD_0SR0 register to 01b, 10b, or 11b.
- To use the TRDIOC0 pin: Set bits TRDIOC0_0SEL1 and TRDIOC0_0SEL0 in the TRD_0SR0 register to 01b, 10b, or 11b.
- To use the TRDIOD0 pin: Set bits TRDIOD0_0SEL1 and TRDIOD0_0SEL0 in the TRD_0SR0 register to 01b or 10b.
- To use the TRDIOA1 pin: Set bits TRDIOA1_0SEL1 and TRDIOA1_0SEL0 in the TRD_0SR1 register to 01b or 10b.
- To use the TRDIOB1 pin: Set bits TRDIOB1_0SEL1 and TRDIOB1_0SEL0 in the TRD_0SR1 register to 01b or 10b.
- To use the TRDIOC1 pin: Set bits TRDIOC1_0SEL1 and TRDIOC1_0SEL0 in the TRD_0SR1 register to 01b, 10b, or 11b.
- To use the TRDIOD1 pin: Set bits TRDIOD1_0SEL1 and TRDIOD1_0SEL0 in the TRD_0SR1 register to 01b, 10b, or 11b.

18.3.2 Input Capture Function

The input capture function can measure the width or period of an external signal. The content of the TRDi register (counter) is transferred to the TRDGRji register when triggered by the TRDIOji pin (i = 0 or 1, j = A, B, C, or D) external signal (input capture). Since this function uses a combination of the TRDIOji pin and TRDGRji register, the input capture function, or any other mode or function, can be selected for each individual pin.

The TRDGRA0 register can also select fOCO128 as the input-capture trigger input.

Figure 18.7 shows the Input Capture Function Block Diagram (i = 0 or 1), Table 18.12 lists the Input Capture Function Specifications, and Figure 18.8 shows an Input Capture Function Operation Example (i = 0 or 1).



Notes:
1. When the BFCi bit in the TRDMR register is set to 1 (TRDGRCi register is buffer register for TRDGRAi register).
2. When the BFDi bit in the TRDMR register is set to 1 (TRDGRDi register is buffer register for TRDGRBi register).
3. The trigger input of the TRDGRA0 register can select TRDIOA0 pin input or fOCO128 signal.

Figure 18.7 Input Capture Function Block Diagram (i = 0 or 1)

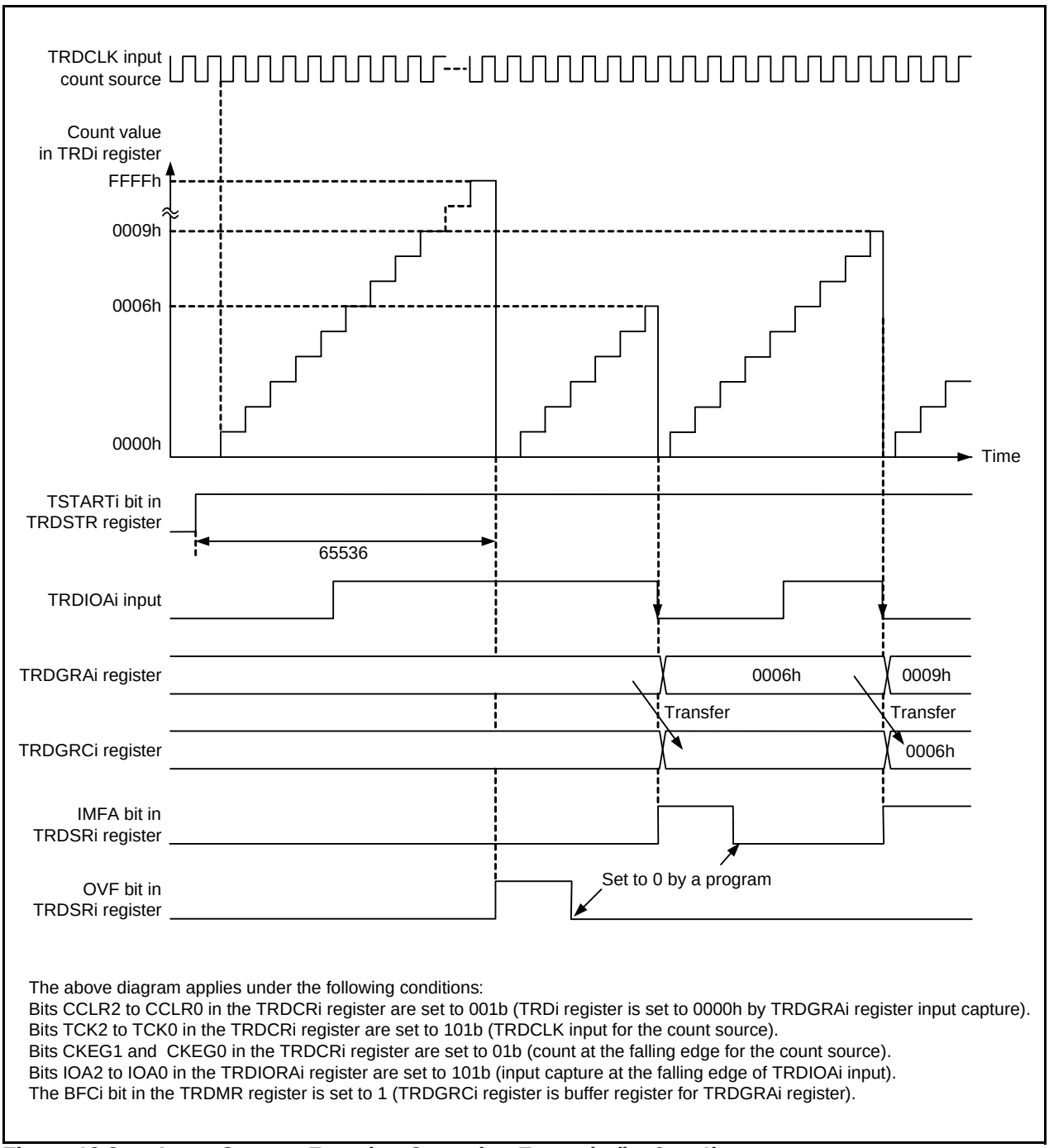
Table 18.12 Input Capture Function Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fHOCO, fHOCO-F External signal input to the TRDCLK pin (active edge selected by a program)
Count operations	Increment
Count period	When bits CCLR2 to CCLR0 in the TRDCRi register are set to 000b (free-running operation). 1/fk × 65536 fk: Frequency of count source
Count start condition	1 (count starts) is written to the TSTARTi bit in the TRDSTR register.
Count stop condition	0 (count stops) is written to the TSTARTi bit in the TRDSTR register when the CSELi bit in the TRDSTR register is set to 1.
Interrupt request generation timing	• Input capture (active edge of TRDIOji input or edge of fOCO128 signal) • TRDi register overflow
TRDIOA0 pin function	Programmable I/O port, input-capture input, or TRDCLK (external clock) input
TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1 to TRDIOD1 pin function	Programmable I/O port or input-capture input (selectable for each pin)
$\overline{\text{INT0}}$ pin function	Not used (programmable I/O port or $\overline{\text{INT0}}$ interrupt input)
Read from timer	The count value can be read by reading the TRDi register.
Write to timer	• When the SYNC bit in the TRDMR register is 0 (timer RD0 and timer RD1 operate independently). Data can be written to the TRDi register. • When the SYNC bit in the TRDMR register is 1 (timer RD0 and timer RD1 operate synchronously). Data can be written to both the TRD0 and TRD1 registers by writing to the TRDi register.
Selectable functions	• Input-capture input pin selection Either one pin or multiple pins of TRDIOAi, TRDIOBi, TRDIOCi, and TRDIODi. • Input-capture input active edge selection Rising edge, falling edge, or both rising and falling edges • Timing for setting the TRDi register to 0000h At overflow or input capture • Buffer operation (refer to **18.3.1.2 Buffer Operation**) • Synchronous operation (refer to **18.3.1.3 Synchronous Operation**) • Digital filter The TRDIOji input is sampled, and when the sampled input level matches three times, that level is determined. • Input-capture trigger selection fOCO128 can be selected as the input-capture trigger input for the TRDGRA0 register. • Input capture operation by event input from the event link controller (ELC).

i = 0 or 1, j = A, B, C, or D

18.3.2.1 Operation Example

When bits CCLR0 to CCLR2 in the TRDCRi register (i = 0 or 1) are set, the counter value of timer RDi is reset by an input capture/compare match. Figure 18.8 shows an operation example with bits CCLR2 to CCLR0 set to 001b. If the input capture operation has been set to clear the count during operation and is performed when the timer count value is FFFFh, depending on the timing between the count source and input capture operation interrupt flags bits IMFA to IMFD and OVF in the TRDSRi register may be set to 1 simultaneously.



The above diagram applies under the following conditions:
Bits CCLR2 to CCLR0 in the TRDCRi register are set to 001b (TRDi register is set to 0000h by TRDGRAi register input capture).
Bits TCK2 to TCK0 in the TRDCRi register are set to 101b (TRDCLK input for the count source).
Bits CKEG1 and CKEG0 in the TRDCRi register are set to 01b (count at the falling edge for the count source).
Bits IOA2 to IOA0 in the TRDIORAi register are set to 101b (input capture at the falling edge of TRDIOAi input).
The BFCi bit in the TRDMR register is set to 1 (TRDGRCi register is buffer register for TRDGRAi register).

Figure 18.8 Input Capture Function Operation Example (i = 0 or 1)

18.3.2.2 Digital Filter

The TRDIOji input (i = 0 or 1, j = A, B, C, or D) is sampled, and when the sampled input level matches three times, that level is determined. Select the digital filter function and sampling clock using the TRDDFi register. Figure 18.9 shows the Digital Filter Block Diagram (i = 0 or 1, j = A, B, C, or D).

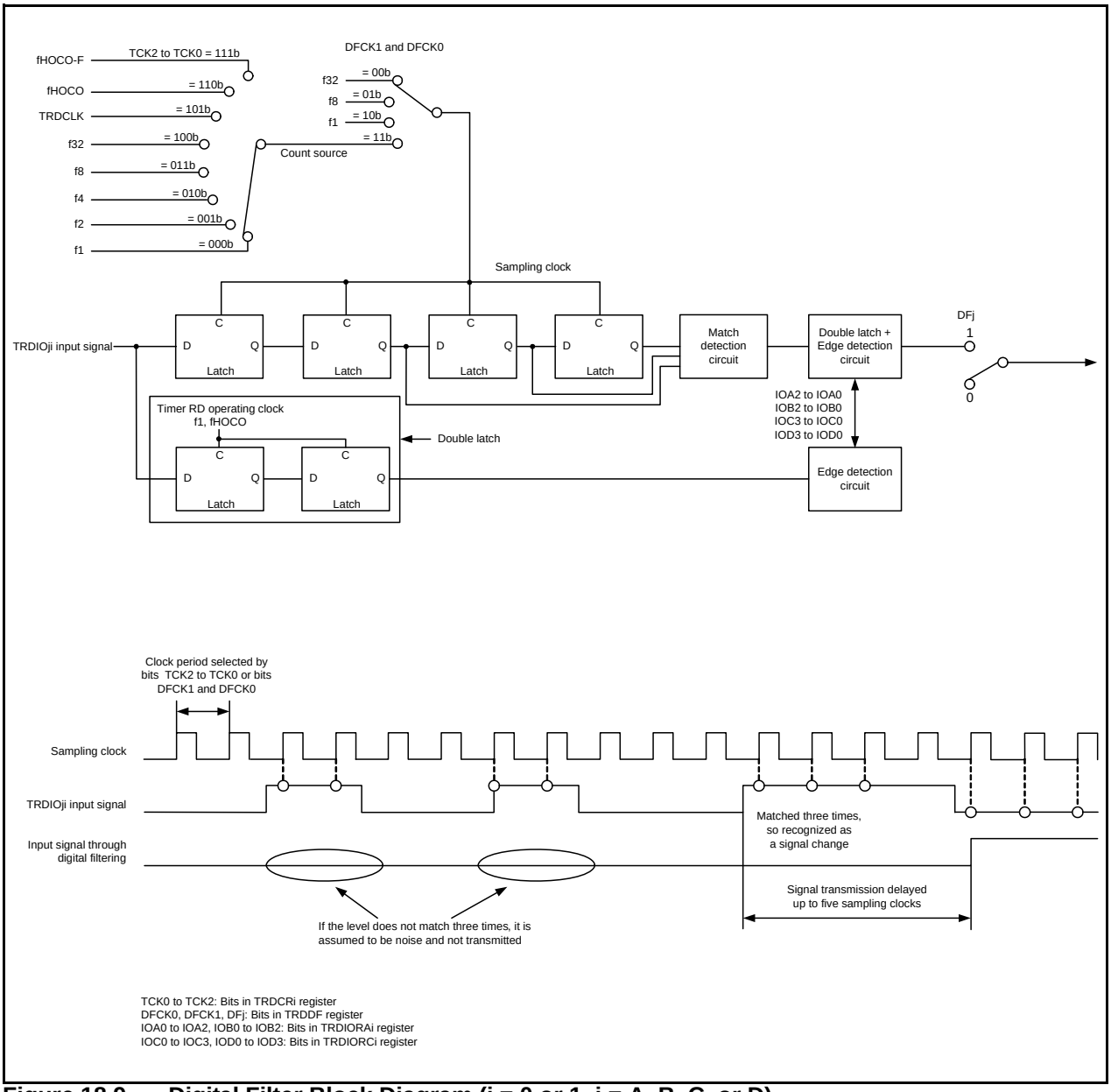


Figure 18.9 Digital Filter Block Diagram (i = 0 or 1, j = A, B, C, or D)

18.3.3 Output Compare Function

This function detects matches (compare match) between the content of the TRDGRji register (j = A, B, C, or D) and the content of the TRDi register (counter) (i = 0 or 1). When the contents match, an arbitrary level is output from the TRDIOji pin. Since this function is enabled with a combination of the TRDIOji pin and TRDGRji register, the output compare function, or any other mode or function, can be selected for each individual pin. Figure 18.10 shows the Output Compare Function Block Diagram, Table 18.13 lists the Output Compare Function Specifications, and Figure 18.11 shows an Output Compare Function Operation Example (i = 0 or 1).

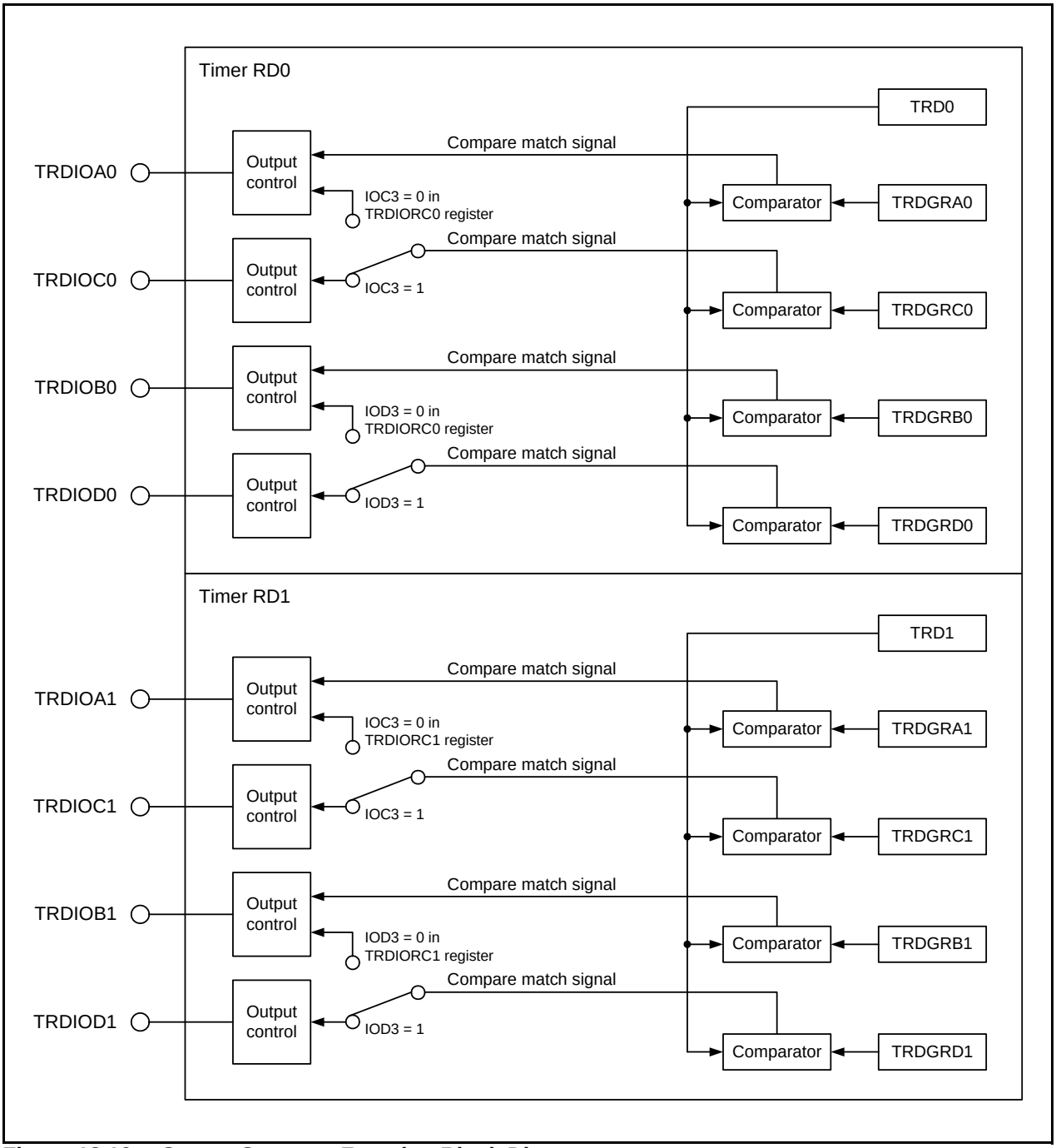


Figure 18.10 Output Compare Function Block Diagram

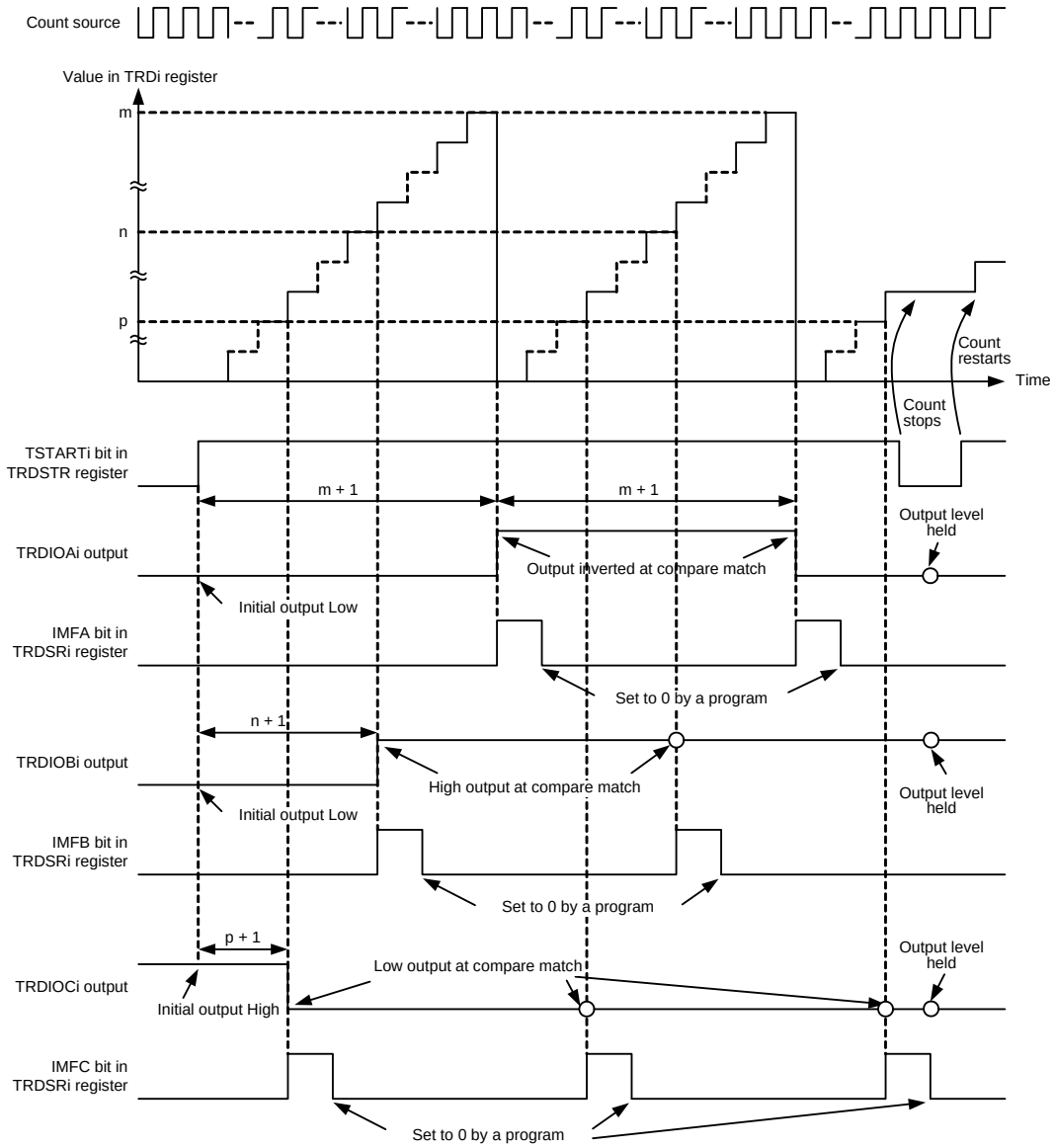
Table 18.13 Output Compare Function Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fHOCO, fHOCO-F External signal input to the TRDCLK pin (active edge selected by a program)
Count operations	Increment
Count period	• When bits CCLR2 to CCLR0 in the TRDCRi register are set to 000b (free-running operation). 1/fk × 65536 fk: Frequency of count source • When bits CCLR1 and CCLR0 in the TRDCRi register are set to 01b or 10b (TRDi register is set to 0000h at compare match with TRDGRji register). 1/fk × (n + 1) n: Value set in the TRDGRji register
Waveform output timing	Compare match (contents of registers TRDi and TRDGRji match)
Count start condition	1 (count starts) is written to the TSTARTi bit in the TRDSTR register.
Count stop conditions	• 0 (count stops) is written to the TSTARTi bit in the TRDSTR register when the CSELi bit in the TRDSTR register is set to 1. The output-compare output pin retains the output level before the count stops. • When the CSELi bit in the TRDSTR register is set to 0, the count stops at a compare match with the TRDGRAi register. The output-compare output pin retains the level after the output change due to the compare match.
Interrupt request generation timing	• Compare match (contents of registers TRDi and TRDGRji match) • TRDi register overflow
TRDIOA0 pin function	Programmable I/O port, output-compare output, or TRDCLK (external clock) input
TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1 to TRDIOD1 pin function	Programmable I/O port or output-compare output (selectable for each pin)
$\overline{\text{INT0}}$ pin function	Pulse output forced cutoff signal input (programmable I/O port or $\overline{\text{INT0}}$ interrupt input)
Read from timer	The count value can be read by reading the TRDi register.
Write to timer	• When the SYNC bit in the TRDMR register is set to 0 (timer RD0 and timer RD1 operate independently). Data can be written to the TRDi register. • When the SYNC bit in the TRDMR register is set to 1 (timer RD0 and timer RD1 operate synchronously). Data can be written to both the TRD0 and TRD1 registers by writing to the TRDi register.
Selectable functions	• Output-compare output pin selection Either one pin or multiple pins of TRDIOAi, TRDIOBi, TRDIOCi, and TRDIODi. • Output level selection at compare match Low output, high output, or inverted output level • Initial output level selection The level can be set for the period from the count start to the compare match. • Timing for setting the TRDi register to 0000h Overflow or compare match in the TRDGRAi register • Buffer operation (refer to **18.3.1.2 Buffer Operation**) • Synchronous operation (refer to **18.3.1.3 Synchronous Operation**) • Changing output pins for registers TRDGRCi and TRDGRDi The TRDGRCi register can be used as output control of the TRDIOAi pin and the TRDGRDi register can be used as output control of the TRDIOBi pin. • Pulse output forced cutoff signal input (refer to **18.3.1.4 Pulse Output Forced Cutoff**) • Timer RD can be used as the internal timer without output. • A/D trigger generation

i = 0 or 1, j = A, B, C, or D

18.3.3.1 Operation Example

When bits CCLR0 to CCLR2 in the TRDCRi register (i = 0 or 1) are set, the counter value of timer RDi is reset by an input capture/compare match. If the expected compare value is FFFFh at this time, FFFFh changes to 0000h, which is the same as an overflow operation, and the overflow flag is set to 1.



The above diagram applies under the following conditions:
The CSELi bit in the TRDSTR register is set to 1 (TRDi is not stopped by compare match).
Bits BFCi and BFDi in the TRDMR register are set to 0 (TRDGRCi and TRDGRDi do not operate as buffers).
Bits EAi, EBi, and ECi in the TRDOER1 register are set to 0 (TRDIOAi, TRDIOBi and TRDIOCi output enabled).
Bits CCLR2 to CCLR0 in the TRDCRi register are set to 001b (TRDi is set to 000h by compare match with TRDGRAi).
Bits TOAi and TOBi in the TRDOCR register is set to 0 (initial output Low until compare match), the TOCi bit is set to 1 (initial output High until compare match).
Bits IOA2 to IOA0 in the TRDIORAi register are set to 011b (TRDIOAi output inverted at TRDGRAi compare match).
Bits IOB2 to IOB0 in the TRDIORAi register are set to 010b (TRDIOBi high output at TRDGRBi compare match).
Bits IOC3 to IOC0 in the TRDIORCi register are set to 1001b (TRDIOCi low output at TRDGRCi register compare match).
Bits IOD3 to IOD0 in the TRDIORCi register are set to 1000b (TRDGRDi register does not control TRDIOBi pin output. Pin output by compare match is disabled).

Figure 18.11 Output Compare Function Operation Example (i = 0 or 1)

18.3.3.2 Changing Output Pins in Registers TRDGRCi (i = 0 or 1) and TRDGRDi

The TRDGRCi register can be used for output control of the TRDIOAi pin, and the TRDGRDi register can be used for output control of the TRDIOBi pin. Therefore, each pin output can be controlled as follows:

- TRDIOAi output is controlled by the values in registers TRDGRAi and TRDGRCi.
- TRDIOBi output is controlled by the values in registers TRDGRBi and TRDGRDi.

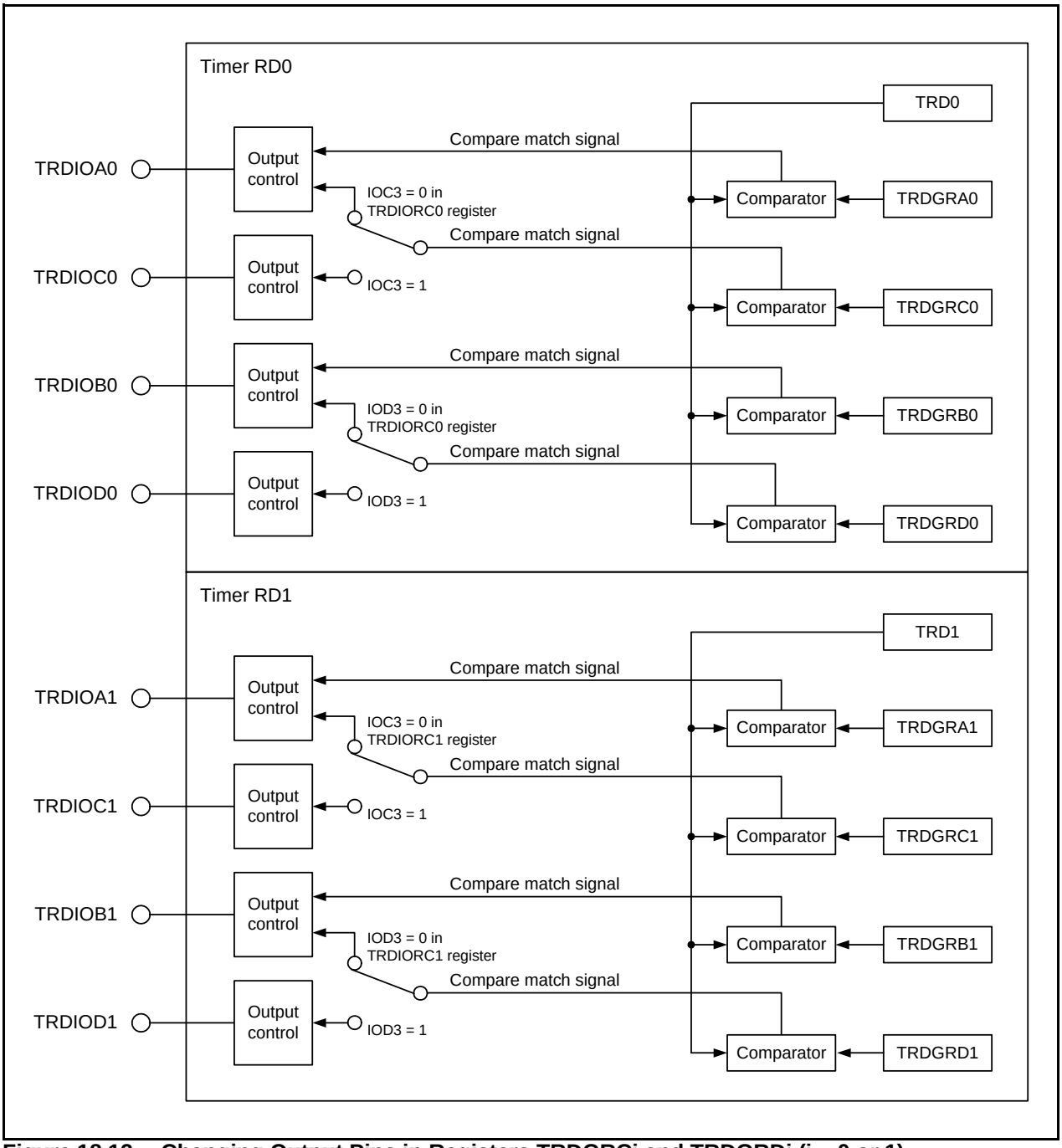
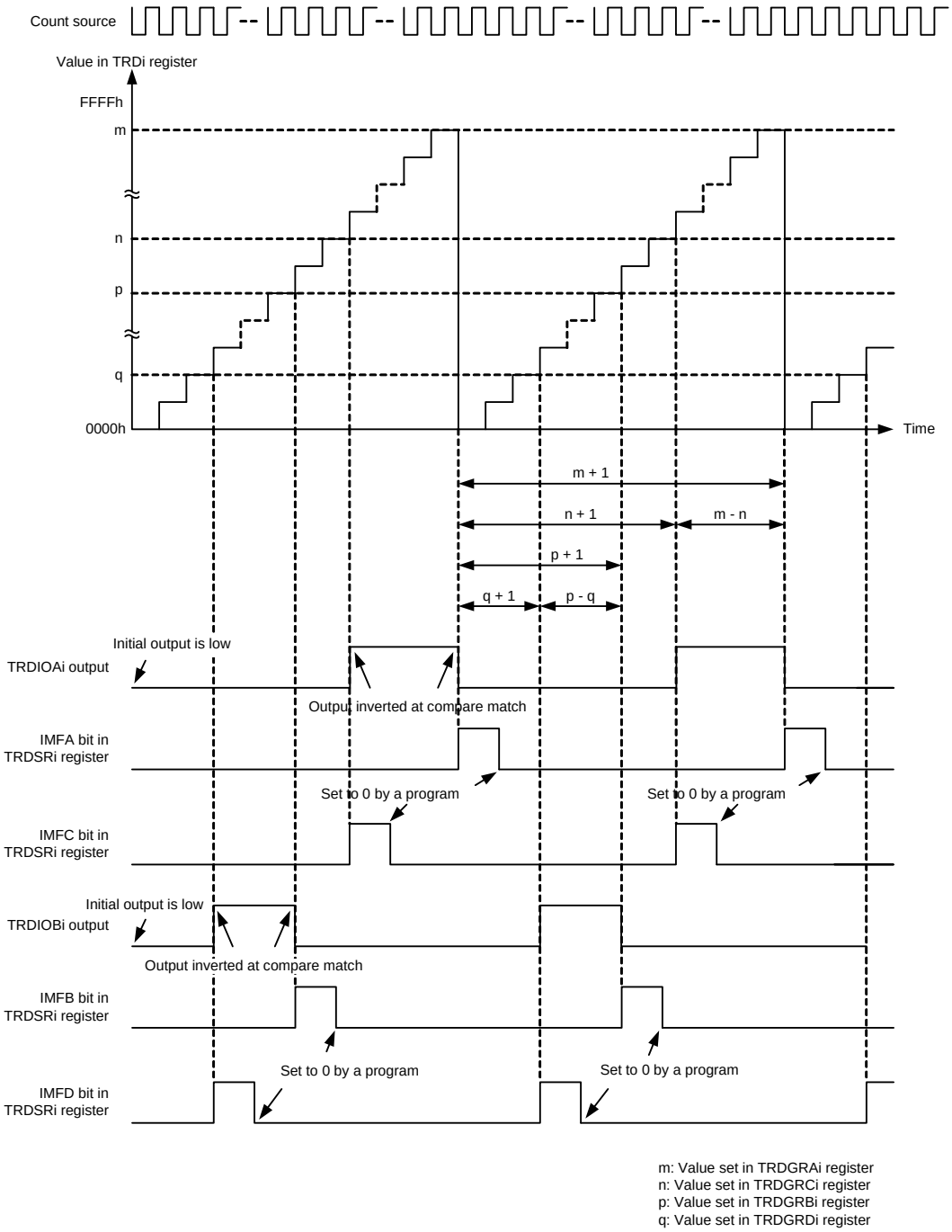


Figure 18.12 Changing Output Pins in Registers TRDGRCi and TRDGRDi (i = 0 or 1)

Change output pins in registers TRDGRCi and TRDGRDi as follows:

- Select 0 (TRDGRji register output pin is changed) using the IOj3 (j = C or D) bit in the TRDIORCi register.
- Set the BFji bit in the TRDMR register to 0 (general register).
- Set different values in registers TRDGRCi and TRDGRAi. Also, set different values in registers TRDGRDi and TRDGRBi.

Figure 18.13 shows an Operation Example When TRDGRCi Register is Used for Output Control of TRDIOAi Pin and TRDGRDi Register is Used for Output Control of TRDIOBi Pin.



The above diagram applies under the following conditions:
The CSELi bit in the TRDSTR register is set to 1 (TRDi register is not stopped by compare match).
Bits BFCi and BFDi in the TRDMR register are set to 0 (TRDGRCi and TRDGRDi do not operate as buffers).
Bits EAi and EBi in the TRDOER1 register are set to 0 (TRDIOAi and TRDIOBi output enabled).
Bits CCLR2 to CCLR0 in the TRDCRi register are set to 001b (TRDi is set to 0000h by compare match with TRDGRAi).
Bits TOAi and TOBi in the TRDOCR register are set to 0 (initial output is low until compare match).
Bits IOA2 to IOA0 in the TRDIORAi register are set to 011b (TRDIOAi output inverted at TRDGRAi compare match).
Bits IOB2 to IOB0 in the TRDIORAi register are set to 011b (TRDIOBi output inverted at TRDGRBi compare match).
Bits IOC3 to IOC0 in the TRDIORCi register are set to 0011b (TRDIOAi output inverted at TRDGRCi compare match).
Bits IOD3 to IOD0 in the TRDIORCi register are set to 0011b (TRDIOBi output inverted at TRDGRDi compare match).

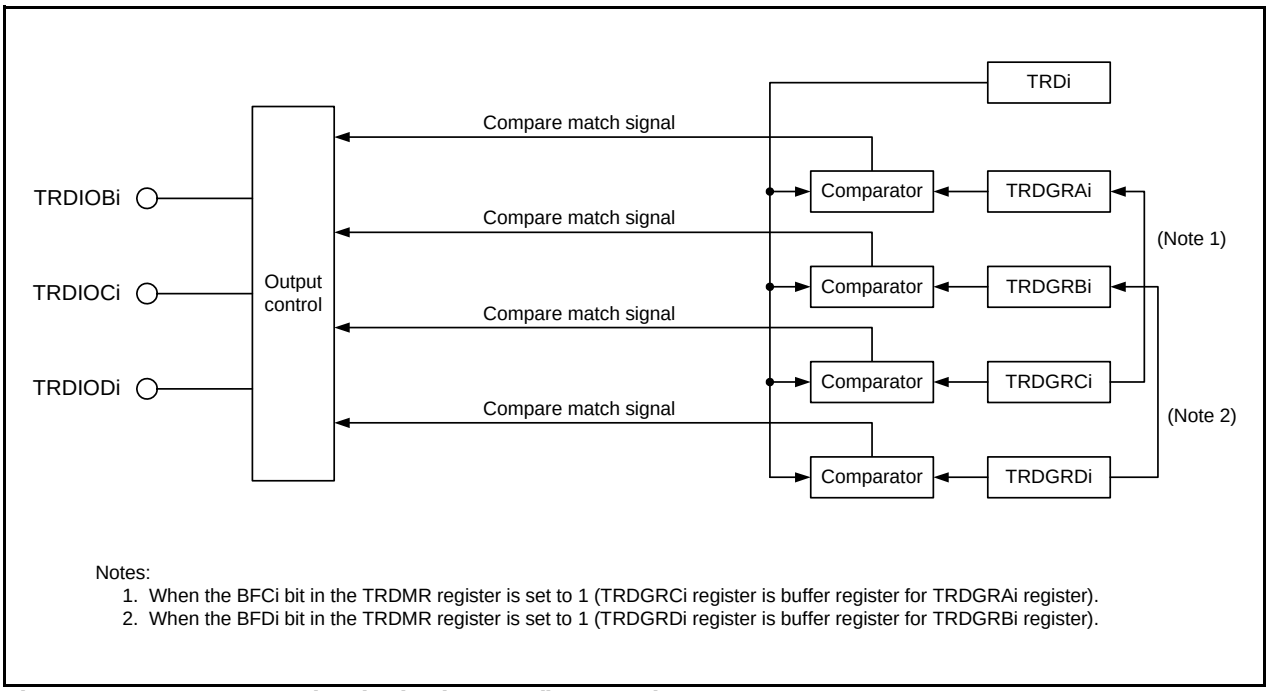
Figure 18.13 Operation Example When TRDGRCi Register is Used for Output Control of TRDIOAi Pin and TRDGRDi Register is Used for Output Control of TRDIOBi Pin

18.3.4 PWM Mode

In PWM mode, a PWM waveform is output. Up to three PWM waveforms with the same period can be output by timer RDi (i = 0 or 1). Also, up to six PWM waveforms with the same period can be output by synchronizing timer RD0 and timer RD1.

Since this mode functions using a combination of the TRDIOji pin (i = 0 or 1, j = B, C, or D) and TRDGRji register, PWM mode, or any other mode or function, can be selected for each individual pin. (However, since the TRDGRAi register is used when using any pin for PWM mode, the TRDGRAi register cannot be used for other modes.)

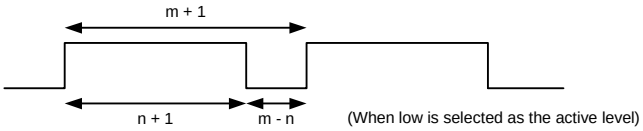
Figure 18.14 shows the PWM Mode Block Diagram (i = 0 or 1), Table 18.14 lists the PWM Mode Specifications, and Figures 18.15 and 18.16 show the Operations in PWM Mode.



Notes:
1. When the BFCi bit in the TRDMR register is set to 1 (TRDGRCi register is buffer register for TRDGRAi register).
2. When the BFDi bit in the TRDMR register is set to 1 (TRDGRDi register is buffer register for TRDGRBi register).

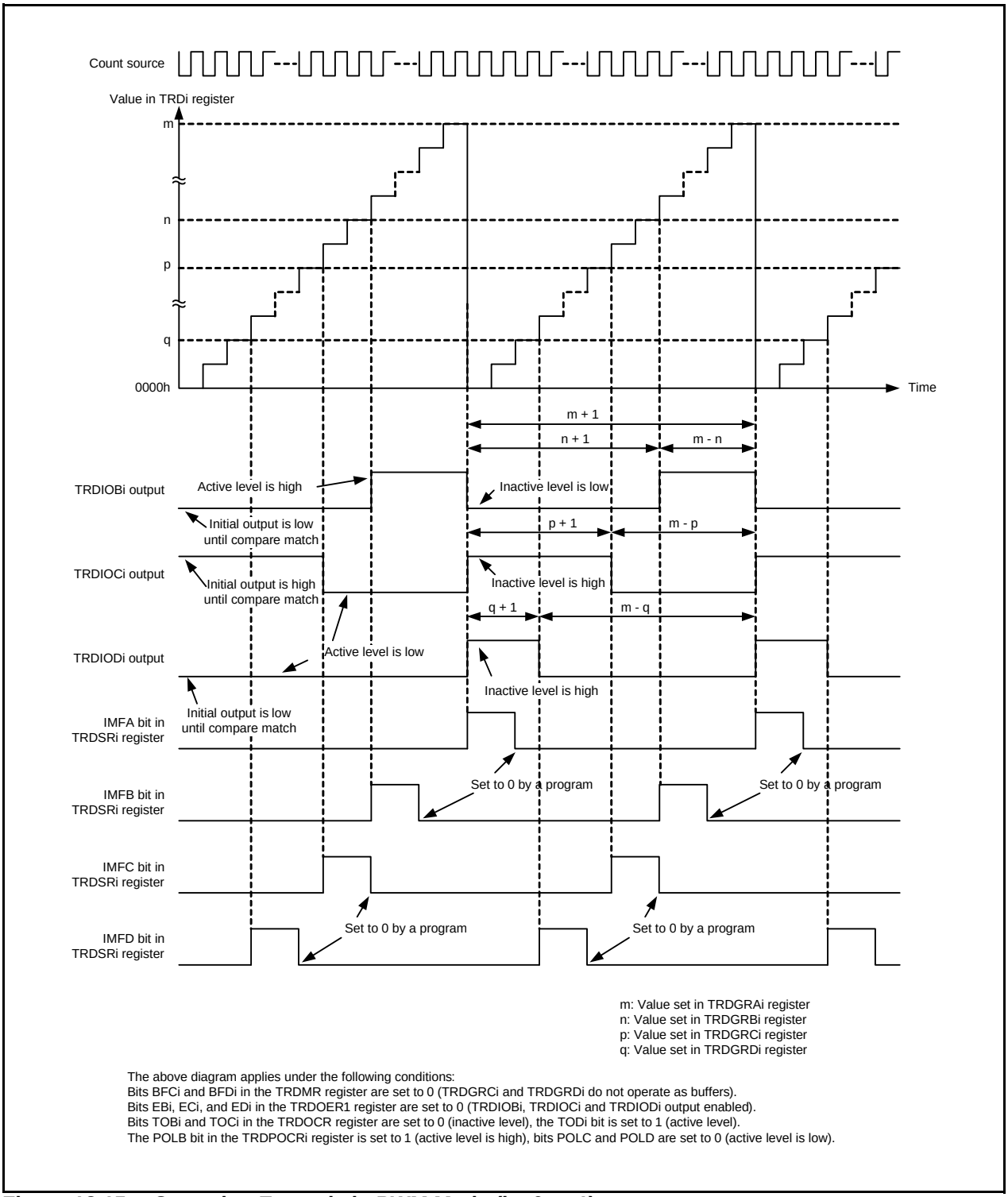
Figure 18.14 PWM Mode Block Diagram (i = 0 or 1)

Table 18.14 PWM Mode Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fHOCO, fHOCO-F External signal input to the TRDCLK pin (active edge selected by a program)
Count operations	Increment
PWM waveform	PWM period: 1/fk x (m + 1) Active level width: 1/fk x (m - n) Inactive level width: 1/fk x (n + 1) fk: Frequency of count source m: Value set in the TRDGRAi register n: Value set in the TRDGRji register 
Count start condition	1 (count starts) is written to the TSTARTi bit in the TRDSTR register.
Count stop conditions	• 0 (count stops) is written to the TSTARTi bit in the TRDSTR register when the CSELi bit in the TRDSTR register is set to 1. The PWM output pin retains the output level before the count stops. • When the CSELi bit in the TRDSTR register is set to 0, the count stops at a compare match with the TRDGRAi register. The PWM output pin retains the level after the output change due to the compare match.
Interrupt request generation timing	• Compare match (content of the TRDi register matches content of the TRDGRhi register) • TRDi register overflow
TRDIOA0 pin function	Programmable I/O port or TRDCLK (external clock) input
TRDIOA1 pin function	Programmable I/O port
TRDIOB0, TRDIOC0, TRDIOD0, TRDIOB1, TRDIOC1, TRDIOD1 pin function	Programmable I/O port or pulse output (selectable for each pin)
$\overline{\text{INT0}}$ pin function	Pulse output forced cutoff signal input (programmable I/O port or $\overline{\text{INT0}}$ interrupt input)
Read from timer	The count value can be read by reading the TRDi register.
Write to timer	The value can be written to the TRDi register.
Selectable functions	• One to three PWM output pins selectable with timer RDi Either one pin or multiple pins of TRDIOBi, TRDIOCi, and TRDIODi. • Active level selectable for each pin. • Initial output level selectable for each pin. • Synchronous operation (refer to **18.3.1.3 Synchronous Operation**) • Buffer operation (refer to **18.3.1.2 Buffer Operation**) • Pulse output forced cutoff signal input (refer to **18.3.1.4 Pulse Output Forced Cutoff**) • A/D trigger generation

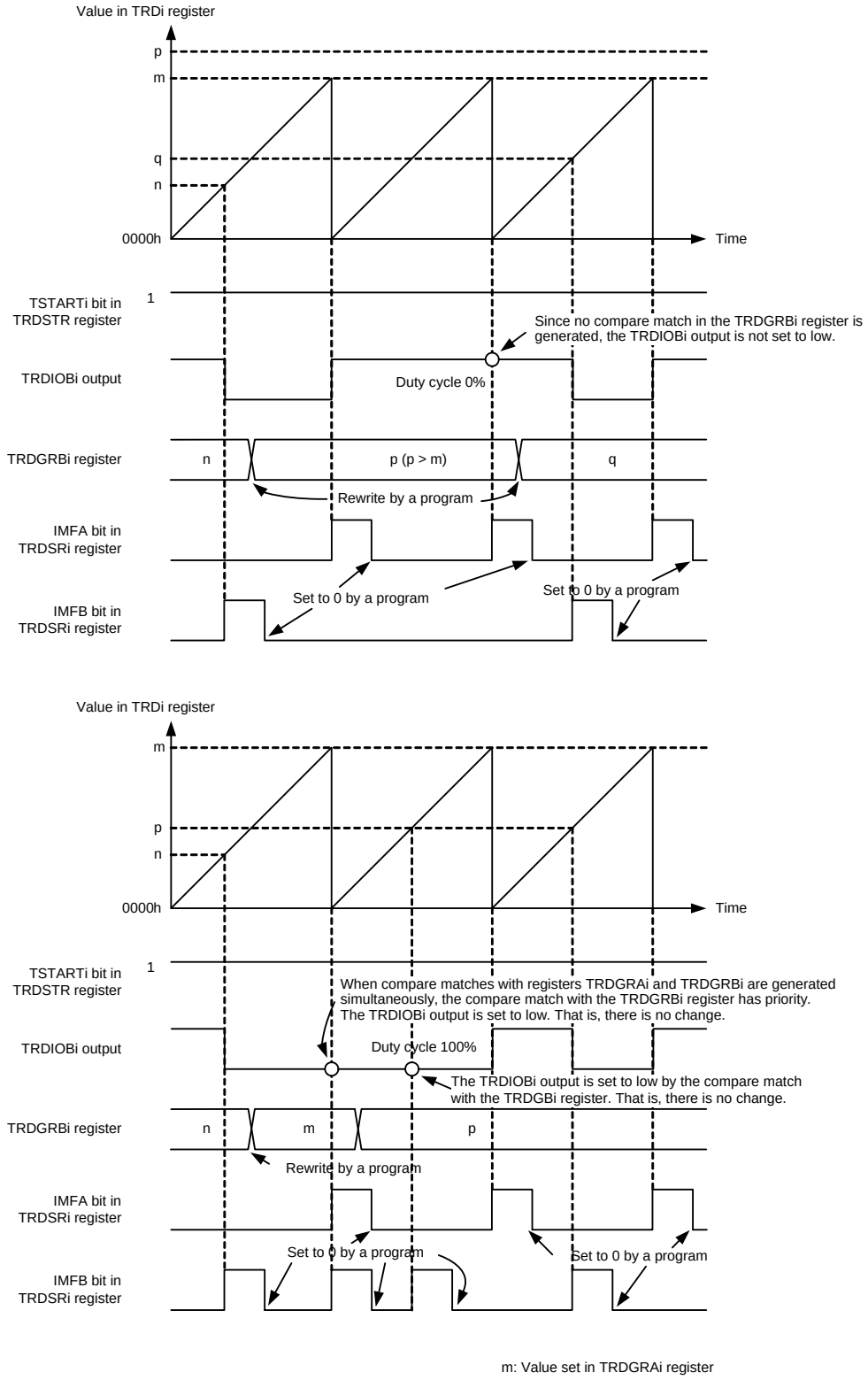
i = 0 or 1, j = B, C, or D, h = A, B, C, or D

18.3.4.1 Operation Example



The above diagram applies under the following conditions:
Bits BFCi and BFDi in the TRDMR register are set to 0 (TRDGRCi and TRDGRDi do not operate as buffers).
Bits EBi, ECi, and EDi in the TRDOER1 register are set to 0 (TRDIOBi, TRDIOCi and TRDIODi output enabled).
Bits TOBi and TOCi in the TRDOCR register are set to 0 (inactive level), the TODi bit is set to 1 (active level).
The POLB bit in the TRDPOCRi register is set to 1 (active level is high), bits POLC and POLD are set to 0 (active level is low).

Figure 18.15 Operation Example in PWM Mode (i = 0 or 1)



The above diagram applies under the following conditions:
The EBi bit in the TRDOER1 register is set to 0 (TRDIOBi output enabled).
The POLB bit in the TRDPOCRi register is set to 0 (active level is low).

Figure 18.16 Operation Example in PWM Mode (Duty Cycle 0%, Duty Cycle 100%) (i = 0 or 1)

18.3.5 Reset Synchronous PWM Mode

In this mode, three normal-phases and three counter-phases of the PWM waveform are output with the same period (three-phase, sawtooth wave modulation, and no dead time).
Figure 18.17 shows the Reset Synchronous PWM Mode Block Diagram and Table 18.15 lists the Reset Synchronous PWM Mode Specifications. Figure 18.18 shows an Operation Example in Reset Synchronous PWM Mode.
Refer to **Figure 18.16 Operation Example in PWM Mode (Duty Cycle 0%, Duty Cycle 100%) (i = 0 or 1)** for an operation example in PWM Mode with duty cycle 0% and duty cycle 100%.

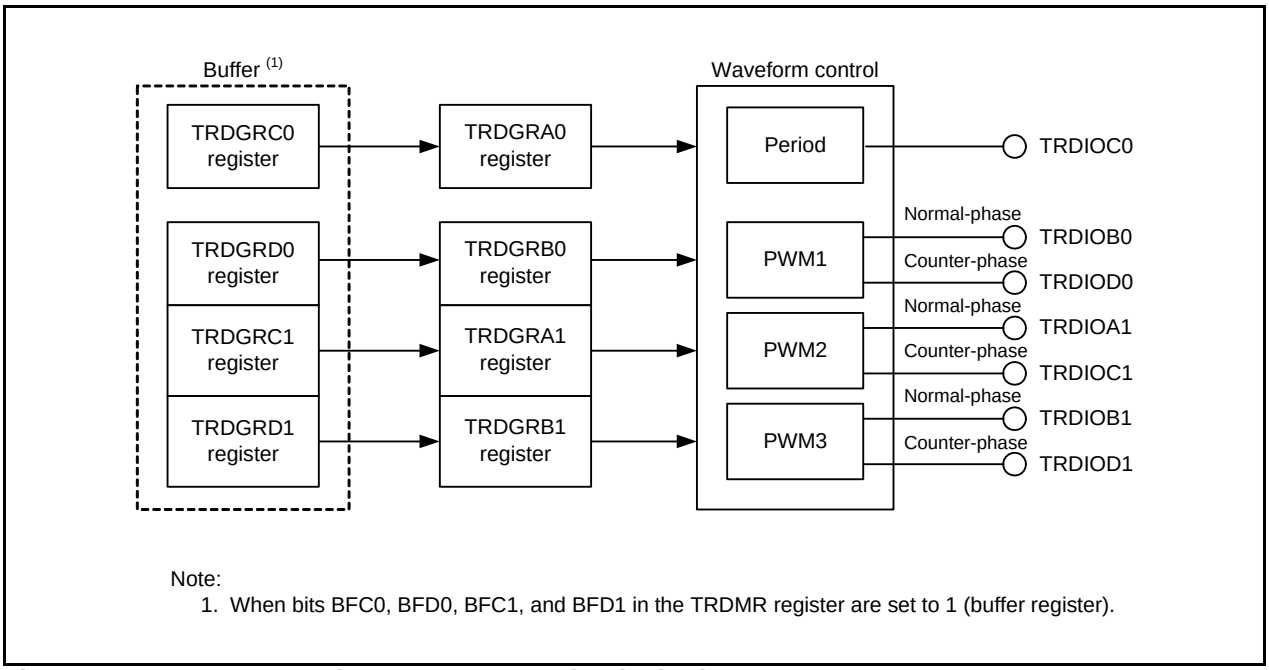
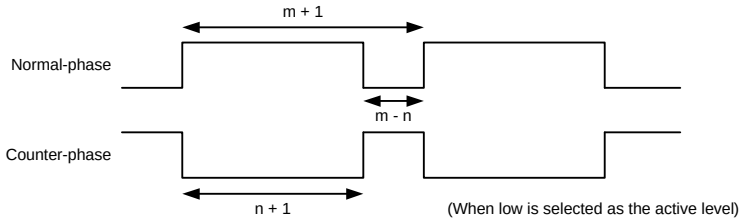


Figure 18.17 Reset Synchronous PWM Mode Block Diagram

Table 18.15 Reset Synchronous PWM Mode Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fHOCO, fHOCO-F External signal input to the TRDCLK pin (active edge selected by a program)
Count operations	The TRD0 register is incremented (the TRD1 register is not used).
PWM waveform	PWM period: 1/fk × (m + 1) Active level width of normal-phase: 1/fk × (m - n) Active level width of counter-phase: 1/fk × (n + 1) fk: Frequency of count source m: Value set in the TRDGRA0 register n: Value set in the TRDGRB0 register (PWM1 output) Value set in the TRDGRA1 register (PWM2 output) Value set in the TRDGRB1 register (PWM3 output) 
Count start condition	1 (count starts) is written to the TSTART0 bit in the TRDSTR register.
Count stop conditions	• 0 (count stops) is written to the TSTART0 bit when the CSEL0 bit in the TRDSTR register is set to 1. The PWM output pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register. • When the CSEL0 bit in the TRDSTR register is set to 0, the count stops at a compare match with the TRDGRA0 register. The PWM output pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register.
Interrupt request generation timing	• Compare match (content of the TRD0 register matches content of registers TRDGRj0, TRDGRA1, and TRDGRB1) • TRD0 register overflow
TRDIOA0 pin function	Programmable I/O port or TRDCLK (external clock) input
TRDIOB0 pin function	PWM1 output normal-phase output
TRDIOD0 pin function	PWM1 output counter-phase output
TRDIOA1 pin function	PWM2 output normal-phase output
TRDIOC1 pin function	PWM2 output counter-phase output
TRDIOB1 pin function	PWM3 output normal-phase output
TRDIOD1 pin function	PWM3 output counter-phase output
TRDIOC0 pin function	Output inverted every PWM period
$\overline{\text{INT0}}$ pin function	Pulse output forced cutoff signal input (programmable I/O port or $\overline{\text{INT0}}$ interrupt input)
Read from timer	The count value can be read by reading the TRD0 register.
Write to timer	The value can be written to the TRD0 register.
Selectable functions	• The normal-phase and counter-phase active level and initial output level are selected individually. • Buffer operation (refer to **18.3.1.2 Buffer Operation**) • Pulse output forced cutoff signal input (refer to **18.3.1.4 Pulse Output Forced Cutoff**) • A/D trigger generation

j = A, B, C, or D

18.3.5.1 Operation Example

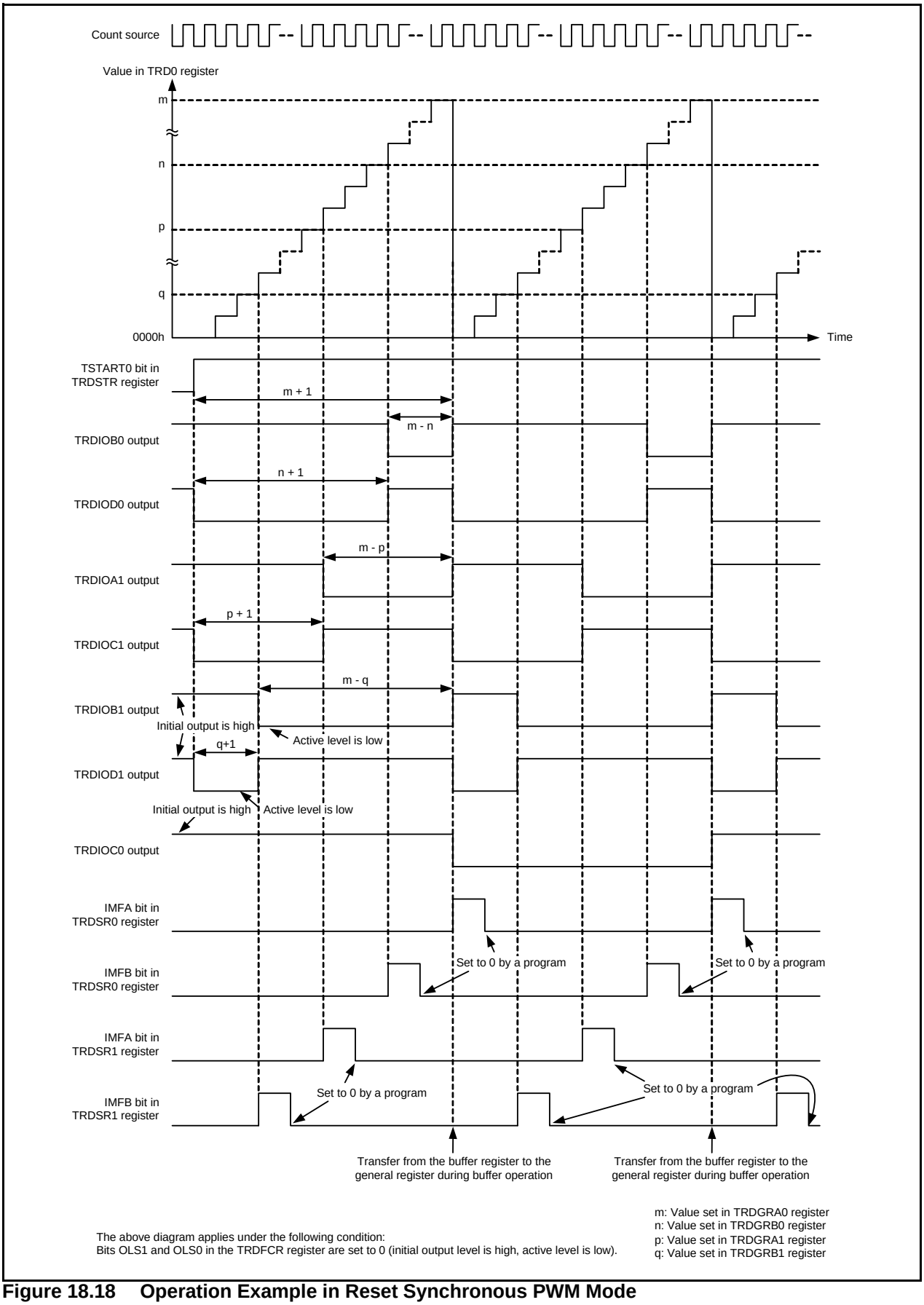


Figure 18.18 Operation Example in Reset Synchronous PWM Mode

18.3.6 Complementary PWM Mode

In this mode, three normal-phases and three counter-phases of the PWM waveform are output with the same period (three-phase, triangular wave modulation, and with dead time).
Figure 18.19 shows the Complementary PWM Mode Block Diagram and Table 18.16 lists the Complementary PWM Mode Specifications. Figure 18.20 shows the Output Model of Complementary PWM Mode (i = 0 or 1) and Figure 18.21 shows an Operation Example in Complementary PWM Mode (i = 0 or 1).

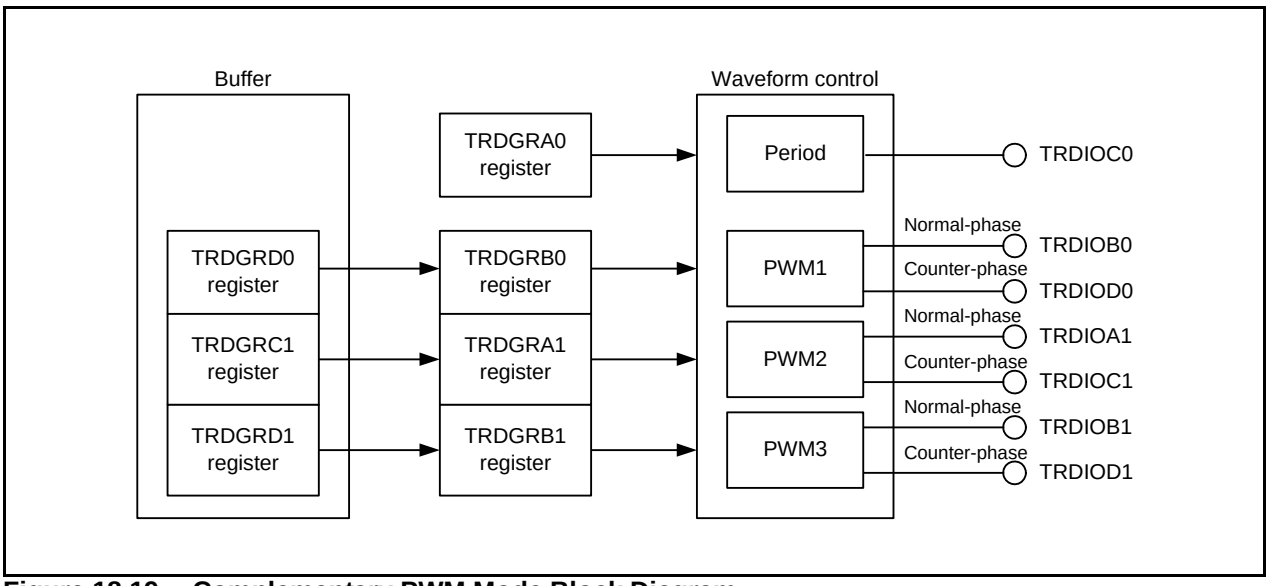
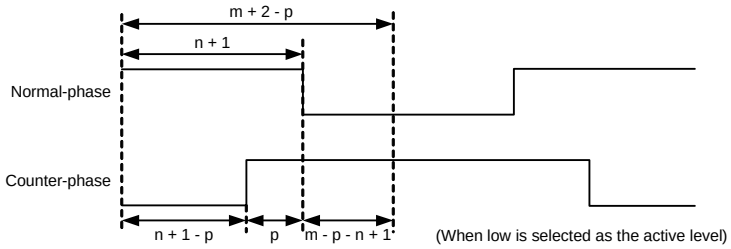


Figure 18.19 Complementary PWM Mode Block Diagram

Table 18.16 Complementary PWM Mode Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fHOCO, fHOCO-F External signal input to the TRDCLK pin (active edge selected by a program) Set bits TCK2 to TCK0 in the TRDCR1 register to the same value (same count source) as bits TCK2 to TCK0 in the TRDCR0 register.
Count operations	Increment or decrement. Registers TRD0 and TRD1 are decremented at a compare match between registers TRD0 and TRDGRA0 during increment operation. When the TRD1 register changes from 0000h to FFFFh during decrement operation, registers TRD0 and TRD1 are incremented.
PWM operations	PWM period: 1/fk × (m + 2 - p) × 2 (1) Dead time: p Active level width of normal-phase: 1/fk × (m - n - p + 1) × 2 Active level width of counter-phase: 1/fk × (n + 1 - p) × 2 fk: Frequency of count source m: Value set in the TRDGRA0 register n: Value set in the TRDGRB0 register (PWM1 output) Value set in the TRDGRA1 register (PWM2 output) Value set in the TRDGRB1 register (PWM3 output) p: Value set in the TRD0 register 
Count start condition	1 (count starts) is written to bits TSTART0 and TSTART1 in the TRDSTR register.
Count stop conditions	0 (count stops) is written to bits TSTART0 and TSTART1 in the TRDSTR register when the CSEL0 bit in the TRDSTR register is set to 1. (The PWM output pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register.)
Interrupt request generation timing	• Compare match (content of the TRDi register matches content of the TRDGRji register) • TRD1 register underflow
TRDIOA0 pin function	Programmable I/O port or TRDCLK (external clock) input
TRDIOB0 pin function	PWM1 output normal-phase output
TRDIOD0 pin function	PWM1 output counter-phase output
TRDIOA1 pin function	PWM2 output normal-phase output
TRDIOC1 pin function	PWM2 output counter-phase output
TRDIOB1 pin function	PWM3 output normal-phase output
TRDIOD1 pin function	PWM3 output counter-phase output
TRDIOC0 pin function	Output inverted every 1/2 period of PWM
$\overline{\text{INT0}}$ pin function	Pulse output forced cutoff signal input (programmable I/O port or $\overline{\text{INT0}}$ interrupt input)
Read from timer	The count value can be read by reading the TRDi register.
Write to timer	The value can be written to the TRDi register.
Selectable functions	• Pulse output forced cutoff signal input (refer to **18.3.1.4 Pulse Output Forced Cutoff**) • The normal-phase and counter-phase active level and initial output level are selected individually. • Transfer timing from the buffer register selection • A/D trigger generation

i = 0 or 1, j = A, B, C, or D

Note:

1. After a count starts, the PWM period is fixed.

18.3.6.1 Operation Example

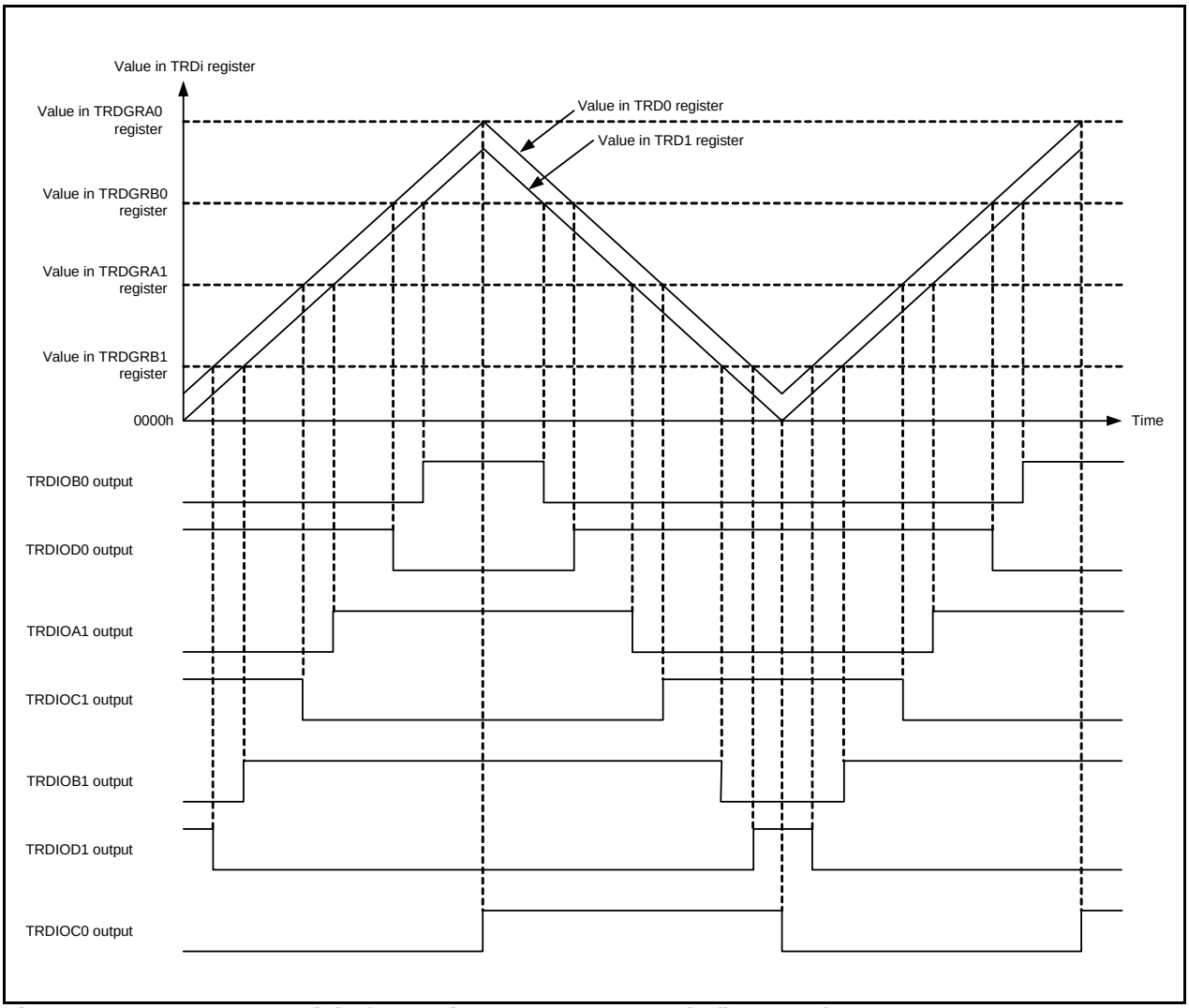


Figure 18.20 Output Model of Complementary PWM Mode (i = 0 or 1)

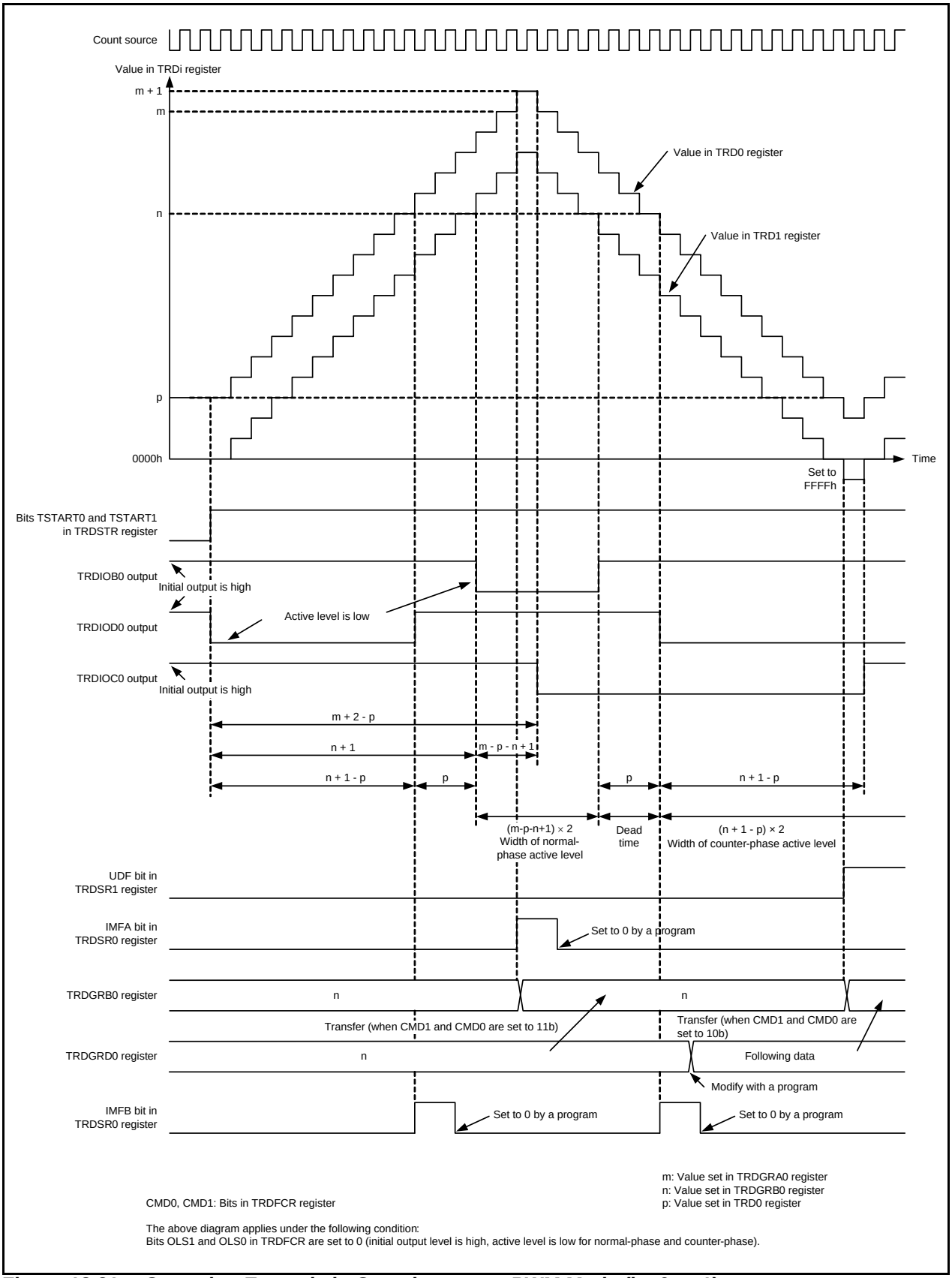


Figure 18.21 Operation Example in Complementary PWM Mode (i = 0 or 1)

18.3.6.2 Transfer Timing from Buffer Register

- Transfer from the TRDGRD0, TRDGRC1, or TRDGRD1 register to the TRDGRB0, TRDGRA1, or TRDGRB1 register.
  When bits CMD1 and CMD0 in the TRDFCR register are set to 10b, the content is transferred when the TRD1 register underflows.
  When bits CMD1 and CMD0 are set to 11b, the content is transferred at compare match between registers TRD0 and TRDGRA0.

18.3.7 PWM3 Mode

In this mode, two PWM waveforms with the same period are output.
Figure 18.22 shows the PWM3 Mode Block Diagram, Table 18.17 lists the PWM3 Mode Specifications, and Figure 18.23 shows an Operation Example in PWM3 Mode.

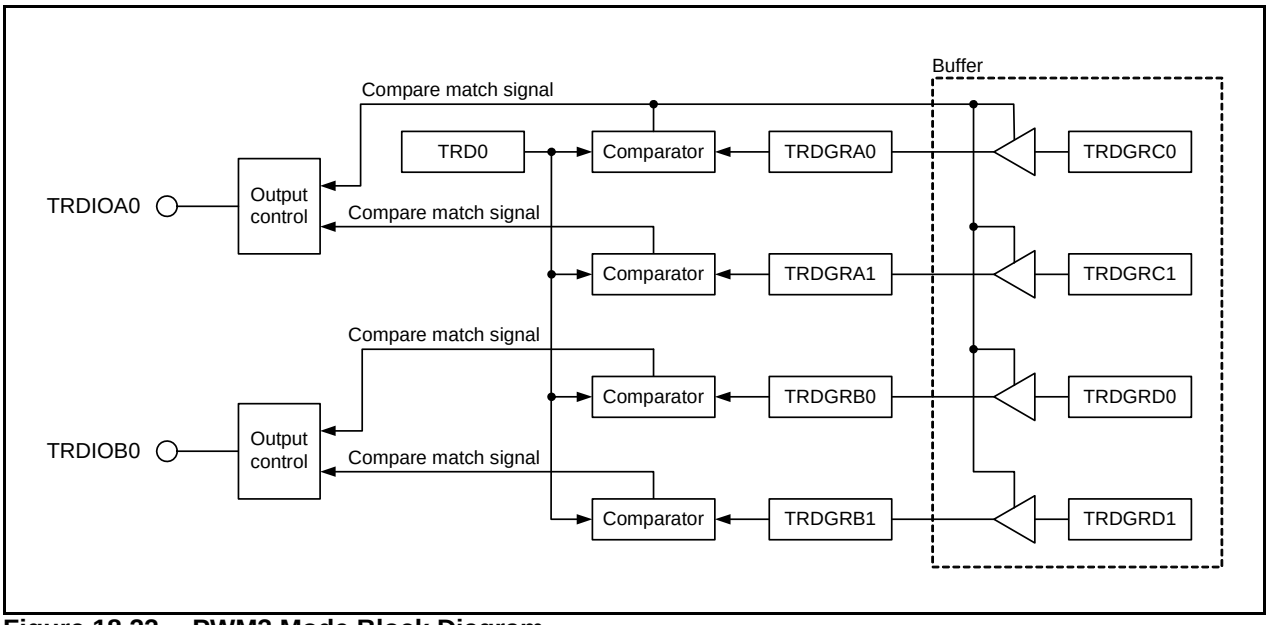
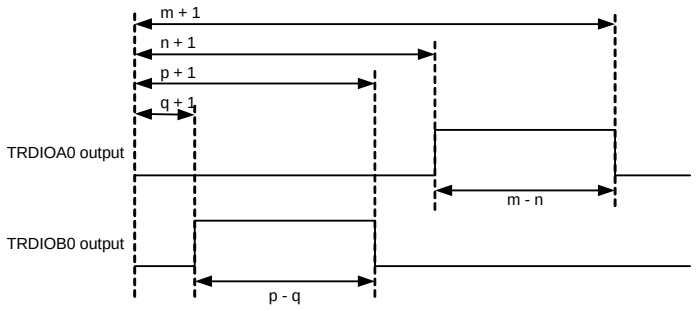


Figure 18.22 PWM3 Mode Block Diagram

Table 18.17 PWM3 Mode Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fHOCO, fHOCO-F
Count operations	The TRD0 register is incremented (the TRD1 register is not used).
PWM waveform	PWM period: 1/fk × (m + 1) Active level width of TRDIOA0 output: 1/fk × (m - n) Active level width of TRDIOB0 output: 1/fk × (p - q) fk: Frequency of count source m: Value set in the TRDGRA0 register n: Value set in the TRDGRA1 register p: Value set in the TRDGRB0 register q: Value set in the TRDGRB1 register  (When high is selected as the active level)
Count start condition	1 (count starts) is written to the TSTART0 bit in the TRDSTR register.
Count stop conditions	• 0 (count stops) is written to the TSTART0 bit in the TRDSTR register when the CSEL0 bit in the TRDSTR register is set to 1. The PWM output pin retains the output level before the count stops. • When the CSEL0 bit in the TRDSTR register is set to 0, the count stops at a compare match with the TRDGRA0 register. The PWM output pin retains the level after the output change due to the compare match.
Interrupt request generation timing	• Compare match (content of the TRD0 register matches content of the TRDGRji register) • TRD0 register overflow
TRDIOA0, TRDIOB0 pin function	PWM output
TRDIOC0, TRDIOD0, TRDIOA1 to TRDIOD1 pin function	Programmable I/O port
$\overline{\text{INT0}}$ pin function	Pulse output forced cutoff signal input (programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRD0 register.
Write to timer	The value can be written to the TRD0 register.
Selectable functions	• Pulse output forced cutoff signal input (refer to **18.3.1.4 Pulse Output Forced Cutoff**) • Buffer operation (refer to **18.3.1.2 Buffer Operation**) • Active level selectable for each pin • A/D trigger generation

i = 0 or 1, j = A, B, C, or D

18.3.7.1 Operation Example

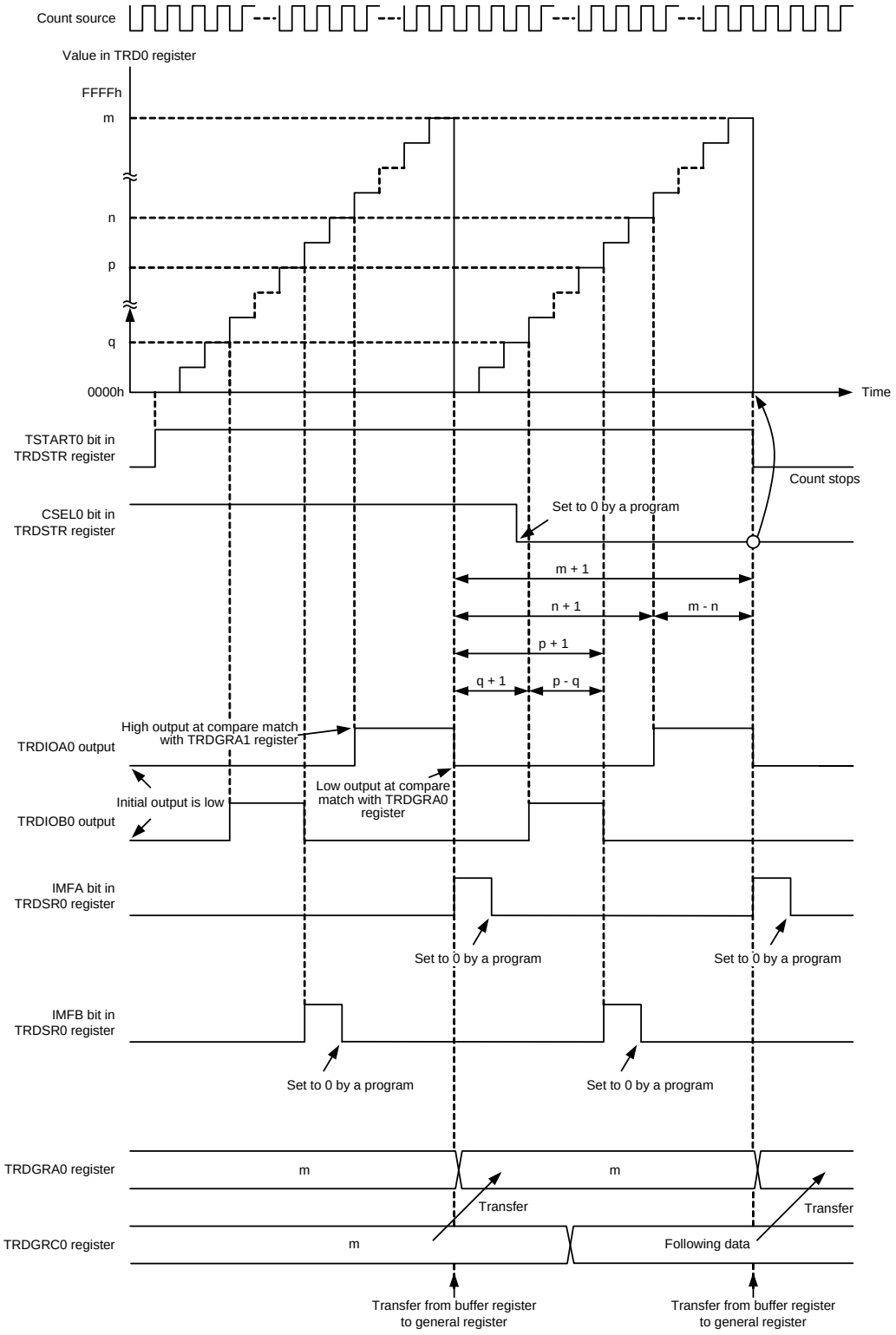


Figure 18.23 Operation Example in PWM3 Mode

18.3.8 Timer RD Interrupt

Timer RD generates the timer RDi (i = 0 or 1) interrupt request from six sources for each timer RD0 and timer RD1. The timer RD interrupt uses the single TRDiIC register (bits IR and ILVL0 to ILVL2) and a single vector for each timer RD0 and timer RD1.
Table 18.18 lists the Registers Associated with Timer RD Interrupt and Figure 18.24 shows the Timer RD Interrupt Block Diagram (i = 0 or 1).

Table 18.18 Registers Associated with Timer RD Interrupt

	Timer RD Status Register	Timer RD Interrupt Enable Register	Timer RD Interrupt Control Register
Timer RD0	TRDSR0	TRDIER0	TRD0IC
Timer RD1	TRDSR1	TRDIER1	TRD1IC

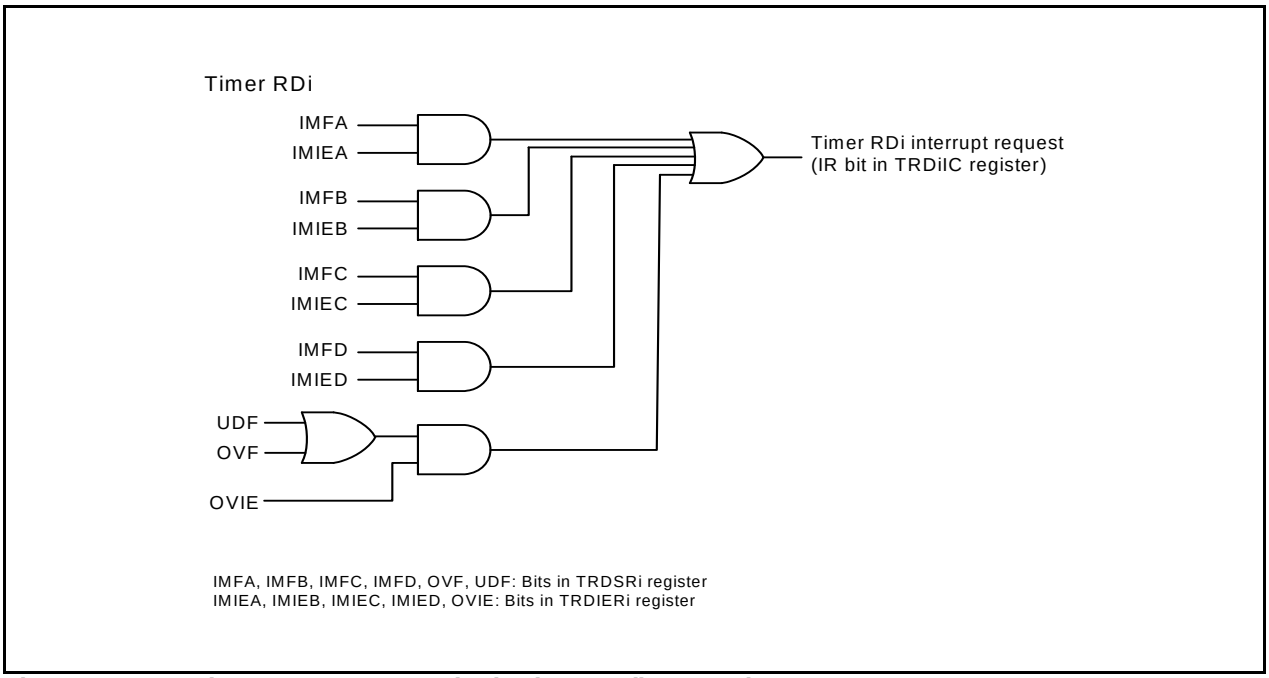


Figure 18.24 Timer RD Interrupt Block Diagram (i = 0 or 1)

As with other maskable interrupts, the timer RD interrupt is controlled by the combination of the I flag, the IR bit in the TRDiIC register, bits ILVL0 to ILVL2, and IPL. However, since the interrupt source (timer RD interrupt) is generated by a combination of multiple interrupt request sources, the following differences from other maskable interrupts apply:

- When bits in the TRDSRi register corresponding to bits set to 1 in the TRDIERi register are set to 1 (interrupt enabled), the IR bit in the TRDiIC register is set to 1 (interrupt requested).
- When either bits in the TRDSRi register or bits in the TRDIERi register corresponding to bits in the TRDSRi register, or both of them, are set to 0, the IR bit is set to 0 (no interrupt requested). Therefore, even though the interrupt is not acknowledged after the IR bit is set to 1, the interrupt request will not be retained.
- When the conditions of other request sources are met, the IR bit remains 1.
- If multiple bits in the TRDIERi register are set to 1, use the TRDSRi register to determine the source of the interrupt request.
- Since the bits in the TRDSRi register are not automatically set to 0 even if the interrupt is acknowledged, set the corresponding bit to 0 in the interrupt routine. For the procedure for setting these bits to 0, refer to **18.2.14 Timer RD Status Register i (TRDSRi) (i = 0 or 1)**.

Refer to **18.2.14 Timer RD Status Register i (TRDSRi) (i = 0 or 1)** for details on the TRDSRi register and **18.2.15 Timer RD Interrupt Enable Register i (TRDIERi) (i = 0 or 1)** for details on the TRDIERi register. Refer to **11.4 Interrupt Control** for details on the TRDiIC register and **11.3.2 Relocatable Vector Table** for information on the interrupt vectors.

18.4 Notes on Timer RD

18.4.1 SFR Read/Write Access

18.4.1.1 TRDELCCR Register

- Do not rewrite the TRDELCCR register during timer operation.

18.4.1.2 TRDSTR Register

- Write to the TRDSTR register using the MOV instruction.
- When the CSELi bit (i = 0 or 1) in the TRDSTR register is set to 0 (count stops at compare match between registers TRDi and TRDGRAi), the count does not stop and the TSTARTi bit remains unchanged even if 0 (count stops) is written to the TSTARTi bit.
  The TSTARTi bit is set to 0 (count stops) only by a compare match with the TRDGRAi register.
  If the CSELi bit is 0 when rewriting the TRDSTR register, write 0 to the TSTARTi bit to change the CSELi bit to 1 without affecting the count operation.
  If 1 is written to the TSTARTi bit while the counter is stopped, the count may be started.
  To stop counting by a program, set the TSTARTi bit after setting the CSELi bit to 1. Even if 1 is written to the CSELi bit and 0 is written to the TSTARTi bit at the same time (using one instruction), the count cannot be stopped.
- Table 18.19 lists the TRDIOji Pin (j = A, B, C, or D) Output Level when Count is Stopped while the TRDIOji pin is used for timer RD output.

Table 18.19 TRDIOji Pin (j = A, B, C, or D) Output Level when Count is Stopped

Count Stop	TRDIOji Pin Output When Count is Stopped
When the CSELi bit is set to 1, write 0 to the TSTARTi bit and the count stops.	The pin retains the output level immediately before the count stops. (The pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register in timer RD complementary and reset synchronous PWM modes.)
When the CSELi bit is set to 0, the count stops at a compare match between registers TRDi and TRDGRAi.	The pin retains the output level after the output change due to the compare match. (The pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register in timer RD complementary and reset synchronous PWM modes.)

i = 0 or 1, j = A, B, C, or D

18.4.1.3 TRDi Register

- When writing to the TRDi register overlaps with the timing for setting the TRDi register to 0000h, the write value has priority.
- When writing a value to the TRDi register and then reading the same register consecutively, the value before writing may be read. In this case, execute the JMP.B instruction between writing and reading.

```
Program example     MOV.W   #XXXXh, TRD0    ; Write
                    JMP.B   L1              ; JMP.B
                L1: MOV.W   TRD0, DATA      ; Read
```

18.4.1.4 TRDSRi Register (i = 0 or 1)

When writing a value to the TRDSRi register and then reading the same register consecutively, the value before writing may be read. In this case, execute the JMP.B instruction between writing and reading.

```
Program example     MOV.B   #XXh, TRDSR0      ; Write
                    JMP.B   L1                ; JMP.B
                L1: MOV.B   TRDSR0, DATA      ; Read
```

18.4.1.5 TRDCRi Register

When setting bits TCK2 to TCK0 in the TRDCRi register to 111b (fHOCO-F), set fHOCO-F to a clock frequency higher than the CPU clock frequency.

18.4.1.6 TRDDFi Register

As a hazard precaution, set bits DFCK0 and DFCK1 in the TRDDFi register before starting the count operation.

18.4.2 Mode Switching

- When switching modes during operation, first stop the count (TSTART = 0) before switching.
- After switching modes, clear the interrupt register before starting operation.
  Refer to **11.9.4 Changing Interrupt Sources**.

18.4.3 Count Source Switching

- Switch the count source after stopping the count.
  Also, after switching the count source, wait for at least two cycles of the CPU clock before writing to the SFR of the module.
  [Changing procedure]
  (1) Set the TSTARTi bit in the TRDSTR register to 0 (count stops).
  (2) Change bits TCK0 to TCK2 in the TRDCRi register.
  (3) Wait for at least two cycles of the CPU clock.
  (4) Writing to the SFR of timer RD is enabled.
- Instead of the setting change in the above step (2), the same processing is also necessary when changing the settings of bits SYNC and PWM3.
  Software processing is not necessary when stopping the high-speed on-chip oscillator using the FRA00 bit.
- When changing the count source from fHOCO-F to fHOCO and stopping fHOCO-F, wait for at least two cycles of fHOCO-F after changing the clock setting before stopping fHOCO-F.
  [Changing procedure]
  (1) Set the TSTARTi bit in the TRDSTR register to 0 (count stops).
  (2) Change bits TCK0 to TCK2 in the TRDCRi register.
  (3) Wait for at least two cycles of fHOCO-F.
  (4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

• When changing the count source from fHOCO-F to a clock other than fHOCO and stopping fHOCO-F, wait at least one cycle of fHOCO-F + one cycle of fHOCO after changing the clock setting before stopping fHOCO-F.
[Changing procedure]
(1) Set the TSTARTi bit (i = 0 or 1) in the TRDSTR register to 0 (count stops).
(2) Change bits TCK0 to TCK2 in the TRDCRi register.
(3) Wait for at least one cycle of fHOCO-F + one cycle of fHOCO.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

Notes:
1. Do not set the FRA00 bit to 0 (high-speed on-chip oscillator off) while fHOCO or fHOCO-F is selected as the count source.
2. Do not change the division ratio of the high-speed on-chip oscillator set by the FRA2 register while fHOCO-F is selected as the count source.

18.4.4 Input Capture Function

• Set the pulse width of the input capture signal to three or more cycles of the timer RD operating clock (refer to **Table 18.1 Timer RD Operating Clocks**).
• The value of the TRDi register is transferred to the TRDGRji register two to three cycles of the timer RD operating clock after the input capture signal is applied to the TRDIOji pin (i = 0 or 1, j = A, B, C, or D) (when no digital filter is used).

18.4.5 Reset Synchronous PWM Mode

• When reset synchronous PWM mode is used for motor control, make sure OLS0 = OLS1.
• When setting reset synchronous PWM mode, use the following procedure:
[Changing procedure]
(1) Set the TSTART0 bit in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 and CMD0 in the TRDFCR register to 00b (timer mode, PWM mode, and PWM3 mode).
(3) Set bits CMD1 and CMD0 to 01b (reset synchronous PWM mode).
(4) Set the other registers associated with timer RD again.
• Notes on Starting Count
(1) If the timer value and the compare value are set to the same value, the count must not be started.
(2) When restarting the count once after it has stopped, verify that the timer value when the count stopped and the compare register value are different before restarting. If their values are the same, rewrite the timer value before restarting the count.

18.4.6 Complementary PWM Mode

- When complementary PWM mode is used for motor control, make sure OLS0 = OLS1.
- Change bits CMD0 and CMD1 in the TRDFCR register in the following procedure.

Changing procedure: When setting to complementary PWM mode (including re-set) or changing the transfer timing from the buffer register to the general register in complementary PWM mode.

(1) Set both the TSTART0 and TSTART1 bits in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 and CMD0 in the TRDFCR register to 00b (timer mode, PWM mode, and PWM3 mode).
(3) Set bits CMD1 and CMD0 to 10b or 11b (complementary PWM mode).
(4) Set the other registers associated with timer RD again.

Changing procedure: When stopping complementary PWM mode

(1) Set both the TSTART0 and TSTART1 bits in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 to CMD0 to 00b (timer mode, PWM mode, and PWM3 mode).

- Do not write to the TRDGRA0, TRDGRB0, TRDGRA1, or TRDGRB1 register during operation.
  When changing the PWM waveform, transfer the values written to registers TRDGRD0, TRDGRC1, and TRDGRD1 to registers TRDGRB0, TRDGRA1, and TRDGRB1 using buffer operation.
  However, to write data to the TRDGRD0, TRDGRC1, or TRDGRD1 register, set bits BFD0, BFC1, and BFD1 to 0 (general register). After this, bits BFD0, BFC1, and BFD1 may be set to 1 (buffer register).
  The PWM period cannot be changed.
- If the value set in the TRDGRA0 register is assumed to be m, the TRD0 register counts m - 1, m, m + 1, m, m - 1, in that order, when changing from increment to decrement operation.
  When changing from m to m + 1, the IMFA bit in the TRDSRi register is set to 1. Also, bits CMD1 and CMD0 in the TRDFCR register are set to 11b (complementary PWM mode, buffer data transferred at compare match between registers TRD0 and TRDGRA0), the content of the buffer registers (TRDGRD0, TRDGRC1, and TRDGRD1) is transferred to the general registers (TRDGRB0, TRDGRA1, and TRDGRB1).
  During the operation of m + 1, m, and m - 1, the IMFA bit remains unchanged and data is not transferred to registers such as the TRDGRA0 register.

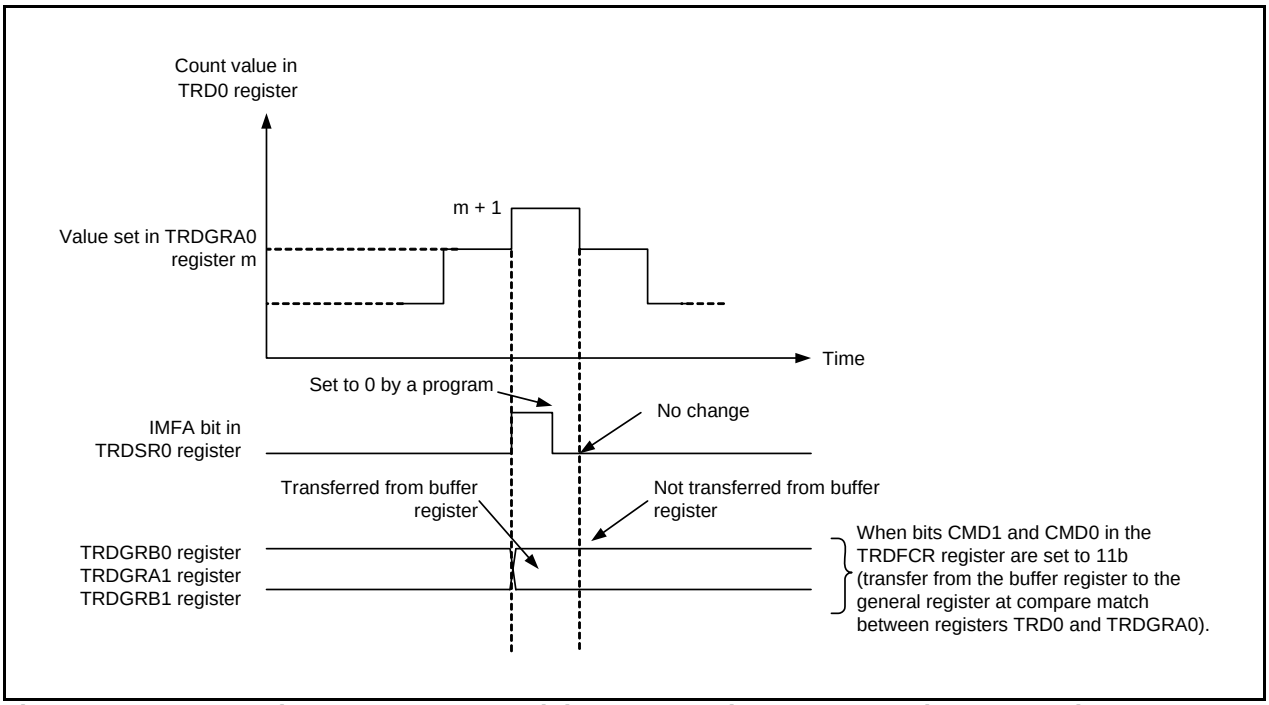


Figure 18.25 Operation at Compare Match between Registers TRD0 and TRDGRA0 in Complementary PWM Mode

- The TRD1 register counts 1, 0, FFFFh, 0, 1, in that order, when changing from decrement to increment operation.
  Counting from 1, to 0, to FFFFh causes the UDF bit in the TRDSRi register to be set to 1. Also, when bits CMD1 and CMD0 in the TRDFCR register are set to 10b (complementary PWM mode, buffer data transferred at underflow of the TRD1 register), the content of the buffer registers (TRDGRD0, TRDGRC1, and TRDGRD1) is transferred to the general registers (TRDGRB0, TRDGRA1, and TRDGRB1).
  During the operation of FFFFh, 0, and 1, data is not transferred to registers such as the TRDGRB0 register. Also, at this time, the OVF bit in the TRDSRi register remains unchanged.

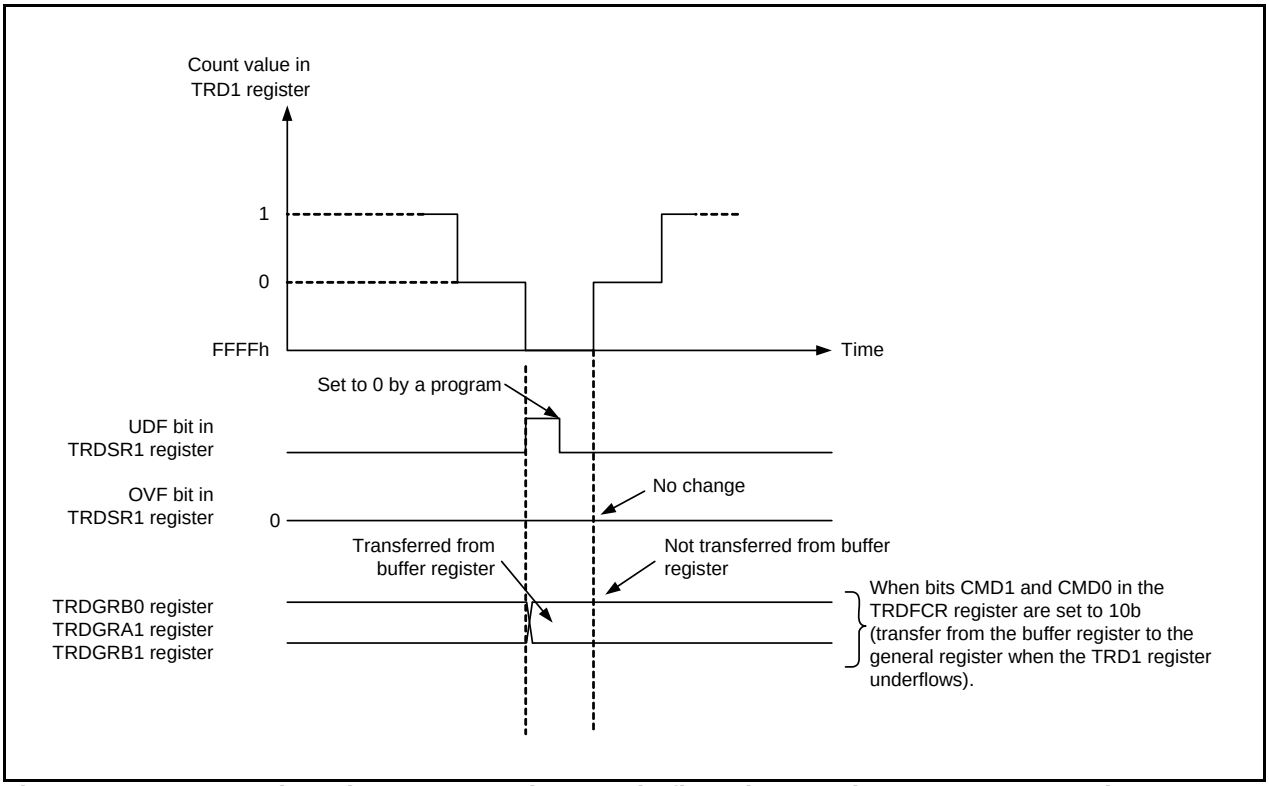


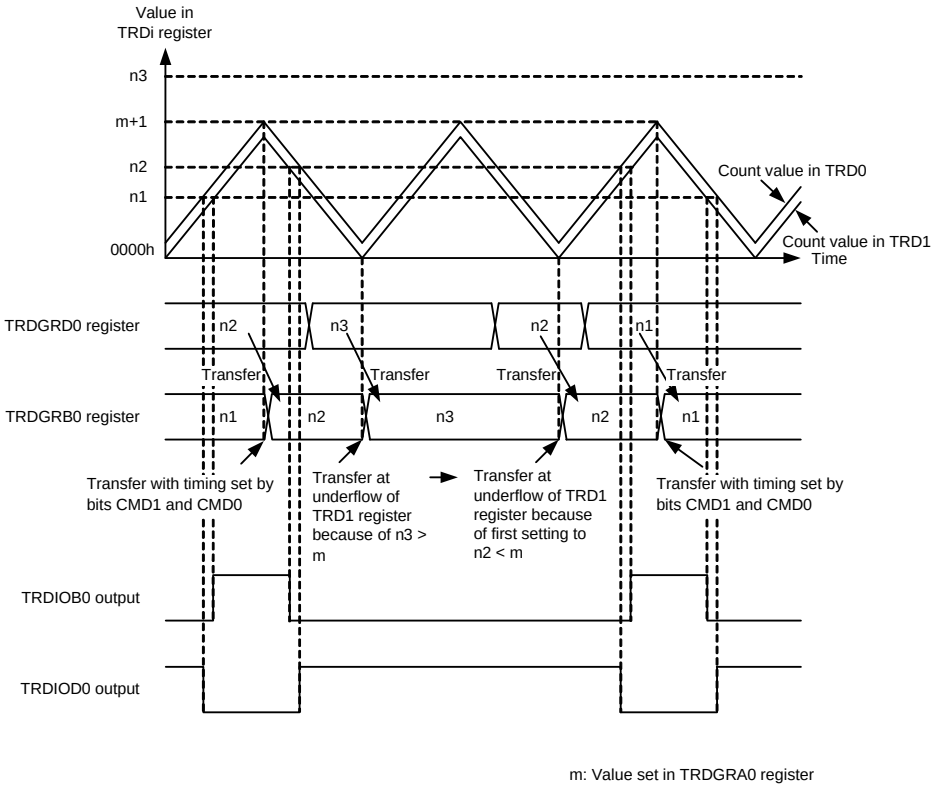
Figure 18.26 Operation when TRD1 Register Underflows in Complementary PWM Mode

• Select the timing of data transfer from the buffer register to the general register using bits CMD1 and CMD0 in the TRDFCR register. However, transfer takes place with the following timing regardless of the value of bits CMD1 and CMD0 in the following cases:

Value in buffer register ≥ value in TRDGRA0 register:

Transfer takes place at underflow of the TRD1 register.

After this, when the buffer register is set to a value that is 0001h or above and smaller than the value of the TRDGRA0 register, and the TRD1 register underflows for the first time after setting, the value is transferred to the general register. After that, the value is transferred with the timing selected by bits CMD1 and CMD0.



The above diagram applies under the following conditions:
- Bits CMD1 and CMD0 in the TRDFCR register are set to 11b (data in the buffer register is transferred at compare match between registers TRD0 and TRDGRA0 in complementary PWM mode).
- Both the OSL0 and OLS1 bits in the TRDFCR register are set to 1 (active high for normal-phase and counter-phase).

Figure 18.27 Operation when Value in Buffer Register ≥ Value in TRDGRA0 Register in Complementary PWM Mode (i = 0 or 1)

When the value in the buffer register is set to 0000h:

Transfer takes place at compare match between registers TRD0 and TRDGRA0.

After this, when the buffer register is set to a value that is 0001h or above and smaller than the value of the TRDGRA0 register, and a compare match occurs between registers TRD0 and TRDGRA0 for the first time after setting, the value is transferred to the general register. After that, the value is transferred with the timing selected by bits CMD0 and CMD1.

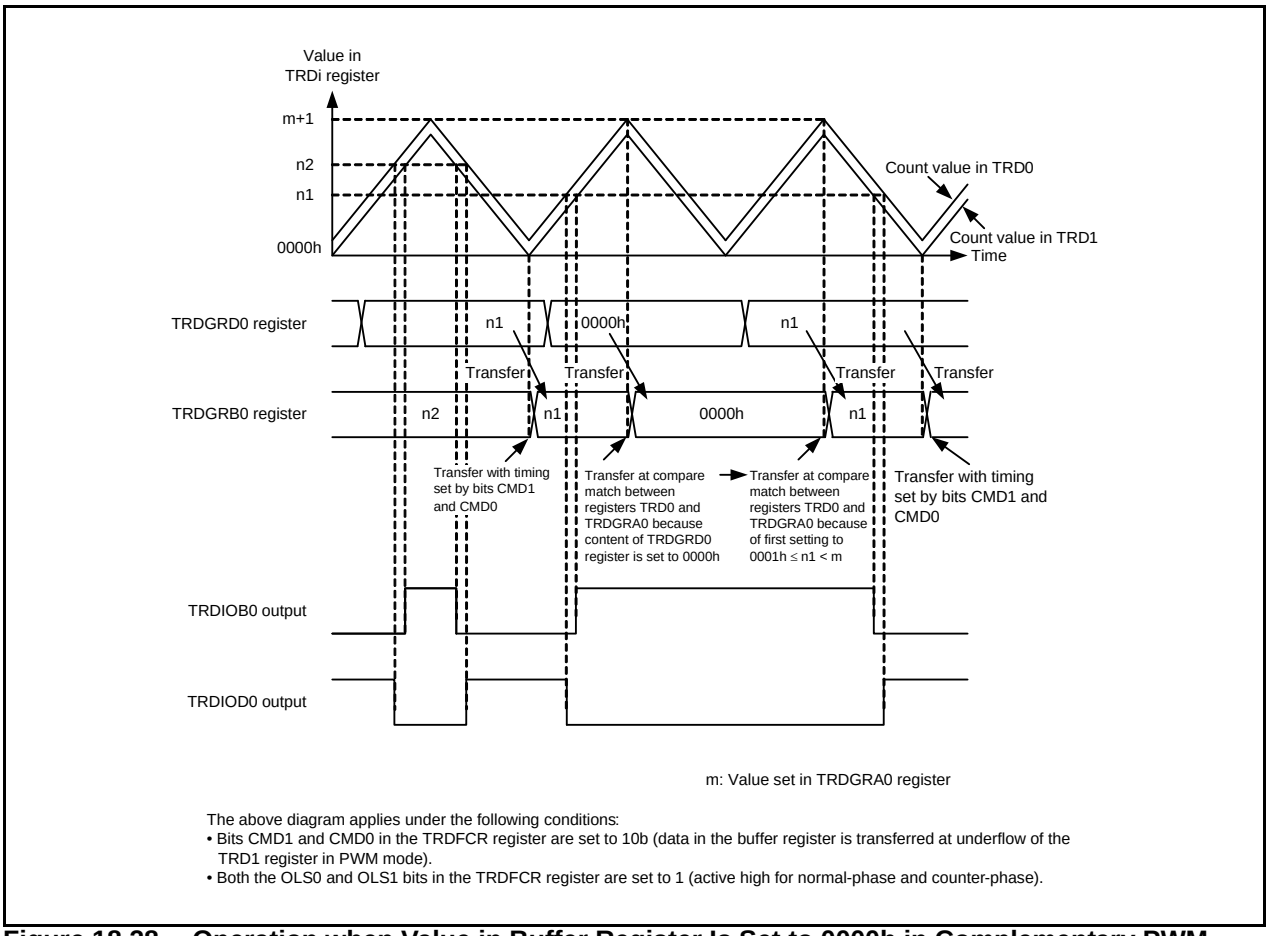


Figure 18.28 Operation when Value in Buffer Register Is Set to 0000h in Complementary PWM Mode (i = 0 or 1)

• Notes on Starting Count

(1) If the timer value and the compare value are set to the same value, the count must not be started.

(2) When restarting the count once after it has stopped, verify that the timer value when the count stopped and the compare register value are different before restarting. If their values are the same, rewrite the timer value before restarting the count.

18.4.7 Input Capture Operation when Count is Stopped

When the input capture function is used, if an input capture signal (edge selected by bits IOj0 and IOj1 (j = A or B) in the TRDIORAi register (i = 0 or 1) or bits IOk0 and IOk1 (k = C or D) in the TRDIORCi register) is input to the TRDIOni pin (n = A, B, C, or D), the IMFn bit in the TRDSRi register is set to 1 even when the TSTARTi bit in the TRDSTR register is set to 0 (count stops).

19. Timer RE2

19.1 Overview

Timer RE2 includes an 8-bit counter.
Timer RE2 supports the following mode:
• Compare match timer mode
A count source is counted and compare matches are detected.

Table 19.1 lists the Compare Match Timer Mode Specifications. Figure 19.1 shows the Compare Match Timer Mode Block Diagram, and Table 19.2 lists the Timer RE2 Pin Configuration.

Table 19.1 Compare Match Timer Mode Specifications

Item	Description
Count sources	f8, f32, f128, f256, f512, f2048, f4096, f8192
Count	Starting or stopping the count can be selected.
Reset	Reset by the RTCRST bit in the TRECR register
Interrupts	• Compare match interrupt • Overflow interrupt
TMRE2O pin functions	Either of the following is selected: • Programmable I/O port • Output of f4, f8, f16, or f32 • Output toggled at every compare match • The standby state can be set for the module only.

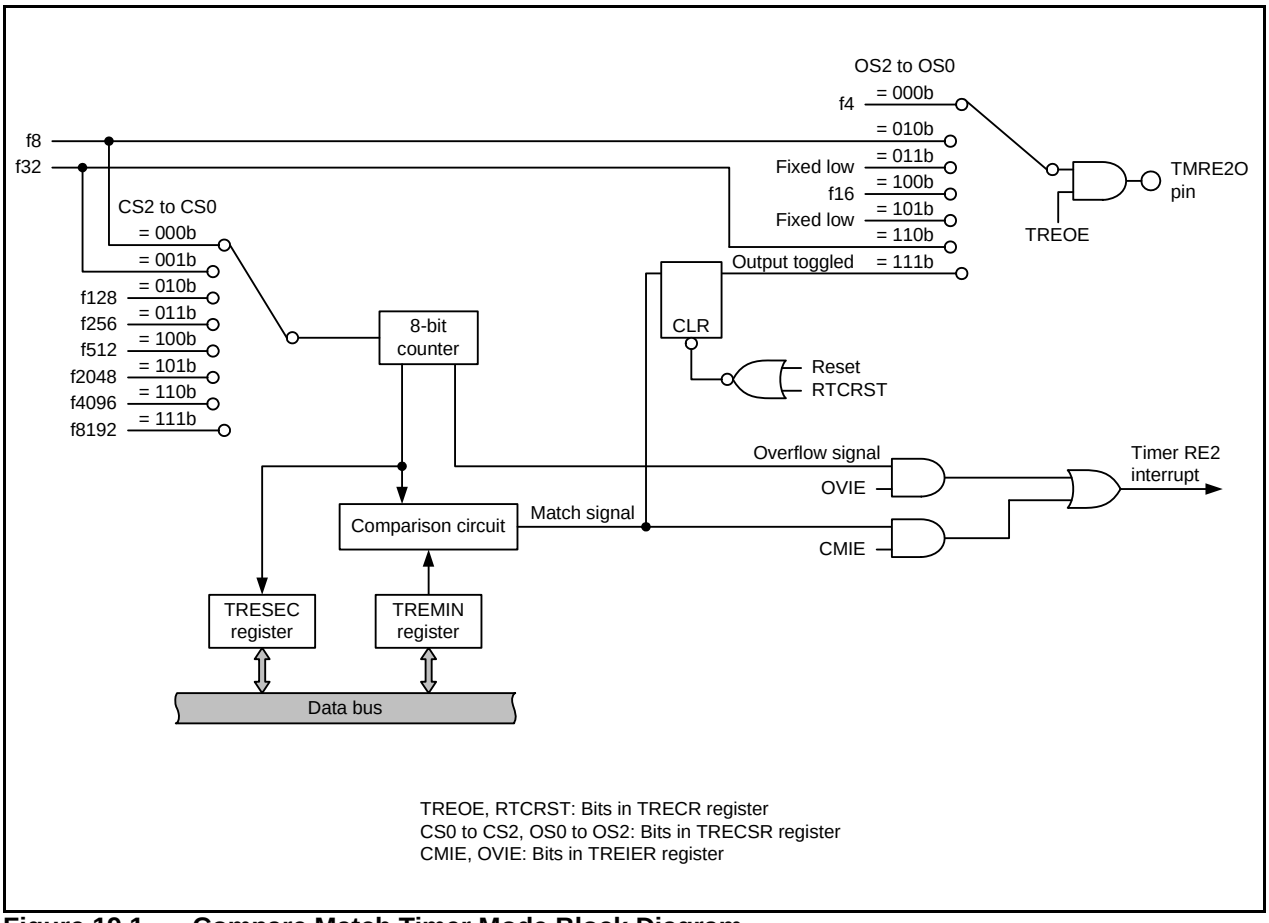


Figure 19.1 Compare Match Timer Mode Block Diagram

Table 19.2 Timer RE2 Pin Configuration

Pin Name	I/O	Function
TMRE2O	Output	Output for timer RE2

19.2 Registers

Table 19.3 lists the Timer RE2 Register Configuration.

Table 19.3 Timer RE2 Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Timer RE2 Counter Data Register	TRESEC	00h	00170h	8
Timer RE2 Compare Data Register	TREMIN	00h	00171h	8
Timer RE2 Control Register	TRECR	00000100b	00177h	8
Timer RE2 Count Source Select Register	TRECSR	00001000b	00178h	8
Timer RE2 Interrupt Flag Register	TREIFR	00h	0017Ah	8
Timer RE2 Interrupt Enable Register	TREIER	00h	0017Bh	8
Timer RE2 Protect Register	TREPRC	00h	0017Fh	8

19.2.1 Timer RE2 Counter Data Register (TRESEC)

Address 00170h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0
After reset by RTCRST bit in TRECR register	0	0	0	0	0	0	0	0

Bit	Function	R/W
b7 to b0	The data of the 8-bit counter can be read. The count value is retained even if timer RE2 stops counting. When the CCLR bit in the TRECR register is 0, the count continues even if a compare match occurs, and the TRESEC register is set to 00h when the CCLR bit is 1.	R

19.2.2 Timer RE2 Compare Data Register (TREMIN)

Address 00171h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MN7	MN6	MN5	MN4	MN3	MN2	MN1	MN0
After Reset	0	0	0	0	0	0	0	0
After reset by RTCRST bit in TRECR register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MN0	Compare data bit 0	The 8-bit compare data is stored. Write the compare value. (1)	R/W
b1	MN1	Compare data bit 1		R/W
b2	MN2	Compare data bit 2		R/W
b3	MN3	Compare data bit 3		R/W
b4	MN4	Compare data bit 4		R/W
b5	MN5	Compare data bit 5		R/W
b6	MN6	Compare data bit 6		R/W
b7	MN7	Compare data bit 7		R/W

Note:
1. The TREMIN register can be changed when the PROTECT bit in the TREPRC register is 1 (write enabled).

The TREMIN register is always compared with the TRESEC register, and the CMIF bit in the TREIFR register is set to 1 (interrupt requested) when the values of both the registers match. When the CMIE bit in the TREIER register is 1 (compare match interrupt enabled), an interrupt request is generated.
Write to the TREMIN register when the RUN bit in the TRECR register is 0 (count stops).

19.2.3 Timer RE2 Control Register (TRECR)

Address 00177h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RUN	—	—	RTCRST	CCLR	—	TREOE	—
After Reset	0	0	0	0	0	1	0	0
After reset by RTCRST bit in TRECR register	0	0	0	X (1)	X (1)	1	X (1)	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	TREOE	Timer RE2 output enable bit	0: TMRE2O output disabled 1: TMRE2O output enabled	R/W
b2	—	Reserved	Set to 1.	R/W
b3	CCLR	Counter clear enable bit	0: TRESEC register initialization by compare match is disabled 1: TRESEC register initialization by compare match is enabled	R/W
b4	RTCRST	Timer RE2 reset bit (2, 3)	0: Normal operation 1: The registers are initialized and the counter control circuit is initialized.	R/W
b5	—	Reserved	Set to 0.	R/W
b6	—			
b7	RUN	Timer RE2 operation start bit (3, 4)	0: Count stops 1: Count starts	R/W

Notes:
1. X indicates that this bit is not cleared by the RTCRST bit.
2. Set the RTCRST bit to 0 after setting it to 1. For the initialized values, refer to each register value after a reset by the RTCRST bit.
3. Low output after a reset is cleared or timer RE is reset by the RTCRST bit in TRECR. The output level is retained when the RUN bit is set to 0 (count stops).
4. The count value is retained while the count is stopped.

TREOE Bit (Timer RE2 output enable bit)

Change this bit when the RUN bit is set to 0 (count stops).

CCLR Bit (Counter clear enable bit)

Change this bit when the RUN bit is set to 0 (count stops).
When registers TRESEC and TREMIN are compared and match, the CCLR bit is used to select whether to initialize the TRESEC register (8-bit counter).

19.2.4 Timer RE2 Count Source Select Register (TRECSR)

Address 00178h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	OS2	OS1	OS0	CS3	CS2	CS1	CS0
After Reset	0	0	0	0	1	0	0	0
After reset by RTCRST bit in TRECR register	0	X (1)	X (1)	X (1)	X (1)	X (1)	X (1)	X (1)

Bit	Symbol	Bit Name	Function	R/W
b0	CS0	Count source select bits (2)	Set the following values in compare match timer mode: b3 b2 b1 b0 0 0 0 0: f8 0 0 0 1: f32 0 0 1 0: f128 0 0 1 1: f256 0 1 0 0: f512 0 1 0 1: f2048 0 1 1 0: f4096 0 1 1 1: f8192 Other than the above: Do not set.	R/W
b1	CS1			R/W
b2	CS2			R/W
b3	CS3			R/W
b4	OS0	Timer RE2 output select bits	b6 b5 b4 0 0 0: f4 0 0 1: Do not set. 0 1 0: f8 0 1 1: Low level is fixed 1 0 0: f16 1 0 1: Low level is fixed 1 1 0: f32 1 1 1: Output toggled at every compare match	R/W
b5	OS1			R/W
b6	OS2			R/W
b7	—	Reserved	Set to 0.	R/W

Notes:
1. X indicates that this bit is not cleared by the RTCRST bit.
2. The value of these bits is set to 1000b after a reset is cleared, but must always be rewritten during operation.

Bits CS0 to CS3 (Count source select bits)

Change these bits when the RUN bit in the TRECR register is 0 (count stops).

Bits OS0 to OS2 (Timer RE2 output select bits)

Change these bit when the RUN bit is 0 (count stops).
These bits are enabled when the TREOE bit in the TRECR register is 1 (TMRE2O output enabled).
When 111b is written to bits OS2 to OS0, the internal output level is set to low.

19.2.5 Timer RE2 Interrupt Flag Register (TREIFR)

Address 0017Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	OVIF	CMIF
After Reset	0	0	0	0	0	0	0	0
After reset by RTCRST bit in TRECR register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CMIF	Compare match interrupt flag	0: No interrupt requested 1: Interrupt requested	R/W
b1	OVIF	Overflow interrupt flag		R/W
b2	—	Reserved	Set to 0.	R/W
b3	—			W
b4	—			W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	—			
b7	—	Reserved	Set to 0.	R/W

CMIF Bit (Compare match interrupt flag)

[Conditions for setting to 0]
- When 0 is written to this bit after reading it. If the result of reading this bit is 1, writing 0 to this bit will set it to 0.
- When an interrupt from the DTC is automatically cleared.

[Condition for setting to 1]
- The contents of registers TRESEC and TREMIN match.

If the result of reading this bit is 0, writing 0 to this bit will not change its value. If this bit changes from 0 to 1 after the read, the bit will remain 1 even if 0 is written. Writing 1 has no effect.

OVIF Bit (Overflow interrupt flag)

[Conditions for setting to 0]
- When 0 is written to this bit after reading it. If the result of reading this bit is 1, writing 0 to this bit will set it to 0.
- When an interrupt from the DTC is automatically cleared.

[Condition for setting to 1]
- The 8-bit counter overflows.

If the result of reading this bit is 0, writing 0 to this bit will not change its value. If this bit changes from 0 to 1 after the read, the bit will remain 1 even if 0 is written. Writing 1 has no effect.

19.2.6 Timer RE2 Interrupt Enable Register (TREIER)

Address 0017Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	OVIE	CMIE
After Reset	0	0	0	0	0	0	0	0
After reset by RTCRST bit in TRECR register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CMIE	Compare match interrupt enable bit	0: Compare match interrupt disabled 1: Compare match interrupt enabled	R/W
b1	OVIE	Overflow interrupt enable bit	0: Overflow interrupt disabled 1: Overflow interrupt enabled	R/W
b2	—	Reserved	Set to 0.	R/W
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Write to the TREIER register when the RUN bit in the TRECR register is 0 (count stops).

19.2.7 Timer RE2 Protect Register (TREPRC)

Address 0017Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PROTECT	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0
After reset by RTCRST bit in TRECR register	X (1)	X (1)	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—	Reserved	Set to 0.	R/W
b7	PROTECT	Protect bit	Writing to the TREMIN register 0: Write disabled 1: Write enabled	R/W

Note:
1. X indicates that this bit is not cleared by the RTCRST bit.

PROTECT Bit (Protect bit)

The TREMIN register can be changed when the PROTECT bit is 1 (write enabled).
When 1 is written to the PROTECT bit by a program, this bit remains 1. Use the following procedure to change the TRESEC register:
(1) Write 1 to the PROTECT bit.
(2) Write a value to the TREMIN register.
(3) Write 0 (write disabled) to this bit.

19.3 Operation in Compare Match Timer Mode

19.3.1 Operation Example

19.3.2 Example of Setting Associated Registers

Figure 19.2 shows the Initial Setting Procedure when Timer RE2 is Used in Compare Match Timer Mode and Figure 19.3 shows an Operation Example in Compare Match Timer Mode. Also, refer to Figure 19.2 when setting these registers again.

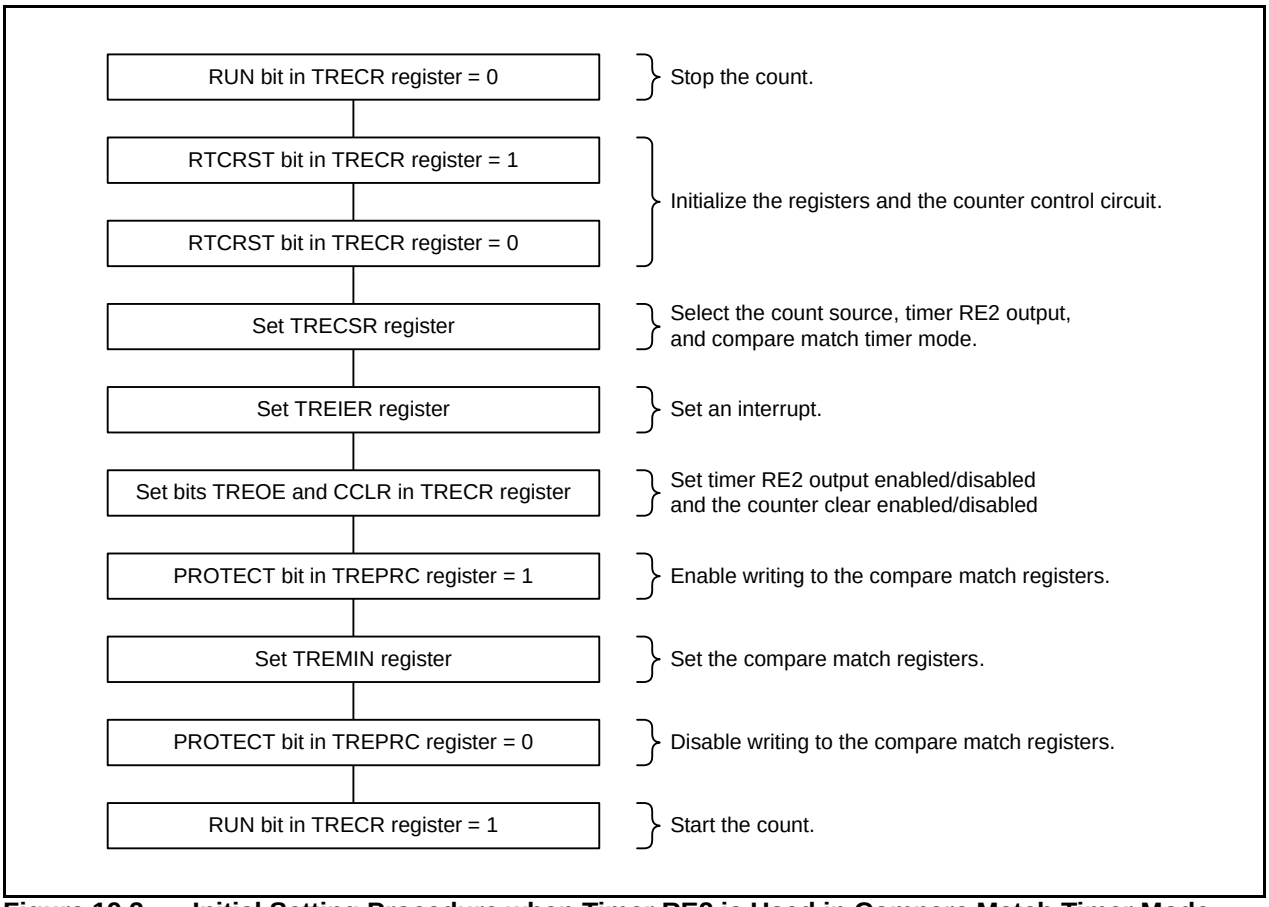


Figure 19.2 Initial Setting Procedure when Timer RE2 is Used in Compare Match Timer Mode

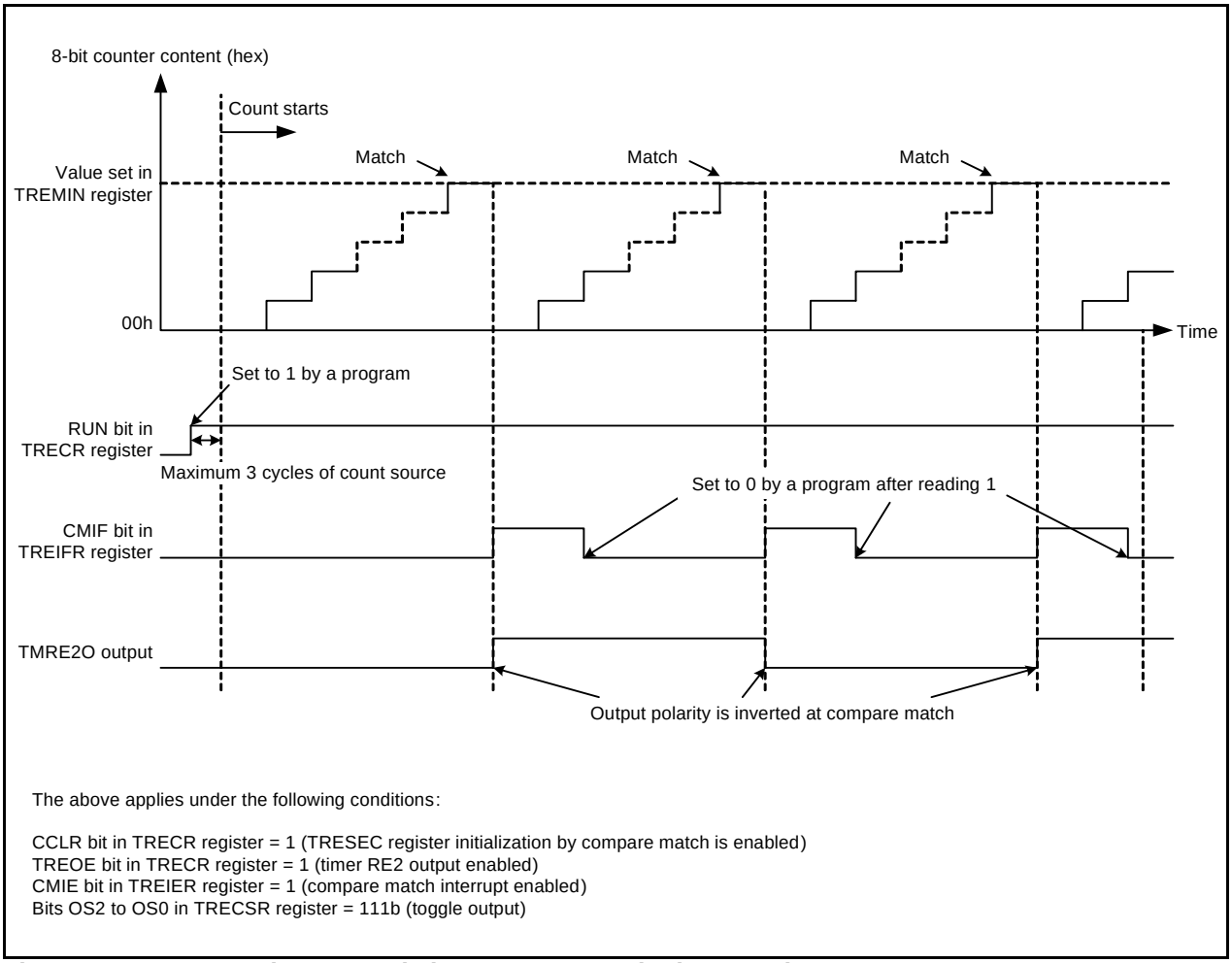


Figure 19.3 Operation Example in Compare Match Timer Mode

19.4 Interrupt Sources

The timer RE2 interrupt sources for are listed below:
• Compare match interrupt
• Overflow interrupt
Table 19.4 lists the Timer RE2 Interrupt Sources.
When using an interrupt, make necessary settings while the RUN bit in the TRECR register is 0 (count stops), and then set the RUN bit to 1 (count starts).

When the compare match timer overflows, the OVIF bit in the TREIFR register is set to 1 (interrupt requested). When the OVIE bit in the TRIER register is 1 (overflow interrupt enabled), an interrupt request is generated.
When the compare match timer is compared and matched, the CMIF bit in the TREIFR register is set to 1 (interrupt requested). When the CMIE bit in the TREIER register is 1 (compare match interrupt enabled), an interrupt request is generated.

Table 19.4 Timer RE2 Interrupt Sources

Source	Operating mode	Source Name	Interrupt Source	Interrupt Enable Bit
Overflow	Compare match timer mode	Overflow interrupt	When the compare match timer overflows.	OVIE
Compare match	Compare match timer mode	Compare match interrupt	When the compare match timer is compared and matched.	CMIE

19.5 Notes on Timer RE2

- When 0 (count stops) is written to the RUN bit in the TRECR register, the count is stopped after three cycles of the count source.
- When entering module standby, set the TREOE bit in the TRECR register to 0 (TMRE2O output disabled) and set the RUN bit to 0 (count stops), and then allow three or more cycles of the count source to elapse before setting the MSTTRE bit in the MSTCR3 register to 1 (standby).
- Switch bits OS0 to OS2 in the TRECSR register while the TREOE bit in the TRECR register is 0 (TMRE2O output disabled).
- Switching registers TREIFR and TREIER must be performed as follows:
  - Switch the CMIE bit in the TREIER register while the CMIF bit in the TREIFR register is 0 (no interrupt requested).
  - Switch the OVIE bit in the TREIER register while the OVIF bit in the TREIFR register is 0 (no interrupt requested).
- Set the RTCRST bit in the TRECR register while the OVIF bit is 0 (no interrupt requested) and the CMIF bit is 0 (no interrupt requested).

20. Serial Interface (UART0)

The serial interface consists of two channels: UART0_0 and UART0_1.
This chapter describes these channels as UART0 unless there are differences between them.

20.1 Overview

Each UART0 channel is independent and has a dedicated timer for generating a transfer clock. It supports two modes: Clock synchronous serial I/O mode and clock asynchronous serial I/O (UART) mode.
Table 20.1 lists the UART0 Specifications. Figure 20.1 shows the UART0 Block Diagram. Figure 20.2 shows the Transmit/Receive Unit Block Diagram. Table 20.2 lists the UART0 Pin Configuration. For details, refer to **Table 20.4 Clock Synchronous Serial I/O Mode Specifications** and **Table 20.6 Clock Asynchronous Serial I/O Mode Specifications**.

Table 20.1 UART0 Specifications

Item		Description
Clock synchronous serial I/O mode	Transfer data format	Transfer data length: 8 bits
	Transfer clock	• The CKDIR bit in the U0MR register is 0 (internal clock): fi/2 (n + 1) fi = f1, f8, or f32 n: Value set in the U0BRG register (00h to FFh) • The CKDIR bit in the U0MR register is 1 (external clock): fEXT (input from the CLK pin)
	Error detection	Overrun error
Clock asynchronous serial I/O mode	Transfer data format	• Character bits (transfer data): 7, 8, or 9 bits selectable • Start bit: 1 bit • Parity bit: Odd, even, or none selectable • Stop bit: 1 or 2 bits selectable
	Transfer clock	• The CKDIR bit in the U0MR register is 0 (internal clock): fj/16 (n + 1) fj = f1, f8, or f32 n: Value set in the U0BRG register (00h to FFh) • The CKDIR bit in the U0MR register is 1 (external clock): fEXT/16 (n + 1) fEXT (input from the CLK pin) n: Value set in the U0BRG register (00h to FFh)
	Error detection	Overrun error (1), framing error, parity error, error sum flag
Interrupt sources		Transmit buffer empty or transmission complete interrupt (multiplexed), and reception complete interrupt
Selectable function		The digital filter enabled or disabled can be selected by the DFE bit in the U0C0 register.

Note:
1. If an overrun error occurs, the IR bit in the U0RIC register is changed to 1 (interrupt requested).

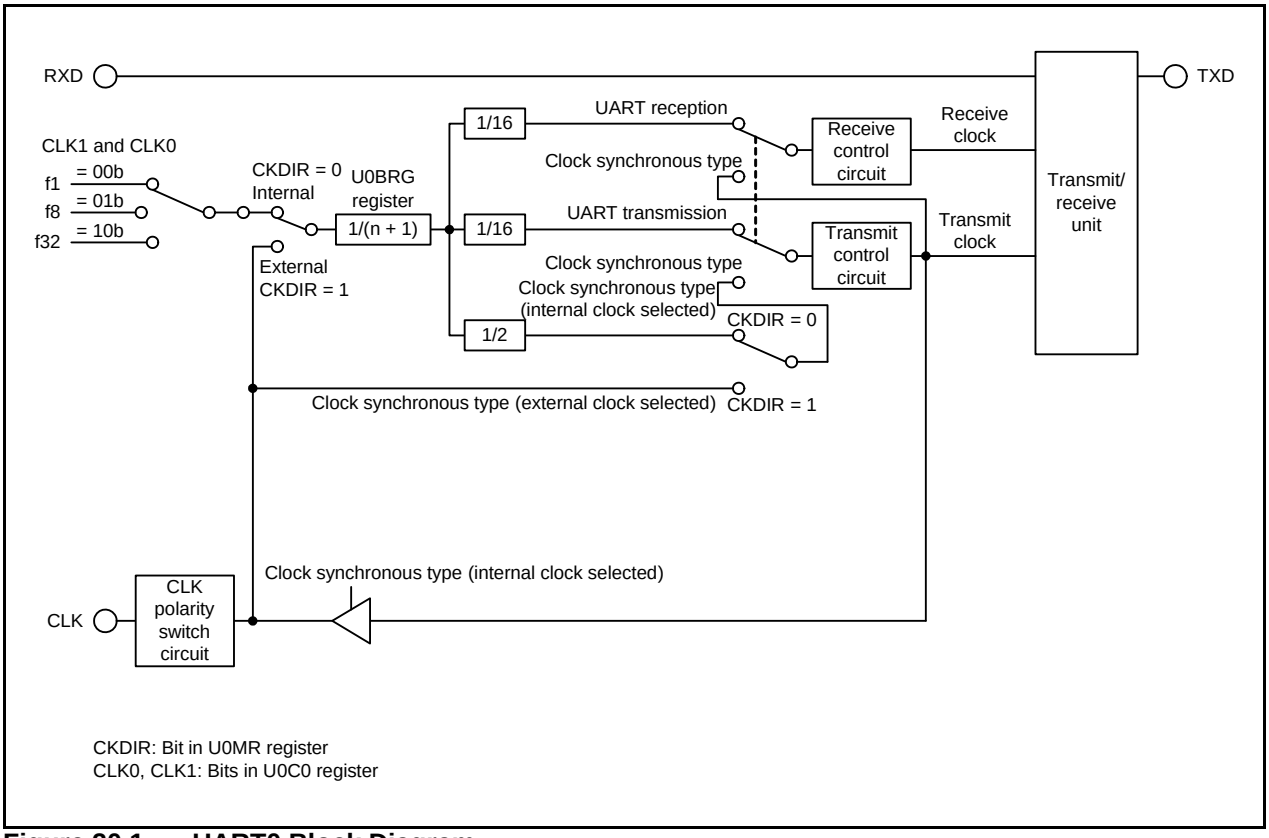
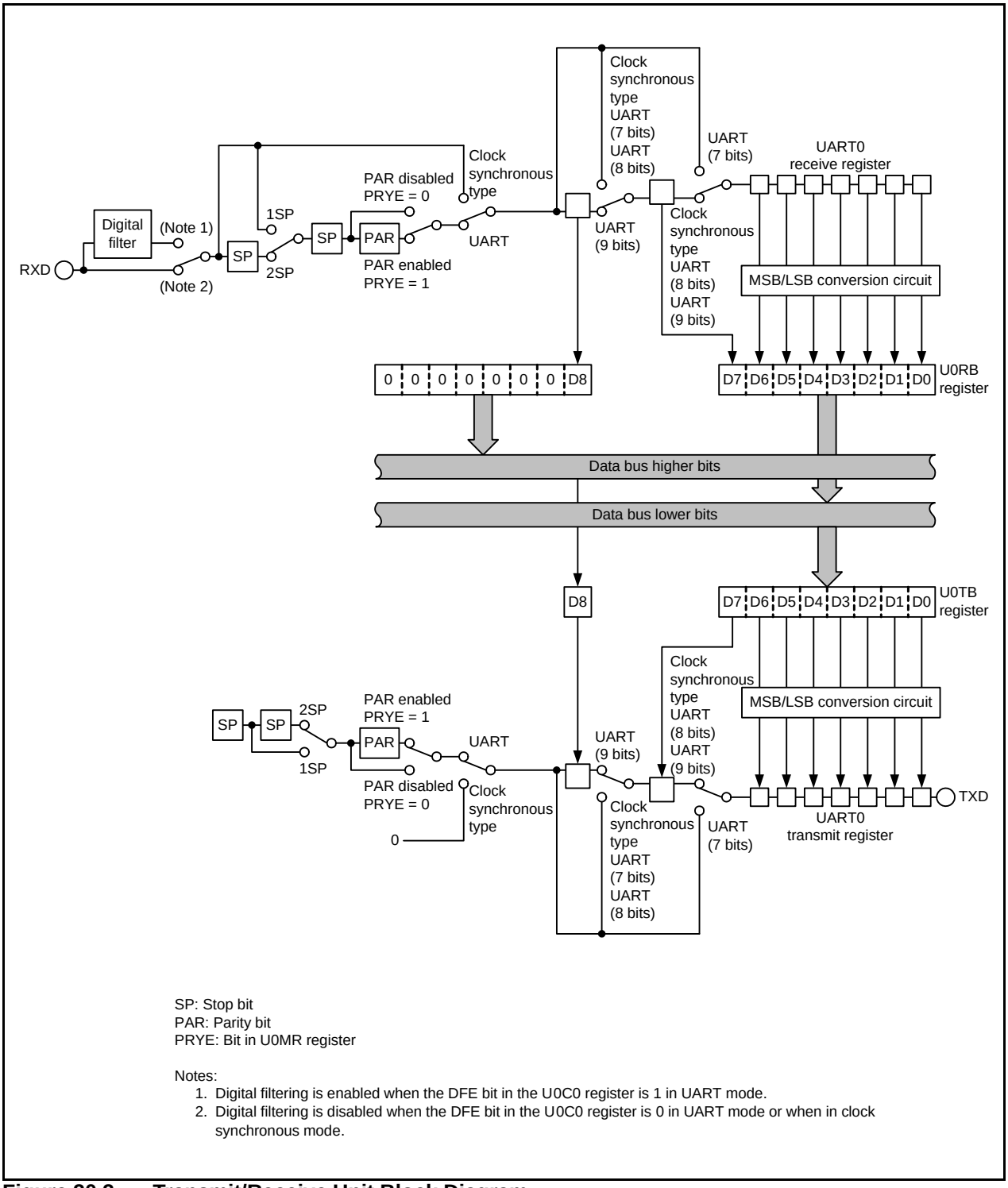


Figure 20.1 UART0 Block Diagram



SP: Stop bit
PAR: Parity bit
PRYE: Bit in U0MR register

Notes:
1. Digital filtering is enabled when the DFE bit in the U0C0 register is 1 in UART mode.
2. Digital filtering is disabled when the DFE bit in the U0C0 register is 0 in UART mode or when in clock synchronous mode.

Figure 20.2 Transmit/Receive Unit Block Diagram

Table 20.2 UART0 Pin Configuration

Pin Name	I/O	Function
CLK	Input/Output	Transfer clock input and output
RXD	Input	Serial data input
TXD	Output	Serial data output

20.2 Registers

Table 20.3 lists the UART0 Register Configuration.

Table 20.3 UART0 Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
UART0_0 Transmit/Receive Mode Register	U0MR_0	00h	00080h	8
UART0_0 Bit Rate Register	U0BRG_0	XXh	00081h	8
UART0_0 Transmit Buffer Register	U0TB_0	XXh	00082h	8 (1)
		XXh	00083h	8 (1)
UART0_0 Transmit/Receive Control Register 0	U0C0_0	00001000b	00084h	8
UART0_0 Transmit/Receive Control Register 1	U0C1_0	00000010b	00085h	8
UART0_0 Receive Buffer Register	U0RB_0	XXXXh	00086h	16 (1)
UART0_0 Interrupt Flag and Enable Register	U0IR_0	00h	00088h	8
UART0_1 Transmit/Receive Mode Register	U0MR_1	00h	00090h	8
UART0_1 Bit Rate Register	U0BRG_1	XXh	00091h	8
UART0_1 Transmit Buffer Register	U0TB_1	XXh	00092h	8 (1)
		XXh	00093h	8 (1)
UART0_1 Transmit/Receive Control Register 0	U0C0_1	00001000b	00094h	8
UART0_1 Transmit/Receive Control Register 1	U0C1_1	00000010b	00095h	8
UART0_1 Receive Buffer Register	U0RB_1	XXXXh	00096h	16 (1)
UART0_1 Interrupt Flag and Enable Register	U0IR_1	00h	00098h	8

X: Undefined

Note:

1. For details on access, refer to the description of the individual registers.

20.2.1 UART0 Transmit/Receive Mode Register (U0MR)

Address 00080h (U0MR_0), 00090h (U0MR_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	PRYE	PRY	STPS	CKDIR	SMD2	SMD1	SMD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SMD0	Serial I/O mode select bits (1, 3)	b2 b1 b0 0 0 0: Serial interface disabled (operation stopped) 0 0 1: Clock synchronous serial I/O mode 1 0 0: UART mode, transfer data 7 bits long 1 0 1: UART mode, transfer data 8 bits long 1 1 0: UART mode, transfer data 9 bits long Other than the above: Do not set.	R/W
b1	SMD1			R/W
b2	SMD2			R/W
b3	CKDIR	Internal/external clock select bit	0: Internal clock 1: External clock	R/W
b4	STPS	Stop bit length select bit	0: One stop bit 1: Two stop bits	R/W
b5	PRY	Odd/even parity select bit (2)	0: Odd parity 1: Even parity	R/W
b6	PRYE	Parity enable bit	0: Parity disabled 1: Parity enabled	R/W
b7	—	Reserved	Set to 0.	R/W

Notes:

1. When setting bits SMD2 to SMD0 in the U0MR register to 000b, set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
2. The PRY bit is enabled when the PRTYE bit is 1 (parity enabled).
3. When bits SMD2 to SMD0 are set to 001b (clock synchronous serial I/O mode), the error flags (bits FER, PER, and SUM) in the U0RB register are disabled. When these bits are read, the values are undefined.

20.2.2 UART0 Bit Rate Register (U0BRG)

Address 00081h (U0BRG_0), 00091h (U0BRG_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	If the set value is n, U0BRG divides the count source by n + 1.	00h to FFh	W

Write to the U0BRG register using the MOV instruction while transmission and reception are stopped.
Set bits CLK0 and CLK1 in the U0C0 register before writing to this register.
Do not write to the U0BRG register successively.

20.2.3 UART0 Transmit Buffer Register (U0TB)

Address 00082h (U0TB_0), 00092h (U0TB_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Function	R/W
b0	—	Transmit data (D8 to D0)	W
b1	—		W
b2	—		W
b3	—		W
b4	—		W
b5	—		W
b6	—		W
b7	—		W
b8	—		W
b9	—	Nothing is assigned. The write value must be 0. The read value is undefined.	—
b10	—		
b11	—		
b12	—		
b13	—		
b14	—		
b15	—		

If the transfer data is 9 bits long, write to the higher byte (b15 to b8) first and then the lower byte (b7 to b0) in 8-bit units.
Write to the U0TB register using the MOV instruction.

20.2.4 UART0 Transmit/Receive Control Register 0 (U0C0)

Address 00084h (U0C0_0), 00094h (U0C0_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	UFORM	CKPOL	NCH	DFE	TXEPT	—	CLK1	CLK0
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK0	U0BRG count source select bits (1)	b1 b0 0 0: f1 0 1: f8 1 0: f32 1 1: Do not set.	R/W
b1	CLK1			R/W
b2	—	Reserved	Set to 0.	R/W
b3	TXEPT	Transmit register empty flag	0: Data present in the transmit register (transmission in progress) 1: No data in the transmit register (transmission completed)	R
b4	DFE	RXD digital filter enable bit	0: Digital filter disabled 1: Digital filter enabled	R/W
b5	NCH	Data output select bit (2)	0: TXD pin is set to CMOS output 1: TXD pin is set to N-channel open-drain output	R/W
b6	CKPOL	CLK polarity select bit (3)	0: Transmit data is output at the falling edge and receive data is input at the rising edge of the transfer clock 1: Transmit data is output at the rising edge and receive data is input at the falling edge of the transfer clock	R/W
b7	UFORM	Transfer format select bit	0: LSB first 1: MSB first	R/W

Notes:
1. If the U0BRG count source is changed, set the U0BRG register again.
2. When UART0 is not used, set the NCH bit to 0 (TXD pin is set to CMOS output).
3. The CKPOL bit is enabled in clock synchronous serial I/O mode.

DFE Bit (RXD digital filter enable bit)

When the RXD digital filter is enabled, noise that is three or fewer pulses of the clock divided by the U0BRG register is reduced.

For details, refer to **20.3.2.3 RXD Digital Filter**.

This bit can be set in clock asynchronous serial I/O mode. In clock synchronous serial I/O mode, set this bit to 0 (digital filter disabled).

20.2.5 UART0 Transmit/Receive Control Register 1 (U0C1)

Address 00085h (U0C1_0), 00095h (U0C1_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	U0RRM	U0IRS	RI	RE	TI	TE
After Reset	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	TE	Transmission enable bit	0: Transmission disabled 1: Transmission enabled	R/W
b1	TI	Transmit buffer empty flag	0: Data present in the U0TB register 1: No data in the U0TB register	R
b2	RE	Reception enable bit	0: Reception disabled 1: Reception enabled	R/W
b3	RI	Reception complete flag (1)	0: No data in the U0RB register 1: Data present in the U0RB register	R
b4	U0IRS	UART0 transmit interrupt source select bit	0: Transmit buffer empty (TI = 1) 1: Transmission completed (TXEPT = 1)	R/W
b5	U0RRM	UART0 continuous receive mode enable bit (2)	0: Continuous receive mode disabled 1: Continuous receive mode enabled	R/W
b6	—	Reserved	Set to 0.	R/W
b7	—			

Notes:
1. The RI bit is set to 0 (no data in the U0RB register) when the U0RB register is read.
2. Can only be set in clock synchronous I/O mode. In clock asynchronous I/O mode, set this bit to 0 (continuous receive mode disabled).

20.2.6 UART0 Receive Buffer Register (U0RB)

Address 00086h (U0RB_0), 00096h (U0RB_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	SUM	PER	FER	OER	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	Receive data (D8 to D0) (2)		R
b1	—			R
b2	—			R
b3	—			R
b4	—			R
b5	—			R
b6	—			R
b7	—			R
b8	—			R
b9	—	Nothing is assigned. The write value must be 0. The read value is undefined.		—
b10	—			
b11	—			
b12	OER	Overrun error flag (1, 3)	0: No overrun error 1: Overrun error	R
b13	FER	Framing error flag (1, 3)	0: No framing error 1: Framing error	R
b14	PER	Parity error flag (1, 3)	0: No parity error 1: Parity error	R
b15	SUM	Error sum flag (1, 3)	0: No error 1: Error	R

Notes:
1. Bits OER, FER, PER, and SUM are set to 0 (no error) when bits SMD2 to SMD0 in the U0MR register are set to 000b (serial interface disabled) or the RE bit in the U0C1 register is set to 0 (reception disabled).
   The SUM bit is set to 0 (no error) when all of bits OER, FER, and PER are set to 0 (no error). In addition, bits FER and PER are set to 0 when the U0RB register is read.
   When setting bits SMD2 to SMD0 in the U0MR register to 000b, set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
2. Read the U0RB register when the RI bit in the U0C1 register is 1 (data present in the U0RB register).
3. These error flags are invalid when bits SMD2 to SMD0 in the U0MR register are set to 001b (clock synchronous serial I/O mode). When these bits are read, the values are undefined.

The U0RB register must be read in 16-bit units.

20.2.7 UART0 Interrupt Flag and Enable Register (U0IR)

Address 00088h (U0IR_0), 00098h (U0IR_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	U0TIE	U0RIE	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	U0RIE	UART0 receive interrupt enable bit	0: Receive interrupt disabled 1: Receive interrupt enabled	R/W
b3	U0TIE	UART0 transmit interrupt enable bit	0: Transmit interrupt disabled 1: Transmit interrupt enabled	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—	Reserved	Set to 0.	R/W
b7	—			

20.3 Operation

UART0 supports two modes: clock synchronous serial I/O mode and clock asynchronous serial I/O (UART) mode.

20.3.1 Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, transmission or reception is performed using a transfer clock.
Table 20.4 lists the Clock Synchronous Serial I/O Mode Specifications and Table 20.5 lists the Registers and Settings Used in Clock Synchronous Serial I/O Mode.

Table 20.4 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	Transfer data length: 8 bits
Transfer clock	• The CKDIR bit in the U0MR register is 0 (internal clock): fi/(2 (n + 1)) fi = f1, f8, or f32 n = Value set in the U0BRG register (00h to FFh) • The CKDIR bit in the U0MR register is 1 (external clock): fEXT (input from the CLK pin)
Transmission start conditions	To start transmission, the following requirements must be met: (1) • The TE bit in the U0C1 register is set to 1 (transmission enabled). • The TI bit in the U0C1 register is set to 0 (data present in the U0TB register).
Reception start conditions	To start reception, the following requirements must be met: (1) • The RE bit in the U0C1 register is set to 1 (reception enabled). • The TE bit in the U0C1 register is set to 1 (transmission enabled). • The TI bit in the U0C1 register is set to 0 (data present in the U0TB register).
Interrupt request generation timing	For transmission, one of the following can be selected. - The U0IRS bit in the U0C1 register is set to 0 (transmit buffer empty): When data is transferred from the U0TB register to the UART0 transmit register (at start of transmission). - The U0IRS bit in the U0C1 register is set to 1 (transmission completed): When data transmission from the UART0 transmit register is completed. For reception When data is transferred from the UART0 receive register to the U0RB register (at completion of reception).
Error detection	Overrun error (2) This error occurs if the next data reception is started and the 7th bit is received before the U0RB register is read.
Selectable functions	• CLK polarity selection The output and input timing of transfer data can be selected to be either the rising or the falling edge of the transfer clock. • LSB first or MSB first selection The start bit can be selected to be bit 0 or bit 7 when transmission and reception are started. • Continuous receive mode selection Reading the U0RB register enables reception at the same time.

Notes:
1. When an external clock is selected, the requirements must be met in either of the following states:
   • The external clock is set to high when the CKPOL bit in the U0C0 register is 0 (transmit data is output at the falling edge and receive data is input at the rising edge of the transfer clock).
   • The external clock is set to low when the CKPOL bit is 1 (transmit data is output at the rising edge and receive data is input at the falling edge of the transfer clock).
2. If an overrun error occurs, the receive data (b0 to b8) in the U0RB register is undefined.
   Also, the IR bit in the U0RIC register is changed to 1 (interrupt requested).

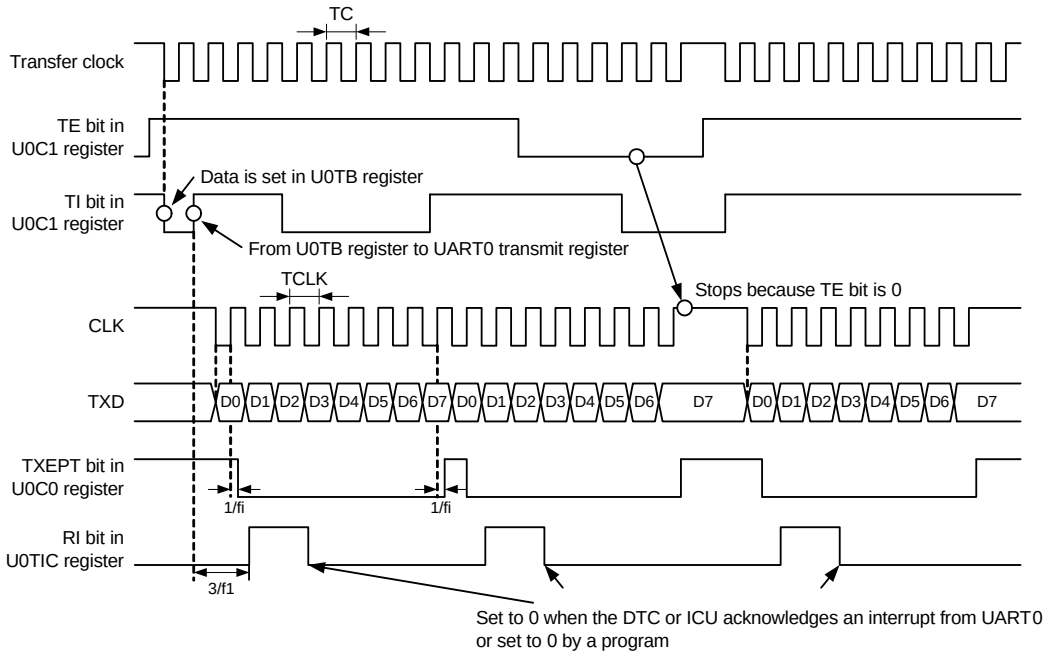
Table 20.5 Registers and Settings Used in Clock Synchronous Serial I/O Mode

Register	Bit	Function
U0TB	b0 to b7	Set transmit data.
U0RB	b0 to b7	Receive data can be read.
	OER	Overrun error flag
U0BRG	b0 to b7	Set the bit rate.
U0MR	SMD2 to SMD0	Set to 001b (clock synchronous serial I/O mode).
	CKDIR	Select an internal or external clock.
U0C0	CLK0, CLK1	Select the U0BRG count source (f1, f8, or f32).
	TXEPT	Transmit register empty flag
	NCH	Select the output type (CMOS or N-channel open-drain output) of the TXD pin.
	CKPOL	Select the polarity of the transfer clock.
	UFORM	Select LSB first or MSB first.
U0C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	U0IRS	Select the UART0 transmit interrupt source to be transmit buffer empty or transmission complete.
	U0RRM	Select continuous receive mode from disabled or enabled.

Note:
1. The write value must be 0 for all bits not listed in this table.

20.3.1.1 Operation Examples

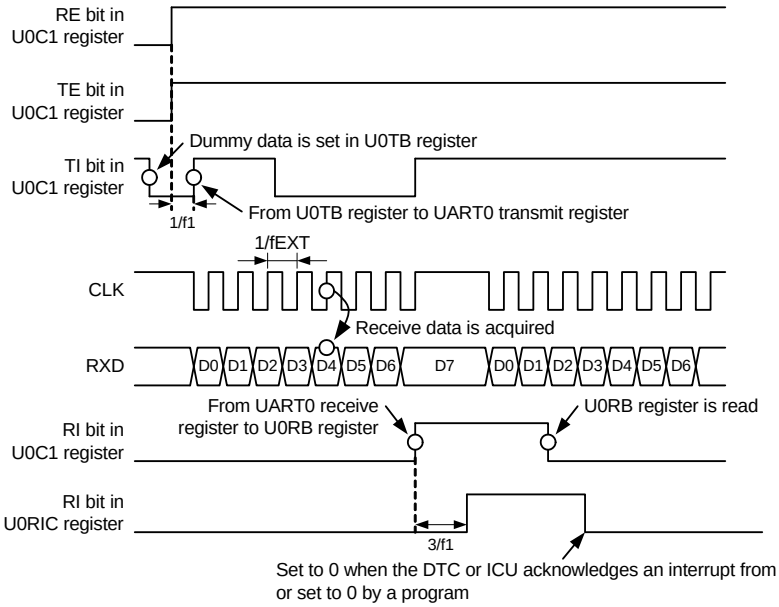
• Transmit timing example (internal clock selected)



The above diagram applies for the following settings:
- CKDIR bit in U0MR register = 0 (internal clock)
- CKPOL bit in U0C0 register = 0 (transmit data is output at the falling edge and receive data is input at the rising edge of the transfer clock)
- U0IRS bit in U0C1 register = 0 (transmit buffer empty)

TC = TCLK = 2 (n + 1)/fi
fi: Frequency of U0BRG count source (f1, f8, or f32)
n: Value set in U0BRG register

• Receive timing example (external clock selected)



fEXT: Frequency of external clock

The following requirements must be met when an input to the CLK0 pin is high before data reception:
- TE bit in U0C1 register → 1 (transmission enabled)
- RE bit in U0C1 register → 1 (reception enabled)
- Dummy data is written to U0TB register

The above diagram applies for the following settings:
- CKDIR bit in U0MR register = 1 (external clock)
- CKPOL bit in U0C0 register = 0 (transmit data is output at the falling edge and receive data is input at the rising edge of the transfer clock)

Figure 20.3 Transmit and Receive Timing in Clock Synchronous Serial I/O Mode

20.3.1.2 Polarity Select Function

Figure 20.4 shows the Transfer Clock Polarity.
The polarity of the transfer clock is selected with the CKPOL bit in the U0C0 register.

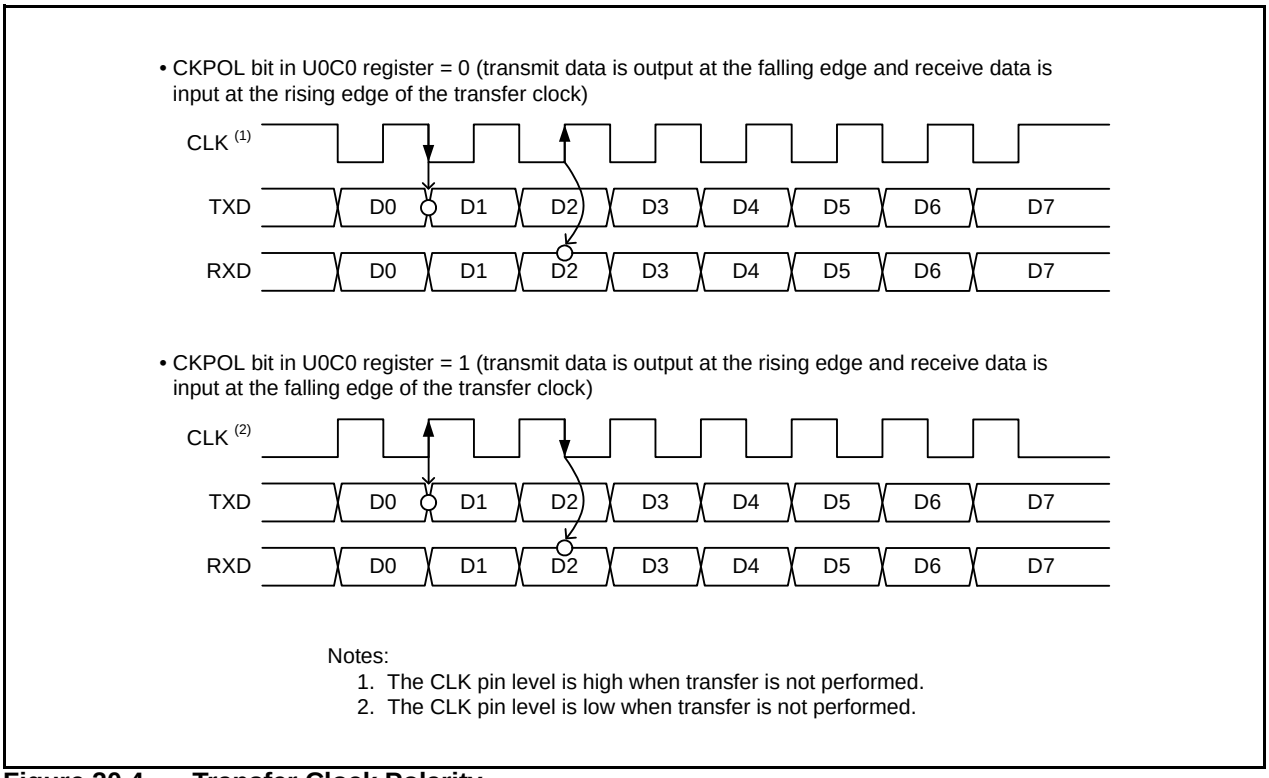


Figure 20.4 Transfer Clock Polarity

20.3.1.3 LSB First or MSB First Selection

Figure 20.5 shows the Transfer Format.
The transfer format is selected with the UFORM bit in the U0C0 register.

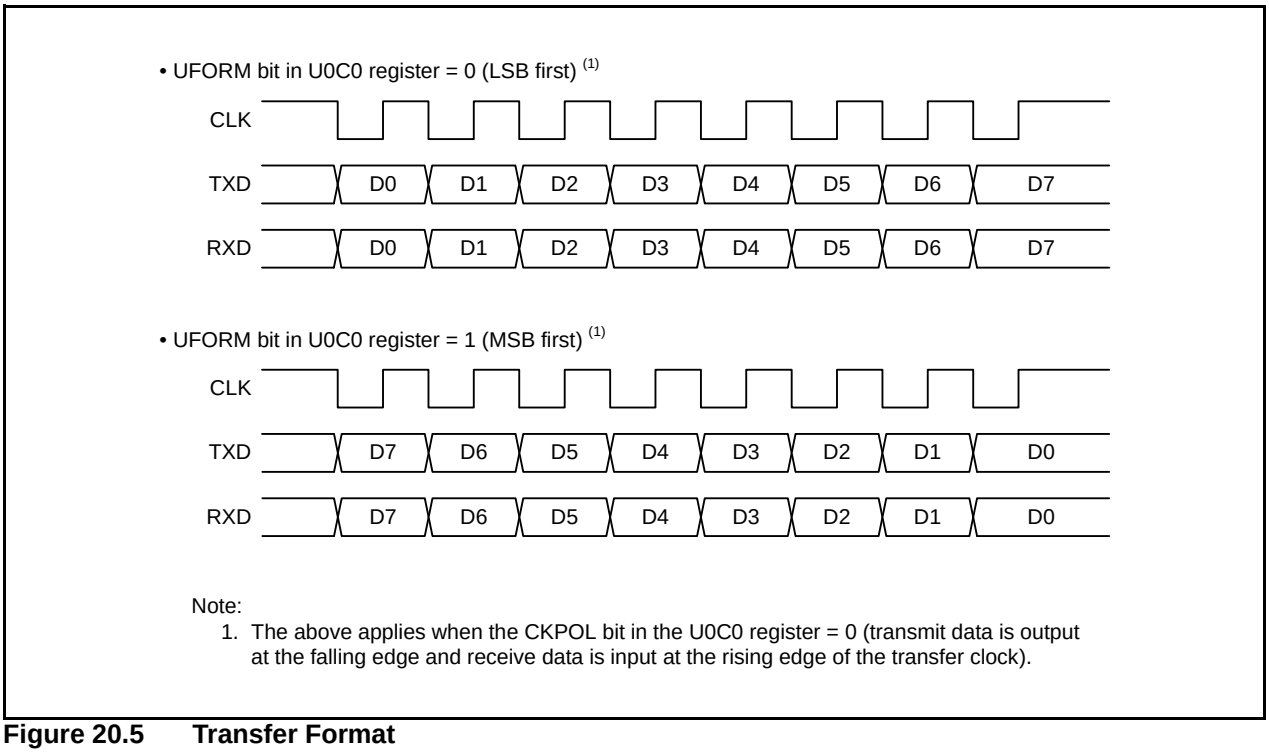


Figure 20.5 Transfer Format

20.3.1.4 Continuous Receive Mode

Continuous receive mode is selected by setting the U0RRM bit in the U0C1 register to 1 (continuous receive mode enabled). In this mode, reading the U0RB register sets the TI bit in the U0C1 register to 0 (data present in the U0TB register). When the U0RRM bit is 1, do not write dummy data to the U0TB register by a program.

20.3.1.5 Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in clock synchronous serial I/O mode, follow the procedure below:

(1) Set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the U0MR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the U0MR register to 001b (clock synchronous serial I/O mode).
(4) Set the TE bit in the U0C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

20.3.2 Clock Asynchronous Serial I/O (UART) Mode

In clock asynchronous serial I/O mode, transmission and reception are performed at an arbitrary bit rate and in an arbitrary format.
Table 20.6 lists the Clock Asynchronous Serial I/O Mode Specifications and Table 20.7 lists the Registers and Settings Used in Clock Asynchronous Serial I/O Mode.

Table 20.6 Clock Asynchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	• Character bits (transfer data): 7, 8 or 9 bits selectable • Start bit: 1 bit • Parity bit: Odd, even, or none selectable • Stop bits: 1 or 2 bits selectable
Transfer clock	• The CKDIR bit in the U0MR register is 0 (internal clock): fj/16 (n + 1) fj = f1, f8, or f32 n = Value set in the U0BRG register (00h to FFh) • The CKDIR bit in the U0MR register is 1 (external clock): fEXT/16 (n + 1) fEXT (input from the CLK pin) n = Value set in the U0BRG register (00h to FFh)
Transmission start conditions	To start transmission, the following requirements must be met: • The TE bit in the U0C1 register is set to 1 (transmission enabled). • The TI bit in the U0C1 register is set to 0 (data present in the U0TB register).
Reception start conditions	To start reception, the following requirements must be met: • The RE bit in the U0C1 register is set to 1 (reception enabled). • Start bit detection
Interrupt request generation timing	For transmission, one of the following can be selected. - The U0IRS bit in the U0C1 register is set to 0 (transmit buffer empty): When data is transferred from the U0TB register to the UART0 transmit register (at start of transmission). - The U0IRS bit in the U0C1 register is set to 1 (transmission completed): When data transmission from the UART0 transmit register is completed. For reception When data is transferred from the UART0 receive register to the U0RB register (at completion of reception).
Error detection	• Overrun error (1) This error occurs if the next data reception starts before the U0RB register is read and the bit prior to the last stop bit in the next data is received. • Framing error (2) This error occurs when the set number of stop bits is not detected. • Parity error (2) This error occurs when parity is enabled, and the number of 1's in the parity and character bits do not match the set number of 1's. • Error sum flag This flag is set to 1 if an overrun, framing, or parity error occurs.

Notes:
1. If an overrun error occurs, the receive data (b0 to b8) in the U0RB register is undefined.
   Also, the IR bit in the U0RIC register is changed to 1 (interrupt requested).
2. The framing error flag and the parity error flag are set to 1 when data is transferred from the UART0 receive register to the U0RB register.

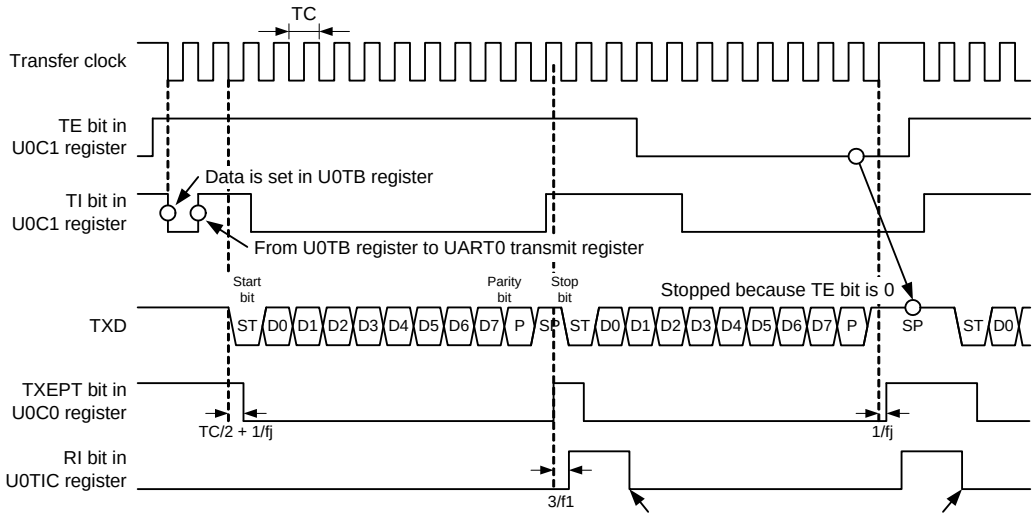
Table 20.7 Registers and Settings Used in Clock Asynchronous Serial I/O Mode

Register	Bit	Function
U0TB	b0 to b8	Set transmit data. (1)
U0RB	b0 to b8	Receive data can be read. (2)
	OER	Overrun error flag
	FER	Framing error flag
	PER	Parity error flag
	SUM	Error sum flag
U0BRG	b0 to b7	Set the bit rate.
U0MR	SMD2 to SMD0	Set to 100b when transfer data is 7 bits long. Set to 101b when transfer data is 8 bits long. Set to 110b when transfer data is 9 bits long.
	CKDIR	Select an internal or external clock.
	STPS	Select one or two stop bits.
	PRY, PRYE	Select whether parity is enabled and whether odd or even.
U0C0	CLK0 and CLK1	Select the U0BRG count source (f1, f8, or f32).
	TXEPT	Transmit register empty flag
	DFE	Select whether the digital filter function is enabled or disabled.
	NCH	Select the output type (CMOS or N-channel open-drain output) of the TXD pin.
	CKPOL	Set to 0 (transmit data is output at the falling edge and receive data is input at the rising edge of the transfer clock).
	UFORM	Select LSB first or MSB first when transfer data is 8 bits long. Set to 0 (LSB first) when transfer data is 7 bits or 9 bits long.
U0C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	U0IRS	Select the UART0 transmit interrupt source to be transmit buffer empty or transmission complete.
	U0RRM	Set to 0 (continuous receive mode disabled).

Notes:
1. The bits used are as follows:
   • Bits 0 to 6 when transfer data is 7 bits long
   • Bits 0 to 7 when transfer data is 8 bits long
   • Bits 0 to 8 when transfer data is 9 bits long
2. The contents of the following are undefined: Bits 7 and 8 when transfer data is 7 bits long, and bit 8 when transfer data is 8 bits long.

20.3.2.1 Operation Examples

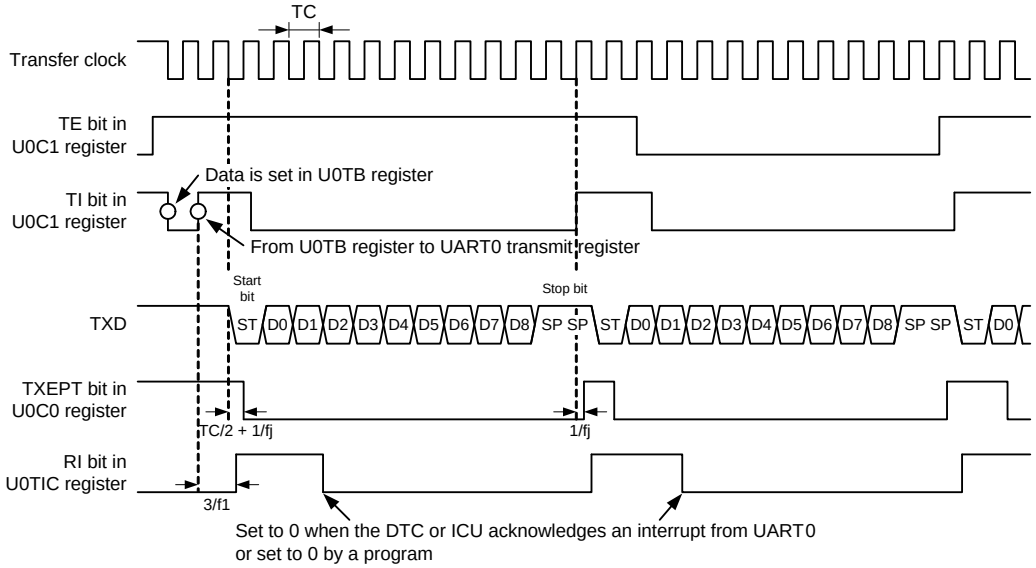
• When transfer data is 8 bits long (parity enabled, one stop bit)



The above diagram applies for the following settings:
- STPS bit in U0MR register = 0 (one stop bit)
- PRYE bit in U0MR register = 1 (parity enabled)
- U0IRS bit in U0C1 register = 1 (transmission completed)

TC = 16 (n + 1)/fj or 16 (n + 1)/fEXT
fj: Frequency of U0BRG count source (f1, f8, or f32)
fEXT: Frequency of U0BRG count source (external clock)
n: Value set in U0BRG register

• When transfer data is 9 bits long (parity disabled, two stop bits)



The above diagram applies for the following settings:
- STPS bit in U0MR register = 1 (two stop bits)
- PRYE bit in U0MR register = 0 (parity disabled)
- U0IRS bit in U0C1 register = 0 (transmit buffer empty)

TC = 16 (n + 1)/fj or 16 (n + 1)/fEXT
fj: Frequency of U0BRG count source (f1, f8, or f32)
fEXT: Frequency of U0BRG count source (external clock)
n: Value set in U0BRG register

Figure 20.6 Transmit Timing in Clock Asynchronous Serial I/O Mode

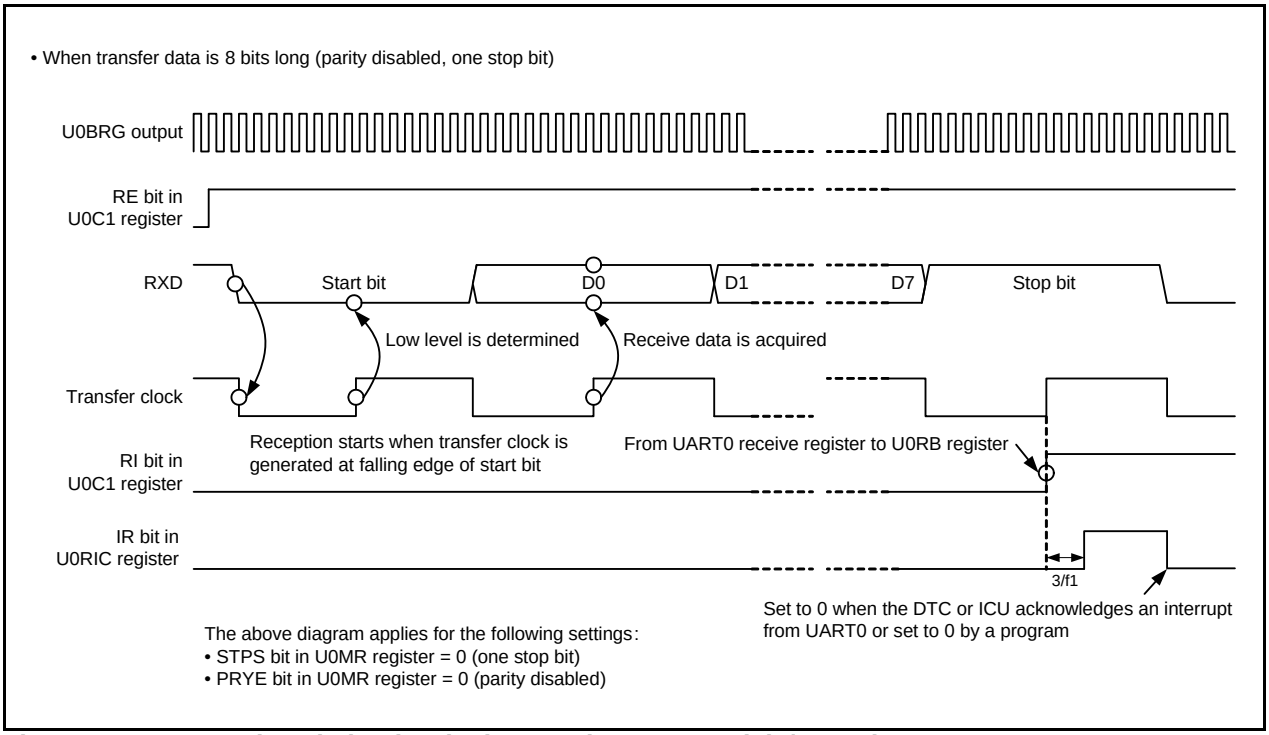


Figure 20.7 Receive Timing in Clock Asynchronous Serial I/O Mode

20.3.2.2 Bit Rate

In clock asynchronous serial I/O mode, the bit rate is obtained by dividing the frequency with the U0BRG register and further dividing it by 16.
The value to be set in the U0BRG register is calculated as follows:

• When an internal clock is selected

$$\text{Value set in U0BRG register} = \frac{\text{fj}}{\text{Bit rate} \times 16} - 1$$

fj: Frequency of U0BRG count source (f1, f8, or f32)

• When an external clock is selected

$$\text{Value set in U0BRG register} = \frac{\text{fEXT}}{\text{Bit rate} \times 16} - 1$$

fEXT: Frequency of U0BRG count source (external clock)

Table 20.8 Setting Example for Clock Asynchronous Serial I/O Mode (Internal Clock Selected)

Bit Rate (bps)	U0BRG Count Source	System Clock = 20 MHz			System Clock = 18.432 MHz (1)			System Clock = 8 MHz		
		Value Set in U0BRG Register	Actual Rate (bps)	Setting Error (%)	Value Set in U0BRG Register	Actual Rate (bps)	Setting Error (%)	Value Set in U0BRG Register	Actual Rate (bps)	Setting Error (%)
1200	f8	129 (81h)	1201.92	0.16	119 (77h)	1200.00	0.00	51 (33h)	1201.92	0.16
2400	f8	64 (40h)	2403.85	0.16	59 (3Bh)	2400.00	0.00	25 (19h)	2403.85	0.16
4800	f8	32 (20h)	4734.85	-1.36	29 (1Dh)	4800.00	0.00	12 (0Ch)	4807.69	0.16
9600	f1	129 (81h)	9615.38	0.16	119 (77h)	9600.00	0.00	51 (33h)	9615.38	0.16
14400	f1	86 (56h)	14367.82	-0.22	79 (4Fh)	14400.00	0.00	34 (22h)	14285.71	-0.79
19200	f1	64 (40h)	19230.77	0.16	59 (3Bh)	19200.00	0.00	25 (19h)	19230.77	0.16
28800	f1	42 (2Ah)	29069.77	0.94	39 (27h)	28800.00	0.00	16 (10h)	29411.76	2.12
38400	f1	32 (20h)	37878.79	-1.36	29 (1Dh)	38400.00	0.00	12 (0Ch)	38461.54	0.16
57600	f1	21 (15h)	56818.18	-1.36	19 (13h)	57600.00	0.00	8 (08h)	55555.56	-3.55
115200	f1	10 (0Ah)	113636.36	-1.36	9 (09h)	115200.00	0.00	—	—	—

Note:
1. This applies when the high-speed on-chip oscillator is selected as the system clock and bits FRA22 to FRA20 in the FRA2 register are set to 000b (divide-by-2 mode). For details on the accuracy of the high-speed on-chip oscillator, refer to **30. Electrical Characteristics**.

20.3.2.3 RXD Digital Filter

The RXD digital filter function is used to latch the RXD input signal internally after reducing noise when the DFE bit in the U0C0 register is 1 (digital filter enabled). The noise canceller consists of three cascaded latch circuits and a match detection circuit. When the RXD input is sampled on the clock divided by the U0BRG register and three latch outputs match, the level is passed forward to the next circuit. When they do not match, the previous level is retained.

That is, if the RXD input retains the same level for three clocks or more, it is recognized as a signal. If not, it is recognized as noise.

Figure 20.8 shows the RXD Digital Filter Block Diagram.

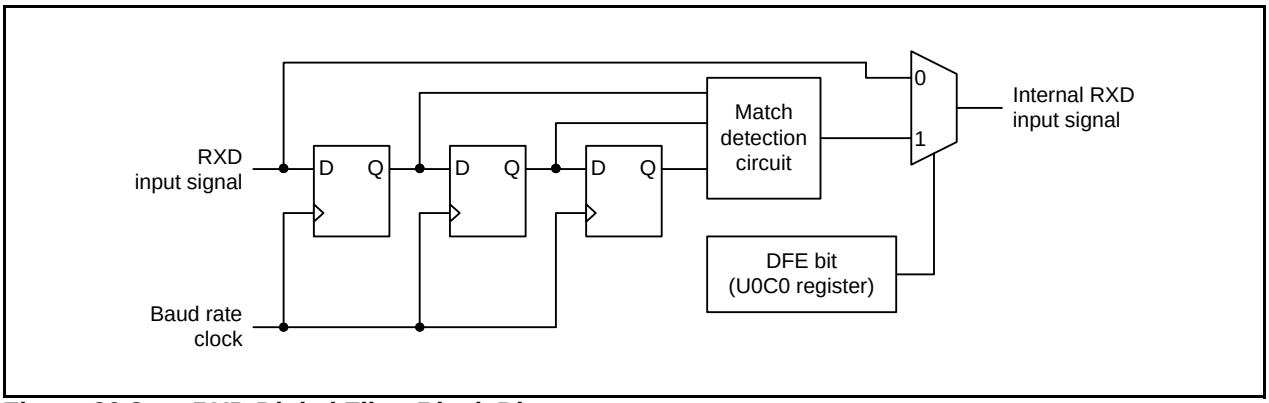


Figure 20.8 RXD Digital Filter Block Diagram

20.3.2.4 Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in UART mode, follow the procedure below:

(1) Set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the U0MR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the U0MR register to 100b (UART mode, transfer data 7 bits long), 101b (UART mode, transfer data 8 bits long), or 110b (UART mode, transfer data 9 bits long).
(4) Set the TE bit in the U0C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

20.4 UART0 Interrupt

Table 20.9 lists the Interrupt Requests.

Table 20.9 Interrupt Requests

Interrupt Request	Abbreviation	Interrupt Generation Condition
Transmit buffer empty	TEI	• The U0IRS bit in the U0C1 register is set to 0 (transmit buffer empty) • The TI bit is set to 1 (no data in the U0TB register) • Bits ILVL3 to ILVL0 in the U0TIC register are set to a value other than 0000b • The U0TIE bit in the U0IR register is set to 1
Transmission complete	TXI	• The U0IRS bit in the U0C1 register is set to 1 (transmission completed) • The TXEPT bit is set to 1 (no data in the transmit register) • Bits ILVL3 to ILVL0 in the U0TIC register are set to a value other than 0000b • The U0TIE bit in the U0IR register is set to 1
Reception complete	RXI	• The RI bit in the U0C1 register is set to 1 (data present in the U0RB register) • Bits ILVL3 to ILVL0 in the U0RIC register are set to a value other than 0000b • The U0RIE bit in the U0IR register is set to 1

U0TIE, U0RIE: Bits in U0IR register

Note:

1. The CPU executes interrupt exception handling when the interrupt generation conditions are met and the I flag in the FLG register is 1.

20.5 Notes on Serial Interface (UART0)

20.5.1 Common to All Operating Modes

20.5.1.1 Register Access

The settings of the following registers can only be changed when the serial interface is disabled. Do not change these settings when the serial interface is enabled.
• Registers U0MR_0 and U0MR_1: CKDIR bit
• Registers U0C0_0 and U0C0_1: Bits CLK0 and CLK1
• Registers U0IR_0 and U0IR_1: Bits U0RIE and U0TIE

The settings of the following registers can only be changed while transmission/reception is stopped. Do not change these settings during transmission/reception.
• Registers U0MR_0 and U0MR_1: Bits SMD0 to SMD2, STPS, PRY, and PRYE
• Registers U0BRG_0 and U0BRG_1: Bits b0 to b7
• Registers U0C0_0 and U0C0_1: Bits DFE, NCH, CKPOL, and UFORM
• Registers U0C1_0 and U0C1_1: Bits U0IRS and U0RRM

Regardless of clock synchronous I/O mode or clock asynchronous I/O mode, read the U0RB register in 16-bit units.
When the higher byte (b15 to b8) in the U0RB register is read, bits FER and PER in the U0RB register are set to 0 (no framing error, no parity error). Also, the RI bit in the U0C1 register is set to 1 (no data in the U0RB register). To check for receive errors, use the data read from the U0RB register.

• Program example for reading the receive buffer register

```
MOV.W   0086H, R0       ; Read the U0RB register
```

When the transfer data is 9 bits long in clock asynchronous I/O mode, write to the higher byte (b15 to b8) first and then the lower byte (b7 to b0) in 8-bit units.

• Program example for writing to the transmit buffer register

```
MOV.B   #XXH, 0083H     ; Write to the higher byte (b15 to b8) in the U0TB register
MOV.B   #XXH, 0082H     ; Write to the lower byte (b7 to b0) in the U0TB register
```

• Do not set the MSTUART_0 or MSTUART_1 bit in the MSTCR0 register to 1 (standby) during communication. When setting the module to the standby state, confirm whether communication has completed. After communication has completed, set bits TE and RE in the U0C1 register to 0 (communication disabled) before setting the module to the standby state. After the module standby state is cleared, the initial settings for communication must be set up again.

20.5.1.2 N-Channel Open-Drain Control Bit

When UART0 is not used, set the NCH bit in the U0C0 register to 0 (TXD pin is set to CMOS output).

21. Serial Interface (UART2)

21.1 Overview

UART2 has a dedicated timer for generating a transfer clock.
Tables 21.1 to 21.3 list the UART2 Specifications, Figure 21.1 shows the UART2 Block Diagram.
UART2 supports the following modes:

- Clock synchronous serial I/O mode (SIO mode)
- Clock asynchronous serial I/O mode (UART mode)
- Serial mode 3 (IE mode)
- Multiprocessor communication mode

Table 21.1 UART2 Specifications (1)

	Item	Specification
Clock synchronous serial I/O mode	Pins used	• TXD2: Transmit data (output) • RXD2: Receive data (input) • CLK2: Transfer clock (master: output, slave: input) • $\overline{\text{CTS2}}$: Transmit request signal (input) • $\overline{\text{RTS2}}$: Receive request signal (output)
	Analog noise filter	15 ns noise filter for CLK2 and RXD2 input
	Transfer data format	Transfer data length: 8 bits
	Transfer clock	• The CKDIR bit in the U2MR register is set to 0 (internal clock): fj/(2(n + 1)) fj = f1, f8, or f32 n = Value set in the U2BRG register (00h to FFh) • The CKDIR bit is set to 1 (external clock): Input from the CLK2 pin
	Transmit/receive control	$\overline{\text{CTS}}$ function, $\overline{\text{RTS}}$ function, or $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function disabled selectable
	Transmission start conditions	To start transmission, the following requirements must be met: (1) • The TE bit in the U2C1 register is set to 1 (transmission enabled). • The TI bit in the U2C1 register is set to 0 (data present in the U2TB register). • If the $\overline{\text{CTS}}$ function is selected, input to the $\overline{\text{CTS2}}$ pin is low.
	Reception start conditions	To start reception, the following requirements must be met: (1) • The RE bit in the U2C1 register is set to 1 (reception enabled). • The TE bit in the U2C1 register is set to 1 (transmission enabled). • The TI bit in the U2C1 register is set to 0 (data present in the U2TB register). • If the $\overline{\text{CTS}}$ function is selected, input to the $\overline{\text{CTS2}}$ pin is low.
	Interrupt request generation timing	For transmission, one of the following conditions can be selected. -The U2IRS bit in the U2C1 register is set to 0 (transmit buffer empty): When data is transferred from the U2TB register to the UART2 transmit register (at start of transmission). -The U2IRS bit is set to 1 (transmission completed): When data transmission from the UART2 transmit register is completed. For reception When data is transferred from the UART2 receive register to the U2RB register (at completion of reception).
	Error detection	• Overrun error (2) This error occurs if the serial interface starts receiving the next unit of data before reading the U2RB register and receives the 7th bit of the next unit of data.
	Selectable functions	• CLK polarity selection Transfer data I/O can be selected to occur synchronously with the rising or falling edge of the transfer clock. • LSB first/MSB first selection Whether transmitting or receiving data begins with bit 0 or begins with bit 7 can be selected. • Continuous receive mode selection A function that enables reception immediately upon reading the U2RB register can be selected. • Serial data logic switching This function inverts the logic value of the transmit/receive data.

Notes:
1. When an external clock is selected, the requirements must be met in either of the following states:
   - The external clock is held high when the CKPOL bit in the U2C0 register is set to 0 (transmit data is output at the falling edge and receive data is input at the rising edge of the transfer clock)
   - The external clock is held low when the CKPOL bit is set to 1 (transmit data is output at the rising edge and receive data is input at the falling edge of the transfer clock)
2. If an overrun error occurs, the receive data in the U2RB register will not be updated (the previous data will be read). Also, the IR bit in the U2RIC register is changed to 1 (interrupt requested).

Table 21.2 UART2 Specifications (2)

	Item	Specification
Clock asynchronous serial I/O mode (UART mode)	Pins used	• TXD2: Transmit data (output) • RXD2: Receive data (input) • CTS2: Transmit request signal (input) • RTS2: Receive request signal (output) • CLK2: Count source clock (input when external clock is selected)
	Analog noise filter	15 ns noise filter for CLK2 and RXD2 input
	Transfer data format	• Character bits (transfer data): 7, 8, or 9 bits selectable • Start bits: 1 bit • Parity bit: Odd, even, or none selectable • Stop bits: 1 or 2 bits selectable
	Transfer clock	• The CKDIR bit in the U2MR register is set to 0 (internal clock): fj/(16(n + 1)) fj = f1, f8, or f32 n = Value set in the U2BRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): fEXT/(16(n + 1)) fEXT: Input from CLK2 pin n = Value set in the U2BRG register (00h to FFh)
	Transmit/receive control	$\overline{\text{CTS}}$ function, $\overline{\text{RTS}}$ function, or $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function disabled selectable
	Transmission start conditions	To start transmission, the following requirements must be met: • The TE bit in the U2C1 register is set to 1 (transmission enabled). • The TI bit in the U2C1 register is set to 0 (data present in the U2TB register). • If the $\overline{\text{CTS}}$ function is selected, input to the $\overline{\text{CTS2}}$ pin is low.
	Reception start conditions	To start reception, the following requirements must be met: • The RE bit in the U2C1 register is set to 1 (reception enabled). • Start bit detection
	Interrupt request generation timing	For transmission, one of the following conditions can be selected. -The U2IRS bit in the U2C1 register is set to 0 (transmit buffer empty): When data is transferred from the U2TB register to the UART2 transmit register (at start of transmission). -The U2IRS bit in the U2C1 register is set to 1 (transmission completed): When data transmission from the UART2 transmit register is completed. For reception When data is transferred from the UART2 receive register to the U2RB register (at completion of reception).
	Error detection	• Overrun error (1) This error occurs if the next data reception starts before the U2RB register is read and the bit prior to the last stop bit in the next data is received. • Framing error (2) This error occurs when the set number of stop bits is not detected. • Parity error (2) This error occurs if parity is enabled and the number of 1's in the parity and character bits does not match the set number of 1's. • Error sum flag This flag is set to 1 if an overrun, framing, or parity error occurs.

Notes:
1. If an overrun error occurs, the receive data in the U2RB register will not be updated (the previous data will be read). Also, the IR bit in the U2RIC register is changed to 1 (interrupt requested).
2. The framing error flag and the parity error flag are set to 1 when data is transferred from the UART2 receive register to the U2RB register.

Table 21.3 UART2 Specifications (3)

	Item	Specification
Clock asynchronous serial I/O mode (UART mode)	Selectable functions	• LSB first/MSB first selection Whether transmitting or receiving data begins with bit 0 or begins with bit 7 can be selected. • Serial data logic switching This function inverts the logic of the transmit/receive data. The start and stop bits are not inverted. • TXD and RXD I/O polarity switching This function inverts the polarities of the TXD pin output and RXD pin input. The logic levels of all I/O data are inverted. • RXD2 digital filter selection The RXD2 input signal can be enabled or disabled.
Special mode 3 (IE mode)	Pins used	• TXD2: Transmit data (output) • RXD2: Receive data (input) • CLK2: UART2 operating clock (input when external clock is selected)
	Transfer data format	• Character bits (transfer data): 9 bits • Start bits: 1 bit • Parity bit: No • Stop bits: 1 bit
	Interrupt request generation timing	• For transmission Interrupt generation timing during transmission - The U2IRS bit in the U2C1 register is set to 0 (transmit buffer empty) When data is transferred from the U2TB register to the UART2 transmit register (at start of transmission). - The U2IRS bit in the U2C1 register is set to 1 (transmission completed) When data transmission from the UART2 transmit register is completed. • For reception When data is transferred from the UART2 receive register to the U2RB register (at completion of reception). • Bus collision generation timing - The ABSCS bit in the U2SMR register is set to 0: When a bus collision is detected at the rising of the transfer clock. - The ABSCS bit in the U2SMR register is set to 1: When a bus collision is detected at an underflow signal of timer RB2.
	Selectable function	• TXD2 and RXD2 I/O polarity switching This function inverts the TXD2 pin output and RXD2 pin input. The levels of all I/O data are inverted.
	Specifications other than the above are identical to clock asynchronous serial I/O mode specifications.	
Multiprocessor communication mode	Pins used	• TXD2: Transmit data (output) • RXD2: Receive data (input) • CLK2: UART2 operating clock (input when external clock is selected)
	Transfer data format	• Character bits (transfer data): 7 or 8 bits selectable • Multiprocessor bits: 1 bit • Start bits: 1 bit • Parity bit: No • Stop bits: 1 or 2 bits selectable
	Selectable function	• RXD2 digital filter selection The RXD2 input signal can be enabled or disabled.
	Specifications other than the above are identical to clock asynchronous serial I/O mode specifications.	

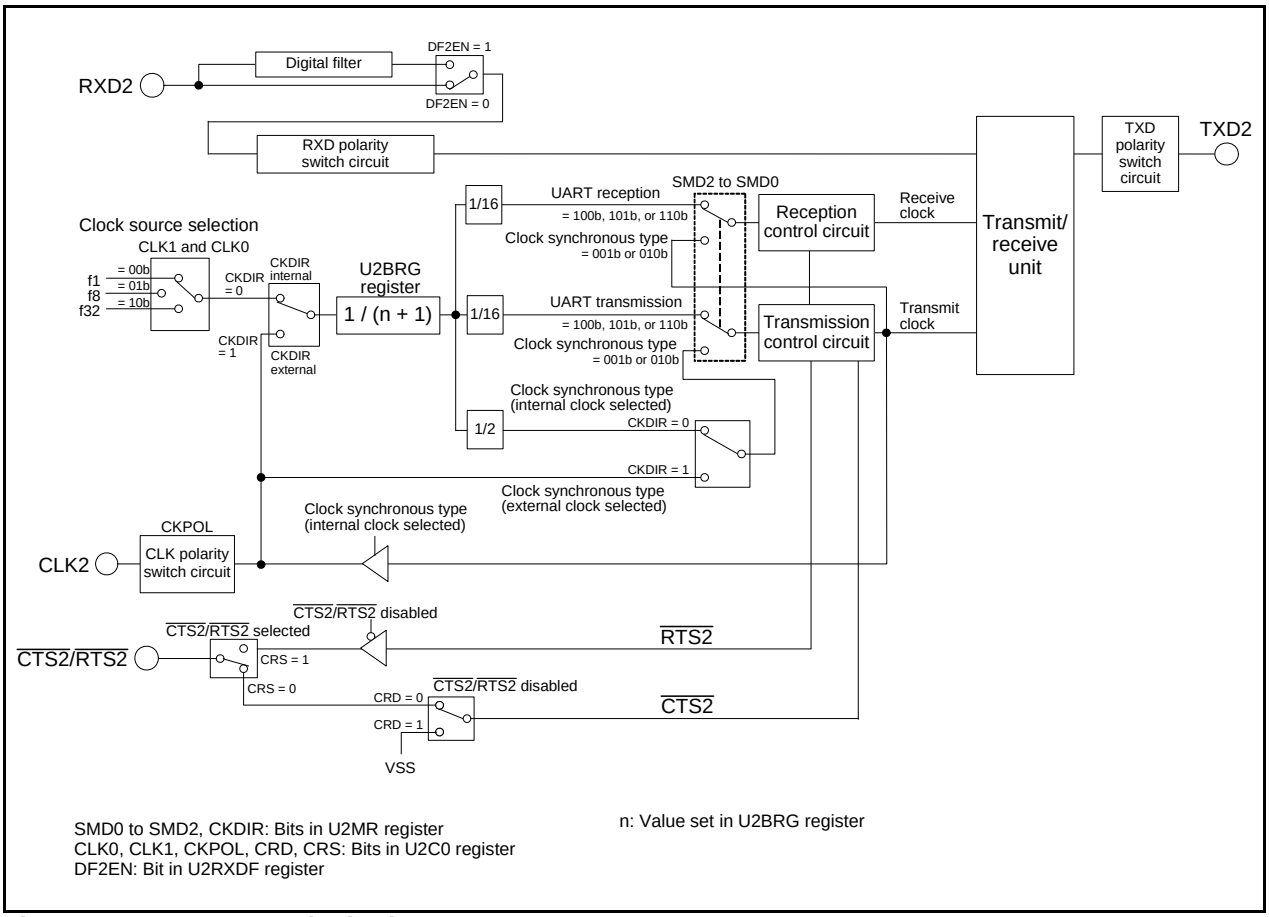


Figure 21.1 UART2 Block Diagram

Table 21.4 UART2 Pin Configuration

Pin Name	I/O	Function
TXD2	Output	Serial data output
RXD2	Input	Serial data input
CLK2	Input/Output	Transfer clock input/output
$\overline{\text{CTS2}}$	Input	Transmission control input
$\overline{\text{RTS2}}$	Output	Reception control input

21.2 Registers

Table 21.5 lists the UART2 Register Configuration.

Table 21.5 UART2 Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
UART2 Transmit/Receive Mode Register	U2MR	00h	000C0h	8
UART2 Bit Rate Register	U2BRG	00h	000C1h	8
UART2 Transmit Buffer Register	U2TB	00h	000C2h	8 or 16
		00h	000C3h	
UART2 Transmit/Receive Control Register 0	U2C0	00001000b	000C4h	8
UART2 Transmit/Receive Control Register 1	U2C1	00000010b	000C5h	8
UART2 Receive Buffer Register	U2RB	0000h	000C6h	16
UART2 Digital Filter Function Select Register	U2RXDF	00h	000C8h	8
UART2 Special Mode Register 5	U2SMR5	00h	000D0h	8
UART2 Special Mode Register 3	U2SMR3	00h	000D5h	8
UART2 Special Mode Register	U2SMR	00h	000D7h	8

21.2.1 UART2 Transmit/Receive Mode Register (U2MR)

Address 000C0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOPOL	PRYE	PRY	STPS	CKDIR	SMD2	SMD1	SMD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SMD0	Serial I/O mode select bits (1, 2, 8)	b2 b1 b0 0 0 0: Serial interface disabled 0 0 1: Clock synchronous serial I/O mode 0 1 0: Do not set. 1 0 0: UART mode, transfer data 7 bits long 1 0 1: UART mode, transfer data 8 bits long 1 1 0: UART mode, transfer data 9 bits long Other than the above: Do not set.	R/W
b1	SMD1			R/W
b2	SMD2			R/W
b3	CKDIR	Internal/external clock select bit (3)	0: Internal clock 1: External clock	R/W
b4	STPS	Stop bit length select bit (4)	0: One stop bit 1: Two stop bits	R/W
b5	PRY	Odd/even parity select bit (5)	0: Odd parity 1: Even parity	R/W
b6	PRYE	Parity enable bit (6)	0: Parity disabled 1: Parity enabled	R/W
b7	IOPOL	TXD and RXD I/O polarity switch bit (7)	0: Not inverted 1: Inverted	R/W

Notes:
1. In IE mode, set to 110b (UART mode transfer data length: 9 bits). In multiprocessor communication mode, set to 100b (UART mode transfer data length: 7 bits) or 101b (UART mode transfer data length: 8 bits).
2. When setting bits SMD2 to SMD0 to 000b, set the TE bit in the U2C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
3. When using as master in SIO mode, set to 0 (internal clock). When using as slave in SIO mode, set to 1 (external clock).
4. Can only be selected in UART mode and multiprocessor communication mode. In other modes, set to 0 (one stop bit).
5. Can only be selected in UART mode. In other modes, because the PRYE bit is set to 0 (no parity bit), the value set to this bit is invalid.
6. Can only be selected in UART mode. In other modes, set to 0 (no parity bit).
   If the PRYE bit is set to 1, the following operation occurs.
   During transmission: Parity bit is added after transmit data.
   During reception: Parity bit causes error checking to be performed.
7. Can only be set in UART mode and IE mode. In other modes, set to 0 (not inverted). If the IOPOL bit is set to 1 (inverted), the polarities of the transmit data and receive data are inverted.
   (Start, stop, and parity bits are included in the inversion.)
8. When bits SMD2 to SMD0 are set to 001b (clock synchronous serial I/O mode), the error flags (bits FER, PER, and SUM) in the U2RB register are disabled. When these bits are read, the values are undefined.

21.2.2 UART2 Bit Rate Register (U2BRG)

Address 000C1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b7 to b0	If the setting value is n, U2BRG divides the count source by n + 1.	00h to FFh	W

Write to the U2BRG register using the MOV instruction while transmission and reception are stopped.
Set bits CLK0 and CLK1 in the U2C0 register before writing to the U2BRG register.

21.2.3 UART2 Transmit Buffer Register (U2TB)

Address 000C2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	MPTB
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
b0	—	Transmit data (D7 to D0)	W
b1	—		W
b2	—		W
b3	—		W
b4	—		W
b5	—		W
b6	—		W
b7	—		W
b8	MPTB (1)	[When the multiprocessor communication function is not used] Transmit data (D8) [When the multiprocessor communication function is used] • To transfer an ID, set the MPTB bit to 1. • To transfer data, set the MPTB bit to 0.	W
b9	—	Nothing is assigned. The write value must be 0. The read value is 0.	—
b10	—		
b11	—		
b12	—		
b13	—		
b14	—		
b15	—		

Note:
1. When 8-bit access is performed when the data transfer length is 9 bits in UART mode or when using the multiprocessor communication function, set b0 to b7 after the MPTB bit is set.

Write to the U2TB register using the MOV instruction.

21.2.4 UART2 Transmit/Receive Control Register 0 (U2C0)

Address 000C4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	UFORM	CKPOL	NCH	CRD	TXEPT	CRS	CLK1	CLK0
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK0	U2BRG count source select bits (1)	b1 b0 0 0: f1 0 1: f8 1 0: f32 1 1: Do not set.	R/W
b1	CLK1			R/W
b2	CRS	$\overline{CTS}$/$\overline{RTS}$ function select bit (2)	Enabled when CRD = 0 0: $\overline{CTS}$ function selected 1: $\overline{RTS}$ function selected	R/W
b3	TXEPT	Transmit register empty flag	0: Data present in the transmit register (transmission in progress) 1: No data in the transmit register (transmission completed)	R
b4	CRD	$\overline{CTS}$/$\overline{RTS}$ disable bit (3)	0: $\overline{CTS}$/$\overline{RTS}$ function enabled 1: $\overline{CTS}$/$\overline{RTS}$ function disabled	R/W
b5	NCH	Data output select bit (4)	0: The TXD2 pin is set to CMOS output 1: The TXD2 pin is set to N-channel open-drain output	R/W
b6	CKPOL	CLK polarity select bit (5)	0: Transmit data is output at the falling edge and receive data is input at the rising edge of the transfer clock 1: Transmit data is output at the rising edge and receive data is input at the falling edge of the transfer clock	R/W
b7	UFORM	Transfer format select bit (6)	0: LSB first 1: MSB first	R/W

Notes:
1. If bits CLK0 and CLK1 are changed, set the U2BRG register again.
2. Can only be selected in SIO/UART mode. In other modes, because the CRD bit is set to 1 ($\overline{CTS}$/$\overline{RTS}$ function disabled), the value set to this bit is invalid.
3. Can only be set in SIO/UART mode. In other modes, set to 1 ($\overline{CTS}$/$\overline{RTS}$ function disabled).
4. When UART2 is not used, set the NCH bit to 0 (the TXD2 pin is set to CMOS output).
5. Can only be set in SIO mode. In other modes, set to 0 (transmit data is output at the falling edge and receive data is input at the rising edge of the transfer clock).
6. Can only be selected while data transfer length is 8 bits in SIO/UART mode. In the mode other than SIO/UART mode, set to 0 (LSB first).

21.2.5 UART2 Transmit/Receive Control Register 1 (U2C1)

Address 000C5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	U2LCH	U2RRM	U2IRS	RI	RE	TI	TE
After Reset	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	TE	Transmission enable bit	0: Transmission disabled 1: Transmission enabled	R/W
b1	TI	Transmit buffer empty flag	0: Data present in the U2TB register 1: No data in the U2TB register	R
b2	RE	Reception enable bit	0: Reception disabled 1: Reception enabled	R/W
b3	RI	Reception complete flag (1)	0: No data in the U2RB register 1: Data present in the U2RB register	R
b4	U2IRS	UART2 transmit interrupt source select bit	0: Transmit buffer empty (TI = 1) 1: Transmission completed (TXEPT = 1)	R/W
b5	U2RRM	UART2 continuous receive mode enable bit (2)	0: Continuous receive mode disabled 1: Continuous receive mode enabled	R/W
b6	U2LCH	Data logic select bit (3)	0: Not inverted 1: Inverted	R/W
b7	—	Reserved	Set to 0.	R/W

Notes:
1. The RI bit is set to 0 (no data in the U2RB register) when the U2RB register is read.
2. Can only be set in clock synchronous serial I/O mode (SIO mode). In other modes, set this bit to 0 (continuous receive mode disabled).
3. Enabled when bits SMD2 to SMD0 in the U2MR register are 001b (clock synchronous serial I/O mode), 100b (UART mode, transfer data 7 bits long), or 101b (UART mode, transfer data 8 bits long). Set this bit to 0 when bits SMD2 to SMD0 in the U2MR register are 001b (UART mode, transfer data 9 bits long).

Write to the U2C1 register using the MOV instruction.

U2LCH Bit (Data logic select bit)

This bit inverts the polarity of transmit data and receive data (data only). When the U2LCH bit is 1 (inverted), the logic of data written to the U2TB register is inverted when writing data to the U2TB register during transmission. When reading data from the U2TB register during reception, data with inverted logic is read.

21.2.6 UART2 Receive Buffer Register (U2RB)

Address 000C6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	SUM	PER	FER	OER	—	—	—	MPRB
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Receive data (D7 to D0) (5)		R
b1	—			R
b2	—			R
b3	—			R
b4	—			R
b5	—			R
b6	—			R
b7	—			R
b8	MPRB	Receive data (D8)/multiprocessor bit (1, 5)	[When the multiprocessor communication function is not used] Receive data (D8) [When the multiprocessor communication function is used] • When the MPRB bit is set to 0, received D0 to D7 are data fields. • When the MPRB bit is set to 1, received D0 to D7 are ID fields.	R
b9	—	Nothing is assigned. The write value must be 0. The read value is undefined.		—
b10	—			
b11	—	Reserved	Set to 0.	R/W
b12	OER	Overrun error flag (2, 3)	0: No overrun error 1: Overrun error	R
b13	FER	Framing error flag (2, 4)	0: No framing error 1: Framing error	R
b14	PER	Parity error flag (2, 4)	0: No parity error 1: Parity error	R
b15	SUM	Error sum flag (2, 3)	0: No error 1: Error	R

Notes:
1. Bit function differs depending on whether the multiprocessor communication function is being used.
2. When bits SMD2 to SMD0 in the U2MR register are set to 000b (serial interface disabled) or the RE bit in the U2C1 register is set to 0 (reception disabled), all of bits SUM, PER, FER, and OER are set to 0 (no error). The SUM bit is set to 0 (no error) when all of bits PER, FER, and OER are set to 0 (no error). Bits PER and FER are set to 0 when the U2RB register is read.
   When setting bits SMD2 to SMD0 in the U2MR register to 000b, set the TE bit in the U2C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
3. Enabled in all modes.
4. Enabled only in UART, IE, and multiprocessor communication modes. Disabled in other modes.
5. Read the U2RB register when the RI flag in the U2C1 register is 1 (data present in the U2RB register).

   Access the U2RB register in word (16-bit) units.

21.2.7 UART2 Digital Filter Function Select Register (U2RXDF)

Address 000C8h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	DF2EN	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	DF2EN	RXD2 digital filter enable bit	0: RXD2 digital filter disabled 1: RXD2 digital filter enabled	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

DF2EN Bit (RXD2 digital filter enable bit)

When the RXD2 digital filter is enabled, noise that is three or fewer pulses of the clock divided by the U2BRG register is reduced.
For details, refer to **21.3.2.7 RXD2 Digital Filter Select Function**.
This bit can only be set in UART mode and multiprocessor communication mode. In other modes, set this bit to 0 (RXD2 digital filter disabled).

21.2.8 UART2 Special Mode Register 5 (U2SMR5)

Address 000D0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	MPIE	—	—	—	MP
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MP	Multiprocessor communication enable bit (1, 2)	0: Multiprocessor communication disabled 1: Multiprocessor communication enabled	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	MPIE	Multiprocessor communication control bit	This bit is enabled when the MP bit is set to 1 (multiprocessor communication enabled). When the MPIE bit is set to 1, the following will result: • Receive data in which the multiprocessor bit is 0 is ignored. Setting of the RI bit in the U2C1 register and bits OER and FER in the U2RB register to 1 is disabled. • On receiving receive data in which the multiprocessor bit is 1, the MPIE bit is set to 0 and a receive operation other than multiprocessor communication is performed. When the MPIE bit is 0, operation is the same as normal receive operation.	R/W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	—			
b7	—			

Notes:
1. When the MP bit is set to 1 (multiprocessor communication enabled), the settings of bits PRY and PRYE in the U2MR register are disabled.
2. Enabled only when transfer data length is 7 bits or 8 bits in UART mode. Set this bit to 0 in other modes.

Write to the U2SMR5 register using the MOV instruction.

21.2.9 UART2 Special Mode Register 3 (U2SMR3)

Address 000D5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	NODC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is undefined.		—
b1	—	Reserved	Set to 0.	R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is undefined.		—
b3	NODC	Clock output select bit (1, 2)	0: CLK2 pin is set to CMOS output 1: CLK2 pin is set to N-channel open-drain output	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is undefined.		—
b5	—	Reserved	Set to 0.	R/W
b6	—			
b7	—			

Notes:
1. Can only be set in SIO mode. In other modes, set to 0 (CLK2 pin is set to CMOS output).
2. When UART2 is not used, set the NODC bit to 0 (CLK2 pin is set to CMOS output).

21.2.10 UART2 Special Mode Register (U2SMR)

Address 000D7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	SSS	ACSE	ABSCS	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			R/W
b2	—			R
b3	—			R/W
b4	ABSCS	Bus collision detect sampling clock select bit (1)	0: Rising edge of transfer clock 1: Underflow signal of timer RB2	R/W
b5	ACSE	Auto clear function select bit of transmission enable bit (1)	0: No auto clear function 1: Auto clear at bus collision	R/W
b6	SSS	Transmission start condition select bit (1, 2)	0: Not synchronized to RXD2 1: Synchronized to RXD2	R/W
b7	—	Nothing is assigned. The write value must be 0. The read value is 0.		—

Notes:
1. Can only be set in IE mode. In other modes, set to 0.
2. The SSS bit is set to 0 (not synchronized to RXD2) when transfer starts.

Write to the U2SMR register using the MOV instruction.

21.3 Operation

21.3.1 Clock Synchronous Serial I/O Mode (SIO mode)

In clock synchronous serial I/O mode, data is transmitted and received using a transfer clock.
Table 21.6 lists the Registers and Settings Used in Clock Synchronous Serial I/O Mode.

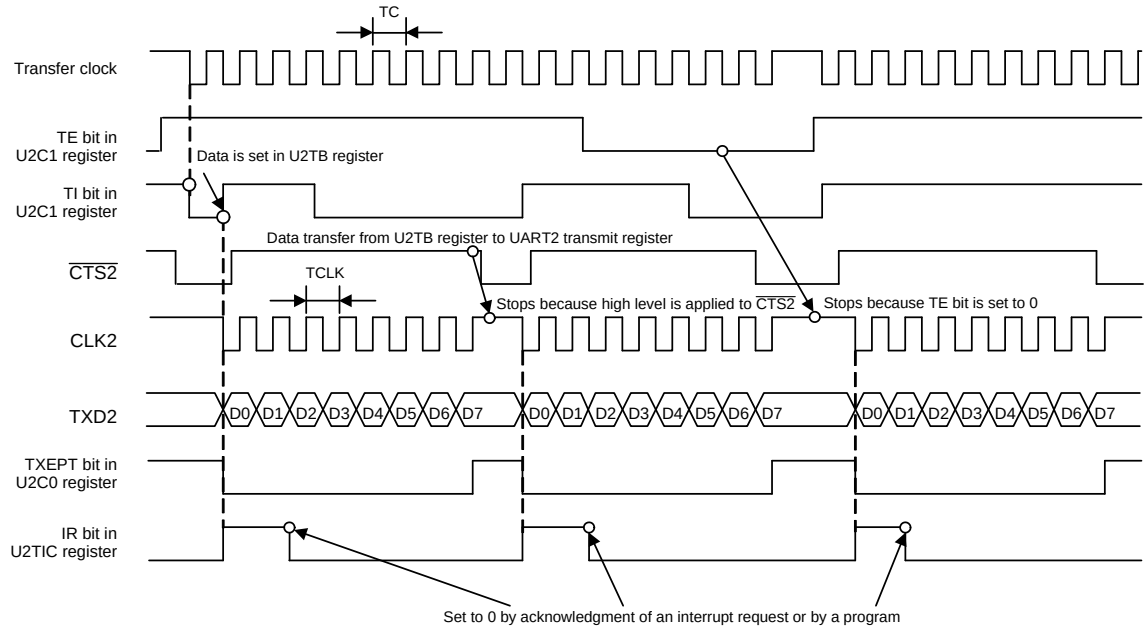
Table 21.6 Registers and Settings Used in Clock Synchronous Serial I/O Mode (1)

Register	Bit	Function
U2TB	b0 to b7	Set transmit data.
U2RB	b0 to b7	Receive data can be read.
	OER	Overrun error flag
U2BRG	b0 to b7	Set the bit rate.
U2MR (1)	SMD2 to SMD0	Set to 001b.
	CKDIR	Select an internal clock or external clock.
	IOPOL	Set to 0.
U2C0	CLK0, CLK1	Select the U2BRG count source.
	CRS	Select either the $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ function, if using.
	TXEPT	Transmit register empty flag
	CRD	Enable or disable the $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ function.
	NCH	Select the output format of the TXD2 pin.
	CKPOL	Select the polarity of the transfer clock.
	UFORM	Select LSB first or MSB first.
U2C1	TE	Set to 1 to enable transmission/reception.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	U2IRS	Select the UART2 transmit interrupt source.
	U2RRM	Set to 1 to use continuous receive mode.
	U2LCH	Set to 1 to use inverted data logic.
U2SMR3	NODC	Select the clock output format.

Note:
1. Write 0 to bits that are not listed above when writing in clock synchronous serial I/O mode.

Figure 21.2 shows the Transmit and Receive Timing in Clock Synchronous Serial I/O Mode.

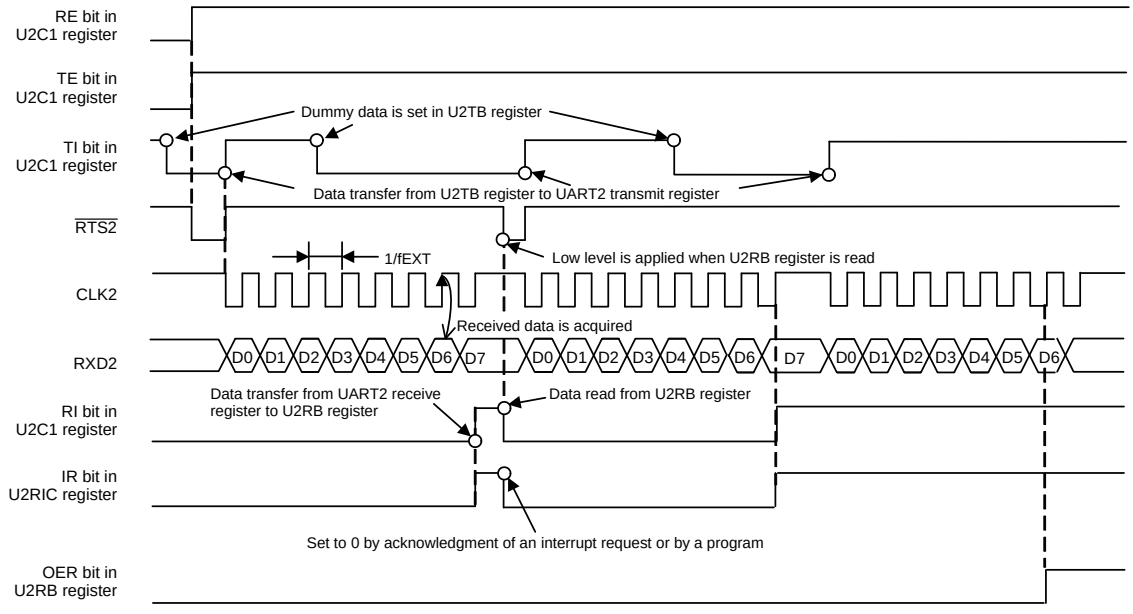
(1) Transmit timing example (internal clock selected)



The above diagram applies under the following conditions:
- CKDIR bit in U2MR register = 0 (internal clock)
- CRD bit in U2C0 register = 0 (CTS/RTS function enabled), CRS bit = 0 (CTS function selected)
- CKPOL bit in U2C0 register = 0 (transmit data is output at the falling edge and receive data is input at the rising edge of the transfer clock)
- U2IRS bit in U2C1 register = 0 (interrupt request generation when the U2TB register is empty)

TC = TCLK = 2 (n + 1) / fj
fj: Frequency of U2BRG count source (f1, f8, or f32)
n: Value set in U2BRG register

(2) Receive timing example (external clock selected)



The above diagram applies under the following conditions:
- CKDIR bit in U2MR register = 1 (external clock)
- CRD bit in U2C0 register = 0 (CTS/RTS function enabled), CRS bit = 1 (RTS function selected)
- CKPOL bit in U2C0 register = 0 (transmit data is output at the falling edge and receive data is input at the rising edge of the transfer clock)

fEXT: Frequency of external clock

Make sure the following conditions are met when the CLK2 pin input is high before receiving data:
- TE bit in U2C1 register = 1 (transmission enabled)
- RE bit in U2C1 register = 1 (reception enabled)
- Dummy data is written to U2TB register

Figure 21.2 Transmit and Receive Timing in Clock Synchronous Serial I/O Mode

21.3.1.1 Measure for Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in clock synchronous serial I/O mode, follow the procedures below:

(1) Set the TE bit in the U2C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the U2MR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the U2MR register to 001b (clock synchronous serial I/O mode).
(4) Set the TE bit in the U2C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

21.3.1.2 CLK Polarity Select Function

The polarity of the transfer clock is selected with the CKPOL bit in the U2C0 register. Figure 21.3 shows the Transfer Clock Polarity.

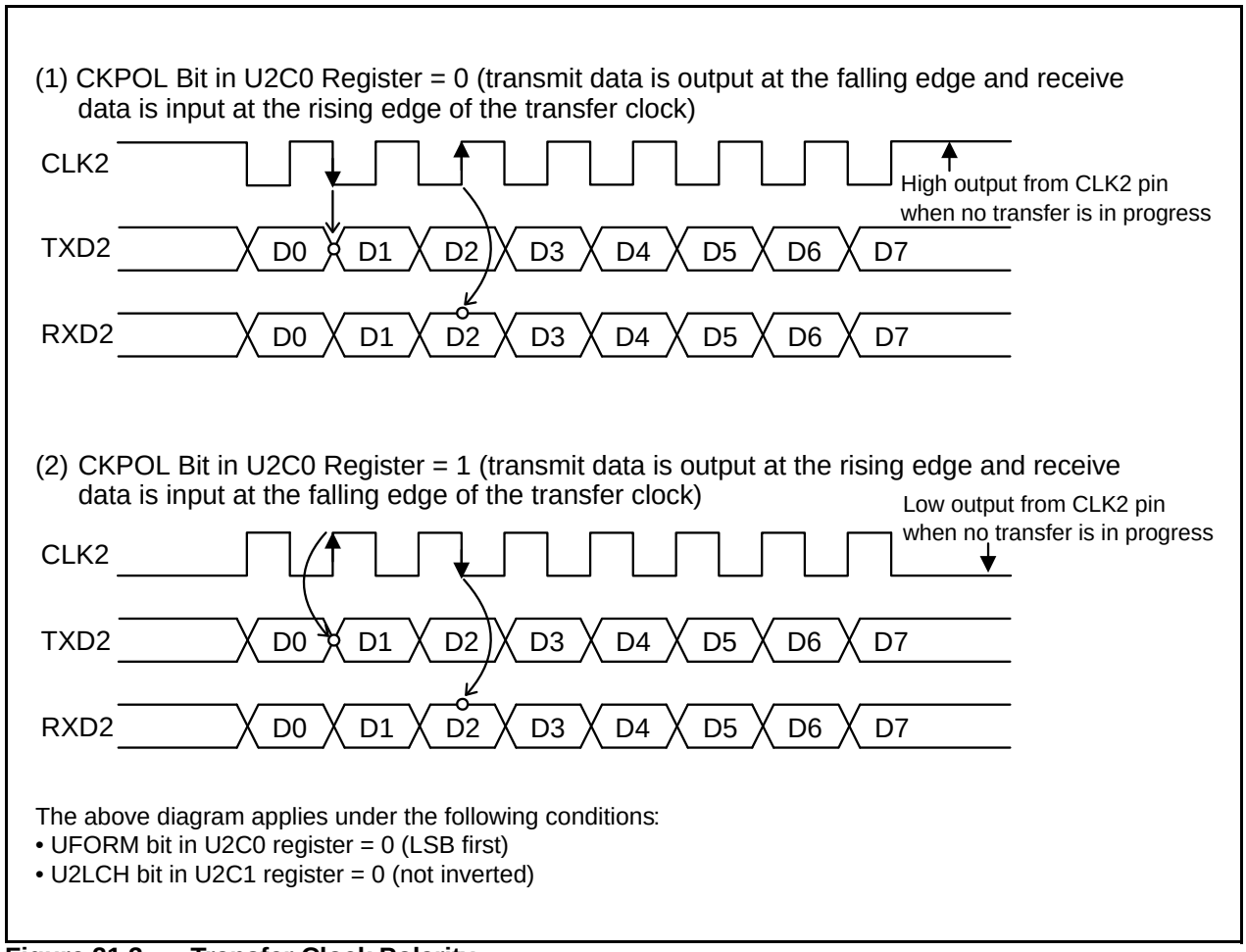


Figure 21.3 Transfer Clock Polarity

21.3.1.3 LSB First/MSB First Select Function

The transfer format is selected with the UFORM bit in the U2C0 register. Figure 21.4 shows the Transfer Format.

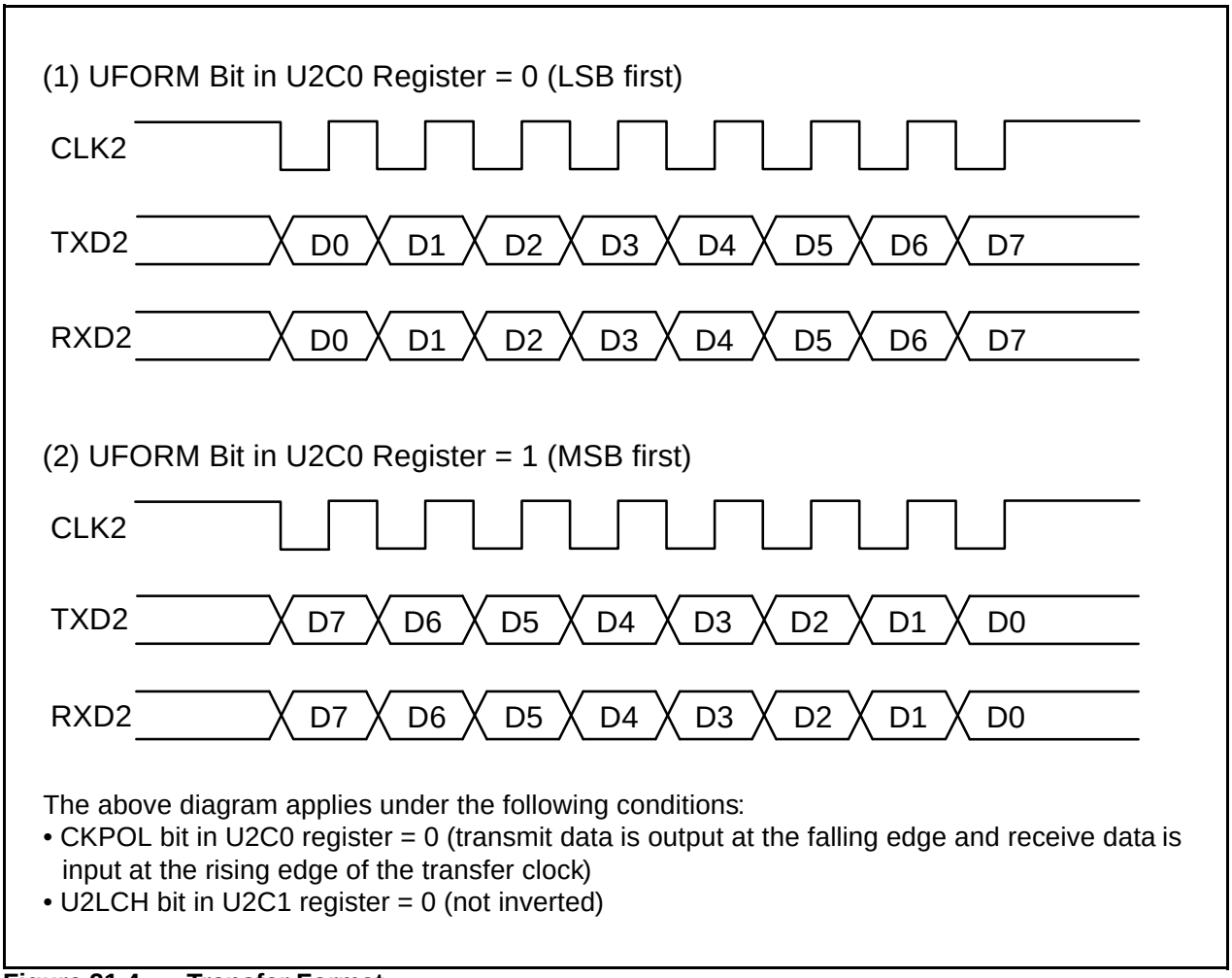


Figure 21.4 Transfer Format

21.3.1.4 Continuous Receive Mode

In continuous receive mode, receive operation is enabled when the receive buffer register is read. It is not necessary to write dummy data to the transmit buffer register to enable receive operation in this mode. However, a dummy read of the receive buffer register is required when starting the operating mode.

When the U2RRM bit in the U2C1 register is set to 1 (continuous receive mode), the TI bit in the U2C1 register is set to 0 (data present in the U2TB register) by reading the U2RB register. If the U2RRM bit is set to 1, do not write dummy data to the U2TB register by a program.

Set the U2RRM bit in the U2C1 register to 0 (continuous receive mode disabled) before reading the final data in continuous receive mode during master operation.

21.3.1.5 Serial Data Logic Switching Function

The U2LCH bit in the U2C1 register is used to select whether the logic of serial data is inverted.
If the U2LCH bit is set to 1 (inverted), the data written to the U2TB register has its logic inverted before being transmitted. Similarly, the received data has its logic inverted when read from the U2RB register. Figure 21.5 shows the Serial Data Logic Switching.

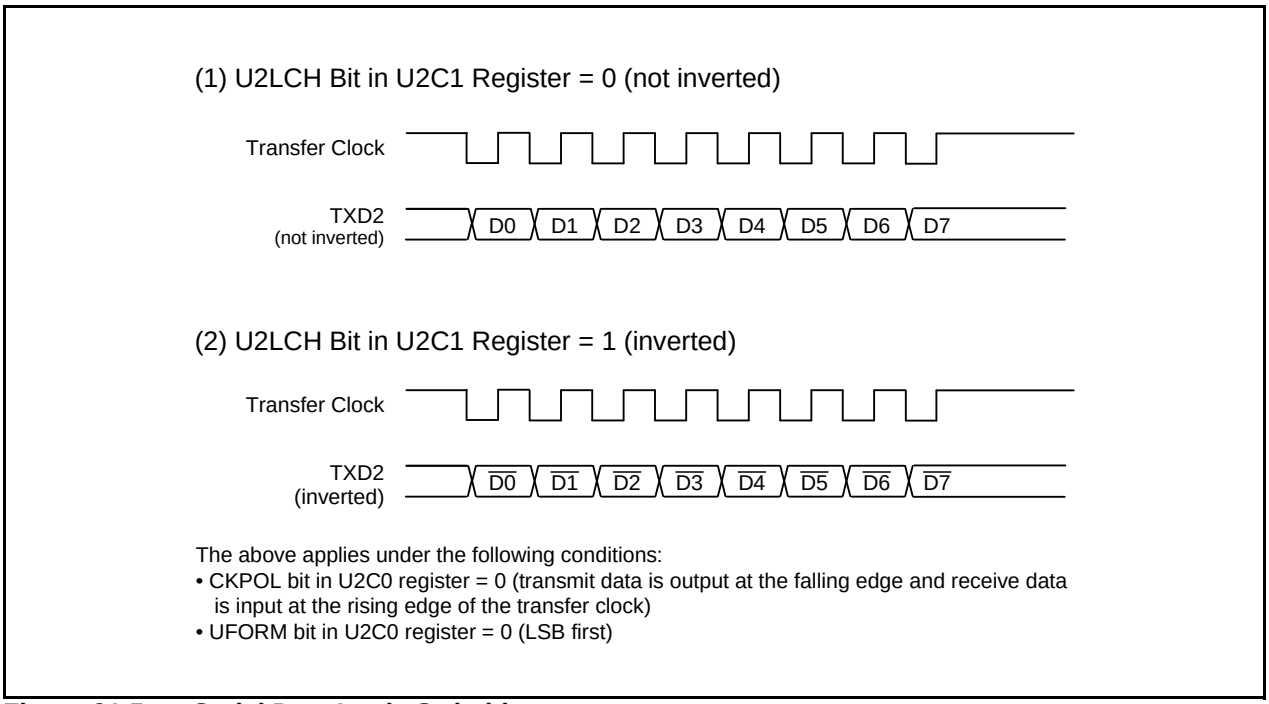


Figure 21.5 Serial Data Logic Switching

21.3.1.6 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Function

The $\overline{\text{CTS}}$ function is used to start transmit and receive operation when a low level is applied to the $\overline{\text{CTS2}}$ pin. Transmit and receive operation begins when the $\overline{\text{CTS2}}$ pin is held low.
If the input level is switched to high during transmit or receive operation, the operation stops before the next data.
For the $\overline{\text{RTS}}$ function, the $\overline{\text{RTS2}}$ pin outputs a low level when the MCU is ready for a receive operation. The output level goes high at the first falling edge of the RXD2 pin.

- CRD bit in the U2C0 register = 1 ($\overline{\text{CTS}}/\overline{\text{RTS}}$ function disabled):
  $\overline{\text{CTS2}}$ pin input is unused, and $\overline{\text{RTS2}}$ pin output is high
- CRD bit = 0 and CRS bit = 0 ($\overline{\text{CTS}}$ function selected):
  $\overline{\text{CTS2}}$ pin input is active, and $\overline{\text{RTS2}}$ pin output is high
- CRD bit = 0 and CRS bit = 1 ($\overline{\text{RTS}}$ function selected):
  $\overline{\text{CTS2}}$ pin input is unused, and $\overline{\text{RTS2}}$ pin output is active

21.3.2 Clock Asynchronous Serial I/O (UART) Mode

In UART mode, data is transmitted and received after setting the desired bit rate and transfer data format. Table 21.7 lists the Registers and Settings Used in UART Mode (1).

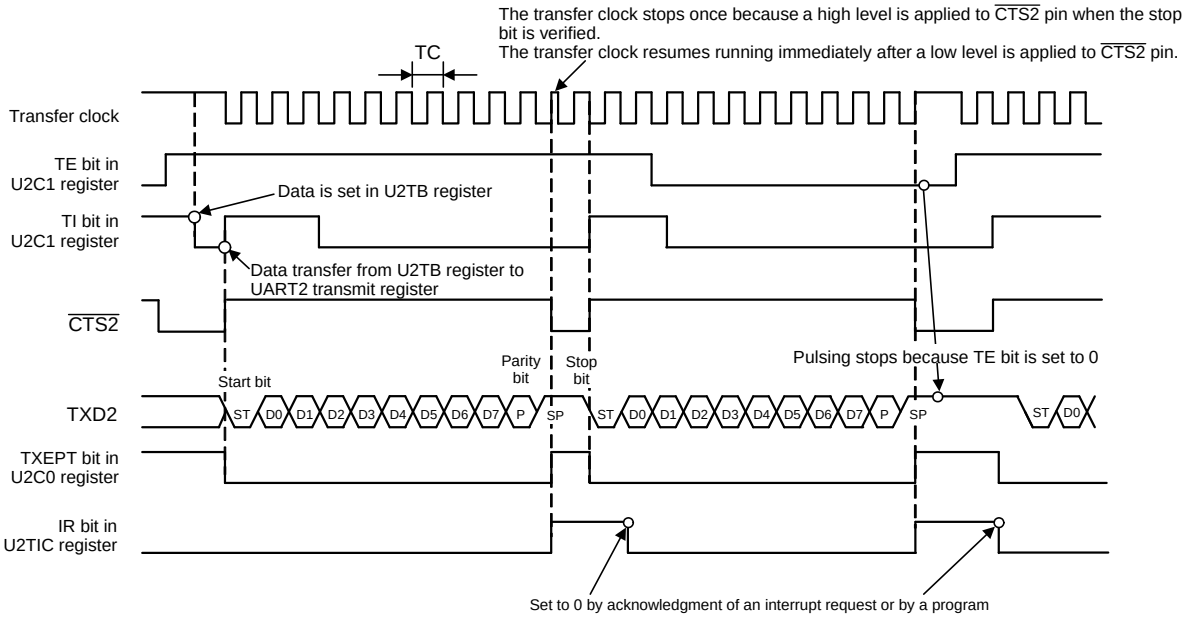
Table 21.7 Registers and Settings Used in UART Mode (1)

Register	Bit	Function
U2TB	b0 to b8	Set transmit data. (2)
U2RB	b0 to b8	Receive data can be read. (2, 3)
	OER, FER, PER, SUM	Error flag
U2BRG	b0 to b7	Set the bit rate.
U2MR	SMD2 to SMD0	Set to 100b when transfer data is 7 bits long.
		Set to 101b when transfer data is 8 bits long.
		Set to 110b when transfer data is 9 bits long.
	CKDIR	Select an internal clock or external clock.
	STPS	Select the stop bit.
	PRY, PRYE	Select whether parity is included and whether odd or even.
	IOPOL	Select the TXD2 and RXD2 I/O polarity.
U2C0	CLK0, CLK1	Select the U2BRG count source.
	CRS	Select either the $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ function, if using.
	TXEPT	Transmit register empty flag
	CRD	Enable or disable the $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ function.
	NCH	Select the output format of the TXD2 pin.
	UFORM	Select LSB first or MSB first when transfer data is 8 bits long. Set to 0 when transfer data is 7 or 9 bits long.
U2C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	U2IRS	Select the UART2 transmit interrupt source.
	U2LCH	Set to 1 to use inverted data logic.
U2RXDF	DF2EN	Select the digital filter disabled or enabled.

Notes:
1. Write 0 to bits that are not listed above when writing in clock asynchronous I/O mode.
2. The bits used for transmit/receive data are as follows:
   - Bits b0 to b6 when transfer data is 7 bits long
   - Bits b0 to b7 when transfer data is 8 bits long
   - Bits b0 to b8 when transfer data is 9 bits long
3. When the transfer data length is 7 bits, the contents of bits b7 and b8 are 0. When the transfer data length is 8 bits, the content of the b8 bit is 0.

Figure 21.6 shows a Transmit Timing Example in UART Mode and Figure 21.7 shows a Receive Timing Example in UART Mode.

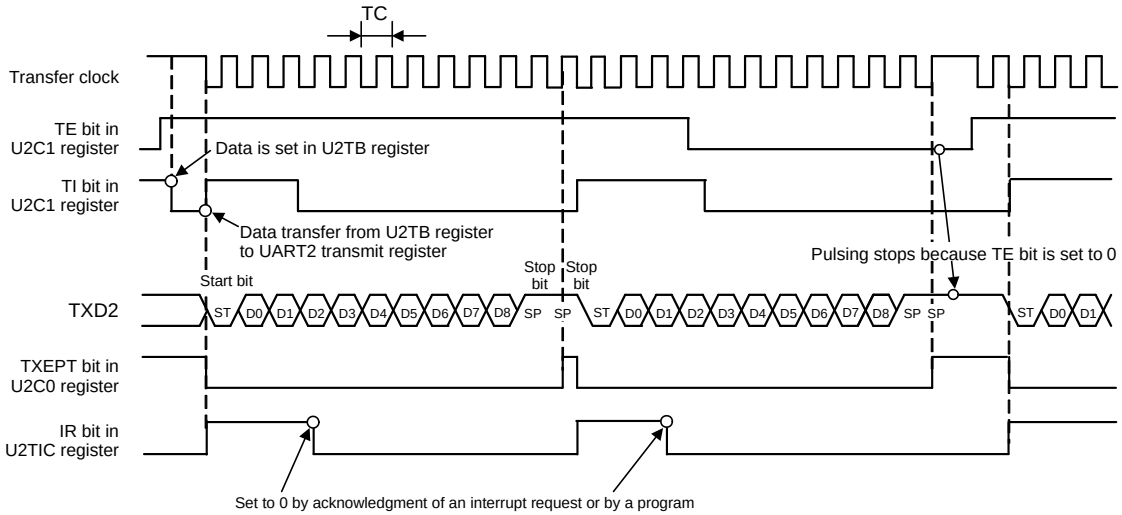
(1) Transmit timing example when transfer data is 8 bits long (parity enabled, one stop bit)



The above diagram applies under the following conditions:
- PRYE bit in U2MR register = 1 (parity enabled)
- STPS bit in U2MR register = 0 (one stop bit)
- CRD bit in U2C0 register = 0 (CTS/RTS function enabled), CRS bit = 0 (CTS function selected)
- U2IRS bit in U2C1 register = 1 (interrupt request generation when transmission is completed)

TC = 16 (n + 1) / fj or 16 (n + 1) / fEXT
Fj: Frequency of U2BRG count source (f1, f8, or f32)
fEXT: Frequency of U2BRG count source (external clock)
n: Value set in U2BRG

(2) Transmit timing example when transfer data is 9 bits long (parity disabled, two stop bits)

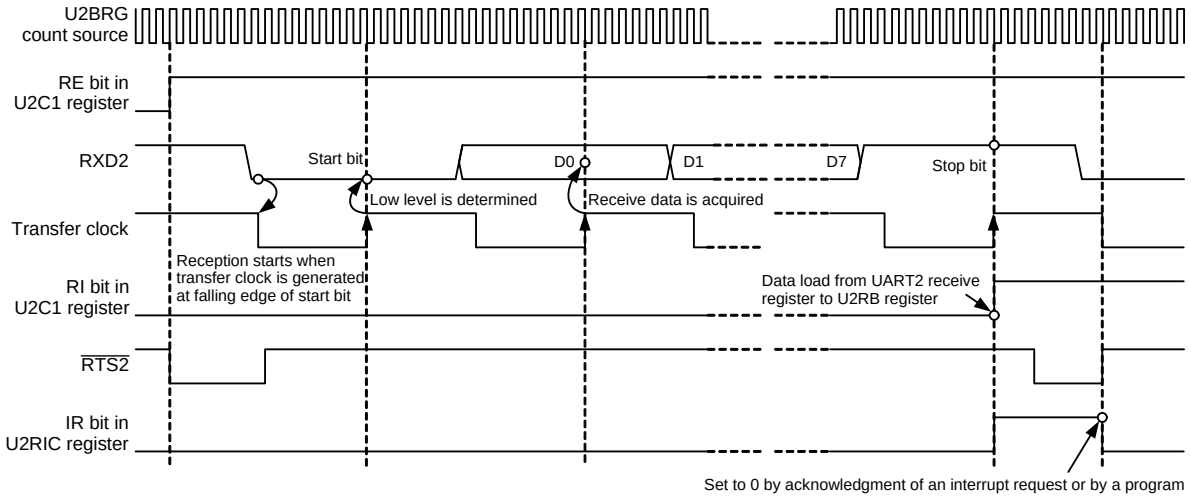


The above diagram applies under the following conditions:
- PRYE bit in U2MR register = 0 (parity disabled)
- STPS bit in U2MR register = 1 (two stop bits)
- CRD bit in U2C0 register = 1 (CTS/RTS function disabled)
- U2IRS bit in U2C1 register = 0 (interrupt request generation when the transmit buffer is empty)

TC = 16 (n + 1) / fj or 16 (n + 1) / fEXT
Fj: Frequency of U2BRG count source (f1, f8, or f32)
fEXT: Frequency of U2BRG count source (external clock)
n: Value set in U2BRG

Figure 21.6 Transmit Timing Example in UART Mode

• Receive timing example when transfer data is 8 bits long (parity disabled, one stop bit)



The above diagram applies under the following conditions:
- PRYE bit in U2MR register = 0 (parity disabled)
- STPS bit in U2MR register = 0 (one stop bit)
- CRD bit in U2C0 register = 0 ($\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function enabled), CRS bit = 1 ($\overline{\text{RTS}}$ function selected)

Figure 21.7 Receive Timing Example in UART Mode

21.3.2.1 Bit Rate

In UART mode, the bit rate is the frequency divided by the U2BRG register divided by 16. Figure 21.8 shows the Formula for Calculating U2BRG Register Setting Value and Table 21.8 lists Bit Rate Setting Examples in UART Mode (Internal Clock Selected).

• When an internal clock is selected

$$\text{Value set in U2BRG register} = \frac{fj}{\text{Bit Rate} \times 16} - 1$$

Fj: Count source frequency of U2BRG register (f1, f8, or f32)

• When an external clock is selected

$$\text{Value set in U2BRG register} = \frac{fEXT}{\text{Bit Rate} \times 16} - 1$$

fEXT: Count source frequency of U2BRG register (external clock)

Figure 21.8 Formula for Calculating U2BRG Register Setting Value

Table 21.8 Bit Rate Setting Examples in UART Mode (Internal Clock Selected)

Bit Rate (bps)	U2BRG Count Source	System Clock = 20 MHz			System Clock = 18.432 MHz			System Clock = 8 MHz		
		U2BRG Set Value	Actual Time (bps)	Setting Error (%)	U2BRG Set Value	Actual Time (bps)	Setting Error (%)	U2BRG Set Value	Actual Time (bps)	Setting Error (%)
1200	f8	129 (81h)	1201.92	0.16	119 (77h)	1200.00	0.00	51 (33h)	1201.92	0.16
2400	f8	64 (40h)	2403.85	0.16	59 (3Bh)	2400.00	0.00	25 (19h)	2403.85	0.16
4800	f8	32 (20h)	4734.85	-1.36	29 (1Dh)	4800.00	0.00	12 (0Ch)	4807.69	0.16
9600	f1	129 (81h)	9615.38	0.16	119 (77h)	9600.00	0.00	51 (33h)	9615.38	0.16
14400	f1	86 (56h)	14367.82	-0.22	79 (4Fh)	14400.00	0.00	34 (22h)	14285.71	-0.79
19200	f1	64 (40h)	19230.77	0.16	59 (3Bh)	19200.00	0.00	25 (19h)	19230.77	0.16
28800	f1	42 (2Ah)	29069.77	0.94	39 (27h)	28800.00	0.00	16 (10h)	29411.76	2.12
38400	f1	32 (20h)	37878.79	-1.36	29 (1Dh)	38400.00	0.00	12 (0Ch)	38461.54	0.16
57600	f1	21 (15h)	56818.18	-1.36	19 (13h)	57600.00	0.00	8 (08h)	55555.56	-3.55
115200	f1	10 (0Ah)	113636.36	-1.36	9 (09h)	115200.00	0.00	—	—	—

21.3.2.2 Measure for Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in UART mode, follow the procedures below:

(1) Set the TE bit in the U2C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the U2MR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the U2MR register to 100b (UART mode, transfer data 7 bits long), 101b (UART mode, transfer data 8 bits long), or 110b (UART mode, transfer data 9 bits long).
(4) Set the TE bit in the U2C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

21.3.2.3 LSB First/MSB First Select Function

As shown in Figure 21.9, the transfer format is selected with the UFORM bit in the U2C0 register. This function is enabled when transfer data is 8 bits long. Figure 21.9 shows the Transfer Format.

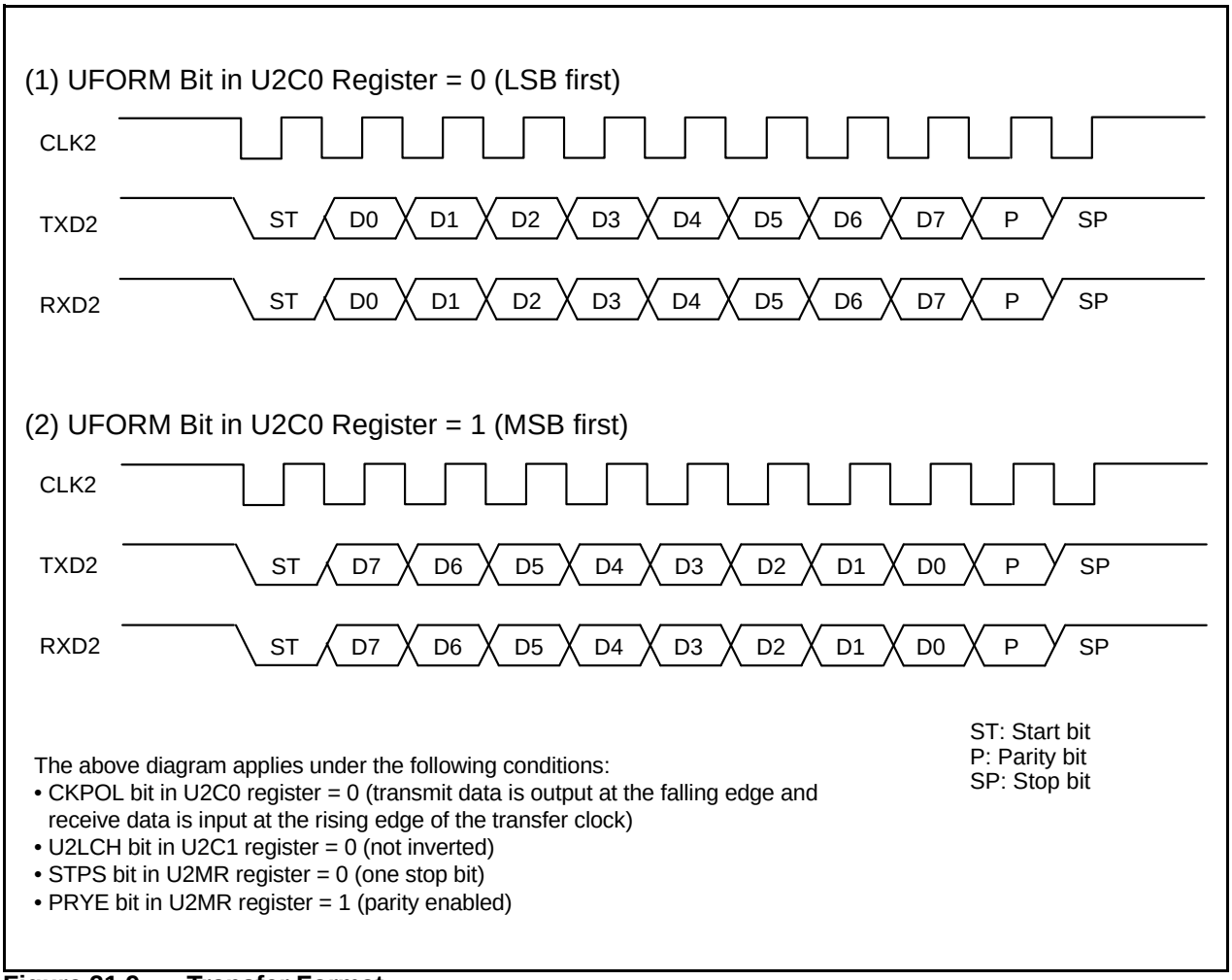


Figure 21.9 Transfer Format

21.3.2.4 Serial Data Logic Switching Function

The U2LCH bit in the U2C1 register is used to select whether the logic of serial data is inverted.
If the U2LCH bit is set to 1 (inverted), the data written to the U2TB register has its logic inverted before being transmitted. Similarly, the received data has its logic inverted when read from the U2RB register. Figure 21.10 shows the Serial Data Logic Switching.

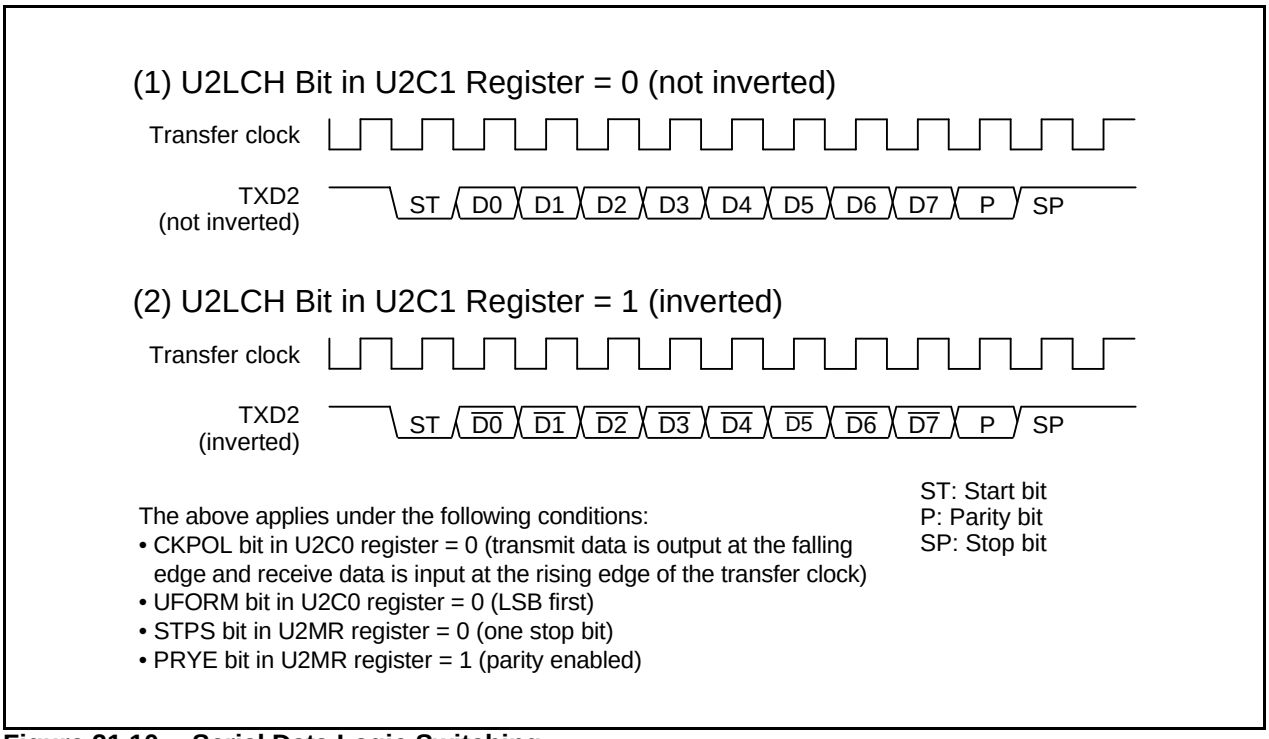


Figure 21.10 Serial Data Logic Switching

21.3.2.5 TXD and RXD I/O Polarity Inverse Function

This function inverts the polarities of the TXD2 pin output and RXD2 pin input. The logic levels of all I/O data (including bits for start, stop, and parity) are inverted. Figure 21.11 shows the TXD and RXD I/O Polarity Inversion.

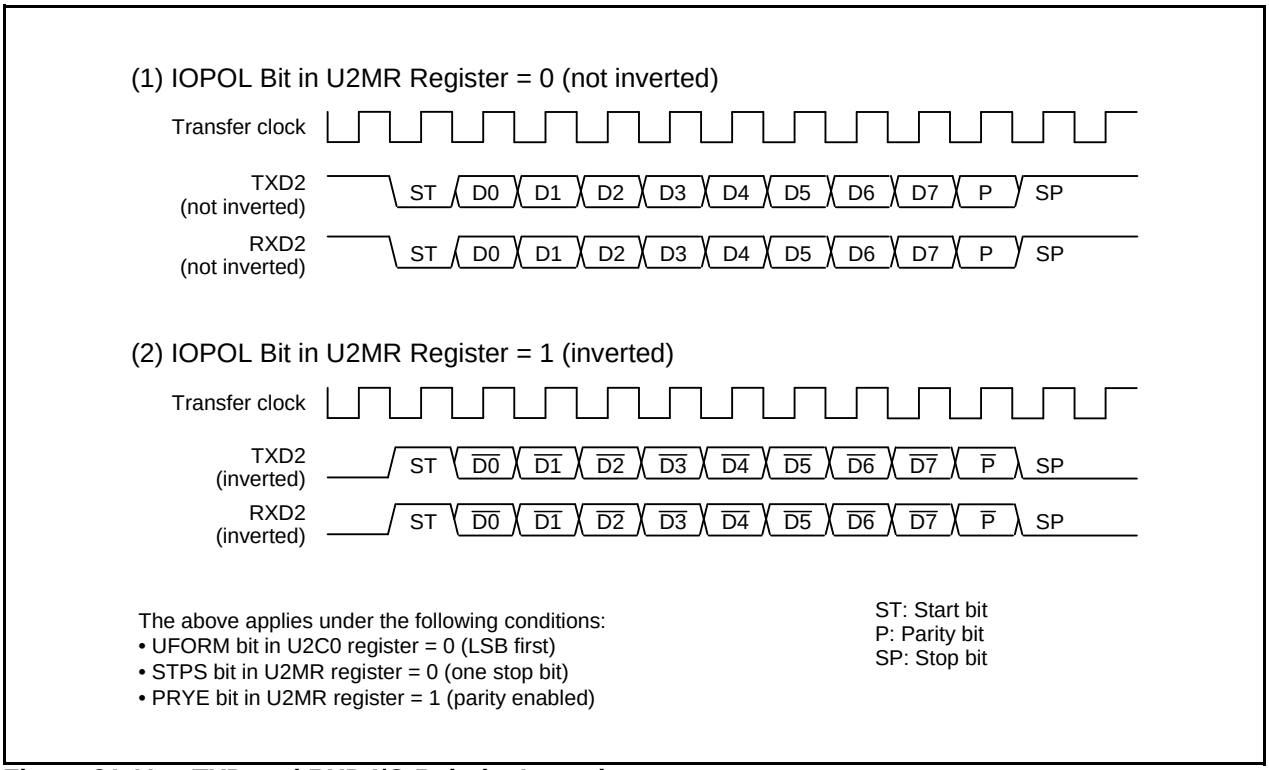


Figure 21.11 TXD and RXD I/O Polarity Inversion

21.3.2.6 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Function

The $\overline{\text{CTS}}$ function is used to start transmit and receive operations when a low level is applied to the $\overline{\text{CTS2}}$ pin. Transmit and receive operations start when the $\overline{\text{CTS2}}$ pin is held low. If the input level is switched to high during a transmit or receive operation, the operation stops before the next data.

For the $\overline{\text{RTS}}$ function, the $\overline{\text{RTS2}}$ pin outputs a low level when the MCU is ready for a receive operation. The output level goes high at the first falling edge of the RXD2 pin.

- CRD bit in the U2C0 register = 1 ($\overline{\text{CTS}}/\overline{\text{RTS}}$ function disabled):
  $\overline{\text{CTS2}}$ pin input is unused, and $\overline{\text{RTS2}}$ pin output is high
- CRD bit = 0 and CRS bit = 0 ($\overline{\text{CTS}}$ function selected):
  $\overline{\text{CTS2}}$ pin input is active, and $\overline{\text{RTS2}}$ pin output is high
- CRD bit = 0 and CRS bit = 1 ($\overline{\text{RTS}}$ function selected):
  $\overline{\text{CTS2}}$ pin input is unused, and $\overline{\text{RTS2}}$ pin output is active

21.3.2.7 RXD2 Digital Filter Select Function

The RXD2 digital filter function is used to latch the RXD2 input signal internally after reducing noise when the DF2EN bit in the U2RXDF register is 1 (RXD2 digital filter enabled). The noise canceller consists of three cascaded latch circuits and a match detection circuit. The RXD2 input signal is sampled on the clock divided by the U2BRG register. It is recognized as a signal and the level is passed forward to the next circuit when the three latch outputs match. When the outputs do not match, the previous value is retained.
In other words, when the level changes within three clocks, the change is recognized not as a signal change but as noise.
Figure 21.12 shows the RXD2 Digital Filter Circuit Block Diagram.

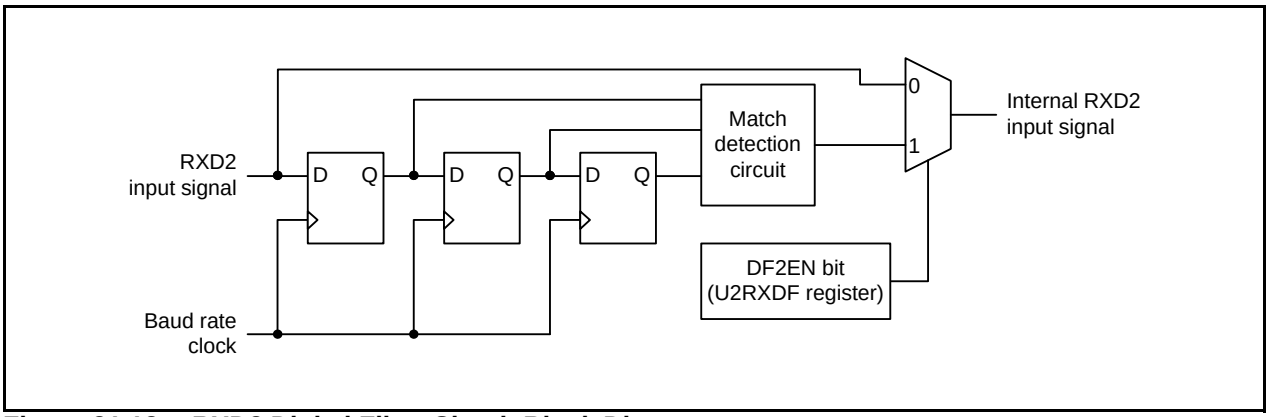


Figure 21.12 RXD2 Digital Filter Circuit Block Diagram

21.3.3 Special Mode 3 (IE mode)

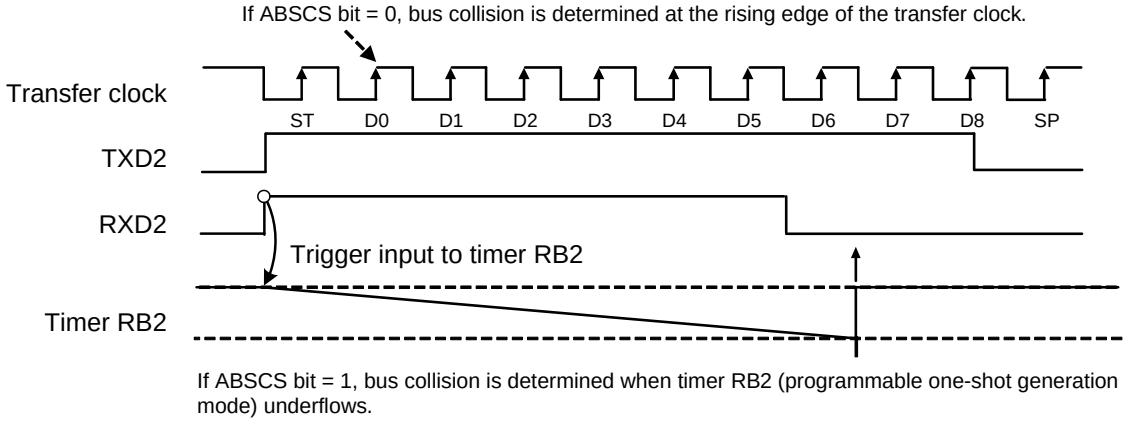
In this mode, one bit of IEBus is approximated with a 9-bit UART mode waveform.
Table 21.9 lists the Registers and Settings Used in IE Mode, and Figure 21.13 shows the Bits Associated with Bus Collision Detect Function.
If the TXD2 pin output level and RXD2 pin input level do not match, a UART2 bus collision detect interrupt request is generated.

Table 21.9 Registers and Settings Used in IE Mode (1)

Register	Bit	Function
U2TB	b0 to b8	Set transmit data. Set to 000000000b for 0 waveform output, and to 111000000b for 1 waveform output.
U2RB	b0 to b8	Receive data can be read.
	OER, FER, PER, SUM	Error flag
U2BRG	b0 to b7 (2)	Set the bit rate.
U2MR	SMD2 to SMD0	Set to 110b.
	CKDIR	Select an internal clock or external clock.
	STPS	Select the stop bit.
	PRY	Disabled
	IOPOL	Select the TXD2 and RXD2 I/O polarity.
U2C0	CLK0, CLK1 (2)	Select the U2BRG count source.
	CRS	Disabled
	TXEPT	Transmit register empty flag
	CRD	Set to 1.
	NCH	Select the output format of the TXD2 pin.
U2C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	U2IRS	Select the UART2 transmit interrupt source.
U2SMR	ABSCS	Select the sampling timing at which a bus collision is detected.
	ACSE	Select whether or not the auto clear function of the transmission enable bit is present.
	SSS	Select the transmission start condition.

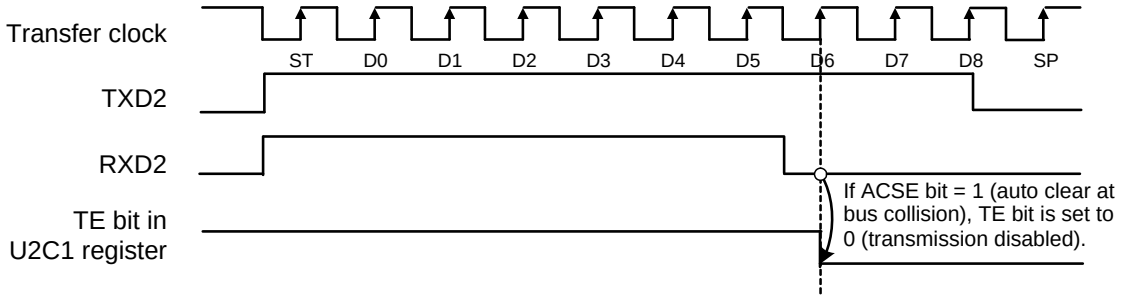
Notes:
1. Write 0 to bits that are not listed above when writing in IE mode.
2. Set bits CLK0 and CLK1 and the U2BRG register so that the transfer clock is 3.2 us/bit.

(1) ABSCS Bit in U2SMR Register (bus collision detect sampling clock select)

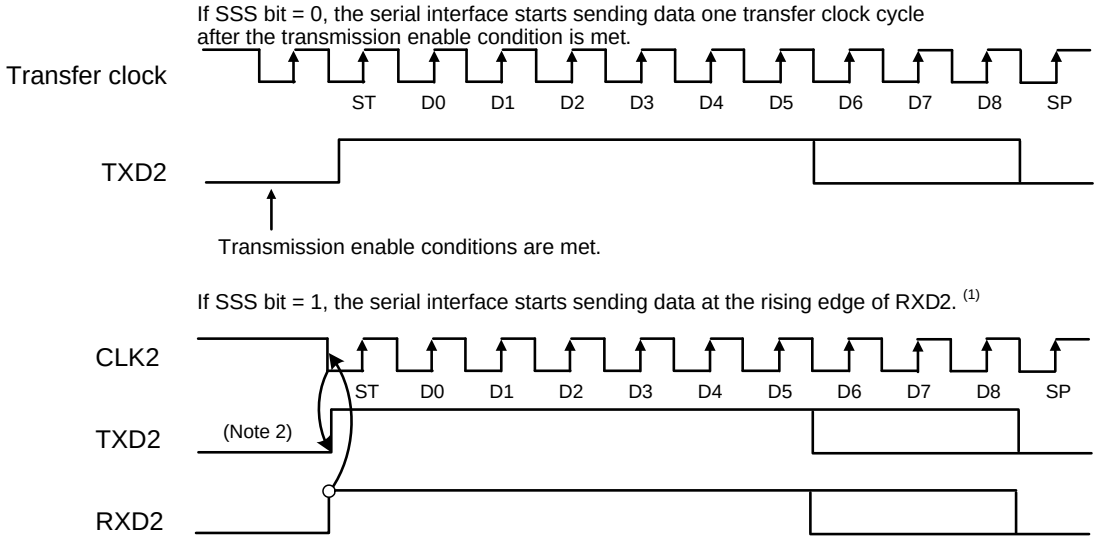


If ABSCS bit = 1, bus collision is determined when timer RB2 (programmable one-shot generation mode) underflows.

(2) ACSE Bit in U2SMR Register (auto clear of transmission enable bit)



(3) SSS Bit in U2SMR Register (transmission start condition select)



The above diagram applies when:
• IOPOL bit = 1 (inverted)

Notes:
1. The falling edge of RXD2 when IOPOL bit = 0; the rising edge of RXD2 when IOPOL bit = 1.
2. The transmit condition must be met before the falling edge of RXD2. (1)

Figure 21.13 Bits Associated with Bus Collision Detect Function

21.3.4 Multiprocessor Communication Function

When the multiprocessor communication function is used, data transmission/reception can be performed between a number of processors sharing communication lines by clock asynchronous serial I/O mode (UART mode), in which a multiprocessor bit is added to the data. For multiprocessor communication, each receiving station is addressed by a unique ID code. The serial communication cycle consists of two component cycles; an ID transmission cycle for specifying the receiving station, and a data transmission cycle for the specified receiving station. The multiprocessor bit is used to differentiate between the ID transmission cycle and the data transmission cycle. When the multiprocessor bit is set to 1, the cycle is an ID transmission cycle; when the multiprocessor bit is set to 0, the cycle is a data transmission cycle. Figure 21.14 shows an Inter-Processor Communication Example Using Multiprocessor Format (Data Transmission to Receiving Station A).

The transmitting station first sends the ID code of the receiving station to perform communication as communication data with a 1 multiprocessor bit added. It then sends transmit data as communication data with a 0 multiprocessor bit added.

When communication data in which the multiprocessor bit is 1 is received, the receiving station compares that data with its own ID. If they match, the data to be sent next is received. If they do not match, the receive station continues to skip communication data until data in which the multiprocessor bit is 1 is again received.

UART2 uses the MPIE bit in the U2SMR5 register to implement this function. When the MPIE bit is set to 1, data transfer from the UART2 receive register to the U2RB register, receive error detection, and the settings of the status flags, the RI bit in the U2C1 register, bits FER and OER in the U2RB register, are disabled until data in which the multiprocessor bit is 1 is received. On receiving a receive character in which the multiprocessor bit is 1, the MPRB bit in the U2RB register is set to 1 and the MPIE in the U2SMR5 register bit is set to 0, thus normal reception is resumed.

When the multiprocessor format is specified, the parity bit specification is invalid. All other bit settings are the same as those in normal clock asynchronous serial I/O mode (UART mode). The clock used for multiprocessor communication is the same as that in normal clock asynchronous serial I/O mode (UART mode).

Table 21.10 lists the Registers and Settings Used by Multiprocessor Communication Function (1).

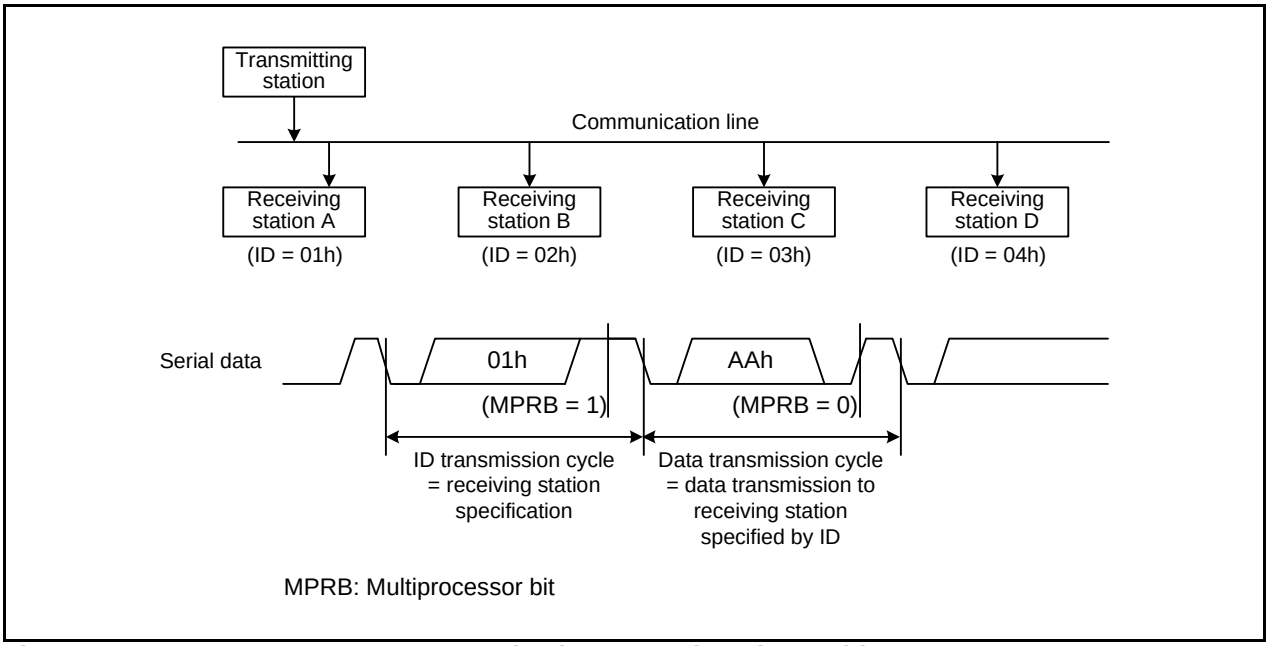


Figure 21.14 Inter-Processor Communication Example Using Multiprocessor Format (Data Transmission to Receiving Station A)

Table 21.10 Registers and Settings Used by Multiprocessor Communication Function (1)

Register	Bit	Function
U2TB (2)	b0 to b7	Set transmit data.
	MPTB	Set the transmit multiprocessor bit.
U2RB (3)	b0 to b7	Receive data can be read.
	MPRB	Multiprocessor bit
	OER, FER, PER, SUM	Error flag
U2BRG	b0 to b7	Set the bit rate.
U2MR	SMD2 to SMD0	Set to 100b when transfer data is 7 bits long.
		Set to 101b when transfer data is 8 bits long.
	CKDIR	Select an internal clock or external clock.
	STPS	Select the stop bit.
	PRY, PRYE	Parity detection function disabled
	IOPOL	Set to 0.
U2C0	CLK0, CLK1	Select the U2BRG count source.
	CRS	$\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ function disabled
	TXEPT	Transmit register empty flag
	CRD	Set to 1.
	NCH	Select the output format of the TXD2 pin.
U2C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	U2IRS	Select the UART2 transmit interrupt source.
U2SMR5	MP	Set to 1.
	MPIE (4)	Set to 1 when performing multiprocessor receive control.
U2RXDF	DF2EN	Select the digital filter enabled or disabled.

Notes:
1. Write 0 to bits that are not listed above in multiprocessor communication mode.
2. Set the MPTB bit to 1 when an ID data frame is transmitted. Set the MPTB bit to 0 when a data frame is transmitted.
3. If the MPRB bit is set to 1, received D7 to D0 are an ID field. If the MPRB bit is set to 0, received D7 to D0 are a data field.
4. When setting the MPIE bit to 1, make sure that there is no receive data (RI bit = 0).

21.3.4.1 Multiprocessor Transmission

Figure 21.15 shows a Flowchart of Multiprocessor Data Transmission. Set the MPTB bit in the U2TB register to 1 for ID transmission cycles. Set the MPTB bit in the U2TB register to 0 for data transmission cycles. Other operations are the same as in clock asynchronous serial I/O mode (UART mode).

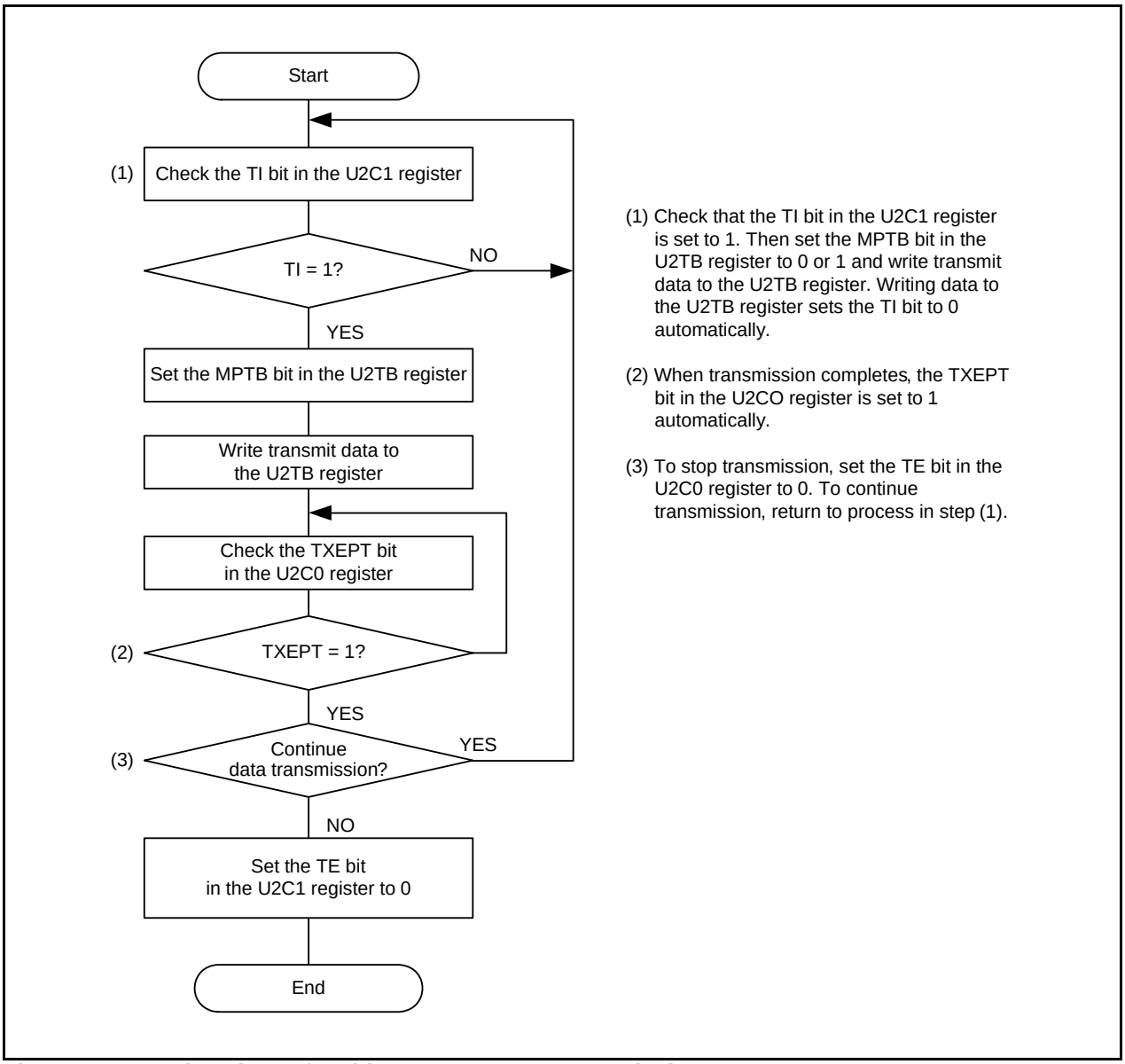


Figure 21.15 Flowchart of Multiprocessor Data Transmission

21.3.4.2 Multiprocessor Reception

Figure 21.16 shows a Flowchart of Multiprocessor Data Reception. When the MPIE bit in the U2SMR5 register is set to 1, communication data is ignored until data in which the multiprocessor bit is 1 is received. Communication data with a 1 multiprocessor bit added is transferred to the U2RB register as receive data. At this time, a reception complete interrupt request is generated. Other operations are the same as in universal asynchronous receiver/transmitter mode (UART mode). Figure 21.17 shows a Receive Operation Example during Multiprocessor Communication (with 8-Bit Data/Multiprocessor Bit/One-Stop Bit).

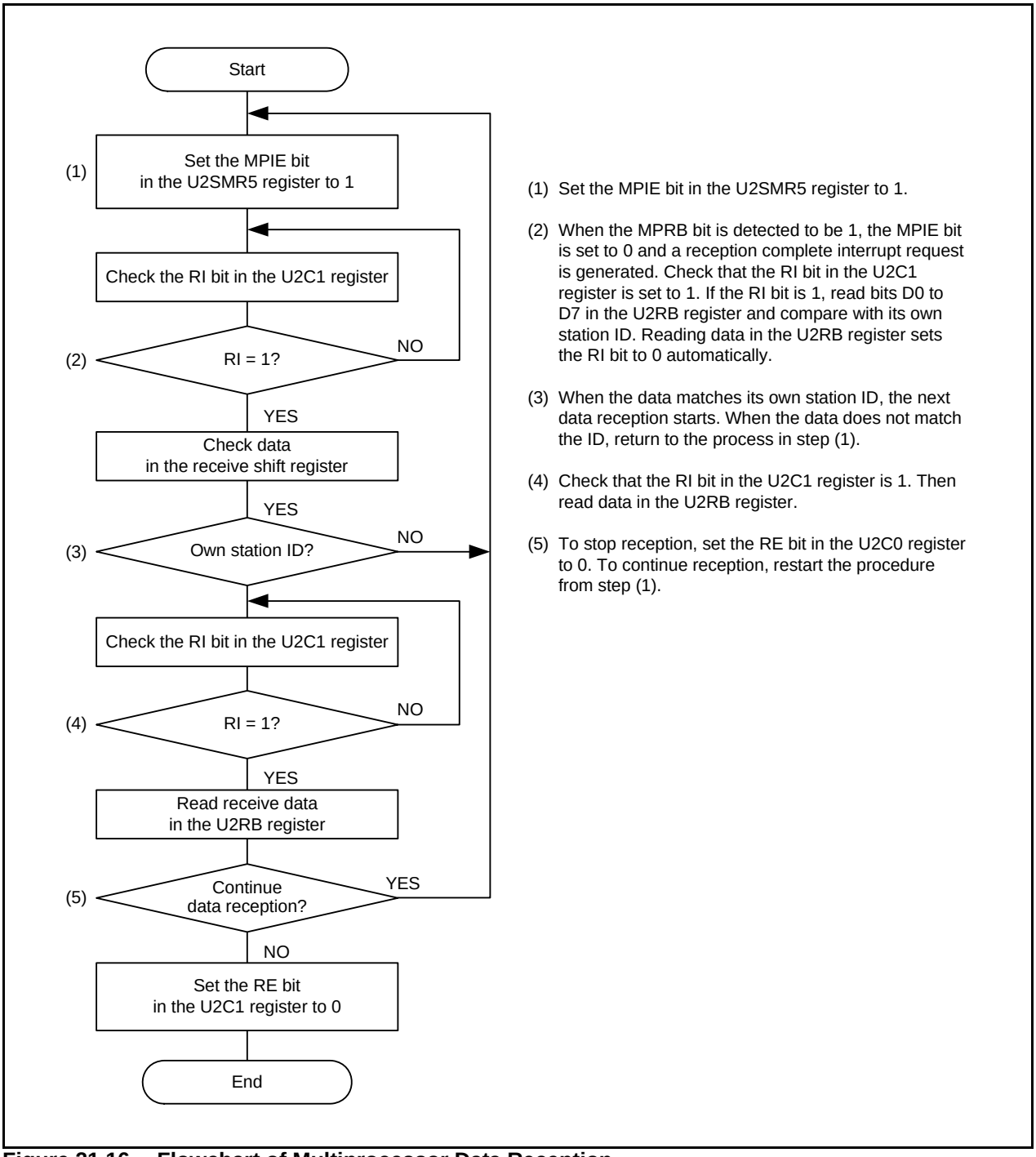


Figure 21.16 Flowchart of Multiprocessor Data Reception

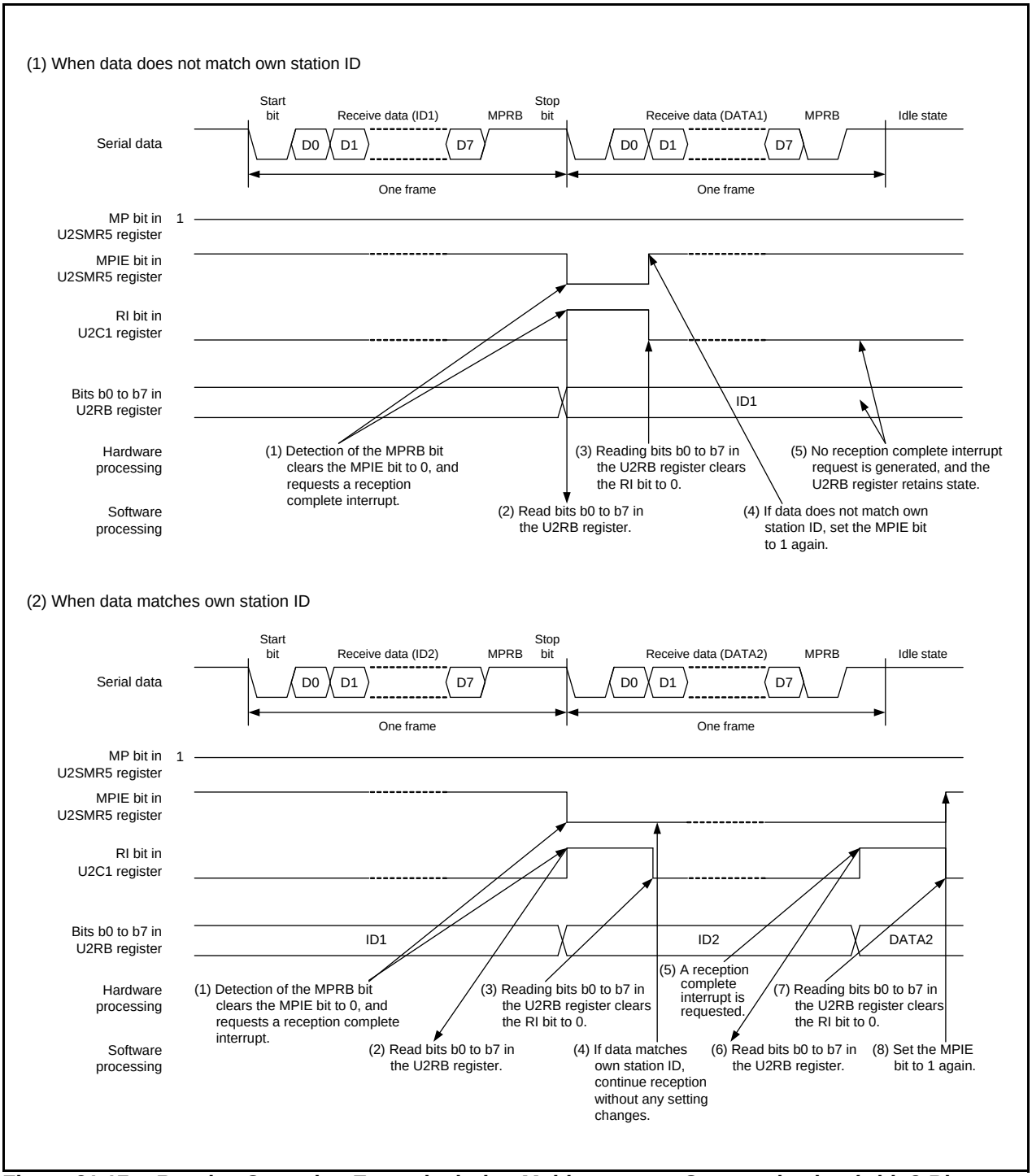


Figure 21.17 Receive Operation Example during Multiprocessor Communication (with 8-Bit Data/Multiprocessor Bit/One-Stop Bit)

21.3.4.3 RXD2 Digital Filter Select Function

This is the same function as in clock asynchronous serial I/O mode. Refer to **21.3.2.7 RXD2 Digital Filter Select Function**.

21.3.5 UART2 Interrupt Sources

Table 21.11 lists the Interrupt Sources.

Table 21.11 Interrupt Sources

UART2 Interrupt Source	Clock Synchronous Serial I/O Mode	UART Mode	IE Mode	Multiprocessor Communication Mode
Bus collision/condition interrupt	Disabled (1)	Disabled (1)	Bus collision detection interrupt	Disabled (1)
NACK interrupt	Disabled	Disabled	Disabled	Disabled
Receive/ACK interrupt	Receive interrupt	Receive interrupt	Receive interrupt	Receive interrupt
Transmit interrupt	Transmit buffer empty or transmission complete interrupt	Transmit buffer empty or transmission complete interrupt	Transmit buffer empty or transmission complete interrupt	Transmit buffer empty or transmission complete interrupt

Note:

1. A bus collision/condition interrupt operates even in clock synchronous serial I/O mode, UART mode, and multiprocessor communication mode. Set bits ILVL2 to ILVL0 in the U2BCNIC register to 000b (level 0 (interrupt disabled)).

21.4 Notes on Serial Interface (UART2)

21.4.1 Common to All Operating Modes

21.4.1.1 Register Access

The settings of the following registers can only be changed when the serial interface is disabled. Do not use these settings when the serial interface is enabled.
U2MR register: CKDIR bit
U2C0 register: Bits CLK0 and CLK1

The settings of the following registers can only be changed while transmission/reception is stopped. Do not use these settings during transmission/reception.
U2MR register: Bits SMD0 to SMD2, STPS, PRY, PRYE, and IOPOL
U2BRG register: Bits b0 to b7
U2C0 register: Bits CRS, CRD, NCH, CKPOL, and UFORM
U2C1 register: Bits U2IRS, U2RRM, U2LCH, and U2ERE
U2RXDF register: DF2EN bit
U2SMR5 register: MP bit
U2SMR3 register: NODC bit
U2SMR register: Bits ABSCS, ACSE, and SSS

21.4.1.2 N-Channel-Open-Drain Control Bit

When UART2 is not used, set the following bits to 0.
U2C0 register: NCH bit
U2SMR3 register: NODC bit

21.4.2 Clock Synchronous Serial I/O Mode

21.4.2.1 Transmission/Reception

When the $\overline{\text{RTS}}$ function is used with an external clock, the $\overline{\text{RTS2}}$ pin outputs a low level, which informs the transmitting side that the MCU is ready for a receive operation. The $\overline{\text{RTS2}}$ pin outputs a high level when a receive operation starts. Therefore, the transmit timing and receive timing can be synchronized by connecting the $\overline{\text{RTS2}}$ pin to the $\overline{\text{CTS2}}$ pin of the transmitting side. The $\overline{\text{RTS}}$ function is disabled when an internal clock is selected.

21.4.2.2 Transmission

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit in the U2C0 register is set to 0 (transmit data is output at the falling edge and receive data is input at the rising edge of the transfer clock), or while the external clock is held low when the CKPOL bit is set to 1 (transmit data is output at the rising edge and receive data is input at the falling edge of the transfer clock).
• The TE bit in the U2C1 register = 1 (transmission enabled)
• The TI bit in the U2C1 register = 0 (data present in the U2TB register)
• If the $\overline{\text{CTS}}$ function is selected, input to the $\overline{\text{CTS2}}$ pin = Low

21.4.2.3 Reception

In clock synchronous serial I/O mode, the shift clock is generated by activating the transmitter. Set the UART2-associated registers for transmit operation even if the MCU is used for receive operation only. Dummy data is output from the TXD2 pin while receiving.

When an internal clock is selected, the shift clock is generated by setting the TE bit in the U2C1 register to 1 (transmission enabled) and placing dummy data in the U2TB register. When an external clock is selected, set the TE bit to 1 (transmission enabled), place dummy data in the U2TB register, and input an external clock to the CLK2 pin to generate the shift clock.

If data is received consecutively, an overrun error occurs when the RE bit in the U2C1 register is set to 1 (data present in the U2RB register) and the next receive data is received in the UART2 receive register. Then, the OER bit in the U2RB register is set to 1 (overrun error). At this time, the U2RB register retains the previous receive data. If an overrun error occurs, use a program on the transmitting and receiving sides to resend the data that caused the error.

To receive data consecutively, set dummy data in the low-order byte in the U2TB register at each receive operation.

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit is set to 0, or while the external clock is held low when the CKPOL bit is set to 1.
- The RE bit in the U2C1 register = 1 (reception enabled)
- The TE bit in the U2C1 register = 1 (transmission enabled)
- The TI bit in the U2C1 register = 0 (data present in the U2TB register)

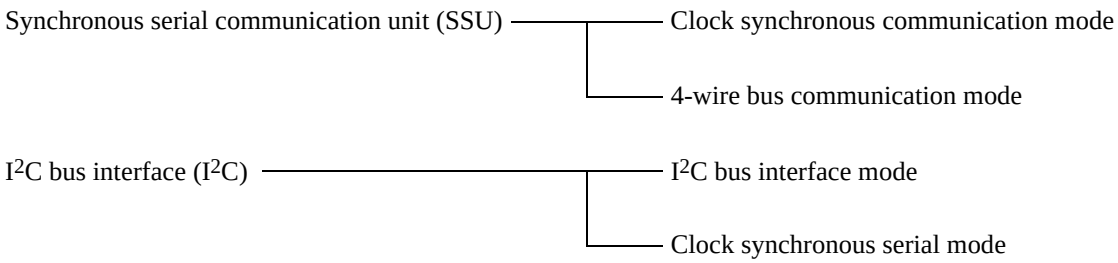
If an internal clock is selected, set the RE bit in the U2C1 register to 1 after setting the TE bit in the U2C1 register to 1 but before setting dummy data in the U2TB register.
Set the U2RRM bit in the U2C1 register to 1 before reading the last data in continuous receive mode during master operation.

22. Clock Synchronous Serial Interface

22.1 Overview

The clock synchronous serial interface is configured as follows:

Clock synchronous serial interface



22.1.1 Mode Selection

The clock synchronous serial interface supports four modes.
Table 22.1 lists the bits associated with mode selection.

Table 22.1 Mode Selections

IICSEL Bit in IICCR Register (1)	ICE Bit in SICR1 Register (1)	MS Bit in SIMR2 Register (1)	Function Name	Mode
0	0	0	Synchronous serial communication unit (SSU)	Clock synchronous communication mode
		1		4-wire bus communication mode
1	1	0	I2C bus interface (I2C)	I2C bus interface mode
		1		Clock synchronous serial mode

Note:
1. Do not use any settings other than the combinations listed in the above table. Operation is not guaranteed for any other combinations.

22.1.2 Synchronous Serial Communication Unit (SSU)

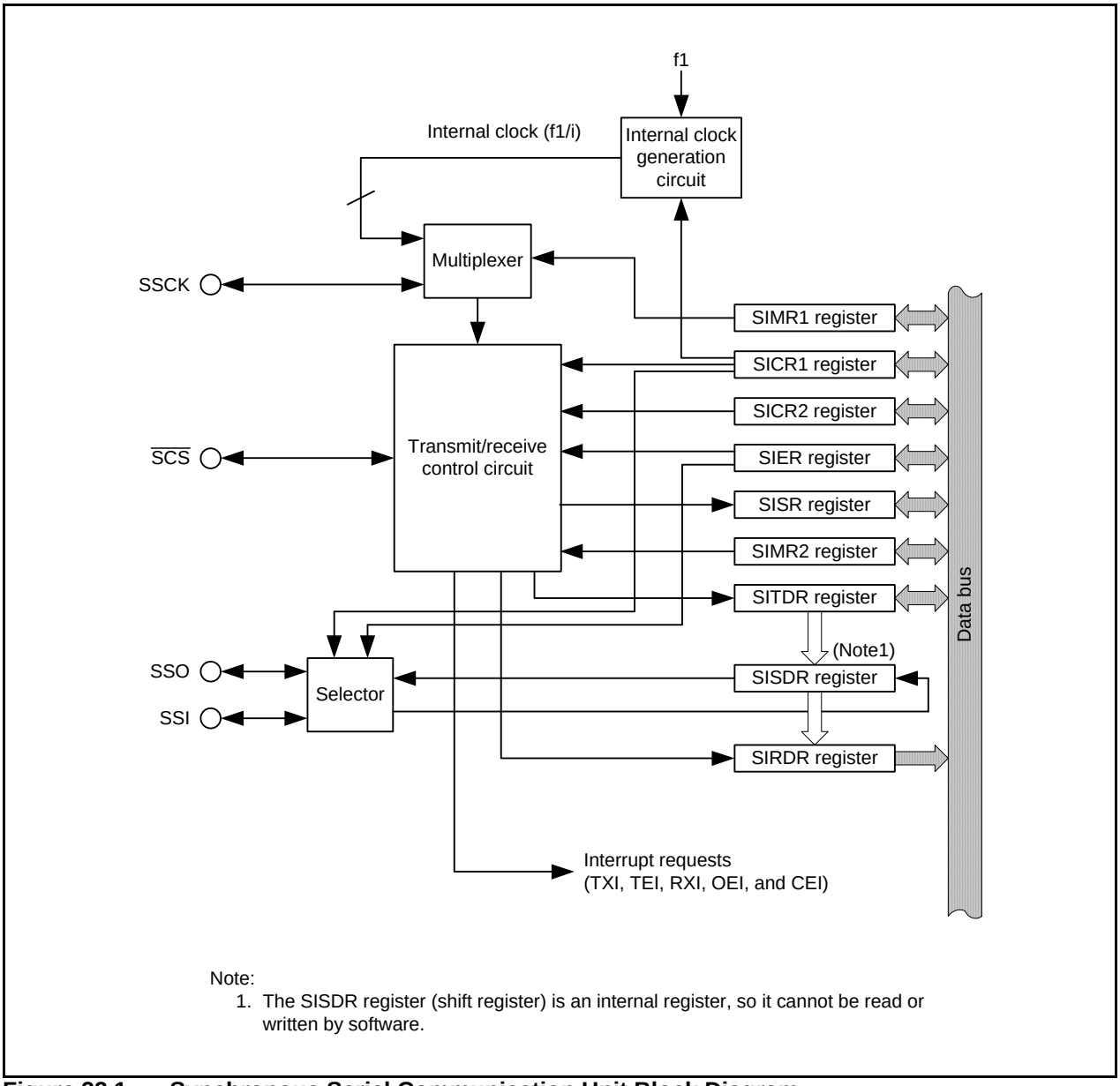
The synchronous serial communication unit (SSU) supports clock synchronous serial data communication. The SSU consists of two channels: SSU_0 and SSU_1. This chapter describes these channels as SSU unless there are differences between them.

Table 22.2 lists the Synchronous Serial Communication Unit Specifications and Figure 22.1 shows the Synchronous Serial Communication Unit Block Diagram (i = 4, 8, 16, 32, 64, 128, or 256).

Table 22.2 Synchronous Serial Communication Unit Specifications

Item	Description
Transfer data format	Transfer data length: 8 to 16 bits
Communication modes	• Clock synchronous communication mode • 4-wire bus communication mode (including bidirectional communication) - Master or slave device can be selected. - Continuous transmission and reception of serial data are supported because the shift, transmit, and receive registers are independent.
I/O pins	SSCK (I/O): Clock I/O pin SSI (I/O): Data I/O pin $\overline{\text{SSO}}$ (I/O): Data I/O pin $\overline{\text{SCS}}$ (I/O): Chip select I/O pin
Transfer clocks	• When the MST bit in the SICR1 register is 0 (slave mode) External clock (input from the SSCK pin) • When the MST bit in the SICR1 register is 1 (master mode) Internal clock (selectable among f1/256, f1/128, f1/64, f1/32, f1/16, f1/8, and f1/4, output from the SSCK pin) • The clock polarity and phase can be selected.
Receive error detection	• Overrun error detection Indicates an overrun error has occurred during reception and reception is terminated in error. When the next serial data reception completes while the RDRF bit in the SISR register is 1 (data present in the SIRDR register), the ORER_AL bit in the SISR register is set to 1 (overrun error).
Multimaster error detection	• Conflict error detection When starting a serial communication while the MS bit in the SIMR2 register is 1 (4-wire bus communication mode) and the MST bit in the SICR1 register is 1 (master mode), the CE_ADZ bit in the SISR register is set to 1 (conflict error) if the $\overline{\text{SCS}}$ pin input is low. When the $\overline{\text{SCS}}$ pin input changes from low to high during transfer while the MS bit in the SIMR2 register is 1 (4-wire bus communication mode) and the MST bit in the SICR1 register is 0 (slave mode), the CE_ADZ bit in the SISR register is set to 1.
Interrupt sources	5 (transmit end, transmit data empty, receive data full, overrun error, and conflict error (1))
Selectable functions	• Data transfer direction MSB first or LSB first can be selected. • SSCK clock polarity The level (low or high) when the clock stops can be selected. • SSCK clock phase The edge for data change and data download can be selected.

Note:
1. A conflict error occurs only in 4-wire bus communication mode.



Note:
1. The SISDR register (shift register) is an internal register, so it cannot be read or written by software.

Figure 22.1 Synchronous Serial Communication Unit Block Diagram (i = 4, 8, 16, 32, 64, 128, or 256)

Table 22.3 Synchronous Serial Communication Unit Pin Configuration

Pin Name	I/O	Function
SSI	Input/Output	Data input/output
$\overline{\text{SCS}}$	Input/Output	Chip select input/output
SSCK	Input/Output	Clock input/output
SSO	Input/Output	Data input/output

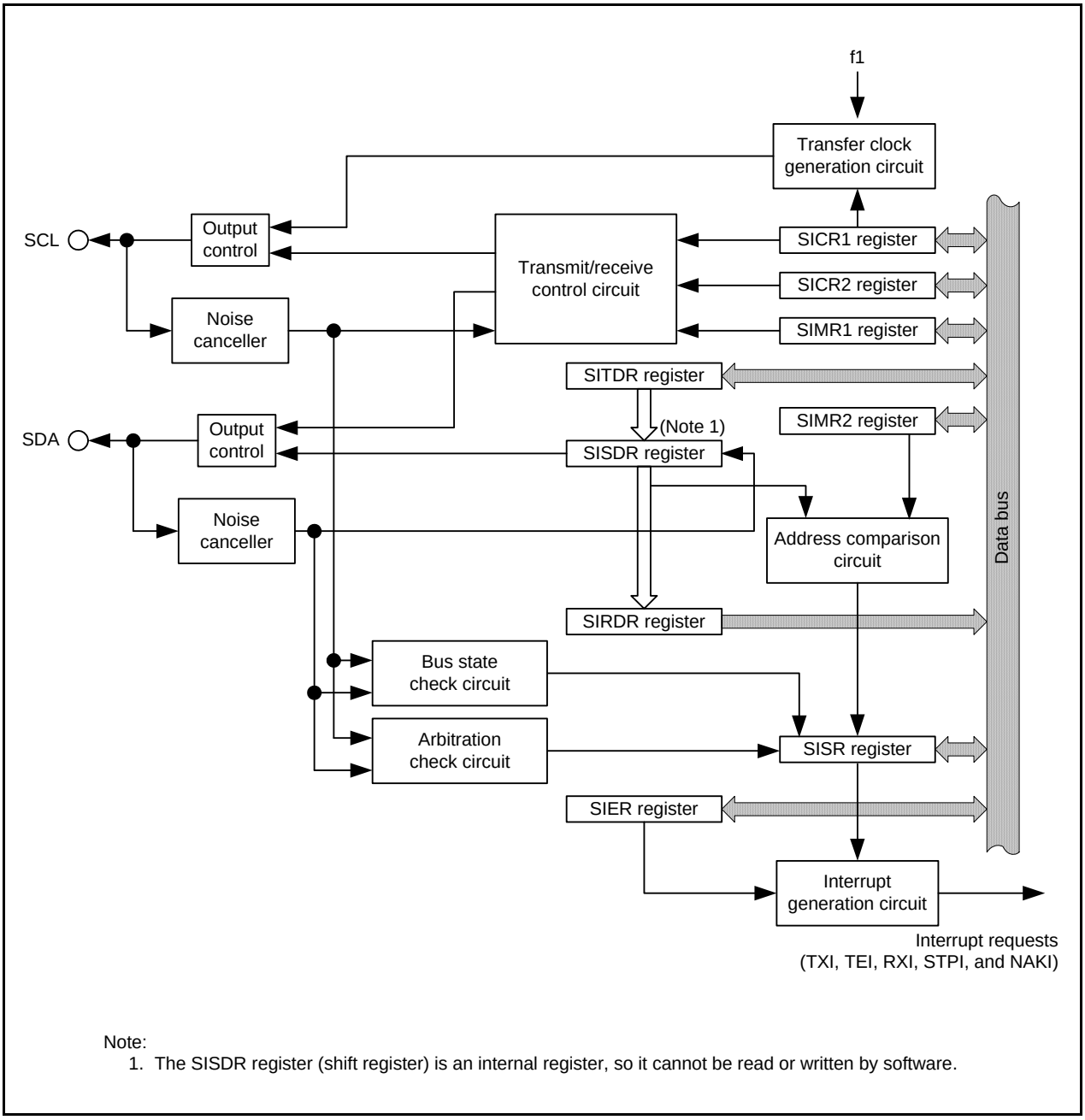
22.1.3 I²C bus Interface

The I²C bus interface is the circuit that performs serial communication based on the data transfer format of the Philips I²C bus. This interface consists of two channels: I²C_0 and I²C_1. This chapter describes these channels as I²C unless there are differences between them.

Table 22.4 lists the I²C bus Interface Specifications, Figure 22.2 shows the I²C bus Interface Block Diagram, Figure 22.3 shows an External Circuit Connection Example for Pins SCL and SDA and Table 22.5 lists the I²C bus Interface Pin Configuration.

Table 22.4 I²C bus Interface Specifications

Item	Description
Communication modes	• I²C bus interface mode - Master or slave device can be selected. - Continuous transmission and reception are supported (because the shift, transmit, and receive registers are independent). - Start/stop conditions are automatically generated in master mode. - Automatic loading of the acknowledge bit during transmission. - Bit synchronization and wait function are included. (In master mode, the state of the SCL signal is monitored per bit and the timing is synchronized automatically. If the transfer is not ready yet, the SCL signal is held low and the interface stands by.) - Direct drive of pins SCL and SDA (N-channel open-drain output) is supported. • Clock synchronous serial mode Continuous transmission and reception are supported (because the shift, transmit, and receive registers are independent).
I/O pins	SCL (I/O): Serial clock I/O pin SDA (I/O): Serial data I/O pin
Transfer clocks	• When the MST bit in the SICR1 register is 0 (slave mode) External clock (input from the SCL pin) • When the MST bit in the SICR1 register is 1 (master mode) Internal clock selected by bits CKS0 to CKS3 in the SICR1 register and bits IICTCTWI and IICTCHALF in the IICCR register (output from the SCL pin)
Receive error detection	• Overrun error detection (clock synchronous serial mode) Indicates an overrun error has occurred during reception. When the last bit of the next data is received while the RDRF bit in the SISR register is 1 (data present in the SIRDR register), the ORER_AL bit in the SISR register is set to 1 (overrun error).
Interrupt sources	• I²C bus interface mode: 6 sources Transmit data empty (including when slave address matches), transmit end, receive data full (including when slave address matches), arbitration lost, NACK detection, and stop condition detection • Clock synchronous serial mode: 4 sources Transmit data empty, transmit end, receive data full, and overrun error
Selectable functions	• I²C bus interface mode The output level of the acknowledge signal during reception can be selected. • Clock synchronous serial mode MSB first or LSB first can be selected as the data transfer direction. • SDA digital delay The digital delay value of the SDA pin can be selected by bits SDADLY0 and SDADLY1 in the IICCR register.



Note:
1. The SISDR register (shift register) is an internal register, so it cannot be read or written by software.

Figure 22.2 I²C bus Interface Block Diagram

Table 22.5 I²C bus Interface Pin Configuration

Pin Name	Function
SCL	Clock input/output
SDA	Data input/output

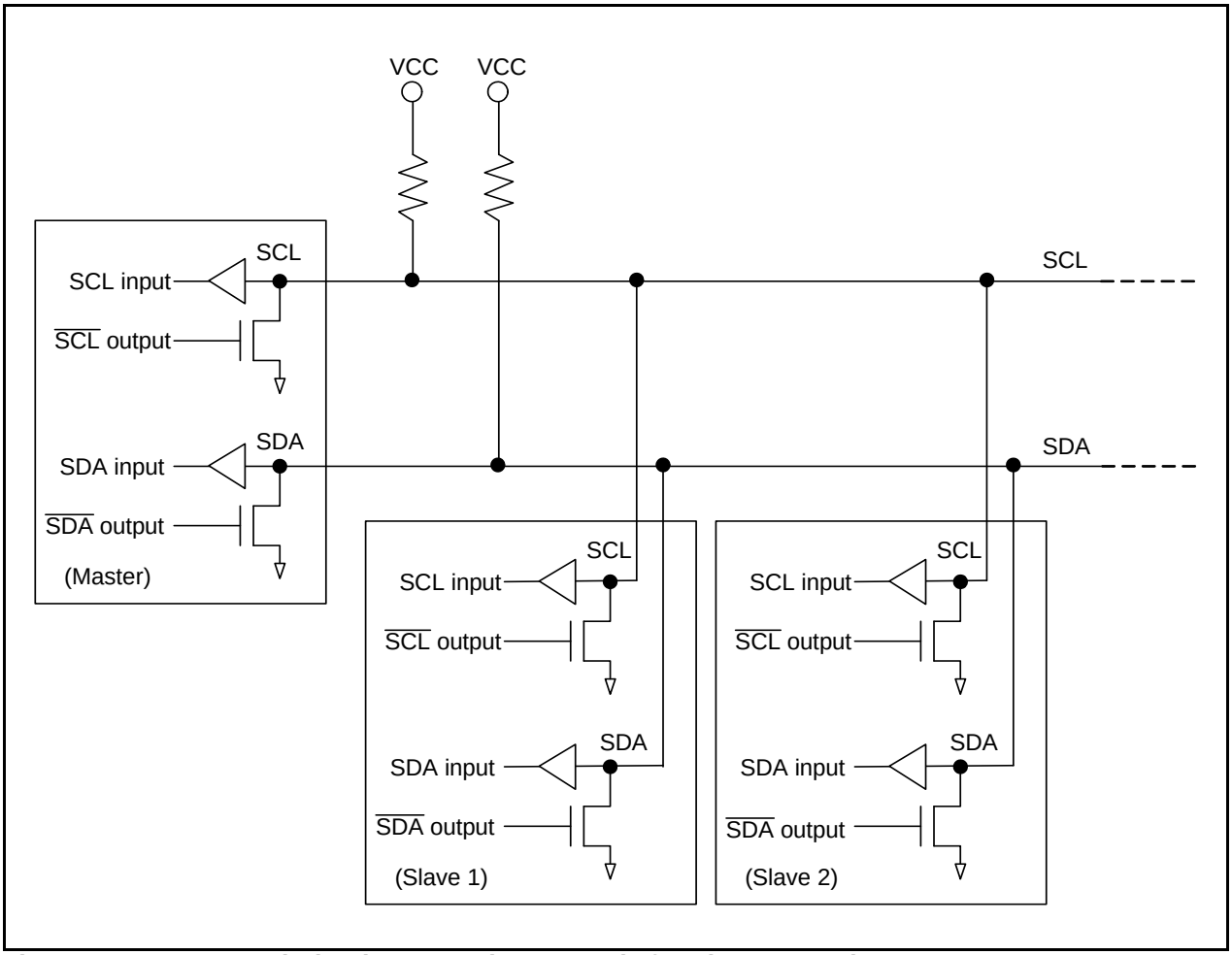


Figure 22.3 External Circuit Connection Example for Pins SCL and SDA

22.2 Registers

The registers of the clock synchronous serial interface are multiplexed with the SSU and I2C bus functions. Table 22.6 lists the Clock Synchronous Serial Interface Register Configuration.

Table 22.6 Clock Synchronous Serial Interface Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
I2C_0 Control Register	IICCR_0	00001110b	000E0h	8
SS_0 Bit Counter Register	SSBR_0	11111000b	000E1h	8
SI_0 Transmit Data Register	SITDR_0	FFh	000E2h	8 or 16 (1)
		FFh	000E3h	
SI_0 Receive Data Register	SIRDR_0	FFh	000E4h	8 or 16 (1)
		FFh	000E5h	
SI_0 Control Register 1	SICR1_0	00h	000E6h	8
SI_0 Control Register 2	SICR2_0	01111101b	000E7h	8
SI_0 Mode Register 1	SIMR1_0	00010000b	000E8h	8
SI_0 Interrupt Enable Register	SIER_0	00h	000E9h	8
SI_0 Status Register	SISR_0	00h	000EAh	8
SI_0 Mode Register 2	SIMR2_0	00h	000EBh	8
I2C_1 Control Register	IICCR_1	00001110b	000F0h	8
SS_1 Bit Counter Register	SSBR_1	11111000b	000F1h	8
SI_1 Transmit Data Register	SITDR_1	FFh	000F2h	8 or 16 (1)
		FFh	000F3h	
SI_1 Receive Data Register	SIRDR_1	FFh	000F4h	8 or 16 (1)
		FFh	000F5h	
SI_1 Control Register 1	SICR1_1	00h	000F6h	8
SI_1 Control Register 2	SICR2_1	01111101b	000F7h	8
SI_1 Mode Register 1	SIMR1_1	00010000b	000F8h	8
SI_1 Interrupt Enable Register	SIER_1	00h	000F9h	8
SI_1 Status Register	SISR_1	00h	000FAh	8
SI_1 Mode Register 2	SIMR2_1	00h	000FBh	8

Notes:
1. Use 8-bit access when the I2C bus function is used and 16-bit access when the SSU function is used.
2. In standby mode, the values of bits SDAO and SCLO in the SICR2 register, bits BC0 to BC3 in the SIMR1 register, and the internal registers are initialized. The other bits in registers SICR2 and SIMR1 and the other registers are not initialized.
3. When performing a write access after standby mode, insert at least one NOP instruction.
4. Do not set to the standby state while the I2C bus or SSU function is operating.
5. In the standby state, all registers cannot be written, but can be read.

22.2.1 I²C Control Register (IICCR)

Address 000E0h (IICCR_0), 000F0h (IICCR_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SDADLY1	SDADLY0	IICTCHALF	IICTCTWI	—	—	—	IICSEL
After Reset	0	0	0	0	1	1	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICSEL	SSU/I²C bus switch bit (1)	0: SSU function 1: I²C bus function	R/W
b1	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b2	—			
b3	—			
b4	IICTCTWI	I²C double transfer rate select bit (2, 3)	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the SICR1 register 1: Transfer rate is twice the value set with bits CKS0 to CKS3 in the SICR1 register	R/W
b5	IICTCHALF	I²C half transfer rate select bit (2, 3)	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the SICR1 register 1: Transfer rate is half the value set with bits CKS0 to CKS3 in the SICR1 register	R/W
b6	SDADLY0	SDA pin digital delay select bits (3, 4, 5)	b7 b6 0 0: Digital delay of 3 × f1 cycles 0 1: Digital delay of 11 × f1 cycles 1 0: Digital delay of 19 × f1 cycles 1 1: Do not set.	R/W
b7	SDADLY1			R/W

Notes:
1. Initialize all the registers before switching between the I²C bus function and the SSU function.
2. Do not set both the IICTCTWI and IICTCHALF bits to 1 when the I²C bus function is used. Set both these bits to 0 when the SSU function is used.
3. Set this bit at the initial setting and do not rewrite it during operation.
4. Do not set a digital delay which is half the transfer rate or greater.
5. Enabled only when the I²C bus function is used. Disabled when the SSU function is used.

22.2.2 SS Bit Counter Register (SSBR)

Address 000E1h (SSBR_0), 000F1h (SSBR_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	BS3	BS2	BS1	BS0
After Reset	1	1	1	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BS0	SSU data transfer length set bits (1, 2)	b3 b2 b1 b0 0 0 0 0: 16 bits 1 0 0 0: 8 bits 1 0 0 1: 9 bits 1 0 1 0: 10 bits 1 0 1 1: 11 bits 1 1 0 0: 12 bits 1 1 0 1: 13 bits 1 1 1 0: 14 bits 1 1 1 1: 15 bits Other than the above: Do not set.	R/W
b1	BS1			R/W
b2	BS2			R/W
b3	BS3			R/W
b4	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b5	—			
b6	—			
b7	—			

Notes:
1. Do not write to bits BS0 to BS3 during operation of the SSU function. Write to bits BS0 to BS3 when the RE_STIE bit in the SIER register is 0 (data reception disabled) and the TE_NAKIE bit is 0 (data transmission disabled).
2. The settings other than the determined values are invalid.

The setting of the SSBR register is valid when the SSU function is used. The setting of the SSBR register is invalid when the I^2C bus function is used.

Bits BS0 to BS3 (SSU data transfer length set bits)

Lengths of 8 to 16 bits can be used as the SSU data transfer length.

22.2.3 SI Transmit Data Register (SITDR)

Address 000E2h (SITDR_0), 000F2h (SITDR_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Store the transmit data. (1) When it is detected that the SISDR register is empty, the transmit data stored in this register is transferred to the SISDR register and transmission is started. If the next transmit data has been written to the SITDR register during the data transmission from the SISDR register, the data can be transmitted consecutively. When the MLS bit in the SIMR1 register is 1 (data transfer with LSB first), the data with inverted MSB and LSB is read after writing to the SITDR register.	R/W

Note:
1. A data transfer length of 9 bits or more (b8 to b15) is only used with the SSU function. When setting the SSU data transfer length to 9 bits or more using the SSBR register, access the SITDR register in 16-bit units.
   When using 8-bit access, the transmit operation will not be started even if the higher byte (b15 to b8) is accessed. When the lower byte (b7 to b0) is accessed, TDRE is negated and the transmit operation starts.

22.2.4 SI Receive Data Register (SIRDR)

Address 000E4h (SIRDR_0), 000F4h (SIRDR_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Store the receive data. (1, 2, 3) When 1 byte of data has been received by the SISDR register, the receive data is transferred to the SIRDR register and the receive operation completes. At this time, the next receive operation is enabled. Continuous reception is possible using registers SISDR and SIRDR.	R

Notes:
1. When the ORER_AL bit in the SISR register is set to 1 (overrun error), the SIRDR register retains the data received before the overrun error occurred. The receive data (data in the SISDR register) when an overrun error occurs is discarded.
2. A SSU data transfer length of 9 bits or more (b8 to b15) is only used with the SSU function. When setting the SSU data transfer length to 9 bits or more using the SSBR register, access the SIRDR register in 16-bit units. When the SIRDR register is accessed in 8-bit units, the RDRF bit in the SISR register is also set to 0 (no data in the SIRDR register).
3. Read the SIRDR register when the RDRF bit is 1 (data present in the SIRDR register).

22.2.5 SI Control Register 1 (SICR1)

In the SICR1 register, the bit functions differ between the SSU and I^2C bus functions.

22.2.5.1 SSU Function

Address 000E6h (SICR1_0), 000F6h (SICR1_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ICE	RCVD	MST	TRS	CKS3	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Transfer clock select bits (1)	b3 b2 b1 b0 0 0 0 0: f1/256 0 0 0 1: f1/128 0 0 1 0: f1/64 0 0 1 1: f1/32 0 1 0 0: f1/16 0 1 0 1: f1/8 0 1 1 0: f1/4 Other than the above: Do not set.	R/W
b1	CKS1			R/W
b2	CKS2			R/W
b3	CKS3			R/W
b4	TRS	Reserved	Set to 0.	R/W
b5	MST	Master/slave select bit (2, 3)	0: Slave mode 1: Master mode	R/W
b6	RCVD	Receive disable bit (4)	0: Next receive operation continues 1: Next receive operation disabled	R/W
b7	ICE	Reserved	Set to 0.	R/W

Notes:
1. In master mode, set these bits according to the required transfer rate. For details on the transfer rate, refer to **22.3.1.1 Transfer Clock**.
2. When the MST bit is 1 (master mode), the SSCK pin functions as the transfer clock output pin. When the CE_ADZ bit in the SISR register is set to 1 (conflict error), the MST bit is set to 0 (slave mode).
3. In multimaster operation, use the MOV instruction to set the MST bit.
4. When the MST bit is 0 (slave mode), do not set the RCVD bit to 1.

22.2.5.2 I²C bus Function

Address 000E6h (SICR1_0), 000F6h (SICR1_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ICE	RCVD	MST	TRS	CKS3	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Transfer clock select bits (1)	b3 b2 b1 b0 0 0 0 0: f1/28 0 0 0 1: f1/40 0 0 1 0: f1/48 0 0 1 1: f1/64 0 1 0 0: f1/80 0 1 0 1: f1/100 0 1 1 0: f1/112 0 1 1 1: f1/128 1 0 0 0: f1/56 1 0 0 1: f1/80 1 0 1 0: f1/96 1 0 1 1: f1/128 1 1 0 0: f1/160 1 1 0 1: f1/200 1 1 1 0: f1/224 1 1 1 1: f1/256	R/W
b1	CKS1			R/W
b2	CKS2			R/W
b3	CKS3			R/W
b4	TRS	Transmit/receive select bit (2, 3, 4, 5, 6)	0: Receive mode 1: Transmit mode	R/W
b5	MST	Master/slave select bit (4, 5, 7)	0: Slave mode 1: Master mode	R/W
b6	RCVD	Receive disable bit (8)	After the SIRDR register is read while TRS = 0, 0: Next receive operation continues 1: Next receive operation disabled	R/W
b7	ICE	I²C bus interface enable bit (9)	0: Output from SCL and SDA is disabled (Input to SCL and SDA is enabled) 1: Transfer with I²C bus function is enabled	R/W

Notes:

1. In master mode, set these bits according to the required transfer rate. For details on the transfer rate, refer to **Tables 22.9** and **22.10 Transfer Rate Examples**. In slave mode, a transfer clock is used for maintaining the data setup time in transmit mode. For details on this function, refer to **22.4.2.5.1 Maintaining Data Setup Time during I²C Slave Transmit Operation**.
2. Rewrite the TRS bit between transfer frames.
3. In slave receive mode, when the first 7 bits after the start condition match the slave address set in the SIMR2 register and the 8th bit is 1, the TRS bit is set to 1 (transmit mode).
4. If arbitration is lost in master mode of I²C bus interface mode, bits MST and TRS are set to 0 and slave receive mode is entered.
5. In multimaster operation, use the MOV instruction to set bits TRS and MST.
6. When the TRS bit is 1, do not set the RCVD bit to 1.
7. When an overrun error occurs in master receive mode of clock synchronous serial mode, the MST bit is set to 0 and slave receive mode is entered.
8. When the MST bit is 0 (slave mode), do not set the RCVD bit to 1.
9. When 0 is written to the ICE bit or 1 is written to the SIRST bit in the SICR2 register while the I²C bus function is operating, the values of the BBSY bit in the SICR2 register and the STOP bit in the SISR register may be undefined. Refer to **22.5 Notes on Clock Synchronous Serial Interface**.

22.2.6 SI Control Register 2 (SICR2)

In the SICR2 register, the bit functions differ between the SSU and I2C bus functions.

22.2.6.1 SSU Function

Address 000E7h (SICR2_0), 000F7h (SICR2_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BBSY	SCP	SDAO	SDAOP	SCLO	—	SIRST	—
After Reset	0	1	1	1	1	1	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b1	SIRST	Control block reset bit	When a hang-up occurs due to communication failure during operation, writing 1 initializes the control block without setting ports or initializing registers (1).	R/W
b2	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b3	SCLO	Reserved	Set to 1.	R
b4	SDAOP	SDAO write protect bit (2)	If 0 is written, the output level can be changed by the SDAO bit. Writing 1 has no effect. The read value is 1.	R/W
b5	SDAO	Serial data output value control bit (3)	The serial data output can be monitored by reading this bit: 0: Serial data output is low 1: Serial data output is high When written: (2, 4) 0: Data output is set to low 1: Data output is set to high	R/W
b6	SCP	Reserved	Set to 1.	R/W
b7	BBSY	Reserved	Set to 0.	R/W

Notes:
1. All SFRs except the shift register, bits SCLO and SDAO, and bits BC0 to BC3 in the SIMR1 register.
2. When writing to the SDAO bit, write 0 to the SDAOP bit and write 0 to the SDAO bit simultaneously using the MOV instruction.
3. Do not rewrite this bit in 4-wire bus communication mode.
4. For the data output after serial data transmission, the last bit value of the transmitted serial data is retained. If the content of the SDAO bit is rewritten before or after serial data transmission, the change is immediately reflected in the data output until transfer starts. Do not write to the SDAO bit during data transfer.

22.2.6.2 I²C bus Function

Address 000E7h (SICR2_0), 000F7h (SICR2_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BBSY	SCP	SDAO	SDAOP	SCLO	—	SIRST	—
After Reset	0	1	1	1	1	1	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b1	SIRST	Control block reset bit	When a hang-up occurs due to communication failure during operation, writing 1 initializes the control block without setting ports or resetting registers (1).	R/W
b2	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b3	SCLO	SCL monitor flag	0: SCL pin is set to low 1: SCL pin is set to high	R
b4	SDAOP	SDAO write protect bit (2)	When rewriting the SDAO bit, write 0 to this bit simultaneously. The read value is 1.	R/W
b5	SDAO	Serial data output value control bit	The serial data output can be monitored by reading this bit: 0: Serial data output is low 1: Serial data output is high When written: (2, 3) 0: Serial data output is set to low 1: Serial data output is set to high	R/W
b6	SCP	Start/stop condition generation disable bit (4)	When writing to the BBSY bit, write 0 to this bit simultaneously. The read value is 1. Writing 1 has no effect.	R/W
b7	BBSY	Bus busy bit (4, 5, 6)	When read: 0: Bus is released (SDA signal changes from low to high while SCL signal is held high) 1: Bus is occupied (SDA signal changes from high to low while SCL signal is held high) When written: 0: Stop condition generated 1: Start condition generated	R/W

Notes:
1. All SFRs except the shift register, bits SCLO and SDAO, and bits BC0 to BC3 in the SIMR1 register.
2. When rewriting the SDAO bit, write 0 to the SDAOP bit simultaneously using the MOV instruction.
3. For the data output after serial data transmission, the last bit value of the transmitted serial data is retained. If the content of the SDAO bit is rewritten before or after serial data transmission, the change is immediately reflected in the data output until transmission starts. Do not write to the SDAO bit during transfer operation.
4. Enabled in master mode with the I²C bus function. When writing to the BBSY bit, write 0 to the SCP bit simultaneously using the MOV instruction. Execute the same way when a start condition is regenerated.
5. Disabled in clock synchronous serial mode.
6. When 0 is written to the ICE bit in the SICR1 register or 1 is written to the SIRST bit in the SICR2 register while the I²C bus function is operating, the values of the BBSY bit in the SICR2 register and the STOP bit in the SISR register may be undefined. Refer to **22.5 Notes on Clock Synchronous Serial Interface**. To reset the control block in I²C bus interface mode, follow **22.4.8 Procedure for Resetting Control Block in I²C bus Interface Mode**. This can be used to prevent the values of bits BBSY and STOP from becoming undefined. When the control block is reset in SSU bus interface mode (clock synchronous communication mode, 4-wire bus communication mode) and clock synchronous serial mode, set TE_NAKIE and RE_STIE again after the control block is reset.

   Even if a start condition is generated by writing 0 to the SDAO bit, the state does not change the transfer enabled state. Only generation of a start condition by writing 1 to the BBSY bit is enabled.
   Since the SCL signal is held low, no stop condition can be generated by writing 1 to the SDAO bit. Generate a stop condition by writing 0 to the BBSY bit.

22.2.7 SI Mode Register 1 (SIMR1)

In the SIMR1 register, the bit functions differ between the SSU and I^2C bus functions.

22.2.7.1 SSU Function

Address 000E8h (SIMR1_0), 000F8h (SIMR1_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MLS	CPOS_WAIT	CPHS	—	BC3	BC2	BC1	BC0
After Reset	0	0	0	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BC0	Bit counter (1)	b3 b2 b1 b0 0 0 0 0: Remaining 16 bits 0 0 0 1: Remaining 1 bit 0 0 1 0: Remaining 2 bits 0 0 1 1: Remaining 3 bits 0 1 0 0: Remaining 4 bits 0 1 0 1: Remaining 5 bits 0 1 1 0: Remaining 6 bits 0 1 1 1: Remaining 7 bits 1 0 0 0: Remaining 8 bits 1 0 0 1: Remaining 9 bits 1 0 1 0: Remaining 10 bits 1 0 1 1: Remaining 11 bits 1 1 0 0: Remaining 12 bits 1 1 0 1: Remaining 13 bits 1 1 1 0: Remaining 14 bits 1 1 1 1: Remaining 15 bits	R
b1	BC1			R
b2	BC2			R
b3	BC3			R
b4	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b5	CPHS	Transfer clock phase select bit (2)	0: Data change at odd edge (data download at even edge) 1: Data change at even edge (data download at odd edge)	R/W
b6	CPOS_WAIT	Clock select bit (2)	0: High when clock stops 1: Low when clock stops	R/W
b7	MLS	MSB first/LSB first select bit	0: Data transfer with MSB first 1: Data transfer with LSB first	R/W

Notes:
1. When the SSU function is used (the IICSEL bit in the IICCR register is 0 and the ICE bit in the SICR1 register is 0), writing has no effect.
2. For the settings of bits CPHS and CPOS_WAIT, refer to **22.3.1.2 Association between Transfer Clock Polarity, Phase, and Data**.
   When the MS bit in the SIMR2 register is 0 (clock synchronous communication mode), set the CPHS bit to 0 and the CPOS_WAIT bit to 0.

Bits BC0 to BC3 (Bit counter)

The state of the shift register during transmission/reception can be read.

22.2.7.2 I²C bus Function

Address 000E8h (SIMR1_0), 000F8h (SIMR1_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MLS	CPOS_WAIT	CPHS	—	BC3	BC2	BC1	BC0
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BC0	Bit counters 0 to 2	I²C bus interface mode (Read: Number of remaining transfer bits; Write: Number of next transfer data bits) (1) b2 b1 b0 0 0 0: 9 bits (2) 0 0 1: 2 bits 0 1 0: 3 bits 0 1 1: 4 bits 1 0 0: 5 bits 1 0 1: 6 bits 1 1 0: 7 bits 1 1 1: 8 bits Clock synchronous serial mode (Read: Number of remaining transfer bits; Write: Always 000b) b2 b1 b0 0 0 0: 8 bits 0 0 1: 1 bit 0 1 0: 2 bits 0 1 1: 3 bits 1 0 0: 4 bits 1 0 1: 5 bits 1 1 0: 6 bits 1 1 1: 7 bits	R/W
b1	BC1			R/W
b2	BC2			R/W
b3	BC3	Bit counter 3	When rewriting bits BC0 to BC2, write 0 to this bit simultaneously. (1, 3) The read value is 1.	R/W
b4	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b5	CPHS	Reserved	Set to 0.	R/W
b6	CPOS_WAIT	Wait insertion bit (4)	0: No wait states (Data and the acknowledge bit are transferred consecutively) 1: Wait states (After the clock of the last data bit falls, a low-level period is extended for two transfer clocks)	R/W
b7	MLS	MSB first/LSB first select bit	0: Data transfer with MSB first (5) 1: Data transfer with LSB first	R/W

Notes:
1. When writing to bits BC0 to BC2, write 0 to the BC3 bit simultaneously using the MOV instruction. The write value of bits BC0 to BC2 when 1 is written is invalid.
2. After data including the acknowledge bit is transferred, bits BC2 to BC0 are automatically set to 000b. When a start condition is detected, these bits are automatically set to 000b.
3. Do not rewrite this bit in clock synchronous serial mode.
4. The setting value is valid in master mode of I²C bus interface mode. The value is invalid in slave mode of I²C bus interface mode and in clock synchronous serial mode.
5. Set to 0 in I²C bus interface mode.

22.2.8 SI Interrupt Enable Register (SIER)

In the SIER register, the bit functions differ between the SSU and I^2C bus functions.

22.2.8.1 SSU Function

Address 000E9h (SIER_0), 000F9h (SIER_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIE	TEIE	RIE	TE_NAKIE	RE_STIE	ACKE	ACKBR	CEIE_ACKBT
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CEIE_ACKBT	Conflict error interrupt enable bit	0: Conflict error interrupt request disabled 1: Conflict error interrupt request enabled	R/W
b1	ACKBR	Reserved	The read value is 0.	R
b2	ACKE	Reserved	Set to 0.	R/W
b3	RE_STIE	Reception enable bit (1)	0: Reception disabled 1: Reception enabled	R/W
b4	TE_NAKIE	Transmission enable bit	0: Transmission disabled 1: Transmission enabled	R/W
b5	RIE	Receive interrupt enable bit	0: Receive data full and overrun error interrupt requests disabled 1: Receive data full and overrun error interrupt requests enabled	R/W
b6	TEIE	Transmit end interrupt enable bit	0: Transmit end interrupt request disabled 1: Transmit end interrupt request enabled	R/W
b7	TIE	Transmit interrupt enable bit	0: Transmit data empty interrupt request disabled 1: Transmit data empty interrupt request enabled	R/W

Note:
1. In 4-wire bus (multidirectional) communication mode, do not set both the TE_NAKIE and RE_STIE bits to 1. If these bits are set to 1, the RE_STIE is set to 0.

22.2.8.2 I²C bus Function

Address 000E9h (SIER_0), 000F9h (SIER_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIE	TEIE	RIE	TE_NAKIE	RE_STIE	ACKE	ACKBR	CEIE_ACKBT
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CEIE_ACKBT	Transmit acknowledge select bit	0: In receive mode, 0 is transmitted as the acknowledge bit 1: In receive mode, 1 is transmitted as the acknowledge bit	R/W
b1	ACKBR	Receive acknowledge bit	0: In transmit mode, the acknowledge bit received from the receive device is 0 1: In transmit mode, the acknowledge bit received from the receive device is 1	R
b2	ACKE	Acknowledge bit detection select bit	0: Content of the receive acknowledge bit is ignored and continuous transfer is performed 1: When the receive acknowledge bit is 1, transfer is halted	R/W
b3	RE_STIE	Stop condition detection interrupt enable bit	0: Stop condition detection interrupt request disabled 1: Stop condition detection interrupt request enabled (1)	R/W
b4	TE_NAKIE	NACK receive interrupt enable bit	0: NACK receive interrupt request and arbitration lost/overrun error interrupt request disabled 1: NACK receive interrupt request and arbitration lost/overrun error interrupt request enabled (2)	R/W
b5	RIE	Receive interrupt enable bit	0: Receive data full and overrun error interrupt request disabled 1: Receive data full and overrun error interrupt request enabled (3)	R/W
b6	TEIE	Transmit end interrupt enable bit	0: Transmit end interrupt request disabled 1: Transmit end interrupt request enabled	R/W
b7	TIE	Transmit interrupt enable bit	0: Transmit data empty interrupt request disabled 1: Transmit data empty interrupt request enabled	R/W

Notes:
1. When the STOP bit in the SISR register is 0, set the RE_STIE bit to 1 (stop condition detection interrupt request enabled).
2. Enabling the overrun error interrupt request with the TE_NAKIE bit is valid in clock synchronous serial mode.
3. Enabling the overrun error interrupt request with the RIE bit is invalid in I²C bus interface mode.

22.2.9 SI Status Register (SISR)

In the SISR register, the bit functions differ between the SSU and I2C bus functions.

22.2.9.1 SSU Function

Address 000EAh (SISR_0), 000FAh (SISR_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TDRE	TEND	RDRF	NACKF	STOP	ORER_AL	AAS	CE_ADZ
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CE_ADZ	Conflict error flag (1)	0: No conflict error 1: Conflict error (2)	R/W
b1	AAS	Reserved	Set to 0.	R/W
b2	ORER_AL	Overrun error flag (1)	0: No overrun error 1: Overrun error (3)	R/W
b3	STOP	Reserved	Set to 0.	R/W
b4	NACKF			R/W
b5	RDRF	Receive data register full flag (1, 4)	0: No data in the SIRDR register 1: Data present in the SIRDR register	R/W
b6	TEND	Transmit end flag (1, 5)	0: The TDRE bit is 0 when the last bit of transmit data is transmitted 1: The TDRE bit is 1 when the last bit of transmit data is transmitted	R/W
b7	TDRE	Transmit data empty flag (1, 5, 6)	0: Data is not transferred from registers SITDR to SISDR 1: Data is transferred from registers SITDR to SISDR	R/W

Notes:

1. Writing 1 to bits CE_ADZ, ORER_AL, RDRF, TEND, and TDRE has no effect. To set any of these bits to 0, write 0 after reading it as 1.
2. When starting a serial communication while the MS bit in the SIMR2 register is 1 (4-wire bus communication mode) and the MST bit in the SICR1 register is 1 (master mode), the CE_ADZ bit is set to 1 if the $\overline{SCS}$ pin input is low. Refer to **22.3.3.4 $\overline{SCS}$ Pin Control and Arbitration**.
   When the $\overline{SCS}$ pin input changes from low to high during transfer while the MS bit in the SIMR2 register is 1 (4-wire bus communication mode) and the MST bit in the SICR1 register is 0 (slave mode), the CE_ADZ bit is set to 1.
3. Indicates an overrun error has occurred during reception and reception is terminated in error. If the next serial data receive operation is completed while the RDRF bit is 1 (data present in the SIRDR register), the ORER_AL bit is set to 1.
   After the ORER_AL bit is set to 1 (overrun error), no reception can be performed while the RDRF bit is 1. Also, no transmission can be performed while the MST bit is 1 (master mode).
4. The RDRF bit is set to 0 when data is read from the SIRDR register. Do not clear this bit by writing 0 when not in I2C bus interface mode or when not clearing the RDRF bit after DTC access.
5. Bits TEND and TDRE are set to 0 when data is written to the SITDR register.
6. When the SSU function is used, the TDRE bit is set to 1 when the TE_NAKIE bit in the SIER register is set to 1 (transmission enabled).

22.2.9.2 I²C bus Function

Address 000EAh (SISR_0), 000FAh (SISR_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TDRE	TEND	RDRF	NACKF	STOP	ORER_AL	AAS	CE_ADZ
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CE_ADZ	General call address recognition flag (1, 2)	This flag is set to 1 when a general call address is detected.	R/W
b1	AAS	Slave address recognition flag (1)	This flag is set to 1 when the first frame immediately after the start condition matches bits SVA0 to SVA6 in the SIMR2 register in slave receive mode (slave address detection, general call address detection).	R/W
b2	ORER_AL	Arbitration lost flag/overrun error flag (1)	In I²C bus interface mode, this flag indicates that arbitration is lost in master mode. This flag is set to 1 when: (3) • The internal SDA signal and SDA pin level do not match at the rising edge of the SCL signal in master transmit mode • The SDA pin is held high at start condition detection in master transmit/receive mode In clock synchronous serial mode, this bit indicates that an overrun error has occurred. This flag is set to 1 when: • The last bit of the next data is received while the RDRF bit is set to 1.	R/W
b3	STOP	Stop condition detection flag (1, 7)	This flag is set to 1 when a stop condition is detected after the frame is transferred.	R/W
b4	NACKF	No acknowledge detection flag (1, 4)	This flag is set to 1 when no ACKnowledge is detected from the receive device after transmission.	R/W
b5	RDRF	Receive data register full flag (1, 5)	This flag is set to 1 when receive data is transferred from registers SISDR to SIRDR.	R/W
b6	TEND	Transmit end flag (1, 6)	In I²C bus interface mode, this flag is set to 1 at the rising edge of the 9th clock cycle of the SCL signal while the TDRE bit is 1. In clock synchronous mode, this flag is set to 1 when the last bit of the transmit frame is transmitted.	R/W
b7	TDRE	Transmit data empty flag (1, 6)	This flag is set to 1 when: • Data is transferred from registers SITDR to SISDR and the SITDR register becomes empty. • The TRS bit in the SICR1 register is set to 1 (transmit mode) • A start condition is generated (including retransmission) • Slave receive mode is changed to slave transmit mode	R/W

Notes:
1. Writing 1 to these bits has no effect. Each of these bits is set to 0 by writing 0 after reading it as 1.
2. Enabled in slave receive mode of I²C bus interface mode.
3. When two or more master devices attempt to occupy the bus at nearly the same time, if the I²C bus interface monitors the SDA pin and the data which the I²C bus interface transmits is different, the ORER_AL bit is set to 1 indicating the bus is occupied by another master.
4. The NACKF bit is enabled when the ACKE bit in the SIER register is 1 (when the receive acknowledge bit is 1, transfer is halted).
5. The RDRF bit is set to 0 when data is read from the SIRDR register. Do not clear this bit by writing 0 when not in I²C bus interface mode or when not clearing the RDRF bit after DTC access.
6. Bits TEND and TDRE are set to 0 when data is written to the SITDR register.
7. When 0 is written to the ICE bit in the SICR1 register or 1 is written to the SIRST bit in the SICR2 register while the I²C bus function is operating, the values of the BBSY bit in the SICR2 register and the STOP bit in the SISR register may be undefined. Refer to **22.5 Notes on Clock Synchronous Serial Interface**. To reset the control block in I²C bus interface mode, follow **22.4.8 Procedure for Resetting Control Block in I²C bus Interface Mode**. This can be used to prevent the values of bits BBSY and STOP from becoming undefined. When the control block is reset in SSU bus interface mode (clock synchronous communication mode, 4-wire bus communication mode) and clock synchronous serial mode, set TE_NAKIE and RE_STIE again after the control block is reset.

22.2.10 SI Mode Register 2 (SIMR2)

In the SIMR2 register, the bit functions differ between the SSU and I^2C bus functions.

22.2.10.1 SSU Function

Address 000EBh (SIMR2_0), 000FBh (SIMR2_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BIDE	SCKS	CSS1	CSS0	SCKOS	SOOS	CSOS	MS
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MS	Mode select bit (1)	0: Clock synchronous communication mode 1: 4-wire bus communication mode	R/W
b1	CSOS	$\overline{SCS}$ pin open-drain output select bit (2, 3, 4, 5)	0: CMOS output 1: N-channel open-drain output	R/W
b2	SOOS	Serial data open-drain output select bit (1, 4)	0: CMOS output (6) 1: N-channel open-drain output	R/W
b3	SCKOS	SSCK pin open-drain output select bit (4, 7)	0: CMOS output 1: N-channel open-drain output	R/W
b4	CSS0	$\overline{SCS}$ pin select bits (5, 8)	b5 b4 0 0: Functions as a port 0 1: Functions as the $\overline{SCS}$ input pin 1 0: Functions as the $\overline{SCS}$ output pin (9) 1 1: Functions as the $\overline{SCS}$ output pin (9)	R/W
b5	CSS1			R/W
b6	SCKS	SSCK pin select bit (7)	0: Functions as a port 1: Functions as the serial clock pin	R/W
b7	BIDE	Bidirectional mode enable bit (1, 10)	0: Standard mode (communication using two pins for data input and data output) 1: Bidirectional mode (communication using one pin for data input and data output)	R/W

Notes:

1. Refer to **22.3.1.3 Association between Data I/O Pins and SS Shift Register** for information on combinations of data I/O pins.
2. When using 4-wire bus communication mode, always use the $\overline{SCS}$ pin as N-channel open-drain output.
3. When the $\overline{SCS}$ pin is used as CMOS output, a conflict error may occur when $\overline{SCS}$ output is enabled. After the error flag is cleared, set to master mode again to continue communication.
4. Set bits CSOS, SOOS, and SCKOS to 0 (CMOS output) when this module is not used.
5. Do not set bits CSOS, CSS0, and CSS1 simultaneously. When the $\overline{SCS}$ pin is selected, first set the CSOS bit and then set bits CSS1 and CSS0 to 01b, 10b, or 11b. When the $\overline{SCS}$ pin is not selected, first set bits CSS1 and CSS0 to 00b and then set the CSOS bit.
6. When the SOOS bit is 0, set the port direction register bits corresponding to pins SSI and SSO to 0 (input mode).
7. Do not set bits SCKOS and SCKS simultaneously. When the SSCK pin is selected, set the SCKOS bit before setting the SCKS bit to 1 (functions as the serial clock pin). When the SSCK pin is not selected, set the SCKS bit to 0 (function as a port) before setting the SCKOS bit.
8. When the MS bit is 0 (clock synchronous communication mode), the $\overline{SCS}$ pin functions as a port regardless of the content of bits CSS0 and CSS1.
9. This bit functions as the $\overline{SCS}$ input pin before transfer starts.
10. The BIDE bit is disabled when the MS bit is 0 (clock synchronous communication mode).

22.2.10.2 I²C bus Function

Address 000EBh (SIMR2_0), 000FBh (SIMR2_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SVA6	SVA5	SVA4	SVA3	SVA2	SVA1	SVA0	MS
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MS	Mode select bit	0: I²C bus interface mode 1: Clock synchronous serial mode	R/W
b1	SVA0	Slave addresses (1)	Set an address different from that of the other slave devices connected to the I²C bus. When the higher 7 bits of the first frame transmitted after the start condition match bits SVA0 to SVA6 in slave mode of I²C bus interface mode, the MCU operates as a slave device.	R/W
b2	SVA1			R/W
b3	SVA2			R/W
b4	SVA3			R/W
b5	SVA4			R/W
b6	SVA5			R/W
b7	SVA6			R/W

Note:
1. Do not set 1111XXXb and 0000XXXb as slave addresses.

22.3 Synchronous Serial Communication Unit (SSU) Operation

22.3.1 Items Common to Clock Synchronous Communication Mode and 4-Wire Bus Communication Mode

22.3.1.1 Transfer Clock

The transfer clock can be selected from among seven internal clocks (f1/256, f1/128, f1/64, f1/32, f1/16, f1/8, and f1/4) and an external clock.

To use the synchronous serial communication unit, set the SCKS bit in the SIMR2 register to 1 and then select the SSCK pin as the serial clock pin.

When the MST bit in the SICR1 register is 1 (master mode), an internal clock is selected and the SSCK pin functions as output. When transfer is started, the SSCK pin outputs a clock of the transfer rate selected by bits CKS0 to CKS2 in the SICR1 register.

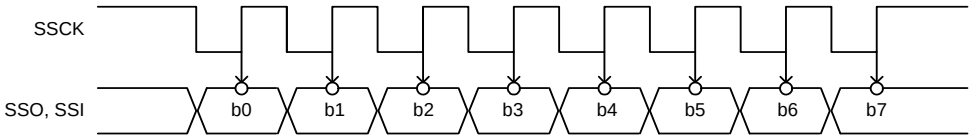
When the MST bit is 0 (slave mode), an external clock is selected and the SSCK pin functions as input.

22.3.1.2 Association between Transfer Clock Polarity, Phase, and Data

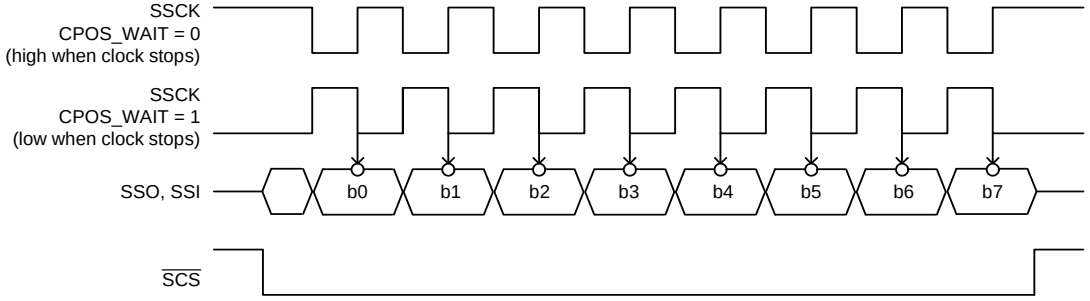
The association between the transfer clock polarity, phase and, data changes according to the combinations of the MS bit in the SIMR2 register and bits CPHS and CPOS_WAIT in the SIMR1 register. Figure 22.4 shows the Association between Transfer Clock Polarity, Phase, and Transfer Data.

Also, MSB-first transfer or LSB-first transfer can be selected by setting the MLS bit in the SIMR1 register. When the MLS bit is 1, transfer is started from the LSB and proceeds to the MSB. When the MLS bit is 0, transfer is started from the MSB and proceeds to the LSB.

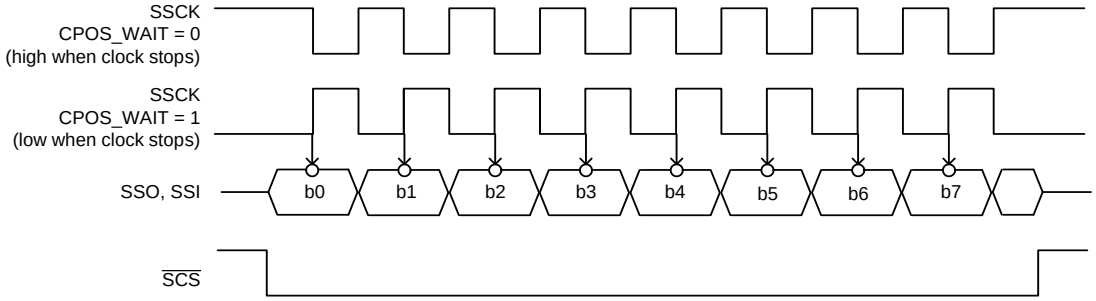
• MS = 0 (clock synchronous communication mode), CPHS = 0 (data change at odd edge), CPOS_WAIT = 0 (high when clock stops), and MLS = 1 (LSB-first transfer)



• MS = 1 (4-wire bus communication mode), CPHS = 0 (data change at odd edge), and MLS = 1 (LSB-first transfer)



• MS = 1 (4-wire bus communication mode), CPHS = 1 (data download at odd edge), and MLS = 1 (LSB-first transfer)



CPHS, CPOS_WAIT, MLS: Bits in SIMR1 register
MS: Bit in SIMR2 register

Figure 22.4 Association between Transfer Clock Polarity, Phase, and Transfer Data

22.3.1.3 Association between Data I/O Pins and SS Shift Register

The connection between the data I/O pins and the SISDR register changes according to the combinations of the MST bit in the SICR1 register and the MS bit in the SIMR2 register. The connection also changes according to the BIDE bit in the SIMR2 register. Figure 22.5 shows the Association between Data I/O Pins and SISDR Register.

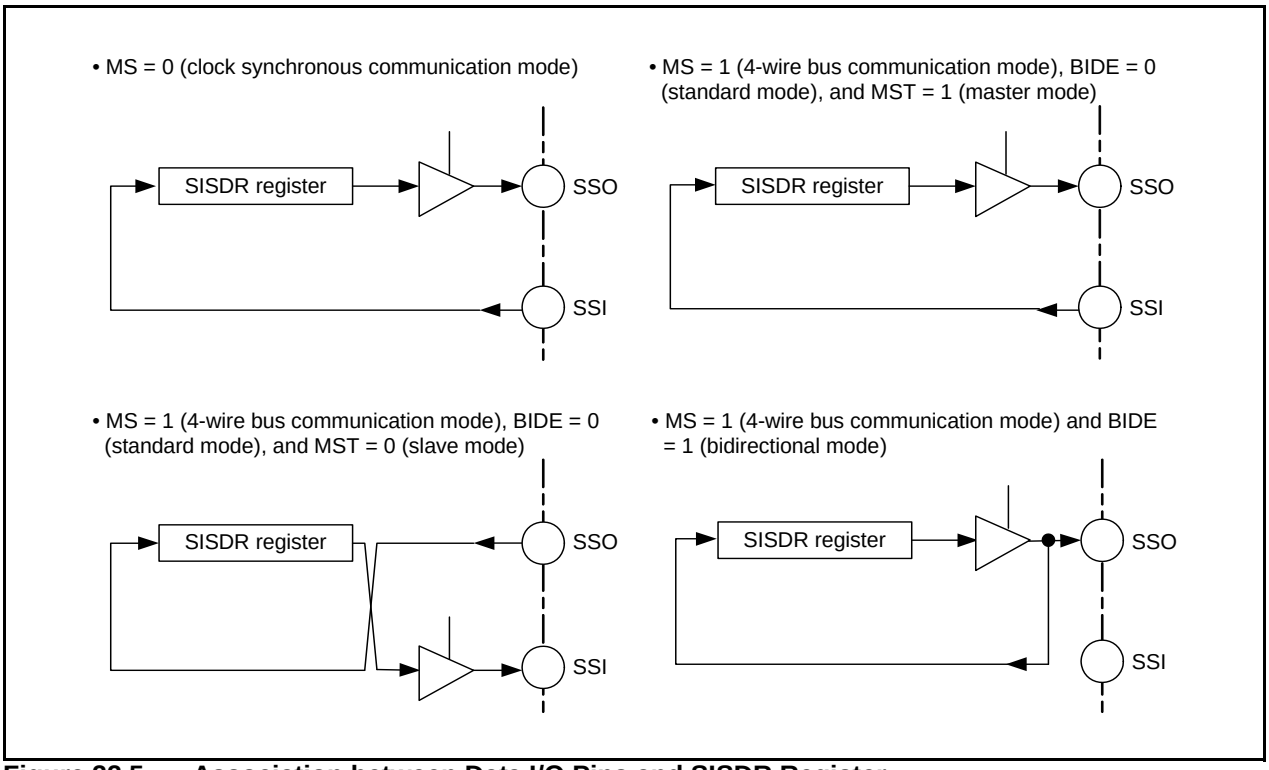


Figure 22.5 Association between Data I/O Pins and SISDR Register

22.3.1.4 Interrupt Requests

The synchronous serial communication unit has five interrupt requests: transmit data empty, transmit end, receive data full, overrun error, and conflict error. Because these interrupt requests are assigned to the synchronous serial communication unit interrupt vector table, interrupt sources must be determined using the flags. Table 22.7 lists the Interrupt Requests of Synchronous Serial Communication Unit.

Table 22.7 Interrupt Requests of Synchronous Serial Communication Unit

Interrupt Request	Abbreviation	Generation Condition
Transmit data empty	TXI	TIE = 1 and TDRE = 1
Transmit end	TEI	TEIE = 1 and TEND = 1
Receive data full	RXI	RIE = 1 and RDRF = 1
Overrun error	OEI	RIE = 1 and ORER_AL = 1
Conflict error	CEI	CEIE_ACKBT = 1 and CE_ADZ = 1 (1)

CEIE_ACKBT, RIE, TEIE, TIE: Bits in SIER register
CE_ADZ, ORER_AL, RDRF, TEND, TDRE: Bits in SISR register
Note:
1. Not generated in clock synchronous communication mode.

If the generation conditions in Table 22.7 are met, a synchronous serial communication unit interrupt request is generated. Set each interrupt source to 0 in the synchronous serial communication unit interrupt routine.

Note that bits TDRE and TEND in the SISR register are automatically set to 0 by writing transmit data to the SITDR register and the RDRF bit in the SISR register is automatically set to 0 by reading the SIRDR register. In particular, the TDRE bit is set back to 1 (data is transferred from registers SITDR to SISDR) at the same time transmit data is written to the SITDR register. If the TDRE bit is set to 0 (data is not transferred from registers SITDR to SISDR) by any method other than the above (register access by software), an additional 1 byte of transferred data may be transmitted.

22.3.1.5 Communication Modes and Pin Functions

The synchronous serial communication unit changes the functions of the I/O pins in each communication mode according to the settings of the MST bit in the SICR1 register and bits RE_STIE and TE_NAKIE in the SIER register. Table 22.8 lists the Association between Communication Modes and I/O Pins.

Table 22.8 Association between Communication Modes and I/O Pins

Communication Mode	Bit Setting					Pin State		
	MS	BIDE	MST	TE_NAKIE	RE_STIE	SSI	SSO	SSCK
Clock synchronous communication mode	0	Disabled	0	0	1	Input	—	Input
				1	0	—	Output	Input
					1	Input	Output	Input
			1	0	1	Input	—	Output
				1	0	—	Output	Output
					1	Input	Output	Output
4-wire bus communication mode	1	0	0	0	1	—	Input	Input
				1	0	Output	—	Input
					1	Output	Input	Input
			1	0	1	Input	—	Output
				1	0	—	Output	Output
					1	Input	Output	Output
4-wire bus (bidirectional) communication mode (1)	1	1	0	0	1	—	Input	Input
				1	0	—	Output	Input
			1	0	1	—	Input	Output
				1	0	—	Output	Output

—: Used as a programmable I/O port.
MS, BIDE: Bits in SIMR2 register
MST: Bit in SICR1 register
TE_NAKIE, RE_STIE: Bits in SIER register
Note:
1. Do not set both the TE_NAKIE and RE_STIE bits to 1 in 4-wire bus (bidirectional) communication mode.

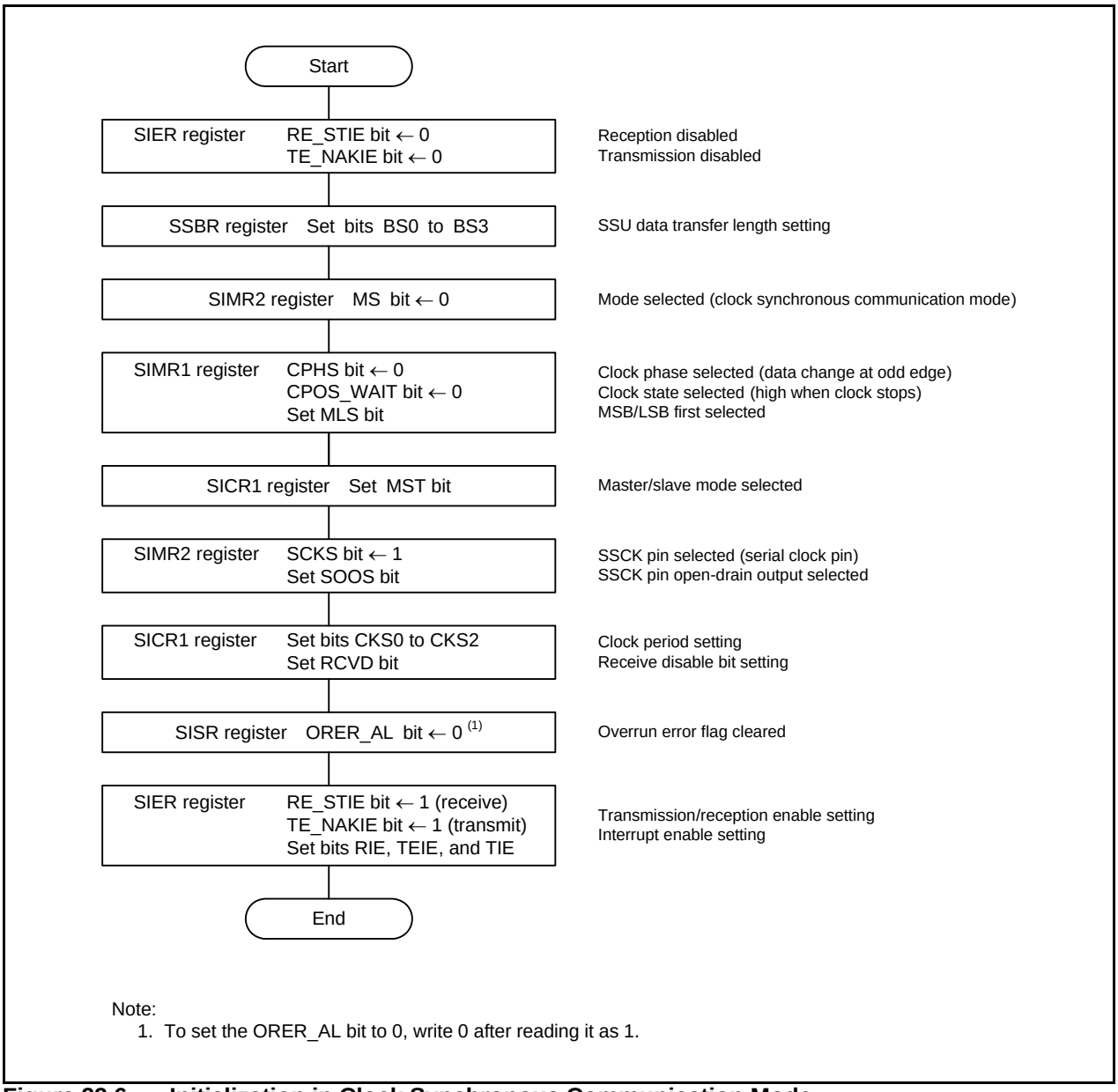
22.3.2 Clock Synchronous Communication Mode

22.3.2.1 Initialization in Clock Synchronous Communication Mode

Figure 22.6 shows the Initialization in Clock Synchronous Communication Mode. Before data transmission or reception, set the TE_NAKIE bit in the SIER register to 0 (transmission disabled) and the RE_ STIE bit to 0 (reception disabled) for initialization.

To change the communication mode (select clock synchronous communication mode by the mode select MS bit in the SIMR2 register) or the communication format, set the TE_NAKIE bit to 0 and the RE_STIE bit to 0 before making the change.

Even if the RE_STIE bit is set to 0, the contents of bits RDRF and ORER_AL in the SISR register and the SIRDR register are retained.



Note:
1. To set the ORER_AL bit to 0, write 0 after reading it as 1.

Figure 22.6 Initialization in Clock Synchronous Communication Mode

22.3.2.2 Data Transmission

Figure 22.7 shows an Operation Example during Data Transmission (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length). During data transmission, the synchronous serial communication unit operates as described below. (The data transfer length can be set from 8 to 16 bits using the SSBR register.)
When the MCU is set as the master device, it outputs a synchronous clock and data. When the MCU is set as a slave device, it outputs data synchronized with the input clock.
When the TE_NAKIE bit in the SIER register is set to 1 (transmission enabled) before writing the transmit data to the SITDR register, the TDRE bit in the SISR register is automatically set to 0 (data is not transferred from registers SITDR to SISDR) and the data is transferred from registers SITDR to SISDR. Then, the TDRE bit is set to 1 (data is transferred from registers SITDR to SISDR) and transmission is started. If the TIE bit in the SIER register is 1 at this time, a TXI interrupt request is generated.
When one frame of data is transferred while the TDRE bit is 0, data is transferred from registers SITDR to SISDR and the next frame transmission is started. If the 8th bit is transmitted while the TDRE bit is 1, the TEND bit in the SISR register is set to 1 (the TDRE bit is 1 when the last bit of transmit data is transmitted) and the state is retained. If the TEIE bit in the SIER register is 1 (transmit end interrupt request enabled) at this time, a TEI interrupt request is generated. The SSCK pin is held high after transmission is completed.
Transmission cannot be performed while the ORER_AL bit in the SISR register is 1 (overrun error). Confirm that the ORER_AL bit is 0 before transmission.
Figure 22.8 shows a Sample Flowchart for Data Transmission (Clock Synchronous Communication Mode).

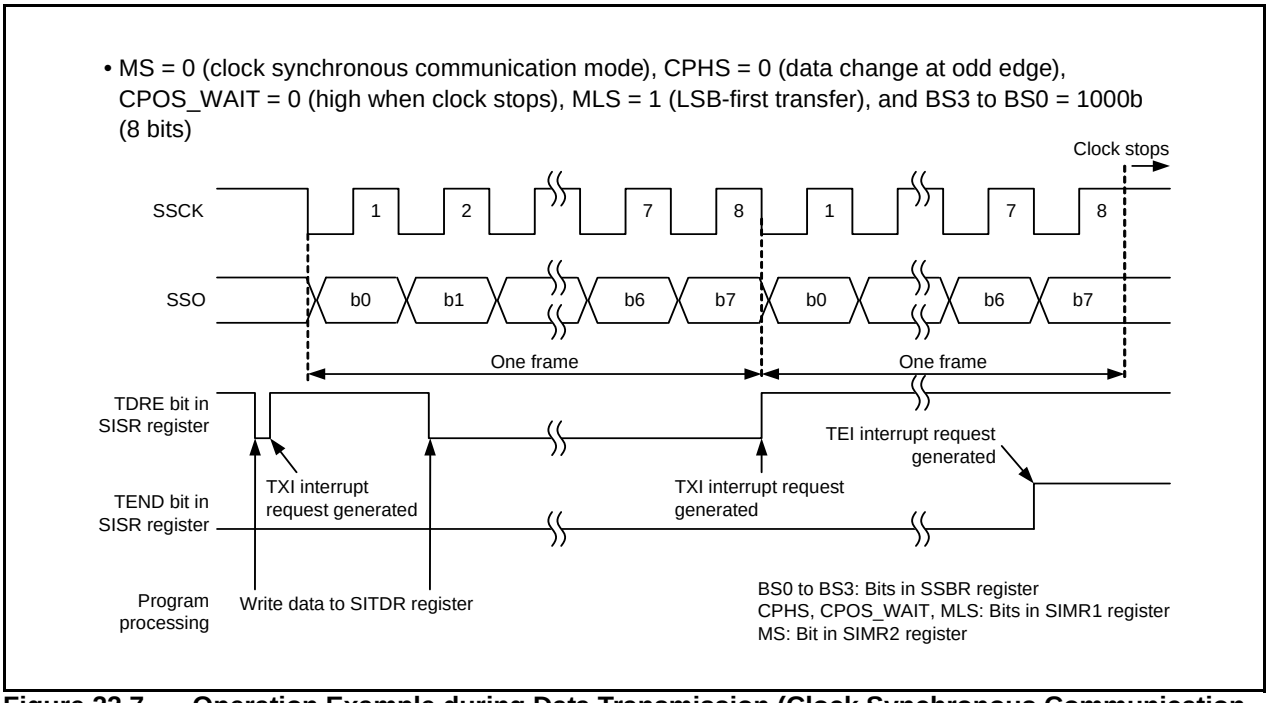
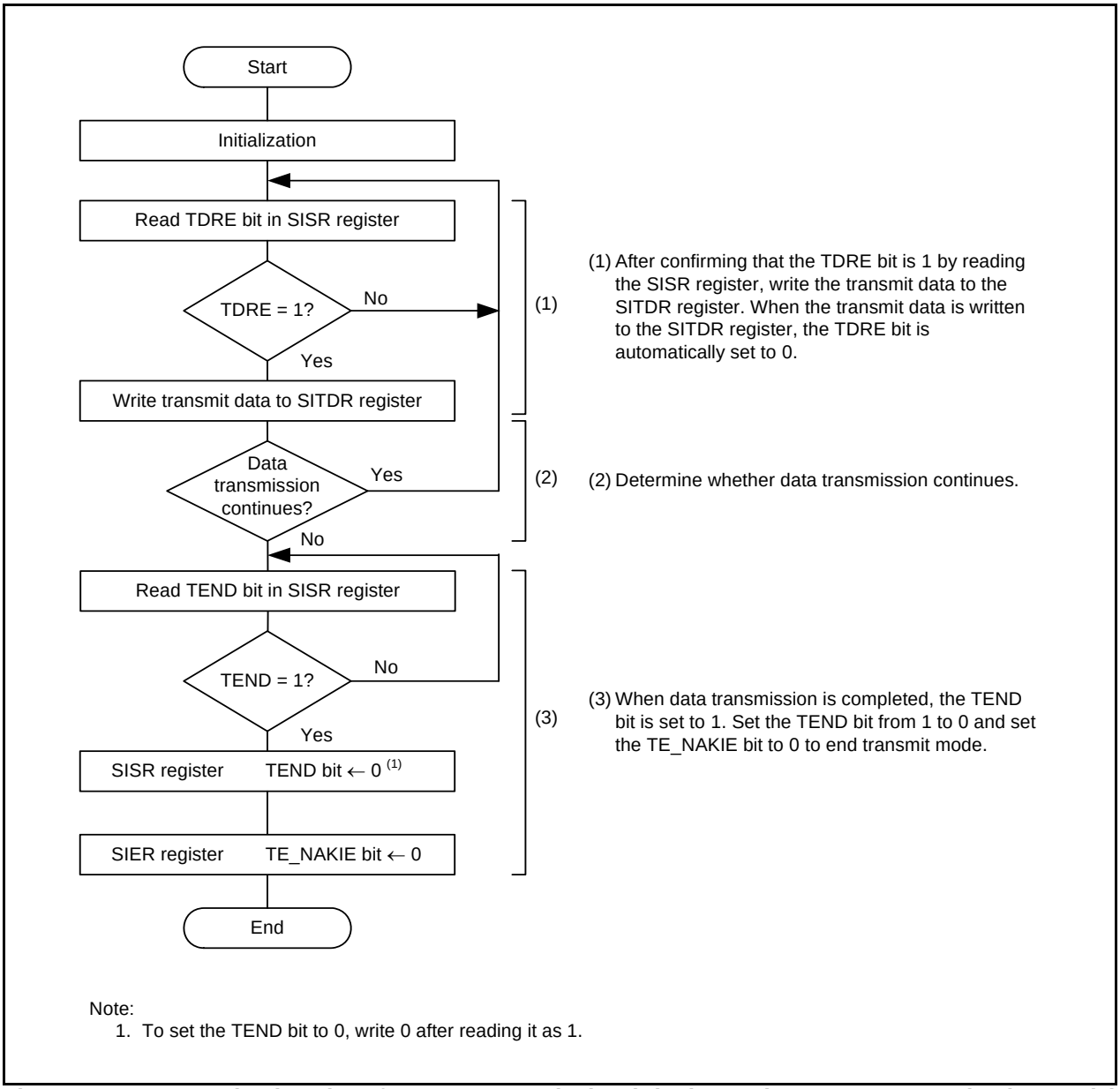


Figure 22.7 Operation Example during Data Transmission (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length)



Note:
1. To set the TEND bit to 0, write 0 after reading it as 1.

Figure 22.8 Sample Flowchart for Data Transmission (Clock Synchronous Communication Mode)

22.3.2.3 Data Reception

Figure 22.9 shows an Operation Example during Data Reception (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length). During data reception, the synchronous serial communication unit operates as described below. (The data transfer length can be set from 8 to 16 bits using the SSBR register.)

When the MCU is set as the master device, it outputs a synchronous clock and inputs data. When the MCU is set as a slave device, it inputs data synchronized with the input clock.

When the MCU is set as the master device, it outputs a receive clock and reception is started by performing a dummy read of the SIRDR register.

After 8 bits of data are received, the RDRF bit in the SISR register is set to 1 (data present in the SIRDR register) and receive data is stored in the SIRDR register. If the RIE bit in the SIER register is 1 (RXI and OEI interrupt requests enabled) at this time, an RXI interrupt request is generated. When the SIRDR register is read, the RDRF bit is automatically set to 0 (no data in the SIRDR register).

When the MCU is set as the master device and reception completes, set the RCVD bit in the SICR1 register to 1 (receive operation is completed after 1 byte of data is received) before reading the [last frame - 1] of the receive data. With this setting, the synchronous serial communication unit outputs a receive clock for the [last frame] and then stops. After that, set the RE_STIE bit in the SIER register to 0 (reception disabled) and the RCVD bit to 0 (receive operation continues after the 1 byte of data is received), and then read the last received data from the SIRDR register. If the SIRDR register is read while the RE_STIE bit is 1 (reception enabled), the receive clock is output again.

When the 8th clock rises while the RDRF bit is 1, the ORER_AL bit in the SISR register is set to 1 (overrun error: OEI) and the operation is stopped. While the ORER_AL bit is 1, reception cannot be performed. Confirm that the ORER_AL bit is 0 before restarting reception. If an overrun error occurs, the data received in the frame where the error has occurred is discarded.

Figure 22.10 shows a Sample Flowchart for Data Reception (MST = 1) (Clock Synchronous Communication Mode).

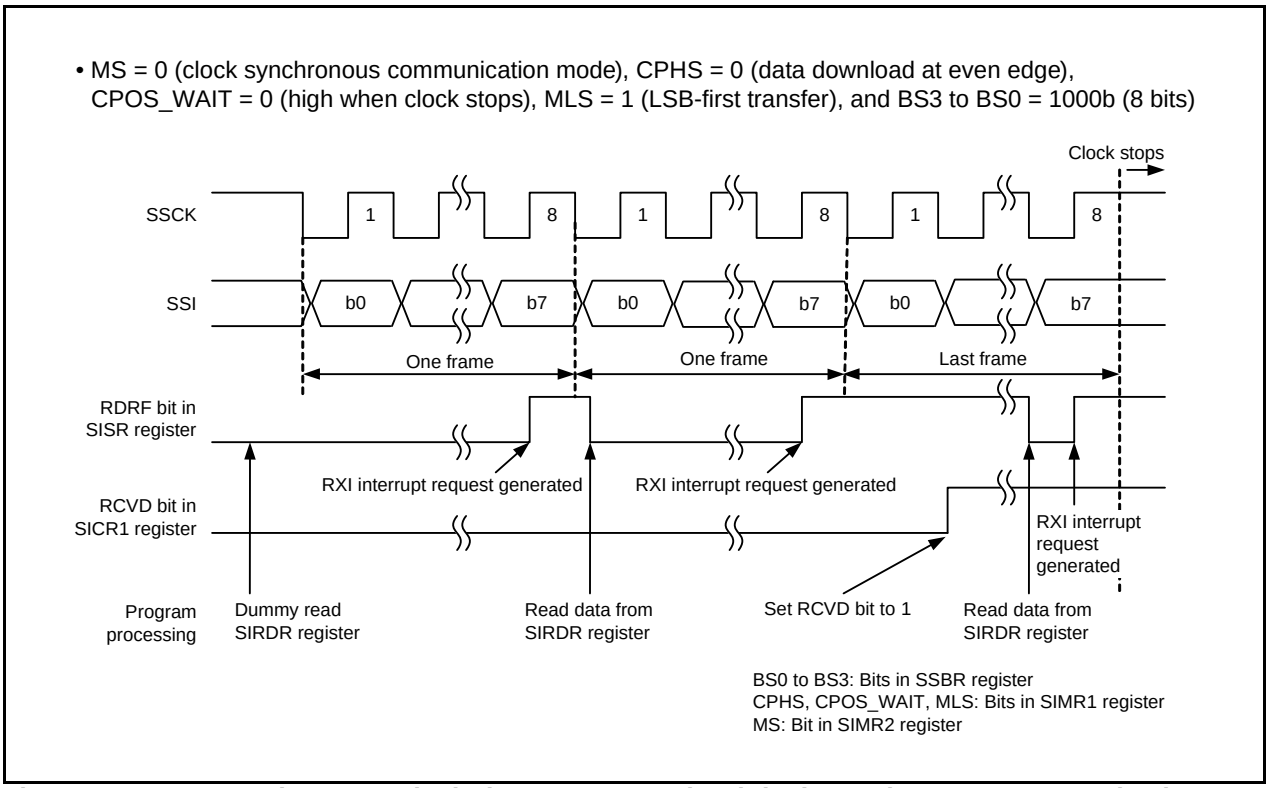


Figure 22.9 Operation Example during Data Reception (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length)

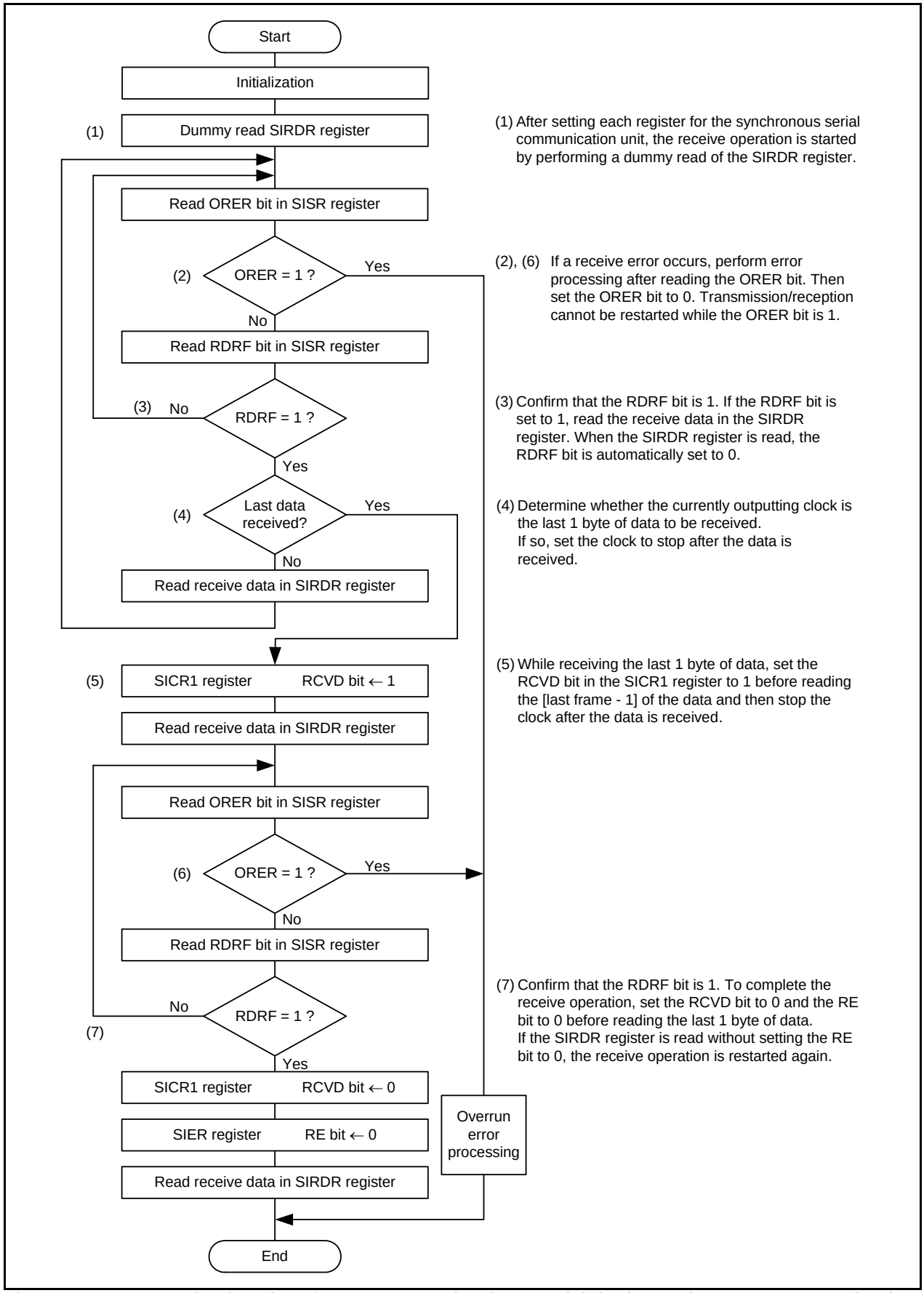


Figure 22.10 Sample Flowchart for Data Reception (MST = 1) (Clock Synchronous Communication Mode)

22.3.2.4 Data Transmission/Reception

Figure 22.11 shows an Operation Example during Data Transmission/Reception (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length).

Data transmission/reception is an operation combining data transmission and reception, which were described earlier.

Transmission/reception is started by writing data to the SITDR register. While the TDRE bit in the SISR register is 1 (data is transferred from registers SITDR to SISDR), if the last transfer clock (the data transfer length can be set from 8 to 16 bits using the SSBR register) rises or the ORER_AL bit in the SISR register is set to 1 (overrun error), the transmit/receive operation is stopped.

When switching from transmit mode (TE_NAKIE = 1) or receive mode (RE_STIE = 1) to transmit/receive mode (TE_NAKIE = RE_STIE = 1), set the TE_NAKIE bit in the SIER register to 0 and RE_STIE bit to 0 once before making the change. After confirming that the TEND bit in the SISR register is 0 (the TDRE bit is 0 when the last bit of transmit data is transmitted), the RDRF bit in the SISR register is 0 (no data in the SIRDR register), and the ORER_AL bit in the SISR register is 0 (no overrun error), set bits TE_NAKIE and RE_STIE to 1.

Figure 22.12 shows a Sample Flowchart for Data Transmission/Reception (Clock Synchronous Communication Mode).

When cancelling transmit/receive mode after this mode is used (TE_NAKIE = RE_STIE = 1), a clock may be output if transmit/receive mode is cancelled after reading the SIRDR register. To avoid any clock outputs, use either of the following procedures:

- Set the RE_STIE bit to 0 and then set the TE_NAKIE bit to 0.
- Set bits TE_NAKIE and RE_STIE to 0 at the same time.

When switching to receive mode (TE_NAKIE = 0 and RE_STIE = 1) after that, write 1 to the SIRST bit and then set this bit to 0 to initialize the SSU control block and the SISDR register before setting the RE_STIE bit to 1.

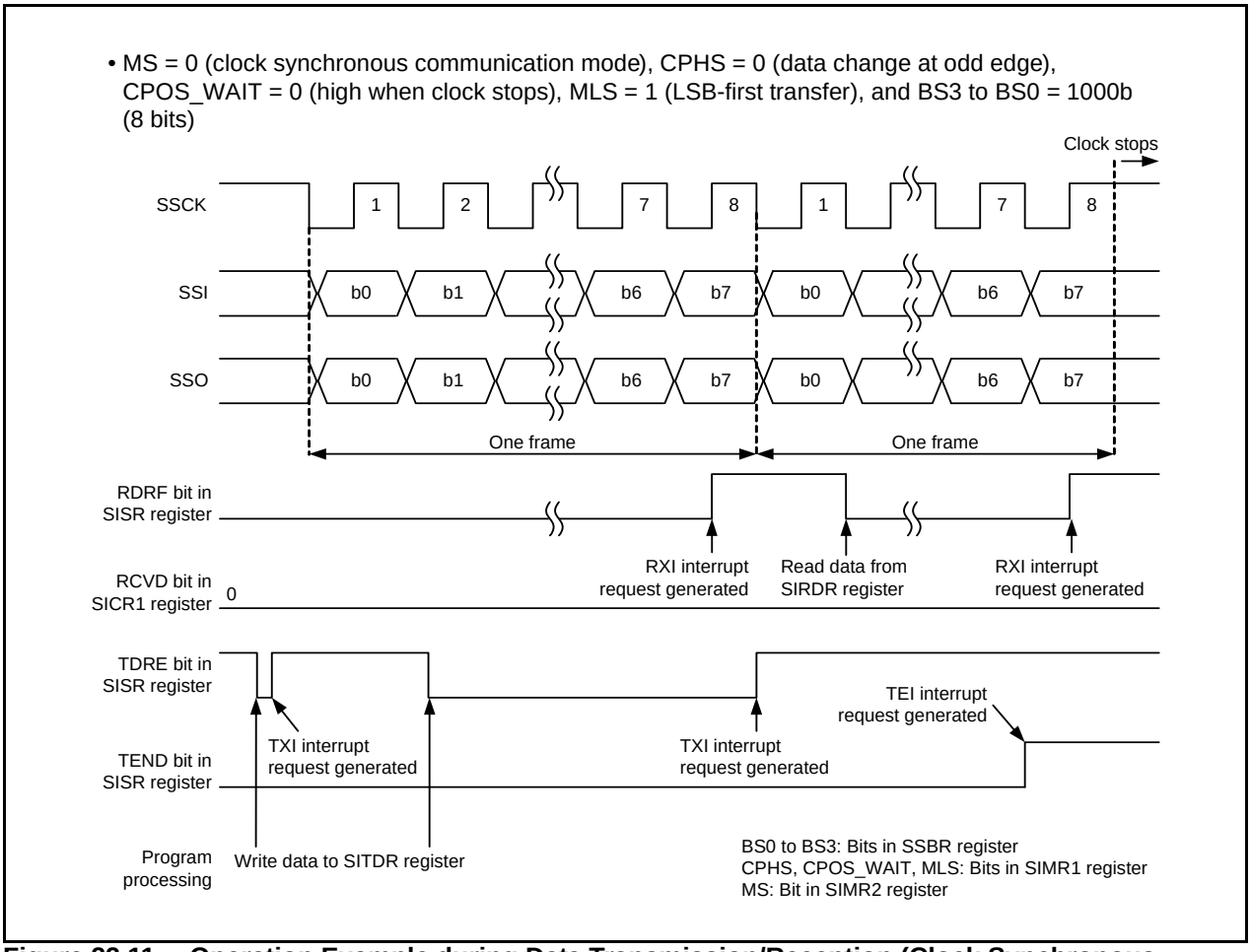
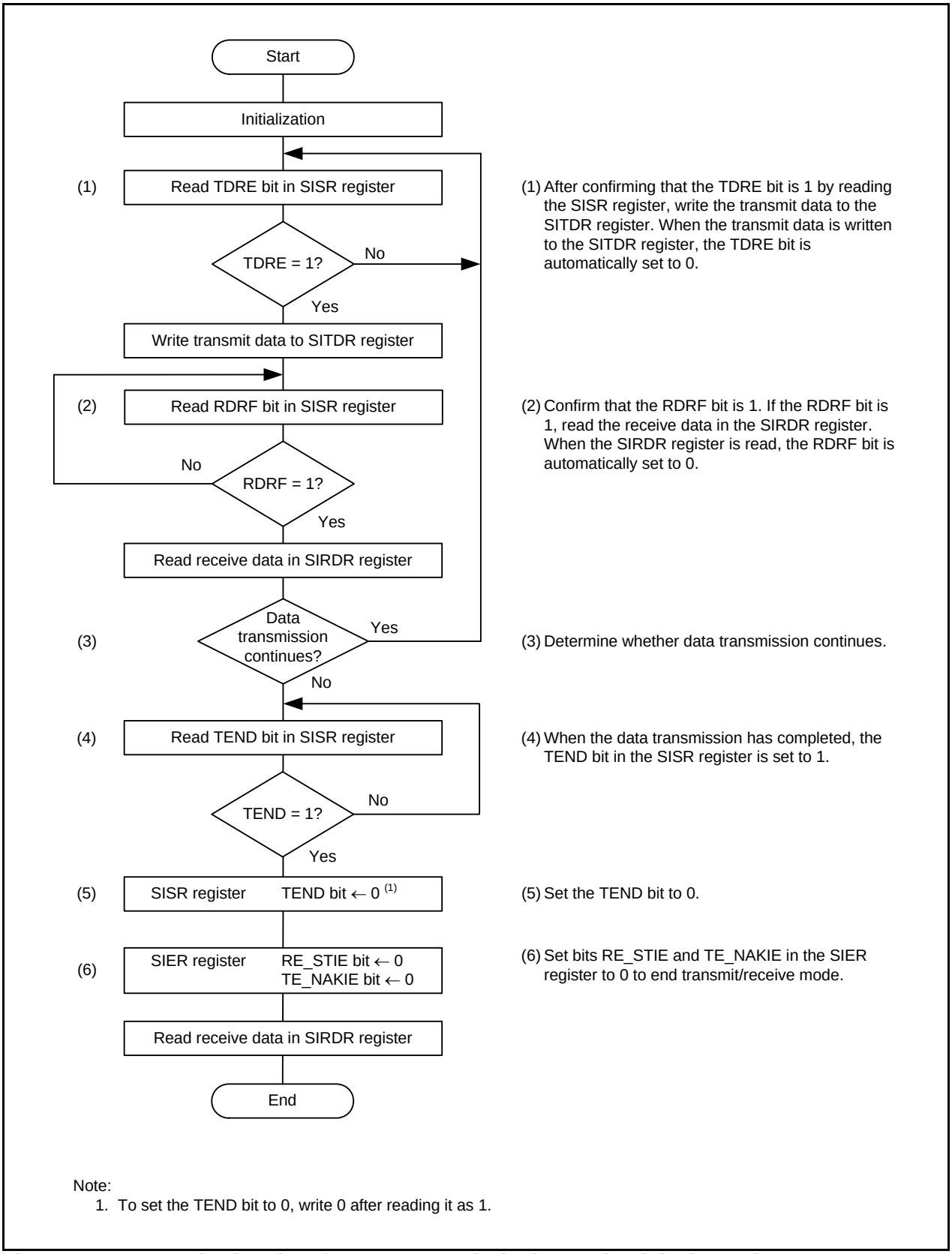


Figure 22.11 Operation Example during Data Transmission/Reception (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length)



Note:
1. To set the TEND bit to 0, write 0 after reading it as 1.

Figure 22.12 Sample Flowchart for Data Transmission/Reception (Clock Synchronous Communication Mode)

22.3.3 4-Wire Bus Communication Mode

In 4-wire bus communication mode, a 4-wire bus consisting of a clock line, a data input line, a data output line, and a chip select line is used for communication. This mode includes a bidirectional mode in which the data input line and data output line use a single pin.

The data input line and output line change according to the settings of the MST bit in the SICR1 register and the BIDE bit in the SIMR2 register. For details, refer to **22.3.1.3 Association between Data I/O Pins and SS Shift Register**. In this mode, the association between clock polarity, phase, and data are set using bits CPOS_WAIT and CPHS in the SIMR1 register. For details, refer to **22.3.1.2 Association between Transfer Clock Polarity, Phase, and Data**.

The chip select line controls output for the master device, and it controls input for the slave device. For the master device, the chip select line controls output of the $\overline{\text{SCS}}$ pin or controls output of an I/O port when the CSS1 bit in the SIMR2 register is set to 1. For the slave device, the chip select line sets the $\overline{\text{SCS}}$ pin to function as an input pin when bits CSS1 and CSS0 in the SIMR2 register are set to 01b.

In 4-wire bus communication mode, the MLS bit in the SIMR1 register is set to 0 and communication is performed MSB first.

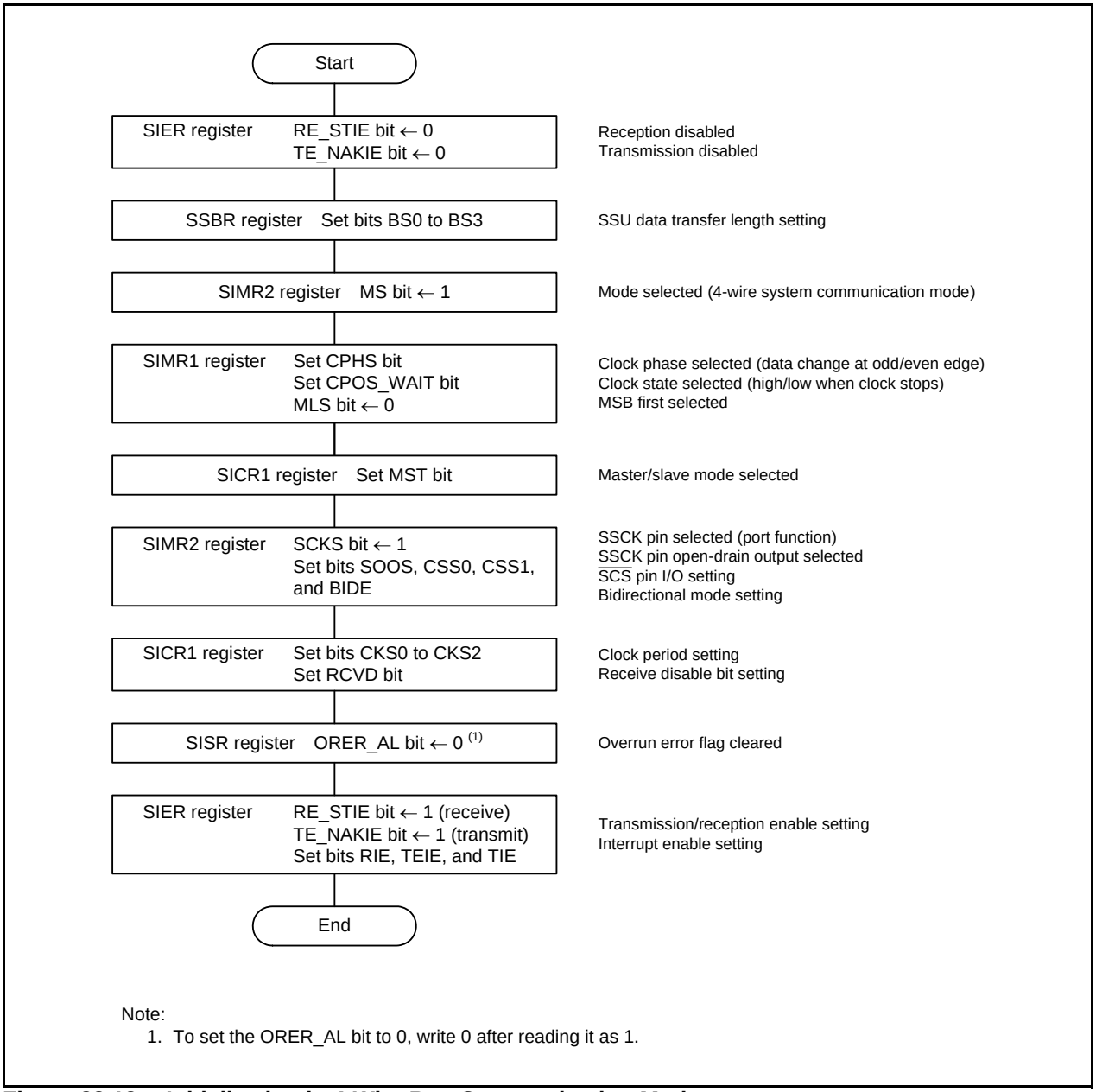
22.3.3.1 Initialization in 4-Wire Bus Communication Mode

Figure 22.13 shows the Initialization in 4-Wire Bus Communication Mode. Before data transmission/reception, set the TE_NAKIE bit in the SIER register to 0 (transmission disabled) and the RE_STIE bit to 0 (reception disabled) for initialization.

To change the communication mode or the communication format, set the TE_NAKIE bit to 0 and the RE_STIE bit to 0 before making the change.

Even if the RE_STIE bit is set to 0, the contents of bits RDRF and ORER_AL and the SIRDR register are retained.

After slave receive operation, $\overline{SCS}$ may be asserted when the mode is switched to master mode even though no transfer start condition is written.



Note:
1. To set the ORER_AL bit to 0, write 0 after reading it as 1.

Figure 22.13 Initialization in 4-Wire Bus Communication Mode

22.3.3.2 Data Transmission

Figure 22.14 shows an Operation Example during Data Transmission (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length). During data transmission, the synchronous serial communication unit operates as described below. (The data transfer length can be set from 8 to 16 bits using the SSBR register.)

When the MCU is set as the master device, it outputs a synchronous clock and data. When the MCU is set as a slave device, it outputs data synchronized with the input clock while the $\overline{SCS}$ pin input is held low.

When the transmit data is written to the SITDR register after setting the TE_NAKIE bit in the SISR register to 1 (transmission enabled), the TDRE bit in the SISR register is automatically set to 0 (data is not transferred from registers SITDR to SISDR) and the data is transferred from registers SITDR to SISDR. After that, the TDRE bit is set to 1 (data is transferred from registers SITDR to SISDR) and transmission is started. If the TIE bit in the SIER register is 1 at this time, a TXI interrupt request is generated.

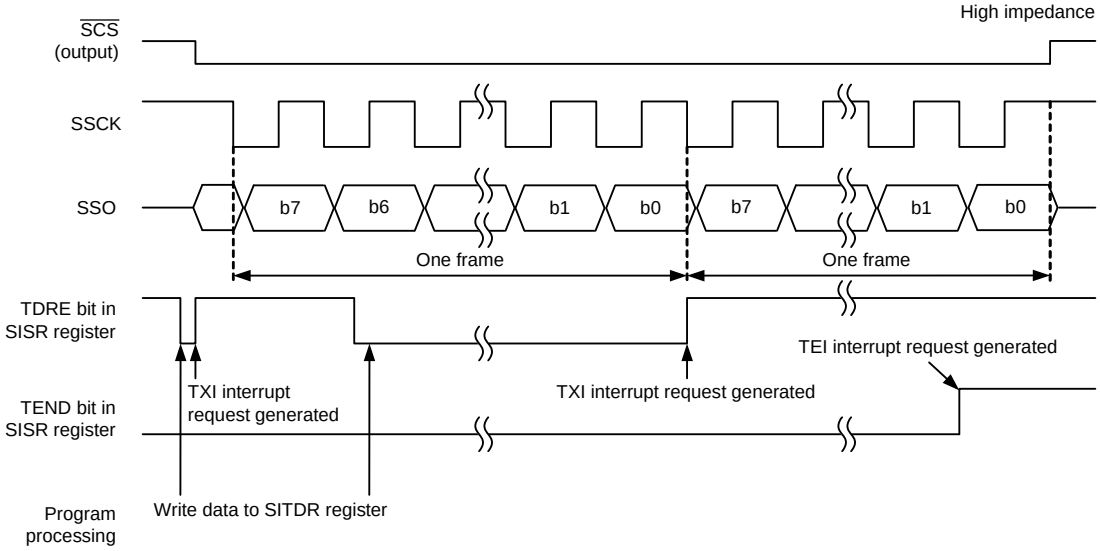
After one frame of data is transferred while the TDRE bit is 0, the data is transferred from registers SITDR to SISDR and the next frame transmission is started. If the 8th bit is transmitted while the TDRE bit is 1, the TEND bit in the SISR register is set to 1 (the TDRE bit is 1 when the last bit of transmit data is transmitted) and the state is retained. If the TEIE bit in the SIER register is 1 (transmit end interrupt request enabled) at this time, a TEI interrupt request is generated. After transmission is completed, the SSCK pin is held high and the $\overline{SCS}$ pin is set to high. To perform transmission continuously while the $\overline{SCS}$ pin is held low, write the next transmit data to the SITDR register before transmitting the 8th bit.

Transmission cannot be performed while the ORER_AL bit in the SISR register is 1 (overrun error). Confirm that the ORER_AL bit is 0 before transmission.

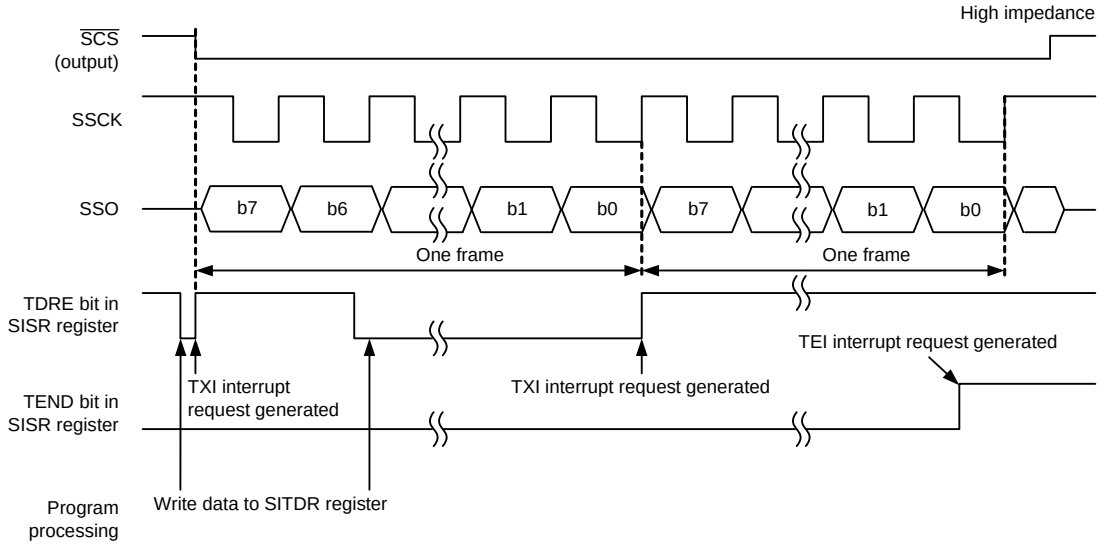
In contrast to clock synchronous communication mode, the SSO pin becomes high-impedance while the $\overline{SCS}$ pin is in a high-impedance state in master device operation, and the SSI pin becomes high-impedance while the $\overline{SCS}$ pin input is held high in slave device operation.

The sample flowchart is the same as that for clock synchronous communication mode (refer to **Figure 22.8 Sample Flowchart for Data Transmission (Clock Synchronous Communication Mode)**).

• CPHS = 0 (data change at odd edge), CPOS_WAIT = 0 (high when clock stops),
MLS = 0 (MSB-first transfer), and BS3 to BS0 = 1000b (8 bits)



• CPHS = 1 (data change at even edge), CPOS_WAIT = 0 (high when clock stops),
MLS = 0 (MSB-first transfer), and BS3 to BS0 = 1000b (8 bits)



BS0 to BS3: Bits in SSBR register
CPHS, CPOS_WAIT, MLS: Bits in SIMR1 register

Figure 22.14 Operation Example during Data Transmission (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length)

22.3.3.3 Data Reception

Figure 22.15 shows an Operation Example during Data Reception (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length). During data reception, the synchronous serial communication unit operates as described below. (The data transfer length can be set from 8 to 16 bits using the SSBR register.)

When the MCU is set as the master device, it outputs a synchronous clock and inputs data. When the MCU is set as a slave device, it outputs data synchronized with the input clock while the $\overline{SCS}$ pin input is held low.

When the MCU is set as the master device, it outputs a receive clock and reception is started by performing a dummy read of the SIRDR register.

After 8 bits of data are received, the RDRF bit in the SISR register is set to 1 (data present in the SIRDR register) and receive data is stored in the SIRDR register. If the RIE bit in the SIER register is 1 (RXI and OEI interrupt requests enabled) at this time, an RXI interrupt request is generated. When the SIRDR register is read, the RDRF bit is automatically set to 0 (no data in the SIRDR register).

When the MCU is set as the master device and reception completes, set the RCVD bit in the SICR1 register to 1 (receive operation is completed after 1 byte of data is received) before reading the [last frame - 1] of the receive data. With this setting, the synchronous serial communication unit outputs a receive clock for the [last frame] and then stops. After that, set the RE_STIE bit in the SIER register to 0 (reception disabled) and the RCVD bit to 0 (receive operation continues after 1-byte data is received), and then read the receive data. When the SIRDR register is read while the RE_STIE bit in the SIER register is set to 1 (reception enabled), the receive clock is output again.

When the 8th clock rises while the RDRF bit is 1, the ORER_AL bit in the SISR register is set to 1 (overrun error: OEI) and the operation is stopped. When the ORER_AL bit is 1, reception cannot be performed. Confirm that the ORER_AL bit is 0 before restarting reception.

The timing at which bits RDRF and ORER_AL are set to 1 varies depending on the setting of the CPHS bit in the SIMR1 register. Figure 22.15 shows this timing. If the CPHS bit is set to 1 (data download at odd edge), care must be taken when reception is completed because these bits are set to 1 at some point during the frame.

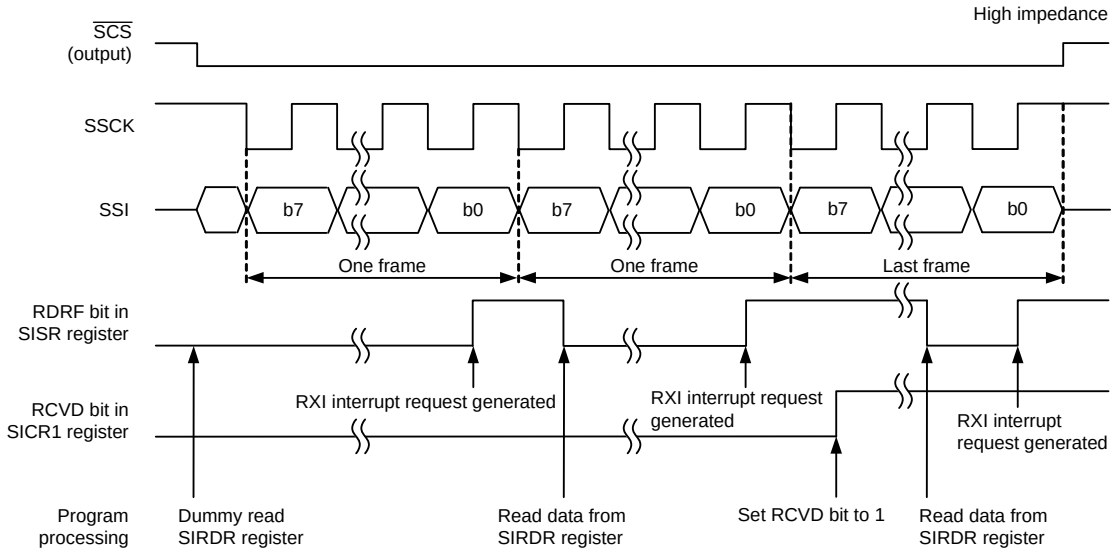
The sample flowchart is the same as that for clock synchronous communication mode (refer to **Figure 22.10 Sample Flowchart for Data Reception (MST = 1) (Clock Synchronous Communication Mode)**).

Notes when Overrun Error Occurs

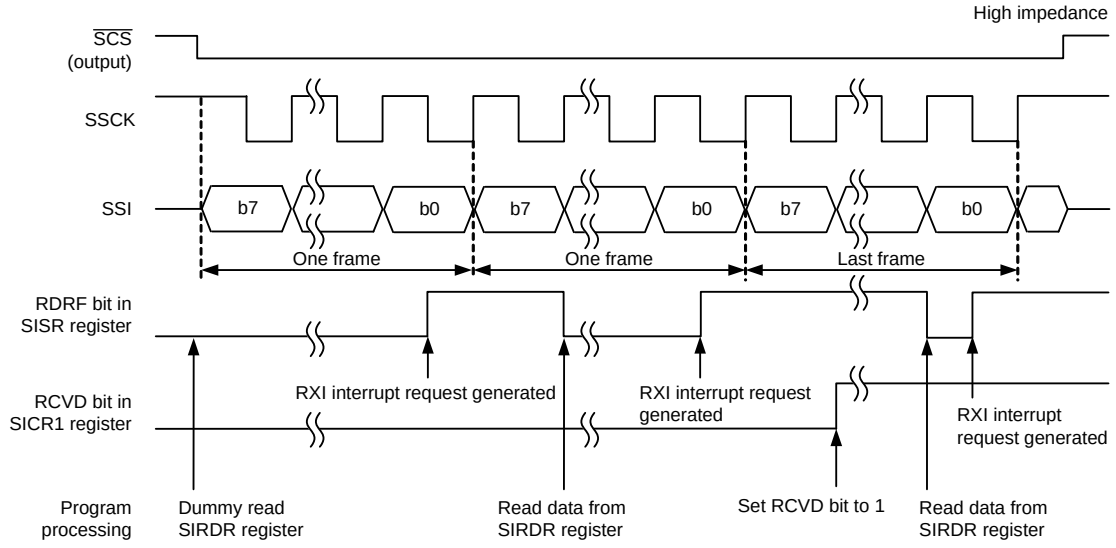
After an overrun error occurs, use the following procedure to cancel the overrun error state:

(1) Transfer operation is completed (confirm that module selection is negated → A conflict error occurs in slave mode).
(2) Read the last received data (data before an overrun error occurs).
(3) Clear the overrun error flag (a conflict error also occurs in slave mode).

• CPHS = 0 (data download at even edge), CPOS_WAIT = 0 (high when clock stops), MLS = 0 (MSB-first transfer), and BS3 to BS0 = 1000b (8 bits)



• CPHS = 1 (data download at even edge), CPOS_WAIT = 0 (high when clock stops), MLS = 0 (MSB-first transfer), and BS3 to BS0 = 1000b (8 bits)



BS0 to BS3: Bits in SSBR register
CPHS, CPOS_WAIT, MLS: Bits in SIMR1 register

Figure 22.15 Operation Example during Data Reception (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length)

22.3.3.4 $\overline{\text{SCS}}$ Pin Control and Arbitration

When the MS bit in the SIMR2 register is set to 1 (4-wire bus communication mode) and the CSS1 bit is set to 1 (functions as the $\overline{\text{SCS}}$ output pin), set the MST bit in the SICR1 register to 1 (master mode) and check the arbitration of the $\overline{\text{SCS}}$ pin before starting serial transfer. If the synchronous serial communication unit detects that the synchronized internal $\overline{\text{SCS}}$ signal is held low in this period, the CE_ADZ bit in the SISR register is set to 1 (conflict error) and the MST bit is automatically set to 0 (slave mode).
Figure 22.16 shows the Arbitration Check Timing.

Future transmit operations are not performed while the CE_ADZ bit in the SISR register is 1. Set the CE_ADZ bit to 0 (no conflict error) before starting transmission.

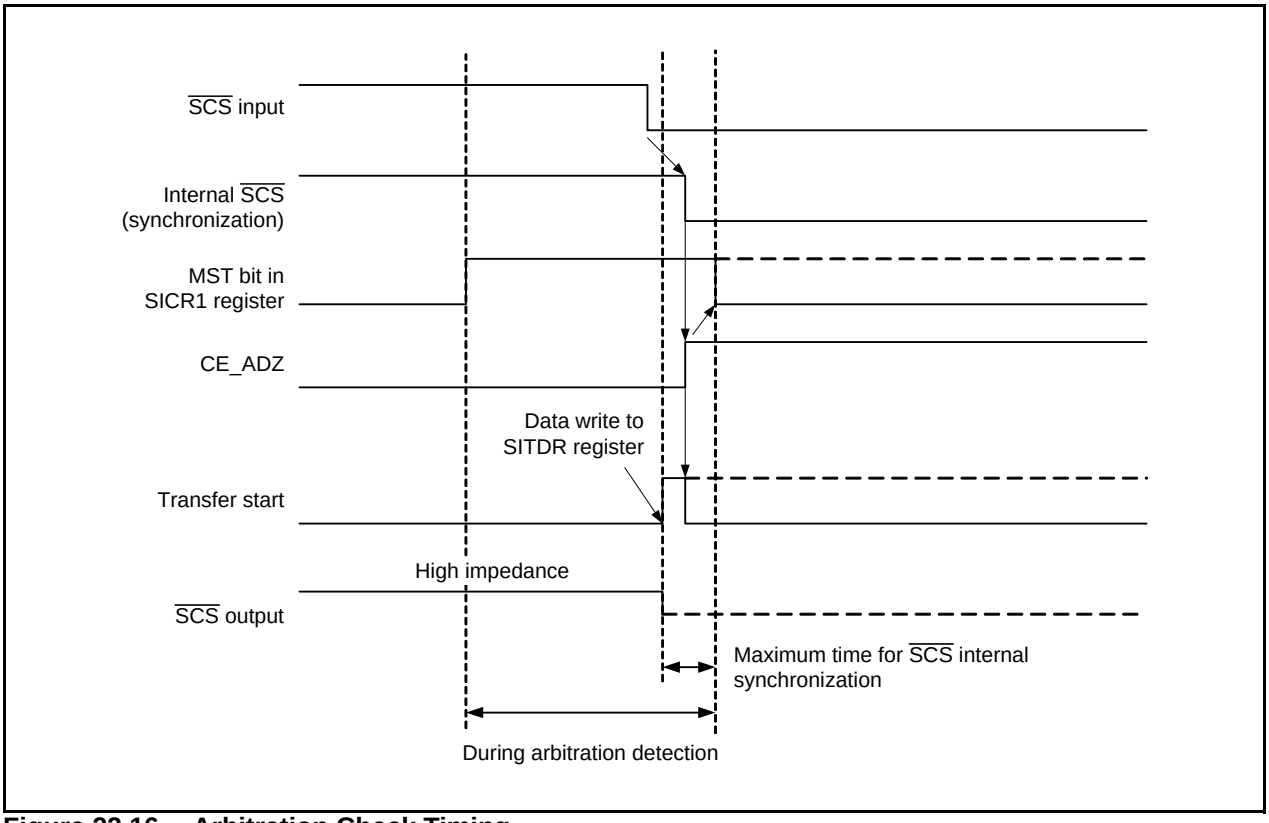


Figure 22.16 Arbitration Check Timing

22.4 I²C bus Interface Operation

22.4.1 Items Common to I²C bus Interface and Clock Synchronous Serial Mode

22.4.1.1 Transfer Clock

When the MST bit in the SICR1 register is 0, the transfer clock is the external clock input from the SCL pin. When the MST bit is 1, the transfer clock is the internal clock selected by bits CKS0 to CKS3 in the SICR1 register and bits IICTCTWI and IICTCHALF in the IICCR register, and the transfer clock is output from the SCL pin. Tables 22.9 and 22.10 list the Transfer Rate Examples.

Table 22.9 Transfer Rate Examples (1)

IICCR Register		SICR1 Register				Transfer Clock	Transfer Rate				
IICTCHALF	IICTCTWI	CKS3	CKS2	CKS1	CKS0		f1 = 5 MHz	f1 = 8 MHz	f1 = 10 MHz	f1 = 16 MHz	f1 = 20 MHz
0	0	0	0	0	0	f1/28	179 kHz	286 kHz	357 kHz	571 kHz	714 kHz
					1	f1/40	125 kHz	200 kHz	250 kHz	400 kHz	500 kHz
				1	0	f1/48	104 kHz	167 kHz	208 kHz	333 kHz	417 kHz
					1	f1/64	78.1 kHz	125 kHz	156 kHz	250 kHz	313 kHz
			1	0	0	f1/80	62.5 kHz	100 kHz	125 kHz	200 kHz	250 kHz
					1	f1/100	50.0 kHz	80.0 kHz	100 kHz	160 kHz	200 kHz
				1	0	f1/112	44.6 kHz	71.4 kHz	89.3 kHz	143 kHz	179 kHz
					1	f1/128	39.1 kHz	62.5 kHz	78.1 kHz	125 kHz	156 kHz
		1	0	0	0	f1/56	89.3 kHz	143 kHz	179 kHz	286 kHz	357 kHz
					1	f1/80	62.5 kHz	100 kHz	125 kHz	200 kHz	250 kHz
				1	0	f1/96	52.1 kHz	83.3 kHz	104 kHz	167 kHz	208 kHz
					1	f1/128	39.1 kHz	62.5 kHz	78.1 kHz	125 kHz	156 kHz
			1	0	0	f1/160	31.3 kHz	50.0 kHz	62.5 kHz	100 kHz	125 kHz
					1	f1/200	25.0 kHz	40.0 kHz	50.0 kHz	80.0 kHz	100 kHz
				1	0	f1/224	22.3 kHz	35.7 kHz	44.6 kHz	71.4 kHz	89.3 kHz
					1	f1/256	19.5 kHz	31.3 kHz	39.1 kHz	62.5 kHz	78.1 kHz

Table 22.10 Transfer Rate Examples (2)

IICCR Register		SICR1 Register				Transfer Clock	Transfer Rate				
IICTCHALF	IICTCTWI	CKS3	CKS2	CKS1	CKS0		f1 = 5 MHz	f1 = 8 MHz	f1 = 10 MHz	f1 = 16 MHz	f1 = 20 MHz
0	1	0	0	0	0	f1/28	358 kHz	572 kHz	714 kHz	1142 kHz	1428 kHz
					1	f1/40	250 kHz	400 kHz	500 kHz	800 kHz	1000 kHz
				1	0	f1/48	208 kHz	334 kHz	416 kHz	666 kHz	834 kHz
					1	f1/64	156 kHz	250 kHz	312 kHz	500 kHz	626 kHz
			1	0	0	f1/80	125 kHz	200 kHz	250 kHz	400 kHz	500 kHz
					1	f1/100	100 kHz	160 kHz	200 kHz	320 kHz	400 kHz
				1	0	f1/112	89 kHz	143 kHz	179 kHz	286 kHz	358 kHz
					1	f1/128	78 kHz	125 kHz	156 kHz	250 kHz	312 kHz
		1	0	0	0	f1/56	179 kHz	286 kHz	358 kHz	572 kHz	714 kHz
					1	f1/80	125 kHz	200 kHz	250 kHz	400 kHz	500 kHz
				1	0	f1/96	104 kHz	167 kHz	208 kHz	334 kHz	416 kHz
					1	f1/128	78 kHz	125 kHz	156 kHz	250 kHz	312 kHz
			1	0	0	f1/160	63 kHz	100 kHz	125 kHz	200 kHz	250 kHz
					1	f1/200	50 kHz	80 kHz	100 kHz	160 kHz	200 kHz
				1	0	f1/224	45 kHz	71 kHz	89 kHz	143 kHz	179 kHz
					1	f1/256	39 kHz	63 kHz	78 kHz	125 kHz	156 kHz
1	0	0	0	0	0	f1/28	90 kHz	143 kHz	179 kHz	286 kHz	357 kHz
					1	f1/40	63 kHz	100 kHz	125 kHz	200 kHz	250 kHz
				1	0	f1/48	52 kHz	84 kHz	104 kHz	167 kHz	209 kHz
					1	f1/64	39 kHz	63 kHz	78 kHz	125 kHz	157 kHz
			1	0	0	f1/80	31 kHz	50 kHz	63 kHz	100 kHz	125 kHz
					1	f1/100	25 kHz	40 kHz	50 kHz	80 kHz	100 kHz
				1	0	f1/112	22 kHz	36 kHz	45 kHz	72 kHz	90 kHz
					1	f1/128	20 kHz	31 kHz	39 kHz	63 kHz	78 kHz
		1	0	0	0	f1/56	45 kHz	72 kHz	90 kHz	143 kHz	179 kHz
					1	f1/80	31 kHz	50 kHz	63 kHz	100 kHz	125 kHz
				1	0	f1/96	26 kHz	42 kHz	52 kHz	84 kHz	104 kHz
					1	f1/128	20 kHz	31 kHz	39 kHz	63 kHz	78 kHz
			1	0	0	f1/160	16 kHz	25 kHz	31 kHz	50 kHz	63 kHz
					1	f1/200	13 kHz	20 kHz	25 kHz	40 kHz	50 kHz
				1	0	f1/224	11 kHz	18 kHz	22 kHz	36 kHz	45 kHz
					1	f1/256	10 kHz	16 kHz	20 kHz	31 kHz	39 kHz

22.4.1.2 SDA Pin Digital Delay Selection

The digital delay value of the SDA pin can be selected by bits SDADLY0 and SDADLY1 in the IICCR register. Figure 22.17 shows an Operation Example of Digital Delay for SDA Pin.

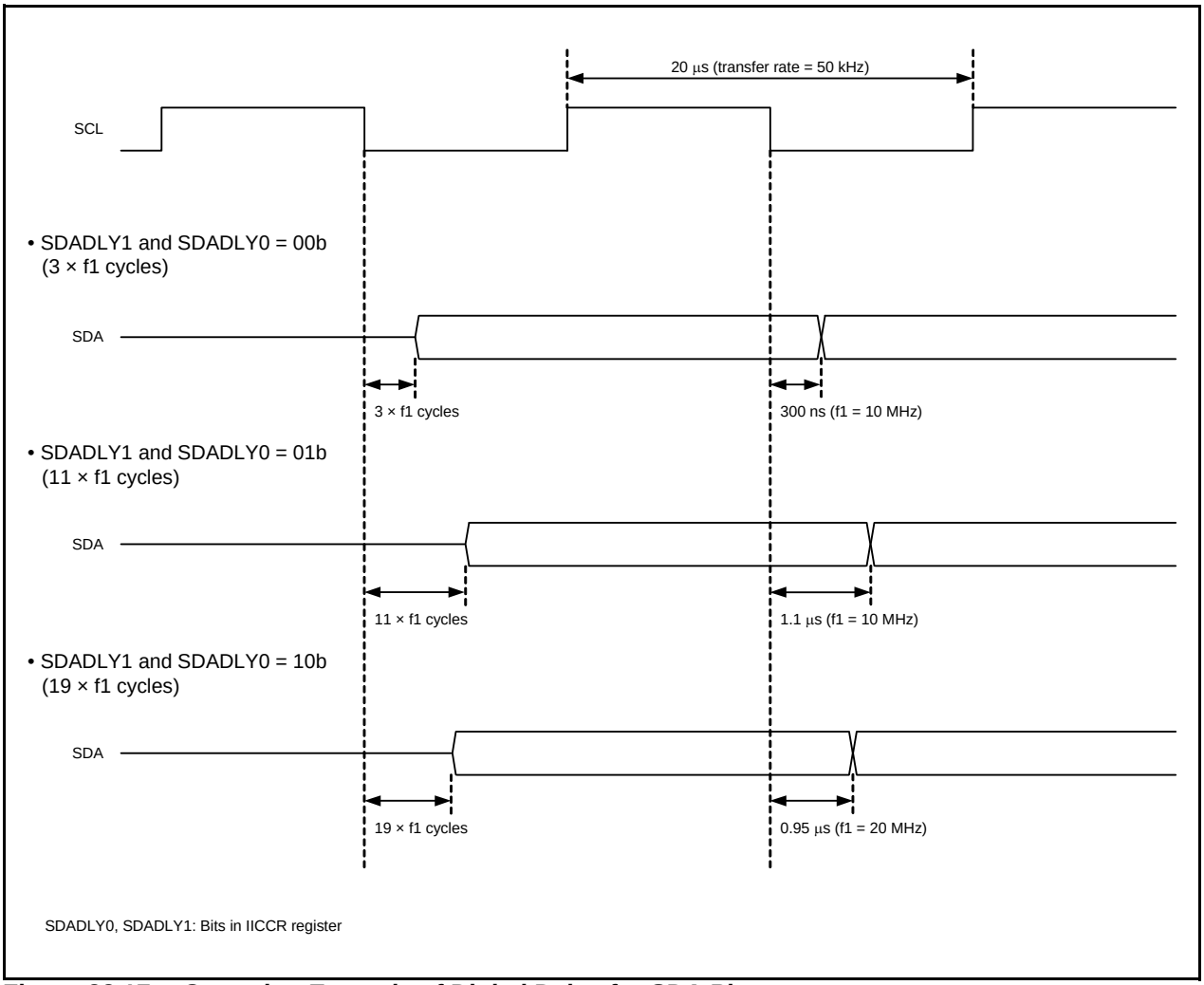


Figure 22.17 Operation Example of Digital Delay for SDA Pin

22.4.1.3 Interrupt Requests

The I²C bus interface has six interrupt requests in I²C bus interface mode and four interrupt requests in clock synchronous serial mode. Table 22.11 lists the Interrupt Requests of I²C bus Interface.

Because these interrupt requests are assigned to the I²C bus interface interrupt vector table, interrupt sources must be determined using the bits.

Table 22.11 Interrupt Requests of I²C bus Interface

Interrupt Request		Generation Condition	Format	
			I²C bus	Clock synchronous serial
Transmit data empty	TXI	TIE = 1 and TDRE = 1	Enabled	Enabled
Transmit end	TEI	TEIE = 1 and TEND = 1	Enabled	Enabled
Receive data full	RXI	RIE = 1 and RDRF = 1	Enabled	Enabled
Stop condition detection	STPI	RE_STIE = 1 and STOP = 1	Enabled	Disabled
NACK detection	NAKI	TE_NAKIE = 1 and ORER_AL = 1 (or TE_NAKIE = 1 and NACKF = 1)	Enabled	Disabled
Arbitration lost			Enabled	Disabled
Overrun error			Disabled	Enabled

RE_STIE, TE_NAKIE, RIE, TEIE, TIE: Bits in SIER register
ORER_AL, STOP, NACKF, RDRF, TEND, TDRE: Bits in SISR register

When the generation conditions listed in Table 22.11 are met, an I²C bus interface interrupt request is generated. Set the interrupt generation conditions to 0 in the I²C bus interface interrupt routine.

Note that bits TDRE and TEND in the SIER register are automatically set to 0 by writing transmit data to the SITDR register and the RDRF bit is automatically set to 0 by reading the SIRDR register. In particular, the TDRE bit is set to 0 when transmit data is written to the SITDR register and set to 1 when data is transferred from registers SITDR to SISDR. If the TDRE bit is further set to 0, an additional 1 byte may be transmitted. Because the data is retained in the transmit buffer, the data is shifted to the shift register by a trigger (the TDRE bit in the SISR register is 0), and thus the same data is retransmitted.

Also, set the RE_STIE bit in the SIER register to 1 (stop condition detection interrupt request enabled) only when the STOP bit in the SISR register is 0.

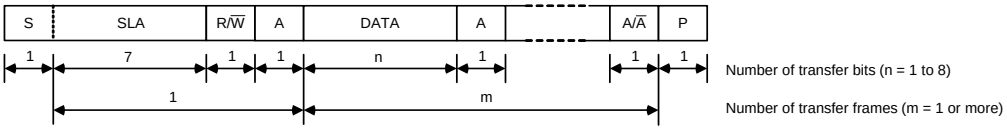
22.4.2 I²C bus Interface Mode

22.4.2.1 I²C bus Format

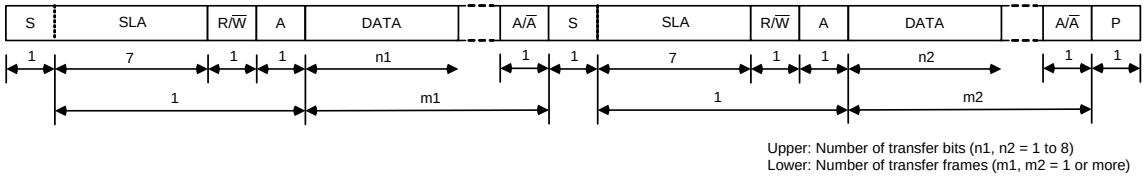
When the MS bit in the SIMR2 register is set to 0, I²C bus interface mode is used for communication. Figure 22.18 shows the I²C bus Format and Bus Timing. The first frame following the start condition consists of 8 bits.

(1) I²C bus format

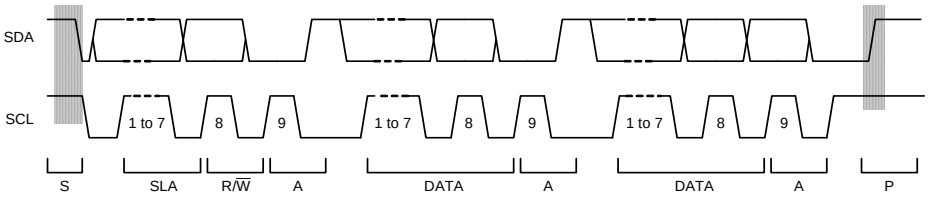
(a) I²C bus format (MS = 0)



(b) I²C bus format (When start condition is retransmitted, MS = 0)



(2) I²C bus timing



Legend:
S : Start condition
The master device changes the SDA signal from high to low while the SCL signal is held high.
SLA : Slave address
R/W : Indicates the direction of data transmission/reception. Data is transmitted when:
R/W value is 1: From the slave device to the master device
R/W value is 0: From the master device to the slave device
A : Acknowledge
The receive device sets the SDA signal to low.
DATA : Transmit/receive data
P : Stop condition
The master device changes the SDA signal from low to high while the SCL signal is held high.

Figure 22.18 I²C bus Format and Bus Timing

22.4.2.2 I²C bus Slave Addressing

In the I²C bus format, the first 1 byte immediately after a start condition is specified as a slave address. When this module operates as a slave device, slave addresses can be programmed using bits SVA0 to SVA6 in the SIMR2 register. However, this does not apply to the “general call address” and the “start byte” defined in the I²C bus specification.

- General call address (0000_000_0)
  Since all the devices are addressed, an acknowledge signal is returned.
- Start byte (0000_000_1)
  All the devices cannot return any acknowledge signal.

22.4.2.3 Master Transmit Operation

In master transmit mode, the master device outputs the transmit clock and data, and the slave device returns an acknowledge signal. Figures 22.19 and 22.20 show the Operation Timing in Master Transmit Mode (I^2C bus Interface Mode).

The transmit procedure and operation in master transmit mode are shown below:

(1) Set the STOP bit in the SISR register to 0 for initialization. Set the ICE bit in the SICR1 register to 1 (transfer operation enabled). Then, set bits CPOS_WAIT and MLS in the SIMR1 register and bits CKS0 to CKS3 in the SICR1 register (initial setting).

(2) After confirming that the bus is released by reading the BBSY bit in the SICR2 register, set bits TRS and MST in the SICR1 register to master transmit mode. Then, write 1 to the BBSY bit and 0 to the SCP bit with the MOV instruction (start condition generated). This will generate a start condition.

(3) After confirming that the TDRE bit in the SISR register is 1, write transmit data to the SITDR register (data in which a slave address and R/W are indicated in the 1st byte). The TDRE bit is automatically set to 0 at this time and data is transferred from registers SITDR to SISDR, and then the TDRE bit is set to 1 again.

(4) When 1 byte of data transmission is completed while the TDRE bit is 1, the TEND bit in the SISR register is set to 1 at the rising edge of the 9th clock cycle of the transmit clock. After confirming that the slave device is selected by reading the ACKBR bit in the SIER register, write the 2nd byte of data to the SITDR register. Write the transmit data after the 2nd byte to the SITDR register every time the TRDE bit is set to 1. Since the slave device is not acknowledged when the ACKBR bit is 1, generate a stop condition or a repeat start condition. A stop condition is generated by writing 0 to the BBSY bit and 0 to the SCP bit with the MOV instruction. A repeat start condition is generated by writing 1 to the BBSY bit and 0 to the SCP bit with the MOV instruction. Clear TEND and NACKF after a repeat start condition has been generated. The SCL signal is held low until data is ready or a stop condition or a repeat start condition is generated.

(5) When the number of bytes to be transmitted is written to the SITDR register, wait until the TEND bit is set to 1 while the TDRE bit is 1. Or wait for NACK (NACKF bit in SISR register = 1) from the receive device while the ACKE bit in the SIER register is 1 (when the receive acknowledge bit is 1, transfer is halted). Then, generate a stop condition and set the TEND bit or the NACKF bit to 0.

(6) When the STOP bit in the SISR register is set to 1, return to slave receive mode.

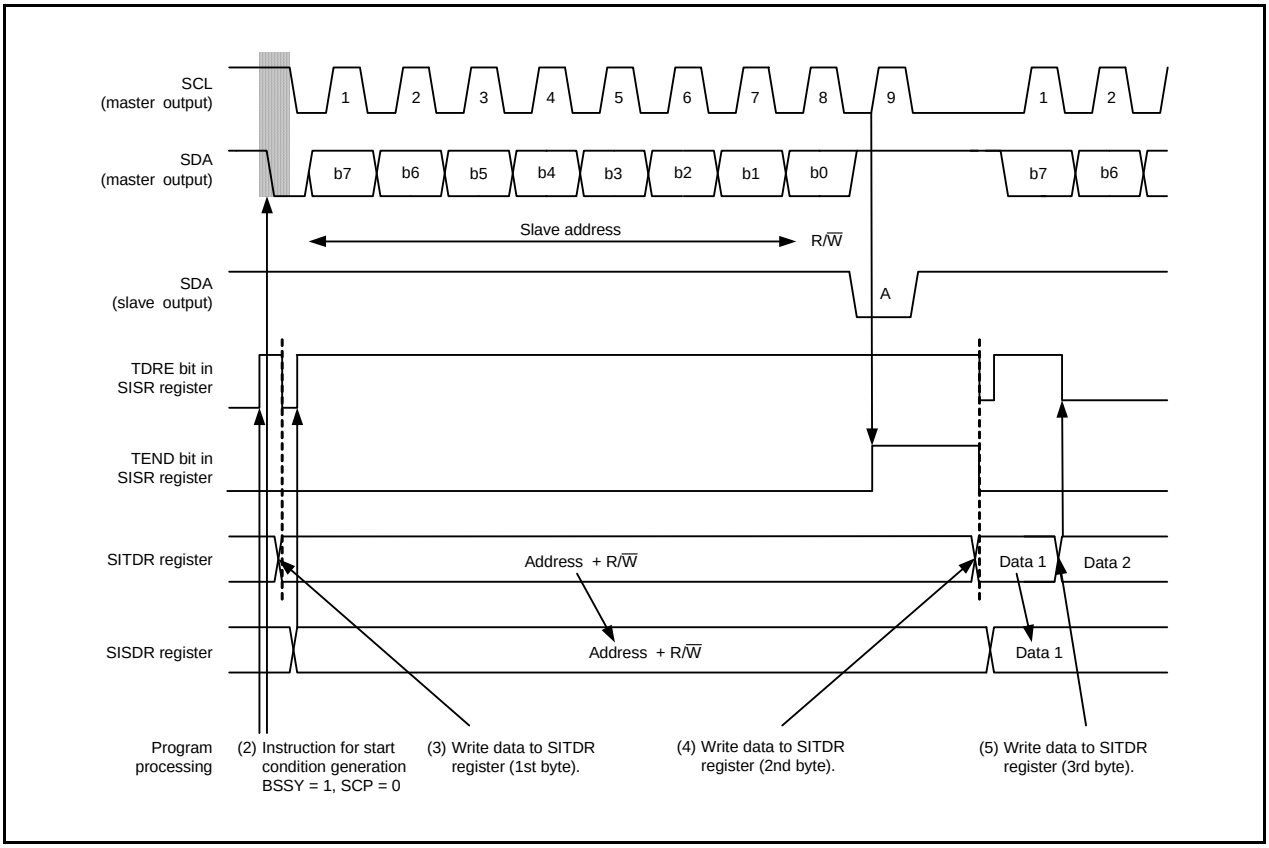


Figure 22.19 Operation Timing in Master Transmit Mode (I²C bus Interface Mode) (1)

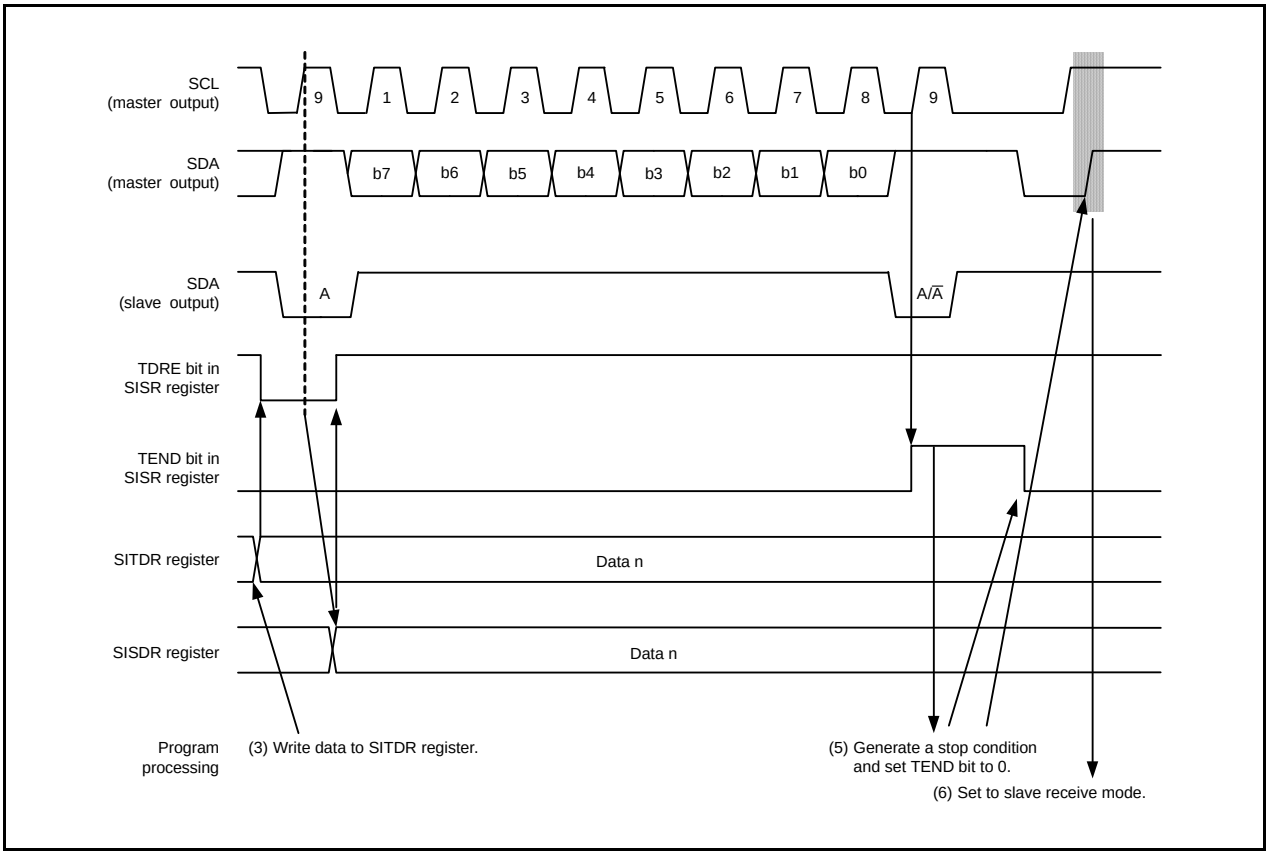


Figure 22.20 Operation Timing in Master Transmit Mode (I²C bus Interface Mode) (2)

22.4.2.3.1 Flow for Generating Repeat Start Condition during I²C Master Transmit Mode

To generate a repeat start condition after receiving NACK, use the following procedure:

(1) Confirm a NACK error.
(2) Generate a repeat start condition (write 1 to the BBSY bit and 1 to the SCP bit in the SICR2 register with the MOV instruction)
(3) Confirm the rising edge of the SCL signal.
(4) Clear bits TEND and NACKF in the SISR register.

22.4.2.3.2 Operation when Start Condition/Stop Condition is Detected during I²C Master Transmit Operation

The following shows the operation and software flow when a start condition/stop condition is detected during I²C master transmit operation.

(1) Detect an arbitration lost and enter slave receive mode.
(2) Clear bits TDRE and ORER_AL in the SISR register.
(3) Confirm the BBSY bit in the SICR2 register.

When 1: Enter slave address reception.
When 0: Either of the host/slave can operate.

22.4.2.4 Master Receive Operation

In master receive mode, the master device outputs the receive clock, receives data from the slave device, and returns an acknowledge signal. Figures 22.21 and 22.22 show the Operation Timing in Master Receive Mode (I²C bus Interface Mode).

The receive procedure and operation in master receive mode are as follows:

(1) After setting the TEND bit in the SISR register to 0, set the TRS bit in the SICR1 register to 0 to switch from master transmit mode to master receive mode. Then, set the TDRE bit in the SISR register to 0.
(2) Reception is started by performing a dummy read of the SIRDR register. The receive clock is output in synchronization with the internal clock and data is received. The master device outputs the level set by the CEIE_ACKBT bit in the SIER register to the SDA pin at the rising edge of the 9th clock cycle of the receive clock.
(3) When one frame of data reception is completed, the RDRF bit in the SISR register is set to 1 at the rising edge of the 9th clock cycle of the receive clock. If the SIRDR register is read at this time, the received data can be read and the RDRF bit is set to 0 at the same time.
(4) Reception can be performed continuously by reading the SIRDR register every time the RDRF bit is set to 1. If reading of the SIRDR register is delayed by another process and the 8th clock cycle falls while the RDRF bit is 1, the SCL signal is held low until the SIRDR register is read. No stop condition or repeat start condition can be generated at this time.
(5) If the next frame is the last receive frame, set the RCVD bit in the SICR1 register to 1 (next receive operation disabled) and the CEIE_ACKBT bit to 1 before reading the SIRDR register. This enables returning NACK to the slave device and a stop condition can be generated after the next reception.
(6) When the RDRF bit is set to 1 at the rising edge of the 9th clock cycle of the receive clock, generate a stop condition.
(7) When the STOP bit in the SISR register is set to 1, read the SIRDR register. Then, set the RCVD bit to 0 (next receive operation continues).
(8) Return to slave receive mode.

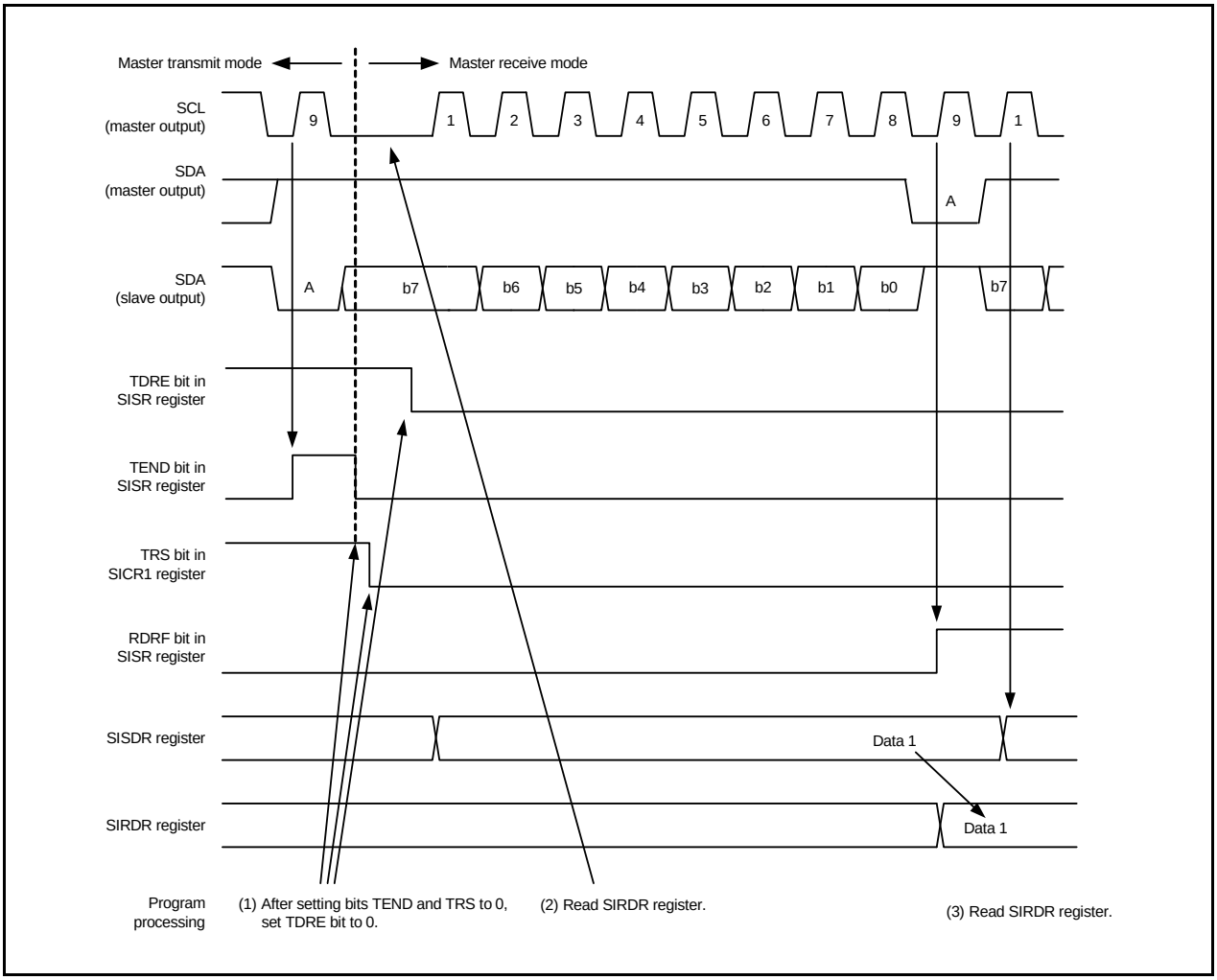


Figure 22.21 Operation Timing in Master Receive Mode (I^2C bus Interface Mode) (1)

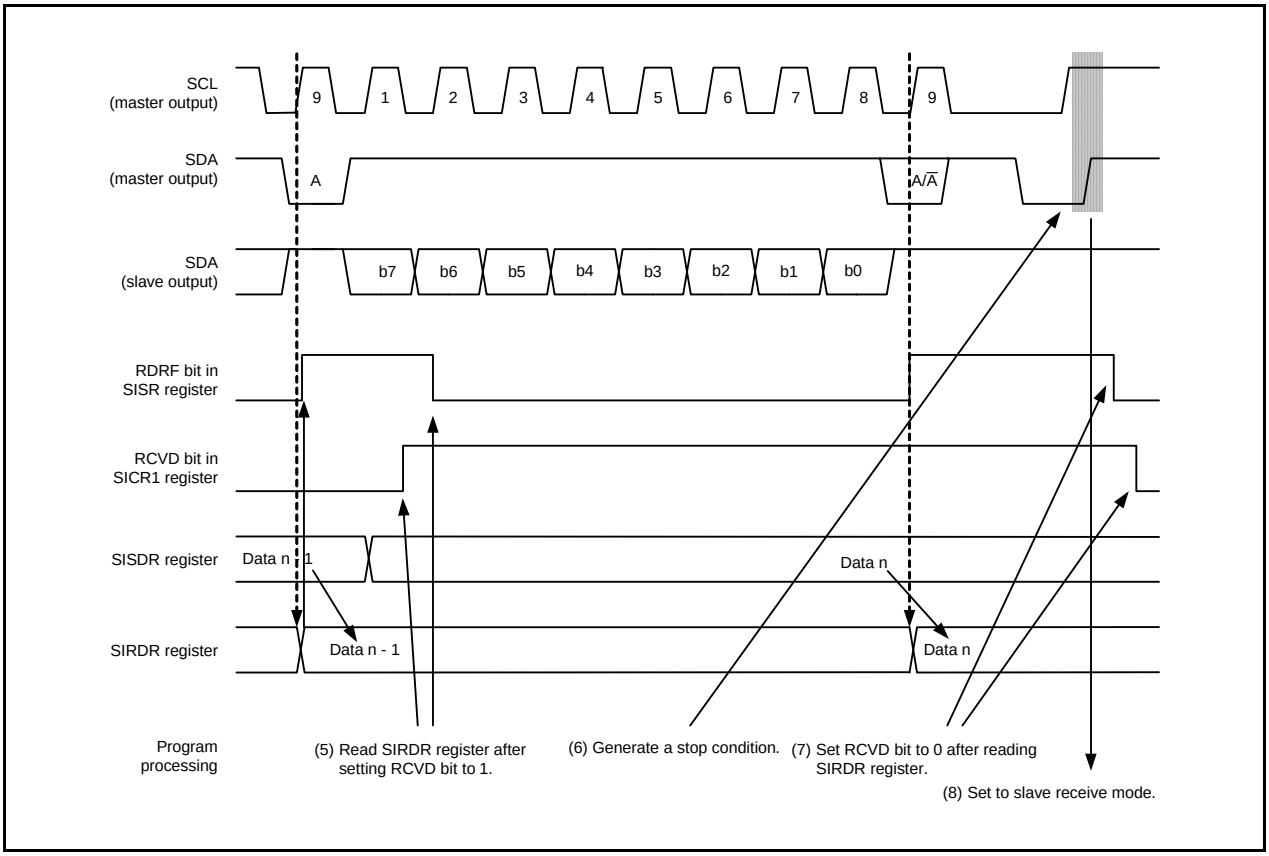


Figure 22.22 Operation Timing in Master Receive Mode (I²C bus Interface Mode) (2)

22.4.2.4.1 Flow for Generating Repeat Start Condition during I²C Master Receive Mode

To generate a repeat start condition after transmitting NACK, use the following procedure:

(1) The same applies as the flow for generating a stop condition until step (5) in 24.4.2.4.
(2) After the RDRF bit in the SISR register is set to 1 at the rising edge of the 9 clock of the receive clock, generate a repeat start condition (write 1 to the BBSY bit and 0 to the SCP bit in the SICR2 register with the MOV instruction).
(3) Read the SIRDR register after setting to master mode (1). Then, set the RCVD bit in the SICR1 register to 0 (next receive operation continues).
(4) Write the data indicating a slave address and R/W to the SITDR register.

Note:

1. After a repeat start condition is generated (by writing 1 to the BBSY bit and 0 to the SCP bit with the MOV instruction), the SCL and SDA signals are held low after 2.5 cycles or later. Be sure to set to master transmit mode before that.

22.4.2.4.2 Operation when Stop Condition is Detected during I²C Master Receive Operation

The following shows the operation and software flow when a stop condition is detected during I²C master receive operation.

(1) Detect a stop condition and enter slave receive mode.
(2) Confirm that the BBSY bit in the SICR2 register is 0.
(3) Clear the STOP bit in the SISR register to 0.
(4) Reset the control block.

22.4.2.5 Slave Transmit Operation

In slave transmit mode, the slave device outputs the transmit data while the master device outputs the receive clock and returns an acknowledge signal. Figures 22.23 and 22.24 show the Operation Timing in Slave Transmit Mode (I^2C bus Interface Mode).

The transmit procedure and operation in slave transmit mode are as follows:

(1) Set the ICE bit in the SICR1 register to 1 (transfer operation enabled). Then, set bits CPOS_WAIT and MLS in the SIMR1 register and bits CKS0 to CKS3 in the SICR1 register (initial setting). Next, set bits TRS and MST in the SICR1 register to 0 and wait until the slave address matches in slave receive mode.

(2) When the slave address matches at the first frame after detecting the start condition, the slave device outputs the level set by the CEIE_ACKBT bit in the SIER register to the SDA pin between the falling edge of the 8th clock cycle and the falling edge of the 9th clock cycle. If the 8th bit of data (R/W) is 1, the TRS bit and the TDRE bit in the SISR register are set to 1, and the mode is switched to slave transmit mode automatically. Continuous transmission is enabled by writing transmit data to the SITDR register every time the TDRE bit is set to 1.

(3) When the TDRE bit is set to 1 after the last transmit data is written to the SITDR register, wait until the TEND bit in the SISR register is set to 1 while the TDRE bit is 1. After the TEND bit is set to 1, set the TEND bit to 0.

(4) Set the TRS bit to 0 and perform a dummy read of the SIRDR register to complete the process. This will release the SCL signal.

(5) Set the TDRE bit to 0.

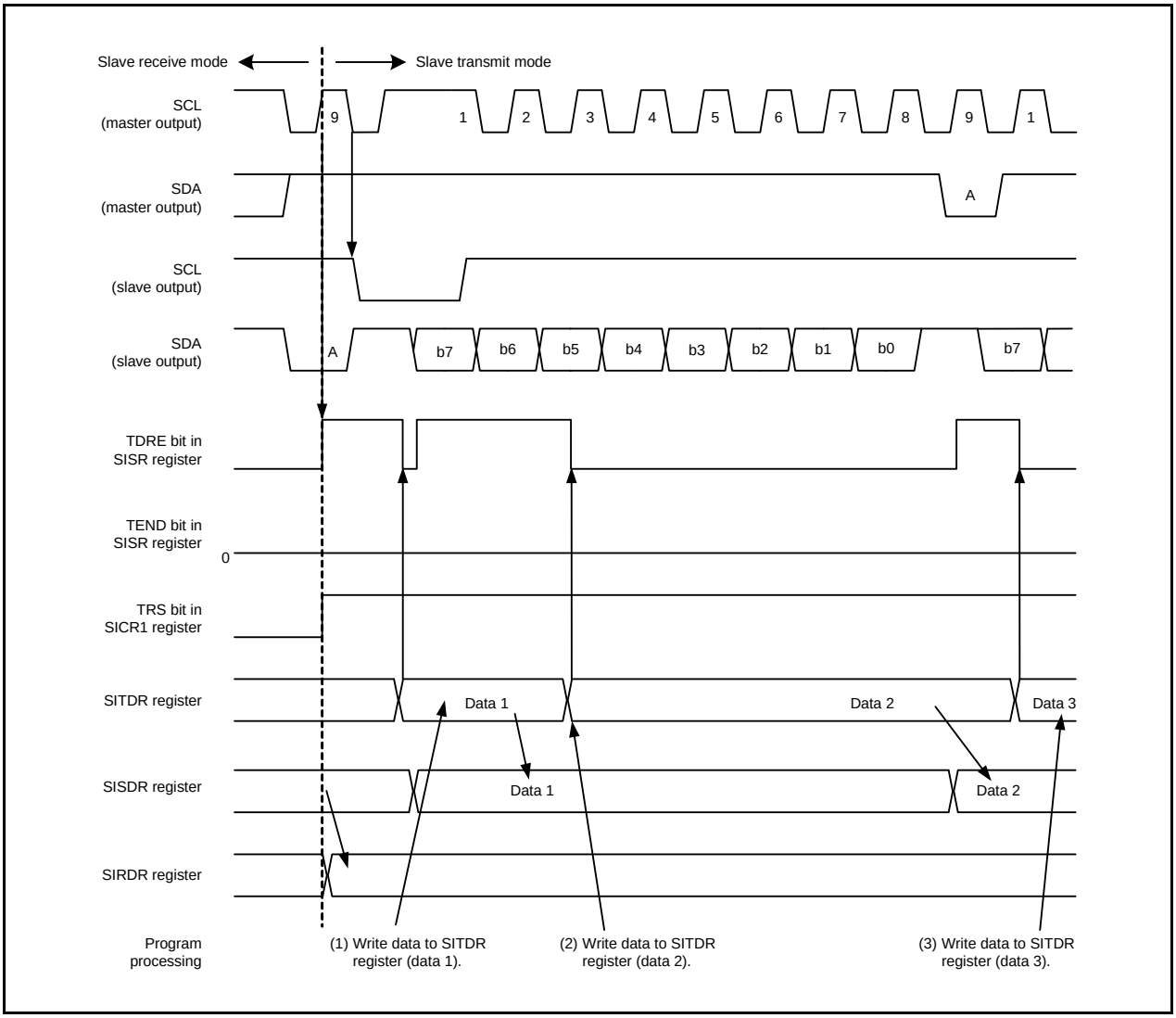


Figure 22.23 Operation Timing in Slave Transmit Mode (I^2C bus Interface Mode) (1)

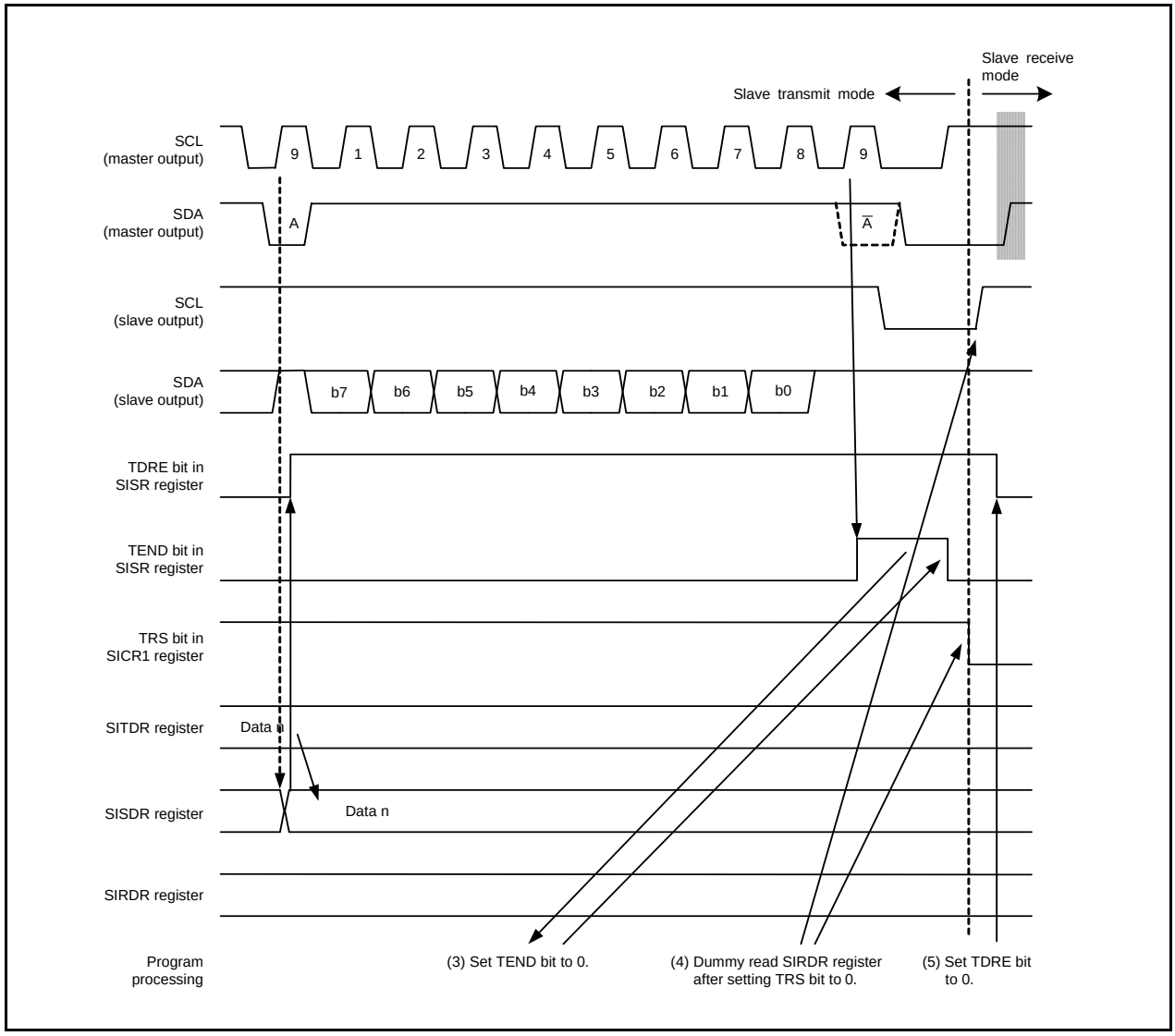


Figure 22.24 Operation Timing in Slave Transmit Mode (I²C bus Interface Mode) (2)

22.4.2.5.1 Maintaining Data Setup Time during I²C Slave Transmit Operation

During data transfer, if the 9th clock cycle falls while the TDRE bit is 1 and the TEND bit is 1, the SCL signal is held low until transmit data is written to the transmit register. After transmit data is written, maintain the data setup time set with the CKS3 bit after the transmit data is output to the SDA pin and release the SCL signal (rising) (refer to **Figure 22.25 Data Setup Time during Slave Transmit Operation**).

The CKS3 bit 0: 9 or 10 Tcyc
1: 17 to 20 Tcyc (1 Tcyc = 1/f1 (s))

The setup time is doubled when the IICTCHALF bit in the IICCR register is set to 1, and halved when the IICTCTWI bit in the IICCR register is set to 1.

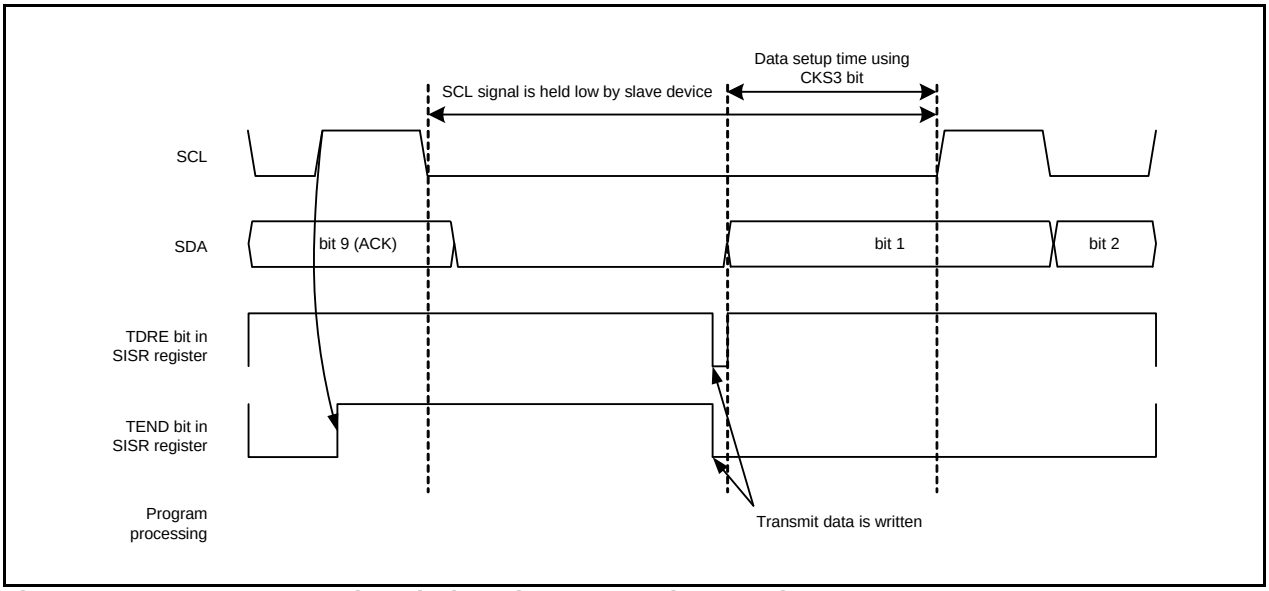


Figure 22.25 Data Setup Time during Slave Transmit Operation

22.4.2.5.2 Operation when Stop Condition is Detected during I²C Slave Transmit Operation (1)

The following shows the operation and software flow when a stop condition is detected during I²C slave transmit operation.

(1) Set to slave receive mode.
(2) Clear the TDRE bit by software.

Note:
1. When a start condition is detected during slave transmit operation, any address following that condition cannot be received. Reset the control block and input a start condition again.

22.4.2.6 Slave Receive Operation

In slave receive mode, the master device outputs the transmit clock and data, and the slave device returns an acknowledge signal. Figures 22.26 and 22.27 show the Operation Timing in Slave Receive Mode (I²C bus Interface Mode).

The receive procedure and operation in slave receive mode are as follows:

(1) Set the ICE bit in the SICR1 register to 1 (transfer operation enabled). Then, set bits CPOS_WAIT and MLS in the SIMR1 register and bits CKS0 to CKS3 in the SICR1 register (initial setting). Next, set bits TRS and MST in the SICR1 register to 0 and wait until the slave address matches in slave receive mode.
(2) When the slave address matches at the first frame after detecting the start condition, the slave device outputs the level set by the CEIE_ACKBT bit in the SIER register to the SDA pin between the falling edge of the 8th clock cycle and the falling edge of the 9th clock cycle. Since the RDRF bit in the SISR register is set to 1 at the rising edge of the 9th clock cycle, perform a dummy read of the SIRDR register (the read data is unnecessary because it indicates the slave address and R/W).
(3) Read the SIRDR register every time the RDRF bit is set to 1. If the 8th clock cycle falls while the RDRF bit is 1, the SCL signal is held low until the SIRDR register is read. The setting change of the acknowledge signal returned to the master device before reading the SIRDR register takes effect from the following transfer frame.
(4) Reading of the last byte is also performed by reading the SIRDR register.

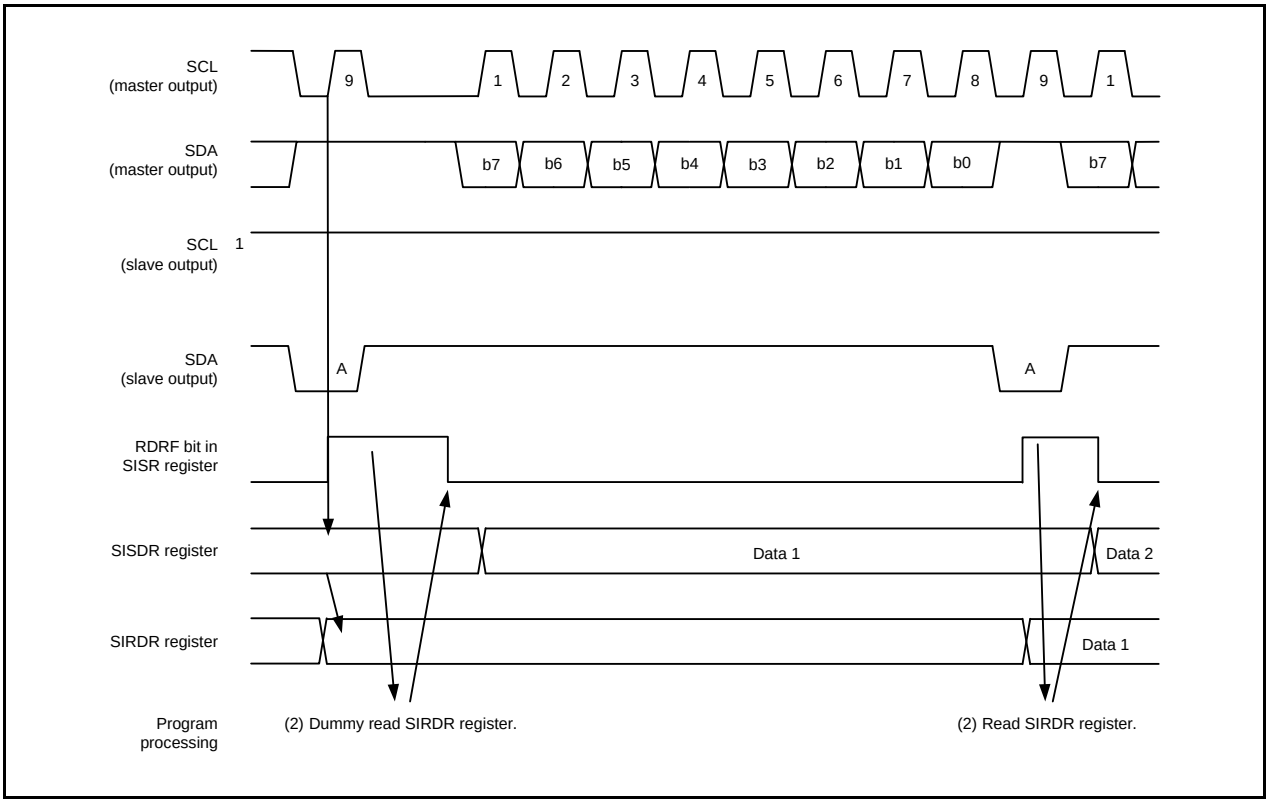


Figure 22.26 Operation Timing in Slave Receive Mode (I^2C bus Interface Mode) (1)

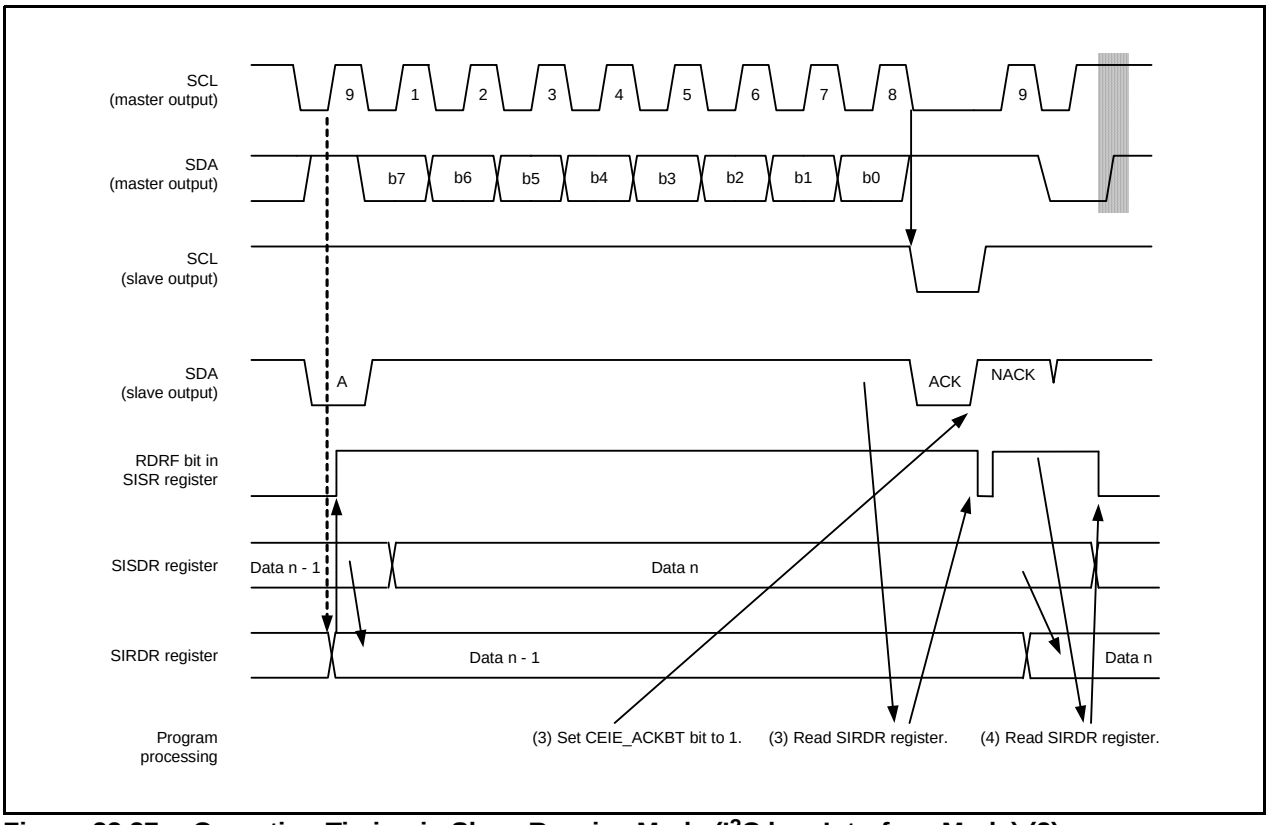


Figure 22.27 Operation Timing in Slave Receive Mode (I^2C bus Interface Mode) (2)

22.4.3 Clock Synchronous Serial Mode

22.4.3.1 Clock Synchronous Serial Format

When the MS bit in the SIMR2 register is set to 1, clock synchronous serial format is used for communication. Figure 22.28 shows the Transfer Format for Clock Synchronous Serial Mode.

When the MST bit in the SICR1 register is 1, the transfer clock is output from the SCL pin. When the MST bit is set to 0, the external clock is input.

The transfer data is output between successive falling edges of the SCL clock, and data is determined at the rising edge of the SCL clock. MSB first or LSB first can be selected as the order of the data transfer by setting the MLS bit in the SIMR1 register. The SDA output level can be changed by the SDAO bit in the SICR2 register during transfer standby.

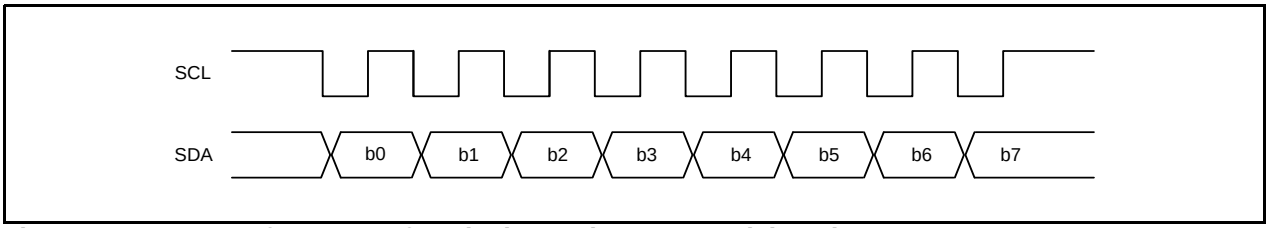


Figure 22.28 Transfer Format for Clock Synchronous Serial Mode

22.4.3.2 Transmit Operation

In transmit mode, transmit data is output from the SDA pin in synchronization with the falling edge of the transfer clock. The transfer clock is output when the MST bit in the SICR1 register is 1 and input when the MST bit is 0.
Figure 22.29 shows the Operation Timing in Transmit Mode (Clock Synchronous Serial Mode).

The transmit procedure and operation in transmit mode are as follows:

(1) Set the ICE bit in the SICR1 register to 1 (transfer operation enabled). Then, set bits CKS0 to CKS3 in the SICR1 register and the MST bit (initial setting).
(2) Set the TRS bit in the SICR1 register to 1 to select transmit mode. This will set the TDRE bit in the SISR register to 1.
(3) After confirming that the TDRE bit is 1, write transmit data to the SITDR register. Data is transferred from registers SITDR to SISDR and the TDRE bit is automatically set to 1. Continuous transmission is enabled by writing data to the SITDR register every time the TDRE bit is set to 1. To switch from transmit to receive mode, set the TRS bit to 0 while the TDRE bit is 1.

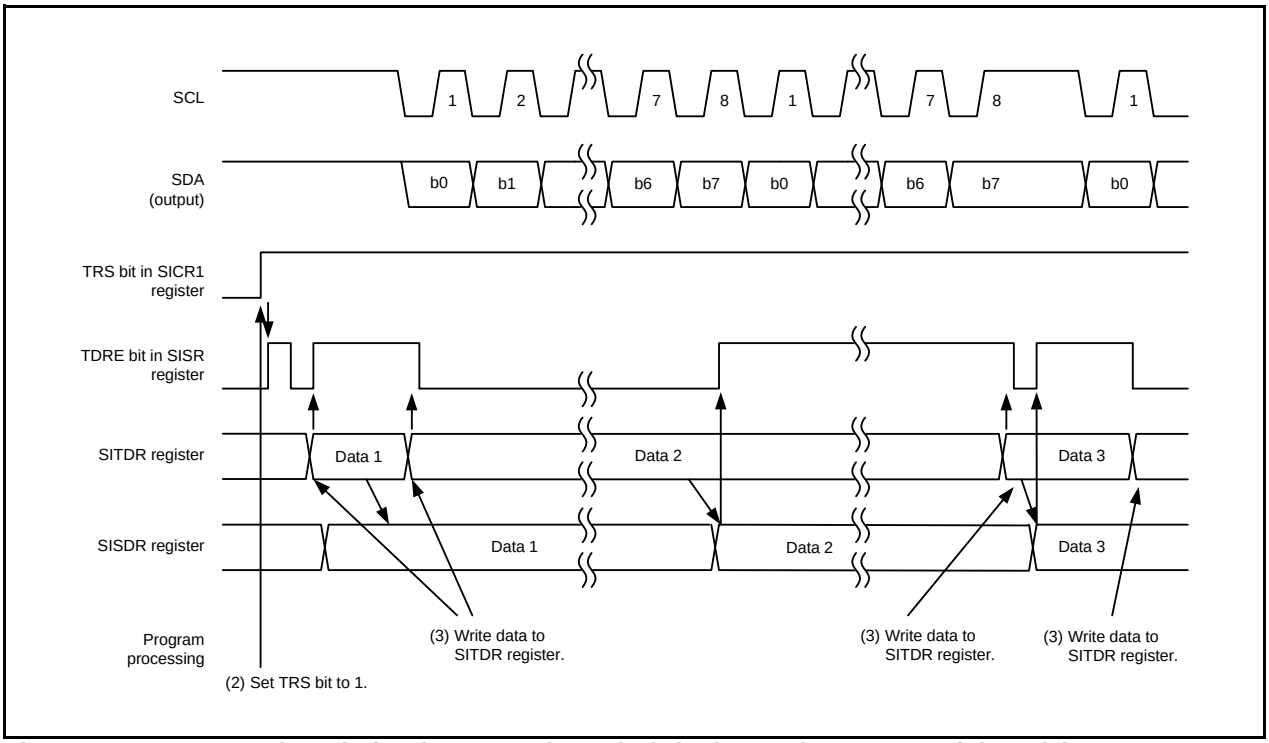


Figure 22.29 Operation Timing in Transmit Mode (Clock Synchronous Serial Mode)

22.4.3.3 Receive Operation

In receive mode, data is latched at the rising edge of the transfer clock. The transfer clock is output when the MST bit in the SICR1 register is 1 and input when the MST bit is 0.
Figure 22.30 shows the Operation Timing in Receive Mode (Clock Synchronous Serial Mode).

The receive procedure and operation in receive mode are as follows:

(1) Set the ICE bit in the SICR1 register to 1 (transfer operation enabled). Then, set bits CKS0 to CKS3 in the SICR1 register and the MST bit (initial setting).
(2) Set the MST bit to 1 while the transfer clock is being output. This will start the output of the receive clock.
(3) When the receive operation is completed, data is transferred from registers SISDR to SIRDR and the RDRF bit in the SISR register is set to 1. When the MST bit is set to 1, the clock is output continuously since the next byte of data is enabled for reception. Continuous reception is enabled by reading the SIRDR register every time the RDRF bit is set to 1. If the 8th clock cycle falls while the RDRF bit is 1, an overrun is detected and the ORER_AL bit in the SISR register is set to 1. At this time, the last receive data is retained in the SIRDR register.
(4) When the MST bit is 1, set the RCVD bit in the SICR1 register to 1 (next receive operation disabled) to stop reception before reading the SIRDR register. The SCL signal is held high after the following byte of data reception is completed.

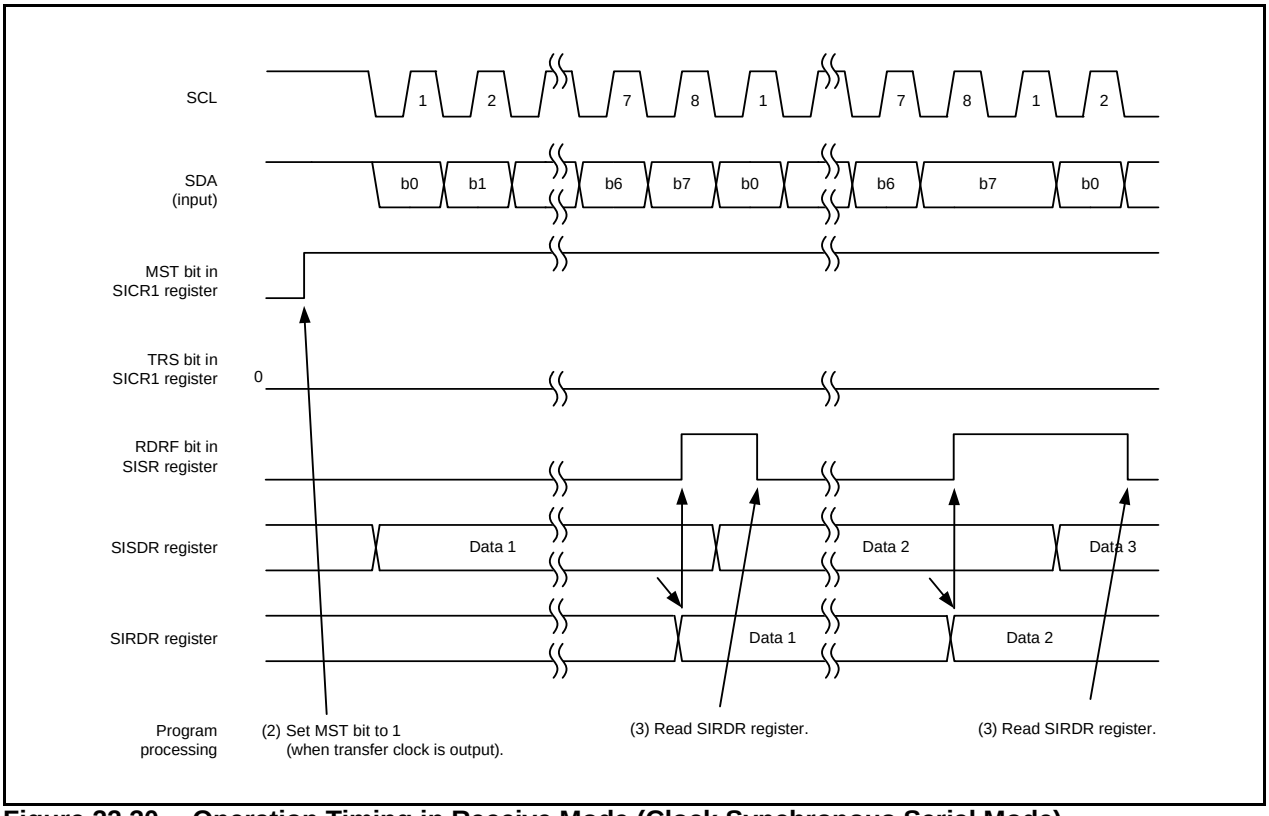


Figure 22.30 Operation Timing in Receive Mode (Clock Synchronous Serial Mode)

22.4.4 Register Setting Examples

Figures 22.31 to 22.34 show examples of register setting when the I²C bus interface is used.

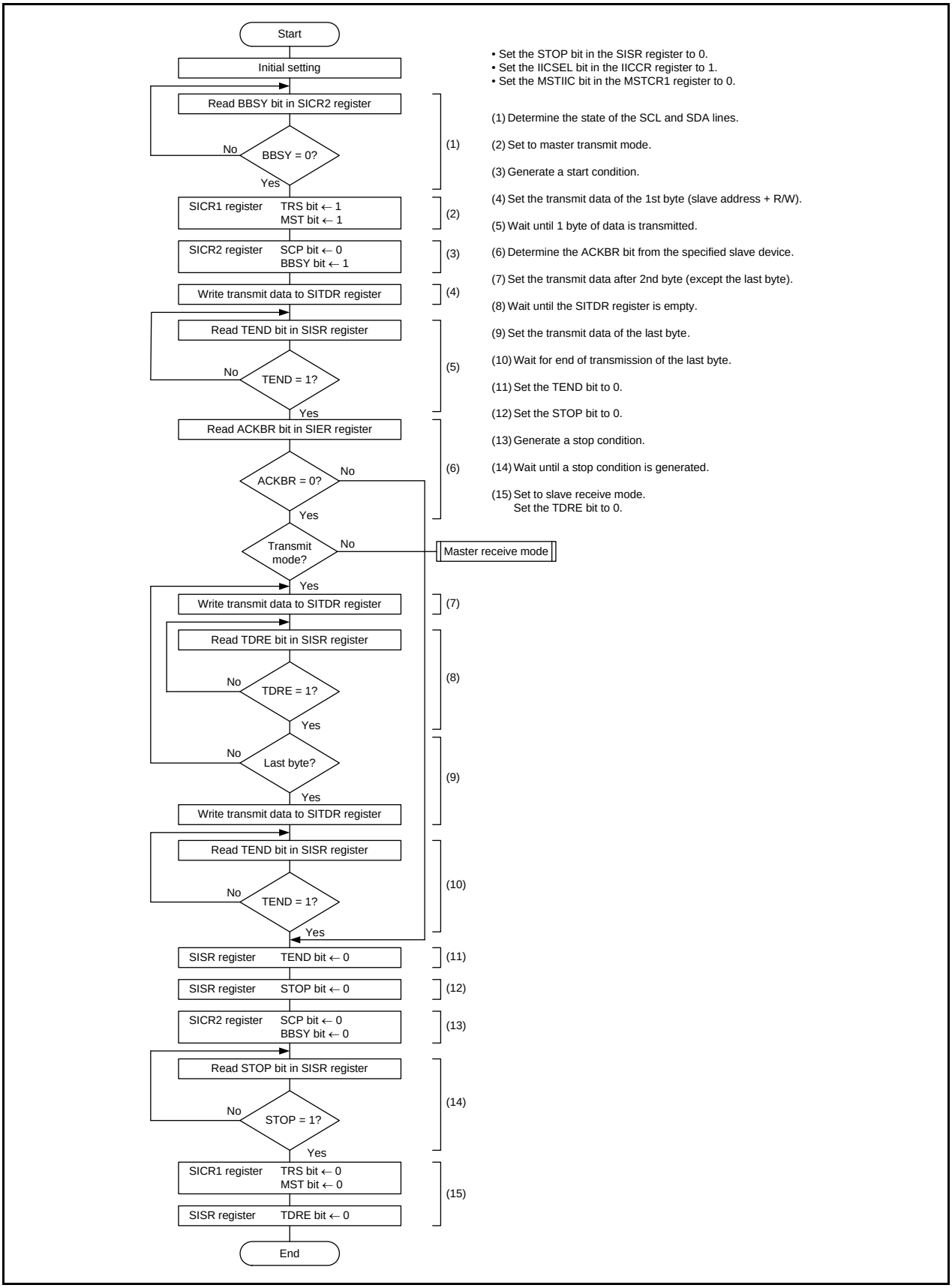
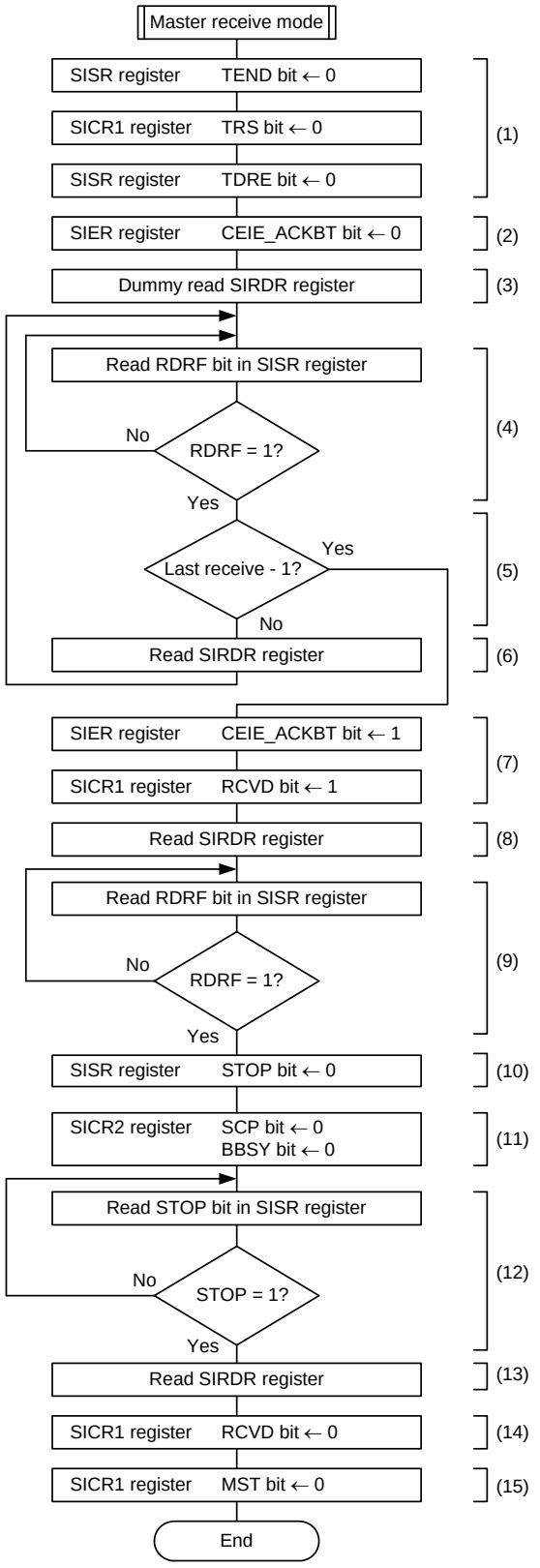


Figure 22.31 Register Setting Example in Master Transmit Mode (I²C bus Interface Mode)



(1) Set the TEND bit to 0 and set to master receive mode. Set the TDRE bit to 0. (1, 2)

(2) Set the CEIE_ACKBT bit to the transmit device. (1)

(3) Dummy read the SIRDR register. (1)

(4) Wait until 1 byte is received.

(5) Determine (last receive - 1).

(6) Read the receive data.

(7) Set the ACKBT bit of the last byte and set continuous receive operation to disable (RCVD = 1). (2)

(8) Read the receive data of (last byte - 1).

(9) Wait until the last byte is received.

(10) Set the STOP bit to 0.

(11) Generate a stop condition.

(12) Wait until a stop condition is generated.

(13) Read the receive data of the last byte.

(14) Set the RCVD bit to 0.

(15) Set to slave receive mode.

Notes:
1. Do not generate interrupts during process steps (1) to (3).
2. For 1 byte of data reception, skip steps (2) to (6) after step (1) and jump to process step (7). Process step (8) is a dummy read from the SIRDR register.

Figure 22.32 Register Setting Example in Master Receive Mode (I^2C bus Interface Mode)

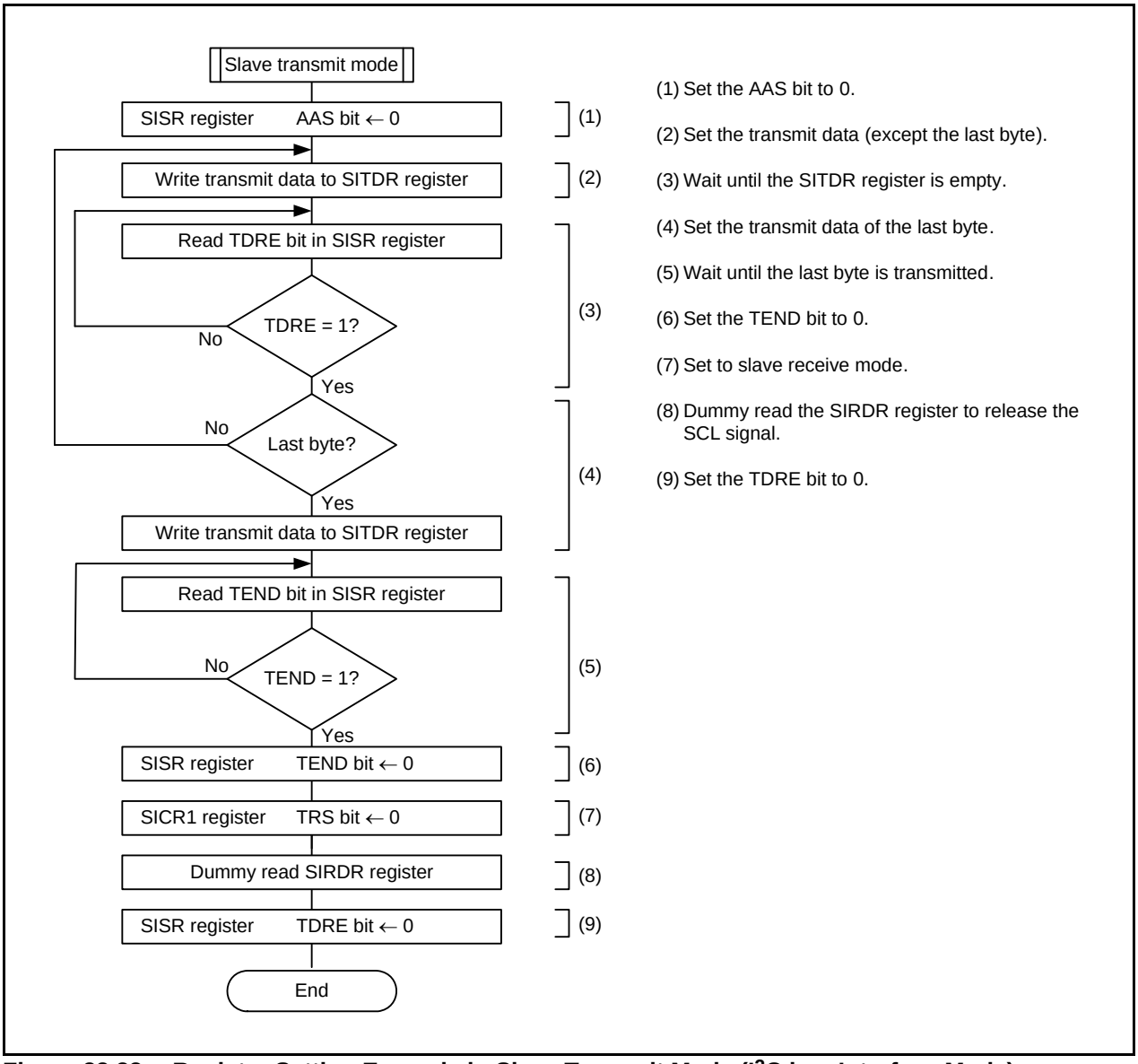
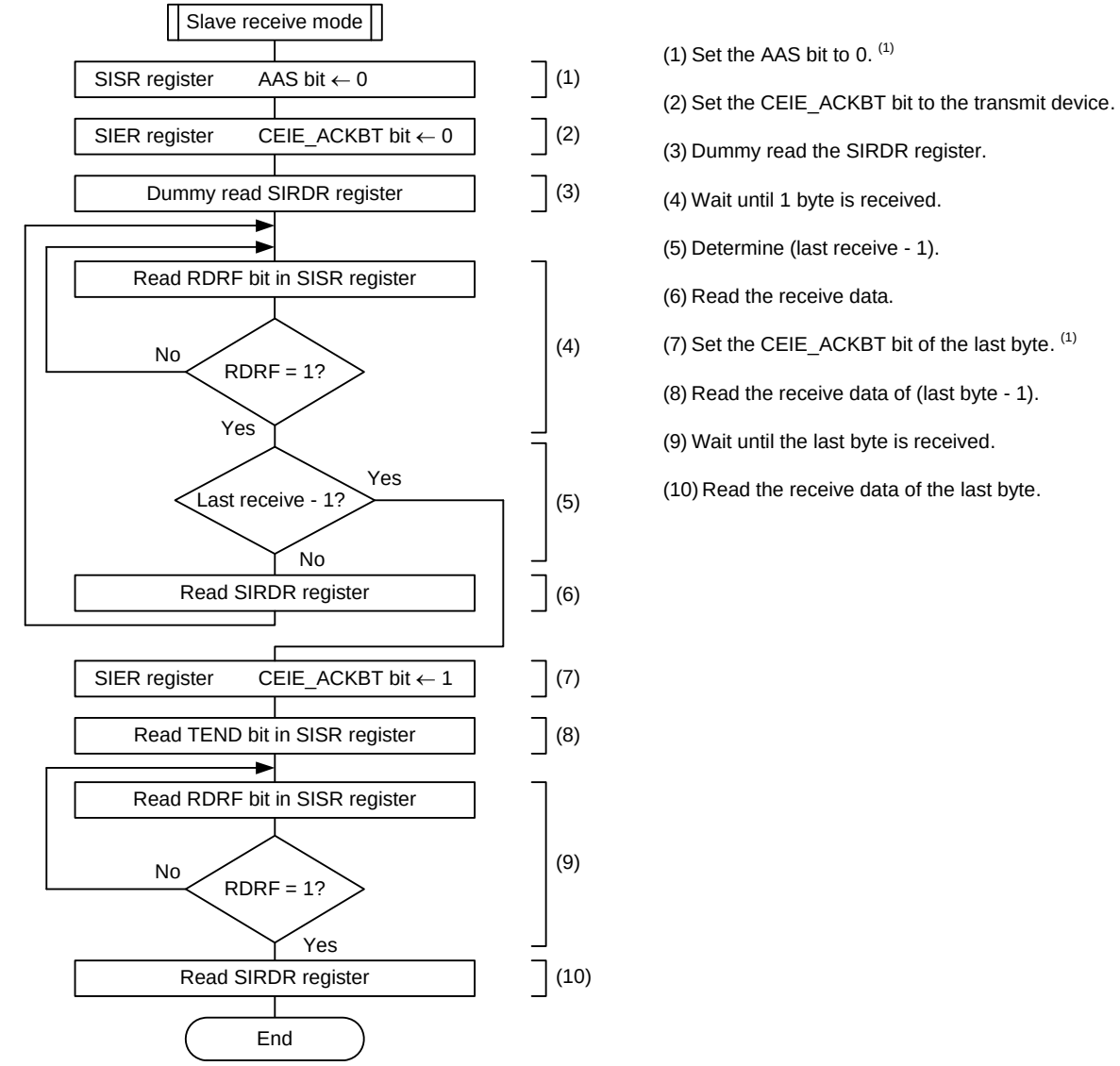


Figure 22.33 Register Setting Example in Slave Transmit Mode (I^2C bus Interface Mode)



Note:
1. For 1 byte of data reception, skip steps (2) to (6) after step (1) and jump to process step (7). Process step (8) is a dummy read from the SIRDR register.

Figure 22.34 Register Setting Example in Slave Receive Mode (I^2C bus Interface Mode)

22.4.5 Noise Canceller

The states of pins SCL and SDA are routed through the noise canceller before being latched internally. Figure 22.35 shows the Noise Canceller Block Diagram.

The noise canceller consists of two cascaded latch and match detection circuits. When the SCL pin input signal (or SDA pin input signal) is sampled on f1 and two latch outputs match, the level is passed forward to the next circuit. When they do not match, the former value is retained.

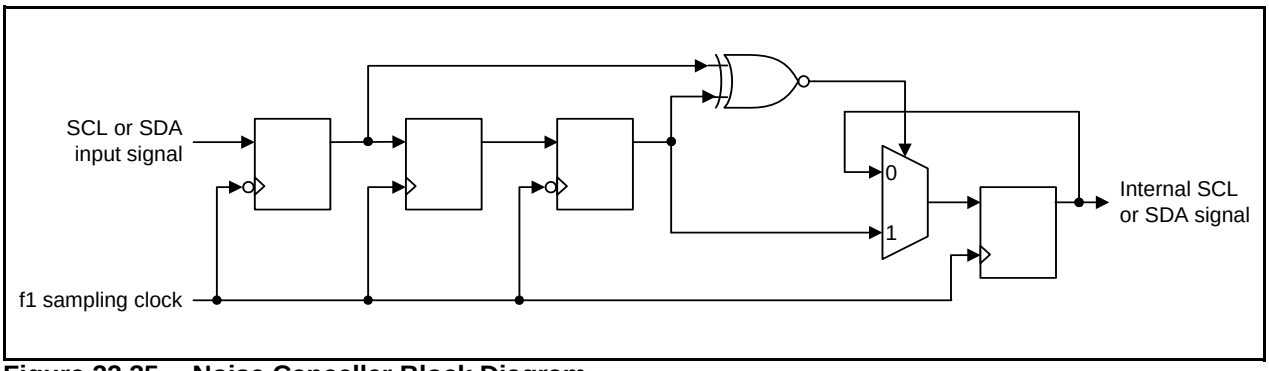


Figure 22.35 Noise Canceller Block Diagram

22.4.6 Bit Synchronization Circuit

When the I^2C bus interface is set to master mode, the high-level period may become shorter in the following two states:

- The SCL signal is held low by a slave device.
- The rising speed of the SCL signal is reduced by a load (load capacity or pull-up resistor) on the SCL line.

In the bit synchronization circuit, the SCL input is monitored after a specified time (MT) from the rising of the SCL output to check whether SCL has become high level. If the SCL is pulled low level by a slave or the rising speed is reduced by a load on the SCL line, it is recognized that SCL is not pulled high level, and the timing for falling of SCL is delayed.

Figure 22.36 shows the Timing of Bit Synchronization Circuit, and Table 22.12 lists the Time between Changing SCL Signal from Low Output to High Impedance and Monitoring SCL Signal.

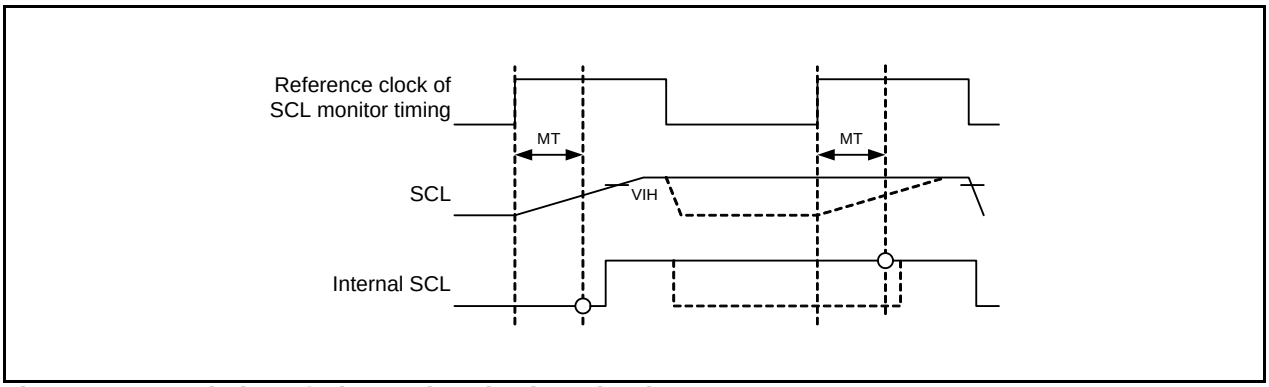


Figure 22.36 Timing of Bit Synchronization Circuit

Table 22.12 Time between Changing SCL Signal from Low Output to High Impedance and Monitoring SCL Signal

SICR1 Register				SCL Monitoring Time (MT)
IICTCHALF	IICTCTW1	CKS3	CKS2	
0	0	0	0	7.5 Tcyc
			1	19.5 Tcyc
		1	0	17.5 Tcyc
			1	41.5 Tcyc
0	1	0	0	2.5 Tcyc
			1	8.5 Tcyc
		1	0	7.5 Tcyc
			1	19.5 Tcyc
1	0	0	0	17.5 Tcyc
			1	41.5 Tcyc
		1	0	37.5 Tcyc
			1	85.5 Tcyc

1 Tcyc = 1/f1 (s)

When CKS3 to CKS0 = 1000b, the bit synchronization circuit does not function even if the high-level width of the SCL signal is 600 ns or less (a breach of the I^2C specification) (when the operating clock is set to 20 MHz).

22.4.7 Coordination with DTC

■ Common to the SSU/I^2C bus functions

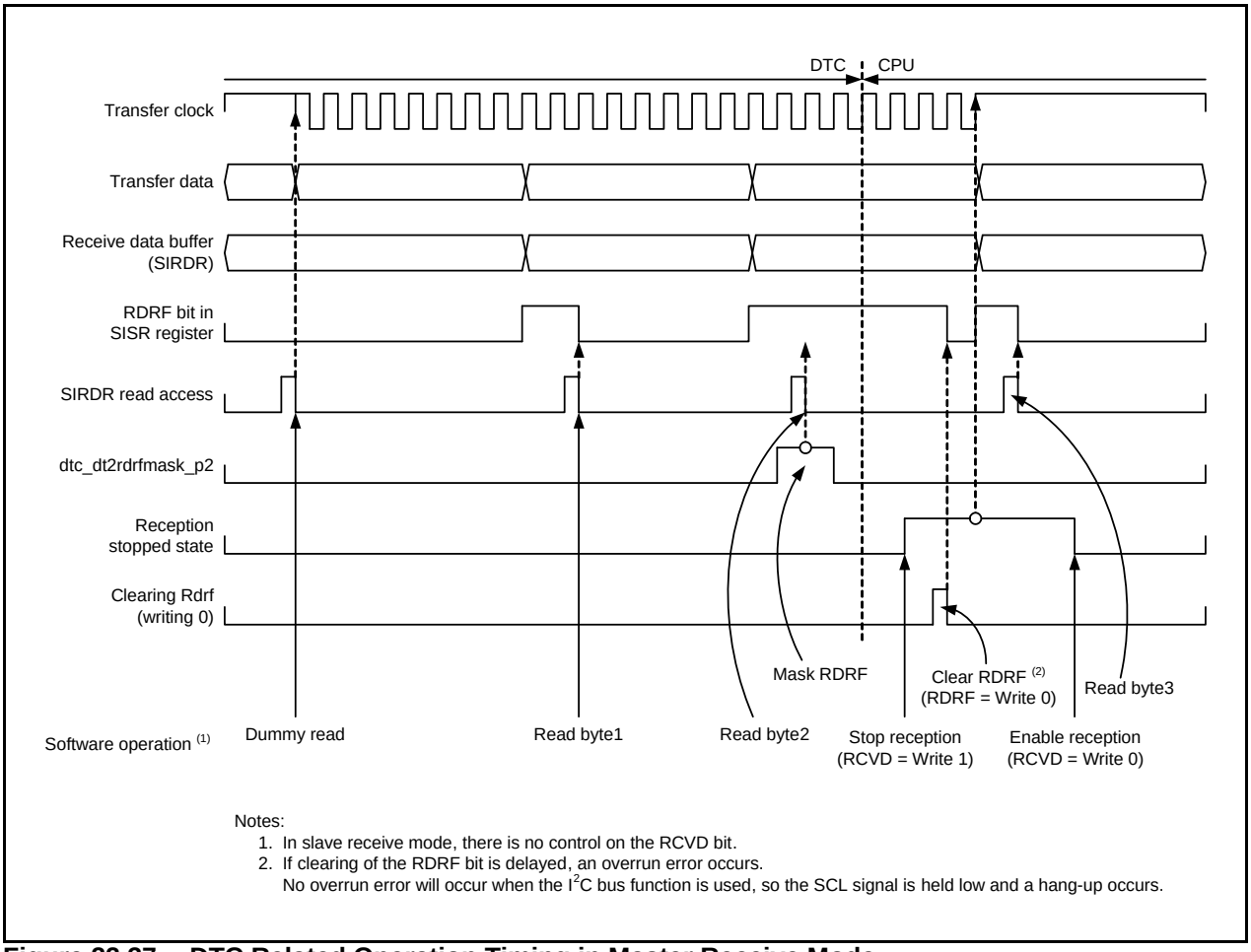
- To read the receive buffer in master mode using the DTC, set the number of transfers minus 1 in the DTC transfer count register.
- After the number of transfers minus 1 of receive data is transferred, an RXI interrupt is generated. Set the RCVD bit in the SICR1 register to 1 (next receive operation disabled) and then set the RDRF bit in the SISR register to 0 (no data in the SIRDR register).
- If clearing of the RDRF bit is delayed and the last byte is transferred, the SCL signal is held low and a hang-up occurs when the I^2C bus function is used. When the SSU function is used, an overrun error occurs.
- Setting of the RCVD bit in the SICR1 register must be performed during the receive operation of the last byte.

■ SSU Function

- After the last data is received, an RXI interrupt is generated. Set the RE_STIE bit in the SIER register to 0 (reception disabled) and the RCVD bit 0 (next receive operation continues) before reading the SIRDR register by software.

■ I^2C bus Function

- After the last data is received, an RXI interrupt is generated. Confirm that the SCLO bit (SCL monitor flag) in the SICR2 register is set to 0 before generating a stop condition.
- When the STOP bit in the SISR register is set to 1 (a stop condition is detected after the frame is transferred), read the SIRDR register. Then set the RCVD bit 0 (next receive operation continues).



Notes:
1. In slave receive mode, there is no control on the RCVD bit.
2. If clearing of the RDRF bit is delayed, an overrun error occurs.
   No overrun error will occur when the I^2C bus function is used, so the SCL signal is held low and a hang-up occurs.

Figure 22.37 DTC Related Operation Timing in Master Receive Mode

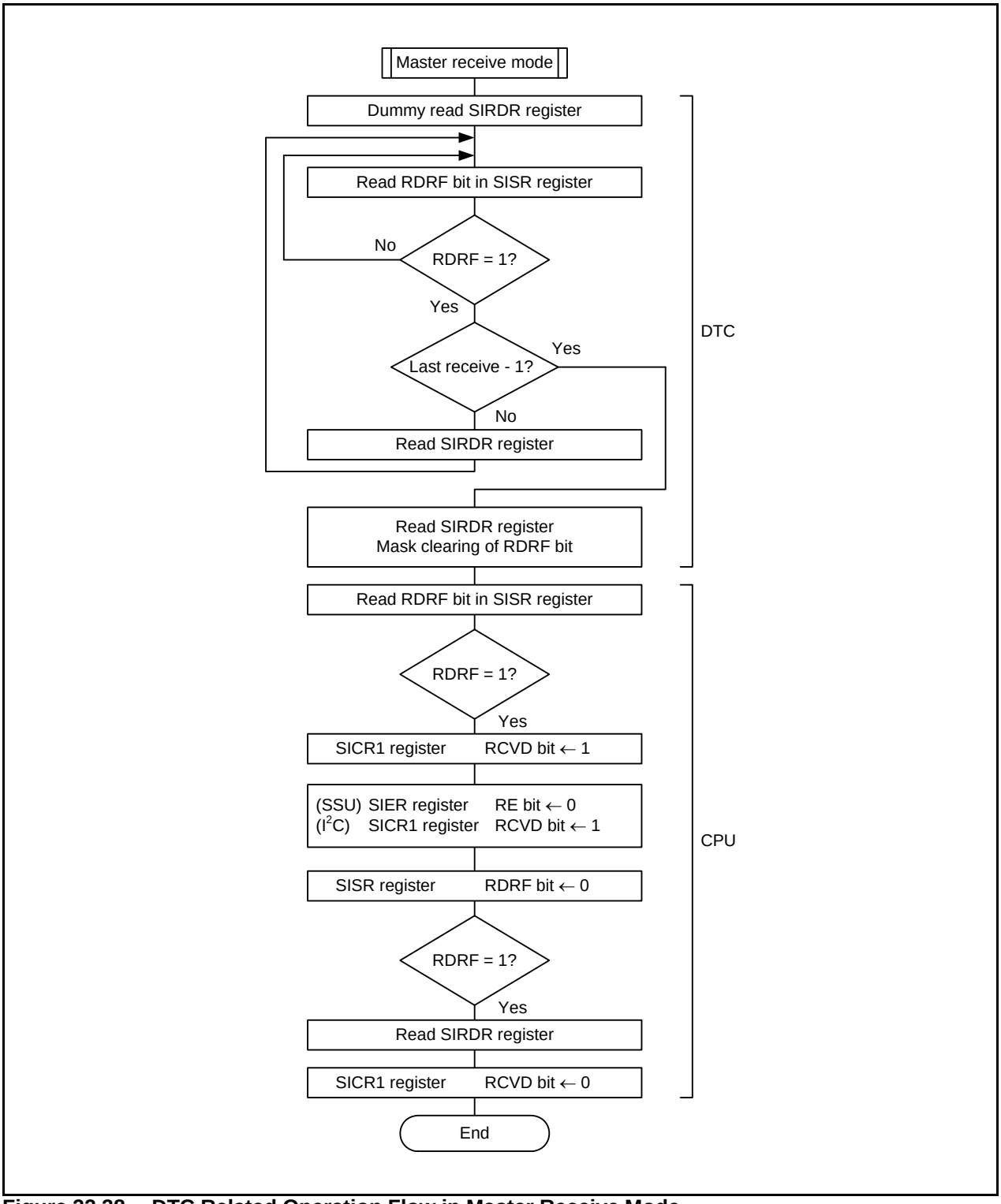


Figure 22.38 DTC Related Operation Flow in Master Receive Mode

22.4.8 Procedure for Resetting Control Block in I²C bus Interface Mode

In the I²C bus interface, some of the I²C bus function registers and the control block can be reset by writing 1 to the SIRST bit in the SICR2 register.
The reset procedure using the SIRST bit is shown below.
When the control block is reset (as in Figure (2)), the corresponding IR bit in the SSUIC_i/IICIC_i register (i = 0 to 2) for the ICU may be set to 1 (interrupt requested).
For the usage notes on clearing the IR bit, refer to **11.9.4 Changing Interrupt Sources**.

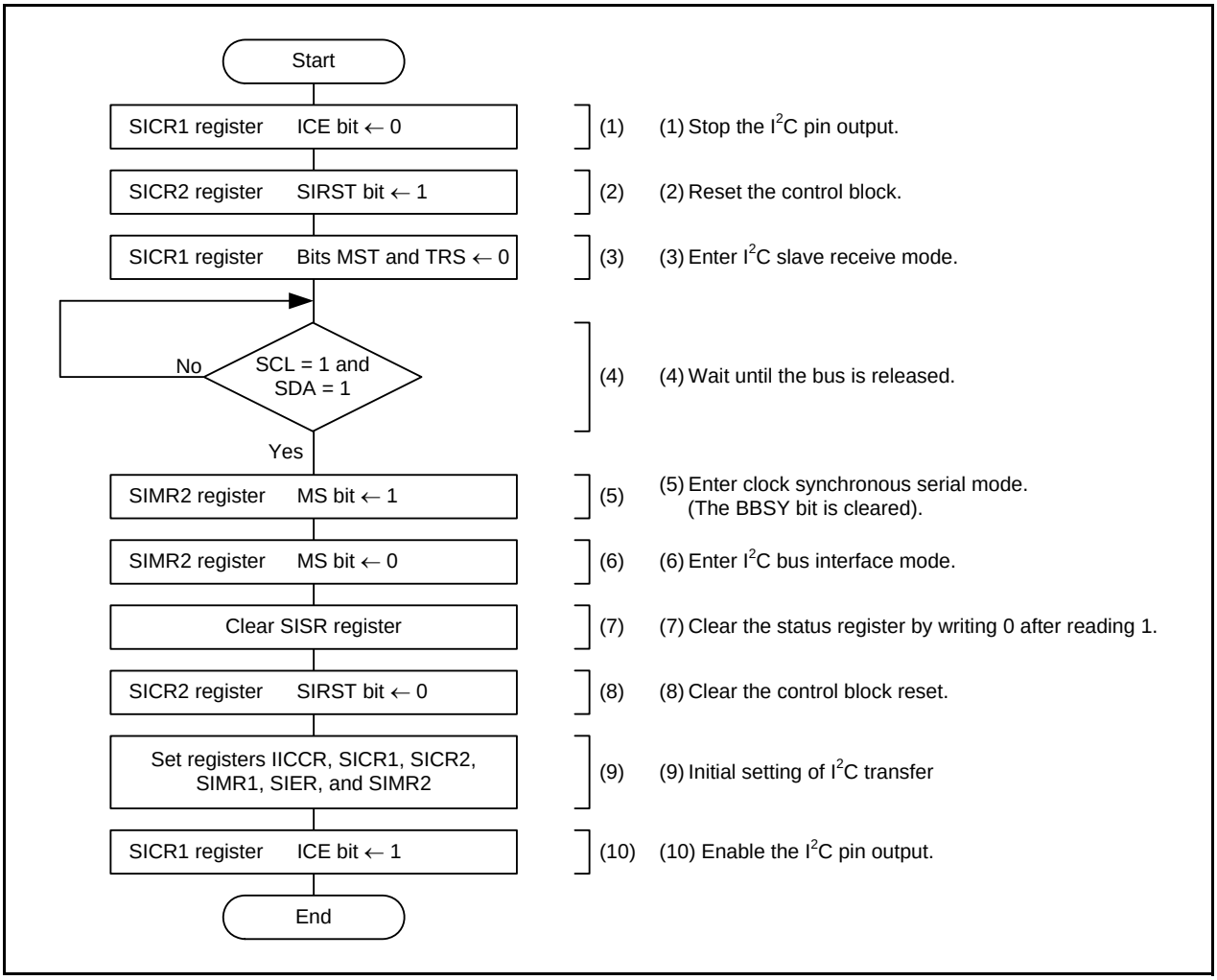


Figure 22.39 Procedure for Resetting Control Block in I²C bus Interface Mode

22.5 Notes on Clock Synchronous Serial Interface

22.5.1 Notes on Synchronous Serial Communication Unit

To use the synchronous serial communication unit, set the IICSEL bit in the IICCR register to 0 (SSU function selected).

22.5.2 Notes on I²C bus Interface

To use the I²C bus interface, set the IICSEL bit in the IICCR register to 1 (I²C bus function selected).

(1) Do not use the I²C interface with settings that do not comply with the I²C specification.
(2) Communication using “Hs-MODE” cannot be performed. The maximum transfer rate is [a maximum of 400 kHz] in “FAST-MODE”.
(3) The low-level period of the SCL signal is [a minimum of 1.3 μs] in “FAST-MODE”. Since the high-level/low-level width of the duty cycle for this module is 50%/50%, this value is not reached during operation at 400 kHz. Therefore, the maximum transfer rate is 2.6 μs for the SCL period (maximum transfer frequency is 384.6 kHz).
(4) There must be a delay of [a minimum of 300 ns] for the SDA pin to change at the rising edge of the SCL signal. The SDA digital delay for this module must be at least 3 x f1 cycles, care must be taken when the reference clock f1 is set to 11 MHz or above. Set bits SDADLY1 and SDADLY0 to 01b or more.
(5) There is no compatibility with the CBUS.
(6) 10-bit addressing cannot used.
(7) When a start condition is detected while data is transmitted in slave transmit mode, any address following that condition cannot be received and the operation is stopped. Initialize the module according to the flow for resetting the control block.
(8) Do not set 1111XXXb and 0000XXXb as slave addresses.
(9) When starting communication by the master after a stop condition is detected, always clear the STOP bit in the SISR register to 0.

22.5.3 ICE Bit in SICR1 Register and SIRST Bit in SICR2 Register

While the I²C bus interface is operating, when 0 is written to the ICE bit or 1 is written to the SIRST bit in the SICR2 register, the values of the BBSY bit in the SICR2 register and the STOP bit in the SISR register may be undefined.

22.5.3.1 Conditions when Values of Bits are Undefined

- When this module occupies the I²C bus in master mode of the I²C bus interface.
- While this module transmits data or an acknowledge in slave mode of the I²C bus interface.

22.5.3.2 Countermeasures

- When a start condition (falling of SDA when SCL is high) is input, the BBSY bit is set to 1.
- When a stop condition (rising of SDA when SCL is high) is input, the BBSY bit is set to 0.
- In master transmit mode, while SCL and SDA are both high, when 1 is written to the BBSY bit, 0 is written to the SCP bit, and a start condition (falling of SDA when SCL is high) is output, the BBSY bit is set to 1.
- In master transmit mode or master receive mode, while SDA is low and this module is the only device that pulls SCL low, when 0 is written to the BBSY bit, 0 is written to the SCP bit in the SICR2 register, and a stop condition (rising of SDA when SCL is high) is output, the BBSY bit is set to 1.
- When 1 is written to the MS bit in the SAR register, the BBSY bit is set to 0.

22.5.3.3 Additional Description on SIRST Bit in SICR2 Register

- When 1 is written to the SIRST bit, bits SDAO and SCLO in the SICR2 register are set to 1.
- In master transmit mode or slave transmit mode, when 1 is written to the SIRST bit, the TDRE bit in the SISR register is set to 1.
- While the I^2C bus control block is reset by the SIRST bit, writing to the BBSY bit in the SICR2 register and bits SCP and SDAO is disabled. Thus, write 0 to the SIRST bit before writing to any of these bits.
- The BBSY bit is not set to 0 even if 1 is written to the SIRST bit. However, depending on the states of SCL and SDA, a stop condition (rising of SDA when SCL is high) is generated, which may set the BBSY bit to 0. Similarly, this may also affect other bits.
- While the I^2C bus control block is reset by the SIRST bit, data transmission and reception are stopped. However, the function to detect a start condition, stop condition, and arbitration lost continues operating. Therefore, the values of registers SICR1, SICR2, and SISR may be updated depending on the signal input to pins SCL and SDA.
- Refer to **22.4.8 Procedure for Resetting Control Block in I^2C bus Interface Mode**, for more details including the above information on the control block reset operation using the SIRST bit.

23. Hardware LIN

The hardware LIN performs LIN communication in cooperation with timer RJ and UART0.
The hardware LIN consists of two channels: HW-LIN_0 and HW-LIN_1.
This chapter describes these channels as LIN unless there are differences between them.

23.1 Overview

The hardware LIN has the features listed below.
Figure 23.1 shows the Hardware LIN Block Diagram.
The wake-up function for each mode is detected using $\overline{\text{INTx}}$ (x = 1 or 2).

[Master mode]
• Synch Break generation
• Bus collision detection

[Slave mode]
• Synch Break detection
• Synch Field measurement
• Control function for Synch Break and Synch Field signal inputs to UART
• Bus collision detection

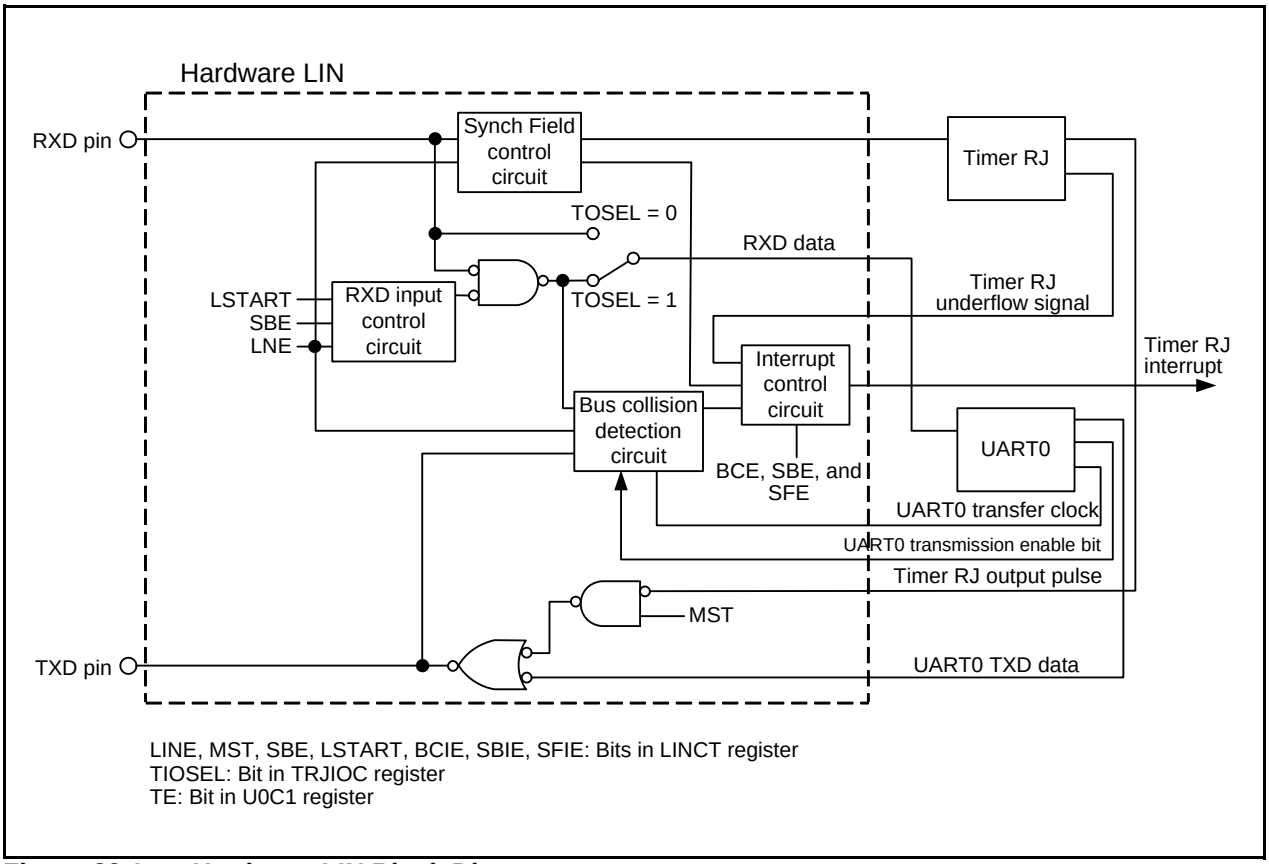


Figure 23.1 Hardware LIN Block Diagram

23.2 Input/Output Pins

Table 23.1 lists the Hardware LIN Pin Configuration.

Table 23.1 Hardware LIN Pin Configuration

Name	Pin Name	I/O	Function
Receive data input	RXD	Input	Receive data input pin for the hardware LIN
Transmit data output	TXD	Output	Transmit data output pin for the hardware LIN

23.3 Registers

Table 23.2 lists the Hardware LIN Register Configuration.

Table 23.2 Hardware LIN Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
LIN_0 Special Function Register	LINCR2_0	00h	0008Ch	8
LIN_0 Control Register	LINCT_0	00h	0008Eh	8
LIN_0 Status Register	LINST_0	00h	0008Fh	8
LIN_1 Special Function Register	LINCR2_1	00h	0009Ch	8
LIN_1 Control Register	LINCT_1	00h	0009Eh	8
LIN_1 Status Register	LINST_1	00h	0009Fh	8

23.3.1 LIN Special Function Register (LINCR2)

Address 0008Ch (LINCR2_0), 0009Ch (LINCR2_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	BCE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BCE	Bus collision detection during Sync Break transmission enable bit	0: Bus collision detection disabled 1: Bus collision detection enabled	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

23.3.2 LIN Control Register (LINCT)

Address 0008Eh (LINCT_0), 0009Eh (LINCT_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LINE	MST	SBE	LSTART	RXDSF	BCIE	SBIE	SFIE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SFIE	Synch Field measurement-completed interrupt enable bit	0: Synch Field measurement-completed interrupt disabled 1: Synch Field measurement-completed interrupt enabled	R/W
b1	SBIE	Synch Break detection interrupt enable bit	0: Synch Break detection interrupt disabled 1: Synch Break detection interrupt enabled	R/W
b2	BCIE	Bus collision detection interrupt enable bit	0: Bus collision detection interrupt disabled 1: Bus collision detection interrupt enabled	R/W
b3	RXDSF	RXD input status flag	0: RXD input enabled 1: RXD input disabled	R
b4	LSTART	Synch Break detection start bit (1)	When this bit is set to 1, timer RJ input is enabled and RXD input is disabled. The read value is 0	R/W
b5	SBE	RXD input unmasking timing select bit (effective only in slave mode)	0: Unmasked after Synch Break detected 1: Unmasked after Synch Field measurement completed	R/W
b6	MST	LIN operation mode set bit (2)	0: Slave mode (Synch Break detection circuit operation) 1: Master mode (timer RJ output OR'ed with TXD)	R/W
b7	LINE	LIN operation start bit	0: LIN operation stops 1: LIN operation starts (3)	R/W

Notes:
1. After setting the LSTART bit, confirm that the RXDSF bit is set to 1 (RXD input disabled) before Synch Break input starts.
2. Before switching LIN operation modes, stop the LIN operation (LINE bit = 0) once.
3. Inputs to timer RJ and UART are disabled immediately after the LINE bit is set to 1 (LIN operation starts). Refer to **Figures 23.3** and **23.4 Header Field Transmission Flowchart Examples** and **Figures 23.6** to **23.8 Header Field Reception Flowchart Examples**.

23.3.3 LIN Status Register (LINST)

Address 0008Fh (LINST_0), 0009Fh (LINST_1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	B2CLR	B1CLR	B0CLR	BCDCT	SBDCT	SFDCT
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SFDCT	Synch Field measurement-completed flag	When this bit is set to 1, Synch Field measurement is completed.	R
b1	SBDCT	Synch Break detection flag	When this bit is set to 1, Synch Break is detected or Synch Break generation is completed.	R
b2	BCDCT	Bus collision detection flag	When this bit is set to 1, bus collision is detected.	R
b3	B0CLR	SFDCT bit clear bit	When this bit is set to 1, the SFDCT bit is set to 0. The read value is 0.	R/W
b4	B1CLR	SBDCT bit clear bit	When this bit is set to 1, the SBDCT bit is set to 0. The read value is 0.	R/W
b5	B2CLR	BCDCT bit clear bit	When this bit is set to 1, the BCDCT bit is set to 0. The read value is 0.	R/W
b6	—	Reserved	The write value must be 0. The read value is 0.	R/W
b7	—			

23.4 Operation

23.4.1 Master Mode

Figure 23.2 shows an Operation Example during Header Field Transmission master mode. Figures 23.3 and 23.4 show Header Field Transmission Flowchart Examples.
During header field transmission, the hardware LIN operates as follows:

(1) When 1 (count starts) is written to the TSTART bit in the TRJCR register of timer RJ, the TXD pin outputs a low level for the period set in the TRJ register of timer RJ.
(2) When timer RJ underflows, the TXD pin output is inverted and the SBDCT bit in the LINST register is set to 1 (Synch Break is detected or Synch Break generation is completed). If the SBIE bit in the LINCT register is set to 1 (Synch Break detection interrupt enabled), a timer RJ interrupt is generated.
(3) The hardware LIN transmits 55h via UART0.
(4) After the hardware LIN completes transmitting 55h, it transmits an ID field via UART0.
(5) After the hardware LIN completes transmitting the ID field, it performs communication for a response field.

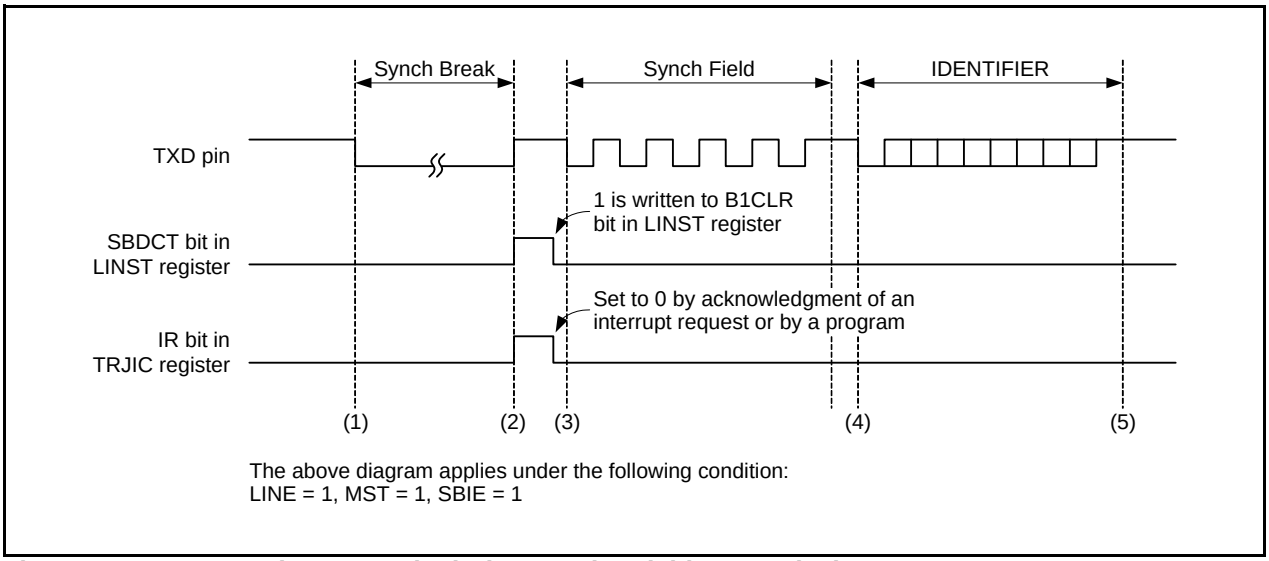
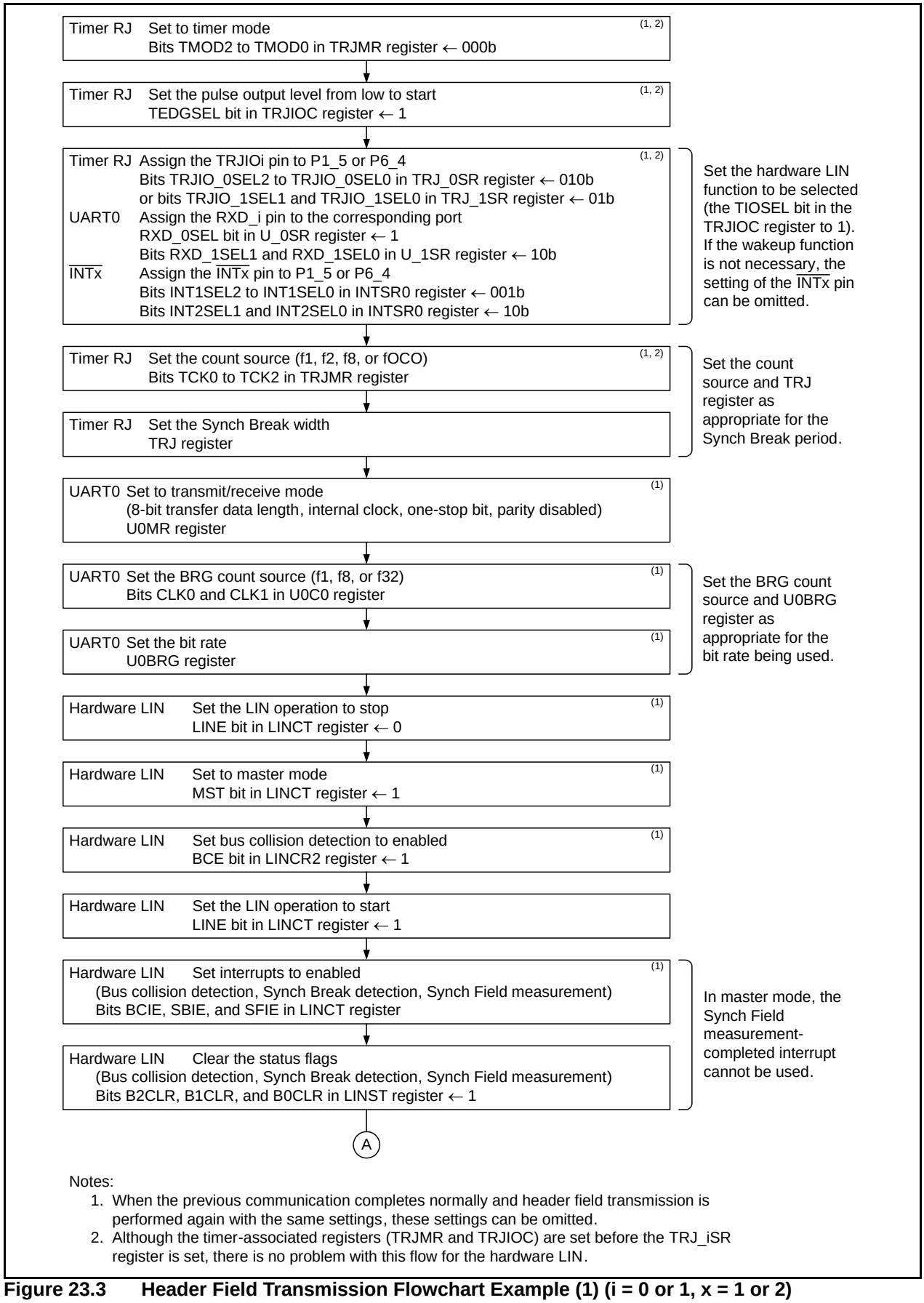


Figure 23.2 Operation Example during Header Field Transmission



Notes:
1. When the previous communication completes normally and header field transmission is performed again with the same settings, these settings can be omitted.
2. Although the timer-associated registers (TRJMR and TRJIOC) are set before the TRJ_iSR register is set, there is no problem with this flow for the hardware LIN.

Figure 23.3 Header Field Transmission Flowchart Example (1) (i = 0 or 1, x = 1 or 2)

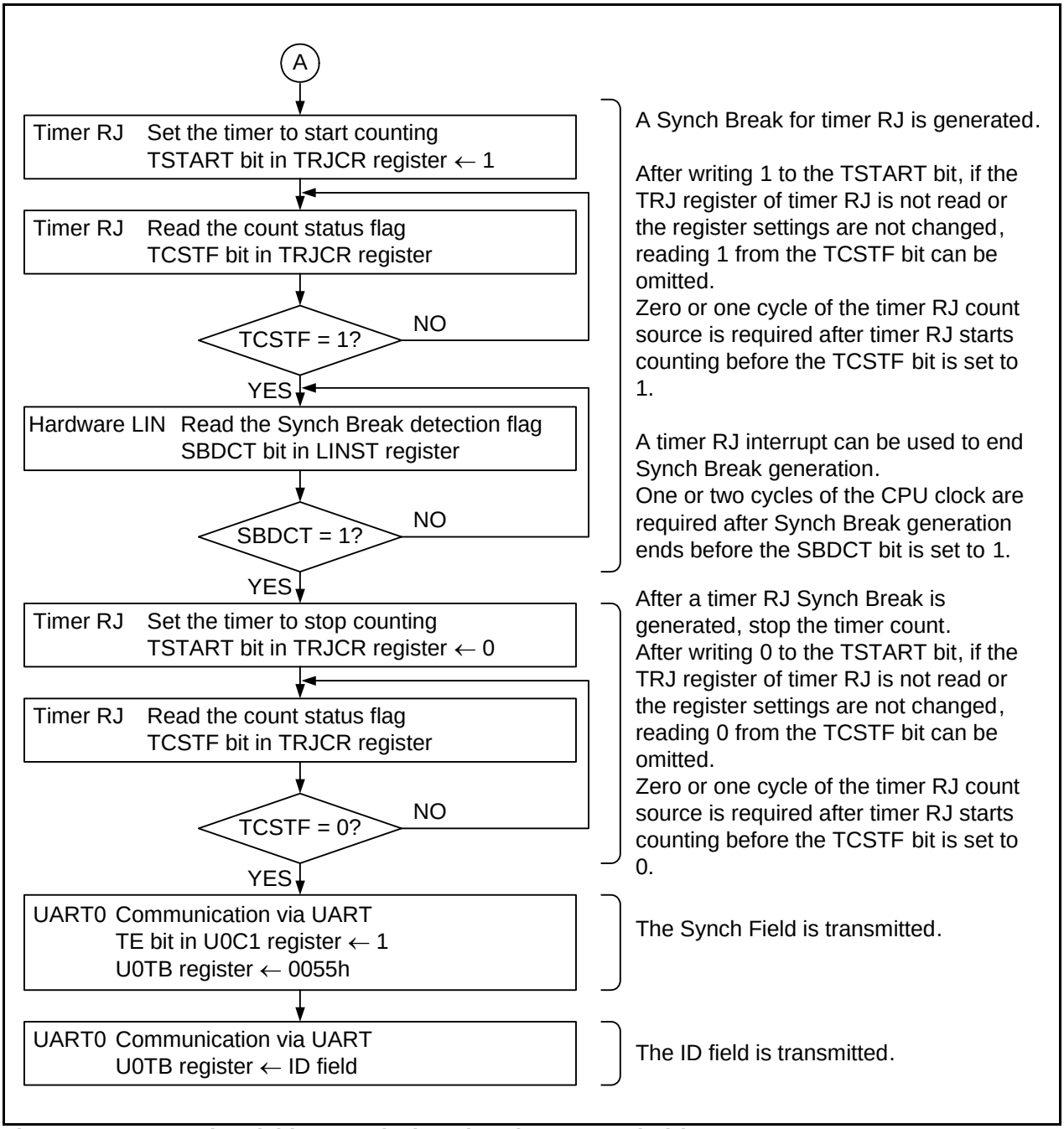


Figure 23.4 Header Field Transmission Flowchart Example (2)

23.4.2 Slave Mode

Figure 23.5 shows an Operation Example during Header Field Reception in slave mode. Figures 23.6 to 23.8 show Examples of Header Field Reception Flowchart.
During header field reception, the hardware LIN operates as follows:

(1) When 1 (timer RJ input enabled, RXD input disabled) is written to the LSTART bit in the LINCT register of the hardware LIN, Synch Break detection is enabled.
(2) If a low level is input for a duration equal to or longer than the period set in timer RJ, the hardware LIN detects it as a Synch Break. At this time, the SBDCT bit in the LINST register is set to 1 (Synch Break is detected or Synch Break generation is completed). If the SBIE bit in the LINCT register is set to 1 (Synch Break detection interrupt enabled), a timer RJ interrupt is generated. Then the hardware LIN enters Synch Field measurement.
(3) The hardware LIN receives a Synch Field (55h) and measures the period of the start bit and bits 0 to 6 using timer RJ. At this time, whether or not to input the Synch Field signal to RXD of UART0 can be selected by the SBE bit in the LINCT register.
(4) When Synch Field measurement is completed, the SFDCT flag in the LINST register is set to 1. If the SFIE bit in the LINCT register is set to 1, a timer RJ interrupt is generated.
(5) After Synch Field measurement is completed, a transfer rate is calculated from the timer RJ count value. The rate is set in UART0 and the TRJ register of timer RJ is set again. Then the hardware LIN receives an ID field via UART0.
(6) After the hardware LIN completes receiving the ID field, it performs communication for a response field.

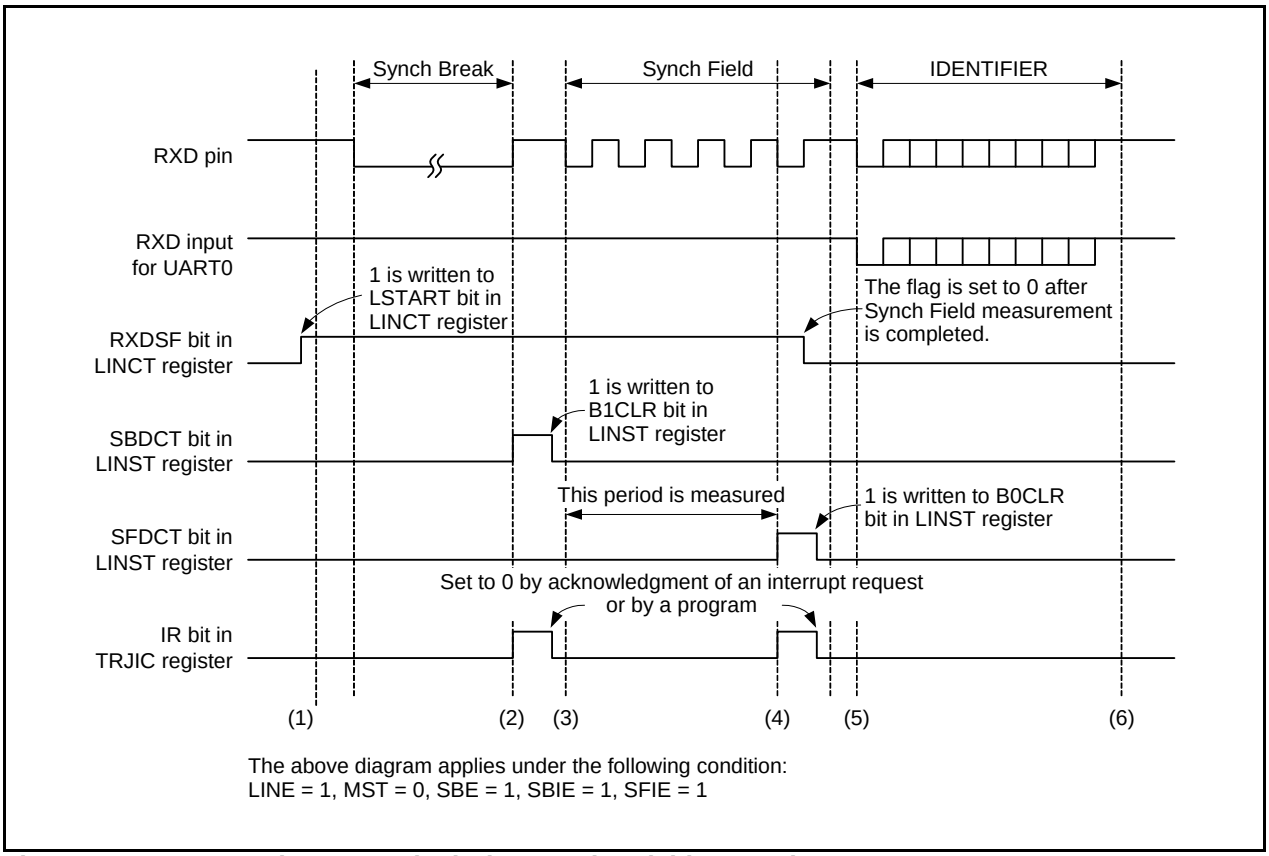
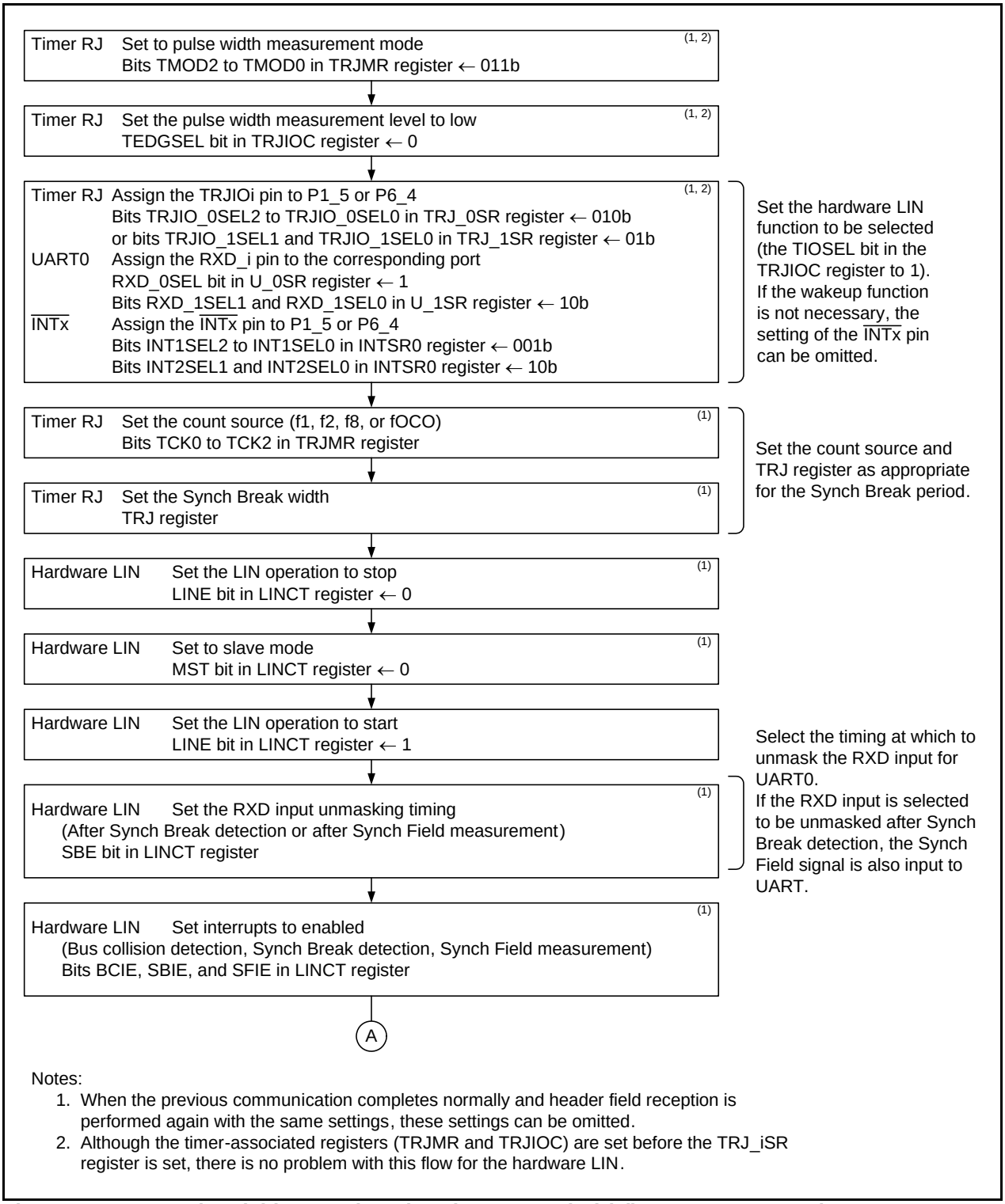


Figure 23.5 Operation Example during Header Field Reception



Notes:
1. When the previous communication completes normally and header field reception is performed again with the same settings, these settings can be omitted.
2. Although the timer-associated registers (TRJMR and TRJIOC) are set before the TRJ_iSR register is set, there is no problem with this flow for the hardware LIN.

Figure 23.6 Header Field Reception Flowchart Example (1) (i = 0 or 1, x = 1 or 2)

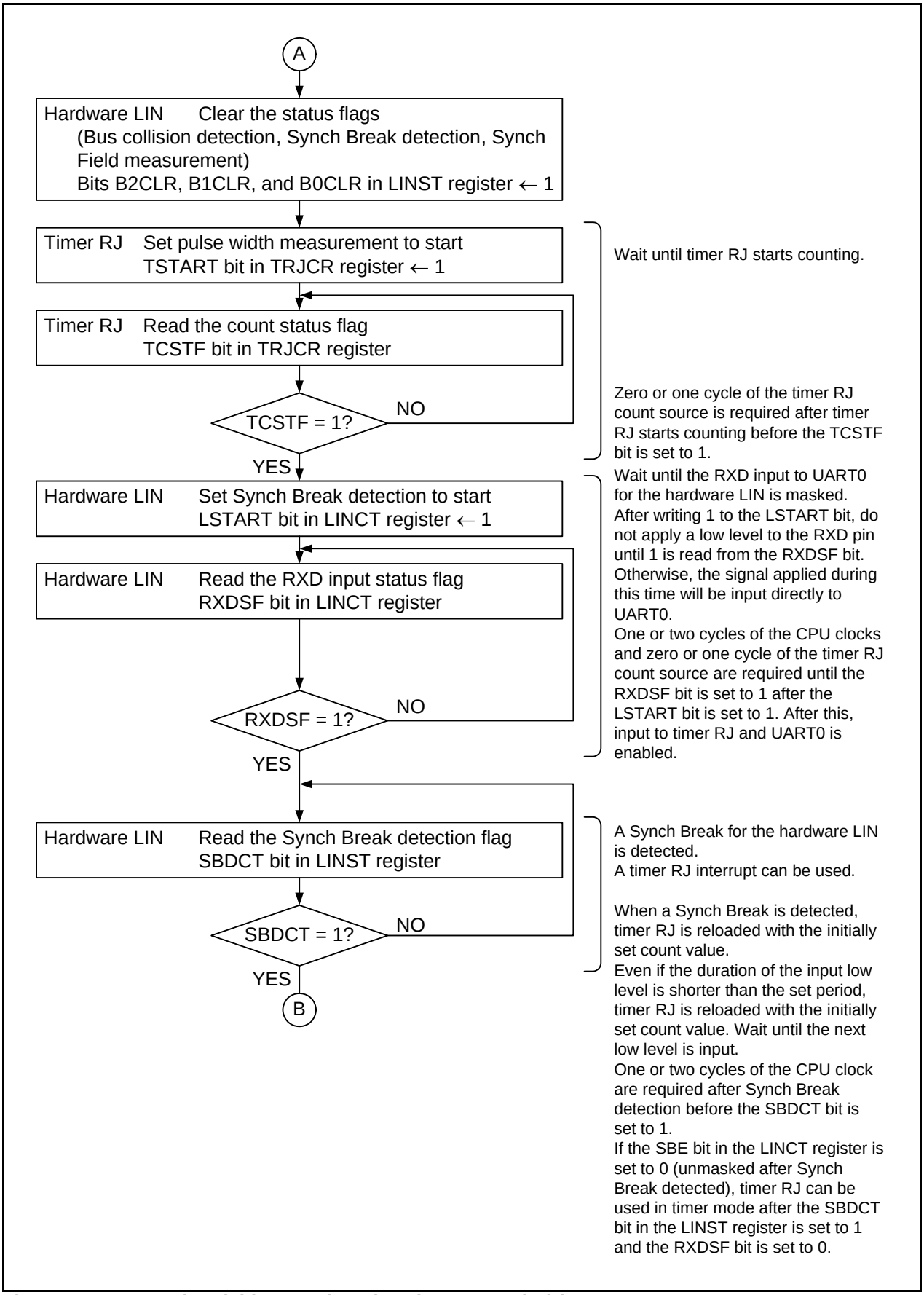


Figure 23.7 Header Field Reception Flowchart Example (2)

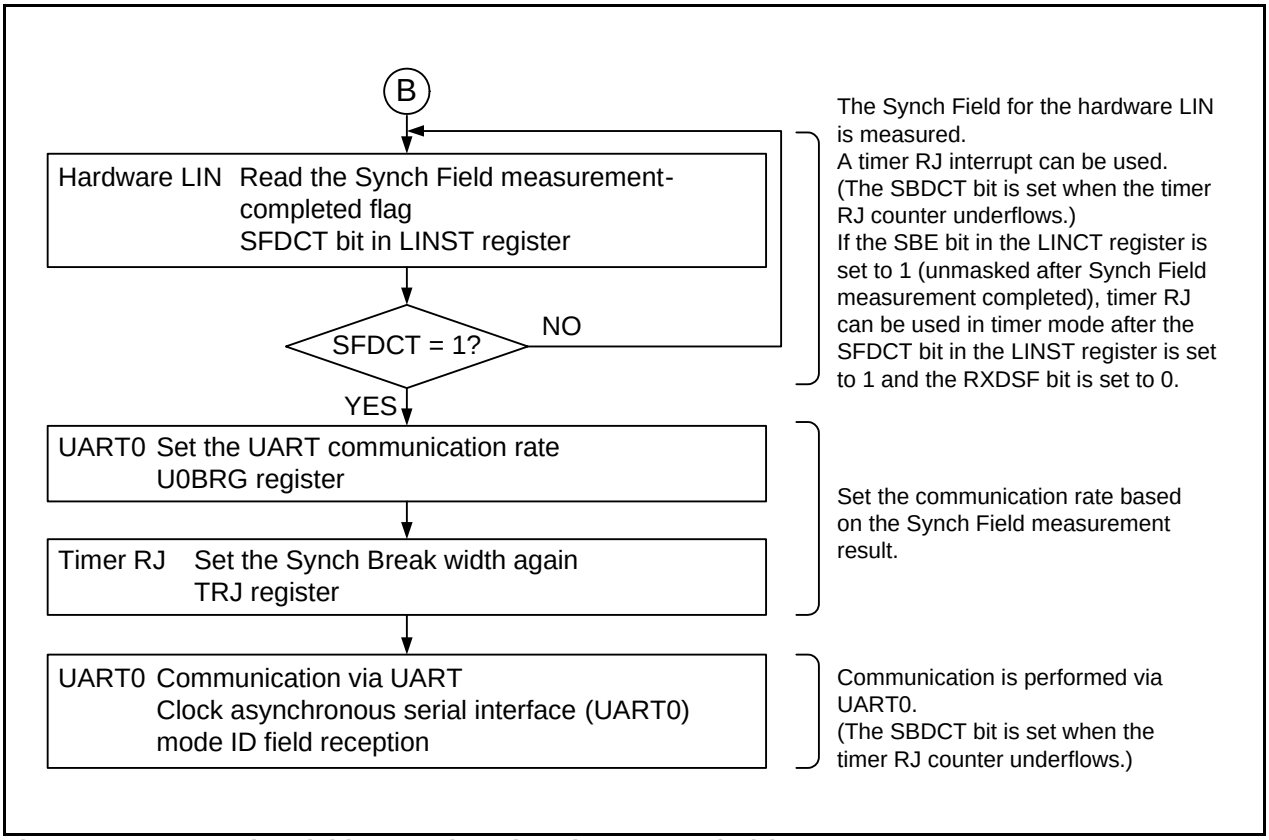


Figure 23.8 Header Field Reception Flowchart Example (3)

23.4.3 Bus Collision Detection Function

The bus collision detection function can be used if UART0 is enabled for transmission (TE bit in the U0C1 register = 1 (transmission enabled)). To detect a bus collision during Synch Break transmission, set the BCE bit in the LINCR2 register to 1 (bus collision detection enabled).
Figures 23.9 shows an Operation Example when Bus Collision is Detected.

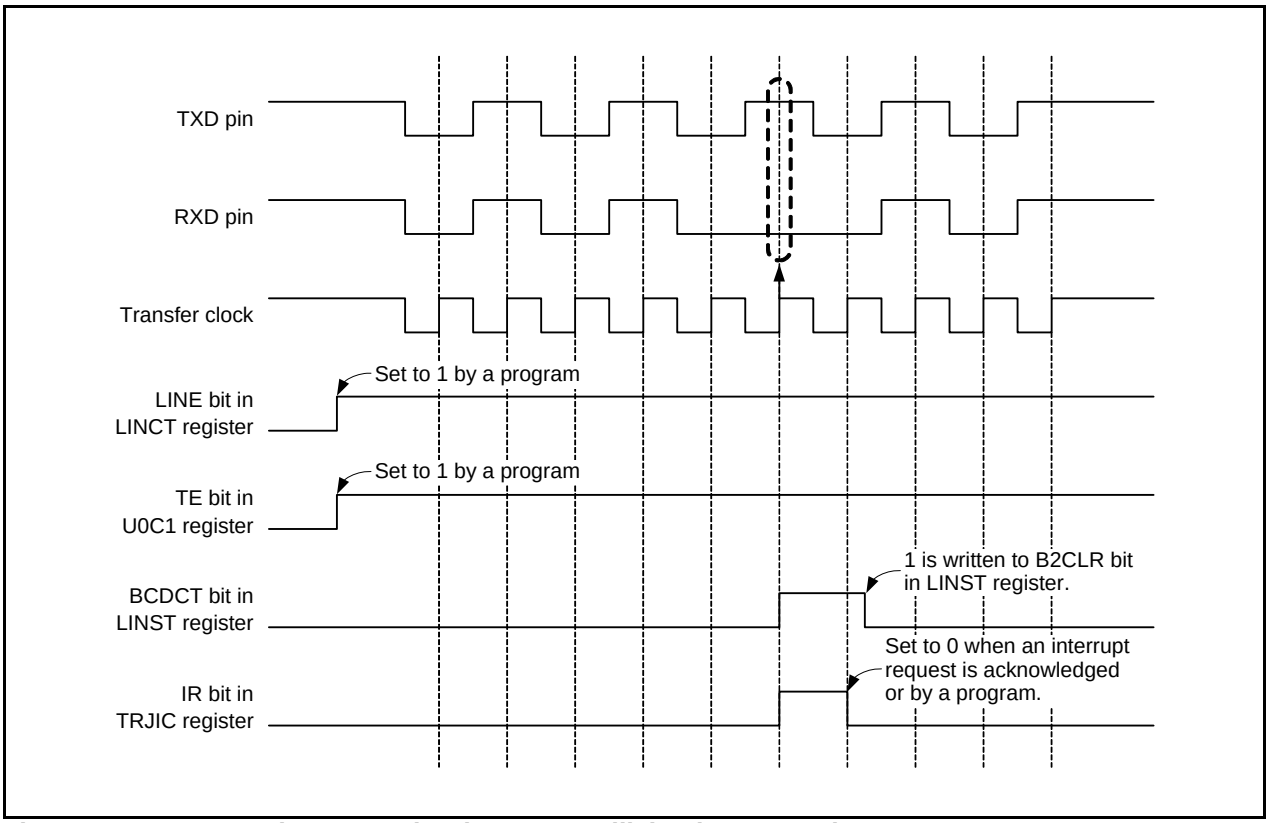


Figure 23.9 Operation Example when Bus Collision is Detected

23.4.4 Hardware LIN Completion Processing

Figure 23.10 shows an Example of Hardware LIN Communication Completion Flowchart.
Use the following timing for hardware LIN completion processing:

- If the hardware bus collision detection function is used
  Perform hardware LIN completion processing after checksum transmission completes.
- If the bus collision detection function is not used
  Perform hardware LIN completion processing after header field transmission and reception complete.

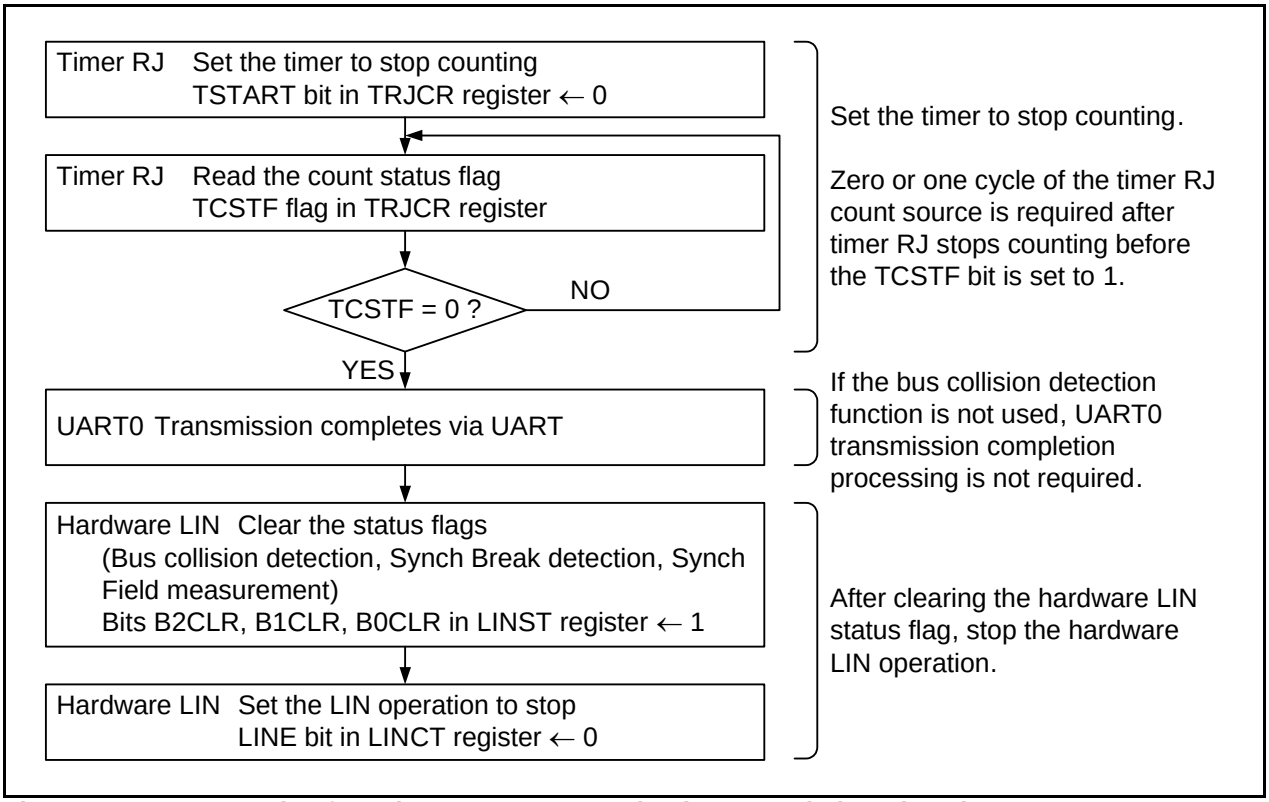


Figure 23.10 Example of Hardware LIN Communication Completion Flowchart

23.5 Interrupt Requests

There are four interrupt requests generated by the hardware LIN: Synch Break detection, Completion of Synch Break generation, Completion of Synch Field measurement, and bus collision detection. These interrupts are shared with timer RJ.
Table 23.3 lists the Hardware LIN Interrupt Requests.

Table 23.3 Hardware LIN Interrupt Requests

Interrupt Request	Status Flag	Interrupt Source
Synch Break detection	SBDCT	Generated when timer RJ underflows after the low level duration for the RXD input is measured, or when a low level is input for a duration longer than the Synch Break period during communication.
Completion of Synch Break generation		Generated when a low level output to TXD for the duration set by timer RJ is completed.
Completion of Synch Field measurement	SFDCT	Generated when measurement for 6 bits of the Synch Field by timer RJ is completed.
Bus collision detection	BCDCT	Generated when the RXD input and TXD output values are different at the data latch timing while UART0 is enabled for transmission.

23.6 Notes on Hardware LIN

For the time-out processing of the header and response fields, use another timer to measure the duration of time with a Synch Break detection interrupt as the starting point.

24. CAN Module

This MCU implements a channel (CAN_0) of CAN (Controller Area Network) module that comply with the ISO11898-1 Specifications.

24.1 Overview

The CAN module transmits and receives both formats of messages, namely the standard identifier (11 bits) (identifier hereafter referred to as ID) and extended ID (29 bits).
Tables 24.1 and 24.2 list the CAN Module Specifications and Figure 24.1 shows the CAN Module Block Diagram.
Connect the CAN bus transceiver externally.

Table 24.1 CAN Module Specifications (1)

Item	Specifications
Protocol	ISO11898-1 compliant
Bit rate	Up to 1 Mbps
Message boxes	16 mailboxes: Two selectable mailbox modes: • Normal mailbox mode All 16 mailboxes can be configured for transmission or reception. • FIFO mailbox mode: 8 mailboxes can be configured for transmission or reception. The remaining mailboxes can be configured as 4-stage FIFO for transmission and 4-stage FIFO for reception.
Reception	• Data frames and remote frames can be received • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable overwrite mode (message overwritten) or overrun mode (message discarded) • The reception complete interrupt can be individually enabled or disabled for each mailbox
Acceptance filtering	• 4 acceptance masks: one mask every 4 mailboxes • The mask can be individually enabled or disabled for each mailbox.
Transmission	• Data frames and remote frames can be transmitted • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable ID priority transmit mode or mailbox number priority transmit mode • Transmission request can be aborted (The completion of abort can be confirmed with a flag) • The transmission complete interrupt can be individually enabled or disabled for each mailbox
Mode transition for bus-off recovery	Mode transition for the recovery from the bus-off state can be selected: • ISO11898-1 compliant • Automatic entry to CAN halt mode at bus-off entry • Automatic entry to CAN halt mode at bus-off end • Entry to CAN halt mode by a program • Transition to the error-active state by a program
Error status monitoring	• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored • Transition to error states can be detected (error-warning, error-passive, bus-off entry, and bus-off recovery) • The error counters can be read
Time stamp function	• Time stamp function using a 16-bit counter • The reference clock can be selected from either 1-, 2-, 4- or 8-bit time periods.

Table 24.2 CAN Module Specifications (2)

Item	Specifications
Interrupt sources	6 types: • Reception complete • Transmission complete • Receive FIFO • Transmit FIFO • Error • Wake-up
CAN sleep mode	Current consumption can be reduced by stopping the CAN clock.
Software support units	3 software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support
CAN clock source	CAN clock or CPU clock can be selected
Test mode	3 test modes available for user evaluation: • Listen-only mode • Self-test mode 0 (external loop back) • Self-test mode 1 (internal loop back)

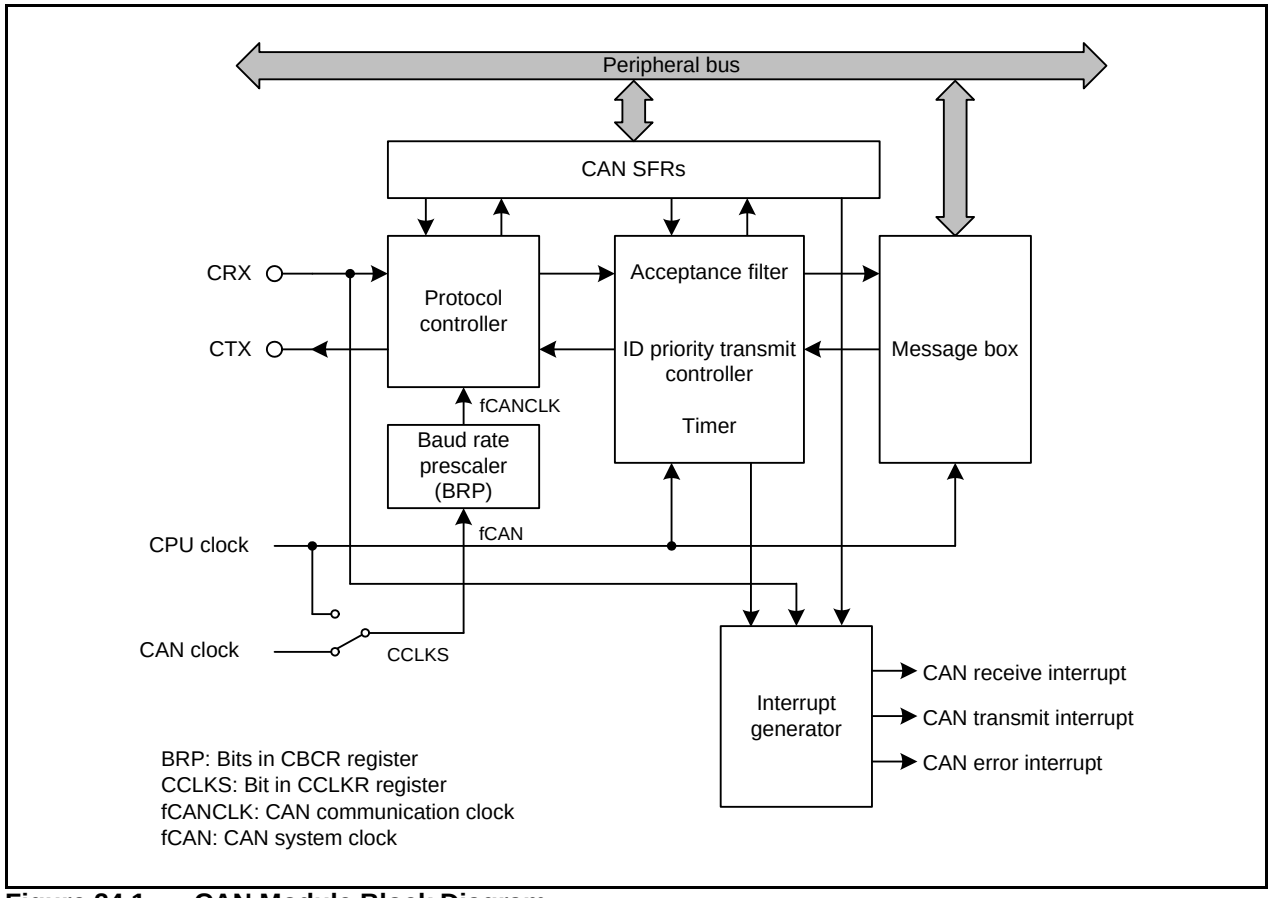


Figure 24.1 CAN Module Block Diagram

- CRX/CTX: CAN input/output pins
- CAN clock: Set the frequency of the clock to equal to or slower than the frequency of the CPU clock.
- Protocol controller: Handles CAN protocol processing such as bus arbitration, bit timing at transmission and reception, stuffing, and error handling, etc.
- Message box: Consists of 16 mailboxes which can be configured as either transmit or receive mailboxes. Each mailbox has an individual ID, data length code, a data field (8 bytes), and a time stamp.
- Acceptance filter: Performs filtering of received messages. Registers CMKR0 to CMKR3 are used for the filtering process.
- Timer: Used for the time stamp function. The timer value when storing a message into the mailbox is written as the time stamp value.
- Wake-up function: Generates a CAN wake-up interrupt request when a message is detected on the CAN bus.
- Interrupt generator: Generates the following three types of interrupts. Interrupt sources for each interrupt can be determined using the CANISR register.
  - CAN receive interrupt
    (shared with CAN reception complete interrupt and CAN receive FIFO interrupt)
  - CAN transmit interrupt
    (shared with CAN transmission complete interrupt and CAN transmit FIFO interrupt)
  - CAN error interrupt
    (shared with CAN error interrupt and CAN wake-up interrupt)
- CAN SFRs: CAN-associated registers. Refer to **24.2 Registers** for details.

24.2 Registers

Tables 24.3 and 24.4 list the CAN Module Register Configuration.

Table 24.3 CAN Module Register Configuration (1)

Register Name	Symbol	After Reset	Address	Access Size
CAN_0 Mailbox 0 to CAN_0 Mailbox 15	CMB0_0 to CMB15_0	(XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXh) × 16	06E00h to 06EF0h	8 or 16
CAN_0 Mask Register 0	CMKR0_0	XXh	06F10h	8 or 16
		XXh	06F11h	
		XXh	06F12h	
		XXh	06F13h	
CAN_0 Mask Register 1	CMKR1_0	XXh	06F14h	8 or 16
		XXh	06F15h	
		XXh	06F16h	
		XXh	06F17h	
CAN_0 Mask Register 2	CMKR2_0	XXh	06F18h	8 or 16
		XXh	06F19h	
		XXh	06F1Ah	
		XXh	06F1Bh	
CAN_0 Mask Register 3	CMKR3_0	XXh	06F1Ch	8 or 16
		XXh	06F1Dh	
		XXh	06F1Eh	
		XXh	06F1Fh	
CAN_0 FIFO Received ID Compare Register 0	CFIDCR0_0	XXh	06F20h	8 or 16
		XXh	06F21h	
		XXh	06F22h	
		XXh	06F23h	
CAN_0 FIFO Received ID Compare Register 1	CFIDCR1_0	XXh	06F24h	8 or 16
		XXh	06F25h	
		XXh	06F26h	
		XXh	06F27h	
CAN_0 Mask Invalid Register	CMKIVLR_0	XXh	06F2Ah	8 or 16
		XXh	06F2Bh	
CAN_0 Mailbox Interrupt Enable Register	CMIER_0	XXh	06F2Eh	8 or 16
		XXh	06F2Fh	
CAN_0 Message Control Register 0	CMCTL0_0	00h	06F30h	8
CAN_0 Message Control Register 1	CMCTL1_0	00h	06F31h	8
CAN_0 Message Control Register 2	CMCTL2_0	00h	06F32h	8
CAN_0 Message Control Register 3	CMCTL3_0	00h	06F33h	8
CAN_0 Message Control Register 4	CMCTL4_0	00h	06F34h	8
CAN_0 Message Control Register 5	CMCTL5_0	00h	06F35h	8
CAN_0 Message Control Register 6	CMCTL6_0	00h	06F36h	8
CAN_0 Message Control Register 7	CMCTL7_0	00h	06F37h	8
CAN_0 Message Control Register 8	CMCTL8_0	00h	06F38h	8
CAN_0 Message Control Register 9	CMCTL9_0	00h	06F39h	8
CAN_0 Message Control Register 10	CMCTL10_0	00h	06F3Ah	8
CAN_0 Message Control Register 11	CMCTL11_0	00h	06F3Bh	8
CAN_0 Message Control Register 12	CMCTL12_0	00h	06F3Ch	8
CAN_0 Message Control Register 13	CMCTL13_0	00h	06F3Dh	8
CAN_0 Message Control Register 14	CMCTL14_0	00h	06F3Eh	8
CAN_0 Message Control Register 15	CMCTL15_0	00h	06F3Fh	8

Table 24.4 CAN Module Register Configuration (2)

Register Name	Symbol	After Reset	Address	Access Size
CAN_0 Control Register	CCTLR_0	00000101b	06F40h	8 or 16
		00h	06F41h	
CAN_0 Status Register	CSTR_0	00000101b	06F42h	8 or 16
		00h	06F43h	
CAN_0 Bit Configuration Register	CBCR_0	00h	06F44h	8 or 16
		00h	06F45h	
		00h	06F46h	
CAN_0 Clock Select Register	CCLKR_0	00h	06F47h	8
CAN_0 Receive FIFO Control Register	CRFCR_0	10000000b	06F48h	8
CAN_0 Receive FIFO Pointer Control Register	CRFPCR_0	XXh	06F49h	8
CAN_0 Transmit FIFO Control Register	CTFCR_0	10000000b	06F4Ah	8
CAN_0 Transmit FIFO Pointer Control Register	CTFPCR_0	XXh	06F4Bh	8
CAN_0 Error Interrupt Enable Register	CEIER_0	00h	06F4Ch	8
CAN_0 Error Interrupt Factor Judge Register	CEIFR_0	00h	06F4Dh	8
CAN_0 Receive Error Count Register	CRECR_0	00h	06F4Eh	8
CAN_0 Transmit Error Count Register	CTECR_0	00h	06F4Fh	8
CAN_0 Error Code Store Register	CECSR_0	00h	06F50h	8
CAN_0 Channel Search Support Register	CCSSR_0	XXh	06F51h	8
CAN_0 Mailbox Search Status Register	CMSSR_0	10000000b	06F52h	8
CAN_0 Mailbox Search Mode Register	CMSMR_0	00h	06F53h	8
CAN_0 Time Stamp Register	CTSR_0	0000h	06F54h	16
CAN_0 Acceptance Filter Support Register	CAFSR_0	XXh	06F56h	8 or 16
		XXh	06F57h	
CAN_0 Test Control Register	CTCR_0	00h	06F58h	8
CAN_0 Interrupt Status Register	CANISR_0	00h	06F7Eh	8
CAN_0 Interrupt Control Register	CANIE_0	00h	06F7Fh	8

24.2.1 CAN Mailbox (CMBj) (j = 0 to 15)

Table 24.5 lists the CAN Mailbox Memory Mapping and Table 24.6 lists the CAN Data Frame Structure. The value after reset of CAN mailbox is undefined.

Address 06E00h (CMB0_0), 06E10h (CMB1_0), 06E20h (CMB2_0), 06E30h (CMB3_0), 06E40h (CMB4_0), 06E50h (CMB5_0), 06E60h (CMB6_0), 06E70h (CMB7_0), 06E80h (CMB8_0), 06E90h (CMB9_0), 06EA0h (CMB10_0), 06EB0h (CMB11_0), 06EC0h (CMB12_0), 06ED0h (CMB13_0), 06EE0h (CMB14_0), 06EF0h (CMB15_0)

Table 24.5 CAN Mailbox Memory Mapping

Address	Message Content
CAN_0	Memory Mapping
06E00h + j × 16 + 0	EID7 to EID0
06E00h + j × 16 + 1	EID15 to EID8
06E00h + j × 16 + 2	SID5 to SID0, EID17, EID16
06E00h + j × 16 + 3	IDE, RTR, SID10 to SID6
06E00h + j × 16 + 4	—
06E00h + j × 16 + 5	Data length code (DLC)
06E00h + j × 16 + 6	Data byte 0
06E00h + j × 16 + 7 : : : 06E00h + j × 16 + 13	Data byte 1 : : : Data byte 7
06E00h + j × 16 + 14	Time stamp lower byte
06E00h + j × 16 + 15	Time stamp upper byte

j: Mailbox number (j = 0 to 15)

Table 24.6 CAN Data Frame Structure

SID10 to SID6	SID5 to SID0	EID17 to EID16	EID15 to EID8	EID7 to EID0	DLC3 to DLC0	DATA0	DATA1	· · · · ·	DATA7

Address 06E00h + j × 16 + 0 to 06E00h + j × 16 + 3 (CMB0_0 to CMB15_0) (j = 0 to 15)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
After Reset	X	X	X	X	X	X	X	X

Bit	b23	b22	b21	b20	b19	b18	b17	b16
Symbol	SID5	SID4	SID3	SID2	SID1	SID0	EID17	EID16
After Reset	X	X	X	X	X	X	X	X

Bit	b31	b30	b29	b28	b27	b26	b25	b24
Symbol	IDE	RTR	—	SID10	SID9	SID8	SID7	SID6
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b17 to b0	EID17 to EID0	Extended ID bits (1)	0: Corresponding EID bit is 0 1: Corresponding EID bit is 1	R/W
b28 to b18	SID10 to SID0	Standard ID bits	0: Corresponding SID bit is 0 1: Corresponding SID bit is 1	R/W
b29	—	Reserved	Set to 0.	R/W
b30	RTR	Remote frame request bit	0: Data frame 1: Remote frame	R/W
b31	IDE	ID extension bit (2)	0: Standard ID 1: Extended ID	R/W

Notes:
1. If the mailbox has received a standard ID message, the value of the EID bit in the mailbox is undefined.
2. The IDE bit is enabled when bits IDFM1 and IDFM0 in the CCTLR register are 10b (mixed ID mode). When bits IDFM1 and IDFM0 are not 10b, write 0 to these bits.

Address 06E00h + j × 16 + 4 to 06E00h + j × 16 + 5 (CMB0_0 to CMB15_0) (j = 0 to 15)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	DLC3	DLC2	DLC1	DLC0
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b7 to b0	—	Reserved	Set to 0.	R/W
b11 to b8	DLC3 to DLC0	Data length code (1)	0h to Fh	R/W
b15 to b12	—	Reserved	Set to 0.	R/W

Note:
1. If the mailbox has received a message with n bytes less than 8 bytes, the values of DATAn to DATA7 in the mailbox are undefined.

Address 06E00h + j × 16 + 6 to 06E00h + j × 16 + 13 (CMB0_0 to CMB15_0) (j = 0 to 15)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DATA07	DATA06	DATA05	DATA04	DATA03	DATA02	DATA01	DATA00
After Reset	X	X	X	X	X	X	X	X

:

:

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DATA77	DATA76	DATA75	DATA74	DATA73	DATA72	DATA71	DATA70
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b7 to b0	DATAi7 to DATAi0 (i = 0 to 7)	Data Bytes 0 to 7 (1, 2)	00h to FFh	R/W

Notes:
1. If the mailbox has received a message with n bytes less than 8 bytes, the values of DATAn to DATA7 in the mailbox are undefined.
2. If the mailbox has received a remote frame, the previous values of DATA0 to DATA7 in the mailbox are retained.

Address 06E00h + j × 16 + 14 to 06E00h + j × 16 + 15 (CMB0_0 to CMB15_0) (j = 0 to 15)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TSL7	TSL6	TSL5	TSL4	TSL3	TSL2	TSL1	TSL0
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	TSH7	TSH6	TSH5	TSH4	TSH3	TSH2	TSH1	TSH0
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b7 to b0	TSL7 to TSL0	Time stamp lower byte	00h to FFh	R/W
b15 to b8	TSH7 to TSH0	Time stamp higher byte		R/W

Write to the CMBj register (j = 0 to 15) only when the associated CMCTLj register is 00h and the corresponding mailbox is not processing an abort request.
Refer to **24.6 Acceptance Filtering and Masking Function** for detailed addresses of the CMBj register.
The previous value of each mailbox is retained unless a new message is received.

Bits EID0 to EID17 (Extended ID bits)

Bits EID0 to EID17 set the extended ID of data frames and remote frames. These bits are used to transmit or receive extended ID messages.

Bits SID0 to SID10 (Standard ID bits)

Bits SID0 to SID10 set the standard ID of data frames and remote frames. These bits are used to transmit or receive both standard ID and extended ID messages.

RTR Bit (Remote frame request bit)

The RTR bit sets the frame format of data frames or remote frames.
This bit specifies the following operation:

- Receive mailbox receives only frames with the format specified by the RTR bit.
- Transmit mailbox transmits according to the frame format specified by the RTR bit.
- Receive FIFO mailbox receives the data frame, remote frame, or both frames specified by the RTR bit in registers CFIDCR0 and CFIDCR1.
- Transmit FIFO mailbox transmits the data frame or remote frame specified by the RTR bit in the relevant transmitting message.

IDE Bit (ID extension bit)

The IDE bit sets the ID format of standard ID or extended ID.
The IDE bit is enabled when bits IDFM1 and IDFM0 in the CCTLR register are 10b (mixed ID mode).
When bits IDFM1 and IDFM0 are 10b, the IDE bit specifies the following operation.

- Receive mailbox receives only the ID format specified by the IDE bit.
- Transmit mailbox transmits according to the ID format specified by the IDE bit.
- Receive FIFO mailbox receives messages with the standard ID, extended ID, or both IDs specified by the IDE bit in registers CFIDCR0 and CFIDCR1.
- Transmit FIFO mailbox transmits messages with the standard ID or extended ID specified by the IDE bit in the relevant transmitting message.

Bits DLC0 to DLC3 (Data length code)

Bits DLC0 to DLC3 are used to set the number of data bytes to be transmitted in a data frame. When data is requested using a remote frame, the number of data bytes to be requested is set.
When a data frame is received, the number of received data bytes is stored. When a remote frame is received, the number of requested data bytes is stored.
Table 24.7 lists the Data Length Corresponding DLC.

Table 24.7 Data Length Corresponding DLC

DLC3	DLC2	DLC1	DLC0	Data Length
0	0	0	0	0 byte
0	0	0	1	1 byte
0	0	1	0	2 bytes
0	0	1	1	3 bytes
0	1	0	0	4 bytes
0	1	0	1	5 bytes
0	1	1	0	6 bytes
0	1	1	1	7 bytes
1	-	-	-	8 bytes

-: Any value

Bits DATA0 to DATA7 (Data bytes)

Bits DATA0 to DATA7 store the transmitted or received CAN message data. Transmission or reception starts from DATA0. The bit order on the CAN bus is MSB first, and transmission or reception starts from bit 7.

Bits TSL0 to TSL7 (Time stamp lower byte)
Bits TSH0 to TSH7 (Time stamp higher byte)

Bits TSL0 to TSL7 and bits TSH0 to TSH7 store the counter value of the time stamp when received messages are stored in the mailbox.

24.2.2 CAN Mask Register k (CMKRk) (k = 0 to 3)

Address 06F10h (CMKR0_0), 06F14h (CMKR1_0), 06F18h (CMKR2_0), 06F1Ch (CMKR3_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
After Reset	X	X	X	X	X	X	X	X

Bit	b23	b22	b21	b20	b19	b18	b17	b16
Symbol	SID5	SID4	SID3	SID2	SID1	SID0	EID17	EID16
After Reset	X	X	X	X	X	X	X	X

Bit	b31	b30	b29	b28	b27	b26	b25	b24
Symbol	—	—	—	SID10	SID9	SID8	SID7	SID6
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b17 to b0	EID17 to EID0	Extended ID bits	0: Corresponding EID bit is not compared 1: Corresponding EID bit is compared	R/W
b28 to b18	SID10 to SID0	Standard ID bits	0: Corresponding SID bit is not compared 1: Corresponding SID bit is compared	R/W
b31 to b29	—	Reserved	Set to 0.	R/W

Write to registers CMKR0 to CMKR3 in CAN reset mode or CAN halt mode.
Refer to **24.6 Acceptance Filtering and Masking Function** about the masking function in FIFO mailbox mode.

Bits EID0 to EID17 (Extended ID bits)

Bits EID0 to EID17 are filter mask bits corresponding to the CAN extended ID bits. These bits are used to receive extended ID messages.
When these bits are 0, the corresponding EID bit is not compared for the received ID and the mailbox ID.
When these bits are 1, the corresponding EID bit is compared for the received ID and the mailbox ID.

Bits SID0 to SID10 (Standard ID bits)

Bits SID0 to SID10 are filter mask bits corresponding to the CAN standard ID bits. These bits are used to receive both standard ID and extended ID messages.
When these bits are 0, the corresponding SID bit is not compared for the received ID and the mailbox ID.
When these bits are 1, the corresponding SID bit is compared for the received ID and the mailbox ID.

24.2.3 CAN FIFO Received ID Compare Register n (CFIDCRn) (n = 0 or 1)

Address 06F20h (CFIDCR0_0), 06F24h (CFIDCR1_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
After Reset	X	X	X	X	X	X	X	X

Bit	b23	b22	b21	b20	b19	b18	b17	b16
Symbol	SID5	SID4	SID3	SID2	SID1	SID0	EID17	EID16
After Reset	X	X	X	X	X	X	X	X

Bit	b31	b30	b29	b28	b27	b26	b25	b24
Symbol	IDE	RTR	—	SID10	SID9	SID8	SID7	SID6
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b17 to b0	EID17 to EID0	Extended ID bits	0: Corresponding EID bit is 0 1: Corresponding EID bit is 1	R/W
b28 to b18	SID10 to SID0	Standard ID bits	0: Corresponding SID bit is 0 1: Corresponding SID bit is 1	R/W
b29	—	Reserved	Set to 0.	R/W
b30	RTR	Remote frame request bit	0: Data frame 1: Remote frame	R/W
b31	IDE	ID extension bit (1)	0: Standard ID 1: Extended ID	R/W

Note:
1. The IDE bit is enabled when bits IDFM1 and IDFM0 in the CCTLR register are 10b (mixed ID mode). When bits IDFM1 and When bits IDFM1 and IDFM0 are 00b (standard ID mode) or 01b (extended ID mode), write 0 to the IDE bit.

Write to registers CFIDCR0 and CFIDCR1 in CAN reset mode or CAN halt mode.
Registers CFIDCR0 and CFIDCR1 are enabled when the MBM bit in the CCTLR register is set to 1 (FIFO mailbox mode). Bits EID0 to EID17, SID0 to SID10, RTR, and IDE in registers CMB12 to CMB15 are disabled.
Refer to **24.6 Acceptance Filtering and Masking Function** about the usage of registers CFIDCR0 and CFIDCR1.

Bits EID0 to EID17 (Extended ID bits)

Bits EID0 to EID17 set the extended ID of data frames and remote frames. These bits are used to receive extended ID messages.

Bits SID0 to SID10 (Standard ID bits)

Bits SID0 to SID10 set the standard ID of data frames and remote frames. These bits are used to receive both standard ID and extended ID messages.

RTR Bit (Remote frame request bit)

The RTR bit sets the specified frame format of data frames or remote frames.
This bit specifies the following operation:

- When both RTR bits in registers CFIDCR0 and CFIDCR1 are set to 0, only data frames can be received.
- When both RTR bits in registers CFIDCR0 and CFIDCR1 are set to 1, only remote frames can be received.
- When the RTR bits in registers CFIDCR0 and CFIDCR1 are set to 0 or 1 individually, both data frames and remote frames can be received.

IDE Bit (ID extension bit)

The IDE bit sets the ID format of standard ID or extended ID.
This bit is enabled when bits IDFM1 and IDFM0 in the CCTLR register are 10b (mixed ID mode).
When bits IDFM1 and IDFM0 are 10b, the IDE bit specifies the following operation:

- When both IDE bits in registers CFIDCR0 and CFIDCR1 are set to 0, only standard ID frames can be received.
- When both IDE bits in registers CFIDCR0 and CFIDCR1 are set to 1, only extended ID frames can be received.
- When the IDE bits in registers CFIDCR0 and CFIDCR1 are set to 0 or 1 individually, both standard ID and extended ID frames can be received.

24.2.4 CAN Mask Invalid Register (CMKIVLR)

Address 06F2Ah (CMKIVLR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Mode	Bit Name	Function	R/W
b15 to b0	Normal mailbox mode	Mask invalid bit	0: Mask valid 1: Mask invalid	R/W

b7 to b0	FIFO mailbox mode	Mask invalid bit	0: Mask valid 1: Mask invalid	R/W
b15 to b8		Reserved	Set to 0.	R/W

Write to the CMKIVLR register in CAN reset mode or CAN halt mode.
Each bit corresponds to the mailbox with the same number. When a bit is 1, the acceptance mask for the mailbox corresponding to the bit number is disabled. In this case, a receiving message is stored into the mailbox only if its ID matches bits SID0 to SID10 and EID0 to EID17 in the CMBj register (j = 0 to 15).

24.2.5 CAN Mailbox Interrupt Enable Register (CMIER)

Address 06F2Eh (CMIER_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Mode	Bit Name	Function	R/W
b15 to b0	Normal mailbox mode	Interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	R/W

b7 to b0	FIFO mailbox mode	Interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	R/W
b8		Transmit FIFO interrupt enable bit		R/W
b9		Transmit FIFO interrupt generation timing control bit	Transmit FIFO interrupt request is generated 0: Every time transmission is completed 1: When transmit FIFO becomes empty due to completion of transmission	R/W
b11 to b10		Reserved	Set to 0.	R/W
b12		Receive FIFO interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	R/W
b13		Receive FIFO interrupt generation timing control bit	Receive FIFO interrupt request is generated 0: Every time reception is completed 1: When receive FIFO becomes buffer warning by completion of reception (1)	R/W
b15 to b14		Reserved	Set to 0.	R/W

Note:
1. No interrupt request is generated when the receive FIFO changes state to buffer warning from full.

Write to the CMIER register only when the associated CMCTLj register (j = 0 to 15) is 00h and the corresponding mailbox is not processing a transmission or reception abort request.
In FIFO mailbox mode, change the bits in the CMIER register for the associated FIFO only when:
- The TFE bit in the CTFCR register is 0 (transmit FIFO disabled) and the TFEST bit is 1 (no unsent messages in transmit FIFO), and
- The RFE bit in the CRFCR register is 0 (receive FIFO disabled) and the RFEST bit is 1 (no unread messages in receive FIFO).

Interrupts can be enabled individually for each mailbox.
In normal mailbox mode (bits 0 to 15) and in FIFO mailbox mode (bits 0 to 7), each bit corresponds to the mailbox with the same number. These bits enable or disable transmission/reception complete interrupts for the corresponding mailboxes.
In FIFO mailbox mode, bits 8, 9, 12, and 13 specify whether transmit/receive FIFO interrupts are enabled/disabled and timing when interrupt requests are generated.
Buffer warning indicates a state in which the third unread message is stored in the receive FIFO.

24.2.6 CAN Message Control Register j (CMCTLj) (j = 0 to 15)

Address 06F30h (CMCTL0_0), 06F31h (CMCTL1_0), 06F32h (CMCTL2_0), 06F33h (CMCTL3_0), 06F34h (CMCTL4_0), 06F35h (CMCTL5_0), 06F36h (CMCTL6_0), 06F37h (CMCTL7_0), 06F38h (CMCTL8_0), 06F39h (CMCTL9_0), 06F3Ah (CMCTL10_0), 06F3Bh (CMCTL11_0), 06F3Ch (CMCTL12_0), 06F3Dh (CMCTL13_0), 06F3Eh (CMCTL14_0), 06F3Fh (CMCTL15_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRMREQ	RECREQ	—	ONESHOT	—	MSGLOST TRMABT	INVALDATA TRMACTIVE	NEWDATA SENTDATA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	NEWDATA	Reception complete flag (1, 2)	(Receiver mailbox setting enabled) 0: No data has been received or 0 is written to the NEWDATA bit 1: A new message is being stored or has been stored to the mailbox	R/W
	SENTDATA	Transmission complete flag (1, 2)	(Transmitter mailbox setting enabled) 0: Transmission is not completed (pending) 1: Transmission is completed (success)	R/W
b1	INVALDATA	Reception-in-progress status flag	(Receiver mailbox setting enabled) 0: Message valid 1: Message being updated	R
	TRMACTIVE	Transmission-in-progress status flag	(Transmitter mailbox setting enabled) 0: Transmission is pending or transmission is not requested 1: From acceptance of transmission request to completion of transmission, or error/arbitration lost	R
b2	MSGLOST	Message lost flag (1, 2)	(Receiver mailbox setting enabled) 0: Message is not overwritten or overrun 1: Message is overwritten or overrun	R/W
	TRMABT	Transmission abort complete flag (1, 2)	(Transmitter mailbox setting enabled) 0: Transmission has started, transmission abort failed because transmission is completed, or transmission abort is not requested 1: Transmission abort is completed	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	ONESHOT	One-shot enable bit (3)	0: One-shot reception or one-shot transmission disabled 1: One-shot reception or one-shot transmission enabled	R/W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	RECREQ	Receive mailbox set bit (2, 4, 5)	0: Not configured for reception 1: Configured for reception	R/W
b7	TRMREQ	Transmit mailbox set bit (2, 4)	0: Not configured for transmission 1: Configured for transmission	R/W

Notes:
1. Write 0 only. Writing 1 has no effect.
2. When writing 0 to bits NEWDATA, SENTDATA, MSGLOST, TRMABT, RECREQ, and TRMREQ by a program, use the MOV instruction to ensure that only the specified bit is set to 0 and the other bits are set to 1.
3. To enter one-shot receive mode, write 1 to the ONESHOT bit at the same time as setting the RECREQ bit to 1. To exit one-shot receive mode, write 0 to the ONESHOT bit after writing 0 to the RECREQ bit and confirming it has been set to 0.
   To enter one-shot transmit mode, write 1 to the ONESHOT bit at the same time as setting the TRMREQ bit to 1. To exit one-shot transmit mode, write 0 to the ONESHOT bit after the message has been transmitted or aborted.
4. Do not set both the RECREQ and TRMREQ bits to 1.
5. When setting the RECREQ bit to 0, set bits MSGLOST, NEWDATA, and RECREQ to 0 simultaneously.

   Write to the CMCTLj register in CAN operation mode or CAN halt mode.
   Do not use registers CMCTL8 to CMCTL15 in FIFO mailbox mode.

NEWDATA Bit (Reception complete flag)

The NEWDATA bit is set to 1 when a new message is being stored or has been stored to the mailbox. The timing for setting this bit to 1 is simultaneous with the INVALDATA bit.
The NEWDATA bit is set to 0 by writing 0 by a program.
This bit is not set to 0 by writing 0 by a program while the related INVALDATA bit is 1.

SENTDATA Bit (Transmission complete flag)

The SENTDATA bit is set to 1 when data transmission from the corresponding mailbox is completed.
This bit is set to 0 by writing 0 by a program.
To set the SENTDATA bit to 0, first set the TRMREQ bit to 0.
Bits SENTDATA and TRMREQ cannot be set to 0 simultaneously.
To transmit a new message from the corresponding mailbox, set the SENTDATA bit to 0.

INVALDATA Bit (Reception-in-progress status flag)

After the completion of a message reception, the INVALDATA bit is set to 1 while the received message is being updated into the corresponding mailbox.
This bit is set to 0 immediately after the message has been stored. If the mailbox is read while this bit is 1, the data is undefined.

TRMACTIVE Bit (Transmission-in-progress status flag)

The TRMACTIVE bit is set to 1 when the corresponding mailbox of the CAN module begins transmitting a message.
This bit is set to 0 when the CAN module has lost CAN bus arbitration, a CAN bus error occurs, or data transmission is completed.

MSGLOST Bit (Message lost flag)

The MSGLOST bit is set to 1 when the mailbox is overwritten or overrun by a new received message while the NEWDATA bit is 1. The MSGLOST bit is set to 1 at the end of the 6th bit of EOF.
This bit is set to 0 by writing 0 by a program.
In both overwrite and overrun modes, this bit is not set to 0 by writing 0 by a program during five cycles of fCAN (CAN system clock) following the 6th bit of EOF.

TRMABT Bit (Transmission abort complete flag)

The TRMABT bit is set to 1 in the following cases:
- Following a transmission abort request, when the transmission abort is completed before starting transmission.
- Following a transmission abort request, when the CAN module detects CAN bus arbitration lost or a CAN bus error.
- In one-shot transmission mode (RECREQ bit = 0, TRMREQ bit = 1, and ONESHOT bit = 1), when the CAN module detects CAN bus arbitration lost or a CAN bus error.

The TRMABT bit is not set to 1 when data transmission is completed. In this case, the SENTDATA bit is set to 1.
The TRMABT bit is set to 0 by writing 0 by a program.

ONESHOT Bit (One-shot enable bit)

The ONESHOT bit can be used in the following two ways, receive mode and transmit mode:

(1) One-Shot Receive Mode

When the ONESHOT bit is set to 1 in receive mode (RECREQ bit = 1 and TRMREQ bit = 0), the mailbox receives a message only one time. The mailbox does not behave as a receive mailbox after having received a message one time. The behavior of bits NEWDATA and INVALDATA is the same as in normal reception mode. In one-shot receive mode, the MSGLOST bit is not set to 1.

To set the ONESHOT bit to 0, first write 0 to the RECREQ bit and ensure that it has been set to 0.

(2) One-Shot Transmission Mode

When the ONESHOT bit is set to 1 in transmit mode (RECREQ bit = 0 and TRMREQ bit = 1), the CAN module transmits a message only one time. The CAN module does not transmit the message again if a CAN bus error or CAN bus arbitration lost occurs. When transmission is completed, the SENTDATA bit is set to 1. If transmission is not completed due to a CAN bus error or CAN bus arbitration lost, the TRMABT bit is set to 1.

Set the ONESHOT bit to 0 after the SENTDATA or TRMABT bit is set to 1.

RECREQ Bit (Receive mailbox set bit)

The RECREQ bit selects the receive modes shown in Table 24.13.

When this bit is set to 1, the corresponding mailbox is configured for reception of a data frame or a remote frame.

When this bit is set to 0, the corresponding mailbox is not configured for reception of a data frame or a remote frame.

Due to HW protection, the RECREQ bit cannot be set to 0 by writing 0 by a program during the following period

HW protection is started

• from the acceptance filter procedure (the beginning of CRC field)

HW protection is released

• for the mailbox that is specified to receive the incoming message, after the received data is stored into the mailbox or a CAN bus error occurs (i.e. a maximum period of HW protection is from the beginning of the CRC field to the end of the 7th bit of EOF).

• for the other mailboxes, after the acceptance filter procedure.

• if no mailbox is specified to receive the message, after the acceptance filter procedure.

When setting the RECREQ bit to 1, do not set the TRMREQ bit to 1.

To change the configuration of a mailbox from transmission to reception, first abort the transmission and then set bits SENTDATA and TRMABT to 0 before changing to reception.

TRMREQ Bit (Transmit mailbox set bit)

The TRMREQ bit selects the transmit modes shown in Table 24.13.

When this bit is set to 1, the corresponding mailbox is configured for transmission of a data frame or a remote frame.

When this bit is set to 0, the corresponding mailbox is not configured for transmission of a data frame or a remote frame.

If the TRMREQ bit is changed from 1 to 0 to cancel the corresponding transmission request, either the TRMABT or SENTDATA bit is set to 1.

When setting the TRMREQ bit to 1, do not set the RECREQ bit to 1.

To change the configuration of a mailbox from reception to transmission, first abort the reception and then set bits NEWDATA and MSGLOST to 0 before changing to transmission.

24.2.7 CAN Control Register (CCTLR)

Address 06F40h (CCTLR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CPE	—	RBOC	BOM1	BOM0	SLPM	CANM1	CANM0
After Reset	0	0	0	0	0	1	0	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	TSPS1	TSPS0	TSRC	TPM	MLM	IDFM1	IDFM0	MBM
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CANM0	CAN operating mode select bits (1)	b1 b0 0 0: CAN operation mode 0 1: CAN reset mode 1 0: CAN halt mode 1 1: Do not use this combination	R/W
b1	CANM1			R/W
b2	SLPM	CAN sleep mode bit (1, 2)	0: Other than CAN sleep mode 1: CAN sleep mode	R/W
b3	BOM0	Bus-off recovery mode bits (3)	b4 b3 0 0: Normal mode (ISO11898-1 compliant) 0 1: Entry to CAN halt mode automatically at bus-off entry 1 0: Entry to CAN halt mode automatically at bus-off end 1 1: Entry to CAN halt mode (during bus-off recovery period) by a program request	R/W
b4	BOM1			R/W
b5	RBOC	Forcible return from bus-off bit (4)	0: Nothing occurred 1: Forcible return from bus-off (5)	R/W
b6	—	Reserved	Set to 0.	R/W
b7	CPE	CAN port enable bit (3, 7)	0: Function as I/O ports 1: Function as CAN I/O	R/W
b8	MBM	CAN mailbox mode select bit (3)	0: Normal mailbox mode 1: FIFO mailbox mode	R/W
b9	IDFM0	ID format mode select bits (3)	b10 b9 0 0: Standard ID mode 0 1: Extended ID mode 1 0: Mixed ID mode 1 1: Do not use this combination	R/W
b10	IDFM1			R/W
b11	MLM	Message lost mode select bit (3)	0: Overwrite mode 1: Overrun mode	R/W
b12	TPM	Transmit priority mode select bit (3)	0: ID priority transmit mode 1: Mailbox number priority transmit mode	R/W
b13	TSRC	Time stamp counter reset bit (6)	0: Nothing occurred 1: Reset (5)	R/W
b14	TSPS0	Time stamp prescaler select bits (3)	b15b14 0 0: Every bit time 0 1: Every 2-bit time 1 0: Every 4-bit time 1 1: Every 8-bit time	R/W
b15	TSPS1			R/W

Notes:
1. When bits CANM0, CANM1, and SLPM are changed, check the CSTR register to ensure that the mode has been switched. Do not change bits CANM0, CANM1, and SLPM until the mode has been switched.
   Change the frequencies of the CPU clock and the CAN clock in modes other than CAN operation mode.
2. Write to the SLPM bit in CAN reset mode or CAN halt mode.
   When rewriting the SLPM bit, set only this bit to 0 or 1.
3. Write to bits BOM0, BOM1, CPE, MBM, IDFM0, IDFM1, MLM, TPM, TSPS0, and TSPS1 in CAN reset mode.
4. Set the RBOC bit to 1 in bus-off state.
5. Bits RBOC and TSRC are automatically set back to 0 after being set to 1. Can be read as 0.
6. Set the TSRC bit to 1 in CAN operation mode.
7. To use a CAN wake-up interrupt, set the CPE bit to 1.

Bits CANM0 and CANM1 (CAN operating mode select bits)

Bits CANM0 and CANM1 select one of the following modes for the CAN module: CAN operation mode, CAN reset mode or CAN halt mode. Refer to **24.3 Operational Mode** for details.
CAN sleep mode is set by the SLPM bit.
Do not set bits CANM1 and CANM0 to 11b.
When the CAN module enters CAN halt mode according to the setting of bits BOM0 and BOM1, bits CANM1 and CANM0 are automatically set to 10b.

SLPM Bit (CAN sleep mode bit)

When the SLPM bit is set to 1, the CAN module enters CAN sleep mode.
When this bit is set to 0, the CAN module exits CAN sleep mode.
Refer to **24.3 Operational Mode** for details.

Bits BOM0 and BOM1 (Bus-off recovery mode bits)

Bits BOM0 and BOM1 are used to select bus-off recovery mode.

When bits BOM1 and BOM0 are 00b, the recovery from bus-off is compliant with ISO11898-1, i.e. the CAN module re-enters CAN communication (error-active state) after detecting 11 consecutive recessive bits 128 times. A bus-off recovery interrupt request is generated when recovering from bus-off.

When bits BOM1 and BOM0 are 01b, as soon as the CAN module reaches the bus-off state, bits CANM1 and CANM0 in the CCTLR register are set to 10b (CAN halt mode) and the CAN module enters CAN halt mode. No bus-off recovery interrupt request is generated when recovering from bus-off and registers CTECR and CRECR are set to 00h.

When bits BOM1 and BOM0 are 10b, bits CANM1 and CANM0 are set to 10b as soon as the CAN module reaches the bus-off state. The CAN module enters CAN halt mode after the recovery from the bus-off state, i.e. after detecting 11 consecutive recessive bits 128 times. A bus-off recovery interrupt request is generated when recovering from bus-off and registers CTECR and CRECR are set to 00h.

When bits BOM1 and BOM0 are 11b, the CAN module enters CAN halt mode by setting bits CANM1 and CANM0 to 10b while the CAN module is still in bus-off state. No bus-off recovery interrupt request is generated when recovering from bus-off and registers CTECR and CRECR are set to 00h. However, if the CAN module recovers from bus-off after detecting 11 consecutive recessive bits 128 times before CANM1 and CANM0 are set to10b, a bus-off recovery interrupt request is generated.

If the CPU requests an entry to CAN reset mode at the same time as the CAN module attempts to enter CAN halt mode (at bus-off entry when bits BOM1 and BOM0 are 01b, or at bus-off end when bits BOM1 and BOM0 are 10b), then the CPU request to enter CAN reset mode has higher priority.

RBOC Bit (Forcible return from bus-off bit)

When the RBOC bit is set to 1 (forcible return from bus-off) in bus-off state, the CAN module forcibly returns from the bus-off state. This bit is automatically set to 0. The error state changes from bus-off to error-active.

When the RBOC bit is set to 1, registers CRECR and CTECR are set to 00h and the BOST bit in the CSTR register is set to 0 (the CAN module is not in bus-off state). The other registers remain unchanged. No bus-off recovery interrupt request is generated by this recovery from the bus-off state.
Use the RBOC bit only when bits BOM1 and BOM0 are 00b (normal mode).

CPE Bit (CAN port enable bit)

When the CPE bit is set to 1, pins CRX and CTX function as CAN I/O pins (CRX and CTX), respectively.
When this bit is set to 0, pins CRX and CTX function as port I/O pins. To use the CAN module, set this bit to 1.

MBM Bit (CAN mailbox mode select bit)

When the MBM bit is 0 (normal mailbox mode), mailboxes [0] to [15] are configured as transmit or receive mailboxes.
When this bit is 1 (FIFO mailbox mode), mailboxes [0] to [7] are configured as transmit or receive mailboxes.
Mailboxes [8] to [11] are configured as a transmit FIFO and mailboxes [12] to [15] as a receive FIFO.
Transmit data is written into mailbox [8] (mailbox [8] is a window mailbox for the transmit FIFO).
Receive data is read from mailbox [12] (mailbox [12] is a window mailbox for the receive FIFO).
Table 24.8 lists the Mailbox Configuration.

Table 24.8 Mailbox Configuration

Mailbox	MBM Bit = 0 (Normal mailbox mode)	MBM Bit = 1 (1) (FIFO mailbox mode)
Mailboxes [0] to [7]	Normal mailbox	Normal mailbox
Mailboxes [8] to [11]		Transmit FIFO
Mailboxes [12] to [15]		Receive FIFO

Note:
1. When the MBM bit is set to 1, note the following:
   - Transmit FIFO is controlled by the CTFCR register.
     The CMCTLj register (j = 0 to 15) for mailboxes [8] to [11] is disabled.
     Registers CMCTL8 to CMCTL11 cannot be used.
   - Receive FIFO is controlled by the CRFCR register.
     The CMCTLj register for mailboxes [12] to [15] is disabled.
     Registers CMCTL12 to CMCTL15 cannot be used.
   - Refer to the CMIER register about the FIFO interrupts.
   - The corresponding bits in the CMKIVLR register for mailboxes [8] to [15] are disabled. Set these bits to 0.
   - Transmit/receive FIFOs can be used for both data frames and remote frames.

Bits IDFM0 and IDFM1 (ID format mode select bits)

Bits IDFM0 and IDFM1 specify the ID format.
When bits IDFM1 and IDFM0 are 00b, all mailboxes (including FIFO mailboxes) handle only standard IDs.
When bits IDFM1 and IDFM0 are 01b, all mailboxes (including FIFO mailboxes) handle only extended IDs.
When bits IDFM1 and IDFM0 are 10b, all mailboxes (including FIFO mailboxes) handle both standard IDs and extended IDs. Standard IDs or extended IDs are specified by using the IDE bit in the corresponding mailbox in normal mailbox mode. In FIFO mailbox mode, the IDE bit in the corresponding mailbox is used for mailboxes [0] to [7], the IDE bit in registers CFIDCR0 and CFIDCR1 is used for the receive FIFO, and the IDE bit in mailbox [8] is used for the transmit FIFO.
Do not set bits IDFM1 and IDFM0 to 11b.

MLM Bit (Message lost mode select bit)

The MLM bit specifies the operation when a new message is captured in an unread mailbox.
Overwrite mode or overrun mode can be selected. All mailboxes (including the receive FIFO) are set to either overwrite mode or overrun mode.

When the MLM bit is 0, all mailboxes are set to overwrite mode and the new message is written over the old message.
When this bit is 1, all mailboxes are set to overrun mode and the new message is discarded.

TPM Bit (Transmit priority mode select bit)

The TPM bit specifies the priority of modes when transmitting messages.
ID priority transmit mode or mailbox number transmit mode can be selected.
All mailboxes are set for either ID priority transmission or mailbox number priority transmission.

When the TPM bit is 0, ID priority transmit mode is selected and transmission priority complies with the CAN bus arbitration rule, as defined in the ISO 11898-1 Specifications. In ID priority transmit mode, mailboxes [0] to [15] (in normal mailbox mode), and mailboxes [0] to [7] (in FIFO mailbox mode), and the transmit FIFO are compared for the IDs of mailboxes configured for transmission. If two or more mailbox IDs are the same, the mailbox with the smaller number has higher priority.

Only the next message to be transmitted from the transmit FIFO is included in transmission arbitration. If a transmit FIFO message is being transmitted, the next pending message within the transmit FIFO is included in transmission arbitration.

When the TPM bit is 1, mailbox number transmit mode is selected and the transmit mailbox with the smallest mailbox number has the highest priority. In FIFO mailbox mode, the transmit FIFO has lower priority than normal mailboxes (mailboxes [0] to [7]).

TSRC Bit (Time stamp counter reset bit)

The TSRC bit is used to reset the time stamp counter.
When this bit is set to 1, the CTSR register is set to 0000h. It is automatically set to 0.

Bits TSPS0 and TSPS1 (Time stamp prescaler select bits)

Bits TSPS0 and TSPS1 select the prescaler for the time stamp.
The reference clock for the time stamp can be selected to be either 1-, 2-, 4- or 8-bit time periods.

24.2.8 CAN Status Register (CSTR)

Address 06F42h (CSTR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	RECST	TRMST	BOST	EPST	SLPST	HLTST	RSTST
After Reset	0	0	0	0	0	1	0	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	EST	TABST	FMLST	NMLST	TFST	RFST	SDST	NDST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RSTST	CAN reset status flag	0: Not in CAN reset mode 1: In CAN reset mode	R
b1	HLTST	CAN halt status flag	0: Not in CAN halt mode 1: In CAN halt mode	R
b2	SLPST	CAN sleep status flag	0: Not in CAN sleep mode 1: In CAN sleep mode	R
b3	EPST	Error-passive status flag	0: Not in error-passive state 1: In error-passive state	R
b4	BOST	Bus-off status flag	0: Not in bus-off state 1: In bus-off state	R
b5	TRMST	Transmit status flag	0: Bus idle or reception in progress 1: Transmission in progress or in bus-off state	R
b6	RECST	Receive status flag	0: Bus idle or transmission in progress 1: Reception in progress	R
b7	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b8	NDST	NEWDATA status flag	0: No mailbox with NEWDATA bit = 1 1: Mailbox(es) with NEWDATA bit = 1	R
b9	SDST	SENTDATA status flag	0: No mailbox with SENTDATA bit = 1 1: Mailbox(es) with SENTDATA bit = 1	R
b10	RFST	Receive FIFO status flag	0: No message in receive FIFO (empty) 1: Message in receive FIFO	R
b11	TFST	Transmit FIFO status flag	0: Transmit FIFO is full 1: Transmit FIFO is not full	R
b12	NMLST	Normal mailbox message lost status flag	0: No mailbox with MSGLOST bit = 1 1: Mailbox(es) with MSGLOST bit = 1	R
b13	FMLST	FIFO mailbox message lost status flag	0: RFMLF bit = 0 1: RFMLF bit = 1	R
b14	TABST	Transmission abort status flag	0: No mailbox with TRMABT bit = 1 1: Mailbox(es) with TRMABT bit = 1	R
b15	EST	Error status flag	0: No error occurred 1: Error occurred	R

RSTST Bit (CAN reset status flag)

The RSTST bit is set to 1 when the CAN module is in CAN reset mode.
This bit is set to 0 when the CAN module is not in CAN reset mode.
This bit remains 1 even when the state changes from CAN reset mode to CAN sleep mode.

HLTST Bit (CAN halt status flag)

The HLTST bit is set to 1 when the CAN module is in CAN halt mode.
This bit is set to 0 when the CAN module is not in CAN halt mode.
This bit remains 1 even when the state changes from CAN halt mode to CAN sleep mode.

SLPST Bit (CAN sleep status flag)

The SLPST bit is set to 1 when the CAN module is in CAN sleep mode.
This bit is set to 0 when the CAN module is not in CAN sleep mode.

EPST Bit (Error-passive status flag)

The EPST bit is set to 1 when the value of the CTECR or CRECR register exceeds 127 and the CAN module is in error-passive state (128 ≤ TEC < 256 or 128 ≤ REC < 256). This bit is set to 0 when the CAN module is not in error-passive state.
TEC indicates the value of the transmit error counter (CTECR register) and REC indicates the value of the receive error counter (CRECR register).

BOST Bit (Bus-off status flag)

The BOST bit is set to 1 when the value of the CTECR register exceeds 255 and the CAN module is in bus-off state (TEC ≥ 256). This bit is set to 0 when the CAN module is not in bus-off state.

TRMST Bit (Transmit status flag)

The TRMST bit is set to 1 when the CAN module performs as a transmitter node or is in bus-off state.
This bit is set to 0 when the CAN module performs as a receiver node or is in bus-idle state.

RECST Bit (Receive status flag)

The RECST bit is set to 1 when the CAN module performs as a receiver node.
This bit is set to 0 when the CAN module performs as a transmitter node or is in bus-idle state.

NDST Bit (NEWDATA status flag)

The NDST bit is set to 1 when at least one NEWDATA bit in the CMCTLj register (j = 0 to 15) is 1 regardless of the value of the CMIER register.
The NDST bit is set to 0 when all NEWDATA bits are 0.

SDST Bit (SENTDATA status flag)

The SDST bit is set to 1 when at least one SENTDATA bit in the CMCTLj register (j = 0 to 15) is 1 regardless of the value of the CMIER register.
The SDST bit is set to 0 when all SENTDATA bits are 0.

RFST Bit (Receive FIFO status flag)

The RFST bit is set to 1 when the receive FIFO is not empty.
This bit is set to 0 when the receive FIFO is empty.
This bit is set to 0 when normal mailbox mode is selected.

TFST Bit (Transmit FIFO status flag)

The TFST bit is set to 1 when the transmit FIFO is not full.
This bit is set to 0 when the transmit FIFO is full.
This bit is set to 0 when normal mailbox mode is selected.

NMLST Bit (Normal mailbox message lost status flag)

The NMLST bit is set to 1 when at least one MSGLOST bit in the CMCTLj register is 1 regardless of the value of the CMIER register.
The NMLST bit is set to 0 when all MSGLOST bits are 0.

FMLST Bit (FIFO mailbox message lost status flag)

The FMLST bit is set to 1 when the RFMLF bit in the CRFCR register is 1 regardless of the value of the CMIER register.
The FMLST bit is set to 0 when the RFMLF bit is 0.

TABST Bit (Transmission abort status flag)

The TABST bit is set to 1 when at least one TRMABT bit in the CMCTLj register is 1 regardless of the value of the CMIER register.
The TABST bit is set to 0 when all TRMABT bits are 0.

EST Bit (Error status flag)

The EST bit is 1 when at least one error is detected by the CEIFR register regardless of the value of the CEIER register.
This bit is set to 0 when no error is detected by the CEIFR register.

24.2.9 CAN Bit Configuration Register (CBCR)

Address 06F44h (CBCR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BRP7	BRP6	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	TSEG13	TSEG12	TSEG11	TSEG10	—	—	BRP9	BRP8
After Reset	0	0	0	0	0	0	0	0

Bit	b23	b22	b21	b20	b19	b18	b17	b16
Symbol	—	—	SJW1	SJW0	—	TSEG22	TSEG21	TSEG20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b9 to b0	BRP9 to BRP0	Prescaler division ratio set bits (10 bits)	If the setting value is P (0 to 1023), the baud rate prescaler divides fCAN by P + 1.	R/W
b10	—	Reserved	Set to 0.	R/W
b11	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b12	TSEG10	Time segment 1 control bits	b15b14b13b12 0 0 0 0: Do not use this combination 0 0 0 1: Do not use this combination 0 0 1 0: Do not use this combination 0 0 1 1: 4 Tq 0 1 0 0: 5 Tq 0 1 0 1: 6 Tq 0 1 1 0: 7 Tq 0 1 1 1: 8 Tq 1 0 0 0: 9 Tq 1 0 0 1: 10 Tq 1 0 1 0: 11 Tq 1 0 1 1: 12 Tq 1 1 0 0: 13 Tq 1 1 0 1: 14 Tq 1 1 1 0: 15 Tq 1 1 1 1: 16 Tq	R/W
b13	TSEG11			R/W
b14	TSEG12			R/W
b15	TSEG13			R/W
b16	TSEG20	Time segment 2 control bits	b18b17b16 0 0 0: Do not use this combination 0 0 1: 2 Tq 0 1 0: 3 Tq 0 1 1: 4 Tq 1 0 0: 5 Tq 1 0 1: 6 Tq 1 1 0: 7 Tq 1 1 1: 8 Tq	R/W
b17	TSEG21			R/W
b18	TSEG22			R/W
b19	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b20	SJW0	Resynchronization jump width control bits	b21b20 0 0: 1 Tq 0 1: 2 Tq 1 0: 3 Tq 1 1: 4 Tq	R/W
b21	SJW1			R/W
b23 to b22	—	Nothing is assigned. The write value must be 0. The read value is 0.		—

Set the CBCR register before entering CAN halt mode from CAN reset mode, or CAN operation mode from CAN reset mode. After the setting is made once, this register can be written to in CAN reset mode or CAN halt mode.
The CBCR register consists of 24 bits.
Refer to **24.4 CAN Communication Speed Configuration** about the bit timing configuration.

Bits BRP0 to BRP9 (Prescaler division ratio set bits)

Bits BRP0 to BRP9 are used to set the frequency of the CAN communication clock (fCANCLK).
The cycle of the fCANCLK is set to be 1 Time Quantum (Tq).

Bits TSEG10 to TSEG13 (Time segment 1 control bits)

Bits TSEG10 to TSEG13 are used to specify the total length of the propagation time segment (PROP_SEG) and phase buffer segment 1 (PHASE_SEG1) with the value of Tq.
A value from 4 to 16 time quanta can be set.

Bits TSEG20 to TSEG22 (Time segment 2 control bits)

Bits TSEG20 to TSEG22 are used to specify the length of phase buffer segment 2 (PHASE_SEG2) with the value of Tq.
A value from 2 to 8 time quanta can be set.
Set the value to be smaller than that of bits TSE10 to TSE13.

Bits SJW0 and SJW1 (Resynchronization jump width control bits)

Bits SJW0 and SJW1 are used to specify the resynchronization jump width with the value of Tq.
A value from 1 to 4 time quanta can be set.
Set the value to be smaller than or equal to that of bits TSE20 to TSE22.

24.2.10 CAN Clock Select Register (CCLKR)

Address 06F47h (CCLKR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	CCLKS
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CCLKS	CAN clock source select bit (1)	0: CPU clock 1: CAN clock	R/W
b1	—	Reserved	Set to 0.	R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	—	Reserved	Set to 0.	R/W
b4	—	Reserved	Set to 0. The read value is undefined.	R/W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	—			
b7	—	Reserved	Set to 0.	R/W

Note:
1. Write to this register in CAN reset mode. To set the CCLKS bit to 1, set the CPU clock to equal to or faster than the frequency of the CAN clock.

CCLKS Bit (CAN clock source select bit)

When this bit is 0, the CPU clock is used as the CAN clock source (fCAN).
When this bit is 1, the CAN clock is used as the CAN clock source (fCAN).

24.2.11 CAN Receive FIFO Control Register (CRFCR)

Address 06F48h (CRFCR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RFEST	RFWST	RFFST	RFMLF	RFUST2	RFUST1	RFUST0	RFE
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RFE	Receive FIFO enable bit (1)	0: Receive FIFO disabled 1: Receive FIFO enabled	R/W
b1	RFUST0	Receive FIFO unread message number status flags	b3 b2 b1 0 0 0: No unread message 0 0 1: 1 unread message 0 1 0: 2 unread messages 0 1 1: 3 unread messages 1 0 0: 4 unread messages 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved	R
b2	RFUST1			R
b3	RFUST2			R
b4	RFMLF	Receive FIFO message lost flag (2)	0: No receive FIFO message lost has occurred 1: Receive FIFO message lost has occurred	R/W
b5	RFFST	Receive FIFO full status flag	0: Receive FIFO is not full 1: Receive FIFO is full (4 unread messages)	R
b6	RFWST	Receive FIFO buffer warning status flag	0: Receive FIFO is not buffer warning 1: Receive FIFO is buffer warning (3 unread messages)	R
b7	RFEST	Receive FIFO empty status flag	0: Unread message in receive FIFO 1: No unread message in receive FIFO	R

Notes:
1. When setting the RFE bit to 0, also set the RFMLF bit to 0 simultaneously.
2. Write 0 only. Writing 1 has no effect.

Write to the CRFCR register in CAN operation mode or CAN halt mode.

RFE Bit (Receive FIFO enable bit)

When the RFE bit is set to 1, the receive FIFO is enabled for reception.
When this bit is set to 0, the receive FIFO is disabled for reception and becomes empty (RFEST bit = 1).
Do not set this bit to 1 in normal mailbox mode (MBM bit in the CCTLR register = 0).
Due to HW protection, the RFE bit is not set to 0 by writing 0 by a program during the following period:
HW protection is started
- from the acceptance filter procedure (the beginning of the CRC field)

HW protection is released
- if the receive FIFO is specified to receive the incoming message, after the received data is stored into the receive FIFO or a CAN bus error occurs. (i.e. a maximum period of HW protection is from the beginning of the CRC field to the end of the 7th bit of EOF.)
- if the receive FIFO is not specified to receive the message, after the acceptance filter procedure.

Bits RFUST0 to RFUST2 (Receive FIFO unread message number status flags)

Bits RFUST0 to RFUST2 indicate the number of unread messages in the receive FIFO.
The value of bits RFUST2 to RFUST0 is initialized to 000b when the RFE bit is set to 0.

RFMLF Bit (Receive FIFO message lost flag)

The RFMLF bit is set to 1 (receive FIFO message lost has occurred) when the receive FIFO receives a new message and the receive FIFO is full. The timing for setting this bit to 1 is at the end of the 6th bit of EOF.
The RFMLF bit is set to 0 by writing 0 by a program.
In both overwrite and overrun modes, this bit cannot be set to 0 (receive FIFO message lost has not occurred) by writing 0 by a program due to HW protection during the five cycles of fCAN (CAN system clock) following the 6th bit of EOF, if the receive FIFO is full and determined to receive the message.

RFFST Bit (Receive FIFO full status flag)

The RFFST bit is set to 1 (receive FIFO is full) when the number of unread messages in the receive FIFO is 4. This bit is set to 0 (receive FIFO is not full) when the number of unread messages in the receive FIFO is less than 4. This bit is set to 0 when the RFE bit is 0.

RFWST Bit (Receive FIFO buffer warning status flag)

The RFWST bit is set to 1 (receive FIFO is buffer warning) when the number of unread messages in the receive FIFO is 3. This bit is set to 0 (receive FIFO is not buffer warning) when the number of unread messages in the receive FIFO is less than 3 or equal to 4. This bit is set to 0 when the RFE bit is 0.

RFEST Bit (Receive FIFO empty status flag)

The RFEST bit is 1 (no unread message in receive FIFO) when the number of unread messages in the receive FIFO is 0. This bit is set to 1 when the RFE bit is set to 0. The RFEST bit is set to 0 (unread message in receive FIFO) when the number of unread messages in the receive FIFO is one or more.

Figure 24.2 shows the Receive FIFO Mailbox Operation (Bits 13 and 12 in CMIER Register = 01b or 11b).

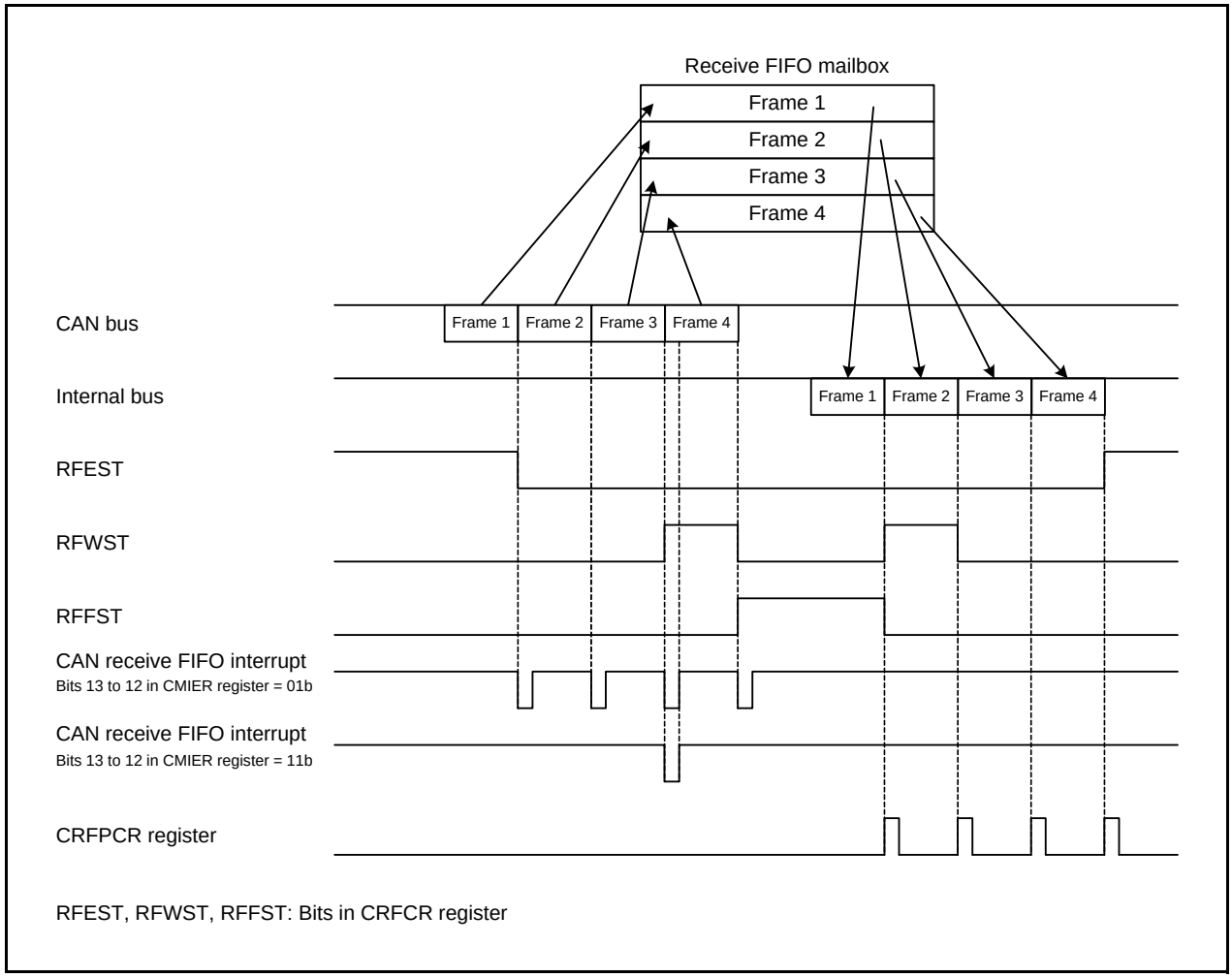


Figure 24.2 Receive FIFO Mailbox Operation (Bits 13 and 12 in CMIER Register = 01b or 11b)

24.2.12 CAN Receive FIFO Pointer Control Register (CRFPCR)

Address 06F49h (CRFPCR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	The CPU-side pointer for the receive FIFO is incremented by writing FFh	FFh	W

When the receive FIFO is not empty, write FFh to the CRFPCR register by a program to increment the CPU-side pointer for the receive FIFO to the next mailbox location.
Do not write to the CRFPCR register when the RFE bit in the CRFCR register is 0 (receive FIFO disabled).
Both the CAN-side pointer and the CPU-side pointer are incremented when a new message is received and the RFFST bit in the CRFCR register is 1 (receive FIFO is full) in overwrite mode. When the RFMLF bit in the CRFCR register is 1 in this condition, the CPU-side pointer cannot be incremented by writing to the CRFPCR register by a program.

24.2.13 CAN Transmit FIFO Control Register (CTFCR)

Address 06F4Ah (CTFCR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TFEST	TFFST	—	—	TFUST2	TFUST1	TFUST0	TFE
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TFE	Transmit FIFO enable bit	0: Transmit FIFO disabled 1: Transmit FIFO enabled	R/W
b1	TFUST0	Transmit FIFO unsent message number status bits	b3 b2 b1 0 0 0: No unsent message 0 0 1: 1 unsent message 0 1 0: 2 unsent messages 0 1 1: 3 unsent messages 1 0 0: 4 unsent messages 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved	R
b2	TFUST1			R
b3	TFUST2			R
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—	Reserved	Set to 0. The read value is undefined.	R
b6	TFFST	Transmit FIFO full status bit	0: Transmit FIFO is not full 1: Transmit FIFO is full (4 unsent messages)	R
b7	TFEST	Transmit FIFO empty status bit	0: Unsent message in transmit FIFO 1: No unsent message in transmit FIFO	R

Write to the CTFCR register in CAN operation mode or CAN halt mode.

TFE Bit (Transmit FIFO enable bit)

When the TFE bit is set to 1, the transmit FIFO is enabled.
When this bit is set to 0, the transmit FIFO becomes empty (TFEST bit = 1) and then unsent messages from the transmit FIFO are lost as described below:

- If a message from the transmit FIFO is not scheduled for the next transmission or during transmission.
- Following the completion of transmission, a CAN bus error, CAN bus arbitration lost, or entry to CAN halt mode if a message from the transmit FIFO is scheduled for the next transmission or already during transmission.

Before setting the TFE bit to 1 again, ensure that the TFEST bit has been set to 1.
After setting the TFE bit to 1, write transmit data into the CMB8 register.
Do not set this bit to 1 in normal mailbox mode (MBM bit in the CCTLR register = 0).

Bits TFUST0 to TFUST2 (Transmit FIFO unsent message number status bits)

Bits TFUST0 to TFUST2 indicate the number of unsent messages in the transmit FIFO.
After the TFE bit is set to 0, the value of bits TFUST2 to TFUST0 is initialized to 000b (no unsent message) when transmission abort or transmission is completed.

TFFST Bit (Transmit FIFO full status bit)

The TFFST bit is set to 1 (transmit FIFO is full) when the number of unsent messages in the transmit FIFO is 4. This bit is set to 0 (transmit FIFO is not full) when the number of unsent messages in the transmit FIFO is less than 4. This bit is set to 0 when transmission from the transmit FIFO has been aborted.

TFEST Bit (Transmit FIFO empty status bit)

The TFEST bit is set to 1 (no message in transmit FIFO) when the number of unsent messages in the transmit FIFO is 0. This bit is set to 1 when transmission from the transmit FIFO has been aborted.
The TFEST bit is set to 0 (message in transmit FIFO) when the number of unsent messages in the transmit FIFO is not 0.

Figure 24.3 shows the Transmit FIFO Mailbox Operation (Bits 9 and 8 in CMIER Register = 01b or 11b).

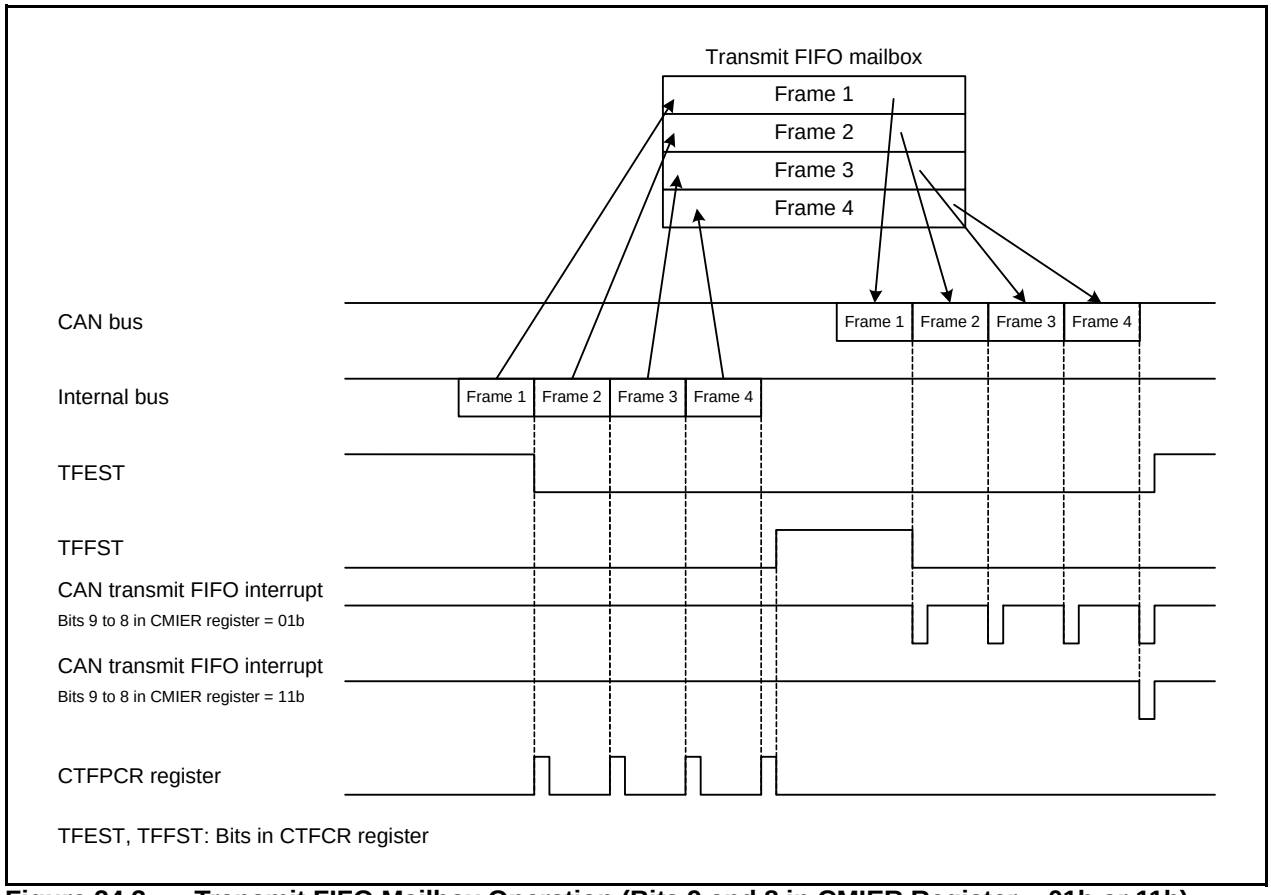


Figure 24.3 Transmit FIFO Mailbox Operation (Bits 9 and 8 in CMIER Register = 01b or 11b)

24.2.14 CAN Transmit FIFO Pointer Control Register (CTFPCR)

Address 06F4Bh (CTFPCR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	The CPU-side pointer for the transmit FIFO is incremented by writing FFh	FFh	W

When the transmit FIFO is not full, write FFh to the CTFPCR register by a program to increment the CPU-side pointer for the transmit FIFO to the next mailbox location.
Do not write to the CTFPCR register when the TFE bit in the CTFPCR register is 0 (transmit FIFO disabled).

24.2.15 CAN Error Interrupt Enable Register (CEIER)

Address 06F4Ch (CEIER_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BLIE	OLIE	ORIE	BORIE	BOEIE	EPIE	EWIE	BEIE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BEIE	Bus error interrupt enable bit	0: Bus error interrupt disabled 1: Bus error interrupt enabled	R/W
b1	EWIE	Error warning interrupt enable bit	0: Error warning interrupt disabled 1: Error warning interrupt enabled	R/W
b2	EPIE	Error passive interrupt enable bit	0: Error passive interrupt disabled 1: Error passive interrupt enabled	R/W
b3	BOEIE	Bus-off entry interrupt enable bit	0: Bus-off entry interrupt disabled 1: Bus-off entry interrupt enabled	R/W
b4	BORIE	Bus-off recovery interrupt enable bit	0: Bus-off recovery interrupt disabled 1: Bus-off recovery interrupt enabled	R/W
b5	ORIE	Receive overrun interrupt enable bit	0: Receive overrun interrupt disabled 1: Receive overrun interrupt enabled	R/W
b6	OLIE	Overload frame transmit interrupt enable bit	0: Overload frame transmit interrupt disabled 1: Overload frame transmit interrupt enabled	R/W
b7	BLIE	Bus lock interrupt enable bit	0: Bus lock interrupt disabled 1: Bus lock interrupt enabled	R/W

Write to the CEIER register in CAN reset mode.
The CEIER register is used to set the error interrupt enabled/disabled individually for each error interrupt source in the CEIFR register.

BEIE Bit (Bus error interrupt enable bit)

When the BEIE bit is 0, no error interrupt request is generated even if the BEIF bit in the CEIFR register is set to 1.
When the BEIE bit is 1, an error interrupt request is generated if the BEIF bit is set to 1.

EWIE Bit (Error warning interrupt enable bit)

When the EWIE bit is 0, no error interrupt request is generated even if the EWIF bit in the CEIFR register is set to 1.
When the EWIE bit is 1, an error interrupt request is generated if the EWIF bit is set to 1.

EPIE Bit (Error passive interrupt enable bit)

When the EPIE bit is 0, no error interrupt request is generated even if the EPIF bit in the CEIFR register is set to 1.
When the EPIE bit is 1, an error interrupt request is generated if the EPIF bit is set to 1.

BOEIE Bit (Bus-off entry interrupt enable bit)

When the BOEIE bit is 0, no error interrupt request is generated even if the BOEIF bit in the CEIFR register is set to 1.
When the BOEIE bit is 1, an error interrupt request is generated if the BOEIF bit is set to 1.

BORIE Bit (Bus-off recovery interrupt enable bit)

When the BORIE bit is 0, an error interrupt request is not generated even if the BORIF bit in the CEIFR register is set to 1.
When the BORIE bit is 1, an error interrupt request is generated if the BORIF bit is set to 1.

ORIE Bit (Receive overrun interrupt enable bit)

When the ORIE bit is 0, no error interrupt request is generated even if the ORIF bit in the CEIFR register is set to 1.
When the ORIE bit is 1, an error interrupt request is generated if the ORIF bit is set to 1.

OLIE Bit (Overload frame transmit interrupt enable bit)

When the OLIE bit is 0, no error interrupt request is generated even if the OLIF bit in the CEIFR register is set to 1.
When the OLIE is 1, an error interrupt request is generated if the OLIF bit is set to 1.

BLIE Bit (Bus lock interrupt enable bit)

When the BLIE bit is 0, no error interrupt request is generated even if the BLIF bit in the CEIFR register is set to 1.
When the BLIE bit is 1, an error interrupt request is generated if the BLIF bit is set to 1.

24.2.16 CAN Error Interrupt Factor Judge Register (CEIFR)

Address 06F4Dh (CEIFR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BLIF	OLIF	ORIF	BORIF	BOEIF	EPIF	EWIF	BEIF
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BEIF	Bus error detect flag	0: No bus error detected 1: Bus error detected	R/W
b1	EWIF	Error warning detect flag	0: No error warning detected 1: Error warning detected	R/W
b2	EPIF	Error passive detect flag	0: No error passive detected 1: Error passive detected	R/W
b3	BOEIF	Bus-off entry detect flag	0: No bus-off entry detected 1: Bus-off entry detected	R/W
b4	BORIF	Bus-off recovery detect flag	0: No bus-off recovery detected 1: Bus-off recovery detected	R/W
b5	ORIF	Receive overrun detect flag	0: No receive overrun detected 1: Receive overrun detected	R/W
b6	OLIF	Overload frame transmission detect flag	0: No overload frame transmission detected 1: Overload frame transmission detected	R/W
b7	BLIF	Bus lock detect flag	0: No bus lock detected 1: Bus lock detected	R/W

If an event corresponding to each bit occurs, the corresponding bit in the CEIFR register is set to 1 regardless of the setting of the CEIER register.
When writing 0 to these bits by a program, use the MOV instruction to ensure that only the specified bit is set to 0 and the other bits are set to 1. Writing 1 has no effect on these bit values. If the set timing occurs simultaneously with the clear timing by the program, the bit becomes 1.

BEIF Bit (Bus error detect flag)

The BEIF bit is set to 1 when a bus error is detected.

EWIF Bit (Error warning detect flag)

The EWIF bit is set to 1 when the value of the receive error counter (REC) or transmit error counter (TEC) exceeds 95.
This bit is set to 1 only when the REC or TEC initially exceeds 95. Thus, if 0 is written to the EWIF bit by a program while the REC or TEC remains greater than 95, this bit is not set to 1 until the REC and the TEC go below 95 and then exceeds 95 again.

EPIF Bit (Error passive detect flag)

The EPIF bit is set to 1 when the CAN error state becomes error-passive (the REC or TEC value exceeds 127).
This bit is set to 1 only when the REC or TEC initially exceeds 127. Thus, if 0 is written to the EPIF bit by a program while the REC or TEC remains greater than 127, this bit is not set to 1 until the REC and the TEC go below 127 and then exceeds 127 again.

BOEIF Bit (Bus-off entry detect flag)

The BOEIF bit is set to 1 when the CAN error state becomes bus-off (the TEC value exceeds 255).
This bit is also set to 1 when bits BOM1 and BOM0 in the CCTLR register are 01b (entry to CAN halt mode automatically at bus-off entry) and the CAN module becomes the bus-off state.

BORIF Bit (Bus-off recovery detect flag)

The BORIF bit is set to 1 when the CAN module recovers from the bus-off state normally by detecting 11 consecutive bits 128 times in the following conditions:
(1) When bits BOM1 and BOM0 in the CCTLR register are 00b.
(2) When bits BOM1 and BOM0 are 10b.
(3) When bits BOM1 and BOM0 are 11b.

The BORIF bit is not set to 1 if the CAN module recovers from the bus-off state in the following conditions:
(1) When bits CANM1 and CANM0 in the CCTLR register are set to 01b (CAN reset mode).
(2) When the RBOC bit in the CCTLR register is set to 1 (forcible return from bus-off).
(3) When bits BOM1 and BOM0 are 01b.
(4) When bits BOM1 and BOM0 are 11b and bits CANM1 and CANM0 are set to 10b (CAN halt mode) before normal recovery occurs.

Table 24.9 lists the Behavior of Bits BOEIF and BORIF according to Setting of Bits BOM0 and BOM1.

Table 24.9 Behavior of Bits BOEIF and BORIF according to Setting of Bits BOM0 and BOM1

CCTLR Register Bits BOM1 and BOM0	BOEIF Bit	BORIF Bit
00b	Set to 1 on entry to the bus-off state.	Set to 1 on exit from the bus-off state.
01b		Do not set to 1.
10b		Set to 1 on exit from the bus-off state.
11b		Set to 1 if normal bus-off recovery occurs before bits CANM1 and CANM0 are set to 10b (CAN halt mode).

ORIF Bit (Receive overrun detect flag)

The ORIF bit is set to 1 when a receive overrun occurs.
This bit is not to set to 1 in overwrite mode. In overwrite mode, a reception complete interrupt request is generated if an overwrite condition occurs and this bit is not set to 1.
In normal mailbox mode, if an overrun occurs in any of mailboxes [0] to [15] in overrun mode, this bit is set to 1.
In FIFO mailbox mode, if an overrun occurs in any of mailboxes [0] to [7] or the receive FIFO in overrun mode, this bit is set to 1.

OLIF Bit (Overload frame transmission detect flag)

The OLIF bit is set to 1 if the transmitting condition of an overload frame is detected when the CAN module performs transmission or reception.

BLIF Bit (Bus lock detect flag)

The BLIF bit becomes 1 if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode.
After the BLIF bit becomes 1, bus lock can be detected again after either of the following conditions is satisfied:
- After this bit is set to 0 from 1, recessive bits are detected (bus lock is resolved).
- After this bit is set to 0 from 1, the CAN module enters CAN reset mode and then enters CAN operation mode again (internal reset).

24.2.17 CAN Receive Error Count Register (CRECR)

Address 06F4Eh (CRECR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b7 to b0	Receive error count function The CRECR register increments or decrements the counter value according to the error status of the CAN module during reception	00h to FFh (1)	R

Note:
1. The value in bus-off state is undefined.

The CRECR register indicates the value of the receive error counter.
Refer to the CAN Specifications (ISO11898-1) about the increment/decrement conditions of the receive error counter.

24.2.18 CAN Transmit Error Count Register (CTECR)

Address 06F4Fh (CTECR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b7 to b0	Transmit error count function The CTECR register increments or decrements the counter value according to the error status of the CAN module during transmission	00h to FFh (1)	R

Note:
1. The value in bus-off state is undefined.

The CTECR register indicates the value of the TEC error counter.
Refer to the CAN Specifications (ISO11898-1) about the increment/decrement conditions of the transmit error counter.

24.2.19 CAN Error Code Store Register (CECSR)

Address 06F50h (CECSR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	EDPM	ADEF	BE0F	BE1F	CEF	AEF	FEF	SEF
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SEF	Stuff error flag (1, 2)	0: No stuff error detected 1: Stuff error detected	R/W
b1	FEF	Form error flag (1, 2)	0: No form error detected 1: Form error detected	R/W
b2	AEF	ACK error flag (1, 2)	0: No ACK error detected 1: ACK error detected	R/W
b3	CEF	CRC error flag (1, 2)	0: No CRC error detected 1: CRC error detected	R/W
b4	BE1F	Bit error (recessive) flag (1, 2)	0: No bit error detected 1: Bit error (recessive) detected	R/W
b5	BE0F	Bit error (dominant) flag (1, 2)	0: No bit error detected 1: Bit error (dominant) detected	R/W
b6	ADEF	ACK delimiter error flag (1, 2)	0: No ACK delimiter error detected 1: ACK delimiter error detected	R/W
b7	EDPM	Error display mode select bit (3, 4)	0: Output of first detected error code 1: Output of accumulated error code	R/W

Notes:
1. Writing 1 has no effect to these bit values.
2. When writing 0 to bits SEF, FEF, AEF, CEF, BE1F, BE0F, and ADEF by a program, use the MOV instruction to ensure that only the specified bit is set to 0 and the other bits are set to 1.
3. Write to the EDPM bit in CAN reset mode or CAN halt mode.
4. If two or more error conditions are detected simultaneously, all related bits are set to 1.

The CECSR register can be used to monitor whether an error has occurred on the CAN bus. Refer to the CAN Specifications (ISO11898-1) to check the generation conditions for each error.
To set each bit except the EDPM bit to 0, write 0 by a program. If the timing at which each bit is set to 1 and the timing at which is written by a program are the same, the relevant bit is set to 1.

SEF Bit (Stuff error flag)

The SEF bit is set to 1 when a stuff error is detected.

FEF Bit (Form error flag)

The FEF bit is set to 1 when a form error is detected.

AEF Bit (ACK error flag)

The AEF bit is set to 1 when an ACK error is detected.

CEF Bit (CRC error flag)

The CEF bit is set to 1 when a CRC error is detected.

BE1F Bit (Bit error (recessive) flag)

The BE1F bit is set to 1 when a recessive bit error is detected.

BE0F Bit (Bit error (dominant) flag)

The BE0F bit is set to 1 when a dominant bit error is detected.

ADEF Bit (ACK delimiter error flag)

The ADEF bit is set to 1 when a form error is detected with the ACK delimiter during transmission.

EDPM Bit (Error display mode select bit)

The EDPM bit selects the output mode of the CECSR register.
When this bit is set to 0, the CECSR register outputs the first error code.
When this bit is set to 1, the CECSR register outputs the accumulated error code.

24.2.20 CAN Channel Search Support Register (CCSSR)

Address 06F51h (CCSSR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	When the value of the channel search is input, the channel number is output to the CMSSR register	Channel value	R/W

Write to the CCSSR register only when bits MBSM1 and MBSM0 in the CMSMR register are 11b (channel search mode).
Write to the CCSSR register in CAN operation mode or CAN halt mode.
The bits in the CCSSR register, which are set to 1, are encoded by an 8 to 3 priority encoder (the LSB has priority) and output to bits MBNST0 to MBNST3 in the CMSSR register.
Whenever the CMSSR register is read, its value is updated.
Figure 24.4 shows the Write and Read of Registers CCSSR and CMSSR.

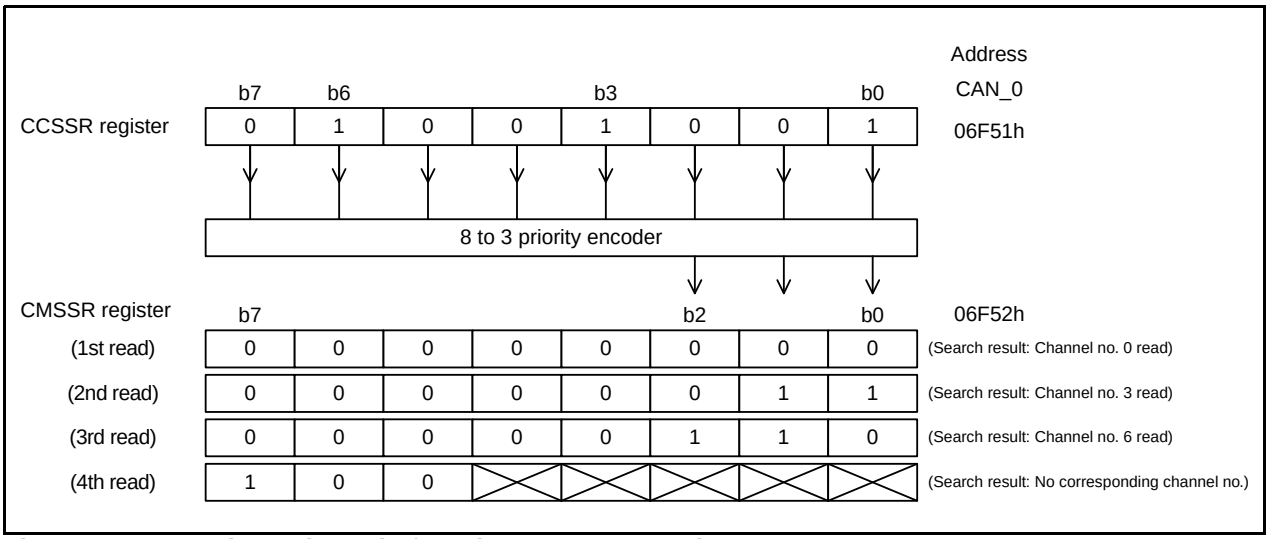


Figure 24.4 Write and Read of Registers CCSSR and CMSSR

The value of the CCSSR register is also updated whenever the CMSSR register is read. When the CCSSR register is read, the value before the 8 to 3 priority encoder conversion is read.

24.2.21 CAN Mailbox Search Status Register (CMSSR)

Address 06F52h (CMSSR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SEST	—	—	—	MBNST3	MBNST2	MBNST1	MBNST0
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MBNST0	Search result mailbox number status bits	Output of search result in each search mode. Output number: 0 to 15	R
b1	MBNST1			R
b2	MBNST2			R
b3	MBNST3			R
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	SEST	Search result status bit	0: Search result found 1: No search result	R

Bits MBNST0 to MBNST3 (Search result mailbox number status bits)

Bits MBNST0 to MBNST3 output the smallest mailbox number that is searched in each mode of the CMSMR register.

In receive mailbox, transmit mailbox, and message lost search modes, the value of the mailbox i.e., the search result to be output, is updated as described below:

- When the NEWDATA, SENTDATA, or MSGLOST bit for the output mailbox is set to 0.
- When the NEWDATA, SENTDATA, or MSGLOST bit for a higher-priority mailbox is set to 1.

In receive mailbox search and message lost search modes, the receive FIFO (mailbox [12]) is output when the receive FIFO is not empty and there are no unread received messages or no lost messages in any of the normal mailboxes (mailboxes [0] to [7]).

In transmit mailbox search mode, the transmit FIFO (mailbox [8]) is not output.

Table 24.10 lists the Behavior of Bits MBNST0 to MBNST3 in FIFO Mailbox Mode.

Table 24.10 Behavior of Bits MBNST0 to MBNST3 in FIFO Mailbox Mode

CMSMR Register Bits MBSM1 and MBSM0	Mailbox [8] (Transmit FIFO)	Mailbox [12] (Receive FIFO)
00b	Mailbox [8] is not output.	Mailbox [12] is output when no NEWDATA bit for the normal mailbox is set to 1 and the receive FIFO is not empty.
01b		Mailbox [12] is not output.
10b		Mailbox [12] is output when no MSGLOST bit for the normal mailbox is set to 1 and the RFMLF bit is set to 1 in the receive FIFO.
11b		Mailbox [12] is not output.

In channel search mode, the corresponding channel number is output. After the CMSSR register is read by a program, the next target channel number is output.

SEST Bit (Search result status bit)

The SEST bit is set to 1 when no corresponding mailbox is found after searching all mailboxes.

For example, in transmit mailbox search mode, the SEST bit is set to 1 when no SENTDATA bit for mailboxes is 1. The SEST bit is set to 0 when at lease one SENTDATA bit is 1.

When the SEST bit is 1, the value of bits MBNST0 to MBNST3 is undefined.

24.2.22 CAN Mailbox Search Mode Register (CMSMR)

Address 06F53h (CMSMR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	MBSM1	MBSM0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MBSM0	Mailbox search mode select bits	b1 b0 0 0: Receive mailbox search mode 0 1: Transmit mailbox search mode 1 0: Message lost search mode 1 1: Channel search mode	R/W
b1	MBSM1			R/W
b7 to b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—

Write to the CMSMR register in CAN operation mode or CAN halt mode.

Bits MBSM0 and MBSM1 (Mailbox search mode select bits)

Bits MBSM0 and MBSM1 select the search mode for the mailbox search function.
When bits MBSM1 and MBSM0 are 00b, receive mailbox search mode is selected. In this mode, the search targets are the NEWDATA bit in the CMCTLj register (j = 0 to 15) for the normal mailbox and the RFESF bit in the CRFCR register.
When bits MBSM1 and MBSM0 are 01b, transmit mailbox search mode is selected. In this mode, the search target is the SENTDATA bit in the CMCTLj register.
When bits MBSM1 and MBSM0 are 10b, message lost search mode is selected. In this mode, the search targets are the MSGLOST bit in the CMCTLj register for the normal mailbox and the RFMLF bit in the CRFCR register.
When bits MBSM1 and MBSM0 are 11b, channel search mode is selected. In this mode, the search target is the CCSSR register. Refer to **24.2.20 CAN Channel Search Support Register (CCSSR)**.

24.2.23 CAN Time Stamp Register (CTSR)

Address 06F54h (CTSR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	Free-running counter value for the time stamp function	0000h to FFFFh	R

Read the CTSR register in 16-bit units.
When the CTSR register is read, the value of the time stamp counter (16-bit free-running counter) at that moment is read.
The value of the time stamp counter reference clock is a multiple of 1 bit time, as configured by bits TSPS0 and TSPS1 in the CCTLR register.
The time stamp counter stops in CAN sleep mode and CAN halt mode, and is initialized in CAN reset mode.
The time stamp counter value is stored to bits TSL0 to TSL7 and TSH0 to TSH7 in the CMBj register (j = 0 to 15) when a received message is stored in a receive mailbox.

24.2.24 CAN Acceptance Filter Support Register (CAFSR)

Address 06F56h (CAFSR_0)

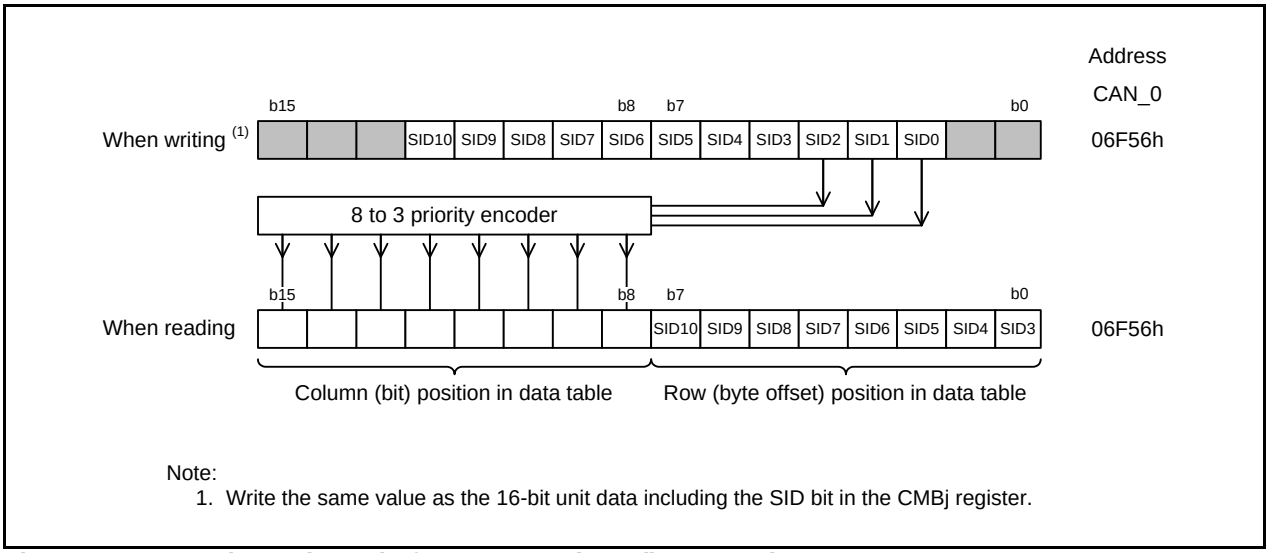
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b15 to b0	After the standard ID of a received message is written, the value converted for data table search can be read	Standard ID/ converted value	R/W

Write to the CAFSR register in CAN operation mode or CAN halt mode.

The acceptance filter support unit (ASU) can be used for data table (8 bits × 256) search. In the data table, all standard IDs created by the user are set to be valid/invalid in bit units. When the CAFSR register is written with the 16-bit unit data including the SID bit in the CMBj register (j = 0 to 15), in which a received ID is stored, a decoded row (byte offset) position and column (bit) position for data table search can be read. The ASU can be used for standard (11-bit) IDs only.
The ASU is enabled in the following cases:
• When the ID to receive cannot be masked by the acceptance filter.
Example) IDs to receive: 078h, 087h, 111h
• When there are too many IDs to receive and software filtering time is must be shortened.
Figure 24.5 shows the Write and Read of CAFSR Register (j = 0 to 15).



Note:
1. Write the same value as the 16-bit unit data including the SID bit in the CMBj register.

Figure 24.5 Write and Read of CAFSR Register (j = 0 to 15)

24.2.25 CAN Test Control Register (CTCR)

Address 06F58h (CTCR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TSTM1	TSTM0	TSTE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTE	CAN test mode enable bit	0: CAN test mode disabled 1: CAN test mode enabled	R/W
b1	TSTM0	CAN test mode select bits	b2 b1 0 0: Other than CAN test mode 0 1: Listen-only mode 1 0: Self-test mode 0 (external loop back) 1 1: Self-test mode 1 (internal loop back)	R/W
b2	TSTM1			R/W
b7 to b3	—	Reserved	Set to 0.	R/W

Write to the CTCR register only in CAN halt mode.

TSTE Bit (CAN test mode enable bit)

When the TSTE bit is set to 0, CAN test mode is disabled.
When this bit is set to 1, CAN test mode is enabled.

Bits TSTM0 and TSTM1 (CAN test mode select bits)

Bits TSTM0 and TSTM1 select the CAN test mode.
The details of each CAN test mode are described below.

24.2.25.1 Listen-Only Mode

The ISO 11898-1 recommends an optional bus monitoring mode. In listen-only mode, the CAN node is able to receive valid data frames and valid remote frames. It sends only recessive bits on the CAN bus, and the protocol controller is not required to send the ACK bit, overload flag, or active error flag.
Listen-only mode can be used for baud rate detection.
Do not request transmission from any mailboxes in this mode.
Figure 24.6 shows the Connection when Listen-Only Mode is Selected.

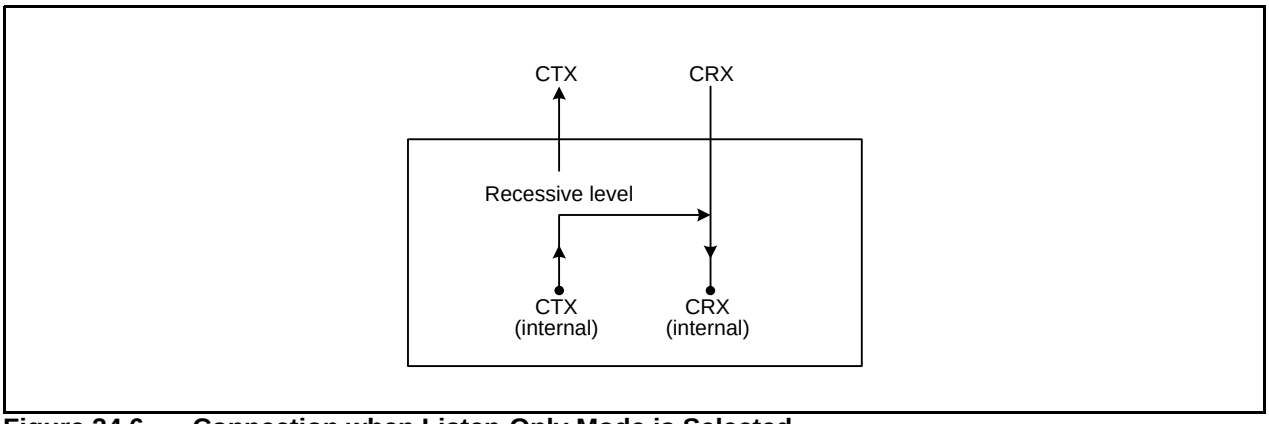


Figure 24.6 Connection when Listen-Only Mode is Selected

24.2.25.2 Self-Test Mode 0 (External Loop Back)

Self-test mode 0 is provided for CAN transceiver tests.
In this mode, the protocol controller treats its own transmitted messages as messages received via the CAN transceiver and stores them into the receive mailbox. To be independent from external stimulation, the protocol controller generates the ACK bit.
Connect the CTX/CRX pins to the transceiver.
Figure 24.7 shows the Connection when Self-Test Mode 0 is Selected.

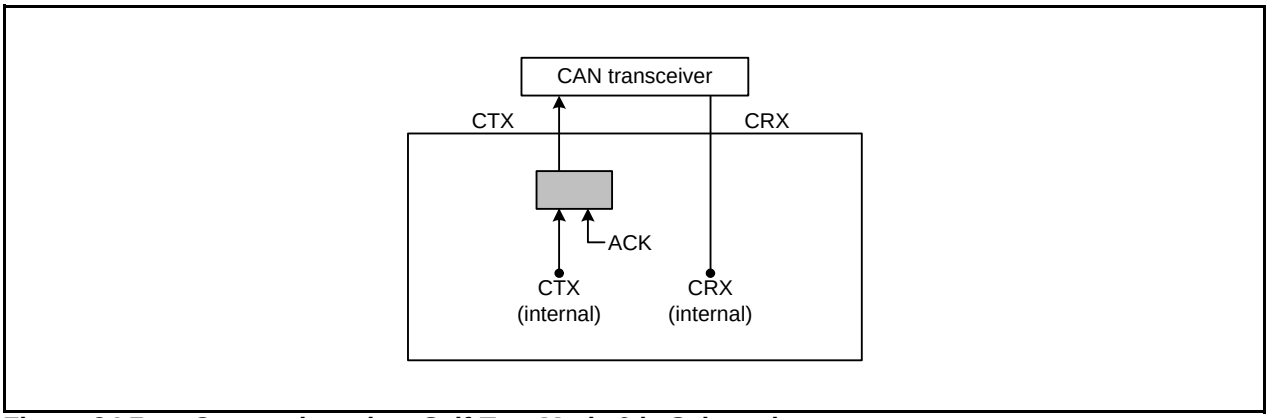


Figure 24.7 Connection when Self-Test Mode 0 is Selected

24.2.25.3 Self-Test Mode 1 (Internal Loop Back)

Self-test mode 1 is provided for self-test functions.
In this mode, the protocol controller treats its transmitted messages as received messages and stores them into the receive mailbox. To be independent from external stimulation, the protocol controller generates the ACK bit.
In self-test mode 1, the protocol controller performs internal feedback from the internal CTX pin to the internal CRX pin. The input value of the external CRX pin is ignored. The external CTX pin outputs only recessive bits. The CTX/CRX pins do not need to be connected to the CAN bus or any external device.
Figure 24.8 shows the Connection when Self-Test Mode 1 is Selected.

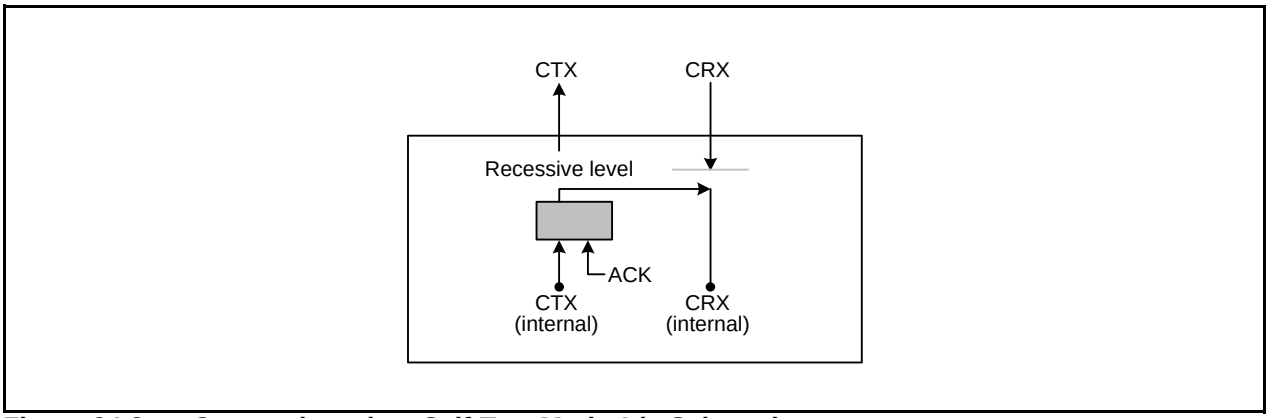


Figure 24.8 Connection when Self-Test Mode 1 is Selected

24.2.26 CAN Interrupt Status Register (CANISR)

Address 06F7Eh (CANISR_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WKUP	ERR	TFIFO	TE	RFIFO	RE	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	RE	Reception complete interrupt flag (1)	0: Interrupt requested 1: Interrupt requested	R
b3	RFIFO	Receive FIFO interrupt flag (1, 2)		R/W
b4	TE	Transmission complete interrupt flag (1)		R
b5	TFIFO	Transmit FIFIO interrupt flag (1, 2)		R/W
b6	ERR	Bus error, warning, error passive, bus-off start, bus-off recovery, overrun, overload, and bus lock interrupt flag (1, 2)		R/W
b7	WKUP	Wake-up interrupt flag (2)		R/W

Notes:
1. This flag is set to 0 when the CAN module enters CAN reset mode.
2. This flag is set to 0 only when 0 is written after reading 1.

24.2.27 CAN Interrupt Control Register (CANIE)

Address 06F7Fh (CANIE_0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WKUPIE	ERRIE	TEIFOIE	TEIE	RFIFOIE	REIE	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	REIE	Reception complete interrupt enable bit	0: Interrupt request disabled 1: Interrupt request enabled	R/W
b3	RFIFOIE	Receive FIFO interrupt enable bit		R/W
b4	TEIE	Transmission complete interrupt enable bit		R/W
b5	TEIFOIE	Transmit FIFIO interrupt enable bit		R/W
b6	ERRIE	Bus error, warning, error passive, bus-off start, bus-off recovery, overrun, overload, and bus lock interrupt enable bit		R/W
b7	WKUPIE	Wake-up interrupt enable bit		R/W

The following three interrupt requests can be generated. Each interrupt request is shared with multiple sources.
- CAN receive interrupt: shared with CAN reception complete interrupt and CAN receive FIFO interrupt
- CAN transmit interrupt: shared with CAN transmission complete interrupt and CAN transmit FIFO interrupt
- CAN error interrupt: shared with CAN error interrupt and CAN wake-up interrupt

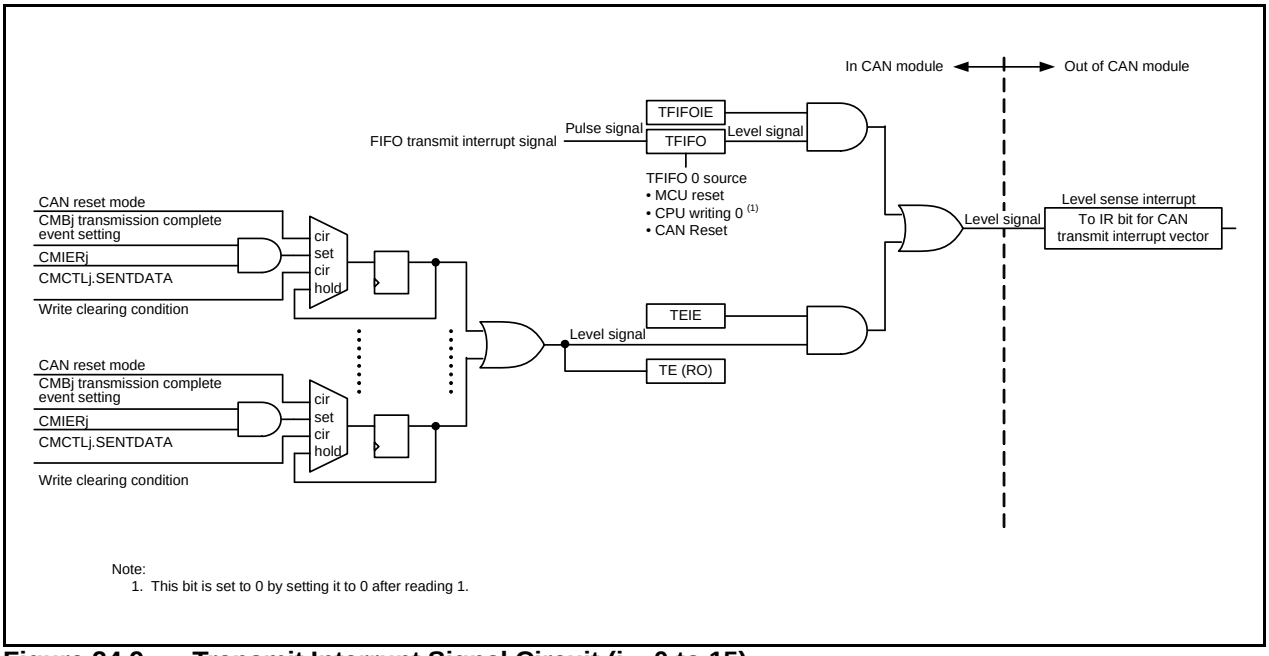


Figure 24.9 Transmit Interrupt Signal Circuit (j = 0 to 15)

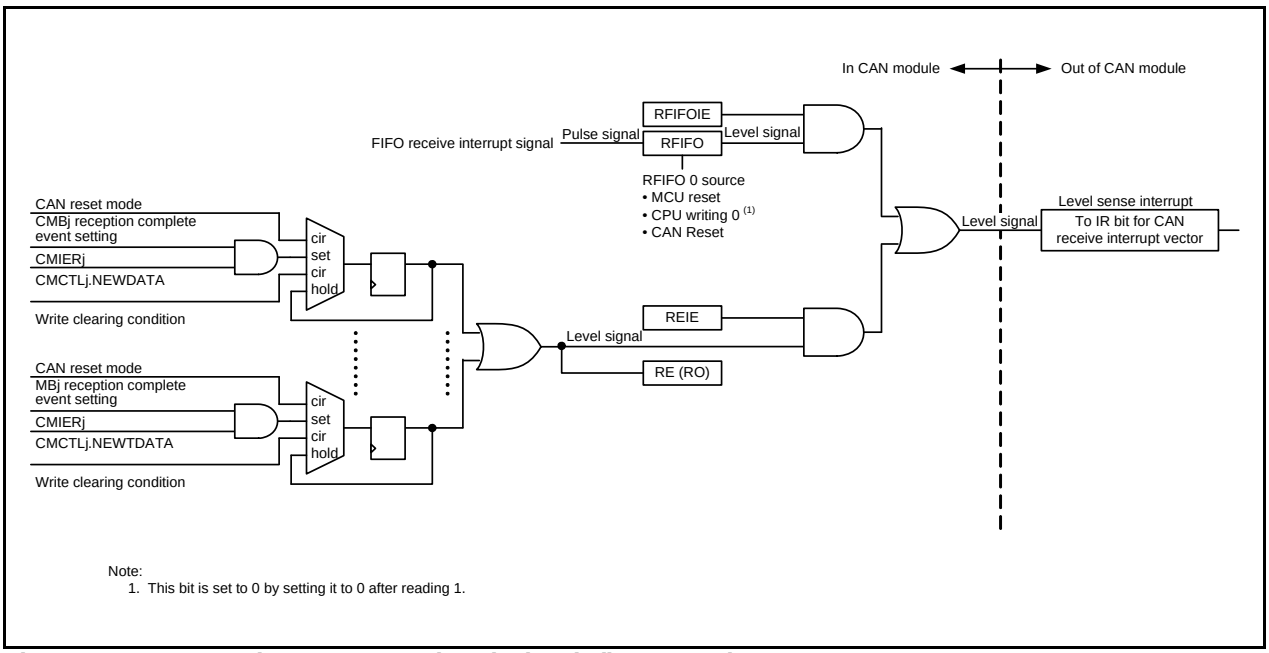


Figure 24.10 Receive Interrupt Signal Circuit (j = 0 to 15)

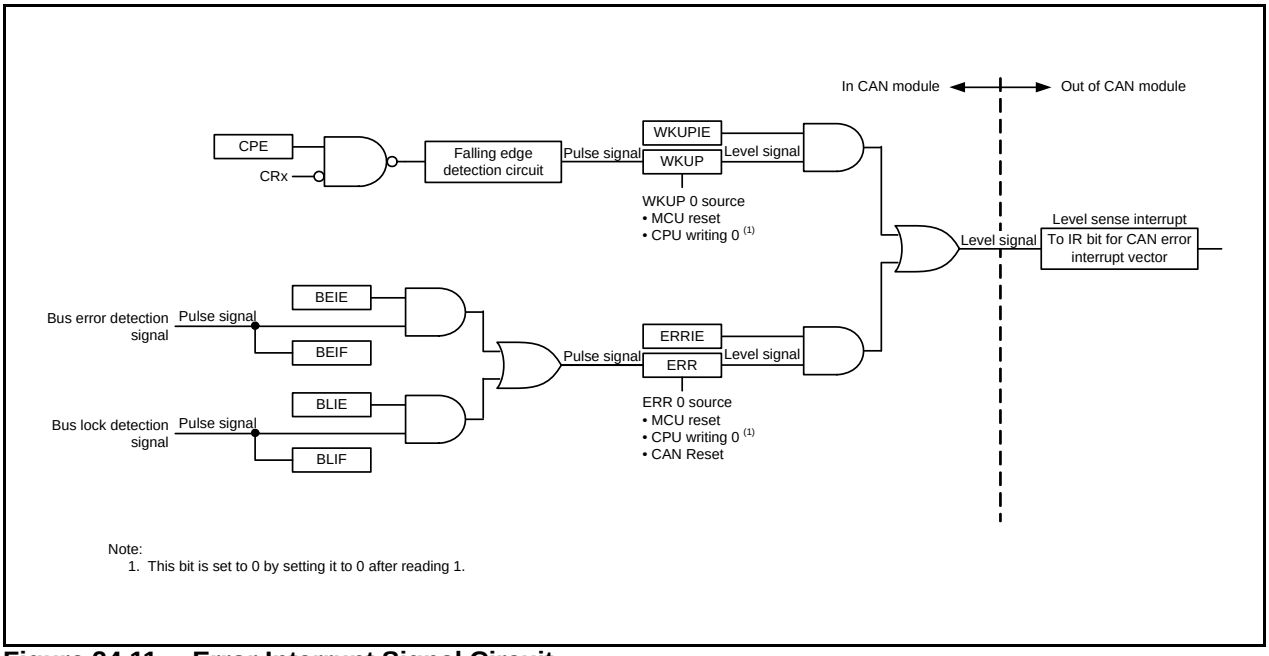
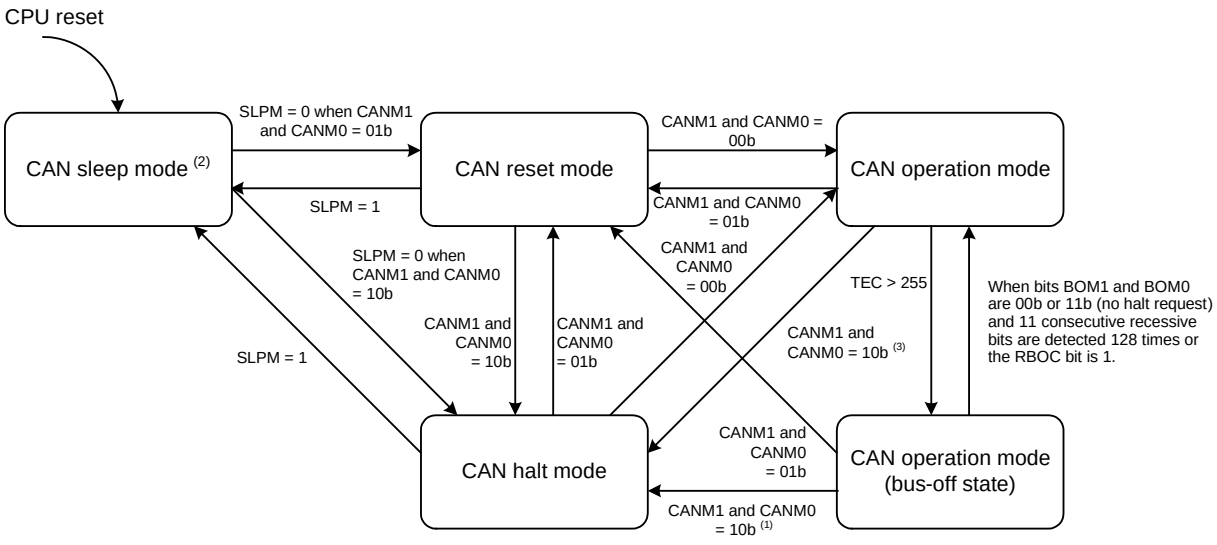


Figure 24.11 Error Interrupt Signal Circuit

24.3 Operational Mode

The CAN module has the following four operating modes.
- CAN reset mode
- CAN halt mode
- CAN operation mode
- CAN sleep mode

Figure 24.12 shows the Transition between CAN Operating Modes.



CANM0, CANM1, SLPM, BOM0, BOM1, RBOC: Bits in the CCTLR register

Notes:
1. The transition timing from the bus-off state to CAN halt mode depends on the setting of bits BOM0 and BOM1.
   - When bits BOM1 and BOM0 are 01b, the state transition timing is immediately after entering the bus-off state.
   - When bits BOM1 and BOM0 are 10b, the state transition timing is at the end of the bus-off state.
   - When bits BOM1 and BOM0 are 11b, the state transition timing is at the setting of bits CANM1 and CANM0 to 10b (CAN halt mode).
2. Write only to the SLPM bit to exit/set CAN sleep mode.
3. The CAN module does not enter CAN halt mode while the CAN bus is locked in dominant state. Enter CAN reset mode instead.

Figure 24.12 Transition between CAN Operating Modes

24.3.1 CAN Reset Mode

CAN reset mode is provided for CAN communication configuration.
When bits CANM1 and CANM0 in the CCTLR register are set to 01b, the CAN module enters CAN reset mode. The RSTST bit in the CSTR register is then set to 1. Do not change bits CANM0 and CANM1 until the RSTST bit is set to 1.
Configure the CBCR register before exiting CAN reset mode to any other modes.

The following registers are initialized to their reset values after entering CAN reset mode and their initialized values are retained during CAN reset mode:
• CMCTLj register (j = 0 to 15)
• CSTR register (except bits SLPST and TFST)
• CEIFR register
• CRECR register
• CTECR register
• CTSR register
• CMSSR register
• CMSMR register
• CRFCR register
• CTFCR register
• CTCR register
• CECSR register (except EDPM bit)
• CANISR register

The previous values of the following registers are retained after entering CAN reset mode.
• CCLKR register
• CCTLR register
• CSTR register (bits SLPST and TFST)
• CMIER register
• CEIER register
• CBCR register
• CCSSR register
• CECSR register (EDPM bit only)
• CMBj register
• Registers CMKR0 to CMKR3
• Registers CFIDCR0 and CFIDCR1
• CMKIVLR register
• CAFSR register
• CRFPCR register
• CTFPCR register
• CANIE register

24.3.2 CAN Halt Mode

CAN halt mode is used for mailbox configuration and test mode setting.
When bits CANM1 and CANM0 in the CCTLR register are set to 10b, CAN halt mode is selected. The HLTST bit in the CSTR register is then set to 1. Do not change bits CANM0 and CANM1 until the HLTST bit is set to 1.
Refer to **Table 24.11 Operation in CAN Reset Mode and CAN Halt Mode** regarding the state transition conditions when transmitting or receiving.
All registers except bits RSTST, HLTST, and SLPST in the CSTR register remain unchanged when the CAN module enters CAN halt mode.
Do not change registers CCLKR, CCTLR (except bits CANM0, CANM1, and SLPM), and CEIER in CAN halt mode. The CBCR register can be changed in CAN halt mode only when listen-only mode is selected to use for automatic bit rate detection.

Table 24.11 Operation in CAN Reset Mode and CAN Halt Mode

Mode	Receiver	Transmitter	Bus-off
CAN reset mode	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode after waiting for the end of message transmission. (1, 4)	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception. (2, 3)	CAN module enters CAN halt mode after waiting for the end of message transmission. (1, 2, 4)	[When bits BOM1 and BOM0 are 00b] A halt request from a program will be acknowledged only after bus-off recovery. [When bits BOM1 and BOM0 are 01b] CAN module enters automatically to CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program). [When bits BOM1 and BOM0 are 10b] CAN module enters automatically to CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program). [When bits BOM1 and BOM0 are 11b] CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off.

BOM0, BOM1: Bits in CCTLR register
Notes:
1. If several messages are requested to be transmitted, mode transition occurs after the completion of the first message transmission. When CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.
2. If the CAN bus is locked in dominant state, the program can detect this state by monitoring the BLIF bit in the CEIFR register. The CAN module does not enter CAN halt mode while the CAN bus is locked in dominant state. Enter CAN reset mode instead.
3. If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN module enters CAN halt mode. However, the CAN module does not enter CAN halt mode when the CAN bus is locked in dominant state.
4. If a CAN bus error or arbitration lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN module enters the requested operating mode. However, the CAN module does not enter CAN halt mode when the CAN bus is locked in dominant state.

24.3.3 CAN Sleep Mode

CAN sleep mode is used for reducing current consumption by stopping the clock supply to the CAN module. After MCU reset, the CAN module starts from CAN module sleep mode.
When the SLPM bit in the CCTLR register is set to 1, the CAN module enters CAN sleep mode. The SLPST bit in the CSTR register is then set to 1. Do not change the value of the SLPM bit until the SLPST bit is set to 1. The other registers remain unchanged when the MCU enters CAN sleep mode.
Write to the SLPM bit in CAN reset mode and CAN halt mode. Do not change any other registers (except the SLPM bit) during CAN sleep mode. Read operation is still allowed.
When the SLPM bit is set to 0, the CAN module is released from CAN sleep mode. When the CAN module exits CAN sleep mode, the other registers remain unchanged.

24.3.4 CAN Operation Mode (Excluding Bus-Off State)

CAN operation mode is used for CAN communication.
When bits CANM1 and CANM0 in the CCTLR register are set to 00b, the CAN module enters CAN operation mode.
Bits RSTST and HLTST in the CSTR register are then set to 0. Do not change the value of bits CANM0 and CANM1 until these bits are set to 0.
If 11 consecutive recessive bits are detected after entering CAN operation mode, the CAN module is in the following states:

- The CAN module becomes an active node on the network that enables transmission and reception of CAN messages.
- Error monitoring of the CAN bus, such as receive and transmit error counters, is performed.

During CAN operation mode, the CAN module may be in one of the following three sub modes, depending on the status of the CAN bus:

- Idle mode: Transmission or reception is not being performed.
- Receive mode: A CAN message sent by another node is being received.
- Transmit mode: A CAN message is being transmitted. The CAN module may receive its own message simultaneously when self-test mode 0 (bits TSTM1 and TSTM0 in the CSTR register = 10b) or self-test mode 1 (bits TSTM1 and TSTM0 = 11b) is selected.

Figure 24.13 shows the Sub Mode in CAN Operation Mode.

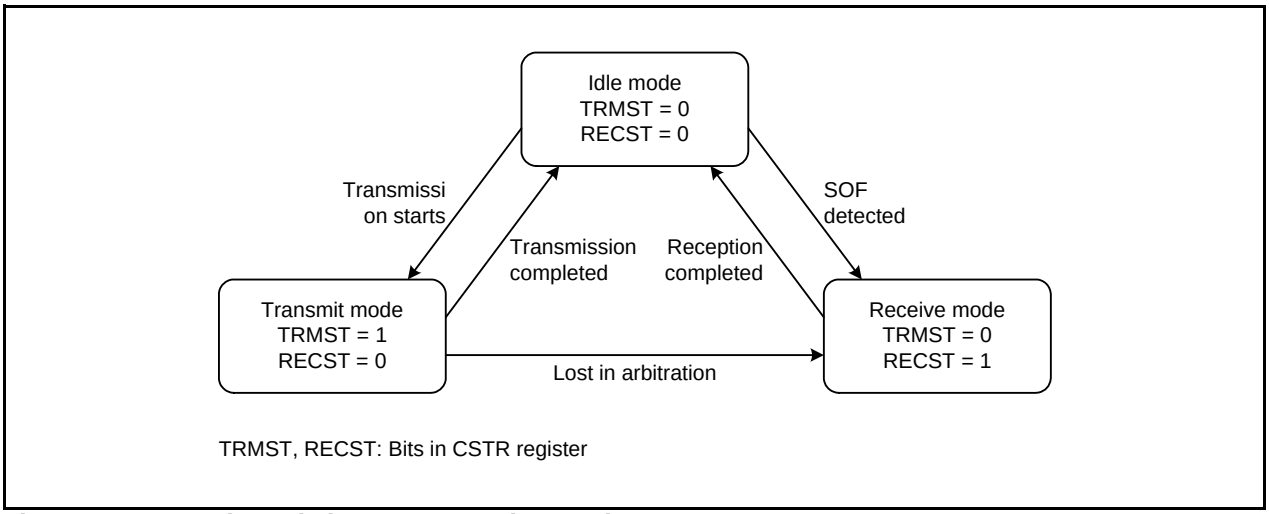


Figure 24.13 Sub Mode in CAN Operation Mode

24.3.5 CAN Operation Mode (Bus-Off State)

The CAN module enters the bus-off state according to the increment/decrement rules for the transmit/error counters in the CAN Specifications.
The following cases apply when recovering from the bus-off state. When the CAN module is in bus-off state, the values of the associated registers, except registers CSTR, CEIFR, CRECR, CTECR and CTSR, remain unchanged.

(1) When bits BOM1 and BOM0 in the CCTLR register are 00b (normal mode)
The CAN module enters the error-active state after it has completed the recovery from the bus-off state and CAN communication is enabled. The BORIF bit in the CEIFR register is set to 1 (bus-off recovery detected) at this time.

(2) When the RBOC bit in the CCTLR register is set to 1 (forcible return from bus-off)
The CAN module enters the error-active state when it is in bus-off state and the RBOC bit is set to 1. CAN communication is enabled again after 11 consecutive recessive bits are detected. The BORIF bit is not set to 1 at this time.

(3) When bits BOM1 and BOM0 are 01b (entry to CAN halt mode automatically at bus-off entry)
The CAN module enters CAN halt mode when it reaches the bus-off state. The BORIF bit is not set to 1 at this time.

(4) When bits BOM1 and BOM0 are 10b (entry to CAN halt mode automatically at bus-off end)
The CAN module enters CAN halt mode when it has completed the recovery from bus-off. The BORIF bit is set to 1 at this time.

(5) When bits BOM1 and BOM0 are 11b (entry to CAN halt mode by a program) and bits CANM1 and CANM0 in the CCTLR register are set to 10b (CAN halt mode) during the bus-off state
The CAN module enters CAN halt mode when it is in bus-off state and bits CANM1 and CANM0 are set to 10b (CAN halt mode). The BORIF bit is not set to 1 at this time.
If bits CANM1 and CANM0 are not set to 10b during bus-off, the same behavior as (1) applies.

24.4 CAN Communication Speed Configuration

The following description explains about the CAN communication speed configuration.

24.4.1 CAN Clock Configuration

The CAN clock selection circuit is available in this group. The CAN clock can be configured by setting bits PCLK10 to PCLK12 in the PCLKR1 register, the CCLKS bit in the CCLKR register, and bits BRP0 to BRP9 in the CBCR register.
Figure 24.14 shows the CAN Clock Generator Block Diagram.

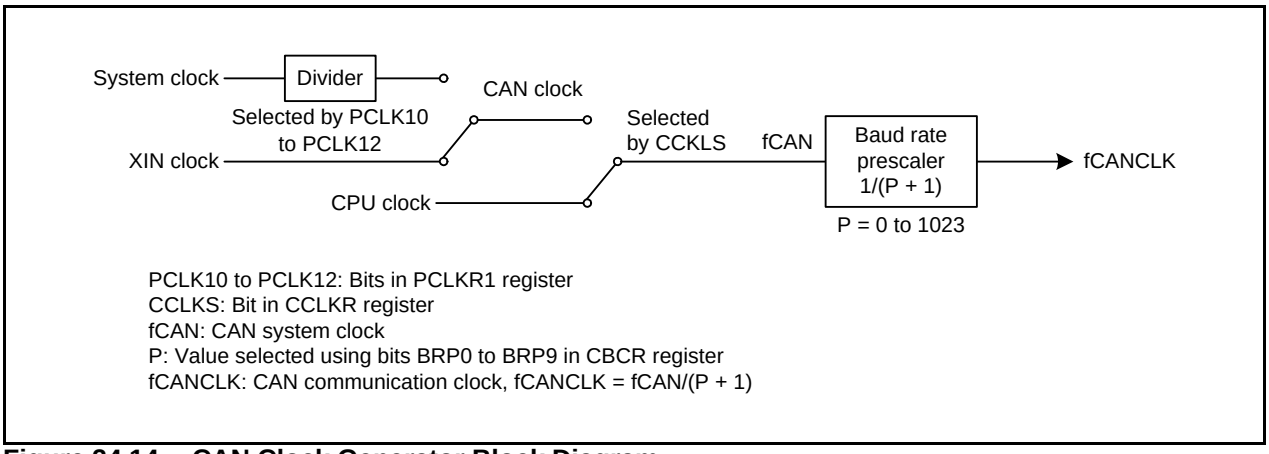


Figure 24.14 CAN Clock Generator Block Diagram

24.4.2 Bit Timing Configuration

The bit time is a single bit time for transmitting/receiving a message and consists of the following three segments.
Figure 24.15 shows the Bit Timing.

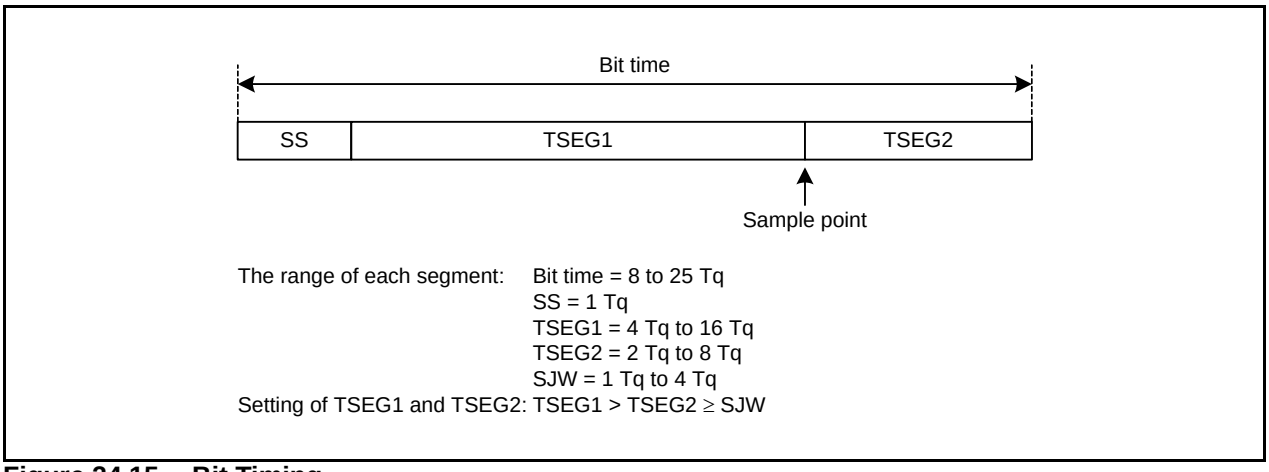


Figure 24.15 Bit Timing

24.4.3 Bit Rate

The bit rate depends on the CAN system clock (fCAN), the division value of the baud rate prescaler, and the number of Tq of one bit time.

$$\text{Bit rate [bps]} = \frac{\text{fCAN}}{\text{Baud rate prescaler division value }^{(1)} \times \text{number of Tq of one bit time}} = \frac{\text{fCANCLK}}{\text{Number of Tq of one bit time}}$$

Note:
1. Division value of the baud rate prescaler = P + 1 (P = 0 to 1023)
   P: Setting value of bits BRP0 to BRP9 in the CBCR register

Table 24.12 lists the Bit Rate Examples.

Table 24.12 Bit Rate Examples

fCAN	32 MHz		24 MHz		20 MHz		16 MHz		8 MHz	
Bit Rate	No. of Tq	P + 1	No. of Tq	P + 1	No. of Tq	P + 1	No. of Tq	P + 1	No. of Tq	P + 1
1 Mbps	8 Tq	4	8 Tq	3	10 Tq	2	8 Tq	2	8 Tq	1
	16 Tq	2	—	—	20 Tq	1	16 Tq	1	—	—
500 kbps	8 Tq	8	8 Tq	6	10 Tq	4	8 Tq	4	8 Tq	2
	16 Tq	4	16 Tq	3	20 Tq	2	16 Tq	2	16 Tq	1
250 kbps	8 Tq	16	8 Tq	12	10 Tq	8	8 Tq	8	8 Tq	4
	16 Tq	8	16 Tq	6	20 Tq	4	16 Tq	4	16 Tq	2
83.3 kbps	8 Tq	48	8 Tq	36	8 Tq	30	8 Tq	24	8 Tq	12
	16 Tq	24	16 Tq	18	10 Tq	24	16 Tq	12	16 Tq	6
	—	—	—	—	16 Tq	15	—	—	—	—
	—	—	—	—	20 Tq	12	—	—	—	—
33.3 kbps	8 Tq	120	8 Tq	90	8 Tq	75	8 Tq	60	8 Tq	30
	10 Tq	96	10 Tq	72	10 Tq	60	10 Tq	48	10 Tq	24
	16 Tq	60	16 Tq	45	20 Tq	30	16 Tq	30	16 Tq	15
	20 Tq	48	20 Tq	36	—	—	20 Tq	24	20 Tq	12

24.5 Mailbox and Mask Register Structure

There are 16 mailboxes with the same structure.
Figure 24.16 shows the Structure of CMBj Register (j = 0 to 15).

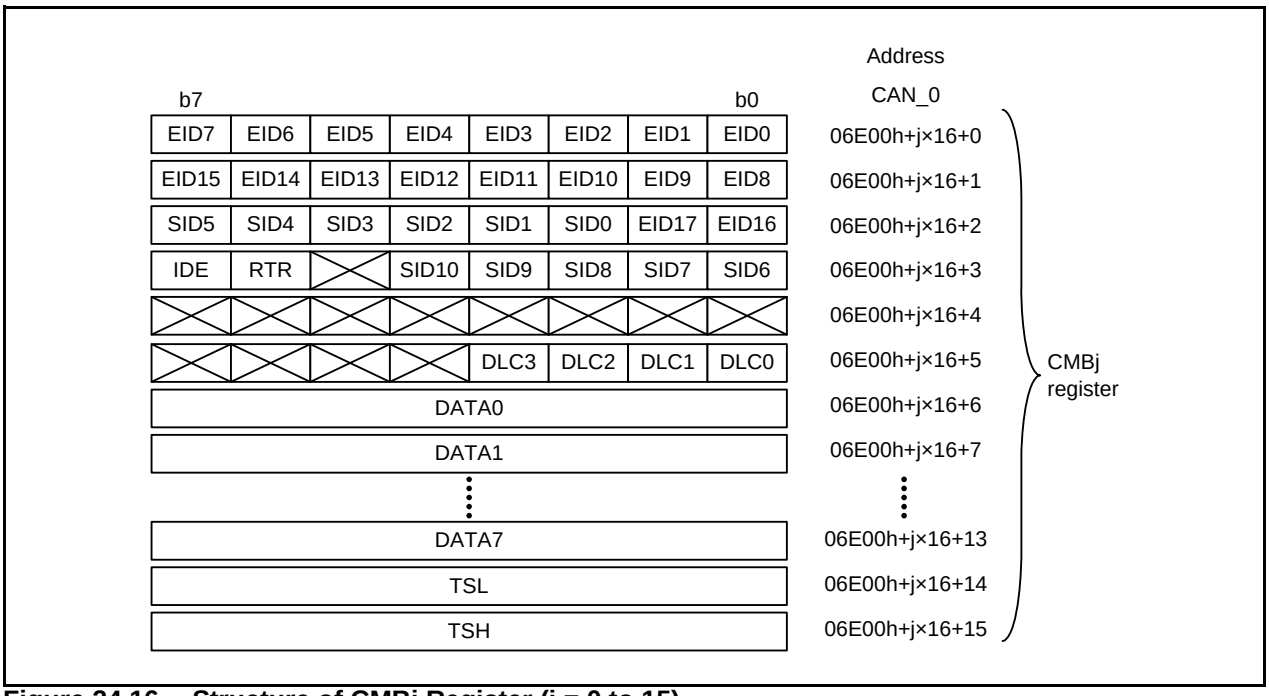


Figure 24.16 Structure of CMBj Register (j = 0 to 15)

There are four mask registers with the same structure.
Figure 24.17 shows the Structure of CMKRk Register (k = 0 to 3).

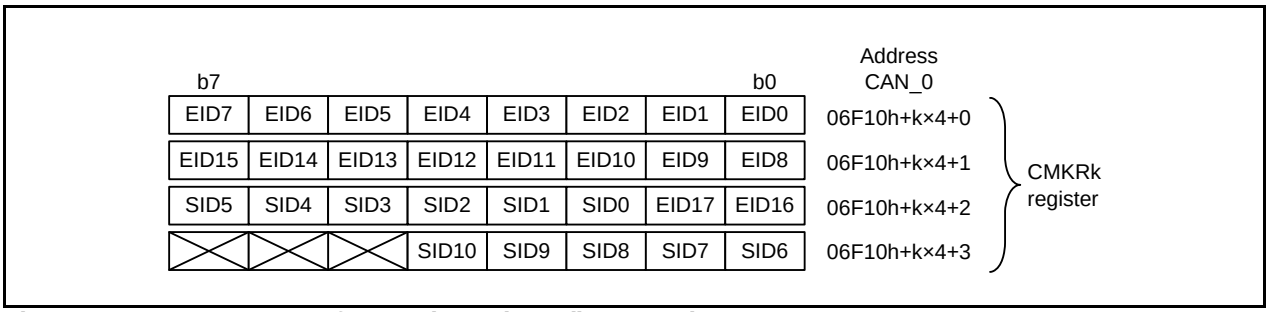


Figure 24.17 Structure of CMKRk Register (k = 0 to 3)

There are two FIFO received ID compare registers with the same structure.
Figure 24.18 shows the Structure of CFIDCRn Register (n = 0 or 1).

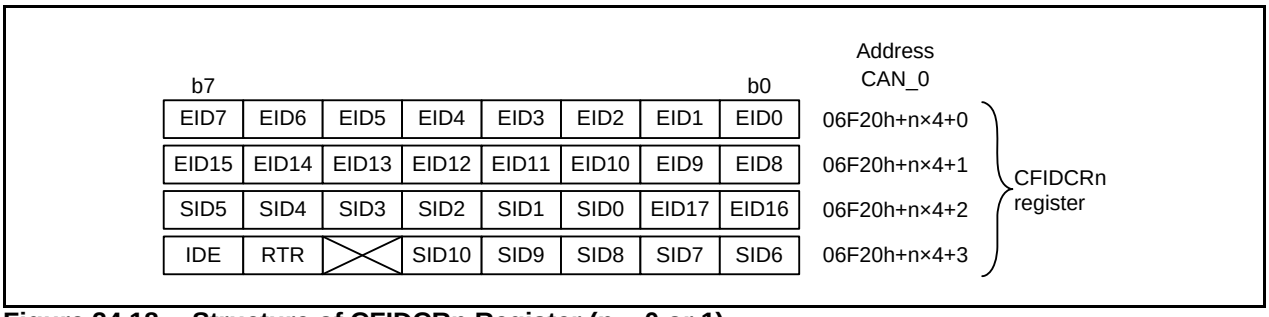


Figure 24.18 Structure of CFIDCRn Register (n = 0 or 1)

24.6 Acceptance Filtering and Masking Function

Acceptance filtering allows the user to receive messages with a specified range of multiple IDs for mailboxes.
Registers CMKR0 to CMKR3 can perform masking of the standard ID and the extended ID of 29 bits.

- The CMKR0 register corresponds to mailboxes [0] to [3].
- The CMKR1 register corresponds to mailboxes [4] to [7].
- The CMKR2 register corresponds to mailboxes [8] to [11] in normal mailbox mode, and receive FIFO mailboxes [12] to [15] in FIFO mailbox mode.
- The CMKR3 register corresponds to mailboxes [12] to [15] in normal mailbox mode, and receive FIFO mailboxes [12] to [15] in FIFO mailbox mode.

The CMKIVLR register disables acceptance filtering individually for each mailbox.

The IDE bit in the CMBj register (j = 0 to 15) is enabled when bits IDFM1 and IDFM0 in the CCTLR register are 10b (mixed ID mode).
The RTR bit in the CMBj register selects a data frame or a remote frame.

In FIFO mailbox mode, normal mailboxes (mailboxes [0] to [7]) use the single corresponding register among registers CMKR0 and CMKR1 for acceptance filtering. Receive FIFO mailboxes (mailboxes [12] to [15]) use two registers CMKR2 and CMKR3 for acceptance filtering.
Also, the receive FIFO uses two registers CFIDCR0 and CFIDCR1 for ID comparison. Bits EID, SID, RTR, and IDE in registers CMB12 to CMB15 for the receive FIFO are disabled. As acceptance filtering depends on the result of two ID-mask sets, two ranges of IDs can be received into the receive FIFO.
The CMKIVLR register is disabled for the receive FIFO.

If both setting of standard ID and extended ID are set in the IDE bits in registers CFIDCR0 and CFIDCR1 individually, both ID formats are received.
If both setting of data frame and remote frame are set in the RTR bits in registers CFIDCR0 and CFIDCR1 individually, both data and remote frames are received.
When a combination of two ranges of IDs is not necessary, set the same mask value and the same ID into both of the FIFO ID/mask register sets.

Figure 24.19 shows the Correspondence of Mask Registers to Mailboxes and Figure 24.20 shows the Acceptance Filtering (j = 0 to 15; k = 0 to 3).

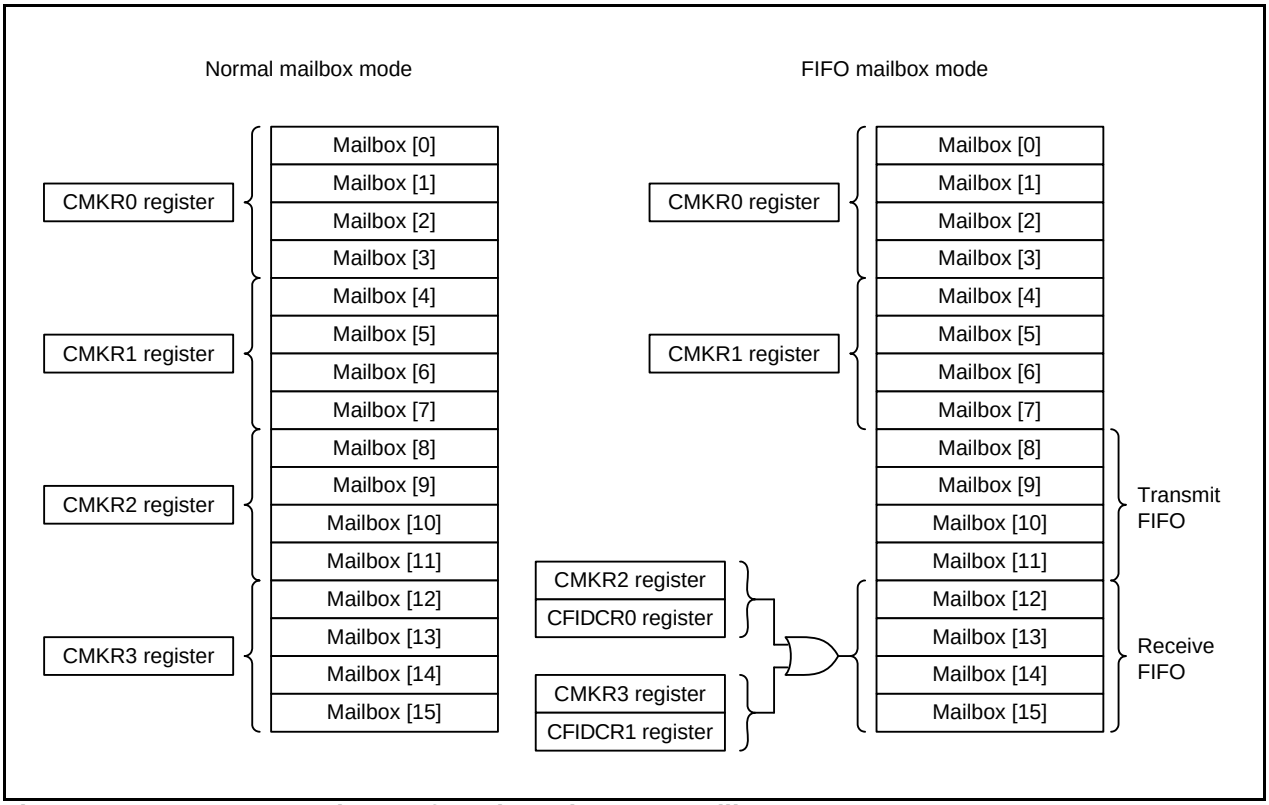


Figure 24.19 Correspondence of Mask Registers to Mailboxes

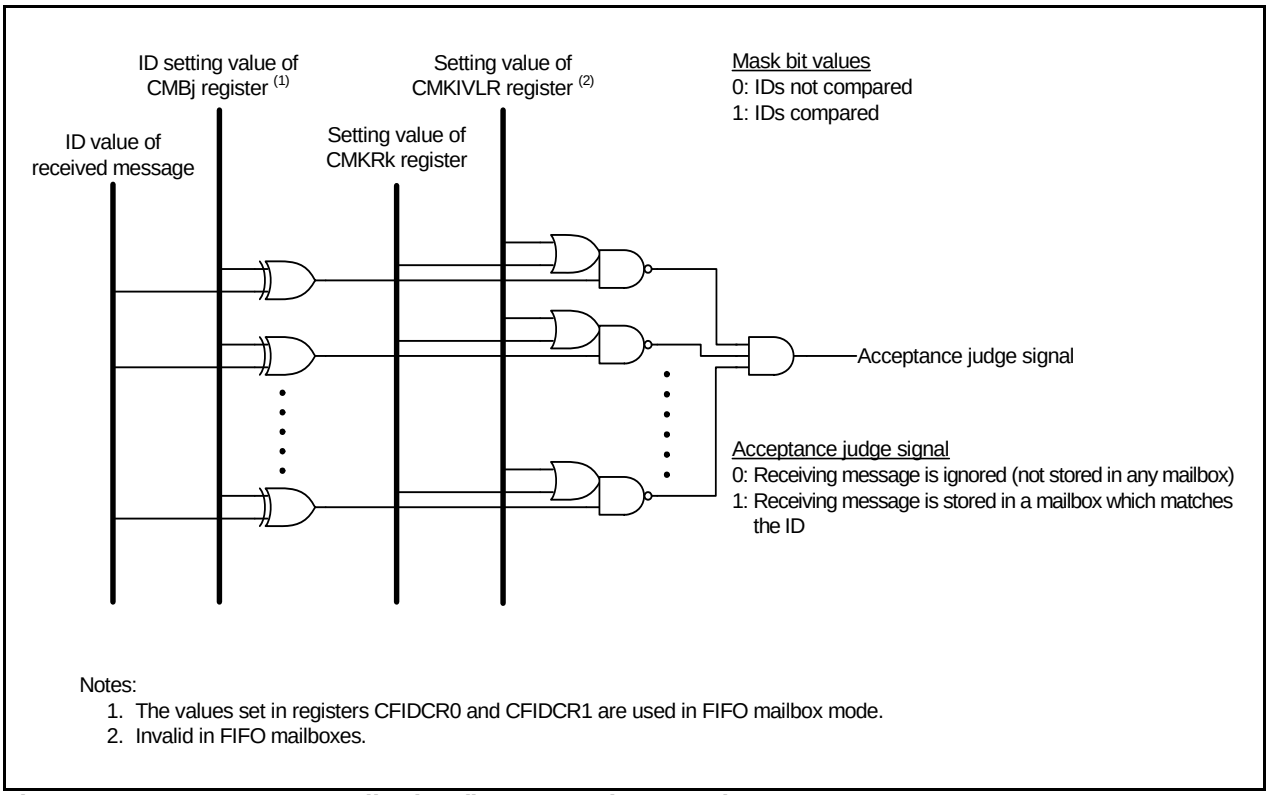


Figure 24.20 Acceptance Filtering (j = 0 to 15; k = 0 to 3)

24.7 Reception and Transmission

Table 24.13 list the Configuration for CAN Reception Mode and Transmission Mode.

Table 24.13 Configuration for CAN Reception Mode and Transmission Mode

TRMREQ	RECREQ	ONESHOT	Communication mode of mailbox
0	0	0	Mailbox disabled or transmission being aborted.
0	0	1	Configurable only when transmission or reception from a mailbox (programmed in one-shot mode) is aborted.
0	1	0	Configured as a receive mailbox for a data frame or a remote frame.
0	1	1	Configured as a one-shot receive mailbox for a data frame or a remote frame.
1	0	0	Configured as a transmit mailbox for a data frame or a remote frame.
1	0	1	Configured as a one-shot transmit mailbox for a data frame or a remote frame.
1	1	0	Do not set.
1	1	1	Do not set.

TRMREQ, RECREQ, ONESHOT: Bits in CMCTLj register (j = 0 to 15)

When a mailbox is configured as a receive mailbox or a one-shot receive mailbox, note the following:

(1) Before a mailbox is configured as a receive mailbox or a one-shot receive mailbox, set the CMCTLj register (j = 0 to 15) to 00h.

(2) A received message is stored into the first mailbox that matches the condition according to the result of receive mode configuration and acceptance filtering. Upon deciding a mailbox which stores the received message, the mailbox with the smaller number has higher priority.

(3) In CAN operation mode, when a CAN module transmits a message whose ID matches with the ID/ mask set of a mailbox configured to receive messages, the CAN module never receives the transmitted data. In self-test mode, however, the CAN module may receive its transmitted data. In this case, the CAN module sends an ACK.

When configuring a mailbox as a transmit mailbox or a one-shot transmit mailbox, note the following:

(1) Before a mailbox is configured as a transmit mailbox or one-shot transmit mailbox, ensure that the CMCTLj register is 00h and that there is no pending abort process.

24.7.1 Reception

Figure 24.21 shows the Operation Example of Data Frame Reception in Overwrite Mode (j = 0 to 15).
This example shows the operation of overwriting the first message when the CAN module receives two consecutive CAN messages that match the receiving conditions of the CMCTL0 register.

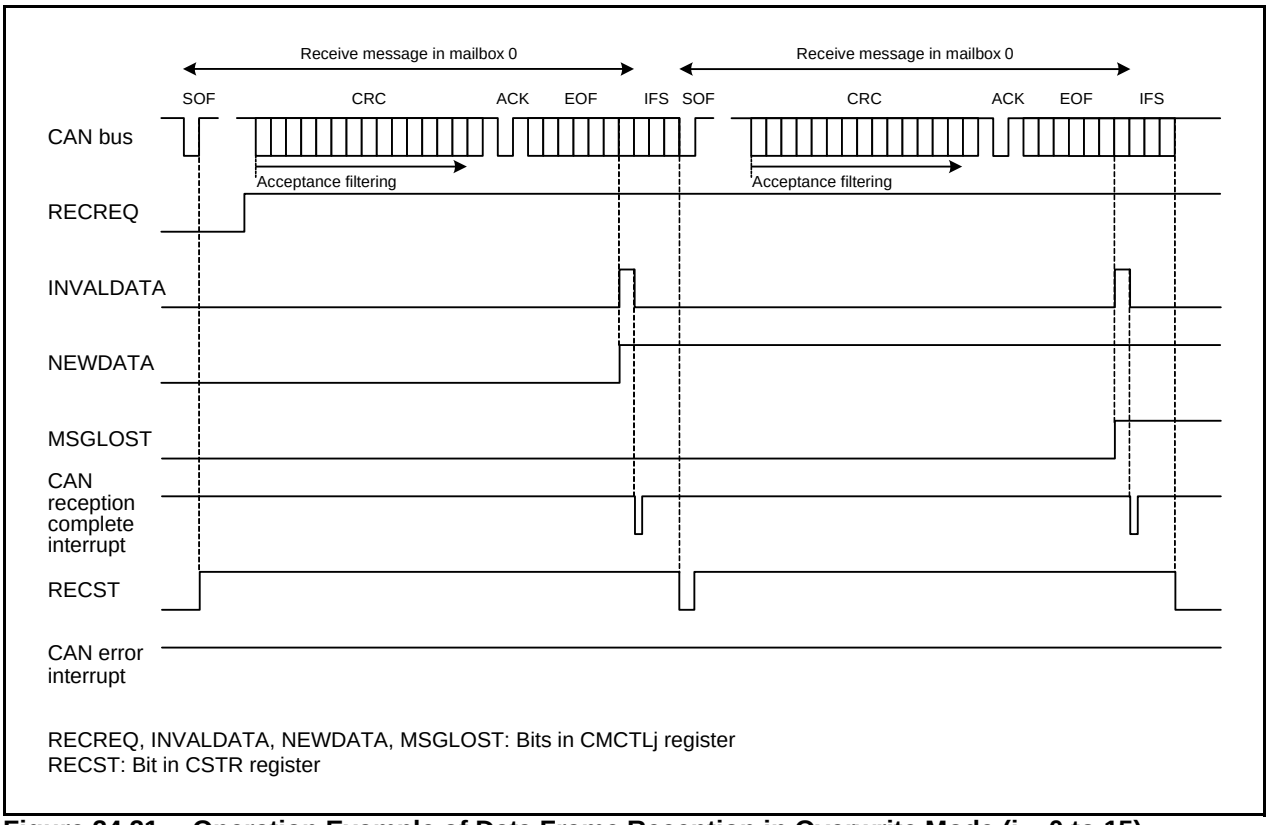


Figure 24.21 Operation Example of Data Frame Reception in Overwrite Mode (j = 0 to 15)

(1) When a SOF is detected on the CAN bus, the RECST bit in the CSTR registers set to 1 (reception in progress) if the CAN module has no message ready to start transmission.
(2) The acceptance filter procedure starts at the beginning of the CRC field to select the receive mailbox.
(3) After a message has been received, the NEWDATA bit in the CMCTLj register (j = 0 to 15) for the receive mailbox is set to 1 (new data being updated/stored in the mailbox). The INVALDATA bit in the CMCTLj register is set to 1 (message is being updated) at the same time, and then the INVALDATA bit is set to 0 (message valid) again after the complete message is transferred to the mailbox.
(4) When the interrupt enable bit in the CMIER register for the receive mailbox is 1 (interrupt enabled), the CAN reception complete interrupt request is generated. This interrupt is generated when the INVALDATA bit is set to 0.
(5) After reading the message from the mailbox, the NEWDATA bit needs to be set to 0 by a program.
(6) In overwrite mode, if the next CAN message has been received in a mailbox whose NEWDATA bit is still set to 1, the MSGLOST bit in the CMCTLj register is set to 1 (message has been overwritten). The new received message is transferred to the mailbox. The CAN reception complete interrupt request is generated the same as in (4).

Figure 24.22 shows the Operation Example of Data Frame Reception in Overrun Mode (j = 0 to 15).
This example shows the operation of overrunning the second message when the CAN module receives two consecutive CAN messages that match the receiving conditions of the CMCTL0 register.

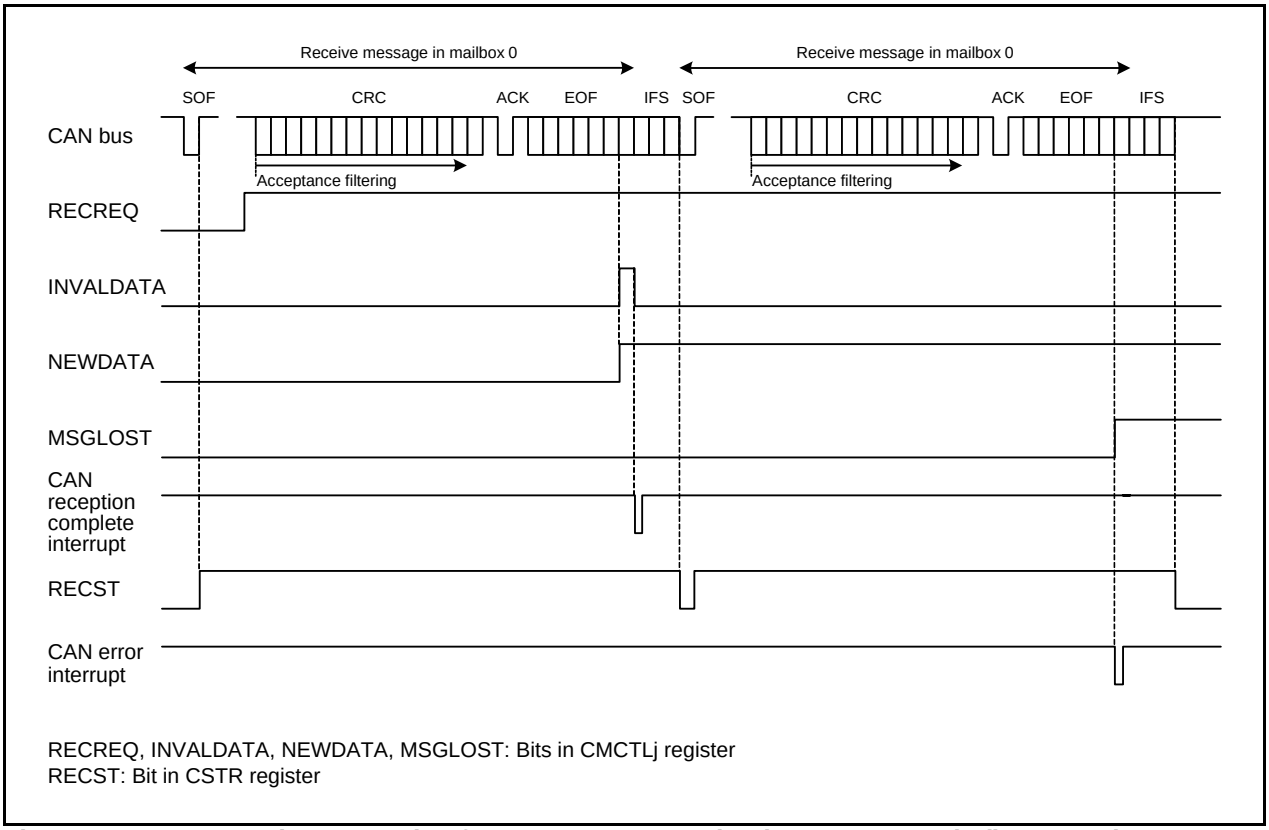


Figure 24.22 Operation Example of Data Frame Reception in Overrun Mode (j = 0 to 15)

(1) to (5) are same as overwrite mode.

(6) In overrun mode, if the next message has been received before the NEWDATA bit is set to 0, the MSGLOST bit in the CMCTLj register (j = 0 to 15) is set to 1 (message has been overrun). The new received message is discarded and a CAN error interrupt request is generated if the corresponding interrupt enable bit in the CEIER register is set to 1 (interrupt enabled).

24.7.2 Transmission

Figure 24.23 shows the Operation Example of Data Frame Transmission (j = 0 to 15). This example shows the operation of transmitting messages that has been set in registers CMCTL0 and CMCTL1.

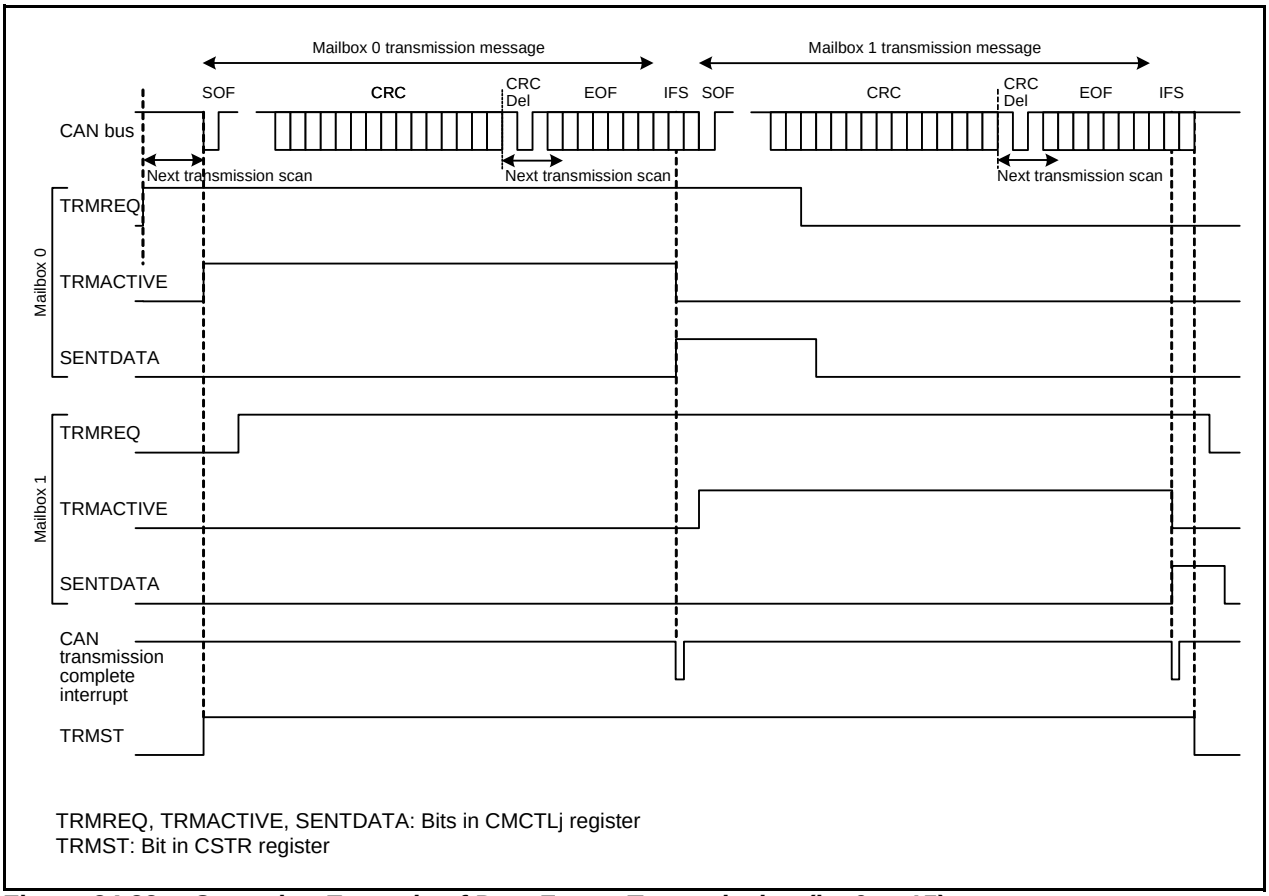


Figure 24.23 Operation Example of Data Frame Transmission (j = 0 to 15)

(1) When a TRMREQ bit in the CMCTLj register (j = 0 to 15) is set to 1 (transmit mailbox) in bus-idle state, the mailbox scan procedure starts to decide the highest-priority mailbox for transmission. Once the transmit mailbox is decided, the TRMACTIVE bit in the CMCTLj register is set to 1 (from when a transmission request is received until transmission is completed, or an error/arbitration lost has occurred), the TRMST bit in the CSTR register is set to 1 (transmission in progress), and the CAN module starts transmission. (1)

(2) If other TRMREQ bits are set, the transmission scan procedure starts with the CRC delimiter for the next transmission.

(3) If transmission is completed without losing arbitration, the SENTDATA bit in the CMCTLj register is set to 1 (transmission completed) and the TRMACTIVE bit is set to 0 (transmission is pending, or no transmission request). If the interrupt enable bit in the CMIER register is 1 (interrupt enabled), a CAN transmission complete interrupt request is generated.

(4) When requesting the next transmission from the same mailbox, set bits SENDTDATA and TRMREQ to 0, then set the TRMREQ bit to 1 after checking that bits SENDTDATA and TRMREQ have been set to 0.

Note:

1. If arbitration is lost after the CAN module starts transmission, the TRMACTIVE bit is set to 0. The transmission scan procedure is performed again to search for the highest-priority transmit mailbox from the beginning of the CRC delimiter. If an error occurs either during transmission or following the loss of arbitration, the transmission scan procedure is performed again from the start of the error delimiter to search for the highest-priority transmit mailbox.

24.8 CAN Interrupt

The following six types of interrupt requests can be generated. The interrupt sources for each interrupt can be determined by checking the CAN interrupt status register.

- CAN reception complete interrupt
- CAN transmission complete interrupt
- CAN receive FIFO interrupt
- CAN transmit FIFO interrupt
- CAN error interrupt
- CAN wake-up interrupt

Each interrupt source is bundled for the following sources and used as a source for peripheral function interrupts.

(1) CAN reception complete interrupt and CAN receive FIFO interrupt are used as the CAN receive interrupts for peripheral function interrupts.

(2) CAN transmission complete interrupt and CAN transmit FIFO interrupt are used as the CAN transmit interrupts for peripheral function interrupts.

(3) CAN error interrupt and CAN wake-up interrupt are used as the CAN error interrupts for peripheral function interrupts.
After an interrupt is generated, determine whether it is a CAN error interrupt or a CAN wake-up interrupt using bits ERR and WKUP in the CANISR register.

There are eight types of interrupt sources for the CAN error interrupts. These sources can be determined by checking the CEIFR register.

- Bus error
- Error warning
- Error passive
- Bus-off entry
- Bus-off recovery
- Reception overrun
- Overload frame transmission
- Bus lock

25. A/D Converter

The A/D converter consists of one 10-bit successive approximation A/D converter circuit with a capacitive coupling amplifier. The analog inputs, AN0 to AN11, share pins P0_0 to P0_7 and P1_0 to P1_3.

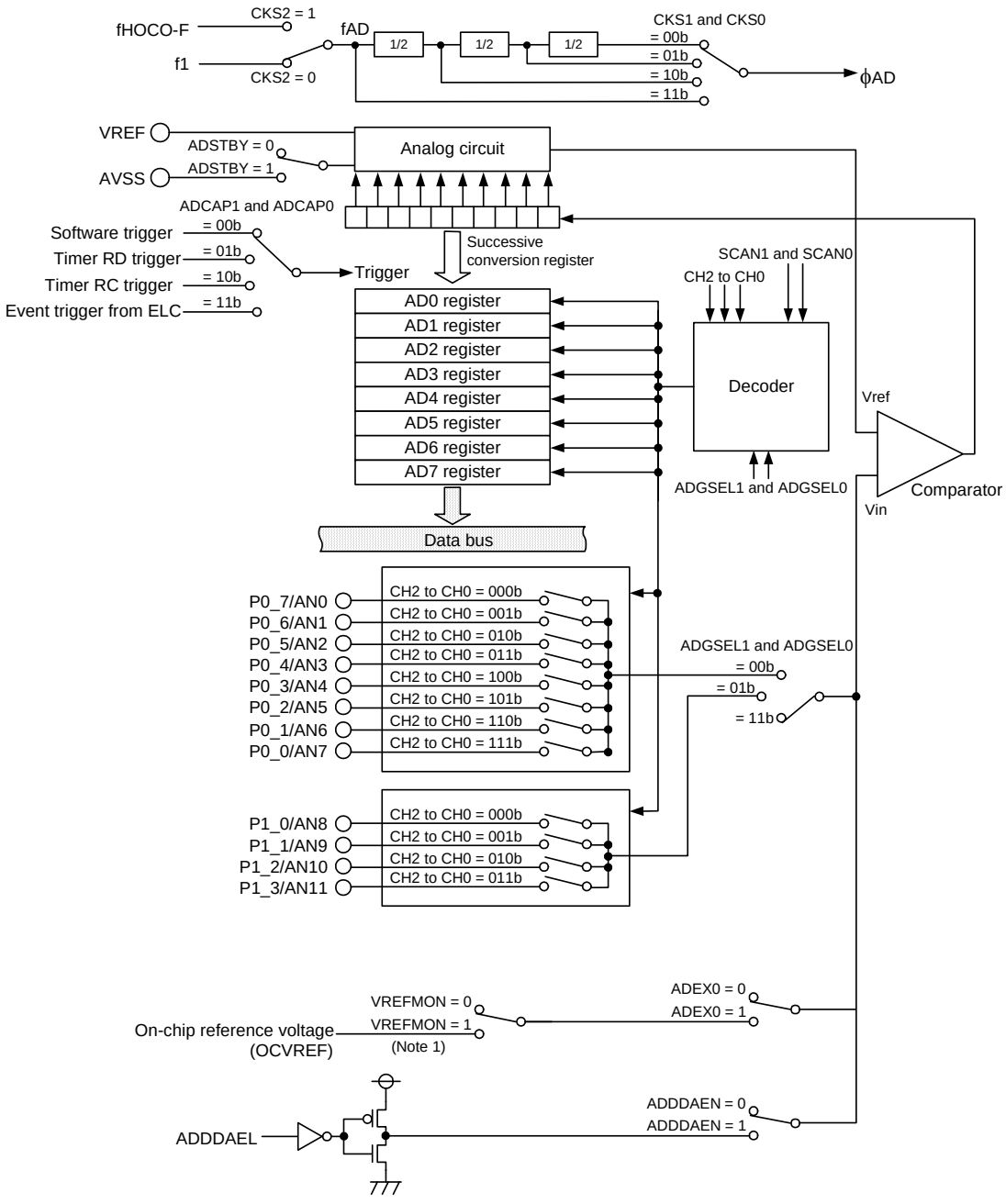
25.1 Overview

Table 25.1 lists the A/D Converter Performance. Figure 25.1 shows the A/D Converter Block Diagram.

Table 25.1 A/D Converter Performance

Item	Performance
A/D conversion method	Successive approximation (with capacitive coupling amplifier)
Analog input voltage (1)	0 V to AVCC
Operating clock ϕAD (2)	fAD, fAD divided by 2, fAD divided by 4, fAD divided by 8 (fAD = f1 or fHOCO-F)
Resolution	8 bits or 10 bits selectable
Absolute accuracy	AVCC = Vref = 5 V, ϕAD = 20 MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±3 LSB AVCC = Vref = 3.0 V, ϕAD = 10 MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±5 LSB
Operating mode	One-shot mode, repeat mode 0, repeat mode 1, single sweep mode, and repeat sweep mode
Analog input pin	12 pins (AN0 to AN11)
A/D conversion start condition	• Software trigger • Timer RD • Timer RC • Event input trigger from event link controller (ELC) (Refer to **25.3.3 A/D Conversion Start Condition**)
Conversion rate per pin (3) (ϕAD = fAD)	Minimum 44 ϕAD cycles

Notes:
1. When the analog input voltage exceeds the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.
2. Refer to **Table 30.5 A/D Converter Characteristics** for the operating clock ϕAD.
3. The conversion rate per pin is a minimum of 44 ϕAD cycles for 8-bit and 10-bit resolution.



CKS0 to CKS2, ADCAP0, ADCAP1: Bits in ADMOD register
CH0 to CH2, SCAN0, SCAN1, ADGSEL0, ADGSEL1: Bits in ADINSEL register
ADEX0, ADSTBY, ADDDAEN, ADDDAEL: Bits in ADCON1 register
VREFMON: Bit in OCVREFCR register

Note:
1. When the on-chip reference voltage is used as analog input, first set the ADEX0 bit to 1 (on-chip reference voltage selected) and then set the VREFMON bit to 1 (on-chip reference voltage and analog input are connected).
When the on-chip reference voltage is not used as analog input, first set the VREFMON bit to 0 (on-chip reference voltage and analog input are cut off) and then set the ADEX0 bit to 0 (extended analog input pin not selected).

Figure 25.1 A/D Converter Block Diagram

Table 25.2 A/D Converter Pin Configuration

Pin Name	I/O	Function
AVCC	Input	Power supply input for the analog block
AVSS	Input	Ground input for the analog block
AN0	Input	Analog input for port P0 group
AN1	Input	
AN2	Input	
AN3	Input	
AN4	Input	
AN5	Input	
AN6	Input	
AN7	Input	
AN8	Input	Analog input for port P1 group
AN9	Input	
AN10	Input	
AN11	Input	

25.2 Registers

Table 25.3 lists the A/D Converter Register Configuration.

Table 25.3 A/D Converter Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
On-Chip Reference Voltage Control Register	OCVREFCR	00h	00032h	8
A/D Register 0	AD0	00h	00200h	8 or 16 (1)
		00h	00201h	
A/D Register 1	AD1	00h	00202h	8 or 16 (1)
		00h	00203h	
A/D Register 2	AD2	00h	00204h	8 or 16 (1)
		00h	00205h	
A/D Register 3	AD3	00h	00206h	8 or 16 (1)
		00h	00207h	
A/D Register 4	AD4	00h	00208h	8 or 16 (1)
		00h	00209h	
A/D Register 5	AD5	00h	0020Ah	8 or 16 (1)
		00h	0020Bh	
A/D Register 6	AD6	00h	0020Ch	8 or 16 (1)
		00h	0020Dh	
A/D Register 7	AD7	00h	0020Eh	8 or 16 (1)
		00h	0020Fh	
A/D Mode Register	ADMOD	00h	00214h	8
A/D Input Select Register	ADINSEL	11000000b	00215h	8
A/D Control Register 0	ADCON0	00h	00216h	8
A/D Control Register 1	ADCON1	00h	00217h	8

Note:
1. For details on access, refer to the description of the individual registers.

25.2.1 On-Chip Reference Voltage Control Register (OCVREFCR)

Address 00032h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	VREFMON
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VREFMON	On-chip reference voltage to analog input connect bit (1)	0: On-chip reference voltage and analog input are cut off 1: On-chip reference voltage and analog input are connected	R/W
b1	—	Reserved	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:

1. When the on-chip reference voltage is used as an analog input, first set the ADEX0 bit in the ADCON1 register to 1 (on-chip reference voltage selected) and then set the VREFMON bit to 1 (on-chip reference voltage and analog input are connected).
   When the on-chip reference voltage is not used as an analog input, first set the VREFMON bit to 0 (on-chip reference voltage and analog input are cut off) and then set the ADEX0 bit to 0 (extended analog input pin not selected).

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the OCVREFCR register.
If the contents of the OCVREFCR register are rewritten during A/D conversion, the conversion result is undefined.

25.2.2 A/D Register i (ADi) (i = 0 to 7)

Address 00200h (AD0), 00202h (AD1), 00204h (AD2), 00206h (AD3), 00208h (AD4), 0020Ah (AD5), 0020Ch (AD6), 0020Eh (AD7)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	AD9	AD8
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function		R/W
		10-Bit Mode (BITS Bit in ADCON1 Register = 1)	8-Bit Mode (BITS Bit in ADCON1 Register = 0)	
b0	AD0	8 low-order bits of A/D conversion result	A/D conversion result	R
b1	AD1			R
b2	AD2			R
b3	AD3			R
b4	AD4			R
b5	AD5			R
b6	AD6			R
b7	AD7			R
b8	AD8	2 high-order bits of A/D conversion result	The read value is 0.	R
b9	AD9			R
b10	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b11	—			
b12	—			
b13	—			
b14	—			
b15	—			

If the contents of the ADCON1, ADMOD, ADINSEL, or OCVREFCR register are written during A/D conversion, the conversion result is undefined.
When using the A/D converter in 10-bit mode, repeat mode 0, repeat mode 1, or repeat sweep mode, access the ADi register in 16-bit units. Do not access it in 8-bit units.

25.2.3 A/D Mode Register (ADMOD)

Address 00214h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADCAP1	ADCAP0	MD2	MD1	MD0	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Division select bits	b1 b0 0 0: fAD divided by 8 0 1: fAD divided by 4 1 0: fAD divided by 2 1 1: fAD divided by 1 (no division)	R/W
b1	CKS1			R/W
b2	CKS2	Clock source select bit (1)	0: f1 selected 1: fHOCO-F selected	R/W
b3	MD0	A/D operating mode select bits (2)	b5 b4 b3 0 0 0: One-shot mode 0 0 1: Do not set. 0 1 0: Repeat mode 0 0 1 1: Repeat mode 1 1 0 0: Single sweep mode 1 0 1: Do not set. 1 1 0: Repeat sweep mode 1 1 1: Do not set.	R/W
b4	MD1			R/W
b5	MD2			R/W
b6	ADCAP0	A/D conversion trigger select bits	b7 b6 0 0: A/D conversion is started by software trigger (ADST bit in ADCON0 register) 0 1: A/D conversion is started by conversion trigger from timer RD 1 0: A/D conversion is started by conversion trigger from timer RC 1 1: A/D conversion is started by event input trigger from ELC	R/W
b7	ADCAP1			R/W

Notes:
1. Stop A/D conversion before switching the clock source. After the CKS2 bit has been changed, allow two or more cycles of the fHOCO-F clock to elapse before starting A/D conversion.
2. When performing A/D conversion in single sweep mode or repeat sweep mode, set bits CH2 to CH0 in the ADINSEL register to 000b.

If the ADMOD register is rewritten during A/D conversion, the conversion result is undefined.

CKS2 Bit (Clock source select bit)

This bit is used to select the fAD clock to be used by the A/D converter.

25.2.4 A/D Input Select Register (ADINSEL)

Address 00215h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADGSEL1	ADGSEL0	SCAN1	SCAN0	—	CH2	CH1	CH0
After Reset	1	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CH0	Analog input pin select bits (1)	Refer to **Table 25.4 Analog Input Pin Selection**	R/W
b1	CH1			R/W
b2	CH2			R/W
b3	—	Reserved	The write value must be 0. The read value is 0.	R/W
b4	SCAN0	A/D sweep pin count select bits	b5 b4 0 0: 2 pins 0 1: 4 pins 1 0: 6 pins 1 1: 8 pins	R/W
b5	SCAN1			R/W
b6	ADGSEL0	A/D input group select bits	b7 b6 0 0: Port P0 group selected 0 1: Port P1 group selected 1 0: Do not set. 1 1: Port group not selected	R/W
b7	ADGSEL1			R/W

Note:
1. When performing A/D conversion in single sweep mode or repeat sweep mode, set bits CH2 to CH0 in the ADINSEL register to 000b.

If the ADINSEL register is rewritten during A/D conversion, the conversion result is undefined.

Table 25.4 Analog Input Pin Selection

Bits CH2 to CH0	Bits ADGSEL1 and ADGSEL0 = 00b	Bits ADGSEL1 and ADGSEL0 = 01b
000b	AN0	AN8
001b	AN1	AN9
010b	AN2	AN10
011b	AN3	AN11
100b	AN4	Do not set.
101b	AN5	
110b	AN6	
111b	AN7	

25.2.5 A/D Control Register 0 (ADCON0)

Address 00216h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	ADST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADST	A/D conversion start flag	0: A/D conversion stops 1: A/D conversion starts	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

ADST Bit (A/D conversion start flag)

[Condition for setting to 1]
When A/D conversion starts and while A/D conversion is in progress.
[Condition for setting to 0]
When A/D conversion ends if it is started by a software trigger in one-shot mode or single sweep mode.

The ADST bit operates as follows:

- If A/D conversion is started by a software trigger in one-shot mode, the ADST bit is set to 0 when A/D conversion ends.
- If A/D conversion is started by a software trigger in single sweep mode, the ADST bit is set to 0 when A/D conversion ends.
- When 1 is written to the ADST bit by a program, it is set to 1 (A/D conversion starts) after start processing time (refer to **Table 25.5 Number of Cycles for A/D Conversion Items**). Thus, if this bit is read immediately after 1 is written, it may be read as 0 (A/D conversion stops) (refer to Figure 25.2).
- If A/D conversion is forcibly stopped by writing 0 to the ADST bit, allow two or more cycles of the ϕAD clock for end processing before writing 1 to the ADST bit.

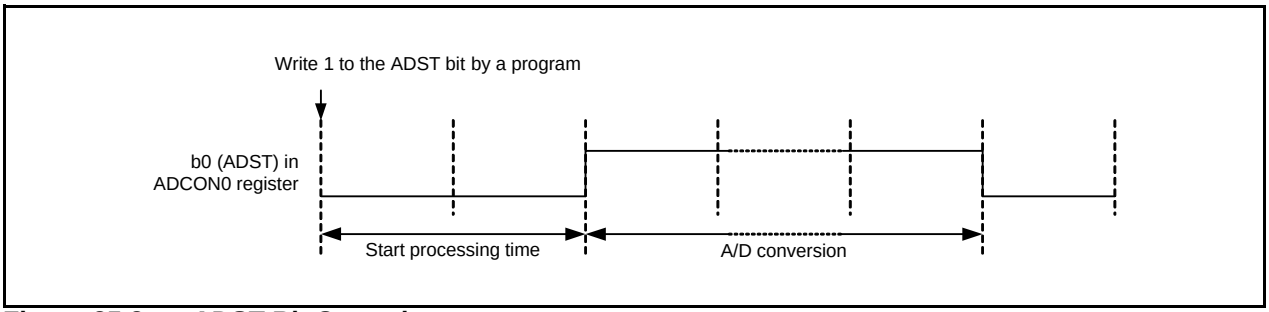


Figure 25.2 ADST Bit Operation

25.2.6 A/D Control Register 1 (ADCON1)

Address 00217h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADDDAEL	ADDDAEN	ADSTBY	BITS	—	—	—	ADEX0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADEX0	Extended analog input pin select bit (1)	0: Extended analog input pin not selected 1: On-chip reference voltage selected (2, 3, 4)	R/W
b1	—	Reserved	Set to 0.	R/W
b2	—			
b3	—			
b4	BITS	8/10-bit mode select bit	0: 8-bit mode 1: 10-bit mode	R/W
b5	ADSTBY	A/D standby bit (5)	0: A/D operation stops (standby) (8) 1: A/D operation enabled	R/W
b6	ADDDAEN	A/D open-circuit detection assist function enable bit (4, 6, 7)	0: Disabled 1: Enabled	R/W
b7	ADDDAEL	A/D open-circuit detection assist method select bit (6, 7)	0: Discharge before conversion 1: Precharge before conversion	R/W

Notes:

1. When the on-chip reference voltage is used as analog input, first set the ADEX0 bit to 1 (on-chip reference voltage selected) and then set the VREFMON bit in the OCVREFCR register to 1 (on-chip reference voltage and analog input are connected).
   When the on-chip reference voltage is not used as analog input, first set the VREFMON bit to 0 (on-chip reference voltage and analog input are cut off) and then set the ADEX0 bit to 0 (extended analog input pin not selected).
2. Do not set to 1 (on-chip reference voltage selected) in single sweep mode or repeat sweep mode.
3. When the ADEX0 bit is 1 (on-chip reference voltage selected), the settings of bits CH0 to CH2 in the ADINSEL register and bits ADGSEL0 and ADGSEL1 (analog input AN0 to AN11 selected) are disabled, and on-chip reference voltage is selected. When on-chip reference voltage is used, set bits CH2 to CH0 in the ADINSEL register to 000b.
   For details on the operation when 1 (on-chip reference voltage selected), refer to **25.3.7 On-Chip Reference Voltage (OCVREF)**.
4. When the on-chip reference voltage is used (ADEX0 = 1), set the ADDDAEN bit to 0 (A/D open-circuit detection assist function disabled).
5. When the ADSTBY bit is changed from 0 (A/D operation stops) to 1 (A/D operation enabled), wait for one ϕAD cycle or more before starting A/D conversion.
6. To enable the A/D open-circuit detection assist function, select the conversion start state with the ADDDAEL bit after setting the ADDDAEN bit to 1 (enabled).
   The conversion result with an open circuit varies according to external circuits. Careful evaluation should be performed according to the system before using this function.
7. When bits ADDDAEN and ADDDAEL are rewritten, allow at least one cycle of fAD to elapse before starting A/D conversion.
8. Stop the A/D function before setting to standby. When the ADSTBY bit is set to 0 (standby), any access to the A/D associated registers (addresses 00C0h to 00CFh, and 00D4h to 00D7h) is disabled. However, only the ADSTBY bit can be accessed in the ADCON1 register at address 00D7h.

If the ADCON1 register is rewritten during A/D conversion, the conversion result is undefined.

25.3 Items Common to Multiple Modes

25.3.1 Input/Output Pins

The analog inputs, AN0 to AN11, share pins P0_0 to P0_7 and P1_0 to P1_3.
When using the pins AN0 to AN11 as input, set the corresponding port direction bit to 0 (input mode).
After changing the A/D operating mode, the analog input pin must be selected again.

25.3.2 A/D Conversion Cycles

Figure 25.3 shows a Timing Diagram of A/D Conversion. Figure 25.4 shows the A/D Conversion Cycles (ϕAD = fAD).

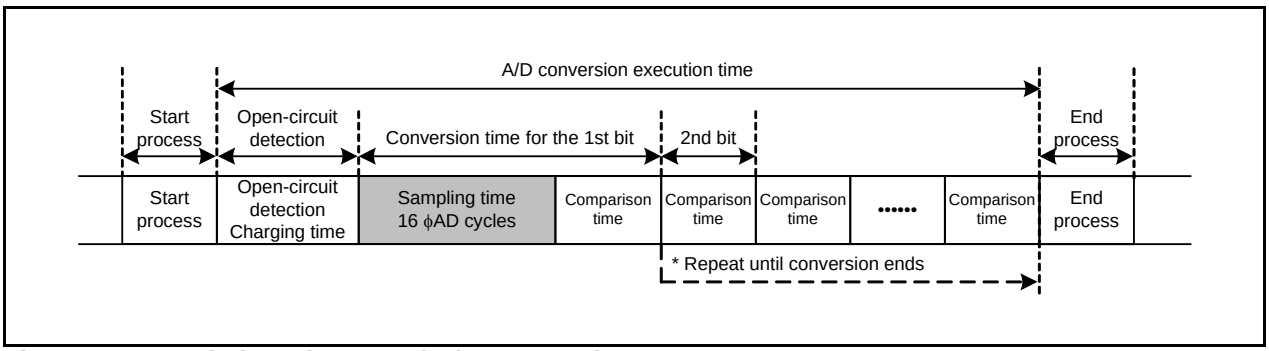
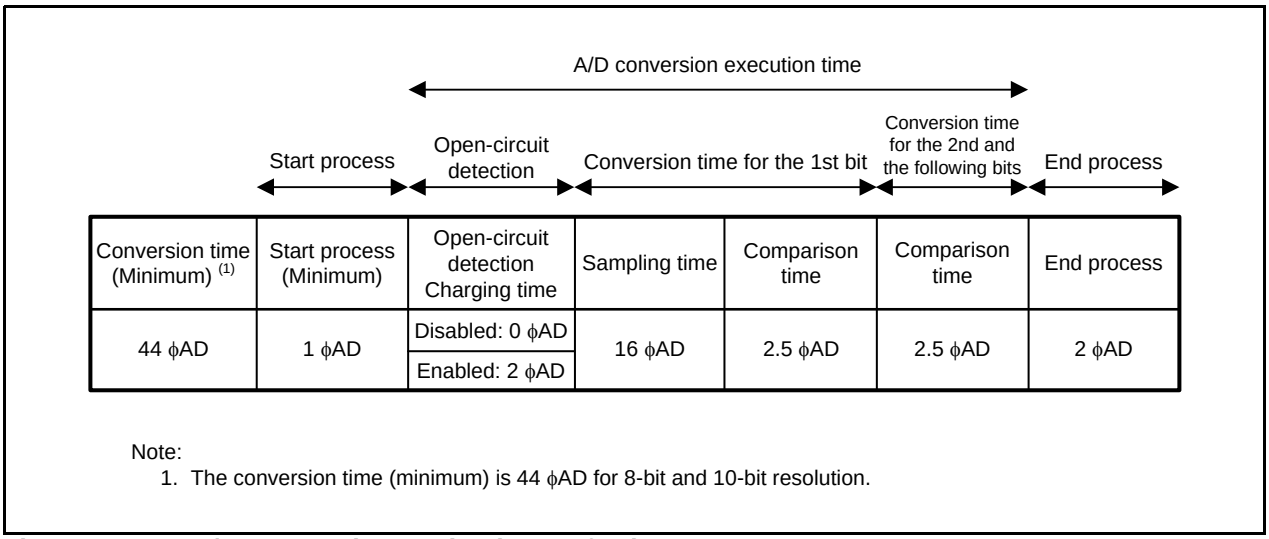


Figure 25.3 Timing Diagram of A/D Conversion



Conversion time (Minimum) (1)	Start process (Minimum)	Open-circuit detection Charging time	Sampling time	Comparison time	Comparison time	End process
44 ϕAD	1 ϕAD	Disabled: 0 ϕAD	16 ϕAD	2.5 ϕAD	2.5 ϕAD	2 ϕAD
		Enabled: 2 ϕAD				

Note:
1. The conversion time (minimum) is 44 ϕAD for 8-bit and 10-bit resolution.

Figure 25.4 A/D Conversion Cycles (ϕAD = fAD)

Table 25.5 lists the Number of Cycles for A/D Conversion Items. The A/D conversion time is defined as follows.
The start process time varies depending on which ϕAD is selected.
When 1 (A/D conversion starts) is written to the ADST bit in the ADCON0 register, an A/D conversion starts after the start process time has elapsed. Reading the ADST bit before the A/D conversion returns 0 (A/D conversion stops).
In the modes where an A/D conversion is performed on multiple pins or multiple times, the between-execution process time is inserted between the A/D conversion execution time for one pin and the next A/D conversion time.
In one-shot mode and single sweep mode, the ADST bit is set to 0 during the end process time and the last A/D conversion result is stored in the ADi register (i = 0 to 7).

- In one-shot mode
  Start process time + A/D conversion execution time + end process time

- When two pins are selected in single sweep mode
  Start process time + (A/D conversion execution time + between-execution process time + A/D conversion execution time) + end process time

Table 25.5 Number of Cycles for A/D Conversion Items

A/D Conversion Item		Number of Cycles
Start process time	ϕAD = fAD	1 or 2 fAD cycles
	ϕAD = fAD divided by 2	2 or 3 fAD cycles
	ϕAD = fAD divided by 4	3 or 4 fAD cycles
	ϕAD = fAD divided by 8	5 or 6 fAD cycles
A/D conversion execution time	Open-circuit detection disabled	40 ϕAD cycles + 1 to 3 fAD cycles
	Open-circuit detection enabled	42 ϕAD cycles + 1 to 3 fAD cycles
Between-execution process time		1 ϕAD cycle
End process time		2 or 3 fAD cycles

25.3.3 A/D Conversion Start Condition

A software trigger, trigger from timer RD or timer RC, and event input trigger from the event link controller (ELC) are used as A/D conversion start triggers.
Figure 25.5 shows the A/D Conversion Start Control Unit Block Diagram (j = A, B, C, or D; k = 0 or 1).

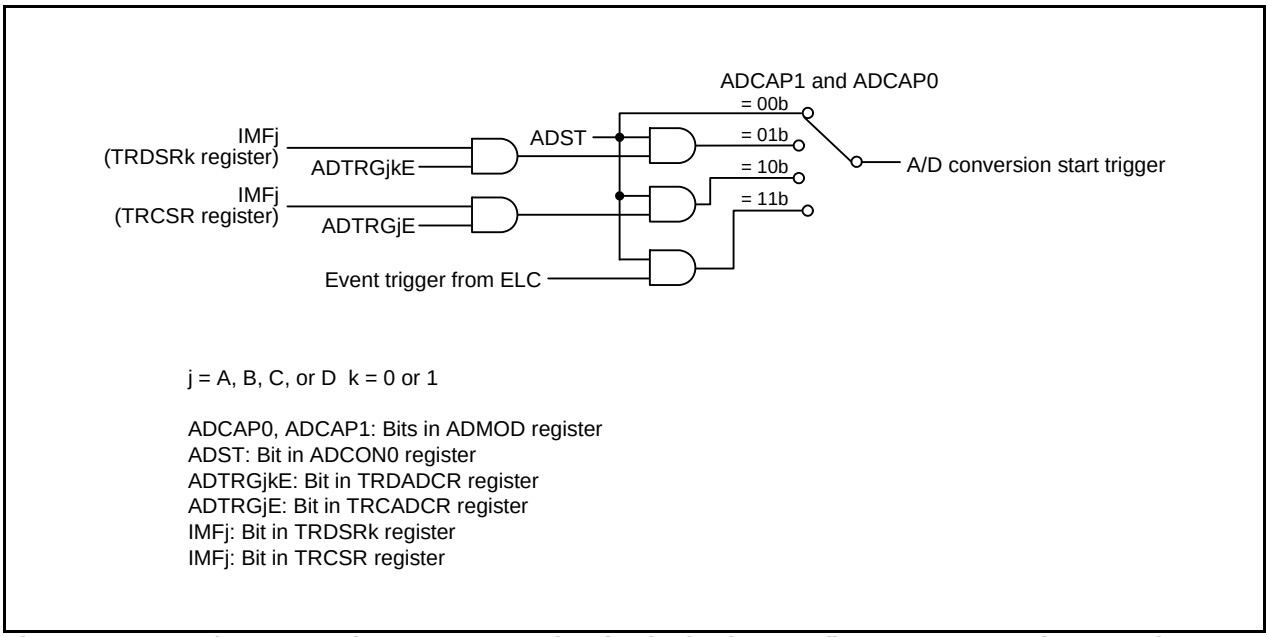


Figure 25.5 A/D Conversion Start Control Unit Block Diagram (j = A, B, C, or D; k = 0 or 1)

25.3.3.1 Software Trigger

A software trigger is selected when bits ADCAP1 and ADCAP0 in the ADMOD register are set to 00b (software trigger).
The A/D conversion starts when the ADST bit in the ADCON0 register is set to 1 (A/D conversion starts).

25.3.3.2 Trigger from Timer RD

This trigger is selected when bits ADCAP1 and ADCAP0 in the ADMOD register are set to 01b (timer RD).
To use this function, the following conditions must be met:

- Bits ADCAP1 and ADCAP0 in the ADMOD register are set to 01b (timer RD).
- Timer RD is used in the output compare function (timer mode, PWM mode, reset synchronous PWM mode, complementary PWM mode, or PWM3 mode).
- The ADTRGjkE bit (j = A, B, C, or D, k = 0 or 1) in the TRDADCR register is set to 1 (A/D trigger occurs at compare match with TRDGRjk register).
- The ADST bit in the ADCON0 register is set to 1 (A/D conversion starts).

When the IMFj bit in the TRDSRk register is changed from 0 to 1, A/D conversion starts.
Refer to **18. Timer RD**, **18.3.3 Output Compare Function**, **18.3.4 PWM Mode**, **18.3.5 Reset Synchronous PWM Mode**, **18.3.6 Complementary PWM Mode**, and **18.3.7 PWM3 Mode** for the details on timer RD and the output compare function (timer mode, PWM mode, reset synchronous PWM mode, complementary PWM mode, and PWM3 mode).

25.3.3.3 Trigger from Timer RC

This trigger is selected when bits ADCAP1 and ADCAP0 in the ADMOD register are set to 10b (timer RC).
To use this function, the following conditions must be met:

- Bits ADCAP1 and ADCAP0 in the ADMOD register are set to 10b (timer RC).
- Timer RC is used in the output compare function (timer mode, PWM mode, PWM2 mode).
- The ADTRGjE bit (j = A, B, C, D) in the TRCADCR register is set to 1 (A/D trigger occurs at compare match with TRCGRj register).
- The ADST bit in the ADCON0 register is set to 1 (A/D conversion starts).

When the IMFj bit in the TRCSR register is changed from 0 to 1, A/D conversion starts.
Refer to **17. Timer RC**, **17.3.1 Timer Mode**, **17.3.2 PWM Mode**, and **17.3.3 PWM2 Mode** for details on timer RC and the output compare function (timer mode, PWM mode, and PWM2 mode).

25.3.3.4 Event Input Trigger from Event Link Controller (ELC)

When bits ADCAP1 and ADCAP0 in the ADMOD register are set to 11b (event input trigger from ELC), A/D conversion can be started by event input from the ELC.
An example using $\overline{\text{INT0}}$ as the A/D conversion start trigger is described below:

- Set the PMCSEL register to either standard pin assignment or communication function priority pin assignment.
- Set bits ADCAP1 and ADCAP0 in the ADMOD register to 11b.
- Set the INT0EN bit in the INTEN register to 1 ($\overline{\text{INT0}}$ input enabled), the INT0PL bit to 0 (one edge), and the INT0POL bit in the INTPOL register to 0 (falling edge selected).
- Set the PD4_5 bit in the PD4 register to 0 (input mode).
- Select the $\overline{\text{INT0}}$ digital filter using bits INT0F0 and INT0F1 in the INTF register.
- Set bits ELSEL3 to ELSEL0 in the ELSELR0 register to 0001b (A/D converter selected as link destination peripheral module)
- Set the ADST bit in the ADCON0 register to 1 (A/D conversion starts).

When the input to the $\overline{\text{INT0}}$ pin changes from high to low, A/D conversion starts.

25.3.4 A/D Conversion Result

The A/D conversion result is stored in the ADi register (i = 0 to 7). The register where the result is stored varies depending on the A/D operating mode used. Values cannot be written to the ADi register.
In repeat mode 0, no interrupt request is generated. After the first A/D conversion is completed, determine if the A/D conversion time has elapsed by a program.
In one-shot mode, repeat mode 1, single sweep mode, and repeat sweep mode, an interrupt request is generated at certain times, such as when an A/D conversion completes (the IR bit in the ADIC register is set to 1).
However, in repeat mode 1 and repeat sweep mode, A/D conversion continues after an interrupt request is generated. Read the ADi register before the next A/D conversion is completed, since at completion the ADi register is rewritten with the new value.
In one-shot mode and single sweep mode, when bits ADCAP1 and ADCAP0 in the ADMOD register is set to 00b (software trigger), the ADST bit in the ADCON0 register is used to determine whether the A/D conversion or sweep has completed.
During an A/D conversion operation, if the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program to forcibly terminate A/D conversion, the conversion result of the A/D converter is undefined. An A/D conversion interrupt request may be generated depending the timing when the ADST bit is written. When the ADST bit is set to 0 by a program, do not use the value of the ADi register or an A/D conversion interrupt. Disable A/D conversion interrupts before setting the ADST bit to 0.
During an A/D conversion operation, after the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program to forcibly end the conversion, allow at least two cycles of the ϕAD clock before writing 1 to the ADST bit to ensure time for end processing.

25.3.5 Resolution (8-Bit/10-Bit Mode)

Either 8 bits or 10 bits can be selected as the resolution of the A/D converter. 8-bit/10 bit mode can be selected by the BITS bit in the ADCON1 register.

25.3.6 Low-Current-Consumption Function

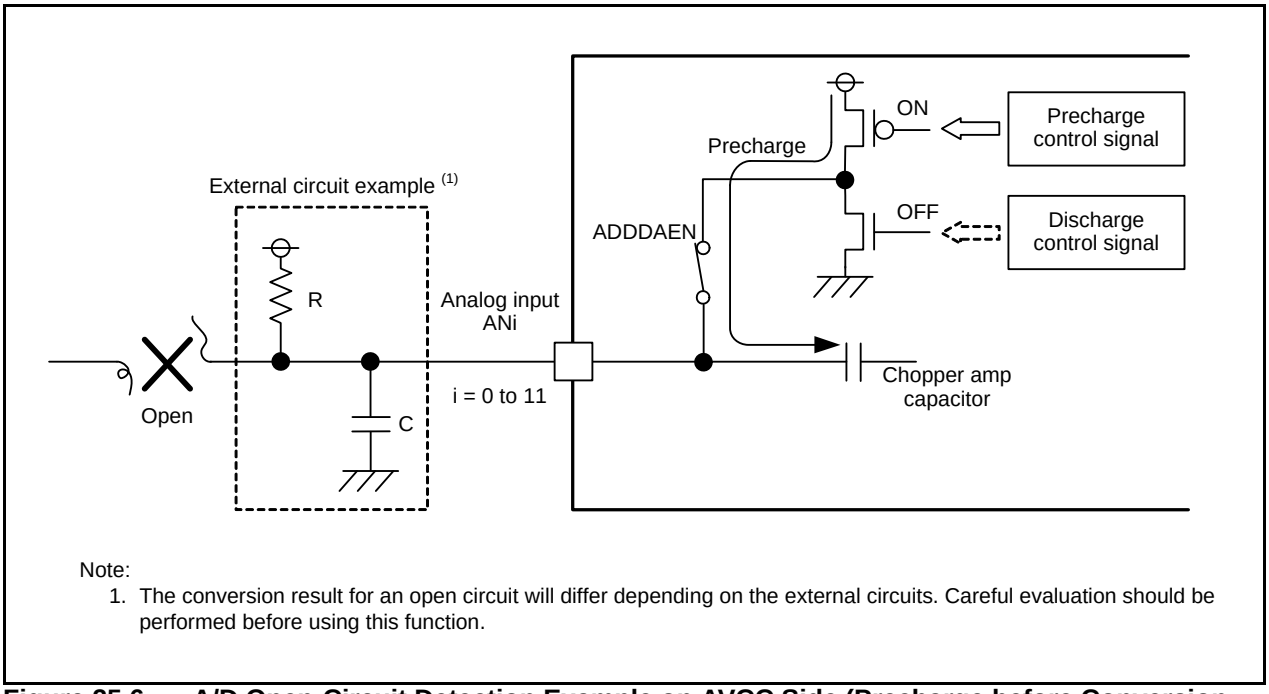
When the A/D converter is not used, power consumption can be reduced by setting the ADSTBY bit in the ADCON1 register to 0 (A/D operation stops (standby)) to shut off any analog circuit current flow.
To use the A/D converter, set the ADSTBY bit to 1 (A/D operation enabled) and wait for at least one ϕAD cycle before setting the ADST bit in the ADCON0 register to 1 (A/D conversion starts). Do not write 1 to bits ADST and ADSTBY at the same time.
Also, do not set the ADSTBY bit to 0 (A/D operation stops (standby)) during A/D conversion.

25.3.7 On-Chip Reference Voltage (OCVREF)

In one-shot mode, repeat mode 0, and repeat mode 1, the on-chip reference voltage (OCVREF) can be used as an analog input.
Any variation in VREF can be confirmed using the on-chip reference voltage.
Use the ADEX0 bit in the ADCON1 register and the VREFMON bit in the OCVREFCR register to select the on-chip reference voltage.
When setting the ADEX0 bit to 1, select bits CH2 to CH0 in the ADINSEL register to be 000b. The A/D conversion result of the on-chip reference voltage in repeat mode 1 is stored in one of registers AD0 to AD7, depending on the number of conversions.

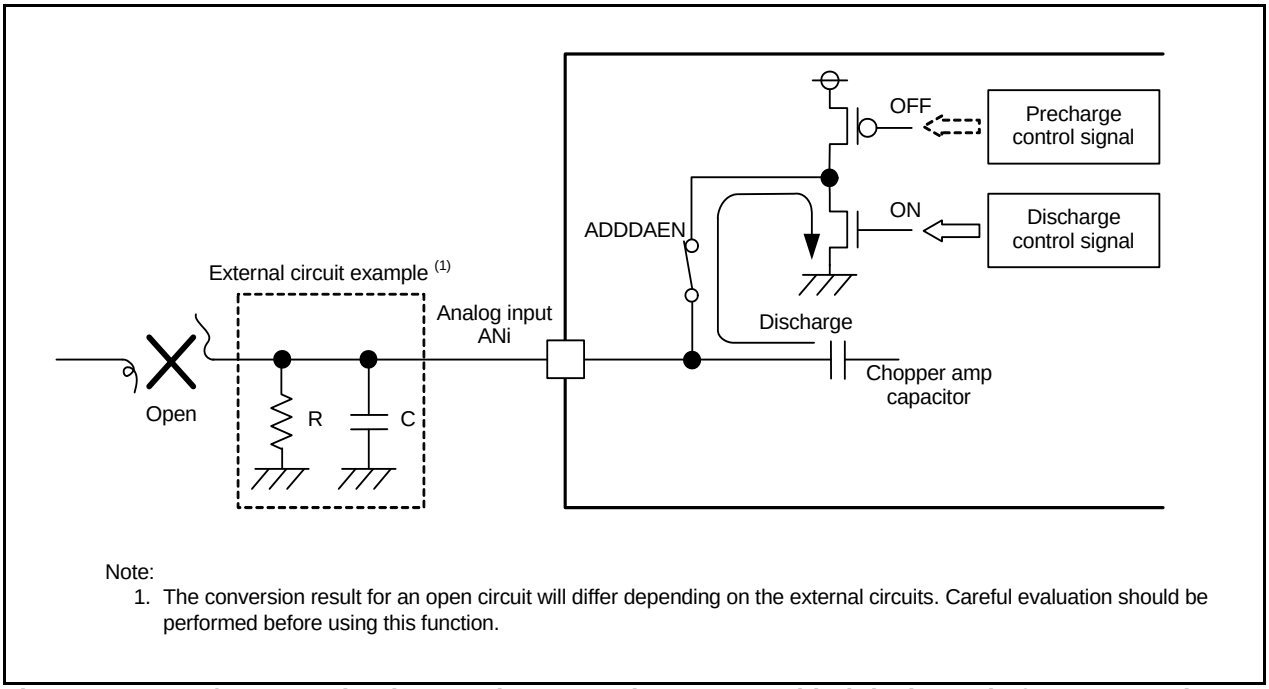
25.3.8 A/D Open-Circuit Detection Assist Function

To suppress influences of the analog input voltage leakage from the previously converted channel during A/D conversion operation, a function is provided that sets and holds the electric charge on the chopper amp capacitor to a predetermined state (AVCC or GND) before starting conversion.
This function enables more reliable detection of an open circuit in the wiring connected to the analog input pins.
Figure 25.6 shows the A/D Open-Circuit Detection Example on AVCC Side (Precharge before Conversion Selected) (i = 0 to 11) and Figure 25.7 shows the A/D Open-Circuit Detection Example on AVSS Side (Discharge before Conversion Selected) (i = 0 to 11).



Note:
1. The conversion result for an open circuit will differ depending on the external circuits. Careful evaluation should be performed before using this function.

Figure 25.6 A/D Open-Circuit Detection Example on AVCC Side (Precharge before Conversion Selected) (i = 0 to 11)



Note:
1. The conversion result for an open circuit will differ depending on the external circuits. Careful evaluation should be performed before using this function.

Figure 25.7 A/D Open-Circuit Detection Example on AVSS Side (Discharge before Conversion Selected) (i = 0 to 11)

25.4 One-Shot Mode

In one-shot mode, the input voltage to one pin selected from among AN0 to AN11 or OCVREF is A/D converted once.

Table 25.6 lists the One-Shot Mode Specifications.

Table 25.6 One-Shot Mode Specifications

Item	Specification
Function	The input voltage to the pin selected by bits CH0 to CH2 and bits ADGSEL0 and ADGSEL1 in the ADINSEL register or the ADEX0 bit in the ADCON1 register is A/D converted once. (1)
Resolution	8 bits or 10 bits
A/D conversion start condition	• Software trigger • Timer RD • Timer RC • Event input trigger from ELC (refer to **25.3.3 A/D Conversion Start Condition**)
A/D conversion stop condition	• A/D conversion completes (If bits ADCAP1 and ADCAP0 in the ADMOD register are set to 00b (software trigger), the ADST bit in the ADCON0 register is set to 0.) • Set the ADST bit to 0
Interrupt request generation timing	When A/D conversion completes
Analog input pin	One pin selectable from among AN0 to AN11 or OCVREF.
Storage resister for A/D conversion result	AD0 register: AN0, AN8, OCVREF AD1 register: AN1, AN9 AD2 register: AN2, AN10 AD3 register: AN3, AN11 AD4 register: AN4 AD5 register: AN5 AD6 register: AN6 AD7 register: AN7
Reading of result of A/D converter	Read the registers from AD0 to AD7 corresponding to the selected pin.

Note:

1. When setting the ADEX0 bit to 1 (on-chip reference voltage selected), set bits CH2 to CH0 in the ADINSEL register to 000b.

25.5 Repeat Mode 0

In repeat mode 0, the input voltage to one pin selected from among AN0 to AN11, or OCVREF is A/D converted repeatedly.
Table 25.7 lists the Repeat Mode 0 Specifications.

Table 25.7 Repeat Mode 0 Specifications

Item	Specification
Function	The input voltage to the pin selected by bits CH0 to CH2 and bits ADGSEL0 and ADGSEL1 in the ADINSEL register or the ADEX0 bit in the ADCON1 register is A/D converted repeatedly. (1)
Resolution	8 bits or 10 bits
A/D conversion start condition	• Software trigger • Timer RD • Timer RC • Event input trigger from ELC (refer to **25.3.3 A/D Conversion Start Condition**)
A/D conversion stop condition	Set the ADST bit in the ADCON0 register to 0
Interrupt request generation timing	Not generated
Analog input pin	One pin selectable from among AN0 to AN11, or OCVREF.
Storage resister for A/D conversion result	AD0 register: AN0, AN8, OCVREF AD1 register: AN1, AN9 AD2 register: AN2, AN10 AD3 register: AN3, AN11 AD4 register: AN4 AD5 register: AN5 AD6 register: AN6 AD7 register: AN7
Reading of result of A/D converter	Read the registers from AD0 to AD7 corresponding to the selected pin.

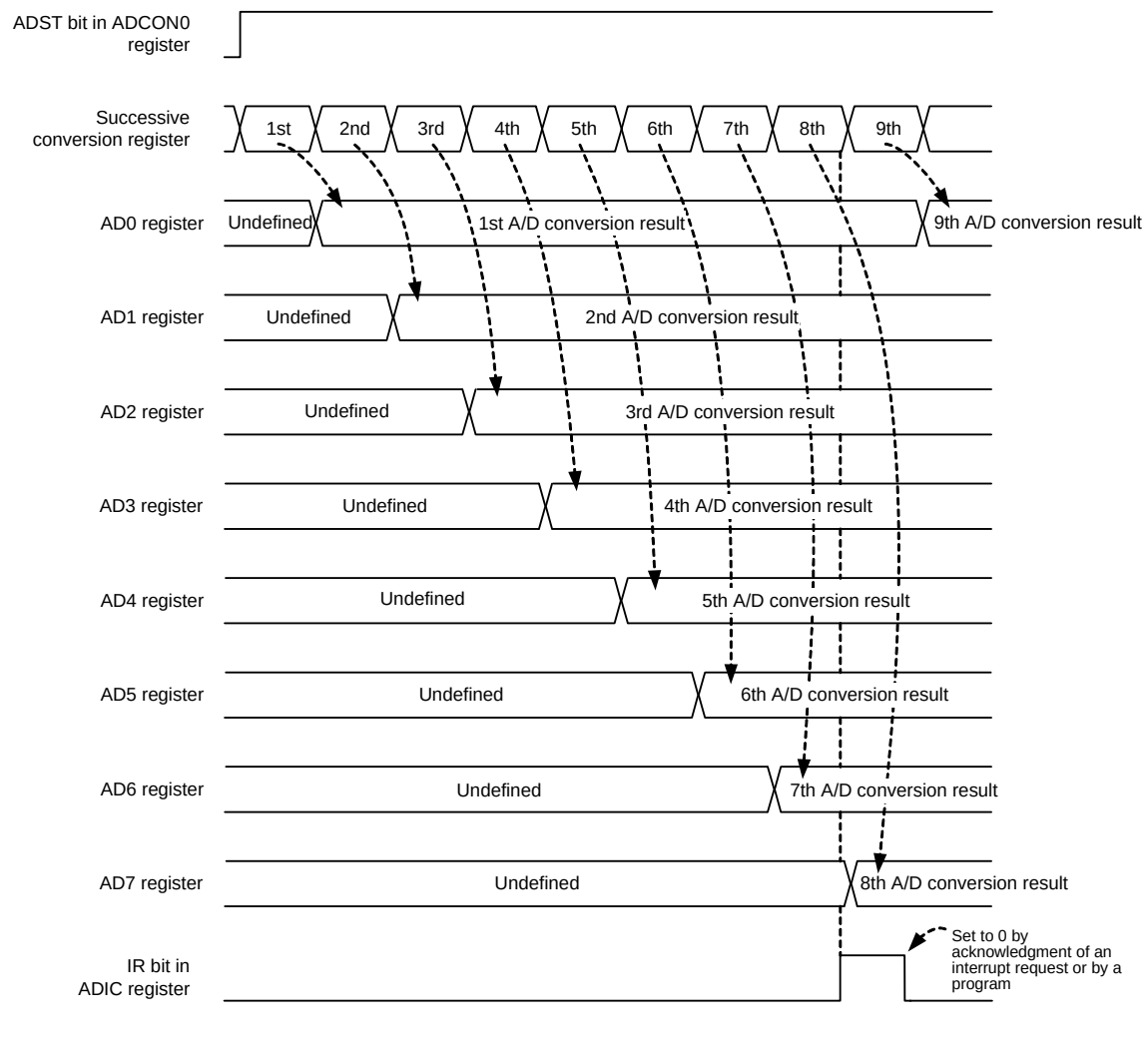
Note:
1. When setting the ADEX0 bit to 1 (on-chip reference voltage selected), set bits CH2 to CH0 in the ADINSEL register to 000b.

25.6 Repeat Mode 1

In repeat mode 1, the input voltage to one pin selected from among AN0 to AN11, or OCVREF is A/D converted repeatedly.
Table 25.8 lists the Repeat Mode 1 Specifications. Figure 25.8 shows an Operation Example in Repeat Mode 1.

Table 25.8 Repeat Mode 1 Specifications

Item	Specification
Function	The input voltage to the pin selected by bits CH0 to CH2 and bits ADGSEL0 and ADGSEL1 in the ADINSEL register or the ADEX0 bit in the ADCON1 register is A/D converted repeatedly.
Resolution	8 bits or 10 bits
A/D conversion start condition	• Software trigger • Timer RD • Timer RC • Event input trigger from ELC (refer to **25.3.3 A/D Conversion Start Condition**)
A/D conversion stop condition	Set the ADST bit in the ADCON0 register to 0
Interrupt request generation timing	When the A/D conversion result is stored in the AD7 register.
Analog input pin	One pin selectable from among AN0 to AN11, or OCVREF.
Storage resister for A/D conversion result	AD0 register: 1st A/D conversion result, 9th A/D conversion result... AD1 register: 2nd A/D conversion result, 10th A/D conversion result... AD2 register: 3rd A/D conversion result, 11th A/D conversion result... AD3 register: 4th A/D conversion result, 12th A/D conversion result... AD4 register: 5th A/D conversion result, 13th A/D conversion result... AD5 register: 6th A/D conversion result, 14th A/D conversion result... AD6 register: 7th A/D conversion result, 15th A/D conversion result... AD7 register: 8th A/D conversion result, 16th A/D conversion result...
Reading of result of A/D converter	Read registers AD0 to AD7.



The above diagram applies under the following conditions:
Bits ADCAP1 and ADCAP0 in the ADMOD register are set to 00b (start by software trigger).

Figure 25.8 Operation Example in Repeat Mode 1

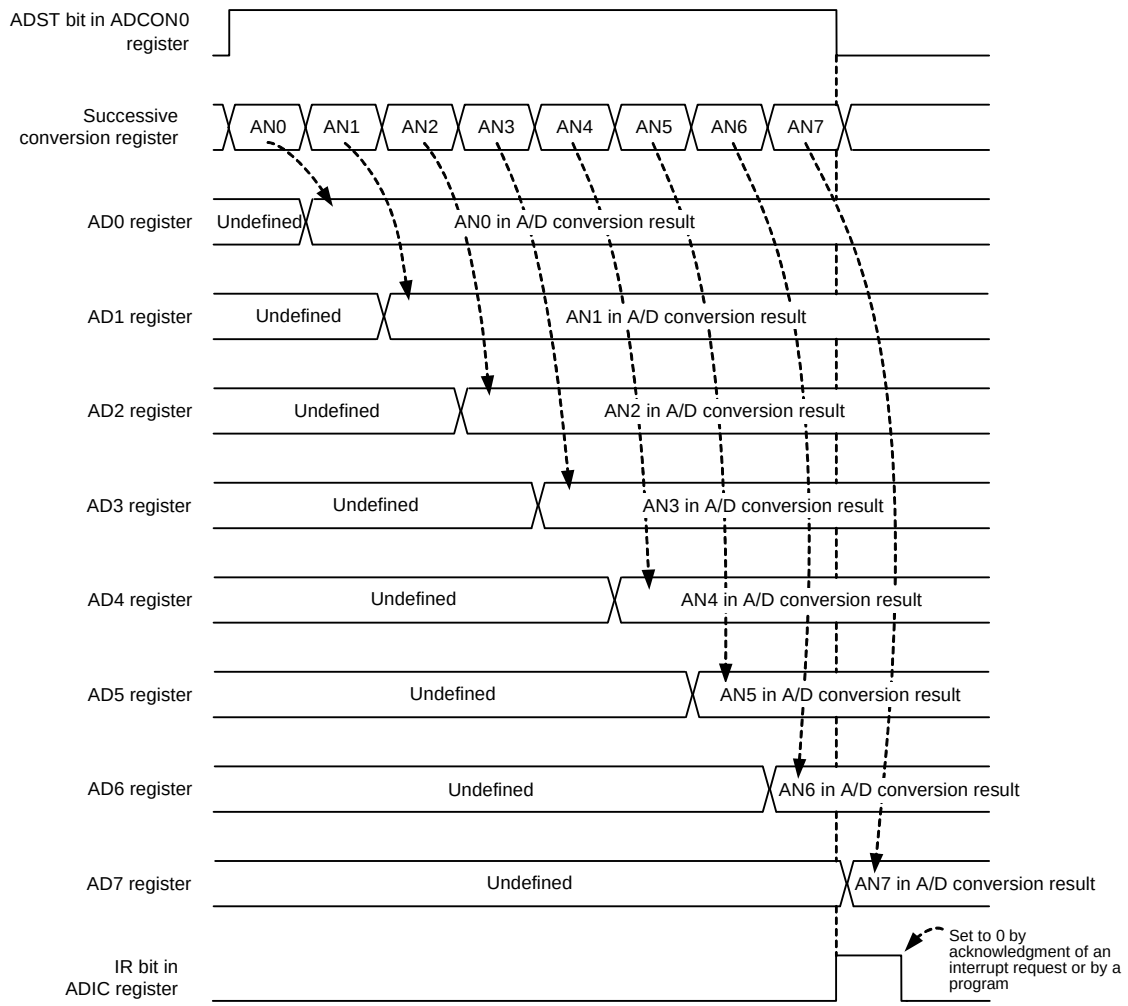
25.7 Single Sweep Mode

In single sweep mode, the input voltages to two, four, six, or eight pins selected from among AN0 to AN11 are A/D converted once.
Table 25.9 lists the Single Sweep Mode Specifications. Figure 25.9 shows an Operation Example in Single Sweep Mode.

Table 25.9 Single Sweep Mode Specifications

Item		Specification
Function		The input voltages to the pins selected by bits ADGSEL0 and ADGSEL1 and bits SCAN0 and SCAN1 in the ADINSEL register are A/D converted once.
Resolution		8 bits or 10 bits
A/D conversion start condition		• Software trigger • Timer RD • Timer RC • Event input trigger from ELC (refer to **25.3.3 A/D Conversion Start Condition**)
A/D conversion stop condition	Software trigger	• If two pins are selected, when A/D conversion of the two selected pins completes (the ADST bit in the ADCON0 register is set to 0). • If four pins are selected, when A/D conversion of the four selected pins completes (the ADST bit is set to 0). • If six pins are selected, when A/D conversion of the six selected pins completes (the ADST bit is set to 0). • If eight pins are selected, when A/D conversion of the eight selected pins completes (the ADST bit is set to 0). • Set the ADST bit to 0.
	Timer RD	Set the ADST bit to 0.
	Timer RC	
	External trigger	
Interrupt request generation timing		• If two pins are selected, when A/D conversion of the two selected pins completes. • If four pins are selected, when A/D conversion of the four selected pins completes. • If six pins are selected, when A/D conversion of the six selected pins completes. • If eight pins are selected, when A/D conversion of the eight selected pins completes.
Analog input pin (1)		AN0 to AN1 (2 pins), AN8 to AN9 (2 pins), AN0 to AN3 (4 pins), AN8 to AN11 (4 pins), AN0 to AN5 (6 pins), AN0 to AN7 (8 pins) (Selectable by bits SCAN1 and SCAN0 and bits ADGSEL1 and ADGSEL0.)
Storage resister for A/D conversion result		AD0 register: AN0, AN8 AD1 register: AN1, AN9 AD2 register: AN2, AN10 AD3 register: AN3, AN11 AD4 register: AN4 AD5 register: AN5 AD6 register: AN6 AD7 register: AN7
Reading of result of A/D converter		Read the registers from AD0 to AD7 corresponding to the selected pin.

Note:
1. When executing single-sweep mode, set bits CH2 to CH0 in the ADINSEL register to 000b.



The above diagram applies under the following conditions:
- Bits ADCAP1 and ADCAP0 in the ADMOD register are set to 00b (start by software trigger).
- Bits SCAN1 and SCAN0 in the ADINSEL register are set to 11b (8 pins), bits ADGSEL1 and ADGSEL0 are set to 00b (AN0, AN1, AN2, AN3, AN4, AN5, AN6, and AN7).

Figure 25.9 Operation Example in Single Sweep Mode

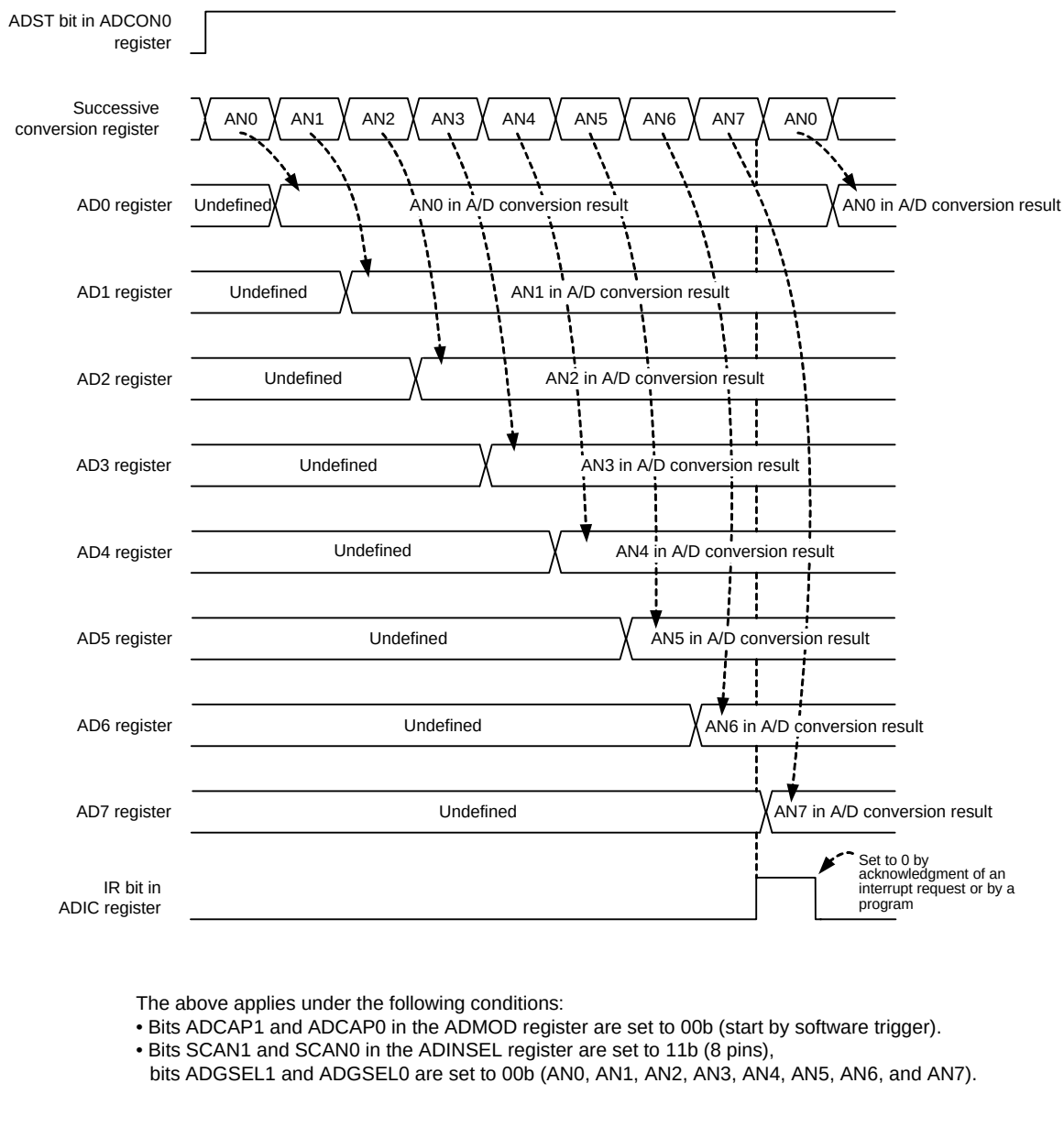
25.8 Repeat Sweep Mode

In repeat sweep mode, the input voltages to two, four, six, or eight pins selected from among AN0 to AN11 are A/D converted repeatedly.
Table 25.10 lists the Repeat Sweep Mode Specifications. Figure 25.10 shows an Operation Example in Repeat Sweep Mode.

Table 25.10 Repeat Sweep Mode Specifications

Item	Specification
Function	The input voltages to the pins selected by bits ADGSEL0 and ADGSEL1 and bits SCAN0 and SCAN1 in the ADINSEL register are A/D converted repeatedly.
Resolution	8 bits or 10 bits
A/D conversion start condition	• Software trigger • Timer RD • Timer RC • Event input trigger from ELC (refer to **25.3.3 A/D Conversion Start Condition**)
A/D conversion stop condition	Set the ADST bit in the ADCON0 register to 0
Interrupt request generation timing	• If two pins are selected, when A/D conversion of the two selected pins completes. • If four pins are selected, when A/D conversion of the four selected pins completes. • If six pins are selected, when A/D conversion of the six selected pins completes. • If eight pins are selected, when A/D conversion of the eight selected pins completes.
Analog input pin (1)	AN0 and AN1 (2 pins), AN8 and AN9 (2 pins), AN0 to AN3 (4 pins), AN8 to AN11 (4 pins), AN0 to AN5 (6 pins), AN0 to AN7 (8 pins) (Selectable by bits SCAN0 and SCAN1 and bits ADGSEL0 and ADGSEL1.)
Storage resister for A/D conversion result	AD0 register: AN0, AN8 AD1 register: AN1, AN9 AD2 register: AN2, AN10 AD3 register: AN3, AN11 AD4 register: AN4 AD5 register: AN5 AD6 register: AN6 AD7 register: AN7
Reading of result of A/D converter	Read the registers from AD0 to AD7 corresponding to the selected pin.

Note:
1. When executing repeat-sweep mode, set bits CH2 to CH0 in the ADINSEL register to 000b.



The above applies under the following conditions:
- Bits ADCAP1 and ADCAP0 in the ADMOD register are set to 00b (start by software trigger).
- Bits SCAN1 and SCAN0 in the ADINSEL register are set to 11b (8 pins), bits ADGSEL1 and ADGSEL0 are set to 00b (AN0, AN1, AN2, AN3, AN4, AN5, AN6, and AN7).

Figure 25.10 Operation Example in Repeat Sweep Mode

25.9 Output Impedance of Sensor during A/D Conversion

To carry out A/D conversion properly, charging the internal capacitor C shown in Figure 25.11 has to be completed within a specified period of time. T (sampling time) as the specified time. Let output impedance of sensor equivalent circuit be R0, internal resistance of microcomputer be R, precision (error) of the A/D converter be X, and the resolution of A/D converter be Y (Y is 1024 in the 10-bit mode, and 256 in the 8-bit mode).

$$\text{VC is generally } VC = VIN\left\{1 - e^{-\frac{1}{C(R0+R)}t}\right\}$$

$$\text{And when } t = T,\ VC = VIN - \frac{X}{Y}VIN = VIN\left(1 - \frac{X}{Y}\right)$$

$$e^{-\frac{1}{C(R0+R)}T} = \frac{X}{Y}$$

$$-\frac{1}{C(R0+R)}T = \ln\frac{X}{Y}$$

$$\text{Hence, } R0 = -\frac{T}{C \bullet \ln\frac{X}{Y}} - R$$

Figure 25.11 shows the Analog Input Pins (AN0 to AN11) and External Sensor Equivalent Circuit. When the difference between VIN and VC becomes 0.1LSB, we find impedance R0 when voltage between pins VC changes from 0 to VIN-(0.1/1024) VIN in time T. (0.1/1024) means that A/D precision drop due to insufficient capacitor charge is held to 0.1LSB at time of A/D conversion in the 10-bit mode. The actual error, however, is the value of absolute precision added to 0.1LSB.
When ϕAD = 20 MHz, T = 0.8 µs. Output impedance R0 for sufficiently charging capacitor C within time T is determined as follows.

T = 0.8 µs, R = 10 kΩ, C = 6.0 pF, X = 0.1, and Y = 1024.

$$\text{Hence, } R0 = -\frac{0.8 \times 10^{-6}}{6.0 \times 10^{-12} \bullet \ln\frac{0.1}{1024}} - 10 \times 10^{3} \fallingdotseq 4.4 \times 10^{3}$$

Thus, the allowable output impedance of the sensor equivalent circuit, making the precision (error) 0.1 LSB or less, is approximately 4.4 kΩ maximum.

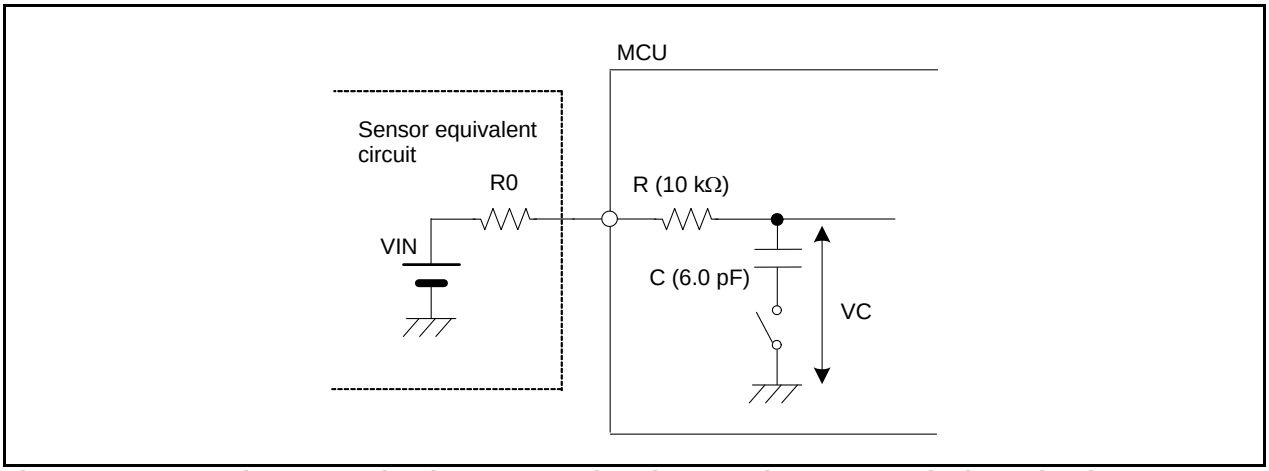


Figure 25.11 Analog Input Pins (AN0 to AN11) and External Sensor Equivalent Circuit

25.10 Notes on A/D Converter

25.10.1 Notes on A/D Conversion

- Do not write to the ADMOD, ADINSEL, ADCON0 (except the ADST bit), ADCON1, or OCVREFCR register during A/D conversion.
- When using the A/D converter in repeat mode 0, repeat mode 1, or repeat sweep mode, the frequency of the CPU clock before starting A/D conversion must be set to be a frequency higher than that of the A/D converter operating clock ϕAD.
  Do not select fHOCO-F as ϕAD.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode during A/D conversion regardless of the state of the CM02 bit in the CM0 register (1: Peripheral function clock stops in wait mode or 0: Peripheral function clock does not stop in wait mode).
- Do not set the FMSTP bit in the FMR0 register to 1 (flash memory stops) or the FMR27 bit to 1 (low-current-consumption read mode enabled) during A/D conversion. Otherwise, the A/D conversion result will be undefined.
- After setting the ADST bit in the ADCON0 register to 0 (A/D conversion stops) by a program during A/D conversion to forcibly end the conversion, allow two or more cycles of the ϕAD clock before writing 1 to the ADST bit to ensure time for end processing.

25.10.2 Clock Source Switching

- Stop A/D conversion before switching the clock source. After switching the clock source, wait for at least two cycles of the fHOCO-F clock to before starting A/D conversion.

[Changing procedure]
(1) Set the ADST bit in the ADCON0 register to 0 (A/D conversion stops).
(2) Change the CKS2 bit in the ADMOD register.
(3) Wait for at least two cycles of the fHOCO-F clock.
(4) Set the ADST bit in the ADCON0 register to 1 (A/D conversion starts).

- To change the clock source from fHOCO-F to another clock and then stop fHOCO-F, after switching the clock source, wait at least two cycles of fHOCO-F before stopping fHOCO-F.

[Changing procedure]
(1) Set the ADST bit in the ADCON0 register to 0 (A/D conversion stops).
(2) Change the CKS2 bit in the ADMOD register.
(3) Wait for at least two cycles of the fHOCO-F clock.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

Notes:
1. Do not set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off) while fHOCO-F is selected as the clock source.
2. Do not change the division ratio of the high-speed on-chip oscillator set by the FRA2 register while fHOCO-F is selected as the count source.

25.10.3 Pin Handling

Connect a 0.1 μF capacitor between pins VREF and AVSS.

26. Comparator B

Comparator B compares a reference input voltage to an analog input voltage. Comparator B1 and comparator B3 are independent of each other.

26.1 Overview

The comparison result of the reference input voltage and analog input voltage can be read by software. An input to the IVREFi (i = 1 or 3) pin can be used as the reference input voltage.
Table 26.1 lists the Comparator B Specifications, Figure 26.1 shows the Comparator B Block Diagram, and Table 26.2 lists the I/O Pins.

Table 26.1 Comparator B Specifications

Item	Specification
Analog input voltage	Input voltage to the IVCMPi pin
Reference input voltage	Input voltage to the IVREFi pin
Comparison result	Read from the INTiCOUT bit in the INTCMP register
Interrupt request generation timing	When the comparison result changes.
Selectable function	Digital filter function Whether the digital filter is used or not and the sampling frequency can be selected.

i = 1 or 3

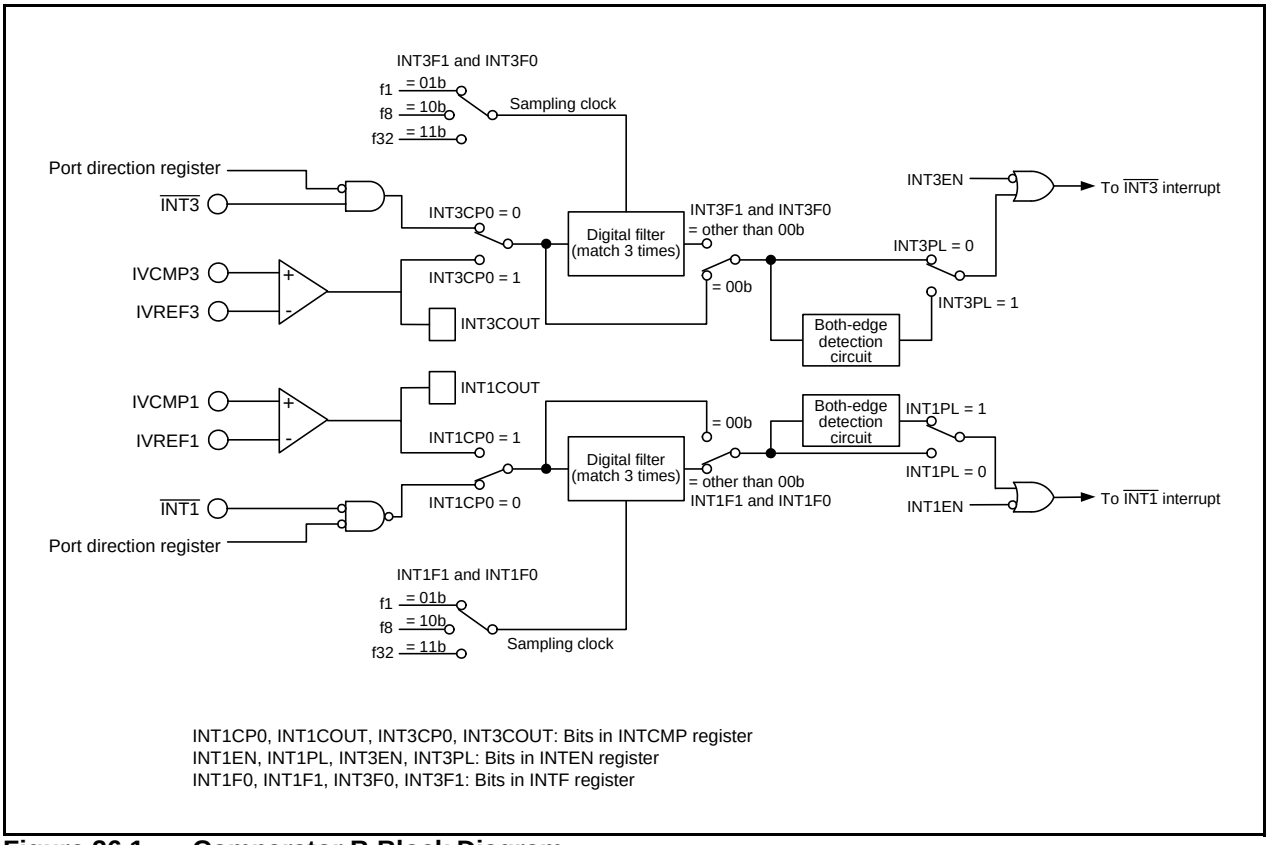


Figure 26.1 Comparator B Block Diagram

Table 26.2 I/O Pins

Pin Name	I/O	Function
IVCMP1	Input	Comparator B1 analog pin
IVREF1	Input	Comparator B1 reference voltage pin
IVCMP3	Input	Comparator B3 analog pin
IVREF3	Input	Comparator B3 reference voltage pin

26.2 Registers

Table 26.3 lists the Comparator B Register Configuration.

Table 26.3 Comparator B Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Comparator B Control Register 0	INTCMP	00h	00228h	8

26.2.1 Comparator B Control Register 0 (INTCMP)

Address 00228h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3COUT	—	—	INT3CP0	INT1COUT	—	—	INT1CP0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT1CP0	Comparator B1 operation enable bit	0: Comparator B1 operation disabled 1: Comparator B1 operation enabled	R/W
b1	—	Reserved	Set to 0.	R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	INT1COUT	Comparator B1 monitor flag	0: IVCMP1 < IVREF1 or comparator B1 operation disabled 1: IVCMP1 > IVREF1	R
b4	INT3CP0	Comparator B3 operation enable bit	0: Comparator B3 operation disabled 1: Comparator B3 operation enabled	R/W
b5	—	Reserved	Set to 0.	R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	INT3COUT	Comparator B3 monitor flag	0: IVCMP3 < IVREF3 or comparator B3 operation disabled 1: IVCMP3 > IVREF3	R

26.3 Operation

Comparator B1 and comparator B3 operate independently. Their operations are the same.
Table 26.4 lists the Procedure for Setting Registers Associated with Comparator B.

Table 26.4 Procedure for Setting Registers Associated with Comparator B

Step	Register	Bit	Setting Value
1	Select the function of pins IVCMPi and IVREFi. Refer to **14.4 I/O of Peripheral Functions**. However, set registers and bits other than those listed in step 2 and later steps.		
2	INTF	Select whether the filter is used or not and the sampling clock.	
3	INTCMP	INTiCP0	1 (operation enabled)
4	Wait for the comparator stabilization time (100 μs max.)		
5	INTEN	INTiEN	When using an interrupt: 1 (interrupt enabled)
		INTiPL	When using an interrupt: Select the input polarity.
6	INTiIC	ILVL2 to ILVL0	When using an interrupt: Select the interrupt priority level.
		IR	When using an interrupt: 0 (no interrupt requested: initialization)

i = 1 or 3

Figure 26.2 shows a Comparator Bi Operation Example (i = 1 or 3).
If the analog input voltage is higher than the reference input voltage, the INTiCOUT bit in the INTCMP register is set to 1. If the analog input voltage is lower than the reference input voltage, the INTiCOUT bit is set to 0. To use the comparator Bi interrupt, set the INTiEN bit in the INTEN register to 1 (interrupt enabled). If the comparison result changes at this time, a comparator Bi interrupt request is generated. Refer to **26.4 Comparator B1 and Comparator B3 Interrupts** for details on interrupts.

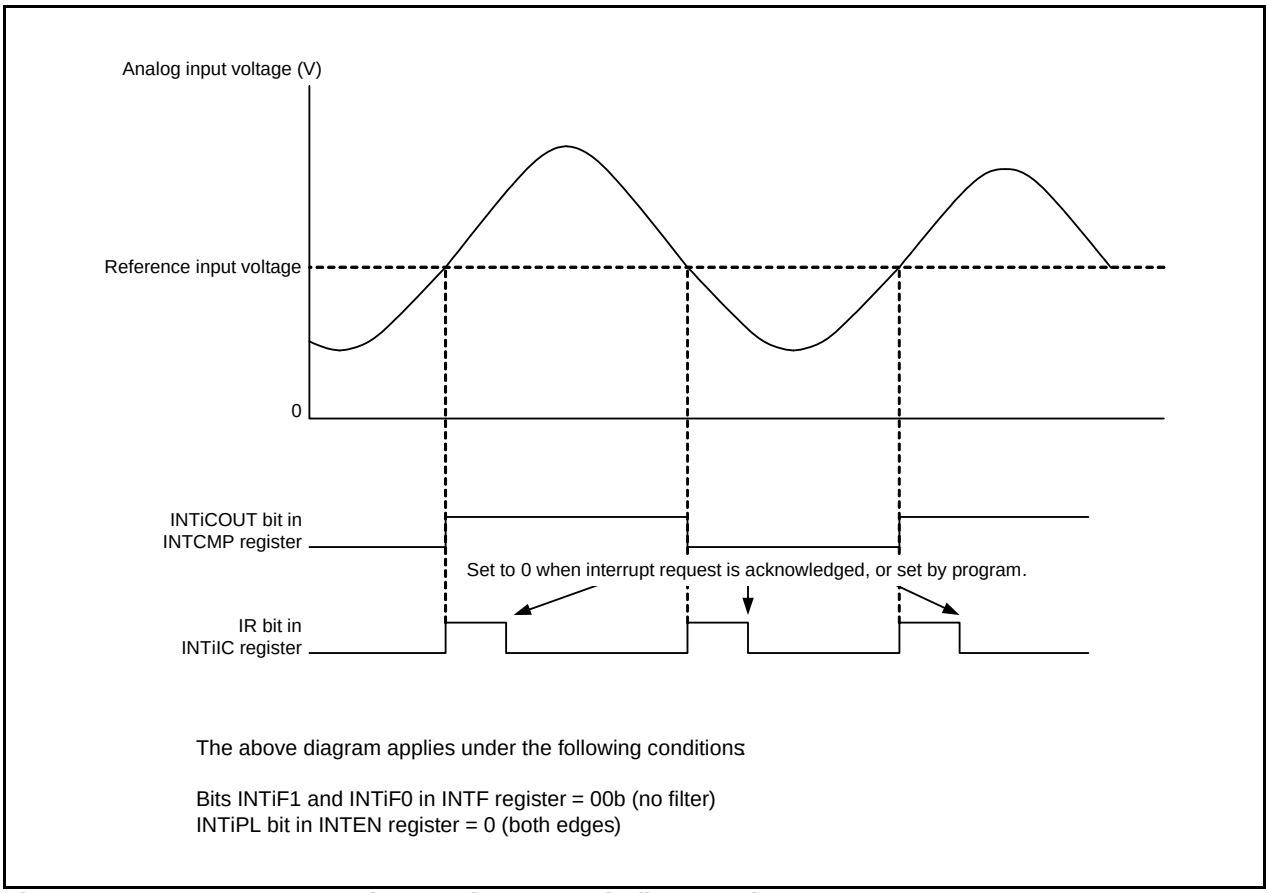


Figure 26.2 Comparator Bi Operation Example (i = 1 or 3)

26.3.1 Comparator Bi Digital Filter (i = 1 or 3)

Comparator Bi can use the same digital filter as the $\overline{\text{INTi}}$ input. The sampling clock can be selected by bits INTiF0 and INTiF1 in the INTF register. The INTiCOUT signal output from comparator Bi is sampled every sampling clock. When the level matches three times, the IR bit in the INTiIC register is set to 1 (interrupt requested).

Figure 26.3 shows the Comparator Bi Digital Filter Configuration (i = 1 or 3) and Figure 26.4 shows a Comparator Bi Digital Filter Operation Example (i = 1 or 3).

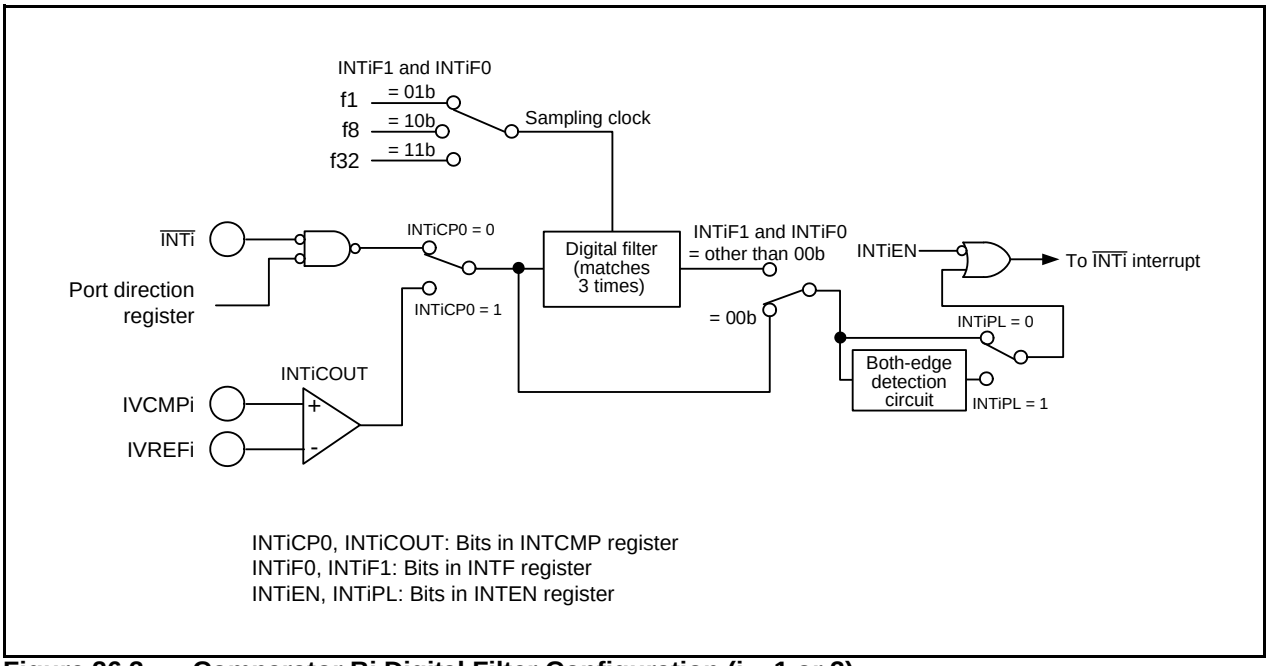


Figure 26.3 Comparator Bi Digital Filter Configuration (i = 1 or 3)

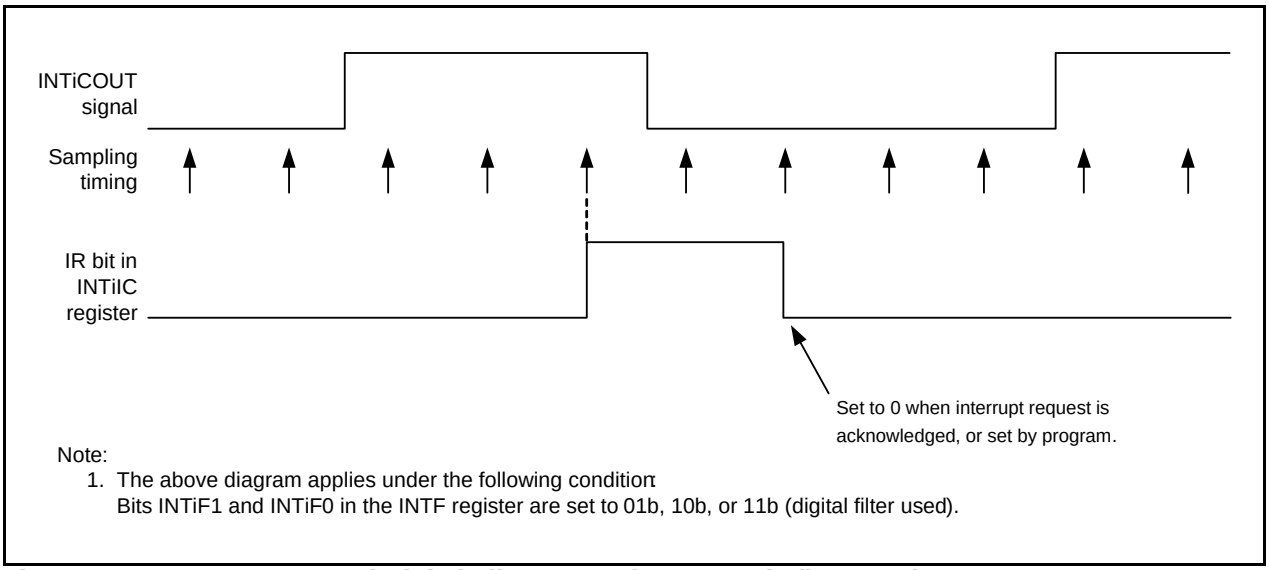


Figure 26.4 Comparator Bi Digital Filter Operation Example (i = 1 or 3)

26.4 Comparator B1 and Comparator B3 Interrupts

Comparator B generates interrupt requests from two sources, comparator B1 and comparator B3. The comparator Bi (i = 1 or 3) interrupt uses the same INTiIC register (bits IR and ILVL0 to ILVL2) as the $\overline{\text{INTi}}$ input and a single vector.

To use the comparator Bi interrupt, set the INTiEN bit in the INTEN register to 1 (enabled). In addition, the polarity is selected with the INTiPL bit in the INTEN register and the INTiPOL bit in the INTPOL register.

Inputs can also be passed through the digital filter with three different sampling clocks.

Figure 26.5 shows the Timing of Comparator Bi Interrupt Generation (Rising Edge Selected) and Figure 26.6 shows the Timing of Comparator Bi Interrupt Generation (Falling Edge Selected).

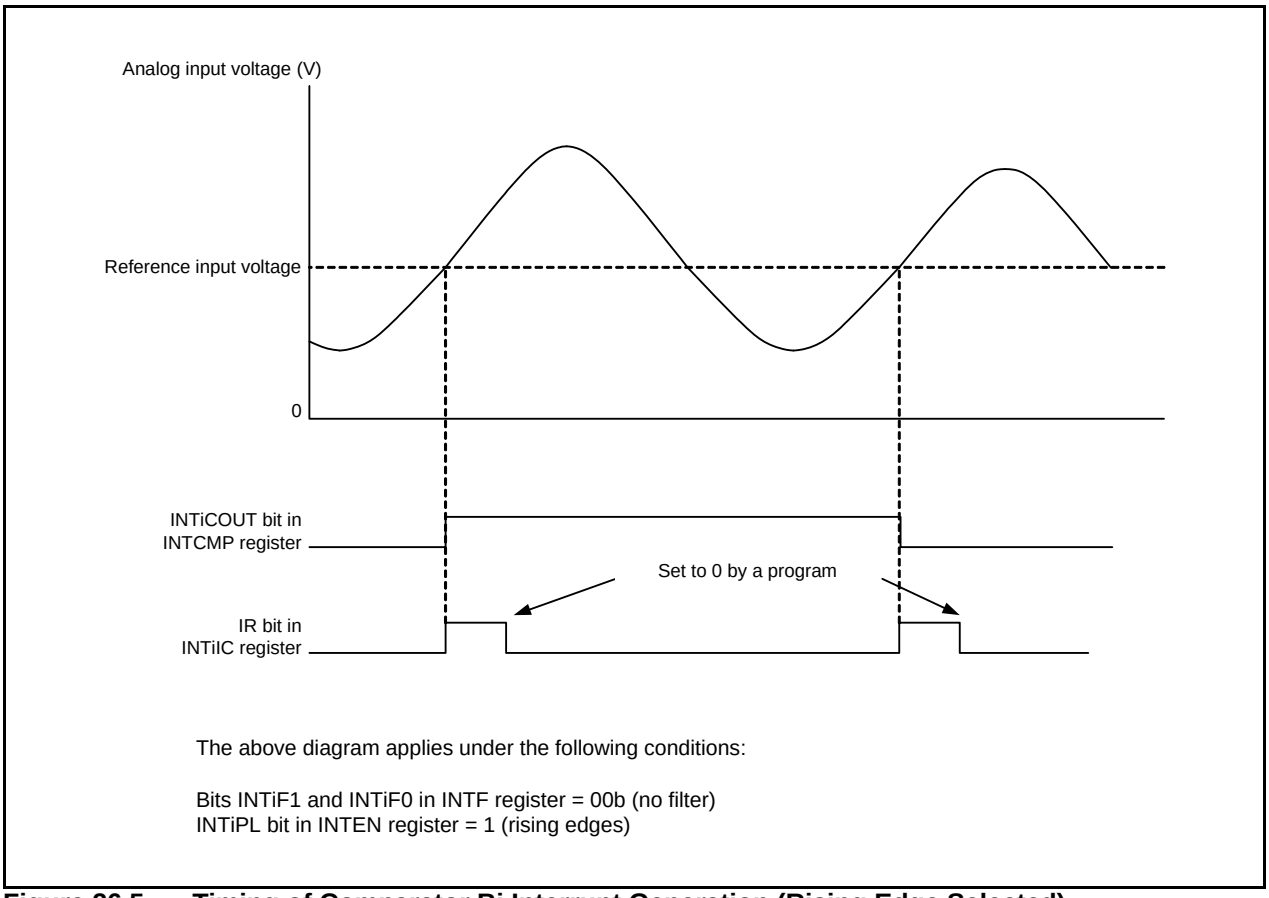
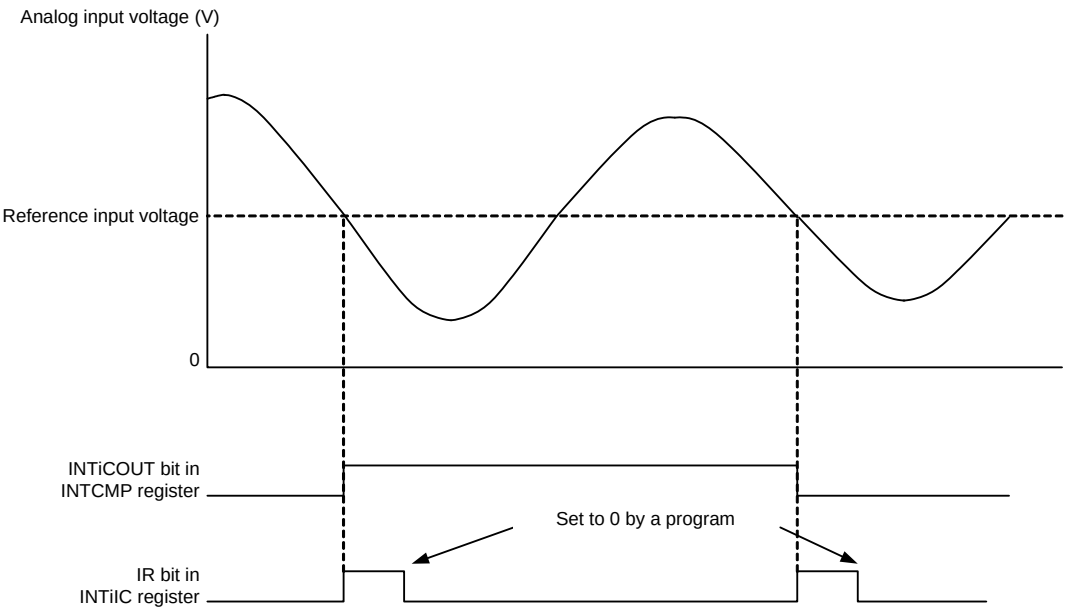


Figure 26.5 Timing of Comparator Bi Interrupt Generation (Rising Edge Selected)



The above diagram applies under the following conditions:

Bits INTiF1 and INTiF0 in INTF register = 00b (no filter)
INTiPL bit in INTEN register = 1 (falling edges)

Figure 26.6 Timing of Comparator Bi Interrupt Generation (Falling Edge Selected)

27. Flash Memory

The flash memory supports the following three rewrite modes: CPU rewrite mode, standard serial I/O mode, and parallel I/O mode.

27.1 Overview

Table 27.1 lists the Flash Memory Specifications (refer to **Tables 1.1** to **1.8 R8C/54E Group, R8C/54F Group, R8C/54G Group, R8C/54H Group Specifications** for items not listed in Table 27.1).
The R8C/54E Group and R8C/54G Group have on-chip data flash (1 KB × 4 blocks) with background operation (BGO) function.

Table 27.1 Flash Memory Specifications

Item		Specification
Flash memory operating modes		3 modes (CPU rewrite, standard serial I/O, and parallel I/O)
Division of erase blocks		Refer to **Figure 27.1**.
Programming method		Byte units/word units (program ROM area only)
Erasure method		Block erase
Programming and erasure control method (1)		Program and erase control by software commands
Rewrite protect control method	Blocks 0 to 6 (Program ROM) (2)	Rewrite protect control in block units by the lock bit
	Blocks A, B, C, and D (Data flash) (4)	Individual rewrite protect control on blocks A, B, C, and D by bits FMR14, FMR15, FMR16, and FMR17 in the FMR1 register
Number of commands		7 commands
Program and erase endurance (3)	Blocks 0 to 6 (Program ROM) (2)	1,000 times
	Blocks A, B, C, and D (Data flash) (4)	10,000 times
ID code check function		Standard serial I/O mode supported
ROM code protection		Parallel I/O mode supported

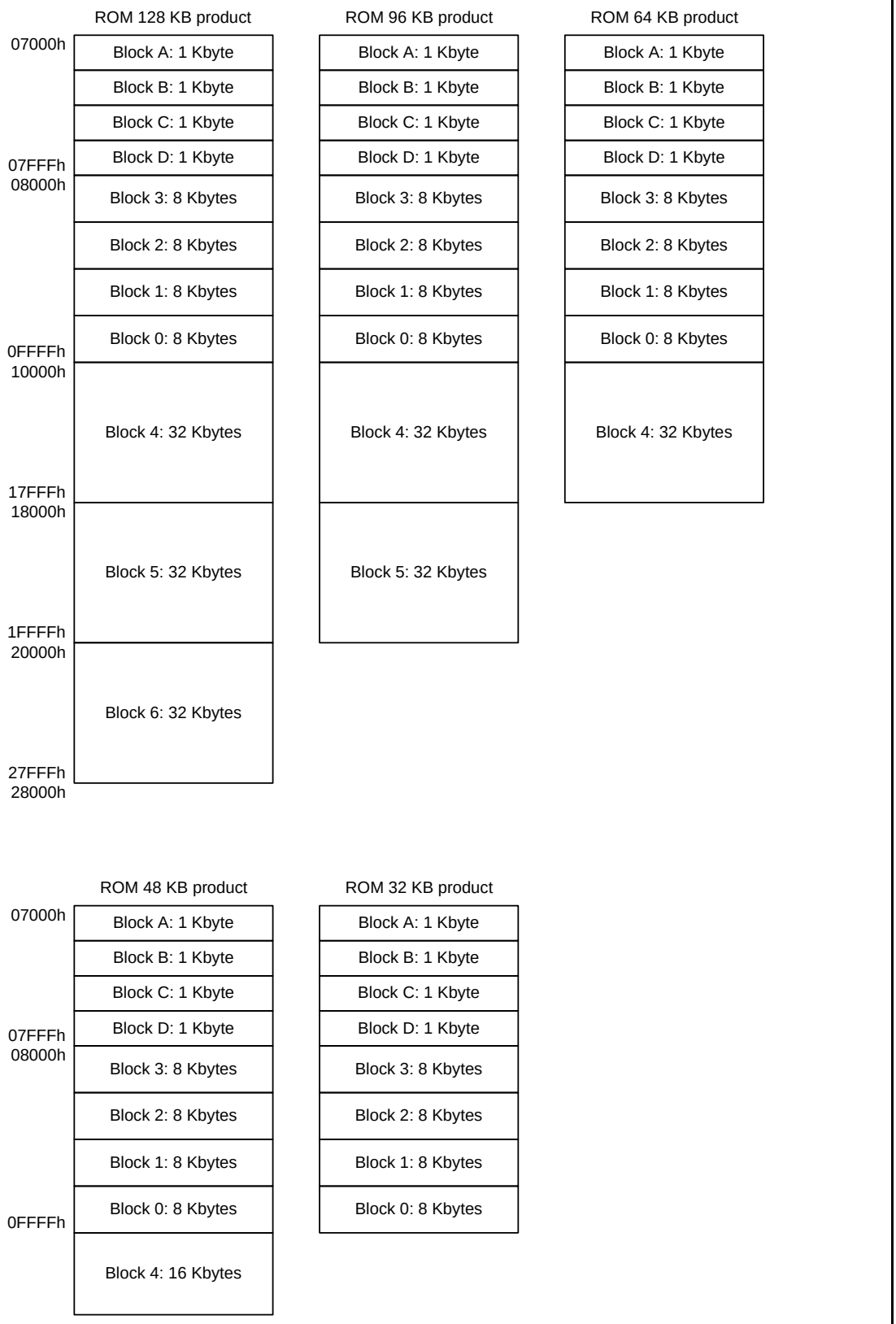
Notes:
1. To perform programming or erasure, use VCC = 2.7 to 5.5 V as the supply voltage. Do not perform programming or erasure at less than 2.7 V.
2. The number of blocks and block division vary with the MCU. Refer to **Figure 27.1 R8C/54E Group, R8C/54F Group, R8C/54G Group, R8C/54H Group Flash Memory Block Diagram** for details.
3. Definition of program and erase endurance
   The program and erase endurance is defined on a per-block basis. If the program and erase endurance is n (n = 1,000 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1-Kbyte block, and then the block is erased, the program/erase endurance still stands at one. When performing 100 or more rewrites, the actual erase count can be reduced by executing program operations in such a way that all blank areas are used before performing an erase operation. Avoid rewriting only particular blocks and try to average out the program and erase endurance of the blocks. It is also advisable to retain data on the erase endurance of each block and limit the number of erase operations to a certain number.
4. The R8C/54F Group and R8C/54H Group do not have on-chip data flash.

Table 27.2 Flash Memory Rewrite Mode

Flash Memory Rewrite Mode	CPU Rewrite Mode	Standard Serial I/O Mode	Parallel I/O Mode
Function	User ROM area is rewritten by executing software commands from the CPU.	User ROM area is rewritten using a dedicated serial programmer.	User ROM area is rewritten using a dedicated parallel programmer.
Rewritable area	User ROM	User ROM	User ROM
Rewrite programs	User program	Standard boot program	—

27.2 Memory Map

The flash memory contains a user ROM area and a boot ROM area (reserved area).
Figure 27.1 shows the Flash Memory Block Diagrams of the R8C/54E Group, R8C/54F Group, R8C/54G Group, R8C/54H Group.
The user ROM area contains program ROM and data flash.
Program ROM: Flash memory mainly used for storing programs
Data flash: Flash memory mainly used for storing data to be rewritten
The user ROM area is divided into several blocks. The user ROM area can be rewritten in CPU rewrite mode, standard serial I/O mode, or parallel I/O mode.
The rewrite control program (standard boot program) for standard serial I/O mode is stored in the boot ROM area before shipment. The boot ROM area is allocated separately from the user ROM area.



Note:
1. The R8C/54F Group and R8C/54H Group do not have on-chip data flash (data block A to data block D).

Figure 27.1 R8C/54E Group, R8C/54F Group, R8C/54G Group, R8C/54H Group Flash Memory Block Diagram

27.3 Registers

Table 27.3 lists the Flash Memory Register Configuration.

Table 27.3 Flash Memory Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Flash Memory Status Register	FST	10000X00b	00252h	8
Flash Memory Control Register 0	FMR0	00h	00254h	8
Flash Memory Control Register 1	FMR1	00h	00255h	8
Flash Memory Control Register 2	FMR2	00h	00256h	8
Option Function Select Register	OFS	(Note 1)	0FFFFh	8

Note:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform any additional writes to the OFS register. Erasing the block that includes the OFS register sets the OFS register to FFh.

27.3.1 Flash Memory Status Register (FST)

Address 00252h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FST7	FST6	FST5	FST4	—	LBDATA	BSYAEI	RDYSTI
After Reset	1	0	0	0	0	X	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RDYSTI	Flash ready status interrupt request flag (1, 4, 5)	0: No flash ready status interrupt requested 1: Flash ready status interrupt requested	R/W
b1	BSYAEI	Flash access error interrupt request flag (2, 4, 5)	0: No flash access error interrupt requested 1: Flash access error interrupt requested	R/W
b2	LBDATA	LBDATA monitor flag	0: Locked 1: Not locked	R
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	FST4	Program error flag (3)	0: No program error 1: Program error	R
b5	FST5	Erase error flag (3)	0: No erase error 1: Erase error	R
b6	FST6	Erase-suspend status flag	0: Other than erase-suspend 1: During erase-suspend	R
b7	FST7	Ready/busy status flag	0: Busy 1: Ready	R

Notes:
1. The RDYSTI bit cannot be set to 1 (flash ready status interrupt requested) by a program.
   When writing 0 (no flash ready status interrupt requested) to the RDYSTI bit, read this bit (dummy read) before writing to it. Make sure the DTC is not activated by the flash ready status source between reading and writing.
   To check this bit, set the RDYSTIE bit in the FMR0 register to 1 (flash ready status interrupt enabled).
2. The BSYAEI bit cannot be set to 1 (flash access error interrupt requested) by a program.
   When writing 0 (no flash access error interrupt requested) to the BSYAEI bit, read this bit (dummy read) before writing to it.
   To check this bit, set the BSYAEIE bit in the FMR0 register to 1 (flash access error interrupt enabled) or set the CMDERIE bit in the FMR0 register to 1 (erase/write error interrupt enabled).
3. This bit is also set to 1 (error) when a command error occurs.
4. When this bit is 1, do not set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled).
5. To set this bit to 0, first read 1, then write 0.

RDYSTI Bit (Flash ready status interrupt request flag)

When the RDYSTIE bit in the FMR0 register is 1 (flash ready status interrupt enabled) and auto-programming or auto-erasure completes, or erase-suspend mode is entered, the RDYSTI bit is set to 1 (flash ready status interrupt requested).
During interrupt handling, set the RDYSTI bit to 0 (no flash ready status interrupt requested).

[Condition for setting to 0]
Set to 0 by the interrupt handling program.
[Condition for setting to 1]
When the flash memory status changes from busy to ready while the RDYSTIE bit in the FMR0 register is 1, the RDYSTI bit is set to 1.
The status is changed from busy to ready in the following states:
• Completion of erasing/programming the flash memory
• Suspend acknowledgement
• Completion of forcible termination
• Completion of the lock bit program
• Completion of the read lock bit status
• When the flash memory can be read after it has been stopped.

BSYAEI Bit (Flash access error interrupt request flag)

If an auto-programming or auto-erase block is accessed while the BSYAEIE bit in the FMR0 register is 1 (flash access error interrupt enabled), the BSYAEI bit is set to 1 (flash access error interrupt requested). During interrupt handling, set the BSYAEI bit to 0 (no flash access error interrupt requested).

If a command sequence error, erase error, or program error occurs while the CMDERIE bit in the FMR0 register is 1 (erase/write error interrupt enabled), the BSYAEI bit is set to 1 (flash access error interrupt requested).
During interrupt handling, execute the clear status register command and set the BSYAEI bit to 0 (no flash access error interrupt requested).

[Conditions for setting to 0]
(1) Set to 0 by an interrupt handling program.
(2) Execute the clear status register command.
[Conditions for setting to 1]
(1) Read or write to the area that is being erased/written when the BSYAEIE bit in the FMR0 register is 1 and while the flash memory is busy.
Or, read the data flash area while erasing/writing to the program ROM area. (Note that the read value is undefined in both cases. Writing has no effect.)
(2) If a command sequence error, erase error, or program error occurs when the CMDERIE bit in the FMR0 register is 1 (erase/write error interrupt enabled).

LBDATA Bit (LBDATA monitor flag)

This is a read-only bit indicating the lock bit status. To confirm the lock bit status, execute the read lock bit status command and read the LBDATA bit after the FST7 bit is set to 1 (ready).
The condition for updating this bit is when the program, erase, read lock bit status commands are generated.
When the read lock bit status command is input, the FST7 bit is set to 0 (busy). At the time when the FST7 bit is set to 1 (ready), the lock bit status is stored in the LBDATA bit. The data in the LBDATA bit is retained until the next command is input.

FST4 Bit (Program error flag)

This is a read-only bit indicating the auto-programming status. The bit is set to 1 if a program error occurs; otherwise, it is set to 0. Refer to **27.5.8 Full Status Check** for details.

FST5 Bit (Erase error flag)

This is a read-only bit indicating the status of auto-erasure. The bit is set to 1 if an erase error occurs; otherwise, it is set to 0. Refer to **27.5.8 Full Status Check** for details.

FST6 Bit (Erase-suspend status flag)

This is a read-only bit indicating the suspend status. The bit is set to 1 when an erase-suspend request is acknowledged and the suspend status is entered; otherwise, it is set to 0.

FST7 Bit (Ready/busy status flag)

When the FST7 bit is 0 (busy), the flash memory is in one of the following states:
- During programming
- During erasure
- During the lock bit program
- During the read lock bit status
- During forced stop operation
- The flash memory is being stopped
- The flash memory is being activated

Otherwise, the FST7 bit is set to 1 (ready).

27.3.2 Flash Memory Control Register 0 (FMR0)

Address 00254h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RDYSTIE	BSYAEIE	CMDERIE	CMDRST	FMSTP	FMR02	FMR01	FMR00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FMR00	Programming unit select bit (1, 5, 6)	0: Byte units 1: Word units	R/W
b1	FMR01	CPU rewrite mode select bit (1, 4)	0: CPU rewrite mode disabled 1: CPU rewrite mode enabled	R/W
b2	FMR02	EW1 mode select bit (1)	0: EW0 mode 1: EW1 mode	R/W
b3	FMSTP	Flash memory stop bit (2)	0: Flash memory operates 1: Flash memory stops (Low-power consumption state, flash memory initialization)	R/W
b4	CMDRST	Erase/write sequence reset bit (3)	When the CMDRST bit is set to 1, the erase/write sequence is reset and erasure/writing can be forcibly stopped. The read value is 0.	R/W
b5	CMDERIE	Erase/write error interrupt enable bit	0: Erase/write error interrupt disabled 1: Erase/write error interrupt enabled	R/W
b6	BSYAEIE	Flash access error interrupt enable bit	0: Flash access error interrupt disabled 1: Flash access error interrupt enabled	R/W
b7	RDYSTIE	Flash ready status interrupt enable bit	0: Flash ready status interrupt disabled 1: Flash ready status interrupt enabled	R/W

Notes:
1. To set this bit to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
2. Write to the FMSTP bit by a program transferred to the RAM. The FMSTP bit is enabled when the FMR01 bit is set to 1 (CPU rewrite mode enabled). Do not set FMSTP bit to 1 (flash memory stops) when the FMR01 bit is 0 (CPU rewrite mode disabled). To set the FMSTP bit to 1 (flash memory stops), set it when the FST7 bit in the FST register is 1 (ready).
3. The CMDRST bit is enabled when the FMR01 bit is set to 1 (CPU rewrite mode enabled) and the FST7 bit in the FST register is set to 0 (busy).
4. To set the FMR01 bit to 0 (CPU rewrite mode disabled), set it when the RDYSTI bit in the FST register is 0 (no flash ready status interrupt requested) and the BSYAEI bit is 0 (no flash access error interrupt requested).
5. Valid only for the program ROM area.
6. When the FMR00 bit in the FMR0 register is set to 1 (word units), use the word instruction to set software commands (addresses and data), and write to even addresses.

FMR00 Bit (Programming unit select bit)

When word units are selected (the FMR00 bit is 1), operation is as follows and commands cannot be input to odd addresses.
Commands cannot be input to the odd addresses of the user ROM area.
Commands can be input to the even addresses of the user ROM area.

FMR01 Bit (CPU rewrite mode select bit)

When the FMR01 bit is set to 1 (CPU rewrite mode enabled), software commands can be accepted.

FMR02 Bit (EW1 mode select bit)

When the FMR02 bit is set to 1 (EW1 mode), EW1 mode is selected.

FMSTP Bit (Flash memory stop bit)

This bit is used to initialize the flash memory control circuits, and also to reduce the amount of current consumed by the flash memory. Access to the flash memory is disabled by setting the FMSTP bit to 1.
Write to the FMSTP bit by a program transferred to the RAM.
To reduce the power consumption further in high-speed on-chip oscillator mode and low-speed on-chip oscillator mode (XIN clock stopped), set the FMSTP bit to 1. Refer to **10.6.10 Stopping Flash Memory** for details.
When the MCU enters stop mode or wait mode while CPU rewrite mode is disabled, the FMR0 register does not need to be set because the power for the flash memory is automatically turned off and is turned back on when the MCU exits stop mode or wait mode.
When the FMSTP bit is set to 1 (including during the busy status (the period while the FST7 bit is 0) immediately after the FMSTP bit is changed from 1 to 0), do not set to low-current-consumption read mode at the same time.

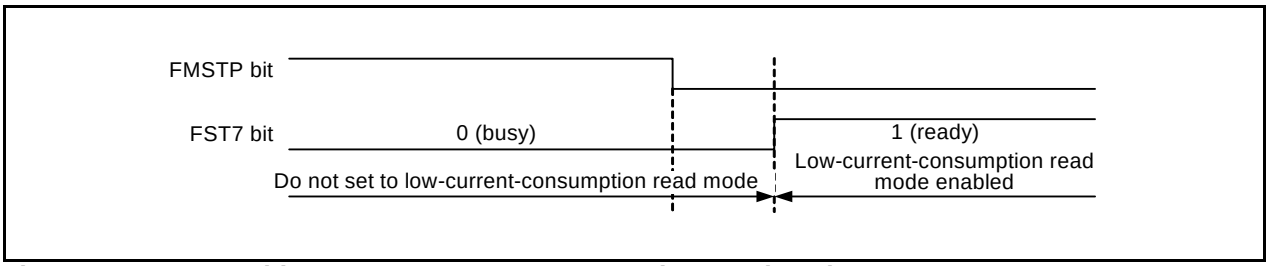


Figure 27.2 Transition to Low-Current-Consumption Read Mode

CMDRST Bit (Erase/write sequence reset bit)

This bit is used to initialize the flash memory sequence and forcibly stop a program or block erase command. The program ROM area can be read when resetting the sequence of programming/erasing the data flash area.
If the program or block erase command is forcibly stopped using the CMDRST bit in the FMR0 register, execute the clear status register command after the FST7 bit in the FST register is set back to 1 (ready). To program the same address again, execute the block erase command again and ensure it has been completed normally before programming. If the addresses and blocks where the program or block erase command is forcibly stopped are allocated in the program area, set the FMR13 bit in the FMR1 register to 1 (lock bit disabled) before executing the block erase command again.
When the CMDRST bit is set to 1 (erasure/writing stops) during erase-suspend, the suspend status is also initialized. Therefore, execute a block erasure again for the block where the block erasure is being suspended.
When td(CMDRST-READY) has elapsed after the CMDRST bit is set to 1 (erasure/writing stops), the currently executing command is forcibly stopped and the flash memory can be read.

CMDERIE Bit (Erase/write error interrupt enable bit)

This bit enables flash command error interrupt generation if the following errors occur:
• Program error
• Block erase error
• Command sequence error
If the CMDERIE bit is set to 1 (erase/write error interrupt enabled), an interrupt is generated if the above errors occur.
If a flash command error interrupt is generated, execute the clear status register command during interrupt handling.

To change the CMDERIE bit from 0 (erase/write error interrupt disabled) to 1 (erase/write error interrupt enabled), make the setting as follows:
(1) Execute the clear status register command.
(2) Set the CMDERIE bit to 1.

BSYAEIE Bit (Flash access error interrupt enable bit)

This bit enables flash access error interrupt generation if the flash memory being rewritten is accessed.

To change the BSYAEIE bit from 0 (flash access error interrupt disabled) to 1 (flash access error interrupt enabled), make the setting as follows:
(1) Read the BSYAEI bit in the FST register (dummy read).
(2) Write 0 (no flash access error interrupt requested) to the BSYAEI bit.
(3) Set the BSYAEIE bit to 1 (flash access error interrupt enabled).

RDYSTIE Bit (Flash ready status interrupt enable bit)

This bit enables flash ready status error interrupt generation when the status of the flash memory sequence changes from busy to ready status.

To change the RDYSTIE bit from 0 (flash ready status interrupt disabled) to 1 (flash ready status interrupt enabled), make the setting as follows:
(1) Read the RDYSTI bit in the FST register (dummy read).
(2) Write 0 (no flash ready status interrupt requested) to the RDYSTI bit.
(3) Set the RDYSTIE bit to 1 (flash ready status interrupt enabled).

27.3.3 Flash Memory Control Register 1 (FMR1)

Address 00255h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FMR17	FMR16	FMR15	FMR14	FMR13	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	FMR13	Lock bit disable select bit (1)	0: Lock bit enabled 1: Lock bit disabled	R/W
b4	FMR14	Data flash block A rewrite disable bit (2, 3)	0: Rewrite enabled (software command acceptable) 1: Rewrite disabled (software command not acceptable, no error occurred)	R/W
b5	FMR15	Data flash block B rewrite disable bit (2, 3)		R/W
b6	FMR16	Data flash block C rewrite disable bit (2, 3)		R/W
b7	FMR17	Data flash block D rewrite disable bit (2, 3)		R/W

Notes:
1. To set the FMR13 bit to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
2. To set this bit to 0, first write 1 and then 0 immediately. Disable interrupts and DTC activation between writing 1 and writing 0.
3. This bit is set to 0 when the FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).

FMR13 Bit (Lock bit disable select bit)

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit is disabled. When the FMR13 bit is set to 0, the lock bit is enabled. Refer to **27.5.6 Data Protect Function** for the details on the lock bit.
The FMR13 bit enables the lock bit function only and the lock bit data does not change. However, when a block erase command is executed while the FMR13 bit is set to 1, the lock bit data set to 0 (locked) changes to 1 (not locked) after erasure completes.

[Conditions for setting to 0]
The FMR13 bit is set to 0 when one of the following conditions is met.
• Completion of the program command
• Completion of the block erase command
• Generation of a command sequence error
• Transition to erase-suspend
• The FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).
• The FMSTP bit in the FMR0 register is set to 1 (flash memory stops).
• The CMDRST bit in the FMR0 register is set to 1 (erasure/writing stops).
[Condition for setting to 1]
Set to 1 by a program.

FMR14 Bit (Data flash block A rewrite disable bit)

When the FMR14 bit is set to 0, data flash block A accepts program and block erase commands.

FMR15 Bit (Data flash block B rewrite disable bit)

When the FMR15 bit is set to 0, data flash block B accepts program and block erase commands.

FMR16 Bit (Data flash block C rewrite disable bit)

When the FMR16 bit is set to 0, data flash block C accepts program and block erase commands.

FMR17 Bit (Data flash block D rewrite disable bit)

When the FMR17 bit is set to 0, data flash block D accepts program and block erase commands.

27.3.4 Flash Memory Control Register 2 (FMR2)

Address 00256h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FMR27	—	—	FMR24	—	FMR22	FMR21	FMR20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FMR20	Erase-suspend enable bit (1)	0: Erase-suspend disabled 1: Erase-suspend enabled	R/W
b1	FMR21	Erase-suspend request bit (2)	0: Erase restart 1: Erase-suspend request	R/W
b2	FMR22	Interrupt request suspend request enable bit (1)	0: Erase-suspend request disabled by interrupt request 1: Erase-suspend request enabled by interrupt request	R/W
b3	—	Reserved	Set to 0.	R/W
b4	FMR24	High-speed read mode disable bit (1, 4)	0: High-speed read mode enabled 1: High-speed read mode disabled	R/W
b5	—	Reserved	Set to 0.	R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	FMR27	Low-current-consumption read mode enable bit (1, 3, 4)	0: Low-current-consumption read mode disabled 1: Low-current-consumption read mode enabled	R/W

Notes:
1. To set this bit to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
2. To set the FMR21 bit to 0 (erase restart), set it when the FMR01 bit in the FMR0 register is 1 (CPU rewrite mode enabled).
3. To use low-current-consumption read mode, set the FMR27 bit to 1 after setting any of the following:
   • Set the CPU clock to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
4. When the MCU exits wait mode or stop mode, if bits CM37 and CM36 (system clock select bits when exiting wait mode or stop mode) in the CM3 register are 10b (high-speed on-chip oscillator clock selected) or 11b (XIN clock selected), or if the CM35 bit in the CM3 register is 1 (no division), this bit is set to the value after reset.

FMR20 Bit (Erase-suspend enable bit)

When the FMR20 bit is set to 1 (enabled), the erase-suspend function is enabled.

FMR21 Bit (Erase-suspend request bit)

When the FMR21 bit is set to 1, erase-suspend mode is entered. If the FMR22 bit is 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request) when an interrupt request for the enabled interrupt is generated, and erase-suspend mode is entered. To restart auto-erasure, set the FMR21 bit to 0 (erase restart).

[Condition for setting to 0]
Set to 0 by a program.
[Conditions for setting to 1]
• When the FMR22 bit is 1 (erase-suspend request enabled by interrupt request) at the time an interrupt is generated.
• Set to 1 by a program.

FMR22 Bit (Interrupt request suspend request enable bit)

When the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request) when an interrupt request is generated during auto-erasure.
Set the FMR22 bit to 1 when using erase-suspend while rewriting the user ROM area in EW1 mode.

FMR24 Bit (High-speed read mode disable bit)

When the CPU clock > 20 MHz, set the FMR24 bit to 0.
When the CPU clock ≤ 20 MHz, set the FMR24 bit to 1.
Set the CPU clock to 20 MHz or less before setting the FMR24 bit to 1.

FMR27 Bit (Low-current-consumption read mode enable bit)

When the FMR27 bit is set to 1 (low-current-consumption read mode enabled) in low-speed on-chip oscillator mode (XIN clock stopped), power consumption when reading the flash memory can be reduced. Refer to **10.6.11 Low-Current-Consumption Read Mode** for details.
Low-current-consumption read mode can be used when the CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16. Do not use low-current-consumption read mode when the clock is divided by 1 (no division) or 2. After setting the division ratio of the CPU clock, set the FMR27 bit to 1.
When entering wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled), set bits CM37 and CM36 in the CM3 register to 00b (MCU exits using the CPU clock used immediately before entering wait or stop mode), and the CM35 bit to 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled).
When the FMR27 bit is 1 (low-current-consumption read mode enabled), do not execute any program, block erase, or lock bit program commands. To change the FMSTP bit from 1 (flash memory stops) to 0 (flash memory operates), make the setting when the FMR27 bit is 0 (low-current-consumption read mode disabled).

27.3.5 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bits (2)	b5 b4 0 0: 3.80 V (typ.) selected (Vdet0_3) 0 1: 2.85 V (typ.) selected (Vdet0_2) Other than the above: Do not set.	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not perform any additional writes to the OFS register. Erasing the block including the OFS register sets the OFS register to FFh. The value of the OFS register is FFh at shipment of blank products. After programming, the value is the same as that programmed by the user. At shipment of factory-programmed products, the value of the OFS register is the same as that set in a program by the user.
2. The same voltage detection 0 level selected by bits VDSEL0 and VDSEL1 is set in both the voltage monitor 0 reset and power-on reset functions.
3. Set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset) to use the power-on reset or voltage monitor 0 reset.

For an example of the OFS register settings, refer to **5.6.1 Option Function Select Area Setting Examples**.

LVDAS Bit (Voltage detection 0 circuit start bit)

The Vdet0 voltage monitored in the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

27.4 Functions to Prevent Flash Memory from being Rewritten

Standard serial I/O mode has an ID code check function, and parallel I/O mode has a ROM code protect function to prevent the flash memory from being read or rewritten easily.

27.4.1 ID Code Check Function

The ID code check function is used in standard serial I/O mode. If the 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to any value other than FFFFFFh, the ID codes sent from the serial programmer or the on-chip debugging emulator and the 7-byte ID codes written in the flash memory are checked to see if they match. If the ID codes do not match, the commands sent from the serial programmer or the on-chip debugging emulator are not accepted. Refer to **5.3 ID Code Area** for details on the ID code check function.

27.4.2 ROM Code Protect Function

The ROM protect function prevents the contents of the flash memory from being read, rewritten, or erased using the OFS register in parallel I/O mode.
Refer to **5.5 Option Function Select Area** for details on the option function select area.

The ROM code protect function is enabled by writing 1 to the ROMCR bit and writing 0 to the ROMCP1 bit. This prevents the contents of the on-chip flash memory from being read or rewritten.
Once ROM code protection is enabled, the contents of the internal flash memory cannot be rewritten in parallel I/O mode. To disable ROM code protection, erase the block including the OFS register using CPU rewrite mode or standard serial I/O mode.

27.5 CPU Rewrite Mode

In CPU rewrite mode, the user ROM area can be rewritten by executing software commands from the CPU. Therefore, the user ROM area can be rewritten directly while the MCU is mounted on a board without using a ROM programmer. These software commands must only be executed for blocks in the user ROM area.
The flash module has an erase-suspend function which halts the erase operation temporarily during an erase operation in CPU rewrite mode. During erase-suspend, the flash memory can be read or programmed.
Erase-write 0 mode (EW0 mode) and erase-write 1 mode (EW1 mode) are available in CPU rewrite mode.
Table 27.4 lists the Differences between EW0 Mode and EW1 Mode.

Table 27.4 Differences between EW0 Mode and EW1 Mode

Item	EW0 Mode	EW1 Mode
Operating mode	Single-chip mode	Single-chip mode
Rewrite control program allocatable areas	User ROM	User ROM
Rewrite control program executable areas	RAM (The rewrite control program must be transferred before being executed.) However, the program can be executed in the program ROM area when rewriting the data flash area.	User ROM or RAM
Rewritable areas	User ROM	User ROM (However, blocks which contain the rewrite control program are excluded.)
Software command restrictions	—	Program and block erase commands (Must not be executed for any block which contains the rewrite control program.)
Mode after programming or block erasure or after entering erase-suspend	Read array mode	Read array mode
CPU and DTC state during programming and block erasure	The CPU and DTC operate.	• The CPU or DTC operates while the data flash area is being programmed or block erased. • The CPU or DTC is put in a hold state while the program ROM area is being programmed or block erased (I/O ports retain the state before the command execution).
Flash memory status detection	Read bits FST7, FST5, and FST4 in the FST register by a program.	Read bits FST7, FST5, and FST4 in the FST register by a program.
Conditions for entering erase-suspend	• Set bits FMR20 and FMR21 in the FMR2 register to 1 by a program. • Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.	• Set bits FMR20 and FMR21 in the FMR2 register to 1 by a program (while rewriting the data flash area). • Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.
CPU clock	32 MHz	32 MHz

27.5.1 EW0 Mode

When the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled), the MCU enters CPU rewrite mode and software commands can be accepted. Since the FMR02 bit in the FMR0 register is set to 0 at this time, EW0 mode is selected.

Software commands are used to control program and erase operations. The FST register can be used to confirm whether programming or erasure has completed.

To enter erase-suspend during auto-erasure, set the FMR20 bit to 1 (erase-suspend enabled) and the FMR21 bit to 1 (erase-suspend request). Next, verify that the FST7 bit in the FST register is set to 1 (ready), and then verify that the FST6 bit is set to 1 (during erase-suspend) before accessing the flash memory. When the FST6 bit is set to 0, erasure completes.

When the FMR21 bit in the FMR2 register is set to 0 (erase restart), auto-erasure restarts. To confirm whether auto-erasure has restarted, verify that the FST7 bit in the FST register is set to 0, and then verify that the FST6 bit is set to 0 (other than erase-suspend).

27.5.2 EW1 Mode

After the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled), EW1 mode is selected by setting the FMR02 bit to 1.

The FST register can be used to confirm whether programming or erasure has completed.

To enable the erase-suspend function during auto-erasure, execute the block erase command after setting the FMR20 bit in the FMR2 register to 1 (suspend enabled). To enter erase-suspend while auto-erasing the user ROM area, set the FMR22 bit in the FMR2 register to 1 (erase-suspend request enabled by interrupt request). Also, the interrupt to enter erase-suspend must be enabled in advance.

When an interrupt request is generated, the FMR21 bit in the FMR2 register is automatically set to 1 (erase-suspend request) and auto-erasure suspends after td(SR-SUS). After interrupt handling completes, set the FMR21 bit to 0 (erase restart) to restart auto-erasure.

27.5.3 Setting and Cancelling Each Mode

Figure 27.3 shows Setting and Cancelling EW0 Mode and Figure 27.4 shows Setting and Cancelling EW0 Mode (when Rewriting Data Flash) and EW1 Mode.

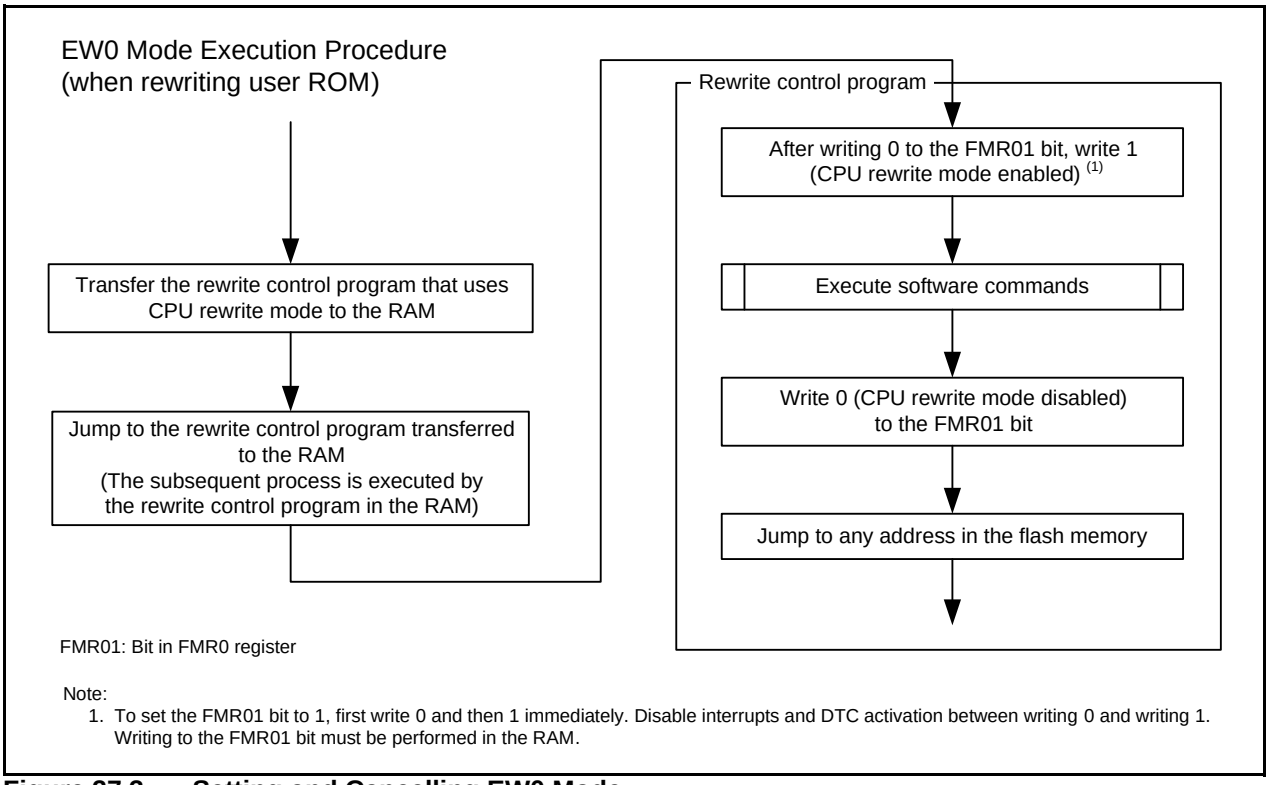


Figure 27.3 Setting and Cancelling EW0 Mode

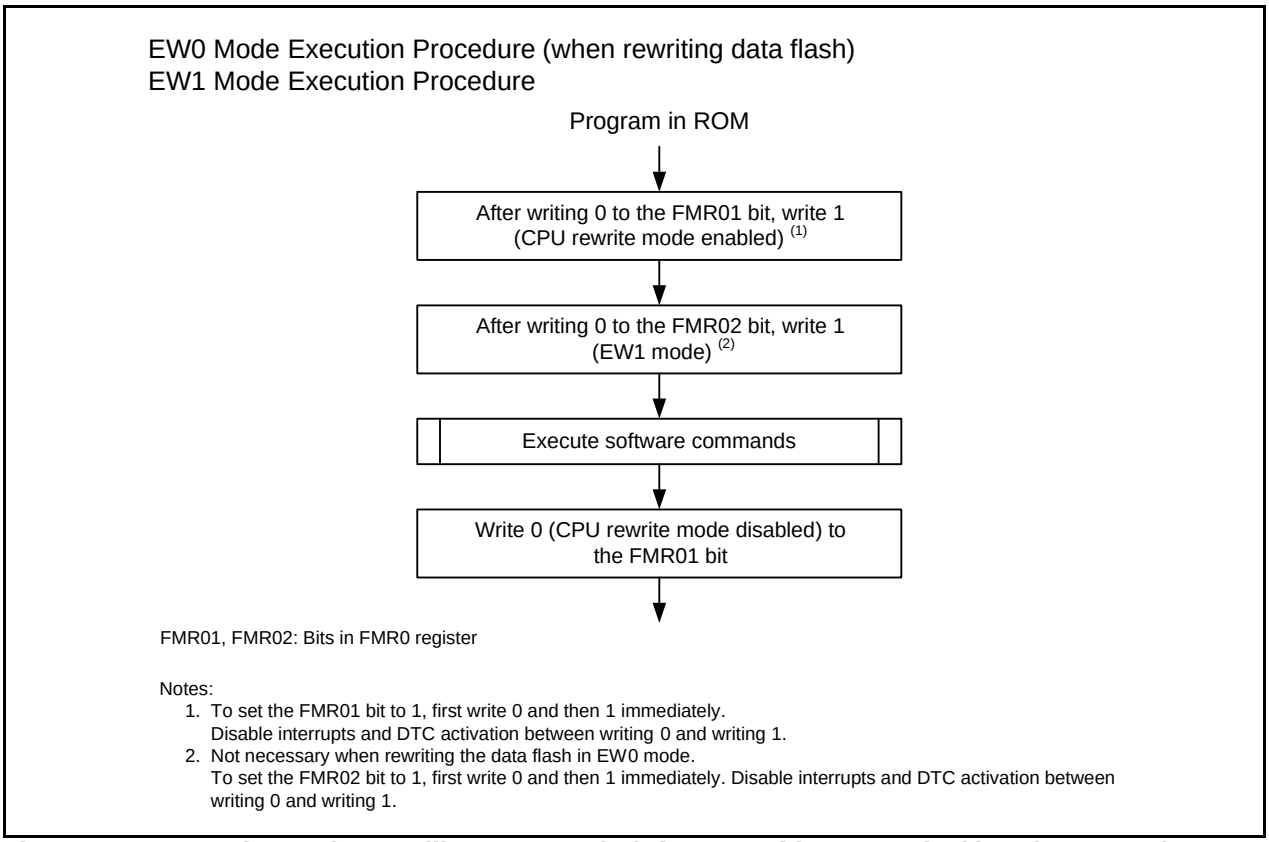


Figure 27.4 Setting and Cancelling EW0 Mode (when Rewriting Data Flash) and EW1 Mode

27.5.4 Suspend Operation

The suspend function halts the auto-erase operation temporarily during auto-erasure.
When auto-erasure is suspended, the next operation can be executed (refer to **Table 27.5 Executable Operation during Suspend**).

- When auto-erasure of any block in data flash is suspended, auto-programming and reading of another block can be executed.
- When auto-erasure of data flash is suspended, auto-programming and reading of program ROM can be executed.
- When auto-erasure of any block in program ROM is suspended, auto-programming and reading of another block can be executed.
- When auto-erasure of program ROM is suspended, auto-programming and reading of data flash can be executed.
- To check the suspend, verify that the FST7 bit in the FST register is set to 1 (ready), and then verify that the FST6 bit in the FST register is set to 1 (during erase-suspend) to confirm whether erasure has been suspended. When the FST6 bit is set to 0 (other than erase-suspend), erasure has completed.

Figure 27.5 shows the Suspend Operation Timing.

Table 27.5 Executable Operation during Suspend

		Operation during Suspend											
		Data flash (Block during erasure execution before entering suspend)			Data flash (Block during no erasure execution before entering suspend)			Program ROM (Block during erasure execution before entering suspend)			Program ROM (Block during no erasure execution before entering suspend)		
		Erase	Program	Read	Erase	Program	Read	Erase	Program	Read	Erase	Program	Read
Areas during erasure execution before entering suspend	Data flash	D	D	D	D	E	E	N/A	N/A	N/A	D	E	E (6)
	Program ROM	N/A	N/A	N/A	D	E	E	D	D	D	D	E	E

Notes:
1. E indicates operation is enabled by using the suspend function, D indicates operation is disabled, and N/A indicates no combination is available.
2. Operation cannot be suspended during programming.
3. The block erase command can be executed for erasure. The program, lock bit program, and read lock bit status commands can be executed for programming.
   The clear status register command can be executed when the FST7 bit in the FST register is set to 1 (ready).
4. The MCU enters read array mode immediately after entering erase-suspend.
5. Applicable only to products with on-chip data flash.
6. The program ROM area can be read with the BGO function while programming or block erasing data flash.

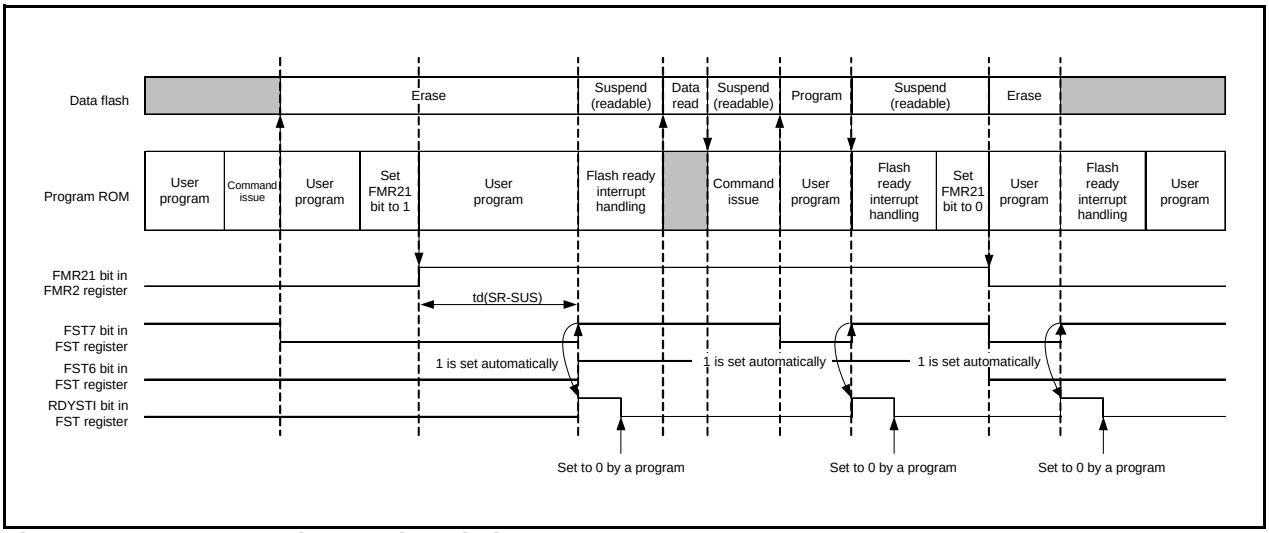


Figure 27.5 Suspend Operation Timing

27.5.5 BGO (Background Operation) Function

The array data can be read when the program ROM area is specified during a data flash program or block erase operation. This eliminates the need to write software commands. The access time is the same as that for normal read operations.
Note that other data flash blocks cannot be read during a data flash program or block erase operation.
Figure 27.6 shows the BGO Function.

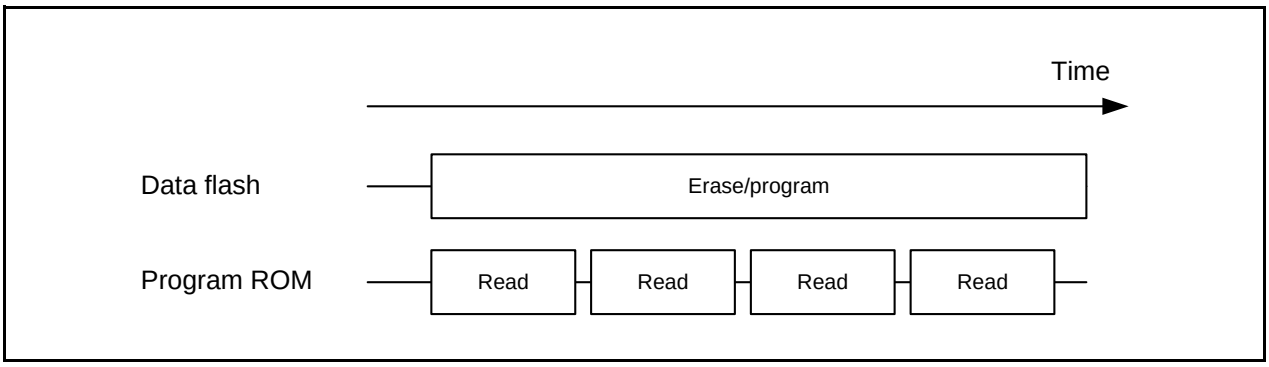


Figure 27.6 BGO Function

27.5.6 Data Protect Function

Each block in the flash memory has a nonvolatile lock bit. The lock bit is enabled by setting the FMR13 bit in the FMR1 register to 0 (lock bit enabled). The lock bit can be used to disable (lock) programming or erasing each block. This prevents data from being written or erased inadvertently. The block status changes according to the lock bit as follows:

• When the lock bit data is set to 0: locked (the block cannot be programmed or erased)
• When the lock bit data is set to 1: not locked (the block can be programmed and erased)

The lock bit data is set to 0 (locked) by executing the lock bit program command and to 1 (not locked) by erasing the block. There are no commands that can be used to set only the lock bit data to 1.
The lock bit data can be read using the read lock bit status command.

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit function is disabled and no blocks are locked (each lock bit data remains unchanged). The lock bit function is enabled by setting the FMR13 bit to 0 (the lock bit data is retained).
When the block erase command is executed while the FMR13 bit is 1, the target block is erased regardless of the lock bit status. The lock bit of the erase target block is set to 1 after erasure completes.
Refer to **27.5.7 Software Commands** for the details on the individual commands.
The FMR13 bit is set to 0 after auto-erasure completes. This bit is also set to 0 if one of the following conditions is met. To erase or program a different locked block, set the FMR 13 bit to 1 again and execute the block erase or program command.

• If the FST7 bit in the FST register is changed from 0 (busy) to 1 (ready).
• If a command sequence error occurs.
• If the FMR01 bit in the FMR0 register is set to 0 (CPU mode disabled).
• If the FMSTP bit in the FM0 register is set to 1 (flash memory stops).
• If the CMDRST bit in the FMR0 register is set to 1 (erasure/writing stops).

Figure 27.7 shows the FMR13 Bit Operation Timing.

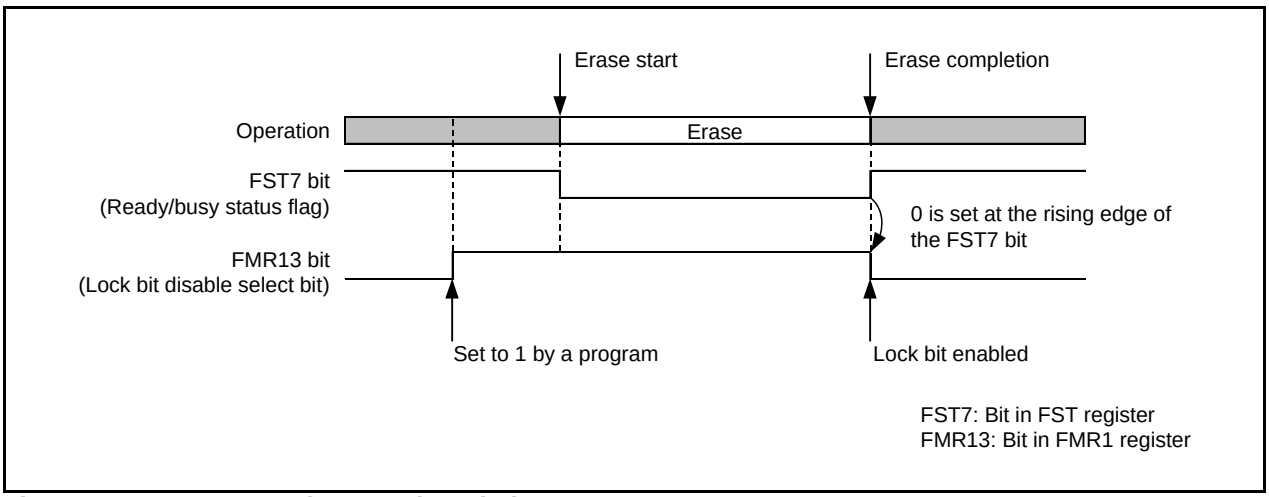


Figure 27.7 FMR13 Bit Operation Timing

27.5.7 Software Commands

The software commands are described below. Commands and data must be read and written in 8-bit units. However, commands and data of programming (word units) must be written in 16-bit units.
Do not input any command other than those listed in the table below.

Table 27.6 Software Commands

Command	First Bus Cycle			Second Bus Cycle		
	Mode	Address	Data	Mode	Address	Data
Read array	Write	×	FFh	—	—	—
Clear status register	Write	×	50h	—	—	—
Program	Write	WA	40h	Write	WA	WD
Block erase	Write	×	20h	Write	BA	D0h
Lock bit program	Write	BT	77h	Write	BT	D0h
Read lock bit status	Write	×	71h	Write	BT	D0h

WA: Write address
WD: Write data
BA: Any address of the block
BT: Start address of the block
×: Any address in the user ROM area

27.5.7.1 Read Array Command

The read array command is used to read the flash memory.
When FFh is written in the first bus cycle, the MCU enters read array mode. When the read address is input in the following bus cycles, the content of the specified address can be read in 8-bit units.
Since read array mode is remained until another command is written, the contents of multiple addresses can be read continuously.
In addition, after a reset, the MCU enters read array mode after a program, block erase, read lock bit status, or clear status register command, or after entering erase-suspend.

27.5.7.2 Clear Status Register Command

The clear status register command is used to set bits FST4 and FST5 in the FST register to 0.
When 50h is written in the first bus cycle, bits FST4 and FST5 in the FST register are set to 0.

27.5.7.3 Program Command

The program command is used to write data to the flash memory in 1-byte units.
When 40h is written in the first bus cycle and data is written in the second bus cycle to the write address, auto-programming (data program and verify operation) starts. Make sure the address value specified in the first bus cycle is the same address as the write address specified in the second bus cycle.
The FST7 bit in the FST register can be used to confirm whether auto-programming has completed. The FST7 bit is set to 0 during auto-programming and is set to 1 when auto-programming completes.
After auto-programming has completed, the auto-program result can be confirmed by the FST4 bit in the FST register (refer to **27.5.8 Full Status Check**).
Do not perform additional writes to previously programmed addresses.

The program command targeting each block in the program ROM can be disabled using the lock bit.
The following commands are not accepted under the following conditions:
- Program commands targeting data flash block A when the FMR14 bit in the FMR1 register is set to 1 (rewrite disabled).
- Program commands targeting data flash block B when the FMR15 bit is set to 1 (rewrite disabled).
- Program commands targeting data flash block C when the FMR16 bit is set to 1 (rewrite disabled).
- Program commands targeting data flash block D when the FMR17 bit is set to 1 (rewrite disabled).

Figure 27.8 shows the Program Flowchart (Flash Ready Status Interrupt Disabled) and Figure 27.9 shows the Program Flowchart (Flash Ready Status Interrupt Enabled).

In EW1 mode, do not execute this command for any address where the rewrite control program is allocated.

When the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled), a flash ready status interrupt can be generated upon completion of auto-programming. The auto-program result can be confirmed by reading the FST register during the interrupt routine.

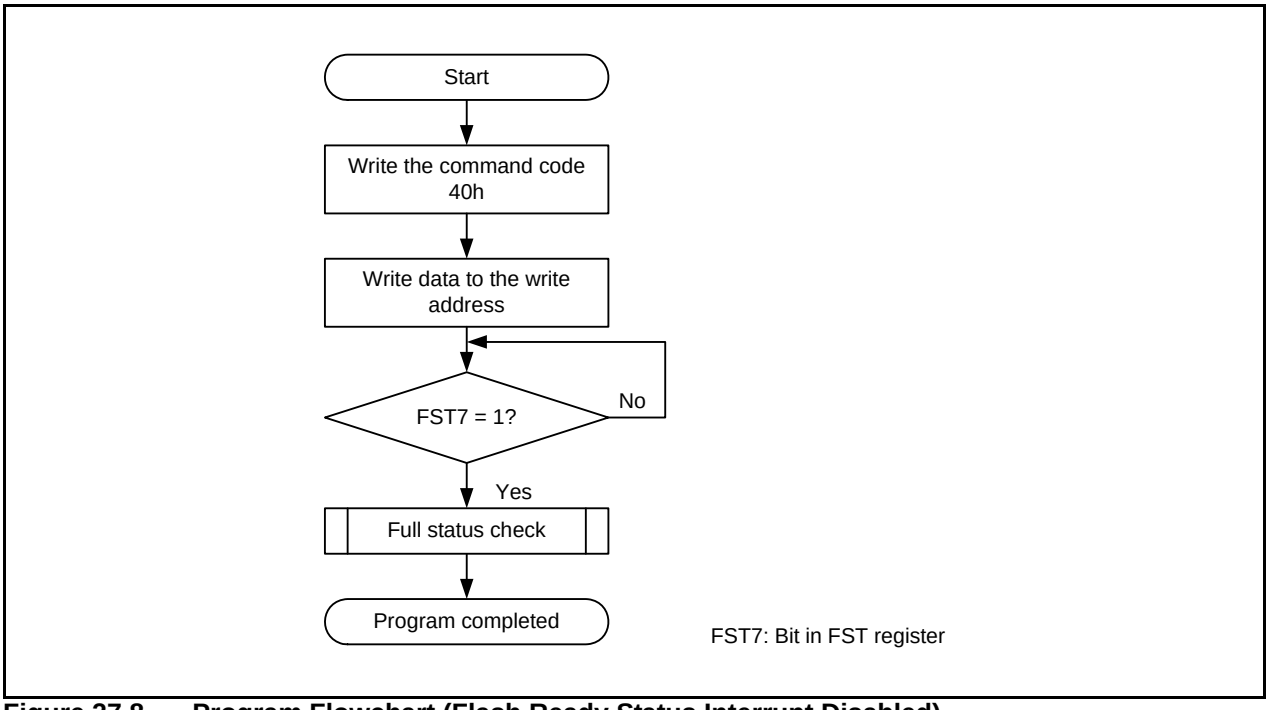


Figure 27.8 Program Flowchart (Flash Ready Status Interrupt Disabled)

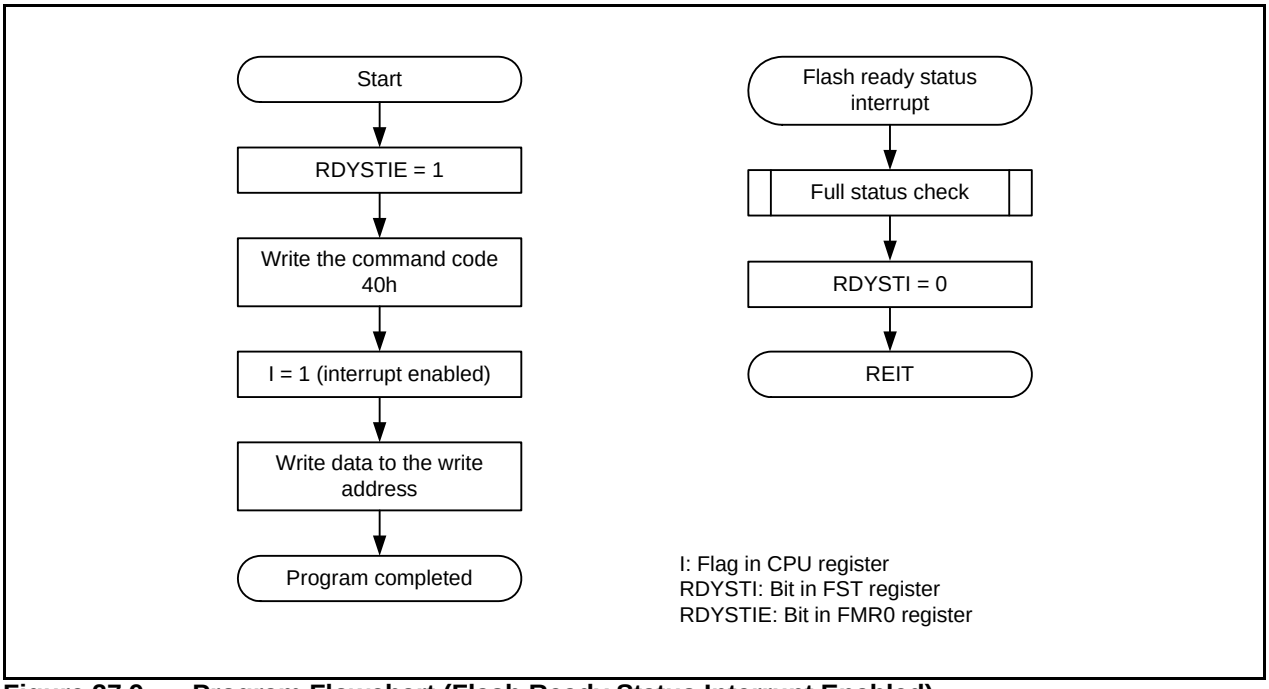


Figure 27.9 Program Flowchart (Flash Ready Status Interrupt Enabled)

27.5.7.4 Block Erase Command

When 20h is written in the first bus cycle and then D0h is written in the second bus cycle to any address of the block, auto-erasure (erase and erase verify operation) starts in the specified block.
The FST7 bit in the FST register can be used to confirm whether auto-erasure has completed. The FST7 bit is set to 0 during auto-erasure and is set to 1 when auto-erasure completes. After auto-erasure completes, all data in the block is set to FFh.
After auto-erasure has completed, the auto-erase result can be confirmed by the FST5 bit in the FST register (refer to **27.5.8 Full Status Check**).

The block erase command targeting each block in the program ROM can be disabled using the lock bit.
The following commands are not accepted under the following conditions:
- Block erase commands targeting data flash block A when the FMR14 bit in the FMR1 register is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block B when the FMR15 bit is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block C when the FMR16 bit is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block D when the FMR17 bit is set to 1 (rewrite disabled).

Figure 27.10 shows the Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled), Figure 27.11 shows the Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled), Figure 27.12 shows the Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Enabled and Suspend Enabled), and Figure 27.13 shows the Block Erase Flowchart in EW1 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled).

In EW1 mode, do not execute this command for any block where the rewrite control program is allocated.

While the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled), a flash ready status interrupt can be generated upon completion of auto-erasure. While the RDYSTIE bit is set to 1 and the FMR20 bit in the FMR2 register is set to 1 (erase-suspend enabled), a flash ready status interrupt is generated when the FMR21 bit is set to 1 (erase-suspend request) and auto-erasure suspends. The auto-erase result can be confirmed by reading the FST register during the interrupt routine.

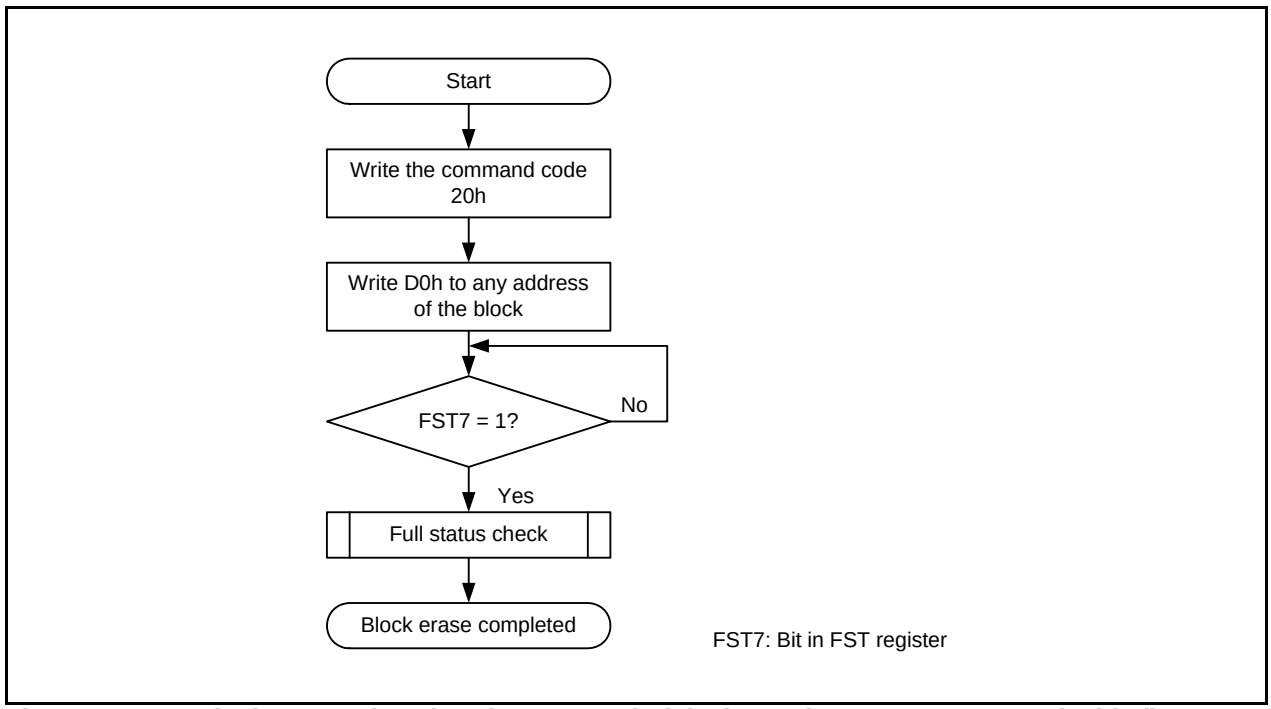
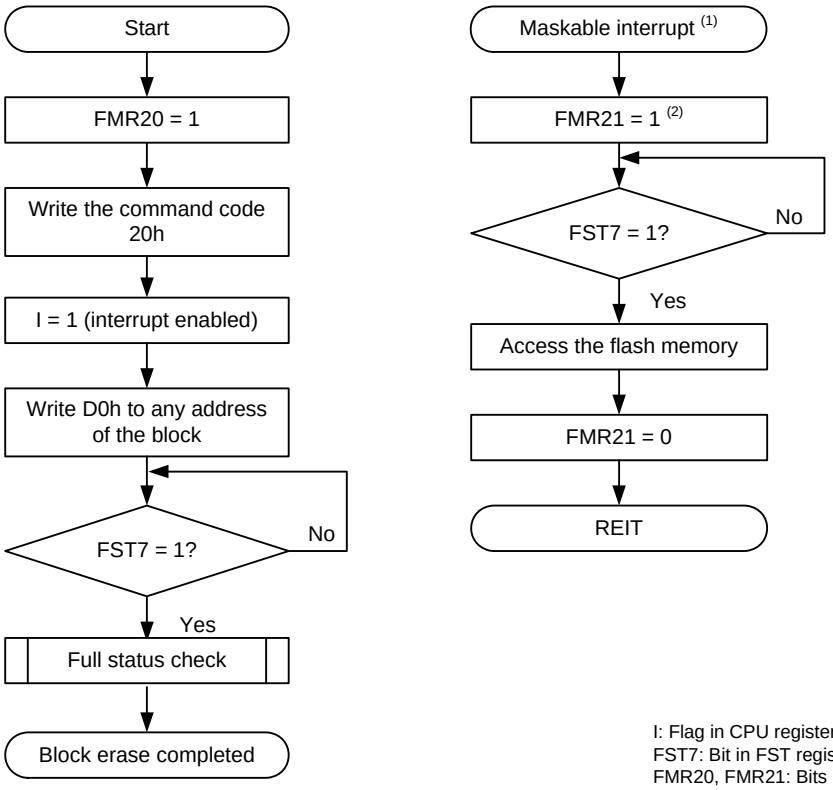
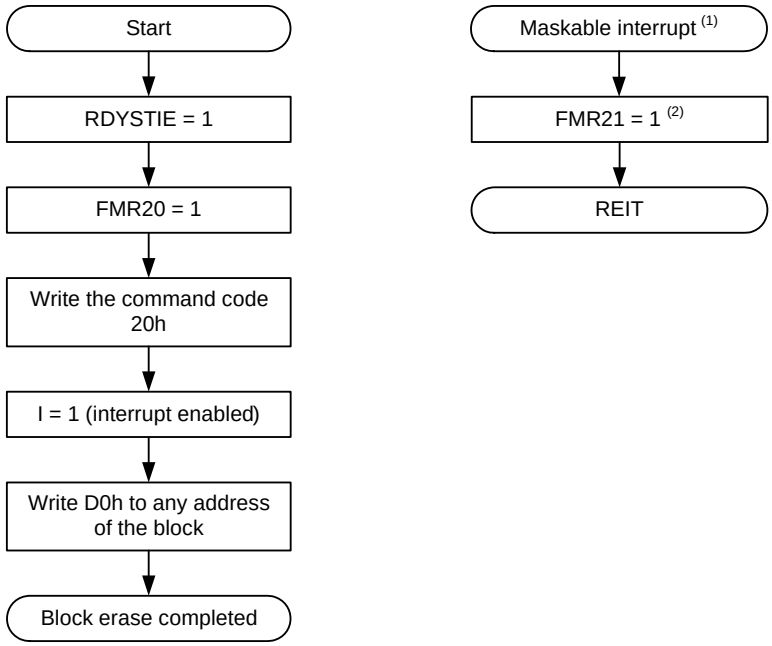


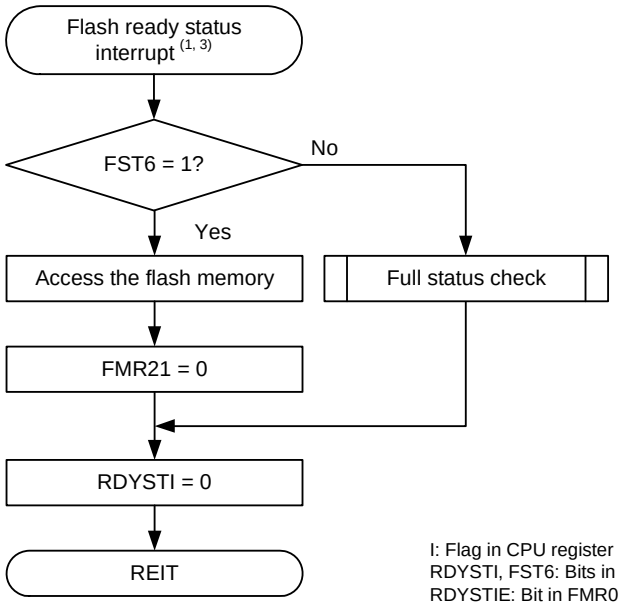
Figure 27.10 Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled)



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the erase target area.
2. Time td(SR-SUS) is required from when the FMR21 bit is set to 1 until suspend is acknowledged. The interrupt used to enter suspend must be enabled beforehand.

Figure 27.11 Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)





I: Flag in CPU register
RDYSTI, FST6: Bits in FST register
RDYSTIE: Bit in FMR0 register
FMR20, FMR21: Bits in FMR2 register

Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the erase target area.
2. Time td(SR-SUS) is required from when the FMR21 bit is set to 1 until suspend is acknowledged. The interrupt used to enter suspend must be enabled beforehand.
3. When auto-erasure suspends, a flash ready status interrupt is generated.

Figure 27.12 Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Enabled and Suspend Enabled)

When the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) when an interrupt request is generated during auto-erasure. Set the FMR22 bit to 1 when suspend is used while the user ROM area is auto-erased in EW1 mode.

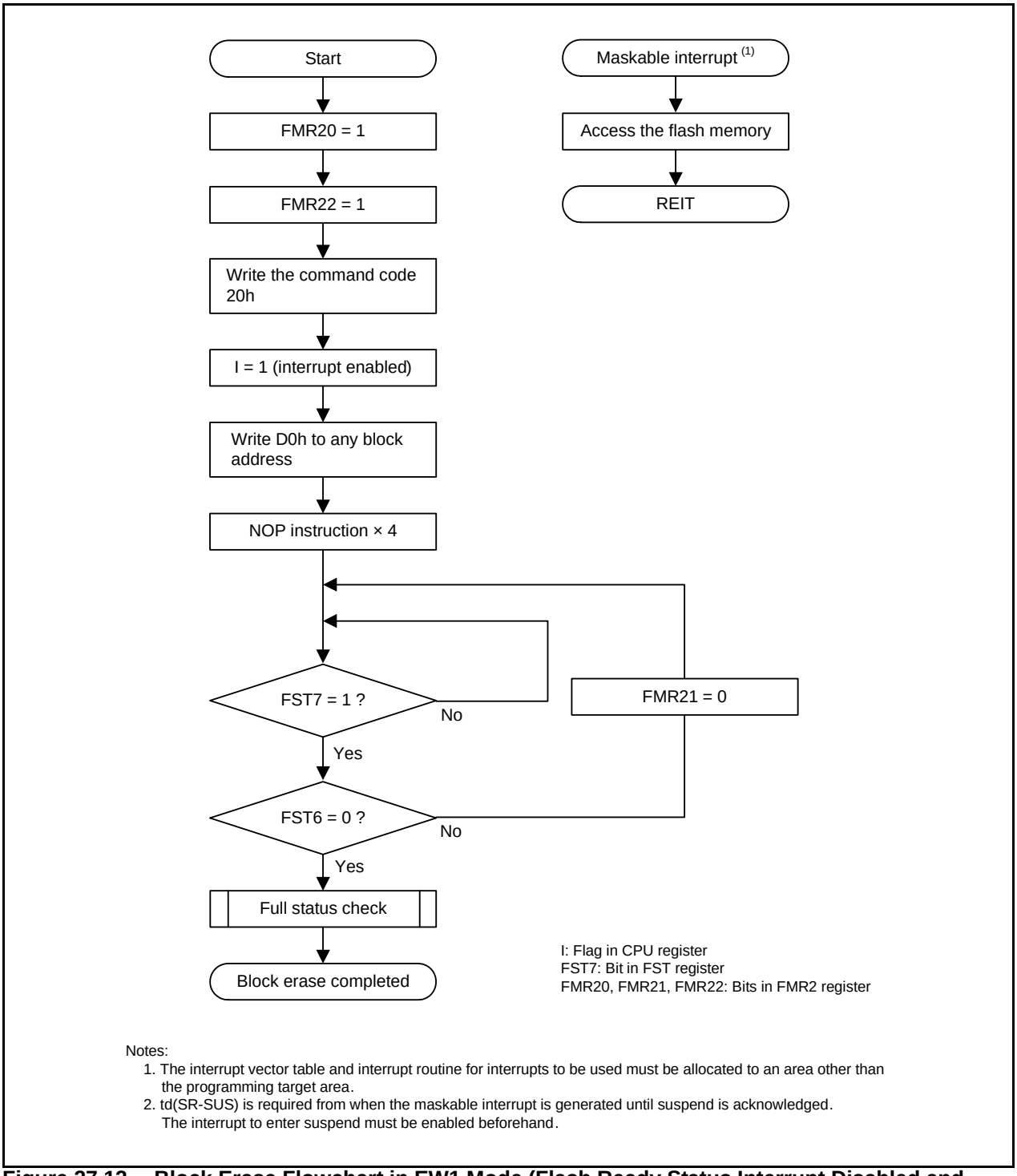


Figure 27.13 Block Erase Flowchart in EW1 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)

27.5.7.5 Lock Bit Program Command

This command is used to set the lock bit of any block in the program ROM area to 0 (locked).
When 77h is written in the first bus cycle and D0h is written in the second bus cycle to the start address of the block, 0 is written to the lock bit of the specified block. Make sure the address value in the first bus cycle is the same address as the start address of the block specified in the second bus cycle.
Figure 27.14 shows the Lock Bit Program Flowchart. The lock bit status (lock bit data) can be read using the read lock bit status command.
The FST7 bit in the FST register can be used to confirm whether writing to the lock bit has completed.
Refer to **27.5.6 Data Protect Function** for the lock bit function and how to set the lock bit to 1 (not locked).

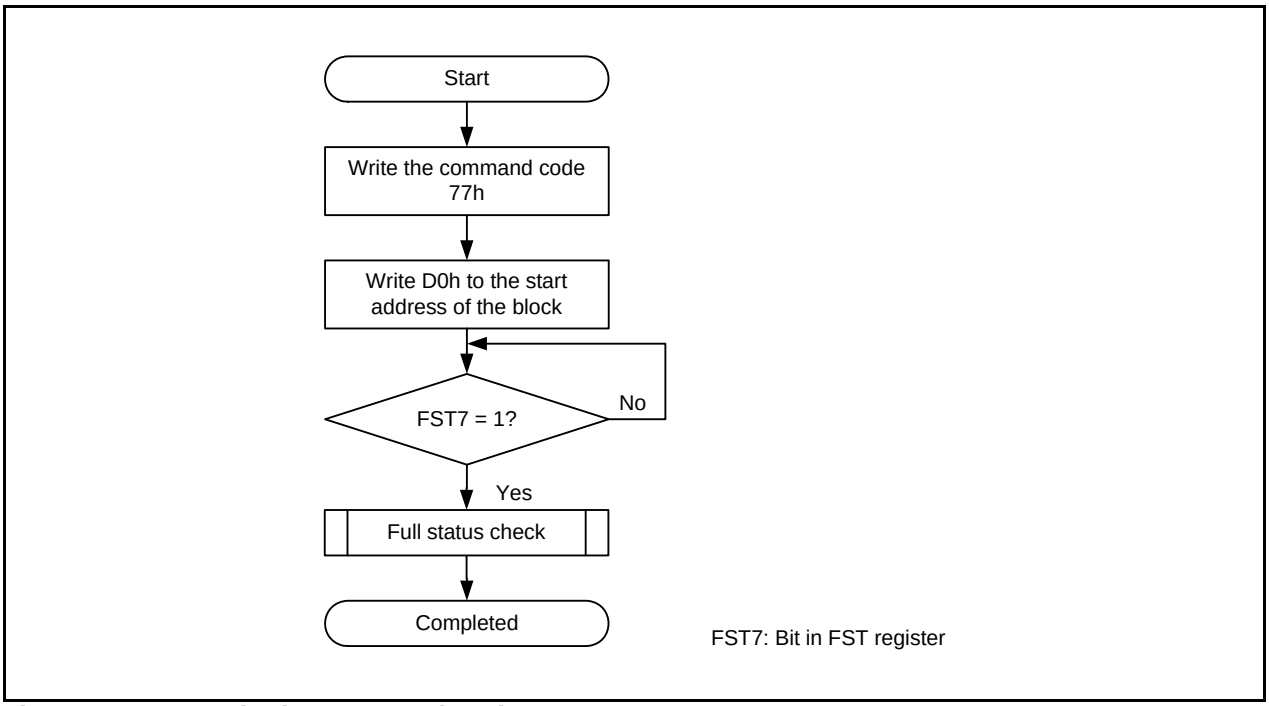


Figure 27.14 Lock Bit Program Flowchart

27.5.7.6 Read Lock Bit Status Command

This command is used to read the lock bit status of any block in the program ROM area.
When 71h is written in the first bus cycle and D0h is written in the second cycle to the start address of the block, the lock bit status of the specified block is stored in the LBDATA bit in the FST register. After the FST7 bit in the FST register has been set to 1 (ready), read the LBDATA bit.
Figure 27.15 shows the Read Lock Bit Status Flowchart.

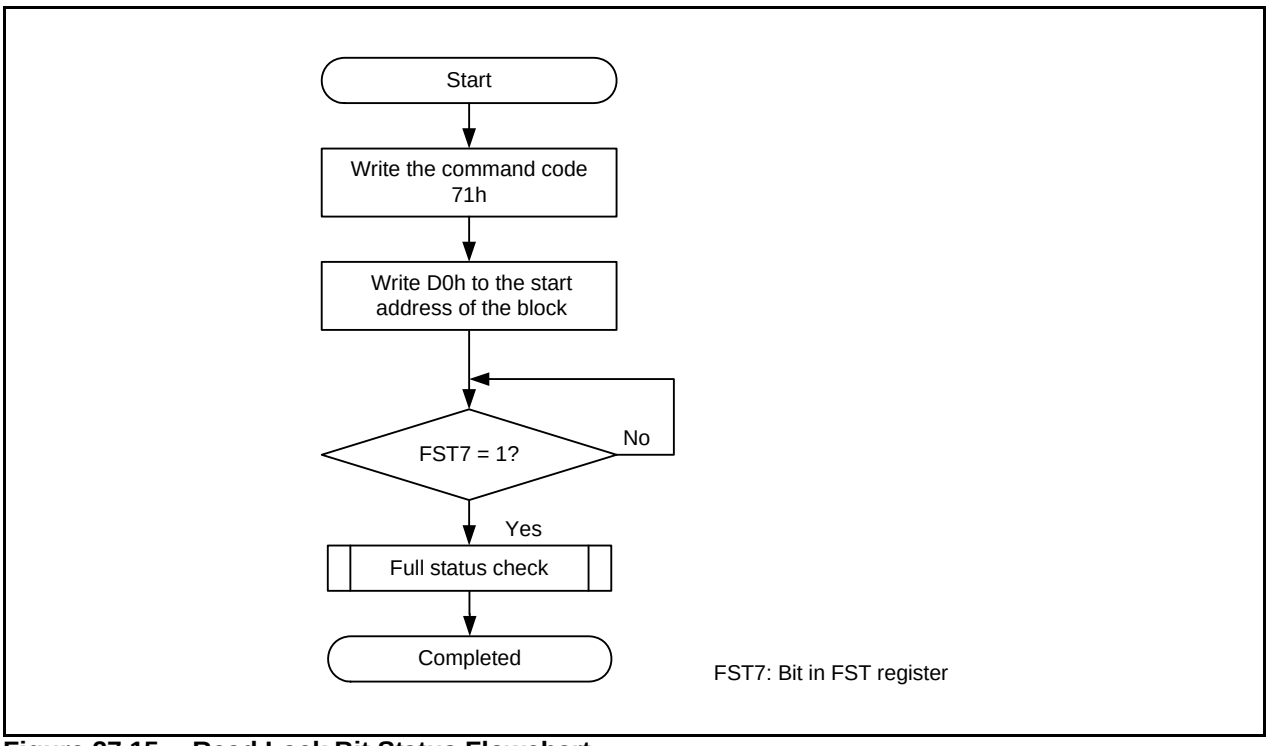


Figure 27.15 Read Lock Bit Status Flowchart

27.5.8 Full Status Check

If an error occurs, bits FST4 and FST5 in the FST register are set to 1, indicating the occurrence of an error. The execution result can be confirmed by checking these status bits (full status check).
Table 27.7 lists the Errors and FST Register Status. Figure 27.16 shows the Full Status Check and Handling Procedure for Individual Errors.

Table 27.7 Errors and FST Register Status

FST Register Status		Error	Error Occurrence Condition
FST5	FST4		
1	1	Command sequence error	• When a command is not written correctly. • When data other than valid data (i.e., D0h or FFh) is written in the second bus cycle of the block erase command. (1) • The erase command is executed during suspend • A command is executed for a block during suspend
1	0	Erase error	When the block erase command is executed, but auto-erasure does not complete correctly.
0	1	Program error/ lock bit program error	When the program command is executed, but auto-programming does not complete correctly.

Note:
1. When FFh is written in the second bus cycle of these commands, the MCU enters read array mode. At the same time, the command code written in the first bus cycle becomes invalid.

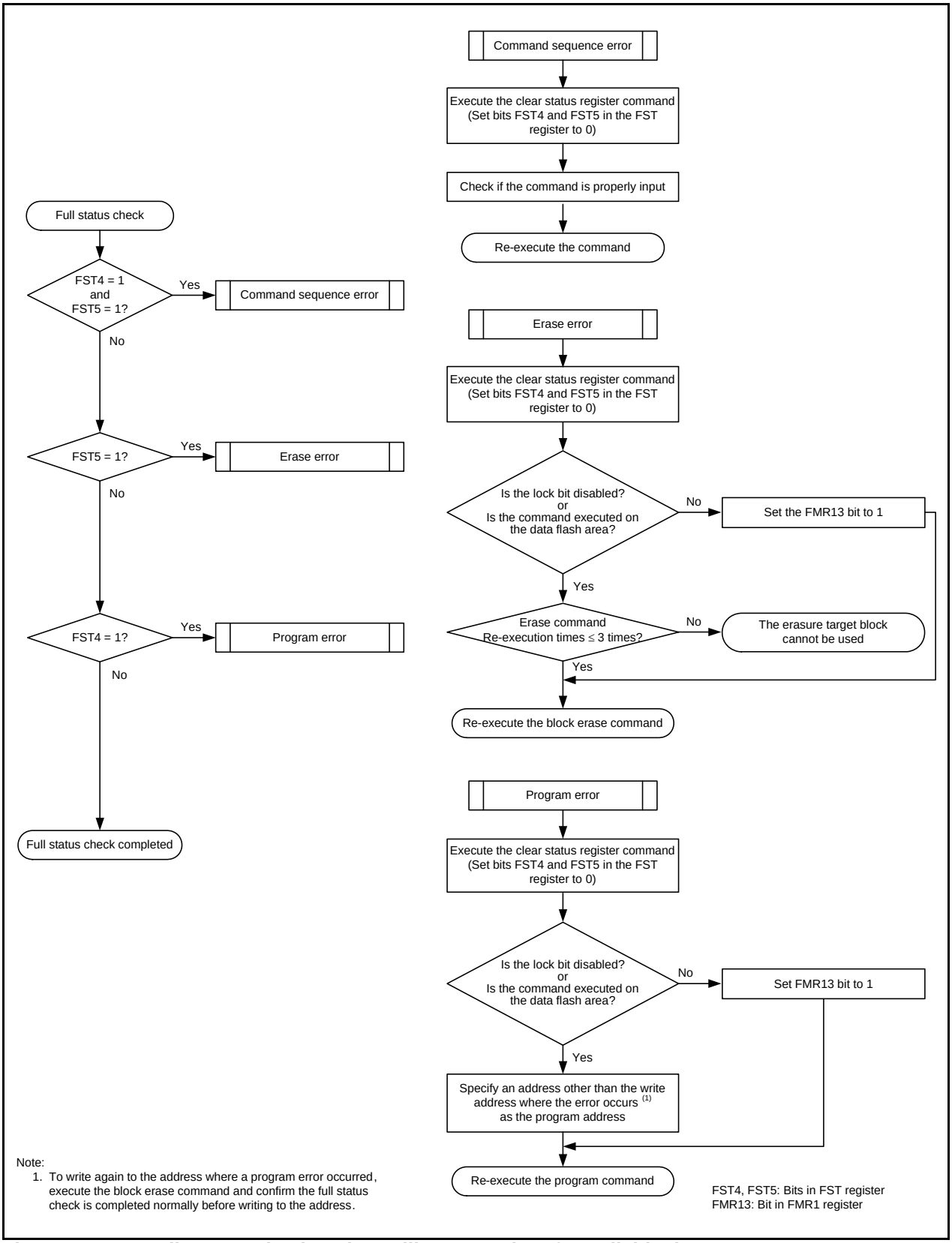


Figure 27.16 Full Status Check and Handling Procedure for Individual Errors

27.6 Standard Serial I/O Mode

In standard serial I/O mode, a serial programmer which supports the MCU can be used to rewrite the user ROM area while the MCU is mounted on-board.
There are three types of standard serial I/O modes:

- Standard serial I/O mode 1 ..... Clock synchronous serial I/O used to connect to a serial programmer
- Standard serial I/O mode 2 ..... Clock asynchronous serial I/O used to connect to a serial programmer
- Standard serial I/O mode 3 ..... Special clock asynchronous serial I/O used to connect to a serial programmer

Standard serial I/O mode 2 and standard serial I/O mode 3 can be used for the MCU.

Refer to **Appendix 2. Connection Examples between Serial Programmer and On-Chip Debugging Emulator** for examples of connecting to a serial programmer. Contact the serial programmer manufacturer for more information. Refer to the user's manual included with your serial programmer for instructions.

Table 27.8 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 2) and Figure 27.17 shows Pin Handling in Standard Serial I/O Mode 2. Table 27.9 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 3) and Figure 27.18 shows Pin Handling in Standard Serial I/O Mode 3.
After handling the pins shown in Table 27.8 and rewriting the flash memory using the programmer, apply a high-level signal to the MODE pin and reset the hardware to run the program in the flash memory in single-chip mode.

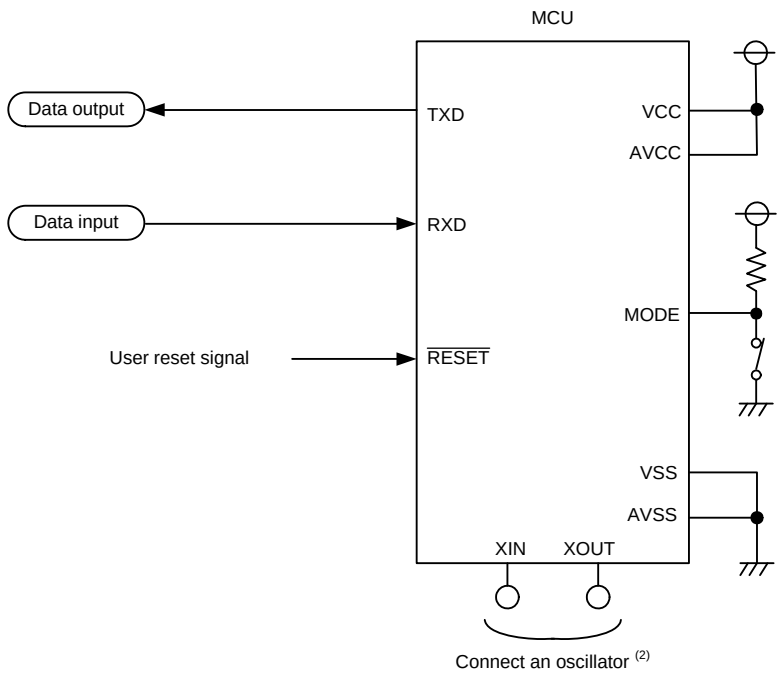
27.6.1 ID Code Check Function

The ID code check function determines whether the ID codes sent from the serial programmer and those written in the flash memory match.
Refer to **5.3 ID Code Area** for details on the ID code check function.

Table 27.8 Pin Functions (Flash Memory Standard Serial I/O Mode 2)

Pin	Name	I/O	Description
VCC, VSS	Power supply input		Apply the guaranteed programming and erasure voltage to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin.
P4_6/XIN	P4_6 input/clock input	I	If an external oscillator is connected, connect a ceramic resonator or crystal oscillator between pins XIN and XOUT. To use as an input port, input a high-level or low-level signal, or leave the pin open.
P4_7/XOUT	P4_7 input/clock output	I/O	
MODE	MODE	I/O	Input a low-level signal.
P1_4	TXD output	O	Serial data output pin.
P1_5	RXD input	I	Serial data input pin.

Note:
1. For I/O ports other than the above, apply a high-level, or low-level signal or leave them open.



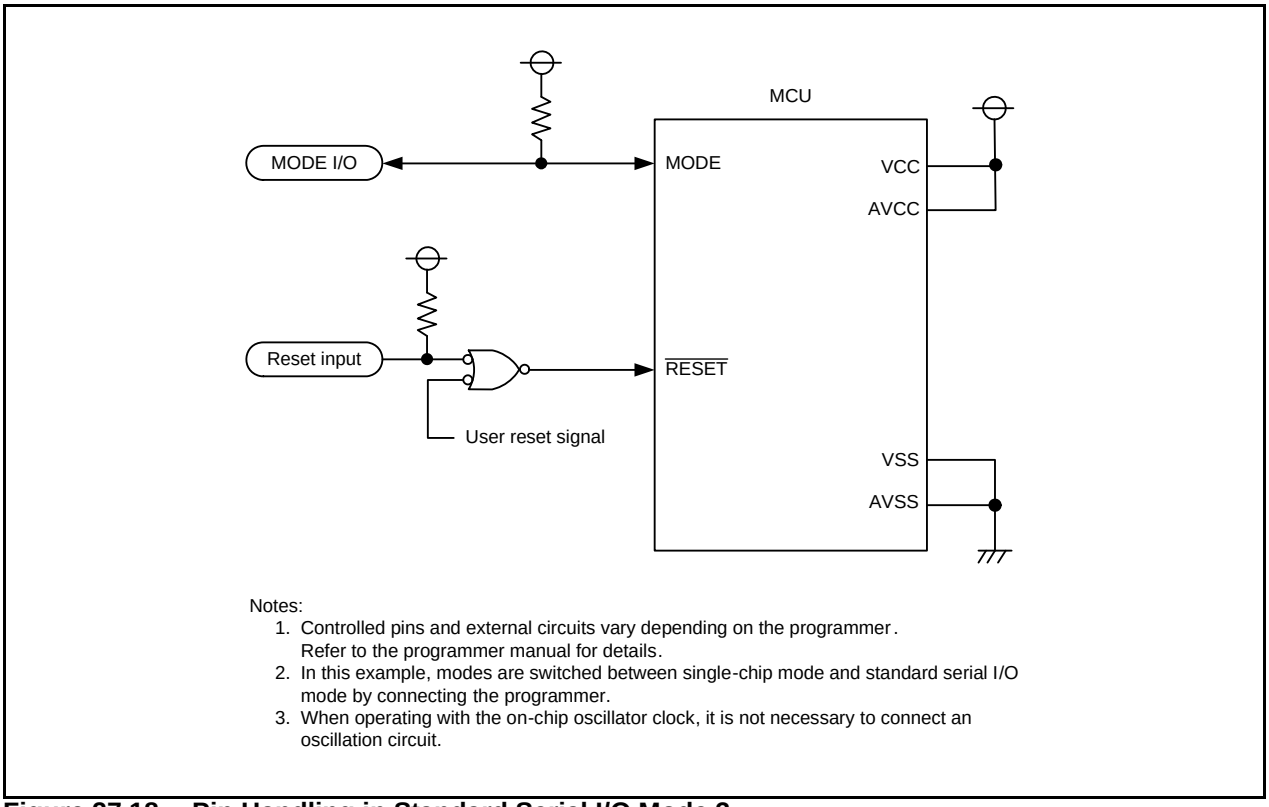
Notes:
1. In this example, modes are switched between single-chip mode and standard serial I/O mode by controlling the MODE input with a switch.
2. When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit.

Figure 27.17 Pin Handling in Standard Serial I/O Mode 2

Table 27.9 Pin Functions (Flash Memory Standard Serial I/O Mode 3)

Pin	Name	I/O	Description
VCC, VSS	Power supply input		Apply the guaranteed programming and erasure voltage to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin.
P4_6/XIN	P4_6 input/clock input	I	If an external oscillator is connected, connect a ceramic resonator or crystal oscillator between pins XIN and XOUT. To use as an input port, input a high-level or low-level signal, or leave the pin open.
P4_7/XOUT	P4_7 input/clock output	I/O	
MODE	MODE	I/O	Serial data I/O pin. Connect this pin to the programmer.

Note:
1. For I/O ports other than the above, apply a high-level or low-level signal, or leave them open.



Notes:
1. Controlled pins and external circuits vary depending on the programmer. Refer to the programmer manual for details.
2. In this example, modes are switched between single-chip mode and standard serial I/O mode by connecting the programmer.
3. When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit.

Figure 27.18 Pin Handling in Standard Serial I/O Mode 3

27.7 Parallel I/O Mode

Parallel I/O mode is used to input and output software commands, addresses, and data necessary to control (read, program, and erase) the on-chip flash memory.
Use a parallel programmer which supports the MCU. Contact the parallel programmer manufacturer for more information. Refer to the user's manual included with your parallel programmer for instructions.
In parallel I/O mode, the user ROM areas shown in Figure 27.1 can be rewritten.

27.7.1 ROM Code Protect Function

The ROM code protect function prevents the flash memory from being read and rewritten (refer to **27.4.2 ROM Code Protect Function**).

27.8 Notes on Flash Memory

27.8.1 CPU Rewrite Mode

27.8.1.1 Prohibited Instructions

The following instructions cannot be used while the program ROM area is being rewritten in EW0 mode because they reference data in the flash memory: UND, INTO, and BRK.

27.8.1.2 Interrupts

Tables 27.10 to 27.12 show CPU Rewrite Mode Interrupts.

Table 27.10 CPU Rewrite Mode Interrupts (1)

Mode	Erase/ Write Target	Status	Maskable Interrupt
EW0	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
		During auto-programming	
	Program ROM	During auto-erasure (suspend enabled)	Usable by allocating a vector in RAM.
		During auto-erasure (suspend disabled)	
		During auto-programming	
EW1	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1, the FMR21 bit is automatically set to 1. The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit to 0.
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
		During auto-programming	
	Program ROM	During auto-erasure (suspend enabled)	Auto-erasure suspends after td(SR-SUS) and interrupt handling is executed. Auto-erasure can be restarted by setting the FMR21 bit to 0 after interrupt handling completes. While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written.
		During auto-erasure (suspend disabled or FMR22 = 0)	Auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.
		During auto-programming	

FMR21, FMR22: Bits in FMR2 register

Table 27.11 CPU Rewrite Mode Interrupts (2)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 2 • Voltage Monitor 1	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step • Address Match • Address Break (Note 1)
EW0	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit is set to 0 (erase restart).	When an interrupt request is acknowledged, interrupt handling is executed. If erase-suspend is required, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit in the FMR2 register is set to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled)		
		During auto-programming		

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

Table 27.12 CPU Rewrite Mode Interrupts (3)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 2 • Voltage Monitor 1	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step • Address Match • Address Break (Note 1)
EW1	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit is set to 0 (erase restart).	When an interrupt request is acknowledged, interrupt handling is executed. If erase-suspend is required, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit in the FMR2 register is set to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled or FMR22 = 0)		
		During auto-programming		

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

27.8.1.3 How to Access

To set one of the following bits to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
• The FMR01 bit or FMR02 bit in the FMR0 register
• The FMR13 bit in the FMR1 register
• The FMR20 bit, FMR22 bit, FMR24 bit, or FMR 27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Disable interrupts and DTC activation between writing 1 and writing 0.
• The FMR14 bit, FMR15 bit, FMR16 bit, or FMR17 bit in the FMR1 register

27.8.1.4 Rewriting User ROM Area

In EW0 mode, if the supply voltage drops while rewriting any block in which a rewrite control program is stored, it may not be possible to rewrite the flash memory because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

27.8.1.5 Programming

Do not write additions to the already programmed address.

27.8.1.6 Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.
If the FST7 bit in the FST register is set to 0 (busy during programming or erasure execution), do not enter to stop mode or wait mode.
Do not enter stop mode or wait mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

27.8.1.7 Programming and Erasure Voltage for Flash Memory

To perform programming and erasure, use VCC = 2.7 to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 2.7 V.

27.8.1.8 Low-Current-Consumption Read Mode

In low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).
Low-current-consumption read mode can be used when the CPU clock is set to either of the following:
• The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.

When divided by 1 (no division) or divided by 2 is set, do not use low-current-consumption read mode.
After setting the divide ratio of the CPU clock, set the FMR27 bit to 1 (low-current-consumption read mode enabled).
To reduce the power consumption, refer to **10. Power Control**.
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

28. CRC Calculator Function

28.1 Overview

The CRC (Cyclic Redundancy Check) calculator detects errors in data blocks. This CRC calculator is enhanced by an additional feature, CRC snoop, which can monitor reads from and writes to a certain SFR address, and perform CRC calculations automatically on the data read from and data written to the SFR address.

Table 28.1 CRC Calculator Specifications

Item	Specifications
Generator polynomial	CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) or CRC-16 ($X^{16} + X^{15} + X^2 + 1$)
Selectable functions	• MSB/LSB select function • SFR access snoop

Figure 28.1 shows the CRC Calculator Block Diagram.

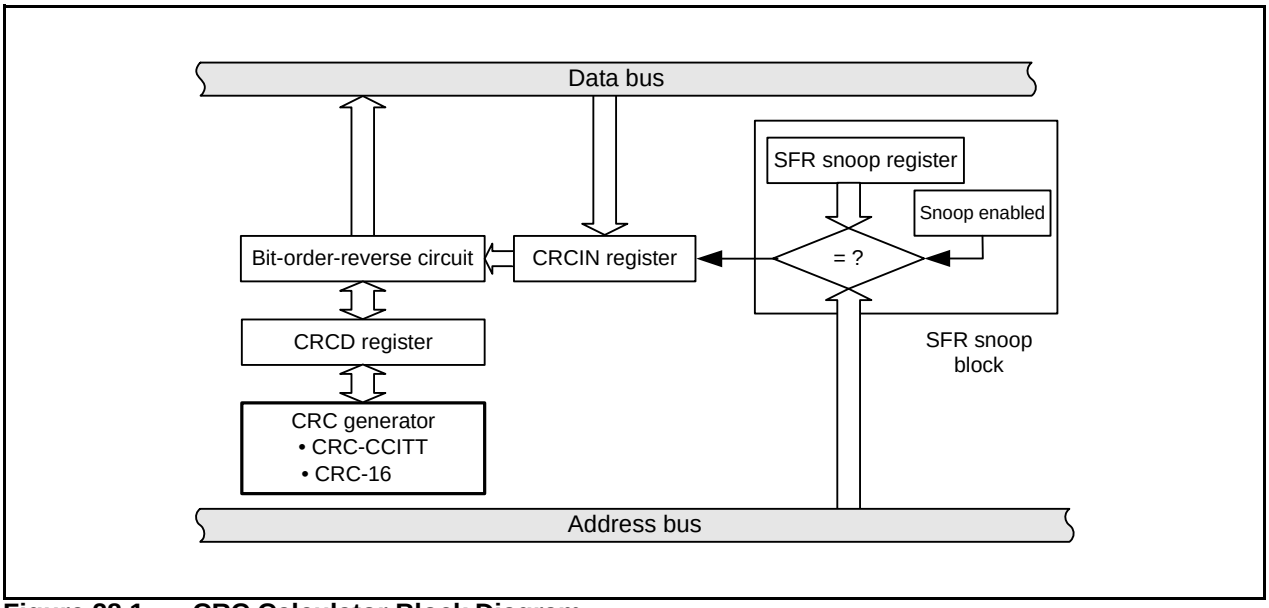


Figure 28.1 CRC Calculator Block Diagram

28.2 Registers

Table 28.2 lists the Register Configuration for CRC Calculator Function.

Table 28.2 Register Configuration for CRC Calculator Function

Register Name	Symbol	After Reset	Address	Access Size
SFR Snoop Address Register	CRCSAR	0000h	00290h	16
CRC Control Register	CRCMR	00h	00292h	8
CRC Data Register	CRCD	0000h	00294h	16
CRC Input Register	CRCIN	00h	00296h	8

28.2.1 SFR Snoop Address Register (CRCSAR)

Address 00290h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol								
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol								
After Reset	0	0	0	0	0	0	0	0

Bit	Function	R/W
b15 to b0	Set the SFR address to snoop.	R/W

The CRCSAR register is used to set the SFR address to snoop.
All SFR addresses from 00080h to 002FFh and from 06800h to 06FFFh are subject to the CRC snoop.

28.2.2 CRC Control Register (CRCMR)

Address 00292h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CRCSW	CRCSR	—	—	—	—	CRCPS	CRCMS
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CRCMS	CRC mode select bit	0: LSB first 1: MSB first	R/W
b1	CRCPS	CRC polynomial select bit	0: $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT) 1: $X^{16} + X^{15} + X^2 + 1$ (CRC-16)	R/W
b5 to b2	—	The write value must be 0. The read value is 0.		—
b6	CRCSR	Snoop-on-read enable bit	0: Disabled 1: Enabled	R/W
b7	CRCSW	Snoop-on-write enable bit		R/W

The CRCMR register is used to control both the CRC snoop and writes to and reads from registers CRCD and CRCIN.
When writing data from the CPU to the CRCIN register, set both the CRCSW and CRCSR bits to 0.

CRCMS Bit (CRC mode select bit)

When the CRCMS bit is set to 0, writes to registers CRCD and CRCIN are performed with the bit order reversed.
When CRC code is read from the CRCD register, the bit-order-reversed CRC code is read. The bit order must be reversed by a program.
When the CRCMS bit is set to 1, writes to registers CRCD and CRCIN do not reverse the bit order. When CRC code is read from the CRCD register, the read CRC code is not bit-order-reversed.

CRCPS Bit (CRC polynomial select bit)

When the CRCPS bit is set to 0, calculation is performed in CRT-CCITT mode and the result is stored in the CRCD register.
When the CRCPS bit is set to 1, calculation is performed in CRC-16 mode and the result is stored in the CRCD register.

CRCSR Bit (Snoop-on-read enable bit)

Setting the CRCSR bit to 1 enables snooping of read operations on the data bus.
When the CRCSR bit is 1, if the address set in the CRCSAR register is read, CRC calculation is performed automatically on the read data on the data bus and the result is stored in the CRCD register.
When the CRCSR bit is set to 1, set the CRCSW bit to 0.

CRCSW Bit (Snoop-on-write enable bit)

Setting the CRCSW bit to 1 enables snooping of write operations on the data bus.
When the CRCSW bit is 1, if the address set in the SRCSAR register is written, CRC calculation is performed automatically on the written data on the data bus and the result is stored in the CRCD register.
When the CRCSW bit is set to 1, set the CRCSR bit to 0.

28.2.3 CRC Data Register (CRCD)

Address 00294h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol								
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol								
After Reset	0	0	0	0	0	0	0	0

Bit	Function	R/W
b15 to b0	Store CRC calculation results.	R/W

The CRC calculation results are stored in the CRCD register.
When the CRCPS bit in the CRCMR register is 0 (CRC-CCITT mode), the result calculated with CRC-CCITT is read.
When the CRCPS bit is 1 (CRC-16 mode), the result calculated with CRC-16 is read.
When the CRCMS bit in the CRCMR register is 0, the initial value is written with the bit order reversed. When data is then written to the CRCIN register, the bit-order-reversed CRC code is read from the CRCD register.
When the CRCMS bit is 1, the initial value is written without reversing the bit order.
When data is then written to the CRCIN register, the CRC code read from the CRCD register is not bit-order-reversed.

28.2.4 CRC Input Register (CRCIN)

Address 00296h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol								
After Reset	0	0	0	0	0	0	0	0

Bit	Function	R/W
b7 to b0	Set data for CRC calculation.	R/W

The data for CRC calculation is input to the CRCIN register.
When writing to the CRCIN register from the CPU, set both the CRCSW and CRCSR bits in the CRCMR register to 0.
When the CRCMS bit in the CRCMR register is 0, writes to the CRCIN register are performed with the bit order reversed.
When the CRCMS bit is 1, writes to the CRCIN register do not reverse the bit order.

28.3 Operation

The CRC calculator generates 16-bit CRC code for an arbitrary length of a data block in 8-bit units. The generator polynomial of CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) or CRC-16 ($X^{16} + X^{15} + X^2 + 1$) is used to generate the CRC code.

After setting the initial value in the CRCD register, the CRC code is stored in the CRCD register every time 1 byte of data is written to the CRCIN register. CRC code generation for 1-byte of data is completed in two CPU clock cycles.

28.4 CRC Snoop

The CRC calculator has a CRC snoop function which monitors reads from and writes to a certain SFR address and performs CRC calculation automatically on the data read from and written to the SFR address. Because the CRC snoop recognizes writes to and reads from a certain SFR address as a trigger to perform CRC calculation, there is no need to write data to the CRCIN register. All SFR addresses from 00080h to 002FFh and 06800h to 06FFFh are subject to the CRC snoop.

To use this function, set a target SFR address in the CRCSAR register. Set the CRCSW bit in the CRCMR register to 1 to enable snooping on writes to the target. Similarly, set the CRCSR bit in the CRCMR register to 1 to enable snooping on reads from the target.

When the CRCSW bit is set to 1, if data is written to a target SFR address, the CRC calculator stores the data in the CRCIN register and performs CRC calculation.

Similarly, when the CRCSR bit is set to 1, and data is written to a target SFR address, the CRC calculator stores the data in the CRCIN register and performs CRC calculation.

The CRC calculation is performed 1 byte at a time. When the target SFR address is accessed in words (16 bits), the CRC code is generated on the lower byte (1 byte) of data at the SFR address set in the CRCSAR register.

28.5 Usage Method

The following shows examples of CRC calculation to generate the CRC code for 80C4h.

• When CRC-CCITT is used with LSB first

(1) Reverse the bit order of 80C4h by a program.
80h → 01h, C4h → 23h
(2) Set the CRCMR register to 00h.
(3) Set the CRCD register to the initial value 0000h.
(4) Set the CRCD register to 01h, a bit-order-reversed value of 80h.
1189h, which is a bit-order-reversed value of the CRC code 9188h for 80h, is stored in the CRCD register.
(5) Set the CRCIN register to 23h, a bit-order-reversed value of C4h.
0A41h, which is a bit-order-reversed value of the CRC code 8250h for 80C4h, is stored in the CRCD register.

• When CRC-16 is used with MSB first

(1) Set the CRCMR register to 03h.
(2) Set the CRCD register to the initial value 0000h.
(3) Set the CRCIN register to 80h.
The CRC code 8303h for 80h is stored in the CRCD register.
(4) Set the CRCIN register to C4h.
The CRC code 0292h for 80C4h is stored in the CRCD register.

29. Peripheral Mapping Controller

29.1 Overview

The peripheral mapping controller (referred to as PMC hereafter) can be used to change the pin assignment of I/O ports to communication function priority.

Standard pin assignment for 48-pin product can be changed to:
• Communication function priority pin assignment for 48-pin product

Changing pins must be performed using bits PMCSEL0 to PMCSEL2 in the PMCSEL register (pin assignment select register).
For details on the setting of the PMCSEL register, refer to **29.3.1 Pin Assignment Select Register (PMCSEL)**.
For details on the pin assignment of communication function priority, refer to **Table 29.1 I/O Port Pin Assignment Information by Pin Number for 48-Pin Automotive Product**.

29.1.1 Pins Not Selected by PMCSEL Register

Accessing the port Pi_j bit and the port Pi_0 direction bit for the pins not selected by the PMCSEL register does not affect the operation of the MCU.
A waveform cannot be input to or output from the pins of the peripheral functions that are not selected by the PMCSEL register, but these pins can be used. The following peripheral functions and I/O pins are restricted by the PMCSEL register.

(1) SSU_1
When the PMCSEL register is set to select a pin assignment other than communication function priority, a waveform cannot be input to or output from pins SSO_1, SCL_1, SSCK_1, SCS1, and SSI_1. However, continuous count operation can be performed for a specified period by coupling with a pseudo one-shot timer or the DTC.

29.2 Allocation of Peripheral Functions

Table 29.1 lists the I/O Port Pin Assignment Information by Pin Number for 48-Pin Automotive Product.

Table 29.1 I/O Port Pin Assignment Information by Pin Number for 48-Pin Automotive Product

Pin No.	Standard Assignment	Communication Function Priority Assignment
1	P3_5/SCL_0/SSCK_0/TRCIOD_0/CLK2/TRDIOD1_0/TRDIOA0_0/TRDCLK_0	P3_5/SCL_0/SSCK_0/TRCIOD_0/CLK2/TRDIOD1_0/TRDIOA0_0/TRDCLK_0
2	P3_3/SSI_0/INT3/TRCCLK_0/SCS_0/CTS2/RTS2/TRDIOD0_0	P3_3/SSI_0/INT3/TRCCLK_0/SCS_0/CTS2/RTS2/TRDIOD0_0
3	P3_4/SDA_0/SCS_0/TRCIOC_0/SSI_0/RXD2/TXD2/TRDIOC1_0/TRDIOB0_0	P3_4/SDA_0/SCS_0/TRCIOC_0/SSI_0/RXD2/TXD2/TRDIOC1_0/TRDIOB0_0
4	MODE	MODE
5	P4_3	P4_3
6	P4_4	P4_4
7	RESET	RESET
8	P4_7/XOUT	P4_7/XOUT
9	VSS/AVSS	VSS/AVSS
10	P4_6/XIN	P4_6/XIN
11	VCC/AVCC	VCC/AVCC
12	P2_7/TRDIOD1_0	P2_7/TRDIOD1_0
13	P2_6/TRDIOC1_0	P2_6/TRDIOC1_0
14	P2_5/TRDIOB1_0/IVREF3	P2_5/TRDIOB1_0/IVREF3
15	P2_4/TRDIOA1_0/IVCMP3	P2_4/TRDIOA1_0/IVCMP3
16	P2_3/TRDIOD0_0	P9_7/SSO_1 (1)
17	P2_2/TRDIOC0_0/TRDIOB0_0/TRCIOD_0	P9_6/SCL_1/SSCK_1/TRBO_1 (1)
18	P2_1/TRDIOB0_0/TRDIOC0_0/TRCIOC_0	P9_5/SDA_1/SCS_1 (1)
19	P2_0/TRDIOA0_0/TRDCLK_0/INT1/TXD2/RXD2/TRCIOB_0	P9_4/SSI_1 (1)
20	P1_7/INT1/TRJIO_0	P1_7/INT1/TRJIO_0
21	P1_6/CLK_0/SSI_0	P1_6/CLK_0/SSI_0
22	P1_5/RXD_0/TRJIO_0/INT1	P1_5/RXD_0/TRJIO_0/INT1
23	P1_4/TXD_0/TRCCLK_0	P1_4/TXD_0/TRCCLK_0
24	P1_3/KI3/AN11/TRBO_0/TRCIOC_0/TRDIOD1_0	P1_3/KI3/AN11/TRBO_0/TRCIOC_0/TRDIOD1_0
25	P4_5/INT0/RXD2	P4_5/INT0/RXD2
26	P6_6/INT2/TXD2/TRCIOC_0	P6_6/INT2/TXD2/TRCIOC_0
27	P6_7/INT3/RXD2/TRCIOD_0	P6_7/INT3/RXD2/TRCIOD_0
28	P1_2/KI2/AN10/TRCIOB_0/TRDIOC1_0	P1_2/KI2/AN10/TRCIOB_0/TRDIOC1_0
29	P1_1/KI1/AN9/TRCIOA_0/TRCTRG_0/TRDIOB1_0/IVCMP1	P1_1/KI1/AN9/TRCIOA_0/TRCTRG_0/TRDIOB1_0/IVCMP1
30	P1_0/KI0/AN8/TRCIOD_0/TRDIOA1_0/IVREF1	P1_0/KI0/AN8/TRCIOD_0/TRDIOA1_0/IVREF1
31	P3_1/TRBO_0/CTS2/RTS2	P3_1/TRBO_0/CTS2/RTS2
32	P3_0/TRJO_0	P3_0/TRJO_0
33	P6_5/INT4/CLK2/CLK_1/TRCIOB_0	P6_5/INT4/CLK2/CLK_1/TRCIOB_0
34	P6_4/RXD_1/INT2/TRJIO_1	P6_4/RXD_1/INT2/TRJIO_1
35	P6_3/TXD_1/TRJO_1	P6_3/TXD_1/TRJO_1
36	P0_7/AN0/TRCIOC_0	P0_7/AN0/TRCIOC_0
37	P0_6/AN1/TRCIOD_0	P0_6/AN1/TRCIOD_0
38	P0_5/AN2/CLK2/TRCIOB_0	P0_5/AN2/CLK2/TRCIOB_0
39	P0_4/AN3/TMRE2O/TRCIOB_0	P0_4/AN3/TMRE2O/TRCIOB_0
40	P4_2/VREF	P4_2/VREF
41	P6_0/TMRE2O	P6_0/TMRE2O
42	P6_2/CRX_0/CLK_1	P6_2/CRX_0/CLK_1
43	P6_1/CTX_0	P6_1/CTX_0
44	P0_3/AN4/CLK_1/TRCIOB_0	P0_3/AN4/CLK_1/TRCIOB_0
45	P0_2/AN5/RXD_1/TRCIOA_0/TRCTRG_0/TRJIO_1/INT2	P0_2/AN5/RXD_1/TRCIOA_0/TRCTRG_0/TRJIO_1/INT2
46	P0_1/AN6/TXD_1/TRCIOA_0/TRCTRG_0/TRJO_1	P0_1/AN6/TXD_1/TRCIOA_0/TRCTRG_0/TRJO_1
47	P0_0/AN7/TXD2/TRCIOA_0/TRCTRG_0	P0_0/AN7/TXD2/TRCIOA_0/TRCTRG_0
48	P3_7/SSO_0/TXD2/RXD2/TRJO_0/SDA_0/INT3/TRCCLK_0/TRDIOC0_0	P3_7/SSO_0/TXD2/RXD2/TRJO_0/SDA_0/INT3/TRCCLK_0/TRDIOC0_0

Note:
1. The pin function is changed when priority pin assignment is selected with the PMCSEL register (bits PMCSEL2 to PMCSEL0 = 100b).

29.3 Registers

Table 29.2 lists the PMC Register Configuration.

Table 29.2 PMC Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Pin Assignment Select Register	PMCSEL	00h	002BEh	8

29.3.1 Pin Assignment Select Register (PMCSEL)

Address 002BEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	PMCSEL2	PMCSEL1	PMCSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PMCSEL0	Pin assignment select bits	b2 b1 b0 0 1 1: Standard pin assignment for 48-pin product 1 0 0: Communication function priority pin assignment for 48-pin product Other than the above: Do not set.	R/W
b1	PMCSEL1			R/W
b2	PMCSEL2			R/W
b3	—	Reserved	Set to 0.	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

The PMCSEL register is used to select the assignment of pins, so set this register before controlling input/output. Set the PMCSEL register to change the pin assignment to communication function priority. Once the PMCSEL register is written, no additional writes can be performed.

29.4 Note on Peripheral Mapping Controller

29.4.1 Setting Pin Assignment Select Register (PMCSEL)

The PMCSEL register is used to select the assignment of pins, so set this register before controlling input/output.

29.4.2 Restrictions on Using Full-Spec Emulator (E100)

In the actual MCU of the R8C/5x Group and the full-spec emulator (E100), the set value of the pin assignment select bits differs when selecting 48-pin products.

	Full-spec emulator (E100)	Actual MCU of R8C/5x Group
Standard pin assignment for 48-pin product:	PMCSEL = 000b	PMCSEL = 011b
Communication function priority pin assignment for 48-pin product:	PMCSEL = 001b	PMCSEL = 100b

30. Electrical Characteristics

30.1 Absolute Maximum Ratings

Table 30.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
Vcc/AVcc	Supply voltage		–0.3 to 6.5	V
V_I	Input voltage (1)		–0.3 to Vcc + 0.3	V
IIN	Input current (1)	(2, 3, 4)	–4 to 4	mA
V_O	Output voltage		–0.3 to Vcc + 0.3	V
P_d	Power dissipation	–40°C ≤ Topr ≤ 85°C	300	mW
		85°C < Topr ≤ 125°C	125	mW
T_{opr}	Operating ambient temperature		–40 to 85 (J version)/ –40 to 125 (K version)	°C
T_{stg}	Storage temperature		–65 to 150	°C

Notes:
1. Meet the specified range for the input voltage or the input current.
2. Applicable ports: P0 to P2, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5, and P6.
3. The total input current must be 12 mA or less.
4. The input current may cause the MCU to be powered on and operate even if no voltage is supplied to Vcc. When a voltage is supplied to Vcc, the input current may cause the supply voltage to rise. Since operations in any cases other than above are not guaranteed, use the power supply circuit in the system to ensure the supply voltage for the MCU is stable within the specified range.

30.2 Recommended Operating Conditions

Table 30.2 Recommended Operating Conditions (1)
(Vcc = 2.7 V to 5.5 V, Topr = –40°C to 85°C (J version)/ –40°C to 125°C (K version), unless otherwise specified)

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
Vcc/AVcc	Supply voltage					2.7	—	5.5	V
Vss/AVss	Supply voltage					—	0	—	V
VIH	Input high voltage	Other than CMOS input				0.8 Vcc	—	Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.5 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.55 Vcc	—	Vcc	V
				Input level selection: 0.5Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.65 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.7 Vcc	—	Vcc	V
				Input level selection: 0.7Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.85 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.85 Vcc	—	Vcc	V
		External clock input (XOUT)				1.2	—	Vcc	V
VIL	Input low voltage	Other than CMOS input				0	—	0.2 Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.2 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.2 Vcc	V
				Input level selection: 0.5Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.4 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.3 Vcc	V
				Input level selection: 0.7Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.55 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.45 Vcc	V
		External clock input (XOUT)				0	—	0.4	V
IOH(sum)	Peak sum output high current		Sum of all pins IOH(peak)			—	—	–80	mA
IOH(sum)	Average sum output high current		Sum of all pins IOH(avg)			—	—	–40	mA
IOH(peak)	Peak output high current		When drive capacity is low			—	—	–10	mA
			When drive capacity is high			—	—	–40	mA
IOH(avg)	Average output high current		When drive capacity is low			—	—	–5	mA
			When drive capacity is high			—	—	–20	mA
IOL(sum)	Peak sum output low current		Sum of all pins IOL(peak)			—	—	80	mA
IOL(sum)	Average sum output low current		Sum of all pins IOL(avg)			—	—	40	mA
IOL(peak)	Peak output low current		When drive capacity is low			—	—	10	mA
			When drive capacity is high			—	—	40	mA
IOL(avg)	Average output low current		When drive capacity is low			—	—	5	mA
			When drive capacity is high			—	—	20	mA
f(XIN)	XIN clock input oscillation frequency				2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz
f(PLL)	PLL clock frequency				2.7 V ≤ Vcc ≤ 5.5 V	10	—	32	MHz
fHOCO	Count source for timer RC and timer RD				2.7 V ≤ Vcc ≤ 5.5 V	32	—	40	MHz
fHOCO-F	fHOCO-F frequency				2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz
—	System clock frequency				2.7 V ≤ Vcc ≤ 5.5 V	—	—	32	MHz
f(BCLK)	CPU clock frequency				2.7 V ≤ Vcc ≤ 5.5 V	—	—	32	MHz
tSU(PLL)	PLL frequency synthesizer stabilization wait time				2.7 V ≤ Vcc ≤ 5.5 V	—	—	1	ms

Note:
1. The average output current indicates the average value of current measured during 100 ms.

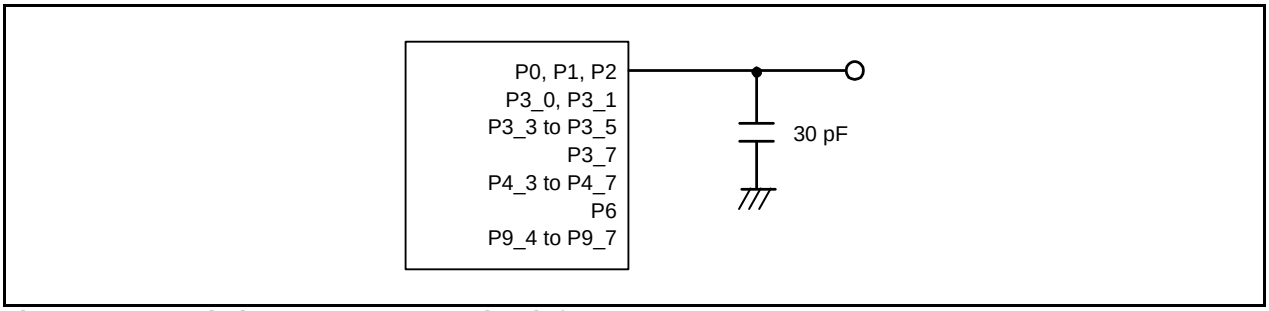


Figure 30.1 Timing Measurement Circuit for Ports P0 to P2, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_7, P6 and P9_4 to P9_7

Table 30.3 Recommended Operating Conditions (2)
(Vcc = 4.5 V to 5.5 V, Topr = –40°C to 85°C (J version)/–40°C to 125°C (K version), unless otherwise specified)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
IIC(H)	Input high injection current	P0, P1, P2, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5, P6	$V_I > V_{CC}$	—	—	2	mA
IIC(L)	Input low injection current	P0, P1, P2, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5, P6	$V_I < V_{SS}$	—	—	–2	mA
Σ[IIC]	Total injection current			—	—	8	mA

Table 30.4 Recommended Operating Conditions (3)
(Vcc = 2.7 V to 5.5 V, Topr = –40°C to 85°C (J version)/–40°C to 125°C (K version), unless otherwise specified)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
$V_{r(VCC)}$	Allowable power supply ripple voltage (1)		—	—	0.1Vcc	V
$dV_{r(VCC)/dt}$	Power supply ripple falling gradient (1)		—	—	10	V/ms

Note:
1. The power supply ripple must meet either or both $V_{r(VCC)}$ and $dV_{r(VCC)/dt}$

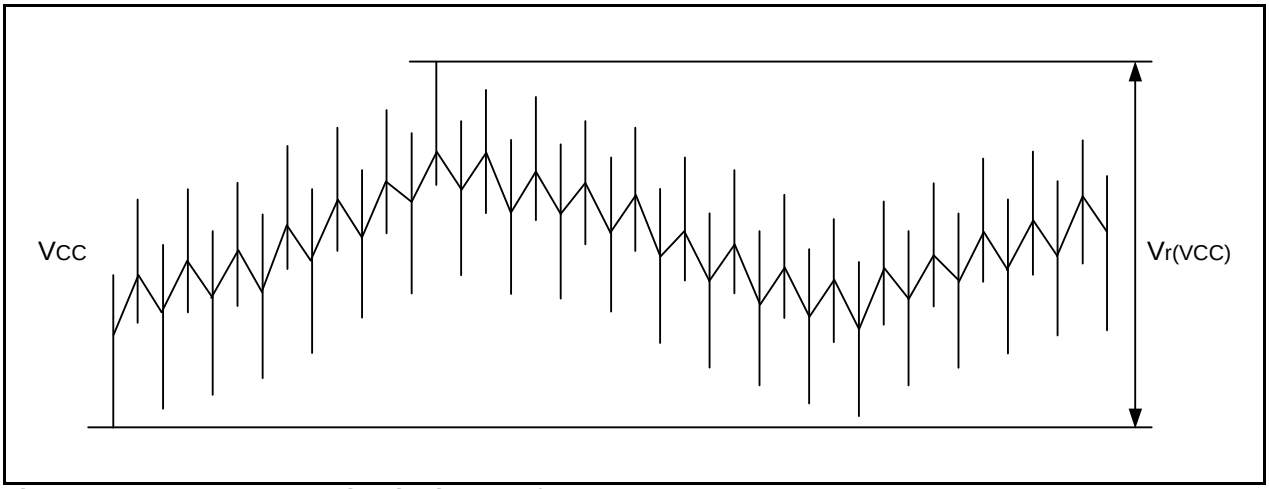


Figure 30.2 Power Supply Ripple Waveform

30.3 Peripheral Function Characteristics

Table 30.5 A/D Converter Characteristics (Vcc/AVcc = Vref = 2.7 V to 5.5 V, Vss = 0 V, Topr = –40°C to 85°C(J version)/ –40°C to 125°C (K version), unless otherwise specified)

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		V_{ref} = AVcc		—	—	10	Bit
—	Absolute accuracy	10-bit mode	V_{ref} = AVcc = 5.0 V	AN0 to AN11 input	—	—	±3	LSB
			V_{ref} = AVcc = 3.3 V	AN0 to AN11 input	—	—	±5	LSB
			V_{ref} = AVcc = 3.0 V	AN0 to AN11 input	—	—	±5	LSB
		8-bit mode	V_{ref} = AVcc = 5.0 V	AN0 to AN11 input	—	—	±2	LSB
			V_{ref} = AVcc = 3.3 V	AN0 to AN11 input	—	—	±2	LSB
			V_{ref} = AVcc = 3.0 V	AN0 to AN11 input	—	—	±2	LSB
ϕAD	A/D conversion clock		4.0 V ≤ V_{ref} = AVcc ≤ 5.5 V (1)		2	—	20	MHz
			3.2 V ≤ V_{ref} = AVcc ≤ 5.5 V (1)		2	—	16	MHz
			2.7 V ≤ V_{ref} = AVcc ≤ 5.5 V (1)		2	—	10	MHz
—	Tolerance level impedance				—	3	—	kΩ
I_{vref}	Vref current		Vcc = 5 V, XIN = f1 = fAD = 20 MHz		—	45	—	µA
t_{CONV}	Conversion time	10-bit mode	V_{ref} = AVcc = 5.0 V, ϕAD = 20 MHz		2.2	—	—	µs
		8-bit mode	V_{ref} = AVcc = 5.0 V, ϕAD = 20 MHz		2.2	—	—	µs
t_{SAMP}	Sampling time		ϕAD = 20 MHz		0.8	—	—	µs
V_{ref}	Reference voltage				2.7	—	AVcc	V
V_{IA}	Analog input voltage (2)				0	—	V_{ref}	V
OCVREF	On-chip reference voltage		2MHz ≤ ϕAD ≤ 4MHz		1.14	1.34	1.54	V

Notes:
1. If the CPU and the flash memory stop, the A/D conversion result will be undefined.
2. When the analog input voltage exceeds the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 30.6 Comparator B Characteristics (Vcc = 2.7 V to 5.5 V, Topr = –40°C to 85°C (J version)/–40°C to 125°C (K version), unless otherwise specified)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{ref}	IVREF1, IVREF3 input reference voltage		0	—	Vcc – 1.4	V
V_I	IVCMP1, IVCMP3 input voltage		–0.3	—	Vcc + 0.3	V
—	Offset		—	5	100	mV
t_d	Comparator output delay time (1)	V_I = V_{ref} ±100 mV	—	0.1	—	µs
I_{CMP}	Comparator operating current	Vcc = 5.0 V	—	17.5	—	µA

Note:
1. When the digital filter is not selected.

Table 30.7 Flash Memory (Program ROM) Characteristics (Vcc = 2.7 V to 5.5 V, Topr = –40°C to 85°C (J version)/–40°C to 125°C (K version), unless otherwise specified)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (1)	MCU with data flash	1,000 (2)	—	—	times
		MCU without data flash	100 (2)	—	—	times
—	Byte program time (Program and erase endurance ≤ 100 times)		—	—	—	µs
—	Byte program time (Program and erase endurance ≤ 1,000 times)		—	—	—	µs
—	Word program time (Program and erase endurance ≤ 100 times)	Topr = 25°C, Vcc = 5.0 V	—	100	200	µs
—	Word program time (Program and erase endurance ≤ 100 times)		—	100	400	µs
—	Word program time (Program and erase endurance ≤ 1,000 times)		—	100	650	µs
—	Block erase time		—	0.3	4	s
td(SR-SUS)	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	µs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
td(CMDRST-READY)	Time from when command is forcibly terminated until reading is enabled		—	—	30 + CPU clock × 1 cycle	µs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		2.7	—	5.5	V
—	Program, erase temperature		–40	—	85 (J version) 125 (K version)	°C
—	Data hold time	Ambient temperature = 55°C (6)	20	—	—	year

Notes:
1. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes 3,000 hours under an environment of ambient temperature 125°C and 7,000 hours under an environment of ambient temperature 85°C.

Table 30.8 Flash Memory (Data flash Block A to Block D) Characteristics (Vcc = 2.7 V to 5.5 V, Topr = –40°C to 85°C (J version)/–40°C to 125°C (K version), unless otherwise specified)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (1)		10,000 (2)	—	—	times
—	Byte program time (Program and erase endurance ≤ 1,000 times)		—	160	950	µs
—	Byte program time (Program and erase endurance > 1,000 times)		—	300	950	µs
—	Block erase time (Program and erase endurance ≤ 1,000 times)		—	0.2	1	s
—	Block erase time (Program and erase endurance > 1,000 times)		—	0.3	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	3 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	µs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		—	—	30 + CPU clock × 1 cycle	µs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		2.7	—	5.5	V
—	Program, erase temperature		–40	—	85 (J ver.) 125 (K ver.)	°C
—	Data hold time	Ambient temperature = 55°C (6)	20	—	—	year

Notes:
1. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100, 1,000 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes 3,000 hours under an environment of ambient temperature 125°C and 7,000 hours under an environment of ambient temperature 85°C.

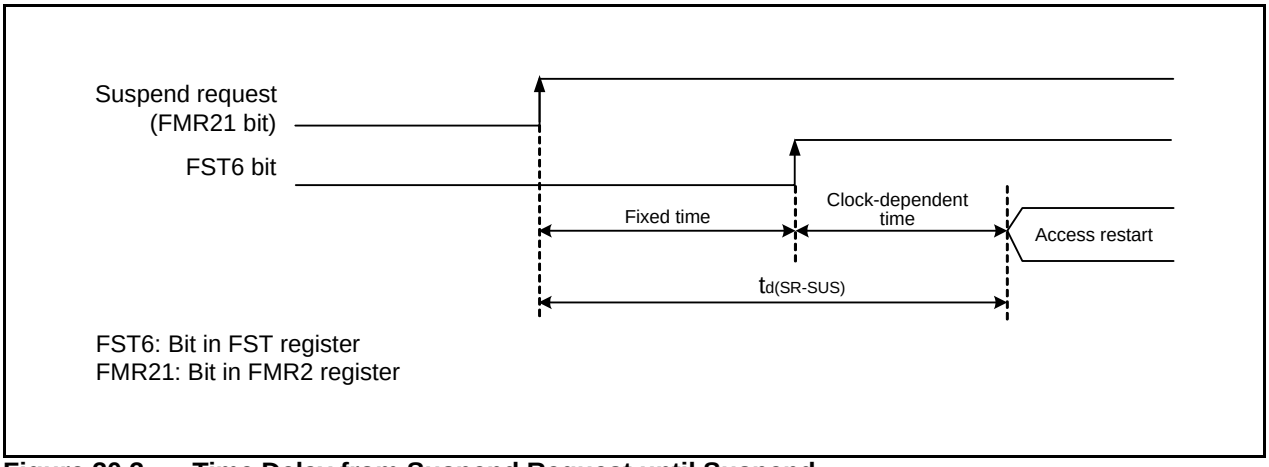


Figure 30.3 Time Delay from Suspend Request until Suspend

Table 30.9 Voltage Detection 0 Circuit Characteristics (Measurement conditions: Vcc = 2.7 V to 5.5 V, Topr = –40°C to 85°C (J version)/ –40°C to 125°C (K version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_2 (1)	When Vcc falls	2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (1)	When Vcc falls	3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time (2)	At the falling of Vcc from 5 V to (Vdet0 – 0.1) V	—	6	150	µs
—	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	—	1.5	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		—	—	100	µs

Notes:
1. The voltage detection level must be selected with bits VDSEL0 and VDSEL1 in the OFS register.
2. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 30.10 Voltage Detection 1 Circuit Characteristics (Measurement conditions: Vcc = 2.7 V to 5.5 V, Topr = –40°C to 85°C (J version)/ –40°C to 125°C (K version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_7 (1)	When Vcc falls	2.95	3.25	3.55	V
	Voltage detection level Vdet1_8 (1)	When Vcc falls	3.10	3.40	3.70	V
	Voltage detection level Vdet1_9 (1)	When Vcc falls	3.25	3.55	3.85	V
	Voltage detection level Vdet1_A (1)	When Vcc falls	3.40	3.70	4.00	V
	Voltage detection level Vdet1_B (1)	When Vcc falls	3.55	3.85	4.15	V
	Voltage detection level Vdet1_C (1)	When Vcc falls	3.70	4.00	4.30	V
	Voltage detection level Vdet1_D (1)	When Vcc falls	3.85	4.15	4.45	V
	Voltage detection level Vdet1_E (1)	When Vcc falls	4.00	4.30	4.60	V
	Voltage detection level Vdet1_F (1)	When Vcc falls	4.15	4.45	4.75	V
—	Hysteresis width at the rising of Vcc in voltage detection 1 circuit		—	0.10	—	V
—	Voltage detection 1 circuit response time (2)	At the falling of Vcc from 5 V to (Vdet1 – 0.1) V	—	60	150	µs
—	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		—	—	100	µs

Notes:
1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 30.11 Voltage Detection 2 Circuit Characteristics (Measurement conditions: Vcc = 2.7 V to 5.5 V, Topr = –40°C to 85°C (J version)/ –40°C to 125°C (K version))

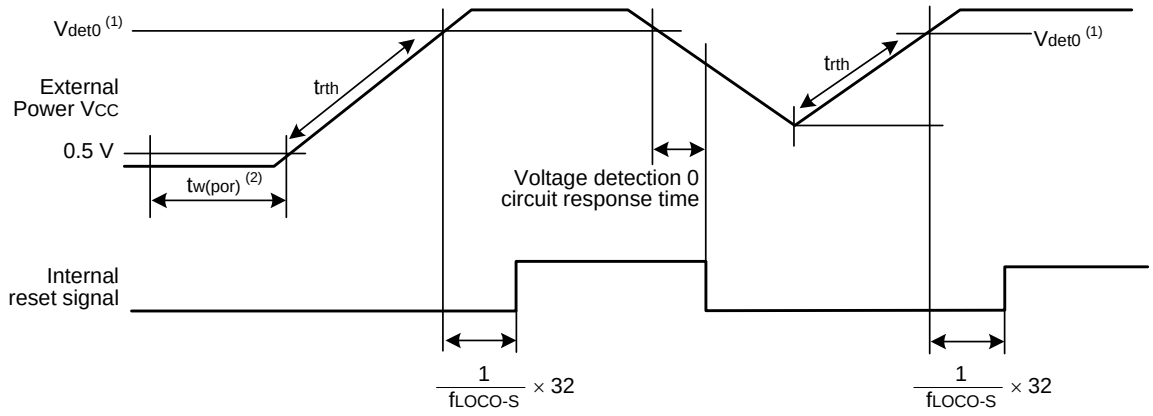
Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level Vdet2_0	When Vcc falls	3.70	4.00	4.30	V
—	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		—	0.1	—	µs
—	Voltage detection 2 circuit response time (1)	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	—	20	150	µs
—	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (2)		—	—	100	µs

Notes:
1. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 30.12 Power-On Reset Circuit Characteristics (1)
(Measurement conditions: Topr = –40°C to 85°C (J version)/ –40°C to 125°C (K version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power VCC rise gradient		0	—	50,000	mV/msec

Note:
1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to the **Voltage Detection Circuit** chapter for details.
2. $t_{w(por)}$ indicates the duration the external power Vcc must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

Figure 30.4 Power-on Reset Circuit Characteristics

Table 30.13 High-Speed On-Chip Oscillator Circuit Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset	Vcc = 2.7 V to 5.5 V, –40°C ≤ Topr ≤ 85°C (J version) –40°C ≤ Topr ≤ 125°C (K version)	—	40	—	MHz
	High-speed on-chip oscillator frequency when 01b is written to bits FRA25 and FRA24 in the FRA2 register (1)		—	36.864	—	MHz
	High-speed on-chip oscillator frequency when 10b is written to bits FRA25 and FRA24 in the FRA2 register		—	32	—	MHz
	High-speed on-chip oscillator frequency temperature and power supply voltage dependency (2)		– 1.5	—	1.5	%
—	Oscillation stability time	Vcc = 5.0 V, Topr = 25°C	—	250	—	µs
—	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	—	400	—	µA

Notes:
1. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.
2. This indicates the precision error for the oscillation frequency of the high-speed on-chip oscillator.

Table 30.14 Low-Speed On-Chip Oscillator Circuit Characteristics (Measurement conditions: Vcc = 2.7 V to 5.5 V, Topr = –40°C to 85°C (J version)/ –40°C to 125°C (K version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
fLOCO	Low-speed on-chip oscillator frequency	2.7 V ≤ Vcc < 4.2 V	106.25	125	143.75	kHz
		4.2 V ≤ Vcc ≤ 5.5 V	112.5	125	137.5	kHz
fLOCOWDT	Low-speed on-chip oscillator frequency for the watchdog timer	2.7 V ≤ Vcc < 4.2 V	106.25	125	143.75	kHz
		4.2 V ≤ Vcc ≤ 5.5 V	112.5	125	137.5	kHz
—	Oscillation stability time	Vcc = 5.0 V, Topr = 25°C	—	30	100	µs
—	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	—	3	—	µA

Table 30.15 Power Supply Circuit Characteristics (Measurement conditions: Vcc = 2.7 V to 5.5 V, Topr = –40°C to 85°C (J version)/ –40°C to 125°C (K version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on (1)		—	—	2,000	µs

Note:
1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

30.4 DC Characteristics

Table 30.16 DC Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]
(Vcc = 4.2 V to 5.5 V, Topr = –40°C to 85°C (J version)/–40°C to 125°C (K version), f(XIN) = 20 MHz, unless otherwise specified)

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	Other than XOUT	Drive capacity is high	I_{OH} = –20 mA	Vcc – 2.0	—	Vcc	V
			Drive capacity is low	I_{OH} = –5 mA	Vcc – 2.0	—	Vcc	V
				I_{OH} = –200 µA	Vcc – 0.3	—	Vcc	V
		XOUT		I_{OH} = –200 µA	1.0	—	Vcc	V
V_{OL}	Output low voltage	Other than XOUT	Drive capacity is high	I_{OL}= 20 mA	—	—	2.0	V
			Drive capacity is low	I_{OL} = 5 mA	—	—	2.0	V
				I_{OL} = 200 µA	—	—	0.45	V
		XOUT		I_{OL} = 200 µA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$ to $\overline{INT4}$, $\overline{KI0}$ to $\overline{KI3}$, TRJIO_0, TRJIO_1, TRCCLK_0, TRCCLK_1, TRCTRG_0, TRCTRG_1, TRCIOA_0, TRCIOB_0, TRCIOC_0, TRCIOD_0, TRDIOA0_0, TRDIOA1_0, TRDIOB0_0, TRDIOB1_0, TRDIOC0_0, TRDIOC1_0, TRDIOD0_0, TRDIOD1_0, TRDCLK_0, CLK_0, CLK_1, RXD_0, RXD_1, $\overline{CTS2}$, RXD2, SCL_0, SCL_1, SDA_0, SDA_1, SSI_0, SSI_1, $\overline{SCS\_0}$, $\overline{SCS\_1}$, SSCK_0, SSCK_1, SSO_0, SSO_1	Vcc = 5.0 V		0.1	1.2	—	V
		$\overline{RESET}$	Vcc = 5.0 V		0.1	1.2	—	V
I_{IH}	Input high current		V_I = 5.0 V, Vcc = 5.0 V		—	—	1.0	µA
I_{IL}	Input low current		V_I = 0 V, Vcc = 5.0 V		—	—	–1.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, Vcc = 5.0 V		25	50	100	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		2.0	—	—	V

Table 30.17 DC Characteristics (2) [3.3 V ≤ Vcc ≤ 5.5 V]
(Topr = –40°C to 85°C (J version), unless otherwise specified)

Symbol	Parameter	Conditions							Standard (4)			Unit
			Oscillation	On-Chip Oscillator		Multiplication, Division	CPU clock	Low-Power-Consumption Setting	Other	Min.	Typ.	Max.	
			XIN (2)	High-Speed	Low-Speed								
ICC	Power supply current (1)	PLL operating mode	4 MHz	Off	125 kHz	Multiply-by-8	32 MHz	—		—	14.0	21	mA
		High-speed clock mode	20 MHz	Off	125 kHz	No division	20 MHz	—		—	8.2	16.4	mA
			16 MHz	Off	125 kHz	No division	16 MHz	—		—	6.7	13.4	mA
			10 MHz	Off	125 kHz	No division	10 MHz	—		—	4.4	—	mA
			20 MHz	Off	125 kHz	Multiply-by-8	2.5 MHz	—		—	3.6	—	mA
			16 MHz	Off	125 kHz	Multiply-by-8	2 MHz	—		—	2.9	—	mA
			10 MHz	Off	125 kHz	Multiply-by-8	1.25 MHz	—		—	2.0	—	mA
		High-speed on-chip oscillator mode	Off	20 MHz (3)	125 kHz	No division	20 MHz	—		—	8.7	17.4	mA
			Off	20 MHz (3)	125 kHz	Divide-by-8	2.5 MHz	—		—	4.1	—	mA
			Off	4 MHz (3)	125 kHz	Divide-by-16	250 MHz	MSTIIC = 1 MSTTRD = 1 MSTTRC = 1		—	1.4	—	mA
		Low-speed on-chip oscillator mode	Off	Off	125 kHz	Divide-by-8	15.625 MHz	FMR27 = 1 SVC0 = 0		—	100	200	µA
		Wait mode	Off	Off	125 kHz	—	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock operation	—	15	120	µA
			Off	Off	125 kHz	—	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	5	110	µA
		Stop mode	Off	Off	Off	—	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	—	2.5	5.0	µA
			Off	Off	Off	—	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	—	30.0	—	µA

Notes:
1. Vcc = 3.3 V to 5.5 V, single-chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. fHOCO-F
4. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
   The maximum value (Max.) indicates the current value when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

Table 30.18 DC Characteristics (3) [3.3 V ≤ Vcc ≤ 5.5 V]
(Topr = –40°C to 125°C (K version), unless otherwise specified)

Symbol	Parameter	Conditions							Standard (4)			Unit
			Oscillation	On-Chip Oscillator		Multiplication, Division	CPU clock	Low-Power-Consumption Setting	Other	Min.	Typ.	Max.	
			XIN (2)	High-Speed	Low-Speed								
ICC	Power supply current (1)	PLL operating mode	4 MHz	Off	125 kHz	Multiply-by-8	32 MHz	—		—	14.0	21	mA
		High-speed clock mode	20 MHz	Off	125 kHz	No division	20 MHz	—		—	8.2	16.4	mA
			16 MHz	Off	125 kHz	No division	16 MHz	—		—	6.7	13.4	mA
			10 MHz	Off	125 kHz	No division	10 MHz	—		—	4.4	—	mA
			20 MHz	Off	125 kHz	Multiply-by-8	2.5 MHz	—		—	3.6	—	mA
			16 MHz	Off	125 kHz	Multiply-by-8	2 MHz	—		—	2.9	—	mA
			10 MHz	Off	125 kHz	Multiply-by-8	1.25 MHz	—		—	2.0	—	mA
		High-speed on-chip oscillator mode	Off	20 MHz (3)	125 kHz	No division	20 MHz	—		—	8.7	17.4	mA
			Off	20 MHz (3)	125 kHz	Divide-by-8	2.5 MHz	—		—	4.1	—	mA
			Off	4 MHz (3)	125 kHz	Divide-by-16	250 MHz	MSTIIC = 1 MSTTRD = 1 MSTTRC = 1		—	1.4	—	mA
		Low-speed on-chip oscillator mode	Off	Off	125 kHz	Divide-by-8	15.625 MHz	FMR27 = 1 SVC0 = 0		—	100	400	µA
		Wait mode	Off	Off	125 kHz	—	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock operation	—	15	330	µA
			Off	Off	125 kHz	—	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	5	320	µA
		Stop mode	Off	Off	Off	—	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	—	2.5	5.0	µA
			Off	Off	Off	—	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 125°C Peripheral clock off	—	120	—	µA

Notes:
1. Vcc = 3.3 V to 5.5 V, single-chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. fHOCO-F
4. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
   The maximum value (Max.) indicates the current value when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

Table 30.19 DC Characteristics (4) [2.7 V ≤ Vcc < 4.2 V]
(Measurement conditions: 2.7 V ≤ Vcc < 4.2 V, Topr = –40°C to 85°C (J version)/ –40°C to 125°C (K version), f(XIN) = 10 MHz))

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	Other than XOUT	Drive capacity is high	I_{OH} = –5 mA	Vcc – 0.5	—	Vcc	V
			Drive capacity is low	I_{OH} = –1 mA	Vcc – 0.5	—	Vcc	V
		XOUT		I_{OH} = –200 µA	1.0	—	Vcc	V
V_{OL}	Output low voltage	Other than XOUT	Drive capacity is high	I_{OL} = 5 mA	—	—	0.5	V
			Drive capacity is low	I_{OL} = 1 mA	—	—	0.5	V
		XOUT		I_{OL} = 200 µA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$ to $\overline{INT4}$, $\overline{KI0}$ to $\overline{KI3}$, TRJIO_0, TRJIO_1, TRCCLK_0, TRCCLK_1, TRCTRG_0, TRCTRG_1, TRCIOA_0, TRCIOB_0, TRCIOC_0, TRCIOD_0, TRDIOA0_0, TRDIOA1_0, TRDIOB0_0, TRDIOB1_0, TRDIOC0_0, TRDIOC1_0, TRDIOD0_0, TRDIOD1_0, TRDCLK_0, CLK_0, CLK_1, RXD_0, RXD_1, $\overline{CTS2}$, RXD2, SCL_0, SCL_1, SDA_0, SDA_1, $\overline{SSI\_0}$, $\overline{SSI\_1}$, $\overline{SCS\_0}$, $\overline{SCS\_1}$, SSCK_0, SSCK_1, SSO_0, SSO_1	Vcc = 3.0 V		0.1	0.4	—	V
		$\overline{RESET}$	Vcc = 3.0 V		0.1	0.5	—	V
I_{IH}	Input high current		V_I = 3.0 V, Vcc = 3.0 V		—	—	1.0	µA
I_{IL}	Input low current		V_I = 0 V, Vcc = 3.0 V		—	—	–1.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, Vcc = 3.0 V		42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		2.0	—	—	V

Table 30.20 DC Characteristics (5) [2.7 V ≤ Vcc < 3.3 V]
(Topr = –40°C to 85°C (J version), unless otherwise specified)

Symbol	Parameter	Conditions								Standard (4)			Unit
			Oscillation	On-Chip Oscillator		Multiplication, Division	CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ.	Max.	
			XIN (2)	High-Speed	Low-Speed								
I_{CC}	Power supply current (1)	PLL operating mode	4 MHz	Off	125 kHz	Multiply-by-8	32 MHz	—		—	14.0	20.5	mA
		High-speed clock mode	20 MHz	Off	125 kHz	No division	20 MHz	—		—	8.2	16	mA
			16 MHz	Off	125 kHz	No division	16 MHz	—		—	6.7	13	mA
			10 MHz	Off	125 kHz	No division	10 MHz	—		—	4.4	—	mA
			20 MHz	Off	125 kHz	Multiply-by-8	2.5 MHz	—		—	3.6	—	mA
			16 MHz	Off	125 kHz	Multiply-by-8	2 MHz	—		—	2.9	—	mA
			10 MHz	Off	125 kHz	Multiply-by-8	1.25 MHz	—		—	2.0	—	mA
		High-speed on-chip oscillator mode	Off	20 MHz (3)	125 kHz	No division	20 MHz	—		—	8.7	17	mA
			Off	20 MHz (3)	125 kHz	Divide-by-8	2.5 MHz	—		—	4.1	—	mA
			Off	4 MHz (3)	125 kHz	Divide-by-16	250 MHz	MSTIIC = 1 MSTTRD = 1 MSTTRC = 1		—	1.4	—	mA
		Low-speed on-chip oscillator mode	Off	Off	125 kHz	Divide-by-8	15.625 MHz	FMR27 = 1 SVC0 = 0		—	100	200	µA
		Wait mode	Off	Off	125 kHz	—	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock operation	—	15	120	µA
			Off	Off	125 kHz	—	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	5	110	µA
		Stop mode	Off	Off	Off	—	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	—	2.5	5.0	µA
			Off	Off	Off	—	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	—	30.0	—	µA

Notes:
1. Vcc = 2.7 V to 3.3 V, single-chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. fHOCO-F
4. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
   The maximum value (Max.) indicates the current value when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

Table 30.21 DC Characteristics (6) [2.7 V ≤ Vcc < 3.3 V]
(Topr = –40°C to 125°C (K version), unless otherwise specified)

Symbol	Parameter	Conditions								Standard (4)			Unit
			Oscillation	On-Chip Oscillator		Multiplication, Division	CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ.	Max.	
			XIN (2)	High-Speed	Low-Speed								
ICC	Power supply current (1)	PLL operating mode	4 MHz	Off	125 kHz	Multiply-by-8	32 MHz	—		—	14.0	20.5	mA
		High-speed clock mode	20 MHz	Off	125 kHz	No division	20 MHz	—		—	8.2	16	mA
			16 MHz	Off	125 kHz	No division	16 MHz	—		—	6.7	13	mA
			10 MHz	Off	125 kHz	No division	10 MHz	—		—	4.4	—	mA
			20 MHz	Off	125 kHz	Multiply-by-8	2.5 MHz	—		—	3.6	—	mA
			16 MHz	Off	125 kHz	Multiply-by-8	2 MHz	—		—	2.9	—	mA
			10 MHz	Off	125 kHz	Multiply-by-8	1.25 MHz	—		—	2.0	—	mA
		High-speed on-chip oscillator mode	Off	20 MHz (3)	125 kHz	No division	20 MHz	—		—	8.7	17	mA
			Off	20 MHz (3)	125 kHz	Divide-by-8	2.5 MHz	—		—	4.1	—	mA
			Off	4 MHz (3)	125 kHz	Divide-by-16	250 MHz	MSTIIC = 1 MSTTRD = 1 MSTTRC = 1		—	1.4	—	mA
		Low-speed on-chip oscillator mode	Off	Off	125 kHz	Divide-by-8	15.625 MHz	FMR27 = 1 SVC0 = 0		—	100	390	µA
		Wait mode	Off	Off	125 kHz	—	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock operation	—	22	320	µA
			Off	Off	125 kHz	—	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	6	310	µA
		Stop mode	Off	Off	Off	—	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	—	2.5	5.0	µA
			Off	Off	Off	—	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 125°C Peripheral clock off	—	120	—	µA

Notes:
1. Vcc = 2.7 V to 3.3 V, single-chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. fHOCO-F
4. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
   The maximum value (Max.) indicates the current value when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

30.5 AC Characteristics

Table 30.22 Timing Requirements of Clock Synchronous Serial I/O with Chip Select (during Master Operation) (Measurement conditions: Vcc = 2.7 V to 5.5 V, Topr = –40°C to 85°C (J version)/ –40°C to 125°C (K version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time		4.00	—	—	t_{CYC} (1)
t_{HI}	SSCK clock high width		0.40	—	0.60	t_{SUCYC}
t_{LO}	SSCK clock low width		0.40	—	0.60	t_{SUCYC}
t_{RISE}	SSCK clock rising time	2.7 V ≤ Vcc ≤ 5.5 V	—	—	0.50	t_{CYC} (1)
t_{FALL}	SSCK clock falling time	2.7 V ≤ Vcc ≤ 5.5 V	—	—	0.50	t_{CYC} (1)
t_{SU}	SSI, SSO data input setup time	4.5 V ≤ Vcc ≤ 5.5 V	60	—	—	ns
		2.7 V ≤ Vcc < 4.5 V	70	—	—	ns
t_H	SSI, SSO data input hold time	2.7 V ≤ Vcc ≤ 5.5 V	2.00	—	—	t_{CYC} (1)
t_{LEAD}	$\overline{SCS}$-SCK output delay time		0.5 t_{SUCYC} - 1 t_{CYC}	—	—	ns
t_{LAG}	SCK -$\overline{SCS}$ output valid time		0.5 t_{SUCYC} - 1 t_{CYC}	—	—	ns
t_{OD}	SSO data output delay time	2.7 V ≤ Vcc ≤ 5.5 V	—	—	30.00	ns

Note:
1. 1t_{CYC} = 1/f1 (s), f1 ≤ 20 MHz

Table 30.23 Timing Requirements of Clock Synchronous Serial I/O with Chip Select (during Slave Operation) (Measurement conditions: Vcc = 2.7 V to 5.5 V, Topr = –40°C to 85°C (J version)/ –40°C to 125°C (K version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time		4.00	—	—	t_{CYC} (1)
t_{HI}	SSCK clock high width		0.40	—	0.60	t_{SUCYC}
t_{LO}	SSCK clock low width		0.40	—	0.60	t_{SUCYC}
t_{RISE}	SSCK clock rising time		—	—	1.00	µs
t_{FALL}	SSCK clock falling time		—	—	1.00	µs
t_{SU}	SSO data input setup time		10.00	—	—	ns
t_{H}	SSO data input hold time		2.00	—	—	t_{CYC} (1)
t_{LEAD}	$\overline{SCS}$ setup time		$1t_{CYC}$ + 50	—	—	ns
t_{LAG}	$\overline{SCS}$ hold time		$1t_{CYC}$ + 50	—	—	ns
t_{OD}	SSI, SSO data output delay time	4.5 V ≤ Vcc ≤ 5.5 V	—	—	60	ns
		2.7 V ≤ Vcc < 4.5 V	—	—	70	ns
t_{SA}	SSI slave access time	2.7 V ≤ Vcc ≤ 5.5 V	—	—	$1.5t_{CYC}$ + 100	ns
t_{OR}	SSI slave out open time	2.7 V ≤ Vcc ≤ 5.5 V	—	—	$1.5t_{CYC}$ + 100	ns

Note:
1. $1t_{CYC} = 1/f1$ (s), f1 ≤ 20 MHz

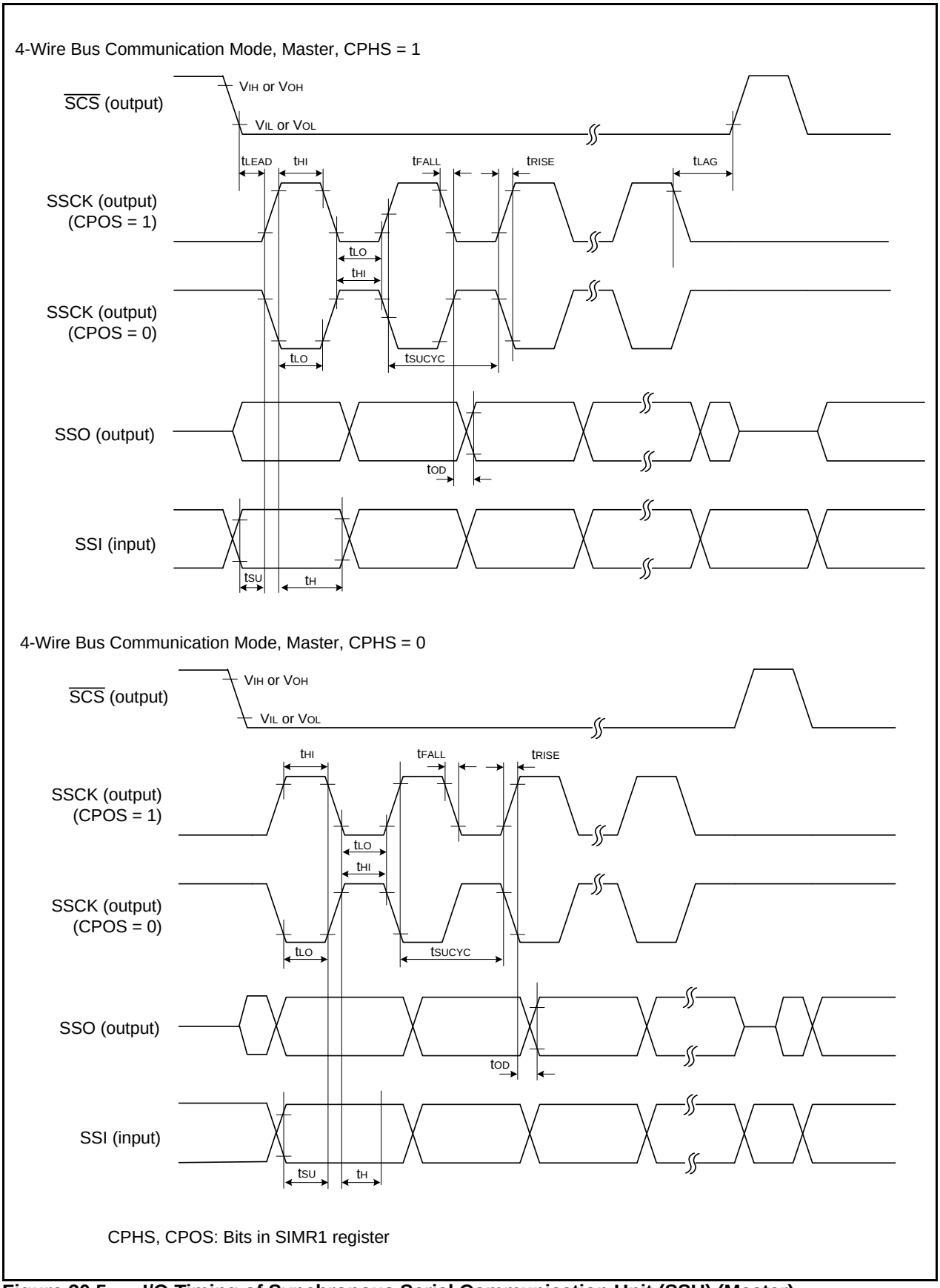


Figure 30.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

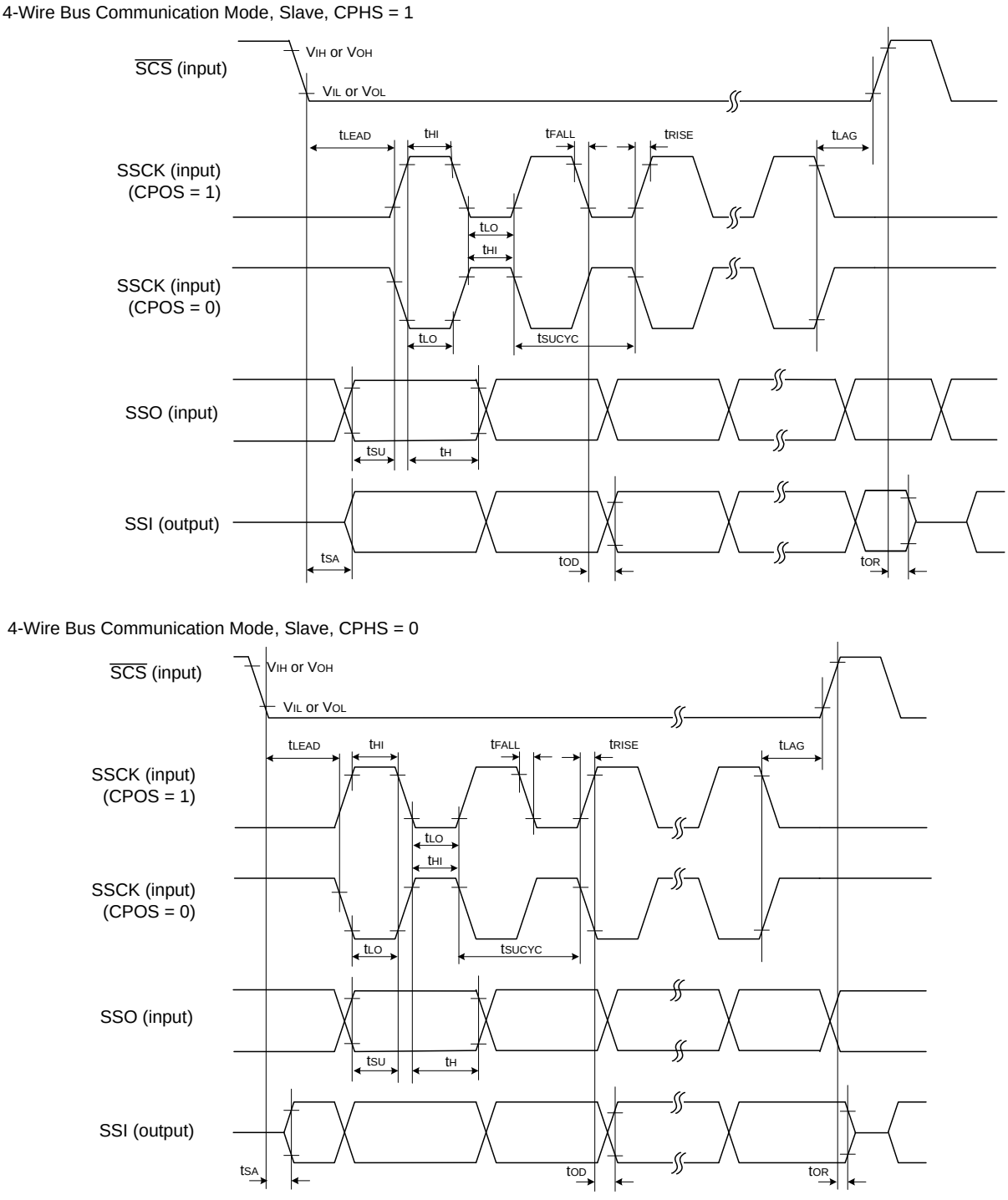


Figure 30.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

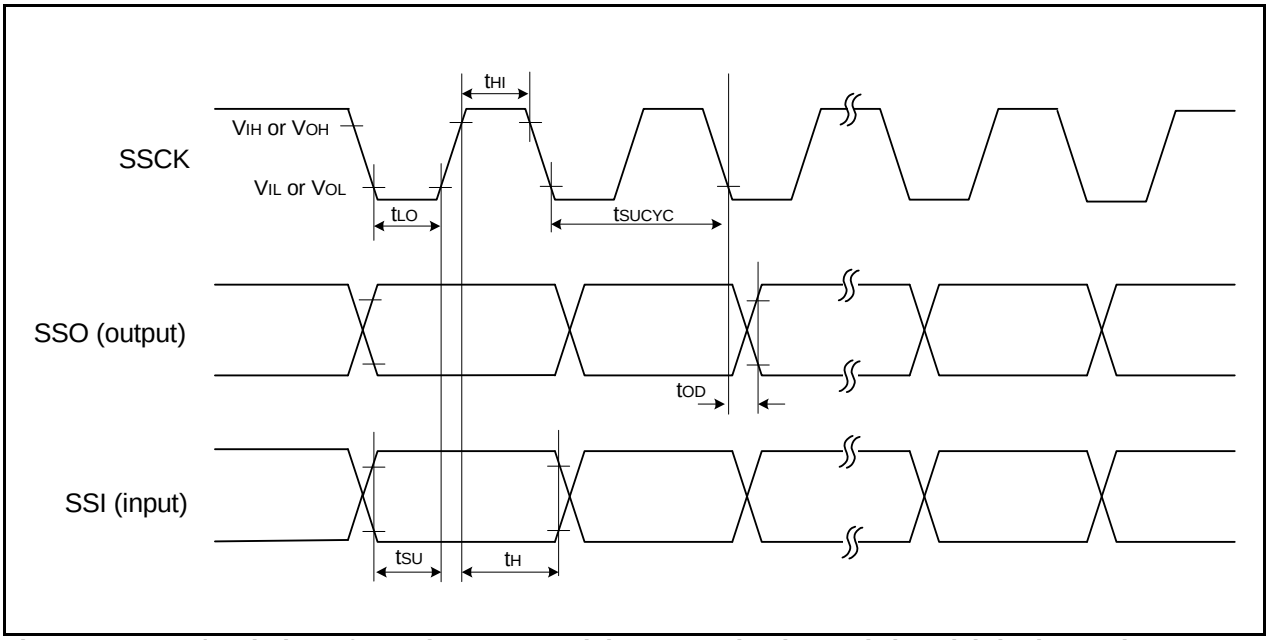
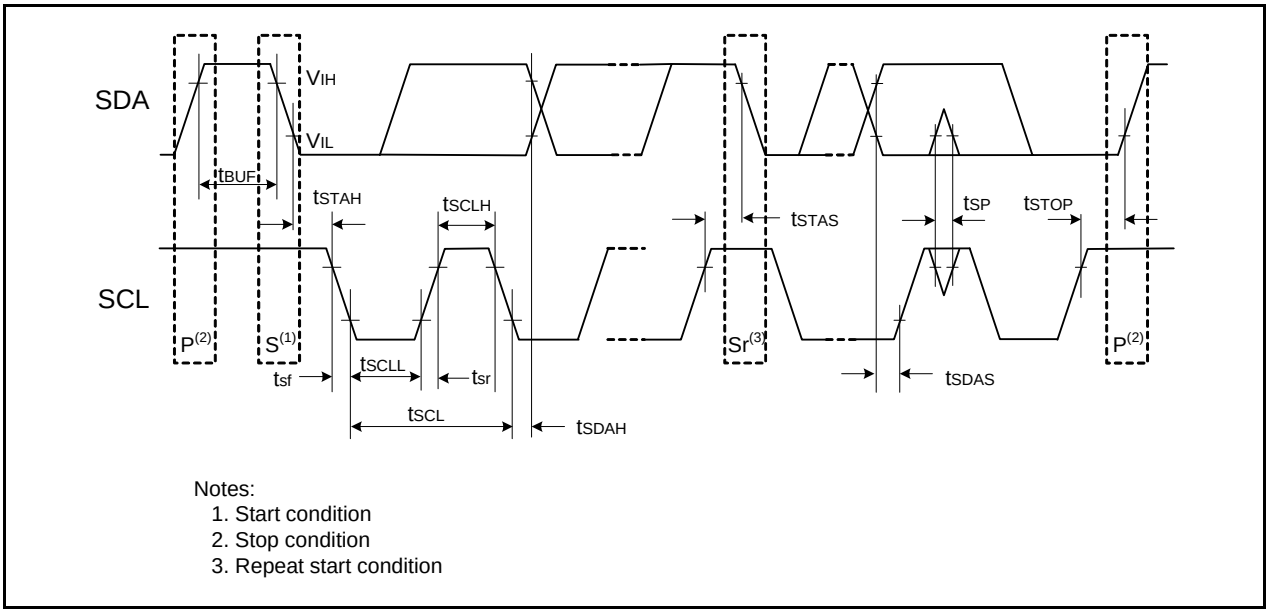


Figure 30.7 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 30.24 Timing Requirements of I²C bus Interface (Measurement conditions: Vcc = 2.7 V to 5.5 V, and Topr = –40 to 85°C (J version)/ –40 to 125°C (K version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC} + 600$ (1)	—	—	ns
t_{SCLH}	SCL input high width		$3t_{CYC} + 300$ (1)	—	—	ns
t_{SCLL}	SCL input low width		$5t_{CYC} + 500$ (1)	—	—	ns
t_{sf}	SCL, SDA input fall time		—	—	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		—	—	$1t_{CYC}$ (1)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$ (1)	—	—	ns
t_{STAH}	Start condition input hold time		$3t_{CYC}$ (1)	—	—	ns
t_{STAS}	Repeat start condition input setup time		$3t_{CYC}$ (1)	—	—	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$ (1)	—	—	ns
t_{SDAS}	Data input setup time		$1t_{CYC} + 40$ (1)	—	—	ns
t_{SDAH}	Data input hold time		10	—	—	ns

Note:
1. $1t_{CYC} = 1/f1$ (s), f1 ≤ 20 MHz



Notes:
1. Start condition
2. Stop condition
3. Repeat start condition

Figure 30.8 I/O Timing of I²C bus Interface

Table 30.25 External Clock Input (XOUT)

Symbol	Parameter	Standard				Unit
		Vcc = 3 V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	—	50	—	ns
$t_{WH(XOUT)}$	XOUT input high width	24	—	24	—	ns
$t_{WL(XOUT)}$	XOUT input low width	24	—	24	—	ns

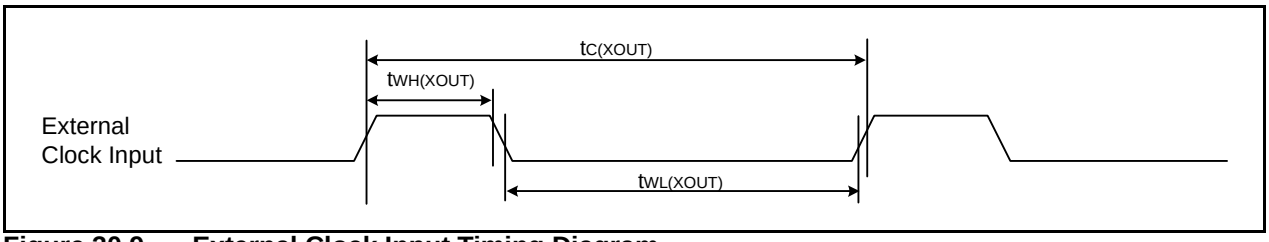


Figure 30.9 External Clock Input Timing Diagram

Table 30.26 Timing Requirements of TRJIO

Symbol	Parameter	Standard				Unit
		Vcc = 3V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	
$t_{c(TRJIO)}$	TRJIO input cycle time	300	—	100	—	ns
$t_{WH(TRJIO)}$	TRJIO input high width	120	—	40	—	ns
$t_{WL(TRJIO)}$	TRJIO input low width	120	—	40	—	ns

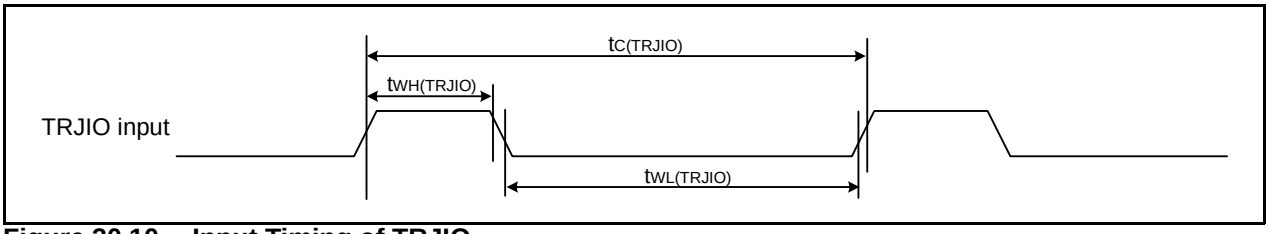


Figure 30.10 Input Timing of TRJIO

Table 30.27 Timing Requirements of Serial Interface (Internal clock selected as transfer clock (master communication))

Symbol	Parameter	Standard				Unit
		Vcc = 3V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	
$t_{d(C-Q)}$	TXDi output delay time	—	30	—	10	ns
$t_{su(D-C)}$	RXDi input setup time (1)	120	—	90	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	90	—	ns

i = 0 or 1

Note:

1. External pin load condition CL = 30 pF

Table 30.28 Timing Requirements of Serial Interface (External clock selected as transfer clock (slave communication))

Symbol	Parameter	Standard				Unit
		Vcc = 3V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	200	—	ns
$t_{W(CKH)}$	CLKi input high width	150	—	100	—	ns
$t_{W(CKL)}$	CLKi input low width	150	—	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	120	—	90	ns
$t_{su(D-C)}$	RXDi input setup time	30	—	10	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	90	—	ns

i = 0 or 1

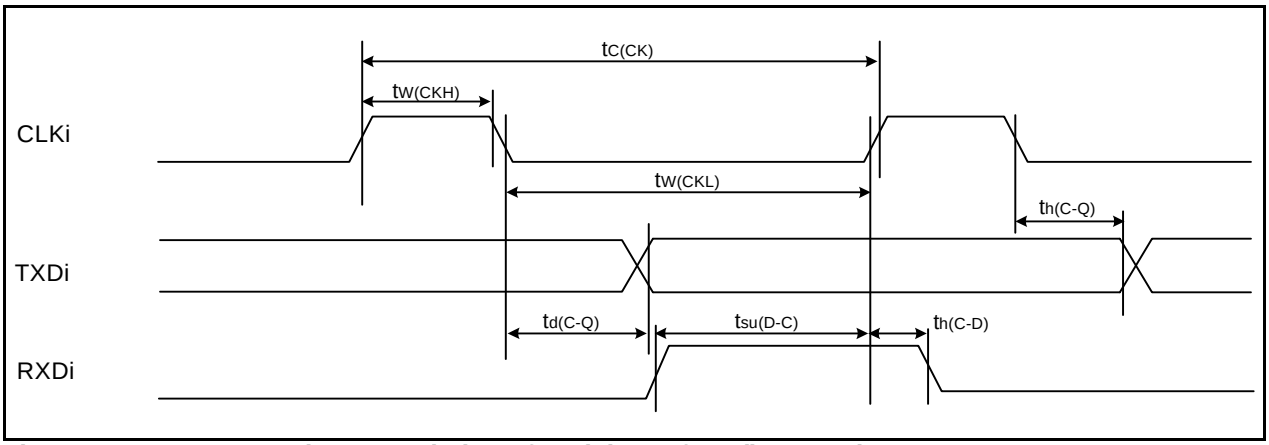


Figure 30.11 Input and Output Timing of Serial Interface (i = 0 or 1)

Table 30.29 Timing Requirements of External Interrupt $\overline{INTi}$ (i = 0 to 4) and Key Input Interrupt $\overline{KIj}$ (j = 0 to 3)

Symbol	Parameter	Standard				Unit
		Vcc = 3V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high width, $\overline{KIj}$ input high width	380 (1)	—	250 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input low width, $\overline{KIj}$ input low width	380 (2)	—	250 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input high pulse width of either (1/digital filter sampling frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input low pulse width of either (1/digital filter sampling frequency × 3) or the minimum value of standard, whichever is greater.

Figure 30.12 Input Timing of External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIj}$ (i = 0 to 4; j = 0 to 3)

31. Usage Notes

31.1 Notes on System Control

31.1.1 Option Function Select Area Setting Examples

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows setting examples.

• To set FFh in the OFS2 register

```
.org 00FFDBH
.byte 0FFh
```

Programming formats vary depending on the compiler. Check the compiler manual.

• To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h)          ; RESET
```

Programming formats vary depending on the compiler. Check the compiler manual.

31.2 Notes on Resets

31.2.1 RSTFR Register

When reading the RSTFR register successively twice or more, write 00h immediately before reading this register.

Program Example

```
MOV.B   #00H, 0028H     ; Write 00h to the RSTFR register (1)
MOV.B   0028H, A0       ; Store the read value of the RSTFR register into A0
```

Note:

1. The value of the CWR bit in the RSTFR register is not changed by writing 0.
   Also, the values of the other bits in this register are not affected because these bits are all read-only.

31.3 Notes on Clock Generation Circuit

31.3.1 Oscillation Stop Detection Function

The oscillation stop detection function cannot be used when the XIN clock frequency is below 2 MHz. In this case, set bits OCD1 and OCD0 in the OCD register to 00b (applicable: bits OCD2 and OCD3).

31.3.2 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system.

31.4 Notes on Power Control

31.4.1 Stop Mode

To enter stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before setting the CM10 bit in the CM1 register to 1 (stop mode). The 4 bytes of instruction data following the instruction that sets the CM10 bit to 1 (stop mode) are prefetched from the instruction queue and then the program stops.
Insert at least four NOP instructions following the JMP.B instruction immediately after the instruction that sets the CM10 bit to 1.

• Program example for entering stop mode

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        BSET    0, PRCR         ; Protection disabled
        FSET    I               ; Interrupt enabled
        BSET    0, CM1          ; Stop mode
        JMP.B   LABEL_001
LABEL_001:
        NOP
        NOP
        NOP
        NOP
```

31.4.2 Wait Mode

To enter wait mode by setting the CM30 bit in the CM3 register to 1, set the FMR01 bit to 0 (CPU rewrite mode disabled) before setting the CM30 bit to 1.
To enter wait mode with the WAIT instruction, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before executing the WAIT instruction. The 4 bytes of instruction data following the instruction that sets the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction are prefetched from the instruction queue and then the program stops. Insert at least four NOP instructions after the instruction that sets the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction.

• Program example for executing the WAIT instruction

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        FSET    I               ; Interrupt enabled
        WAIT                    ; Wait mode
        NOP
        NOP
        NOP
        NOP
```

• Program example for executing the instruction that sets the CM30 bit to 1

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        BSET    0, PRCR         ; Writing to CM3 register enabled
        FCLR    I               ; Interrupt enabled
        BSET    0, CM3          ; Wait mode
        NOP
        NOP
        NOP
        NOP
        BCLR    0, PRCR         ; Writing to CM3 register disabled
        FSET    I               ; Interrupt enabled
```

31.5 Notes on Interrupts

31.5.1 Reading Address 00000h

Do not read address 00000h by a program. When an external interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from address 00000h in the interrupt sequence. At this time, the corresponding IR bit in the interrupt control register for the acknowledged interrupt is set to 0.

If a program is used to read address 00000h, the corresponding IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

31.5.2 SP Setting

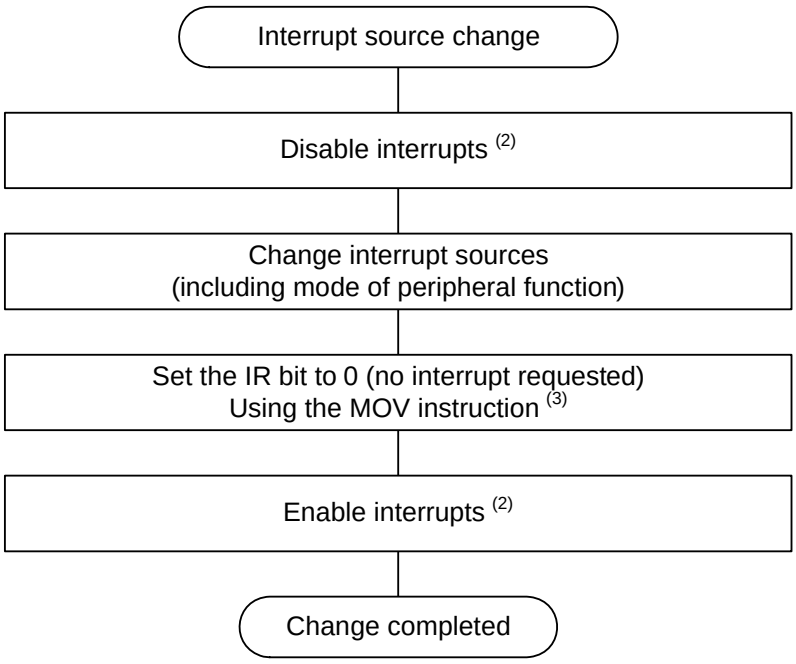
Set a value in the SP before any interrupt is acknowledged. The SP is 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

31.5.3 External Interrupt, Key Input Interrupt

Signal input to pins $\overline{\text{INT0}}$ to $\overline{\text{INT4}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ must meet either the low-level width or the high-level width requirements shown in External Interrupt $\overline{\text{INT0}}$ to $\overline{\text{INT4}}$ Input in the Electrical Characteristics, regardless of the CPU operating clock.

31.5.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source is changed. To use an interrupt, set the IR bit to 0 (no interrupt requested) after changing interrupt sources.
Changing interrupt sources as referred to here includes all factors that change the source, polarity, or timing of the interrupt assigned to a software interrupt number. Therefore, if a mode change of a peripheral function involves the source, polarity, or timing of an interrupt, set the IR bit to 0 (no interrupt requested) after making these changes. Refer to the descriptions of the individual peripheral functions for related interrupts.
Figure 31.1 shows a Procedure Example for Changing Interrupt Sources.



IR bit: Corresponding interrupt control register bit for the interrupt whose source is to be changed

Notes:
1. The above settings must be executed individually. Do not execute two or more settings simultaneously (using one instruction).
2. To prevent interrupt requests from being generated, disable the peripheral function before changing the interrupt source. In this case, use the I flag if all maskable interrupts can be disabled.
   If all maskable interrupts cannot be disabled, use bits ILVL0 to ILVL2 for the interrupt whose source is to be changed.
3. To change the interrupt source to an input with the digital filter used, wait for at least three cycles of the digital filter sampling clock + two cycles of the CPU clock before setting the IR bit to 0 (no interrupt requested).
   Refer to **11.9.5 Rewriting Interrupt Control Registers** for the instructions to use and related notes.

Figure 31.1 Procedure Example for Changing Interrupt Sources

31.5.5 Rewriting Interrupt Control Register

(a) The contents of the interrupt control register can be rewritten only while no interrupt requests corresponding to that register are generated. If an interrupt request may be generated, disable the interrupt before rewriting the contents of the interrupt control register.

(b) When rewriting the contents of the interrupt control register after disabling the interrupt, be careful to choose appropriate instructions

Changing any bit other than the IR bit

If an interrupt request corresponding to the register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt may be ignored. If this causes a problem, use one of the following instructions to rewrite the contents of the register:

Applicable instructions..... AND, OR, BCLR, and BSET

Changing the IR bit

Depending on the instruction used, the IR bit may not be set to 0 (no interrupt requested). Use the MOV instruction to set the IR bit to 0.

(c) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below. (Refer to (b) regarding rewriting the contents of interrupt control registers using the sample programs.)

Examples 1 to 3 show how to prevent the I flag from being set to 1 (interrupt enabled) before the contents of the interrupt control register are rewritten due to effects of the internal bus and the instruction queue buffer.

Example 1: Use the NOP instructions to pause the program until the interrupt control register is rewritten

```
INT_SWITCH1:
  FCLR    I              ; Interrupt disabled
  MOV.B   #00H, 0056H    ; Set the TRJIC_0 register to 00h
  NOP                    ;
  NOP
  FSET    I              ; Interrupt enabled
```

Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
  FCLR    I              ; Interrupt disabled
  MOV.B   #00H, 0056H    ; Set the TRJIC_0 register to 00h
  MOV.W   MEM, R0        ; Dummy read
  FSET    I              ; Interrupt enabled
```

Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
  PUSHC   FLG
  FCLR    I              ; Interrupt disabled
  MOV.B   #00H, 0056H    ; Set the TRJIC_0 register to 00h
  POPC    FLG            ; Interrupt enabled
```

31.6 Notes on DTC

31.6.1 DTC Activation Source

- When entering wait mode, complete DTC transfer before the cycle to execute wait mode.
- When entering stop mode, complete DTC transfer before the cycle to execute stop mode.

31.6.2 DTCENi Registers (i = 0 to 6)

- Modify bits DTCENi0 to DTCENi7 only while an interrupt request corresponding to the register is not generated.
- When the interrupt source flag in the status register for the peripheral function is 1, do not modify the corresponding activation source bit among bits DTCENi0 to DTCENi7.
- Do not access the DTCENi registers using DTC transfers.

31.6.3 Peripheral Modules

- Do not set the status register bit for the peripheral function to 0 using a DTC transfer.
- When the DTC activation source is SSU/I^2C receive data full, read the SIRDR register using a DTC transfer. The RDRF bit in the SISR register is set to 0 (no data in the SIRDR register) by reading the SIRDR register. However, the RDRF bit is not set to 0 by reading the SIRDR register when the DTC data transfer setting is either of the following:
  - Transfer causing the DTCCTj (j = 0 to 23) register value to change from 1 to 0 in normal mode
  - Transfer causing the DTCCTj register value to change from 1 to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode.
- When the DTC activation source is SSU/I^2C transmit data empty, write to the SITDR register using a DTC transfer. The TDRE bit in the SISR register is set to 0 (data is not transferred from registers SITDR to SISDR) by writing to the SITDR register.

31.6.4 Interrupt Requests

- When the DTC activation source is either SSU/I^2C transmit data empty or flash ready status, no interrupt request is generated for the CPU in either of the following cases:
  - When the DTC performs a data transfer that causes the DTCCTj register value to change to 0 in normal mode.
  - When the DTC performs a data transfer that causes the DTCCRj register value to change to 0 while the RPTINT bit in the DTCCRj register is 1 in repeat mode.

31.6.5 DTC Activation

- When the DTC is activated, operation may be shifted for one cycle before reading a vector.

31.7 Notes on Timer RJ

(1) The timer count is stopped after a reset. Start the count only after setting the values of the registers associated timer RJ (1).
Note:
1. Registers associated with timer RJ: TRJCR, TRJIOC, TRJMR, TRJ, and TRJISR

(2) There are the following restrictions on register access while the count is stopped, depending on the timer mode:
• Event counter mode
After 1 (count starts) is written to the TSTART bit in the TRJCR register while the count is stopped, the TCSTF bit in the TRJCR register remains 0 (count stops) for two cycles of the CPU clock. Do not write to the TRJCR register until the TCSTF bit is set to 1. Also, do not access other registers associated with timer RJ (1). After the TCSTF bit is set to 1, the count is started from the first active edge of the count source.
After 0 (count stops) is written to the TSTART bit during a count operation, the TCSTF bit remains 1 for two cycles of the CPU clock. When the TCSTF bit is set to 0, the count is stopped. Do not write to the TRJCR register until the TCSTF bit is set to 0. Also, do not access other registers associated with timer RJ (1). Writing to the TRJ register has no effect until the TRJIO pin is set to the inactive level (low level when the TEDGSEL bit in the TRJIOC register is 0 and high level when this bit is 1). To change the TRJ register in this case, use the following procedure:
1. Write 0 to the TSTART bit to stop the count.
2. Wait until the TCSTF bit is set to 0.
3. Set bits TIPF1 and TIPF0 in the TRJIOC register to 00b (no filter). This setting is not necessary when no digital filter is used.
4. Write 1 and then write 0 to the TEDGSEL bit.
5. Set the TEDGSEL bit to the previous value (value before step 4).
Step 5 is not necessary if the value before step 4 is 0.
6. Set bits TIPF1 and TIPF0 to the previous value (value before step 3).
This step is not necessary when the digital filter is not used.
7. Access the TRJ register.

• Modes other than event counter mode
After 1 (count starts) is written to the TSTART bit while the count is stopped, the TCSTF bit remains 0 (count stops) for three cycles of the count source. Do not write to the TRJCR register until the TCSTF bit is set to 1. Also, do not access other registers associated with timer RJ (1). After the TCSTF bit is set to 1, the count is started at the first active edge of the counter source.
After 0 (count stops) is written to the TSTART bit during a count operation, the TCSTF bit remains 1 for three cycles of the count source. When the TCSTF bit is set to 0, the count is stopped. Do not write to the TRJCR register until the TCSTF bit is set to 0. Also, do not access other registers associated with timer RJ (1).

Note:
1. Registers associated with timer RJ: TRJIOC, TRJMR, TRJ, and TRJISR

(3) In event counter mode, set the TSTART bit in the TRJCR register to 1 (count starts), and then input an external pulse after the TCSTF bit is set to 1.

(4) In pulse width/pulse period measurement modes, bits TEDGF and TUNDF in the TRJCR register used are set to 0 by writing 0 by a program, but remain unchanged even if 1 is written to these bits. If a bit manipulation instruction is used to set the TRJCR register, bits TEDGF and TUNDF may be erroneously set to 0 depending on the timing, even when the TEDGF bit is set to 1 (active edge received) and the TUNDF bit is set to 1 (underflow) during execution of the instruction.
In order to avoid this, set bits TEDGF and TUNDF to 1 using the MOV instruction.

(5) Insert two NOP instructions between writing to and reading from registers associated with timer RJ (1) while the timer RJ count is stopped.
Note:
1. Registers associated with timer RJ: TRJCR, TRJIOC, TRJMR, TRJ, and TRJISR

(6) When the TSTART bit in the TRJCR register is 1 (count starts) and the TCSTF bit is 1 (count in progress), allow at least three cycles of the count source clock between writes when writing to the TRJ register successively.

(7) After changing to pulse width measurement mode or pulse period measurement mode from another mode, the values of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before starting timer RJ count.

(8) To lower current consumption, switch to module standby state when bits TSTART and TCSTF in TRJCR are 0 (count stops). For details on the bits for switching to module standby state, refer to **10.2.9 Module Standby Control Register 2 (MSTCR2)**.

(9) In pulse width measurement mode or pulse period measurement mode, perform settings in the following order:

1. Set the registers associated with timer RJ (1).
2. Set the TSTART bit to 1 (count starts) and then wait until the TCSTF bit is set to 1 (count is in progress).
3. Input an external event.

Note:

1. Registers associated with timer RJ: TRJCR, TRJIOC, TRJMR, TRJ, and TRJISR

(10) In pulse period measurement mode, the processing on completion of the first measurement is invalid (the measured value is valid for the second and subsequent times)

(11) The TRJ register must not be set to 0000h.

(12) In pulse width measurement mode and event counter mode, do not select an event from the event link controller (ELC) as the count source.

(13) In pulse output mode, set the TOPCR bit in the TRJIOC register after setting the TRJMR register.

(14) The registers associated with timer RJ operating mode (TRJIOC, TRJMR, and TRJISR) can be changed only when the count is stopped (both the TSTART and TCSTF bits in the TRJCR register are 0 (count stops)). Do not change these registers during count operation.

• Applicable: All modes of timer RJ

31.8 Notes on Timer RB2

(1) Timer RB2 stops counting after a reset. Start the count after setting the values in the timer and prescaler.

(2) While using the 16-bit timer, when accessing registers TRBPRE, TRBPR, and TRBSC in 8-bit units (8-bit access), always access TRBPRE, TRBPR, and TRBSC in that order.

(3) In programmable one-shot and programmable wait one-shot generation modes, when the TOSSP bit in the TRBOCR register is set to 1 and the one-shot is stopped, the timer reloads the reload register value and is stopped. The timer count value must be read before the timer is stopped.

(4) After 1 (count starts) is written to the TSTART bit in the TRBCR register while the count is stopped, the TCSTF bit in the TRBCR register remains 0 (count stops) for two or three cycles of the count source. Do not access the registers associated with timer RB2 (1) other than the TCSTF bit until this bit is set to 1 (count in progress).
After 0 (count stops) is written to the TSTART bit during count operation, the TCSTF bit remains 1 for two or three cycles of the count source. When the TCSTF bit is set to 0, the count is stopped. Do not access the registers associated with timer RB2 (1) other than the TCSTF bit until this bit is set to 0.

Note:
1. Registers associated with timer RB2:
TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBPR, and TRBSC

(5) When the TSTART bit is 0 (count stops), wait for at least two cycles of the CPU clock and then set the TSTART bit to 1 (count starts) to change the values of registers TRBPRE, TRBPR, and TRBSC.

(6) When the TSTART bit is 1 (count starts) or the TCSTF bit is 1 (count in progress), do not change the values of registers TRBIOC and TRBMR, and the TRBIE bit in the TRBIR register. The TOCNT bit can be changed during count operation, according to the specifications shown in 16.5.3.

(7) When 1 is written to the TSTOP bit in the TRBCR register during count operation (the TCSTF bit is 1), timer RB2 stops without any wait time (the TSTART bit is 0, the TCSTF bit is 0, the TOSST bit is 0, and the TOSSTF bit is 0).

(8) When 1 (one-shot starts) is written to the TOSST bit in the TRBOCR register, the TOSSTF bit changes after three cycles of the timer RB count source. If 1 (one-shot stops) is written to the TOSSP bit in the TRBOCR register, the TOSSTF bit changes after two or three cycles of the RB count source. If 1 is written to the TOSSP bit during the period after 1 is written to the TOSST bit but before the TOSSTF bit can become 1 (one-shot is operating (including wait period)), depending on the internal state the TOSSTF bit may become 0 (one-shot is stopped) or 1. Similarly, if 1 is written to the TOSST bit during the period after 1 is written to the TOSSP bit but before the TOSSTF bit can become 0, the TOSSTF bit may become 0 or 1.

(9) When the underflow signal from timer RJ is used as the count source for timer RB2, set timer RJ to timer mode, pulse output mode, or event counter mode.

(10) Make sure that the TCSTF bit is 1 (count in progress) before writing 1 (one-shot count starts) to the TOSST bit in the TRBOCR register. When the TCSTF bit is 0 (count stops), writing 1 (one-shot count starts) to the TOSST bit has no effect.

(11) In programmable waveform and programmable wait one-shot generation modes of timer RB2, write to the TRBSC register before writing to the TRBPR register. The value of the TRBPR register is reflected to the counter during the underflow of the secondary period after the TRBPR register is written. If registers TRBSC and TRBPR are written multiple times during the period after the TRBPR register was written but before the secondary period underflow, the data that was written last will be reflected in the counter. However, do not write to the TRBSC register only on its own. Write to both the TRBSC and TRBPR registers.

(12) When writing to and reading from the TRBPRE or TRBPR register successively while the count is stopped, insert NOP instructions between writing and reading.

(13) When writing to registers TRBPRE, TRBPR, and TRBSC during count operation (the TSTART bit is 1 or the TCSTF bit is 1), note the following points:
- When writing to the TRBPRE register successively, allow at least three cycles of the count source between writes.
- When writing to the TRBPR register successively, allow at least three cycles of the prescaler underflow between writes.
- When writing to the TRBSC register successively, allow at least three cycles of the prescaler underflow between writes.

(14) To lower current consumption, switch to standby module state while bits TSTART and TCSTF in the TRBCR register are both 0 (count stops). For details on the bits for switching to module standby state, refer to **10.2.9 Module Standby Control Register 2 (MSTCR2)**

(15) To forcibly stop the count using the TSTOP bit, set as follows:
(1) Set the interrupt priority level of the TRB2IC_0 register to 0 (interrupt disabled).
(2) Set the TSTOP bit to 1 (count is forcibly stopped).
(3) Set the TRBIF bit to 0 (no interrupt requested)

(16) When the TRBPR register is rewritten in programmable waveform generation mode, do not write to the TRBPRE, TRBPR, or TRBSC register at the following timing during the next secondary period after rewriting.
- 8-bit timer with 8-bit prescaler:
  Two cycles of the prescaler underflow before the secondary output period ends.
- 16-bit timer:
  Two cycles of the count source clock before the secondary output period ends.

31.9 Notes on Timer RC

31.9.1 TRCCNT Register

The following notes apply when the CCLR bit in the TRCCR1 register is set to 1 (TRCCNT counter is cleared by input capture/compare match A).

- When writing a value to the TRCCNT register by a program while the CTS bit in the TRCMR register is set to 1 (count starts), ensure that the write timing does not coincide with when the TRCCNT register is set to 0000h.
- If the timing when the TRCCNT register is set to 0000h and is written coincide, the value is not written and the TRCCNT register is set to 0000h.

If the TRCCNT register is written and read, the value before this register is written may be read. In this case, execute the JMP.B instruction between the write and read instructions.

- Program Example

```
        MOV.W   #XXXXh, TRCCNT      ; Write
        JMP.B   L1                  ; JMP.B instruction
L1:     MOV.W   TRCCNT, DATA        ; Read
```

31.9.2 TRCCR1 Register

When setting bits CKS2 to CKS0 in the TRCCR1 register to 111b (fHOCO-F), set fHOCO-F to a clock frequency higher than the CPU clock frequency.

31.9.3 TRCSR Register

If the TRCSR register is written and read, the value before this register is written may be read. In this case, execute the JMP.B instruction between the write and read instructions.

- Program Example

```
        MOV.B   #XXh, TRCSR         ; Write
        JMP.B   L1                  ; JMP.B instruction
L1:     MOV.B   TRCSR, DATA         ; Read
```

31.9.4 Count Source Switching

- When switching the count source, stop the count before switching. After switching the count source, wait for at least two cycles of the CPU clock before writing to the registers (at addresses 00138h to 0014Dh) associated with timer RC.

[Changing procedure]

(1) Set the CTS bit in the TRCMR register to 0 (count stops).
(2) Change bits CKS0 to CKS2 in the TRCCR1 register.
(3) Wait for at least two cycles of the CPU clock.
(4) Write to the registers (at addresses 00138h to 0014Dh) associated with timer RC.

- When changing the count source from fHOCO-F to fHOCO and stopping fHOCO-F, wait for at least two cycles of fHOCO-F after changing the clock setting before stopping fHOCO-F.

[Changing procedure]

(1) Set the CTS bit in the TRCMR register to 0 (count stops).
(2) Change bits CKS0 to CKS2 in the TRCCR1 register.
(3) Wait for at least two cycles of fHOCO-F.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

• When changing the count source from fHOCO-F to another source and stopping fHOCO-F, wait for at least one cycle of fHOCO-F + one cycle of fHOCO after changing the clock setting before stopping fHOCO-F.

[Changing procedure]

(1) Set the CTS bit in the TRCMR register to 0 (count stops).
(2) Change bits CKS0 to CKS2 in the TRCCR1 register.
(3) Wait for at least one cycle of fHOCO-F + one cycle of fHOCO.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

Notes:

1. Do not set the FRA00 bit to 0 (high-speed on-chip oscillator off) while fHOCO or fHOCO-F is selected as the count source.
2. Do not change the division ratio of the high-speed on-chip oscillator set by the FRA2 register while fHOCO-F is selected as the count source.

31.9.5 Input Capture Function

Set the pulse width of the input capture signal as follows:
[When the digital filter is not used]
Three or more cycles of the timer RC operation clock (refer to Table 17.1 Timer RC Specifications)
[When the digital filter is used]
Five cycles of the digital filter sampling clock + three cycles of the timer RC operating clock, minimum (refer to **Figure 17.19 Digital Filter Circuit Block Diagram**)

The value of the TRCCNT register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).

31.9.6 TRCMR Register in PWM2 Mode

When the CSTP bit in the TRCCR2 register is 1 (count is stopped at compare match with TRCGRA register), do not set the TRCMR register when a compare match occurs between registers TRCCNT and TRCGRA.

31.9.7 Module Standby

Write to the MSTTRC_0 bit in the MSTCR2 register while the timer RC count is stopped. The timer RC module standby bit exists in the MSTCR2 register.

31.9.8 Mode Switching

- When switching modes during operation, set the CTS bit in the TRCMR register to 0 (count stops) before switching.
- After switching modes, set the flags in the TRCSR register to 0 and set the IR bit in the TRCIC register to 0 before starting operation.
  For details, refer to **11.9.4 Changing Interrupt Sources**.

31.9.9 Input Capture Operation when Count is Stopped

When the input capture function is used, if an input capture signal (edge selected by bits IOj0 and IOj1 (j = A or B) in the TRCIOR0 register or bits IOk0 and IOk1 (k = C or D) in the TRCIOR1 register) is input to the TRCIOi pin (i = A, B, C, or D), the IMFi bit in the TRCSR register is set to 1 even when the CTS bit in the TRCMR register is set to 0 (count stops).

31.10 Notes on Timer RD

31.10.1 SFR Read/Write Access

31.10.1.1 TRDELCCR Register

- Do not rewrite the TRDELCCR register during timer operation.

31.10.1.2 TRDSTR Register

- Write to the TRDSTR register using the MOV instruction.
- When the CSELi bit (i = 0 or 1) in the TRDSTR register is set to 0 (count stops at compare match between registers TRDi and TRDGRAi), the count does not stop and the TSTARTi bit remains unchanged even if 0 (count stops) is written to the TSTARTi bit.
  The TSTARTi bit is set to 0 (count stops) only by a compare match with the TRDGRAi register.
  If the CSELi bit is 0 when rewriting the TRDSTR register, write 0 to the TSTARTi bit to change the CSELi bit to 1 without affecting the count operation.
  If 1 is written to the TSTARTi bit while the counter is stopped, the count may be started.
  To stop counting by a program, set the TSTARTi bit after setting the CSELi bit to 1. Even if 1 is written to the CSELi bit and 0 is written to the TSTARTi bit at the same time (using one instruction), the count cannot be stopped.
- Table 31.1 lists the TRDIOji Pin (j = A, B, C, or D) Output Level when Count is Stopped while the TRDIOji pin is used for timer RD output.

Table 31.1 TRDIOji Pin (j = A, B, C, or D) Output Level when Count is Stopped

Count Stop	TRDIOji Pin Output When Count is Stopped
When the CSELi bit is set to 1, write 0 to the TSTARTi bit and the count stops.	The pin retains the output level immediately before the count stops. (The pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register in timer RD complementary and reset synchronous PWM modes.)
When the CSELi bit is set to 0, the count stops at a compare match between registers TRDi and TRDGRAi.	The pin retains the output level after the output change due to the compare match. (The pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register in timer RD complementary and reset synchronous PWM modes.)

i = 0 or 1, j = A, B, C, or D

31.10.1.3 TRDi Register

- When writing to the TRDi register overlaps with the timing for setting the TRDi register to 0000h, the write value has priority.
- When writing a value to the TRDi register and then reading the same register consecutively, the value before writing may be read. In this case, execute the JMP.B instruction between writing and reading.

```
Program example     MOV.W   #XXXXh, TRD0    ; Write
                    JMP.B   L1              ; JMP.B
                L1: MOV.W   TRD0, DATA      ; Read
```

31.10.1.4 TRDSRi Register (i = 0 or 1)

When writing a value to the TRDSRi register and then reading the same register consecutively, the value before writing may be read. In this case, execute the JMP.B instruction between writing and reading.

```
Program example     MOV.B   #XXh, TRDSR0      ; Write
                    JMP.B   L1                ; JMP.B
                L1: MOV.B   TRDSR0, DATA      ; Read
```

31.10.1.5 TRDCRi Register

When setting bits TCK2 to TCK0 in the TRDCRi register to 111b (fHOCO-F), set fHOCO-F to a clock frequency higher than the CPU clock frequency.

31.10.1.6 TRDDFi Register

As a hazard precaution, set bits DFCK0 and DFCK1 in the TRDDFi register before starting the count operation.

31.10.2 Mode Switching

- When switching modes during operation, first stop the count (TSTART = 0) before switching.
- After switching modes, clear the interrupt register before starting operation.
  Refer to **11.9.4 Changing Interrupt Sources**.

31.10.3 Count Source Switching

- Switch the count source after stopping the count.
  Also, after switching the count source, wait for at least two cycles of the CPU clock before writing to the SFR of the module.
  [Changing procedure]
  (1) Set the TSTARTi bit in the TRDSTR register to 0 (count stops).
  (2) Change bits TCK0 to TCK2 in the TRDCRi register.
  (3) Wait for at least two cycles of the CPU clock.
  (4) Writing to the SFR of timer RD is enabled.
- Instead of the setting change in the above step (2), the same processing is also necessary when changing the settings of bits SYNC and PWM3.
  Software processing is not necessary when stopping the high-speed on-chip oscillator using the FRA00 bit.
- When changing the count source from fHOCO-F to fHOCO and stopping fHOCO-F, wait for at least two cycles of fHOCO-F after changing the clock setting before stopping fHOCO-F.
  [Changing procedure]
  (1) Set the TSTARTi bit in the TRDSTR register to 0 (count stops).
  (2) Change bits TCK0 to TCK2 in the TRDCRi register.
  (3) Wait for at least two cycles of fHOCO-F.
  (4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

• When changing the count source from fHOCO-F to a clock other than fHOCO and stopping fHOCO-F, wait at least one cycle of fHOCO-F + one cycle of fHOCO after changing the clock setting before stopping fHOCO-F.
[Changing procedure]
(1) Set the TSTARTi bit (i = 0 or 1) in the TRDSTR register to 0 (count stops).
(2) Change bits TCK0 to TCK2 in the TRDCRi register.
(3) Wait for at least one cycle of fHOCO-F + one cycle of fHOCO.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

Notes:
1. Do not set the FRA00 bit to 0 (high-speed on-chip oscillator off) while fHOCO or fHOCO-F is selected as the count source.
2. Do not change the division ratio of the high-speed on-chip oscillator set by the FRA2 register while fHOCO-F is selected as the count source.

31.10.4 Input Capture Function

• Set the pulse width of the input capture signal to three or more cycles of the timer RD operating clock (refer to **Table 18.1 Timer RD Operating Clocks**).
• The value of the TRDi register is transferred to the TRDGRji register two to three cycles of the timer RD operating clock after the input capture signal is applied to the TRDIOji pin (i = 0 or 1, j = A, B, C, or D) (when no digital filter is used).

31.10.5 Reset Synchronous PWM Mode

• When reset synchronous PWM mode is used for motor control, make sure OLS0 = OLS1.
• When setting reset synchronous PWM mode, use the following procedure:
[Changing procedure]
(1) Set the TSTART0 bit in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 and CMD0 in the TRDFCR register to 00b (timer mode, PWM mode, and PWM3 mode).
(3) Set bits CMD1 and CMD0 to 01b (reset synchronous PWM mode).
(4) Set the other registers associated with timer RD again.
• Notes on Starting Count
(1) If the timer value and the compare value are set to the same value, the count must not be started.
(2) When restarting the count once after it has stopped, verify that the timer value when the count stopped and the compare register value are different before restarting. If their values are the same, rewrite the timer value before restarting the count.

31.10.6 Complementary PWM Mode

- When complementary PWM mode is used for motor control, make sure OLS0 = OLS1.
- Change bits CMD0 and CMD1 in the TRDFCR register in the following procedure.

Changing procedure: When setting to complementary PWM mode (including re-set) or changing the transfer timing from the buffer register to the general register in complementary PWM mode.

(1) Set both the TSTART0 and TSTART1 bits in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 and CMD0 in the TRDFCR register to 00b (timer mode, PWM mode, and PWM3 mode).
(3) Set bits CMD1 and CMD0 to 10b or 11b (complementary PWM mode).
(4) Set the other registers associated with timer RD again.

Changing procedure: When stopping complementary PWM mode

(1) Set both the TSTART0 and TSTART1 bits in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 to CMD0 to 00b (timer mode, PWM mode, and PWM3 mode).

- Do not write to the TRDGRA0, TRDGRB0, TRDGRA1, or TRDGRB1 register during operation.
  When changing the PWM waveform, transfer the values written to registers TRDGRD0, TRDGRC1, and TRDGRD1 to registers TRDGRB0, TRDGRA1, and TRDGRB1 using buffer operation.
  However, to write data to the TRDGRD0, TRDGRC1, or TRDGRD1 register, set bits BFD0, BFC1, and BFD1 to 0 (general register). After this, bits BFD0, BFC1, and BFD1 may be set to 1 (buffer register).
  The PWM period cannot be changed.
- If the value set in the TRDGRA0 register is assumed to be m, the TRD0 register counts m - 1, m, m + 1, m, m - 1, in that order, when changing from increment to decrement operation.
  When changing from m to m + 1, the IMFA bit in the TRDSRi register is set to 1. Also, bits CMD1 and CMD0 in the TRDFCR register are set to 11b (complementary PWM mode, buffer data transferred at compare match between registers TRD0 and TRDGRA0), the content of the buffer registers (TRDGRD0, TRDGRC1, and TRDGRD1) is transferred to the general registers (TRDGRB0, TRDGRA1, and TRDGRB1).
  During the operation of m + 1, m, and m - 1, the IMFA bit remains unchanged and data is not transferred to registers such as the TRDGRA0 register.

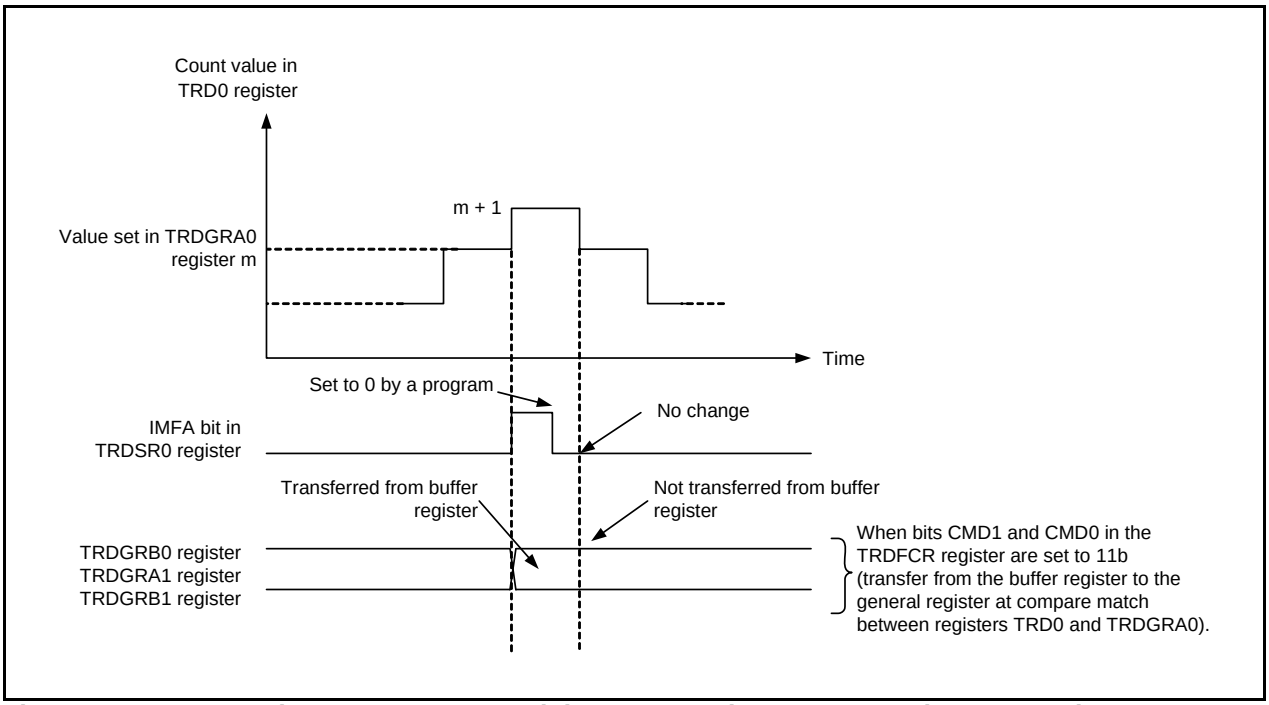


Figure 31.2 Operation at Compare Match between Registers TRD0 and TRDGRA0 in Complementary PWM Mode

• The TRD1 register counts 1, 0, FFFFh, 0, 1, in that order, when changing from decrement to increment operation.
Counting from 1, to 0, to FFFFh causes the UDF bit in the TRDSRi register to be set to 1. Also, when bits CMD1 and CMD0 in the TRDFCR register are set to 10b (complementary PWM mode, buffer data transferred at underflow of the TRD1 register), the content of the buffer registers (TRDGRD0, TRDGRC1, and TRDGRD1) is transferred to the general registers (TRDGRB0, TRDGRA1, and TRDGRB1).
During the operation of FFFFh, 0, and 1, data is not transferred to registers such as the TRDGRB0 register. Also, at this time, the OVF bit in the TRDSRi register remains unchanged.

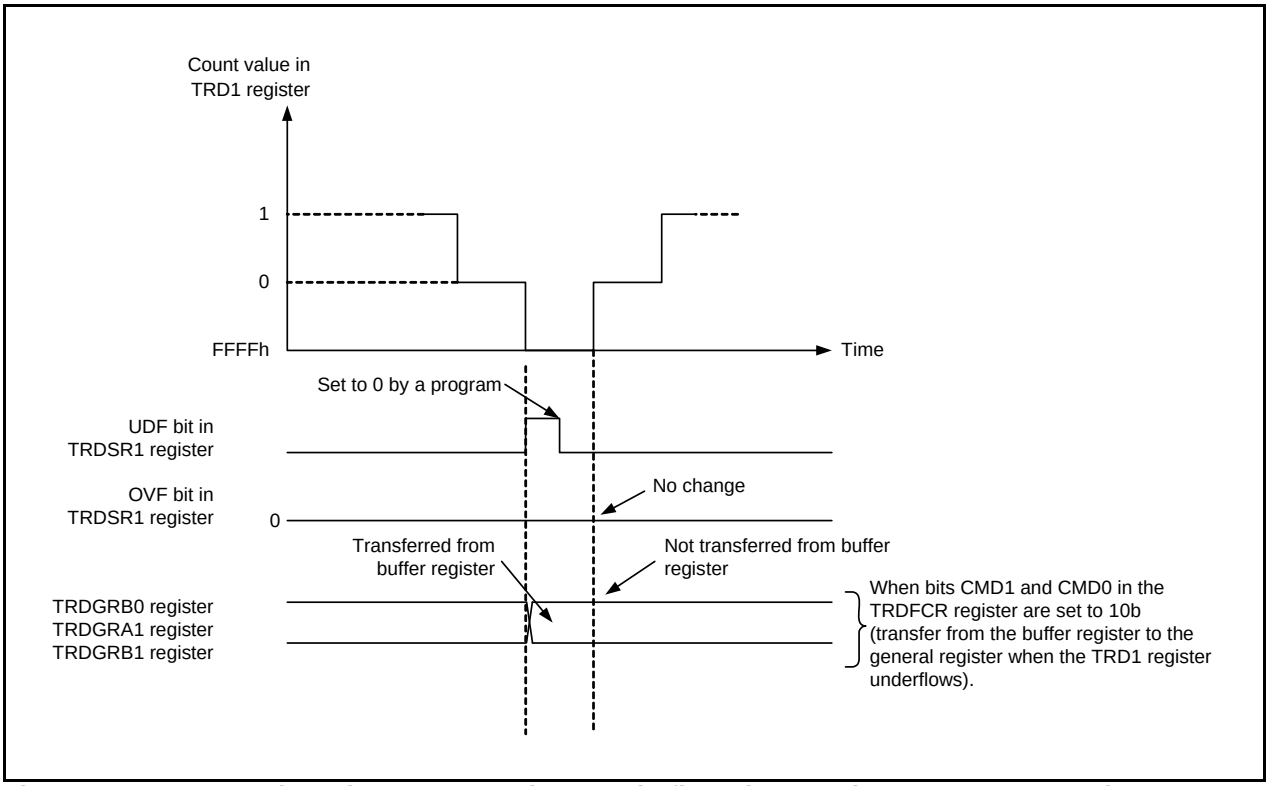


Figure 31.3 Operation when TRD1 Register Underflows in Complementary PWM Mode

• Select the timing of data transfer from the buffer register to the general register using bits CMD1 and CMD0 in the TRDFCR register. However, transfer takes place with the following timing regardless of the value of bits CMD1 and CMD0 in the following cases:

Value in buffer register ≥ value in TRDGRA0 register:

Transfer takes place at underflow of the TRD1 register.

After this, when the buffer register is set to a value that is 0001h or above and smaller than the value of the TRDGRA0 register, and the TRD1 register underflows for the first time after setting, the value is transferred to the general register. After that, the value is transferred with the timing selected by bits CMD1 and CMD0.

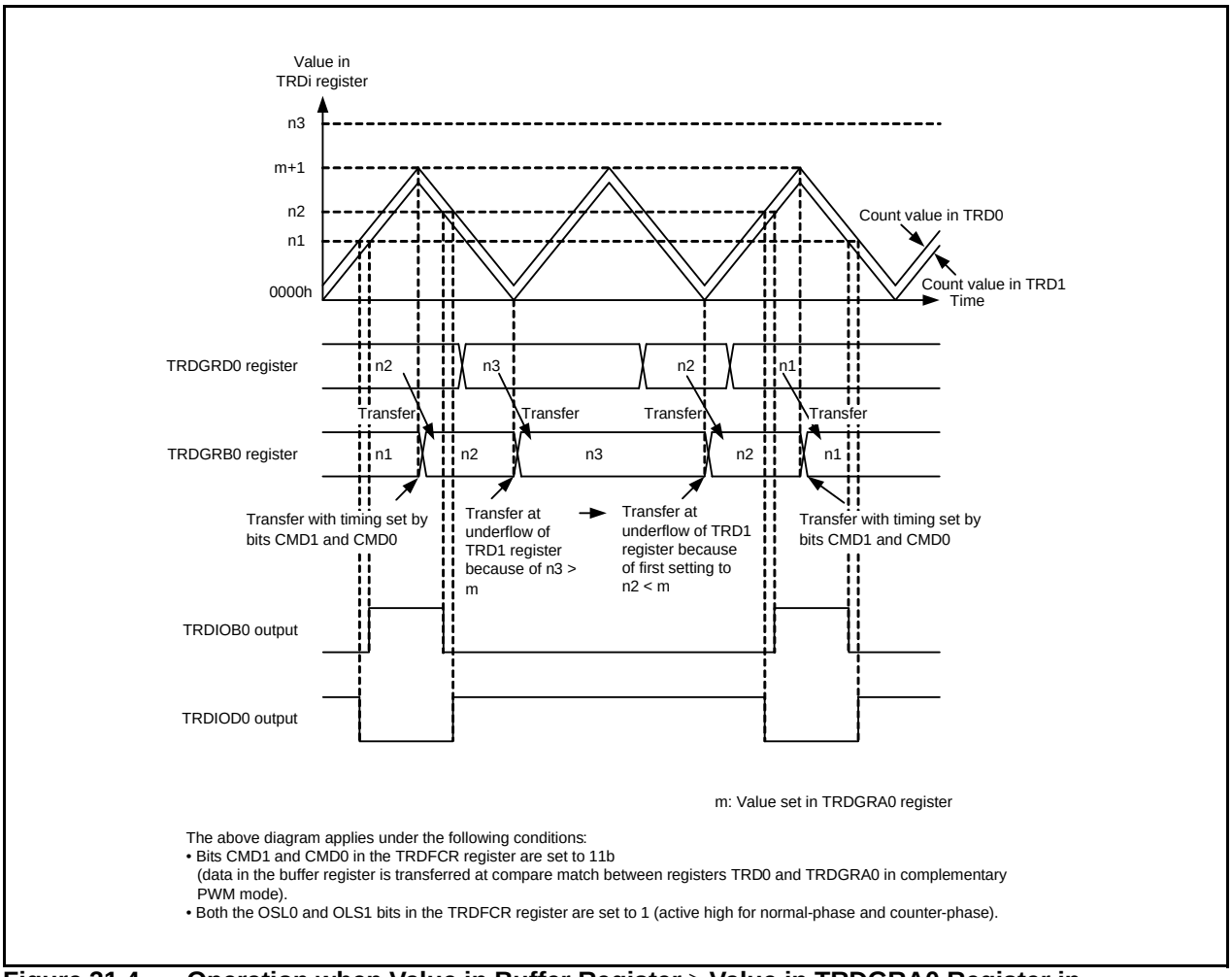


Figure 31.4 Operation when Value in Buffer Register ≥ Value in TRDGRA0 Register in Complementary PWM Mode (i = 0 or 1)

When the value in the buffer register is set to 0000h:

Transfer takes place at compare match between registers TRD0 and TRDGRA0.

After this, when the buffer register is set to a value that is 0001h or above and smaller than the value of the TRDGRA0 register, and a compare match occurs between registers TRD0 and TRDGRA0 for the first time after setting, the value is transferred to the general register. After that, the value is transferred with the timing selected by bits CMD0 and CMD1.

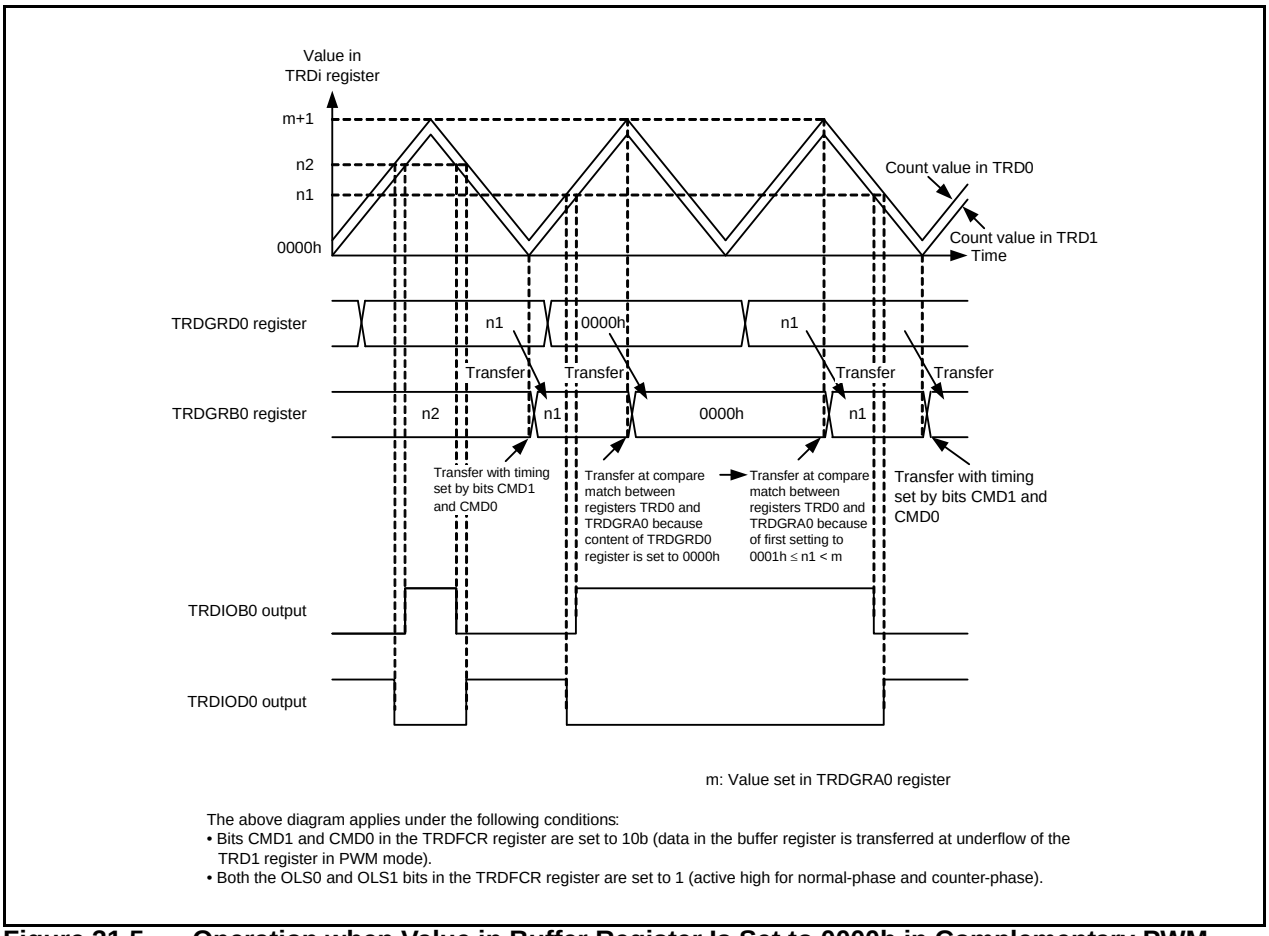


Figure 31.5 Operation when Value in Buffer Register Is Set to 0000h in Complementary PWM Mode (i = 0 or 1)

• Notes on Starting Count

(1) If the timer value and the compare value are set to the same value, the count must not be started.

(2) When restarting the count once after it has stopped, verify that the timer value when the count stopped and the compare register value are different before restarting. If their values are the same, rewrite the timer value before restarting the count.

31.10.7 Input Capture Operation when Count is Stopped

When the input capture function is used, if an input capture signal (edge selected by bits IOj0 and IOj1 (j = A or B) in the TRDIORAi register (i = 0 or 1) or bits IOk0 and IOk1 (k = C or D) in the TRDIORCi register) is input to the TRDIOni pin (n = A, B, C, or D), the IMFn bit in the TRDSRi register is set to 1 even when the TSTARTi bit in the TRDSTR register is set to 0 (count stops).

31.11 Notes on Timer RE2

- When 0 (count stops) is written to the RUN bit in the TRECR register, the count is stopped after three cycles of the count source.
- When entering module standby, set the TREOE bit in the TRECR register to 0 (TMRE2O output disabled) and set the RUN bit to 0 (count stops), and then allow three or more cycles of the count source to elapse before setting the MSTTRE bit in the MSTCR3 register to 1 (standby).
- Switch bits OS0 to OS2 in the TRECSR register while the TREOE bit in the TRECR register is 0 (TMRE2O output disabled).
- Switching registers TREIFR and TREIER must be performed as follows:
  - Switch the CMIE bit in the TREIER register while the CMIF bit in the TREIFR register is 0 (no interrupt requested).
  - Switch the OVIE bit in the TREIER register while the OVIF bit in the TREIFR register is 0 (no interrupt requested).
- Set the RTCRST bit in the TRECR register while the OVIF bit is 0 (no interrupt requested) and the CMIF bit is 0 (no interrupt requested).

31.12 Notes on Serial Interface (UART0)

31.12.1 Common to All Operating Modes

31.12.1.1 Register Access

The settings of the following registers can only be changed when the serial interface is disabled. Do not change these settings when the serial interface is enabled.
• Registers U0MR_0 and U0MR_1: CKDIR bit
• Registers U0C0_0 and U0C0_1: Bits CLK0 and CLK1
• Registers U0IR_0 and U0IR_1: Bits U0RIE and U0TIE

The settings of the following registers can only be changed while transmission/reception is stopped. Do not change these settings during transmission/reception.
• Registers U0MR_0 and U0MR_1: Bits SMD0 to SMD2, STPS, PRY, and PRYE
• Registers U0BRG_0 and U0BRG_1: Bits b0 to b7
• Registers U0C0_0 and U0C0_1: Bits DFE, NCH, CKPOL, and UFORM
• Registers U0C1_0 and U0C1_1: Bits U0IRS and U0RRM

Regardless of clock synchronous I/O mode or clock asynchronous I/O mode, read the U0RB register in 16-bit units.
When the higher byte (b15 to b8) in the U0RB register is read, bits FER and PER in the U0RB register are set to 0 (no framing error, no parity error). Also, the RI bit in the U0C1 register is set to 1 (no data in the U0RB register). To check for receive errors, use the data read from the U0RB register.

• Program example for reading the receive buffer register

```
MOV.W    0086H, R0          ; Read the U0RB register
```

When the transfer data is 9 bits long in clock asynchronous I/O mode, write to the higher byte (b15 to b8) first and then the lower byte (b7 to b0) in 8-bit units.

• Program example for writing to the transmit buffer register

```
MOV.B    #XXH, 0083H        ; Write to the higher byte (b15 to b8) in the U0TB register
MOV.B    #XXH, 0082H        ; Write to the lower byte (b7 to b0) in the U0TB register
```

• Do not set the MSTUART_0 or MSTUART_1 bit in the MSTCR0 register to 1 (standby) during communication. When setting the module to the standby state, confirm whether communication has completed. After communication has completed, set bits TE and RE in the U0C1 register to 0 (communication disabled) before setting the module to the standby state. After the module standby state is cleared, the initial settings for communication must be set up again.

31.12.1.2 N-Channel Open-Drain Control Bit

When UART0 is not used, set the NCH bit in the U0C0 register to 0 (TXD pin is set to CMOS output).

31.13 Notes on Serial Interface (UART2)

31.13.1 Common to All Operating Modes

31.13.1.1 Register Access

The settings of the following registers can only be changed when the serial interface is disabled. Do not use these settings when the serial interface is enabled.
U2MR register: CKDIR bit
U2C0 register: Bits CLK0 and CLK1

The settings of the following registers can only be changed while transmission/reception is stopped. Do not use these settings during transmission/reception.
U2MR register: Bits SMD0 to SMD2, STPS, PRY, PRYE, and IOPOL
U2BRG register: Bits b0 to b7
U2C0 register: Bits CRS, CRD, NCH, CKPOL, and UFORM
U2C1 register: Bits U2IRS, U2RRM, U2LCH, and U2ERE
U2RXDF register: DF2EN bit
U2SMR5 register: MP bit
U2SMR3 register: NODC bit
U2SMR register: Bits ABSCS, ACSE, and SSS

31.13.1.2 N-Channel-Open-Drain Control Bit

When UART2 is not used, set the following bits to 0.
U2C0 register: NCH bit
U2SMR3 register: NODC bit

31.13.2 Clock Synchronous Serial I/O Mode

31.13.2.1 Transmission/Reception

When the $\overline{\text{RTS}}$ function is used with an external clock, the $\overline{\text{RTS2}}$ pin outputs a low level, which informs the transmitting side that the MCU is ready for a receive operation. The $\overline{\text{RTS2}}$ pin outputs a high level when a receive operation starts. Therefore, the transmit timing and receive timing can be synchronized by connecting the $\overline{\text{RTS2}}$ pin to the $\overline{\text{CTS2}}$ pin of the transmitting side. The $\overline{\text{RTS}}$ function is disabled when an internal clock is selected.

31.13.2.2 Transmission

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit in the U2C0 register is set to 0 (transmit data is output at the falling edge and receive data is input at the rising edge of the transfer clock), or while the external clock is held low when the CKPOL bit is set to 1 (transmit data is output at the rising edge and receive data is input at the falling edge of the transfer clock).
• The TE bit in the U2C1 register = 1 (transmission enabled)
• The TI bit in the U2C1 register = 0 (data present in the U2TB register)
• If the $\overline{\text{CTS}}$ function is selected, input to the $\overline{\text{CTS2}}$ pin = Low

31.13.2.3 Reception

In clock synchronous serial I/O mode, the shift clock is generated by activating the transmitter. Set the UART2-associated registers for transmit operation even if the MCU is used for receive operation only. Dummy data is output from the TXD2 pin while receiving.

When an internal clock is selected, the shift clock is generated by setting the TE bit in the U2C1 register to 1 (transmission enabled) and placing dummy data in the U2TB register. When an external clock is selected, set the TE bit to 1 (transmission enabled), place dummy data in the U2TB register, and input an external clock to the CLK2 pin to generate the shift clock.

If data is received consecutively, an overrun error occurs when the RE bit in the U2C1 register is set to 1 (data present in the U2RB register) and the next receive data is received in the UART2 receive register. Then, the OER bit in the U2RB register is set to 1 (overrun error). At this time, the U2RB register retains the previous receive data. If an overrun error occurs, use a program on the transmitting and receiving sides to resend the data that caused the error.

To receive data consecutively, set dummy data in the low-order byte in the U2TB register at each receive operation.

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit is set to 0, or while the external clock is held low when the CKPOL bit is set to 1.
• The RE bit in the U2C1 register = 1 (reception enabled)
• The TE bit in the U2C1 register = 1 (transmission enabled)
• The TI bit in the U2C1 register = 0 (data present in the U2TB register)

If an internal clock is selected, set the RE bit in the U2C1 register to 1 after setting the TE bit in the U2C1 register to 1 but before setting dummy data in the U2TB register.
Set the U2RRM bit in the U2C1 register to 1 before reading the last data in continuous receive mode during master operation.

31.14 Notes on Clock Synchronous Serial Interface

31.14.1 Notes on Synchronous Serial Communication Unit

To use the synchronous serial communication unit, set the IICSEL bit in the IICCR register to 0 (SSU function selected).

31.14.2 Notes on I²C bus Interface

To use the I²C bus interface, set the IICSEL bit in the IICCR register to 1 (I²C bus function selected).

(1) Do not use the I²C interface with settings that do not comply with the I²C specification.
(2) Communication using “Hs-MODE” cannot be performed. The maximum transfer rate is [a maximum of 400 kHz] in “FAST-MODE”.
(3) The low-level period of the SCL signal is [a minimum of 1.3 μs] in “FAST-MODE”. Since the high-level/low-level width of the duty cycle for this module is 50%/50%, this value is not reached during operation at 400 kHz. Therefore, the maximum transfer rate is 2.6 μs for the SCL period (maximum transfer frequency is 384.6 kHz).
(4) There must be a delay of [a minimum of 300 ns] for the SDA pin to change at the rising edge of the SCL signal. The SDA digital delay for this module must be at least 3 x f1 cycles, care must be taken when the reference clock f1 is set to 11 MHz or above. Set bits SDADLY1 and SDADLY0 to 01b or more.
(5) There is no compatibility with the CBUS.
(6) 10-bit addressing cannot used.
(7) When a start condition is detected while data is transmitted in slave transmit mode, any address following that condition cannot be received and the operation is stopped. Initialize the module according to the flow for resetting the control block.
(8) Do not set 1111XXXb and 0000XXXb as slave addresses.
(9) When starting communication by the master after a stop condition is detected, always clear the STOP bit in the SISR register to 0.

31.14.3 ICE Bit in SICR1 Register and SIRST Bit in SICR2 Register

While the I²C bus interface is operating, when 0 is written to the ICE bit or 1 is written to the SIRST bit in the SICR2 register, the values of the BBSY bit in the SICR2 register and the STOP bit in the SISR register may be undefined.

31.14.3.1 Conditions when Values of Bits are Undefined

- When this module occupies the I²C bus in master mode of the I²C bus interface.
- While this module transmits data or an acknowledge in slave mode of the I²C bus interface.

31.14.3.2 Countermeasures

- When a start condition (falling of SDA when SCL is high) is input, the BBSY bit is set to 1.
- When a stop condition (rising of SDA when SCL is high) is input, the BBSY bit is set to 0.
- In master transmit mode, while SCL and SDA are both high, when 1 is written to the BBSY bit, 0 is written to the SCP bit, and a start condition (falling of SDA when SCL is high) is output, the BBSY bit is set to 1.
- In master transmit mode or master receive mode, while SDA is low and this module is the only device that pulls SCL low, when 0 is written to the BBSY bit, 0 is written to the SCP bit in the SICR2 register, and a stop condition (rising of SDA when SCL is high) is output, the BBSY bit is set to 1.
- When 1 is written to the MS bit in the SAR register, the BBSY bit is set to 0.

31.14.3.3 Additional Description on SIRST Bit in SICR2 Register

- When 1 is written to the SIRST bit, bits SDAO and SCLO in the SICR2 register are set to 1.
- In master transmit mode or slave transmit mode, when 1 is written to the SIRST bit, the TDRE bit in the SISR register is set to 1.
- While the I^2C bus control block is reset by the SIRST bit, writing to the BBSY bit in the SICR2 register and bits SCP and SDAO is disabled. Thus, write 0 to the SIRST bit before writing to any of these bits.
- The BBSY bit is not set to 0 even if 1 is written to the SIRST bit. However, depending on the states of SCL and SDA, a stop condition (rising of SDA when SCL is high) is generated, which may set the BBSY bit to 0. Similarly, this may also affect other bits.
- While the I^2C bus control block is reset by the SIRST bit, data transmission and reception are stopped. However, the function to detect a start condition, stop condition, and arbitration lost continues operating. Therefore, the values of registers SICR1, SICR2, and SISR may be updated depending on the signal input to pins SCL and SDA.
- Refer to **22.4.8 Procedure for Resetting Control Block in I^2C bus Interface Mode**, for more details including the above information on the control block reset operation using the SIRST bit.

31.15 Notes on Hardware LIN

For the time-out processing of the header and response fields, use another timer to measure the duration of time with a Synch Break detection interrupt as the starting point.

31.16 Notes on A/D Converter

31.16.1 Notes on A/D Conversion

- Do not write to the ADMOD, ADINSEL, ADCON0 (except the ADST bit), ADCON1, or OCVREFCR register during A/D conversion.
- When using the A/D converter in repeat mode 0, repeat mode 1, or repeat sweep mode, the frequency of the CPU clock before starting A/D conversion must be set to be a frequency higher than that of the A/D converter operating clock ϕAD.
  Do not select fHOCO-F as ϕAD.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode during A/D conversion regardless of the state of the CM02 bit in the CM0 register (1: Peripheral function clock stops in wait mode or 0: Peripheral function clock does not stop in wait mode).
- Do not set the FMSTP bit in the FMR0 register to 1 (flash memory stops) or the FMR27 bit to 1 (low-current-consumption read mode enabled) during A/D conversion. Otherwise, the A/D conversion result will be undefined.
- After setting the ADST bit in the ADCON0 register to 0 (A/D conversion stops) by a program during A/D conversion to forcibly end the conversion, allow two or more cycles of the ϕAD clock before writing 1 to the ADST bit to ensure time for end processing.

31.16.2 Clock Source Switching

- Stop A/D conversion before switching the clock source. After switching the clock source, wait for at least two cycles of the fHOCO-F clock to before starting A/D conversion.

[Changing procedure]
(1) Set the ADST bit in the ADCON0 register to 0 (A/D conversion stops).
(2) Change the CKS2 bit in the ADMOD register.
(3) Wait for at least two cycles of the fHOCO-F clock.
(4) Set the ADST bit in the ADCON0 register to 1 (A/D conversion starts).

- To change the clock source from fHOCO-F to another clock and then stop fHOCO-F, after switching the clock source, wait at least two cycles of fHOCO-F before stopping fHOCO-F.

[Changing procedure]
(1) Set the ADST bit in the ADCON0 register to 0 (A/D conversion stops).
(2) Change the CKS2 bit in the ADMOD register.
(3) Wait for at least two cycles of the fHOCO-F clock.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

Notes:
1. Do not set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off) while fHOCO-F is selected as the clock source.
2. Do not change the division ratio of the high-speed on-chip oscillator set by the FRA2 register while fHOCO-F is selected as the count source.

31.16.3 Pin Handling

Connect a 0.1 μF capacitor between pins VREF and AVSS.

31.17 Notes on Flash Memory

31.17.1 CPU Rewrite Mode

31.17.1.1 Prohibited Instructions

The following instructions cannot be used while the program ROM area is being rewritten in EW0 mode because they reference data in the flash memory: UND, INTO, and BRK.

31.17.1.2 Interrupts

Tables 31.2 to 31.4 show CPU Rewrite Mode Interrupts.

Table 31.2 CPU Rewrite Mode Interrupts (1)

Mode	Erase/ Write Target	Status	Maskable Interrupt
EW0	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
		During auto-programming	
	Program ROM	During auto-erasure (suspend enabled)	Usable by allocating a vector in RAM.
		During auto-erasure (suspend disabled)	
		During auto-programming	
EW1	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1, the FMR21 bit is automatically set to 1. The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit to 0.
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
		During auto-programming	
	Program ROM	During auto-erasure (suspend enabled)	Auto-erasure suspends after td(SR-SUS) and interrupt handling is executed. Auto-erasure can be restarted by setting the FMR21 bit to 0 after interrupt handling completes. While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written.
		During auto-erasure (suspend disabled or FMR22 = 0)	Auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.
		During auto-programming	

FMR21, FMR22: Bits in FMR2 register

Table 31.3 CPU Rewrite Mode Interrupts (2)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 2 • Voltage Monitor 1	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step • Address Match • Address Break (Note 1)
EW0	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit is set to 0 (erase restart).	When an interrupt request is acknowledged, interrupt handling is executed. If erase-suspend is required, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit in the FMR2 register is set to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled)		
		During auto-programming		

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

Table 31.4 CPU Rewrite Mode Interrupts (3)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 2 • Voltage Monitor 1	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step • Address Match • Address Break (Note 1)
EW1	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit is set to 0 (erase restart).	When an interrupt request is acknowledged, interrupt handling is executed. If erase-suspend is required, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit in the FMR2 register is set to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled or FMR22 = 0)		
		During auto-programming		

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

31.17.1.3 How to Access

To set one of the following bits to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
• The FMR01 bit or FMR02 bit in the FMR0 register
• The FMR13 bit in the FMR1 register
• The FMR20 bit, FMR22 bit, FMR24 bit, or FMR 27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Disable interrupts and DTC activation between writing 1 and writing 0.
• The FMR14 bit, FMR15 bit, FMR16 bit, or FMR17 bit in the FMR1 register

31.17.1.4 Rewriting User ROM Area

In EW0 mode, if the supply voltage drops while rewriting any block in which a rewrite control program is stored, it may not be possible to rewrite the flash memory because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

31.17.1.5 Programming

Do not write additions to the already programmed address.

31.17.1.6 Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.
If the FST7 bit in the FST register is set to 0 (busy during programming or erasure execution), do not enter to stop mode or wait mode.
Do not enter stop mode or wait mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

31.17.1.7 Programming and Erasure Voltage for Flash Memory

To perform programming and erasure, use VCC = 2.7 to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 2.7 V.

31.17.1.8 Low-Current-Consumption Read Mode

In low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).
Low-current-consumption read mode can be used when the CPU clock is set to either of the following:
• The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.

When divided by 1 (no division) or divided by 2 is set, do not use low-current-consumption read mode.
After setting the divide ratio of the CPU clock, set the FMR27 bit to 1 (low-current-consumption read mode enabled).
To reduce the power consumption, refer to **10. Power Control**.
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

31.18 Note on Peripheral Mapping Controller

31.18.1 Setting Pin Assignment Select Register (PMCSEL)

The PMCSEL register is used to select the assignment of pins, so set this register before controlling input/output.

31.18.2 Restrictions on Using Full-Spec Emulator (E100)

In the actual MCU of the R8C/5x Group and the full-spec emulator (E100), the set value of the pin assignment select bits differs when selecting 48-pin products.

	Full-spec emulator (E100)	Actual MCU of R8C/5x Group
Standard pin assignment for 48-pin product:	PMCSEL = 000b	PMCSEL = 011b
Communication function priority pin assignment for 48-pin product:	PMCSEL = 001b	PMCSEL = 100b

32. Notes on On-Chip Debugger

When using the on-chip debugger to develop and debug programs for the R8C/54E Group, R8C/54F Group, R8C/54G Group, R8C/54H Group, take note of the following.

(1) Some of the user flash memory and RAM areas are used by the on-chip debugger. These areas cannot be accessed by the user.
Refer to the on-chip debugger manual for which areas are used.
(2) Do not set the address match interrupt (registers AIENi, AIADRij (i = 0 or 1, j = L or H), and fixed vector table) in a user system.
(3) Do not use the BRK instruction in a user system.

There are some special restrictions regarding connection and use of the on-chip debugger. Refer to the on-chip debugger manual for details.

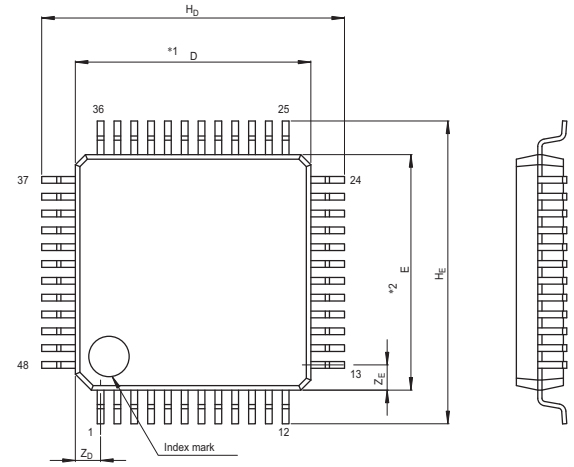
33. Notes on Emulator Debugger

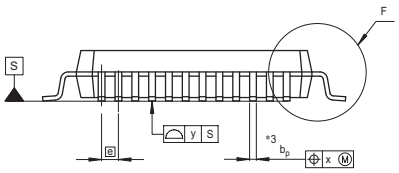
There are some special restrictions regarding connection and use of the emulator debugger. Refer to the emulator debugger manual for details.

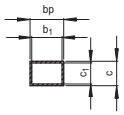
Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

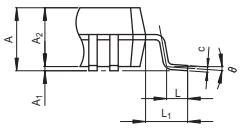
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g







Terminal cross section



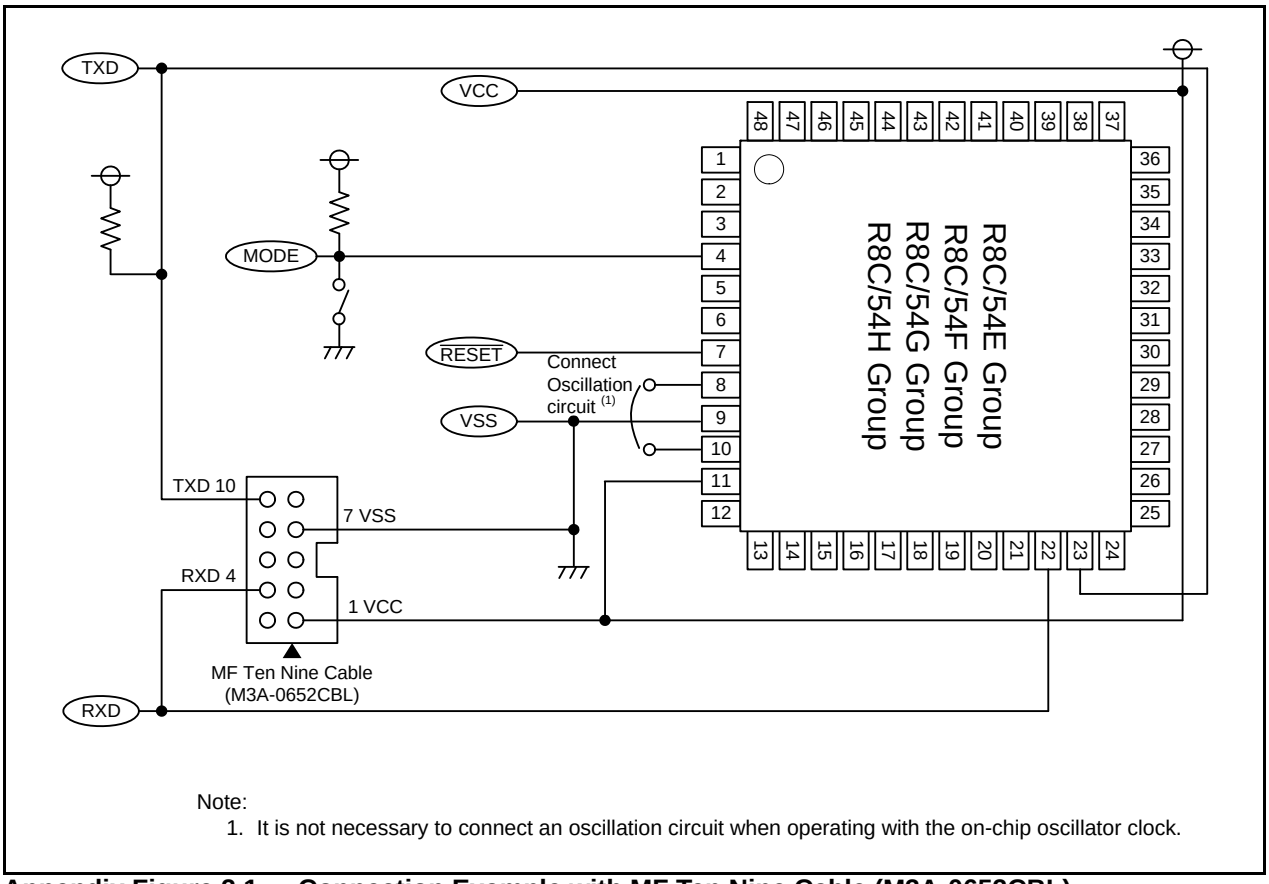
Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

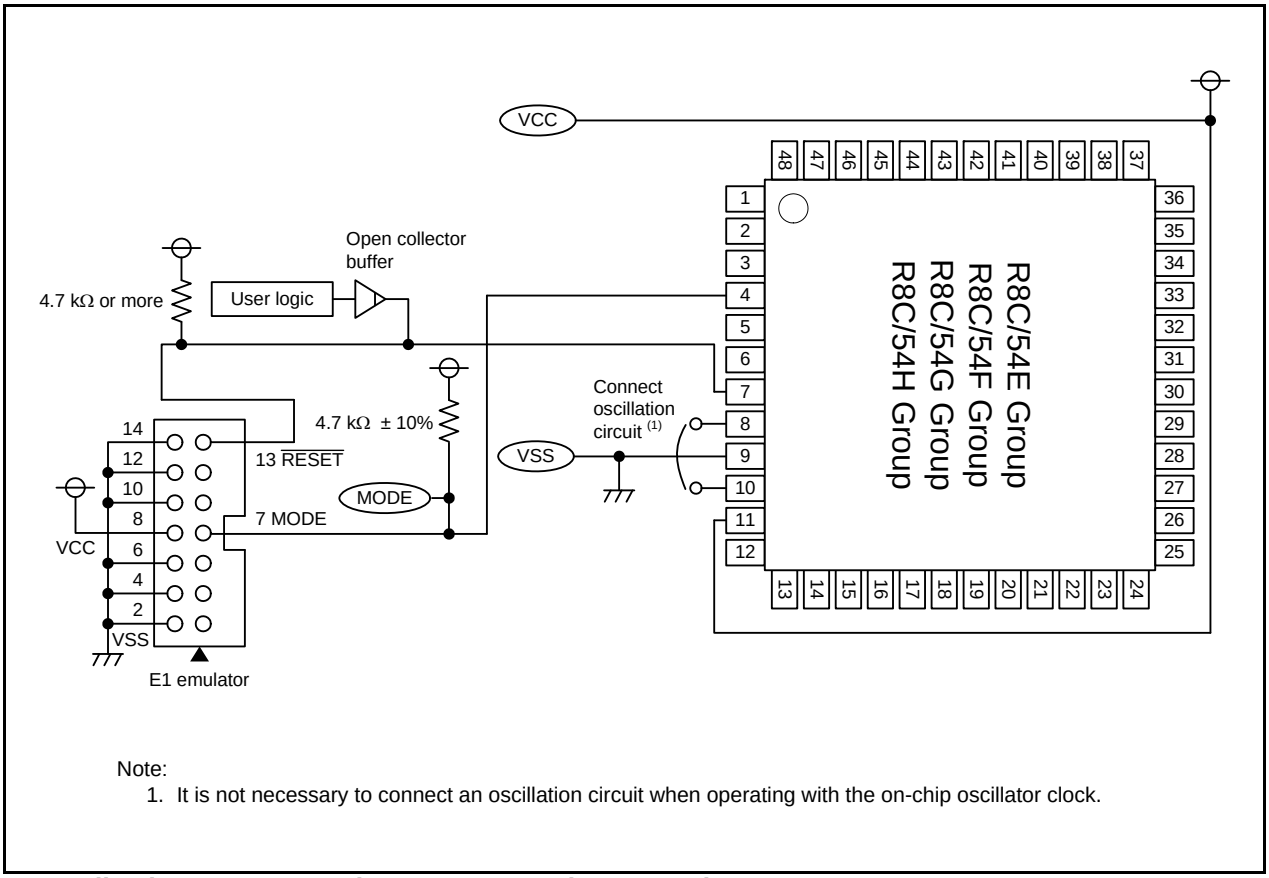
Appendix 2. Connection Examples between Serial Programmer and On-Chip Debugging Emulator

Appendix Figure 2.1 shows the Connection Example with MF Ten Nine Cable (M3A-0652CBL) and Appendix Figure 2.2 shows the Emulator E1 Connection Example.



Note:
1. It is not necessary to connect an oscillation circuit when operating with the on-chip oscillator clock.

Appendix Figure 2.1 Connection Example with MF Ten Nine Cable (M3A-0652CBL)

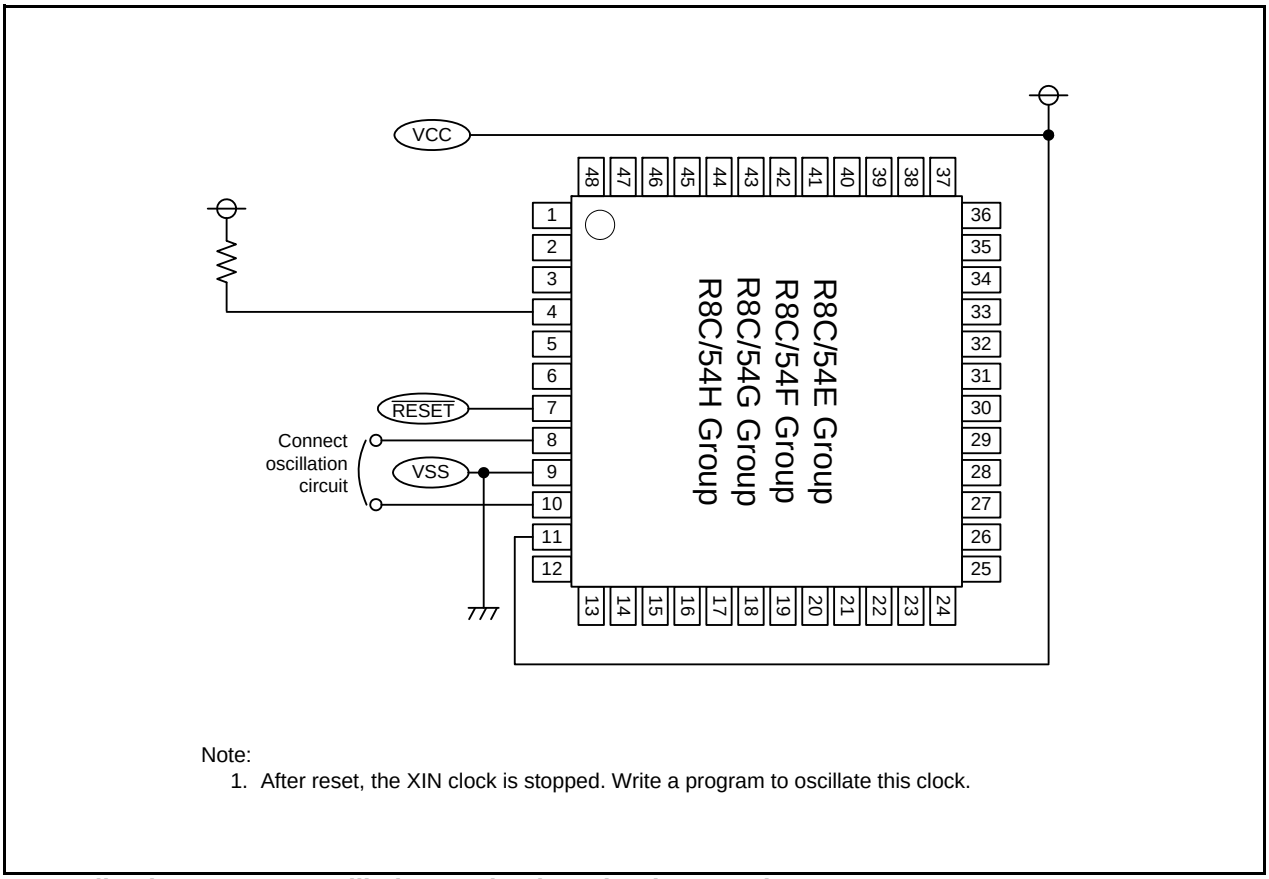


Note:
1. It is not necessary to connect an oscillation circuit when operating with the on-chip oscillator clock.

Appendix Figure 2.2 Emulator E1 Connection Example

Appendix 3. Oscillation Evaluation Circuit Example

Appendix Figure 3.1 shows the Oscillation Evaluation Circuit Example.



Note:
1. After reset, the XIN clock is stopped. Write a program to oscillate this clock.

Appendix Figure 3.1 Oscillation Evaluation Circuit Example

Index

REVISION HISTORY	R8C/54E Group, R8C/54F Group, R8C/54G Group, R8C/54H Group User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
0.10	Mar 02, 2011	—	First Edition issued
0.20	Jun 24, 2011	All	R8C/54F Group, R8C/54G Group, R8C/54H Group added
			Register symbol name changed: "Pi" → "PORTi"
			Terms changed: "SRAM" → "RAM", "Flash memory ready" → "Flash memory"
			Register name changed: "Timer RB2_0 interrupt request and status register" → "Timer RB2_0 interrupt request register"
		14	Figure 1.5 Note 1 added
		15	Figure 1.6 Notes 1 and 2 added
		17	Table 1.14 Note 1 added
		22	Table 1.19 Note 1 added
		42	Table 3.13 changed
		55	5.2.2 Note 1 added
		57, 67, 97	5.2.4, 6.2.3, 8.2.6 changed
		88	Table 7.3 changed
		90	Table 7.4 changed
		92 to 101	8. Watchdog Timer Term changed: "Low-speed on-chip oscillator clock" → "Watchdog timer low-speed on-chip oscillator clock (Low-speed on-chip oscillator clock for the watchdog timer)"
		93	Figure 8.1 changed
		95	8.2.1 Note 1 changed
		102	Table 9.1 Note 2 changed
		103	Figure 9.1 changed
		105	Table 9.3 changed
		106, 128	9.2.1 and 10.2.1 changed
		108	9.2.3 Note 5 added
		110, 131	9.2.4 and 10.2.3 CM30 Bit (Wait control bit) description changed, 9.2.5 and 10.2.4 changed
		111, 132	9.2.7 and 10.2.5 changed
		112	9.2.8 Descriptions changed
		113	9.2.9 changed
		115, 234	9.2.11 and 14.5.16 changed
		116	Figure 9.3 changed
		118	Figure 9.4 changed
		119	Figure 9.5 Term descriptions and notes changed, Table 9.6 changed
		121	9.6.10 Title changed
		123	Table 9.8 changed
		126	Figure 10.1 changed
		135	10.3 Descriptions changed, Table 10.2 changed, Note 1 deleted
		136	10.3.1, 10.3.2, and 10.3.3 Descriptions changed, 10.3.4 added
		137	10.4 and 10.4.2 Descriptions changed
		138 to 140	10.4.4 Descriptions changed, Table 10.3 changed

REVISION HISTORY	R8C/54E Group, R8C/54F Group, R8C/54G Group, R8C/54H Group User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
0.20	Jun 24, 2011	142	10.5.3 Descriptions changed
		143	10.6.3 "Stopping PLL: PLC07 bit in PLC0 register" added, 10.6.6 Descriptions changed
		144	10.6.8 and 10.6.9 Descriptions changed
		153	11.2.1 changed
		162	Table 11.5 "SSUIC_1" → "Synchronous serial communication unit/I^2C bus interface"
		164	11.4.4 Note 1 changed
		169	Figure 11.8 changed
		172	Figure 11.11 changed
		174, 175	11.8 "Synchronous serial communication unit" → "Synchronous serial communication unit/I2C bus interface"
		183	12.3 Descriptions changed
		184	Table 12.4 added
		192	13.2.3 changed
		199	Figure 13. 7 Figure Title changed
		202, 203	13.3.6 and 13.3.8 Descriptions changed
		206	13.4.5 added
		207	14.1 Descriptions changed, Table 14. 1 Note 7 added
		213	Figure 14.5 changed
		217	14.4.2 Descriptions changed
		218	Table 14.4 Note 1 added
		221	14.5.3 changed
		235	14.5.17 changed
		236	14.5.19 changed
		237	14.5.20 changed
		240, 241	14.5.24 and 14.5.25 changed
		243	14.5.27 changed:
		247	14.5.31 (3) CAN I/O pins added
		251	15.3.1 Title changed
		253	15.3.3 changed, Table 15.4 changed
		256	15.3.5 Descriptions added
		257	Figure 15.2 changed
		259	15.4.3 Descriptions changed, Figure 15.4 changed
		262	Figure 15.7 changed
		263	15.4.7 Descriptions changed
		264, 265	15.5 (2), (3), (5), (9), and (10) changed, (15) added
		267	Figure 16.1 changed
		268	16.2 Descriptions changed
		270	16.3.1 Note 2 changed, TSTART Bit (Timer RB2 count start bit) description added
		271	16.3.2 changed
		278	16.4.1 Note 1 changed, Figure 16.2 changed

Rev.	Date	Description	
		Page	Summary
0.20	Jun 24, 2011	279	Figure 16.3 added
		280	16.4.2 Descriptions changed
		281, 282	Figures 16.4 and 16.5 changed
		283	16.4.3 Descriptions changed
		284, 285	Figures 16.6 and 16.7 changed
		286	16.4.4 Descriptions changed
		287, 288	Figures 16.8 and 16.9 changed
		296	Table 16.8 "Undefined value" → "High impedance"
		300, 302	Tables 17.1 and 17.3 changed
		303	17.2.1 Descriptions changed
		305	17.2.3 Note 3 added
		306	17.2.4 Bit descriptions changed
		308	Table 17.5 changed
		309, 310	17.2.7 and 17.2.8 Note 2 added
		312	17.2.10 Descriptions changed
		315	17.2.13 Descriptions added
		316	17.2.14 changed
		322	17.3.2 Descriptions changed
		324	Figure 17.10 changed
		326	Table 17.12 Note 1 deleted
		346	17.6.8 and 17.6.9 Descriptions changed, 17.6.10 added
		361, 362	18.2.11.3 and 18.2.11.5 "TRDi " → "TRD0"
		412, 416	18.4.5 and 18.4.6 • Notes on Starting Count added
		416	18.4.8 added
		421, 422	19.2.4 and 19.2.5 changed
		424	19.2.7 "TRESEC" → "TREMIN"
		428	19.5 Bit names changed: "RTCF/OVIF bit" → "OVIF bit", "ALIF/CMIF bit" → "CMIF bit"
		434	20.2.4 DFE Bit (RXD digital filter enable bit) description added
		435	20.2.5 Notes 1 and 2 changed
		436	20.2.6 Note 1 changed
		437	20.2.7 changed
		438	Table 20.4 Note 2 changed
		443	Table 20.6 Note 1 changed, Note 2 added
		445, 446	Figures 20.6 and 20.7 changed
		449	Table 20.9 changed
		457	21.2.2 Descriptions changed
		460	21.2.5 changed
		461	21.2.6 Descriptions changed
		462	21.2.7 Note 1 deleted, DF2EN Bit (RXD2 digital filter enable bit) description added
		463	21.2.8 changed

Rev.	Date	Description	
		Page	Summary
0.20	Jun 24, 2011	485	Table 21.11 Note 1 changed
		518, 545	Figures 22.10 and 22.29 changed
		574	Table 24.2 changed
		575	Figure 24.1 "CCKLS" → "CCLKS"
		595	24.2.8 Bit names changed: "Transmit status flag (transmitter)" → "Transmit status flag", "Receive status flag (receiver)" → "Receive status flag"
		599	24.2.10 changed
		600	24.2.11 Note 1 changed
		603	24.2.13 changed
		610	24.2.19 Note 2 changed
		611, 615	24.2.20 and Figure 24.5 "8/3 encoder" → "8 to 3 priority encoder"
		618	24.2.26 Note 1 changed
		622	24.3.1 • CCLKR register added
		623, 624	24.3.2 and 24.3.3 Descriptions changed
		626	24.4.1 Descriptions changed, Figure 24.14 changed
		627	Table 24.12 changed
		629	24.6 Descriptions changed
		704 to 707, 766 to 769	27.8 and 30.16 Notes on Flash Memory added
		719, 720	Tables 29.9 and 29.10 changed
		721	Table 29.13 Note 1 deleted
		729	Table 29.22 changed
1.00	Jan 20, 2012	All pages	"PRELIMINARY" and "Under development" deleted Register symbol name changed: "TRDELC_0" → "TRDELCCR_0"
		2, 4, 6, 8	Tables 1.1, 1.3, 1.5, and 1.7 Minimum instruction execution time changed
		3, 5, 7, 9	Tables 1.2, 1.4, 1.6, and 1.8 "Read voltage", "Operating frequency/Power supply voltage", and "Current consumption" changed
		21	Table 1.18 Power supply input changed
		30	Table 3.1 After Reset of Voltage Monitor 0 Circuit Control Register changed
		34, 269	Tables 3.5 and 16.3 Symbol "TRBPRSC_0" added
		52	Table 3.23 changed, Note 2 added
		56	5.2.2 Note 1 changed
		57	5.2.3 PRC0 Bit description changed
		59, 69, 86, 100, 682	5.2.5, 6.2.4, 7.2.8, 8.2.7, and 27.3.5 b4 and b5 function changed
		63	Table 5.4 "PLCF" deleted
		74	Figure 6.6 Note 2 changed
		76	Figure 6.8 changed
		77	7.1 Description changed, Table 7.1 changed
		78	Figure 7.1 changed
		80	Table 7.2 changed
		82	7.2.4 changed

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		Page	Summary
1.00	Jan 20, 2012	83	7.2.5 After Reset changed
		85	7.2.7 Bit name of b3 "(4)" → "(5)", Note 4 changed
		94	Figure 8.1 changed
		97	8.2.4 changed, Table 8.3 added
		105	Figure 9.1 changed
		108, 130	9.2.1 and 10.2.1 Note 5 changed
		109, 131	9.2.2 and 10.2.2 Note 1 changed
		112, 133	9.2.5 and 10.2.4 Note 1 added
		113	9.2.6 Note 1 added
		113, 134	9.2.7 and 10.2.5 Note 1 changed
		115	9.2.9 Note 2 changed
		120	Figure 9.4 changed
		123	9.6.8 to 9.6.10 changed
		127, 745	9.8.2 and 31.2.2 changed
		128	Figure 10.1 changed
		145	10.6.6 changed
		162	Table 11.3 "0FFE7h" → "0FFE6h"
		172	11.5.1 Description changed
		177	11.8 Description changed
		179, 748	Figures 11.13 and 31.1 Note 3 added
		181	12.1 Description changed
		187	Table 13.1 Unit of transfers changed
		206	Table 13.13 changed, 13.3.9 Description changed
		207	13.3.10.1 and 13.3.10.2 changed
		208, 750	13.4.2 and 31.5.2 changed
		209	14. Note added, Table 14.1 Note 8 changed
		219	14.4.2 and 14.4.3 deleted → Moved to chapter 31
		220	Table 14.4 "Pin Assignment Select Register" deleted → Moved to chapter 31
		235	14.5.17 "Pin Assignment Select Register" deleted → Moved to chapter 31
		252	15.3.2 Note 3 changed
		253	15.3.3 Note 2 and 3 added, Table 15.4 and 15.5 changed
		254	Table 15.6 changed
		255	15.3.4 b4 to b6 function changed, Note 1, 2, and 4 changed, Descriptions changed
		260	Figure 15.5 changed, Figure15.6 added
		263	Table 15.7 and 15.8 Note 1 added
		264, 751	15.5 and 31.6 (1) Note 1 changed
		267	Figure 16.1 Note 3 added
		269	Table 16.3 Note 1 changed
		270	16.3.1 b1 and b2 changed, TSTART Bit description changed
		274	16.3.5 Descriptions changed
		277	Table 16.5 changed

Rev.	Date	Description	
		Page	Summary
1.00	Jan 20, 2012	278, 284, 285	Figures 16.2, 16.6, and 16.7 changed "registers TRBPR, TRBSC, and TRBPRE" → "registers TRBPR and TRBPRE"
		279	Figure 16.3 changed "registers TRBPR, TRBSC, and TRBPRE" → "registers TRBPR and TRBPRE", "TRBPRE register = 02h, TRBPR register = 01h" → "TRBPRSC register = 0102h"
		280	16.4.2 Descriptions changed, Note 1 changed
		282, 285, 288	Figures 16.5, 16.7, and 16.9 changed "TRBPRE register = 01h, TRBPR register = 01h" → "TRBPRSC register = 0101h"
		283	16.4.3 changed
		286	16.4.4 changed
		287, 288	Figures 16.8 and 16.9 "TRBSC register = 03h" added
		290	Tables 16.6 and 16.7 changed
		291	16.5.2 changed
		293	Figure 16.12 changed
		294	Figures 16.13 "Write 01h to TRBPRE register and 25h to TRBPR register" → "Write 2501h to TRBPRSC register"
		295	Figure 16.14 changed and "Write 01h to TRBPRE register and 25h to TRBPR register" → "Write 2501h to TRBPRSC register"
		296	16.5.3 Descriptions changed, Table 16.8 and 16.5.4 changed
		297	16.6 Descriptions changed
		298, 753	16.8 and 31.7 (2) and (3) changed
		300	Table 17.1 Others changed
		302	Figure 17.1 changed
		306	17.2.4 Note 2 changed
		307	17.2.5 changed
		309, 310	17.2.7 and 17.2.8 Descriptions changed
		313	17.2.11 changed
		315	17.2.13 changed
		318 to 320	17.3.1 Description changed
		321	Figure 17.8 changed
		322	17.3.2 Description changed
		326, 328	17.3.3 Description changed
		327	Figure 17.13 changed
		334	Figure 17.20 changed
		337	17.4.4 Description changed
		346	17.6.5 changed
		346, 756	17.6.8 and 31.8.8 Description changed
		348	Figure 18.1 changed
		350	18.2.1 changed
		352	18.2.3 Notes 1 and 3 changed
		359	18.2.10.1 Note 1 changed
		370	18.2.17.2 Setting Range "0001h to FFFFh" → "0000h to FFFFh"
		383	Figure 18.6 changed

Rev.	Date	Description	
		Page	Summary
1.00	Jan 20, 2012	384	18.3.1.5 ELC Event Input added, 18.3.1.7 Setting External Pins added
		411, 412, 758, 759	18.4.3 and 31.9.3 changed
		416, 763	18.4.7 and 32.9.7 deleted
		417	19.1 description and Figure 19.1 changed
		420	19.2.3 Notes 1, 3, and 4 added
		421	19.2.4 Notes 1 and 2 added
		424	19.2.7 Note 1 added
		429	Table 20.1 changed, Note 1 added
		432	20.2.1 Note 1 added
		433	20.2.3 Description changed
		434	20.2.4 Note 2 deleted, DFE Bit description changed
		436	20.2.6 Note 2 added
		438	Table 20.4 Note 2 changed
		440	Figure 20.3 changed
		443	Table 20.6 Note 1 changed
		444	Table 20.7 changed
		445, 446	Figure 20.6 and 20.7 changed
		448	20.3.2.3 Description changed, Figure 20.8 changed
		450, 765	20.5.1.1 and 31.11.1.1 Description changed, 20.5.1.2 and 31.11.1.2 added
		452	Table 21.1 Note 2 changed
		453	Table 21.2 Note 1 changed
		461	21.2.6 Note 2 deleted, Note 5 added
		462	21.2.7 DF2EN Bit description changed
		477	21.3.2.7 Description changed
		500	22.2.6.1 changed
		619, 620	Figures 24.9 to 24.11 Note 1 changed
		622	24.3.1 changed
		626	24.4.1 Description changed
		636	Table 25.1 changed, Note 2 and 3 changed
		641	25.2.2 b15 function changed
		644	25.2.5 ADST Bit description changed
		646	Figure 25.3 and 25.4 changed
		647	Table 25.5 changed
		649	25.3.3.4 changed, 25.3.3.5 deleted
		651	Figure 25.6 changed
		660	25.9 changed, Figure 25.11 changed
		661, 771	25.10.1 and 31.15.1 changed
		662	Figure 26.1 changed
		667, 668	26.4 Description changed, Figures 26.5 and 26.6 added
		669	Table 27.1 changed, Note 4 added
		671	Figure 27.1 Note 1 added

Rev.	Date	Description	
		Page	Summary
1.00	Jan 20, 2012	675	27.3.2 b0 changed, Note 5 added
		676	27.3.2 CMDRST Bit description changed
		681	27.3.4 FMR27 Bit description changed
		684	Table 27.4 changed
		690	27.5.7 Description changed
		708, 775	27.8.1.9 and 31.16.1.9 changed
		711	28.2.2 changed
		714 to 717	29. Peripheral Mapping Controller added 14.4.2 → Moved to 29.1, 29.1.1 added 14.4.3, Tables 14.4 and 14.5 → Moved to 29.2, Tables 29.1 and 29.2 14.5.17 → Moved to 29.3.1
		718, 776	29.4 and 31.17 "Note on Peripheral Mapping Controller"added
		719	Table 30.1 changed
		720	Table 30.2 changed
		721	Table 30.4 Title "Vcc = 1.8 V to 5.5 V..." → "Vcc = 2.7 V to 5.5 V..."
		722	Table 30.5 changed
		723	Table 30.7 changed
		724	Table 30.8 Note 6 deleted
		725, 726	Table 30.9 and 30.10 changed
		727	Table 30.13 changed
		729	Table 30.16 changed
		730	Table 30.17 changed, Note 4 added
		731	Tables 30.18 added
		732	Table 30.19 changed
		733	Table 30.20 changed, Note 4 added
		734	Tables 30.21 added
		735, 736, 740	Table 30.22 to 30.24 Title "Vcc = 1.8 V to 5.5 V..." → "Vcc = 2.7 V to 5.5 V..."
		735, 736	Tables 30.22 and 30.23 changed
		741	Tables 30.25 and 30.26 changed
		742	Table 30.27 changed, Note 1 added, Table 30.28 changed
		743	Table 30.29 changed
		780	Appendix Figure 2.1 changed, Title changed
2.00	Aug 20, 2012	2, 4, 6, 8	Tables 1.1, 1.3, 1.5, and 1.7 changed
		56	5.2.2 Note 1 changed
		57	5.2.3 PRC1 Bit Description changed
		63	Table 5.4 "PRC1" changed
		77, 749	"6.5 Notes on Resets" and "31.2 Notes on Resets" added
		105	Table 9.1 "State after reset" changed
		106	Figure 9.1 changed
		111	9.2.3 Notes 3 and 4 changed
		116	9.2.9 Note 1 changed
		128, 750	9.8.1 and 31.3.1 Description changed

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		Page	Summary
2.00	Aug 20, 2012	150	10.6.11 Description and Figure 10.7 Note 2 changed
		181, 754	11.9.5 and 31.5.5 Example 1 to 3 "AND.B" → "MOV.B"
		186	12.3 Description changed
		199	Table 13.8 changed
		209, 755	13.4.1 and 31.6.1 Description changed
		223	14.5.3 Description changed, Note 1 added
		250	15. Description and Table 15.1 changed
		251	Figure 15.1 and Table 15.2 changed, Note 1 added
		252	15.3.1 Description changed
		253	15.3.2 Note 3 changed
		254	15.3.3 Note 1 changed
		255	15.3.3 TOPCR Bit Description changed
		256	15.3.4 Note 1 deleted, Note 3 and Description changed
		258	15.4.1 Description and Figure 15.2 changed
		260	15.4.3 Description and Figure 15.4 changed
		261	15.4.4 Description and Figure 15.6 changed
		263	15.4.6 Description changed
		265, 266, 756	15.5 and 31.7 (2) to (14) changed
		268	Figure 16.1 Note 3 changed
		270	Table 16.3 Note 1 changed
		271	16.3.1 Note 1 and TSTART Bit Description changed, Note 1 added
		272	16.3.2 Description added, TOSSTF Bit Description changed
		273	Table 16.4 "Timer mode" changed
		275	16.3.5 Description changed
		276	16.3.6 "Function" and Description changed, Note 1 added
		277	16.3.7 "Function" changed
		279	16.4.1 Note 1 and Figure 16.2 changed
		280	Figure 16.3 changed
		281	16.4.2 Description and Note 1 changed
		282, 283	Figures 16.4 and 16.5 changed
		284	16.4.3 Description and Note 1 changed
		285, 286	Figures 16.6 and 16.7 changed
		287	16.4.4 Description changed
		288, 289	Figures 16.8 and 16.9 changed
		290	16.5.1 Description changed
		291	16.5.2 Description changed
		293 to 296	Figures 16.11 to 16.14 changed
		297	Table 16.8 and 16.5.3 Description changed
		298	16.6 and 16.7 Description changed
		299, 300, 758, 759	16.8 and 31.8 (2), (3), (6) to (8), (12) to (16) changed

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		Page	Summary
2.00	Aug 20, 2012	301	Table 17.1 "Operating clock" added
		303	Figure 17.1 changed
		304	17.2.1 "Function" and Description changed
		305, 306	17.2.2 changed, Tables 17.5 to 17.8 added
		307, 308	17.2.3 Note 1 changed, Note 2 deleted, CTS Bit Description changed
		309	17.2.4 b0 to b3, b7, Notes 1 and 2 changed, Notes 4 and 5 added, TOA, TOB, TOC, and TOD Bits Description changed
		311	17.2.6 Note 1 added, Table 17.9 Notes 1and 2 changed
		312, 313	17.2.7, 17.2.8 b0, b1, b4, b5, and Note 1 changed
		314	17.2.9 b5 Description changed, Notes 1 to 3 added, CSTP Bit Description changed
		315	17.2.10 b0 to b4, b6, b7 changed, Notes 1 and 2 added, Bit Description deleted
		316	17.2.11 b0 to b3 changed, Note 1 added
		318	17.2.13 b2, b3, b5, and Note 1 changed, Notes 2 and 3 deleted, RESTATS, OPE Bit Description added
		319	17.2.14 ELCP2TE Bit Description changed
		320	Table 17.10 changed
		321	Title "17.3.1.1 Free-Running Operation" added, Description changed, Title "17.3.1.2 Period Count Operation" added, Description changed
		322	Title "17.3.1.3 Output Compare Function" added
		323	Title "17.3.1.4 Input Capture Function" added
		324	17.3.1.4 Description changed
		325	17.3.2 Description changed
		327	Figure 17.10 changed
		329	17.3.3 Description and Table 17.16 changed
		331, 332	17.3.3 Description, Figures 17.14 and 17.15 changed
		333 to 335	17.3.3 Description, Figures 17.16 and 17.18 changed
		336	17.4.1 Description, Figure 17.19 changed
		337	17.4.2 Description, Figure 17.19 and Title changed
		338	17.4.3 Description changed
		340	17.4.4 Description changed
		343	Figure 17.27 changed
		345	Figure 17.31 changed
		347	17.5.8 and Figure 17.34 changed
		348	"17.6 Timer RC Interrupt" added
		349 to 351, 760 to 762	17.7.4 to 17.7.6 and 31.9.4 to 31.9.6 Description changed
		353	Figure 18.1 Notes 1 and 2 changed
		368	18.2.12.1 Note 3 deleted
		369	18.2.12.2 Note 2 deleted
		389	18.3.1.5 Description changed
		424	19.2.1 Title changed, 19.2.2 Title changed and Note 1 added
		425	19.2.3 Title and CCLR Bit Description changed

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2.00	Aug 20, 2012	426 to 429	19.2.4 to 19.2.7 Titles changed
		431	Figure 19.3 and Title changed
		432	19.4 Description changed
		433, 770	19.5 and 31.11 Description changed
		434	20.1 Description changed
		437	20.2.1 Note 3 added
		438	20.2.3 b0 to b8 changed
		441	20.2.6 b0 to b8, and Note 1 changed, Note 3 added
		454	20.4 Description changed
		462	21.2.1 Note 1 changed, Note 8 added
		465	21.2.5 Note 3 changed
		466	21.2.6 b0 to b7, Notes 4, and 5 changed
		480	Figure 21.10 changed
		486	Table 21.10 Note 1 changed
		494	Table 22.2 Note 1 added
		506	22.2.6.2 Note 6 changed
		510	22.2.8.2 b5 changed
		512	22.2.9.2 Note 7 added
		548	Figure 22.26 changed
		556	Figure 22.36 "SCL" → "VIH"
		655	25.3.4 Description changed
		677	27.3.1 RDYSTI Bit Description changed
		679	27.3.1 FST5 and FST7 Bit Description changed
		680	27.3.2 Note 6 and FMR00 Bit Description changed
		681	27.3.2 CMDERIE Bit Description changed
		685	27.3.4 Note 3 changed
		691	Figure 27.4 Note 2 changed
		692	Table 27.5 Note 3 changed
		695	Table 27.6, 27.5.7.1 Description changed
		702	"27.5.7.7 Block Blank Check Command" deleted
		703	Table 27.7 changed
		712, 781	27.8.1.3 and 31.17.1.3 Description changed, 27.8.1.8 and 31.17.1.8 deleted, 27.8.1.8 and 31.17.1.8 Description changed
		718	29.1 Description changed
		721	29.3.1 Description and b0 to b2 changed
		722, 782	29.4.2 and 31.18.2 Description changed
		731	Table 30.13 changed
		733, 736	Tables 30.16 and 30.19 "VRAM" changed
		734, 735	Tables 30.17 and 30.18 changed
		737, 738	Tables 30.20 and 30.21 changed
		739, 740, 744,	Tables 30.22 to 30.24 Note 1 changed

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		Page	Summary
2.10	2014.09.26	72	Figures 6.3 and 6.4 "1.8 V" → "2.7 V"
		82	7.2.2 Notes 1 and 2 deleted
		85	7.2.6 Note 6 deleted
		86	7.2.7 Note 6 deleted
		90	Table 7.3 changed
		91	Figure 7.6 "1.8 V" → "2.7 V"
		92	Table 7.4 changed
		93	Figure 7.7 "1.8 V" → "2.7 V"
		127	Figure 9.7 changed
		132	10.2.2 Note 1 changed
		144	10.5.2 Description changed
		164	Table 11.4 "00007Bh" → "0000Bh"
		178, 180, 754	11.8 Description changed, Figure 11.13 and Figure 31.1 "bus clock" → "CPU clock"
		212 to 215, 218	Figures 14.1 to 14.4, and Figure 14.7 "Pin select register" → "Pin function selection"
		223	14.5.3 changed
		260	Figure 15.4 "1234h" → "0004h"
		265, 756	15.5 and 31.7 Description changed
		305	17.2.2 changed
		351, 762	17.7.7 and 31.9.7 deleted
		487	21.3.4.1 and Figure 21.15 "MPBT" → "MPTB"
		613	24.2.16 BLIF Bit Description changed
		626	Figure 24.12 changed
		628	Table 24.11 changed
		642	Figure 25.1 "100b, 101b, 110b, 111b" → "000b, 001b, 010b, 011b"
		650	25.2.6 Note 8 added
		661	Table 25.9 changed
		670, 671	Figures 26.2 and 26.4 "Set to 0 by a program" → "Set to 0 when interrupt request is acknowledged, or set by program."
		677 to 679, 705	27.3.1 and Figure 27.16 "blank check error" deleted
		698	27.5.7.4 Description changed
		698, 699, 700	Figures 27.10, 27.11, and 27.12 Titles changed
		701	27.5.7.4 Description and Figure 27.13 added
		723, 783	29.4.1, 31.18.1 Description changed

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