User's Manual

16

R8C/12 Group

Hardware Manual

RENESAS 16-BIT SINGLE-CHIP MICROCOMPUTER
M16C FAMILY / R8C /Tiny SERIES

All information contained in these materials, including products and product specifications, represents information on the product at the time of publication and is subject to change by Renesas Electronics Corp. without notice. Please review the latest information published by Renesas Electronics Corp. through various means, including the Renesas Electronics Corp. website (http://www.renesas.com).

Renesas Electronics
www.renesas.com

Rev.1.20 2006.01

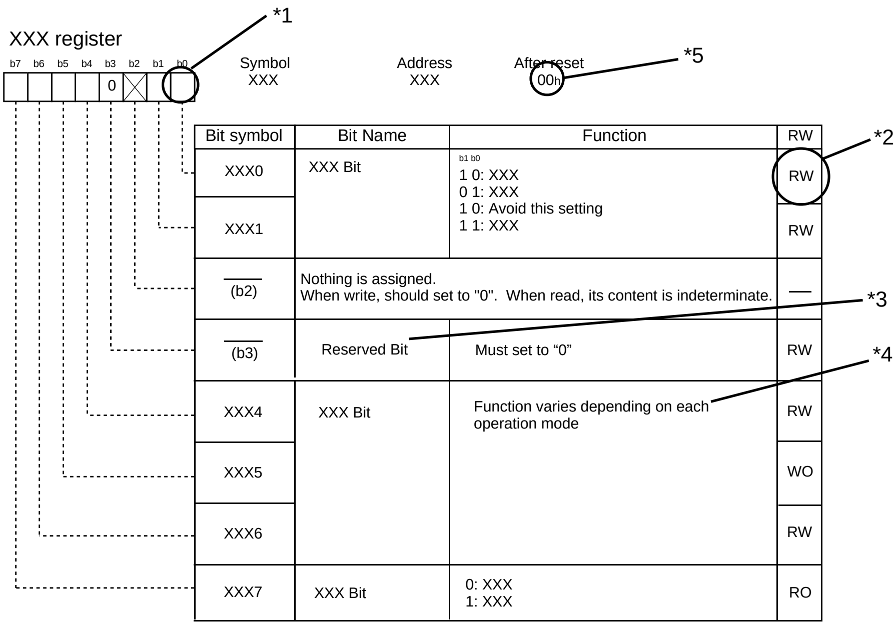
How to Use This Manual

1. Introduction

This hardware manual provides detailed information on the R8C/12 Group of microcomputers.
Users are expected to have basic knowledge of electric circuits, logical circuits and microcomputers.

2. Register Diagram

The symbols, and descriptions, used for bit function in each register are shown below.



*1
Blank:Set to “0” or “1” according to the application
0: Set to “0”
1: Set to “1”
X: Nothing is assigned

*2
RW: Read and write
RO: Read only
WO: Write only
–: Nothing is assigned

*3
- Reserved bit
  Reserved bit. Set to specified value.

*4
- Nothing is assigned
  Nothing is assigned to the bit concerned. As the bit may be use for future functions, set to “0” when writing to this bit.
- Do not set to this value
  The operation is not guaranteed when a value is set.
- Function varies depending on mode of operation
  Bit function varies depending on peripheral function mode.
  Refer to respective register for each mode.

*5
Follow the text in each manual for binary and hexadecimal notations.

3. M16C Family Documents

The following documents were prepared for the M16C family.(1)

Document	Contents
Short Sheet	Hardware overview
Data Sheet	Hardware overview and electrical characteristics
Hardware Manual	Hardware specifications (pin assignments, memory maps, peripheral specifications, electrical characteristics, timing charts). *Refer to the application note for how to use peripheral functions.
Software Manual	Detailed description of assembly instructions and microcomputer performance of each instruction
Application Note	• Usage and application examples of peripheral functions • Sample programs • Introduction to the basic functions in the M16C family • Programming method with Assembly and C languages
RENESAS TECHNICAL UPDATE	Preliminary report about the specification of a product, a document, etc.

NOTES:

1. Before using this material, please visit the our website to verify that this is the most updated document available.

Table of Contents

SFR Page Reference

Address	Register	Symbol	Page
0000_{16}			
0001_{16}			
0002_{16}			
0003_{16}			
0004_{16}	Processor mode register 0	PM0	31
0005_{16}	Processor mode register 1	PM1	31
0006_{16}	System clock control register 0	CM0	19
0007_{16}	System clock control register 1	CM1	19
0008_{16}			
0009_{16}	Address match interrupt enable register	AIER	52
$000A_{16}$	Protect register	PRCR	30
$000B_{16}$			
$000C_{16}$	Oscillation stop detection register	OCD	20
$000D_{16}$	Watchdog timer reset register	WDTR	54
$000E_{16}$	Watchdog timer start register	WDTS	54
$000F_{16}$	Watchdog timer control register	WDC	54
0010_{16} 0011_{16} 0012_{16}	Address match interrupt register 0	RMAD0	52
0013_{16}			
0014_{16} 0015_{16} 0016_{16}	Address match interrupt register 1	RMAD1	52
0017_{16}			
0018_{16}			
0019_{16}			
$001A_{16}$			
$001B_{16}$			
$001C_{16}$			
$001D_{16}$			
$001E_{16}$	$\overline{\text{INT0}}$ input filter select register	INT0F	46
$001F_{16}$			
0020_{16}			
0021_{16}			
0022_{16}			
0023_{16}			
0024_{16}			
0025_{16}			
0026_{16}			
0027_{16}			
0028_{16}			
0029_{16}			
$002A_{16}$			
$002B_{16}$			
$002C_{16}$			
$002D_{16}$			
$002E_{16}$			
$002F_{16}$			
0030_{16}			
0031_{16}			
0032_{16}			
0033_{16}			
0034_{16}			
0035_{16}			
0036_{16}			
0037_{16}			
0038_{16}			
0039_{16}			
$003A_{16}$			
$003B_{16}$			
$003C_{16}$			
$003D_{16}$			
$003E_{16}$			
$003F_{16}$			

Address	Register	Symbol	Page
0040_{16}			
0041_{16}			
0042_{16}			
0043_{16}			
0044_{16}			
0045_{16}			
0046_{16}			
0047_{16}			
0048_{16}			
0049_{16}			
$004A_{16}$			
$004B_{16}$			
$004C_{16}$			
$004D_{16}$	Key input interrupt control register	KUPIC	39
$004E_{16}$	AD conversion interrupt control register	ADIC	39
$004F_{16}$			
0050_{16}			
0051_{16}	UART0 transmit interrupt control register	S0TIC	39
0052_{16}	UART0 receive interrupt control register	S0RIC	39
0053_{16}	UART1 transmit interrupt control register	S1TIC	39
0054_{16}	UART1 receive interrupt control register	S1RIC	39
0055_{16}	$\overline{\text{INT2}}$ interrupt control register	INT2IC	39
0056_{16}	Timer X interrupt control register	TXIC	39
0057_{16}	Timer Y interrupt control register	TYIC	39
0058_{16}	Timer Z interrupt control register	TZIC	39
0059_{16}	$\overline{\text{INT1}}$ interrupt control register	INT1IC	39
$005A_{16}$	$\overline{\text{INT3}}$ interrupt control register	INT3IC	39
$005B_{16}$	Timer C interrupt control register	TCIC	39
$005C_{16}$			
$005D_{16}$	$\overline{\text{INT0}}$ interrupt control register	INT0IC	39
$005E_{16}$			
$005F_{16}$			
0060_{16}			
0061_{16}			
0062_{16}			
0063_{16}			
0064_{16}			
0065_{16}			
0066_{16}			
0067_{16}			
0068_{16}			
0069_{16}			
$006A_{16}$			
$006B_{16}$			
$006C_{16}$			
$006D_{16}$			
$006E_{16}$			
$006F_{16}$			
0070_{16}			
0071_{16}			
0072_{16}			
0073_{16}			
0074_{16}			
0075_{16}			
0076_{16}			
0077_{16}			
0078_{16}			
0079_{16}			
$007A_{16}$			
$007B_{16}$			
$007C_{16}$			
$007D_{16}$			
$007E_{16}$			
$007F_{16}$			

Blank columns are all reserved space. No use is allowed.

SFR Page Reference

Address	Register	Symbol	Page
0080_{16}	Timer Y, Z mode register	TYZMR	65/73
0081_{16}	Prescaler Y register	PREY	66
0082_{16}	Timer Y secondary register	TYSC	66
0083_{16}	Timer Y primary register	TYPR	66
0084_{16}	Timer Y, Z waveform output control register	PUM	67/75
0085_{16}	Prescaler Z register	PREZ	74
0086_{16}	Timer Z secondary register	TZSC	74
0087_{16}	Timer Z primary register	TZPR	74
0088_{16}			
0089_{16}			
$008A_{16}$	Timer Y, Z output control register	TYZOC	66/74
$008B_{16}$	Timer X mode register	TXMR	56
$008C_{16}$	Prescaler X register	PREX	57
$008D_{16}$	Timer X register register	TX	57
$008E_{16}$	Timer count source setting register	TCSS	57
$008F_{16}$			
0090_{16}	Timer C register	TC	87
0091_{16}			
0092_{16}			
0093_{16}			
0094_{16}			
0095_{16}			
0096_{16}	External input enable register	INTEN	46
0097_{16}			
0098_{16}	Key input enable register	KIEN	50
0099_{16}			
$009A_{16}$	Timer C control register 0	TCC0	87
$009B_{16}$	Timer C control register 1	TCC1	87
$009C_{16}$	Capture register	TM0	87
$009D_{16}$			
$009E_{16}$			
$009F_{16}$			
$00A0_{16}$	UART0 transmit/receive mode register	U0MR	92
$00A1_{16}$	UART0 bit rate generator	U0BRG	91
$00A2_{16}$	UART0 transmit buffer register	U0TB	91
$00A3_{16}$			
$00A4_{16}$	UART0 transmit/receive control register 0	U0C0	92
$00A5_{16}$	UART0 transmit/receive control register 1	U0C1	93
$00A6_{16}$	UART0 receive buffer register	U0RB	91
$00A7_{16}$			
$00A8_{16}$	UART1 transmit/receive mode register	U1MR	92
$00A9_{16}$	UART1 bit rate generator	U1BRG	91
$00AA_{16}$	UART1 transmit buffer register	U1TB	91
$00AB_{16}$			
$00AC_{16}$	UART1 transmit/receive control register 0	U1C0	92
$00AD_{16}$	UART1 transmit/receive control register 1	U1C1	93
$00AE_{16}$	UART1 receive buffer register	U1RB	91
$00AF_{16}$			
$00B0_{16}$	UART transmit/receive control register 2	UCON	93
$00B1_{16}$			
$00B2_{16}$			
$00B3_{16}$			
$00B4_{16}$			
$00B5_{16}$			
$00B6_{16}$			
$00B7_{16}$			
$00B8_{16}$			
$00B9_{16}$			
$00BA_{16}$			
$00BB_{16}$			
$00BC_{16}$			
$00BD_{16}$			
$00BE_{16}$			
$00BF_{16}$			

Blank columns are all reserved space. No use is allowed.

Address	Register	Symbol	Page
$00C0_{16}$	AD register	AD	107
$00C1_{16}$			
$00C2_{16}$			
$00C3_{16}$			
$00C4_{16}$			
$00C5_{16}$			
$00C6_{16}$			
$00C7_{16}$			
$00C8_{16}$			
$00C9_{16}$			
$00CA_{16}$			
$00CB_{16}$			
$00CC_{16}$			
$00CD_{16}$			
$00CE_{16}$			
$00CF_{16}$			
$00D0_{16}$			
$00D1_{16}$			
$00D2_{16}$			
$00D3_{16}$			
$00D4_{16}$	AD control register 2	ADCON2	107
$00D5_{16}$			
$00D6_{16}$	AD control register 0	ADCON0	106
$00D7_{16}$	AD control register 1	ADCON1	106
$00D8_{16}$			
$00D9_{16}$			
$00DA_{16}$			
$00DB_{16}$			
$00DC_{16}$			
$00DD_{16}$			
$00DE_{16}$			
$00DF_{16}$			
$00E0_{16}$	Port P0 register	P0	121
$00E1_{16}$	Port P1 register	P1	121
$00E2_{16}$	Port P0 direction register	PD0	121
$00E3_{16}$	Port P1 direction register	PD1	121
$00E4_{16}$			
$00E5_{16}$	Port P3 register	P3	121
$00E6_{16}$			
$00E7_{16}$	Port P3 direction register	PD3	121
$00E8_{16}$	Port P4 register	P4	121
$00E9_{16}$			
$00EA_{16}$	Port P4 direction register	PD4	121
$00EB_{16}$			
$00EC_{16}$			
$00ED_{16}$			
$00EE_{16}$			
$00EF_{16}$			
$00F0_{16}$			
$00F1_{16}$			
$00F2_{16}$			
$00F3_{16}$			
$00F4_{16}$			
$00F5_{16}$			
$00F6_{16}$			
$00F7_{16}$			
$00F8_{16}$			
$00F9_{16}$			
$03FA_{16}$			
$00FB_{16}$			
$00FC_{16}$	Pull-up control register 0	PUR0	122
$00FD_{16}$	Pull-up control register 1	PUR1	122
$00FE_{16}$	Port P1 drive capacity control register	DRR	122
$00FF_{16}$			
$01B3_{16}$	Flash memory control register 4	FMR4	148
$01B4_{16}$			
$01B5_{16}$	Flash memory control register 1	FMR1	148
$01B6_{16}$			
$01B7_{16}$	Flash memory control register 0	FMR0	147

$0FFFF_{16}$	Option function select register	OFS	54

REJ09B0110-0120
Rev.1.20
Jan 27, 2006

1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.
The data flash ROM (2 KB X 2 blocks) is embedded.

1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

1.2 Performance Overview

Table 1.1. lists the performance outline of this MCU.

Table 1.1 Performance outline

Item		Performance
CPU	Number of basic instructions	89 instructions
	Minimum instruction execution time	62.5 ns (f(XIN) = 16 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1M bytes
	Memory capacity	See Table 1.2 “Product List”
Peripheral function	Port	Input/Output: 22 (including LED drive port), Input: 2
	LED drive port	I/O port: 8
	Timer	Timer X: 8 bits x 1 channel, Timer Y: 8 bits x 1 channel, Timer Z: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits x 1 channel (Input capture circuit)
	Serial Interface	•1 channel Clock synchronous, UART •1 channel UART
	A/D converter	10-bit A/D converter: 1 circuit, 8 channels
	Watchdog timer	15 bits x 1 (with prescaler) Reset start function selectable
	Interrupt	Internal: 9 factors, External: 5 factors, Software: 4 factors, Priority level: 7 levels
	Clock generation circuit	2 circuits •Main clock generation circuit (Equipped with a built-in feedback resistor) •On-chip oscillator
	Oscillation stop detection function	Main clock oscillation stop detection function
Electrical characteristics	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)
	Power consumption	Typ.8mA (VCC = 5.0 V (f(XIN) = 16 MHz) Typ.5mA (VCC = 3.0 V, (f(XIN) = 10 MHz) Typ.35µA (VCC = 3.0 V, Wait mode, peripheral clock stops) Typ.0.7µA (VCC = 3.0 V, Stop mode)
Flash memory	Program/erase supply voltage	VCC = 2.7 to 5.5 V
	Program/erase endurance	10,000 times (Data flash)
		1,000 times (Program ROM)
Operating ambient temperature		-20 to 85 °C -40 to 85 °C (D-version)
Package		32-pin plastic mold LQFP

1.3 Block Diagram

Figure 1.1. shows this MCU block diagram.

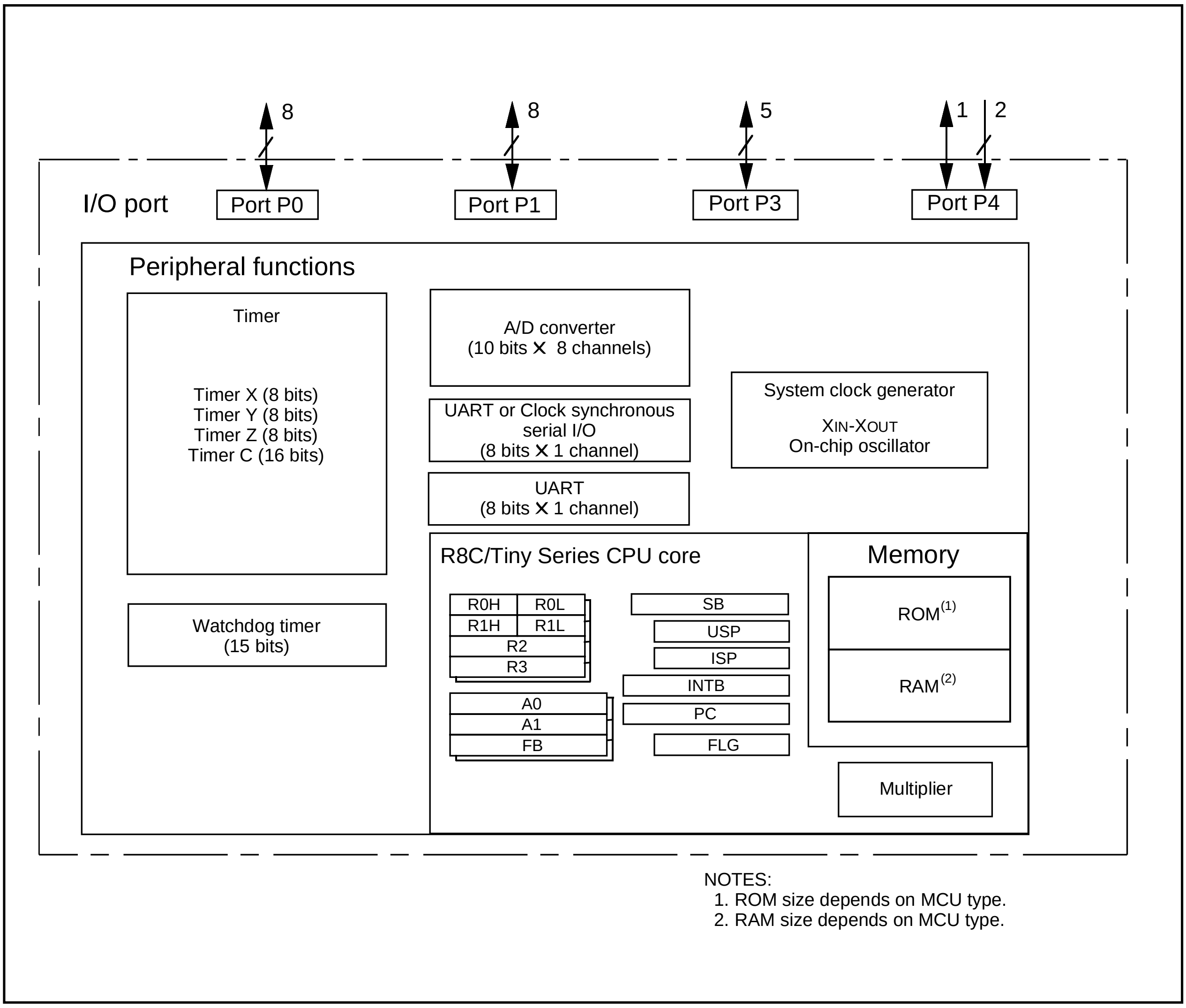


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.2 lists the product information.

Table 1.2 Product Information

As of January 2006

Type No.	ROM capacity		RAM capacity	Package type	Remarks
	Program ROM	Data flash			
R5F21122FP	8K bytes	2K bytes x 2	512 bytes	PLQP0032GB-A	Flash memory version
R5F21123FP	12K bytes	2K bytes x 2	768 bytes	PLQP0032GB-A	
R5F21124FP	16K bytes	2K bytes x 2	1K bytes	PLQP0032GB-A	
R5F21122DFP	8K bytes	2K bytes x 2	512 bytes	PLQP0032GB-A	D version
R5F21123DFP	12K bytes	2K bytes x 2	768 bytes	PLQP0032GB-A	
R5F21124DFP	16K bytes	2K bytes x 2	1K bytes	PLQP0032GB-A	

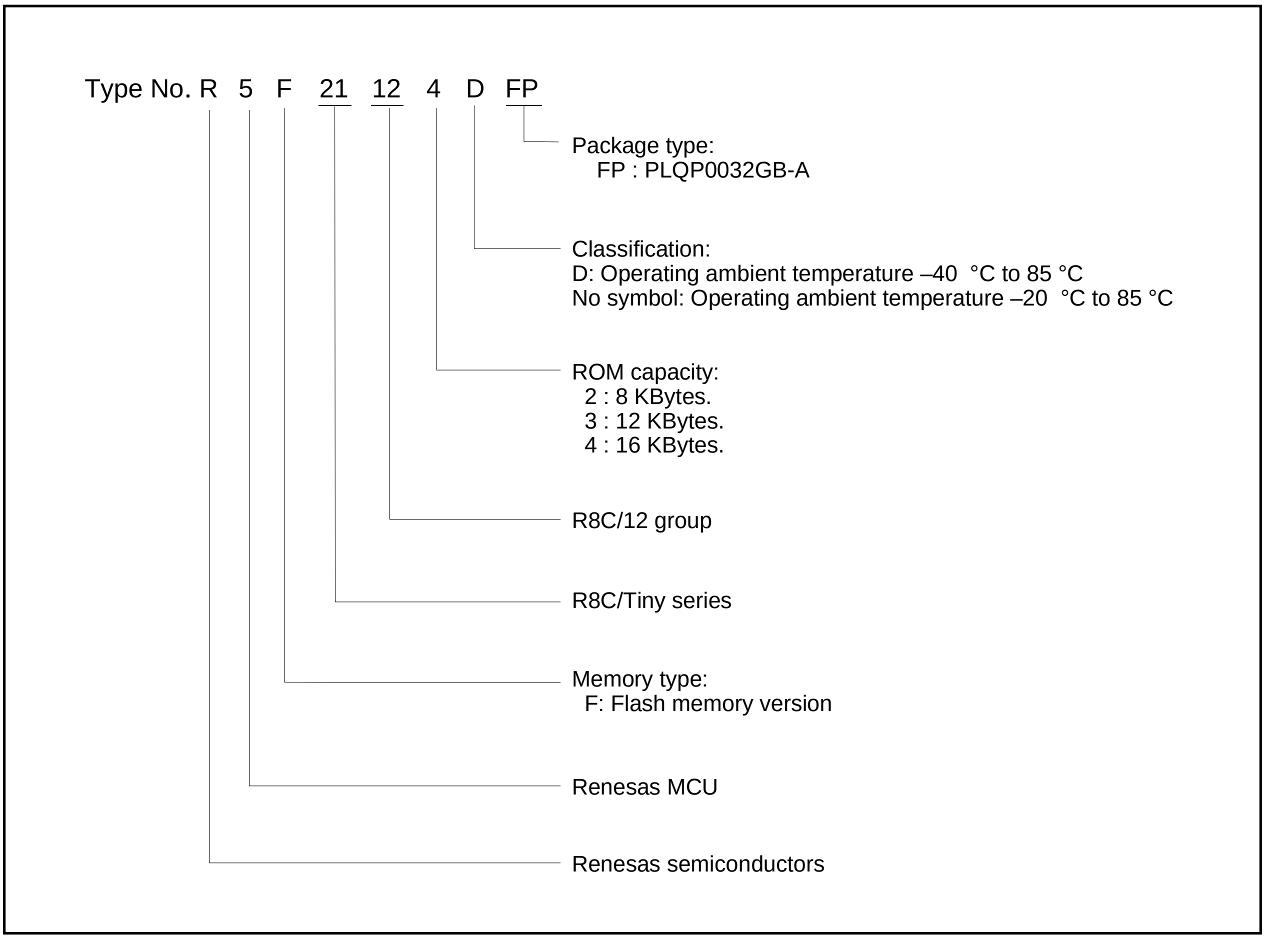
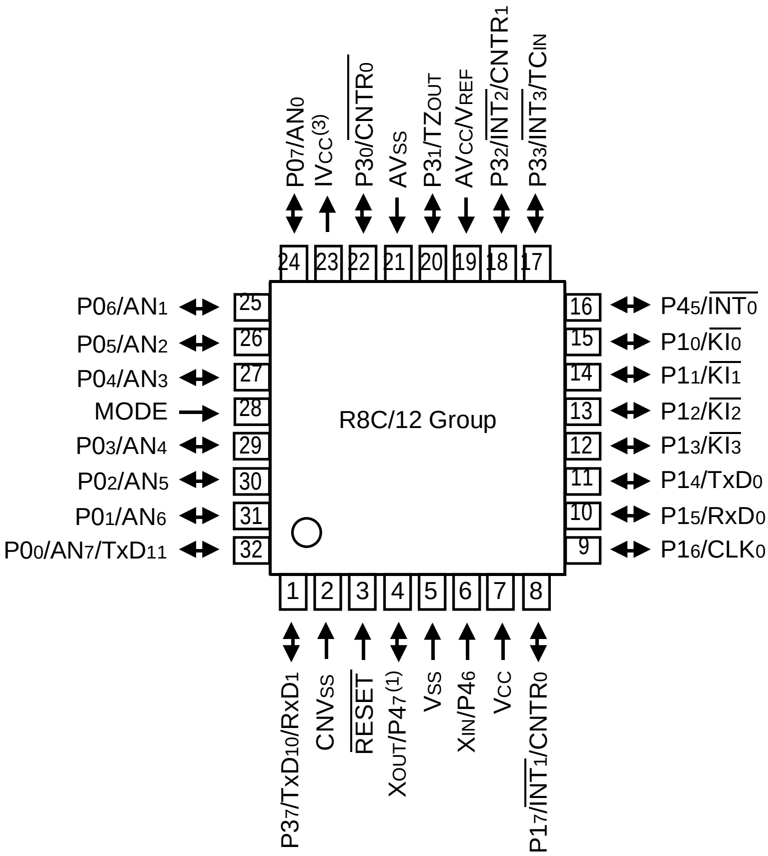


Figure 1.2 Type No., Memory Size, and Package

1.5 Pin Assignments

Figure 1.3 shows the pin configuration (top view).

PIN CONFIGURATION (top view)



NOTES:
1. $P4_7$ functions only as an input port.
2. When using on-chip debugger, do not use $P0_0/AN_7/TxD_{11}$ and $P3_7/TxD_{10}/RxD_1$.
3. Do not connect IVcc to Vcc.

Package: PLQP0032GB-A (32P6U-A)

Figure 1.3 Pin Configuration (Top View)

1.6 Pin Description

Table 1.3 shows the pin description

Table 1.3 Pin description

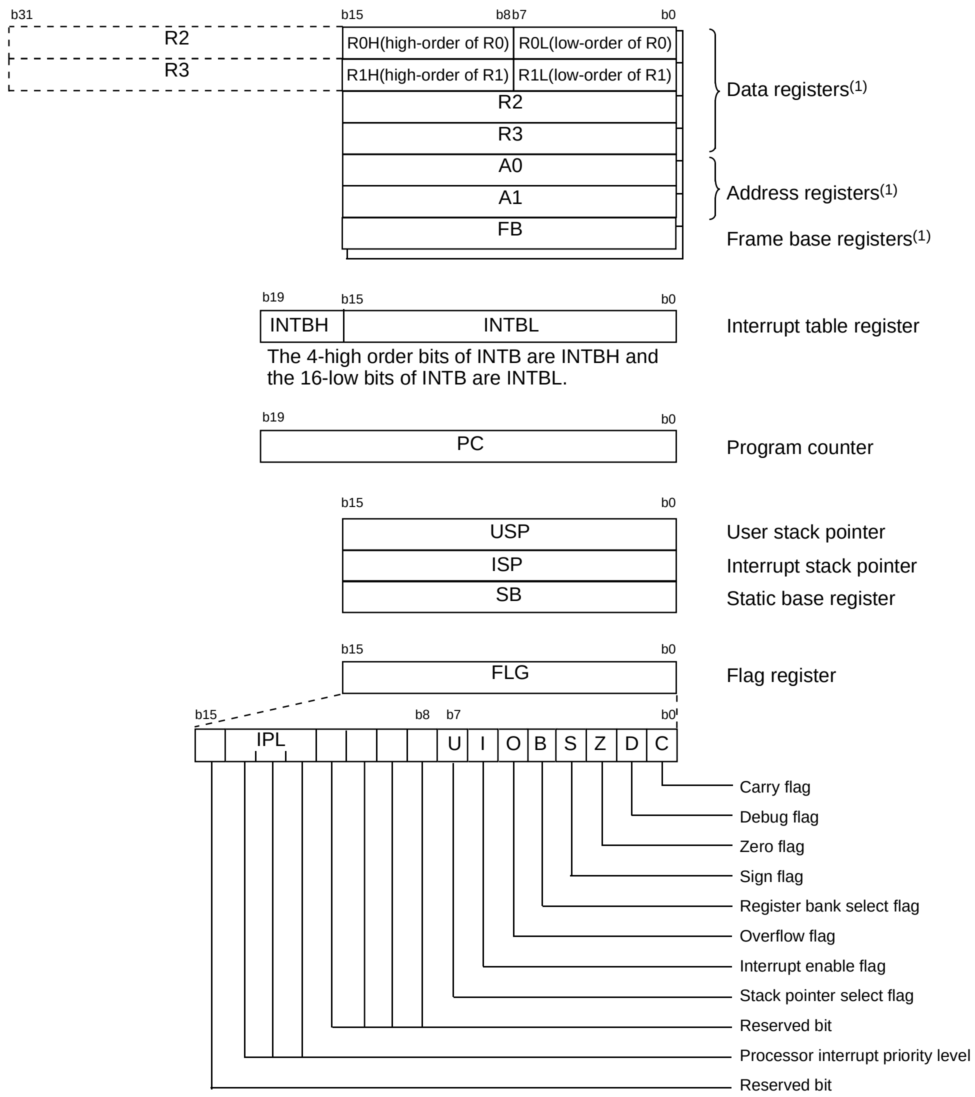
Signal name	Pin name	I/O type	Function
Power supply input	Vcc, Vss	I	Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin.
IVcc	IVcc	O	This pin is to stabilize internal power supply. Connect this pin to Vss via a capacitor (0.1 µF). Do not connect to Vcc.
Analog power supply input	AVcc, AVss	I	Power supply input pins for A/D converter. Connect the AVcc pin to Vcc. Connect the AVss pin to Vss. Connect a capacitor between pins AVcc and AVss.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
CNVss	CNVss	I	Connect this pin to Vss via a resistor.(1)
MODE	MODE	I	Connect this pin to Vcc via a resistor.
Main clock input	XIN	I	These pins are provided for the main clock generating circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
Main clock output	XOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt pins.
Timer X	CNTR0	I/O	Timer X I/O pin
	$\overline{\text{CNTR0}}$	O	Timer X output pin
Timer Y	CNTR1	I/O	Timer Y I/O pin
Timer Z	TZOUT	O	Timer Z output pin
Timer C	TCIN	I	Timer C input pin
Serial interface	CLK0	I/O	Transfer clock I/O pin.
	RxD0, RxD1	I	Serial data input pins.
	TxD0, TxD10, TxD11	O	Serial data output pins.
Reference voltage input	VREF	I	Reference voltage input pin for A/sD converter. Connect the VREF pin to Vcc.
A/D converter	AN0 to AN7	I	Analog input pins for A/D converter
I/O port	P00 to P07, P10 to P17, P30 to P33, P37, P45	I/O	These are 8-bit CMOS I/O ports. Each port has an input/output select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P10 to P17 also function as LED drive ports.
Input port	P46, P47	I	Port for input-only.

NOTES :

1. Refer to "19.8 Noise" for the connecting reference resistor value.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. Two sets of register banks are provided.



NOTES:
1. A register bank comprises these registers. Two sets of register banks are provided

Figure 2.1 CPU Register

2.1 Data Registers (R0, R1, R2 and R3)

R0 is a 16-bit register for transfer, arithmetic and logic operations. The same applies to R1 to R3. The R0 can be split into high-order bit (R0H) and low-order bit (R0L) to be used separately as 8-bit data registers. The same applies to R1H and R1L as R0H and R0L. R2 can be combined with R0 to be used as a 32-bit data register (R2R0). The same applies to R3R1 as R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. They also are used for transfer, arithmetic and logic operations. The same applies to A1 as A0. A0 can be combined with A0 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC, 20 bits wide, indicates the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP and ISP, are 16 bits wide each. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is a 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic logic unit.

2.8.2 Debug Flag (D)

The D flag is for debug only. Set to “0”.

2.8.3 Zero Flag (Z)

The Z flag is set to “1” when an arithmetic operation resulted in 0; otherwise, “0”.

2.8.4 Sign Flag (S)

The S flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, “0”.

2.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is “0”. The register bank 1 is selected when this flag is set to “1”.

2.8.6 Overflow Flag (O)

The O flag is set to “1” when the operation resulted in an overflow; otherwise, “0”.

2.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

An interrupt is disabled when the I flag is set to “0”, and are enabled when the I flag is set to “1”. The I flag is set to “0” when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to “0”, USP is selected when the U flag is set to “1”.

The U flag is set to “0” when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

When write to this bit, set to “0”. When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map of this MCU. This MCU provides 1-Mbyte address space from addresses 00000_{16} to $FFFFF_{16}$.

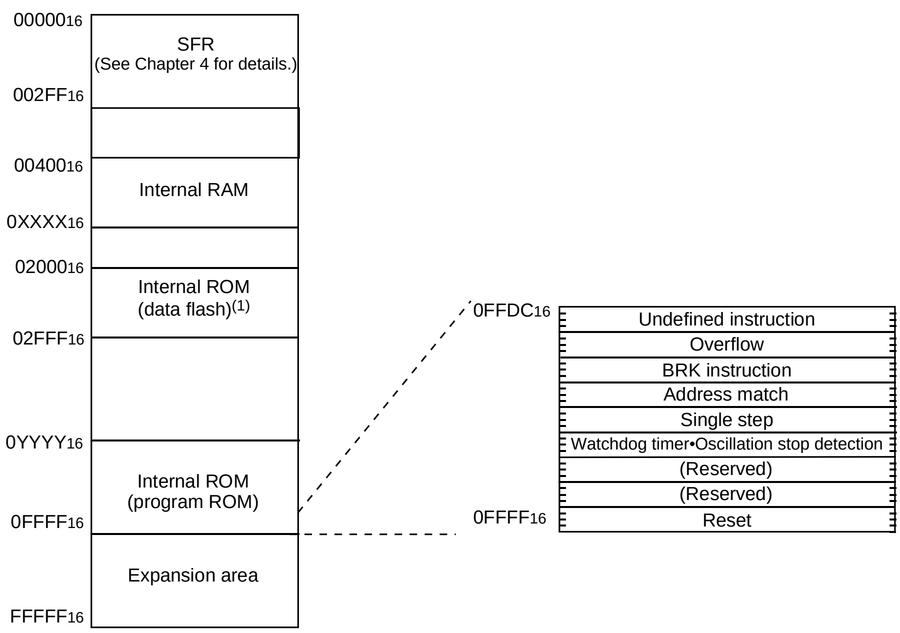
The internal ROM (program ROM) is allocated lower addresses beginning with address $0FFFF_{16}$. For example, a 16-Kbyte internal ROM is allocated addresses from $0C000_{16}$ to $0FFFF_{16}$.

The fixed interrupt vector table is allocated addresses $0FFDC_{16}$ to $0FFFF_{16}$. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses from 02000_{16} to $02FFF_{16}$.

The internal RAM is allocated addresses beginning with address 00400_{16}. For example, a 1-Kbyte internal RAM is allocated addresses 00400_{16} to $007FF_{16}$. The internal RAM is used not only for storing data, but for calling subroutines and stacks when interrupt request is acknowledged.

Special function registers (SFR) are allocated addresses 00000_{16} to $002FF_{16}$. The peripheral function control registers are located them. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.



NOTES:
1. The data flash block A (2K bytes) and block B (2K bytes) are shown.
2. Blank space are reserved. No access is allowed.

Type name	Internal ROM		Internal RAM	
	Size	Address $0YYYY_{16}$	Size	Address $0XXXX_{16}$
R5F21124FP, R5F21124DFP	16K bytes	$0C000_{16}$	1K bytes	$007FF_{16}$
R5F21123FP, R5F21123DFP	12K bytes	$0D000_{16}$	768 bytes	$006FF_{16}$
R5F21122FP, R5F21122DFP	8K bytes	$0E000_{16}$	512 bytes	$005FF_{16}$

Figure 3.1 Memory Map

4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information

Table 4.1 SFR Information(1)[1]

Address	Register	Symbol	After reset
0000_{16}			
0001_{16}			
0002_{16}			
0003_{16}			
0004_{16}	Processor mode register 0	PM0	$XXXX0X00_2$
0005_{16}	Processor mode register 1	PM1	$00XXX0X0_2$
0006_{16}	System clock control register 0	CM0	01101000_2
0007_{16}	System clock control register 1	CM1	00100000_2
0008_{16}			
0009_{16}	Address match interrupt enable register	AIER	$XXXXXX00_2$
$000A_{16}$	Protect register	PRCR	$00XXX000_2$
$000B_{16}$			
$000C_{16}$	Oscillation stop detection register	OCD	00000100_2
$000D_{16}$	Watchdog timer reset register	WDTR	XX_{16}
$000E_{16}$	Watchdog timer start register	WDTS	XX_{16}
$000F_{16}$	Watchdog timer control register	WDC	00011111_2
0010_{16}	Address match interrupt register 0	RMAD0	00_{16}
0011_{16}			00_{16}
0012_{16}			$X0_{16}$
0013_{16}			
0014_{16}	Address match interrupt register 1	RMAD1	00_{16}
0015_{16}			00_{16}
0016_{16}			$X0_{16}$
0017_{16}			
0018_{16}			
0019_{16}			
$001A_{16}$			
$001B_{16}$			
$001C_{16}$			
$001D_{16}$			
$001E_{16}$	$\overline{INT0}$ input filter select register	INT0F	$XXXXX000_2$
$001F_{16}$			
0020_{16}			
0021_{16}			
0022_{16}			
0023_{16}			
0024_{16}			
0025_{16}			
0026_{16}			
0027_{16}			
0028_{16}			
0029_{16}			
$002A_{16}$			
$002B_{16}$			
$002C_{16}$			
$002D_{16}$			
$002E_{16}$			
$002F_{16}$			
0030_{16}			
0031_{16}			
0032_{16}			
0033_{16}			
0034_{16}			
0035_{16}			
0036_{16}			
0037_{16}			
0038_{16}			
0039_{16}			
$003A_{16}$			
$003B_{16}$			
$003C_{16}$			
$003D_{16}$			
$003E_{16}$			
$003F_{16}$			

NOTES :
1. Blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.2 SFR Information(2)[1]

Address	Register	Symbol	After reset
0040_{16}			
0041_{16}			
0042_{16}			
0043_{16}			
0044_{16}			
0045_{16}			
0046_{16}			
0047_{16}			
0048_{16}			
0049_{16}			
$004A_{16}$			
$004B_{16}$			
$004C_{16}$			
$004D_{16}$	Key input interrupt control register	KUPIC	$XXXXX000_2$
$004E_{16}$	AD conversion interrupt control register	ADIC	$XXXXX000_2$
$004F_{16}$			
0050_{16}			
0051_{16}	UART0 transmit interrupt control register	S0TIC	$XXXXX000_2$
0052_{16}	UART0 receive interrupt control register	S0RIC	$XXXXX000_2$
0053_{16}	UART1 transmit interrupt control register	S1TIC	$XXXXX000_2$
0054_{16}	UART1 receive interrupt control register	S1RIC	$XXXXX000_2$
0055_{16}	$\overline{INT2}$ interrupt control register	INT2IC	$XXXXX000_2$
0056_{16}	Timer X interrupt control register	TXIC	$XXXXX000_2$
0057_{16}	Timer Y interrupt control register	TYIC	$XXXXX000_2$
0058_{16}	Timer Z interrupt control register	TZIC	$XXXXX000_2$
0059_{16}	$\overline{INT1}$ interrupt control register	INT1IC	$XXXXX000_2$
$005A_{16}$	$\overline{INT3}$ interrupt control register	INT3IC	$XXXXX000_2$
$005B_{16}$	Timer C interrupt control register	TCIC	$XXXXX000_2$
$005C_{16}$			
$005D_{16}$	$\overline{INT0}$ interrupt control register	INT0IC	$XX00X000_2$
$005E_{16}$			
$005F_{16}$			
0060_{16}			
0061_{16}			
0062_{16}			
0063_{16}			
0064_{16}			
0065_{16}			
0066_{16}			
0067_{16}			
0068_{16}			
0069_{16}			
$006A_{16}$			
$006B_{16}$			
$006C_{16}$			
$006D_{16}$			
$006E_{16}$			
$006F_{16}$			
0070_{16}			
0071_{16}			
0072_{16}			
0073_{16}			
0074_{16}			
0075_{16}			
0076_{16}			
0077_{16}			
0078_{16}			
0079_{16}			
$007A_{16}$			
$007B_{16}$			
$007C_{16}$			
$007D_{16}$			
$007E_{16}$			
$007F_{16}$			

NOTES :
1. Blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.3 SFR Information(3)[1]

Address	Register	Symbol	After reset
0080_{16}	Timer Y, Z mode register	TYZMR	00_{16}
0081_{16}	Prescaler Y register	PREY	FF_{16}
0082_{16}	Timer Y secondary register	TYSC	FF_{16}
0083_{16}	Timer Y primary register	TYPR	FF_{16}
0084_{16}	Timer Y, Z waveform output control register	PUM	00_{16}
0085_{16}	Prescaler Z register	PREZ	FF_{16}
0086_{16}	Timer Z secondary register	TZSC	FF_{16}
0087_{16}	Timer Z primary register	TZPR	FF_{16}
0088_{16}			
0089_{16}			
$008A_{16}$	Timer Y, Z output control register	TYZOC	00_{16}
$008B_{16}$	Timer X mode register	TXMR	00_{16}
$008C_{16}$	Prescaler X register	PREX	FF_{16}
$008D_{16}$	Timer X register	TX	FF_{16}
$008E_{16}$	Timer count source setting register	TCSS	00_{16}
$008F_{16}$			
0090_{16} 0091_{16}	Timer C register	TC	00_{16} 00_{16}
0092_{16}			
0093_{16}			
0094_{16}			
0095_{16}			
0096_{16}	External input enable register	INTEN	00_{16}
0097_{16}			
0098_{16}	Key input enable register	KIEN	00_{16}
0099_{16}			
$009A_{16}$	Timer C control register 0	TCC0	00_{16}
$009B_{16}$	Timer C control register 1	TCC1	00_{16}
$009C_{16}$ $009D_{16}$	Capture register	TM0	00_{16} 00_{16}
$009E_{16}$			
$009F_{16}$			
$00A0_{16}$	UART0 transmit/receive mode register	U0MR	00_{16}
$00A1_{16}$	UART0 bit rate register	U0BRG	XX_{16}
$00A2_{16}$ $00A3_{16}$	UART0 transmit buffer register	U0TB	XX_{16} XX_{16}
$00A4_{16}$	UART0 transmit/receive control register 0	U0C0	00001000_2
$00A5_{16}$	UART0 transmit/receive control register 1	U0C1	00000010_2
$00A6_{16}$ $00A7_{16}$	UART0 receive buffer register	U0RB	XX_{16} XX_{16}
$00A8_{16}$	UART1 transmit/receive mode register	U1MR	00_{16}
$00A9_{16}$	UART1 bit rate generator	U1BRG	XX_{16}
$00AA_{16}$ $00AB_{16}$	UART1 transmit buffer register	U1TB	XX_{16} XX_{16}
$00AC_{16}$	UART1 transmit/receive control register 0	U1C0	00001000_2
$00AD_{16}$	UART1 transmit/receive control register 1	U1C1	00000010_2
$00AE_{16}$ $00AF_{16}$	UART1 receive buffer register	U1RB	XX_{16} XX_{16}
$00B0_{16}$	UART transmit/receive control register 2	UCON	00_{16}
$00B1_{16}$			
$00B2_{16}$			
$00B3_{16}$			
$00B4_{16}$			
$00B5_{16}$			
$00B6_{16}$			
$00B7_{16}$			
$00B8_{16}$			
$00B9_{16}$			
$00BA_{16}$			
$00BB_{16}$			
$00BC_{16}$			
$00BD_{16}$			
$00BE_{16}$			
$00BF_{16}$			

NOTES :
1. Blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.4 SFR Information(4)[1]

Address	Register	Symbol	After reset
$00C0_{16}$ $00C1_{16}$	AD register	AD	$XXXXXXXX_2$ $XXXXXXXX_2$
$00C2_{16}$			
$00C3_{16}$			
$00C4_{16}$			
$00C5_{16}$			
$00C6_{16}$			
$00C7_{16}$			
$00C8_{16}$			
$00C9_{16}$			
$00CA_{16}$			
$00CB_{16}$			
$00CC_{16}$			
$00CD_{16}$			
$00CE_{16}$			
$00CF_{16}$			
$00D0_{16}$			
$00D1_{16}$			
$00D2_{16}$			
$00D3_{16}$			
$00D4_{16}$	AD control register 2	ADCON2	00_{16}
$00D5_{16}$			
$00D6_{16}$	AD control register 0	ADCON0	$00000XXX_2$
$00D7_{16}$	AD control register 1	ADCON1	00_{16}
$00D8_{16}$			
$00D9_{16}$			
$00DA_{16}$			
$00DB_{16}$			
$00DC_{16}$			
$00DD_{16}$			
$00DE_{16}$			
$00DF_{16}$			
$00E0_{16}$	Port P0 register	P0	XX_{16}
$00E1_{16}$	Port P1 register	P1	XX_{16}
$00E2_{16}$	Port P0 direction register	PD0	00_{16}
$00E3_{16}$	Port P1 direction register	PD1	00_{16}
$00E4_{16}$			
$00E5_{16}$	Port P3 register	P3	XX_{16}
$00E6_{16}$			
$00E7_{16}$	Port P3 direction register	PD3	00_{16}
$00E8_{16}$	Port P4 register	P4	XX_{16}
$00E9_{16}$			
$00EA_{16}$	Port P4 direction register	PD4	00_{16}
$00EB_{16}$			
$00EC_{16}$			
$00ED_{16}$			
$00EE_{16}$			
$00EF_{16}$			
$00F0_{16}$			
$00F1_{16}$			
$00F2_{16}$			
$00F3_{16}$			
$00F4_{16}$			
$00F5_{16}$			
$00F6_{16}$			
$00F7_{16}$			
$00F8_{16}$			
$00F9_{16}$			
$03FA_{16}$			
$00FB_{16}$			
$00FC_{16}$	Pull-up control register 0	PUR0	$00XX0000_2$
$00FD_{16}$	Pull-up control register 1	PUR1	$XXXXXX0X_2$
$00FE_{16}$	Port P1 drive capacity control register	DRR	00_{16}
$00FF_{16}$			
$01B3_{16}$	Flash memory control register 4	FMR4	01000000_2
$01B4_{16}$			
$01B5_{16}$	Flash memory control register 1	FMR1	$1000000X_2$
$01B6_{16}$			
$01B7_{16}$	Flash memory control register 0	FMR0	00000001_2
$0FFFF_{16}$	Option function select register[2]	OFS	(Note 2)

NOTES :
1. Blank columns, 0100_{16} to $01B2_{16}$ and $01B8_{16}$ to $02FF_{16}$ are all reserved. No access is allowed.
2. The watchdog timer control bit is assigned. Refer to "Figure11.2 OFS, WDC, WDTR and WDTS registers" for the OFS register details

X : Undefined

5. Reset

There are three types of resets: a hardware reset, a software reset, and an watchdog timer reset.

5.1 Hardware Reset

A reset is applied using the $\overline{\text{RESET}}$ pin. When an “L” signal is applied to the $\overline{\text{RESET}}$ pin while the power supply voltage is within the recommended operating condition, the pins are initialized (see Table 5.1 “Pin Status When $\overline{\text{RESET}}$ Pin Level is 'L'”). When the input level at the $\overline{\text{RESET}}$ pin is released from “L” to “H”, the CPU and SFR are initialized, and the program is executed starting from the address indicated by the reset vector. Figure 5.1 shows the CPU register status after reset and figure 5.2 shows the reset sequence. After reset, the on-chip oscillator clock divided by 8 is automatically selected for the CPU. The internal RAM is not initialized. If the $\overline{\text{RESET}}$ pin is pulled “L” while writing to the internal RAM, the internal RAM becomes indeterminate. Figures 5.3 to 5.4 show the reset circuit example. Refer to Chapter 4, “Special Function Register (SFR)” for the status of SFR after reset.

• When the power supply is stable
(1) Apply an “L” signal to the $\overline{\text{RESET}}$ pin.
(2) Wait for 500 µs ($1/f_{RING} \times 20$).
(3) Apply an “H” signal to the $\overline{\text{RESET}}$ pin.
• Power on
(1) Apply an “L” signal to the $\overline{\text{RESET}}$ pin.
(2) Let the power supply voltage increase until it meets the recommended operating condition.
(3) Wait td(P-R) or more until the internal power supply stabilizes.
(4) Wait for 500 µs ($1/f_{RING} \times 20$).
(5) Apply an “H” signal to the $\overline{\text{RESET}}$ pin.

Table 5.1 Pin Status When $\overline{\text{RESET}}$ Pin Level is “L”

Pin name	Status
P0	Input port
P1	Input port
$P3_0$ to $P3_3$, $P3_7$	Input port
$P4_5$ to $P4_7$	Input port

5.2 Software Reset

When the PM03 bit in the PM0 register is set to “1” (microcomputer reset), the microcomputer has its pins, CPU, and SFR initialized. Then the program is executed starting from the address indicated by the reset vector. After reset, the on-chip oscillator clock divided by 8 is automatically selected for the CPU.

5.3 Watchdog Timer Reset

Where the PM12 bit in the PM1 register is “1” (reset when watchdog timer underflows), the microcomputer initializes its pins, CPU and SFR if the watchdog timer underflows. Then the program is executed starting from the address indicated by the reset vector. After reset, the on-chip oscillator clock divided by 8 is automatically selected for the CPU.

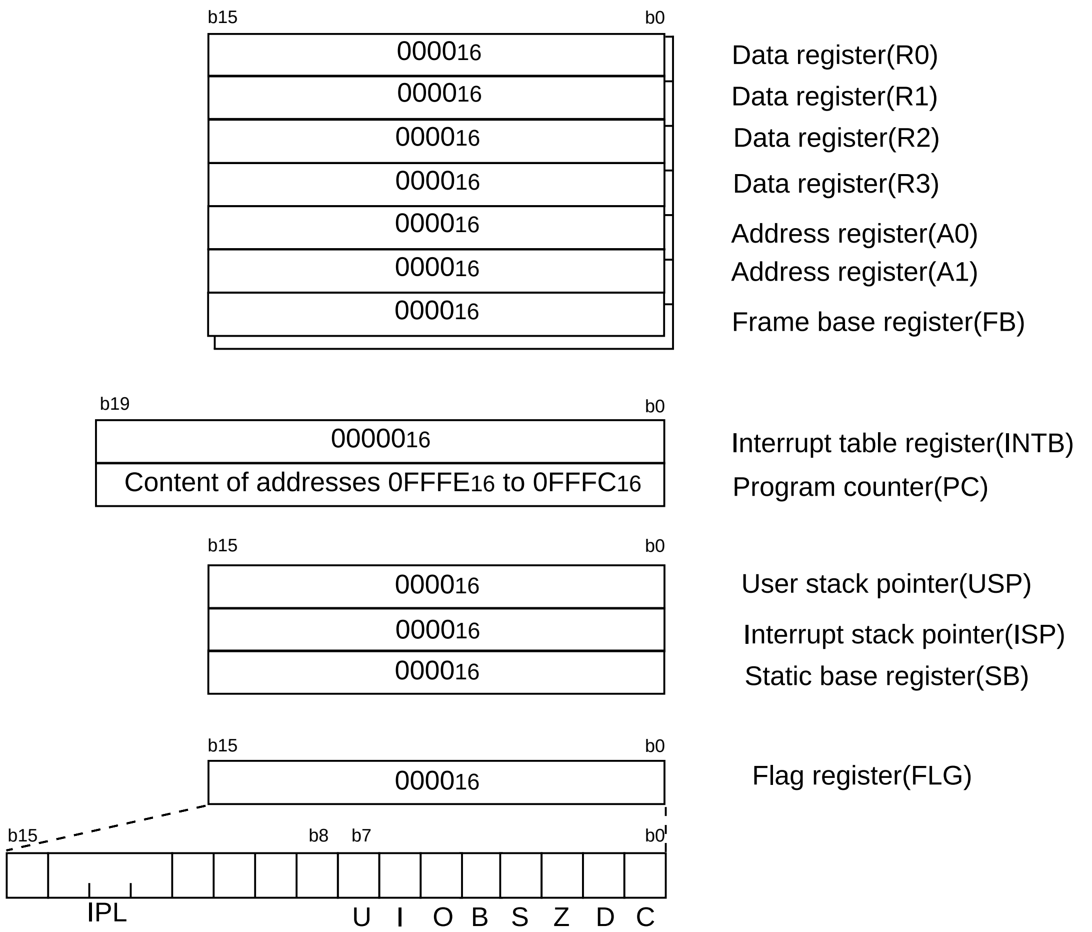


Figure 5.1 CPU Register Status After Reset

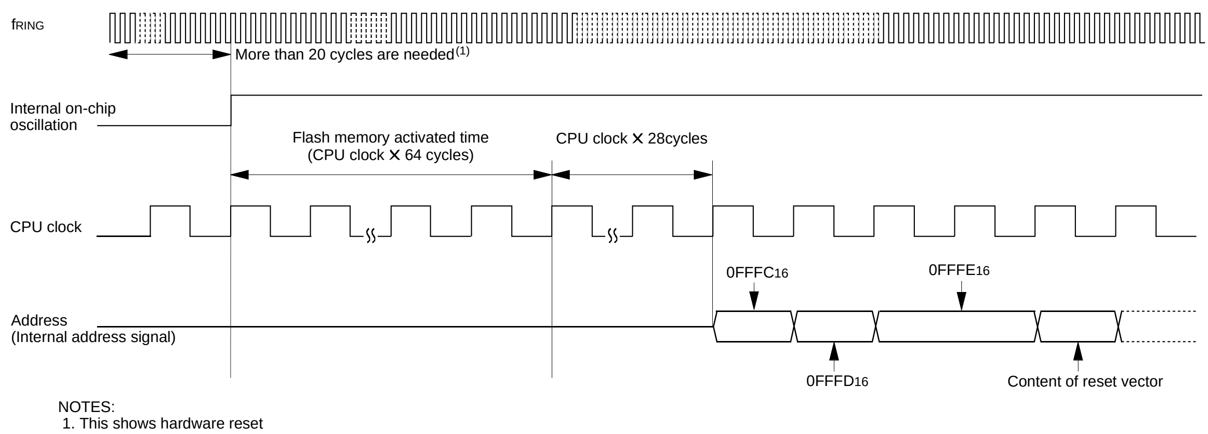


Figure 5.2 Reset Sequence

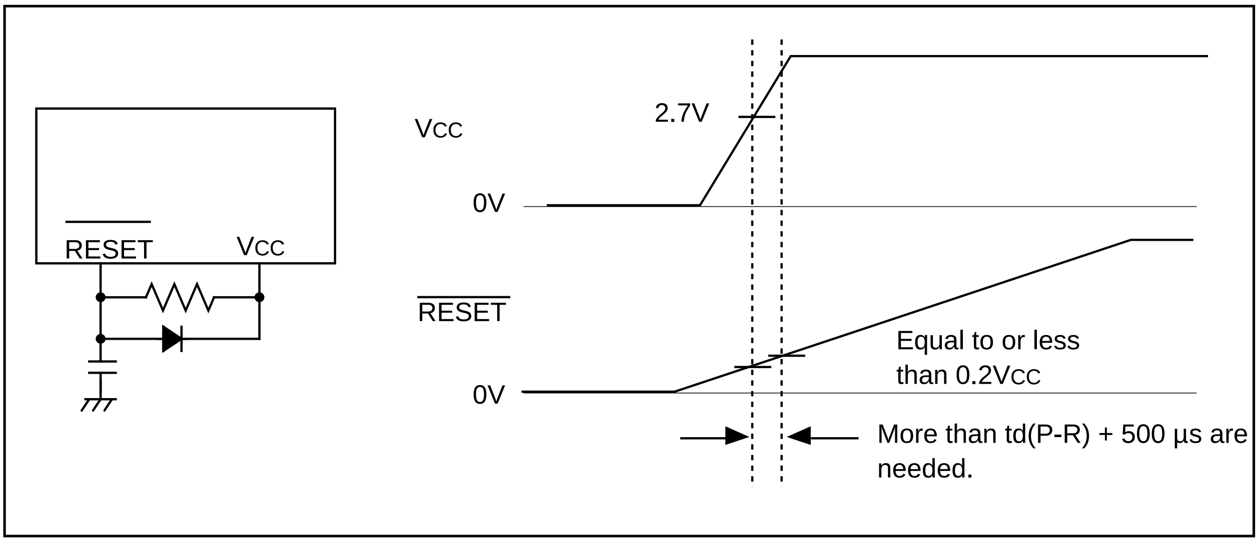


Figure 5.3 Example Reset Circuit

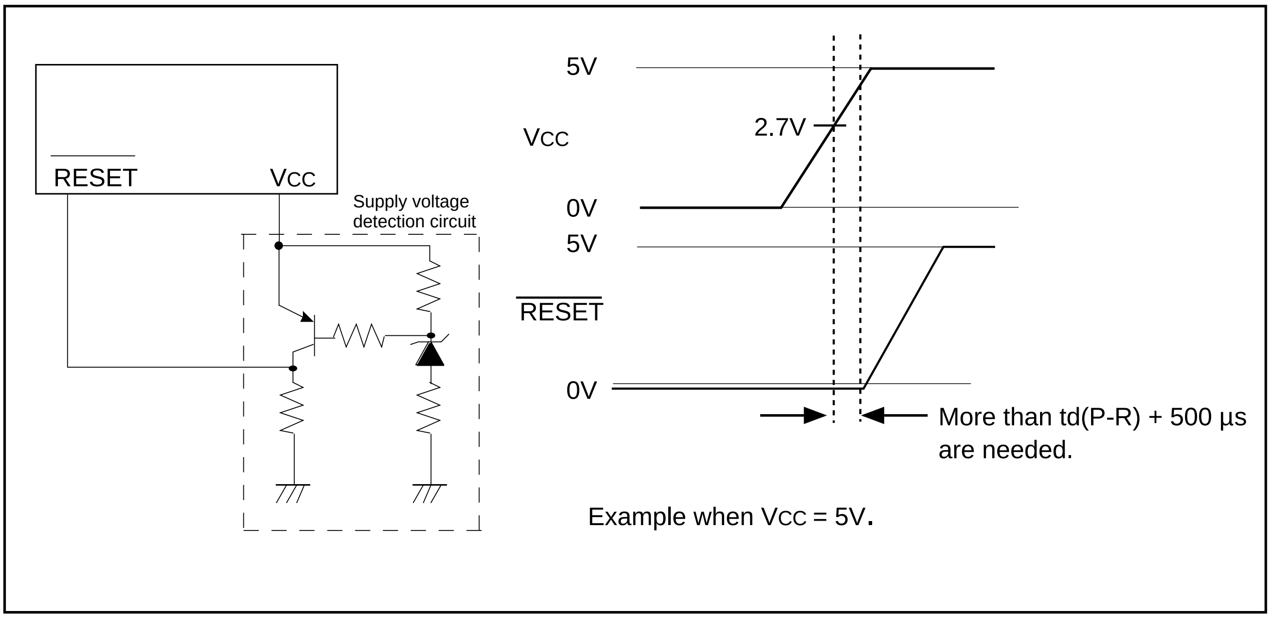


Figure 5.4 Example Reset Circuit (Voltage Check Circuit)

6. Clock Generation Circuit

The clock generation circuit contains two oscillator circuits as follows:

- Main clock oscillation circuit
- On-chip oscillator (with oscillation stop detection function)

Table 6.1 lists the clock generation circuit specifications. Figure 6.1 shows the clock generation circuit. Figures 6.2 and 6.3 show the clock-related registers.

Table 6.1 Clock Generation Circuit Specifications

Item	Main clock oscillation circuit	On-chip oscillator
Use of clock	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock sources when the main clock stops oscillating	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock sources when the main clock stops oscillating
Clock frequency	0 to 16 MHz	About 125 kHz
Usable oscillator	• Ceramic resonator • Crystal oscillator	———
Pins to connect oscillator	XIN, XOUT(1)	(Note 1)
Oscillation starts and stops	Present	Present
Oscillator status after reset	Stopped	Oscillating
Other	Externally derived clock can be input	———

NOTES:
1. Can be used as P46 and P47 when the on-chip oscillator clock is used for CPU clock while the main clock oscillation circuit is not used.

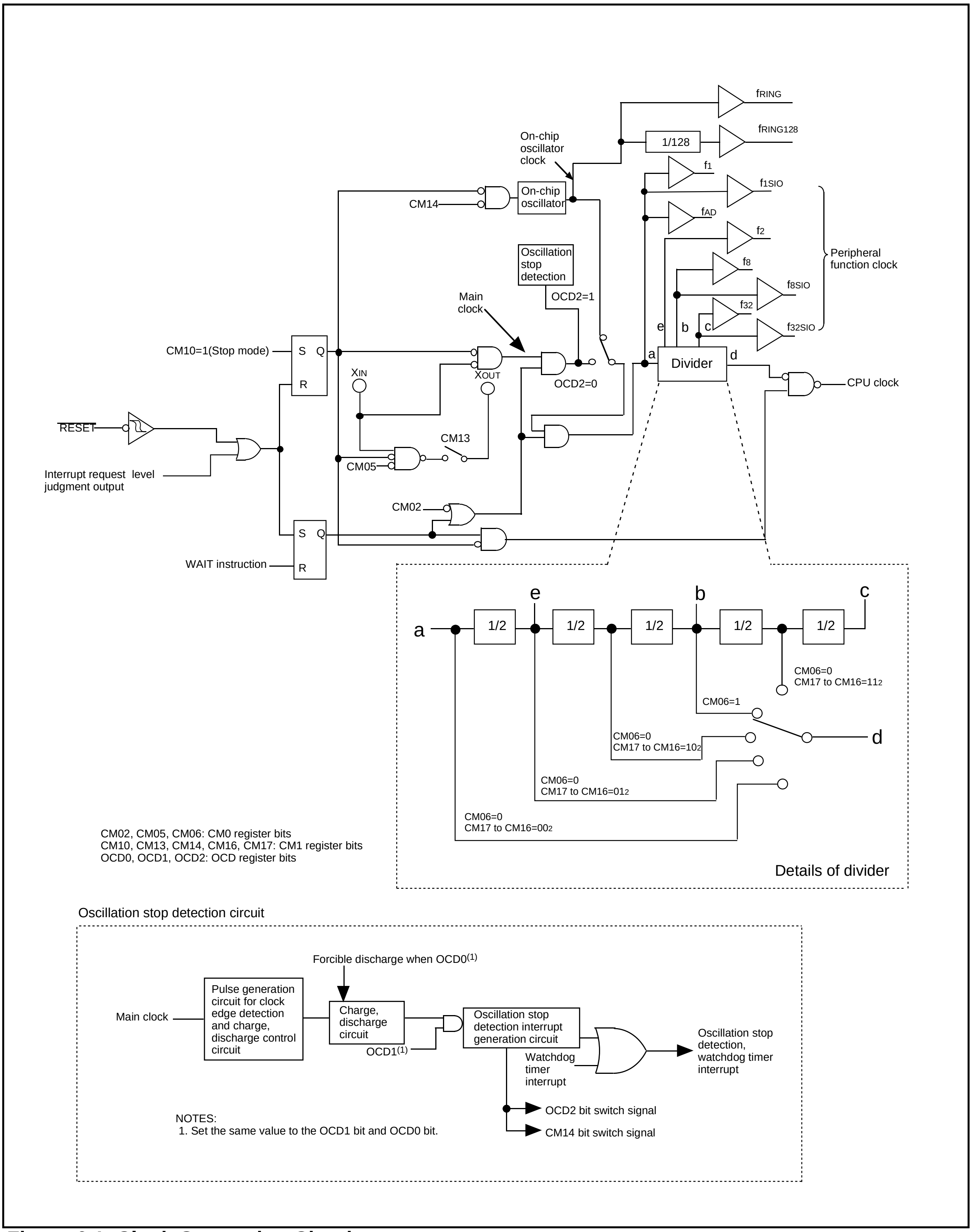


Figure 6.1 Clock Generation Circuit

System clock control register 0[1]

b7	b6	b5	b4	b3	b2	b1	b0
0			0	1		0	0

Symbol	Address	After reset
CM0	0006_{16}	68_{16}

Bit symbol	Bit name	Function	RW
— (b1-b0)	Reserved bit	Set to “0”	RW
CM02	WAIT peripheral function clock stop bit	0 : Do not stop peripheral function clock in wait mode 1 : Stop peripheral function clock in wait mode	RW
— (b3)	Reserved bit	Set to “1”	RW
— (b4)	Reserved bit	Set to “0”	RW
CM05	Main clock (XIN-XOUT)stop bit[2, 4]	0 : On 1 : Off[3]	RW
CM06	CPU clock division select bit 0[5]	0 : CM16 and CM17 valid 1 : Divide-by-8 mode	RW
— (b7)	Reserved bit	Set to “0”	RW

NOTES:
1. Set the PRC0 bit of PRCR register to “1” (write enable) before writing to this register.
2. The CM05 bit is provided to stop the main clock when the on-chip oscillator mode is selected. This bit cannot be used for detection as to whether the main clock stopped or not. To stop the main clock, the following setting is required:
   (1) Set the OCD0 and OCD1 bits in the OCD register to “00_2” (disable oscillation stop detection function).
   (2) Set the OCD2 bit to “1” (select on-chip oscillator clock).
3. Set the CM05 bit to “1” (main clock stops) and the CM13 bit in the CM1 register to “1” (XIN-XOUT pin) when the external clock is input.
4. When the CM05 bit is set to “1” (main clock stop), $P4_6$ and $P4_7$ can be used as input ports.
5. When entering stop mode from high or middle speed mode, the CM06 bit is set to “1” (divide-by-8 mode).

System clock control register 1[1]

b7	b6	b5	b4	b3	b2	b1	b0
					0	0	

Symbol	Address	After reset
CM1	0007_{16}	20_{16}

Bit symbol	Bit name	Function	RW
CM10	All clock stop control bit[4, 6]	0 : Clock on 1 : All clocks off (stop mode)	RW
— (b1)	Reserved bit	Set to “0”	RW
— (b2)	Reserved bit	Set to “0”	RW
CM13	Port XIN-XOUT switch bit[6]	0 : Input port $P4_6$, $P4_7$ 1 : XIN-XOUT pin	RW
CM14	On-chip oscillation stop bit	0 : On-chip oscillator on 1 : On-chip oscillator off[5]	RW
CM15	XIN-XOUT drive capacity select bit[2]	0 : LOW 1 : HIGH	RW
CM16	CPU clock division select bit 1[3]	b7 b6 0 0 : No division mode 0 1 : Division by 2 mode 1 0 : Division by 4 mode 1 1 : Division by 16 mode	RW
CM17			RW

NOTES:
1. Write to this register after setting the PRC0 bit of PRCR register to “1” (write enable).
2. When entering stop mode from high or middle speed mode, the CM15 bit is set to “1” (drive capacity high).
3. Effective when the CM06 bit is “0” (CM16 and CM17 bits enable).
4. If the CM10 bit is “1” (stop mode), the internal feedback resistor becomes ineffective.
5. The CM14 bit can be set to “1” (on-chip oscillator off) if the OCD2 bit=0 (selecting main clock). When the OCD2 bit is set to “1” (selecting on-chip oscillator clock), the CM14 bit is set to “0” (on-chip oscillator on). This bit remains unchanged when “1” is written.
6. When the CM10 bit is set to “1” (stop mode) or the CM05 bit in the CM0 register to “1” (main clock stops) and the CM13 bit is set to “1” (XIN-XOUT pin), the XOUT ($P4_7$) pin is held “H”.
   When the CM13 bit is set to “0” (input port $P4_6$, $P4_7$), the $P4_7$ is in input state.

Figure 6.2 CM0 Register and CM1 Register

Oscillation stop detection register(1)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0				

Symbol OCD — Address 000C16 — After reset 0416

Bit symbol	Bit name	Function	RW
OCD0	Oscillation stop detection enable bit	b1 b0 0 0: The function is disabled(4) 0 1: Avoid this setting 1 0: Avoid this setting 1 1: The function is enabled(7)	RW
OCD1			
OCD2	System clock select bit(6)	0: Select main clock(7) 1: Select on-chip oscillator clock(2)	RW
OCD3	Clock monitor bit(3, 5)	0: Main clock on 1: Main clock off	RO
— (b7-b4)	Reserved bit	Set to "0"	RW

NOTES:
1. Set the PRC0 bit in the PRCR register to “1” (write enable) before rewriting this register.
2. The OCD2 bit is set to “1” (selecting on-chip oscillator clock) automatically if a main clock oscillation stop is detected while the OCD1 to OCD0 bits are set to “112” (oscillation stop detection function disabled). If the OCD3 bit is set to “1” (main clock stop), the OCD2 bit remains unchanged when trying to write “0” (selecting main clock).
3. The OCD3 bit is enabled when the OCD1 to OCD0 bits are set to “112” (oscillation stop detection function enabled).
4. The OCD1 to OCD0 bits must be set to “002” (oscillation stop detection function disabled)before entering stop mode or on-chip oscillator mode (main clock stops).
5. The OCD3 bit remains set to “0” (main clock on) if the OCD1 to OCD0 bits are set to “002”.
6. The CM14 bit goes to “0” (on-chip oscillator on) if the OCD2 bit is set to “1” (selecting on-chip oscillator clock).
7. Refer to Figure 6.6 “switching clock source from on-chip oscillator to main clock” for the switching procedure when the main clock re-oscillates after detecting an oscillation stop.

Figure 6.3 OCD Register

The following describes the clocks generated by the clock generation circuit.

6.1 Main Clock

This clock is supplied by a main clock oscillation circuit. This clock is used as the clock source for the CPU and peripheral function clocks. The main clock oscillator circuit is configured by connecting a resonator between the X_{IN} and X_{OUT} pins. The main clock oscillator circuit contains a feedback resistor, which is disconnected from the oscillator circuit during stop mode in order to reduce the amount of power consumed in the chip. The main clock oscillator circuit may also be configured by feeding an externally generated clock to the X_{IN} pin. Figure 6.4 shows examples of main clock connection circuit. During reset and after reset, the main clock is turned off.

The main clock starts oscillating when the CM05 bit in the CM0 register is set to “0” (main clock on) after setting the CM13 bit in the CM1 register to “1” (X_{IN}- X_{OUT} pin).

To use the main clock for the CPU clock, set the OCD2 bit in the OCD register to “0” (selecting main clock) after the main clock becomes oscillating stably.

The power consumption can be reduced by setting the CM05 bit in the CM0 register to “1” (main clock off) if the OCD2 bit is set to “1” (selecting on-chip oscillator clock).

Note that if an externally generated clock is fed into the X_{IN} pin, the main clock cannot be turned off by setting the CM05 bit to “1”. If necessary, use an external circuit to turn off the clock.

During stop mode, all clocks including the main clock are turned off. Refer to Section 6.3, “Power Control.”

NOTES:
1. Insert a damping resistor if required. The resistance will vary depending on the oscillator and the oscillation drive capacity setting. Use the value recommended by the maker of the oscillator.
When the oscillation drive capacity is set to low, check that oscillation is stable. Also, if the oscillator manufacturer's data sheet specifies that a feedback resistor be added external to the chip, insert a feedback resistor between X_{IN} and X_{OUT} following the instruction.

Figure 6.4 Examples of Main Clock Connection Circuit

6.2 On-Chip Oscillator Clock

This clock, approximately 125 kHz, is supplied by a on-chip oscillator. This clock is used as the clock source for the CPU clock, peripheral function clock, f_{RING}, and $f_{RING128}$.

After reset, the on-chip oscillator clock divided by 8 is selected for the CPU clock.

To use the main clock for the CPU clock, set the OCD2 in the OCD register to “0” (selecting main clock) after the main clock becomes oscillating stably. If the main clock stops oscillating when the OCD1 to OCD0 bits in the OCD register is “11_2” (oscillation stop detection function enabled), the on-chip oscillator automatically starts operating, supplying the necessary clock for the microcomputer.

The frequency of the on-chip oscillator varies depending on the supply voltage and the operation ambient temperature. The application products must be designed with sufficient margin for the frequency change.

6.3 CPU Clock and Peripheral Function Clock

There are two types of clocks: CPU clock to operate the CPU and peripheral function clock to operate the peripheral functions. Also refer to “Figure 6.1 Clock Generating Circuit”.

6.3.1 CPU Clock

This is an operating clock for the CPU and watchdog timer.

The clock source for the CPU clock can be chosen to be the main clock or on-chip oscillator clock.

The selected clock source can be divided by 1 (undivided), 2, 4, 8 or 16 to produce the CPU clock. Use the CM06 bit in the CM0 register and the CM17 to CM16 bits in the CM1 register to select the divide-by-n value.

After reset, the low-speed on-chip oscillator clock divided by 8 provides the CPU clock.

Note that when entering stop mode from high or middle speed mode, the CM06 bit is set to “1” (divide-by-8 mode).

6.3.2 Peripheral Function Clock (f_1, f_2, f_8, f_{32}, f_{AD}, f_{1SIO}, f_{8SIO}, f_{32SIO})

These are operating clocks for the peripheral functions.

Of these, fi (i=1, 2, 8, 32) is derived from the main clock or on-chip oscillator clock by dividing them by i. The clock fi is used for timers X, Y, Z and C.

The clock f_{jSIO} (j=1, 8, 32) is derived from the main clock or on-chip oscillator clock by dividing them by j. The clock f_{jSIO} is used for serial interface.

The f_{AD} clock is produced from the main clock is used for the A/D converter.

When the WAIT instruction is executed after setting the CM02 bit in the CM0 register to “1” (peripheral function clock turned off during wait mode), the clocks fi, f_{jSIO}, and f_{AD} are turned off.

6.3.3 f_{RING} and $f_{RING128}$

These are operating clocks for the peripheral functions.

The f_{RING} runs at the same frequency as the on-chip oscillator, and can be used as the source for the timer Y. The $f_{RING128}$ is derived from the f_{RING} by dividing it by 128, and can used for Timer C.

When the WAIT instruction is executed, the clocks f_{RING} and $f_{RING128}$ are not turned off.

6.4 Power Control

There are three power control modes. All modes other than wait and stop modes are referred to as normal operation mode.

6.4.1 Normal Operation Mode

Normal operation mode is further classified into three modes.

In normal operation mode, because the CPU clock and the peripheral function clocks both are on, the CPU and the peripheral functions are operating. Power control is exercised by controlling the CPU clock frequency. The higher the CPU clock frequency, the greater the processing capability. The lower the CPU clock frequency, the smaller the power consumption in the chip. If the unnecessary oscillator circuits are turned off, the power consumption is further reduced.

Before the clock sources for the CPU clock can be switched over, the new clock source to which switched must be oscillating stably. If the new clock source is the main clock, allow a sufficient wait time in a program until it becomes oscillating stably.

- **High-speed Mode**

  The main clock divided by 1 undivided provides the CPU clock. If the CM14 bit is set to “0” (on-chip oscillator on), the f_{RING} is used as the count source for timer Y.

- **Medium-speed Mode**

  The main clock divided by 2, 4, 8 or 16 provides the CPU clock. If the CM14 bit is set to “0” (on-chip oscillator on), the f_{RING} is used as the count source for Timer Y.

- **On-Chip Oscillator Mode**

  The on-chip oscillator clock divided by 1 (undivided), 2, 4, 8 or 16 provides the CPU clock. The on-chip oscillator clock is also the clock source for the peripheral function clocks.

Table 6.2 Setting Clock Related Bit and Modes

Modes		OCD register	CM1 register		CM0 register	
		OCD2	CM17, CM16	CM13	CM06	CM05
High-speed mode		0	00_2	1	0	0
Medium-speed mode	divided by 2	0	01_2	1	0	0
	divided by 4	0	10_2	1	0	0
	divided by 8	0	—	1	1	0
	divided by 16	0	11_2	1	0	0
On-chip oscillator mode	no division	1	00_2	—	0	0 or 1
	divided by 2	1	01_2	—	0	0 or 1
	divided by 4	1	10_2	—	0	0 or 1
	divided by 8	1	—	—	1	0 or 1
	divided by 16	1	11_2	—	0	0 or 1

6.4.2 Wait Mode

In wait mode, the CPU clock is turned off, so are the CPU and the watchdog timer because both are operated by the CPU clock. Because the main clock and on-chip oscillator clock both are on, the peripheral functions using these clocks keep operating.

• Peripheral Function Clock Stop Function

If the CM02 bit is "1" (peripheral function clocks turned off during wait mode), the f_1, f_2, f_8, f_{32}, f_{1SIO}, f_{8SIO}, f_{32SIO}, and f_{AD} clocks are turned off when in wait mode, with the power consumption reduced that much.

• Entering Wait Mode

The microcomputer is placed into wait mode by executing the WAIT instruction.

• Pin Status During Wait Mode

The status before wait mode is retained.

• Exiting Wait Mode

The microcomputer is moved out of wait mode by a hardware reset or peripheral function interrupt. When using a hardware reset to exit wait mode, set the ILVL2 to ILVL0 bits for the peripheral function interrupts to "000_2" (interrupts disabled) before executing the WAIT instruction.

The peripheral function interrupts are affected by the CM02 bit. If CM02 bit is "0" (peripheral function clocks not turned off during wait mode), all peripheral function interrupts can be used to exit wait mode. If CM02 bit is "1" (peripheral function clocks turned off during wait mode), the peripheral functions using the peripheral function clocks stop operating, so that only the peripheral functions clocked by external signals can be used to exit wait mode.

Table 6. 3 lists the interrupts to exit wait mode and the usage conditions.

When using a peripheral function interrupt to exit wait mode, set up the following before executing the WAIT instruction.

1. In the ILVL2 to ILVL0 bits in the interrupt control register, set the interrupt priority level of the peripheral function interrupt to be used to exit wait mode.
   Also, for all of the peripheral function interrupts not used to exit wait mode, set the ILVL2 to ILVL0 bits to "000_2" (interrupt disable).
2. Set the I flag to "1".
3. Enable the peripheral function whose interrupt is to be used to exit wait mode.
   In this case, when an interrupt request is generated and the CPU clock is thereby turned on, an interrupt sequence is executed.

The CPU clock turned on when exiting wait mode by a peripheral function interrupt is the same CPU clock that was on when the WAIT instruction was executed.

Table 6.3 Interrupts to Exit Wait Mode and Usage Conditions

Interrupt	CM02=0	CM02=1
Serial interface interrupt	Can be used when operating with internal or external clock	Can be used when operating with external clock
Key input interrupt	Can be used	Can be used
A/D conversion interrupt	Can be used in one-shot mode	— (Do not use)
Timer X interrupt	Can be used in all modes	Can be used in event counter mode
Timer Y interrupt	Can be used in all modes	Can be used when counting inputs from CNTR1 pin in timer mode
Timer Z interrupt	Can be used in all modes	— (Do not use)
Timer C interrupt	Can be used in all modes	— (Do not use)
$\overline{INT}$ interrupt	Can be used	Can be used ($\overline{INT0}$ and $\overline{INT3}$ can be used if there is no filter.
Voltage detection interrupt	Can be used	Can be used
Oscillation stop detection interrupt	Can be used	— (Do not use)

6.4.3 Stop Mode

In stop mode, all oscillator circuits are turned off, so are the CPU clock and the peripheral function clocks. Therefore, the CPU and the peripheral functions clocked by these clocks stop operating. The least amount of power is consumed in this mode. If the voltage applied to Vcc pin is V_{RAM} or more, the internal RAM is retained.

However, the peripheral functions clocked by external signals keep operating. The following interrupts can be used to exit stop mode.

- Key interrupt
- $\overline{INT0}$ to $\overline{INT2}$ interrupts ($\overline{INT0}$ can be used only when there is no filter.)
- Timer X interrupt (when counting external pulses in event counter mode)
- Timer Y interrupt (when counting inputs from CNTR1 pin in timer mode)
- Serial interface interrupt (when external clock is selected)

• Entering Stop Mode

The microcomputer is placed into stop mode by setting the CM10 bit of CM1 register to “1” (all clocks turned off). At the same time, the CM06 bit of CM0 register is set to “1” (divide-by-8 mode) and the CM15 bit of CM10 register is set to “1” (main clock oscillator circuit drive capacity high).

Before entering stop mode, set the OCD1 to OCD0 bits to “00_2” (oscillation stop detection function disable).

• Pin Status in Stop Mode

The status before wait mode is retained.

However, the X_{OUT}($P4_7$) pin is held “H” when the CM13 bit in the CM1 register is set to “1” (X_{IN}-X_{OUT} pin). The $P4_7$(X_{OUT}) is in input state when the CM13 bit is set to “0” (input port $P4_6$, $P4_7$).

• Exiting Stop Mode

The microcomputer is moved out of stop mode by a hardware reset or peripheral function interrupt.

When using a hardware reset to exit stop mode, set the ILVL2 to ILVL0 bits for the peripheral function interrupts to “000_2” (interrupts disabled) before setting the CM10 bit to “1”.

When using a peripheral function interrupt to exit stop mode, set up the following before setting the CM10 bit to “1”.

1. In the ILVL2 to ILVL0 bits in the interrupt control register, set the interrupt priority level of the peripheral function interrupt to be used to exit stop mode.
   Also, for all of the peripheral function interrupts not used to exit stop mode, set the ILVL2 to ILVL0 bits to “000_2”.
2. Set the I flag to “1”.
3. Enable the peripheral function whose interrupt is to be used to exit stop mode.
   In this case, when an interrupt request is generated and the CPU clock is thereby turned on, an interrupt sequence is executed.

The main clock divided by 8 of the clock which is used right before stop mode is used for the CPU clock when exiting stop mode by a peripheral function interrupt.

Figure 6.5 shows the state transition of power control.

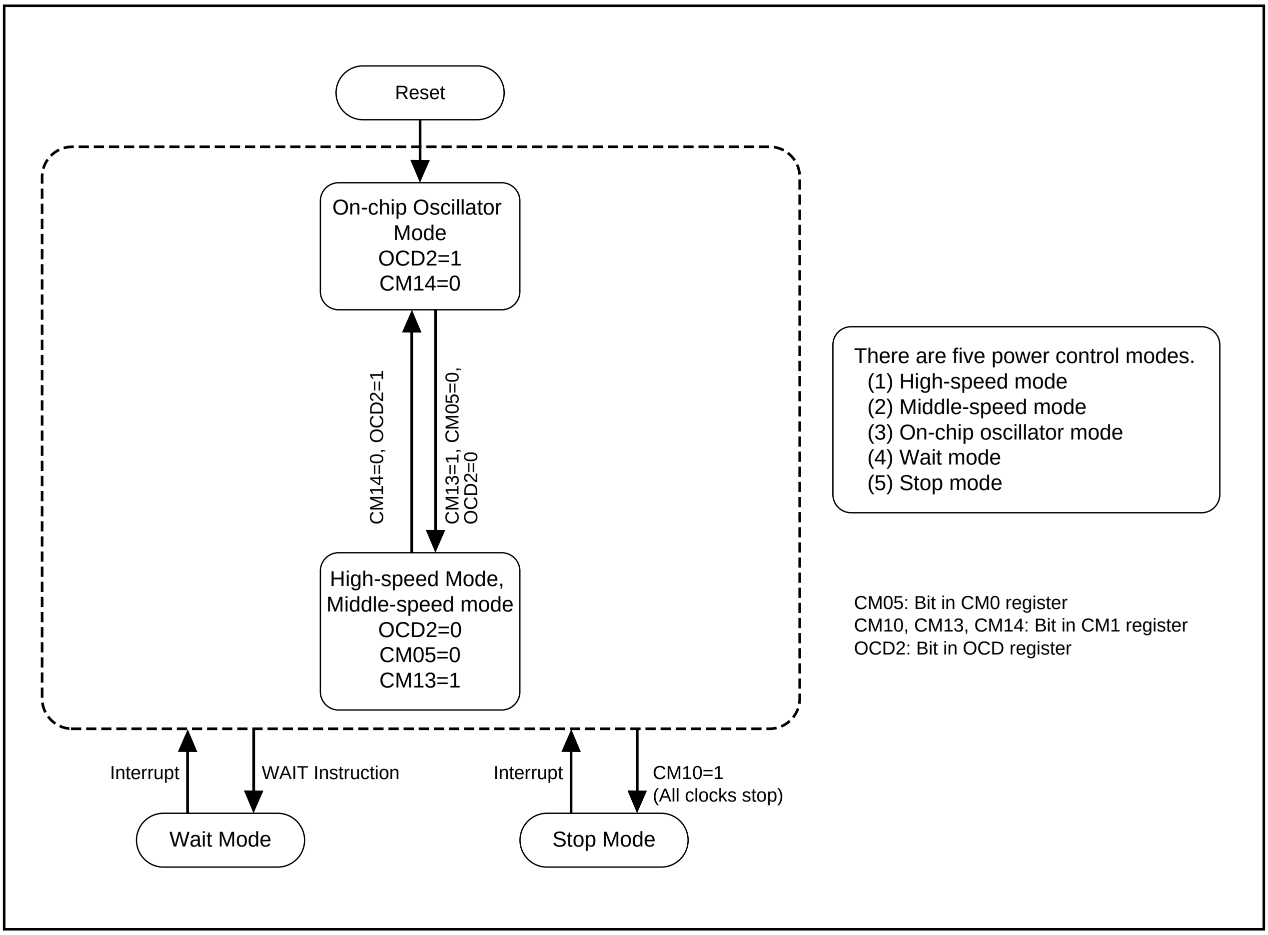


Figure 6.5 State Transition of Power Control

6.5 Oscillation Stop Detection Function

The oscillation stop detection function is such that main clock oscillation circuit stop is detected. The oscillation stop detection function can be enabled and disabled by the OCD1 to OCD0 bits in the OCD register.
Table 6.4 lists the specifications of the oscillation stop detection function.

Where the main clock corresponds to the CPU clock source and the OCD1 to OCD0 bits are "11_2" (oscillation stop detection function enabled), the system is placed in the following state if the main clock comes to a halt:

- The on-chip oscillator starts oscillation, and the on-chip oscillator clock becomes the clock source for CPU clock and peripheral functions in place of the main clock
- OCD register OCD2 bit = 1 (selecting on-chip oscillator clock)
- OCD register OCD3 bit = 1 (main clock stopped)
- CM1 register CM14 bit = 0 (on-chip oscillator oscillating)
- Oscillation stop detection interrupt request occurs

Table 6.4 Oscillation Stop Detection Function Specifications

Item	Specification
Oscillation stop detectable clock and frequency bandwidth	$f(X_{IN}) \geq 2$ MHz
Enabling condition for oscillation stop detection function	Set OCD1 to OCD0 bits to "11_2" (oscillation stop detection function enabled)
Operation at oscillation stop detection	Oscillation stop detection interrupt occurs

6.5.1 How to Use Oscillation Stop Detection Function

- The oscillation stop detection interrupt shares the vector with the watchdog timer interrupt. If the oscillation stop detection and watchdog timer interrupts both are used, the interrupt factor must be determined. Table 6.5 shows to determine the interrupt factor with the oscillation stop detection interrupt and watchdog timer interrupt.
- Where the main clock re-oscillated after oscillation stop, the clock source for the CPU clock and peripheral functions must be switched to the main clock in the program.
  Figure 6.6 shows the procedure for switching the clock source from the on-chip oscillator to the main clock.
- To enter wait mode while using the oscillation stop detection function, set the CM02 bit to "0" (peripheral function clocks not turned off during wait mode).
- Since the oscillation stop detection function is provided in preparation for main clock stop due to external factors, set the OCD1 to OCD0 bits to "00_2" (oscillation stop detection function disabled) where the main clock is stopped or oscillated in the program, that is where the stop mode is selected or the CM05 bit is altered.
- This function cannot be used when the main clock frequency is below 2 MHz. Set the OCD1 to OCD0 bits to "00_2" (oscillation stop detection function disabled).

Table 6.5 Determination of Interrupt Factor of Oscillation Stop Detection or Watchdog Timer Interrupt)

Generated Interrupt Factor	Bit showing interrupt factor
Oscillation stop detection ((a) or (b))	(a) The OCD3 bit in the OCD register = 1 (b) The OCD1 to OCD0 bits in the OCD register = 11_2 and the OCD2 bit = 1

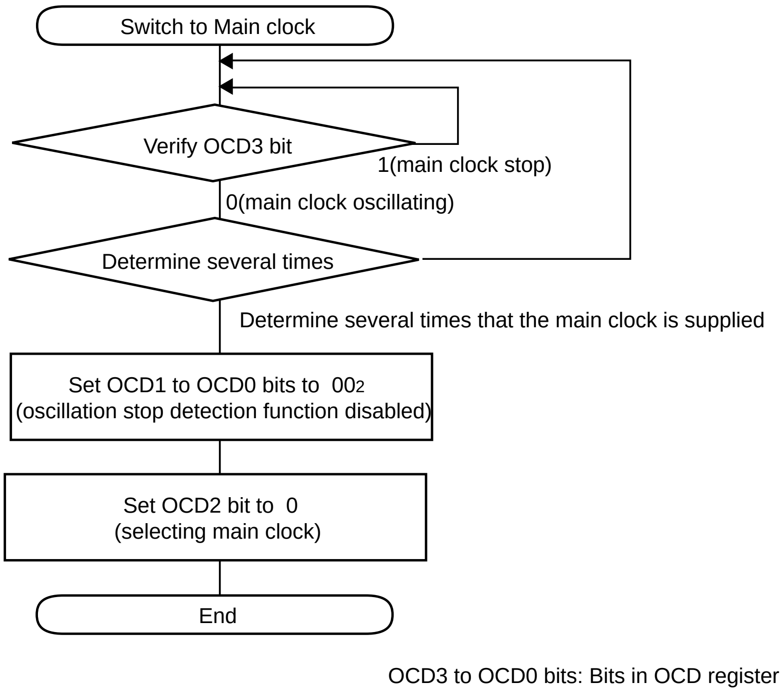


Figure 6.6 Switching Clock Source From On-Chip Oscillator to Main Clock

7. Protection

In the event that a program runs out of control, this function protects the important registers so that they will not be rewritten easily. Figure 7.1 shows the PRCR register. The following lists the registers protected by the PRCR register.

- Registers protected by PRC0 bit: CM0, CM1, and OCD registers
- Registers protected by PRC1 bit: PM0 and PM1 registers
- Registers protected by PRC2 bit: PD0 register

Set the PRC2 bit to “1” (write enabled) and then write to any address, and the PRC2 bit will be set to “0” (write protected). The registers protected by the PRC2 bit should be changed in the next instruction after setting the PRC2 bit to “1”. Make sure no interrupts will occur between the instruction in which the PRC2 bit is set to “1” and the next instruction. The PRC0 to PRC1 bits are not automatically set to “0” by writing to any address. They can only be set to “0” in a program.

Protect register

b7	b6	b5	b4	b3	b2	b1	b0
		0	0	0			

Symbol	Address	After reset
PRCR	$000A_{16}$	$00XXX000_2$

Bit symbol	Bit name	Function	RW
PRC0	Protect bit 0	Enable write to CM0, CM1, OCD registers 0 : Write protected 1 : Write enabled	RW
PRC1	Protect bit 1	Enable write to PM0, PM1 registers 0 : Write protected 1 : Write enabled	RW
PRC2	Protect bit 2	Enable write to PD0 register 0 : Write protected 1 : Write enabled[1]	RW
— (b5-b3)	Reserved bit	When write, must set to "0"	RW
— (b7-b6)	Reserved bit	When read, its content is “0”.	RO

NOTES:
1. The PRC2 bit is set to “0” by writing to any address after setting it to “1”. Other bits are not set to “0” by writing to any address, and must therefore be set to “0” in a program.

Figure 7.1 PRCR Register

8. Processor Mode

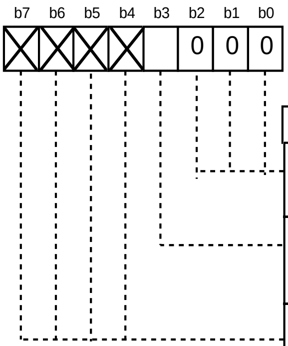
8.1 Types of Processor Mode

The processor mode is single-chip mode. Table 8.1 shows the features of the processor mode. Figure 8.1 shows the PM0 and PM1 register.

Table 8.1 Features of Processor Mode

Processor mode	Access space	Pins which are assigned I/O ports
Single-chip mode	SFR, internal RAM, internal ROM	All pins are I/O ports or peripheral function I/O pins

Processor mode register 0[(1)]

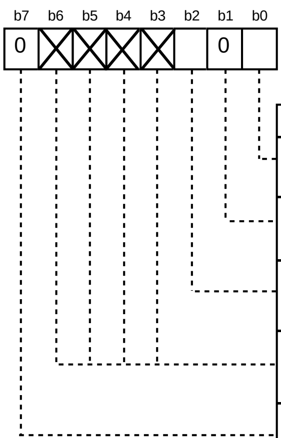


Symbol PM0 | Address 0004_{16} | After reset 00_{16}

Bit symbol	Bit name	Function	RW
— (b2-b0)	Reserved bit	Set to “0”	RW
PM03	Software reset bit	Setting this bit to “1” resets the microcomputer. When read, its content is “0”.	RW
— (b7-b4)	Nothing is assigned. When write, set to “0”. When read, its content is 0.		—

NOTES:
1. Set the PRC1 bit in the PRCR register to "1" (write enable) before writing to this register.

Processor mode register 1[(1)]



Symbol PM1 | Address 0005_{16} | After reset 00_{16}

Bit symbol	Bit name	Function	RW
PM10	Data area access enable bit	0 : Disabled 1 : Enabled	RW
— (b1)	Reserved bit	Set to “0”	RW
PM12	WDT interrupt/reset switch bit[(2)]	0 : Watchdog timer interrupt 1 : Watchdog timer reset[(2)]	RW
— (b6-b3)	Nothing is assigned. When write, set to “0”. When read, its content is 0.		—
— (b7)	Reserved bit	Set to “0”	RW

NOTES:
1. Set the PRC1 bit in the PRCR register to "1" (write enable) before writing to this register.
2. PM12 bit is set to “1” by writing a “1” in a program. (Writing a “0” has no effect.)

Figure 8.1 PM0 Register and PM1 Register

9. Bus

During access, the ROM/RAM and the SFR have different bus cycles. Table 9.1 shows bus cycles for access space.

The ROM/RAM and SFR are connected to the CPU through an 8-bit bus. When accessing in word (16 bits) units, these spaces are accessed twice in 8-bit units. Table 9.2 shows bus cycles in each access space.

Table 9.1 Bus Cycles for Access Space

Access space	Bus cycle
SFR/Data flash	2 CPU clock cycles
Program ROM/RAM	1 CPU clock cycles

Table 9.2 Access Unit and Bus Operation

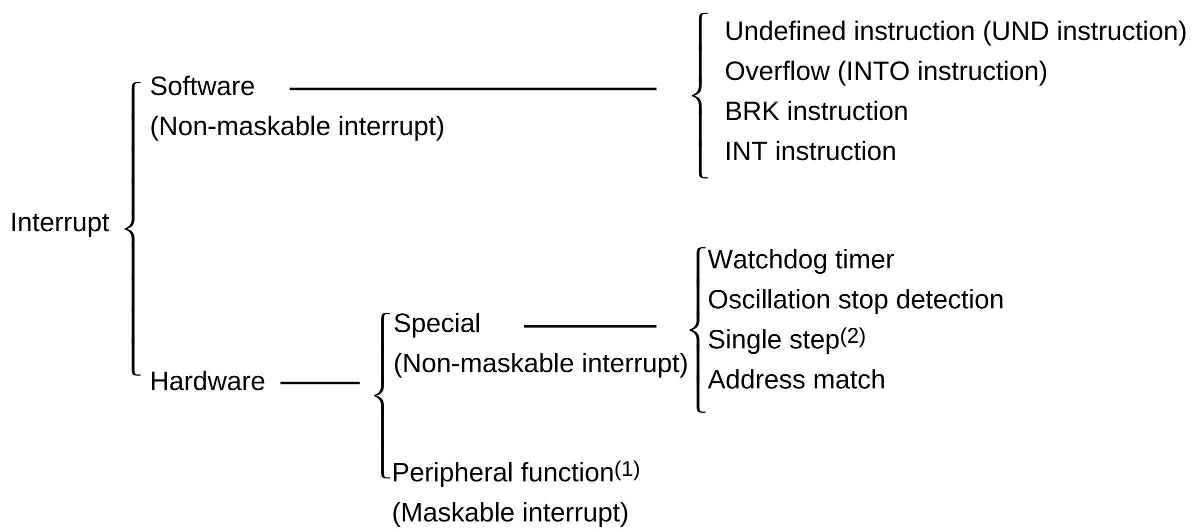
Space	SFR, Data flash	Program ROM/RAM
Even address byte access	CPU clock Address: Even Data: Data	CPU clock Address: Even Data: Data
Odd address byte access	CPU clock Address: Odd Data: Data	CPU clock Address: Odd Data: Data
Even address word access	CPU clock Address: Even, Even+1 Data: Data, Data	CPU clock Address: Even, Even+1 Data: Data, Data
Odd address word access	CPU clock Address: Odd, Odd+1 Data: Data, Data	CPU clock Address: Odd, Odd+1 Data: Data, Data

10. Interrupt

10.1 Interrupt Overview

10.1.1 Type of Interrupts

Figure 10.1 shows types of interrupts.



NOTES:

1. Peripheral function interrupts are generated by the peripheral functions built in the microcomputer system.
2. Avoid using this interrupt because this is a dedicated interrupt for development support tools only.

Figure 10.1 Interrupts

- Maskable Interrupt: An interrupt which can be enabled (disabled) by the interrupt enable flag (I flag) or whose interrupt priority **can be changed** by priority level.
- Non-maskable Interrupt: An interrupt which cannot be enabled (disabled) by the interrupt enable flag (I flag) or whose interrupt priority **cannot be changed** by priority level.

10.1.2 Software Interrupts

A software interrupt occurs when executing certain instructions. Software interrupts are non-maskable interrupts.

- **Undefined Instruction Interrupt**

  An undefined instruction interrupt occurs when executing the UND instruction.
- **Overflow Interrupt**

  An overflow interrupt occurs when executing the INTO instruction with the O flag set to "1" (the operation resulted in an overflow). The following are instructions whose O flag changes by arithmetic:

  ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, SUB
- **BRK Interrupt**

  A BRK interrupt occurs when executing the BRK instruction.
- **INT Instruction Interrupt**

  An INT instruction interrupt occurs when executing the INT instruction. Software interrupt numbers 0 to 63 can be specified for the INT instruction. Because software interrupt numbers 4 to 31 are assigned to peripheral function interrupts, the same interrupt routine as for peripheral function interrupts can be executed by executing the INT instruction.

  In software interrupt numbers 0 to 31, the U flag is saved to the stack during instruction execution and is cleared to "0" (ISP selected) before executing an interrupt sequence. The U flag is restored from the stack when returning from the interrupt routine. In software interrupt numbers 32 to 63, the U flag does not change state during instruction execution, and the SP then selected is used.

10.1.3 Hardware Interrupts

Hardware interrupts are classified into two types — special interrupts and peripheral function interrupts.

(1) Special Interrupts

Special interrupts are non-maskable interrupts.

- **Watchdog Timer Interrupt**

  Generated by the watchdog timer. Once a watchdog timer interrupt is generated, be sure to initialize the watchdog timer. For details about the watchdog timer, refer to Chapter 11, “Watchdog Timer.”

- **Oscillation Stop Detection Interrupt**

  Generated by the oscillation stop detection function. For details about the oscillation stop detection function, refer to Chapter 6, “Clock Generation Circuit.”

- **Single-step Interrupt**

  Do not normally use this interrupt because it is provided exclusively for use by development support tools.

- **Address Match Interrupt**

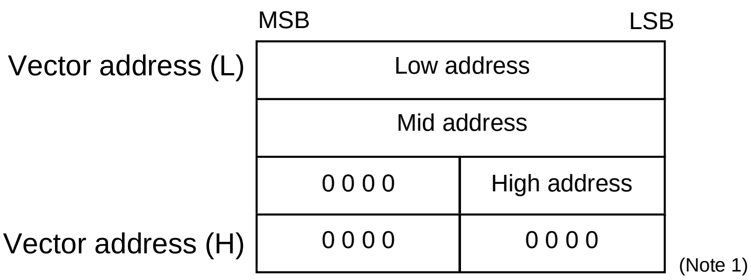
  An address match interrupt is generated immediately before executing the instruction at the address indicated by the RMAD0 to RMAD1 register that corresponds to one of the AIER register's AIER0 or AIER1 bit which is "1" (address match interrupt enabled). For details about the address match interrupt, refer to Section 10.4, “Address Match Interrupt.”

(2) Peripheral Function Interrupts

Peripheral function interrupts are maskable interrupts and generated by the microcomputer's internal functions. The interrupt factors for peripheral function interrupts are listed in Table 10.2. “Relocatable Vector Tables”. For details about the peripheral functions, refer to the description of each peripheral function in this manual.

10.1.4 Interrupts and Interrupt Vector

One interrupt vector consists of 4 bytes. Set the start address of each interrupt routine in the respective interrupt vectors. When an interrupt request is accepted, the CPU branches to the address set in the corresponding interrupt vector. Figure 10.2 shows the interrupt vector.



NOTES:
1. The OFS register is assigned to the $0FFFF_{16}$ address. Refer to "Figure11.2 OFS, WDC, WDTR and WDTS registers" for the OFS register details

Figure 10.2 Interrupt Vector

• Fixed Vector Tables

The fixed vector tables are allocated to the addresses from $0FFDC_{16}$ to $0FFFF_{16}$. Table 10.1 lists the fixed vector tables. In the flash memory version of microcomputer, the vector addresses (H) of fixed vectors are used by the ID code check function. For details, refer to Section 17.3, "Functions to Prevent Flash Memory from Rewriting."

Table 10.1 Fixed Vector Tables

Interrupt factor	Vector addresses Address (L) to address (H)	Remarks	Reference
Undefined instruction	$0FFDC_{16}$ to $0FFDF_{16}$	Interrupt on UND instruction	R8C/Tiny series software manual
Overflow	$0FFE0_{16}$ to $0FFE3_{16}$	Interrupt on INTO instruction	
BRK instruction	$0FFE4_{16}$ to $0FFE7_{16}$	If the contents of address $0FFE7_{16}$ is FF_{16}, program execution starts from the address shown by the vector in the relocatable vector table.	
Address match	$0FFE8_{16}$ to $0FFEB_{16}$		10.4 Address match interrupt
Single step(1)	$0FFEC_{16}$ to $0FFEF_{16}$		
Watchdog timer, oscillation stop detection	$0FFF0_{16}$ to $0FFF3_{16}$		11. Watchdog timer, 6. Clock generation circuit
(Reserved)	$0FFF4_{16}$ to $0FFF7_{16}$		
(Reserved)	$0FFF8_{16}$ to $0FFFB_{16}$		
Reset	$0FFFC_{16}$ to $0FFFF_{16}$		5. Reset

NOTES:
1. Do not normally use this interrupt because it is provided exclusively for use by development support tools.

• **Relocatable Vector Tables**

The 256 bytes beginning with the start address set in the INTB register comprise a relocatable vector table area. Table 10.2 lists interrupts and vector tables located in the relocatable vector table.

Table 10.2 Relocatable Vector Tables

Interrupt factor	Vector address[1] Address (L) to address (H)	Software interrupt number	Reference
BRK instruction[2]	+0 to +3 (0000_{16} to 0003_{16})	0	R8C/Tiny Series software manual
——— (Reserved)		1 to 12	
Key input	+52 to +55 (0034_{16} to 0037_{16})	13	10.3 Key input interrupt
A/D Conversion	+56 to +59 (0038_{16} to $003B_{16}$)	14	14. A/D converter
——— (Reserved)		15, 16	
UART0 transmit	+68 to +71 (0044_{16} to 0047_{16})	17	13. Serial interface
UART0 receive	+72 to +75 (0048_{16} to $004B_{16}$)	18	
UART1 transmit	+76 to +79 ($004C_{16}$ to $004F_{16}$)	19	
UART1 receive	+80 to +83 (0050_{16} to 0053_{16})	20	
$\overline{INT2}$	+84 to +87 (0054_{16} to 0057_{16})	21	10.2.3 $\overline{INT}$ interrupt
Timer X	+88 to +91 (0058_{16} to $005B_{16}$)	22	12.1 Timer X
Timer Y	+92 to +95 ($005C_{16}$ to $005F_{16}$)	23	12.2 Timer Y
Timer Z	+96 to +99 (0060_{16} to 0063_{16})	24	12.3 Timer Z
$\overline{INT1}$	+100 to +103 (0064_{16} to 0067_{16})	25	10.2.3 $\overline{INT1}$ interrupt
$\overline{INT3}$	+104 to +107 (0068_{16} to $006B_{16}$)	26	10.2.4 $\overline{INT3}$ interrupt
Timer C	+108 to +111 ($006C_{16}$ to $006F_{16}$)	27	12.4 Timer C
——— (Reserved)		28	
$\overline{INT0}$	+116 to +119 (0074_{16} to 0077_{16})	29	10.2.1 $\overline{INT0}$ interrupt
——— (Reserved)		30	
——— (Reserved)		31	
Software interrupt[2]	+128 to +131 (0080_{16} to 0083_{16}) to +252 to +255 ($00FC_{16}$ to $00FF_{16}$)	32 to 63	R8C/Tiny Series software manual

NOTES:
1. Address relative to address in INTB.
2. These interrupts cannot be disabled using the I flag.

10.1.5 Interrupt Control

The following describes how to enable/disable the maskable interrupts, and how to set the priority in which order they are accepted. What is explained here does not apply to nonmaskable interrupts.

Use the FLG register’s I flag, IPL, and each interrupt control register's ILVL2 to ILVL0 bits to enable/disable the maskable interrupts. Whether an interrupt is requested is indicated by the IR bit in each interrupt control register.

Figure 10.3 shows the interrupt control registers.

Interrupt control register(2)

Symbol	Address	After reset
KUPIC	004D16	XXXXX0002
ADIC	004E16	XXXXX0002
S0TIC, S1TIC	005116, 005316	XXXXX0002
S0RIC, S1RIC	005216, 005416	XXXXX0002
INT2IC	005516	XXXXX0002
TXIC	005616	XXXXX0002
TYIC	005716	XXXXX0002
TZIC	005816	XXXXX0002
INT1IC	005916	XXXXX0002
INT3IC	005A16	XXXXX0002
TCIC	005B16	XXXXX0002

b7 b6 b5 b4 b3 b2 b1 b0

Bit symbol	Bit name	Function	RW
ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0 : Level 0 (interrupt disabled) 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	RW
ILVL1			RW
ILVL2			RW
IR	Interrupt request bit	0 : Interrupt not requested 1 : Interrupt requested	RW(1)
— (b7-b4)	Nothing is assigned. When write, set to “0”. When read, its content is indeterminate.		—

b7 b6 b5 b4 b3 b2 b1 b0 (b5 = 0)

Symbol	Address	After reset
INT0IC	005D16	XX00X0002

Bit symbol	Bit name	Function	RW
ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0 : Level 0 (interrupt disabled) 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	RW
ILVL1			RW
ILVL2			RW
IR	Interrupt request bit	0: Interrupt not requested 1: Interrupt requested	RW(1)
POL	Polarity select bit(3, 4)	0 : Selects falling edge 1 : Selects rising edge	RW
(b5)	Reserved bit	Set to “0”	RW
— (b7-b6)	Nothing is assigned. When write, set to “0”. When read, its content is indeterminate.		—

NOTES:
1. Only "0" can be written to the IR bit. (Do not write "1").
2. To rewrite the interrupt control register, do so at a point that does not generate the interrupt request for that register. Refer to the paragraph 19.2.6 “Changing Interrupt Control Registers”.
3. If the INTOPL bit in the INTEN register is set to “1” (both edges), set the POL bit to "0 " (selecting falling edge).
4. The IR bit may be set to “1” (interrupt requested) when the POL bit is rewritten. Refer to the paragraph 19.2.5 “Changing Interrupt Factor”.

Figure 10.3 Interrupt Control Registers

• I Flag

The I flag enables or disables the maskable interrupt. Setting the I flag to “1” (enabled) enables the maskable interrupt. Setting the I flag to “0” (disabled) disables all maskable interrupts.

• IR Bit

The IR bit is set to “1” (interrupt requested) when an interrupt request is generated. Then, when the interrupt request is accepted and the CPU branches to the corresponding interrupt vector, the IR bit is cleared to “0” (= interrupt not requested).
The IR bit can be cleared to “0” in a program. Note that do not write “1” to this bit.

• ILVL2 to ILVL0 Bits and IPL

Interrupt priority levels can be set using the ILVL2 to ILVL0 bits.
Table 10.3 shows the settings of interrupt priority levels and Table 10.4 shows the interrupt priority levels enabled by the IPL.

The following are conditions under which an interrupt is accepted:

· I flag = 1
· IR bit = 1
· interrupt priority level > IPL

The I flag, IR bit, ILVL2 to ILVL0 bits and IPL are independent of each other. In no case do they affect one another.

Table 10.3 Settings of Interrupt Priority Levels

ILVL2 to ILVL0 bits	Interrupt priority level	Priority order
000_2	Level 0 (interrupt disabled)	—
001_2	Level 1	Lowest
010_2	Level 2	↓
011_2	Level 3	↓
100_2	Level 4	↓
101_2	Level 5	↓
110_2	Level 6	↓
111_2	Level 7	Highest

Table 10.4 Interrupt Priority Levels Enabled by IPL

IPL	Enabled interrupt priority levels
000_2	Interrupt levels 1 and above are enabled
001_2	Interrupt levels 2 and above are enabled
010_2	Interrupt levels 3 and above are enabled
011_2	Interrupt levels 4 and above are enabled
100_2	Interrupt levels 5 and above are enabled
101_2	Interrupt levels 6 and above are enabled
110_2	Interrupt levels 7 and above are enabled
111_2	All maskable interrupts are disabled

• Interrupt Sequence

An interrupt sequence — what are performed over a period from the instant an interrupt is accepted to the instant the interrupt routine is executed — is described here.

If an interrupt occurs during execution of an instruction, the processor determines its priority when the execution of the instruction is completed, and transfers control to the interrupt sequence from the next cycle. If an interrupt occurs during execution of either the SMOVB, SMOVF, SSTR or RMPA instruction, the processor temporarily suspends the instruction being executed, and transfers control to the interrupt sequence.

The CPU behavior during the interrupt sequence is described below. Figure 10.4 shows time required for executing the interrupt sequence.

(1) The CPU gets interrupt information (interrupt number and interrupt request priority level) by reading the address 00000_{16}. Then it clears the IR bit for the corresponding interrupt to "0" (interrupt not requested).

(2) The FLG register immediately before entering the interrupt sequence is saved to the CPU internal temporary register(1).

(3) The I, D and U flags in the FLG register become as follows:
The I flag is cleared to "0" (interrupts disabled).
The D flag is cleared to "0" (single-step interrupt disabled).
The U flag is cleared to "0" (ISP selected).
However, the U flag does not change state if an INT instruction for software interrupt numbers 32 to 63 is executed.

(4) The CPU's internal temporary register (1) is saved to the stack.

(5) The PC is saved to the stack.

(6) The interrupt priority level of the accepted interrupt is set in the IPL.

(7) The start address of the relevant interrupt routine set in the interrupt vector is stored in the PC.

After the interrupt sequence is completed, the processor resumes executing instructions from the start address of the interrupt routine.

NOTES:
1. This register cannot be used by user.

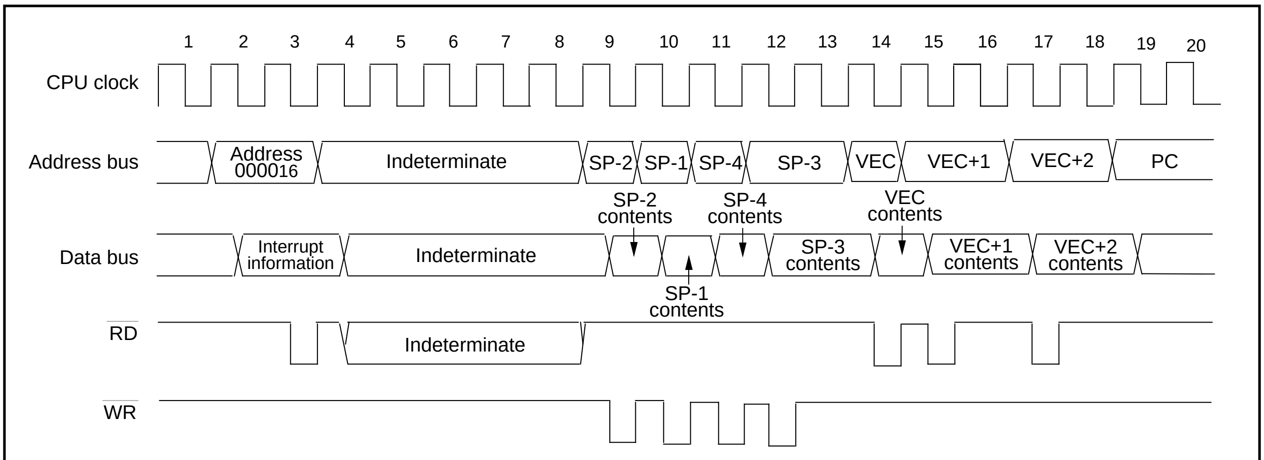
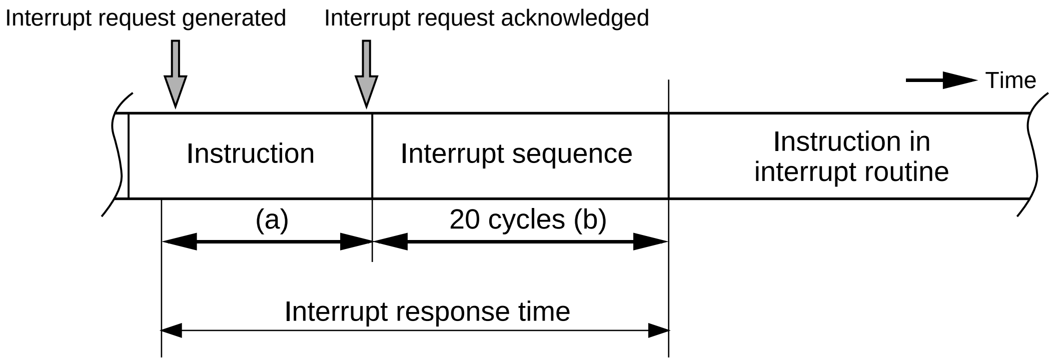


Figure 10.4 Time Required for Executing Interrupt Sequence

- **Interrupt Response Time**

Figure 10.5 shows the interrupt response time. The interrupt response or interrupt acknowledge time denotes a time from when an interrupt request is generated till when the first instruction in the interrupt routine is executed. Specifically, it consists of a time from when an interrupt request is generated till when the instruction then executing is completed (see #a in Figure 10.5) and a time during which the interrupt sequence is executed (20 cycles, see #b in Figure 10.5).



(a) A time from when an interrupt request is generated till when the instruction then executing is completed. The length of this time varies with the instruction being executed. The DIVX instruction requires the longest time, which is equal to 30 cycles (without wait state, the divisor being a register).
(b) 21 cycles for address match and single-step interrupts.

Figure 10.5 Interrupt Response Time

- **Variation of IPL when Interrupt Request is Accepted**

When a maskable interrupt request is accepted, the interrupt priority level of the accepted interrupt is set in the IPL.

When a software interrupt or special interrupt request is accepted, one of the interrupt priority levels listed in Table 10.5 is set in the IPL. Shown in Table 10.5 are the IPL values of software and special interrupts when they are accepted.

Table 10.5 IPL Level That Is Set to IPL When A Software or Special Interrupt Is Accepted

Interrupt factors	Level that is set to IPL
Watchdog timer, oscillation stop detection	7
Software, address match, single-step	Not changed

• Saving Registers

In the interrupt sequence, the FLG register and PC are saved to the stack.

At this time, the 4 high-order bits in the PC and the 4 high-order (IPL) and 8 low-order bits in the FLG register, 16 bits in total, are saved to the stack first. Next, the 16 low-order bits in the PC are saved.

Figure 10.6 shows the stack status before and after an interrupt request is accepted.

The other necessary registers must be saved in a program at the beginning of the interrupt routine. The PUSHM instruction can save several registers in the register bank being currently used(1) with a single instruction.

NOTES:

1. Selectable from registers R0, R1, R2, R3, A0, A1, SB, and FB.

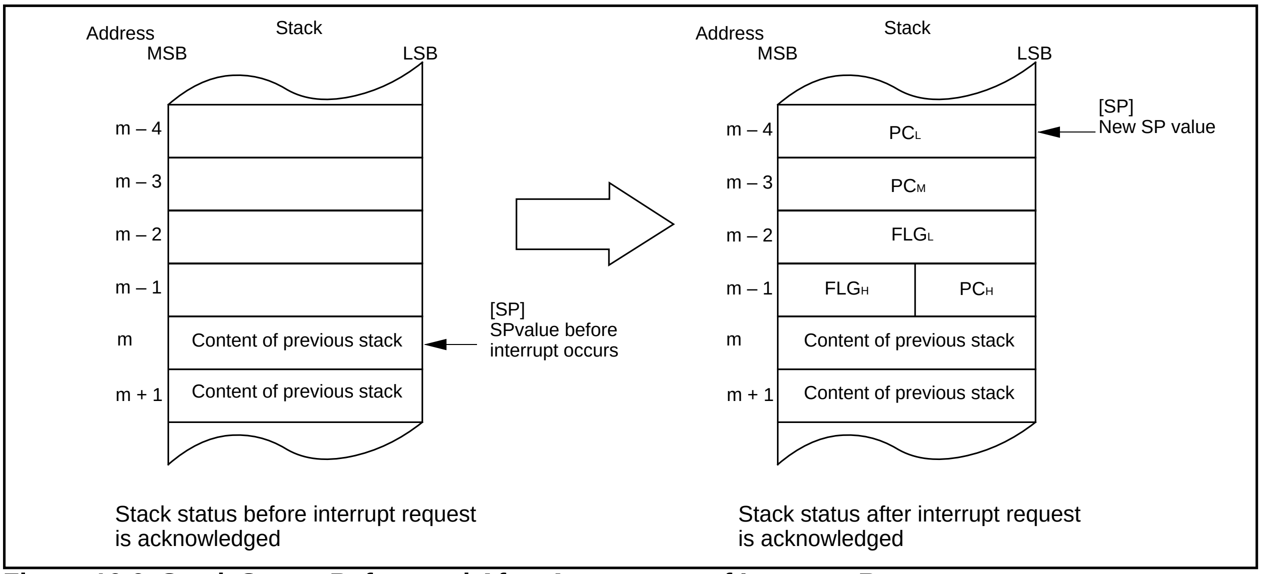
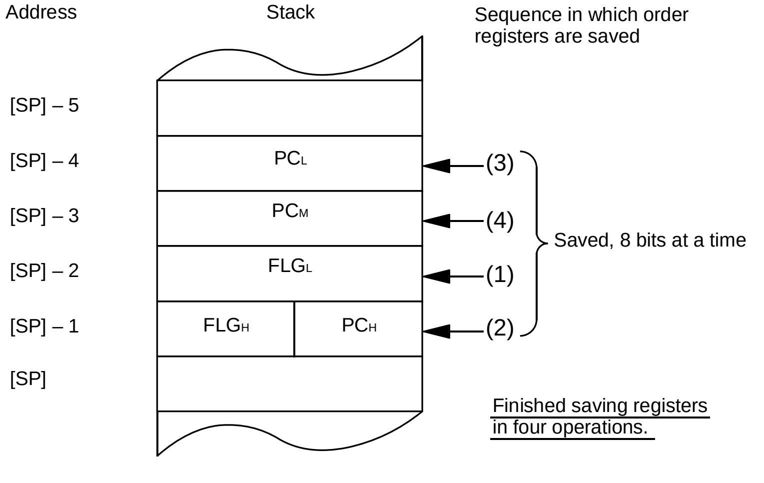


Figure 10.6 Stack Status Before and After Acceptance of Interrupt Request

The registers are saved in four steps, 8 bits at a time. Figure 10.7 shows the operation of the saving registers.

NOTES:

1. When any INT instruction in software numbers 32 to 63 has been executed, this is the SP indicated by the U flag. Otherwise, it is the ISP.



NOTES:

1. [SP] denotes the initial value of the SP when interrupt request is acknowledged. After registers are saved, the SP content is [SP] minus 4.

Figure 10.7 Operation of Saving Register

• **Returning from an Interrupt Routine**

The FLG register and PC in the state in which they were immediately before entering the interrupt sequence are restored from the stack by executing the REIT instruction at the end of the interrupt routine. Thereafter the CPU returns to the program which was being executed before accepting the interrupt request.

Return the other registers saved by a program within the interrupt routine using the POPM or similar instruction before executing the REIT instruction.

• **Interrupt Priority**

If two or more interrupt requests are generated while executing one instruction, the interrupt request that has the highest priority is accepted.

For maskable interrupts (peripheral functions), any desired priority level can be selected using the ILVL2 to ILVL0 bits. However, if two or more maskable interrupts have the same priority level, their interrupt priority is resolved by hardware, with the highest priority interrupt accepted.

The watchdog timer and other special interrupts have their priority levels set in hardware. Figure 10.8 shows the Hardware Interrupt Priority.

Software interrupts are not affected by the interrupt priority. If an instruction is executed, control branches invariably to the interrupt routine.

Reset > WDT/Oscillation stop detection > Peripheral function > Single step > Address match

Figure 10.8 Hardware Interrupt Priority

• **Interrupt Priority Resolution Circuit**

The interrupt priority resolution circuit is used to select the interrupt with the highest priority among those requested.

Figure 10.9 shows the Interrupts Priority Select Circuit

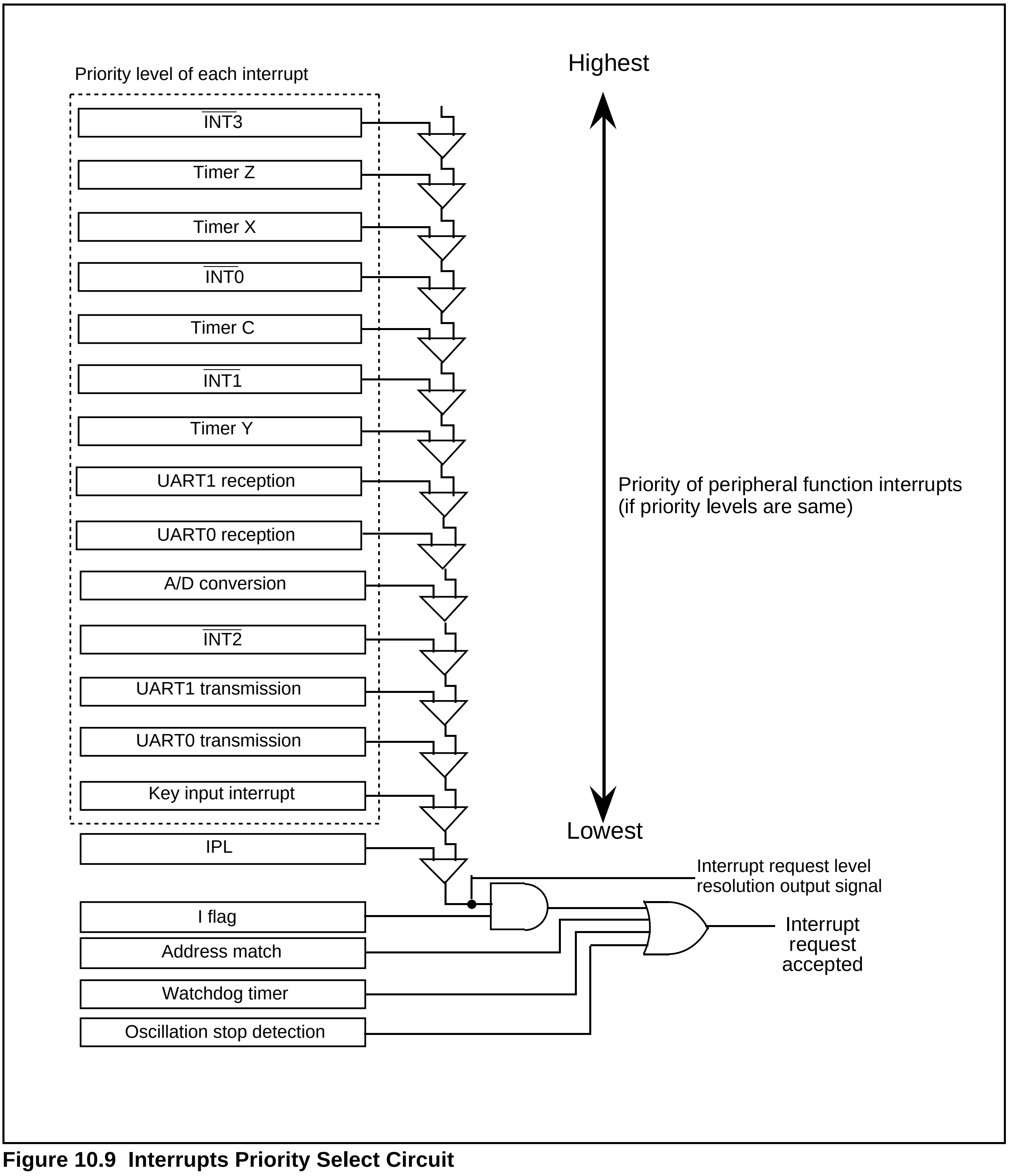


Figure 10.9 Interrupts Priority Select Circuit

10.2 INT Interrupt

10.2.1 INT0 Interrupt

INT0 interrupt is triggered by an INT0 input. When using INT0 interrupts, the INT0EN bit in the INTEN register must be set to “1” (enabling). The edge polarity is selected using the INT0PL bit in the INTEN register and the POL bit in the INT0IC register.

Inputs can be passed through a digital filter with three different sampling clocks.

The INT0 pin is shared with the external trigger input pin of Timer Z.

Figure 10.10 shows the INTEN and INT0F registers.

External input enable register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0		

Symbol: INTEN — Address: 0096_{16} — After reset: 00_{16}

Bit symbol	Bit name	Function	RW
INT0EN	INT0 input enable bit(1)	0 : Disabled 1 : Enabled	RW
INT0PL	INT0 input polarity select bit(2)	0 : One edge 1 : Both edges	RW
— (b7-b2)	Reserved bit	Set to “0”	RW

NOTES:
1. This bit must be set while the INT0STG bit in the PUM register is set to “0” (one-shot trigger disabled).
2. When setting the INT0PL bit to “1” (selecting both edges), the POL bit in the INT0IC must be set to “0” (selecting falling edge).
3. The IR bit in the INT0IC register may be set to “1” (interrupt requested) when the INT0PL bit is rewritten. Refer to the paragraph 19.2.5 “Changing Interrupt Factor” in the Usage Notes Reference Book.

INT0 input filter select register

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	0		

Symbol: INT0F — Address: $001E_{16}$ — After reset: $XXXXX000_2$

Bit symbol	Bit name	Function	RW
INT0F0	INT0 input filter select bit	b1 b0 0 0 : No filter 0 1 : Filter with f_1 sampling 1 0 : Filter with f_8 sampling 1 1 : Filter with f_{32} sampling	RW
INT0F1			RW
— (b2)	Reserved bit	Set to “0”	RW
— (b7-b3)	Nothing is assigned. When write, set to “0”. If read, it content is indeterminate.		—

Figure 10.10 INTEN Register and INT0F Register

10.2.2 INT0 Input Filter

The INT0 input has a digital filter which can be sampled by one of three sampling clocks. The sampling clock is selected using the INT0F1 to INT0F0 bits in the INT0F register. The IR bit in the INT0IC register is set to "1" (interrupt requested) when the sampled input level matches three times. When the INT0F1 to INT0F0 bits are set to "01_2", "10_2", or "11_2", the P4_5 bit in the P4 register indicates the filtered value.

Figure 10.11 shows the INT0 input filter configuration. Figure 10.12 shows an operation example of INT0 input filter.

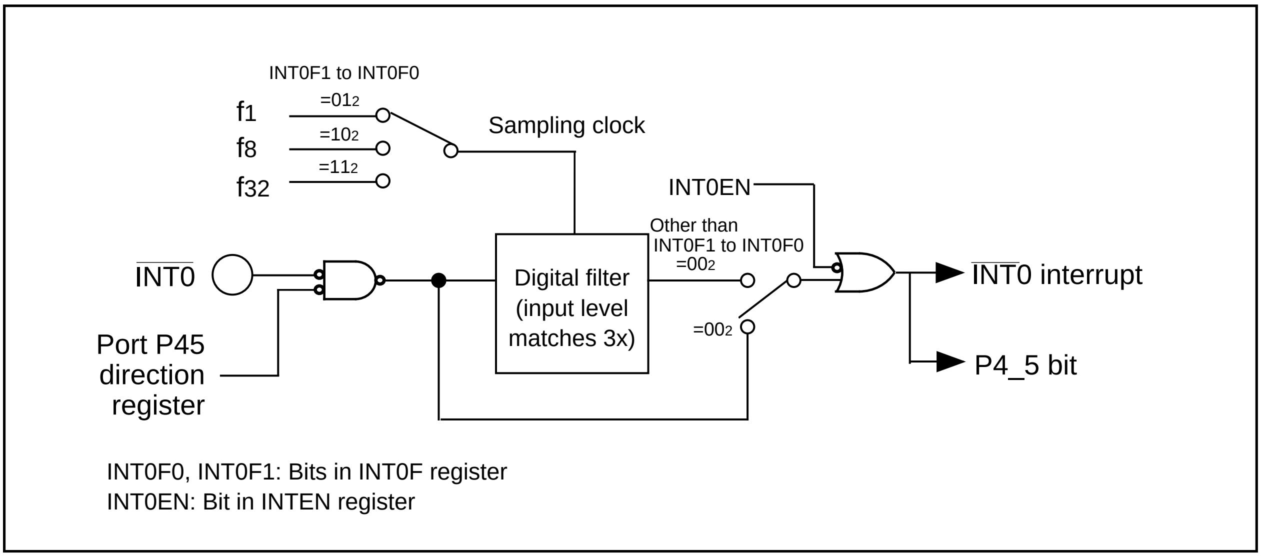


Figure 10.11 INT0 Input Filter

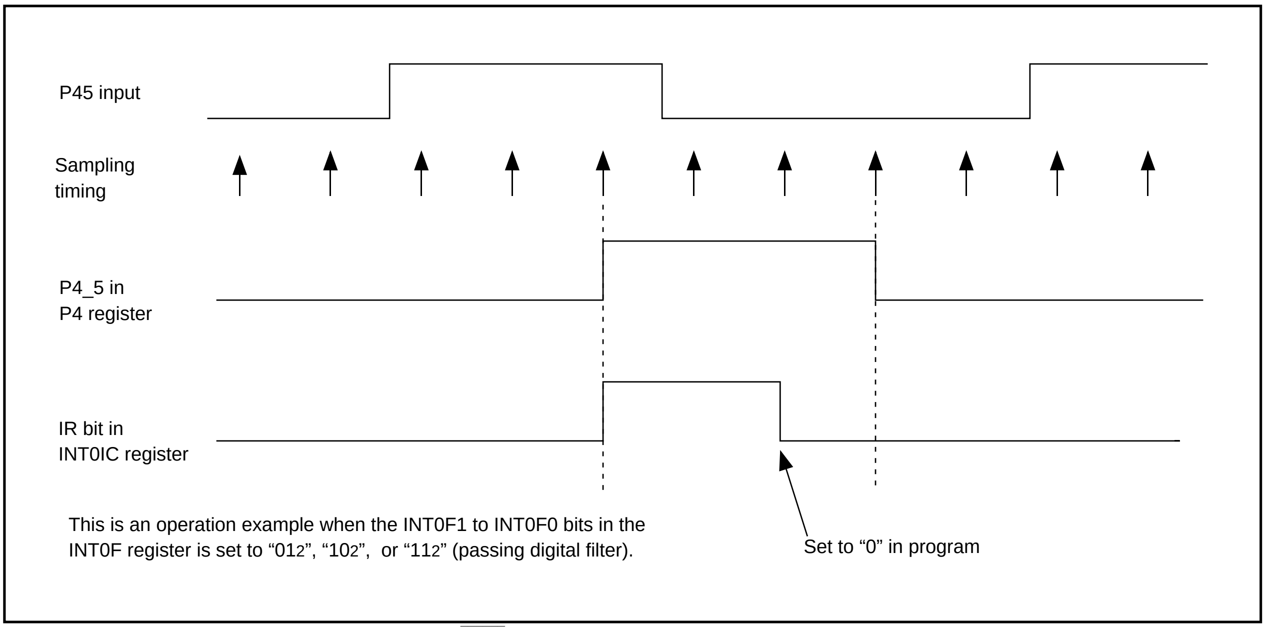


Figure 10.12 Operation Example of INT0 Input Filter

10.2.3 $\overline{\text{INT1}}$ Interrupt and $\overline{\text{INT2}}$ Interrupt

$\overline{\text{INT1}}$ interrupts are triggered by $\overline{\text{INT1}}$ inputs. The edge polarity is selected with the R0EDG bit in the TXMR register. The $\overline{\text{INT1}}$ pin can be used only when the Timer X is in timer mode because the $\overline{\text{INT1}}$ pin shares the same pin with the CNTR0 pin.
$\overline{\text{INT2}}$ interrupts are triggered by $\overline{\text{INT2}}$ inputs. The edge polarity is selected with the R1EDG bit in the TYZMR register. The $\overline{\text{INT2}}$ pin can be used only when the Timer Y is in timer mode because the $\overline{\text{INT2}}$ pin shares the same pin with the CNTR1 pin. The $\overline{\text{INT2}}$ pin can be used use with the CNTR1 pin
Figure 10.13 shows the TXMR and TYZMR registers when using $\overline{\text{INT1}}$ and $\overline{\text{INT2}}$ interrupts.

Timer X mode register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0			0	0

Symbol: TXMR — Address: 008B16 — After reset: 0016

Bit symbol	Bit name	Function	RW
TXMOD0	Operation mode select bit 0, 1	b1 b0 0 0 : Timer mode or pulse period measurement mode(3)	RW
TXMOD1			RW
R0EDG	$\overline{\text{INT1}}$/CNTR0 polarity switching bit(1, 2)	0 : Rising edge 1 : Falling edge	RW
TXS	Timer X count start flag	0 : Stops counting 1 : Starts counting	RW
TXOCNT	Set to "0" in timer mode		RW
TXMOD2	Operation mode select bit 2	0 : Other than pulse period measurement mode(3)	RW
TXEDG	Set to "0" in timer mode		RW
TXUND	Set to "0" in timer mode		RW

NOTES:
1. The IR bit in the INT1IC may be set to “1” (interrupt requested) when the R0EDG bit is rewritten. Refer to the paragraph 19.2.5 “Changing Interrupt Factor” in the Usage Notes Reference Book.
2. This bit is used to select the polarity of $\overline{\text{INT1}}$ interrupt in timer mode.
3. When using $\overline{\text{INT1}}$ interrupts, should select timer mode.

Timer Y, Z mode register

b7	b6	b5	b4	b3	b2	b1	b0
							0

Symbol: TYZMR — Address: 008016 — After reset: 0016

Bit symbol	Bit name	Function	RW
TYMOD0	Timer Y operation mode bit	0 : Timer mode(1)	RW
R1EDG	$\overline{\text{INT2}}$/CNTR1 polarity switching bit(2)	0 : Rising edge 1 : Falling edge	RW
TYWC	Timer Y write control bit	Function varies depending on the operation mode	RW
TYS	Timer Y count start flag	0 : Stops counting 1 : Starts counting	RW
TZMOD0	Timer Z-related bit		RW
TZMOD1			RW
TZWC			RW
TZS			RW

NOTES:
1. When using $\overline{\text{INT2}}$ interrupts, must set to timer mode.
2. The IR bit in the INT2IC may be set to “1” (interrupt requested) when the R1EDG bit is rewritten. Refer to the paragraph 19.2.5 “Changing Interrupt Factor” in the Usage Notes Reference Book.

Figure 10.13 TXMR Register and TYZMR Register when $\overline{\text{INT1}}$ and $\overline{\text{INT2}}$ Interrupt Used

10.2.4 INT3 Interrupt

INT3 interrupts are triggered by INT3 inputs. The TCC07 bit in the TCC0 register should be se to “0” (INT3). The INT3 input has a digital filter which can be sampled by one of three sampling clocks. The sampling clock is selected using the TCC11 to TCC10 bits in the TCC1 register. The IR bit in the INT3IC register is set to “1” (interrupt requested) when the sampled input level matches three times. The P3_3 bit in the P3 register indicates the previous value before filtering regardless of values set in the TCC11 to TCC10 bits.

The INT3 pin is shared with the TCIN pin.

When setting the TCC07 bit to “1” ($f_{RING128}$), INT3 interrupts are triggered by $f_{RING128}$ clock. The IR bit in the INT3IC register is set to “1” (interrupt requested) every $f_{RING128}$ clock cycle or every half $f_{RING128}$ clock cycle.

Figure 10.14 shows the TCC0 and TCC1 registers.

Timer C control register 0

b7	b6	b5	b4	b3	b2	b1	b0
	0	0					

Symbol: TCC0 Address: 009A$_{16}$ After reset: 00$_{16}$

Bit symbol	Bit name	Function	RW
TCC00	Capture control bit	0 : Capture disabled 1 : Capture enabled	RW
TCC01	Timer C count source select bit(1)	b2 b1 0 0 : f_1 0 1 : f_8 1 0 : f_{32} 1 1 : Avoid this setting	RW
TCC02			RW
TCC03	INT3 interrupt/capture input polarity select bit(1, 2)	b4 b3 0 0 : Rising edge 0 1 : Falling edge 1 0 : Both edges 1 1 : Avoid this setting	RW
TCC04			RW
(b6-b5)	reserved bit	Set to "0"	RW
TCC07	INT3 interrupt/capture input switching bit(1, 2)	0 : INT3 1 : $f_{RING128}$	RW

NOTES:
1. Change this bit when TCC00 bit is set to “0” (count stop).
2. The IR bit in the INT3IC may be set to “1” (interrupt requested) when the TCC03, TCC04, or TCC07 bit is rewritten. Refer to the paragraph 19.2.5 “Changing Interrupt Factor” in the Usage Notes Reference Book.

Timer C control register 1

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0		

Symbol: TCC1 Address: 009B$_{16}$ After reset: 00$_{16}$

Bit symbol	Bit name	Function	RW
TCC10	INT3 input filter select bit(1)	b1 b0 0 0 : No filter 0 1 : Filter with f_1 sampling 1 0 : Filter with f_8 sampling 1 1 : Filter with f_{32} sampling	RW
TCC11			RW
(b7-b2)	Reserved bit	Set to "0"	RW

NOTES:
1. Input is recognized only when the same value from INT3 pin is sampled three times in succession.

Figure 10.14 TCC0 Register and TCC1 Register

10.3 Key Input Interrupt

A key input interrupt is generated on an input edge of any of the $\overline{\mathrm{KI0}}$ to $\overline{\mathrm{KI3}}$ pins. Key input interrupts can be used as a key-on wakeup function to exit wait or stop mode. $\overline{\mathrm{KIi}}$ input can be enabled or disabled selecting with the KIiEN (i=0 to 3) bit in the KIEN register. The edge polarity can be rising edge or falling edge selecting with the KIiPL bit in the KIEN register. Note, however, that while input on any $\overline{\mathrm{KIi}}$ pin which has had the KIiPL bit set to “0” (falling edge) is pulled low, inputs on all other pins of the port are not detected as interrupts. Similarly, while input on any $\overline{\mathrm{KIi}}$ pin which has had the KIiPL bit set to “1” (rising edge) is pulled high, inputs on all other pins of the port are not detected as interrupts.

Figure 10.15 shows a block diagram of the key input interrupt.

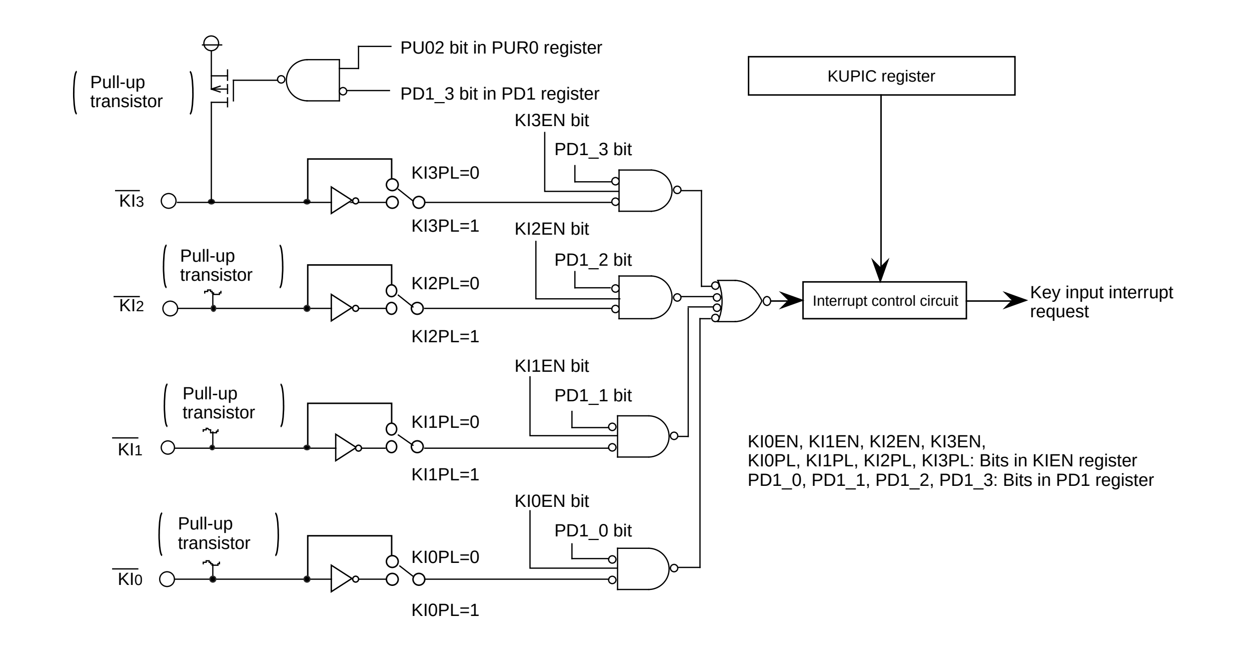


Figure 10.15 Key Input Interrupt

Key input enable register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After reset
KIEN	0098_{16}	00_{16}

Bit symbol	Bit name	Function	RW
KI0EN	KI0 input enable bit	0 : Disabled 1 : Enabled	RW
KI0PL	KI0 input polarity select bit	0 : Falling edge 1 : Rising edges	RW
KI1EN	KI1 input enable bit	0 : Disabled 1 : Enabled	RW
KI1PL	KI1 input polarity select bit	0 : Falling edge 1 : Rising edges	RW
KI2EN	KI2 input enable bit	0 : Disabled 1 : Enabled	RW
KI2PL	KI2 input polarity select bit	0 : Falling edge 1 : Rising edges	RW
KI3EN	KI3 input enable bit	0 : Disabled 1 : Enabled	RW
KI3PL	KI3 input polarity select bit	0 : Falling edge 1 : Rising edges	RW

NOTES:
1. The IR bit in the KUPIC register may be set to “1” (interrupt requested) when the KIEN register is rewritten. Refer to the paragraph 19.2.5 “Changing Interrupt Factor” in the Usage Notes Reference Book.

Figure 10.16 KIEN Register

10.4 Address Match Interrupt

An address match interrupt is generated immediately before executing the instruction at the address indicated by the RMADi register (i=0, 1). Set the start address of any instruction in the RMADi register. Use the AIER0 and AIER1 bits in the AIER register to enable or disable the interrupt. Note that the address match interrupt is unaffected by the I flag and IPL.

The value of the PC that is saved to the stack when an address match interrupt is acknowledged varies depending on the instruction at the address indicated by the RMAD i register (see the paragraph "register saving" for the value of the PC). Not appropriate return address is pushed on the stack. There are two ways to return from the address match interrupt as follows:

• Change the content of the stack and use a REIT instruction.

• Use an instruction such as POP to restore the stack as it was before an interrupt request was acknowledged. And then use a jump instruction.

Table 10.6 lists the value of the PC that is saved to the stack when an address match interrupt is acknowledged.

Figure 10.17 shows the AIER, and RMAD1 to RMAD0 registers.

Table 10.6 Value of PC Saved to Stack when Address Match Interrupt Acknowledged

Address indicated by RMADi register (i=0,1)	PC value saved[1]
• 16-bit operation code instruction • Instruction shown below among 8-bit operation code instructions ADD.B:S #IMM8,dest SUB.B:S #IMM8,dest AND.B:S #IMM8,dest OR.B:S #IMM8,dest MOV.B:S #IMM8,dest STZ.B:S #IMM8,dest STNZ.B:S #IMM8,dest STZX.B:S #IMM81,#IMM82,dest CMP.B:S #IMM8,dest PUSHM src POPM dest JMPS #IMM8 JSRS #IMM8 MOV.B:S #IMM,dest (However, dest = A0 or A1)	Address indicated by RMADi register + 2
• Instructions other than the above	Address indicated by RMADi register + 1

NOTES:
1. See the paragraph "saving registers" for the PC value saved.

Table 10.7 Relationship Between Address Match Interrupt Factors and Associated Registers

Address match interrupt factors	Address match interrupt enable bit	Address match interrupt register
Address match interrupt 0	AIER0	RMAD0
Address match interrupt 1	AIER1	RMAD1

Address match interrupt enable register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After reset
AIER	0009_{16}	$XXXXXX00_2$

Bit symbol	Bit name	Function	RW
AIER0	Address match interrupt 0 enable bit	0 : Interrupt disabled 1 : Interrupt enabled	RW
AIER1	Address match interrupt 1 enable bit	0 : Interrupt disabled 1 : Interrupt enabled	RW
— (b7-b2)	Nothing is assigned. When write, set to “0”. When read, their contents are indeterminate.		—

Address match interrupt register i (i = 0, 1)

(b23) b7 (b19) b3 (b16) b0 (b15) b7 (b8) b0 b7 b0

Symbol	Address	After reset
RMAD0	0012_{16} to 0010_{16}	$X00000_{16}$
RMAD1	0016_{16} to 0014_{16}	$X00000_{16}$

Function	Setting range	RW
Address setting register for address match interrupt	00000_{16} to $FFFFF_{16}$	RW
— (b7-b4) Nothing is assigned. When write, set to “0”. When read, its content is indeterminate.		—

Figure 10.17 AIER Register and RMAD0 to RMAD1 Registers

11. Watchdog Timer

The watchdog timer is the function of detecting when the program is out of control. Therefore, we recommend using the watchdog timer to improve reliability of a system. Figure 11.1 shows the watchdog timer block diagram. The watchdog timer contains a 15-bit counter which counts down the clock derived by dividing the CPU clock using the prescaler. Whether to generate a watchdog timer interrupt request or apply a watchdog timer reset as an operation to be performed when the watchdog timer underflows after reaching the terminal count can be selected using the PM12 bit in the PM1 register. The PM12 bit can only be set to "1" (reset). Once this bit is set to "1", it cannot be set to "0" (watchdog timer interrupt) in a program. Refer to Section 5.3, "Watchdog Timer Reset" for details.
The divide-by-N value for the prescaler can be chosen to be 16 or 128 with the WDC7 bit in the WDC register. The period of watchdog timer can be calculated as given below. The period of watchdog timer is, however, subject to an error due to the prescaler.

$$\text{Watchdog timer period} = \frac{\text{Prescaler dividing (16 or 128) X Watchdog timer count (32768)}}{\text{CPU clock}}$$

For example, when CPU clock = 16 MHz and the divide-by-N value for the prescaler= 16, the watchdog timer period is approx. 32.8 ms.

Figure 11.2 shows the OFS, the WDC, the WDTR and the WDTS registers. The watchdog timer operation after reset can be selected using the WDTON bit in the option function select register ($0FFFF_{16}$ address).

- When the WDTON bit is "0" (the watchdog timer is started automatically after reset), the watchdog timer and the prescaler both start counting automatically after reset.
- When the WDTON bit is "1" (the watchdog timer is inactive after reset), the watchdog timer and the prescaler both are inactive after reset, so that the watchdog timer is activated to start counting by writing to the WDTS register.

The WDTON bit can not be changed in a program. When setting the WDTON bit, write "0" into bit 0 of $0FFFF_{16}$ address using a flash writer. The watchdog timer is nitialized by writing to the WDTR register and the counting continues.

In stop mode and wait mode, the watchdog timer and the prescaler are stopped. Counting is resumed from the held value when the modes or state are released.

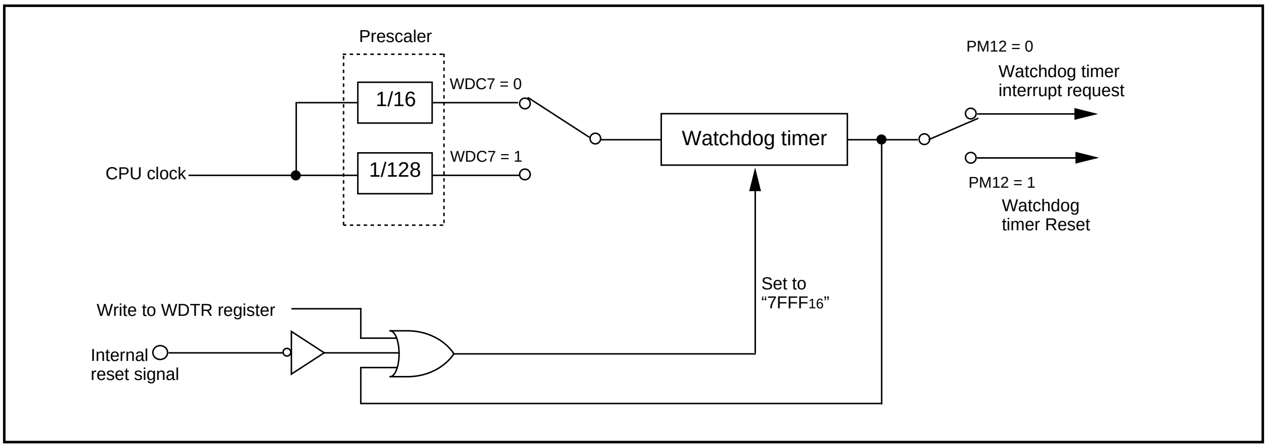


Figure 11.1 Watchdog Timer Block Diagram

Option function select register(1)

b7	b6	b5	b4	b3	b2	b1	b0
1	1	1	1	1	1	1	

Symbol OFS — Address $0FFFF_{16}$ — Before shipment FF_{16}

Bit symbol	Bit name	Function	RW
WDTON	Watchdog timer start select bit	0: The watchdog timer starts automatically after reset 1: The watchdog timer is inactive after reset	RW
— (b7 - b1)	Reserved bit	Set to “1”	RW

NOTES:
1. The OFS register can not be changed in a program. Write using a flash writer.

Watchdog timer control register

b7	b6	b5	b4	b3	b2	b1	b0
	0	0					

Symbol WDC — Address $000F_{16}$ — After reset 00011111_2

Bit symbol	Bit name	Function	RW
— (b4-b0)	High-order bit of watchdog timer		RO
— (b5)	Reserved bit	Must set to “0”	RW
— (b6)	Reserved bit	Must set to “0”	RW
WDC7	Prescaler select bit	0 : Divided by 16 1 : Divided by 128	RW

Watchdog timer reset register

b7 … b0

Symbol WDTR — Address $000D_{16}$ — After reset Indeterminate

Function	RW
The watchdog is initialized after a write instruction to this register. The watchdog timer value is always initialized to “$7FFF_{16}$” regardless of whatever value is written.	WO

Watchdog timer start register

b7 … b0

Symbol WDTS — Address $000E_{16}$ — After reset Indeterminate

Function	RW
The watchdog timer starts counting after a write instruction to this register.	WO

Figure 11.2 OFS, WDC, WDTR , and WDTS Registers

12. Timers

The microcomputer has three 8-bit timers and one 16-bit timer. The three 8-bit timers are Timer X, Timer Y, and Timer Z and each one has an 8-bit prescaler. The 16-bit timer is Timer C and has a capture. All these timers function independently. The count source for each timer is the operating clock that regulates the timing of timer operations such as counting and reloading.

Table 12.1 lists functional comparison.

Table 12.1 Functional Comparison

Item		Timer X	Timer Y	Timer Z	Timer C
Configuration		8-bit timer with 8-bit prescaler	8-bit timer with 8-bit prescaler	8-bit timer with 8-bit prescaler	16-bit timer
Count		Down	Down	Down	Up
Count source		•f1 •f2 •f8 •f32	•f1 •f8 •fRING •Input from CNTR1 pin	•f1 •f2 •f8 •Timer Y underflow	•f1 •f8 •f32
Function	Timer mode	provided	provided	provided	not provided
	Pulse output mode	provided	not provided	not provided	not provided
	Event counter mode	provided	provided(1)	not provided	not provided
	Pulse width measurement mode	provided	not provided	not provided	not provided
	Pulse period measurement mode	provided	not provided	not provided	not provided
	Programmable waveform generation mode	not provided	provided	provided	not provided
	Programmable one-shot generation mode	not provided	not provided	provided	not provided
	Programmable wait one-shot generation mode	not provided	not provided	provided	not provided
	Capture	not provided	not provided	not provided	provided
Input pin		CNTR0	CNTR1	$\overline{\text{INT0}}$	TCIN
Output pin		CNTR0 $\overline{\text{CNTR0}}$	CNTR1	TZOUT	not provided
Related interrupt		Timer X int $\overline{\text{INT1}}$ int	Timer Y int $\overline{\text{INT2}}$ int	Timer Z int $\overline{\text{INT0}}$ int	Timer C int $\overline{\text{INT3}}$ int
Timer stop		provided	provided	provided	provided

NOTES:
1. Select the input from the CNTR1 pin as a count source of timer mode.

12.1 Timer X

The Timer X is an 8-bit timer with an 8-bit prescaler. Figure 12.1 shows the block diagram of Timer X. Figures 12.2 and 12.3 show the Timer X-related registers.

The Timer X has five operation modes listed as follows:

- Timer mode: The timer counts an internal count source.
- Pulse output mode: The timer counts an internal count source and outputs the pulses whose polarity is inverted at the timer the timer underflows.
- Event counter mode: The timer counts external pulses.
- Pulse width measurement mode: The timer measures an external pulse's pulse width.
- Pulse period measurement mode:The timer measures an external pulse's period.

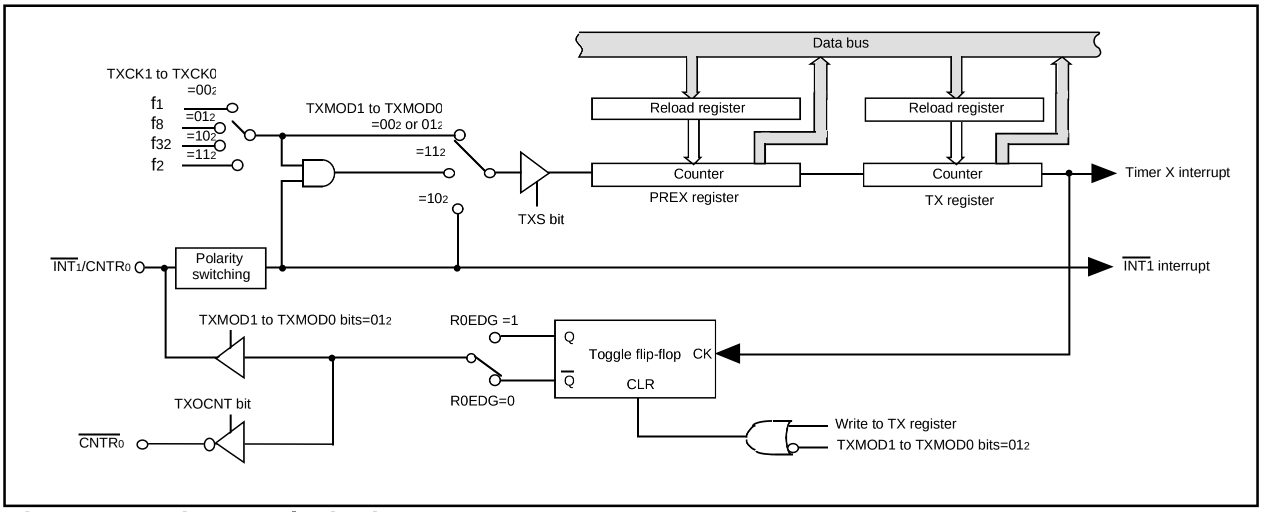


Figure 12.1 Timer X Block Diagram

Timer X mode register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol: TXMR
Address: 008B16
After reset: 0016

Bit symbol	Bit name	Function	RW
TXMOD0	Operation mode select bit 0, 1	b1 b0 0 0 : Timer mode or pulse period measurement mode 0 1 : Pulse output mode 1 0 : Event counter mode 1 1 : Pulse width measurement mode	RW
TXMOD1			RW
R0EDG	$\overline{INT1}$/CNTR0 polarity switching bit(1)	Function varies with each operation mode	RW
TXS	Timer X count start flag	0 : Stops counting 1 : Starts counting	RW
TXOCNT	P30/$\overline{CNTR0}$ select bit	Function varies with each operation mode	RW
TXMOD2	Operation mode select bit 2	0 : Except in pulse period measurement mode 1 : Pulse period measurement mode	RW
TXEDG	Active edge reception flag	Function varies depending on operation mode	RW
TXUND	Timer X under flow flag	Function varies depending on operation mode	RW

NOTES:
1. The IR bit in the INT1IC register may be set to “1” (interrupt requested) when the R0EDG bit is rewritten. Refer to the paragraph 19.2.5 “Changing Interrupt Factor” in the Usage Notes Reference Book.

Figure 12.2 TXMR Register

Prescaler X Register

b7–b0	Symbol	Address	After reset
	PREX	008C16	FF16

Mode	Function	Setting range	RW
Timer mode	Internal count source is counted	0016 to FF16	RW
Pulse output mode	Internal count source is counted	0016 to FF16	RW
Event counter mode	Externally input pulses are counted	0016 to FF16	RW
Pulse width measurement mode	Pulse width of externally input pulses is measured (Internal count source is counted)	0016 to FF16	RW
Pulse period measurement mode	Pulse period of externally input pulses is measured (Internal count source is counted)	0016 to FF16	RW

Timer X Register

b7–b0	Symbol	Address	After reset
	TX	008D16	FF16

Function	Setting range	RW
Underflow of Prescaler X is counted	0016 to FF16	RW

Timer count source setting register

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After reset
0	0							TCSS	008E16	0016

Bit symbol	Bit name	Function	RW
TXCK0	Timer X count source select bit(1)	b1 b0 0 0 : f1 0 1 : f8 1 0 : f32 1 1 : f2	RW
TXCK1			RW
TYCK0	Timer Y count source select bit(1)	b3 b2 0 0 : f1 0 1 : f8 1 0 : fRING 1 1 : Selects input from CNTR1 pin	RW
TYCK1			RW
TZCK0	Timer Z count source select bit(1)	b5 b4 0 0 : f1 0 1 : f8 1 0 : Selects Timer Y underflow 1 1 : f2	RW
TZCK1			RW
—— (b7-b6)	Reserved bit	Must be set to “0”	RW

NOTES:
1. Avoid switching a count source, while a counter is in progress. Timer counter must be stopped before switching a count source.

Figure 12.3 PREX Register, TX Register, and TCSS Register

12.1.1 Timer Mode

In this mode, the timer counts an internally generated count source (See “Table 12.2 Timer Mode Specifications”). Figure 12.4 shows the TXMR register in timer mode.

Table 12.2 Timer Mode Specifications

Item	Specification
Count source	f_1, f_2, f_8, f_{32}
Count operation	• Down-count • When the timer underflows, it reloads the reload register contents before continuing counting
Divide ratio	1/(n+1)(m+1) n: set value of PREX register, m: set value of TX register
Count start condition	Write “1” (count start) to TXS bit in TXMR register
Count stop condition	Write “0” (count stop) to TXS bit in TXMR register
Interrupt request generation timing	When Timer X underflows [Timer X interruption]
$\overline{INT1}$/$\overline{CNTR_0}$ pin function	Programmable I/O port, or $\overline{INT1}$ interrupt input
$\overline{CNTR_0}$ pin function	Programmable I/O port
Read from timer	Count value can be read by reading TX register Same applies to PREX register.
Write to timer	Value written to TX register is written to both reload register and counter. Same applies to PREX register.

Timer X mode register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0			0	0

Symbol: TXMR   Address: 008B16   After reset: 0016

Bit symbol	Bit name	Function	RW
TXMOD0	Operation mode select bit 0, 1	b1 b0 0 0 : Timer mode or pulse period measurement mode	RW
TXMOD1			RW
R0EDG	$\overline{INT1}$/$\overline{CNTR_0}$ polarity switching bit(1, 2)	0 : Rising edge 1 : Falling edge	RW
TXS	Timer X count start flag	0 : Stops counting 1 : Starts counting	RW
TXOCNT	Set to "0" in timer mode		RW
TXMOD2	Operation mode select bit 2	0 : Other than pulse period measurement mode	RW
TXEDG	Set to "0" in timer mode		RW
TXUND	Set to "0" in timer mode		RW

NOTES:
1. The IR bit in the INT1IC register may be set to “1” (interrupt requested) when the R0EDG bit is rewritten. Refer to the paragraph 19.2.5 “Changing Interrupt Factor” in the Usage Notes Reference Book.
2. This bit is used to select the polarity of $\overline{INT1}$ interrupt in timer mode.

Figure 12.4 TXMR Register in Timer Mode

12.1.2 Pulse Output Mode

In this mode, the timer counts an internally generated count source, and outputs from the CNTR0 pin a pulse whose polarity is inverted each time the timer underflows (See "Table 12.3 Pulse Output mode Specifications"). Figure 12.5 shows TXMR register in pulse output mode.

Table 12.3 Pulse Output Mode Specifications

Item	Specification
Count source	f_1, f_2, f_8, f_{32}
Count operation	• Down-count • When the timer underflows, it reloads the reload register contents before continuing counting
Divide ratio	1/(n+1)(m+1) n: set value of PREX register, m: set value of TX register
Count start condition	Write "1" (count start) to TXS bit in TXMR register
Count stop condition	Write "0" (count stop) to TXS bit in TXMR register
Interrupt request generation timing	• When Timer X underflows [Timer X interruption]
$\overline{INT1}$/$CNTR_0$ pin function	Pulse output
$\overline{CNTR_0}$ pin function	Programmable I/O port or inverted output of $CNTR_0$
Read from timer	Count value can be read by reading TX register. Same applies to PREX register.
Write to timer	Value written to TX register is written to both reload register and counter. Same applies to PREX register.
Select function	• $\overline{INT1}$/$CNTR_0$ polarity switching function Polarity level at starting of pulse output can be selected with R0EDG bit(1) • Inverted pulse output function Inverted pulse of CNTR0 output polarity can be output from the $\overline{CNTR0}$ pin (selected by TXOCNT bit)

NOTES:
1. The level of the output pulse becomes the level when the pulse output starts when the TX register is written to.

Timer X mode register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0				0	1

Symbol: TXMR — Address: $008B_{16}$ — After reset: 00_{16}

Bit symbol	Bit name	Function	RW
TXMOD0	Operation mode select bit 0, 1	b1 b0 0 1 : Pulse output mode	RW
TXMOD1			RW
R0EDG	$\overline{INT1}$/$CNTR_0$ polarity switching bit(1)	0: $CNTR_0$ output starts at "H" 1: $CNTR_0$ output starts at "L"	RW
TXS	Timer X count start flag	0 : Stops counting 1 : Starts counting	RW
TXOCNT	$P3_0$/$\overline{CNTR_0}$ select bit	0 : Port $P3_0$ 1 : $\overline{CNTR_0}$ output	RW
TXMOD2	Set to "0" in pulse output mode		RW
TXEDG	Set to "0" in pulse output mode		RW
TXUND	Set to "0" in pulse output mode		RW

NOTES:
1. The IR bit in the INT1IC register may be set to "1" (interrupt requested) when the R0EDG bit is rewritten. Refer to the paragraph 19.2.5 "Changing Interrupt Factor" in the Usage Notes Reference Book.

Figure 12.5 TXMR Register in Pulse Output Mode

12.1.3 Event Counter Mode

In this mode, the timer counts an external signal fed to $\overline{\text{INT1}}$/CNTR0 pin (See “Table 12.4 Event Counter Mode Specifications”). Figure 12.6 shows TXMR register in event counter mode.

Table 12.4 Event Counter Mode Specifications

Item	Specification
Count source	External signals fed to CNTR0 pin (Active edge is selected by program)
Count operation	• Down count • When the timer underflows, it reloads the reload register contents before continuing counting
Divide ratio	1/(n+1)(m+1) n: set value of PREX register, m: set value of TX register
Count start condition	Write “1” (count start) to TXS bit in TXMR register
Count stop condition	Write “0” (count stop) to TXS bit in TXMR register
Interrupt request generation timing	• When Timer X underflows [Timer X interrupt]
INT1/CNTR0 pin function	Count source input ($\overline{\text{INT1}}$ interrupt input)
$\overline{\text{CNTR0}}$ pin function	Programmable I/O port
Read from timer	Count value can be read by reading TX register Same applies to PREX register.
Write to timer	Value written to TX register is written to both reload register and counter. Same applies to PREX register.
Select function	• $\overline{\text{INT1}}$/CNTR0 polarity switching function Active edge of count source can be selected with R0EDG.

Timer X mode register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0			1	0

Symbol	Address	After reset
TXMR	008B16	0016

Bit symbol	Bit name	Function	RW
TXMOD0	Operation mode select bit 0, 1	b1 b0 1 0 : Event counter mode	RW
TXMOD1			RW
R0EDG	$\overline{\text{INT1}}$/CNTR0 polarity switching bit(1)	0 : Rising edge 1 : Falling edge	RW
TXS	Timer X count start flag	0 : Stops counting 1 : Starts counting	RW
TXOCNT	Set to "0" in event counter mode		RW
TXMOD2	Set to "0" in event counter mode		RW
TXEDG	Set to "0" in event counter mode		RW
TXUND	Set to "0" in event counter mode		RW

NOTES:
1. The IR bit in the INT1IC register may be set to “1” (interrupt requested) when the R0EDG bit is rewritten.
Refer to the paragraph 19.2.5 “Changing Interrupt Factor” in the Usage Notes Reference Book.

Figure 12.6 TXMR Register in Event Counter Mode

12.1.4 Pulse Width Measurement Mode

In this mode, the timer measures the pulse width of an external signal fed to $\overline{\text{INT1}}$/CNTR0 pin (See "Table 12.5 Pulse Width Measurement Mode Specifications"). Figure 12.7 shows the TXMR register in pulse width measurement mode. Figure 12.8 shows an operation example in pulse width measurement mode.

Table 12.5 Pulse Width Measurement Mode Specifications

Item	Specification
Count source	f1, f2, f8, f32
Count operation	• Down-count • Continuously counts the selected signal only when the measurement pulse is "H" level, or conversely only "L" level. • When the timer underflows, it reloads the reload register contents before continuing counting
Count start condition	Write "1" (count start) to TXS bit in TXMR register
Count stop condition	Write "0" (count stop) to TXS bit in TXMR register
Interrupt request generation timing	• When Timer X underflows [Timer X interruption] • Rising or falling of CNTR0 input (end of measurement period) [$\overline{\text{INT1}}$ interrupt]
$\overline{\text{INT1}}$/CNTR0 pin function	Measurement pulse input
$\overline{\text{CNTR0}}$ pin function	Programmable I/O port
Read from timer	Count value can be read by reading TX register Same applies to PREX register.
Write to timer	Value written to TX register is written to both reload register and counter. Same applies to PREX register.
Select function	• $\overline{\text{INT1}}$/CNTR0 polarity switching function "H" or "L" level duration can be selected with R0EDG bit as the input pulse measurement

Timer X mode register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0			1	1

Symbol: TXMR Address: 008B$_{16}$ After reset: 00$_{16}$

Bit symbol	Bit name	Function	RW
TXMOD0	Operation mode select bit 0, 1	b1 b0 1 1 : Pulse width measurement mode	RW
TXMOD1			RW
R0EDG	$\overline{\text{INT1}}$/CNTR0 polarity switching bit(1)	[CNTR0] 0 : Measures "H" level width 1 : Measures "L" level width [$\overline{\text{INT1}}$] 0 : Rising edge 1 : Falling edge	RW
TXS	Timer X count start flag	0 : Stops counting 1 : Starts counting	RW
TXOCNT	Set to "0" in pulse width measurement mode		RW
TXMOD2	Set to "0" in pulse width measurement mode		RW
TXEDG	Set to "0" in pulse width measurement mode		RW
TXUND	Set to "0" in pulse width measurement mode		RW

NOTES:
1. The IR bit in the INT1IC register may be set to "1" (interrupt requested) when the R0EDG bit is rewritten. Refer to the paragraph 19.2.5 "Changing Interrupt Factor" in the Usage Notes Reference Book.

Figure 12.7 TXMR Register in Pulse Width Measurement Mode

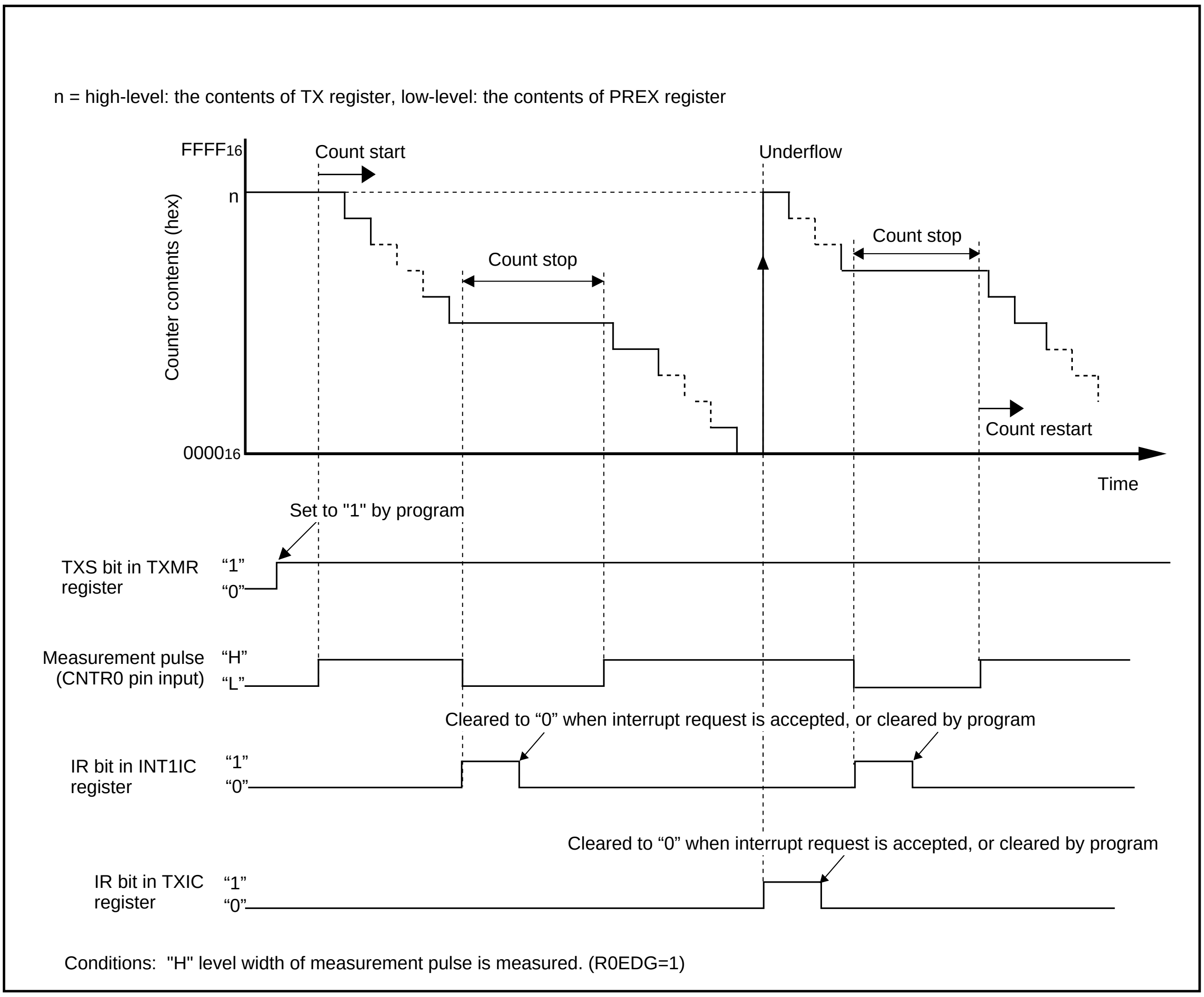


Figure 12.8 Operation Example in Pulse Width Measurement Mode

12.1.5 Pulse Period Measurement Mode

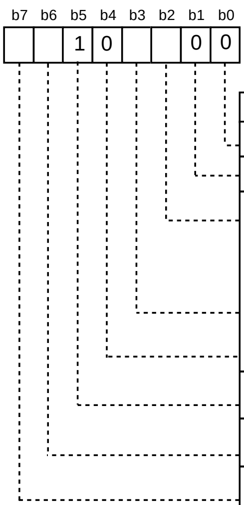
In this mode, the timer measures the pulse period of an external signal fed to $\overline{\text{INT1}}$/CNTR0 pin (See "Table 12.6 Pulse Period Measurement Mode Specifications"). Figure 12.9 shows the TXMR register in pulse period measurement mode. Figure 12.10 shows an operation example in pulse period measurement mode.

Table 12.6 Pulse Period Measurement Mode Specifications

Item	Specification
Count source	f_1, f_2, f_8, f_{32}
Count operation	• Down-count • After an active edge of measurement pulse is input, contents in the read-out buffer is retained in the first underflow of prescaler X. Then the timer X reloads contents in the reload register in the second underflow of prescaler X and continues counting.
Count start condition	Write "1" (count start) to TXS bit in TXMR register
Count stop condition	Write "0" (count stop) to TXS bit in TXMR register
Interrupt request generation timing	• When Timer X underflows or reloads [Timer X interrupt] • Rising or falling of CNTR0 input (end of measurement period) [$\overline{\text{INT1}}$ interrupt]
$\overline{\text{INT1}}$/CNTR0 pin function	Measurement pulse input(1) ($\overline{\text{INT1}}$ interrupt input)
$\overline{\text{CNTR0}}$ pin function	Programmable I/O port
Read from timer	Contents in the read-out buffer can be read by reading TX register. The value retained in the read-out buffer is released by reading TX register.
Write to timer	Value written to TX register is written to both reload register and counter. Same applies to PREX register.
Select function	• $\overline{\text{INT1}}$/CNTR0 polarity switching function Measurement period of input pulse can be selected with R0EDG bit.

NOTES:
1. The period of input pulse must be longer than twice the period of prescaler X. Longer pulse for H width and L width than the prescaler X period must be input. If shorter pulse than the period is input to the CNTR0 pin, the input may be disabled.

Timer X mode register

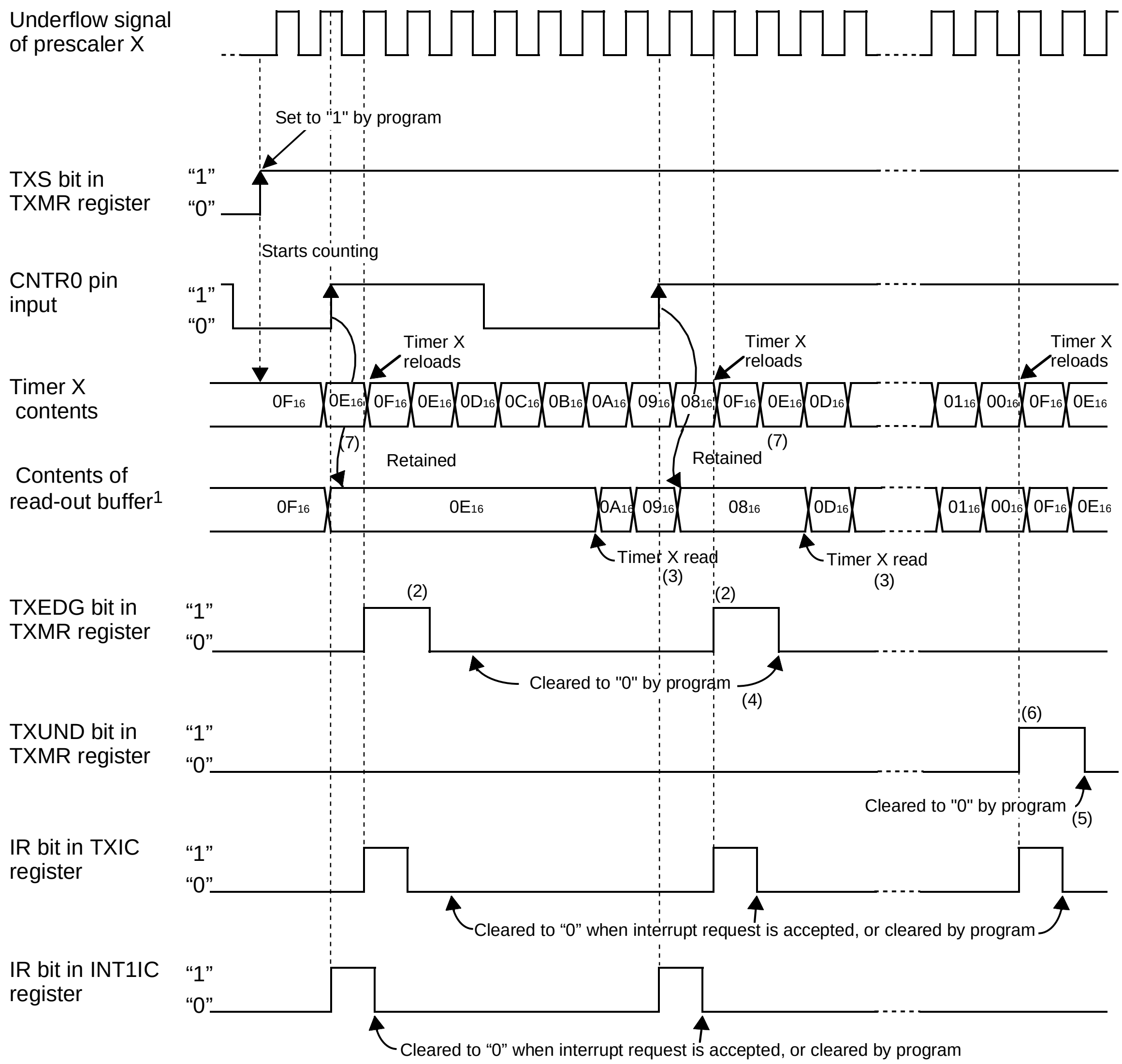


Symbol: TXMR | Address: $008B_{16}$ | After reset: 00_{16}

Bit symbol	Bit name	Function	RW
TXMOD0	Operation mode select bit 0, 1	b1 b0 0 0 : Timer mode or pulse period measurement mode	RW
TXMOD1			RW
R0EDG	$\overline{\text{INT1}}$/CNTR0 polarity switching bit(1)	[CNTR0] 0: Measures a measurement pulse from one rising edge to the next rising edge 1: Measures a measurement pulse from one falling edge to the next falling edge [$\overline{\text{INT1}}$] 0 : Rising edge 1 : Falling edge	RW
TXS	Timer X count start flag	0 : Stops counting 1 : Starts counting	RW
TXOCNT	Set to "0" in pulse period measurement mode		RW
TXMOD2	Operation mode select bit 2	1 : Pulse period measurement mode	RW
TXEDG(2)	Active edge judgment flag	0 : No active edge 1 : Active edge found	RW
TXUND(2)	Timer X underflow flag	0 : No under flow 1 : Under flow found	RW

NOTES:
1. The IR bit in the INT1IC register may be set to "1" (interrupt requested) when the R0EDG bit is rewritten. Refer to the paragraph 19.2.5 "Changing Interrupt Factor" in the Usage Notes Reference Book.
2. This bit is set to "0" by writing "0" in a program. (It remains unchanged even if writing "1")

Figure 12.9 TXMR Register in Pulse Period Measurement Mode



Conditions: A period from one rising edge to the next rising edge of measurement pulse is measured (R0EDG=0) with TX register initial value=0F16.

NOTES:
1. The contents of the read-out buffer can be read when the TX register is read in pulse period measurement mode.
2. After an active edge of measurement pulse is input, the TXEDG bit in the TXMR register is set to "1" (active edge found) when the prescaler X underflows for the second time.
3. The TX register should be read before the next active edge is input after the TXEDG bit is set to "1" (active edge found). The contents in the read-out buffer is retained until the TX register is read. If the TX register is not read before the next active edge is input, the measured result of the previous period is retained.
4. When set to "0" by program, use a MOV instruction to write "0" to the TXEDG in the TXMR register. At the same time, write "1" to the TXUND bit.
5. When set to "0" by program, use a MOV instruction to write "0" to the TXUND in the TXMR register. At the same time, write "1" to the TXEDG bit.
6. The TXUND and TXEDG bits are both set to "1" if the timer underflows and reloads on an active edge simultaneously. In this case, the validity of the TXUND bit should be determined by the contents of the read-out buffer.
7. If the CNTR0 active edge is input, when the prescaler X underflow signal is "H" level, its count value is the one of the read buffer. If "L" level, the following count value is the one of the read buffer.

Figure 12.10 Operation Example in Pulse Period Measurement Mode

12.2 Timer Y

Timer Y is an 8-bit timer with an 8-bit prescaler and has two reload registers-Timer Y Primary and Timer Y Secondary. Figure 12.11 shows a block diagram of Timer Y. Figures 12.12 to 12.14 show the TYZMR, PREY, TYSC, TYPR, TYZOC, PUM, and YCSS registers.

The Timer Y has two operation modes as follows:

- Timer mode: The timer counts an internal count source.
- Programmable waveform generation mode: The timer outputs pulses of a given width successively.

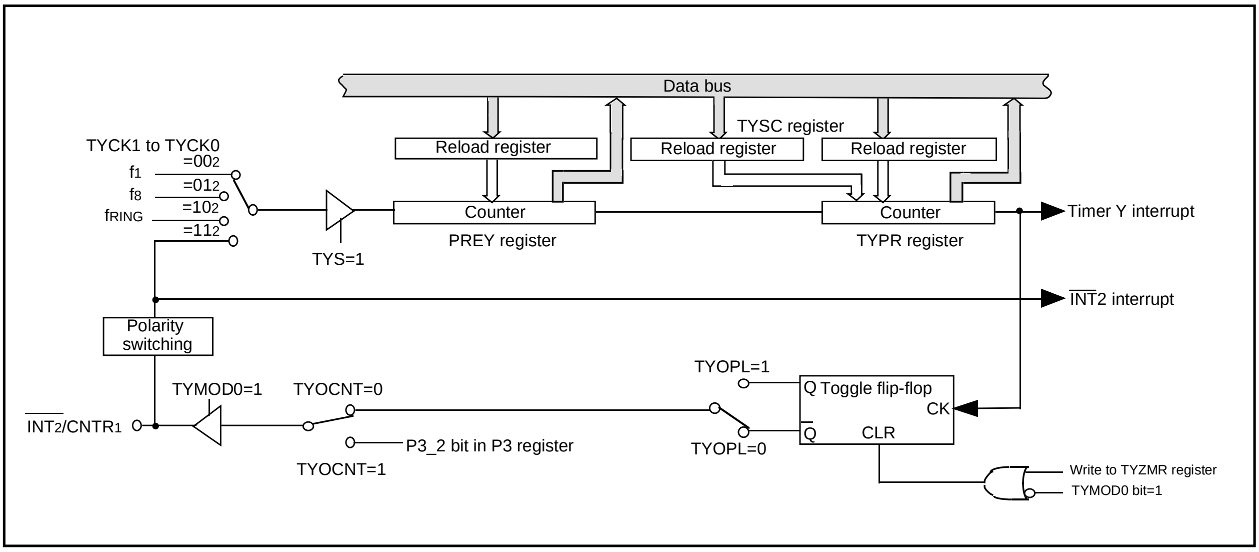


Figure 12.11 Timer Y Block Diagram

Timer Y, Z mode register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After reset
TYZMR	0080_{16}	00_{16}

Bit symbol	Bit name	Function	RW
TYMOD0	Timer Y operation mode bit	0 : Timer mode 1 : Programmable waveform generation mode	RW
R1EDG	INT2/CNTR1 polarity switching bit(1)	0 : Rising edge 1 : Falling edge	RW
TYWC	Timer Y write control bit	Function varies depending on the operation mode	RW
TYS	Timer Y count start flag	0 : Stops counting 1 : Starts counting	RW
TZMOD0	Timer Z operation mode bit	b5 b4 0 0 : Timer mode 0 1 : Programmable waveform generation mode 1 0 : Programmable one-shot generation mode 1 1 : Programmable wait one-shot generation mode	RW
TZMOD1			RW
TZWC	Timer Z write control bit	Function varies depending on the operation mode	RW
TZS	Timer Z count start flag	0 : Stops counting 1 : Starts counting	RW

NOTES:
1. The IR bit in the INT2IC register may be set to “1” (interrupt requested) when the R1EDG bit is rewritten. Refer to the paragraph 19.2.5 “Changing Interrupt Factor” in the Usage Notes Reference Book.

Figure 12.12 TYZMR Register

Prescaler Y register

b7 b0

Symbol PREY | Address 0081_{16} | After reset FF_{16}

Mode	Function	Setting range	RW
Timer mode	Internal count source or CNTR1 input is counted	00_{16} to FF_{16}	RW
Programmable waveform generation mode	Internal count source is counted	00_{16} to FF_{16}	RW

Timer Y secondary register

b7 b0

Symbol TYSC | Address 0082_{16} | After reset FF_{16}

Mode	Function	Setting range	RW
Timer mode	Disabled	—	—
Programmable waveform generation mode	Underflow of Prescaler Y is counted(1)	00_{16} to FF_{16}	WO(2)

NOTES:
1. The values of TYPR register and TYSC register are reloaded to the counter alternately for counting.
2. The count value can be read out by reading the TYPR register even when the secondary period is being counted.

Timer Y primary register

b7 b0

Symbol TYPR | Address 0083_{16} | After reset FF_{16}

Mode	Function	Setting range	RW
Timer mode	Underflow of Prescaler Y is counted	00_{16} to FF_{16}	RW
Programmable waveform generation mode	Underflow of Prescaler Y is counted(1)	00_{16} to FF_{16}	RW

NOTES:
1. The values of TYPR register and TYSC register are reloaded to the counter alternately for counting.

Timer Y, Z output control register(3)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol TYZOC | Address $008A_{16}$ | After reset 00_{16}

Bit symbol	Bit name	Function	RW
TZOS	Timer Z one-shot start bit(1)	0 : Stops one-shot 1 : Starts one-shot	RW
TYOCNT	Timer Y programmable waveform generation output switching bit(2)	0 : Outputs programmable waveform 1 : Outputs the value of $P3_2$ port register	RW
TZOCNT	Timer Z programmable waveform generation output switching bit(2)	0 : Outputs programmable waveform 1 : Outputs the value of $P3_1$ port register	RW
— (b7-b3)	Nothing is assigned. When write, set to "0". When read, its content is "0".		—

NOTES:
1. This bit is set to "0" when the output of one-shot waveform is completed. The TZOS bit should be set to "0" if the one-shot waveform output is terminated by setting the TZS bit in the TYZMR to "0" during the waveform output.
2. This bit is enabled only when operating in programmable waveform generation mode.
3. If executing an instruction which changes this register when the TZOS bit is "1" (during the count), the TZOS is automatically set to "0" when the count completes while the instruction is executed. If this causes some problems, execute an instruction which changes this register when the TZOS bit is "0" (one shot stop).

Figure 12.13 PREY Register, TYSC Register, TYPR Register, and TYZOC Register

Timer Y, Z waveform output control register

b7	b6	b5	b4	b3	b2	b1	b0
				0	0	0	0

Symbol: PUM
Address: 0084_{16}
After reset: 00_{16}

Bit symbol	Bit name	Function	RW
— (b3-b0)	Reserved bit	Must set to "0"	RW
TYOPL	Timer Y output level latch	Function varies depending on the operation mode	RW
TZOPL	Timer Z output level latch	Function varies depending on the operation mode	RW
INOSTG	$\overline{INT0}$ pin one-shot trigger control bit(2) (Timer Z)	0 : $\overline{INT0}$ pin one-shot trigger invalid 1 : $\overline{INT0}$ pin one-shot trigger valid	RW
INOSEG	$\overline{INT0}$ pin one-shot trigger polarity select bit(1) (Timer Z)	0 : Edge trigger at falling edge 1 : Edge trigger at rising edge	RW

NOTES:
1. The INOSEG bit is valid only when the INT0PL bit in the INTEN register is "0" (one-edge).
2. The INOSGT bit must be set to "1" after the INT0EN bit in the INTEN register and the INOSEG bit in the PUM register are set.

Timer count source setting register

b7	b6	b5	b4	b3	b2	b1	b0
0	0						

Symbol: TCSS
Address: $008E_{16}$
After reset: 00_{16}

Bit symbol	Bit name	Function	RW
TXCK0	Timer X count source select bit(1)	b1 b0 0 0 : f_1 0 1 : f_8 1 0 : f_{32} 1 1 : f_2	RW
TXCK1			RW
TYCK0	Timer Y count source select bit(1)	b3 b2 0 0 : f_1 0 1 : f_8 1 0 : f_{RING} 1 1 : Selects input from $CNTR_1$ pin	RW
TYCK1			RW
TZCK0	Timer Z count source select bit(1)	b5 b4 0 0 : f_1 0 1 : f_8 1 0 : Selects Timer Y underflow 1 1 : f_2	RW
TZCK1			RW
— (b7-b6)	Reserved bit	Must be set to "0"	RW

NOTES:
1. Avoid switching a count source, while a counter is in progress. Timer counter must be stopped before switching a count source.

Figure 12.14 PUM Register and TCSS Register

12.2.1 Timer Mode

In this mode, the timer counts an internally generated count source (see “Table 12.7 Timer Mode Specifications”). An external signal input to the CNTR1 pin can be counted. The TYSC register is unused in timer mode. Figure 12.15 shows the TYZMR and PUM registers in timer mode.

Table 12.7 Timer Mode Specifications

Item	Specification
Count source	f_1, f_8, f_{RING}, external signal fed to CNTR1 pin
Count operation	• Down-count • When the timer underflows, it reloads the reload register contents before continuing counting (When the Timer Y underflows, the contents of the Timer Y primary reload register is reloaded.)
Divide ratio	1/(n+1)(m+1) n: set value in PREY register, m: set value in TYPR register
Count start condition	Write “1” (count start) to TYS bit in TYZMR register
Count stop condition	Write “0” (count stop) to TYS bit in TYZMR register
Interrupt request generation timing	• When Timer Y underflows [Timer Y interrupt]
$\overline{INT2}$/CNTR1 pin function	Programmable I/O port, count source input or $\overline{INT2}$ interrupt input • When the TYCK1 to TYCK0 bits in the TCSS register are set to “00b”, “01b” or “10b” (Timer Y count source is f_1, f_8 or f_{RING}), programmable I/O port or $\overline{INT2}$ interrupt input • When the TYCK1 to TYCK0 bits are set to “11b” (Timer Y count source is CNTR1 input), count source input ($\overline{INT2}$ interrupt input)
Read from timer	Count value can be read out by reading TYPR register. Same applies to PREY register.
Write to timer(1)	Value written to TYPR register is written to both reload register and counter or written to only reload register. Selected by program. Same applies to PREY register.
Select function	• Event counter function When setting TYCK1 to TYCK0 bits to “11_2”, an external signal fed to CNTR1 pin is counted. • $\overline{INT2}$/CNTR1 switching bit Active edge of count source is selected by R1EDG bit.

NOTES:

1. The IR bit in the TYIC register is set to "1" (interrupt requested) if you write to the TYPR or PREY register while both of the following conditions are met.

   Conditions:
   - TYWC bit in TYZMR register is "0" (write to reload register and counter simultaneously)
   - TYS bit is "1" (count start)

   To write to the TYPR or PREY register in the above state, disable interrupts before writing.

Timer Y, Z mode register

b7	b6	b5	b4	b3	b2	b1	b0
							0

Symbol: TYZMR | Address: 0080_{16} | After reset: 00_{16}

Bit symbol	Bit name	Function	RW
TYMOD0	Timer Y operation mode bit	0 : Timer mode	RW
R1EDG	$\overline{INT2}$/CNTR1 polarity switching bit(1)	0 : Rising edge 1 : Falling edge	RW
TYWC	Timer Y write control bit(2)	0 : Write to reload register and counter simultaneously 1 : Write to reload register	RW
TYS	Timer Y count start flag	0 : Stops counting 1 : Starts counting	RW
TZMOD0	Timer Z-related bit		RW
TZMOD1			RW
TZWC			RW
TZS			RW

NOTES:
1. The IR bit in the INT2IC register may be set to “1” (interrupt requested) when the R1EDG bit is rewritten. Refer to the paragraph 19.2.5 “Changing Interrupt Factor” in the Usage Notes Reference Book.
2. When TYS bit=1 (starts counting), the value set in the TYWC bit is valid. If TYWC bit=0, the timer Y count value is written to both reload register and counter. If TYWC bit=1, the timer Y count value is written to the reload register only.
When TYS bit=0 (stops counting), the timer Y count value is written to both reload register and counter regardless of how the TYWC bit is set.

Timer Y, Z waveform output control register

b7	b6	b5	b4	b3	b2	b1	b0
				0	0	0	0

Symbol: PUM | Address: 0084_{16} | After reset: 00_{16}

Bit symbol	Bit name	Function	RW
— (b3-b0)	Reserved bit	Must set to “0”	RW
TYOPL	Timer Y output level latch	Invalid in timer mode	RW
TZOPL	Timer Z-related bits		RW
INOSTG			RW
INOSEG			RW

Figure 12.15 TYZMR Register and PUM Register in Timer Mode

12.2.2 Programmable Waveform Generation Mode

In this mode, an signal output from the TYOUT pin is inverted each time the counter underflows, while the values in the TYPR register and TYSC register are counted alternately (see “Table 12.8 Programmable Waveform Generation Mode Specifications”). A counting starts by counting the set value in the TYPR register. Figure 12.16 shows the TYZMR register in programmable waveform generation mode. Figure 12.17 shows the operation example.

Table 12.8 Programmable Waveform Generation Mode Specifications

Item	Specification
Count source	f_1, f_8, f_{RING}
Count operation	• Down count • When the timer underflows, it reloads the contents of primary reload register and secondary reload register alternately before continuing counting.
Output waveform width and period	Primary period : $(n+1)(m+1)/f_i$ Secondary period : $(n+1)(p+1)/f_i$ Period : $(n+1)\{(m+1)+(p+1)\}/f_i$ n: set value in PREY register, m: set value in TYPR register, p: set value in TYSC register f_i : Count source frequency
Count start condition	Write “1” (count start) to TYS bit in TYZMR register
Count stop condition	Write “0” (count stop) to TYS bit in TYZMR register
Interrupt request generation timing	In half of count source, after timer Y underflows during secondary period (at the same time as the CNTR, output change) [Timer Y interrupt]
$\overline{INT2}$/CNTR1 pin functions	Pulse output Use timer mode when using this pin as a programmable I/O port.
Read from timer	Count value can be read out by reading TYPR register. Same applies to PREY register(1).
Write to timer	Value written to TYPR register is written to only reload register. Same applies to TYSC register and PREY register(2).
Select function	• Output level latch select function The output level during primary and secondary periods is selected by the TYOPL bit. • Programmable waveform generation output switching function When the TYOCNT bit in the TYZOC register is set to “0”, the output from TYOUT is inverted synchronously when Timer Y underflows during the secondary period. And when set to “1”, a value in the P3_2 bit is output from TYOUT synchronously when Timer Y underflows during the secondary period(3).

NOTES:
1. Even when counting the secondary period, read out the TYPR register.
2. The set value in the TYPR register and TYSC register are made effective by writing a value to the TYPR register. The written values are reflected to the waveform output from the next primary period after writing to the TYPR register.
3. The TYOCNTbit is enabled in the following timings
   • When count starts
   • When Timer Y interrupt request is generated

   Therefore, pulse is output from the next primary period depending on the setting value of the TYOCNT bit

Timer Y, Z mode register

b7	b6	b5	b4	b3	b2	b1	b0
					1		1

Symbol: TYZMR Address: 0080_{16} After reset: 00_{16}

Bit symbol	Bit name	Function	RW
TYMOD0	Timer Y operation mode bit	1 : Programmable waveform generation mode	RW
R1EDG	$\overline{INT2}$/CNTR1 polarity switching bit(1, 3)	Disabled in programmable waveform generation mode	RW
TYWC	Timer Y write control bit	Set to “1” in programmable waveform generation mode(2).	RW
TYS	Timer Y count start flag	0 : Stops counting 1 : Starts counting	RW
TZMOD0	Timer Z-related bit		RW
TZMOD1			RW
TZWC			RW
TZS			RW

NOTES:
1. The IR bit in the INT2IC register may be set to “1” (interrupt requested) when the R1EDG bit is rewritten. Refer to the paragraph 19.2.5 “Changing Interrupt Factor” in the Usage Notes Reference Book.
2. When TYS bit= 1 (starts counting), the timer Y count value is written to the reload register only. When TYS bit=0 (stops counting), the timer Y count value is written to both reload register and counter.
3. The $\overline{INT2}$ interrupt request is not generated when the TYMOD0 bit is set to “1” (programmable waveform generation mode).

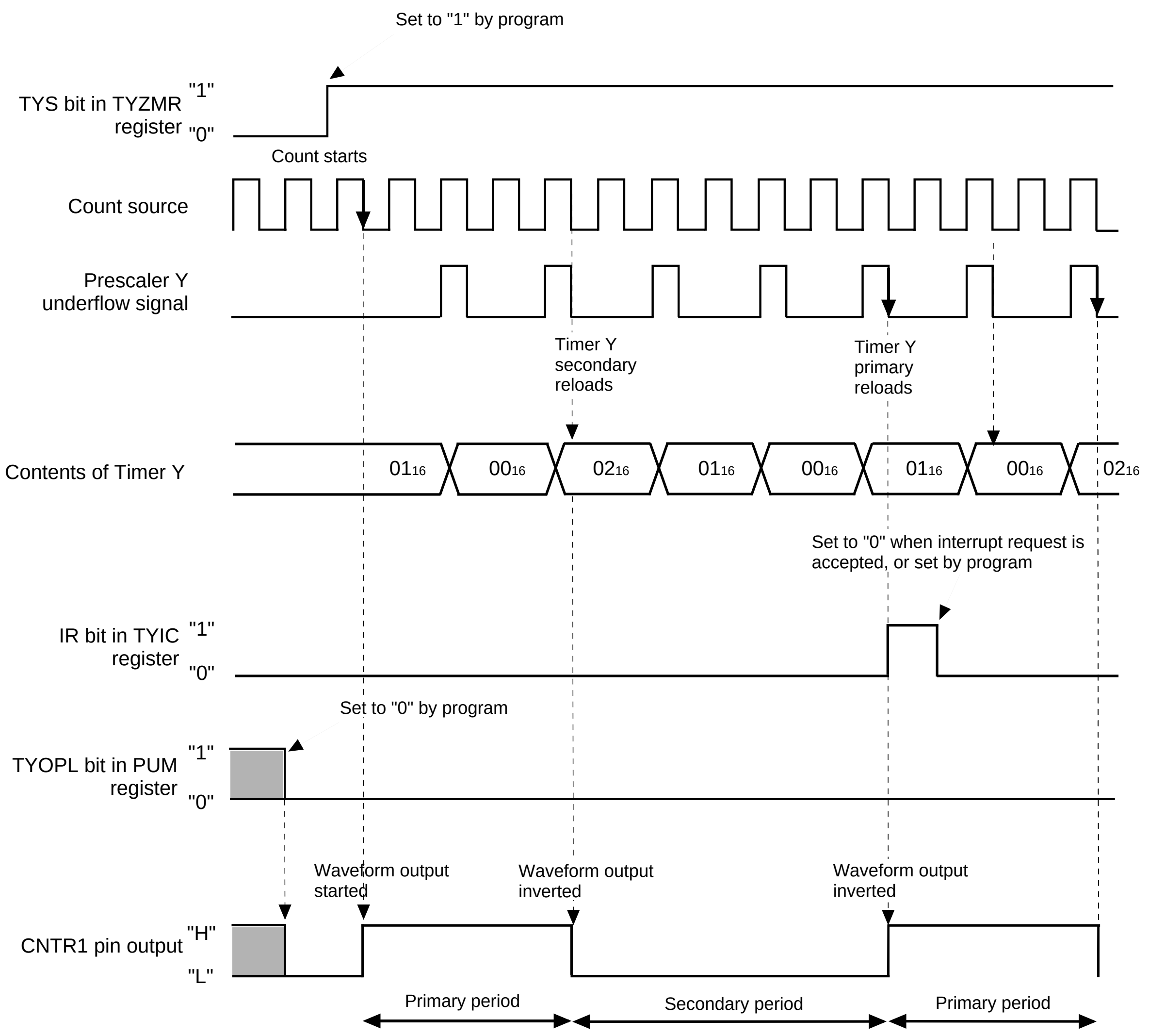
Timer Y, Z waveform output control register

b7	b6	b5	b4	b3	b2	b1	b0
				0	0	0	0

Symbol: PUM Address: 0084_{16} After reset: 00_{16}

Bit symbol	Bit name	Function	RW
— (b3-b0)	Reserved bit	Must set to “0”	RW
TYOPL	Timer Y output level latch	0 : Outputs "H" for primary period Outputs "L" for secondary period Outputs "L" when the timer is stopped 1 : Outputs "L" for primary period Outputs "H" for secondary period Outputs "H" when the timer is stopped	RW
TZOPL	Timer Z-related bits		RW
INOSTG			RW
INOSEG			RW

Figure 12.16 TYZMR Register and PUM Register in Programmable Waveform Generation Mode



Conditions: PREY=01_{16}, TYPR=01_{16}, TYSC=02_{16}
TYZOC register TYOCNT bit = 0

Figure 12.17 Timer Y Operation Example in Programmable Waveform Generation Mode

12.3 Timer Z

Timer Z is an 8-bit timer with an 8-bit prescaler and has two reload registers-Timer Z Primary and Timer Z Secondary. Figure 12.18 shows a block diagram of Timer Z. Figures 12.19 to 12.21 show the TYZMR, PREZ, TZSC, TZPR, TYZOC, PUM, and TCSS registers.

Timer Z has the following four operation modes.

- Timer mode: The timer counts an internal count source or Timer Y underflow.
- Programmable waveform generation mode: The timer outputs pulses of a given width successively.
- Programmable one-shot generation mode: The timer outputs one-shot pulse.
- Programmable wait one-shot generation mode: The timer outputs delayed one-shot pulse.

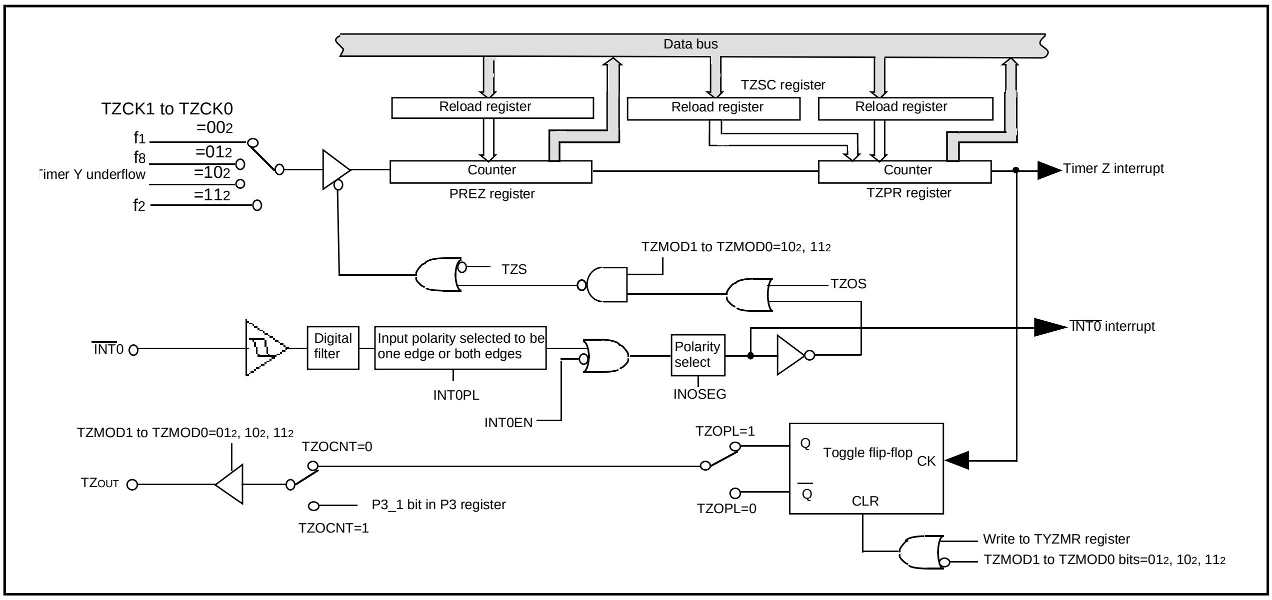


Figure 12.18 Timer Z Block Diagram

Timer Y, Z mode register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After reset
TYZMR	0080₁₆	00₁₆

Bit symbol	Bit name	Function	RW
TYMOD0	Timer Y operation mode bit	0 : Timer mode 1 : Programmable waveform generation mode	RW
R1EDG	INT2/CNTR1 polarity switching bit(1)	0 : Rising edge 1 : Falling edge	RW
TYWC	Timer Y write control bit	Function varies depending on the operation mode	RW
TYS	Timer Y count start flag	0 : Stops counting 1 : Starts counting	RW
TZMOD0	Timer Z operation mode bit	b5 b4 0 0 : Timer mode 0 1 : Programmable waveform generation mode 1 0 : Programmable one-shot generation mode 1 1 : Programmable wait one-shot generation mode	RW
TZMOD1			RW
TZWC	Timer Z write control bit	Function varies depending on the operation mode	RW
TZS	Timer Z count start flag	0 : Stops counting 1 : Starts counting	RW

NOTES:
1. The IR bit in the INT2IC register may be set to “1” (interrupt requested) when the R1EDG bit is rewritten. Refer to the paragraph 19.2.5 “Changing Interrupt Factor” in the Usage Notes Reference Book.

Figure 12.19 TYZMR Register

Prescaler Z register

b7 b0

Symbol PREZ · Address 0085_{16} · After reset FF_{16}

Mode	Function	Setting range	RW
Timer mode	Internal count source or Timer Y underflow is counted	00_{16} to FF_{16}	RW
Programmable waveform generation mode	Internal count source or Timer Y underflow is counted	00_{16} to FF_{16}	RW
Programmable one-shot generation mode	Internal count source or Timer Y underflow is counted	00_{16} to FF_{16}	RW
Programmable wait one-shot generation mode	Internal count source or Timer Y underflow is counted	00_{16} to FF_{16}	RW

Timer Z Secondary register

b7 b0

Symbol TZSC · Address 0086_{16} · After reset FF_{16}

Mode	Function	Setting range	RW
Timer mode	Invalid	—	—
Programmable waveform generation mode	Underflow of Prescaler Z is counted(1)	00_{16} to FF_{16}	WO(2)
Programmable one-shot generation mode	Invalid	—	—
Programmable wait one-shot generation mode	Underflow of Prescaler Z is counted (One-shot width is counted)	00_{16} to FF_{16}	WO

NOTES:
1. Each value in the TZPR register and TZSC register is reloaded to the counter alternately for counting.
2. The count value can be read out by reading the TZSC register even when the secondary period is being counted.

Timer Z Primary register

b7 b0

Symbol TZPR · Address 0087_{16} · After reset FF_{16}

Mode	Function	Setting range	RW
Timer mode	Underflow of Prescaler Z is counted	00_{16} to FF_{16}	RW
Programmable waveform generation mode	Underflow of Prescaler Z is counted(1)	00_{16} to FF_{16}	RW
Programmable one-shot generation mode	Underflow of Prescaler Z is counted (One-shot width is counted)	00_{16} to FF_{16}	RW
Programmable wait one-shot generation mode	Underflow of Prescaler Z is counted (Wait period is counted)	00_{16} to FF_{16}	RW

NOTES:
1. Each value in the TZPR register and TZSC register is reloaded to the counter alternately for counting.

Timer Y, Z output control register(3)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol TYZOC · Address $008A_{16}$ · After reset 00_{16}

Bit symbol	Bit name	Function	RW
TZOS	Timer Z one-shot start bit(1)	0 : Stops one-shot 1 : Starts one-shot	RW
TYOCNT	Timer Y programmable waveform generation output switching bit(2)	0 : Outputs programmable waveform 1 : Outputs the value of $P3_2$ port register	RW
TZOCNT	Timer Z programmable waveform generation output switching bit(2)	0 : Outputs programmable waveform 1 : Outputs the value of $P3_1$ port register	RW
— (b7-b3)	Nothing is assigned. When write, set to "0". When read, its content is "0".		—

NOTES:
1. This bit is set to "0" when the output of one-shot waveform is completed. The TZOS bit should be set to "0" if the one-shot waveform output is terminated by setting the TZS bit in the TYZMR to "0" during the waveform output.
2. This bit is enabled only when operating in programmable waveform generation mode.
3. If executing an instruction which changes this register when the TZOS bit is “1” (during the count), the TZOS is automatically set to “0” when the count completes while the instruction is executed. If this causes some problems, execute an instruction which changes this register when the TZOS bit is “0” (one shot stop).

Figure 12.20 PREZ Register, TZSC Register, TZPR Register, and TYZOC Register

Timer Y, Z waveform output control register

b7	b6	b5	b4	b3	b2	b1	b0
				0	0	0	0

Symbol: PUM Address: 0084_{16} After reset: 00_{16}

Bit symbol	Bit name	Function	RW
(b3-b0)	Reserved bit	Must set to “0”	RW
TYOPL	Timer Y output level latch	Function varies depending on the operation mode	RW
TZOPL	Timer Z output level latch	Function varies depending on the operation mode	RW
INOSTG	$\overline{INT0}$ pin one-shot trigger control bit(2) (Timer Z)	0 : $\overline{INT0}$ pin one-shot trigger invalid 1 : $\overline{INT0}$ pin one-shot trigger valid	RW
INOSEG	$\overline{INT0}$ pin one-shot trigger polarity select bit(1) (Timer Z)	0 : Edge trigger at falling edge 1 : Edge trigger at rising edge	RW

NOTES:
1. The INOSEG bit is valid only when the INT0PL bit in the INTEN register is "0" (one-edge).
2. The INOSGT bit must be set to "1" after the INT0EN bit in the INTEN register and the INOSEG bit in the PUM register are set.

Timer count source setting register

b7	b6	b5	b4	b3	b2	b1	b0
0	0						

Symbol: TCSS Address: $008E_{16}$ After reset: 00_{16}

Bit symbol	Bit name	Function	RW
TXCK0	Timer X count source select bit(1)	b1 b0 0 0 : f_1 0 1 : f_8 1 0 : f_{32} 1 1 : f_2	RW
TXCK1			RW
TYCK0	Timer Y count source select bit(1)	b3 b2 0 0 : f_1 0 1 : f_8 1 0 : f_{RING} 1 1 : Selects input from $CNTR_1$ pin	RW
TYCK1			RW
TZCK0	Timer Z count source select bit(1)	b5 b4 0 0 : f_1 0 1 : f_8 1 0 : Selects Timer Y underflow 1 1 : f_2	RW
TZCK1			RW
(b7-b6)	Reserved bit	Must be set to “0”	RW

NOTES:
1. Avoid switching a count source, while a counter is in progress. Timer counter must be stopped before switching a count source.

Figure 12.21 PUM Register and TCSS Register

12.3.1 Timer Mode

In this mode, the timer counts an internally generated count source or Timer Y underflow (see "Table 12.9 Timer Mode Specifications"). The Timer Z secondary is unused in timer mode. Figure 12.22 shows the TYZMR register and PUM register in timer mode.

Table 12.9 Timer Mode Specifications

Item	Specification
Count source	f_1, f_2, f_8, Timer Y underflow
Count operation	• Down-count • When the timer underflows, it reloads the reload register contents before continuing counting (When the Timer Z underflows, the contents of the Timer Z primary reload register is reloaded.)
Divide ratio	1/(n+1)(m+1) n: set value in PREZ register, m: set value in TZPR register
Count start condition	Write "1" (count start) to TZS bit in TYZMR register
Count stop condition	Write "0" (count stop) to TZS bit in TYZMR register
Interrupt request generation timing	• When Timer Z underflows [Timer Z interrupt]
TZOUT pin function	Programmable I/O port
$\overline{\text{INT0}}$ pin function	Programmable I/O port, or $\overline{\text{INT0}}$ interrupt input
Read from timer	Count value can be read out by reading TZPR register. Same applies to PREZ register.
Write to timer(1)	Value written to TZPR register is written to both reload register and counter or written to reload register only. Selected by program. Same applies to PREZ register.

NOTES:

1. The IR bit in the TZIC register is set to "1" (interrupt requested) if you write to the TZPR or PREZ register while both of the following conditions are met.
   <Conditions>
   • TZWC bit in TYZMR register is set to "0" (write to reload register and counter simultaneously)
   • TZS bit in TYZMR register is set to "1" (count start)
   To write to the TZPR or PREZ register in the above state, disable interrupts before the writing.

Timer Y, Z mode register

b7	b6	b5	b4	b3	b2	b1	b0
		0	0				

Symbol TYZMR — Address 0080_{16} — After reset 00_{16}

Bit symbol	Bit name	Function	RW
TYMOD0	Timer Y-related bit		RW
R1EDG			RW
TYWC			RW
TYS			RW
TZMOD0	Timer Z operation mode bit	b5 b4 0 0 : Timer mode	RW
TZMOD1			RW
TZWC	Timer Z write control bit(1)	0 : Write to reload register and counter 1 : Write to reload register only	RW
TZS	Timer Z count start flag	0 : Stops counting 1 : Starts counting	RW

NOTES:
1. When TZS bit=1 (starts counting), the value set in the TZWC bit is valid. If TZWC bit=0, the timer Z count value is written to both reload register and counter. If TZWC bit=1, the timer Z count value is written to the reload register only.
When TZS bit=0 (stops counting), the timer Z count value is written to both reload register and counter regardless of how the TZWC bit is set.

Timer Y, Z waveform output control register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0		0	0	0	0

Symbol PUM — Address 0084_{16} — After reset 00_{16}

Bit symbol	Bit name	Function	RW
—— (b3-b0)	Reserved bit	Must set to “0”	RW
TYOPL	Timer Y-related bit		RW
TZOPL	Timer Z output level latch	Must set to “0” in timer mode	RW
INOSTG	$\overline{\text{INT0}}$ pin one-shot trigger control bit	Must set to “0” in timer mode	RW
INOSEG	$\overline{\text{INT0}}$ pin one-shot trigger polarity select bit	Must set to “0” in timer mode	RW

Figure 12.22 TYZMR Register and PUM Register in Timer Mode

12.3.2 Programmable Waveform Generation Mode

In this mode, an signal output from the TZOUT pin is inverted each time the counter underflows, while the values in the TZPR register and TZSC register are counted alternately (see "Table 12.10 Programmable Waveform Generation Mode Specifications"). A counting starts by counting the value set in the TZPR register. Figure 12.23 shows TYZMR and PUM registers in this mode. The Timer Z operates in the same way as the Timer Y in this mode. See Figure 12.17 (Timer Y operation example in programmable waveform generation mode).

Table 12.10 Programmable Waveform Generation Mode Specifications

Item	Specification
Count source	f_1, f_2, f_8, Timer Y underflow
Count operation	• Down-count • When the timer underflows, it reloads the contents of primary reload register and secondary reload register alternately before continuing counting.
Output waveform width and period	Primary period : $(n+1)(m+1)/f_i$ Secondary period : $(n+1)(p+1)/f_i$ Period : $(n+1)\{(m+1)+(p+1)\}/f_i$ f_i : Count source frequency n: Set value in PREZ register, m: Set value in TZPR register, p: Set value in TZSC register
Count start condition	Write "1" (count start) to the TZS bit in the TYZMR register
Count stop condition	Write "0" (count stop) to the TZS bit in the TYZMR register
Interrupt request generation timing	In half of count source, after timer Z underflows during secondary period (at the same time as the TZout output change) [Timer Z interrupt]
TZOUT pin function	Pulse output Use timer mode when using this pin as a programmable I/O port.
$\overline{INT0}$ pin functions	Programmable I/O port, or $\overline{INT0}$ interrupt input
Read from timer	Count value can be read out by reading TZPR register. Same applies to PREZ register(2).
Write to timer	Value written to TZPR register is written to reload register only. Same applies to TZSC register and PREZ register(3).
Select function	• Output level latch select function The output level during primary and secondary periods is selected by the TZOPL bit. • Programmable waveform generation output switching function The output from TZOUT is inverted synchronously when Timer Z underflows by setting the TZOCNT bit in the TYZOC register to "0". A value in the P3_1 bit is output from the TZOUT by setting to "1"(3).

NOTES:
1. Even when counting the secondary period, read out the TZPR register.
2. The set value in the TZPR register and TZSC register are made effective by writing a value to the TZPR register. The set values are reflected to the waveform output beginning with the next primary period after writing to the Timer Z primary register.
3. The TZOCNTbit is enabled in the following timings
   • When count starts
   • When Timer Z interrupt request is generated
   Therefore, pulse is output from the next primary period depending on the setting value of the TZOCNT bit.

Timer Y, Z mode register

b7	b6	b5	b4	b3	b2	b1	b0
	1	0	1				

Symbol	Address	After reset
TYZMR	0080_{16}	00_{16}

Bit symbol	Bit name	Function	RW
TYMOD0	Timer Y-related bit		RW
R1EDG			RW
TYWC			RW
TYS			RW
TZMOD0	Timer Z operation mode bit	b5 b4 0 1 : Programmable waveform generation mode	RW
TZMOD1			RW
TZWC	Timer Z write control bit	Set to "1" in programmable waveform generation mode(1)	RW
TZS	Timer Z count start flag	0 : Stops counting 1 : Starts counting	RW

NOTES:
1. When TZS bit=1(starts counting), the timer Y count vaue is written to the reload register only.
When TZS bit=0(stops counting), the timer Y count value is written to both reload register and counter.

Timer Y, Z waveform output control register

b7	b6	b5	b4	b3	b2	b1	b0
0	0			0	0	0	0

Symbol	Address	After reset
PUM	0084_{16}	00_{16}

Bit symbol	Bit name	Function	RW
— (b3-b0)	Reserved bit	Must set to “0”	RW
TYOPL	Timer Y-related bit		RW
TZOPL	Timer Z output level latch	0 : Outputs "H" for primary period Outputs "L" for secondary period Outputs "L" when the timer is stopped 1 : Outputs "L" for primary period Outputs "H" for secondary period Outputs "H" when the timer is stopped	RW
INOSTG	$\overline{INT0}$ pin one-shot trigger control bit	Must set to “0” in programmable waveform generation mode	RW
INOSEG	$\overline{INT0}$ pin one-shot trigger polarity select bit	Must set to “0” in programmable waveform generation mode	RW

Figure 12.23 TYZMR Register and PUM Register in Programmable Waveform Generation Mode

12.3.3 Programmable One-shot Generation Mode

In this mode, upon program command or external trigger input (input to the $\overline{\text{INT0}}$ pin), the microcomputer outputs the one-shot pulse from the TZ_{OUT} pin (see “Table 12.11 Programmable One-shot Generation Mode Specifications”). When a trigger occurs, the timer starts operating from the point only once for a given period equal to the set value in the TZPR register. The TZSC is unused in this mode. Figure 12.24 shows the TYZMR register and PUM register in this mode. Figure 12.25 shows an operation example in this mode.

Table 12.11 Programmable One-shot Generation Mode Specifications

Item	Specification
Count source	f_1, f_2, f_8, Timer Y underflow
Count operation	• Downcounts set value in TZPR register • When the timer underflows, it reloads the contents of reload register before completing counting. • When a count stops, the timer reloads the contents of the reload register before it stops.
Divide ratio	(n+1)(m+1)/fi n: set value in PREZ register, m: set value in TZPR register
Count start condition	• Set TZOS bit in TYZOC register to “1” (start one-shot)(1) • Input active trigger to $\overline{\text{INT0}}$ pin(2)
Count stop condition	• When reloading is completed after count value was set to "00_{16}" • When TZS bit in TYZMR register is set to “0” (stop counting) • When TZOS bit in TYZOC register is set to “0” (stop one-shot)
Interrupt request generation timing	In half cycles of count source, after the timer underflows (at the same time as the TZout output ends) [Timer Z interrupt]
TZ_{OUT} pin function	Pulse output Use timer mode when using this pin as a programmable I/O port.
$\overline{\text{INT0}}$ pin function	Programmable I/O port, external interrupt input pin, or external trigger input pin • When the INOSTG bit in the PUM register is set to “0” ($\overline{\text{INT0}}$ one-shot trigger disabled) Programmable I/O port or $\overline{\text{INT0}}$ interrupt input • When the INOSTG bit in the PUM register is set to “1” ($\overline{\text{INT0}}$ one-shot trigger enabled) external trigger ($\overline{\text{INT0}}$ interrupt input)
Read from timer	Count value can be read out by reading TZPR register. Same applies to PREZ register.
Write to timer	Value written to TZPR register is written to reload register only(3). Same applies to PREZ register.
Select function	• Output level latch select function Output level for one-shot pulse waveform is selected by TZOPL bit. • $\overline{\text{INT0}}$ pin one-shot trigger control function and polarity select function Trigger input from $\overline{\text{INT0}}$ pin can be set to active or inactive by INOSTG bit. Also, an active trigger's polarity can be selected by INOSEG bit.

NOTES:
1. The TZS bit in the TYZMR register must be set to "1" (start counting).
2. The TZS bit must be set to "1" (start counting), the INT0EN bit in the INTEN register to "1" (enabling $\overline{\text{INT0}}$ input), and the INOSTG bit in the PUM register to "1" (enabling $\overline{\text{INT0}}$ one-shot trigger).
Although the trigger input during counting cannot be acknowledged, the $\overline{\text{INT0}}$ interrupt request is generated.
3. The set values are reflected beginning with the next one-shot pulse after writing to the TZPR register.

Timer Y, Z mode register

b7	b6	b5	b4	b3	b2	b1	b0
	1	1	0				

Symbol: TYZMR Address: 0080_{16} After reset: 00_{16}

Bit symbol	Bit name	Function	RW
TYMOD0	Timer Y-related bit		RW
R1EDG			RW
TYWC			RW
TYS			RW
TZMOD0	Timer Z operation mode bit	b5 b4 1 0 : Programmable one-shot generation mode	RW
TZMOD1			RW
TZWC	Timer Z write control bit	Set to "1" in programmable one-shot generation mode(1)	RW
TZS	Timer Z count start flag	0 : Stops counting 1 : Starts counting	RW

NOTES:
1. When the TZS bit is set to “1”(count starts), the count value is written to the reload register only.
   When the TZS bit is set to “0”(count stops), the count value is written to both the reload register and counter.

Timer Y, Z waveform output control register

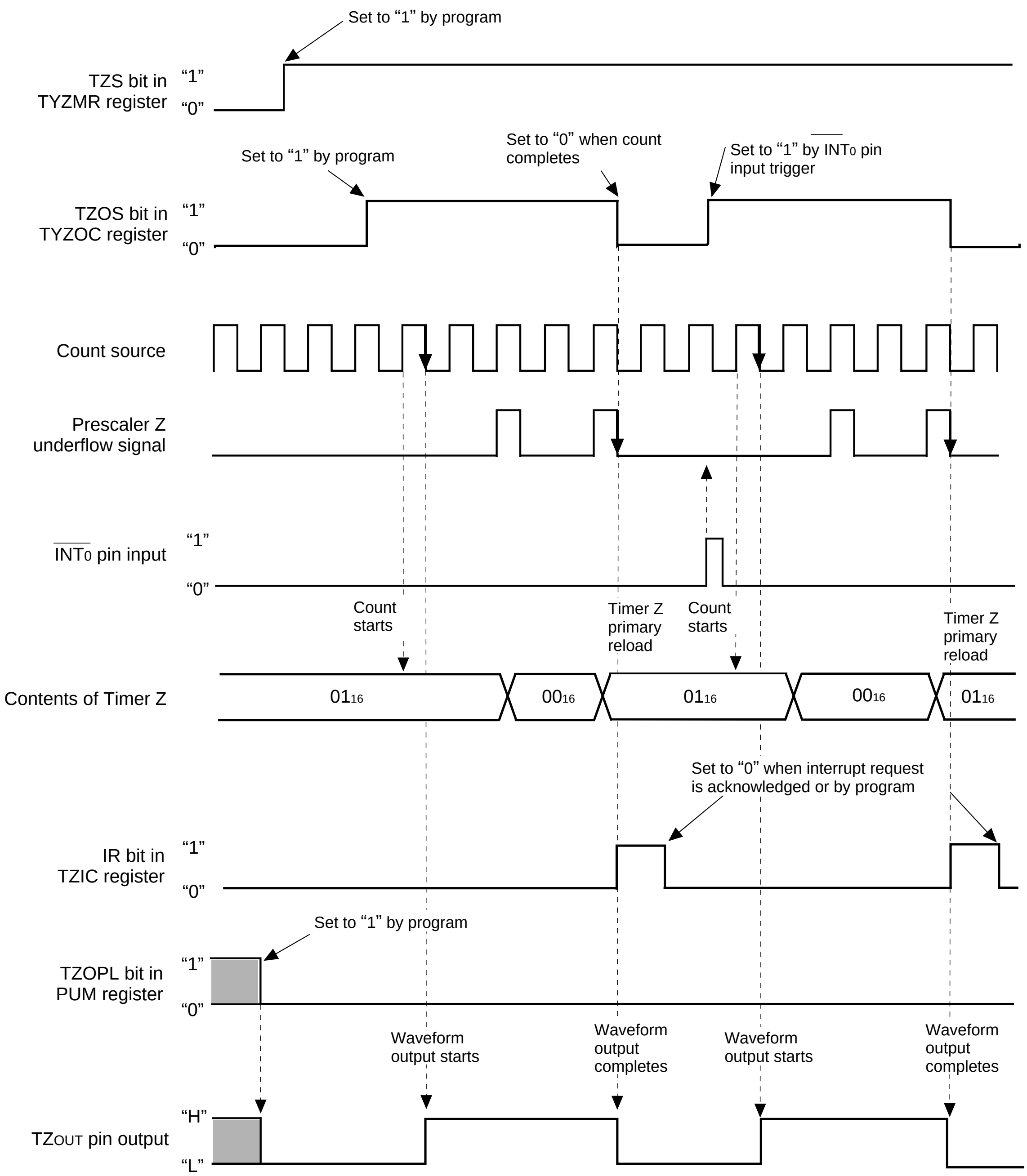
b7	b6	b5	b4	b3	b2	b1	b0
				0	0	0	0

Symbol: PUM Address: 0084_{16} After reset: 00_{16}

Bit symbol	Bit name	Function	RW
— (b3-b0)	Reserved bit	Must set to “0”	RW
TYOPL	Timer Y-related bit		RW
TZOPL	Timer Z output level latch	0 : Outputs "H" level one-shot pulse. Outputs "L" when the timer is stopped. 1 : Outputs "L" level one-shot pulse Outputs "H" when the timer is stopped.	RW
INOSTG	$\overline{\text{INT0}}$ pin one-shot trigger control bit(2)	0 : $\overline{\text{INT0}}$ pin one-shot trigger disabled 1 : $\overline{\text{INT0}}$ pin one-shot trigger enabled(2)	RW
INOSEG	$\overline{\text{INT0}}$ pin one-shot trigger polarity select bit(1)	0 : Edge trigger at falling edge 1 : Edge trigger at rising edge	RW

NOTES:
1. The INOSEG bit is valid only when the INT0PL bit in the INTEN register is set to "0" (one-edge).
2. The INOSGT bit must be set to “1” after the INT0EN bit in the INTEN register and the INOSEG bit in the PUM register are set.
   When setting the INOSTG bit to "1" ($\overline{\text{INT0}}$ pin one-shot trigger enabled), the INT0F0 and INT0F1 bits in the INT0F register must be set.
   The INOSTG bit must be set to “0” ($\overline{\text{INT0}}$ pin one-shot trigger disabled) after the TZS bit in the TYZMR register is set to “0” (count stop).

Figure 12.24 TYZMR Register and PUM Register in Programmable One-shot Generation Mode



The above applies to the following conditions;
PREZ=01₁₆, TZPR=01₁₆
TZOPL bit in PUM register=0, INOSTG bit= 1(INT0 one-shot trigger enabled)
INOSEG bit= 1(rising edge trigger)

Figure 12.25 Operation Example in Programmable One-shot Generation Mode

12.3.4 Programmable Wait One-shot Generation Mode

In this mode, upon program or external trigger input (input to the $\overline{\text{INT0}}$ pin), the microcomputer outputs the one-shot pulse from the TZOUT pin after waiting for a given length of time (see “Table 12.12 Programmable Wait One-shot Generation Mode Specifications”). When a trigger occurs, from this point, the timer starts outputting pulses only once for a given length of time equal to the set value in the TZSC register after waiting for a given length of time equal to the set value in the TZPR register. Figure 12.26 shows the TYZMR and PUM registers in this mode. Figure 12.27 shows an operation example in this mode.

Table 12.12 Programmable Wait One-shot Generation Mode Specifications

Item	Specification
Count source	f_1, f_2, f_8, Timer Y underflow
Count operation	• Downcounts set value in Timer Z primary • When a counting of TZPR register underflows, the timer reloads the contents of TZSC register before continuing counting. • When a counting of TZSC register underflows, the timer reloads the contents of TZPR register before completing counting. • When a count stops, the timer reloads the contents of the reload register before it stops.
Wait time	(n+1)(m+1)/fi n: set value in PREZ register, m: set value in TZPR register
One-shot pulse output time	(n+1)(p+1)/fi n : set value in PREZ, p: set value in TZSC register
Count start condition	• Set TZOS bit in TYZOC register to “1” (start one-shot)(1) • Input active trigger to $\overline{\text{INT0}}$ pin(2)
Count stop condition	• When reloading is completed after count value at counting TZSC register was set to "00_{16}" • When TZS bit in TYZMR register is set to “0” (stop counting) • When TZOS bit in TYZOC register is set to “0” (stop one-shot)
Interrupt request generation timing	In half cycles of count source, after count value at counting TZSC register is set "00_{16}" (at the same time as the TZout output change) [Timer Z interrupt]
TZOUT pin function	Pulse output Use timer mode when using this pin as a programmable I/O port.
$\overline{\text{INT0}}$ pin function	Programmable I/O port, $\overline{\text{INT0}}$ interrupt input or external trigger input • When the INOSTG bit in the PUM register is set to “0” ($\overline{\text{INT0}}$ one-shot trigger disabled) Programmable I/O port or $\overline{\text{INT0}}$ interrupt input • When the INOSTG bit in the PUM register is set to “1” ($\overline{\text{INT0}}$ one-shot trigger enabled) external trigger ($\overline{\text{INT0}}$ interrupt input)
Read from timer	Count value can be read out by reading TZPR register. Same applies to PREZ register.
Write to timer	Value written to TZPR register and PREZ register are written to reload register only(3). Same applies to TZSC register.
Select function	• Output level latch select function Output level for one-shot pulse waveform is selected by TZOPL bit. • $\overline{\text{INT0}}$ pin one-shot trigger control function and polarity select function Trigger input from $\overline{\text{INT0}}$ pin can be set to active or inactive by INOSTG bit. Also, an active trigger's polarity can be selected by INOSEG bit.

NOTES:
1. The TZS bit in the TYZMR register must be set to "1" (start counting).
2. The TZS bit must be set to "1" (start counting), the INT0EN bit in the INTEN register to "1" (enabling $\overline{\text{INT0}}$ input), and the INOSTG bit in the PUM register to "1" (enabling INT0 one-shot trigger).
Although the trigger input during counting cannot be acknowledged, the $\overline{\text{INT0}}$ interrupt request is generated.
3. The set values are reflected beginning with the next one-shot pulse after writing to the TZPR register.

Timer Y, Z mode register

b7	b6	b5	b4	b3	b2	b1	b0
	1	1	1				

Symbol: TYZMR Address: 0080$_{16}$ After reset: 00$_{16}$

Bit symbol	Bit name	Function	RW
TYMOD0	Timer Y-related bit		RW
R1EDG			RW
TYWC			RW
TYS			RW
TZMOD0	Timer Z operation mode bit	b5 b4 1 1 : Programmable wait one-shot generation mode	RW
TZMOD1			RW
TZWC	Timer Z write control bit	Must set to "1" in programmable wait one-shot generation mode(1)	RW
TZS	Timer Z count start flag	0 : Stops counting 1 : Starts counting	RW

NOTES:
1. When TZS bit=1(starts counting), the timer Z count value is written to the reload register only.
When TZS bit=0(stops counting), the timer Z count value is written to both reload register and counter.

Timer Y, Z waveform output control register

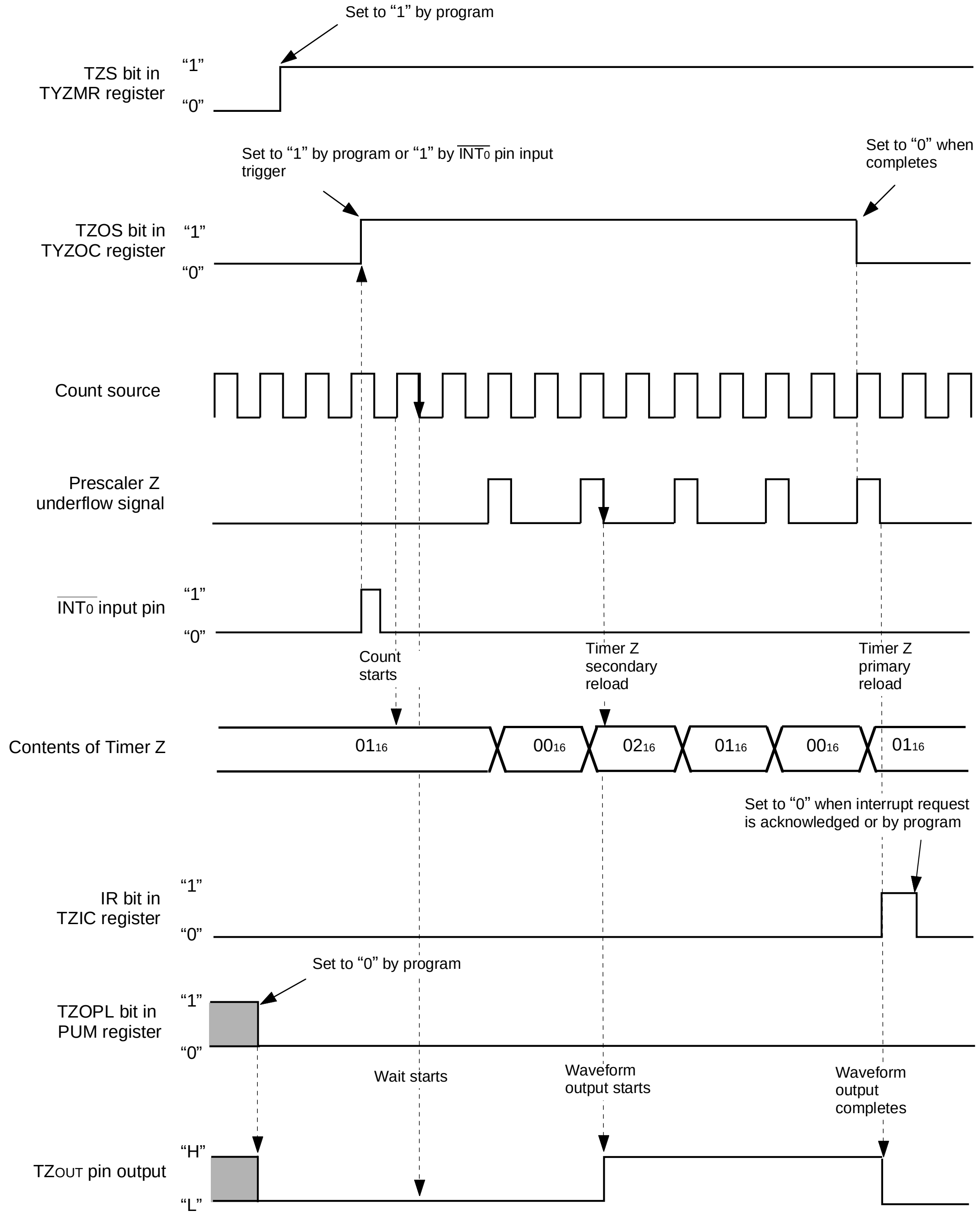
b7	b6	b5	b4	b3	b2	b1	b0
				0	0	0	0

Symbol: PUM Address: 0084$_{16}$ After reset: 00$_{16}$

Bit symbol	Bit name	Function	RW
— (b3-b0)	Reserved bit	Must set to "0"	RW
TYOPL	Timer Y-related bit		RW
TZOPL	Timer Z output level latch	0 : Outputs "H" level one-shot pulse. Outputs "L" when the timer is stopped. 1 : Outputs "L" level one-shot pulse Outputs "H" when the timer is stopped.	RW
INOSTG	$\overline{INT0}$ pin one-shot trigger control bit(2)	0 : $\overline{INT0}$ pin one-shot trigger disabled 1 : $\overline{INT0}$ pin one-shot trigger enabled(2)	RW
INOSEG	$\overline{INT0}$ pin one-shot trigger polarity select bit(1)	0 : Edge trigger at falling edge 1 : Edge trigger at rising edge	RW

NOTES:
1. The INOSEG bit is valid only when the INT0PL bit in the INTEN register is set to "0" (one-edge).
2. The INOSGT bit must be set to "1" after the INT0EN bit in the INTEN register and the INOSEG bit in the PUM register are set.
When setting the INOSTG bit to "1" ($\overline{INT0}$ pin one-shot trigger enabled), the INT0F0 and INT0F1 bits in the INT0F register must be set.
The INOSTG bit must be set to "0" ($\overline{INT0}$ pin one-shot trigger disabled) after the TZS bit in the TYZMR register is set to "0" (count stop).

Figure 12.26 TYZMR Register and PUM Register in Programmable Wait One-shot Generation Mode



The above applies to the following conditions;
PREZ=01_{16}, TZPR=01_{16}, TZSC=02_{16}
TZOPL bit in PUM register=0, INOSTG bit=1($\overline{INT0}$ one-shot trigger enabled)
INOSEG bit=1(rising edge trigger)

Figure 12.27 Operation Example in Programmable Wait One-shot Generation Mode

12.4 Timer C

Timer C is a 16-bit free-running timer. Figure 12.28 shows a block diagram of Timer C. The Timer C uses an edge input to TCIN pin or the fRING128 clock as trigger to latch the timer count value and generates an interrupt request. The TCIN input has a digital filter and this prevents an error caused by noise or so on from occurring. Table 12.13 shows Timer C specifications. Figure 12.29 shows TC, TM0, TCC0, and TCC1 registers. Figure 12.30 shows an operation example of Timer C.

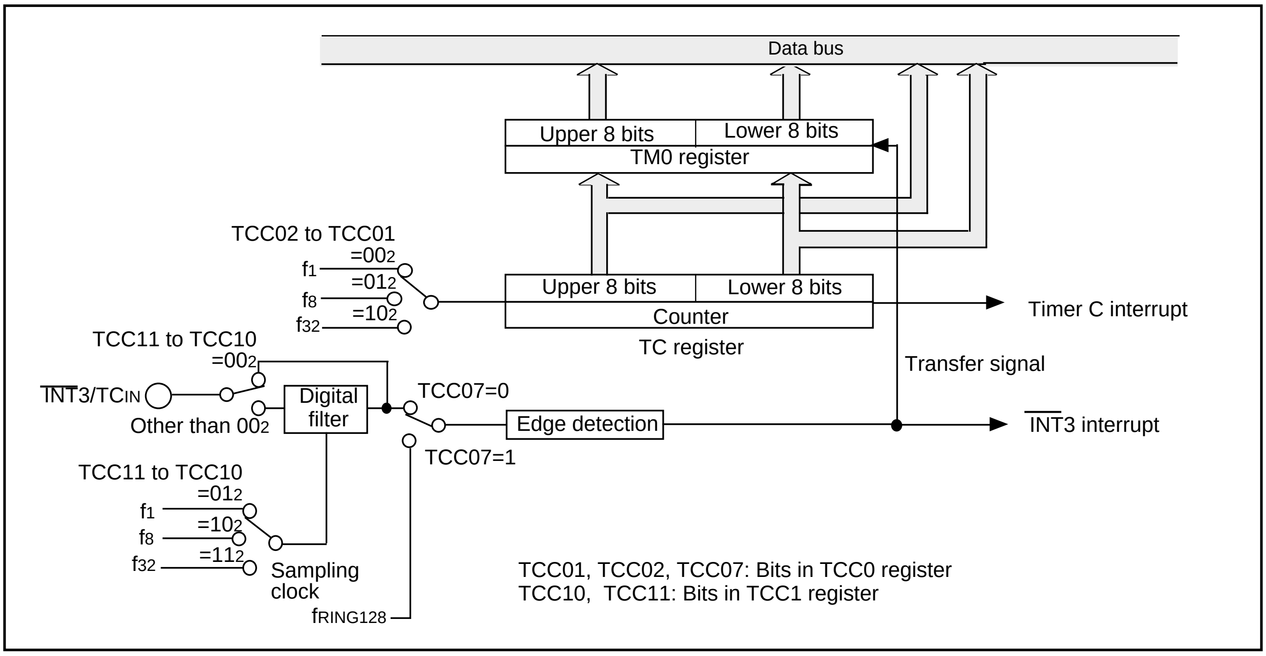


Figure 12.28 Timer C Block Diagram

Table 12.13 Timer C Specifications

Item	Specification
Count source	f1, f8, f32
Count operation	• Count up • Transfer value in TC register to TM0 register at active edge of measurement pulse • Value in TC register is set to “000016” when a counting stops
Count start condition	TCC00 bit in TCC0 register is set to “1” (capture enabled)
Count stop condition	TCC00 bit in TCC0 register is set to “0” (capture disabled)
Interrupt request generation timing	• When active edge of measurement pulse is input [INT3 interrupt] • When Time C underflows [Timer C interrupt]
INT3/TCIN pin function	Programmable I/O or measurement pulse input
Counter value reset timing	When TCC00 bit in TCC0 register is set to “0” (capture disabled)
Read from timer(1)	• Counter value can be read out by reading TC register. • Counter value at measurement pulse active edge input can be read out by reading TM0 register.
Write to timer	Write to TC register and TM0 register is disabled
Select function	• INT3/TCIN switching function Measurement pulse active edge is selected by TCC03 to TCC04 bits • Digital filter function Digital filter sampling frequency is selected by TCC11 to TCC10 bits • Trigger select function TCIN input or fRING128 is selected by TCC07 bit.

NOTES:
1. TC register and TM0 register must be read in 16-bit units.

Timer C register

(b15) b7 (b8) b0 b7 b0

Symbol	Address	After reset
TC	0091_{16}-0090_{16}	0000_{16}

Function	RW
Internal count source is counted "0000_{16}" can be read out by reading when TCC00 bit = 0 (stops counting) Count value can be read out by reading when TCC00 bit = 1 (start counting)	RO

Capture register

(b15) b7 (b8) b0 b7 b0

Symbol	Address	After reset
TM0	$009D_{16}$-$009C_{16}$	0000_{16}

Function	RW
When active edge of measurement pulse is input, the counter value of Timer C is stored	RO

Timer C control register 0

b7 b6 b5 b4 b3 b2 b1 b0: [ ] [0] [0] [ ] [ ] [ ] [ ] [ ]

Symbol	Address	After reset
TCC0	$009A_{16}$	00_{16}

Bit symbol	Bit name	Function	RW
TCC00	Timer C count start bit	0 : Count stop 1 : Count start	RW
TCC01	Timer C count source select bit[1]	b2 b1 0 0 : f_1 0 1 : f_8 1 0 : f_{32} 1 1 : Avoid this setting	RW
TCC02			RW
TCC03	$\overline{INT3}$ interrupt and capture input polarity select bit[1, 2]	b4 b3 0 0 : Rising edge 0 1 : Falling edge 1 0 : Both edges 1 1 : Avoid this setting	RW
TCC04			RW
— (b6-b5)	reserved bit	Set to "0"	RW
TCC07	$\overline{INT3}$ interrupt and capture input switching bit[1, 2]	0 : $\overline{INT3}$ 1 : $f_{RING128}$	RW

NOTES:
1. Change this bit when TCC00 bit is set to “0” (count stop).
2. The IR bit in the INT3IC may be set to “1” (interrupt requested) when the TCC03, TCC04, or TCC07 bit is rewritten. Refer to the paragraph 19.2.5 “Changing Interrupt Factor” in the Usage Notes Reference Book.

Timer C control register 1

b7 b6 b5 b4 b3 b2 b1 b0: [0] [0] [0] [0] [0] [0] [ ] [ ]

Symbol	Address	After reset
TCC1	$009B_{16}$	00_{16}

Bit symbol	Bit name	Function	RW
TCC10	$\overline{INT3}$ input filter select bit[1]	b1 b0 0 0 : No filter 0 1 : Filter with f_1 sampling 1 0 : Filter with f_8 sampling 1 1 : Filter with f_{32} sampling	RW
TCC11			RW
— (b7-b2)	Reserved bit	Set to "0"	RW

NOTES:
1. Input is recognized only when the same value from $\overline{INT3}$ pin is sampled three times in succession.

Figure 12.29 TC Register, TM0 Register, TCC0 Register, and TCC1 Register

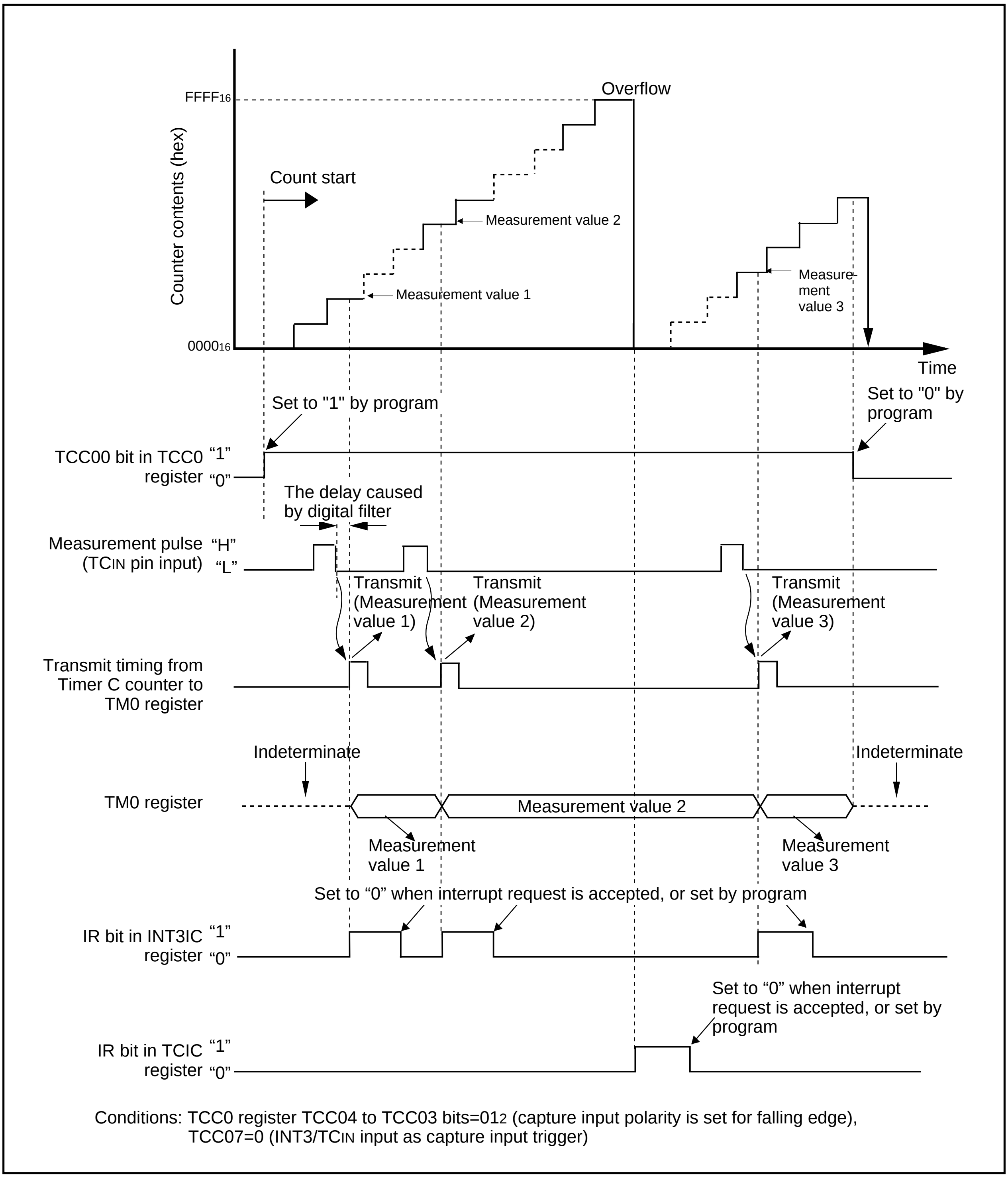


Figure 12.30 Operation Example of Timer C

13. Serial Interface

Serial interface is configured with two channels: UART0 to UART1. UART0 and UART1 each have an exclusive timer to generate a transfer clock, so they operate independently of each other.

Figure 13.1 shows a block diagram of UARTi (i=0, 1). Figure 13.2 shows a block diagram of the UARTi transmit/receive.

UART0 has two modes: clock synchronous serial I/O mode, and clock asynchronous serial I/O mode (UART mode).

UART1 has only one mode, clock asynchronous serial I/O mode (UART mode).

Figures 13.3 to 13.5 show the UARTi-related registers.

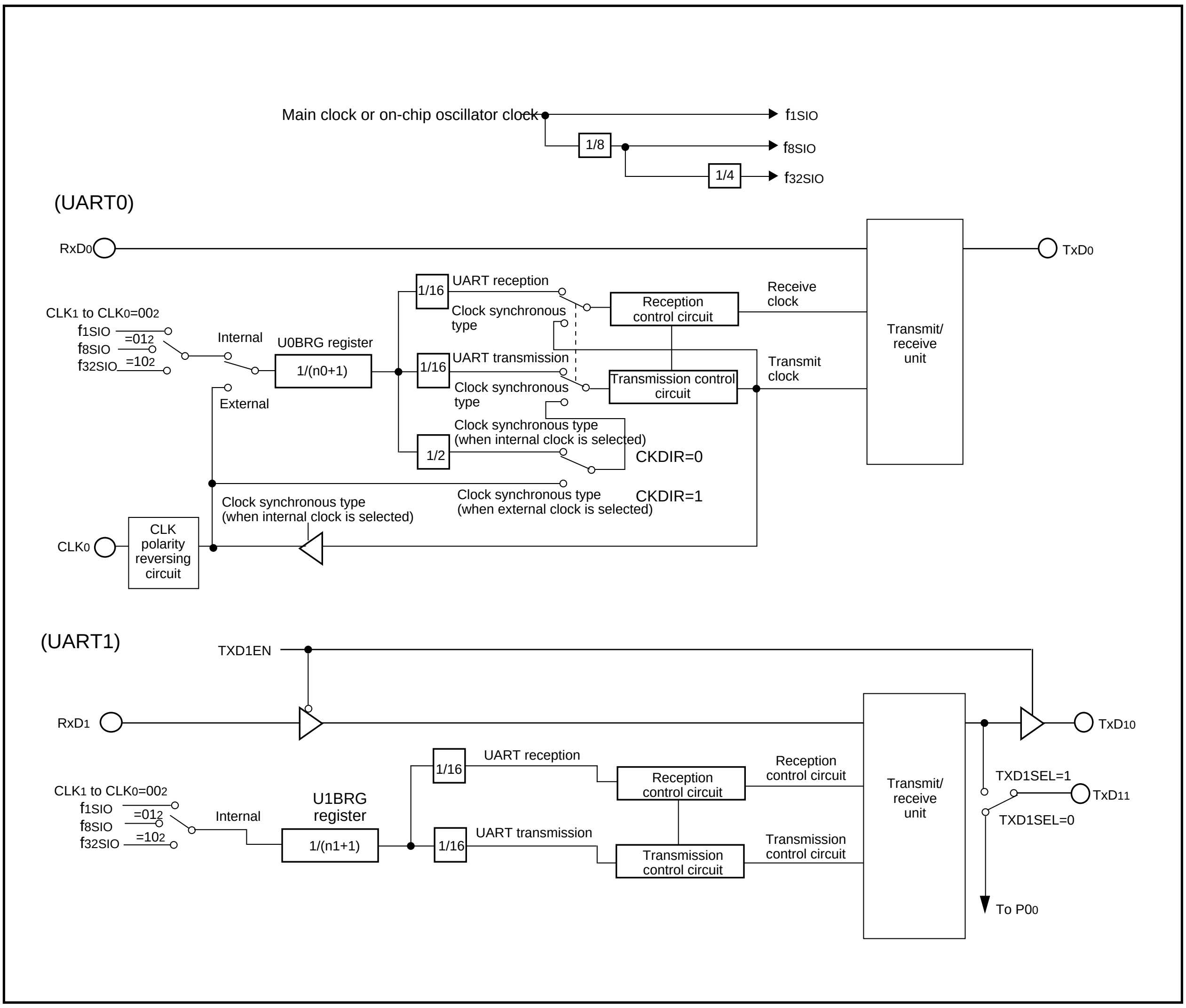


Figure 13.1 UARTi (i=0, 1) Block Diagram

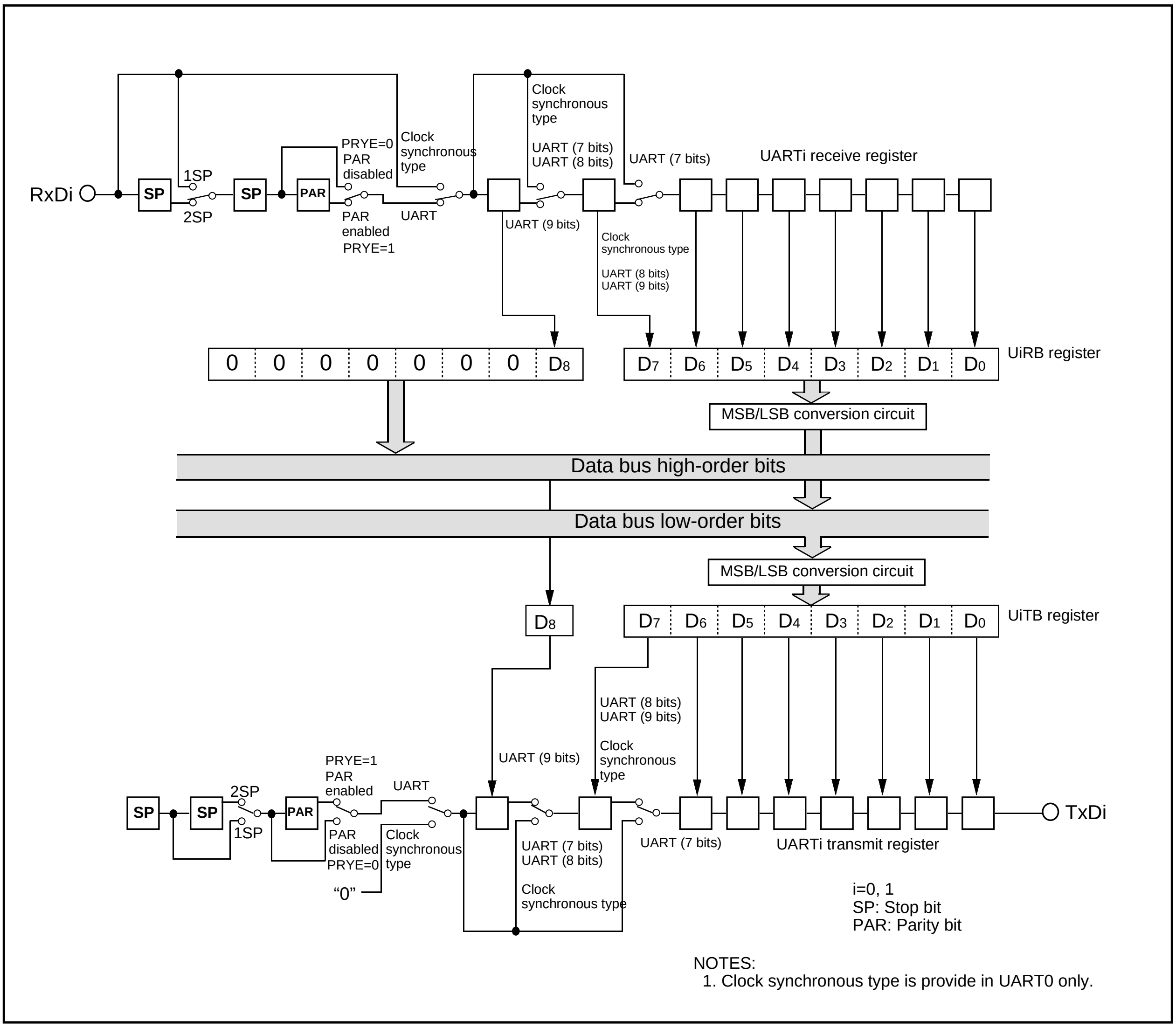
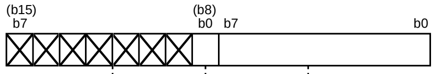


Figure 13.2 UARTi Transmit/Receive Unit

UARTi transmit buffer register[1, 2] (i=0, 1)

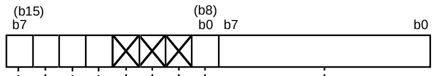


Symbol	Address	After reset
U0TB	$00A3_{16}$-$00A2_{16}$	Indeterminate
U1TB	$00AB_{16}$-$00AA_{16}$	Indeterminate

Bit symbol	Function	RW
— (b8-b0)	Transmit data	WO
— (b15-b9)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.	—

NOTES:
1. When transfer data length is 9-bit long, write high-byte first then low-byte.
2. Use MOV instruction to write to this register.

UARTi receive buffer register[1] (i=0, 1)

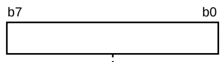


Symbol	Address	After reset
U0RB	$00A7_{16}$-$00A6_{16}$	Indeterminate
U1RB	$00AF_{16}$-$00AE_{16}$	Indeterminate

Bit symbol	Bit name	Function	RW
— (b7-b0)	—	Receive data (D_7 to D_0)	RO
— (b8)	—	Receive data (D_8)	RO
— (b11-b9)	Nothing is assigned. When write, set to "0". When read, its content is indeterminate.		—
OER	Overrun error flag[2]	0 : No overrun error 1 : Overrun error found	RO
FER	Framing error flag[2]	0 : No framing error 1 : Framing error found	RO
PER	Parity error flag[2]	0 : No parity error 1 : Parity error found	RO
SUM	Error sum flag[2]	0 : No error 1 : Error found	RO

NOTES:
1. Read out the UiRB register in 16-bit unit.
2. All of the SUM, PER, FER and OER bits are set to "0" (no error) when the SMD2 to SMD0 bits in the UiMR register are set to "000_2" (serial interface disabled) or the RE bit in the UiC1 register is set to "0" (reception disabled). The SUM bit is set to "0" (no error) when all of the PER, FER and OER bits are set to "0" (no error).
The PER and FER bits are set to "0" even when the higher byte of the UiRB register is read.

UARTi bit rate register[1, 2, 3] (i=0, 1)



Symbol	Address	After reset
U0BRG	$00A1_{16}$	Indeterminate
U1BRG	$00A9_{16}$	Indeterminate

Function	Setting range	RW
Assuming that set value = n, UiBRG divides the count source by n + 1	00_{16} to FF_{16}	WO

NOTES:
1. Write to this register while serial interface is neither transmitting nor receiving.
2. Use MOV instruction to write to this register.
3. After setting the CLK0 to CLK1 bits of the UiC0 register, write to the UiBRG register.

Figure 13.3 U0TB and U1TB Registers, U0RB and U1RB Registers, and U0BRG and U1BRG Registers

UARTi transmit/receive mode register (i=0, 1)

b7	b6	b5	b4	b3	b2	b1	b0
0							

Symbol	Address	After reset
U0MR	$00A0_{16}$	00_{16}
U1MR	$00A8_{16}$	00_{16}

Bit symbol	Bit name	Function	RW
SMD0	Serial interface mode select bit(2)	b2 b1 b0 0 0 0 : Serial interface disabled 0 0 1 : Clock synchronous serial I/O mode 1 0 0 : UART mode transfer data 7 bits long 1 0 1 : UART mode transfer data 8 bits long 1 1 0 : UART mode transfer data 9 bits long Must not be set except above	RW
SMD1			RW
SMD2			RW
CKDIR	Internal/external clock select bit(3)	0 : Internal clock 1 : External clock(1)	RW
STPS	Stop bit length select bit	0 : 1 stop bit 1 : 2 stop bits	RW
PRY	Odd/even parity select bit	Effective when PRYE = 1 0 : Odd parity 1 : Even parity	RW
PRYE	Parity enable bit	0 : Parity disabled 1 : Parity enabled	RW
— (b7)	Reserved bit	Set to “0”	RW

NOTES:
1. Must set the P1_6 bit in the PD1 register to “0” (input).
2. For the U1MR register, the SMD2 to SMD0 bits must not be set except the followings: “000_2”, “100_2”, “101_2”, or “110_2”.
3. Must set the CKDIR bit to “0” (internal clock) in UART1.

UARTi transmit/receive control register 0 (i=0, 1)

b7	b6	b5	b4	b3	b2	b1	b0
			X		0		

Symbol	Address	After reset
U0C0	$00A4_{16}$	08_{16}
U1C0	$00AC_{16}$	08_{16}

Bit symbol	Bit name	Function	RW
CLK0	BRG count source select bit(1)	b1 b0 0 0 : f_{1SIO} is selected 0 1 : f_{8SIO} is selected 1 0 : f_{32SIO} is selected 1 1 : Avoid this setting	RW
CLK1			RW
— (b2)	Reserved bit	Set to “0”	RW
TXEPT	Transmit register empty flag	0 : Data present in transmit register (during transmission) 1 : No data present in transmit register (transmission completed)	RO
— (b4)	Nothing is assigned. When write, set to “0”. When read, its content is indeterminate.		—
NCH	Data output select bit	0 : TxDi pin is a pin of CMOS output 1 : TxDi pin is a pin of N-channel open-drain output	RW
CKPOL	CLK polarity select bit	0 : Transmit data is output at falling edge of transfer clock and receive data is input at rising edge 1 : Transmit data is output at rising edge of transfer clock and receive data is input at falling edge	RW
UFORM	Transfer format select bit	0 : LSB first 1 : MSB first	RW

NOTES:
1. If the BRG count source is switched, set the UiBRG register again.

Figure 13.4 U0MR and U1MR Registers and U0C0 and U1C0 Registers

UARTi transmit/receive control register 1 (i=0, 1)

Symbol	Address	After reset
U0C1	$00A5_{16}$	02_{16}
U1C1	$00AD_{16}$	02_{16}

Bit symbol	Bit name	Function	RW
TE	Transmit enable bit	0 : Transmission disabled 1 : Transmission enabled	RW
TI	Transmit buffer empty flag	0 : Data present in UiTB register 1 : No data present in UiTB register	RO
RE	Receive enable bit(1)	0 : Reception disabled 1 : Reception enabled	RW
RI	Receive complete flag(2)	0 : No data present in UiRB register 1 : Data present in UiRB register	RO
— (b7-b4)	Nothing is assigned. When write, set “0”. When read, its content is “0”.		—

NOTES:
1. As for the UART1, set the TXD1EN bit in the UCON register before setting this bit to reception enabled.
2. The RI bit is set to "0" when the higher byte of the UiRB register is read.

UART transmit/receive control register 2

Symbol	Address	After reset
UCON	$00B0_{16}$	00_{16}

Bit symbol	Bit name	Function	RW
U0IRS	UART0 transmit interrupt cause select bit	0 : Transmit buffer empty (TI = 1) 1 : Transmission completed (TXEPT = 1)	RW
U1IRS	UART1 transmit interrupt cause select bit	0 : Transmit buffer empty (TI = 1) 1 : Transmission completed (TXEPT = 1)	RW
U0RRM	UART0 continuous receive mode enable bit	0 : Continuous receive mode disabled 1 : Continuous receive mode enable	RW
— (b4-b3)	Reserved bit	Must set to “0”	RW
TXD1SEL	Port TxD_{11} switching bit(2)	0 : I/O port $P0_0$ 1 : TxD_{11}	RW
TXD1EN	TxD_{10}/RxD_1 select bit(1, 2)	0 : RxD_1 1 : TxD_{10}	RW
— (b7)	Nothing is assigned. When write, set “0”. When read, its content is “0”.		—

NOTES:
1. For $P3_7$, select “0” (RxD_1) for data receive, and “1” (TxD_{10}) for data transfer.
Set the PD3_7 bit in the PD3 register to “0” (input mode) when receiving.
2. Do not set the TXD1SEL and TXD1EN bits to “1” at the same time since they function independently.

Figure 13.5 U0C1 and U1C1 Registers and UCON Register

13.1 Clock Synchronous Serial I/O Mode

The clock synchronous serial I/O mode uses a transfer clock to transmit and receive data. This mode can be selected with UART0. Table 13.1 lists the specifications of the clock synchronous serial I/O mode. Table 13.2 lists the registers used in clock synchronous serial I/O mode and the register values set.

Table 13.1 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	• Transfer data length: 8 bits
Transfer clock	• CKDIR bit in U0MR register is set to “0” (internal clock): fi/(2(n+1)) fi=f1SIO, f8SIO, f32SIO n=setting value in UiBRG register: 00_{16} to FF_{16} • CKDIR bit is set to “1” (external clock): input from CLK0 pin
Transmission start condition	• Before transmission can start, the following requirements must be met(1) – TE bit in U0C1 register is set to “1” (transmission enabled) – TI bit in U0C1 register is set to “0” (data present in U0TB register)
Reception start condition	• Before reception can start, the following requirements must be met(1) – RE bit in U0C1 register is set to “1” (reception enabled) – TE bit in U0C1 register is set to “1” (transmission enabled) – TI bit in U0C1 register is set to “0” (data present in the U0TB register)
Interrupt request generation timing	• For transmission, one of the following conditions can be selected – U0IRS bit is set to “0” (transmit buffer empty): when transferring data from U0TB register to UART0 transmit register (at start of transmission) – U0IRS bit is set to “1” (transfer completed): when serial interface finished sending data from UARTi transmit register • For reception When transferring data from the UART0 receive register to the U0RB register (at completion of reception)
Error detection	• Overrun error(2) This error occurs if serial interface started receiving the next data before reading the U0RB register and received the 7th bit of the next data
Select function	• CLK polarity selection Transfer data I/O can be chosen to occur synchronously with the rising or the falling edge of the transfer clock • LSB first, MSB first selection Whether to start sending/receiving data beginning with bit 0 or beginning with bit 7 can be selected • Continuous receive mode selection Reception is enabled immediately by reading the U0RB register

NOTES:

1. When an external clock is selected, the conditions must be met while if the U0C0 register 0 CKPOL bit = 0 (transmit data output at the falling edge and the receive data taken in at the rising edge of the transfer clock), the external clock is in the high state; if the CKPOL bit in the U0C0 register is set to “1” (transmit data output at the rising edge and the receive data taken in at the falling edge of the transfer clock), the external clock is in the low state.
2. If an overrun error occurs, the value of U0RB register will be indeterminate. The IR bit of S0RIC register does not change.

Table 13. 2 Registers to Be Used and Settings in Clock Synchronous Serial I/O Mode

Register	Bit	Function
U0TB	0 to 7	Set transmission data
U0RB	0 to 7	Reception data can be read
	OER	Overrun error flag
U0BRG	0 to 7	Set a bit rate
U0MR	SMD2 to SMD0	Set to "001₂"
	CKDIR	Select the internal clock or external clock
U0C0	CLK1 to CLK0	Select the count source for the U0BRG register
	TXEPT	Transmit register empty flag
	NCH	Select TxD0 pin output mode
	CKPOL	Select the transfer clock polarity
	UFORM	Select the LSB first or MSB first
U0C1	TE	Set this bit to "1" to enable transmission/reception
	TI	Transmit buffer empty flag
	RE	Set this bit to "1" to enable reception
	RI	Reception complete flag
UCON	U0IRS	Select the source of UART0 transmit interrupt
	U0RRM	Set this bit to "1" to use continuous receive mode
	TXDISEL	Set to "0"
	TXDIEN	Set to "0"

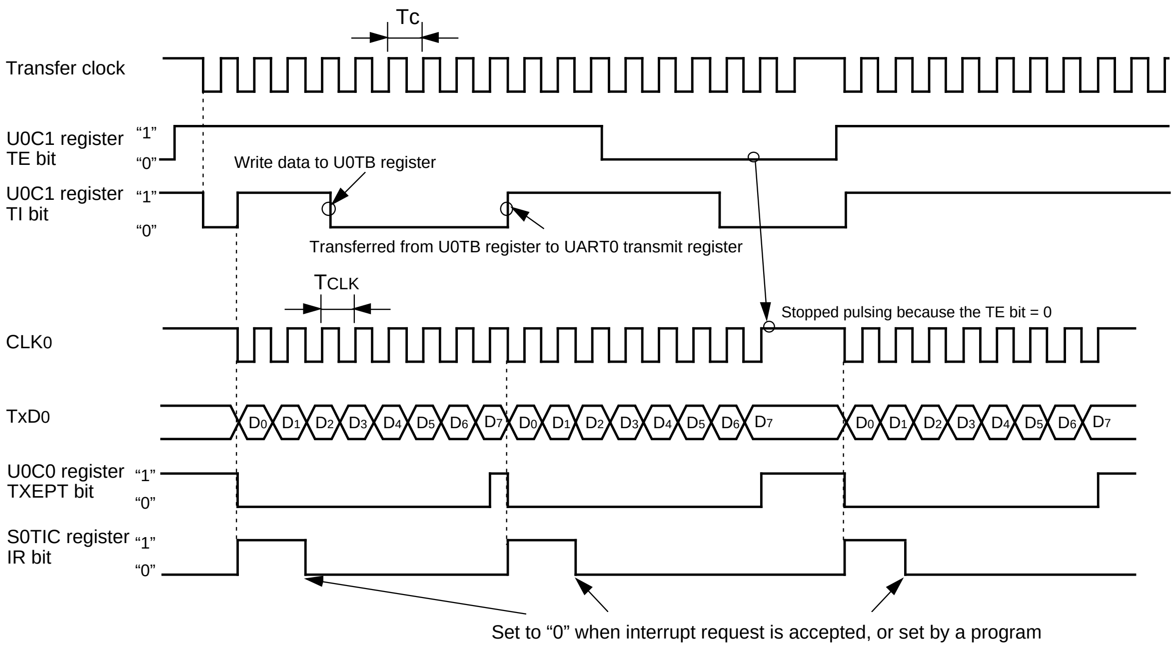
NOTES:
1. Not all register bits are described above. Set those bits to "0" when writing to the registers in clock synchronous serial I/O mode.

Table 13.3 lists the functions of the I/O pins during clock synchronous serial I/O mode. Note that for a period from when the UART0 operation mode is selected to when transfer starts, the TxD0 pin outputs an "H". (If the NCH bit is set to "1"(N-channel open-drain output), this pin is in a high-impedance state.)

Table 13.3 Pin Functions

Pin name	Function	Method of selection
TxD0 (P14)	Serial data output	(Outputs dummy data when performing reception only)
RxD0 (P15)	Serial data input	PD1 register PD1_5 bit=0 (P15 can be used as an input port when performing transmission only)
CLK0 (P16)	Transfer clock output	U0MR register CKDIR bit=0
	Transfer clock input	U0MR register CKDIR bit=1 PD1 register PD1_6 bit=0

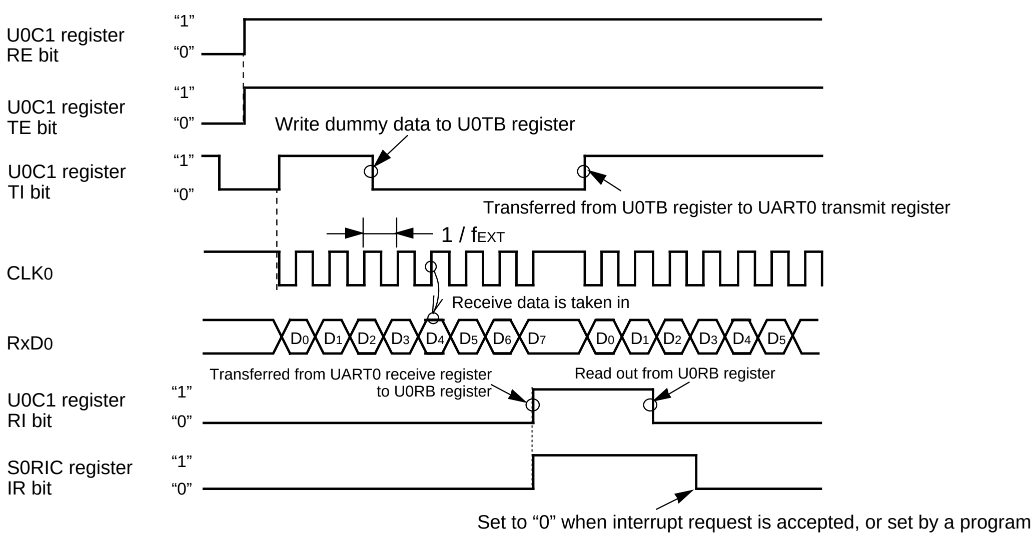
• Example of transmit timing (when internal clock is selected)



Tc = TCLK = 2(n + 1) / fi
fi: frequency of U0BRG count source (f1SIO, f8SIO, f32SIO)
n: value set to U0BRG register

The above timing diagram applies to the case where the register bits are set as follows:
- U0MR register CKDIR bit = 0 (internal clock)
- U0C0 register CKPOL bit = 0 (transmit data output at the falling edge and receive data taken in at the rising edge of the transfer clock)
- U0IRS bit = 0 (an interrupt request occurs when the transmit buffer becomes empty):

• Example of receive timing (when external clock is selected)



The above timing diagram applies to the case where the register bits are set as follows:
- U0MR register CKDIR bit = 1 (external clock)
- U0C0 register CKPOL bit = 0 (transmit data output at the falling edge and receive data taken in at the rising edge of the transfer clock)

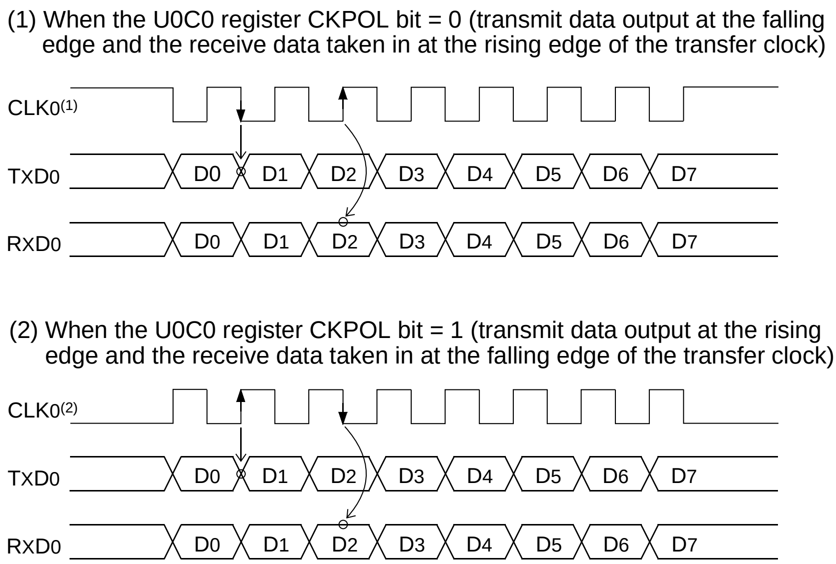
Make sure the following conditions are met when input to the CLK0 pin before receiving data is high:
- U0C1 register TE bit = 1 (transmit enabled)
- U0C1 register RE bit = 1 (receive enabled)
- Write dummy data to the U0TB register

fEXT: frequency of external clock

Figure 13.6 Transmit and Receive Operation

13.1.1 Polarity Select Function

Figure 13.7 shows the polarity of the transfer clock. Use the CKPOL bit in the U0C0 register to select the transfer clock polarity.

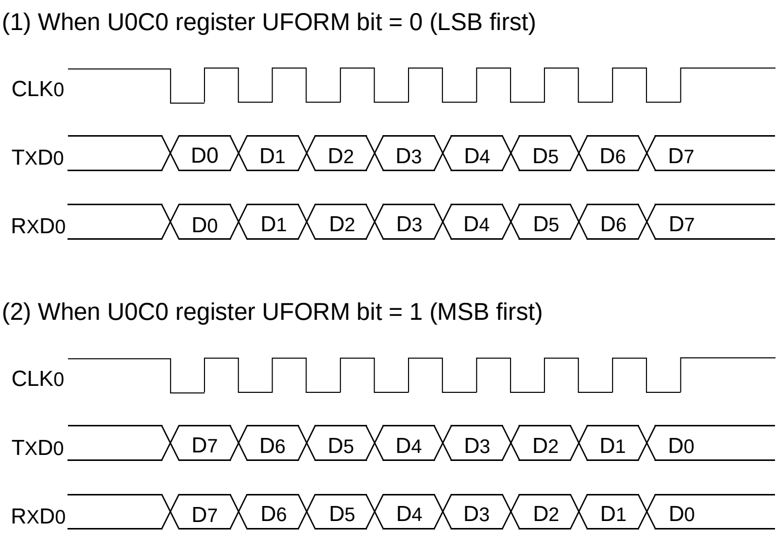


NOTES:
1. When not transferring, the CLK0 pin outputs a high signal.
2. When not transferring, the CLK0 pin outputs a low signal.

Figure 13.7 Transfer Clock Polarity

13.1.2 LSB First/MSB First Select Function

Figure 13.8 shows the transfer format. Use the UFORM bit in the U0C0 register to select the transfer format.



NOTES:
1. This applies to the case where the CKPOL bit in the U0C0 register is set to "0" (transmit data output at the falling edge and the receive data taken in at the rising edge of the transfer clock).

Figure 13.8 Transfer Format

13.1.3 Continuous Receive Mode

Continuous receive mode is held by setting setting the U0RRM bit in the UCON register to “1” (enables continuous receive mode). In this mode, reading the U0RB register sets the TI bit in the U0C1 register to “0”(data in the U0TB register). When the U0RRM bit is set to “1”, do not write dummy data to tge U0TB register in a program.

13.2 Clock Asynchronous Serial I/O (UART) Mode

The UART mode allows transmitting and receiving data after setting the desired bit rate and transfer data format. Tables 13.4 lists the specifications of the UART mode. Table 13.5 lists the registers and settings for UART mode.

Table 13.4 UART Mode Specifications

Item	Specification
Transfer data format	• Character bit (transfer data): selectable from 7, 8 or 9 bits • Start bit: 1 bit • Parity bit: selectable from odd, even, or none • Stop bit: selectable from 1 or 2 bits
Transfer clock	• UiMR(i=0, 1) register CKDIR bit = 0 (internal clock) : fj/(16(n+1)) fj=f_{1SIO}, f_{8SIO}, f_{32SIO} n=setting value in UiBRG register: 00_{16} to FF_{16} • CKDIR bit = “1” (external clock) : f_{EXT}/(16(n+1)) f_{EXT}: input from CLKi pin n=setting value in UiBRG register: 00_{16} to FF_{16}
Transmission start condition	• Before transmission can start, the following requirements must be met – TE bit in UiC1 register= 1 (transmission enabled) – TI bit in UiC1 register = 0 (data present in UiTB register)
Reception start condition	• Before reception can start, the following requirements must be met – RE bit in UiC1 register= 1 (reception enabled) – Start bit detection
Interrupt request generation timing	• For transmission, one of the following conditions can be selected – UiIRS bit = 0 (transmit buffer empty): when transferring data from UiTB register to UARTi transmit register (at start of transmission) – UiIRS bit =1 (transfer completed): when serial interface finished sending data from UARTi transmit register • For reception When transferring data from UARTi receive register to UiRB register (at completion of reception)
Error detection	• Overrun error(1) This error occurs if serial interfaces started receiving the next data before reading UiRB register and received the bit one before the last stop bit of the next data • Framing error This error occurs when the number of stop bits set is not detected • Parity error This error occurs when if parity is enabled, the number of 1’s in parity and character bits does not match the number of 1’s set • Error sum flag This flag is set (= 1) when any of the overrun, framing, and parity errors is encountered
Select function	• TxD_{10}, RxD_1 selection (UART) $P3_7$ pin can be used as RxD_1 pin or TxD_{10} pin in UART1. Select by a program. • TxD_{11} pin selection (UART1) $P0_0$ pin can be used as TxD_{11} pin in UART1 or port $P0_0$. Select by a program.

NOTES:
1. If an overrun error occurs, the value of U0RB register will be indeterminate. The IR bit in the S0RIC register does not change.

Table 13.5 Registers to Be Used and Settings in UART Mode

Register	Bit	Function
UiTB	0 to 8	Set transmission data(1)
UiRB	0 to 8	Reception data can be read(1)
	OER,FER,PER,SUM	Error flag
UiBRG	0 to 7	Set a bit rate
UiMR	SMD2 to SMD0	Set these bits to '100_2' when transfer data is 7 bits long Set these bits to '101_2' when transfer data is 8 bits long Set these bits to '110_2' when transfer data is 9 bits long
	CKDIR	Select the internal clock or external clock(2)
	STPS	Select the stop bit
	PRY, PRYE	Select whether parity is included and whether odd or even
UiC0	CLK0, CLK1	Select the count source for the UiBRG register
	TXEPT	Transmit register empty flag
	NCH	Select TxDi pin output mode
	CKPOL	Set to "0"
	UFORM	LSB first or MSB first can be selected when transfer data is 8 bits long. Set this bit to "0" when transfer data is 7 or 9 bits long.
UiC1	TE	Set this bit to "1" to enable transmission
	TI	Transmit buffer empty flag
	RE	Set this bit to "1" to enable reception
	RI	Reception complete flag
UCON	U0IRS, U1IRS	Select the source of UART0/UART1 transmit interrupt
	U0RRM	Set to "0"
	TXD1SEL	Select output pin for UART1 transfer data
	TXD1EN	Select TxD$_{10}$ or RxD$_1$ to be used

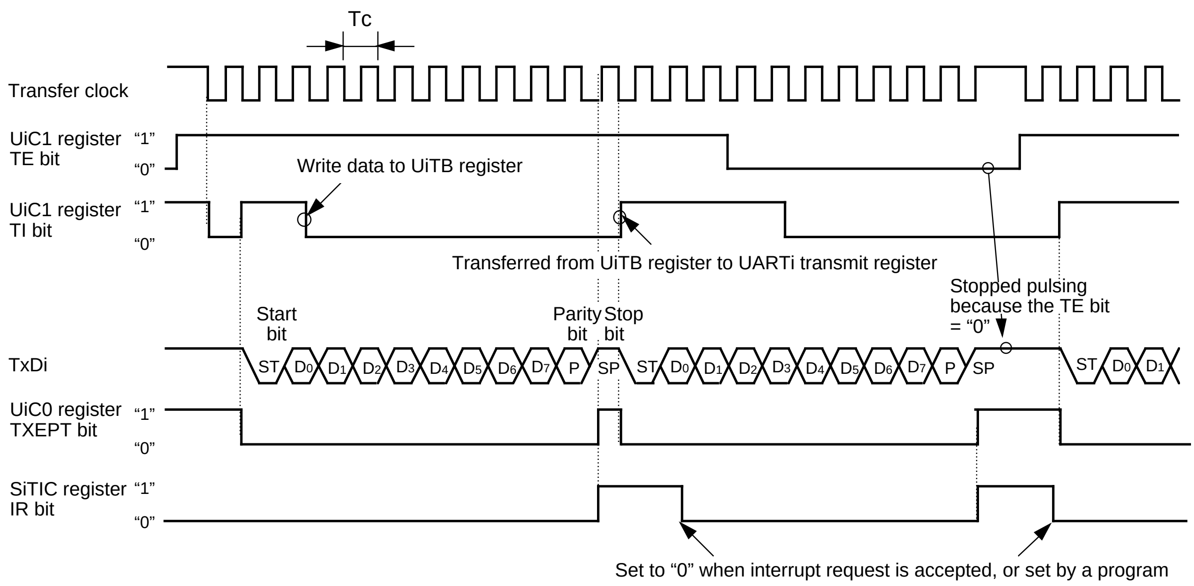
NOTES:
1. The bits used for transmit/receive data are as follows: Bit 0 to bit 6 when transfer data is 7 bits long; bit 0 to bit 7 when transfer data is 8 bits long; bit 0 to bit 8 when transfer data is 9 bits long.
2. An external clock can be selected in UART0 only.

Table 13.6 lists the functions of the input/output pins during UART mode. Note that for a period from when the UARTi operation mode is selected to when transfer starts, the TxDi pin outputs an "H". (If the NCH bit is set to "1"(N-channel open-drain output), this pin is in a high-impedance state.)

Table 13.6 I/O Pin Functions in UART Mode

Pin name	Function	Method of selection
TxD$_0$ (P1$_4$)	Serial data output	(Cannot be used as a port when performing reception only)
RxD$_0$ (P1$_5$)	Serial data input	PD1 register PD1_5 bit=0 (Can be used as an input port when performing transmission only)
CLK$_0$ (P1$_6$)	Programmable I/O port	U0MR register CKDIR bit=0
	Transfer clock input	U0MR register CKDIR bit=1 PD1 register PD1_6 bit=0
TxD$_{10}$/RxD$_1$ (P3$_7$)	Serial data output	TXD1EN=1
	Serial data input	TXD1EN=0, PD3 register PD3_7 bit=0
TxD$_{11}$ (P0$_0$)	Serial data output	Serial data output, TXD1SEL=1

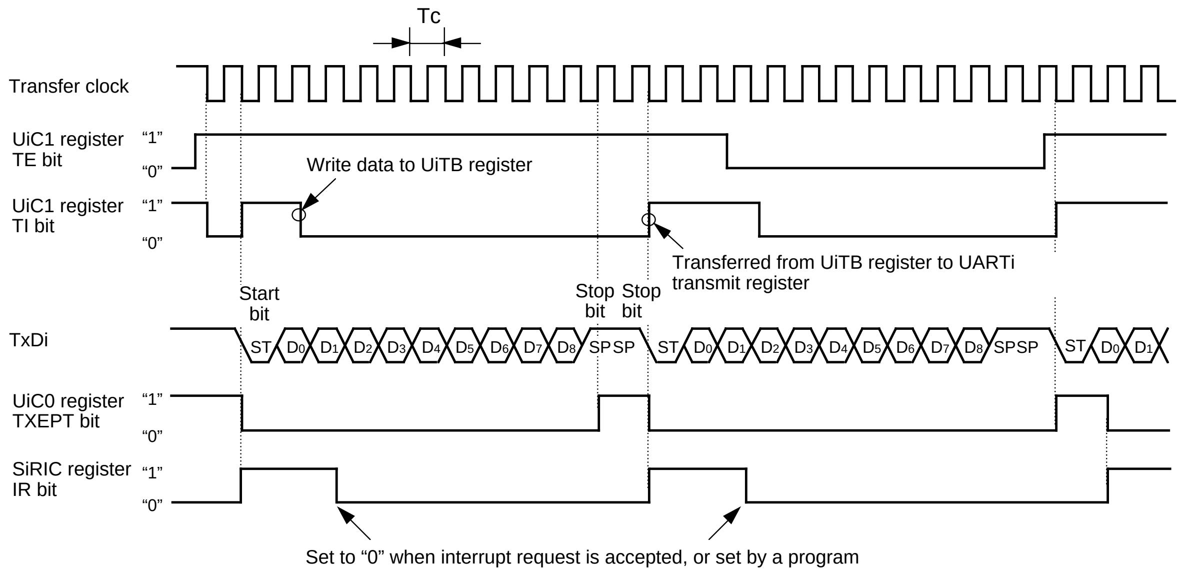
• Example of transmit timing when transfer data is 8 bits long (parity enabled, one stop bit)



The above timing diagram applies to the case where the register bits are set as follows:
- UiMR register PRYE bit = 1 (parity enabled)
- UiMR register STPS bit = 0 (1 stop bit)
- UiIRS bit = 1 (an interrupt request occurs when transmit completed):

Tc = 16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: frequency of UiBRG count source (f1SIO, f8SIO, f32SIO)
fEXT: frequency of UiBRG count source (external clock)
n: value set to UiBRG
i: 0, 1

• Example of transmit timing when transfer data is 9 bits long (parity disabled, two stop bits)



The above timing diagram applies to the case where the register bits are set as follows:
- UiMR register PRYE bit = 0 (parity disabled)
- UiMR register STPS bit = 1 (2 stop bits)
- UiIRS bit = 0 (an interrupt request occurs when transmit buffer becomes empty)

Tc = 16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: frequency of UiBRG count source (f1SIO, f8SIO, f32SIO)
fEXT: frequency of UiBRG count source (external clock)
n: value set to UiBRG
i: 0, 1

Figure 13.9 Transmit Operation

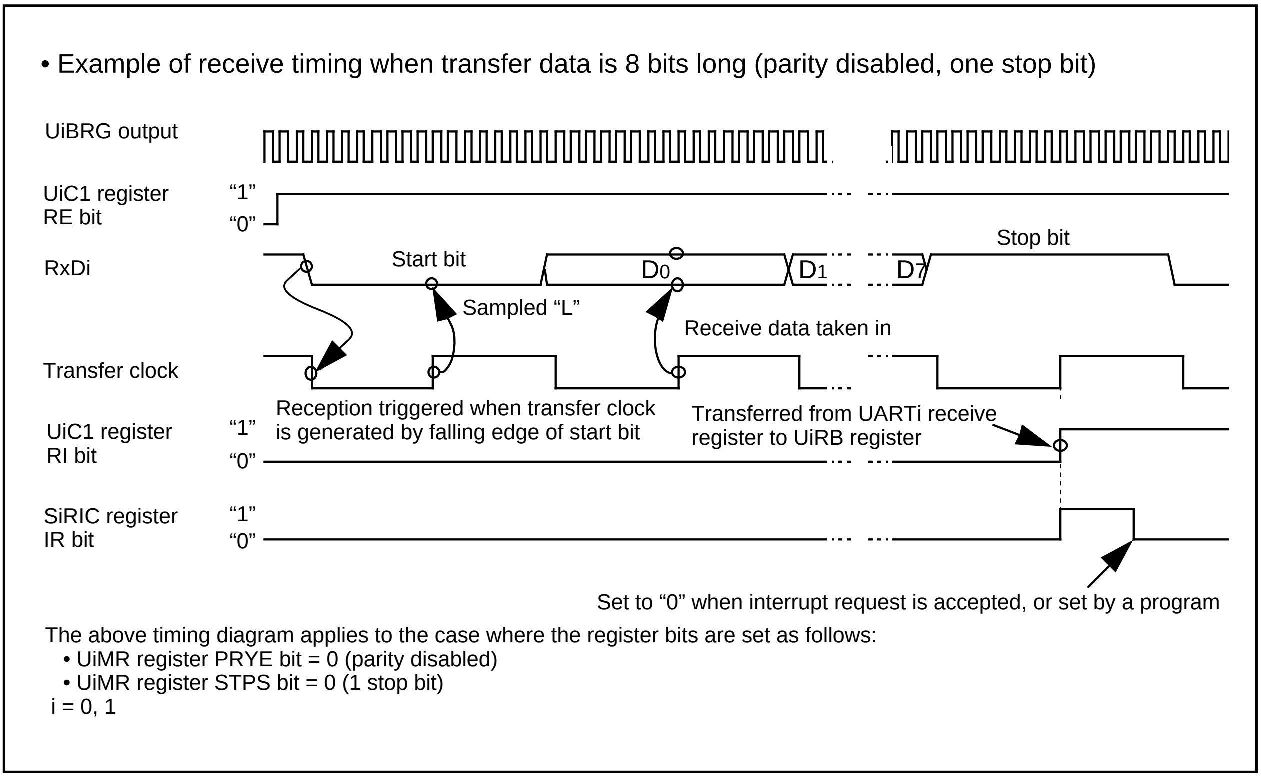


Figure 13.10 Receive Operation

13.2.1 TxD_{10}/RxD_1 Select Function (UART1)

$P3_7$ can be used as TxD_{10} output pin or RxD_1 input pin by selecting with the TXD1EN bit in the UCON register. $P3_7$ is used as TxD_{10} output pin if the TXD1EN bit is set to "1" (TxD_{10}) and used as RxD_1 input pin if set to "0" (RxD_1).

13.2.2 TxD_{11} Select Function (UART1)

$P0_0$ can be used as TxD_{11} output pin or a port by selecting with the TXD1SEL bit in the UCON register. $P0_0$ is used as TxD_{11} output pin if the TXD1SEL bit is set to "1" (TxD_{11}) and used as an I/O port if set to "0" ($P0_0$).

13.2.3 Bit Rate

Divided-by-16 of frequency by the UiBRG (i=0 to 1) register in UART mode is a bit rate.

<UART Mode>

• When selecting internal clock

$$\text{Setting value to the UiBRG register} = \frac{fj}{\text{Bit Rate} \times 16} - 1$$

fj : Count source frequency of the UiBRG register (f1SIO, f8SIO and f32SIO)

• When selecting external clock

$$\text{Setting value to the UiBRG register} = \frac{fEXT}{\text{Bit Rate} \times 16} - 1$$

fEXT : Count source frequency of the UiBRG register (external clock)

Figure 13.11 Calculation Formula of UiBRG (i=0 to 1) Register Setting Value

Table 13.7 Bit Rate Setting Example in UART Mode

Bit Rate (bps)	BRG Count Source	System Clock = 16MHz			System Clock = 8MHz		
		BRG Setting Value	Actual Time(bps)	Error(%)	BRG Setting Value	Actual Time(bps)	Error(%)
1200	f8	103 (67_{16})	1201.92	0.16	51 (33_{16})	1201.92	0.16
2400	f8	51 (33_{16})	2403.85	0.16	25 (19_{16})	2403.85	0.16
4800	f8	25 (19_{16})	4807.69	0.16	12 ($0C_{16}$)	4807.69	0.16
9600	f1	103 (67_{16})	9615.38	0.16	51 (33_{16})	9615.38	0.16
14400	f1	68 (44_{16})	14492.75	0.64	34 (22_{16})	14285.71	–0.79
19200	f1	51 (33_{16})	19230.77	0.16	25 (19_{16})	19230.77	0.16
28800	f1	34 (22_{16})	28571.43	–0.79	16 (10_{16})	29411.76	2.12
31250	f1	31 ($1F_{16}$)	31250.00	0.00	15 ($0F_{16}$)	31250.00	0.00
38400	f1	25 (19_{16})	38461.54	0.16	12 ($0C_{16}$)	38461.54	0.16
51200	f1	19 (13_{16})	50000.00	–2.34	9 (09_{16})	50000.00	–2.34

14. A/D Converter

The A/D converter consists of one 10-bit successive approximation A/D converter circuit with a capacitive coupling amplifier. The analog inputs share the pins with $P0_0$ to $P0_7$. Therefore, when using these pins, make sure the corresponding port direction bits are set to "0" (input mode).

When not using the A/D converter, set the VCUT bit to "0" (Vref unconnected), so that no current will flow from the VREF pin into the resistor ladder, helping to reduce the power consumption of the chip.

The result of A/D conversion is stored in the AD register.

Table 14.1 shows the performance of the A/D converter. Figure 14.1 shows a block diagram of the A/D converter, and Figures 14.2 and 14.3 show the A/D converter-related registers.

Table 14.1 Performance of A/D converter

Item	Performance
Method of A/D conversion	Successive approximation (capacitive coupling amplifier)
Analog input voltage(1)	0V to Vref
Operating clock ϕ_{AD}(2)	AV_{CC} = 5V f_{AD}, divide-by-2 of f_{AD}, divide-by-4 of f_{AD} AV_{CC} = 3V divide-by-2 of f_{AD}, divide-by-4 of f_{AD}
Resolution	8-bit or 10-bit (selectable)
Integral nonlinearity error	AV_{CC} = Vref = 5V • 8-bit resolution ±2LSB • 10-bit resolution ±3LSB AVcc = Vref = 3.3V • 8-bit resolution ±2LSB • 10-bit resolution ±5LSB
Operating modes	One-shot mode and repeat mode(3)
Analog input pins	8 pins (AN_0 to AN_7)
A/D conversion start condition	ADST bit in ADCON0 register is set to "1" (A/D conversion starts)
Conversion speed per pin	• Without sample and hold function 8-bit resolution: 49 ϕ_{AD} cycles, 10-bit resolution: 59 ϕ_{AD} cycles • With sample and hold function 8-bit resolution: 28 ϕ_{AD} cycles, 10-bit resolution: 33 ϕ_{AD} cycles

NOTES:
1. Does not depend on use of sample and hold function.
2. The frequency of ϕ_{AD} must be 10 MHz or less.
   When AVcc is less than 4.2V, ϕ_{AD} must be f_{AD}/2 or less by dividing f_{AD}.
   Without sample and hold function, the ϕ_{AD} frequency should be 250 kHz or more.
   With the sample and hold function, the ϕ_{AD} frequency should be 1 MHz or more.
3. In repeat mode, only 8-bit mode can be used.

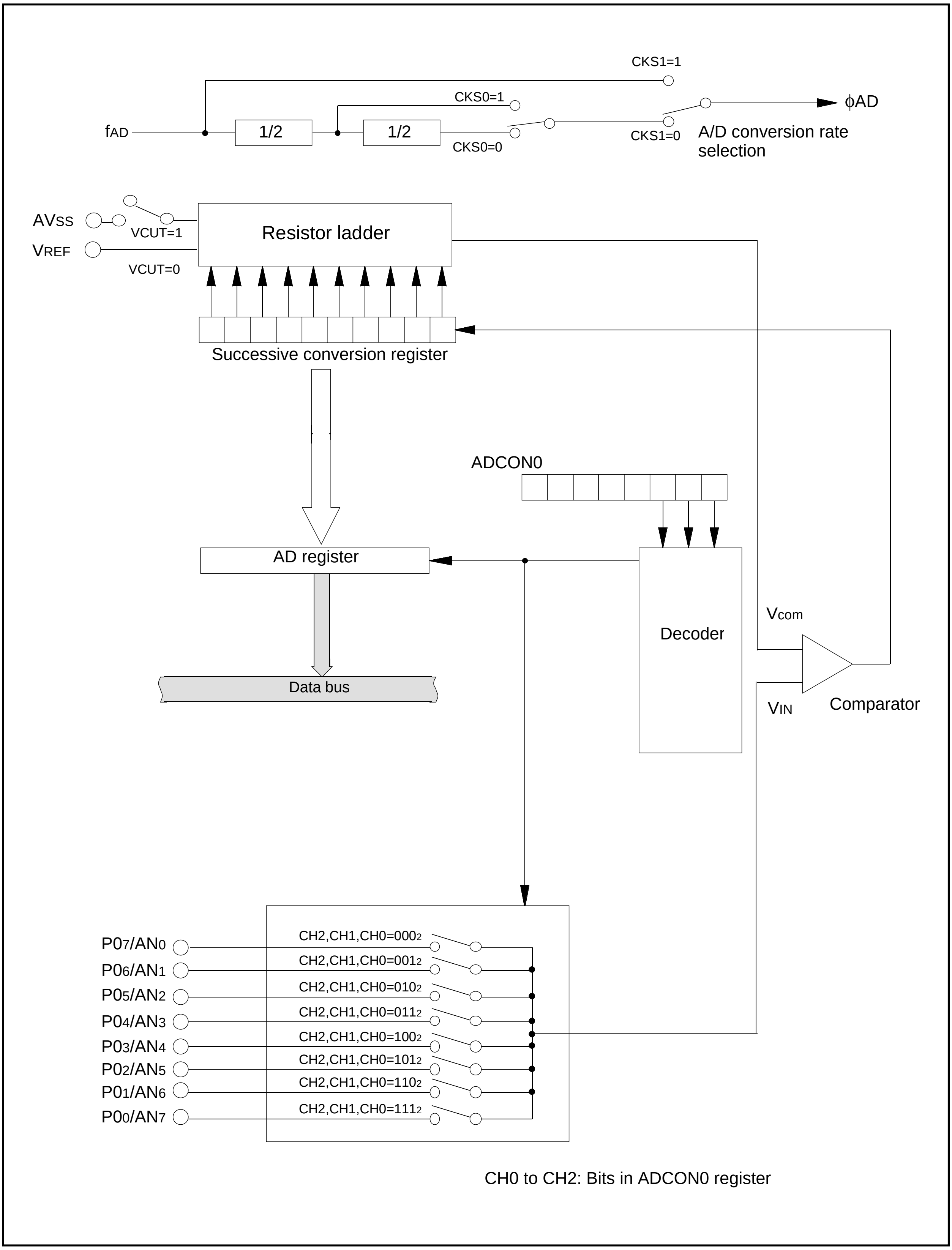


Figure 14.1 A/D Converter Block Diagram

AD control register 0[1]

b7	b6	b5	b4	b3	b2	b1	b0
		0	0				

Symbol	Address	After reset
ADCON0	$00D6_{16}$	$00000XXX_2$

Bit symbol	Bit name	Function	RW
CH0	Analog input pin select bit[2]	b2 b1 b0 0 0 0 : AN_0 is selected 0 0 1 : AN_1 is selected 0 1 0 : AN_2 is selected 0 1 1 : AN_3 is selected 1 0 0 : AN_4 is selected 1 0 1 : AN_5 is selected 1 1 0 : AN_6 is selected 1 1 1 : AN_7 is selected	RW
CH1			RW
CH2			RW
MD	AD operation mode select bit 0[2]	0 : One-shot mode 1 : Repeat mode	RW
— (b4)	Reserved bit	Set to “0”	RW
— (b5)	Reserved bit	Set to “0”	RW
ADST	A/D conversion start flag	0 : A/D conversion disabled 1 : A/D conversion started	RW
CKS0	Frequency select bit 0[3]	0 : $f_{AD}/4$ is selected 1 : $f_{AD}/2$ is selected	RW

NOTES:
1. If the ADCON register is rewritten during A/D conversion, the conversion result is indeterminate.
2. When changing A/D operation mode, set analog input pin again.
3. This bit is valid when the CKS1 bit in the ADCON1 register is set to “0”.

AD control register 1[1]

b7	b6	b5	b4	b3	b2	b1	b0
0	0				0	0	0

Symbol	Address	After reset
ADCON1	$00D7_{16}$	00_{16}

Bit symbol	Bit name	Function	RW
— (b2-b0)	Reserved bit	Set to “0”	RW
BITS	8/10-bit mode select bit[2]	0 : 8-bit mode 1 : 10-bit mode	RW
CKS1	Frequency select bit 1[3]	0 : CKS0 bit in ADCON0 register is valid 1 : f_{AD} is selected	RW
VCUT	Vref connect bit[4]	0 : Vref not connected 1 : Vref connected	RW
— (b6-b7)	Reserved bit	Set to “0”	RW

NOTES:
1. If the ADCON1 register is rewritten during A/D conversion, the conversion result is indeterminate.
2. In repeat mode, the BITS bit must be set to “0” (8-bit mode).
3. The ϕ_{AD} frequency must be 10 MHz or less.
4. If the VCUT bit is reset from “0” (Vref unconnected) to “1” (Vref connected), wait for 1 µs or more before starting A/D conversion.

Figure 14.2 ADCON0 Register and ADCON1 Register

AD control register 2(1)

b7 b6 b5 b4 b3 b2 b1 b0: × × × × 0 0 0 (b0)

Symbol: ADCON2 | Address: 00D4$_{16}$ | After reset: 00$_{16}$

Bit symbol	Bit name	Function	RW
SMP	AD conversion method select bit	0 : Without sample and hold 1 : With sample and hold	RW
— (b3-b1)	Reserved bit	Set to “0”	RW
— (b7-b4)	Nothing is assigned. When write, write “0”. When read, its content is “0”.		—

NOTES:
1. If the ADCON2 register is rewritten during A/D conversion, the conversion result is indeterminate.

AD register

Symbol: AD | Address: 00C1$_{16}$-00C0$_{16}$ | After reset: Indeterminate

(b15) b7 × × × × × × (b8) b0 | b7 b0

	Function: When BITS bit in ADCON1 register is set to “1” (10-bit mode)	Function: When BITS bit in ADCON1 register is set to “0” (8-bit mode)	RW
(b7-b0)	8 low-order bits of A/D conversion result	A/D conversion result	RO
(b9-b8)	2 high-order bits of A/D conversion result	When read, its content is indeterminate.	RO
(b15-b10)	Nothing is assigned. When write, set to “0”. When read, its content is “0”.		—

Figure 14.3 ADCON2 Register and AD Register

14.1 One-shot Mode

In one-shot mode, the input voltage on one selected pin is A/D converted once. Table 14.2 lists the specifications of one-shot mode. Figure 14.4 shows the ADCON0 and ADCON1 registers in one-shot mode.

Table 14.2 One-shot Mode Specifications

Item	Specification
Function	Input voltage on one pin selected by CH2 to CH0 bits is A/D converted once.
Start condition	Set ADST bit to “1”
Stop condition	• Completion of A/D conversion (ADST bit is set to “0”) • Set ADST bit to “0”
Interrupt request generation timing	End of A/D conversion
Input pin	One of AN_0 to AN_7, as selected
Reading of result of A/D converter	Read AD register

AD control register 0(1)

b7 b6 b5 b4 b3 b2 b1 b0: _ _ 0 0 0 _ _ _

Symbol: ADCON0 Address: $00D6_{16}$ After reset: $00000XXX_2$

Bit symbol	Bit name	Function	RW
CH0	Analog input pin select bit(2)	b2 b1 b0 0 0 0 : AN_0 is selected 0 0 1 : AN_1 is selected 0 1 0 : AN_2 is selected 0 1 1 : AN_3 is selected 1 0 0 : AN_4 is selected 1 0 1 : AN_5 is selected 1 1 0 : AN_6 is selected 1 1 1 : $AN_7$1 is selected	RW
CH1			RW
CH2			RW
MD	AD operation mode select bit(2)	0 : One-shot mode	RW
— (b4)	Reserved bit	Set to “0”	RW
— (b5)	Reserved bit	Set to “0”	RW
ADST	A/D conversion start flag	0 : A/D conversion disabled 1 : A/D conversion started	RW
CKS0	Frequency select bit 0(3)	0 : $f_{AD}/4$ is selected 1 : $f_{AD}/2$ is selected	RW

NOTES:
1. If the ADCON0 register is rewritten during A/D conversion, the conversion result is indeterminate.
2. When changing A/D operation mode, set analog input pin again.
3. This bit is valid when the CKS1 bit in the ADCON1 register is set to “0”.

AD control register 1(1)

b7 b6 b5 b4 b3 b2 b1 b0: 0 0 1 _ _ 0 0 0

Symbol: ADCON1 Address: $00D7_{16}$ After reset: 00_{16}

Bit symbol	Bit name	Function	RW
— (b2-b0)	Reserved bit	Set to “0”	RW
BITS	8/10-bit mode select bit	0 : 8-bit mode 1 : 10-bit mode	RW
CKS1	Frequency select bit 1(2)	0 : CKS0 bit in ADCON0 register is valid 1 : f_{AD} is selected	RW
VCUT	Vref connect bit(3)	1 : Vref connected	RW
— (b6-b7)	Reserved bit	Set to “0”	RW

NOTES:
1. If the ADCON1 register is rewritten during A/D conversion, the conversion result is indeterminate.
2. The ϕ_{AD} frequency must be 10 MHz or less.
3. If the VCUT bit is reset from “0” (Vref unconnected) to “1” (Vref connected), wait for 1 µs or more before starting A/D conversion.

Figure 14.4 ADCON0 Register and ADCON1 Registers in One-shot Mode

14.2 Repeat Mode

In repeat mode, the input voltage on one selected pin is A/D converted repeatedly. Table 14.3 lists the specifications of repeat mode. Figure 14.5 shows the ADCON0 and ADCON1 registers in repeat mode.

Table 14.3 Repeat Mode Specifications

Item	Specification
Function	Input voltage on one pin selected by CH2 to CH0 bits is A/sD converted repeat- edly
Start condition	Set ADST bit to “1”
Stop condition	Set ADST bit to “0”
Interrupt request generation timing	None generated
Input pin	One of AN_0 to AN_7, as selected
Reading of result of A/D converter	Read AD register

AD control register 0(1)

b7	b6	b5	b4	b3	b2	b1	b0
		0	0	1			

Symbol: ADCON0 Address: 00D6₁₆ → $00D6_{16}$ After reset: $00000XXX_2$

Bit symbol	Bit name	Function	RW
CH0	Analog input pin select bit(2)	b2 b1 b0 0 0 0 : AN_0 is selected 0 0 1 : AN_1 is selected 0 1 0 : AN_2 is selected 0 1 1 : AN_3 is selected 1 0 0 : AN_4 is selected 1 0 1 : AN_5 is selected 1 1 0 : AN_6 is selected 1 1 1 : AN_7 is selected	RW
CH1			RW
CH2			RW
MD	AD operation mode select bit(2)	1 : Repeat mode	RW
— (b4)	Reserved bit	Set to “0”	RW
— (b5)	Reserved bit	Set to “0”	RW
ADST	A/D conversion start flag	0 : A/D conversion disabled 1 : A/D conversion started	RW
CKS0	Frequency select bit 0(3)	0 : $f_{AD}/4$ is selected 1 : $f_{AD}/2$ is selected	RW

NOTES:
1. If the ADCON0 register is rewritten during A/D conversion, the conversion result is indeterminate.
2. When changing A/D operation mode, set analog input pin again.
3. This bit is valid when the CKS1 bit in the ADCON1 register is set to “0”.

AD control register 1(1)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	1		0	0	0	0

Symbol: ADCON1 Address: $00D7_{16}$ After reset: 00_{16}

Bit symbol	Bit name	Function	RW
— (b2-b0)	Reserved bit	Set to “0”	RW
BITS	8/10-bit mode select bit(2)	0 : 8-bit mode	RW
CKS1	Frequency select bit 1(3)	0 : CKS0 bit in ADCON0 register is valid 1 : f_{AD} is selected	RW
VCUT	Vref connect bit(4)	1 : Vref connected	RW
— (b6-b7)	Reserved bit	Set to “0”	RW

NOTES:
1. If the ADCON1 register is rewritten during A/D conversion, the conversion result is indeterminate.
2. In repeat mode, the BITS bit must be set to “0” (8-bit mode).
3. The ϕ_{AD} frequency must be 10 MHz or less.
4. If the VCUT bit is reset from “0” (Vref unconnected) to “1” (Vref connected), wait for 1 µs or more before starting A/D conversion.

Figure 14.5 ADCON0 Register and ADCON1 Register in Repeat Mode

14.3 Sample and Hold

If the SMP bit in the ADCON2 register is set to “1” (with sample-and-hold), the conversion speed per pin is increased to 28 ØAD cycles for 8-bit resolution or 33 ØAD cycles for 10-bit resolution. Sample-and-hold is effective in all operation modes. Select whether or not to use the sample-and-hold function before starting A/D conversion.

When performing the A/D conversion, charge the comparator capacitor inside the microcomputer.

Figure 14.6 shows the A/D conversion timing diagram.

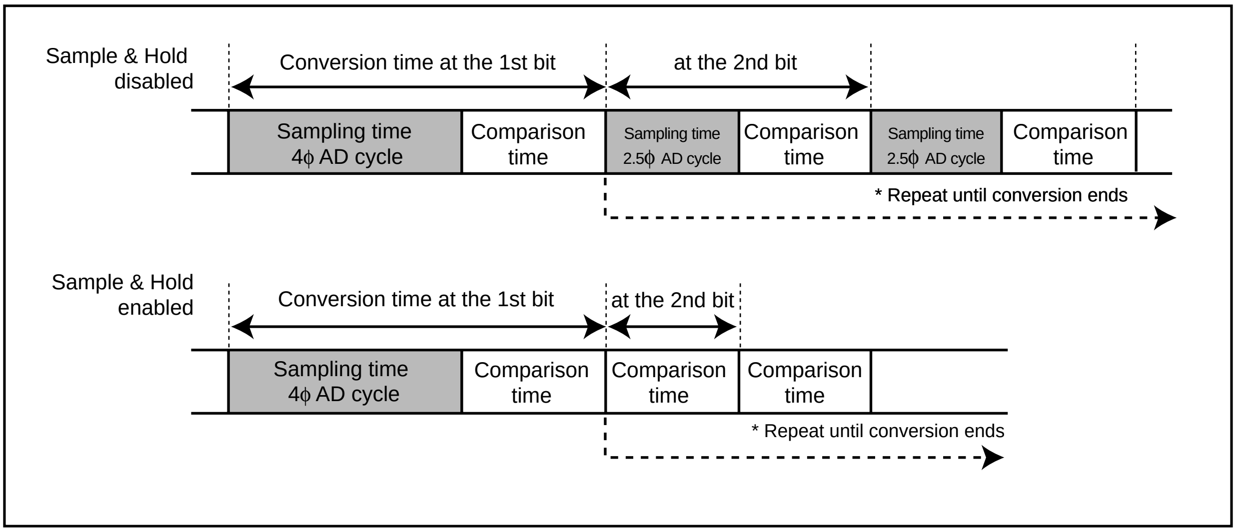


Figure 14.6 A/D Conversion Timing Diagram

14.4 A/D conversion cycles

Figure 14.7 shows the A/D conversion cycles.

Conversion time at the 1st bit | Conversion time at the 2nd bit and the follows | End process

A/D conversion mode		Conversion time	Sampling time	Comparison time	Sampling time	Comparison time	End process
Without sample & hold	8 bits	49 ϕ AD	4 ϕ AD	2.0 ϕ AD	2.5 ϕ AD	2.5 ϕ AD	8.0 ϕ AD
Without sample & hold	10 bits	59 ϕ AD	4 ϕ AD	2.0 ϕ AD	2.5 ϕ AD	2.5 ϕ AD	8.0 ϕ AD
With sample & hold	8 bits	28 ϕ AD	4 ϕ AD	2.5 ϕ AD	0.0 ϕ AD	2.5 ϕ AD	4.0 ϕ AD
With sample & hold	10 bits	33 ϕ AD	4 ϕ AD	2.5 ϕ AD	0.0 ϕ AD	2.5 ϕ AD	4.0 ϕ AD

Figure 14.7 A/D Conversion Cycles

14.5 Internal Equivalent Circuit of Analog Input

Figure 14.8 shows the internal equivalent circuit of analog input.

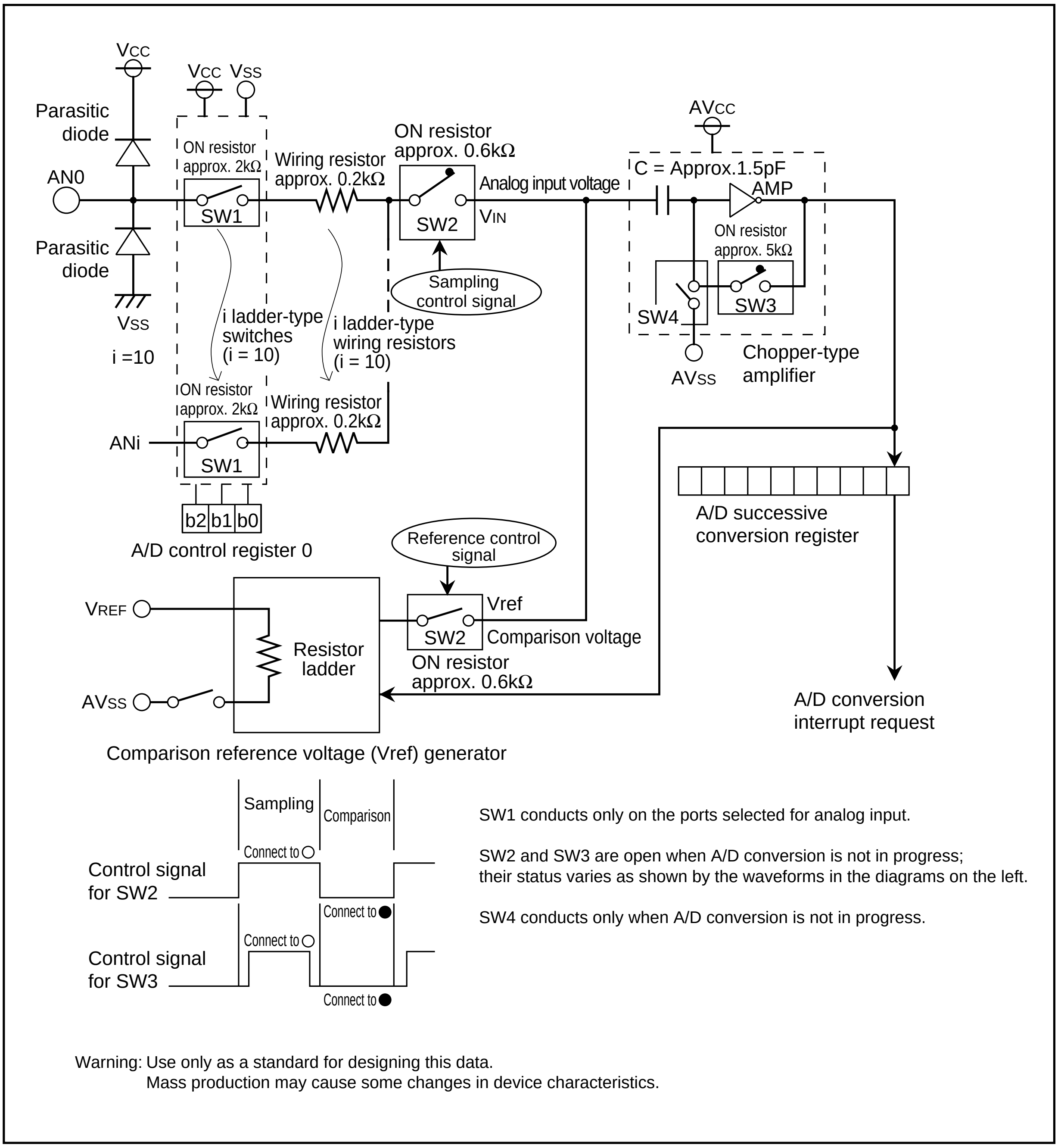


Figure 14.8 Internal Equivalent Circuit to Analog Input

14.6 Inflow Current Bypass Circuit

Figure 14.9 shows the configuration of the inflow current bypass circuit, figure 14.10 shows the example of an inflow current bypass circuit where VCC or more is applied.

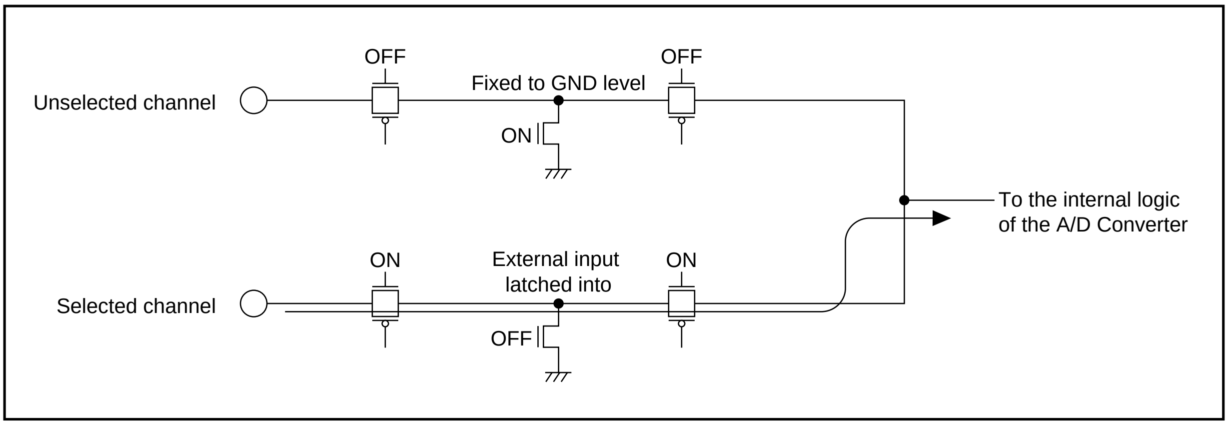


Figure 14.9 Configuration of the Inflow Current Bypass Circuit

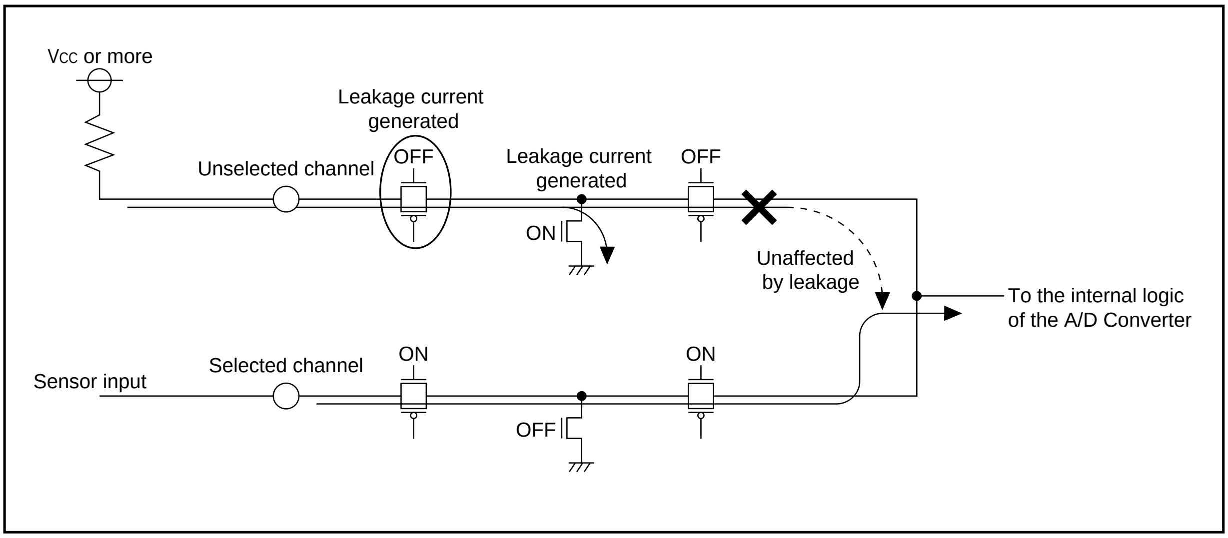


Figure 14.10 Example of an Inflow Current Bypass Circuit where VCC or More is Applied

14.7 Output Impedance of Sensor under A/D Conversion

To carry out A/D conversion properly, charging the internal capacitor C shown in Figure 14.11 has to be completed within a specified period of time. T (sampling time) as the specified time. Let output impedance of sensor equivalent circuit be R0, microcomputer's internal resistance be R, precision (error) of the A/D converter be X, and the A/D converter's resolution be Y (Y is 1024 in the 10-bit mode, and 256 in the 8-bit mode).

VC is generally $VC = VIN \{1 - e^{-\frac{1}{C(R0+R)}t}\}$

And when t = T, $VC = VIN - \frac{X}{Y} VIN = VIN(1 - \frac{X}{Y})$

$$e^{-\frac{1}{C(R0+R)}T} = \frac{X}{Y}$$

$$-\frac{1}{C(R0+R)} T = \ln\frac{X}{Y}$$

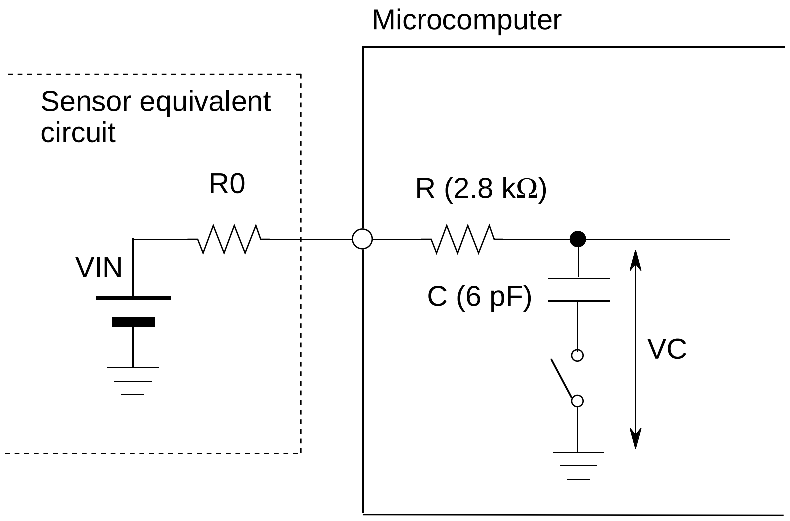
Hence, $R0 = -\dfrac{T}{C \bullet \ln\frac{X}{Y}} - R$

Figure 14.11 shows analog input pin and external sensor equivalent circuit. When the difference between VIN and VC becomes 0.1 LSB, we find impedance R0 when voltage between pins VC changes from 0 to VIN – (0.1/1024) VIN in time T. (0.1/1024) means that A/D precision drop due to insufficient capacitor charge is held to 0.1 LSB at time of A/D conversion in the 10-bit mode. Actual error however is the value of absolute precision added to 0.1 LSB. When $f(X_{IN})$ = 10 MHz, T = 0.25 µs in the A/D conversion mode with sample & hold. Output impedance R0 for sufficiently charging capacitor C within time T is determined as follows.

T = 0.25 µs, R = 2.8 kΩ, C = 1.5 pF, X = 0.1, and Y = 1024 . Hence,

$$R0 = -\frac{0.25 \times 10^{-6}}{6.0 \times 10^{-12} \bullet \ln\frac{0.1}{1024}} - 2.8 \times 10^{3} \fallingdotseq 7.3 \times 10^{3}$$

Thus, the allowable output impedance of the sensor circuit capable of thoroughly driving the A/D converter turns out to be approximately 7.3 kΩ.



NOTE:
1. The capacity of the terminal is assumed to be 4.5 pF.

Figure 14.11 Analog Input Pin and External Sensor Equivalent Circuit

15. Programmable I/O Ports

15. 1 Description

The programmable input/output ports (hereafter referred to as “I/O ports”) consist of 22 lines P0, P1, $P3_0$ to $P3_3$, $P3_7$, and $P4_5$. Each port can be set for input or output every line by using a direction register, and can also be chosen to be or not be pulled high every 4 lines. The port P1 allows the drive capacity of its N-channel output transistor to be set as necessary. The port P1 can be used as LED drive port if the drive capacity is set to “HIGH”.

$P4_6$ and $P4_7$ can be used as an input only port if the main clock oscillation circuit is not used.

Figures 15.1 to 15.4 show the I/O ports. Figure 15.5 shows the I/O pins.

Each pin functions as an I/O port or a peripheral function input/output.

For details on how to set peripheral functions, refer to each functional description in this manual. If any pin is used as a peripheral function input, set the direction bit for that pin to “0” (input mode). Any pin used as an output pin for peripheral functions is directed for output no matter how the corresponding direction bit is set.

15.1.1 Port Pi Direction Register (PDi Register, i = 0, 1, 3, 4)

Figure 15.7 shows the PDi register.

This register selects whether the I/O port is to be used for input or output. The bits in this register correspond one for one to each port.

15.1.2 Port Pi Register (Pi Register, i = 0 to 4)

Figure 15.8 shows the Pi register.

Data I/O to and from external devices are accomplished by reading and writing to the Pi register. The Pi register consists of a port latch to hold the output data and a circuit to read the pin status. For ports set for input mode, the input level of the pin can be read by reading the corresponding Pi register, and data can be written to the port latch by writing to the Pi register.

For ports set for output mode, the port latch can be read by reading the corresponding Pi register, and data can be written to the port latch by writing to the Pi register. The data written to the port latch is output from the pin. The bits in the Pi register correspond one for one to each port.

15.1.3 Pull-up Control Register 0, Pull-up Control Register 1 (PUR0 and PUR1 Registers)

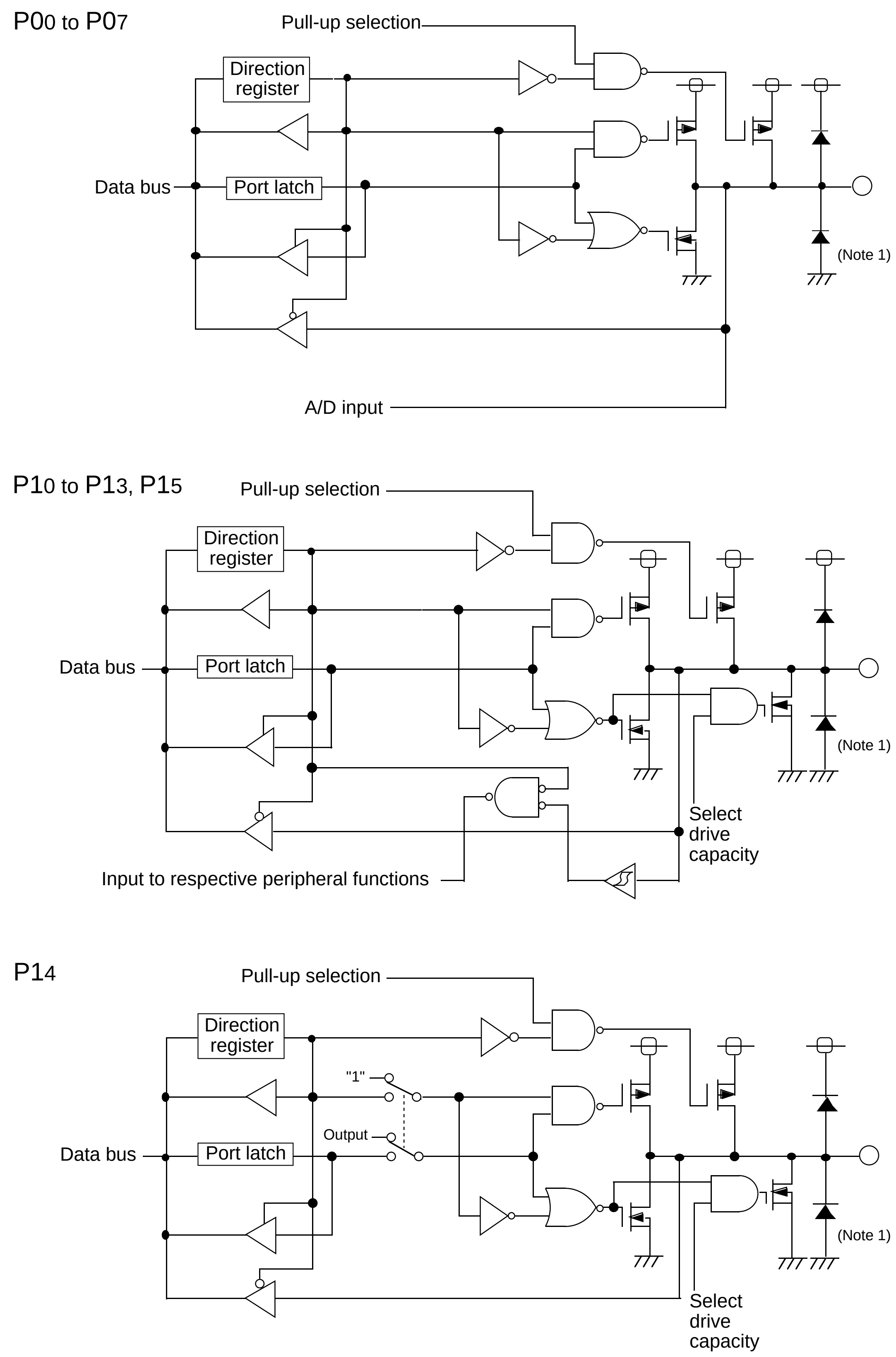
Figure 15.9 shows the PUR0 and PUR1 registers.

The PUR0 and PUR1 register bits can be used to select whether or not to pull the corresponding port high in 4 bit units. The port chosen to be pulled high has a pull-up resistor connected to it when the direction bit is set for input mode.

15.1.4 Port P1 Drive Capacity Control Register (DRR Register)

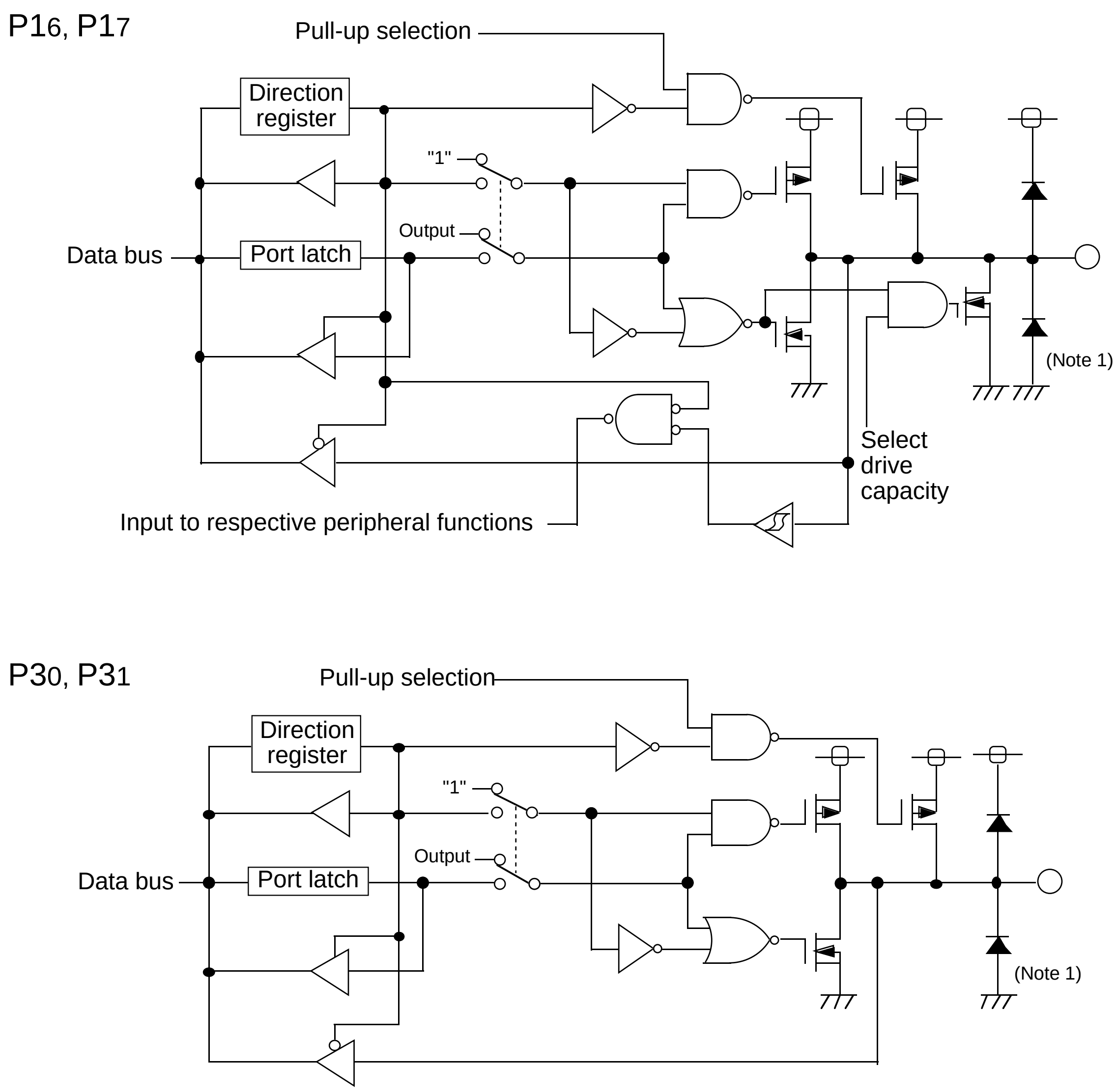
Figure 15.9 shows the DRR register.

The DRR register is used to control the drive capacity of the port P1 N-channel output transistor. The bits in this register correspond one for one to each port.



NOTES:
1. —|◄— symbolizes a parasitic diode.
Make sure the input voltage on each pin will not exceed Vcc.

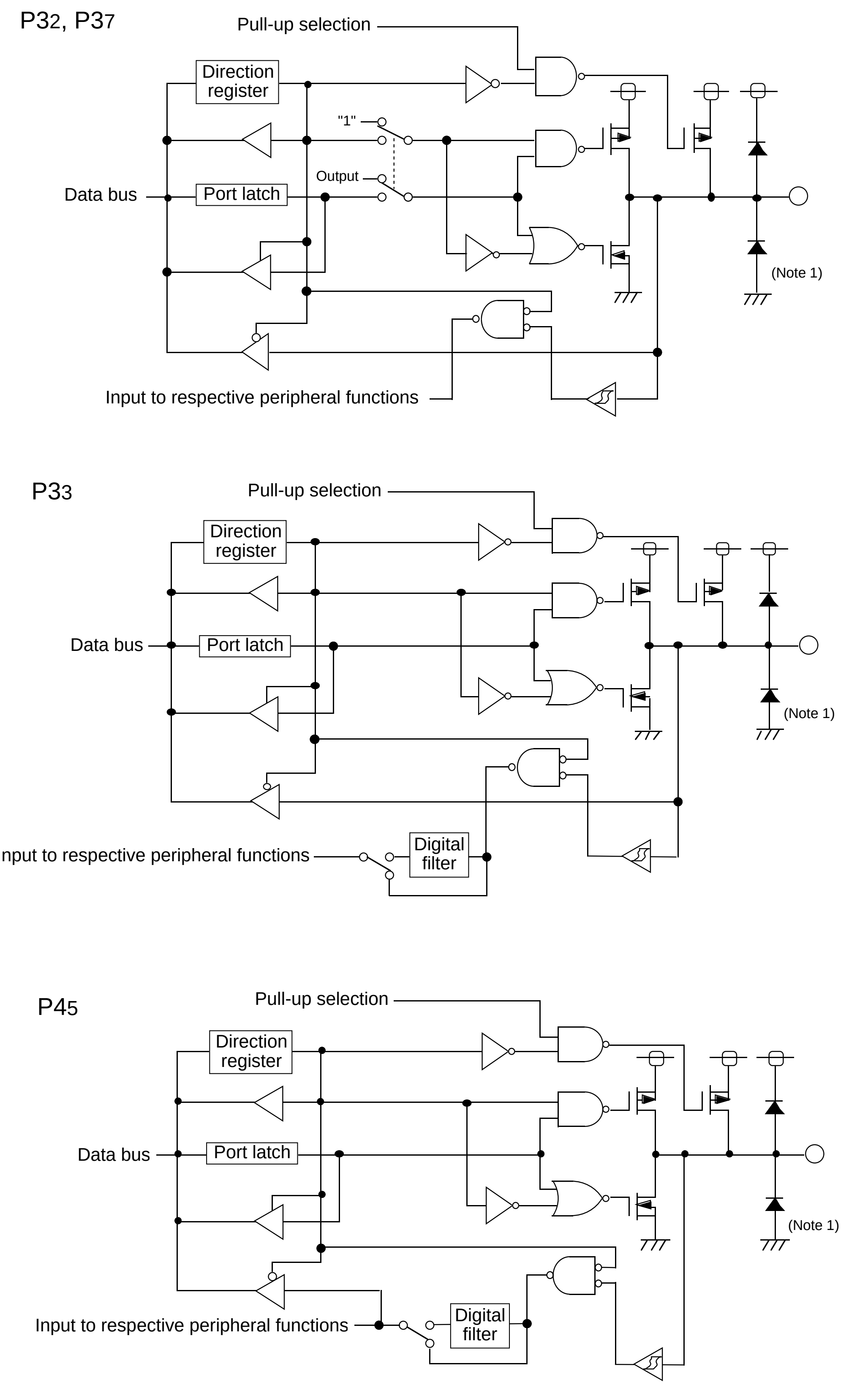
Figure 15.1 Programmable I/O Ports (1)



NOTES:

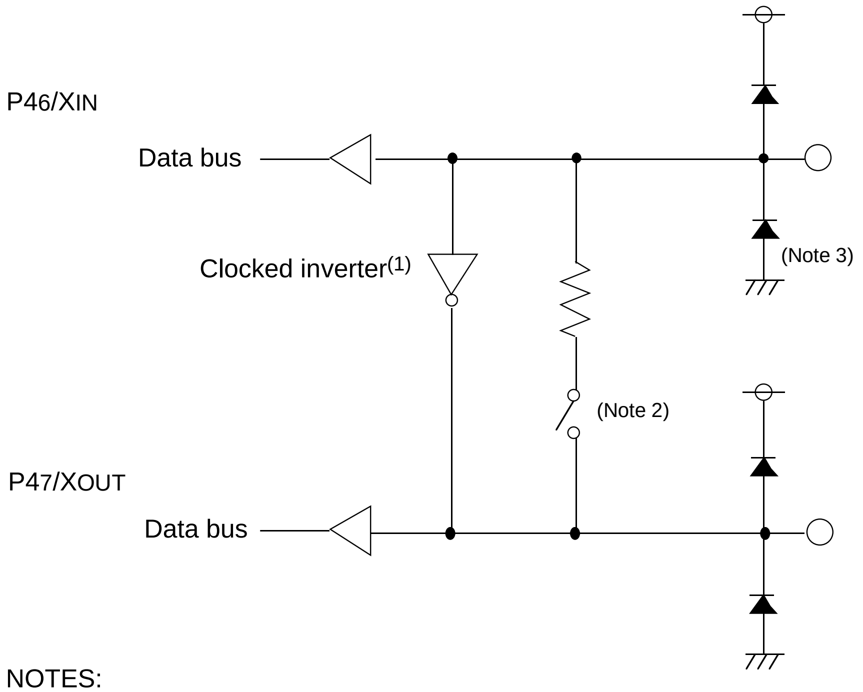
1. —▶|— symbolizes a parasitic diode.
   Make sure the input voltage on each pin will not exceed Vcc.

Figure 15.2 Programmable I/O Ports (2)



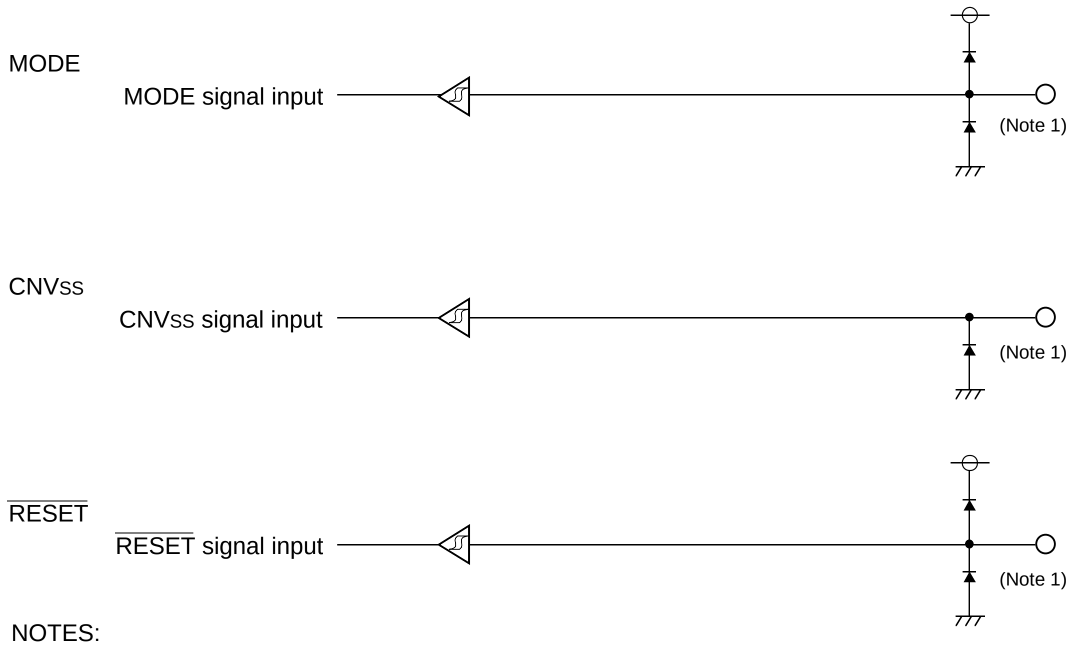
NOTES:
1. —|◄— symbolizes a parasitic diode.
Make sure the input voltage on each pin will not exceed Vcc.

Figure 15.3 Programmable I/O Ports (3)



NOTES:
1. When CM05=1, CM10=1, or CM13=0, the clocked inverter is cutoff.
2. When CM10=1 or CM13=0, the feedback resistor is unconnected.
3. —▶|— symbolizes a parasitic diode.
Make sure the input voltage on each pin will not exceed Vcc.

Figure 15.4 Programmable I/O Port (4)



NOTES:
1. ····▶|····· symbolizes a parasitic diode.
Make sure the input voltage on each pin will not exceed Vcc.

Figure 15.5 I/O Pins

Port Pi direction register (i=0, 1, 3, 4)(1, 2, 3)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After reset
PD0	$00E2_{16}$	00_{16}
PD1	$00E3_{16}$	00_{16}
PD3	$00E7_{16}$	00_{16}
PD4	$00EA_{16}$	00_{16}

Bit symbol	Bit name	Function	RW
PDi_0	Port Pi$_0$ direction bit	0 : Input mode (Functions as an input port) 1 : Output mode (Functions as an output port)	RW
PDi_1	Port Pi$_1$ direction bit		RW
PDi_2	Port Pi$_2$ direction bit		RW
PDi_3	Port Pi$_3$ direction bit		RW
PDi_4	Port Pi$_4$ direction bit		RW
PDi_5	Port Pi$_5$ direction bit		RW
PDi_6	Port Pi$_6$ direction bit		RW
PDi_7	Port Pi$_7$ direction bit		RW

NOTES:
1. The PD0 register must be written to by the next instruction after setting the PRC2 bit in the PRCR register to “1” (write enabled).
2. Bits PD3_4 to PD3_6 in the PD3 register are unavailable on this MCU. If it is necessary to set bits PD3_4 to PD3_6, set to “0” (input mode). When read, the content is indeterminate.
3. Bits PD4_0 to PD4_4, PD4_6 and PD4_7 in the PD4 register are unavailable on this MCU. If it is necessary to set bits PD4_0 to PD4_4, PD4_6 and PD4_7, set to “0” (input mode). When read, the content is indeterminate.

Figure 15.6 PD0 Register, PD1 Register, PD3 Register, and PD4 Register

Port Pi register (i=0, 1, 3, 4)(1, 2)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After reset
P0	$00E0_{16}$	Indeterminate
P1	$00E1_{16}$	Indeterminate
P3	$00E5_{16}$	Indeterminate
P4	$00E8_{16}$	Indeterminate

Bit symbol	Bit name	Function	RW
Pi_0	Port Pi$_0$ bit	The pin level on any I/O port which is set for input mode can be read by reading the corresponding bit in this register. The pin level on any I/O port which is set for output mode can be controlled by writing to the corresponding bit in this register 0 : “L” level 1 : “H” level (i = 0, 1, 3, 4)	RW
Pi_1	Port Pi$_1$ bit		RW
Pi_2	Port Pi$_2$ bit		RW
Pi_3	Port Pi$_3$ bit		RW
Pi_4	Port Pi$_4$ bit		RW
Pi_5	Port Pi$_5$ bit		RW
Pi_6	Port Pi$_6$ bit		RW
Pi_7	Port Pi$_7$ bit		RW

NOTES:
1. Bits P3_4 to P3_6 in the P3 register are unavailable on this MCU. If it is necessary to set bits P3_4 to P3_6, set to “0” (“L” level). When read, the content is indeterminate.
2. Bits P4_0 to P4_4 in the P4 register are unavailable on this MCU. If it is necessary to set bits P4_0 to P4_4, set to “0” (“L” level). When read, the content is indeterminate.

Figure 15.7 P0 Register, P1 Register, P3 Register, and P4 Register

Pull-up control register 0

Symbol	Address	After reset
PUR0	$00FC_{16}$	$00XX0000_2$

Bit symbol	Bit name	Function	RW
PU00	$P0_0$ to $P0_3$ pull-up[1]	0 : Not pulled high 1 : Pulled high[1]	RW
PU01	$P0_4$ to $P0_7$ pull-up[1]		RW
PU02	$P1_0$ to $P1_3$ pull-up[1]		RW
PU03	$P1_4$ to $P1_7$ pull-up[1]		RW
— (b5-b4)	Nothing is assigned. When write, set to “0”. When read, its content is indeterminate.		—
PU06	$P3_0$ to $P3_3$ pull-up[1]	0 : Not pulled high 1 : Pulled high[1]	RW
PU07	$P3_7$ pull-up[1]		RW

NOTES:
1. The pin for which this bit is “1” (pulled high) and the direction bit is “0” (input mode) is pulled high.

Pull-up control register 1

Symbol	Address	After reset
PUR1	$00FD_{16}$	$XXXXXX0X_2$

Bit symbol	Bit name	Function	RW
— (b0)	Nothing is assigned. When write, set to “0”. When read, its content is indeterminate.		—
PU11	$P4_5$ pull-up[1]	0 : Not pulled up 1 : Pulled up[1]	RW
— (b7-b2)	Nothing is assigned. When write, set to “0”. When read, its content is indeterminate.		—

NOTES:
1. The $P4_5$ pin for which the PU11 bit is “1” (pulled high) and the PD4_5 bit is “0” (input mode) is pulled high.

Port P1 drive capacity control register

Symbol	Address	After reset
DRR	$00FE_{16}$	00_{16}

Bit symbol	Bit name	Function	RW
DRR0	$P1_0$ drive capacity	Set P1 N-channel output transistor drive capacity 0 : LOW 1 : HIGH	RW
DRR1	$P1_1$ drive capacity		RW
DRR2	$P1_2$ drive capacity		RW
DRR3	$P1_3$ drive capacity		RW
DRR4	$P1_4$ drive capacity		RW
DRR5	$P1_5$ drive capacity		RW
DRR6	$P1_6$ drive capacity		RW
DRR7	$P1_7$ drive capacity		RW

Figure 15.8 PUR0 Register, PUR1 Register, and DRR Register

15.2 Port setting

Table 15.1 to Table 15.23 list the port setting.

Table 15.1 Port $P0_0/AN_7/TxD_{11}$ Setting

Register	PD0	PUR0	ADCON0	UCON	U1MR	U1C0	Function
Bit	PD0_0	PU00	CH2, CH1, CH0	TXD1SEL	SMD2, SMD0	NCH	
Setting value	0	0	XXX	X	00_2	X	Input port (not pulled up)
	0	0	XXX	0	XX	X	Input port (not pulled up)
	0	1	XXX	X	00_2	X	Input port (pulled up)
	0	1	XXX	0	XX	X	Input port (pulled up)
	0	0	111_2	X	00_2	X	A/D input (AN_7)
	0	0	111_2	0	XX	X	A/D input (AN_7)
	1	X	XXX	X	00_2	X	Output port
	1	X	XXX	0	XX	X	Output port
	X	X	XXX	1	1X	0	TxD_{11}
	X	X	XXX	1	X1	0	TxD_{11}
	X	0	XXX	1	1X	1	TxD_{11}, N-channel open output
	X	0	XXX	1	X1	1	TxD_{11}, N-channel open output

X: "0" or "1"

Table 15.2 Port $P0_1/AN_6$ Setting

Register	PD0	PUR0	ADCON0	Function
Bit	PD0_1	PU00	CH2, CH1, CH0	
Setting value	0	0	XXX	Input port (not pulled up)
	0	1	XXX	Input port (pulled up)
	0	0	110_2	A/D input (AN_6)
	1	X	XXX	Output port

X: "0" or "1"

Table 15.3 Port $P0_2/AN_5$ Setting

Register	PD0	PUR0	ADCON0	Function
Bit	PD0_2	PU00	CH2, CH1, CH0	
Setting value	0	0	XXX	Input port (not pulled up)
	0	1	XXX	Input port (pulled up)
	0	0	101_2	A/D input (AN_5)
	1	X	XXX	Output port

X: "0" or "1"

Table 15.4 Port $P0_3/AN_4$ Setting

Register	PD0	PUR0	ADCON0	Function
Bit	PD0_3	PU00	CH2, CH1, CH0	
Setting value	0	0	XXX	Input port (not pulled up)
	0	1	XXX	Input port (pulled up)
	0	0	100_2	A/D input (AN_4)
	1	X	XXX	Output port

X: "0" or "1"

Table 15.5 Port P04/AN3 Setting

Register	PD0	PUR0	ADCON0	Function
Bit	PD0_4	PU01	CH2, CH1, CH0	
Setting value	0	0	XXX	Input port (not pulled up)
	0	1	XXX	Input port (pulled up)
	0	0	011_2	A/D input (AN3)
	1	X	XXX	Output port

X: “0” or “1”

Table 15.6 Port P05/AN2 setting

Register	PD0	PUR0	ADCON0	Function
Bit	PD0_5	PU01	CH2, CH1, CH0	
Setting value	0	0	XXX	Input port (not pulled up)
	0	1	XXX	Input port (pulled up)
	0	0	010_2	A/D input (AN2)
	1	X	XXX	Output port

X: “0” or “1”

Table 15.7 Port P06/AN1 Setting

Register	PD0	PUR0	ADCON0	Function
Bit	PD0_6	PU01	CH2, CH1, CH0	
Setting value	0	0	XXX	Input port (not pulled up)
	0	1	XXX	Input port (pulled up)
	0	0	001_2	A/D input (AN1)
	1	X	XXX	Output port

X: “0” or “1”

Table 15.8 Port P07/AN0 Setting

Register	PD0	PUR0	ADCON0	Function
Bit	PD0_7	PU01	CH2, CH1, CH0	
Setting value	0	0	XXX	Input port (not pulled up)
	0	1	XXX	Input port (pulled up)
	0	0	000_2	A/D input (AN0)
	1	X	XXX	Output port

X: “0” or “1”

Table 15.9 Port P10/$\overline{KI0}$ Setting

Register	PD1	PUR0	DRR	KIEN	P1	Function
Bit	PD1_0	PU02	DRR0	KI0EN	P1_0	
Setting value	0	0	X	X	X	Input port (not pulled up)
	0	1	X	X	X	Input port (pulled up)
	0	0	X	1	X	$\overline{KI0}$ input
	1	X	0	X	X	Output port
	1	X	1	X	X	Output port (High drive)

X: “0” or “1”

Table 15.10 Port P11/$\overline{KI1}$ Setting

Register	PD1	PUR0	DRR	KIEN	P1	Function
Bit	PD1_1	PU02	DRR1	KI1EN	P1_1	
Setting value	0	0	X	X	X	Input port (not pulled up)
	0	1	X	X	X	Input port (pulled up)
	0	0	X	1	X	$\overline{KI1}$ input
	1	X	0	X	X	Output port
	1	X	1	X	X	Output port (High drive)

X: “0” or “1”

Table 15.11 Port P12/$\overline{KI2}$ Setting

Register	PD1	PUR0	DRR	KIEN	P1	Function
Bit	PD1_2	PU02	DRR2	KI2EN	P1_2	
Setting value	0	0	X	X	X	Input port (not pulled up)
	0	1	X	X	X	Input port (pulled up)
	0	0	X	1	X	$\overline{KI2}$ input
	1	X	0	X	X	Output port
	1	X	1	X	X	Output port (High drive)

X: “0” or “1”

Table 15.12 Port P13/$\overline{KI3}$ Setting

Register	PD1	PUR0	DRR	KIEN	Function
Bit	PD1_3	PU02	DRR3	KI3EN	
Setting value	0	0	X	X	Input port (not pulled up)
	0	1	X	X	Input port (pulled up)
	0	0	X	1	$\overline{KI3}$ input
	1	X	0	X	Output port
	1	X	1	X	Output port (High drive)

X: “0” or “1”

Table 15.13 Port P14/TxD0 Setting

Register	PD1	PUR0	DRR	U0MR	U0C0	Function
Bit	PD1_4	PU03	DRR4	SMD2, SMD0	NCH	
Setting value	0	0	X	00₂	X	Input port (not pulled up)
	0	1	X	00₂	X	Input port (pulled up)
	1	X	0	00₂	X	Output port
	1	X	1	00₂	X	Output port (High drive)
	X	X	0	X1 1X	0	TxD0 output, CMOS output
	X	X	1	X1 1X	0	TxD0 output, CMOS output (High drive)
	X	X	0	X1 1X	1	TxD0 output, N-channel open output
	X	X	1	X1 1X	1	TxD0 output, N-channel open output (High drive)

X: “0” or “1”

Table 15.14 Port P15/RxD0 Setting

Register	PD1	PUR0	DRR	Function
Bit	PD1_5	PU03	DRR5	
Setting value	0	0	X	Input port (not pulled up)
	0	1	X	Input port (pulled up)
	0	0	X	RxD0 input
	1	X	0	Output port
	1	X	1	Output port (High drive)

X: “0” or “1”

Table 15.15 Port P16/CLK0 Setting

Register	PD1	PUR0	DRR	U0MR	Function
Bit	PD1_6	PU03	DRR6	SMD2, SMD0, CKDIR	
Setting value	0	0	X	Other than 010₂	Input port (not pulled up)
	0	1	X	Other than 010₂	Input port (pulled up)
	0	0	X	XX1	CLK0 (external clock) input
	1	X	0	Other than 010₂	Output port
	1	X	1	Other than 010₂	Output port (High drive)
	X	X	0	010₂	CLK0 (internal clock) output
	X	X	1	010₂	CLK0 (internal clock) output (High drive)

X: “0” or “1”

Table 15.16 Port P17/$\overline{\text{INT1}}$/CNTR0 Setting

Register	PD1	PUR0	DRR	TXMR	Function
Bit	PD1_7	PU03	DRR5	TXMOD1, TXMOD0	
Setting value	0	0	X	Other than 01_2	Input port (not pulled up)
	0	1	X	Other than 01_2	Input port (pulled up)
	0	0	X	Other than 01_2	CNTR0/$\overline{\text{INT1}}$ input
	1	X	0	Other than 01_2	Output port
	1	X	1	Other than 01_2	Output port (High drive)
	X	X	0	01_2	CNTR0 output
	X	X	1	01_2	CNTR0 (High drive)

X: “0” or “1”

Table 15.17 Port P30/$\overline{\text{CNTR0}}$ Setting

Register	PD3	PUR0	TXMR	P3	Function
Bit	PD3_0	PU06	TXOCNT	P3_0	
Setting value	0	0	0	X	Input port (not pulled up)
	0	1	0	X	Input port (pulled up)
	1	X	0	X	Output port
	X	X	1	X	$\overline{\text{CNTR0}}$ output

X: “0” or “1”

Table 15.18 Port P31/TZOUT Setting

Register	PD3	PUR0	TYZMR	TYZOC	P3	Function
Bit	PD3_1	PU06	TZMOD1, TZMOD0	TZOCNT	P3_1	
Setting value	0	0	00_2	X	X	Input port (not pulled up)
			01_2	1		
	0	1	00_2	X	X	Input port (pulled up)
			01_2	1		
	1	X	00_2	X	X	Output port
			01_2	1		
	X	X	1X	X	X	TZOUT output
			01_2	0		

X: “0” or “1”

Table 15.19 Port P32/$\overline{\text{INT2}}$/CNTR1 Setting

Register	PD3	PUR0	TYZMR	TYZOC	P3	Function
Bit	PD3_2	PU06	TYMOD1	TZOCNT	P3_2	
Setting value	0	0	0	1	X	Input port (not pulled up)
	0	1	0	1	X	Input port (pulled up)
	0	0	0	1	X	CNTR1/$\overline{\text{INT2}}$ input
	1	X	0	1	X	Output port
	X	X	1	0	X	CNTR1 output

X: “0” or “1”

Table 15.20 Port P3$_3$/$\overline{\text{INT3}}$/TC$_{\text{IN}}$ Setting

Register	PD3	PUR0	Function
Bit	PD3_3	PU06	
Setting value	0	0	Input port (not pulled up)
	0	1	Input port (pulled up)
	0	0	TC$_{\text{IN}}$/INT$_3$ input
	1	X	Output port

X: “0” or “1”

Table 15.21 Port P3$_7$/TxD$_{10}$/RxD$_1$ Setting

Register	PD3	PUR0	UCON	U1MR	U1C0	Function
Bit	PD3_7	PU07	TXD1EN	SMD2, SMD0	NCH	
Setting value	0	0	X	00$_2$	X	Input port (not pulled up)
	0	1	X	00$_2$	X	Input port (pulled up)
	0	0	0	1X	X	RxD$_1$
				X1		
	1	X	X	00$_2$	X	Output port
	X	X	1	1X	0	TxD$_0$ output, CMOS output
				X1		
	X	X	1	1X	1	TxD$_{10}$ output, N-channel open output
				X1		

X: “0” or “1”

Table 15.22 Port P4$_5$/$\overline{\text{INT0}}$ Setting

Register	PD4	PUR1	INTEN	Function
Bit	PD4_5	PU11	INT0EN	
Setting value	0	0	0	Input port (not pulled up)
	0	1	0	Input port (pulled up)
	0	0	1	$\overline{\text{INT0}}$ input
	1	X	X	Output port

X: “0” or “1”

Table 15.23 Port X$_{\text{IN}}$/P4$_6$, X$_{\text{OUT}}$/P4$_7$ Setting

Register	CM1	CM1	CM0	Circuit specification		Function
Bit	CM13	CM10	CM05	Oscillation buffer	Feedback resistance	
Setting value	1	1	1	OFF	OFF	X$_{\text{IN}}$-X$_{\text{OUT}}$ oscillatoin stop
	1	0	1	OFF	ON	External input to X$_{\text{IN}}$ pin, “H” output from X$_{\text{OUT}}$ pin
	1	0	1	OFF	ON	X$_{\text{IN}}$-X$_{\text{OUT}}$ oscillatoin stop
	1	0	0	ON	ON	X$_{\text{IN}}$-X$_{\text{OUT}}$ oscillatoin
	0	X	X	OFF	OFF	Input port

X: “0” or “1”

15.3 Unassigned Pin Handling

Table 15.24 lists the handling of unassigned pins.

Table 15.24 Unassigned Pin Handling

Pin name	Connection
Ports P0, P1, P30 to P33, P37, P45	•After setting for input mode, connect every pin to VSS via a resistor(pull-down) or connect every pin to VCC via a resistor(pull-up) •Set to output mode and leave these pins open(1, 2)
Ports P46, P47	Connect to VCC via resistor (pull-up)(2)
AVCC, VREF	Connect to VCC
AVSS	Connect to VSS

NOTES:
1. When these ports are set for output mode and left open, they remain input mode until they are set for output mode by a program. The voltage level of these pins may be unstable and the power supply current may increase for the time the ports remain input mode.
   The content of the direction registers may change due to noise or runaway caused by noise. In order to enhance program reliability, set the direction registers periodically by a program.
2. Connect these unassigned pins to the microcomputer using the shortest wire length (within 2 cm) possible.

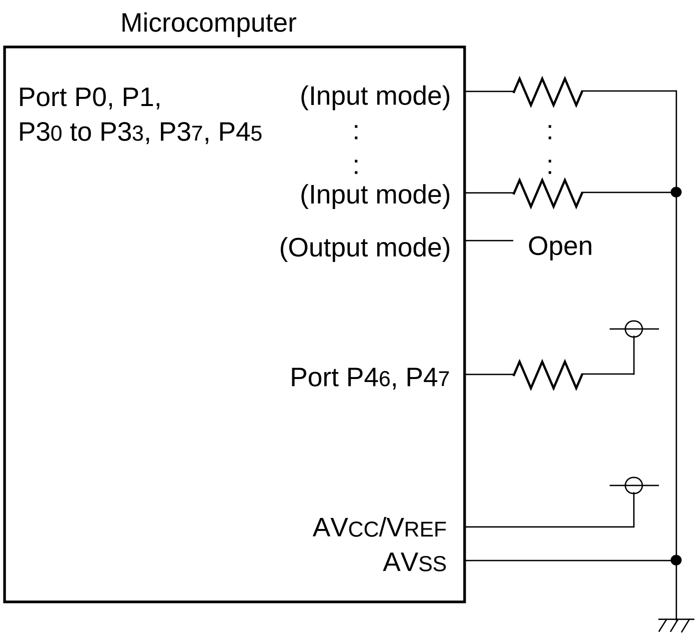


Figure 15.9 Unassigned Pin Handling

16. Electrical Characteristics

Table 16.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
V_{CC}	Supply voltage	$V_{CC}=AV_{CC}$	-0.3 to 6.5	V
AV_{CC}	Analog supply voltage	$V_{CC}=AV_{CC}$	-0.3 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC}+0.3	V
V_O	Output voltage		-0.3 to V_{CC}+0.3	V
P_d	Power dissipation	Topr=25 °C	300	mW
T_{opr}	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	°C
T_{stg}	Storage temperature		-65 to 150	°C

Table 16.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard Min.	Standard Typ.	Standard Max.	Unit
V_{CC}	Supply voltage			2.7	—	5.5	V
AV_{CC}	Analog supply voltage			—	V_{CC}(3)	—	V
V_{SS}	Supply voltage			—	0	—	V
AV_{SS}	Analog supply voltage			—	0	—	V
V_{IH}	"H" input voltage			0.8V_{CC}	—	V_{CC}	V
V_{IL}	"L" input voltage			0	—	0.2V_{CC}	V
$I_{OH (sum)}$	"H" peak all output currents	Sum of all pins' IOH (peak)		—	—	-60.0	mA
$I_{OH (peak)}$	"H" peak output current			—	—	-10.0	mA
$I_{OH (avg)}$	"H" average output current			—	—	-5.0	mA
$I_{OL (sum)}$	"L" peak all output currents	Sum of all pins' IOL (peak)		—	—	60	mA
$I_{OL (peak)}$	"L" peak output current	Except $P1_0$ to $P1_7$		—	—	10	mA
		$P1_0$ to $P1_7$	Drive ability HIGH	—	—	30	mA
			Drive ability LOW	—	—	10	mA
$I_{OL (avg)}$	"L" average output current	Except $P1_0$ to $P1_7$		—	—	5	mA
		$P1_0$ to $P1_7$	Drive ability HIGH	—	—	15	mA
			Drive ability LOW	—	—	5	mA
f (X_{IN})	Main clock input oscillation frequency		3.0V ≤ Vcc ≤ 5.5V	0	—	16	MHz
			2.7V ≤ Vcc < 3.0V	0	—	10	MHz

NOTES:
1. V_{CC} = AV_{CC} = 2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. The typical values when average output current is 100ms.
3. Hold Vcc=AVcc.

Table 16.3 A/D Conversion Characteristics

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		Vref =VCC	—	—	10	Bit
–	Absolute accuracy	10 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	—	—	±3	LSB
		8 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	—	—	±2	LSB
		10 bit mode	øAD=10 MHz, Vref=Vcc=3.3V(3)	—	—	±5	LSB
		8 bit mode	øAD=10 MHz, Vref=Vcc=3.3V(3)	—	—	±2	LSB
R_{LADDER}	Ladder resistance		VREF=VCC	10	—	40	kΩ
t_{CONV}	Conversion time	10 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	3.3	—	—	µs
		8 bit mode	øAD=10 MHz, Vref=Vcc=5.0V	2.8	—	—	µs
V_{REF}	Reference voltage			—	V_{CC}(4)	—	V
V_{IA}	Analog input voltage			0	—	V_{ref}	V
–	A/D operating clock frequency(2)	Without sample & hold		0.25	—	10	MHz
		With sample & hold		1.0	—	10	MHz

NOTES:
1. V_{CC}=AV_{CC}=2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. If f_{AD} exceeds 10 MHz, divide the f_{AD} and hold A/D operating clock frequency ($Ø_{AD}$) 10 MHz or below.
3. If the AVcc is less than 4.2V, divide the f_{AD} and hold A/D operating clock frequency ($Ø_{AD}$) f_{AD}/2 or below.
4. Hold Vcc=Vref.

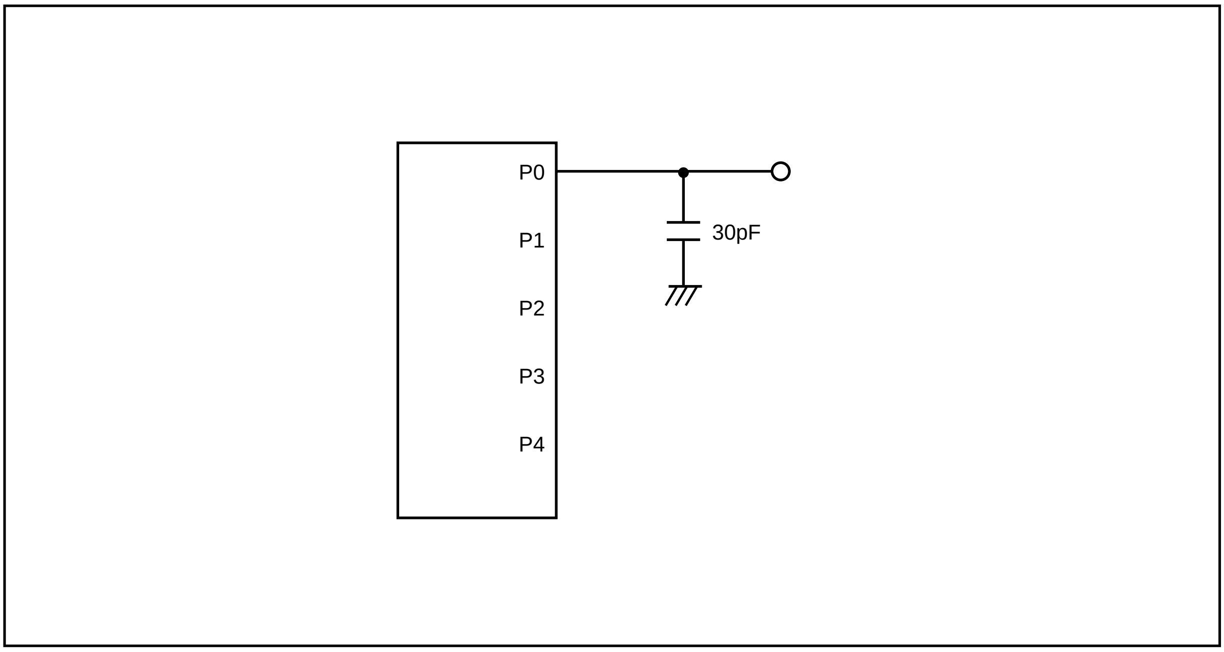


Figure 16.1 Port P0 to P4 measurement circuit

Table 16.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Program/Erase endurance(2)		1,000(3)	—	—	times
–	Byte program time		—	50	—	µs
–	Block erase time		—	0.4	—	s
$t_{d(SR-ES)}$	Time delay from Suspend Request until Erase Suspend		—	—	8	ms
–	Erase Suspend Request Interval		10	—	—	ms
–	Program, Erase Voltage		2.7	—	5.5	V
–	Read Voltage		2.7	—	5.5	V
–	Program, Erase Temperature		0	—	60	°C
–	Data hold time(7)	Ambient temperature = 55 °C	20	—	—	year

NOTES:
1. VCC=AVcc=2.7 to 5.5V at Topr = 0 to 60 °C, unless otherwise specified.
2. Definition of Program/Erase
   The endurance of Program/Erase shows a time for each block.
   If the program/erase number is “n” (n = 1,000, 10,000), “n” times erase can be performed for each block.
   For example, if performing one-byte write to the distinct addresses on Block A of 2K-byte block 2048 times and then erasing that block, the number of Program/Erase cycles is one time.
   However, performing multiple writes to the same address before an erase operation is prohibited (overwriting prohibited).
3. Numbers of Program/Erase cycles for which all electrical characteristics is guaranteed.
4. To reduce the number of Program/Erase cycles, a block erase should ideally be performed after writing in series as many distinct addresses (only one time each) as possible. If programming a set of 16 bytes, write up to 128 sets and then erase them one time. This will result in ideally reducing the number of Program/Erase cycles. Additionally, averaging the number of Program/Erase cycles for Block A and B will be more effective. It is important to track the total number of block erases and restrict the number.
5. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error disappears.
6. Customers desiring Program/Erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 16.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics(4)

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Program/Erase endurance(2)		10000(3)	—	—	times
–	Byte program time(program/erase endurance ≤1000 times)		—	50	400	µs
–	Byte program time(program/erase endurance >1000 times)		—	65	—	µs
–	Block erase time(program/erase endurance ≤1000 times)		—	0.2	9	s
–	Block erase time(program/erase endurance >1000 times)		—	0.3	—	s
$t_{d(SR-ES)}$	Time delay from Suspend Request until Erase Suspend		—	—	8	ms
–	Erase Suspend Request Interval		10	—	—	ms
–	Program, Erase Voltage		2.7	—	5.5	V
–	Read Voltage		2.7	—	5.5	V
–	Program/Erase Temperature		-20(-40)(8)	—	85	°C
–	Data hold time(9)	Ambient temperature = 55 °C	20	—	—	year

NOTES:
1. Referenced to VCC=AVcc=2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
2. Definition of Program/Erase
   The endurance of Program/Erase shows a time for each block.
   If the program/erase number is “n” (n = 1,000, 10,000), “n” times erase can be performed for each block.
   For example, if performing one-byte write to the distinct addresses on Block A of 2K-byte block 2048 times and then erasing that block, the number of Program/Erase cycles is one time.
   However, performing multiple writes to the same address before an erase operation is prohibited (overwriting prohibited).
3. Numbers of Program/Erase cycles for which all electrical characteristics is guaranteed.
4. Table 16.5 applies for Block A or B when the Program/Erase cycles are more than 1000. The byte program time up to 1000 cycles are the same as that of the program area (see Table 5.4).
5. To reduce the number of Program/Erase cycles, a block erase should ideally be performed after writing in series as many distinct addresses (only one time each) as possible. If programming a set of 16 bytes, write up to 128 sets and then erase them one time. This will result in ideally reducing the number of Program/Erase cycles. Additionally, averaging the number of Program/Erase cycles for Block A and B will be more effective. It is important to track the total number of block erases and restrict the number.
6. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error disappears.
7. Customers desiring Program/Erase failure rate information should contact their Renesas technical support representa-tive.
8. -40 °C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

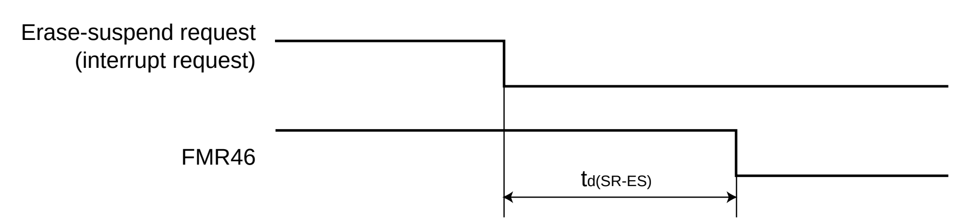


Figure 16.2 Time delay from Suspend Request until Erase Suspend

Table 16.6 Power Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during powering-on(2)		1	—	2000	µs
$t_{d(R-S)}$	STOP release time(3)		—	—	150	µs

NOTES:
1. The measuring condition is Vcc=AVcc=2.7 to 5.5 V and Topr=25 °C.
2. This shows the waiting time until the internal power supply generating circuit is stabilized during powering-on.
3. This shows the time until BCLK starts from the interrupt acknowledgement to cancel stop mode.

Table 16.7 Electrical Characteristics (1) [Vcc=5V]

Symbol	Parameter		Measuring condition		Standard Min.	Standard Typ.	Standard Max.	Unit
V_{OH}	"H" output voltage	Except X_{OUT}	I_{OH}=-5mA		V_{CC}-2.0	—	V_{CC}	V
			I_{OH}=-200μA		V_{CC}-0.3	—	V_{CC}	V
		X_{OUT}	Drive capacity HIGH	I_{OH}=-1 mA	V_{CC}-2.0	—	V_{CC}	V
			Drive capacity LOW	I_{OH}=-500μA	V_{CC}-2.0	—	V_{CC}	V
V_{OL}	"L" output voltage	Except P10 to P17, X_{OUT}	I_{OL}= 5 mA		—	—	2.0	V
			I_{OL}= 200 μA		—	—	0.45	V
		P10 to P17	Drive capacity HIGH	I_{OL}= 15 mA	—	—	2.0	V
			Drive capacity LOW	I_{OL}= 5 mA	—	—	2.0	V
			Drive capacity LOW	I_{OL}= 200 μA	—	—	0.45	V
		X_{OUT}	Drive capacity HIGH	I_{OL}= 1 mA	—	—	2.0	V
			Drive capacity LOW	I_{OL}=500 μA	—	—	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, CNTR0, CNTR1, TCIN, RxD0, RxD1, P45			0.2	—	1.0	V
		$\overline{RESET}$			0.2	—	2.2	V
I_{IH}	"H" input current		V_I=5V		—	—	5.0	μA
I_{IL}	"L" input current		V_I=0V		—	—	-5.0	μA
R_{PULLUP}	Pull-up resistance		V_I=0V		30	50	167	kΩ
R_{fXIN}	Feedback resistance	X_{IN}			—	1.0	—	MΩ
f_{RING-S}	Low-speed on-chip oscillator frequency				40	125	250	kHz
V_{RAM}	RAM retention voltage		At stop mode		2.0	—	—	V

NOTES:
1. Referenced to V_{CC} = AV_{CC} = 4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=20MHz unless otherwise specified.

Table 16.8 Electrical Characteristics (2) [Vcc=5V]

Symbol	Parameter	Measuring condition		Standard Min.	Standard Typ.	Standard Max.	Unit
I_{CC}	Power supply current (V_{CC}=3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are V_{SS}	High-speed mode	X_{IN}=16 MHz (square wave) On-chip oscillator on=125 kHz No division	—	8	14	mA
			X_{IN}=10 MHz (square wave) On-chip oscillator on=125 kHz No division	—	5	—	mA
		Medium-speed mode	X_{IN}=16 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	—	3	—	mA
			X_{IN}=10 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	—	2	—	mA
		On-chip oscillator mode	Main clock off On-chip oscillator on=125 kHz Division by 8	—	470	900	μA
		Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed(1) Peripheral clock operation	—	40	80	μA
		Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed(1) Peripheral clock off	—	38	76	μA
		Stop mode	Main clock off, Topr = 25 °C On-chip oscillator off CM10="1" Peripheral clock off	—	0.8	3.0	μA

NOTES:
1. Timer Y is operated with timer mode.
2. Referenced to V_{CC} = AV_{CC} = 4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=20MHz unless otherwise specified.

Timing requirements (Unless otherwise noted: V_{CC} = 5V, V_{SS} = 0V at Topr = 25 °C) [V_{CC}=5V]

Table 16.9 XIN input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(XIN)	XIN input cycle time	62.5	–	ns
tWH(XIN)	XIN input HIGH pulse width	30	–	ns
tWL(XIN)	XIN input LOW pulse width	30	–	ns

Table 16.10 CNTR0 input, CNTR1 input, $\overline{INT2}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CNTR0)	CNTR0 input cycle time	100	–	ns
tWH(CNTR0)	CNTR0 input HIGH pulse width	40	–	ns
tWL(CNTR0)	CNTR0 input LOW pulse width	40	–	ns

Table 16.11 TCIN input, $\overline{INT3}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(TCIN)	TCIN input cycle time	400(1)	–	ns
tWH(TCIN)	TCIN input HIGH pulse width	200(2)	–	ns
tWL(TCIN)	TCIN input LOW pulse width	200(2)	–	ns

NOTES:
1. When using the Timer C capture function, adjust the cycle time above (1/ Timer C count source frequency x 3).
2. When using the Timer C capture function, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 16.12 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tC(CK)	CLKi input cycle time	200	–	ns
tW(CKH)	CLKi input HIGH pulse width	100	–	ns
tW(CKL)	CLKi input LOW pulse width	100	–	ns
td(C-Q)	TxDi output delay time	–	80	ns
th(C-Q)	TxDi hold time	0	–	ns
tsu(D-C)	RxDi input setup time	35	–	ns
th(C-D)	RxDi input hold time	90	–	ns

Table 16.13 External interrupt $\overline{INT0}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tW(INH)	$\overline{INT0}$ input HIGH pulse width	250(1)	–	ns
tW(INL)	$\overline{INT0}$ input LOW pulse width	250(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.

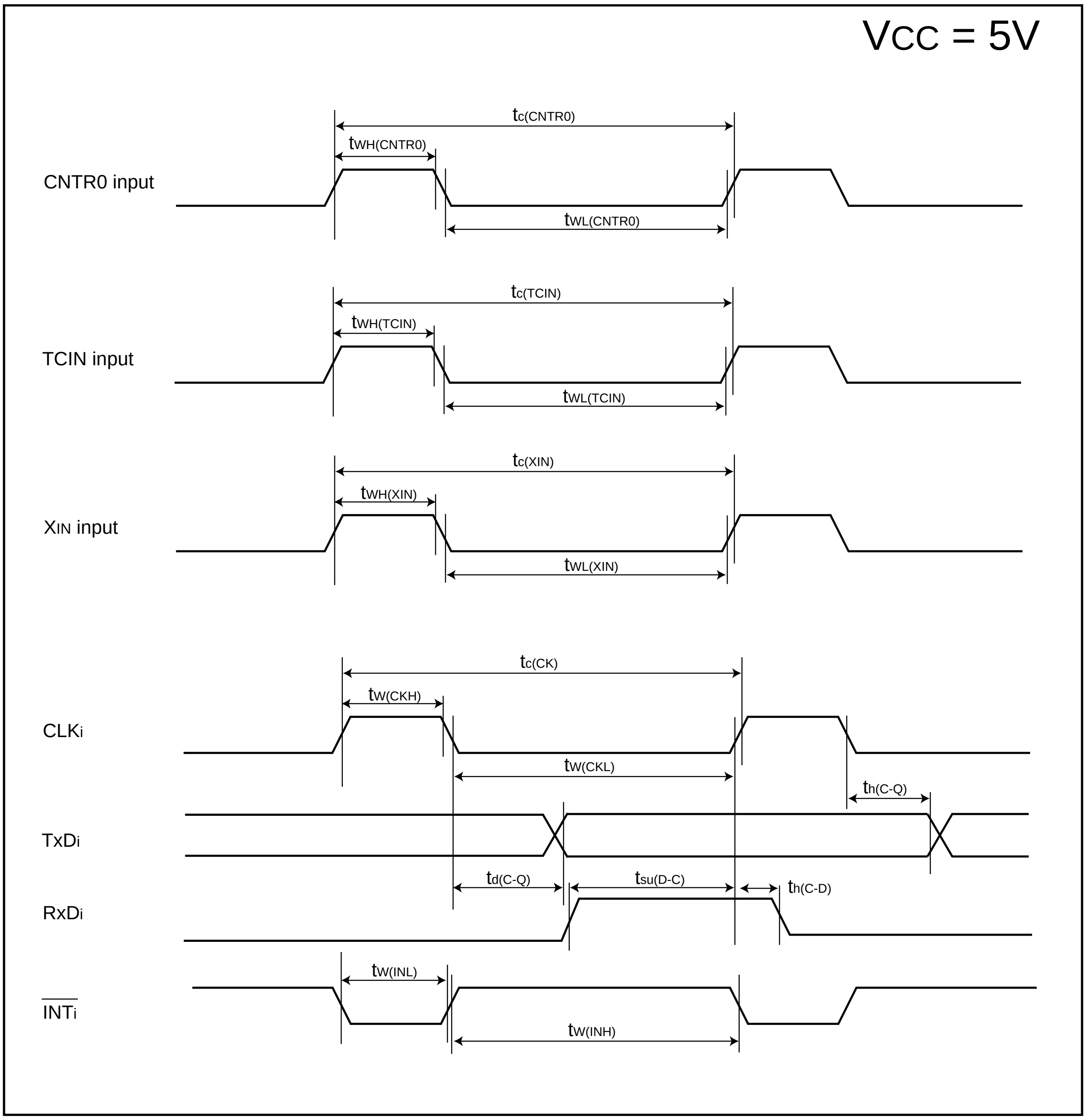


Figure 16.3 Vcc=5V timing diagram

Table 16.14 Electrical Characteristics (3) [Vcc=3V]

Symbol	Parameter		Measuring condition		Standard Min.	Standard Typ.	Standard Max.	Unit
V_{OH}	"H" output voltage	Except X_{OUT}	I_{OH}=-1mA		V_{CC}-0.5	—	V_{CC}	V
		X_{OUT}	Drive capacity HIGH	I_{OH}=-0.1 mA	V_{CC}-0.5	—	V_{CC}	V
			Drive capacity LOW	I_{OH}=-50 µA	V_{CC}-0.5	—	V_{CC}	V
V_{OL}	"L" output voltage	Except $P1_0$ to $P1_7$, X_{OUT}	I_{OL}= 1 mA		—	—	0.5	V
		$P1_0$ to $P1_7$	Drive capacity HIGH	I_{OL}= 2 mA	—	—	0.5	V
			Drive capacity LOW	I_{OL}= 1 mA	—	—	0.5	V
		X_{OUT}	Drive capacity HIGH	I_{OL}= 0.1 mA	—	—	0.5	V
			Drive capacity LOW	I_{OL}=50 µA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT_0}$, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{INT_3}$, $\overline{KI_0}$, $\overline{KI_1}$, $\overline{KI_2}$, KI_3, $CNTR_0$, $CNTR_1$, TC_{IN}, RxD_0, RxD_1, $P4_5$			0.2	—	0.8	V
		$\overline{RESET}$			0.2	—	1.8	V
I_{IH}	"H" input current		V_I=3V		—	—	4.0	µA
I_{IL}	"L" input current		V_I=0V		—	—	-4.0	µA
R_{PULLUP}	Pull-up resistance		V_I=0V		66	160	500	kΩ
R_{fXIN}	Feedback resistance	X_{IN}			—	3.0	—	MΩ
f_{RING}	On-chip oscillator frequency				40	125	250	kHz
V_{RAM}	RAM retention voltage		At stop mode		2.0	—	—	V

NOTES:
1. Referenced to V_{CC}=AV_{CC}=2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=10MHz unless otherwise specified.

RENESAS

Table 16.15 Electrical Characteristics (4) [Vcc=3V]

Symbol	Parameter	Measuring condition		Standard Min.	Standard Typ.	Standard Max.	Unit
I_{CC}	Power supply current (V_{CC1}=2.7 to 3.3V) In single-chip mode, the output pins are open and other pins are V_{SS}	High-speed mode	X_{IN}=16 MHz (square wave) On-chip oscillator on=125 kHz No division	—	7	12	mA
			X_{IN}=10 MHz (square wave) On-chip oscillator on=125 kHz No division	—	5	—	mA
		Medium-speed mode	X_{IN}=16 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	—	2.5	—	mA
			X_{IN}=10 MHz (square wave) On-chip oscillator on=125 kHz Division by 8	—	1.6	—	mA
		On-chip oscillator mode	Main clock off On-chip oscillator on=125 kHz Division by 8	—	420	800	µA
		Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed(1) Peripheral clock operation	—	37	74	µA
		Wait mode	Main clock off On-chip oscillator on=125 kHz When a WAIT instruction is executed(1) Peripheral clock off	—	35	70	µA
		Stop mode	Main clock off, Topr = 25°C On-chip oscillator off CM10="1" Peripheral clock off	—	0.7	3.0	µA

NOTES:
1. Timer Y is operated with timer mode.
2. Referenced to V_{CC}=AV_{CC}=2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=10MHz unless otherwise specified.

Timing requirements (Unless otherwise noted: Vcc = 3V, Vss = 0V at Topr = 25 °C) [Vcc=3V]

Table 16.16 XIN input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(XIN)	XIN input cycle time	100	–	ns
tWH(XIN)	XIN input HIGH pulse width	40	–	ns
tWL(XIN)	XIN input LOW pulse width	40	–	ns

Table 16.17 CNTR0 input, CNTR1 input, $\overline{\text{INT2}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CNTR0)	CNTR0 input cycle time	300	–	ns
tWH(CNTR0)	CNTR0 input HIGH pulse width	120	–	ns
tWL(CNTR0)	CNTR0 input LOW pulse width	120	–	ns

Table 16.18 TCIN input, $\overline{\text{INT3}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TCIN)	TCIN input cycle time	1200[1]	–	ns
tWH(TCIN)	TCIN input HIGH pulse width	600[2]	–	ns
tWL(TCIN)	TCIN input LOW pulse width	600[2]	–	ns

NOTES:
1. When using the Timer C capture function, adjust the cycle time above (1/ Timer C count source frequency x 3).
2. When using the Timer C capture function, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 16.19 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(CK)	CLKi input cycle time	300	–	ns
tW(CKH)	CLKi input HIGH pulse width	150	–	ns
tW(CKL)	CLKi input LOW pulse width	150	–	ns
td(C-Q)	TxDi output delay time	–	160	ns
th(C-Q)	TxDi hold time	0	–	ns
tsu(D-C)	RxDi input setup time	55	–	ns
th(C-D)	RxDi input hold time	90	–	ns

Table 16.20 External interrupt $\overline{\text{INT0}}$ input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tW(INH)	$\overline{\text{INT0}}$ input HIGH pulse width	380[1]	–	ns
tW(INL)	$\overline{\text{INT0}}$ input LOW pulse width	380[2]	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{\text{INT0}}$ input filter select bit, use the $\overline{\text{INT0}}$ input HIGH pulse width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{\text{INT0}}$ input filter select bit, use the $\overline{\text{INT0}}$ input LOW pusle width to the greater value,either (1/ digital filter clock frequency x 3) or the minimum value of standard.

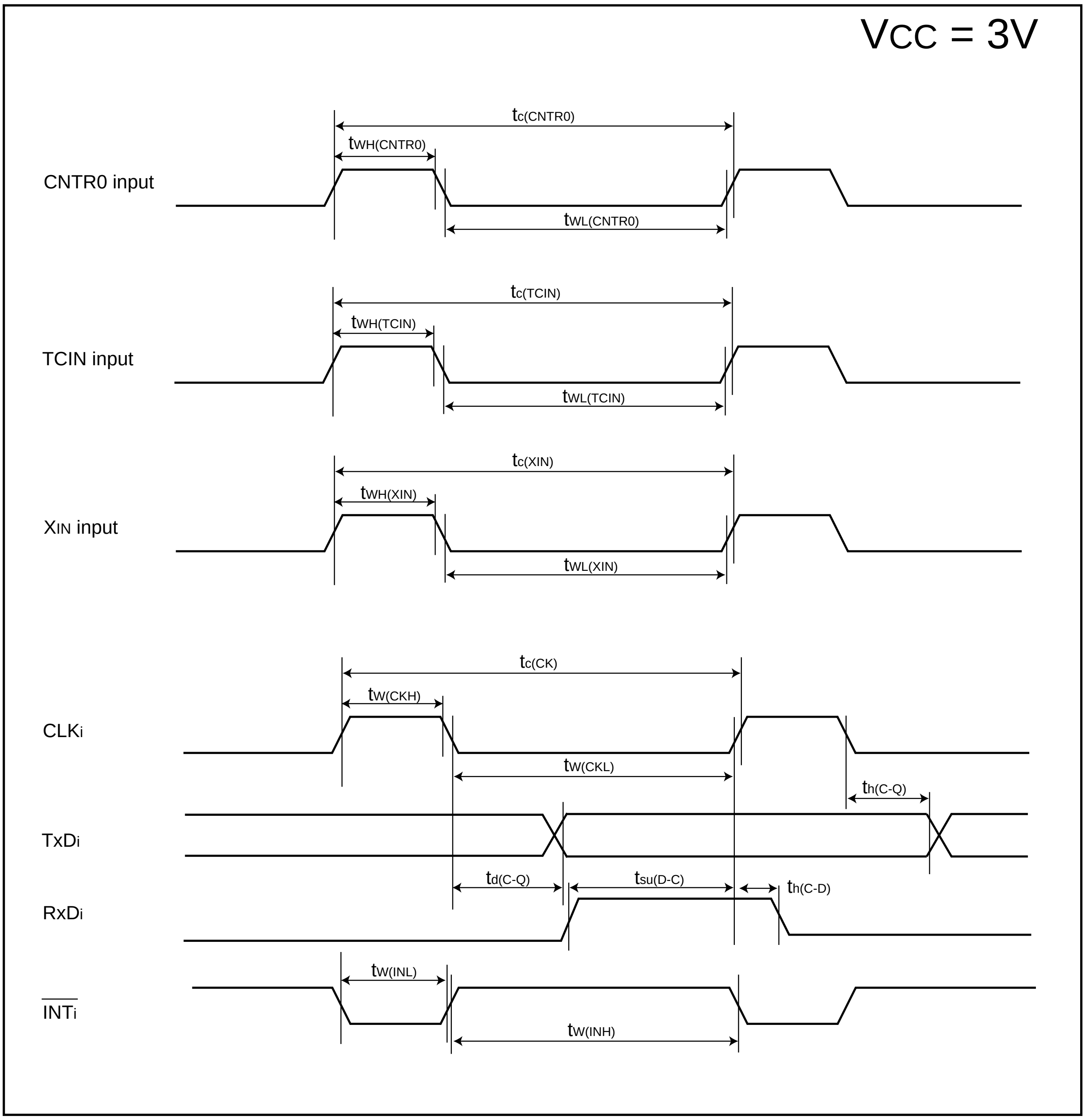


Figure 16.4 Vcc=3V timing diagram

17. Flash Memory Version

17.1 Overview

The flash memory version has two modes—CPU rewrite and standard serial I/O—in which its flash memory can be operated on.

Table 17.1 outlines the performance of flash memory version (see “Table 1.1 Performance” for the items not listed on Table 17.1).

Table 17.1 Flash Memory Version Performance

Item		Specification
Flash memory operating mode		2 modes (CPU rewrite and standard serial I/O)
Erase block		See “Figure 17.1. Flash Memory Block Diagram”
Method for program		In units of byte
Method for erasure		Block erase
Program, erase control method		Program and erase controlled by software command
Protect method		Protect for Block 0 and 1 by FMR02 bit in FMR0 register
		Protect for Block 0 by FMR16 bit and Block 1 by FMR16 bit
Number of commands		5 commands
Number of program and erasure(1)	Block0 and 1 (program ROM)	1,000 times
	BlockA and B (data flash)	10,000 times
ROM code protection		Standard serial I/O mode is supported.

NOTES:
1. Definition of program/erase times
   The program/erase times are defined to be per-block erase times. When the program/erase times are n times (n=1,000 or 10,000 times), to erase n times per block is possible. For example, if performing one-byte write to the distinct addresses on the Block A of 2K-byte block 2,048 times and then erasing that block, the number of the program/erase cycles is one time. if rewriting more than 1,000 times, run the program until the vacant areas are all used to reduce the substantial rewrite times and then erase. Avoid rewriting only particular blocks and rewrite to average the program and erase times to each block. Also keep the erase times as inrformation and set up the limit times.

Table 17.2 Flash Memory Rewrite Modes

Flash memory rewrite mode	CPU rewrite mode	Standard serial I/O mode
Function	User ROM area is rewritten by executing software commands from the CPU. EW0 mode: Can be rewritten in any area other than the flash memory EW1 mode: Can be rewritten in the flash memory	User ROM area is rewritten by using a dedicated serial programmer. Standard serial I/O mode 1 : Clock synchronous serial I/O Standard serial I/O mode 2 : UART
Areas which can be rewritten	User ROM area	User ROM area
Operation mode	Single chip mode	Boot mode
ROM programmer	None	Serial programmer

17.2 Memory Map

The ROM in the flash memory version is separated between a user ROM area and a boot ROM area (reserved area). Figure 17.1 shows the block diagram of flash memory.

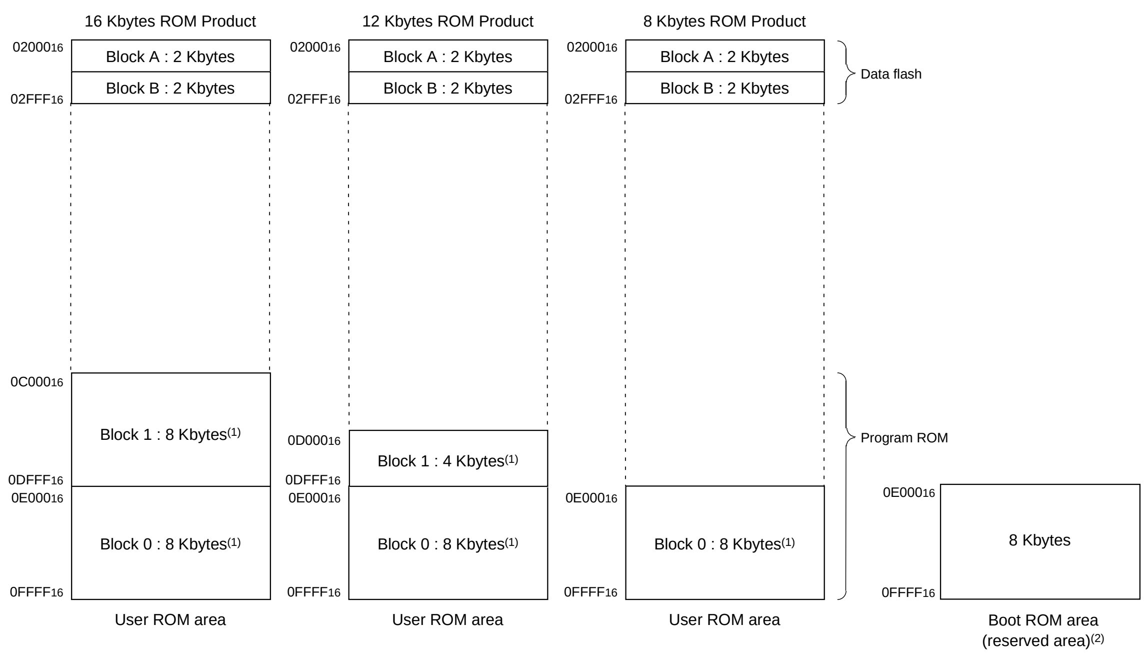
The user ROM area has the 2K-byte Block A and the 2K-byte Block B (data flash), in addition to an area (program ROM) which stores the microcomputer operation program.

The user ROM area is divided into several blocks. The user ROM area can be rewritten in CPU rewrite and standard serial I/O modes.

When rewriting the Block 0 and Block 1 in CPU rewrite mode, set the FMR02 bit in the FMR0 register to “1” (rewrite enabled), and when setting the FMR15 bit in the FMR1 register to “0” (rewrite enabled), the Block 0 is rewritable. When setting the FMR16 bit to “0” (rewrite enabled), the Block 1 is rewritable. Also when setting the PM10 bit in the PM1 register to “1”(enabled), the Block A and Block B are usable.

The rewrite program for standard serial I/O mode is stored in the boot ROM area before shipment.

The boot ROM area and the user ROM area share the same address, but have an another memory.



NOTES:
1. When setting the FMR02 bit in the FMR0 register to “1” (rewrite enabled) and the FMR15 bit in the FMR1 register to “0” (rewrite enabled), the Block 0 is rewritable. When setting the FMR16 bit to “0” (rewrite enabled), the Block 1 is rewritable (only for CPU rewrite mode).
2. This area is to store the boot program provided by Renesas Technology.

Figure 17.1 Flash Memory Block Diagram

17.3 Functions To Prevent Flash Memory from Rewriting

To prevent the flash memory from being read or rewritten easily, standard serial input/output mode has an ID code check function.

17.3.1 ID Code Check Function

Use this function in standard serial input/output mode. Unless the flash memory is blank, the ID codes sent from the programmer and the ID codes written in the flash memory are compared to see if they match. If the ID codes do not match, the commands sent from the programmer are not accepted. The ID code consists of 8-bit data, the areas of which, beginning with the first byte, are $00FFDF_{16}$, $00FFE3_{16}$, $00FFEB_{16}$, $00FFEF_{16}$, $00FFF3_{16}$, $00FFF7_{16}$, and $00FFFB_{16}$. Prepare a program in which the ID codes are preset at these addresses and write it in the flash memory.

Address		
$00FFDF_{16}$ to $00FFDC_{16}$	ID1	Undefined instruction vector
$00FFE3_{16}$ to $00FFE0_{16}$	ID2	Overflow vector
$00FFE7_{16}$ to $00FFE4_{16}$		BRK instruction vector
$00FFEB_{16}$ to $00FFE8_{16}$	ID3	Address match vector
$00FFEF_{16}$ to $00FFEC_{16}$	ID4	Single step vector
$00FFF3_{16}$ to $00FFF0_{16}$	ID5	Oscillation stop detection/watchdog timer vector/voltage detection
$00FFF7_{16}$ to $00FFF4_{16}$	ID6	(Reserved)
$00FFFB_{16}$ to $00FFF8_{16}$	ID7	(Reserved)
$00FFFF_{16}$ to $00FFFC_{16}$	(Note 1)	Reset vector

4 bytes

NOTES:
1. The OFS register is assigned to the $00FFFF_{16}$ address. Refer to "Figure11.2 OFS, WDC, WDTR and WDTS registers for the OFS register details.

Figure 17.2 Address for ID Code Stored

17.4 CPU Rewrite Mode

In CPU rewrite mode, the user ROM area can be rewritten by executing software commands from the CPU. Therefore, the user ROM area can be rewritten directly while the microcomputer is mounted on-board without having to use a ROM programmer, etc. Make sure the Program and the Block Erase commands are executed only on each block in the user ROM area.

For interrupts requested during an erase operation in CPU rewrite mode, the R8C/10 flash module offers an `erase-suspend` feature which allow the erase operation to be suspended, and access made available to the flash.

During CPU rewrite mode, the user ROM area be operated on in either Erase Write 0 (EW0) mode or Erase Write 1 (EW1) mode. Table 17.3 lists the differences between Erase Write 0 (EW0) and Erase Write 1 (EW1) modes.

Table 17.3 EW0 Mode and EW1 Mode

Item	EW0 mode	EW1 mode
Operation mode	Single chip mode	Single chip mode
Areas in which a rewrite control program can be located	User ROM area	User ROM area
Areas in which a rewrite control program can be executed	Must be transferred to any area other than the flash memory (e.g., RAM) before being executed	Can be executed directly in the user ROM area
Areas which can be rewritten	User ROM area	User ROM area However, this does not include the block in which a rewrite control program exists(1)
Software command limitations	None	• Program, Block Erase command Cannot be executed on any block in which a rewrite control program exists • Read Status Register command Cannot be executed
Modes after Program or Erase	Read Status Register mode	Read Array mode
CPU status during Auto Write and Auto Erase	Operating	Hold state (I/O ports retain the state in which they were before the command was executed)
Flash memory status detection	• Read the FMR0 register FMR00, FMR06, and FMR07 bits in a program • Execute the Read Status Register command to read the status register SR7, SR5, and SR4.	Read the FMR0 register FMR00, FMR06, and FMR07 bits in a program
Conditions for transferring to erase-suspend	Set the FMR40 and FMR41 bits in the FMR4 register to “1” by program.	When an interrupt which is set for enabled occurs while the FMR40 bit in the FMR4 register is set to “1”.
CPU Clock	5MHz or below	No restriction to the following (clock frequency to be used)

NOTES:
1. Block 1 and Block 0 are enabled for rewrite by setting the FMR02 bit in the FMR0 register to “1” (rewrite enabled).

17.4.1 EW0 Mode

The microcomputer is placed in CPU rewrite mode by setting the FMR01 bit in the FMR0 register to “1” (CPU rewrite mode enabled), ready to accept commands. In this case, because the FMR1 register's FMR11 bit = 0, EW0 mode is selected.

Use software commands to control program and erase operations. Read the FMR0 register or status register to check the status of program or erase operation at completion.

When moving to an erase-suspend during auto-erase, set the FMR40 bit to “1” (erase-suspend enabled) and the FMR41 bit to “1” (erase-suspend requested). Make sure that the FMR46 bit is set to “1” (enables reading) before accessing the user ROM space. The auto-erase operation resumes by setting the FMR41 bit to “0” (erase restart).

17.4.2 EW1 Mode

EW1 mode is selected by setting FMR11 bit to “1” (EW1 mode) after setting the FMR01 bit to “1” (CPU rewrite mode enabled).

Read the FMR0 register to check the status of program or erase operation at completion. Avoid executing software commands of Read Status register in EW1 mode.

To enable the erase-suspend function, the Block Erase command should be executed after setting the FMR40 bit to “1” (erase-suspend enabled). An interrupt to request an erase-suspend must be in enabled state. After passing td(SR-ES) since the block erase command is executed, an interrupt request can be acknowledged.

The FMR41 bit is automatically set to “1” (erase-suspend requested) if the auto-erase operation is halted by an interrupt request. If the erase operation is not completed (FMR00 bit is “0”) when the interrupt routine is ended, the Block Erase command should be executed again by setting the FMR41 bit to “0” (erase restart).

Figure 17.3 shows the FMR0 register. Figure 17.4 shows the FMR1 and FMR4 registers.

- **FMR00 Bit**

  This bit indicates the operating status of the flash memory. The bit is “0” during programming, erasing, or erase-suspend mode; otherwise, the bit is “1”.

- **FMR01 Bit**

  The microcomputer is made ready to accept commands by setting the FMR01 bit to “1” (CPU rewrite mode).

- **FMR02 Bit**

  The Block1 and Block0 do not accept the Program and Block Erase commands if the FMR02 bit is set to “0” (rewrite disabled).

  The Block0 and Block1 are controlled rewriting in the FMR15 and FMR16 bits if the FMR02 bit is set to “1” (rewrite enabled).

- **FMSTP Bit**

  This bit is provided for initializing the flash memory control circuits, as well as for reducing the amount of current consumed in the flash memory. The flash memory is disabled against access by setting the FMSTP bit to “1”. Therefore, the FMSTP bit must be written to by a program in other than the flash memory.

  In the following cases, set the FMSTP bit to “1”:

  - When flash memory access resulted in an error while erasing or programming in EW0 mode (FMR00 bit not reset to “1” (ready))
  - When entering on-chip oscillator mode (main clock stop).

  Figure 17.7 shows a flow chart to be followed before and after entering on-chip oscillator mode (main clock stop).

  Note that when going to stop or wait mode while the CPU rewrite mode is disabled, the FMR0 register does not need to be set because the power for the flash memory is automatically turned off and is turned back on again after returning from stop or wait mode.

- **FMR06 Bit**

  This is a read-only bit indicating the status of auto program operation. The bit is set to “1” when a program error occurs; otherwise, it is cleared to “0”. For details, refer to the description of “17.4.5 Full Status Check”.

- **FMR07 Bit**

  This is a read-only bit indicating the status of auto erase operation. The bit is set to “1” when an erase error occurs; otherwise, it is set to “0”. For details, refer to the description of "17.4.5 Full status check".

- **FMR11 Bit**

  Setting this bit to “1” (EW1 mode) places the microcomputer in EW1 mode.

- **FMR15 Bit**

  When the FMR02 bit is set to “1” (rewrite enabled) and the FMR15 bit is set to “0” (rewrite enabled), the Block0 accepts the program command and block erase command.

- **FMR16 Bit**

  When the FMR02 bit is set to “1” (rewrite enabled) and the FMR16 bit is set to “0” (rewrite enabled), the Block1 accepts the program command and block erase command.

- **FMR40 bit**

  The erase-suspend function is enabled by setting the FMR40 bit to “1” (valid).

- **FMR41 bit**

  In EW0 mode, the flash module goes to erase-suspend mode when the FMR41 bit is set to “1”. In EW1 mode, the FMR41 bit is automatically set to “1” (erase-suspend requested) when an enabled interrupt occurred, and then the flash module goes to erase-suspend mode.

  The auto-erase operation restarts when the FMR41 bit is set to “0” (erase restart).

- **FMR46 bit**

  The FMR46 bit is set to “0”(disables reading) during auto-erase execution and set to “1”(enables reading) during erase-suspend mode. Do not access to the flash memory when this bit is set to “0”.

Flash memory control register 0

b7	b6	b5	b4	b3	b2	b1	b0
		0	0				

Symbol: FMR0 Address: $01B7_{16}$ After reset: 00000001_2

Bit symbol	Bit name	Function	RW
FMR00	RY/$\overline{BY}$ status flag	0: Busy (being written or erased) 1: Ready	RO
FMR01	CPU rewrite mode select bit(1, 6)	0: Disable CPU rewrite mode 1: Enable CPU rewrite mode	RW
FMR02	Block0 and 1 rewrite enable bit(2, 6, 7)	0: Rewrite disabled 1: Rewrite enabled	RW
FMSTP	Flash memory stop bit(3, 5, 6)	0: Enable flash memory operation 1: Stops flash memory operation (placed in low power mode, flash memory initialized)	RW
(b5-b4)	Reserved bit	Set to “0”	RW
FMR06	Program status flag(4)	0: Terminated normally 1: Terminated in error	RO
FMR07	Erase status flag(4)	0: Terminated normally 1: Terminated in error	RO

NOTES:
1. To set this bit to “1”, write “0” and then “1” in succession. Make sure no interrupts will occur before writing “1” after writing “0”.
   Set the microcomputer in read array mode before writing to this bit.
2. To set this bit to “1”, write “0” and then “1” in succession when the FMR01 bit = 1. Make sure no interrupts will occur before writing “1” after writing “0”.
3. Write to this bit from a program in other than the flash memory.
4. This flag is set to “0” by executing the Clear Status command.
5. Effective when the FMR01 bit = 1 (CPU rewrite mode). If the FMR01 bit = 0, although the FMSTP bit can be set to “1” by writing “1”, the flash memory is neither placed in low power mode nor initialized.
6. Use the bit process instruction to set the FMR01, FMR02 and FMSTP bits (Refer to “R8C/Tiny Series Sofware Manual”.
7. When setting the FMR01 bit to “0” (disable CPU rewrite mode), the FMR02 bit is set to “0” (rewrite disabled).

Figure 17.3 FMR0 Register

Flash memory control register 1

b7	b6	b5	b4	b3	b2	b1	b0
1			0	0	0		

Symbol: FMR1 Address: $01B5_{16}$ After reset: $1000000X_2$

Bit symbol	Bit name	Function	RW
(b0)	Reserved bit	When read, its content is indeterminate.	RO
FMR11	EW1 mode select bit(1, 2)	0: EW0 mode 1: EW1 mode	RW
(b4-b2)	Reserved bit	Set to “0”	RW
FMR15	Block0 rewrite disable bit(2, 3)	0 : Rewrite enabled 1 : Rewrite disabled	RW
FMR16	Block1 rewrite disable bit(2, 3)	0 : Rewrite enabled 1 : Rewrite disabled	RW
(b7)	Reserved bit	Set to “1”	RW

NOTES:
1. To set this bit to “1”, write “0” and then “1” (CPU rewrite mode enabled) in succession when the FMR01 bit = 1. Make sure no interrupts will occur before writing “1” after writing “0”.
2. This bit is set to “0” by setting the FMR01 bit to “0” (CPU rewrite mode disabled).
3. When the FMR01 bit is “1” (CPU rewrite mode enabled), the FMR15 and FMR16 bits are rewritable.
   To set this bit to “0”, write “1” and then “0” in succession.
   To set this bit to “1”, write “1”.

Flash memory control register 4

b7	b6	b5	b4	b3	b2	b1	b0
0		0	0	0	0		

Symbol: FMR4 Address: $01B3_{16}$ After reset: 01000000_2

Bit symbol	Bit name	Function	RW
FMR40	Erase-suspend function enable bit(1)	0: Invalid 1: Valid	RW
FMR41	Erase-suspend request bit(2)	0: Erase restart 1: Erase-suspend request	RW
(b5-b2)	Reserved bit	Set to “0”	RO
FMR46	Read status flag	0: Disable reading 1: Enable reading	RO
(b7)	Reserved bit	Set to “0”	RW

NOTES:
1. To set this bit to “1”, write “0” and then “1” in succession. Make sure no interrupts will occur before writing “1” after writing “0”.
2. This bit is valid only when the FMR40 bit is set to “1” (valid) and can only be written before ending an erase after issuing an erase command. Other than this period, this bit is set to “0”.
   In EW0 mode, this bit can be set to “0” and “1” by program.
   In EW1 mode, this bit is automatically set to “1” if a maskable interrupt occurs during an erase operation while the FMR40 bit is set to “1”. This bit can not be set to “1” by program. (Can be set to “0”.)

Figure 17.4 FMR1 and FMR4

Figures 17.5 shows the timing on suspend operation.

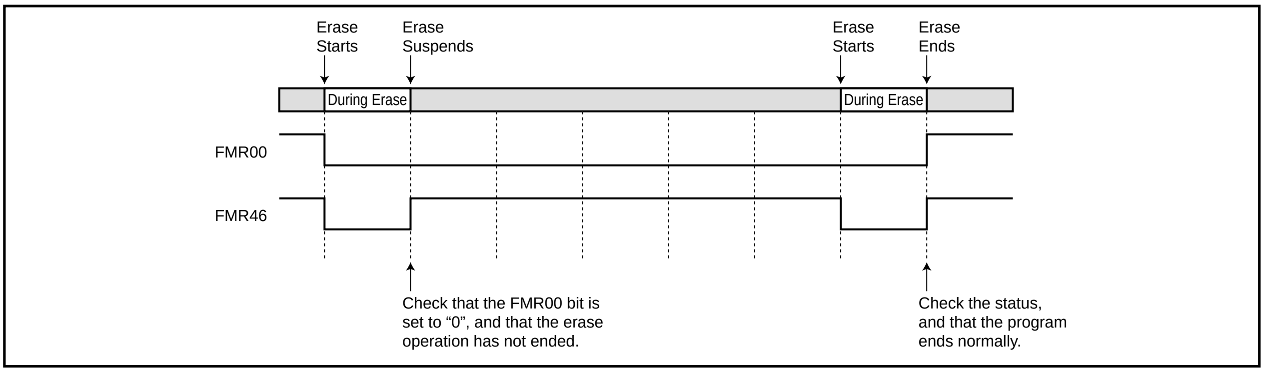
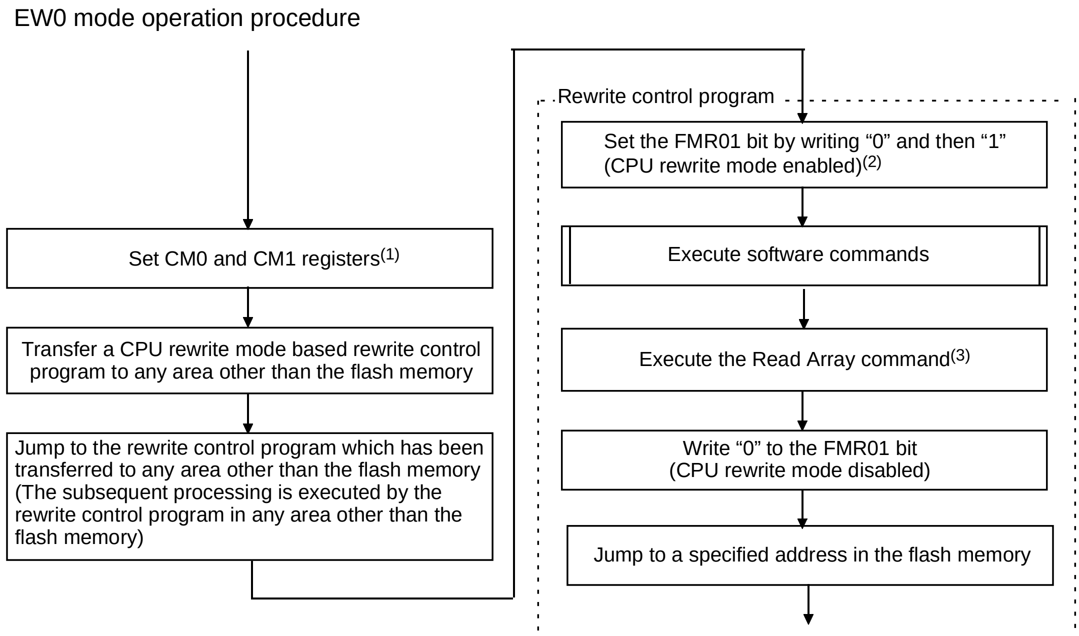


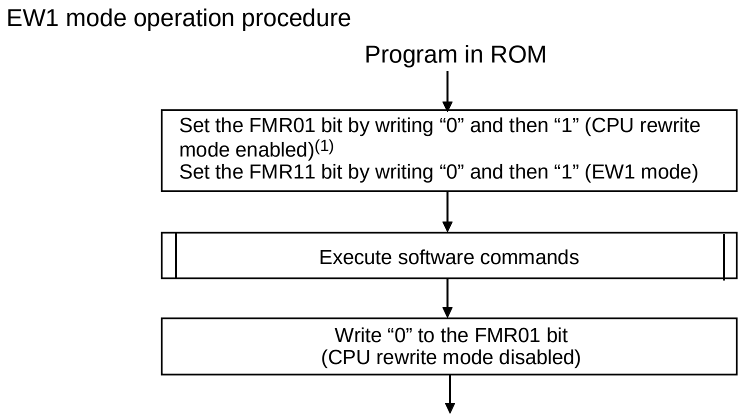
Figure 17.5 Timing on Suspend Operation

Figures 17.6 and 17.7 show the setting and resetting of EW0 mode and EW1 mode, respectively.



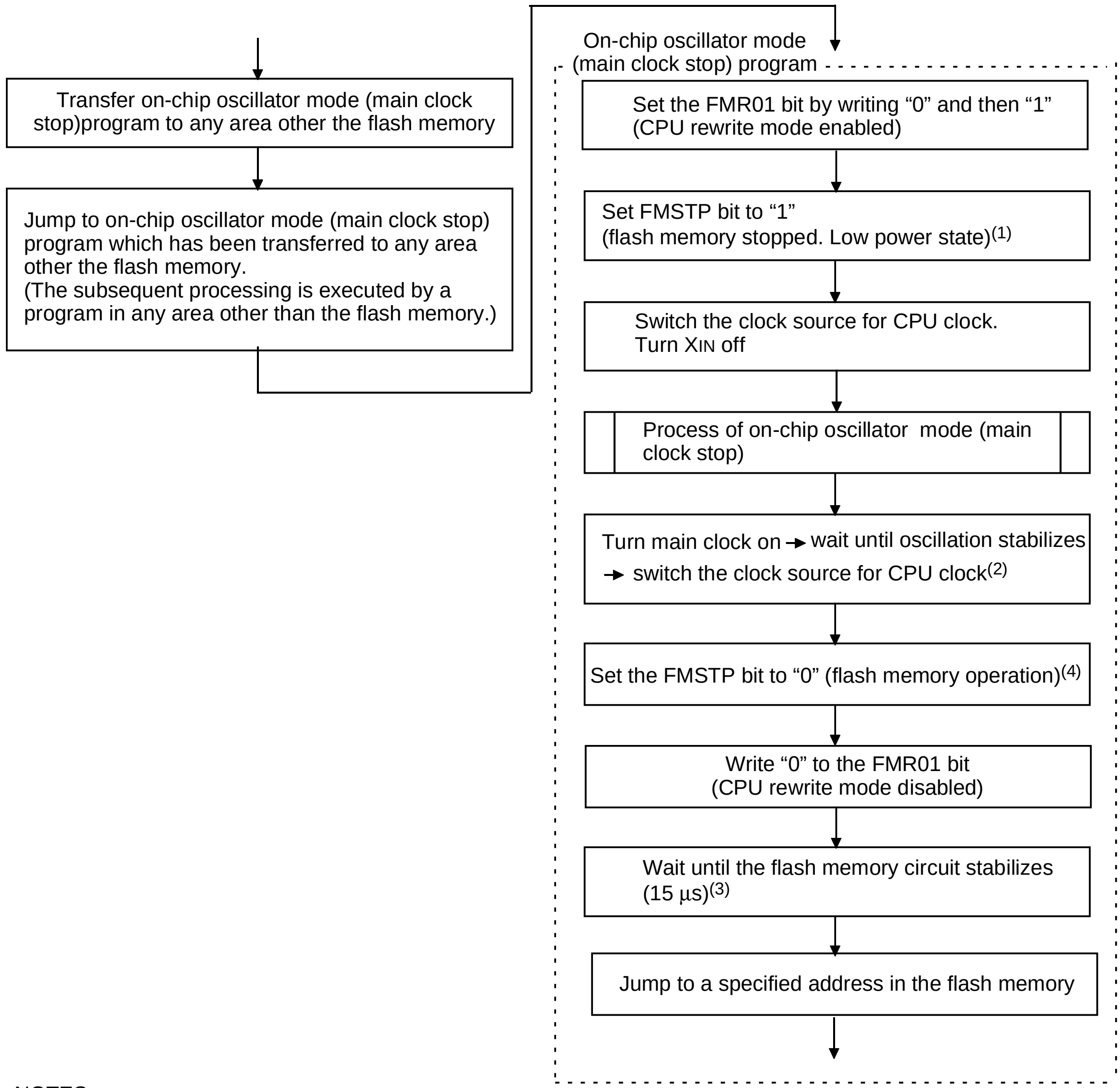
NOTES:
1. Select 5 MHz or less for CPU clock using the CM06 bit in the CM0 register and the CM17 to CM16 bits in the CM1 register.
2. To set the FMR01 bit to "1", write "0" and then "1" in succession. Make sure no interrupts will occur before writing "1" after writing "0". Write to the FMR01 bit from a program in other than the flash memory.
3. Disables the CPU rewrite mode after executing the Read Array command.

Figure 17.6 Setting and Resetting of EW0 Mode



NOTES:
1. To set the FMR01 bit to "1", write "0" and then "1" in succession. Make sure no interrupts will occur before writing "1" after writing "0".

Figure 17.7 Setting and Resetting of EW1 Mode



NOTES:
1. Set the FMR01 bit to “1” (CPU rewrite mode) before setting the FMSTP bit to “1” .
2. Before the clock source for CPU clock can be changed, the clock to which to be changed must be stable.
3. Insert a 15 µs wait time in a program. Avoid accessing to the flash memory during this wait time.
4. Ensure 10 µs until setting “0” (flash memory operates) after setting the FMSTP bit to “1” (flash memory stops).

Figure 17.8 Process to Reduce Power Consumption in On-Chip Oscillator Mode (Main Clock Stop)

17.4.3 Software Commands

Software commands are described below. The command code and data must be read and written in 8-bit units.

Table 17.4 Software Commands

Command	First bus cycle			Second bus cycle		
	Mode	Address	Data (D_7 to D_0)	Mode	Address	Data (D_7 to D_0)
Read array	Write	X	FF_{16}			
Read status register	Write	X	70_{16}	Read	X	SRD
Clear status register	Write	X	50_{16}			
Program	Write	WA	40_{16}	Write	WA	WD
Block erase	Write	X	20_{16}	Write	BA	$D0_{16}$

SRD: Status register data (D_7 to D_0)
WA: Write address (Make sure the address value specified in the the first bus cycle is the same address as the write address specified in the second bus cycle.)
WD: Write data (8 bits)
BA: Given block address
X: Any address in the user ROM area

- **Read Array Command**

This command reads the flash memory.

Writing 'FF_{16}' in the first bus cycle places the microcomputer in read array mode. Enter the read address in the next or subsequent bus cycles, and the content of the specified address can be read in 8-bit units.

Because the microcomputer remains in read array mode until another command is written, the contents of multiple addresses can be read in succession.

- **Read Status Register Command**

This command reads the status register.

Write '70_{16}' in the first bus cycle, and the status register can be read in the second bus cycle. (Refer to Section 17.4.4, "Status Register.") When reading the status register too, specify an address in the user ROM area.

Avoid executing this command in EW1 mode.

- **Clear Status Register Command**

This command sets the status register to "0".

Write '50_{16}' in the first bus cycle, and the FMR06 to FMR07 bits in the FMR0 register and SR4 to SR5 in the status register will be set to "0".

• **Program**

This command writes data to the flash memory in one byte units.
Write ‘40_{16}’ in the first bus cycle and write data to the write address in the second bus cycle, and an auto program operation (data program and verify) will start. Make sure the address value specified in the first bus cycle is the same address as the write address specified in the second bus cycle.
Check the FMR00 bit in the FMR0 register to see if auto programming has finished. The FMR00 bit is “0” during auto programming and set to “1” when auto programming is completed.
Check the FMR06 bit in the FMR0 register after auto programming has finished, and the result of auto programming can be known. (Refer to Section 17.4.5, “Full Status Check.”)
Writing over already programmed addresses is inhibited.
When the FMR02 bit in the FMR0 register is set to “0” (rewrite disabled), or the FMR02 bit is set to “1” (rewrite enabled) and the FMR15 bit in the FMR1 register is set to “1” (rewrite disabled), the program command on the Block0 is not accepted. When the FMR16 bit is set to “1” (rewrite disabled), the program command on the Block1 is not accepted.
When the FMR02 bit in the FMR0 register is set to “0” (rewrite disabled), the Program command on the Block0 and Block1 is not accepted.
In EW1 mode, do not execute this command on any address at which the rewrite control program is located.
In EW0 mode, the microcomputer goes to read status register mode at the same time auto programming starts, making it possible to read the status register. The status register bit 7 (SR7) is set to “0” at the same time auto programming starts, and set back to “1” when auto programming finishes. In this case, the microcomputer remains in read status register mode until a read array command is written next. The result of auto programming can be known by reading the status register after auto programming has finished.

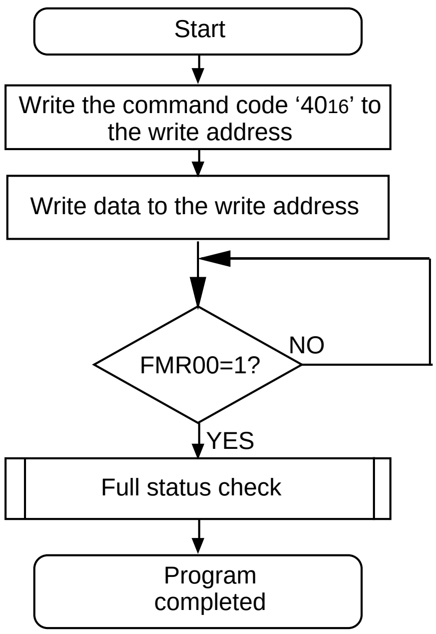


Figure 17.9 Program Flow Chart

• **Block Erase**

Write '20_{16}' in the first bus cycle and write '$D0_{16}$' to the given address of a block in the second bus cycle, and an auto erase operation (erase and verify) will start.
Check the FMR00 bit in the FMR0 register to see if auto erasing has finished.
The FMR00 bit is "0" during auto erasing and set to "1" when auto erasing is completed.
Check the FMR07 bit in the FMR0 register after auto erasing has finished, and the result of auto erasing can be known. (Refer to Section 17.4.5, "Full Status Check.")
When the FMR02 bit in the FMR0 register is set to "0" (rewrite disabled), the Block Erase command on the Block0 and Block1 is not accepted.
Figure 17.10 shows an example of a block erase flowchart when the erase-suspend function is not used. Figure 17.11 shows an example of a block erase flowchart when the erase-suspend function is used.
In EW1 mode, do not execute this command on any address at which the rewrite control program is located.
In EW0 mode, the microcomputer goes to read status register mode at the same time auto erasing starts, making it possible to read the status register. The status register bit 7 (SR7) is cleared to "0" at the same time auto erasing starts, and set back to "1" when auto erasing finishes. In this case, the microcomputer remains in read status register mode until the Read Array command is written next.

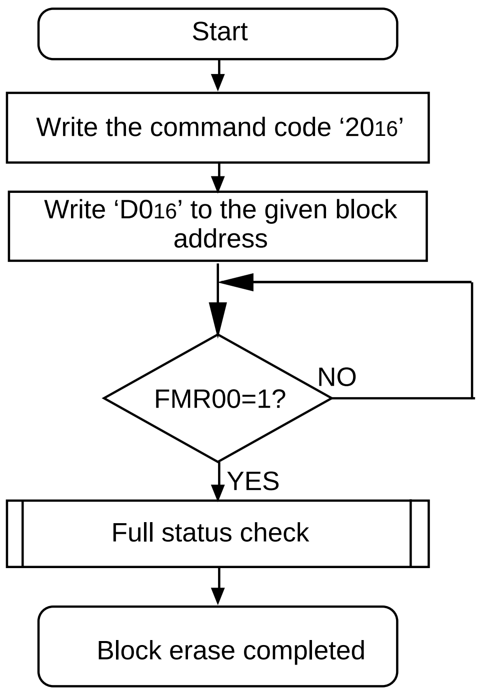
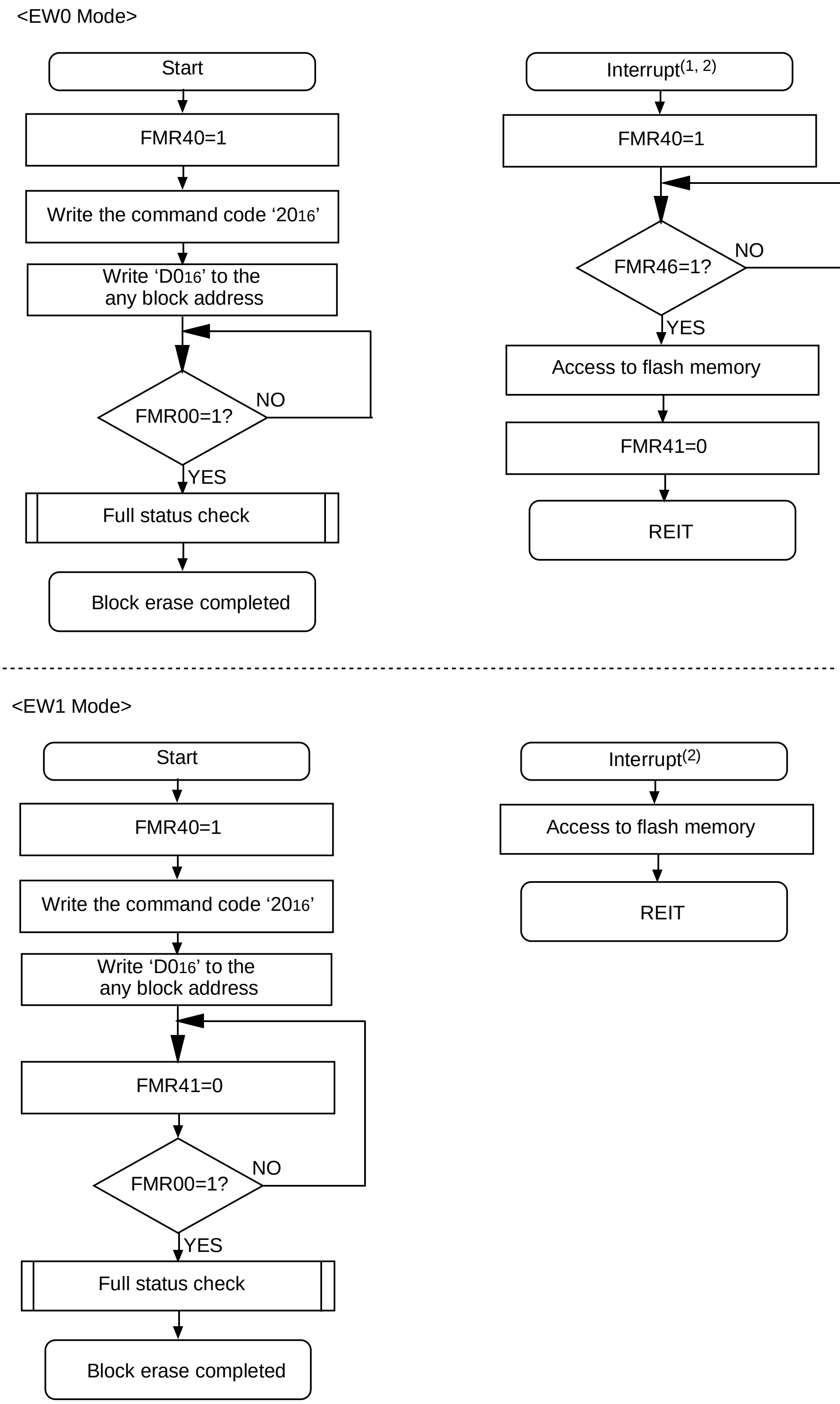


Figure 17.10 Block Erase Flow Chart (When Not Using Erase-suspend Function)



NOTES:
1. In EW0 mode, interrupt vector table for an interrupt used should be located in the RAM space.
2. td(SR-ES) is needed after an interrupt requst is generated before being acknowledged.
The interrupt to enter an erase-suspend should be in interrupt enabled status.

Figure 17.11 Block Erase Command (When Using Erase-suspend Function)

17.4.4 Status Register

The status register indicates the operating status of the flash memory and whether an erase or programming operation terminated normally or in error. The status of the status register can be known by reading the FMR00, FMR06, and FMR07 bits in the FMR0 register.

Table 17.5 lists the status register.

In EW0 mode, the status register can be read in the following cases:

(1) When a given address in the user ROM area is read after writing the Read Status Register command

(2) When a given address in the user ROM area is read after executing the Program or Block Erase command but before executing the Read Array command.

• Sequence Status (SR7 and FMR00 Bits)

The sequence status indicates the operating status of the flash memory. SR7 = 0 (busy) during auto programming and auto erase, and is set to “1” (ready) at the same time the operation finishes.

• Erase Status (SR5 and FMR07 Bits)

Refer to Section 17.4.5, “Full Status Check.”

• Program Status (SR4 and FMR06 Bits)

Refer to Section 17.4.5, “Full Status Check.”

Table 17.5 Status Register

Status register bit	FMR0 register bit	Status name	Contents		Value after reset
			"0"	"1"	
SR7 (D7)	FMR00	Sequencer status	Busy	Ready	1
SR6 (D6)	——	Reserved	-	-	——
SR5 (D5)	FMR07	Erase status	Terminated normally	Terminated in error	0
SR4 (D4)	FMR06	Program status	Terminated normally	Terminated in error	0
SR3 (D3)	——	Reserved	-	-	——
SR2 (D2)	——	Reserved	-	-	——
SR1 (D1)	——	Reserved	-	-	——
SR0 (D0)	——	Reserved	-	-	——

• D7 to D0: Indicates the data bus which is read out when the Read Status Register command is executed.
• The FMR07 bit (SR5) and FMR06 bit (SR4) are set to “0” by executing the Clear Status Register command.
• When the FMR07 bit (SR5) or FMR06 bit (SR4) = 1, the Program and Block Erase commands are not accepted.

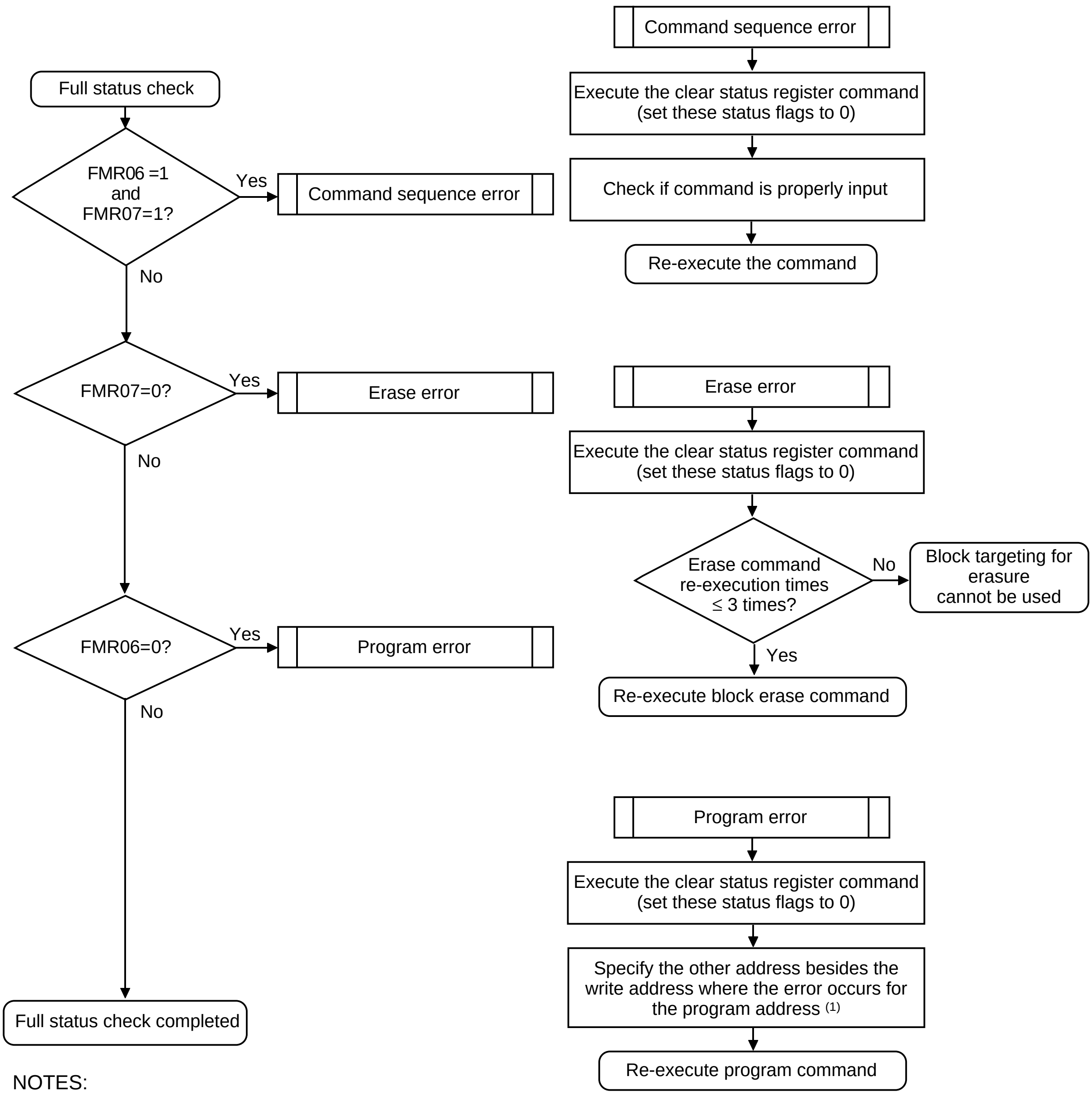
17.4.5 Full Status Check

When an error occurs, the FMR06 to FMR07 bits in the FMR0 register are set to “1”, indicating occurrence of each specific error. Therefore, execution results can be verified by checking these status bits (full status check). Table 17.6 lists errors and FMR0 register status. Figure 17.12 shows a full status check flowchart and the action to be taken when each error occurs.

Table 17.6 Errors and FMR0 Register Status

FRM00 register (status register) status		Error	Error occurrence condition
FMR07 (SR5)	FMR06 (SR4)		
1	1	Command sequence error	• When any command is not written correctly • When invalid data was written other than those that can be written in the second bus cycle of the Block Erase command (i.e., other than “D0$_{16}$” or “FF$_{16}$”)[1] • When executing the program command or block erase command while rewriting is disabled using the FMR02 bit in the FMR0 register, the FMR15 or FMR16 bit in the FMR1 register. • When inputting and erasing the address in which the Flash memory is not allocated during the erase command input. • When executing to erase the block which disables rewriting during the erase command input. • When inputting and writing the address in which the Flash memory is not allocated during the write command input. • When executing to write the block which disables rewriting during the write command input.
1	0	Erase error	• When the Block Erase command was executed but not automatically erased correctly
0	1	Program error	• When the Program command was executed but not automatically programmed correctly.

NOTES:
1. Writing ‘FF$_{16}$’ in the second bus cycle of these commands places the microcomputer in read array mode, and the command code written in the first bus cycle is nullified.



NOTES:
1. To rewrite to the address where the program error occurs, check if the full status check is complete normally and write to the address after the block erase command is executed.

Figure 17.12 Full Status Check and Handling Procedure for Each Error

17.5 Standard Serial I/O Mode

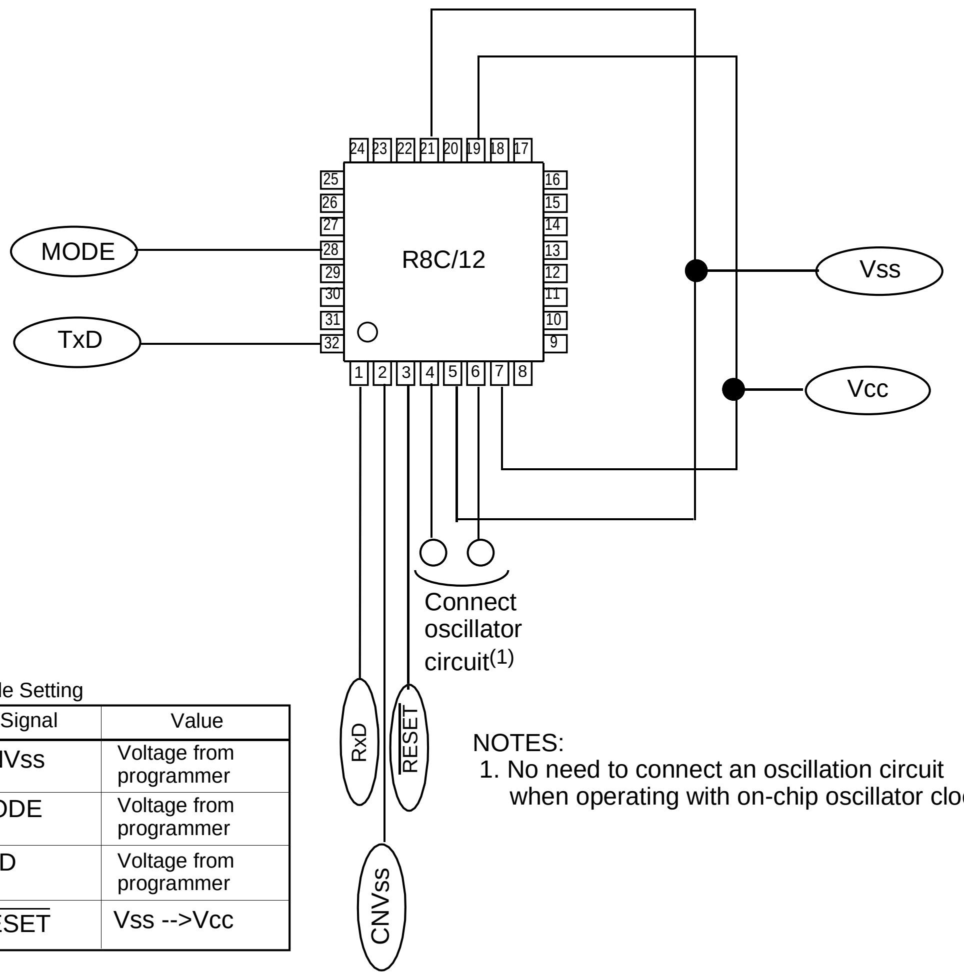
In standard serial I/O mode, the user ROM area can be rewritten while the microcomputer is mounted on-board by using a serial programmer suitable for this microcomputer. Standard serial I/O mode has standard serial I/O mode 1 of the clock synchronous serial and standard serial I/O mode 2 of the clock asynchronous serial. Refer to "Appendix 2 Connecting Examples for Serial Writer and On-chip Debugging Emulator".For more information about serial programmers, contact the manufacturer of your serial programmer. For details on how to use, refer to the user's manual included with your serial programmer. Table 17.7 lists pin functions (flash memory standard serial I/O mode). Figures 17.13 to 17.15 show pin connections for standard serial I/O mode.

17.5.1 ID Code Check Function

This function determines whether the ID codes sent from the serial programmer and those written in the flash memory match (refer to Section 17.3, "Functions to Prevent Flash Memory from Rewriting").

Table 17.7 Pin Functions (Flash Memory Standard Serial I/O Mode)

Pin	Name	I/O	Description
V_{CC},V_{SS}	Power input		Apply the voltage guaranteed for Program and Erase to Vcc pin and 0V to Vss pin.
IV_{CC}	IV_{CC}		Connect capacitor (0.1 µF) to Vss.
$\overline{RESET}$	Reset input	I	Reset input pin.
$P4_6$/X_{IN}	$P4_6$ input/Clock input	I	Connect a ceramic resonator or crystal oscillator between X_{IN} and X_{OUT} pins in standard serial I/O mode 2. When using the main clock in standard serial I/O mode 1, connect a ceramic resonator or crystal oscillator between X_{IN} and X_{OUT} pins. When not using the main clock in standard serial I/O mode 1, connect this pin to Vcc via a resistor(pull-up).
$P4_7$/X_{OUT}	$P4_7$ input/Clock output	I/O	
AV_{CC}, AV_{SS}	Analog power supply input	I	Connect AVss to Vss and AVcc to Vcc, respectively.
V_{REF}	Reference voltage input	I	Enter the reference voltage for AD from this pin.
$P0_1$ to $P0_7$	Input port P0	I	Input "H" or "L" level signal or open.
$P1_0$ to $P1_7$	Input port P1	I	Input "H" or "L" level signal or open.
$P3_0$ to $P3_3$	Input port P3	I	Input "H" or "L" level signal or open.
$P4_5$	Input port P4	I	Input "H" or "L" level signal or open.
$P0_0$	TxD output	O	Serial data output pin
MODE	MODE	I/O	Standard serial I/O mode 1: connect to flash programmer Standard serial I/O mode 2: Input "L".
CNV_{SS}	CNV_{SS}	I/O	Standard serial I/O mode 1: connect to flash programmer Standard serial I/O mode 2: Input "L".
$P3_7$	RxD input	I	Serial data input pin



Mode Setting

Signal	Value
CNVss	Voltage from programmer
MODE	Voltage from programmer
RxD	Voltage from programmer
$\overline{\text{RESET}}$	Vss -->Vcc

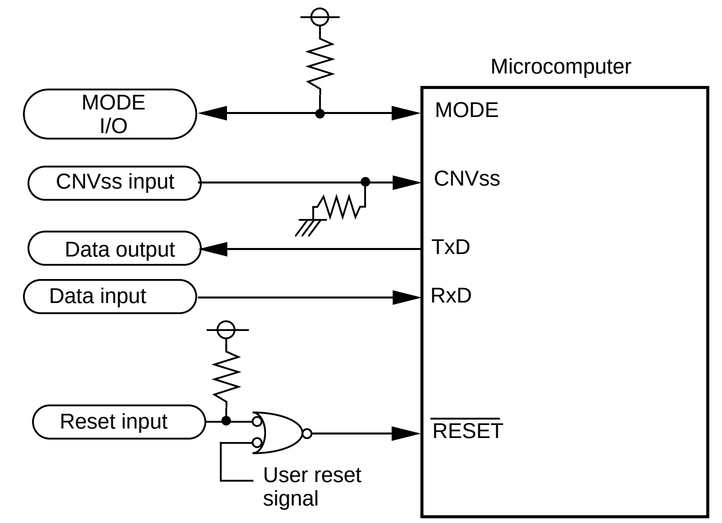
NOTES:
1. No need to connect an oscillation circuit when operating with on-chip oscillator clock.

Package: PLQP0032GB-A (32P6U-A)

Figure 17.13 Pin Connections for Standard Serial I/O Mode

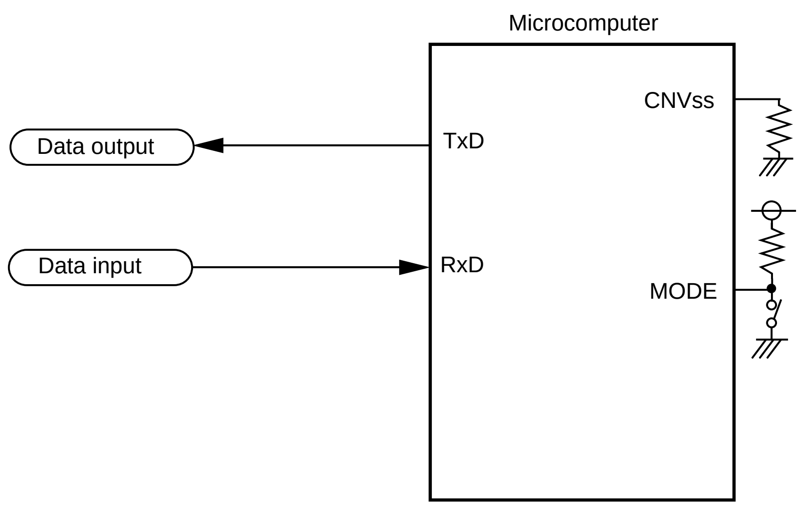
- **Example of Circuit Application in the Standard Serial I/O Mode**

Figures 17.14 and 17.15 show examples of circuit application in standard serial I/O mode 1 and mode 2, respectively. Refer to the serial programmer manual of your programmer to handle pins controlled by the programmer.



(1) Control pins and external circuitry will vary according to programmer. For more information, see the programmer manual.
(2) In this example, modes are switched between single-chip mode and standard serial I/O mode by connecting a programmer.
(3) When operating with on-chip oscillator clock, connecting the oscillation circuit is not necessary. Refer to "Appendix figure 2.1 Connecting Examples with USB Flash Writer (M3A-0665)".

Figure 17.14 Circuit Application in Standard Serial I/O Mode 1



(1) In this example, modes are switched between single-chip mode and standard serial I/O mode by controlling the MODE input with a switch.
(2) Connecting the oscillation is necessary. Set the main clock frequency 1MHz to 20 MHz. Refer to "Appendix 2.2 Connecting examples with M16C Flash Starter (M3A-0806)".

Figure 17.15 Circuit Application in Standard Serial I/O Mode 2

18. On-chip debugger

The microcomputer has functions to execute the on-chip debugger. Refer to "Appendix 2 Connecting examples for serial writer and on-chip debugging emulator". Refer to the respective on-chip debugger manual for the details of the on-chip debugger. Next, here are some explanations for the respective functions. Debugging the user system which uses these functions is not available. When using the on-chip debugger, design the system without using these functions in advance. Additionally, the on-chip debugger uses the address "$0C000_{16}$ to $0C7FF_{16}$ of the flash memory, thus avoid using for the user system.

18.1 Address match interrupt

The interrupt request is generated right before the arbitrary address instruction is executed. The debugger break function uses the address match interrupt. Refer to "10.4 Address match interrupt" for the details of the address match interrupt. Also, avoid setting the address match interrupt (the registers of AIER, RMAD0, RMAD1 and the fixed vector tables) with using the user system when using the on-chip debugger.

18.2 Single step interrupt

The interrupt request is generated every time one instruction is executed. The debugger single step function uses the single step interrupt. The other interrupt is not generated when using the single step interrupt. The single step interrupt is only for the developed support tool.

18.3 UART1

The UART1 is used for the communication with the debugger (or the personal computer). Refer to "13. Serial Interface" for the details of UART1. Also, avoid using the UART1 and the functions ($P0_0$/AN_7 and $P3_7$) which share the UART1 pins.

18.4 BRK instruction

The BRK interrupt request is generated. Refer to "10.1 Interrupt overview" and "R8C/Tiny series software manual". Also, avoid using the BRK instruction with using the user system when using the on-chip debugger.

19. Usage Notes

19.1 Stop Mode and Wait Mode

19.1.1 Stop Mode

When entering stop mode, set the CM10 bit to “1” (stop mode) after setting the FMR01 bit to “0” (CPU rewrite mode disabled). The instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit in the CM1 register to “1” (stop mode) and the program stops. Insert at least 4 NOP instructions after inserting the JMP.B instruction immediately after the instruction which sets the CM10 bit to “1”.

Use the next program to enter stop mode.

• Program of entering stop mode

```
          BCLR     1, FMR0     ; CPU rewrite mode disabled
          BSET     0, PRCR     ; Protect exited
          BSET     0, CM1      ; Stop mode
          JMP.B    LABEL_001
LABEL_001:
          NOP
          NOP
          NOP
          NOP
```

19.1.2 Wait Mode

When entering wait mode, execute the WAIT instruction after setting the FMR01 bit to “0” (CPU rewrite mode disabled). The instruction queue pre-reads 4 bytes from the WAIT instruction and the program stops. Insert at least 4 NOP instructions after the WAIT instruction.

Also, the value in the specific internal RAM area may be rewritten when exiting wait mode if writing to the interna RAM area before executing the WAIT instruction and entering wait mode. The area for a maximum of 3 bytes is rewirtten from the following address of the internal RAM in which the writing is performed before the WAIT instruction. If this causes a problem, avoid by inserting the JMP.B instruction between the writing instruction to the internal RAM area and WAIT instruction as shown in the following program example.

• Example to execute WAIT instruction

```
Program Example  MOV.B    #055h,0601h    ; Write to internal RAM area
                 •••
                 JMP.B    LABEL_001
      LABEL_001 :
                 FSET     I              ; Interrupt enabled
                 BCLR     1,FMR0         ; CPU rewrite mode disabled
                 WAIT                    ; Wait mode
                 NOP
                 NOP
                 NOP
                 NOP
```

When accessing any area other than the internal RAM area between the writing instruction to the internal RAM area and execution of the WAIT instruction, this situation will not occur.

19.2 Interrupt

19.2.1 Reading Address 00000_{16}

Do not read the address 00000_{16} by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000_{16} in the interrupt sequence. At this time, the acknowledged interrupt IR bit is set to “0”.

If the address 00000_{16} is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to “0”. This may cause a problem that the interrupt is canceled, or an unexpected interrupt is generated.

19.2.2 SP Setting

Set any value in the SP before an interrupt is acknowledged. The SP is set to “0000_{16}” after reset. Therefore, if an interrupt is acknowledged before setting any value in the SP, the program may run out of control.

19.2.3 External Interrupt and Key Input Interrupt

Either an “L” level or an ”H” level of at least 250ns width is necessary for the signal input to the $\overline{INT_0}$ to $\overline{INT_3}$ pins and $\overline{KI_0}$ to $\overline{KI_3}$ pins regardless of the CPU clock.

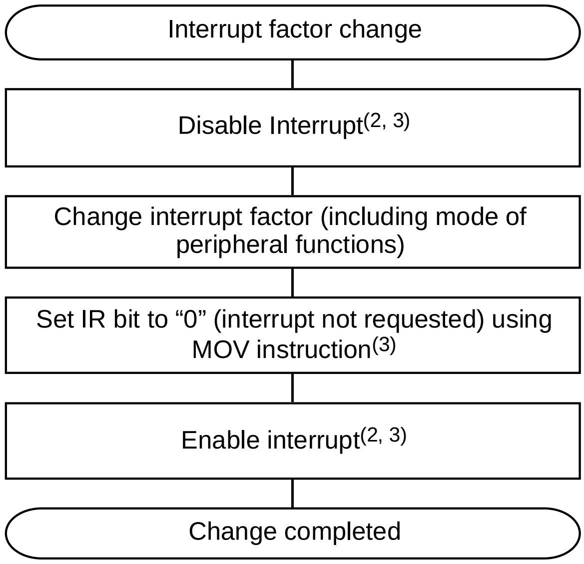
19.2.4 Watchdog Timer Interrupt

Reset the watchdog timer after a watchdog timer interrupt is generated.

19.2.5 Changing Interrupt Factor

The IR bit in the interrupt control register may be set to “1” (interrupt requested) when the interrupt factor is changed. When using an interrupt, set the IR bit to “0” (interrupt not request) after changing the interrupt factor. In addition, the changes of interrupt factors include all elements that change the interrupt factors assigned to individual software interrupt numbers, polarities, and timing. Therefore, when a mode change of the peripheral functions involves interrupt factors, edge polarities, and timing, set the IR bit to “0” (interrupt not requested) after the change. Refer to each peripheral function for the interrupts caused by the peripheral functions.

Figure 19.1 shows an Example of Procedure for Changing Interrupt Factor.



• IR bit: The interrupt control register bit of an interrupt whose factor is changed

NOTES:
1. Execute the above setting individually. Do not execute two or more settings at once (by one instruction).
2. Use the I flag for the $\overline{\text{INTi}}$ (i=0 to 3) interrupt. To prevent interrupt requests from being generated when using peripheral function interrupts other than the $\overline{\text{INTi}}$ interrupt factor. In this case, use the I flag when all maskable interrupts can be disabled. When all maskable interrupts cannot be disabled, use the ILVL0 to ILVL2 bits of the interrupt whose factor is changed.
3. Refer to “19.2.6 Changing Interrupt Control Register” for the instructions to be used and their usage notes.

Figure 19.1 Example of Procedure for Changing Interrupt Factor

19.2.6 Changing Interrupt Control Register

(1) Each interrupt control register can only be changed while interrupt requests corresponding to that register are not generated. If interrupt requests may be generated, disable the interrupts before changing the interrupt control register.

(2) When changing any interrupt control register after disabling interrupts, be careful with the instruction to be used.

When Changing Any Bit Other Than IR Bit

If an interrupt request corresponding to that register is generated while executing the instruction, the IR bit may not be set to “1” (interrupt requested), and the interrupt request may be ignored. If this causes a problem, use the following instructions to change the register.

Instructions to use: AND, OR, BCLR, BSET

When Changing IR Bit

If the IR bit is set to “0” (interrupt not requested), it may not be set to “0” depending on the instruction used. Use the MOV instruction to set the IR bit to “0”.

(3) When disabling interrupts using the I flag, set the I flag according to the following sample programs. Refer to (2) for the change of interrupt control registers in the sample programs.

Sample programs 1 to 3 are preventing the I flag from being set to “1” (interrupt enabled) before writing to the interrupt control registers for reasons of the internal bus or the instruction queue buffer.

Example 1: Use NOP instructions to prevent I flag being set to “1” before interrupt control register is changed

```
INT_SWITCH1:
      FCLR    I              ; Disable interrupts
      AND.B   #00H, 0056H    ; Set TXIC register to “0016”
      NOP
      NOP
      FSET    I              ; Enable interrupts
```

Example 2: Use dummy read to have FSET instruction wait

```
INT_SWITCH2:
      FCLR    I              ; Disable interrupts
      AND.B   #00H, 0056H    ; Set TXIC register to “0016”
      MOV.W   MEM, R0        ; Dummy read
      FSET    I              ; Enable interrupts
```

Example 3: Use POPC instruction to change I flag

```
INT_SWITCH3:
      PUSHC   FLG
      FCLR    I              ; Disable interrupts
      AND.B   #00H, 0056H    ; Set TXIC register to “0016”
      POPC    FLG            ; Enable interrupts
```

19.3 Clock Generation Circuit

19.3.1 Oscillation Stop Detection Function

Since the oscillation stop detection function cannot be used if the main clock frequency is below 2MHz, set the OCD1 to OCD0 bits to "00_2" (oscillation stop detection function disabled).

19.3.2 Oscillation Circuit Constants

Ask the maker of the oscillator to specify the best oscillation circuit constants on your system.

19.4 Timers

19.4.1 Timers X, Y and Z

(1) Timers X, Y and Z stop counting after reset. Therefore, a value must be set to these timers and prescalers before starting counting.

(2) Even if the prescalers and timers are read out simultaneously in 16-bit units, these registers are read byte-by-byte in the microcomputer. Consequently, the timer value may be updated during the period these two registers are being read.

19.4.2 Timer X

(1) Do not rewrite the TXMOD0 to TXMOD1 bits, the TXMOD2 bit and TXS bit simultaneously.

(2) In pulse period measurement mode, the TXEDG bit and TXUND bit in the TXMR register can be set to “0” by writing “0” to these bits in a program. However, these bits remain unchanged when “1” is written. To set one flag to “0” in a program, write "1" to the other flag by using the MOV instruction. (This prevents any unintended changes of flag.)

Example (when setting TXEDG bit to “0”):

```
MOV.B     #10XXXXXXB,008BH
```

(3) When changing to pulse period measurement mode from other mode, the contents of the TXEDG bit and TXUND bit are indeterminate. Write "0" to the TXEDG bit and TXUND bit before starting counting.

(4) The prescaler X underflow which is generated for the first time after the count start may cause that the TXEDG bit is set to “1”. When using the pulse period measurement mode, leave more than two periods of the prescaler X right after count starts and set the TXEDG bit to “0”.

19.4.3 Timer Y

(1) Do not rewrite the TYMOD0 and TYS bits simultaneously.

19.4.4 Timer Z

(1) Do not rewrite the TZMOD0 to TZMOD1 bits and the TZS bit simultaneously.

(2) In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TZS bit in the TC register to “0” (stops counting) or setting the TZOS bit in the TZOC register to “0” (stops one-shot), the timer reloads the value of reload register and stops. Therefore, the timer count value should be read out in programmable one-shot generation mode and programmable wait one-shot generation mode before the timer stops.

19.4.5 Timer C

(1) Access the TC, TM0 and TM1 registers in 16-bit units.
This prevents the timer value from being updated between the low-order byte and high-order byte are being read.

Example (when Timer C is read):

```
MOV.W     0090H,R0     ; Read out timer C
```

19.5 Serial Interface

(1) When reading data from the UiRB (i=0,1) register even in the clock asynchronous serial I/O mode or in the clock synchronous serial I/O mode. Be sure to read data in 16-bit unit. When the high-byte of the UiRB register is read, the PER and FER bits of the UiRB register and the RI bit of the UiC1 register are set to "0".

Example (when reading receive buffer register):

```
MOV.W    00A6H, R0        ; Read the U0RB register
```

(2) When writing data to the UiTB register in the clock asynchronous serial I/O mode with 9-bit transfer data length, data should be written high-byte first then low-byte in 8-bit unit.

Example (when reading transmit buffer register):

```
MOV.B    #XXH, 00A3H      ; Write the high-byte of U0TB register
MOV.B    #XXH, 00A2H      ; Write the low-byte of U0TB register
```

19.6 A/D Converter

(1) When writing to each bit but except bit 6 in the ADCON0 register, each bit in the ADCON1 register, or the SMP bit in the ADCON2 register, A/D conversion must be stopped (before a trigger occurs).
When the VCUT bit in the ADCON1 register is changed from “0” (VREF not connected) to “1” (VREF connected), wait at least 1 µs before starting A/D conversion.

(2) When changing AD operation mode, select an analog input pin again.

(3) In one-shot mode, A/D conversion must be completed before reading the AD register. The IR bit in the ADIC register or the ADST bit in the ADCON0 register can indicates whether the A/D conversion is completed or not.

(4) In repeat mode, the undivided main clock must be used for the CPU clock.

(5) If A/D conversion is forcibly terminated while in progress by setting the ADST bit in the ADCON0 register to “0” (A/D conversion halted), the conversion result of the A/D converter is indeterminate. If the ADST bit is set to “0” in a program, ignore the value of AD register.

(6) A 0.1 µF capacitor should be connected between the AVcc/VREF pin and AVss pin.

19.7 Flash Memory Version

19.7.1 CPU Rewrite Mode

● Operation Speed

Before entering CPU rewrite mode (EW0 mode), select 5MHz or below for the CPU clock using the CM06 bit in the CM0 register and the CM16 to CM17 bits in the CM1 register. This usage note is not needed for EW1 mode.

● Instructions Diabled Against Use

The following instructions cannot be used in EW0 mode because the flash memory internal data is referenced: UND, INTO and BRK instructions.

● How to Access

Write “0” to the corresponding bits before writing “1” when setting the FMR01, FMR02, and FMR11 bits to ”1”. Do not generate an interrupt between writing “0” and “1”.

● Rewriting User ROM Area

In EW0 mode, if the power supply voltage drops while rewriting any block in which the rewrite control program is stored, the flash memory may not be able to be rewritten because the rewrite control program cannot be rewritten correctly. In this case, use stnadard serial I/O mode.

● Reset Flash Memory

Since the CPU stops and cannot return when setting the FMSTP bit in the FMR0 register to “1” (flash memory stops) during erase suspend in EW1 mode, do not set the FMSTP bit to “1”.

● Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.

● Interrupt

Table 19.1 list the Interrupt in EW0 Mode and Table 19.2 lists the Interrupt in EW1 Mode.

Table 19.1 Interrupt in EW0 Mode

<table>
<tr><th>Mode</th><th>Status</th><th>When maskable interrupt request is acknowledged</th><th>When watchdog timer, oscillation stop detection, and voltage detection interrupt request are acknowledged</th></tr>
<tr><td rowspan="2">EW0</td><td>During automatic erasing</td><td rowspan="2">Any interrupt can be used by allocating a vector to RAM</td><td rowspan="2">Once an interrupt request is acknowledged, the auto-programming or auto-erasing is forcibly stoped and resets the flash memory. An interrupt process starts after the fixed period and the flash memory restarts. Since the block during the auto-erasing or the address during the auto-programming is forcibly stopped, the normal value may not be read. Execute the auto-erasing again and ensure the auto-erasing is completed normally.
Since the watchdog timer does not stop during the command operation, the interrupt request may be generated. Reset the watchdogi timer regularly.</td></tr>
<tr><td>Automatic writing</td></tr>
</table>

NOTES:

1. Do not use the address match interrupt while the command is executed because the vector of the address match interrupt is allocated on ROM.
2. Do not use the non-maskable interrupt while Block 0 is automatically erased because the fixed bector is allocated Block 0.

Table 19.2 Interrupt in EW1 Mode

Mode	Status	When maskable interrupt request is acknowledged	When watchdog timer, oscillation stop detection and voltage detection interrupt request area acknowledged
EW1	During automatic erasing (erase-suspend function is enabled)	The auto-erasing is suspended and the interrupt process is executed. The auto-erasing can be restarted by setting the FMR41 bit in the FMR4 register to "0" (erase restart) after the interrupt process completes	Once an interrupt request is acknowledged, the auto-programming or auto-erasing is forcibly stopped and resets the flash memory. An interrupt process starts after the fixed period and the flash memory restarts. Since the block during the auto-erasing or the address during the auto-programming is forcibly stopped, the normal value may not be read. Execute the auto-erasing again and ensure the auto-erasing is competed normally. Since the watchdog timer does not stop during the command operation, the interrupt request may be generated. Reset the watchdog timer regularly using the erase-suspend function.
	During automatic erasing (erase-suspend function is disabled)	The auto-erasing has a priority and the interrupt request acknowledgement is waited. The interrupt process is executed after the auto-erasing completes	
	Auto programming	The auto-programming has a priority and the interrupt request acknowledgement is waited. The interrupt process is executed after the auto-programming completes	

NOTES:

1. Do not use the address match interrupt while the command is executed because the vector of the address match interrupt is allocated on ROM.
2. Do not use the non-maskable interrupt while Block 0 is automatically erased because the fixed bector is allocated Block 0.

19.8 Noise

(1) Bypass Capacitor between VCC and VSS Pins

Insert a bypass capacitor (at least 0.1 µF) between VCC and VSS pins as the countermeasures against noise and latch-up. The connecting wires must be the shortest and widest possible.

(2) Port Control Registers Data Read Error

During severe noise testing, mainly power supply system noise, and introduction of external noise, the data of port related registers may changed. As a firmware countermeasure, it is recommended to periodically reset the port registers, port direction registers and pull-up control registers. However, you should fully examine before introducing the reset routine as conflicts may be created between this reset routine and interrupt routines (i. e. ports are switched during interrupts).

(3) CNVss Pin Wiring

In order to improve the pin tolerance to noise, insert a pull down resistance (about 5 kΩ) between CNVss and Vss, and placed as close as possible to the CNVss pin.

20. Usage notes for on-chip debugger

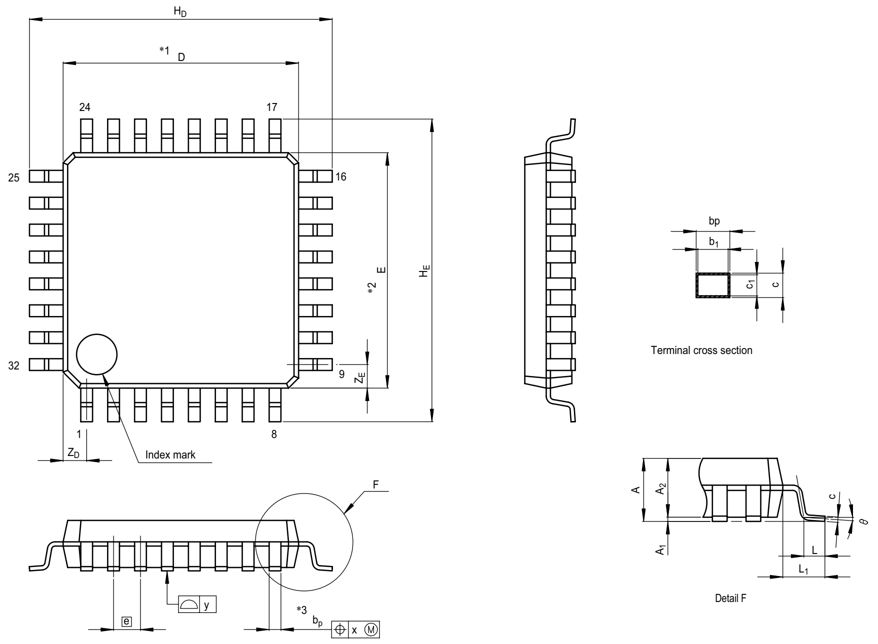
When using the on-chip debugger to develop the R8C/12 group program and debug, pay the following attention.

(1) Do not use $P0_0/AN_7/TxD_{11}$ pin and $P3_7/TxD_{10}/RxD_1$ pin.
(2) When write in the PD3 register ($00E7_{16}$ address), set bit 7 to "0".
(3) Do not access the related serial interface 1 register.
(4) Do not use from $OC000_{16}$ address to $OC7FF_{16}$ address because the on-chip debugger uses these addresses.
(5) Do not set the address match interrupt (the registers of AIER, RMAD0, RMAD1 and the fixed vector tables) in a user system.
(6) Do not use the BRK instruction in a user system.
(7) Do not set the b5 to “0” by a user program since the on-chip debugger uses after setting the b5 in the FMR0 register to “1”
(8) The stack pointer with up to 8 bytes is used during the user program break. Therefore, save space of 8 bytes for the stack area.

Connecting and using the on-chip debugger has some peculiar restrictions. Refer to each on-chip debugger manual for on-chip debugger details.

Appendix 1. Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP32-7x7-0.80	PLQP0032GB-A	32P6U-A	0.2g

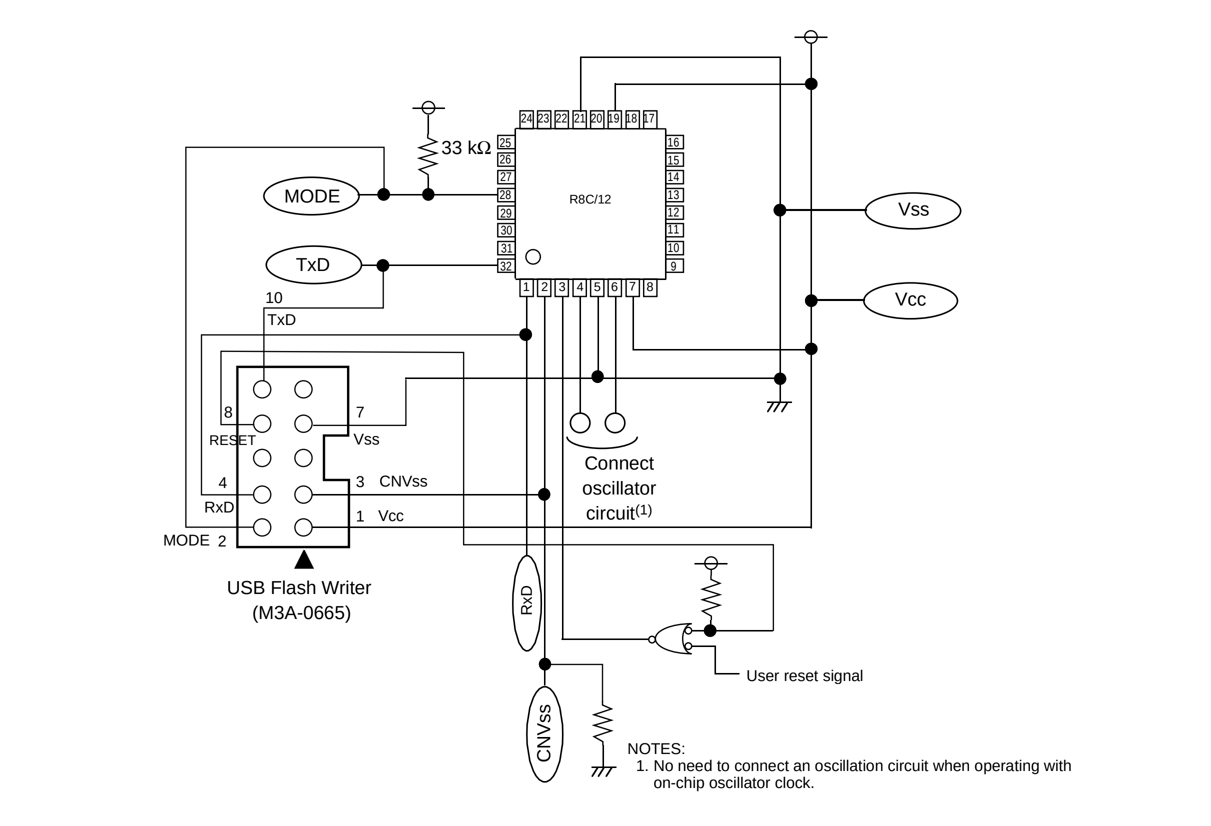


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

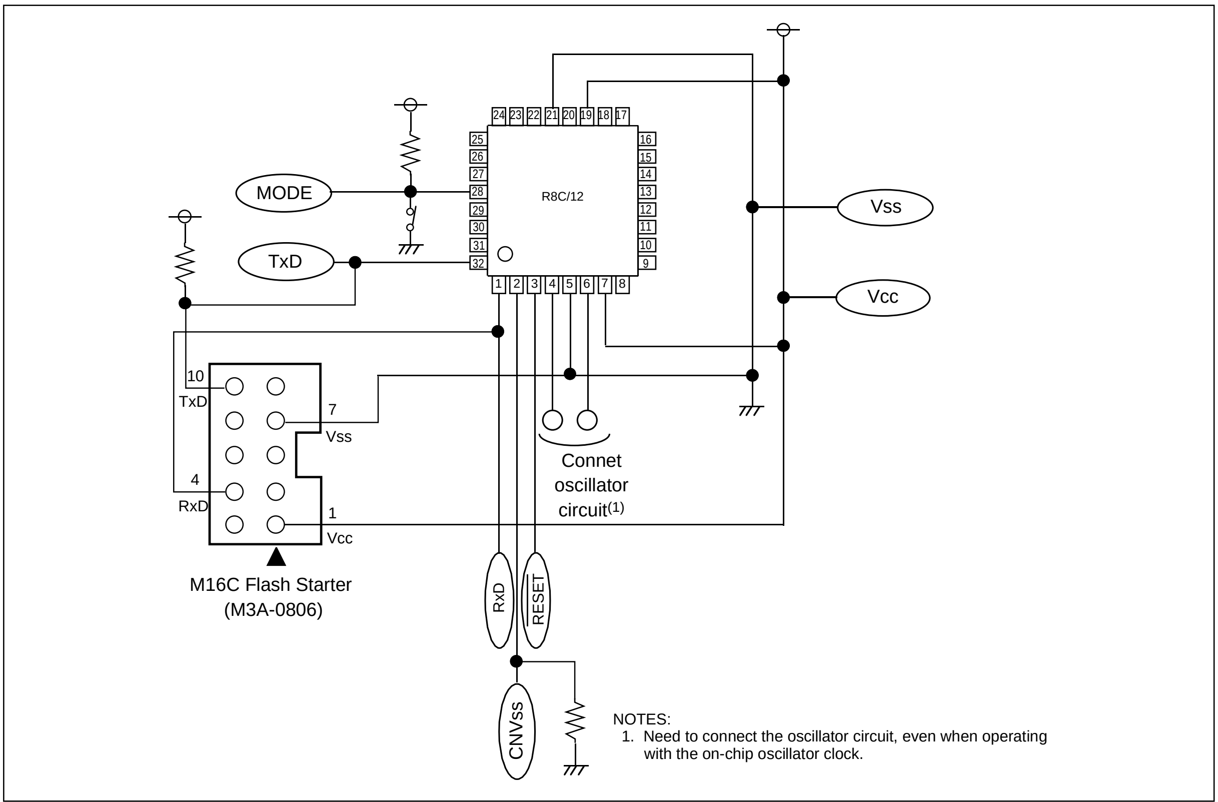
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	0.7	—
Z_E	—	0.7	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Appendix 2. Connecting examples for serial writer and on-chip debugging emulator

Appendix figure. 2.1 shows connecting examples with USB Flash Writer and appendix figure 2.2 shows connecting examples with M16C Flash Starter.

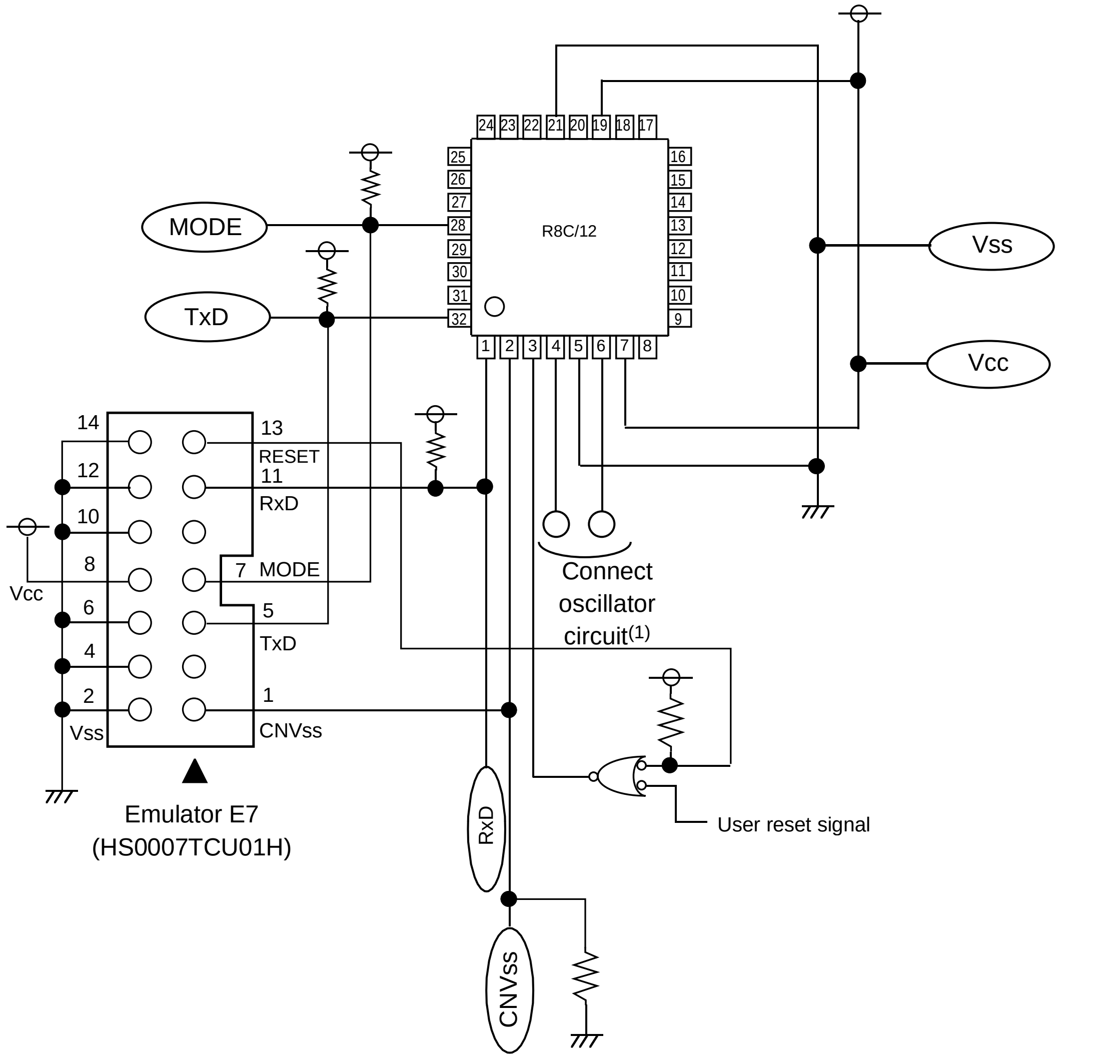


Appendix figure 2.1 Connecting examples with USB Flash Writer (M3A-0665)



Appendix figure 2.2 Connecting examples with M16C Flash Starter (M3A-0806)

Appendix figure 2.3 shows connecting examples with emulator E7.

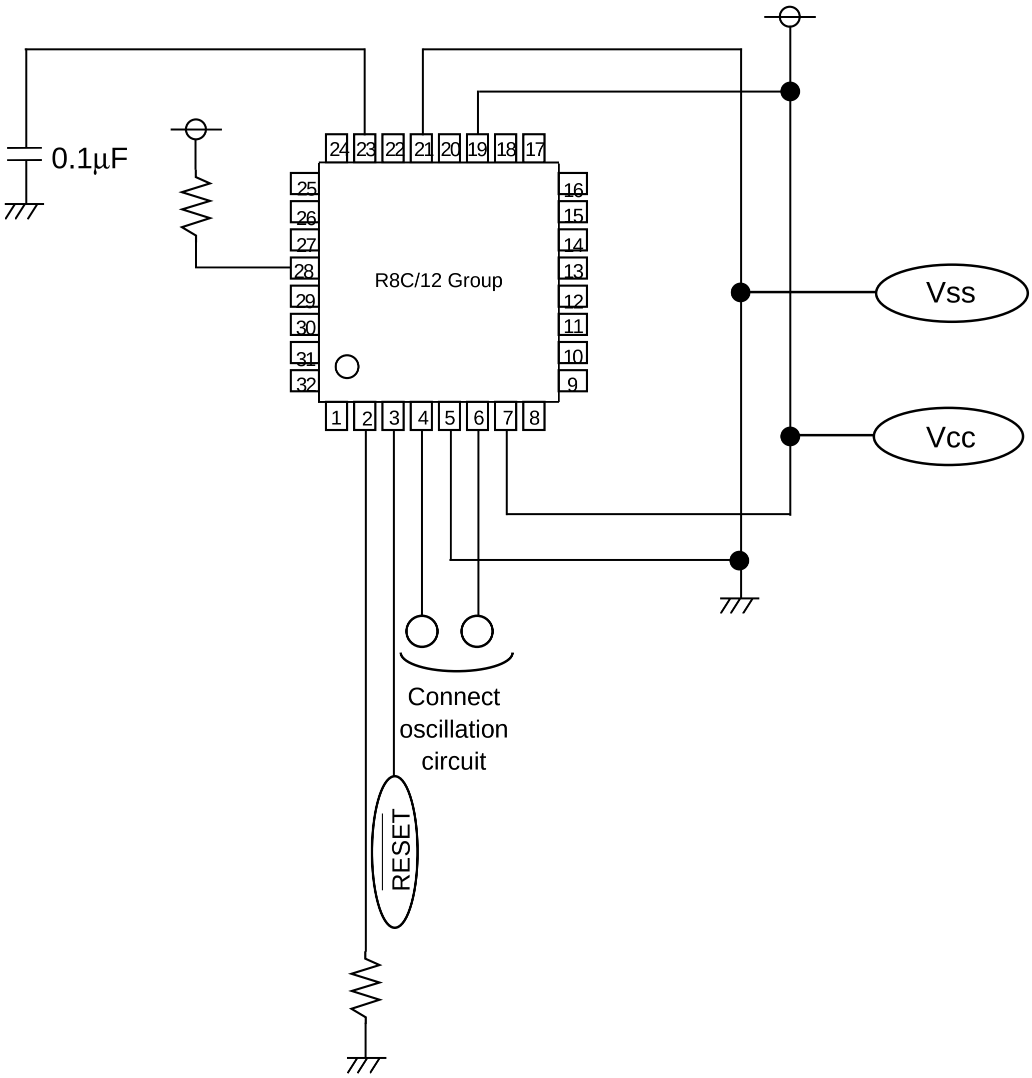


NOTES:
1. No need to connect an oscillation circuit when operating with on-chip oscillator clock.

Appendix figure 2.3 Connecting examples with emulator E7 (HS0007TCU01H)

Appendix 3. Example of Oscillation Evaluation Circuit

Appendix Figure 3.1 shows the Example of Oscillation Evaluation Circuit.



NOTES:
1. Set a program before evaluating.

Appendix figure 3.1 Example of Oscillation Evaluation Circuit

Register Index

REVISION HISTORY	R8C/12 Group Hardware Manual

Rev.	Date	Description	
		Page	Summary
0.10	Nov 05, 2003	–	First edition issued
1.00	Sep 10, 2004	all pages	Words standardized (on-chip oscillator, serial interface, A/D)
		2	Table 1.1 revised
		5	Figure 1.3, NOTES 3 added
		6	Table 1.3 revised
		9	Figure 3.1, NOTES added
		10-13	One body sentence in chapter 4 added ; Titles of Table4.1 to 4.4 added Table 4.3 revised ; Table 4.4 revised
		19	Figure 6.2 revised (CM0 and CM1)
		25	Table 6.3, Timer Z and Timer C interrupt added
		26	6.4.3 Stop Mode, in “Pin Status in Stop Mode”, one sentence added
		29	One sentence in 6.5.1 moves to Chapter 19
		47	One body sentence in 10.2.1 added
		49	One body sentence in 10.2.3 added
		50	One body sentence in 10.2.4 added
		51	Figure 10.15 revised
		54	Figure 11.1 revised
		57	Line 4 in 12.1 revised
		60	Table 12.3 revised
		61	Table 12.4 revised
		62	Figure 12.7 revised
		64	Table 12.6 revised ; Figure 12.9 revised
		69	Table 12.7 revised
		71	Table 12.8 revised, NOTES revised
		72	Figure 12.16 revised
		74	5 line in 12.3 revised ; Figure 12.18 revised
		77	Table 12.9 revised
		79	Table 12.10 revised, NOTES revised
		81	Table 12.11 revised, NOTES revised
		83	Figure 12.25 revised
		84	Table 12.12 revised, NOTES revised
		86	Figure 12.27 revised
		87	Table 12.13 revised
		88	Figure 12.29 revised
		89	Figure 12.30 revised
		91	Figure 13.2 revised
		99	13.1.3 revised
		103	Figure 13.10 revised
		112	Figure numbers in 15.1.1, 15.1.2, 15.1.3 and 15.1.4 revised
		119	Table 15.1 revised
		120	Table 16.2 revised
		121	Table 16.3 revised
		122	Table 16.4 and 16.5 revised
		123	Table 16.7 revised
		124	Table 16.8 revised
		125	Table 16.13 revised
		127	Table 16.14 revised
		128	Table 16.15 revised

Rev.	Date	Description: Page	Description: Summary
1.00	Sep 10, 2004	129	Table 16.17 revised
		131	Table 17.1 “Number of program and erasure” revised (1,000 times)
		135	Line 2 and 8 in 17.4.2 revised
		136	Figure number in FMSTP bit revised ; FMR46 bit revised
		137	Figure 17.3 revised
		138	Figure 17.4 revised (FMR4)
		140	Figure 17.7 revised ; Figure title revised
		141	Table 17.4 revised
		143	Figure 17.9 revised
		144	Figure 17.10 revised
		146	Table 17.6 revised
		153-164	Compositions in Chapter 19 modified ; 19.3 added ; 19.4.5 revised ; 19.7 revised
		165	(7) in Chapter 20 added
		169	Appendix 3 added
		170-171	Page numbers in Register Index revised
1.10	Apr.27.2005	4	Table 1.2, Figure 1.2 package name revised
		5	Figure 1.3 package name revised
		10	Table 4.1 revised
		12	Table 4.3 revised
		14	5.1 partly revised
		15	Figure 5.2 partly revised
		17	Table 6.1 partly added
		19	Figure 6.2 partly revised
		21	6.1 partly revised
		23	6.3.1 partly deleted
		24	6.4.1 partly revised
		27	Figure 6.5 revised
		28	Figure 6.6 deleted
		54	Figure 11.2 partly revised
		63	Figure 12.9 partly revised
		80	Table 12.11 partly revised
		83	Table 12.12 partly revised
		87	Figure 12.29 partly revised
		100	Table 13.6 partly revised
		103	13.2.3 Bit Rate added
		111	Figure 14.6 partly revised
			14.4 added
		112	14.5 added
		113	14.6 added
		115	Figure 15.1 revised
		116	Figure 15.2 revised
		117	Figure 15.3 revised
		121-126	15.2 added
		127	Table15.24 partly revised
			Figure 15.9 added
		129	Table 16.3 partly revised
		130	Table 16.4, Table 16.5 partly added
		131	Table 16.6, Table 16.7 partly revised
		135	Table 16.14 partly revised
		140	Figure 17.1 revised

Rev.	Date	Description	
		Page	Summary
1.10	Apr.27.2005	142	Table 17.3 partly added
		147	Figure 17.5 added
		150	•Program partly revised
		152	Figure 17.11 partly added
		158	Figure 17.13 package name revised
		160	18.1 partly revised
		165	19.3.2 added
		166	19.4.4 partly revised
		168	19.6 partly revised
		169	19.7.1 partly added
		173	20 partly revised
		174	Package Dimensions revised
1.20	Jan.27.2006	2	Table 1.1 Performance outline revised
		3	Figure 1.1 Block diagram partly revised
		4	1.4 Product Information, title of Table 1.2 “Product List” → “Product Informaton” revised ROM capacity; “Program area” → “Program ROM”, “Data area” → “Data flash” revised Figure 1.2 Type No., Memory Size, and Package partly revised
		6	Table 1.3 Pin description revised
		7-8	2 Central Processing Unit (CPU) revised Figure 2.1 CPU register revised
		9	3 Memory, Figure 3.1 Memory Map; “Program area” → “Program ROM”, “Data area” → “Data flash” revised
		10	Table 4.1 SFR Information(1) NOTES:1 revised
		11	Table 4.2 SFR Information(2) NOTES:1 revised
		12	Table 4.3 SFR Information(3); 0081_{16}: “Prescaler Y” → “Prescaler Y Register” 0082_{16}: “Timer Y Secondary” → “Timer Y Secondary Register” 0083_{16}: “Timer Y Primary” → “Timer Y Primary Register” 0085_{16}: “Prescaler Z” → “Prescaler Z Register” 0086_{16}: “Timer Z Secondary” → “Timer Z Secondary Register” 0087_{16}: “Timer Z Primary” → “Timer Z Primary Register” $008C_{16}$: “Prescaler X” → “Prescaler X Register” revised NOTES:1 revised
		13	Table 4.4 SFR Information(4) NOTES:1 revised
		15	Figure 5.2 Reset Sequence; “72cycles” → “64cycles” revised
		17	6 Clock Generation Circuit; “(oscillation stop detect function)” → “(oscillation stop detection function)” revised Table 6.1 Clock Generation Circuit Specifications NOTES: 2 deleted
		20	Figure 6.3 OCD Register NOTES: 3 partly deleted
		22	6.2 On-Chip Oscillator Clock; “The application products ... to accommodate the frequency range.” → “The application products ... for the frequency change.” revised
		24	Table 6.2 Setting Clock Related Bit and Modes CM13 added
		28	6.5.1 How to Use Oscillation Stop Detection Function: “This function cannot ... is below 2 MHz.” added
		32	Table 9.1 Bus Cycles for Access Space, Table 9.2 Access Unit and Bus Operation; “SFR” → “SFR, Data flash”, ROM/RAM” → “Program ROM/RAM” revised
		37	Table 10.2 Relocatable Vector Tables; “A/D” → “A/D Conversion” revised

Rev.	Date	Description	
		Page	Summary
1.20	Jan.27.2006	45	Figure 10.9 Interrupts Priority Select Circuit NOTES: 1 deleted
		56	Figure 12.1 Timer X Block Diagram; “Peripheral data bus” → “Data bus” revised
		73	Figure 12.18 Timer Z Block Diagram; “Peripheral data bus” → “Data bus” revised
		91	Figure 13.3 U0TB to U1TB Registers, U0RB and U1RB Registers, and U0BRG and U1BRG Registers; UARTi transmit buffer register (i=0, 1) revised UARTi bit rate register (i=0, 1); NOTES: 3 added
		92	Figure 13.4 U0MR to U1MR Registers and U0C0 and U1C0 Registers; UARTi transmit/receive control register 0 (i=0, 1); NOTES: 1 added
		93	Figure 13.5 U0C1 and U1C1 Registers and UCON Register; UART transmit/receive control register 2; NOTES: 2 added
		100	Table 13.5 Registers to Be Used and Settings in UART Mode; UiBRG: “–” → “0 to 7” revised
		105	Figure 14.1 A/D Converter Block Diagram “Vref” → “Vcom” revised
		114	14.7 Output Impedance of Sensor under A/D Conversion added
		117	Figure 15.1 Programmable I/O Ports (1); NOTES: 1 added
		118	Figure 15.2 Programmable I/O Ports (2); NOTES: 1 added
		119	Figure 15.3 Programmable I/O Ports (3); NOTES: 1 added
		120	Figure 15.4 Programmable I/O Ports (4); NOTES: 3 added
		128	Table 15.20 Port $P3_3$/$\overline{INT_3}$/TC_{IN} Setting; Bit: “PD3_1” → “PD3_3” Table 15.22 Port $P4_5$/$\overline{INT_0}$ Setting; Bit: “PD3_3” → “PD4_5” Table 15.23 Port X_{IN}/$P4_6$, X_{OUT}/$P4_7$ Setting; Setting value: External input to X_{IN} pin, “H” output from X_{OUT} pin; CM1: “1” → “0”, CM0: “0” → “1”, Feedback resistance: “OFF” → “ON”
		130	Table 16.2 Recommended Operating Conditions; NOTES: 1, 2, 3 revised
		131	Table 16.3 A/D Conversion Characteristics; “A/D operation clock frequency” → “A/D operating clock frequency” revised NOTES: 1, 2, 3, 4 revised
		132	Table 16.4 Flash Memory (Program ROM) Electrical Characteristics; “Data retention duration” → “Data hold time” revised “Topr” → “Ambient temperature” NOTES: 1 to 7 added Measuring condition of byte program time and block erase time deleted
		133	Table 16.5 Flash Memory (Data flash Block A, Block B) Electrical characteristics “Data retention duration” → “Data hold time” revised “Topr” → “Ambient temperature” NOTES: 1, 3 revised, NOTES: 9 added Measuring condition of byte program time and block erase time deleted
		134	Table 16.7 Electrical Characteristics (1) [V_{CC}=5V]; “$P1_0$ to $P1_7$ Except X_{OUT}” → “Except $P1_0$ to $P1_7$, X_{OUT}” revised Table 16.8 Electrical Characteristics (2) [V_{CC}=5V] NOTES: 1, 2 revised Measuring condition Stop mode: “Topr= 25°C” added
		137	Table 16.14 Electrical Characteristics (3) [V_{CC}=3V] “$P1_0$ to $P1_7$ Except X_{OUT}” → “Except $P1_0$ to $P1_7$, X_{OUT}” revised
		138	Table 16.15 Electrical Characteristics (4) [V_{CC}=3V] NOTES: 1, 2 revised Measuring condition Stop mode: “Topr= 25°C” added
		142	17.2 Memory Map; “The user ROM ... Block B, in...area which ...” → “The user ROM ... Block B (data flash), in...area (program ROM) which ...” revised

Rev.	Date	Description	
		Page	Summary
1.20	Jan.27.2006		Figure 17.1 Flash Memory Block Diagram revised
		147	Figure 17.3 FMR0 Register; NOTES: 7 added
		148	Figure 17.4 FMR1 and FMR4; Flash memory control register 4 NOTES: 2 “Other than this period, this bit is set to “0 ”.” revised
		154	Figure 17.11 Block Erase Command (When Using Erase-suspend Function); “Write ‘$D0_{16}$’ to the uppermost block address” → “Write ‘$D0_{16}$’ to the any block address” revised
		157	Figure 17.12 Full Status Check and Handling Procedure for Each Error revised
		159	Table 17.7 Pin Functions (Flash Memory Standard Serial I/O Mode); $\overline{\text{RESET}}$: revised
		163	19.1.1 Stop Mode “Use the next program to enter stop mode.” added “• Example of entering stop mode” → “• Program of entering stop mode” “Program Example” deleted
		167	19.3.1 Oscillation Stop Detection Function “Since the oscillation stop ... is 2 MHz or below, ...” → “Since the oscillation stop ... is below 2 MHz, ...” revised
		177	Appendix figure 2.2 Connecting examples with M16C Flash Starter (M3A-0806); NOTES: 1 revised Pulled up added

RENESAS 16-BIT SINGLE-CHIP MICROCOMPUTER
HARDWARE MANUAL
R8C/12 Group

Publication Data : Rev.0.10 Nov 05, 2003
Rev.1.20 Jan 27, 2006
Published by : Sales Strategic Planning Div.
Renesas Technology Corp.

R8C/12 Group
Hardware Manual

Renesas Electronics Corporation
1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan

REJ09B0110-0120