User's Manual

R-IN32M3 Series

User's Manual

R-IN32M3-CL

UPD60510BF1-HN4-A

UPD60510BF1-HN4-M1-A

arm

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Purpose and Target Readers

This manual is intended for users who wish to understand the functions of industrial Ethernet network ASSP (application specific standard product) "R-IN32M3-CL" (UPD60510BF1-HN4-A, UPD60510BF1-HN4-M1-A) for designing application of it.
It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

Literature — Literature may be preliminary versions. Note, however, that the following descriptions do not indicate "Preliminary". Some documents on cores were created when they were planned or still under development. So, they may be directed to specific customers. Last four digits of document number (described as ****) indicate version information of each document. Please download the latest document from our web site and refer to it.

The document related to R-IN32M3-CL

Document Name	Document Number
R-IN32M3 Series Datasheet	R18DS0008EJ****
R-IN32M3-EC User's Manual	R18UZ0003EJ****
R-IN32M3 Series User's Manual (Peripheral Modules)	R18UZ0007EJ****
R-IN32M3 Series Programming Manual (OS edition)	R18UZ0011EJ****
R-IN32M3 Series Programming Manual (Driver edition)	R18UZ0009EJ****
R-IN32M3 Series User's Manual (Board design edition)	R18UZ0021EJ****
R-IN32M3-CL User's Manual	This manual

2. Notation of Numbers and Symbols

Weight in data notation: Left is high-order column, right is low-order column

Active low notation:

xxxZ (capital letter Z after pin name or signal name)

or xxx_N (capital letter _N after pin name or signal name)

or xxnx (pin name or signal name contains small letter n)

Note:

Explanation of (Note) in the text

Caution:

Item deserving extra attention

Remark:

Supplementary explanation to the text

Numeric notation:

Binary ⋯ xxxx , xxxxB or n'bxxxx (n bits)

Decimal ⋯ xxxx

Hexadecimal ⋯ xxxxH or n'hxxxx (n bits)

Prefixes representing powers of 2 (address space, memory capacity):

K (kilo)⋯ $2^{10} = 1024$

M (mega)⋯ $2^{20} = 1024^2$

G (giga)⋯ $2^{30} = 1024^3$

Data Type:

Word ⋯ 32 bits

Halfword ⋯ 16 bits

Byte ⋯ 8 bits

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1. Overview

1.1 Introduction

Ethernet communication continues to spread rapidly in the field of industrial automation as manufacturers seek to improve the capability, efficiency, and flexibility of their organizations. Modern industrial Ethernet applications require high-speed real-time response, low power consumption, and high performance. These requirements are not necessarily met by traditional methods such as hard-wired Ethernet processors or dedicated high-speed CPUs.

Renesas R-IN32M3-CL of large-scale integrated circuits (LSI) are specifically tailored to meet the demands of industrial Ethernet applications. Key features include:

- Integrated Arm® Cortex®-M3 core for flexibility
- Integrated real-time OS accelerator with support for µITRON version 4.0
- Integrated Gigabit Ethernet MAC
- Dedicated DMA controller and buffer for the network processor
- Timers, multiple serial interfaces, general purpose I/O (GPIO), external memory interfaces
- High-speed, real-time, deterministic, low-latency, low-jitter response for real-time applications
- High performance with low CPU usage by offloading functions to real-time OS accelerator
- Low power consumption

1.2 Overview

Table 1.1 Overview of R-IN32M3-CL

(1/2)

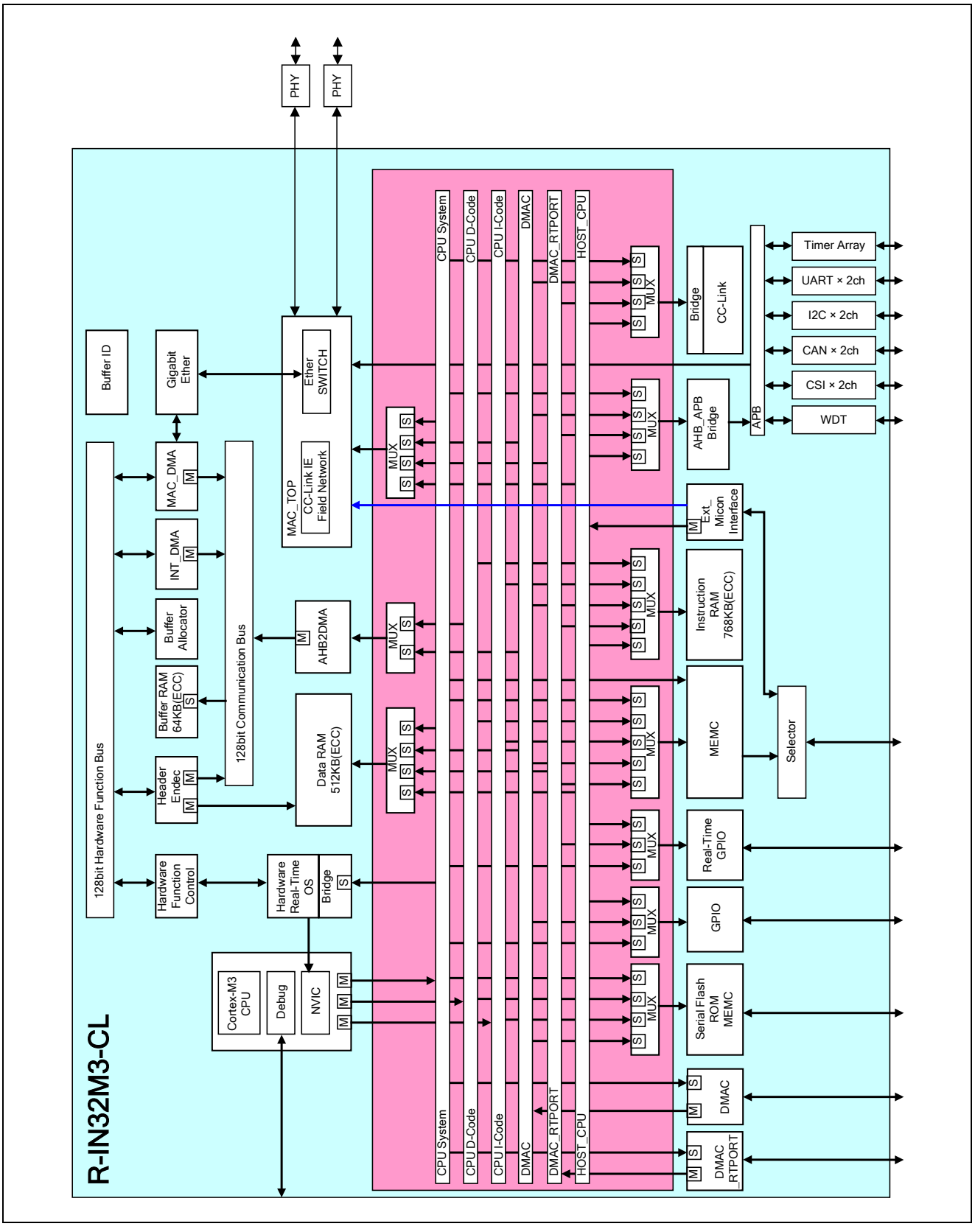
Item \ Product	R-IN32M3-CL
CPU cores	Arm Cortex-M3 32-bit RISC CPU + Real-Time OS Accelerator (Hardware Real-Time OS, HW-RTOS)
Operating frequency	100 MHz
Instruction set	Thumb®-2 instruction Arm v7-M architecture
Instruction RAM	768 Kbytes (RAM with ECC)
Data RAM	512 Kbytes (RAM with ECC)
Buffer RAM	64 Kbytes (RAM with ECC)
Internal system bus	- 32-bit system bus at 100 MHz - 128-bit communication bus at 100 MHz
DMA bus (system bus side)	- 4 channels + 1 channel (for real-time port) - Supports software and various interrupt-triggered DMA
Boot options	- Serial flash ROM boot - External memory boot - External MCU boot
External memory support	- 16-bit or 32-bit bus interface - Page ROM / ROM / SRAM interface - Synchronous burst memory interface - Four chip selects for external SRAM - 256-Mbyte (max) external memory space - Programmable wait function
External MCU interface	- 16-bit or 32-bit bus interface - General-purpose interface for static memory - Address space: 2 Mbytes (instruction RAM, data RAM, register area)
Serial flash ROM memory controller	- Support serial interface compatible with SPI of the companies - Support direct boot from serial memory device - Support Fast Read, Fast Read Dual Output, Fast Read Dual I/O mode - Direct layout in memory space
Interrupt	- 29 external interrupt pins
Internal peripheral circuit	
I/O ports	CMOS I/O: 96 pins (max.)
Timers (three systems)	- Internal timer of Hardware RTOS
	- Internal timer of CPU
	- 4-channel timer array - 32-bit counter & 32-bit data register - Counter by external signal

(2/2)

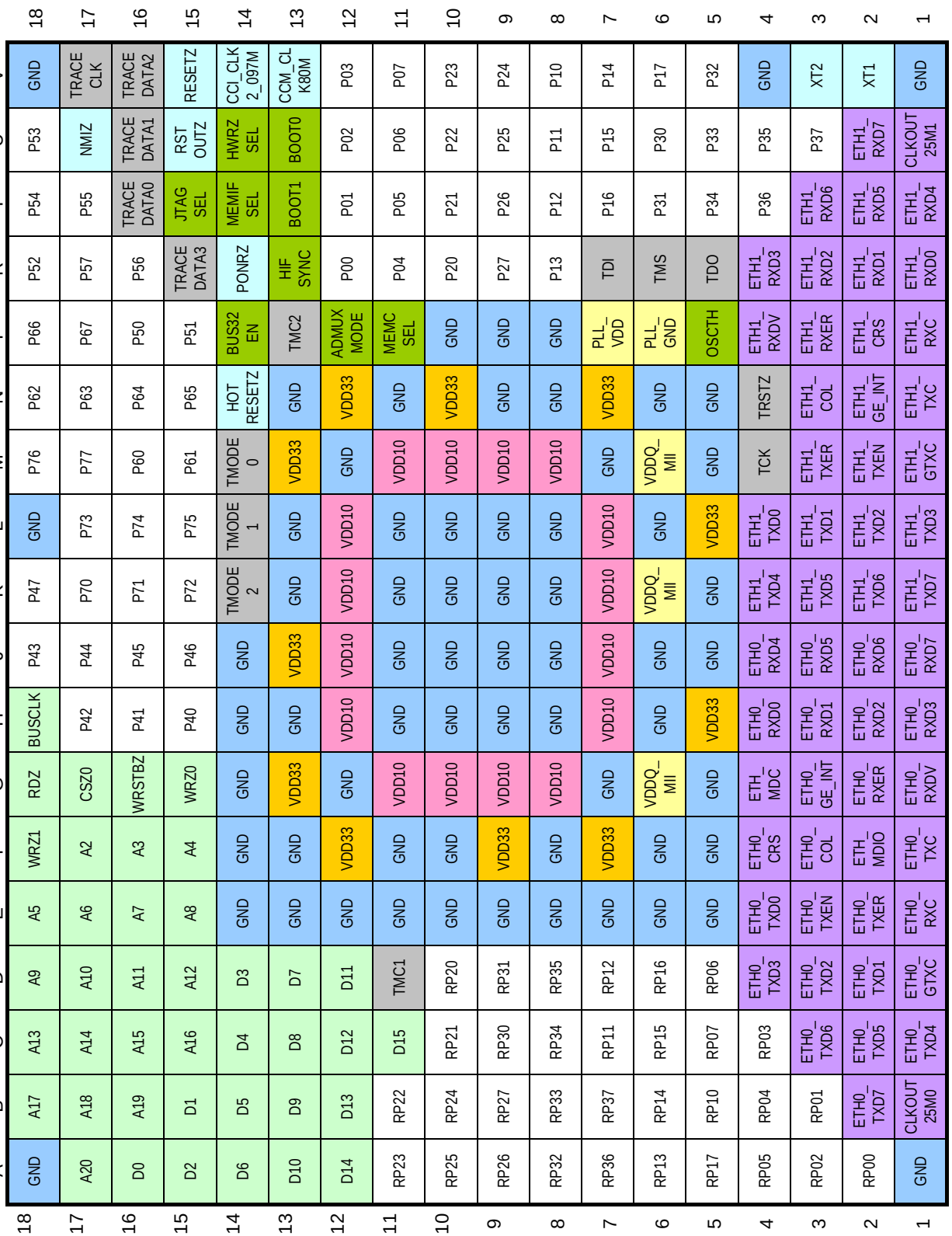
Item \ Product	R-IN32M3-CL
Internal peripheral circuit	
Watchdog timer	- 1 channel - Software-triggered start mode - Selectable operations in response to errors: - Generation of a non-maskable interrupt (NMIZ) - Generation of a reset
Asynchronous serial interface	- 2 channels - Full duplex - FIFOs: 10 bits x 16 receive and 8 bits x 16 transmit - Support output of receive errors and status - Character length: 7 or 8 bits - Parity bit options: Odd, even, 0, none - Transmit stop bits: 1 or 2 bits
I2C serial interface	- 2 channels - Operating modes: Normal or high-speed - Transfer modes: Single-transfer mode or continuous-transfer mode - Transmission data length: 8 bits
CAN controller	- 2 channels - Conforming to ISO11898 - Support to transfer and receive normal frame and expand frame - Transmission speed: 1 Mbps (max.)
Clock synchronous serial interface	- 2 channels - Synchronized serial data transmission by three-wire system - Selectable master mode or slave mode - Built-in baud-rate generator - Transmission data length: 7 bits to 16 bits
CC-Link	- Intelligent device station[Note] - Remote device station
10/100/1000-Mbps Ether MAC	- 1 channel - Built-in 2-port switch - GMII / MII interface
CC-Link IE	CC-Link IE field (intelligent device station)
On-chip debug function	- Select serial wire or JTAG - Support Full Trace (Built-in ETM)
Internal PLL	Generates various clocks from 25-MHz input clock
Power supply voltage	I/O: VDD33 = 3.3±0.3 V Internal circuit: VDD10 = 1.0±0.1 V

Note: Please contact our sales representative for details.

1.3 Internal Block Diagram



1.4 Pin Assignments (Top View)



	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	GND	A20	D0	D2	D6	D10	D14	RP23	RP25	RP26	RP32	RP36	RP13	RP17	RP05	RP02	RP00	GND
B	A17	A18	A19	D1	D5	D9	D13	RP22	RP24	RP27	RP33	RP37	RP14	RP10	RP04	RP01	ETH0_TXD7	CLKOUT 25M0
C	A13	A14	A15	A16	D4	D8	D12	D15	RP21	RP30	RP34	RP11	RP15	RP07	RP03	ETH0_TXD6	ETH0_TXD5	ETH0_TXD4
D	A9	A10	A11	A12	D3	D7	D11	TMC1	RP20	RP31	RP35	RP12	RP16	RP06	ETH0_TXD3	ETH0_TXD2	ETH0_TXD1	ETH0_GTXC
E	A5	A6	A7	A8	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	ETH0_TXD0	ETH0_TXEN	ETH0_TXER	ETH0_RXC
F	WRZ1	A2	A3	A4	GND	GND	VDD33	GND	GND	VDD33	GND	VDD33	GND	GND	ETH0_CRS	ETH0_COL	ETH_MDIO	ETH0_TXC
G	RDZ	CS20	WRSTBZ	WRZ0	GND	VDD33	GND	VDD10	VDD10	VDD10	VDD10	GND	VDDQ_MII	GND	ETH_MDC	ETH0_GE_INT	ETH0_RXER	ETH0_RXDV
H	BUSCLK	P42	P41	P40	GND	GND	VDD10	GND	GND	GND	GND	VDD10	GND	VDD33	ETH0_RXD0	ETH0_RXD1	ETH0_RXD2	ETH0_RXD3
J	P43	P44	P45	P46	GND	VDD33	VDD10	GND	GND	GND	GND	VDD10	GND	GND	ETH0_RXD4	ETH0_RXD5	ETH0_RXD6	ETH0_RXD7
K	P47	P70	P71	P72	TMODE 2	GND	VDD10	GND	GND	GND	GND	VDD10	VDDQ_MII	GND	ETH1_TXD4	ETH1_TXD5	ETH1_TXD6	ETH1_TXD7
L	GND	P73	P74	P75	TMODE 1	GND	VDD10	GND	GND	GND	GND	VDD10	GND	VDD33	ETH1_TXD0	ETH1_TXD1	ETH1_TXD2	ETH1_TXD3
M	P76	P77	P60	P61	TMODE 0	VDD33	GND	VDD10	VDD10	VDD10	VDD10	GND	VDDQ_MII	GND	ETH1_TXER	ETH1_TXEN	ETH1_GTXC	
N	P62	P63	P64	P65	HOT RESETZ	GND	VDD33	GND	VDD33	GND	GND	VDD33	GND	GND	TRSTZ	ETH1_COL	ETH1_GE_INT	ETH1_TXC
P	P66	P67	P50	P51	BUS32 EN	TMC2	ADMUX MODE	MEMC SEL	GND	GND	GND	PLL_VDD	PLL_GND	OSCTH	ETH1_RXDV	ETH1_RXER	ETH1_CRS	ETH1_RXC
R	P52	P57	P56	TRACE DATA3	PONRZ	HIF SYNC	P00	P04	P20	P27	P13	TDI	TMS	TDO	ETH1_RXD3	ETH1_RXD2	ETH1_RXD1	ETH1_RXD0
T	P54	P55	TRACE DATA0	JTAG SEL	MEMIF SEL	BOOT1	P01	P05	P21	P26	P12	P16	P31	P34	P36	ETH1_RXD6	ETH1_RXD5	ETH1_RXD4
U	P53	NMIZ	TRACE DATA1	RST OUTZ	HWRZ SEL	BOOT0	P02	P06	P22	P25	P11	P15	P30	P33	P35	P37	ETH1_RXD7	CLKOUT 25M1
V	GND	TRACE CLK	TRACE DATA2	RESETZ	CCI_CLK 2_097M	CCM_CLK 80M	P03	P07	P23	P24	P10	P14	P17	P32	GND	XT2	XT1	GND

1.5 Base Addresses of the System Registers Area

The addresses of registers given in the subsequent sections are relative to the base addresses. In access to the registers via the external MCU interface, the base address is D_0000H. In access by the internal CPU or DMA controller, the base address is 4001_0000H.

- In access by the CPU or DMA controller
  BASE = 4001_0000H
- In access via the external microcontroller interface
  BASE = D_0000H

2. Pin Functions

The meanings of the symbols and abbreviations used in this document are given below.

Table 2.1 Meanings of the Items in the List of Pins

Item	Meaning
Pin name	Name of the pin shown in section 1.4, Pin Assignments (Top View).
I/O	I/O direction of the given pin
Function	Summary of the given pin function
Active	Active level of the given pin
Level during reset Level after reset	"Level during reset" indicates the pin state while RSTOUTZ = low, and "Level after reset" indicates the pin state directly after the transition to RSTOUTZ = high. For details on the reset specifications, see the R-IN32M3 Series User's Manual (Peripheral Modules).

Table 2.2 Meanings of the Symbols and Abbreviations in the List of Pins

Target	Symbol and Abbreviation	Meaning
Pin name	- (hyphen)	Indicates that the pin is a dedicated pin and is not multiplexed with a port-pin function.
I/O	- (hyphen)	Indicates that the pin is a pin such as a power supply or ground pin and so does not have an I/O direction.
Active	- (hyphen)	Indicates that there is no active level (clock signals, data bus, and address bus).
	High	The active level is high.
	Low	The active level is low.
Level during reset Level after reset	- (hyphen)	Indicates an input-dedicated pin that has no initial level or state following a reset.
	High	The pin state during a reset is high.
	Low	The pin state during a reset is low.
	Hi-Z (high)	The pin state during a reset is Hi-Z (high) with the internal pull-up resistor pulling it to the high level.
	Hi-Z (low)	The pin state during a reset is Hi-Z (low) with the internal pull-up resistor pulling it to the low level.

2.1 List of Pins

2.1.1 Ethernet Pins

(1) PHY Interface Pins

Pin Name	I/O	Function	Active	Level during Reset	Level after Reset
ETH0_TXC	I	Ethernet 0 10-M/100-M transmit clock (2.5 MHz/25 MHz)	-	-	
ETH0_GTXC[Note]	O	Ethernet 0 1-G transmit clock (125 MHz)	-	High	
ETH0_TXEN[Note]	O	Ethernet 0 transmit enable output signal	High	Low	
ETH0_TXER[Note]	O	Ethernet 0 transmit error output signal	High	Low	
ETH0_TXD0-ETH0_TXD7[Note]	O	Ethernet 0 transmit data output signal	-	Low	
ETH0_GE_INT	I	Ethernet 0 PHY interrupt signal	High/Low	-	
ETH0_RXC	I	Ethernet 0 receive clock	-	-	
ETH0_RXDV	I	Ethernet 0 receive data enable input signal	High	-	
ETH0_RXER	I	Ethernet 0 receive data error input signal	High	-	
ETH0_RXD0-ETH0_RXD7	I	Ethernet 0 receive data input signal	-	-	
ETH0_CRS	I	Ethernet 0 carrier sense input signal	High	-	
ETH0_COL	I	Ethernet 0 collision detection input signal	High	-	
ETH1_TXC	I	Ethernet 1 10-M/100-M transmit clock (2.5 MHz/25 MHz)	-	-	
ETH1_GTXC[Note]	O	Ethernet 1 1-G transmit clock (125 MHz)	-	High	
ETH1_TXEN[Note]	O	Ethernet 1 transmit enable output signal	High	Low	
ETH1_TXER[Note]	O	Ethernet 1 transmit error output signal	High	Low	
ETH1_TXD0-ETH1_TXD7[Note]	O	Ethernet 1 transmit data output signal	-	Low	
ETH1_GE_INT	I	Ethernet 1 PHY interrupt signal	High/Low	-	
ETH1_RXC	I	Ethernet 1 receive clock	-	-	
ETH1_RXDV	I	Ethernet 1 receive data enable input signal	High	-	
ETH1_RXER	I	Ethernet 1 receive data error input signal	High	-	
ETH1_RXD0-ETH1_RXD7	I	Ethernet 1 receive data input signal	-	-	
ETH1_CRS	I	Ethernet 1 carrier sense input signal	High	-	
ETH1_COL	I	Ethernet 1 collision detection input signal	High	-	
ETH_MDC	O	Ethernet management interface clock	-	Low	Clock output
ETH_MDIO	I/O	Ethernet management data signal	-	Hi-Z	

Note: The driving ability can be switched by the setting of the ETHDRCTRL register. For details, see section 7.3.3.2, Ethernet Interface Buffer Function Select Register (ETHDRCTRL), in the R-IN32M3 Series User's Manual (Peripheral Modules).

(2) Other Pins

Pin Name	I/O	Function	Shared Port	Active	Level during Reset	Level after Reset
PHYLINK0, PHYLINK1	I	PHY Link port (for EtherSwitch)	P06-P07	High	Hi-Z (High)	
ETHSWSECOUT	O	EtherSwitch event output per second (output pulses have a width of 2 cycles of HCLK)	P24	High		

2.1.2 External Memory Interface Pins

Pin Name	I/O	Function	Shared Pin	Shared Port	Active	Level during Reset	Level after Reset
BUSCLK	O	Bus clock output	-	-	-	Clock output	
CSZ0	O	Chip select signal output	HCSZ	-	Low	Hi-Z (High)	High
CSZ1	O		HPGCSZ	P44			Hi-Z (High)
CSZ2	O		-	P51			
CSZ3	O		-	P50			
A1/MA0 Note4	O	Address output	HA1	P40	-	Hi-Z (High)	Low
A2-A20/ MA1-MA19 Note4	O		HA2-HA20	-		Hi-Z (Low)	
A21-A27/ MA20-MA26 Note4	O		-	RP21-RP27			Hi-Z (Low)
D0-D15/ MD0-MD15 Note1 Note4	I/O	Data bus	HD0-HD15	-			
D16-D31/ MD16-MD31 Note1 Note4	I/O		HD16-HD31	RP30-RP37 RP10-RP17	-	Hi-Z (High)	
RDZ	O	Read strobe output	HRDZ	-	Low	Hi-Z (High)	High
WRSTBZ	O	Write strobe output	HWRSTBZ	-	Low		
WRZ0, WRZ1/ BENZ0, BENZ1	O	Valid byte lane strobe output	HWRZ0, HWRZ1/ HBENZ0, HBENZ1	-	Low		
WRZ2, WRZ3/ BENZ2, BENZ3	O		HWRZ2, HWRZ3/ HBENZ2, HBENZ3	RP06, RP07			Hi-Z (High)
WAITZ	I	Wait signal input	HWAITZ	P41	Low	Hi-Z (High)	
WAITZ1-WAITZ3 Note2	I	Wait signal input	-	P45-P47	Low		
BCYSTZ / ADVZ Note3	O	Address valid output	HBCYSTZ	RP20	Low		

Remark: Pins of the external memory interface pins other than BUSCLK are input pins while the internal reset signal (HRESETZ) is at its active level.

Notes 1. While the synchronous burst access memory controller is in use, these signals are multiplexed with the address signals if the ADMUXMODE pin is driven high.
ADMUXMODE = 0: MD0-MD31 (Separate address and data lines)
ADMUXMODE = 1: MD0-MD31/MA0-MA31 (Multiplexed address and data lines)

2. These pins are only available when the synchronous burst access memory controller is in use.

3. This pin functions as BCYSTZ when the asynchronous SRAM memory controller is in use and as ADVZ when the synchronous burst access memory controller is in use.

4. This pin functions as A1-A27 and D0-D31 functions when the asynchronous SRAM memory controller is in use and as MA0-MA26 and MD0-MD31 functions when the synchronous burst access memory controller is in use.

2.1.3 External MCU Interface Pins

Pin Name	I/O	Function	Shared Pin	Shared Port	Active	Level during & after Reset
HBUSCLK	I	Bus clock input for host	INTPZ11	P43	-	Hi-Z (High)
HCSZ	I	Chip select signal input	CSZ0	-	Low	
HPGCSZ	I	Page ROM mode chip select input	CSZ1	P44	Low	
HWAITZ	O	Wait signal output	WAITZ	P41	Low	
HA1	I	Address signal input	A1	P40	-	
HA2-HA20	I		A2-A20	-		Hi-Z (Low)
HD0-HD15	I/O	Data bus	D0-D15	-	-	
HD16-HD31	I/O		D16-D31	RP30-RP37 RP10-RP17		Hi-Z (High)
HRDZ	I	Read strobe input	RDZ	-	Low	
HWRSTBZ	I	Write strobe input	WRSTBZ	-	Low	
HWRZ0, HWRZ1/ HBENZ0, HBENZ1	I	Valid byte lane strobe input	WRZ0, WRZ1/ BENZ0, BENZ1	-	Low	
HWRZ2, HWRZ3/ HBENZ2, HBENZ3	I		WRZ2, WRZ3/ BENZ2, BENZ3	RP06, RP07		
HERROUTZ	O	Error interrupt output	SLEEPING	P42	Low	High
HBCYSTZ	I	Bus cycle input	BCYSTZ / ADVZ	RP20	Low	Hi-Z (High)

Caution: Input the low level to the HBUSCLK pin while asynchronous mode is in use.

Remark: The external MCU interface pins continue to operate during a reset.

2.1.4 Port Pins and Real-Time Port Pins

The ports and pins are configured as 12 sets of 8-bit ports.

They are accessible in 32-bit units by grouping sets of 4 ports; i.e. ports 0 to 3, ports 4 to 7, and real-time ports 0 to 3.

(1/4)

	Pin Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during & after Reset
P0	P00	INTPZ0	-	CCI_RUNLEDZ	-	Hi-Z (High)
	P01	INTPZ1	-	-	-	
	P02	INTPZ2	-	CCI_DLINKLEDZ	-	
	P03	INTPZ3	-	CCI_ERRLEDZ	CCS_MON5	
	P04	INTPZ4	-	CCI_LERR1LEDZ	CCS_MON6	
	P05	INTPZ5	-	CCI_LERR2LEDZ	CCS_MON7	
	P06	PHYLINK0	-	CCI_SDLEDZ	CCS_MON0	
	P07	PHYLINK1	-	CCI_RDLEDZ	CCS_RESOUT	
P1	P10	-	-	-	CCS_REFSTB	
	P11	-	-	-	CCS_MON4	Hi-Z (Low)
	P12	INTPZ6	-	CCI_NMIZ	-	Hi-Z (High)
	P13	INTPZ7	-	CCI_WDTIZ / CCS_WDTZ / CCM_WDTENZ	-	
	P14	SMSCK	-	-	-	
	P15	SMSI	-	-	-	
	P16	SMSO	-	-	-	
	P17	SMCSZ	-	-	-	
P2	P20	RXD0	-	CCM_LINKERRZ	-	
	P21	TXD0	-	CCM_ERRZ	-	
	P22	INTPZ8	-	CCS_IOTENSU	-	
	P23	INTPZ9	-	CCS_SENYU0	-	
	P24	INTPZ10	ETHSWSECOUT	CCS_SENYU1	-	
	P25	WDTOUTZ	−	CCS_ERRZ	-	
	P26	TIN1	TOUT1	CCM_RUNZ / CCS_RUNZ	-	
	P27	TIN0	TOUT0	-	-	

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	Pin Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during & after Reset
P3	P30	RXD1	-	-	-	Hi-Z (High)
	P31	TXD1	-	-	-	
	P32	DMAREQZ1	-	-	CCS_MON1	
	P33	DMAACKZ1	CCI_ WAITEDGEH	-	CCS_MON2	
	P34	DMATCZ1	CCI_WRLENH	-	CCS_MON3	
	P35	CSISCK1	INTPZ22	CCM_IRLZ	-	
	P36	CSISI1	INTPZ23	CCS_FUSEZ	-	
	P37	CSISO1	INTPZ24	CCM_MSTZ	-	
P4	P40	A1/MA0	HA1	-	-	
	P41	WAITZ	HWAITZ	-	-	
	P42	SLEEPING	HERROUTZ	CCM_SDGCZ	-	
	P43	INTPZ11	HBUSCLK	-	-	
	P44	CSZ1	HPGCSZ	-	-	
	P45	CSISCK0	WAITZ1	-	-	
	P46	CSISI0	WAITZ2	-	-	
	P47	CSISO0	WAITZ3	-	-	
P5	P50	CSZ3	-	CCM_LNKRUNZ / CCS_LNKRUNZ	-	
	P51	CSZ2	-	CCM_RDLEDZ / CCS_RDLEDZ	-	
	P52	TIN3	TOUT3	CCS_SDGATEON	-	Hi-Z (Low)
	P53	CRXD0	CCS_RD	CCM_RD	-	Hi-Z (High)
	P54	CTXD0	CCS_SD	CCM_SD	-	
	P55	CRXD1	-	-	-	
	P56	CTXD1	-	CCI_PHYREZ1	-	
	P57	TIN2	TOUT2	CCI_PHYREZ0	-	

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	Pin Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during & after Reset
P6	P60	SCL0	-	-	-	Hi-Z (High)
	P61	SDA0	-	-	-	
	P62	RTDMAREQZ	-	CCM_MDIN0	-	
	P63	RTDMAACKZ	-	CCM_MDIN1	-	
	P64	RTDMATCZ	-	CCM_MDIN2	-	
	P65	DMAREQZ0	-	CCM_MDIN3	-	
	P66	DMAACKZ0	-	CCI_INTZ	-	
	P67	DMATCZ0	-	-	-	
P7	P70	CSICS00	-	CCS_STATION_NO_0 / CCM_SNIN0	-	
	P71	CSICS01	-	CCS_STATION_NO_1 / CCM_SNIN1	-	
	P72	CSICS10	-	CCS_STATION_NO_2 / CCM_SNIN2	-	
	P73	CSICS11	-	CCS_STATION_NO_3 / CCM_SNIN3	-	
	P74	INTPZ12	-	CCS_STATION_NO_4 / CCM_SNIN4	-	
	P75	INTPZ13	-	CCS_STATION_NO_5 / CCM_SNIN5	-	
	P76	INTPZ14	-	CCS_STATION_NO_6 / CCM_SNIN6	-	
	P77	INTPZ15	-	CCS_STATION_NO_7 / CCM_SNIN7	-	

RP0x to RP3x function as real-time ports which can transfer data via a dedicated DMA controller. They are able to input and output data in 32-bit units in synchronization with the DMA transfer trigger.

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	Pin Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during & after Reset
RP0	RP00	INTPZ16	SCL1	CCM_SDLEDZ / CCS_SDLEDZ	-	Hi-Z (High)
	RP01	INTPZ17	SDA1	CCM_SMSTZ	-	
	RP02	INTPZ18	-	CCS_BS1	-	
	RP03	INTPZ19	-	CCS_BS2	-	
	RP04	INTPZ20	-	CCS_BS4	-	
	RP05	INTPZ21	-	CCS_BS8	-	
	RP06[Note]	WRZ2/BENZ2	HWRZ2/HBENZ2	-	-	
	RP07[Note]	WRZ3/BENZ3	HWRZ3/HBENZ3	-	-	
RP1	RP10	D24/MD24/HD24	-	-	-	
	RP11	D25/MD25/HD25	-	-	-	
	RP12	D26/MD26/HD26	-	-	-	
	RP13	D27/MD27/HD27	-	-	-	
	RP14	D28/MD28/HD28	-	-	-	
	RP15	D29/MD29/HD29	-	-	-	
	RP16	D30/MD30/HD30	-	-	-	
	RP17	D31/MD31/HD31	-	-	-	
RP2	RP20	BCYSTZ / ADVZ	HBCYSTZ	-	-	
	RP21	A21/MA20	-	-	-	Hi-Z (Low)
	RP22	A22/MA21	-	-	-	
	RP23	A23/MA22	-	-	-	
	RP24	A24/MA23	INTPZ25	-	-	
	RP25	A25/MA24	INTPZ26	-	-	
	RP26	A26/MA25	INTPZ27	-	-	
	RP27	A27/MA26	INTPZ28	-	-	
RP3	RP30	D16/MD16/HD16	-	-	-	Hi-Z (High)
	RP31	D17/MD17/HD17	-	-	-	
	RP32	D18/MD18/HD18	-	-	-	
	RP33	D19/MD19/HD19	-	-	-	
	RP34	D20/MD20/HD20	-	-	-	
	RP35	D21/MD21/HD21	-	-	-	
	RP36	D22/MD22/HD22	-	-	-	
	RP37	D23/MD23/HD23	-	-	-	

Note: Selected only when BUS32EN = 1.

2.1.5 Serial Flash ROM Interface Pins

The serial flash ROM interface pins are pins of the serial flash ROM memory controller.
They support the fast read, fast read dual output, and fast read dual I/O modes.

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
SMSCK	O	Serial clock output signal for serial flash ROM	P14	-	Hi-Z (High)
SMSI	I/O	Serial data I/O signal for serial flash ROM (connected to the SO pin of serial flash ROM)	P15	High	
SMSO	I/O	Serial data I/O signal for serial flash ROM (connected to the SI pin of serial flash ROM)	P16	High	
SMCSZ	O	Chip select output signal for serial flash ROM	P17	Low	

2.1.6 DMA Interface Pins

The DMA interface pins are external interface pins of the DMA controllers for the internal AHB bus.
As the external DMA interface, they control two types of DMA controllers incorporated in the R-IN32M3-CL; a general DMA controller for channel 0 and channel 1, and a DMA controller for real-time ports.

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
RTDMAREQZ	I	RTDMAC DMA transfer request input	P62	Low	Hi-Z (High)
RTDMAACKZ	O	RTDMAC DMA acknowledge output	P63	Low	
RTDMATCZ	O	RTDMAC terminal count output	P64	Low	
DMAREQZ0	I	DMA transfer request input 0	P65	Low	
DMAACKZ0	O	DMA acknowledge output 0	P66	Low	
DMATCZ0	O	Terminal count output 0	P67	Low	
DMAREQZ1	I	DMA transfer request input 1	P32	Low	
DMAACKZ1	O	DMA acknowledge output 1	P33	Low	
DMATCZ1	O	Terminal count output port 1	P34	Low	

Caution: The DMA interface pin is fixed to the specific channel of the DMA controller, and not assigned to any other DMA controller or channel. For details, see section 13, DMA Controllers, in the R-IN32M3 Series User's Manual: Peripheral Modules.

2.1.7 External Interrupt Input Pins

The chip has one non-maskable interrupt and 29 maskable interrupt input pins.

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
NMIZ	I	Non-maskable external interrupt input	-	Low	Hi-Z (High)
INTPZ0-INTPZ5	I	External interrupt input	P00-P05	Low	
INTPZ6, INTPZ7			P12, P13	Low	
INTPZ8-INTPZ10			P22-P24	Low	
INTPZ11			P43	Low	
INTPZ12-INTPZ15			P74-P77	Low	
INTPZ16-INTPZ21			RP00-RP05	Low	
INTPZ22-INTPZ24			P35-P37	Low	
INTPZ25-INTPZ28			RP24-RP27	Low	Hi-Z (Low)

2.1.8 Timer I/O Pins

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
TIN0 / TOUT0	I/O	Timer TAUJ0 I/O pin	P27	-	Hi-Z (High)
TIN1 / TOUT1	I/O	Timer TAUJ1 I/O pin	P26	-	
TIN2 / TOUT2	I/O	Timer TAUJ2 I/O pin	P57	-	
TIN3 / TOUT3	I/O	Timer TAUJ3 I/O pin	P52	-	Hi-Z (Low)

2.1.9 Watchdog Timer Output Pin

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
WDTOUTZ	O	Watchdog timer output pin	P25	Low	Hi-Z (High)

2.1.10 Trace Pins

Pin Name	I/O	Function	Active	Level during & after Reset
TRACECLK	O	Trace port clock output	-	Clock output
TRACEDATA3-TRACEDATA0	O	Trace port data output	-	Low

2.1.11 CPU Power Control Pin

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
SLEEPING	O	CPU SLEEP mode output	P42	High	Hi-Z (High)

2.1.12 Serial Interface Pins

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
TXD0	O	UART0 serial data output	P21	-	Hi-Z (High)
RXD0	I	UART0 serial data input	P20	-	
TXD1	O	UART1 serial data output	P31	-	
RXD1	I	UART1 serial data input	P30	-	
CSISCK0	I/O	CSI0 serial clock I/O	P45	-	
CSISI0	I	CSI0 serial data input	P46	-	
CSISO0	O	CSI0 serial data output	P47	-	
CSICS00, CSICS01	O	CSI0 chip select output 0, 1	P70, P71	Low	
CSISCK1	I/O	CSI1 serial clock I/O	P35	-	
CSISI1	I	CSI1 serial data input	P36	-	
CSISO1	O	CSI1 serial data output	P37	-	
CSICS10, CSICS11	O	CSI1 chip select 0, 1	P72, P73	Low	
SCL0	I/O	I2C0 serial clock	P60	-	
SDA0	I/O	I2C0 serial data	P61	-	
SCL1	I/O	I2C1 serial clock	RP00	-	
SDA1	I/O	I2C1 serial data	RP01	-	
CRXD0	I	CAN0 receive data input (5V-Tolerant buffer)	P53	-	
CTXD0	O	CAN0 transmit data output	P54	-	
CRXD1	I	CAN1 receive data input (5V-Tolerant buffer)	P55	-	
CTXD1	O	CAN1 transmit data output	P56	-	

2.1.13 CC-Link IE Field Pins (Intelligent Device Station)

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
CCI_RUNLEDZ	O	Run status output	P00	Low	Hi-Z (High)
CCI_DLINKLEDZ	O	Cyclic communication status output	P02	Low	
CCI_ERRLEDZ	O	Field network error status output	P03	Low	
CCI_LERR1LEDZ	O	Link error status output 1	P04	Low	
CCI_LERR2LEDZ	O	Link error status output 2	P05	Low	
CCI_SDLEDZ	O	Transmission state output	P06	Low	
CCI_RDLEDZ	O	Port reception state output	P07	Low	
CCI_NMIZ	O	Output NMI interrupt to MCU	P12	Low	Hi-Z (High)
CCI_WDTIZ	I	Input from external watchdog timer	P13	Low	
CCI_WAITEDGEH Note	I/O	Wait synchronized edge setting 0: Fall edge mode 1: Rise edge mode	P33	-	
CCI_WRLENH Note	I/O	WRL signal enable setting 0: Write byte enable operation 1: Normal byte enable operation	P34	-	
CCI_PHYREZ1	O	PHY reset output 1	P56	Low	
CCI_PHYREZ0	O	PHY reset output 0	P57	Low	
CCI_INTZ	O	Output interrupt to MCU	P66	Low	
CCI_CLK2_097M	I	2.097152-MHz clock (crystal oscillator)	-	-	-

Note: When user does boot with the external memory boot mode, external serial flash ROM boot mode, or instruction RAM boot mode, be sure not to input the low level to P33 (multiplexed with CCI_WAITEDGEH) and P34 (multiplexed with CCI_WRLENH) pins during a reset. P33 and P34 pins should be left open circuit or the high level should be input to the pins during a reset.
If you input the low level to P33 and P34 pins during a reset, you cannot access the CC-Link IE field from the CPU and DMA controller of the R-IN32M3.

2.1.14 CC-Link Pins (Intelligent Device Station)

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
CCM_LINKERRZ	O	Link error LED control output	P20	Low	Hi-Z (High)
CCM_ERRZ	O	Not used	P21	Low	
CCM_RUNZ	O	Run LED control output	P26	Low	
CCM_MDIN0-CCM_MDIN3	I	Transfer rate setting input	P62-P65	-	
CCM_SNIN0-CCM_SNIN7	I	Station no. setting switch input	P70-P77	-	
CCM_LNKRUNZ	O	Link run LED control output	P50	Low	
CCM_RDLEDZ	O	Receive data LED control output	P51	Low	
CCM_SDLEDZ	O	Transmit data LED control output	RP00	Low	
CCM_IRLZ	O	Interrupt signal output from communications circuit	P35	Low	
CCM_WDTENZ	I	Watchdog timer error input	P13	Low	
CCM_MSTZ	O	Note used	P37	Low	
CCM_SMSTZ	O	Note used	RP01	Low	
CCM_RD	I	Communications circuit data reception pin	P53	-	
CCM_SD	O	Communications circuit data transmission pin	P54	-	
CCM_SDGCZ	O	Communications circuit transmit data & gate control pin	P42	Low	
CCM_CLK80M	I	CC-Link clock (80 MHz)	-	-	-

2.1.15 CC-Link Pins (Remote Device Station)

Caution: To use a remote device station, it is necessary to connect a CCS_REFSTB (P10) pin to a port pin with the external interrupt function (INTPZ).

Pin Name	I/O	Function	Shared Port	Active	Level during & after Reset
CCS_MON0	O	Monitor signal	P06	-	Hi-Z (High)
CCS_MON1-CCS_MON3	O	Monitor signal	P32-P34	-	
CCS_MON4	O	Monitor signal	P11	-	Hi-Z (Low)
CCS_MON5-CCS_MON7	O	Monitor signal	P03-P05	-	Hi-Z (High)
CCS_RESOUT	O	Reset output signal	P07	High	
CCS_IOTENSU	I	Initial setting pin	P22	-	
CCS_SENYU0	I	Initial setting pin	P23	-	
CCS_SENYU1	I	Initial setting pin	P24	-	
CCS_ERRZ	O	Operation check LED	P25	Low	
CCS_RUNZ	O	Operation check LED	P26	Low	
CCS_LNKRUNZ	O	Link run LED control output	P50	Low	
CCS_STATION_NO_0-CCS_STATION_NO_7	I	Station no. setting switch input	P70-P77	-	
CCS_REFSTB	O	Interrupt signal	P10	High	
CCS_WDTZ	I	Watchdog timer input	P13	Low	
CCS_RDLEDZ	O	Receive data LED control output	P51	Low	
CCS_RD	I	Communications circuit data reception pin	P53	-	
CCS_SD	O	Communications circuit data transmission pin	P54	-	
CCS_SDLEDZ	O	Operation check LED	RP00	Low	
CCS_SDGATEON	O	Communications circuit transmit data & gate control pin	P52	High	Hi-Z (Low)
CCS_BS1	I	Baud rate setting switch input pin	RP02	-	Hi-Z (High)
CCS_BS2	I	Baud rate setting switch input pin	RP03	-	
CCS_BS4	I	Baud rate setting switch input pin	RP04	-	
CCS_BS8	I	Baud rate setting switch input pin	RP05	-	
CCS_FUSEZ	I	Fuse cutting input signal	P36	Low	
CCM_CLK80M Note	I	CC-Link clock input (80 MHz)	-	-	-

Note: This pin is shared with CC-Link (intelligent device station).

2.1.16 System Pins

Pin Name	I/O	Function	Active	Level during & after Reset
XT1	I	Clock input pins	-	-
XT2	I/O	OSCTH = 1: Oscillator is in use. XT1 and XT2 are respectively connected to GND and oscillator. CSCTH = 0: Resonator is in use. XT1 and XT2 are connected to resonator.	-	-
RESETZ	I	Reset input	Low	-
HOTRESETZ	I	Hot reset input	Low	-
PONRZ	I	Power on reset input	Low	-
OSCTH	I	External clock input mode setting 0: Resonator using mode 1: External clock input mode	High	-
JTAGSEL	I	JTAG pin operating mode setting 0: Cortex-M3 JTAG mode 1: B-SCAN JTAG mode	-	-
RSTOUTZ	O	External reset output	Low	Low (after reset: High)
CLKOUT25M0	O	PHY clock output	-	Oscillation source is passed through to these pins
CLKOUT25M1	O	PHY clock output	-	
PLL_VDD	-	PLL power supply (VDD) (1.0 V)	-	-
PLL_GND	-	PLL ground level (GND)	-	-
VDD33	-	I/O power supply (3.3 V)	-	-
VDD10	-	Internal power supply (1.0 V)	-	-
GND	-	Power supply ground level (GND)	-	-
VDDQ_MII	-	Ethernet I/O power supply (3.3 V)	-	-

2.1.17 Test Pins

Pin Name	I/O	Function	Active	Level during & after Reset
TMODE0-TMODE2	I	Test mode select pin	-	-
TMS	I/O	Mode select signal	-	-
TDI	I	Serial data input	-	-
TDO	O	Serial data output	-	-
TRSTZ	I	Reset signal	Low	-
TCK	I	Clock signal (JTAG clock)	-	-
TMC1	I	Renesas test pins	-	-
TMC2	I		-	-

2.1.18 Operating Mode Setting Pins

Pin Name	I/O	Function	Active	Level during & after Reset
BOOT1-BOOT0	I	Boot mode select 00: External memory boot 01: External serial flash ROM boot 10: External MCU boot 11: Instruction RAM boot (only available for debugging)	-	-
MEMIFSEL	I	External memory interface select 0: Slave memory interface 1: External MCU interface	-	-
BUS32EN	I	External memory interface bus width select 0: 16-bit bus 1: 32-bit bus	-	-
HIFSYNC	I	External MCU interface operating mode 0: Asynchronous SRAM interface 1: Synchronous SRAM interface	-	-
HWRZSEL	I	External MCU interface HWRZ/HBENZ select 0: Used as HBENZ 1: Used as HWRZ	-	-
MEMCSEL	I	Internal memory controller select 0: Asynchronous SRAM memory controller 1: Synchronous burst access memory controller	-	-
ADMUXMODE	I	Multiplexing of address and data lines 0: Separate address and data lines 1: Multiplexed address and data lines	-	-

The combinations of available operating mode setting pins in this product are as follows.

Boot Mode	External Memory Boot				External MCU Boot				External Serial Flash ROM Boot							
External Memory Interface	Slave Memory Interface				External MCU Interface				Slave Memory Interface				External MCU Interface			
MEMC Type	Asynchronous		Synchronous		Asynchronous		Synchronous		Asynchronous		Synchronous		Asynchronous		Synchronous	
External Bus Width	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit
BOOT1-0	00	00	00	00	10	10	10	10	01	01	01	01	01	01	01	01
MEMIFSEL	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
MEMCSEL	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
BUS32EN	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HIFSYNC	0	0	0	0	Note1	Note1	1	1	0	0	0	0	Note1	Note1	1	1
HWRZSEL	0	0	0	0	Note2	Note2	0	0	0	0	0	0	Note2	Note2	0	0
ADMUXMODE	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1

Caution: Any combination of operating mode setting pins other than the above is prohibited.

Notes 1. The mode of the external MCU interface is selectable by the level on the HIFSYNC pin.
HIFSYNC = 0: Asynchronous SRAM interface mode
HIFSYNC = 1: Synchronous SRAM interface mode
For details, see section 11, External MCU Interface, in the R-IN32M3 Series User's Manual (Peripheral Modules).
2. The external MCU interface HWRZ or HBENZ is selectable by the level on the HWRZSEL pin.
For details, see section 2.1.3.1, External MCU Interface Pins.

Remarks 1. The combination of operating-mode setting pins used to select booting for instruction RAM (BOOT1-0 = 11) is the same as that for booting from external memory (BOOT1-0 = 00).
2. Asynchronous: Asynchronous SRAM memory controller (MEMCSEL = 0)
Synchronous: Synchronous burst access memory controller (MEMCSEL = 1)

2.2 Pin States

The initial state of the port functions after release from the reset state differs depending on the state of the operating mode setting pins. For the state of the operating mode setting pins in each boot mode and the supported combinations, see section 2.1.18, Operating Mode Setting Pins.

Remarks 1. Entries in cells shaded in light green indicate multiplexed pin functions that are enabled in the initial state.

2. The initial state of booting for instruction RAM is the same as that for booting from external memory.

2.2.1 Pin States when Booting is from External Memory

Pin Name	External Memory Boot (BOOT1-0 = 00)			
	Slave Memory Interface (MEMIFSEL = 0)			
	Asynchronous SRAM Memory Controller (MEMCSEL = 0)		Synchronous Burst Access Memory Controller (MEMCSEL = 1)	
	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)
P00	P00	P00	P00	P00
P01	P01	P01	P01	P01
P02	P02	P02	P02	P02
P03	P03	P03	P03	P03
P04	P04	P04	P04	P04
P05	P05	P05	P05	P05
P06	P06	P06	P06	P06
P07	P07	P07	P07	P07
P10	P10	P10	P10	P10
P11	P11	P11	P11	P11
P12	P12	P12	P12	P12
P13	P13	P13	P13	P13
P14	P14	P14	P14	P14
P15	P15	P15	P15	P15
P16	P16	P16	P16	P16
P17	P17	P17	P17	P17
P20	P20	P20	P20	P20
P21	P21	P21	P21	P21
P22	P22	P22	P22	P22
P23	P23	P23	P23	P23
P24	P24	P24	P24	P24
P25	P25	P25	P25	P25
P26	P26	P26	P26	P26
P27	P27	P27	P27	P27
P30	P30	P30	P30	P30
P31	P31	P31	P31	P31
P32	P32	P32	P32	P32
P33	CCI_WAITEDGEH	CCI_WAITEDGEH	CCI_WAITEDGEH	CCI_WAITEDGEH
P34	CCI_WRLENH	CCI_WRLENH	CCI_WRLENH	CCI_WRLENH
P35	P35	P35	P35	P35
P36	P36	P36	P36	P36
P37	P37	P37	P37	P37

Pin Name	External Memory Boot (BOOT1-0 = 00)			
	Slave Memory Interface (MEMIFSEL = 0)			
	Asynchronous SRAM Memory Controller (MEMCSEL = 0)		Synchronous Burst Access Memory Controller (MEMCSEL = 1)	
	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)
P40	A1	P40	MA0	MA0
P41	P41	P41	P41	P41
P42	P42	P42	P42	P42
P43	P43	P43	P43	P43
P44	P44	P44	P44	P44
P45	P45	P45	P45	P45
P46	P46	P46	P46	P46
P47	P47	P47	P47	P47
P50	P50	P50	P50	P50
P51	P51	P51	P51	P51
P52	P52	P52	P52	P52
P53	P53	P53	P53	P53
P54	P54	P54	P54	P54
P55	P55	P55	P55	P55
P56	P56	P56	P56	P56
P57	P57	P57	P57	P57
P60	P60	P60	P60	P60
P61	P61	P61	P61	P61
P62	P62	P62	P62	P62
P63	P63	P63	P63	P63
P64	P64	P64	P64	P64
P65	P65	P65	P65	P65
P66	P66	P66	P66	P66
P67	P67	P67	P67	P67
P70	P70	P70	P70	P70
P71	P71	P71	P71	P71
P72	P72	P72	P72	P72
P73	P73	P73	P73	P73
P74	P74	P74	P74	P74
P75	P75	P75	P75	P75
P76	P76	P76	P76	P76
P77	P77	P77	P77	P77

Pin Name	External Memory Boot (BOOT1-0 = 00)			
	Slave Memory Interface (MEMIFSEL = 0)			
	Asynchronous SRAM Memory Controller (MEMCSEL = 0)		Synchronous Burst Access Memory Controller (MEMCSEL = 1)	
	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)
RP00	RP00	RP00	RP00	RP00
RP01	RP01	RP01	RP01	RP01
RP02	RP02	RP02	RP02	RP02
RP03	RP03	RP03	RP03	RP03
RP04	RP04	RP04	RP04	RP04
RP05	RP05	RP05	RP05	RP05
RP06	RP06	WRZ2	RP06	WRZ2
RP07	RP07	WRZ3	RP07	WRZ3
RP10	RP10	D24	RP10	MD24
RP11	RP11	D25	RP11	MD25
RP12	RP12	D26	RP12	MD26
RP13	RP13	D27	RP13	MD27
RP14	RP14	D28	RP14	MD28
RP15	RP15	D29	RP15	MD29
RP16	RP16	D30	RP16	MD30
RP17	RP17	D31	RP17	MD31
RP20	RP20	RP20	ADVZ	ADVZ
RP21	RP21	RP21	RP21	RP21
RP22	RP22	RP22	RP22	RP22
RP23	RP23	RP23	RP23	RP23
RP24	RP24	RP24	RP24	RP24
RP25	RP25	RP25	RP25	RP25
RP26	RP26	RP26	RP26	RP26
RP27	RP27	RP27	RP27	RP27
RP30	RP30	D16	RP30	MD16
RP31	RP31	D17	RP31	MD17
RP32	RP32	D18	RP32	MD18
RP33	RP33	D19	RP33	MD19
RP34	RP34	D20	RP34	MD20
RP35	RP35	D21	RP35	MD21
RP36	RP36	D22	RP36	MD22
RP37	RP37	D23	RP37	MD23

2.2.2 Pin States when Booting is from External Serial Flash ROM

Remarks 1. Asynchronous type: Asynchronous SRAM memory controller (MEMCSEL = 0)
Synchronous type: Synchronous burst access memory controller (MEMCSEL = 1)
2. 16-bit: 16-bit bus width of the external memory interface (BUS32EN = 0)
32-bit: 32-bit bus width of the external memory interface (BUS32EN = 1)

Pin Name	External Serial Flash ROM Boot (BOOT1-0 = 01)							
	Slave Memory Interface (MEMIFSEL = 0)				External MCU Interface (MEMIFSEL = 1)			
	Asynchronous Type		Synchronous Type		Asynchronous Type		Synchronous type	
	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit
P00	P00	P00	P00	P00	P00	P00	P00	P00
P01	P01	P01	P01	P01	P01	P01	P01	P01
P02	P02	P02	P02	P02	P02	P02	P02	P02
P03	P03	P03	P03	P03	P03	P03	P03	P03
P04	P04	P04	P04	P04	P04	P04	P04	P04
P05	P05	P05	P05	P05	P05	P05	P05	P05
P06	P06	P06	P06	P06	P06	P06	P06	P06
P07	P07	P07	P07	P07	P07	P07	P07	P07
P10	P10	P10	P10	P10	P10	P10	P10	P10
P11	P11	P11	P11	P11	P11	P11	P11	P11
P12	P12	P12	P12	P12	P12	P12	P12	P12
P13	P13	P13	P13	P13	P13	P13	P13	P13
P14	SMSCK	SMSCK	SMSCK	SMSCK	SMSCK	SMSCK	SMSCK	SMSCK
P15	SMSI	SMSI	SMSI	SMSI	SMSI	SMSI	SMSI	SMSI
P16	SMSO	SMSO	SMSO	SMSO	SMSO	SMSO	SMSO	SMSO
P17	SMCSZ	SMCSZ	SMCSZ	SMCSZ	SMCSZ	SMCSZ	SMCSZ	SMCSZ
P20	P20	P20	P20	P20	P20	P20	P20	P20
P21	P21	P21	P21	P21	P21	P21	P21	P21
P22	P22	P22	P22	P22	P22	P22	P22	P22
P23	P23	P23	P23	P23	P23	P23	P23	P23
P24	P24	P24	P24	P24	P24	P24	P24	P24
P25	P25	P25	P25	P25	P25	P25	P25	P25
P26	P26	P26	P26	P26	P26	P26	P26	P26
P27	P27	P27	P27	P27	P27	P27	P27	P27
P30	P30	P30	P30	P30	P30	P30	P30	P30
P31	P31	P31	P31	P31	P31	P31	P31	P31
P32	P32	P32	P32	P32	P32	P32	P32	P32
P33	CCI_ WAITEDGEH	CCI_ WAITEDGEH	CCI_ WAITEDGEH	CCI_ WAITEDGEH	CCI_ WAITEDGEH	CCI_ WAITEDGEH	CCI_ WAITEDGEH	CCI_ WAITEDGEH
P34	CCI_ WRLENH	CCI_ WRLENH	CCI_ WRLENH	CCI_ WRLENH	CCI_ WRLENH	CCI_ WRLENH	CCI_ WRLENH	CCI_ WRLENH
P35	P35	P35	P35	P35	P35	P35	P35	P35
P36	P36	P36	P36	P36	P36	P36	P36	P36
P37	P37	P37	P37	P37	P37	P37	P37	P37

Pin Name	External Serial Flash ROM Boot (BOOT1-0 = 01)							
	Slave Memory Interface (MEMIFSEL = 0)				External MCU Interface (MEMIFSEL = 1)			
	Asynchronous Type		Synchronous Type		Asynchronous Type		Synchronous type	
	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit
P40	A1	P40	MA0	MA0	HA1	P40	HA1	HA1
P41	P41	P41	P41	P41	HWAITZ	HWAITZ	HWAITZ	HWAITZ
P42	P42	P42	P42	P42	HERROUTZ	HERROUTZ	HERROUTZ	HERROUTZ
P43	P43	P43	P43	P43	HBUSCLK	HBUSCLK	HBUSCLK	HBUSCLK
P44	P44	P44	P44	P44	HPGCSZ	HPGCSZ	HPGCSZ	HPGCSZ
P45	P45	P45	P45	P45	P45	P45	P45	P45
P46	P46	P46	P46	P46	P46	P46	P46	P46
P47	P47	P47	P47	P47	P47	P47	P47	P47
P50	P50	P50	P50	P50	P50	P50	P50	P50
P51	P51	P51	P51	P51	P51	P51	P51	P51
P52	P52	P52	P52	P52	P52	P52	P52	P52
P53	P53	P53	P53	P53	P53	P53	P53	P53
P54	P54	P54	P54	P54	P54	P54	P54	P54
P55	P55	P55	P55	P55	P55	P55	P55	P55
P56	P56	P56	P56	P56	P56	P56	P56	P56
P57	P57	P57	P57	P57	P57	P57	P57	P57
P60	P60	P60	P60	P60	P60	P60	P60	P60
P61	P61	P61	P61	P61	P61	P61	P61	P61
P62	P62	P62	P62	P62	P62	P62	P62	P62
P63	P63	P63	P63	P63	P63	P63	P63	P63
P64	P64	P64	P64	P64	P64	P64	P64	P64
P65	P65	P65	P65	P65	P65	P65	P65	P65
P66	P66	P66	P66	P66	P66	P66	P66	P66
P67	P67	P67	P67	P67	P67	P67	P67	P67
P70	P70	P70	P70	P70	P70	P70	P70	P70
P71	P71	P71	P71	P71	P71	P71	P71	P71
P72	P72	P72	P72	P72	P72	P72	P72	P72
P73	P73	P73	P73	P73	P73	P73	P73	P73
P74	P74	P74	P74	P74	P74	P74	P74	P74
P75	P75	P75	P75	P75	P75	P75	P75	P75
P76	P76	P76	P76	P76	P76	P76	P76	P76
P77	P77	P77	P77	P77	P77	P77	P77	P77

Pin Name	External Serial Flash ROM Boot (BOOT1-0 = 01)							
	Slave Memory Interface (MEMIFSEL = 0)				External MCU Interface (MEMIFSEL = 1)			
	Asynchronous Type		Synchronous Type		Asynchronous Type		Synchronous type	
	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit
RP00	RP00	RP00	RP00	RP00	RP00	RP00	RP00	RP00
RP01	RP01	RP01	RP01	RP01	RP01	RP01	RP01	RP01
RP02	RP02	RP02	RP02	RP02	RP02	RP02	RP02	RP02
RP03	RP03	RP03	RP03	RP03	RP03	RP03	RP03	RP03
RP04	RP04	RP04	RP04	RP04	RP04	RP04	RP04	RP04
RP05	RP05	RP05	RP05	RP05	RP05	RP05	RP05	RP05
RP06	RP06	WRZ2	RP06	WRZ2	RP06	HWRZ2	RP06	HWRZ2
RP07	RP07	WRZ3	RP07	WRZ3	RP07	HWRZ3	RP07	HWRZ3
RP10	RP10	D24	RP10	MD24	RP10	HD24	RP10	HD24
PR11	RP11	D25	RP11	MD25	RP11	HD25	RP11	HD25
RP12	RP12	D26	RP12	MD26	RP12	HD26	RP12	HD26
RP13	RP13	D27	RP13	MD27	RP13	HD27	RP13	HD27
RP14	RP14	D28	RP14	MD28	RP14	HD28	RP14	HD28
RP15	RP15	D29	RP15	MD29	RP15	HD29	RP15	HD29
RP16	RP16	D30	RP16	MD30	RP16	HD30	RP16	HD30
RP17	RP17	D31	RP17	MD31	RP17	HD31	RP17	HD31
RP20	RP20	RP20	ADVZ	ADVZ	HBCYSTZ	HBCYSTZ	HBCYSTZ	HBCYSTZ
RP21	RP21	RP21	RP21	RP21	RP21	RP21	RP21	RP21
RP22	RP22	RP22	RP22	RP22	RP22	RP22	RP22	RP22
RP23	RP23	RP23	RP23	RP23	RP23	RP23	RP23	RP23
RP24	RP24	RP24	RP24	RP24	RP24	RP24	RP24	RP24
RP25	RP25	RP25	RP25	RP25	RP25	RP25	RP25	RP25
RP26	RP26	RP26	RP26	RP26	RP26	RP26	RP26	RP26
RP27	RP27	RP27	RP27	RP27	RP27	RP27	RP27	RP27
RP30	RP30	D16	RP30	MD16	RP30	HD16	RP30	HD16
RP31	RP31	D17	RP31	MD17	RP31	HD17	RP31	HD17
RP32	RP32	D18	RP32	MD18	RP32	HD18	RP32	HD18
RP33	RP33	D19	RP33	MD19	RP33	HD19	RP33	HD19
RP34	RP34	D20	RP34	MD20	RP34	HD20	RP34	HD20
RP35	RP35	D21	RP35	MD21	RP35	HD21	RP35	HD21
RP36	RP36	D22	RP36	MD22	RP36	HD22	RP36	HD22
RP37	RP37	D23	RP37	MD23	RP37	HD23	RP37	HD23

2.2.3 Pin States when Booting is for External MCU

Pin Name	External MCU Boot (BOOT1-0 = 10)			
	External MCU Interface (MEMIFSEL = 1)			
	Asynchronous SRAM Memory Controller (MEMCSEL = 0)		Synchronous Burst Access Memory Controller (MEMCSEL = 1)	
	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)
P00	P00	P00	P00	P00
P01	P01	P01	P01	P01
P02	P02	P02	P02	P02
P03	P03	P03	P03	P03
P04	P04	P04	P04	P04
P05	P05	P05	P05	P05
P06	P06	P06	P06	P06
P07	P07	P07	P07	P07
P10	P10	P10	P10	P10
P11	P11	P11	P11	P11
P12	P12	P12	P12	P12
P13	P13	P13	P13	P13
P14	P14	P14	P14	P14
P15	P15	P15	P15	P15
P16	P16	P16	P16	P16
P17	P17	P17	P17	P17
P20	P20	P20	P20	P20
P21	P21	P21	P21	P21
P22	P22	P22	P22	P22
P23	P23	P23	P23	P23
P24	P24	P24	P24	P24
P25	P25	P25	P25	P25
P26	P26	P26	P26	P26
P27	P27	P27	P27	P27
P30	P30	P30	P30	P30
P31	P31	P31	P31	P31
P32	P32	P32	P32	P32
P33	CCI_WAITEDGEH	CCI_WAITEDGEH	CCI_WAITEDGEH	CCI_WAITEDGEH
P34	CCI_WRLENH	CCI_WRLENH	CCI_WRLENH	CCI_WRLENH
P35	P35	P35	P35	P35
P36	P36	P36	P36	P36
P37	P37	P37	P37	P37

Pin Name	External MCU Boot (BOOT1-0 = 10)			
	External MCU Interface (MEMIFSEL = 1)			
	Asynchronous SRAM Memory Controller (MEMCSEL = 0)		Synchronous Burst Access Memory Controller (MEMCSEL = 1)	
	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)
P40	HA1	P40	HA1	HA1
P41	HWAITZ	HWAITZ	HWAITZ	HWAITZ
P42	HERROUTZ	HERROUTZ	HERROUTZ	HERROUTZ
P43	HBUSCLK	HBUSCLK	HBUSCLK	HBUSCLK
P44	HPGCSZ	HPGCSZ	HPGCSZ	HPGCSZ
P45	P45	P45	P45	P45
P46	P46	P46	P46	P46
P47	P47	P47	P47	P47
P50	P50	P50	P50	P50
P51	P51	P51	P51	P51
P52	P52	P52	P52	P52
P53	P53	P53	P53	P53
P54	P54	P54	P54	P54
P55	P55	P55	P55	P55
P56	P56	P56	P56	P56
P57	P57	P57	P57	P57
P60	P60	P60	P60	P60
P61	P61	P61	P61	P61
P62	P62	P62	P62	P62
P63	P63	P63	P63	P63
P64	P64	P64	P64	P64
P65	P65	P65	P65	P65
P66	P66	P66	P66	P66
P67	P67	P67	P67	P67
P70	P70	P70	P70	P70
P71	P71	P71	P71	P71
P72	P72	P72	P72	P72
P73	P73	P73	P73	P73
P74	P74	P74	P74	P74
P75	P75	P75	P75	P75
P76	P76	P76	P76	P76
P77	P77	P77	P77	P77

Pin Name	External MCU Boot (BOOT1-0 = 10)			
	External MCU Interface (MEMIFSEL = 1)			
	Asynchronous SRAM Memory Controller (MEMCSEL = 0)		Synchronous Burst Access Memory Controller (MEMCSEL = 1)	
	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)	16-bit (BUS32EN = 0)	32-bit (BUS32EN = 1)
RP00	RP00	RP00	RP00	RP00
RP01	RP01	RP01	RP01	RP01
RP02	RP02	RP02	RP02	RP02
RP03	RP03	RP03	RP03	RP03
RP04	RP04	RP04	RP04	RP04
RP05	RP05	RP05	RP05	RP05
RP06	RP06	HWRZ2	RP06	HWRZ2
RP07	RP07	HWRZ3	RP07	HWRZ3
RP10	RP10	HD24	RP10	HD24
RP11	RP11	HD25	RP11	HD25
RP12	RP12	HD26	RP12	HD26
RP13	RP13	HD27	RP13	HD27
RP14	RP14	HD28	RP14	HD28
RP15	RP15	HD29	RP15	HD29
RP16	RP16	HD30	RP16	HD30
RP17	RP17	HD31	RP17	HD31
RP20	HBCYSTZ	HBCYSTZ	HBCYSTZ	HBCYSTZ
RP21	RP21	RP21	RP21	RP21
RP22	RP22	RP22	RP22	RP22
RP23	RP23	RP23	RP23	RP23
RP24	RP24	RP24	RP24	RP24
RP25	RP25	RP25	RP25	RP25
RP26	RP26	RP26	RP26	RP26
RP27	RP27	RP27	RP27	RP27
RP30	RP30	HD16	RP30	HD16
RP31	RP31	HD17	RP31	HD17
RP32	RP32	HD18	RP32	HD18
RP33	RP33	HD19	RP33	HD19
RP34	RP34	HD20	RP34	HD20
RP35	RP35	HD21	RP35	HD21
RP36	RP36	HD22	RP36	HD22
RP37	RP37	HD23	RP37	HD23

2.3 Operating Mode Monitoring

The levels on the operating mode setting pins can be confirmed by using the operating mode monitoring register.
The table below lists the operating mode setting pins for which the settings can be checked.

For details of the operating mode monitor register, refer to the R-IN32M3 Series User's Manual (Peripheral Modules).

Table 2.3 Operating Mode Setting Pins for which the Settings can be Checked

Pin Name	Function
BUS32EN	Selects the bus width when the external memory interface is started
MEMIFSEL	Selects the type of external memory interface
HIFSYNC	Sets the operating mode of the external MCU interface
HWRZSEL	Selects HWRZ or HBENZ of the external MCU interface
JTAGSEL	Sets the operating mode of JTAG pins
OSCTH	Inputs high level in external clock input mode
BOOT0, BOOT1	Selects boot mode
MEMCSEL	Selects the internal memory controller
ADMUXMODE	Multiplexing of address and data lines

2.4 Buffer Switching

The driving ability and use of a pull-up or pull-down resistor is programmable for real-time and general-purpose port pins (with some exceptions).
The former function provides stable operation in systems with large loads by providing the ability to raise the driving ability.
Use the buffer-switching registers (DRCTL) to change the output buffers as required.

For details of the buffer switching registers, refer to the R-IN32M3 Series User's Manual (Peripheral Modules).

2.5 Buffer Types and Handling of Unused Pins

2.5.1 Ethernet Pins

(1) PHY Interface Pins

Pin Name	I/O	Interface	Recommended Connection when Not in Use
ETH0_TXC	I	Input buffer (3.3 V)	Connect to GND
ETH0_GTXC	O	BID_BUF(3.3V_GMII_MII)_with_IOLH_Control	Open
ETH0_TXEN			
ETH0_TXER			
ETH0_TXD0- ETH0_TXD7			
ETH0_GE_INT	I	Input buffer (3.3 V)	Connect to GND
ETH0_RXC	I	BID_BUF(3.3V_GMII_MII)_with_IOLH_Control	Connect to GND
ETH0_RXDV			
ETH0_RXER			
ETH0_RXD0- ETH0_RXD7			
ETH0_CRS	I	Input buffer (3.3 V)	Connect to GND
ETH0_COL			
ETH1_TXC			
ETH1_GTXC	O	BID_BUF(3.3V_GMII_MII)_with_IOLH_Control	Open
ETH1_TXEN			
ETH1_TXER			
ETH1_TXD0- ETH1_TXD7			
ETH1_GE_INT	I	Input buffer (3.3 V)	Connect to GND
ETH1_RXC	I	BID_BUF(3.3V_GMII_MII)_with_IOLH_Control	Connect to GND
ETH1_RXDV			
ETH1_RXER			
ETH1_RXD0- ETH1_RXD7			
ETH1_CRS	I	Input buffer (3.3 V)	Connect to GND
ETH1_COL			
ETH_MDC	O	Output buffer (3.3 V) 6 mA	Open
ETH_MDIO	I/O	I/O buffer (3.3 V) 6 mA	Connect to GND

2.5.2 External Memory/MCU Interface Pins

Pin Name	I/O	Interface	Recommended Connection when Not in Use
BUSCLK	O	Output buffer (3.3 V) 9 mA	Open
CSZ0 / HCSZ	I/O	I/O buffer (3.3 V) 6 mA 50kΩ pull-up	Open
A2-A20 / HA2-HA20	I/O	I/O buffer (3.3 V) 6 mA 50kΩ pull-down	Open
D0-D15 / HD0-HD15			
RDZ / HRDZ	I/O	I/O buffer (3.3 V) 6 mA 50kΩ pull-up	Open
WRSTBZ / HWRSTBZ			
WRZ0, WRZ1 / BENZ0, BENZ1 / HWRZ0, HWRZ1 / HBENZ0, HBENZ1			

2.5.3 External Interrupt Input Pins

Pin Name	I/O	Interface	Recommended Connection when Not in Use
NMIZ	I	Input buffer (3.3 V) Schmitt in, 50kΩ pull-up	Connect to VDD33 (3.3 V)

2.5.4 System Pins

Pin Name	I/O	Interface	Recommended Connection when Not in Use
XT1	I	Oscillator with EN	Note
XT2	I/O		Note
RSTOUTZ	O	Output buffer (3.3 V) 6 mA	Open
RESETZ	I	Input buffer (3.3 V) Schmitt in	Connect a reset signal since these pins are always used
PONRZ			
HOTRESETZ			Connect to VDD33 (3.3 V)
OSCTH	I	Input buffer (3.3 V) Schmitt in, 50kΩ pull-down	Set these pins according to the operating mode
JTAGSEL			
CLKOUT25M0	O	Output buffer (3.3 V) 6 mA	Open
CLKOUT25M1			

Note: The pin connection differs depending on the setting of the OSCTH pin.
For details, see the R-IN32M3 Series User's Manual (Board design edition).

2.5.5 Test Pins

Pin Name	I/O	Interface	Required Connection when Not in Use
TMODE0-TMODE2	I	Input buffer (3.3 V) Schmitt in, 50kΩ pull-down	Connect to GND
TMS	I/O	I/O buffer (3.3 V) 6 mA 50kΩ pull-up	Open
TDI	I	Input buffer (3.3 V), 50kΩ pull-up	Open
TDO	O	3-state output buffer (3.3 V) 6mA	Open
TRSTZ	I	Input buffer (3.3 V) Schmitt in, 50kΩ pull-up	Open
TCK	I	Input buffer (3.3 V), 50kΩ pull-down	Open
TMC1	I	(TMC1) input buffer (3.3 V) for TMC terminal	Connect to GND
TMC2	I	(TMC2) input buffer (3.3 V) for TMC terminal	Connect to GND

2.5.6 Port Pins

(1/2)

Pin Name	I/O	Interface	Recommended connection when Not in use
P00-P07 P10	I/O	Programmable I/O buffer (3.3 V) Load drive select function (6 mA, 12 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or less)	Open
P11-P17, P22-P24, P27	I/O	Programmable I/O buffer (3.3 V) (6 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or less)	
P20, P21, P25, P26	I/O	Programmable I/O buffer (3.3 V) Load drive select function (6 mA, 12 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or less)	
P30-P36	I/O	Programmable I/O buffer (3.3 V) (6 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or less)	
P37	I/O	Programmable I/O buffer (3.3 V) Load drive select function (6 mA, 12 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or less)	
P40-P47	I/O	Programmable I/O buffer (3.3 V) (6 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or less)	
P50, P51	I/O	Programmable I/O buffer (3.3 V) Load drive select function (6 mA, 12 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or less)	
P52	I/O	Programmable I/O buffer (3.3 V) (6 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or less)	
P53-P56	I/O	5V-tolerant I/O buffer 4 mA 50kΩ pull-up	
P57 P60-P67	I/O	Programmable I/O buffer (3.3 V) (6 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or less)	

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Pin Name	I/O	Interface	Recommended Connection when Not in Use
P70-P77	I/O	Programmable I/O buffer (3.3 V) (6 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or less)	Open
RP00-RP07 RP10-RP17 RP20-RP27 RP30-RP37	I/O	Programmable I/O buffer (3.3 V) Load drive select function (6 mA, 12 mA) Resistor select function (50kΩ pull-up or 50kΩ pull-down or less)	

2.5.7 Operating Mode Setting Pins

Pin Name	I/O	Interface	Recommended Connection when not in Use
BOOT0, BOOT1 MEMIFSEL BUS32EN HIFSYNC HWRZSEL MEMCSEL ADMUXMODE	I	Input buffer (3.3 V) Schmitt in	Set these pins according to the operating mode

2.5.8 CC-Link IE Field Pin (Intelligent Device Station)

Pin Name	I/O	Interface	Recommended Connection when Not in Use
CCI_CLK2_097M	I	Input buffer (3.3 V)	Connect a 2.097152-MHz oscillator even when the CC-Link IE field is not in use

Caution: This pin requires a clock input even when the CC-Link IE field is not in use.

2.5.9 CC-Link Pin (Intelligent Device Station, Remote Device Station)

Pin Name	I/O	Interface	Recommended Connection when Not in Use
CCM_CLK80M	I	Input buffer (3.3 V)	Connect to GND

2.5.10 Trace Pins

Pin Name	I/O	Interface	Recommended Connection when Not in Use
TRACECLK TRACEDATA0-3	O	Output buffer (3.3 V) 6 mA	Open

3. Memory Maps

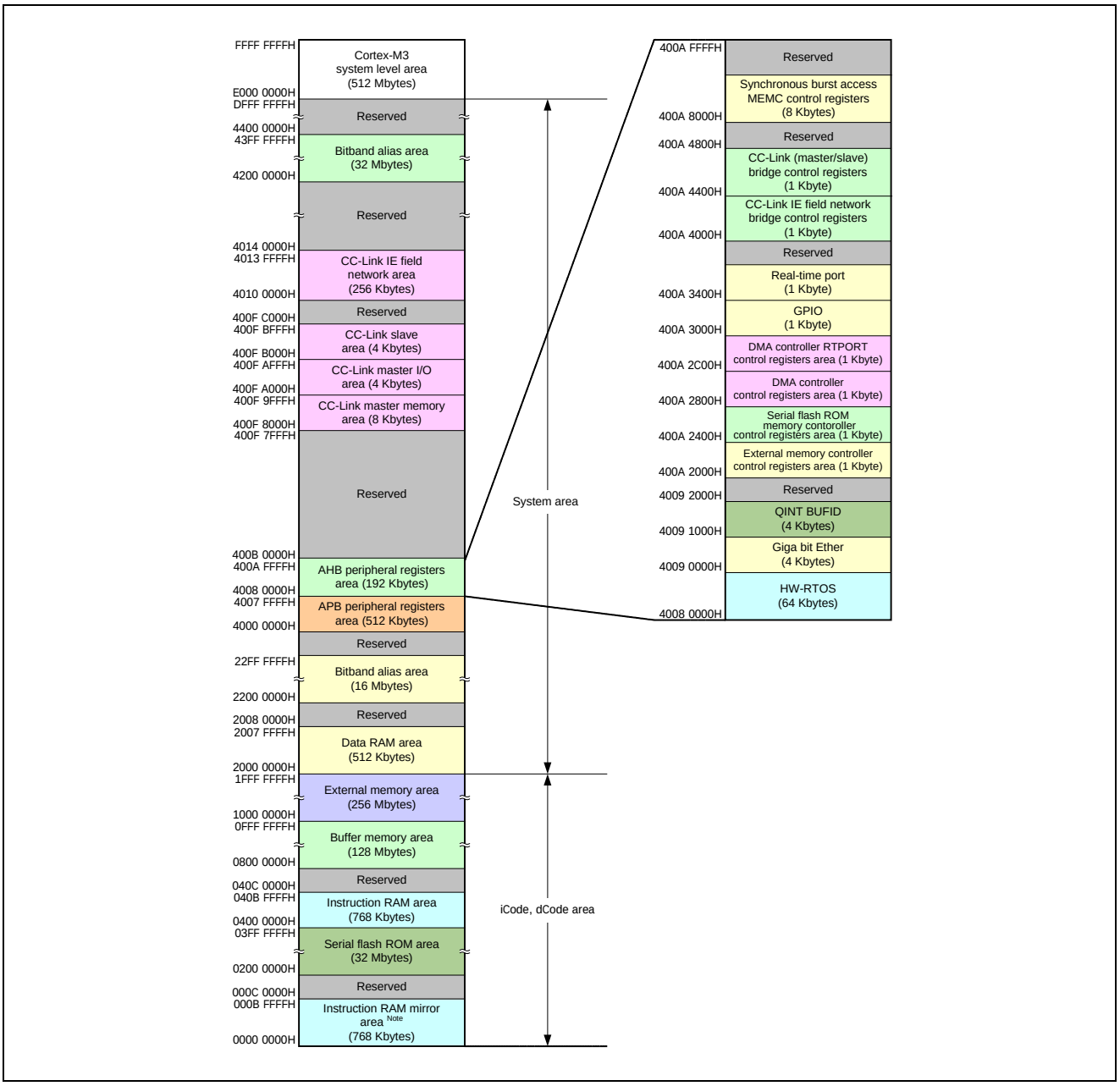

Figure 3.1 Memory Map (All)

Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode. For details, see section 5.3, Memory MAP in Each Boot Mode, in the R-IN32M3 Series User's Manual: Peripheral Modules.

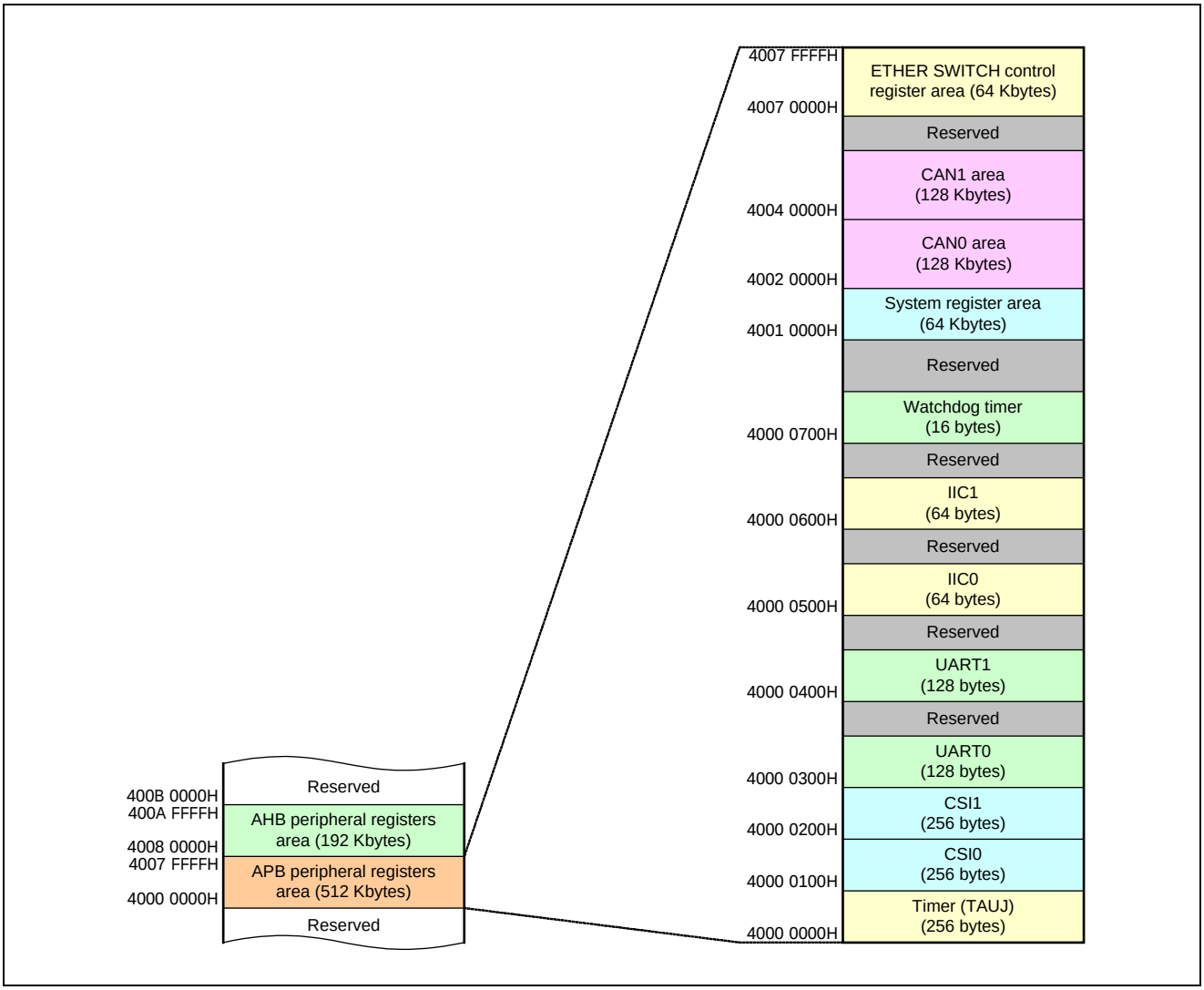

Figure 3.2 Memory Map (APB Peripheral Registers Area)

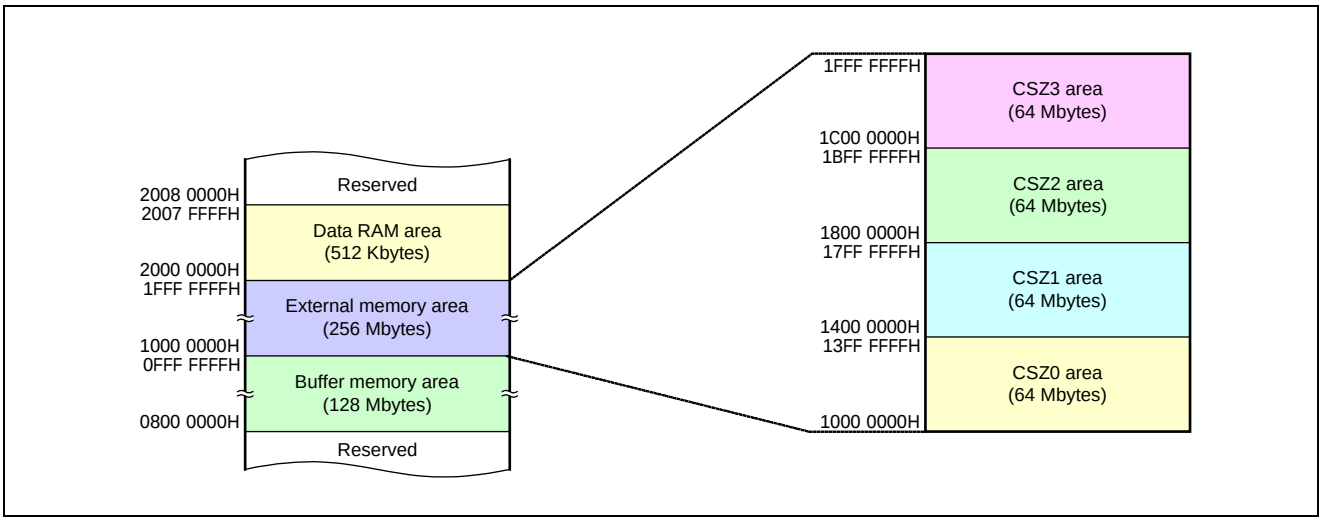

Figure 3.3 Memory Map (External Memory Area)

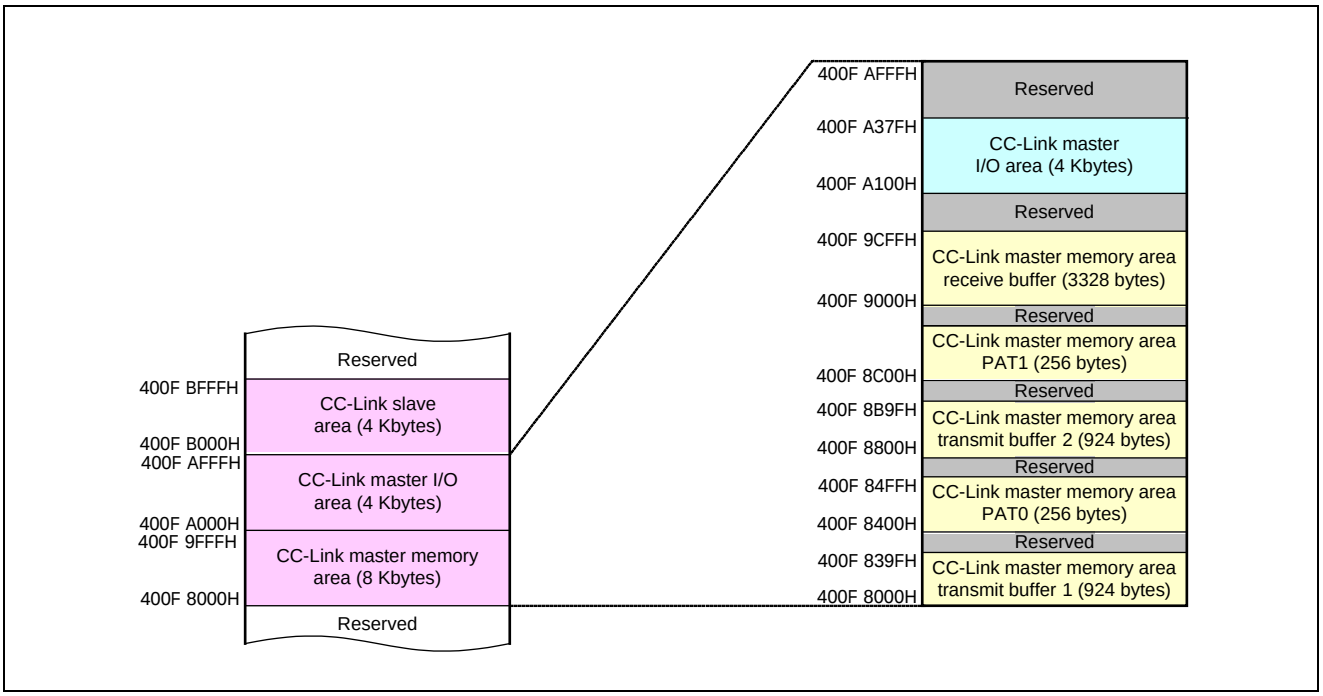

Figure 3.4 Memory Map (CC-Link Master Area)

Cautions 1. The CC-Link master shows a function block of intelligent station.

2. The CC-Link slave shows a function block of remote device station.

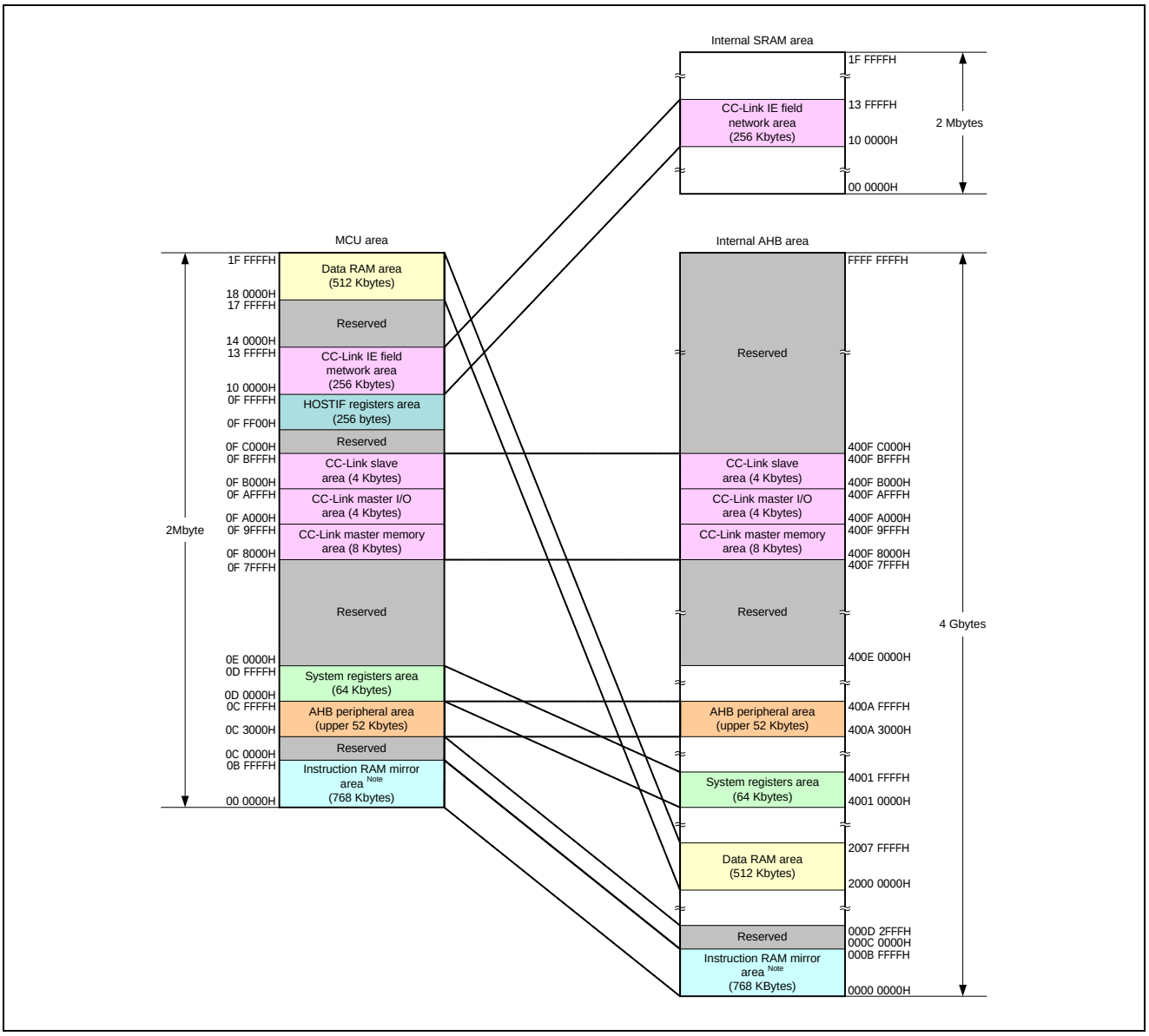

Figure 3.5 External MCU Interface Area

Note: The addresses of the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the selected boot mode, as shown in the table below. For details, see section 5.3, Memory MAP in Each Boot Mode, and section 4, Bus Architecture, in the R-IN32M3 Series User's Manual: Peripheral Modules.

BOOT1	BOOT0	Boot Mode	Access Destination Area	Remarks
0	0	External memory boot	—	External MCU interface is disabled
0	1	External serial flash ROM boot	Reserved	Access disabled
1	0	External MCU boot	Instruction RAM area	—
1	1	Instruction RAM boot	Instruction RAM area	Enabled only for debugging

4. Exception Handling

The R-IN32M3 uses the interrupt controller of Cortex-M3.
Refer to the following URL of Arm for the exceptions handling operation of Cortex-M3.
http://infocenter.arm.com/help/topic/com.arm.doc.set.cortexm/index.html

4.1 Exceptions List

Exception numbers 1 to 15 are system exceptions of the Cortex-M3 CPU. Interrupts from the internal hardware of the R-IN32M3 and external pins are assigned to exception number 16 and higher exception numbers.

Exception No.	Exception Type	Priority	Remark
1	Reset	-3 (highest)	- Input on the reset pin (RESETZ, PONRZ, or HOTRESETZ) - Reset by the watchdog timer - Set the SYSRESETREQ bit in NVIC of the Cortex-M3 CPU to 1 - Reset by the SYSRESET register
2	NMI	-2	- Input on the NMI pin - Generation of NMI by the watchdog timer
3	Hard fault	-1	All classes of exceptions that no other exception handler can handle. Used to call up a response to a fault.
4	Memory manage fault	Programmable	Exception from the MPU
5	Bus fault	Programmable	Bus error in access through the bus to the area outside the scope of management by the MPU
6	Use fault	Programmable	Error in instruction execution, including the execution of an undefined instruction
7 to 10	Reserved	-	-
11	SVCall	Programmable	System service call by an SVC instruction
12	Debug monitor	Programmable	Debug monitor
13	Reserved	-	-
14	PendSV	Programmable	Request for system service that can be kept pending
15	SysTick	Programmable	Indication from the system timer
16 and higher	R-IN32M3 specific Interrupt	Programmable	Interrupt from the internal hardware of the R-IN32M3 and external pins

4.2 List of Interrupts

The interrupts below are the exceptions (interrupts) with exception numbers 16 and higher, which are assigned to the NVIC of the Cortex-M3 CPU.
In the R-IN32M3, interrupts from the internal hardware and external pins are connected not only to the NVIC of the Cortex-M3 but also to the internal hardware real-time OS (HW-RTOS), trigger for starting the internal DMA controllers (common to both the general-purpose DMAC and real-time port DMAC), real-time ports, and timers.
The R-IN32M3 supports the following interrupts.

Table 4.1 List of Interrupts

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Exception No.	Name	Interrupt Source	Connected to				
			NVIC	HW-RTOS	DMAC	Real-Time Port	Timer
16	INTTAUJ2I0	Timer array TAUJ2 channel 0 interrupt	○	○	○	○	○
17	INTTAUJ2I1	Timer array TAUJ2 channel 1 interrupt	○	○	○	○	○
18	INTTAUJ2I2	Timer array TAUJ2 channel 2 interrupt	○	○	○	○	○
19	INTTAUJ2I3	Timer array TAUJ2 channel 3 interrupt	○	○	○	○	○
20	INTUAJ0TIT	UARTJ0 transmission interrupt	○	○	○	○	○
21	INTUAJ0TIR	UARTJ0 reception interrupt	○	○	○	○	○
22	INTUAJ1TIT	UARTJ1 transmission interrupt	○	○	○	○	○
23	INTUAJ1TIR	UARTJ1 reception interrupt	○	○	○	○	○
24	INTCSIH0IC	CSIH0 communication status interrupt	○	○	○	○	○
25	INTCSIH0IR	CSIH0 reception status interrupt	○	○	○	○	○
26	INTCSIH0IJC	CSIH0 job completion interrupt	○	○	○	○	○
27	INTCSIH1IC	CSIH1 communication status interrupt	○	○	○	○	○
28	INTCSIH1IR	CSIH1 reception status interrupt	○	○	○	○	○
29	INTCSIH1IJC	CSIH1 job completion interrupt	○	○	○	○	○
30	INTIICB0TIA	IICB0 transmission/reception interrupt request	○	○	○	○	○
31	INTIICB1TIA	IICB1 transmission/reception interrupt request	○	○	○	○	○
32	INTFCN0REC	FCN0 reception completion	○	○	○	○	○
33	INTFCN0TRX	FCN0 transmission completion	○	○	○	○	○
34	INTFCN0WUP	FCN0 sleep and wakeup/transmission suspension	○	○	○	○	○
35	INTFCN1REC	FCN1 reception completion	○	○	○	○	○
36	INTFCN1TRX	FCN1 transmission completion	○	○	○	○	○
37	INTFCN1WUP	FCN1 sleep and wakeup/transmission suspension	○	○	○	○	○
38	INTDMA00	General DMAC channel 0 transfer completion interrupt	○	○	○	○	○
39	INTDMA01	General DMAC channel 1 transfer completion interrupt	○	○	○	○	○
40	INTDMA02	General DMAC channel 2 transfer completion interrupt	○	○	○	○	○
41	INTDMA03	General DMAC channel 3 transfer completion interrupt	○	○	○	○	○
42	INTRTDMA	Real-time port DMAC transfer completion interrupt	○	○	○	○	○
43	-	Reserved	-	-	-	-	-
44	-	Reserved	-	-	-	-	-
45	-	Reserved	-	-	-	-	-

○: Connectable -: Not used

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Exception No.	Name	Interrupt Source	Connected to				
			NVIC	HW-RTOS	DMAC	Real-Time Port	Timer
46	-	Reserved	-	-	-	-	-
47	-	Reserved	-	-	-	-	-
48	INTBUFDMA	Inter-buffer DMA transfer completion	○	○	○	○	○
49	INTPHY0	Ether PHY interrupt 0	○	○	○	○	○
50	INTPHY1	Ether PHY interrupt 1	○	○	○	○	○
51	INTETHMII	Ether MII management access completion interrupt	○	○	○	○	○
52	INTETHPAUSE	Ether pause packet transmission completion	○	○	○	○	○
53	INTETHTX	Ether transmission completion interrupt	○	○	○	○	○
54	INTETHSW	Ether SWITCH Timer interrupt	○	○	○	○	○
55	INTETHSWDLR	Ether SWITCH DLR interrupt	○	○	○	○	○
56	INTETHSWSEC	Ether SWITCH SEC interrupt	○	○	○	○	○
57	INTETHRXFIFO	RX FIFO overflow	○	○	-	-	-
58	INTETHTXFIFO	TX FIFO underflow	○	○	-	-	-
59	INTETHRXDMA	Ether MACDMA reception completion	○	○	○	○	○
60	INTETHTXDMA	Ether MACDMA transmission completion	○	○	○	○	○
61	INTMACDMARXFRM	Receive frame successful interrupt	○	○	○	○	○
62	INTHOSTIF	External MCU interface interrupt	○	○	○	○	○
63	INTPZ0	INTPZ0 input	○	○	○	○	○
64	INTPZ1	INTPZ1 input	○	○	○	○	○
65	INTPZ2	INTPZ2 input	○	○	○	○	○
66	INTPZ3	INTPZ3 input	○	○	○	○	○
67	INTPZ4	INTPZ4 input	○	○	○	○	○
68	INTPZ5	INTPZ5 input	○	○	○	○	○
69	INTPZ6	INTPZ6 input	○	○	○	○	○
70	INTPZ7	INTPZ7 input	○	○	○	○	○
71	INTPZ8	INTPZ8 input	○	○	○	○	○
72	INTPZ9	INTPZ9 input	○	○	○	○	○
73	INTPZ10	INTPZ10 input	○	○	○	○	○
74	INTPZ11	INTPZ11 input	○	○	○	○	○
75	INTPZ12	INTPZ12 input	○	○	○	○	○
76	INTPZ13	INTPZ13 input	○	○	○	○	○
77	INTPZ14	INTPZ14 input	○	○	○	○	○
78	INTPZ15	INTPZ15 input	○	○	○	○	○
79	INTPZ16	INTPZ16 input	○	○	○	○	○
80	INTPZ17	INTPZ17 input	○	○	○	○	○
81	INTPZ18	INTPZ18 input	○	○	○	○	○
82	INTPZ19	INTPZ19 input	○	○	○	○	○

○: Connectable -: Not used

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Exception No.	Name	Interrupt Source	Connected to				
			NVIC	HW-RTOS	DMAC	Real-Time Port	Timer
83	INTPZ20	INTPZ20 input	○	○	○	○	○
84	INTPZ21	INTPZ21 input	○	○	○	○	○
85	INTPZ22	INTPZ22 input	○	○	○	○	○
86	INTPZ23	INTPZ23 input	○	○	○	○	○
87	INTPZ24	INTPZ24 input	○	○	○	○	○
88	INTPZ25	INTPZ25 input	○	○	○	○	○
89	INTPZ26	INTPZ26 input	○	○	○	○	○
90	INTPZ27	INTPZ27 input	○	○	○	○	○
91	INTPZ28	INTPZ28 input	○	○	○	○	○
92	INTHWRTOS	HW-RTOS interrupt	○	-	-	-	-
93	INTBRAMERR	Buffer RAM area access error	○	○	-	-	-
94	INTIICB0TIS	I2C0 status interrupt	○	○	-	-	-
95	INTIICB1TIS	I2C1 status interrupt	○	○	-	-	-
96	-	Reserved	-	-	-	-	-
97	INTSFLASH	Serial flash ROM controller error interrupt	○	○	-	-	-
98	INTUAJ0TIS	UARTJ0 status interrupt	○	○	-	-	-
99	INTUAJ1TIS	UARTJ1 status interrupt	○	○	-	-	-
100	INTCSIH0IRE	CSIH0 communication error interrupt	○	○	-	-	-
101	INTCSIH1IRE	CSIH1 communication error interrupt	○	○	-	-	-
102	INTFCN0ERR	FCN0 error detection	○	○	-	-	-
103	INTFCN1ERR	FCN1 error detection	○	○	-	-	-
104	INTDERR0	General DMAC error response interrupt	○	○	-	-	-
105	INTDERR1	Real-time port DMAC error response interrupt	○	○	-	-	-
106	INTETHTXFIFOERR	TX-FIFO error interrupt	○	○	-	-	-
107	INTETHRXERR	Ether receive flame error	○	○	-	-	-
108	INTETHRXDERR	MACDMA reception error interrupt	○	○	-	-	-
109	INTETHTXDERR	MACDMA transmission error interrupt	○	○	-	-	-
110	INTBUFDMAERR	Internal buffer DMA error	○	○	-	-	-
111	-	Reserved	-	-	-	-	-
112	-	Reserved	-	-	-	-	-
113	-	Reserved	-	-	-	-	-
114	-	Reserved	-	-	-	-	-
115	IRAMECCSEC	Internal instruction RAM 1-bit ECC error correction interrupt	○	-	-	-	-
116	DRAMECCSEC	Data RAM 1-bit ECC error correction interrupt	○	-	-	-	-
117	BRAMECCSEC	Buffer RAM 1-bit ECC error correction interrupt	○	-	-	-	-
118	IRAMECCDED	Internal instruction RAM 2-bit ECC error detection interrupt	○	-	-	-	-
119	DRAMECCDED	Data RAM 2-bit ECC error detection interrupt	○	-	-	-	-

○: Connectable -: Not used

(4/4)

Exception No.	Name	Interrupt Source	Connected to				
			NVIC	HW-RTOS	DMAC	Real-Time Port	Timer
120	BRAMECCDED	Buffer RAM 2-bit ECC error detection interrupt	○	-	-	-	-
121	INTCCISYCO	CC-Link IE Synco interrupt	○	○	○	○	○
122	INTCCISYNCI	CC-Link IE Synci interrupt	○	○	○	○	○
123	INTCCINMIZ	CC-Link IE NMIZ interrupt	○	○	○	○	○
124	INTCCIWDTZ	CC-Link IE WDTZ interrupt	○	○	○	○	○
125	INTCCIINTZ	CC-Link IE INTZ interrupt	○	○	○	○	○
126	INTCCICLKLOSSZ	CC-Link IE CLKLOSSZ interrupt	○	○	○	○	○
127	INTCCIMON0	CC-Link IE MON0 interrupt	○	○	○	○	○
128	INTCCIMON1	CC-Link IE MON1 interrupt	○	○	○	○	○
129	INTCCIMON2	CC-Link IE MON2 interrupt	○	○	○	○	○
130	INTCCIMON3	CC-Link IE MON3 interrupt	○	○	○	○	○
131	INTCCMRQ	CC-Link INTRQ interrupt	○	○	○	○	○
132	INTCCSRFSTB	CC-Link RFSTB interrupt Note	○	○	○	○	○
133	INTCCSMON3	CC-Link MON3 interrupt	○	○	○	○	○

○: Connectable -: Not used

Note: To use the CC-Link remote device station, connect the CCS_REFSTB (multiplexed with P10) pin to a pin with an external interrupt function (INTPZ) so as to generate an interrupt. In addition, select "both edges" as the mode for the interrupt trigger.

5. Peripheral Modules

For details of the following peripheral modules, refer to the R-IN32M3 Series User's Manual (Peripheral Modules).

- Clock function/Reset function
- CPU/Internal RAM
- Bus structure
- Hardware real-time OS
- Gigabit Ethernet interface
- Asynchronous SRAM memory controller
- Synchronous burst access memory controller
- External MCU interface
- Serial flash ROM memory controller
- DMA function
- Timer array unit J (TAUJ2)
- Window watchdog timer A (WDTA)
- Asynchronous serial interface J (UARTJ)
- Clocked serial interface H (CSIH)
- I^2C BUS (IICB)
- CAN controller (FCN)
- CC-Link (Intelligent device station, Remote device station)
- System registers (APB peripheral register area)
- Debug function

6. CC-Link IE Field (Intelligent Device Station) Function

The CC-Link IE field intelligent device station has functionality equivalent to that of the dedicated CP220 communications LSI chip manufactured by Mitsubishi Electric Corporation.
The outline specifications of the CC-Link IE field are as follows. For detailed specifications on the CC-Link IE field network, see the following CC-Link Partner Association website.

https://www.cc-link.org/en/cclink/cclinkie/index.html

Table 6.1 Outline Specifications of CC-Link IE Field

Item	Specification
Ethernet standards	IEEE802.3ab (1000BASE-T) compliant
Transfer rate	1 Gbps
Topology	Line, star, ring
Maximum number of connected units	254 modules
Maximum station-to-station distance	100 m

6.1 CC-Link IE Field (Intelligent Device Station) Control Registers

These control registers are used to adjust the timing for access to the CC-Link IE field network by the CPU.

Table 6.2 Overview of CC-Link IE Field (Intelligent Device Station) Control Registers

Register Name	Symbol	Address
CC-Link IE field (Intelligent device station) clock gate register	CIECLKGTD	4001 0938H
CC-Link IE field (Intelligent device station) wait delay register	CIEWAITDLY	4001 093CH
CC-Link IE field (Intelligent device station) bus size control register	CIEBSC	400A 4004H
CC-Link IE field (Intelligent device station) bus bridge control register	CIESMC	400A 4008H

6.1.1 CC-Link IE Field (Intelligent Device Station) Clock Gate Register (CIECLKGTD)

The CIECLKGTD register is used to temporarily stop supply of the bus clock signal. This is to prevent the generation of a clock glitch when switching the bus clock signal from the CC-Link IE field network. Writing 1 to the effective bit of this register stops supply of the clock signal and writing 0 to it causes supply to resume. Before making the setting to enable the SRAM bus path from an external MCU, be sure to use this register to stop the bus clock signal.

- Access This register can be read and written in 32-bit or 16-bit units.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
CIECLKGTD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CIECLKGTD	4001 0938H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	0000 0000H

Bit Position	Bit Name	Description
0	CIECLKGTD	Stops supply of the bus clock signal in the CC-Link IE field network. 0: Operating 1: Stopped

6.1.2 CC-Link IE Field (Intelligent Device Station) Wait Delay Register (CIEWAITDLY)

The CIEWAITDLY register is used to extend the wait period cycle to the bus of the CC-Link IE field network. From 4 to 0 cycles are selectable as the period of waiting. This register should be set before starting access to a CC-Link IE field network.

- Access This register can be read and written in 32-bit or 16-bit units.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
CIEWAITDLY	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	WAITDLY2	WAITDLY1	WAITDLY0	4001 093CH
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	0000 0000H

Bit Position	Bit Name	Description
2 to 0	WAITDLY2-0	These bits set the wait period cycle to the bus of the CC-Link IE field network. 000: 4 bus cycles 001: 3 bus cycles 010: 2 bus cycles 011: 1 bus cycle 100: 0 bus cycle (through) Other than above: Setting prohibited

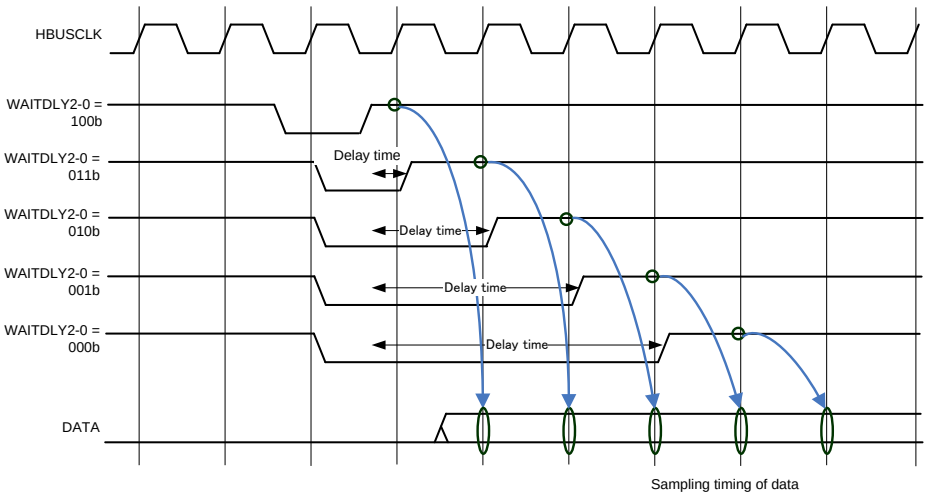

Figure 6.1 Timing of Data Sampling and Period of Waiting for the Bus of a CC-Link IE Field Network

6.1.3 CC-Link IE Field (Intelligent Device Station) Bus Size Control Register (CIEBSC)

The CIEBSC register is for setting the data bus width to access the CC-Link IE field (intelligent device station). When using the CC-Link IE field (intelligent device station), set the bits of this register to 0000 5555H.

- Access This register can be read and written in 32-bit units.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
CIEBSC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CIEBSC15	CIEBSC14	CIEBSC13	CIEBSC12	CIEBSC11	CIEBSC10	CIEBSC9	CIEBSC8	CIEBSC7	CIEBSC6	CIEBSC5	CIEBSC4	CIEBSC3	CIEBSC2	CIEBSC1	CIEBSC0	400A 4004H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000 5555H

Bit Position	Bit Name	Description
15 to 0	CIEBSC15-0	These bits should be set to 5555H.

6.1.4 CC-Link IE Field (Intelligent Device Station) Bus Bridge Control Register (CIESMC)

The CIESMC register is used for access control. When using the CC-Link IE field (intelligent device station), be sure to set the bits of this register to 0000 1151H.

- Access This register can be read and written in 32-bit units.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
CIESMC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CIESMC15	CIESMC14	CIESMC13	CIESMC12	CIESMC11	CIESMC10	CIESMC9	CIESMC8	CIESMC7	CIESMC6	CIESMC5	CIESMC4	CIESMC3	CIESMC2	CIESMC1	CIESMC0	400A 4008H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000 FFFFH

Bit Position	Bit Name	Description
15 to 0	CIESMC15-0	These bits should be set to 1151H.

6.2 Cautionary Notes

The following cautionary notes apply when accessing the CC-Link IE Field (Intelligent device station).

(1) Accessing when the MEMIFSEL Pin being Low

The on-chip CPU (Cortex-M3) and DMA controller of the R-IN32M3-CL can access the CC-Link IE field.

(2) Accessing when the MEMIFSEL Pin being High

In the initial state, only the external MCU interface can access the CC-Link IE field and not the Cortex-M3 or DMA controller. Access to the CC-Link IE field from the Cortex-M3 and DMA controller is enabled by switching the access paths by using the SRAM bridge select register (SRAMBRSEL). For the detailed specification of the register, refer to the R-IN32M3 Series User's Manual (Peripheral Modules).

Below is an example procedure for switching access paths.

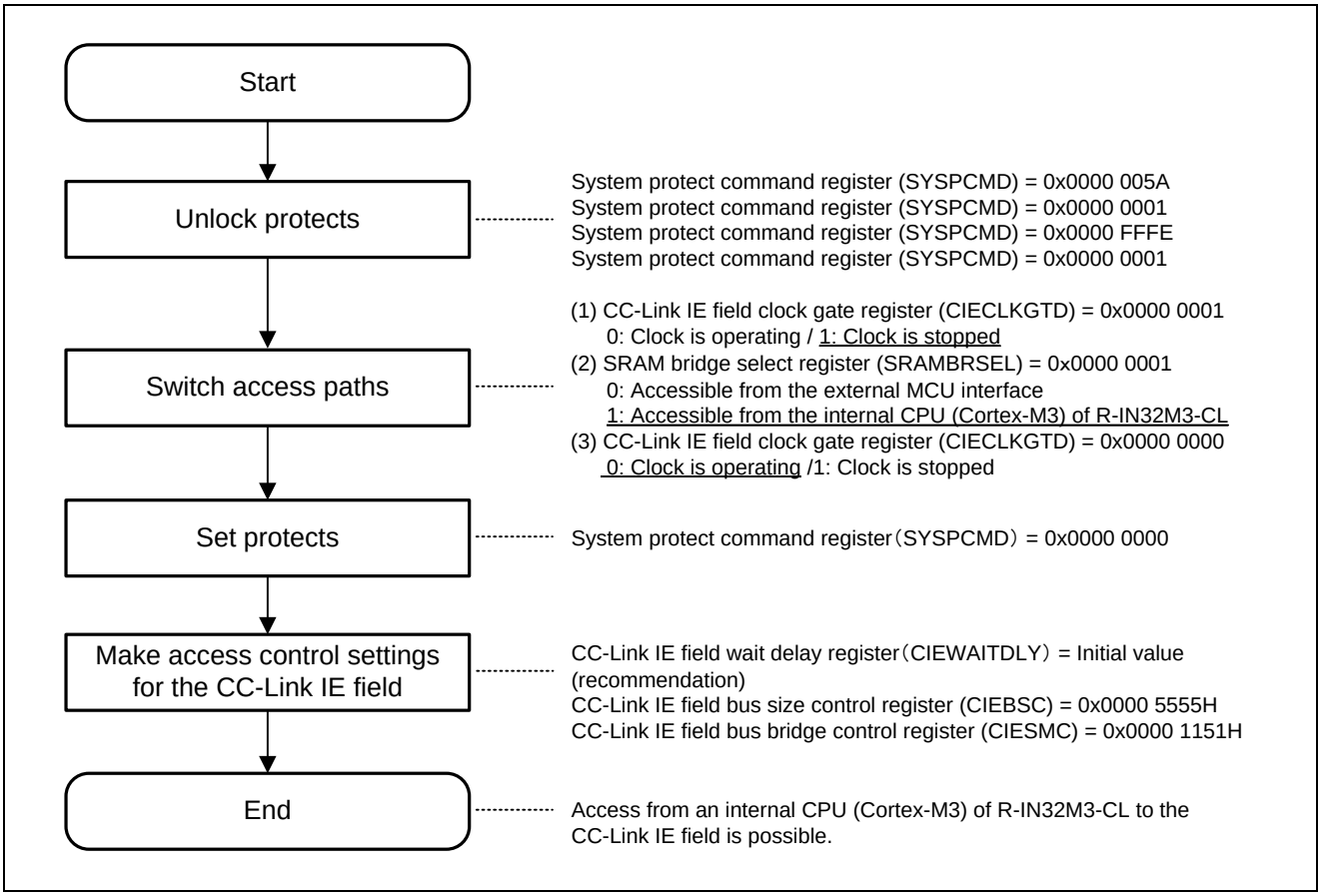

Figure 6.2 Procedure for Switching Access Path to the CC-Link IE Field

Caution: When accessing the CC-Link IE field from an internal master of the R-IN32M3-CL (Cortex-M3 or DMA controller), high level must be input to the P33 and P34 pins during a reset. For details, see section 2.1.13, CC-Link IE Field Pins (Intelligent Device Station).

(3) Setting when the CC-Link IE Field is not used

On the CC-Link IE Field in the R-IN32M4-CL2, the watch dog time (WDT) counting in the CC-Link IE Field starts after the reset is released. Therefore, it is necessary to stop the WDT operation during initialization in program when the CC-Link IE Field is not used. Also, when using the debugger, it is necessary to stop the WDT in the CC-Link IE Field by the setup macro.

7. Port Functions

7.1 Features

- I/O pins: 96
- Multiplexed with I/O pin functions of peripheral modules
- Input or output can be specified by bit units.

Cautions 1. Switching from a signal for a peripheral module that is multiplexed with a port pin to port mode might lead to a spike, depending on the state of the pin at the time.
The following general countermeasure for spikes should therefore be implemented in software.
- **Switch the pin function while the peripheral function is stopped.**
- **If the multiplexed pin function in use is an interrupt signal, clear the interrupt request flag and then remove masking of the interrupt.**
- **Only switch the mode after the output value is fixed.**

2. Do not externally apply an intermediate voltage to input buffers because these buffers do not implement through-current countermeasures.

7.2 Port Configuration

The R-IN32M3-CL incorporates eight 3-state I/O ports and four real-time control ports. Input or output mode can be specified for ports in 1-bit units. The basic structure of ports is the 8-bit unit, but ports 0 to 3 can also be grouped to enable reading and writing in 32-bit units. The real-time port pins (RP00 to RP37) can be used for input and output in synchronization with interrupt signals.

Each port has the registers shown below, which are used to make the I/O settings and to select and specify the multiplexed functions of the port pins. Figure 7.1 shows the basic circuit configuration of port registers and port pin.

Register Name	Application and Operation	
	Read	Write
Port registers (Pn, RPm)	Used to read the value of the output latch.	Used to set a value to the output latch.
Port mode registers (PMn, RPMm)	Used to read whether the port is in input or output mode.	Used to set the port to input or output mode.
Port mode control registers (PMCn, RPMCm)	Used to read whether the port pins are selected as port pins or as multiplexed function pins.	Used to select whether the port pins are used as port pins or as multiplexed function pins.
Port function control registers (PFCn, RPFCm)	Used to read which function is selected for the multiplexed pin.	Used to select the function of the multiplexed pin.
Port function control expansion registers (PFCEn, RPFCEm)		
Port pin input registers (PINn, RPINm)	Used to read the input level of the port pin.	Cannot be written.

Caution: Operation is not guaranteed if an unsupported function is allocated to the multiplexed pin. For example, if multiplexed function 4 is allocated to the P00 pin, which does not support multiplexed function 4, operation does not proceed correctly. For the allocation of multiplexed pins, see section 7.4, List of Selectable Multiplexed Functions.

Remark: n = 0 to 7, m = 0 to 3

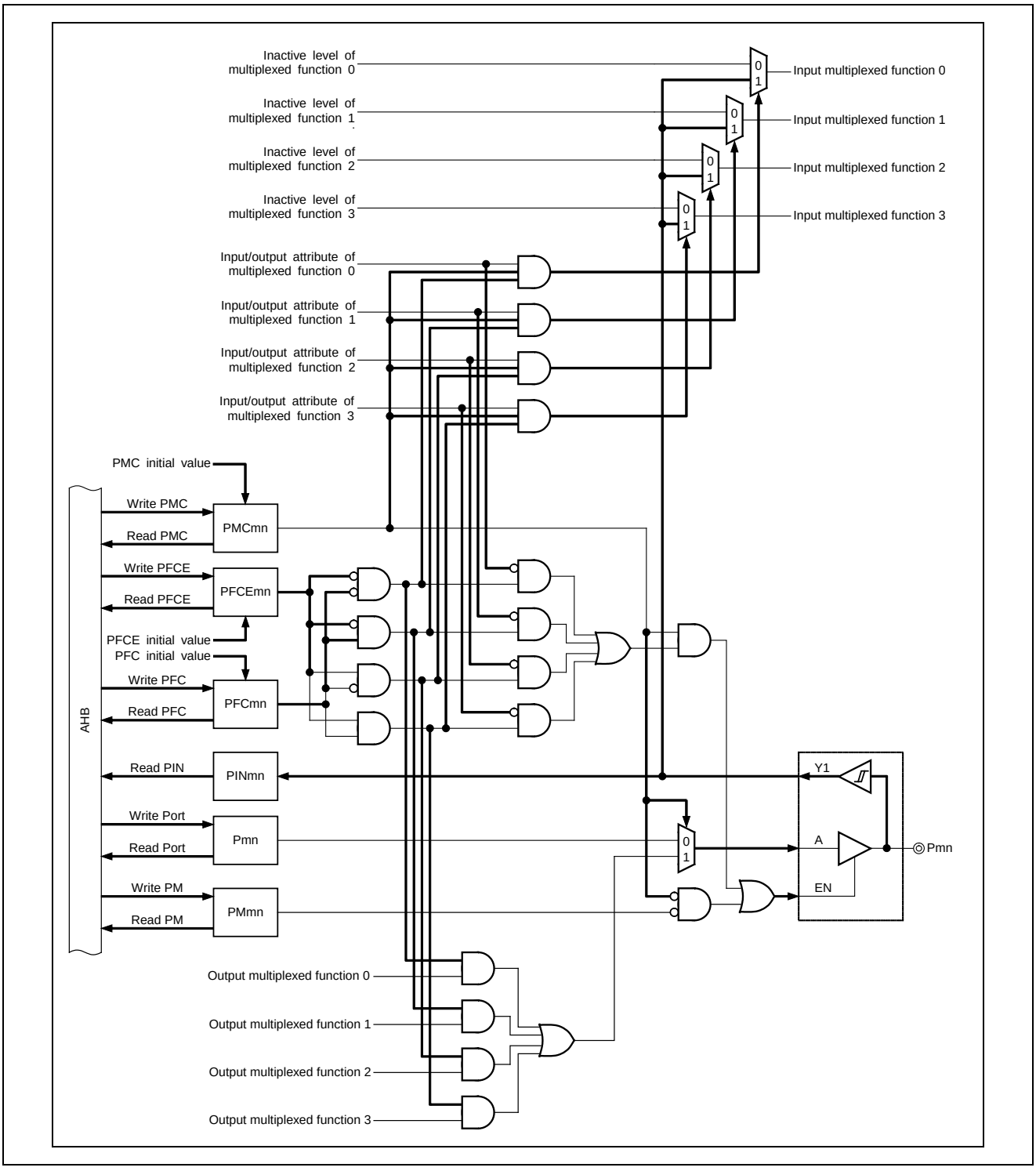

Figure 7.1 Basic Circuit Configuration of Ports

7.3 List of Registers

(1/6)

Register Name	Symbol	Address
Port register 0 (8 bits)	P0B	400A 3000H
Port register 1 (8 bits)	P1B	400A 3001H
Port register 2 (8 bits)	P2B	400A 3002H
Port register 3 (8 bits)	P3B	400A 3003H
Port register 4 (8 bits)	P4B	400A 3004H
Port register 5 (8 bits)	P5B	400A 3005H
Port register 6 (8 bits)	P6B	400A 3006H
Port register 7 (8 bits)	P7B	400A 3007H
Port register 0 (16 bits)	P0H	400A 3000H
Port register 2 (16 bits)	P2H	400A 3002H
Port register 4 (16 bits)	P4H	400A 3004H
Port register 6 (16 bits)	P6H	400A 3006H
Port register 0 (32 bits)	P0W	400A 3000H
Port register 4 (32 bits)	P4W	400A 3004H
Port mode register 0 (8 bits)	PM0B	400A 3010H
Port mode register 1 (8 bits)	PM1B	400A 3011H
Port mode register 2 (8 bits)	PM2B	400A 3012H
Port mode register 3 (8 bits)	PM3B	400A 3013H
Port mode register 4 (8 bits)	PM4B	400A 3014H
Port mode register 5 (8 bits)	PM5B	400A 3015H
Port mode register 6 (8 bits)	PM6B	400A 3016H
Port mode register 7 (8 bits)	PM7B	400A 3017H
Port mode register 0 (16 bits)	PM0H	400A 3010H
Port mode register 2 (16 bits)	PM2H	400A 3012H
Port mode register 4 (16 bits)	PM4H	400A 3014H
Port mode register 6 (16 bits)	PM6H	400A 3016H
Port mode register 0 (32 bits)	PM0W	400A 3010H
Port mode register 4 (32 bits)	PM4W	400A 3014H

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Register Name	Symbol	Address
Port mode control register 0 (8 bits)	PMC0B	400A 3020H
Port mode control register 1 (8 bits)	PMC1B	400A 3021H
Port mode control register 2 (8 bits)	PMC2B	400A 3022H
Port mode control register 3 (8 bits)	PMC3B	400A 3023H
Port mode control register 4 (8 bits)	PMC4B	400A 3024H
Port mode control register 5 (8 bits)	PMC5B	400A 3025H
Port mode control register 6 (8 bits)	PMC6B	400A 3026H
Port mode control register 7 (8 bits)	PMC7B	400A 3027H
Port mode control register 0 (16 bits)	PMC0H	400A 3020H
Port mode control register 2 (16 bits)	PMC2H	400A 3022H
Port mode control register 4 (16 bits)	PMC4H	400A 3024H
Port mode control register 6 (16 bits)	PMC6H	400A 3026H
Port mode control register 0 (32 bits)	PMC0W	400A 3020H
Port mode control register 4 (32 bits)	PMC4W	400A 3024H
Port function control register 0 (8 bits)	PFC0B	400A 3030H
Port function control register 1 (8 bits)	PFC1B	400A 3031H
Port function control register 2 (8 bits)	PFC2B	400A 3032H
Port function control register 3 (8 bits)	PFC3B	400A 3033H
Port function control register 4 (8 bits)	PFC4B	400A 3034H
Port function control register 5 (8 bits)	PFC5B	400A 3035H
Port function control register 6 (8 bits)	PFC6B	400A 3036H
Port function control register 7 (8 bits)	PFC7B	400A 3037H
Port function control register 0 (16 bits)	PFC0H	400A 3030H
Port function control register 2 (16 bits)	PFC2H	400A 3032H
Port function control register 4 (16 bits)	PFC4H	400A 3034H
Port function control register 6 (16 bits)	PFC6H	400A 3036H
Port function control register 0 (32 bits)	PFC0W	400A 3030H
Port function control register 4 (32 bits)	PFC4W	400A 3034H

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Register Name	Symbol	Address
Port function control expansion register 0 (8 bits)	PFCE0B	400A 3040H
Port function control expansion register 1 (8 bits)	PFCE1B	400A 3041H
Port function control expansion register 2 (8 bits)	PFCE2B	400A 3042H
Port function control expansion register 3 (8 bits)	PFCE3B	400A 3043H
Port function control expansion register 4 (8 bits)	PFCE4B	400A 3044H
Port function control expansion register 5 (8 bits)	PFCE5B	400A 3045H
Port function control expansion register 6 (8 bits)	PFCE6B	400A 3046H
Port function control expansion register 7 (8 bits)	PFCE7B	400A 3047H
Port function control expansion register 0 (16 bits)	PFCE0H	400A 3040H
Port function control expansion register 2 (16 bits)	PFCE2H	400A 3042H
Port function control expansion register 4 (16 bits)	PFCE4H	400A 3044H
Port function control expansion register 6 (16 bits)	PFCE6H	400A 3046H
Port function control expansion register 0 (32 bits)	PFCE0W	400A 3040H
Port function control expansion register 4 (32 bits)	PFCE4W	400A 3044H
Port pin input register 0 (8 bits)	PIN0B	400A 3050H
Port pin input register 1 (8 bits)	PIN1B	400A 3051H
Port pin input register 2 (8 bits)	PIN2B	400A 3052H
Port pin input register 3 (8 bits)	PIN3B	400A 3053H
Port pin input register 4 (8 bits)	PIN4B	400A 3054H
Port pin input register 5 (8 bits)	PIN5B	400A 3055H
Port pin input register 6 (8 bits)	PIN6B	400A 3056H
Port pin input register 7 (8 bits)	PIN7B	400A 3057H
Port pin input register 0 (16 bits)	PIN0H	400A 3050H
Port pin input register 2 (16 bits)	PIN2H	400A 3052H
Port pin input register 4 (16 bits)	PIN4H	400A 3054H
Port pin input register 6 (16 bits)	PIN6H	400A 3056H
Port pin input register 0 (32 bits)	PIN0W	400A 3050H
Port pin input register 4 (32 bits)	PIN4W	400A 3054H

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Register Name	Symbol	Address
RT port register 0 (8 bits)	RP0B	400A 3400H
RT port register 1 (8 bits)	RP1B	400A 3401H
RT port register 2 (8 bits)	RP2B	400A 3402H
RT port register 3 (8 bits)	RP3B	400A 3403H
RT port register 0 (16 bits)	RP0H	400A 3400H
RT port register 2 (16 bits)	RP2H	400A 3402H
RT port register 0 (32 bits)	RP0W	400A 3400H
RT port mode register 0 (8 bits)	RPM0B	400A 3410H
RT port mode register 1 (8 bits)	RPM1B	400A 3411H
RT port mode register 2 (8 bits)	RPM2B	400A 3412H
RT port mode register 3 (8 bits)	RPM3B	400A 3413H
RT port mode register 0 (16 bits)	RPM0H	400A 3410H
RT port mode register 2 (16 bits)	RPM2H	400A 3412H
RT port mode register 0 (32 bits)	RPM0W	400A 3410H
RT port mode control register 0 (8 bits)	RPMC0B	400A 3420H
RT port mode control register 1 (8 bits)	RPMC1B	400A 3421H
RT port mode control register 2 (8 bits)	RPMC2B	400A 3422H
RT port mode control register 3 (8 bits)	RPMC3B	400A 3423H
RT port mode control register 0 (16 bits)	RPMC0H	400A 3420H
RT port mode control register 2 (16 bits)	RPMC2H	400A 3422H
RT port mode control register 0 (32 bits)	RPMC0W	400A 3420H
RT port function control register 0 (8 bits)	RPFC0B	400A 3430H
RT port function control register 1 (8 bits)	RPFC1B	400A 3431H
RT port function control register 2 (8 bits)	RPFC2B	400A 3432H
RT port function control register 3 (8 bits)	RPFC3B	400A 3433H
RT port function control register 0 (16 bits)	RPFC0H	400A 3430H
RT port function control register 2 (16 bits)	RPFC2H	400A 3432H
RT port function control register 0 (32 bits)	RPFC0W	400A 3430H

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Register Name	Symbol	Address
RT port function control expansion register 0 (8 bits)	RPFCE0B	400A 3440H
RT port function control expansion register 1 (8 bits)	RPFCE1B	400A 3441H
RT port function control expansion register 2 (8 bits)	RPFCE2B	400A 3442H
RT port function control expansion register 3 (8 bits)	RPFCE3B	400A 3443H
RT port function control expansion register 0 (16 bits)	RPFCE0H	400A 3440H
RT port function control expansion register 2 (16 bits)	RPFCE2H	400A 3442H
RT port function control expansion register 0 (32 bits)	RPFCE0W	400A 3440H
RT port pin input register 0 (8 bits)	RPIN0B	400A 3450H
RT port pin input register 1 (8 bits)	RPIN1B	400A 3451H
RT port pin input register 2 (8 bits)	RPIN2B	400A 3452H
RT port pin input register 3 (8 bits)	RPIN3B	400A 3453H
RT port pin input register 0 (16 bits)	RPIN0H	400A 3450H
RT port pin input register 2 (16 bits)	RPIN2H	400A 3452H
RT port pin input register 0 (32 bits)	RPIN0W	400A 3450H

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Register Name	Symbol	Address
Buffer function change register P0L	DRCTLP0L	4001 0220H
Buffer function change register P0H	DRCTLP0H	4001 0224H
Buffer function change register P1L	DRCTLP1L	4001 0228H
Buffer function change register P1H	DRCTLP1H	4001 022CH
Buffer function change register P2L	DRCTLP2L	4001 0230H
Buffer function change register P2H	DRCTLP2H	4001 0234H
Buffer function change register P3L	DRCTLP3L	4001 0238H
Buffer function change register P3H	DRCTLP3H	4001 023CH
Buffer function change register P4L	DRCTLP4L	4001 0240H
Buffer function change register P4H	DRCTLP4H	4001 0244H
Buffer function change register P5L	DRCTLP5L	4001 0248H
Buffer function change register P5H	DRCTLP5H	4001 024CH
Buffer function change register P6L	DRCTLP6L	4001 0250H
Buffer function change register P6H	DRCTLP6H	4001 0254H
Buffer function change register P7L	DRCTLP7L	4001 0258H
Buffer function change register P7H	DRCTLP7H	4001 025CH
Buffer function change register RP0L	DRCTLRP0L	4001 0260H
Buffer function change register RP0H	DRCTLRP0H	4001 0264H
Buffer function change register RP1L	DRCTLRP1L	4001 0268H
Buffer function change register RP1H	DRCTLRP1H	4001 026CH
Buffer function change register RP2L	DRCTLRP2L	4001 0270H
Buffer function change register RP2H	DRCTLRP2H	4001 0274H
Buffer function change register RP3L	DRCTLRP3L	4001 0278H
Buffer function change register RP3H	DRCTLRP3H	4001 027CH

7.3.1 Port Registers (P, RP)

The R-IN32M3-CL incorporates twelve 3-state I/O ports. Input or output can be specified in 1-bit units. The port registers are used for writing the output levels for output port pins. When read, the value of the given port register is read. The PIN and RPIN registers are used to read the levels on input pins.

	7	6	5	4	3	2	1	0	Address	Initial value
P0B	P07	P06	P05	P04	P03	P02	P01	P00	400A 3000H	00H
P1B	P17	P16	P15	P14	P13	P12	P11	P10	400A 3001H	00H
P2B	P27	P26	P25	P24	P23	P22	P21	P20	400A 3002H	00H
P3B	P37	P36	P35	P34	P33	P32	P31	P30	400A 3003H	00H
P4B	P47	P46	P45	P44	P43	P42	P41	P40	400A 3004H	00H
P5B	P57	P56	P55	P54	P53	P52	P51	P50	400A 3005H	00H
P6B	P67	P66	P65	P64	P63	P62	P61	P60	400A 3006H	00H
P7B	P77	P76	P75	P74	P73	P72	P71	P70	400A 3007H	00H
RP0B	RP07	RP06	RP05	RP04	RP03	RP02	RP01	RP00	400A 3400H	00H
RP1B	RP17	RP16	RP15	RP14	RP13	RP12	RP11	RP10	400A 3401H	00H
RP2B	RP27	RP26	RP25	RP24	RP23	RP22	RP21	RP20	400A 3402H	00H
RP3B	RP37	RP36	RP35	RP34	RP33	RP32	RP31	RP30	400A 3403H	00H

Bit Position	Bit Name	Description
7 to 0	Pmn/RPln	These bits set the value of the output latch when the port is used in output mode. If read, the value of the output latch is read.

Figure 7.2 Port Registers (in 8-Bit Notation)

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

P0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
P17	P16	P15	P14	P13	P12	P11	P10	P07	P06	P05	P04	P03	P02	P01	P00	400A 3000H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

P2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
P37	P36	P35	P34	P33	P32	P31	P30	P27	P26	P25	P24	P23	P22	P21	P20	400A 3002H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

P4H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
P57	P56	P55	P54	P53	P52	P51	P50	P47	P46	P45	P44	P43	P42	P41	P40	400A 3004H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

P6H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
P77	P76	P75	P74	P73	P72	P71	P70	P67	P66	P65	P64	P63	P62	P61	P60	400A 3006H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

RP0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RP17	RP16	RP15	RP14	RP13	RP12	RP11	RP10	RP07	RP06	RP05	RP04	RP03	RP02	RP01	RP00	400A 3400H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

RP2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RP37	RP36	RP35	RP34	RP33	RP32	RP31	RP30	RP27	RP26	RP25	RP24	RP23	RP22	RP21	RP20	400A 3402H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

Bit Position	Bit Name	Description
15 to 0	Pmn/RPln	These bits set the value of the output latch when the port is used in output mode. If read, the value of the output latch is read.

Figure 7.3 Port Registers (in 16-Bit Notation)

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

P0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
P37	P36	P35	P34	P33	P32	P31	P30	P27	P26	P25	P24	P23	P22	P21	P20	P17	P16	P15	P14	P13	P12	P11	P10	P07	P06	P05	P04	P03	P02	P01	P00	400A 3000H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																																0000 0000H

P4W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
P77	P76	P75	P74	P73	P72	P71	P70	P67	P66	P65	P64	P63	P62	P61	P60	P57	P56	P55	P54	P53	P52	P51	P50	P47	P46	P45	P44	P43	P42	P41	P40	400A 3004H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																																0000 0000H

RP0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RP37	RP36	RP35	RP34	RP33	RP32	RP31	RP30	RP27	RP26	RP25	RP24	RP23	RP22	RP21	RP20	RP17	RP16	RP15	RP14	RP13	RP12	RP11	RP10	RP07	RP06	RP05	RP04	RP03	RP02	RP01	RP00	400A 3400H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																																0000 0000H

Bit Position	Bit Name	Description
31 to 0	Pmn/RPln	These bits set the value of the output latch when the port is used in output mode. If read, the value of the output latch is read.

Figure 7.4 Port Registers (in 32-Bit Notation)

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

7.3.2 Port Mode Registers (PM, RPM)

These registers are used to set a port to input or output mode.

	7	6	5	4	3	2	1	0	Address	Initial value
PM0B	PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00	400A 3010H	FFH
PM1B	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	400A 3011H	FFH
PM2B	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	400A 3012H	FFH
PM3B	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	400A 3013H	FFH
PM4B	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	400A 3014H	FFH
PM5B	PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	400A 3015H	FFH
PM6B	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	400A 3016H	FFH
PM7B	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	400A 3017H	FFH
RPM0B	RPM07	RPM06	RPM05	RPM04	RPM03	RPM02	RPM01	RPM00	400A 3410H	FFH
RPM1B	RPM17	RPM16	RPM15	RPM14	RPM13	RPM12	RPM11	RPM10	400A 3411H	FFH
RPM2B	RPM27	RPM26	RPM25	RPM24	RPM23	RPM22	RPM21	RPM20	400A 3412H	FFH
RPM3B	RPM37	RPM36	RPM35	RPM34	RPM33	RPM32	RPM31	RPM30	400A 3413H	FFH

Bit Position	Bit Name	Description
7 to 0	PMmn/ RPMln	These bits set the port to input or output mode. 0: Output mode (output buffer is on) 1: Input mode (output buffer is off) (initial value)

Figure 7.5 Port Mode Registers (in 8-Bit Notation)

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

PM0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00	400A 3010H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																FFFFH

PM2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	400A 3012H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																FFFFH

PM4H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	400A 3014H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																FFFFH

PM6H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	400A 3016H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																FFFFH

RPM0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPM 17	RPM 16	RPM 15	RPM 14	RPM 13	RPM 12	RPM 11	RPM 10	RPM 07	RPM 06	RPM 05	RPM 04	RPM 03	RPM 02	RPM 01	RPM 00	400A 3410H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																FFFFH

RPM2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPM 37	RPM 36	RPM 35	RPM 34	RPM 33	RPM 32	RPM 31	RPM 30	RPM 27	RPM 26	RPM 25	RPM 24	RPM 23	RPM 22	RPM 21	RPM 20	400A 3412H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																FFFFH

Bit Position	Bit Name	Description
15 to 0	PMmn/ RPMln	These bits set the port to input or output mode. 0: Output mode (output buffer is on) 1: Input mode (output buffer is off) (initial value)

Figure 7.6 Port Mode Registers (in 16-Bit Notation)

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

PM0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00	400A 3010H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																																FFFF FFFFH

PM4W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	400A 3014H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																																FFFF FFFFH

RPM0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPM37	RPM36	RPM35	RPM34	RPM33	RPM32	RPM31	RPM30	RPM27	RPM26	RPM25	RPM24	RPM23	RPM22	RPM21	RPM20	RPM17	RPM16	RPM15	RPM14	RPM13	RPM12	RPM11	RPM10	RPM07	RPM06	RPM05	RPM04	RPM03	RPM02	RPM01	RPM00	400A 3410H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																																FFFF FFFFH

Bit Position	Bit Name	Description
31 to 0	PMmn/RPMln	These bits set the port to input or output mode. 0: Output mode (output buffer is on) 1: Input mode (output buffer is off) (initial value)

Figure 7.7 Port Mode Registers (in 32-Bit Notation)

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

7.3.3 Port Mode Control Registers (PMC, RPMC)

These registers are used to select whether to use a port as a port or for its alternate function.

	7	6	5	4	3	2	1	0	Address	Initial value
PMC0B	PMC07	PMC06	PMC05	PMC04	PMC03	PMC02	PMC01	PMC00	400A 3020H	00H
PMC1B	PMC17	PMC16	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	400A 3021H	00H Note 1
PMC2B	PMC27	PMC26	PMC25	PMC24	PMC23	PMC22	PMC21	PMC20	400A 3022H	00H Note 1
PMC3B	PMC37	PMC36	PMC35	PMC34	PMC33	PMC32	PMC31	PMC30	400A 3023H	00H Note 1
PMC4B	PMC47	PMC46	PMC45	PMC44	PMC43	PMC42	PMC41	PMC40	400A 3024H	00H Note 1
PMC5B	PMC57	PMC56	PMC55	PMC54	PMC53	PMC52	PMC51	PMC50	400A 3025H	00H Note 1
PMC6B	PMC67	PMC66	PMC65	PMC64	PMC63	PMC62	PMC61	PMC60	400A 3026H	00H Note 1
PMC7B	PMC77	PMC76	PMC75	PMC74	PMC73	PMC72	PMC71	PMC70	400A 3027H	00H
RPMC0B	RPMC07	RPMC06	RPMC05	RPMC04	RPMC03	RPMC02	RPMC01	RPMC00	400A 3420H	00H Note 1
RPMC1B	RPMC17	RPMC16	RPMC15	RPMC14	RPMC13	RPMC12	RPMC11	RPMC10	400A 3421H	00H Note 1
RPMC2B	RPMC27	RPMC26	RPMC25	RPMC24	RPMC23	RPMC22	RPMC21	RPMC20	400A 3422H	00H Note 1
RPMC3B	RPMC37	RPMC36	RPMC35	RPMC34	RPMC33	RPMC32	RPMC31	RPMC30	400A 3423H	00H Note 1

Bit Position	Bit Name	Description
7 to 0	PMCmn/ RPMCln	These bits select whether the port pins are used as port pins or as multiplexed function pins. Note 2 0: Port mode (the inactive level is input for multiplexed input pin functions.) 1: Multiplexed function (control mode)

Figure 7.8 Port Mode Control Registers (in 8-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 7.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

PMC0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PMC17	PMC16	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	PMC07	PMC06	PMC05	PMC04	PMC03	PMC02	PMC01	PMC00	400A 3020H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																0000H Note 1

PMC2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PMC37	PMC36	PMC35	PMC34	PMC33	PMC32	PMC31	PMC30	PMC27	PMC26	PMC25	PMC24	PMC23	PMC22	PMC21	PMC20	400A 3022H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																0000H Note 1

PMC4H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PMC57	PMC56	PMC55	PMC54	PMC53	PMC52	PMC51	PMC50	PMC47	PMC46	PMC45	PMC44	PMC43	PMC42	PMC41	PMC40	400A 3024H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																0000H Note 1

PMC6H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PMC77	PMC76	PMC75	PMC74	PMC73	PMC72	PMC71	PMC70	PMC67	PMC66	PMC65	PMC64	PMC63	PMC62	PMC61	PMC60	400A 3026H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																0000H Note 1

RPMC0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPMC17	RPMC16	RPMC15	RPMC14	RPMC13	RPMC12	RPMC11	RPMC10	RPMC07	RPMC06	RPMC05	RPMC04	RPMC03	RPMC02	RPMC01	RPMC00	400A 3420H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																0000H Note 1

RPMC2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPMC37	RPMC36	RPMC35	RPMC34	RPMC33	RPMC32	RPMC31	RPMC30	RPMC27	RPMC26	RPMC25	RPMC24	RPMC23	RPMC22	RPMC21	RPMC20	400A 3422H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																0000H Note 1

Bit Position	Bit Name	Description
15 to 0	PMCmn/ RPMCln	These bits select whether the port pins are used as port pins or as multiplexed function pins. Note 2 0: Port mode (the inactive level is input for multiplexed input pin functions.) 1: Multiplexed function (control mode)

Figure 7.9 Port Mode Control Registers (in 16-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 7.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PMC0W	PMC37	PMC36	PMC35	PMC34	PMC33	PMC32	PMC31	PMC30	PMC27	PMC26	PMC25	PMC24	PMC23	PMC22	PMC21	PMC20	PMC17	PMC16	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	PMC07	PMC06	PMC05	PMC04	PMC03	PMC02	PMC01	PMC00	400A 3020H Initial value 0000 0000H Note 1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PMC4W	PMC77	PMC76	PMC75	PMC74	PMC73	PMC72	PMC71	PMC70	PMC67	PMC66	PMC65	PMC64	PMC63	PMC62	PMC61	PMC60	PMC57	PMC56	PMC55	PMC54	PMC53	PMC52	PMC51	PMC50	PMC47	PMC46	PMC45	PMC44	PMC43	PMC42	PMC41	PMC40	400A 3024H Initial value 0000 0000H Note 1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPMC0W	RPMC37	RPMC36	RPMC35	RPMC34	RPMC33	RPMC32	RPMC31	RPMC30	RPMC27	RPMC26	RPMC25	RPMC24	RPMC23	RPMC22	RPMC21	RPMC20	RPMC17	RPMC16	RPMC15	RPMC14	RPMC13	RPMC12	RPMC11	RPMC10	RPMC07	RPMC06	RPMC05	RPMC04	RPMC03	RPMC02	RPMC01	RPMC00	400A 3420H Initial value 0000 0000H Note 1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit Position	Bit Name	Description
31 to 0	PMCmn/RPMCln	These bits select whether the port pins are used as port pins or as multiplexed function pins. Note 2 0: Port mode (the inactive level is input for multiplexed input pin functions.) 1: Multiplexed function (control mode)

Figure 7.10 Port Mode Control Registers (in 32-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 7.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

7.3.4 Port Function Control Registers (PFC, RPFC)

These registers are used to specify which multiplexed function is to be used. These registers can be set in 1-bit units.

	7	6	5	4	3	2	1	0	Address	Initial value
PFC0B	PFC07	PFC06	PFC05	PFC04	PFC03	PFC02	0	0	400A 3030H	00H
PFC1B	0	0	0	0	0	PFC12	PFC11	PFC10	400A 3031H	00H
PFC2B	PFC27	PFC26	0	PFC24	0	0	0	0	400A 3032H	00H Note 1
PFC3B	PFC37	PFC36	PFC35	PFC34	PFC33	PFC32	0	0	400A 3033H	00H Note 1
PFC4B	PFC47	PFC46	PFC45	PFC44	PFC43	PFC42	PFC41	PFC40	400A 3034H	00H Note 1
PFC5B	PFC57	0	0	PFC54	PFC53	PFC52	0	0	400A 3035H	00H Note 1
PFC6B	0	0	0	0	0	0	0	0	400A 3036H	00H
PFC7B	0	0	0	0	0	0	0	0	400A 3037H	00H
RPFC0B	RPFC07	RPFC06	0	0	0	0	RPFC01	RPFC00	400A 3430H	00H
RPFC1B	0	0	0	0	0	0	0	0	400A 3431H	00H
RPFC2B	RPFC27	RPFC26	RPFC25	RPFC24	0	0	0	RPFC20	400A 3432H	00H
RPFC3B	0	0	0	0	0	0	0	0	400A 3433H	00H

Bit Position	Bit Name	Description
7 to 0	PFCmn/ RPFCmn	These bits select the multiplexed function. Note 2 0: Multiplexed function 1 or multiplexed function 3 1: Multiplexed function 2 or multiplexed function 4

Figure 7.11 Port Function Control Registers (in 8-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 7.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

PFC0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
0	0	0	0	0	PFC12	PFC11	PFC10	PFC07	PFC06	PFC05	PFC04	PFC03	PFC02	0	0	400A 3030H
0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	Initial value 0000H

PFC2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFC37	PFC36	PFC35	PFC34	PFC33	PFC32	0	0	PFC27	PFC26	0	PFC24	0	0	0	0	400A 3032H
R/W	R/W	R/W	R/W	R/W	R/W	0	0	R/W	R/W	0	R/W	0	0	0	0	Initial value 0000H Note 1

PFC4H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFC57	0	0	PFC54	PFC53	PFC52	0	0	PFC47	PFC46	PFC45	PFC44	PFC43	PFC42	PFC41	PFC40	400A 3034H
R/W	0	0	R/W	R/W	R/W	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H Note 1

PFC6H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	400A 3036H
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Initial value 0000H Note 1

RPFC0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
0	0	0	0	0	0	0	0	RPFC07	RPFC06	0	0	0	0	RPFC01	RPFC00	400A 3430H
0	0	0	0	0	0	0	0	R/W	R/W	0	0	0	0	R/W	R/W	Initial value 0000H

RPFC2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
0	0	0	0	0	0	0	0	RPFC27	RPFC26	RPFC25	RPFC24	0	0	0	RPFC20	400A 3432H
0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	0	0	0	R/W	Initial value 0000H

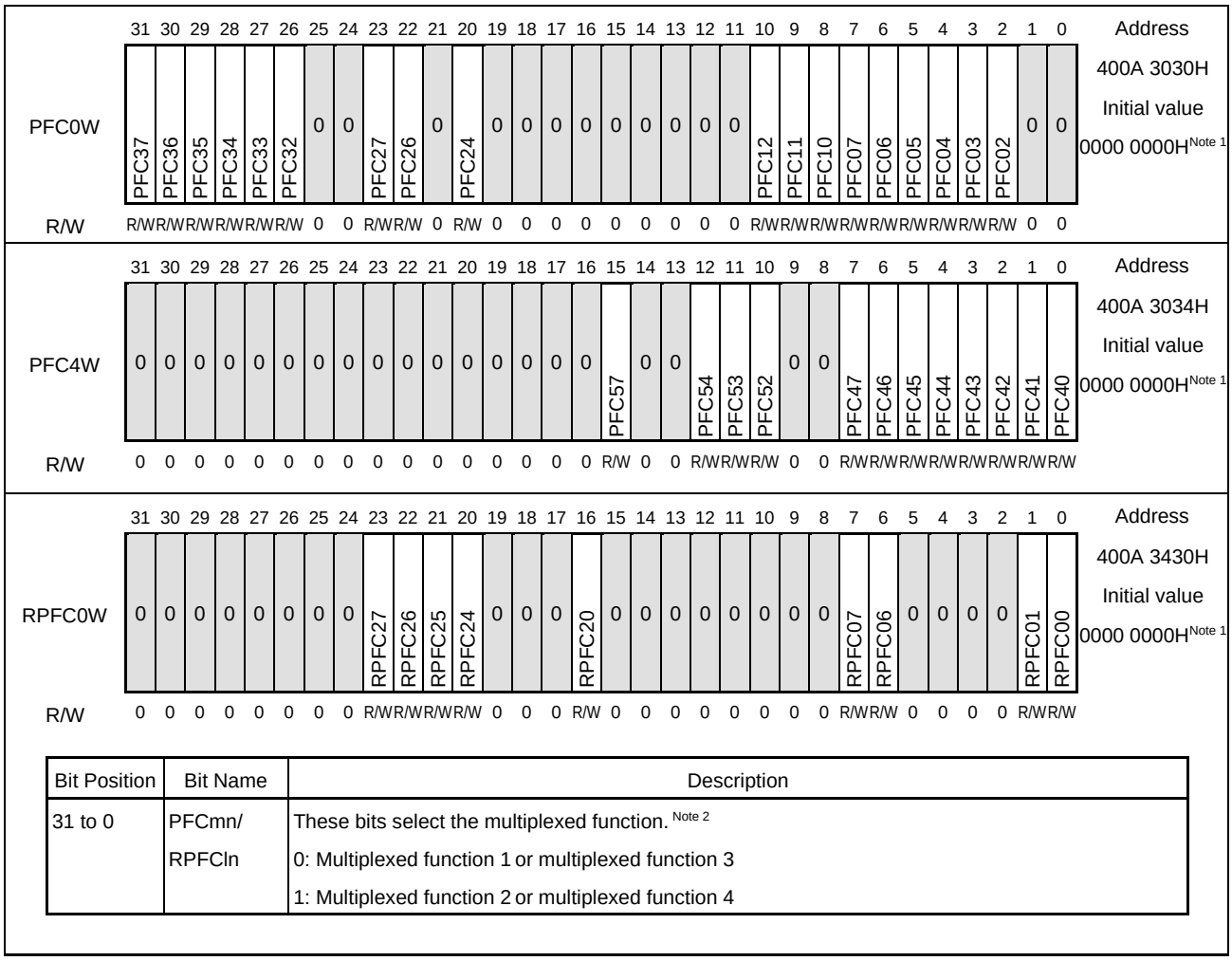
Bit Position	Bit Name	Description
15 to 0	PFCmn/ RPFCmn	These bits select the multiplexed function. Note 2 0: Multiplexed function 1 or multiplexed function 3 1: Multiplexed function 2 or multiplexed function 4

Figure 7.12 Port Function Control Registers (in 16-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 7.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7



Bit Position	Bit Name	Description
31 to 0	PFCmn/ RPFCln	These bits select the multiplexed function. Note 2 0: Multiplexed function 1 or multiplexed function 3 1: Multiplexed function 2 or multiplexed function 4

Figure 7.13 Port Function Control Registers (in 32-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 7.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

7.3.5 Port Function Control Expansion Registers (PFCE, RPFCE)

These registers are used to specify which multiplexed extended function is to be used. These registers can be set in 1-bit units.

	7	6	5	4	3	2	1	0	Address	Initial value
PFCE0B	PFCE07	PFCE06	PFCE05	PFCE04	PFCE03	PFCE02	0	PFCE00	400A 3040H	00H
PFCE1B	0	0	0	0	PFCE13	PFCE12	1	1	400A 3041H	00H
PFCE2B	0	PFCE26	PFCE25	PFCE24	PFCE23	PFCE22	PFCE21	PFCE20	400A 3042H	00H
PFCE3B	PFCE37	PFCE36	PFCE35	PFCE34	PFCE33	PFCE32	0	0	400A 3043H	00H Note 1
PFCE4B	0	0	0	0	0	PFCE42	0	0	400A 3044H	00H Note 1
PFCE5B	PFCE57	PFCE56	0	PFCE54	PFCE53	PFCE52	PFCE51	PFCE50	400A 3045H	00H
PFCE6B	0	PFCE66	PFCE65	PFCE64	PFCE63	PFCE62	0	0	400A 3046H	00H
PFCE7B	PFCE77	PFCE76	PFCE75	PFCE74	PFCE73	PFCE72	PFCE71	PFCE70	400A 3047H	00H
RPFCE0B	0	0	RPFCE05	RPFCE04	RPFCE03	RPFCE02	RPFCE01	RPFCE00	400A 3440H	00H Note 1
RPFCE1B	0	0	0	0	0	0	0	0	400A 3441H	00H
RPFCE2B	0	0	0	0	0	0	0	0	400A 3442H	00H
RPFCE3B	0	0	0	0	0	0	0	0	400A 3443H	00H

Bit Position	Bit Name	Description
7 to 0	PFCEmn/ RPFCEln	These bits select the multiplexed function. Note 2 0: Multiplexed function 1 or multiplexed function 2 1: Multiplexed function 3 or multiplexed function 4

Figure 7.14 Port Function Control Expansion Registers (in 8-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 7.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

PFCE0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
0	0	0	0	PFCE13	PFCE12	1	1	PFCE07	PFCE06	PFCE05	PFCE04	PFCE03	PFCE02	0	PFCE00	400A 3040H
0	0	0	0	R/W	R/W	1	1	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

PFCE2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFCE37	PFCE36	PFCE35	PFCE34	PFCE33	PFCE32	0	0	0	PFCE26	PFCE25	PFCE24	PFCE23	PFCE22	PFCE21	PFCE20	400A 3042H
R/W	R/W	R/W	R/W	R/W	R/W	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H Note 1

PFCE4H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFCE57	PFCE56	0	PFCE54	PFCE53	PFCE52	PFCE51	PFCE50	0	0	0	0	0	PFCE42	0	0	400A 3044H
R/W	R/W	0	R/W	R/W	R/W	R/W	R/W	0	0	0	0	0	R/W	0	0	Initial value 0000H Note 1

PFCE6H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFCE77	PFCE76	PFCE75	PFCE74	PFCE73	PFCE72	PFCE71	PFCE70	0	PFCE66	PFCE65	PFCE64	PFCE63	PFCE62	0	0	400A 3046H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	R/W	R/W	R/W	R/W	R/W	0	0	Initial value 0000H

RPFCE0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
0	0	0	0	0	0	0	0	0	0	RPFCE05	RPFCE04	RPFCE03	RPFCE02	RPFCE01	RPFCE00	400A 3440H
0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H Note 1

RPFCE2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	400A 3442H
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Initial value 0000H

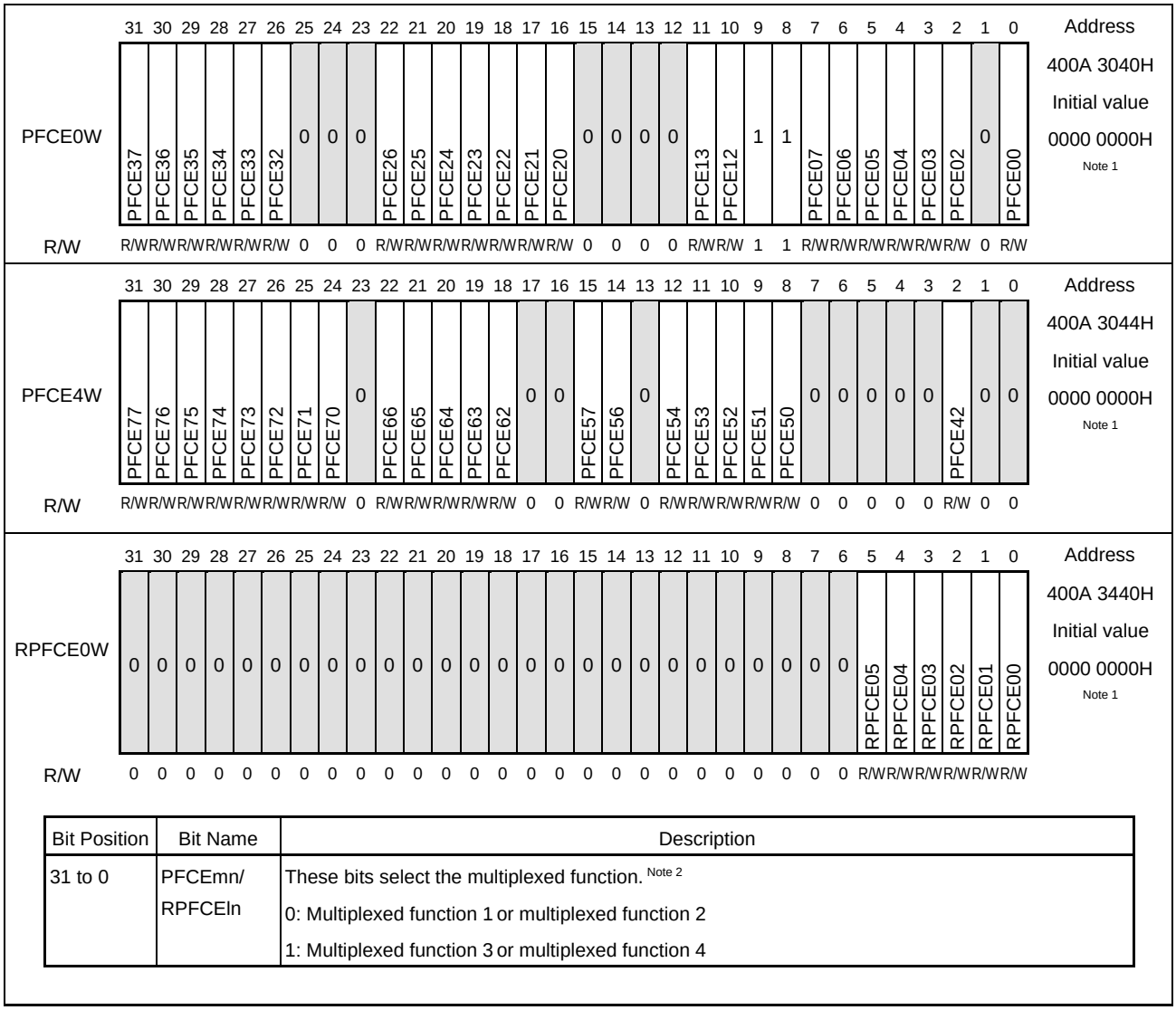
Bit Position	Bit Name	Description
15 to 0	PFCEmn/ RPFCEln	These bits select the multiplexed function. Note 2 0: Multiplexed function 1 or multiplexed function 2 1: Multiplexed function 3 or multiplexed function 4

Figure 7.15 Port Function Control Expansion Registers (in 16-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 7.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7



Bit Position	Bit Name	Description
31 to 0	PFCEmn/ RPFCEln	These bits select the multiplexed function. Note 2 0: Multiplexed function 1 or multiplexed function 2 1: Multiplexed function 3 or multiplexed function 4

Figure 7.16 Port Function Control Expansion Registers (in 32-Bit Notation)

Notes 1. The initial value depends on the state of the pins. For details, see section 2.2, Pin States.

2. The multiplexed function is selected by the port mode control register, port function control register, and the port function control expansion register. For details, see section 7.4, List of Selectable Multiplexed Functions.

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

7.3.6 Port Pin Input Registers (PIN, RPIN)

These are read-only registers for reading the input level of port pins.

	7	6	5	4	3	2	1	0	Address	Initial value
PIN0B	PIN07	PIN06	PIN05	PIN04	PIN03	PIN02	PIN01	PIN00	400A 3050H	Pin level
PIN1B	PIN17	PIN16	PIN15	PIN14	PIN13	PIN12	PIN11	PIN10	400A 3051H	Pin level
PIN2B	PIN27	PIN26	PIN25	PIN24	PIN23	PIN22	PIN21	PIN20	400A 3052H	Pin level
PIN3B	PIN37	PIN36	PIN35	PIN34	PIN33	PIN32	PIN31	PIN30	400A 3053H	Pin level
PIN4B	PIN47	PIN46	PIN45	PIN44	PIN43	PIN42	PIN41	PIN40	400A 3054H	Pin level
PIN5B	PIN57	PIN56	PIN55	PIN54	PIN53	PIN52	PIN51	PIN50	400A 3055H	Pin level
PIN6B	PIN67	PIN66	PIN65	PIN64	PIN63	PIN62	PIN61	PIN60	400A 3056H	Pin level
PIN7B	PIN77	PIN76	PIN75	PIN74	PIN73	PIN72	PIN71	PIN70	400A 3057H	Pin level
RPIN0B	RPIN07	RPIN06	RPIN05	RPIN04	RPIN03	RPIN02	RPIN01	RPIN00	400A 3450H	Pin level
RPIN1B	RPIN17	RPIN16	RPIN15	RPIN14	RPIN13	RPIN12	RPIN11	RPIN10	400A 3451H	Pin level
RPIN2B	RPIN27	RPIN26	RPIN25	RPIN24	RPIN23	RPIN22	RPIN21	RPIN20	400A 3452H	Pin level
RPIN3B	RPIN37	RPIN36	RPIN35	RPIN34	RPIN33	RPIN32	RPIN31	RPIN30	400A 3453H	Pin level

Bit Position	Bit Name	Description
7 to 0	PINmn/ RPINln	These bits are for reading the input level of the port pins.

Figure 7.17 Port Pin Input Registers (in 8-Bit Notation)

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PIN0H	PIN 17	PIN 16	PIN 15	PIN 14	PIN 13	PIN 12	PIN 11	PIN 10	PIN 07	PIN 06	PIN 05	PIN 04	PIN 03	PIN 02	PIN 01	PIN 00	400A 3050H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
																	Pin level

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PIN2H	PIN 37	PIN 36	PIN 35	PIN 34	PIN 33	PIN 32	PIN 31	PIN 30	PIN 27	PIN 26	PIN 25	PIN 24	PIN 23	PIN 22	PIN 21	PIN 20	400A 3052H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
																	Pin level

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PIN4H	PIN 57	PIN 56	PIN 55	PIN 54	PIN 53	PIN 52	PIN 51	PIN 50	PIN 47	PIN 46	PIN 45	PIN 44	PIN 43	PIN 42	PIN 41	PIN 40	400A 3054H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
																	Pin level

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PIN6H	PIN 77	PIN 76	PIN 75	PIN 74	PIN 73	PIN 72	PIN 71	PIN 70	PIN 67	PIN 66	PIN 65	PIN 64	PIN 63	PIN 62	PIN 61	PIN 60	400A 3056H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
																	Pin level

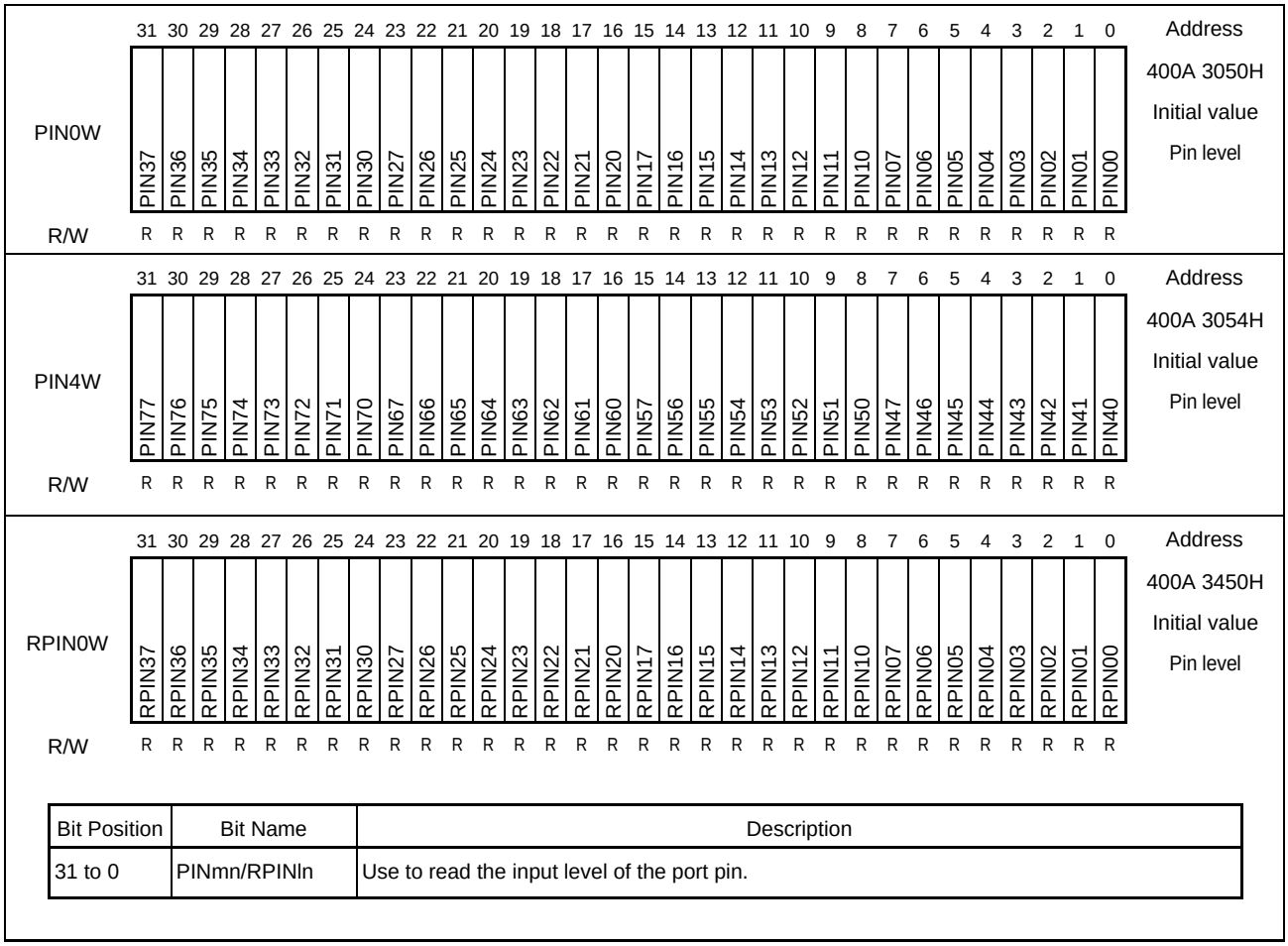
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPIN0H	RPIN 17	RPIN 16	RPIN 15	RPIN 14	RPIN 13	RPIN 12	RPIN 11	RPIN 10	RPIN 07	RPIN 06	RPIN 05	RPIN 04	RPIN 03	RPIN 02	RPIN 01	RPIN0 0	400A 3450H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
																	Pin level

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPIN2H	RPIN 37	RPIN 36	RPIN 35	RPIN 34	RPIN 33	RPIN 32	RPIN 31	RPIN 30	RPIN 27	RPIN 26	RPIN 25	RPIN 24	RPIN 23	RPIN 22	RPIN 21	RPIN2 0	400A 3452H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
																	Pin level

Bit Position	Bit Name	Description
15 to 0	PINmn/ RPINIn	These bits are for reading the input level of the port pins.

Figure 7.18 Port Pin Input Registers (in 16-Bit Notation)

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7



Bit Position	Bit Name	Description
31 to 0	PINmn/RPINln	Use to read the input level of the port pin.

Figure 7.19 Port Pin Input Registers (in 32-Bit Notation)

Remark: l = 0 to 3, m = 0 to 7, n = 0 to 7

7.4 List of Selectable Multiplexed Functions

The table below lists the combinations of multiplexed functions that can be specified by using the port-related registers.

(1) Ports (P00 to P77)

(1/3)

Pin Name	PMCmn = 0 (Port Mode)		PMCmn = 1 (Control Mode)			
			PFCEmn = 0		PFCEmn = 1	
	PMmn = 0 (Output Port)	PMmn = 1 (Input Port)	PFCmn = 0 (Multiplexed Function 1)	PFCmn = 1 (Multiplexed Function 2)	PFCmn = 0 (Multiplexed Function 3)	PFCmn = 1 (Multiplexed Function 4)
P00	P00 (output mode)	P00 (input mode)	INTPZ0	-	CCI_RUNLEDZ	-
P01	P01 (output mode)	P01 (input mode)	INTPZ1	-	-	-
P02	P02 (output mode)	P02 (input mode)	INTPZ2	-	CCI_DLINKLEDZ	-
P03	P03 (output mode)	P03 (input mode)	INTPZ3	-	CCI_ERRLEDZ	CCS_MON5
P04	P04 (output mode)	P04 (input mode)	INTPZ4	-	CCI_LERR1LEDZ	CCS_MON6
P05	P05 (output mode)	P05 (input mode)	INTPZ5	-	CCI_LERR2LEDZ	CCS_MON7
P06	P06 (output mode)	P06 (input mode)	PHYLINK0	-	CCI_SDLEDZ	CCS_MON0
P07	P07 (output mode)	P07 (input mode)	PHYLINK1	-	CCIRDLEDZ	CCS_RESOUT
P10	P10 (output mode)	P10 (input mode)	-	-	-	CCS_REFSTB
P11	P11 (output mode)	P11 (input mode)	-	-	-	CCS_MON4
P12	P12 (output mode)	P12 (input mode)	INTPZ6	-	CCI_NMIZ	-
P13	P13 (output mode)	P13 (input mode)	INTPZ7	-	CCI_WDTIZ / CCS_WDTZ / CCM_WDTENZ	-
P14	P14 (output mode)	P14 (input mode)	SMSCK	-	-	-
P15	P15 (output mode)	P15 (input mode)	SMSI	-	-	-
P16	P16 (output mode)	P16 (input mode)	SMSO	-	-	-
P17	P17 (output mode)	P17 (input mode)	SMCSZ	-	-	-
P20	P20 (output mode)	P20 (input mode)	RXD0	−	CCM_LINKERRZ	-
P21	P21 (output mode)	P21 (input mode)	TXD0	−	CCM_ERRZ	-
P22	P22 (output mode)	P22 (input mode)	INTPZ8	−	CCS_IOTENSU	-
P23	P23 (output mode)	P23 (input mode)	INTPZ9	−	CCS_SENYU0	-
P24	P24 (output mode)	P24 (input mode)	INTPZ10	ETHSWSECOUT	CCS_SENYU1	-
P25	P25 (output mode)	P25 (input mode)	WDTOUTZ	−	CCS_ERRZ	-
P26	P26 (output mode)	P26 (input mode)	TIN1	TOUT1	CCM_RUNZ / CCS_RUNZ	-
P27	P27 (output mode)	P27 (input mode)	TIN0	TOUT0	-	-

Remark: m = 0 to 7, n = 0 to 7

(2/3)

Pin Name	PMCmn = 0 (Port Mode)		PMCmn = 1 (Control Mode)			
			PFCEmn = 0		PFCEmn = 1	
	PMmn = 0 (Output Port)	PMmn = 1 (Input Port)	PFCmn = 0 (Multiplexed Function 1)	PFCmn = 1 (Multiplexed Function 2)	PFCmn = 0 (Multiplexed Function 3)	PFCmn = 1 (Multiplexed Function 4)
P30	P30 (output mode)	P30 (input mode)	RXD1	-	-	-
P31	P31 (output mode)	P31 (input mode)	TXD1	-	-	-
P32	P32 (output mode)	P32 (input mode)	DMAREQZ1	-	-	CCS_MON1
P33	P33 (output mode)	P33 (input mode)	DMAACKZ1	CCI_ WAITEDGEH	-	CCS_MON2
P34	P34 (output mode)	P34 (input mode)	DMATCZ1	CCI_WRLENH	-	CCS_MON3
P35	P35 (output mode)	P35 (input mode)	CSISCK1	INTPZ22	CCM_IRLZ	-
P36	P36 (output mode)	P36 (input mode)	CSISI1	INTPZ23	CCS_FUSEZ	-
P37	P37 (output mode)	P37 (input mode)	CSISO1	INTPZ24	CCM_MSTZ	-
P40	P40 (output mode)	P40 (input mode)	A1	HA1	-	-
P41	P41 (output mode)	P41 (input mode)	WAITZ	HWAITZ	-	-
P42	P42 (output mode)	P42 (input mode)	SLEEPING	HERROUTZ	CCM_SDGCZ	-
P43	P43 (output mode)	P43 (input mode)	INTPZ11	HBUSCLK	-	-
P44	P44 (output mode)	P44 (input mode)	CSZ1	HPGCSZ	-	-
P45	P45 (output mode)	P45 (input mode)	CSISCK0	WAITZ1	-	-
P46	P46 (output mode)	P46 (input mode)	CSISI0	WAITZ2	-	-
P47	P47 (output mode)	P47 (input mode)	CSISO0	WAITZ3	-	-
P50	P50 (output mode)	P50 (input mode)	CSZ3	-	CCM_LNKRUNZ / CCS_LNKRUNZ	-
P51	P51 (output mode)	P51 (input mode)	CSZ2	-	CCM_RDLEDZ / CCS_RDLEDZ	-
P52	P52 (output mode)	P52 (input mode)	TIN3	TOUT3	CCS_SDGATEON	-
P53	P53 (output mode)	P53 (input mode)	CRXD0	CCS_RD	CCM_RD	-
P54	P54 (output mode)	P54 (input mode)	CTXD0	CCS_SD	CCM_SD	-
P55	P55 (output mode)	P55 (input mode)	CRXD1	–	–	-
P56	P56 (output mode)	P56 (input mode)	CTXD1	-	CCI_PHYREZ1	-
P57	P57 (output mode)	P57 (input mode)	TIN2	TOUT2	CCI_PHYREZ0	-

Remark: m = 0 to 7, n = 0 to 7

(3/3)

Pin Name	PMCmn = 0 (Port Mode)		PMCmn = 1 (Control Mode)			
			PFCEmn = 0		PFCEmn = 1	
	PMmn = 0 (Output Port)	PMmn = 1 (Input Port)	PFCmn = 0 (Multiplexed Function 1)	PFCmn = 1 (Multiplexed Function 2)	PFCmn = 0 (Multiplexed Function 3)	PFCmn = 1 (Multiplexed Function 4)
P60	P60 (output mode)	P60 (input mode)	SCL0	-	-	-
P61	P61 (output mode)	P61 (input mode)	SDA0	-	-	-
P62	P62 (output mode)	P62 (input mode)	RTDMAREQZ	-	CCM_MDIN0	-
P63	P63 (output mode)	P63 (input mode)	RTDMAACKZ	-	CCM_MDIN1	-
P64	P64 (output mode)	P64 (input mode)	RTDMATCZ	-	CCM_MDIN2	-
P65	P65 (output mode)	P65 (input mode)	DMAREQZ0	-	CCM_MDIN3	-
P66	P66 (output mode)	P66 (input mode)	DMAACKZ0	-	CCI_INTZ	-
P67	P67 (output mode)	P67 (input mode)	DMATCZ0	-	-	-
P70	P70 (output mode)	P70 (input mode)	CSICS00	-	CCS_STATION_NO_0 / CCM_SNIN0	-
P71	P71 (output mode)	P71 (input mode)	CSICS01	-	CCS_STATION_NO_1 / CCM_SNIN1	-
P72	P72 (output mode)	P72 (input mode)	CSICS10	-	CCS_STATION_NO_2 / CCM_SNIN2	-
P73	P73 (output mode)	P73 (input mode)	CSICS11	-	CCS_STATION_NO_3 / CCM_SNIN3	-
P74	P74 (output mode)	P74 (input mode)	INTPZ12	-	CCS_STATION_NO_4 / CCM_SNIN4	-
P75	P75 (output mode)	P75 (input mode)	INTPZ13	-	CCS_STATION_NO_5 / CCM_SNIN5	-
P76	P76 (output mode)	P76 (input mode)	INTPZ14	-	CCS_STATION_NO_6 / CCM_SNIN6	-
P77	P77 (output mode)	P77 (input mode)	INTPZ15	-	CCS_STATION_NO_7 / CCM_SNIN7	-

Remark: m = 0 to 7, n = 0 to 7

(2) Real-Time Ports (RP00 to RP37)

Pin Name	PMCmn = 0 (Port Mode)		PMCmn = 1 (Control Mode)			
			RPFCEmn = 0		RPFCEmn = 1	
	PMmn = 0 (Output Port)	PMmn = 1 (Input Port)	PFCmn = 0 (Multiplexed Function 1)	PFCmn = 1 (Multiplexed Function 2)	PFCmn = 0 (Multiplexed Function 3)	PFCmn = 1 (Multiplexed Function 4)
RP00	RP00 (output mode)	RP00 (input mode)	INTPZ16	SCL1	CCM_SDLEDZ / CCS_SDLEDZ	-
RP01	RP01 (output mode)	RP01 (input mode)	INTPZ17	SDA1	CCM_SMSTZ	-
RP02	RP02 (output mode)	RP02 (input mode)	INTPZ18	-	CCS_BS1	-
RP03	RP03 (output mode)	RP03 (input mode)	INTPZ19	-	CCS_BS2	-
RP04	RP04 (output mode)	RP04 (input mode)	INTPZ20	-	CCS_BS4	-
RP05	RP05 (output mode)	RP05 (input mode)	INTPZ21	-	CCS_BS8	-
RP06	RP06 (output mode)	RP06 (input mode)	WRZ2/BENZ2	HWRZ2 / HBENZ2	-	-
RP07	RP07 (output mode)	RP07 (input mode)	WRZ3/BENZ3	HWRZ3 / HBENZ3	-	-
RP10	RP10 (output mode)	RP10 (input mode)	D24/HD24	-	-	-
RP11	RP11 (output mode)	RP11 (input mode)	D25/HD25	-	-	-
RP12	RP12 (output mode)	RP12 (input mode)	D26/HD26	-	-	-
RP13	RP13 (output mode)	RP13 (input mode)	D27/HD27	-	-	-
RP14	RP14 (output mode)	RP14 (input mode)	D28/HD28	-	-	-
RP15	RP15 (output mode)	RP15 (input mode)	D29/HD29	-	-	-
RP16	RP16 (output mode)	RP16 (input mode)	D30/HD30	-	-	-
RP17	RP17 (output mode)	RP17 (input mode)	D31/HD31	-	-	-
RP20	RP20 (output mode)	RP20 (input mode)	BCYSTZ	HBCYSTZ	-	-
RP21	RP21 (output mode)	RP21 (input mode)	A21	–	-	-
RP22	RP22 (output mode)	RP22 (input mode)	A22	–	–	-
RP23	RP23 (output mode)	RP23 (input mode)	A23	–	–	-
RP24	RP24 (output mode)	RP24 (input mode)	A24	INTPZ25	–	-
RP25	RP25 (output mode)	RP25 (input mode)	A25	INTPZ26	–	-
RP26	RP26 (output mode)	RP26 (input mode)	A26	INTPZ27	–	-
RP27	RP27 (output mode)	RP27 (input mode)	A27	INTPZ28	–	-
RP30	RP30 (output mode)	RP30 (input mode)	D16/HD16	-	–	-
RP31	RP31 (output mode)	RP31 (input mode)	D17/HD17	-	–	-
RP32	RP32 (output mode)	RP32 (input mode)	D18/HD18	-	–	-
RP33	RP33 (output mode)	RP33 (input mode)	D19/HD19	-	–	-
RP34	RP34 (output mode)	RP34 (input mode)	D20/HD20	-	–	-
RP35	RP35 (output mode)	RP35 (input mode)	D21/HD21	-	–	-
RP36	RP36 (output mode)	RP36 (input mode)	D22/HD22	-	–	-
RP37	RP37 (output mode)	RP37 (input mode)	D23/HD23	-	–	-

Remark: m = 0 to 3, n = 0 to 7

7.5 Buffer Switching Registers (DRCTL)

For some port pins, the driving ability and the connection or disconnection of a pull-up or pull-down resistor is programmable.
Set up the DRCTL registers during initialization after release from the reset state. After that, change the setting of a given DRCTL register only while the buffer functions for the corresponding pins are not in use. For example, change the setting while only internal access is proceeding.
The settings of the DRCTL registers are effective for output pins regardless of their operating mode (port mode, or control mode, in which a multiplexed function is used).

- Access These registers can be read and written in 32-bit or 16-bit units.

Cautions 1. These registers are only writable after protection has been released by a special sequence of writing to the system protection command register (SYSPCMD). For how to release protection, see the description of the system protection command register (SYSPCMD). No special sequence is required for reading the register.
2. Take special care with pins in the high-impedance state, since changing the settings for the pull-up and pull-down resistors will affect levels on the pins.

7.5.1 Port 0 Buffer Switching Registers (DRCTLP0L, DRCTLP0H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP0L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP03	PDIOP03	IOLP031	IOLP030	PUIOP02	PDIOP02	IOLP021	IOLP020	PUIOP01	PDIOP01	IOLP011	IOLP010	PUIOP00	PDIOP00	IOLP001	IOLP000	BASE+0220H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP0H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP07	PDIOP07	IOLP071	IOLP070	PUIOP06	PDIOP06	IOLP061	IOLP060	PUIOP05	PDIOP05	IOLP051	IOLP050	PUIOP04	PDIOP04	IOLP041	IOLP040	BASE+0224H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000 9999H

Bit Position	Bit Name	Description
31 to 16	–	Reserved (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIOP0n, PDIOP0n	These bits specify whether to connect a pull-up or pull-down resistor to the P07 to P00 pins.
13, 12, 9, 8, 5, 4, 1, 0	IOLP0n1, IOLP0n0	These bits specify the driving ability of the P07 to P00 pins.

PUIO	PDIO	Connection of a Pull-Up or Pull-Down Resistor to the P07 to P00 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

IOL1	IOL0	Driving Ability of the P07 to P00 Pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark: n = 7 to 0

7.5.2 Port 1 Buffer Switching Registers (DRCTLP1L, DRCTLP1H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP1L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP13	PDIOP13	0	1	PUIOP12	PDIOP12	0	1	PUIOP11	PDIOP11	0	1	PUIOP10	PDIOP10	IOLP101	IOLP100	BASE+0228H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	R/W	R/W	0000 9959H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP1H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP17	PDIOP17	0	1	PUIOP16	PDIOP16	0	1	PUIOP15	PDIOP15	0	1	PUIOP14	PDIOP14	0	1	BASE+022CH
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

Bit Position	Bit Name	Description
31 to 16	–	Reserved (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIOP1n, PDIOP1n	These bits specify whether to connect a pull-up or pull-down resistor to the P17 to P10 pins.

PUIO	PDIO	Connection of a Pull-Up or Pull-Down Resistor to the P17 to P10 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

1, 0	IOLP101, IOLP100	These bits specify the driving ability of the P10 pin.

IOL1	IOL0	Driving Ability of the P10 Pin
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark: n = 7 to 0

7.5.3 Port 2 Buffer Switching Registers (DRCTLP2L, DRCTLP2H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP2L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP23	PDIOP23	0	1	PUIOP22	PDIOP22	0	1	PUIOP21	PDIOP21	IOLP211	IOLP210	PUIOP20	PDIOP20	IOLP201	IOLP200	BASE+0230H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP2H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP27	PDIOP27	0	1	PUIOP26	PDIOP26	IOLP261	IOLP260	PUIOP25	PDIOP25	IOLP251	IOLP250	PUIOP24	PDIOP24	0	1	BASE+0234H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	1	0000 9999H

Bit Position	Bit Name	Description
31 to 16	–	Reserved (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIOP2n, PDIOP2n	These bits specify whether to connect a pull-up or pull-down resistor to the P27 to P20 pins.

PUIO	PDIO	Connection of a Pull-Up or Pull-Down Resistor to the P27 to P20 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

9, 8, 5, 4	IOLP2n1, IOLP2n0	These bits specify the driving ability of the P26, P25, P21, and P20 pins

IOL1	IOL0	Driving Ability of the P26, P25, P21, and P20 Pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark: n = 7 to 0

7.5.4 Port 3 Buffer Switching Registers (DRCTLP3L, DRCTLP3H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP3L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP33	PDIOP33	0	1	PUIOP32	PDIOP32	0	1	PUIOP31	PDIOP31	0	1	PUIOP30	PDIOP30	0	1	BASE+0238H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP3H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP37	PDIOP37	IOLP371	IOLP370	PUIOP36	PDIOP36	0	1	PUIOP35	PDIOP35	0	1	PUIOP34	PDIOP34	0	1	BASE+023CH
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

Bit Position	Bit Name	Description
31 to 16	–	Reserved (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIOP3n, PDIOP3n	These bits specify whether to connect a pull-up or pull-down resistor to the P37 to P30 pins.
13, 12	IOLP371, IOLP370	These bits specify the driving ability of the P37 pin.

PUIO	PDIO	Connection of a Pull-Up or Pull-Down Resistor to the P37 to P30 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

IOL1	IOL0	Driving Ability of the P37 Pin
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark: n = 7 to 0

7.5.5 Port 4 Buffer Switching Registers (DRCTLP4L, DRCTLP4H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP4L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP43	PDIOP43	0	1	PUIOP42	PDIOP42	0	1	PUIOP41	PDIOP41	0	1	PUIOP40	PDIOP40	0	1	BASE+0240H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP4H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP47	PDIOP47	0	1	PUIOP46	PDIOP46	0	1	PUIOP45	PDIOP45	0	1	PUIOP44	PDIOP44	0	1	BASE+0244H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

Bit Position	Bit Name	Description
31 to 16	–	Reserved (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIOP4n, PDIOP4n	These bits specify whether to connect a pull-up or pull-down resistor to the P47 to P40 pins.

PUIO	PDIO	Connection of a Pull-Up or Pull-Down Resistor to the P47 to P40 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

Remark: n = 7 to 0

7.5.6 Port 5 Buffer Switching Registers (DRCTLP5L, DRCTLP5H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP5L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP52	PDIOP52	0	1	PUIOP51	PDIOP51	IOLP511	IOLP510	PUIOP50	PDIOP50	IOLP501	IOLP500	BASE+0248H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 0599H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP5H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP57	PDIOP57	0	1	0	0	0	0	0	0	0	0	0	0	0	0	BASE+024CH
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0000 9000H

Bit Position	Bit Name	Description
31 to 16	–	Reserved (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIOP5n, PDIOP5n	These bits specify whether to connect a pull-up or pull-down resistor to the P57 and P52 to P50 pins.

PUIO	PDIO	Connection of a Pull-Up or Pull-Down Resistor to the P57 and P52 to P50 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

5, 4, 1, 0	IOLP5n1, IOLP5n0	These bits specify the driving ability of the P51 and P50 pins.

IOL1	IOL0	Driving Ability of the P51 and P50 Pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark: n = 7 to 0

7.5.7 Port 6 Buffer Switching Registers (DRCTLP6L, DRCTLP6H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP6L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP63	PDIOP63	0	1	PUIOP62	PDIOP62	0	1	PUIOP61	PDIOP61	0	1	PUIOP60	PDIOP60	0	1	BASE+0250H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP6H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP67	PDIOP67	0	1	PUIOP66	PDIOP66	0	1	PUIOP65	PDIOP65	0	1	PUIOP64	PDIOP64	0	1	BASE+0254H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

Bit Position	Bit Name	Description
31 to 16	–	Reserved (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIOP6n, PDIOP6n	These bits specify whether to connect a pull-up or pull-down resistor to the P67 to P60 pins.

PUIO	PDIO	Connection of a Pull-Up or Pull-Down Resistor to the P67 to P60 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

Remark: n = 7 to 0

7.5.8 Port 7 Buffer Switching Registers (DRCTLP7L, DRCTLP7H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP7L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP73	PDIOP73	0	1	PUIOP72	PDIOP72	0	1	PUIOP71	PDIOP71	0	1	PUIOP70	PDIOP70	0	1	BASE+0258H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	Initial value 0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP7H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP77	PDIOP77	0	1	PUIOP76	PDIOP76	0	1	PUIOP75	PDIOP75	0	1	PUIOP74	PDIOP74	0	1	BASE+025CH
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	Initial value 0000 9999H

Bit Position	Bit Name	Description
31 to 16	–	Reserved (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIOP7n, PDIOP7n	These bits specify whether to connect a pull-up or pull-down resistor to the P77 to P70 pins.

PUIO	PDIO	Connection of a Pull-Up or Pull-Down Resistor to the P77 to P70 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

Remark: n = 7 to 0

7.5.9 Real-Time Port 0 Buffer Switching Registers (DRCTLRP0L, DRCTLRP0H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP0L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP03	PDIORP03	IOLRP031	IOLRP030	PUIORP02	PDIORP02	IOLRP021	IOLRP020	PUIORP01	PDIORP01	IOLRP011	IOLRP010	PUIORP00	PDIORP00	IOLRP001	IOLRP000	BASE+0260H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP0H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP07	PDIORP07	IOLRP071	IOLRP070	PUIORP06	PDIORP06	IOLRP061	IOLRP060	PUIORP05	PDIORP05	IOLRP051	IOLRP050	PUIORP04	PDIORP04	IOLRP041	IOLRP040	BASE+0264H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 9999H

Bit Position	Bit Name	Description
31 to 16	–	Reserved (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIORP0n, PDIORP0n	These bits specify whether to connect a pull-up or pull-down resistor to the RP07 to RP00 pins.
13, 12, 9, 8, 5, 4, 1, 0	IOLRP0n1, IOLRP0n0	These bits specify the driving ability of the RP07 to RP00 pins.

PUIO	PDIO	Connection of a Pull-Up or Pull-Down Resistor to the RP07 to RP00 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

IOL1	IOL0	Driving Ability of the RP07 to RP00 Pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark: n = 7 to 0

7.5.10 Real-Time Port 1 Buffer Switching Registers (DRCTLRP1L, DRCTLRP1H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP1L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP13	PDIORP13	IOLRP131	IOLRP130	PUIORP12	PDIORP12	IOLRP121	IOLRP120	PUIORP11	PDIORP11	IOLRP111	IOLRP110	PUIORP10	PDIORP10	IOLRP101	IOLRP100	BASE+0268H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP1H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP17	PDIORP17	IOLRP171	IOLRP170	PUIORP16	PDIORP16	IOLRP161	IOLRP160	PUIORP15	PDIORP15	IOLRP151	IOLRP150	PUIORP14	PDIORP14	IOLRP141	IOLRP140	BASE+026CH
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 9999H

Bit Position	Bit Name	Description
31 to 16	–	Reserved (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIORP1n, PDIORP1n	These bits specify whether to connect a pull-up or pull-down resistor to the RP17 to RP10 pins.

PUIO	PDIO	Connection of a Pull-Up or Pull-Down Resistor to the RP17 to RP10 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

13, 12, 9, 8, 5, 4, 1, 0	IOLRP1n1, IOLRP1n0	These bits specify the driving ability of the RP17 to RP10 pins.

IOL1	IOL0	Driving Ability of the RP17 to RP10 Pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark: n = 7 to 0

7.5.11 Real-Time Port 2 Buffer Switching Registers (DRCTLRP2L, DRCTLRP2H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP2L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP23	PDIORP23	IOLRP231	IOLRP230	PUIORP22	PDIORP22	IOLRP221	IOLRP220	PUIORP21	PDIORP21	IOLRP211	IOLRP210	PUIORP20	PDIORP20	IOLRP201	IOLRP200	BASE+0270H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 5559H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP2H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP27	PDIORP27	IOLRP271	IOLRP270	PUIORP26	PDIORP26	IOLRP261	IOLRP260	PUIORP25	PDIORP25	IOLRP251	IOLRP250	PUIORP24	PDIORP24	IOLRP241	IOLRP240	BASE+0274H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0000 5555H

Bit Position	Bit Name	Description
31 to 16	–	Reserved (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIORP2n, PDIORP2n	These bits specify whether to connect a pull-up or pull-down resistor to the RP27 to RP20 pins.

PUIO	PDIO	Connection of a Pull-Up or Pull-Down Resistor to the RP27 to RP20 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

13, 12, 9, 8, 5, 4, 1, 0	IOLRP2n1, IOLRP2n0	These bits specify the driving ability of the RP27 to RP20 pins.

IOL1	IOL0	Driving Ability of the RP27 to RP20 Pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark: n = 7 to 0

7.5.12 Real-Time Port 3 Buffer Switching Registers (DRCTLRP3L, DRCTLRP3H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP3L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP33	PDIORP33	IOLRP331	IOLRP330	PUIORP32	PDIORP32	IOLRP321	IOLRP320	PUIORP31	PDIORP31	IOLRP311	IOLRP310	PUIORP30	PDIORP30	IOLRP301	IOLRP300	BASE+0278H
																																	Initial value
																																	0000 9999H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP3H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP37	PDIORP37	IOLRP371	IOLRP370	PUIORP36	PDIORP36	IOLRP361	IOLRP360	PUIORP35	PDIORP35	IOLRP351	IOLRP350	PUIORP34	PDIORP34	IOLRP341	IOLRP340	BASE+027CH
																																	Initial value
																																	0000 9999H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit Position	Bit Name	Description
31 to 16	–	Reserved (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIORP3n, PDIORP3n	These bits specify whether to connect a pull-up or pull-down resistor to the RP37 to RP30 pins.

PUIO	PDIO	Connection of a Pull-Up or Pull-Down Resistor to the RP37 to RP30 Pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

Bit Position	Bit Name	Description
13, 12, 9, 8, 5, 4, 1, 0	IOLRP3n1, IOLRP3n0	These bits specify the driving ability of the RP37 to RP30 pins.

IOL1	IOL0	Driving Ability of the RP37 to RP30 Pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark: n = 7 to 0

7.6 Operation of Port Functions

Operation of the ports differs depending on the I/O mode setting as described below.

7.6.1 Reading and Writing via I/O Ports

(1) In Output Mode

If a value is written to port register n (Pn or RPn), the value is written to that port's output latch (Pn or RPn). The value of the output latch is output from the pin.
The value written to the output latch is held until another value is written.
The value of the output latch (Pn or RPn) can be read by reading port register n (Pn or RPn).
To directly read the pin level, read port pin input register n (PINn or RPINn).

(2) In Input Mode

If a value is written to port register n (Pn or RPn), the value is written to that port's output latch (Pn or RPn). However, the pin state does not change because the output buffer is off.
The value written to the output latch is held until another value is written.
To read the input level, read port pin input register n (PINn or RPINn).

7.6.2 Multiplexed Function Pin Output State in Control Mode

The port pin level can be read directly by reading port pin input register n (PINn or RPINn), regardless of the settings of the PMCn, PMn, PFCn, and PFCEn registers.

7.7 Trigger-Synchronous Ports (RP00 to RP37)

The state of the 32-bit port pins RP00 to RP37 can be updated in synchronization with an interrupt from an on-chip peripheral function.

Use the RPTRGMD register to set trigger-synchronous port control mode in 1-bit units. To select the target trigger, use the RPTFR0 to RPTFR3 registers.
For details, see the R-IN32M3 Series User's Manual (Peripheral Modules).

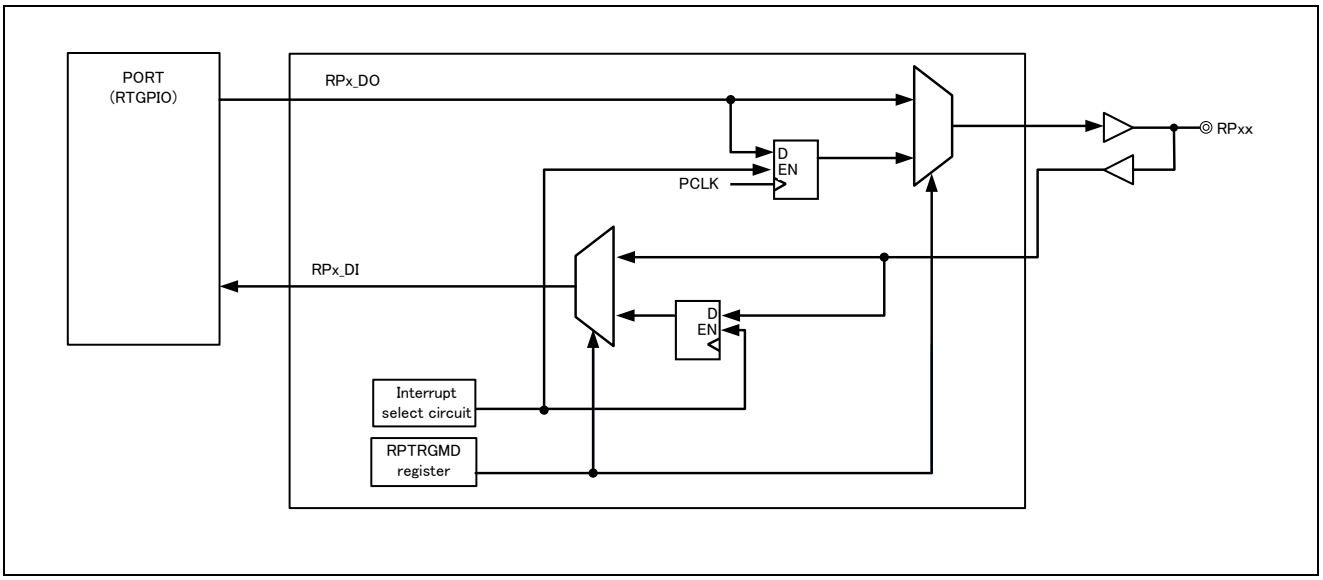


Figure 7.20 Configuration of Trigger-Synchronous Ports

8. Electrical Characteristics

For details on the electrical characteristics, refer to the R-IN32M3 Series Datasheet.

REVISION HISTORY	R-IN32M3 Series User's Manual: R-IN32M3-CL

Rev.	Date	Description	
		Page	Summary
1.00 (Preliminary)	Feb. 8, 2013	-	First edition issued
1.00	Apr. 03,2013	Overall	Modification of English expressions
		Overall	Change the description of "CC-Link IE Field" "CC-Link IE field slave" → "CC-Link IE field (intelligent device station)"
		Overall	Change the description of "CC-Link" "CC-Link (slave)" → "CC-Link (remote device station)"
		1	Modification of the contents of **1.1 Overview**
		2	Modification of the status of ETH_MDC during the reset of **2.1.1 Ethernet Pins** Modification of the contents of Note of **2.1.1 Ethernet Pins**
		3	Standby mode deletion
		8	Modification of the status of BUSCLK during the reset of **2.1.2 External Memory Interface Pins** Addition of synchronous burst access MEMC information of **2.1.2 External Memory Interface Pins**
		9	Modification of the status of HD0-HD15, HBCYSTZ during the reset of **2.1.3 External MCU Interface Pins**
		20	Modification of PONRZ function of **2.1.16 System Pins** Addition the signals of HOTRESETZ, VDDQ_MII, CLKOUT25M0, CLKOUT25M1 of **2.1.16 System Pins**
		22	Modification of the contents of Note1 and Note2 of **2.2 Pin States**
1.01	Dec. 09, 2013	overall	Modification of the supported station of CC-Link
2.00	Feb. 07, 2014	4	Modification of block diagram of **1.3 Internal Block Diagram**
		6-21	Addition the status after reset timing of **2.1 List of Pins**
		17	Addition explanation of Function of **2.1.13 CC-Link IE Field Pins (Intelligent Device Station)**
		19	Add **CCM_CLK80M** pins to list of **2.1.15 CC-Link Pins (Remote Device Station)**
		21	Modification of Boot mode select of **2.1.18 Operation Mode Setting Pins**
		22	Addition of Synchronous burst MEMC of **2.2 Pin States**
		25	Addition of the signals of CLKOUT25M0/CLKOUT25M1 of **2.5.3 External Interrupt Input Pins**
		27-28	Addition of a resistor value of pull up/down of **2.3.5 Port Pins** Modification of a description of the drive current of P30/P31/P52/P61-P64 of **2.3.5 Port Pins**
		28	Modification of title name of **2.5.8 CC-Link Pin (Intelligent Device Station, Remote Device Station)**
		37	Addition of the contents of Note of INTCCSRFSTB register of **4.2 List of Interrupts**
		40	Addition the register of **6.1.1 CC-Link IE Field (Intelligent Device Station) Clock Gate Register (CIECLKGTD)**

Rev.	Date	Description	
		Page	Summary
2.00	Feb. 07, 2014	41	Addition the register of **6.1.2 CC-Link IE Field (Intelligent Device Station) Wait Delay Register (CIEWAITDLY)**
		42	Modification of Address of **6.1.4 CC-Link IE Field (Intelligent Device Station) Bus Bridge Control Register (CIESMC)**
		57	Modification of initial value of PM0W, PM4W, and PRM0W registers of **7.3.2 Port Mode Registers (PM, RPM)**
2.01	Apr. 18, 2014	overall	Modification of **CC-Link pins (remote device station)**
		17	Addition of the contents of Note of **2.1.13 CC-Link IE Field Pins (Intelligent Device Station)**
		28	Modification of pin setting of **2.5.7 CC-Link IE Field Pin (Intelligent Device Station)**
		71	Addition of the signals of CCI_WAITEDGEH / CCI_WRLENH of **7.4 List of Selectable Multiplexed Functions**
2.02	Dec. 25, 2014	3	Change status for Intelligent device station for CC-Link in **1.3 Overview**
		80	Remove IOLP521, IOLP520 bit at **7.5.6 Port 5 Buffer Switching Registers (DRCTLP5L, DRCTLP5H)** (because driving capability of P52 is fixed to 6mA.)
3.00	Jan. 22, 2016	6-24	2. Pin Functions Meaning of the items, symbols, and abbreviations, added to the list of pins Description unified
		7	2.1.1 (1) PHY Interface Pins ・Note for the value during reset and after reset, modified ・The value of the ETH_MDC pin during reset and after reset, modified
		9	2.1.2 External Memory Interface Pins ・The value of BUSCLK during reset and after reset, modified ・Supplemental explanations added to Note 1
		17	2.1.10 Trace Pins The value of TRACECLK during reset and after reset, modified
		21	2.1.15 CC-Link Pins (Remote Device Station) Note added to CCM_CLK80M
		22	2.1.16 System Pins ・Functional description and active level of XT1/XT2/OSCTH/JTAGSEL, modified ・The value of RSTOUTZ/CLKOUT25M0-1 during reset and after reset, modified
		23-24	2.1.18 Operating Mode Setting Pins ・Functional description of the ADMUXMODE pin, modified ・The list of the combinations of available operating mode setting pins, added
		25-33	2.2 Pin States The initial states for all boot modes and all port pins, added
		36	2.5.4 System Pins ・Recommended connection when not using XT1/XT2, modified Note added ・Recommended connection when not using RESETZ/PONRZ/OSCTH/ JTAGSEL, modified

Rev.	Date	Description	
		Page	Summary
3.00	Jan. 22, 2016	39	2.5.7 Operating Mode Setting Pins Recommended connection when not in use, modified
			2.5.8 CC-Link IE Field Pin (Intelligent Device Station) Recommended connection when not in use, modified
		41	Figure 3.1 Memory Map (ALL) Instruction RAM area and instruction RAM mirror area, modified
		44	Figure 3.5External MCU Interface Area Instruction RAM mirror area, modified
		45	4.1 Exceptions List Abbreviations of reset pins, modified SYSRESET register, added
		55	6.1.3 CC-Link IE Field (Intelligent Device Station) Bus Size Control Register (CIEBSC) Description modified
			6.1.4 CC-Link IE Field (Intelligent Device Station) Bus Bridge Control Register (CIESMC) Description modified
		90	7.5.3 Port 2 Buffer Switching Registers (DRCTLP2L, DRCTLP2H) Description on bits 9, 8, 5, and 4 modified
3.01	Feb. 28, 2017	18	2.1.13 CC-Link IE Field Pins (Intelligent Device Station) Note modified (complement)
		19	2.1.14 CC-Link Pins (Intelligent Device Station) Description to the CCM_MDIN0-CCM_MDIN3 signals modified (complement)
		21	2.1.16 System Pins Function of PONRZ modified
		46	4.2 List of Interrupts, Table 4.1 (2/4) Exception No.54 INTETHSW: Interrupt source name changed
		48-49	4.2 List of Interrupts, Table 4.1 List of Interrupts (3/4), (4/4) ECC error interrupts are added to exception No. 115 to 120. (new function)
		50	5. Peripheral Modules Expressions of peripheral functions are unified to that in the User's Manual (Peripheral Modules). (expression alignment)
		55	6.2 Cautionary Notes Newly added (complement)

Rev.	Date	Description	
		Page	Summary
4.00	Dec. 28, 2018	6	1.5 Base Addresses of the System Registers Area The description on the base addresses of the system registers area was added.
		13	2.1.4 Port Pins and Real-Time Port Pins The pin name indicated as "CCM_IRZ" was modified to "CCM_IRLZ".
		16	2.1.6 DMA Interface Pins The description on the section and caution was modified.
		20	2.1.14 CC-Link Pins (Intelligent Device Station) The name and functional descriptions of the CC-Link (intelligent device station) pins were modified.
		41, 44	3. Memory Maps Note describing that the addresses the instruction RAM mirror area (768 Kbytes) where access actually occurs will change according to the select boot mode, was added. Figure 3.1 Memory Map (All) Figure 3.5 External MCU Interface Area
		44	Figure 3.5 External MCU Interface Area Locations of instruction RAM area and instruction RAM mirror area, corrected
		58	7.2 Port Configuration "Application and Operation" for the port function control registers and the port function control expansion registers was modified.
		58	7.2 Port Configuration Caution on the port configuration was modified.
		72 to 80	7.3.3 Port Mode Control Registers (PMC, RPMC) 7.3.4 Port Function Control Registers (PFC, RPFC) 7.3.5 Port Function Control Expansion Registers (PFCE, RPFCE) Notes on the multiplexed functions were modified.
		85	7.4 List of Selectable Multiplexed Functions Pins name indicated as "CCM_IRZ" was modified to "CCM_IRLZ".
		—	Error corrected, description modified, and contents and expressions adjusted
5.00	May 31, 2024	57	6.2 Cautionary Notes (3) Setting when the CC-Link IE Field is not used was added.

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